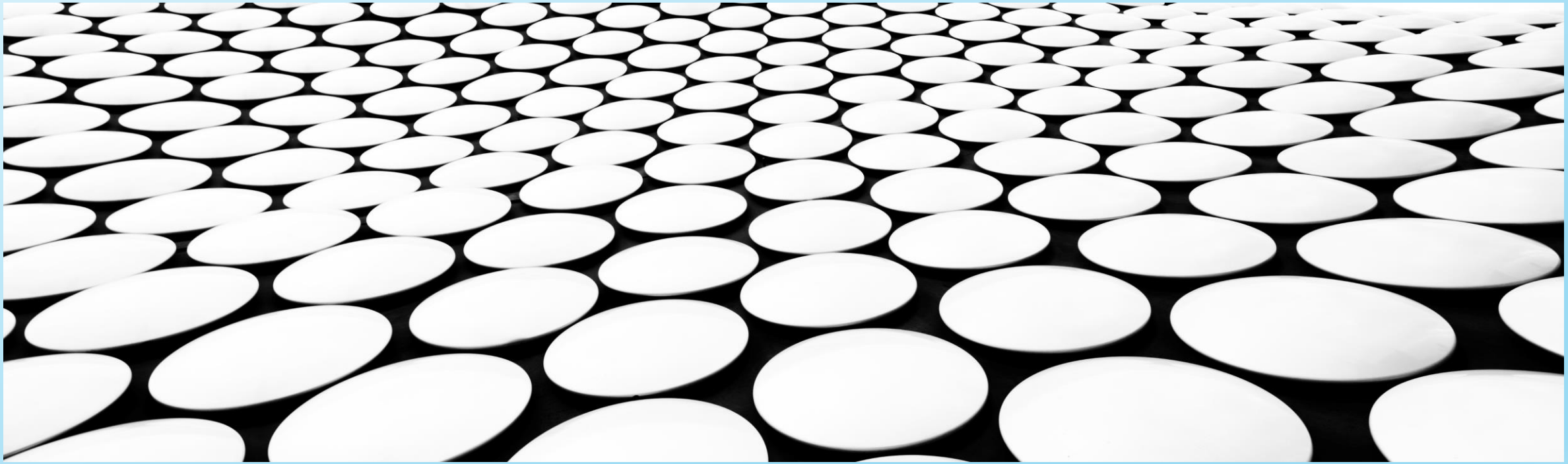
ARHITECTURA SISTEMELOR DE CALCUL

UB, FMI, CTI, ANUL III, 2021-2022

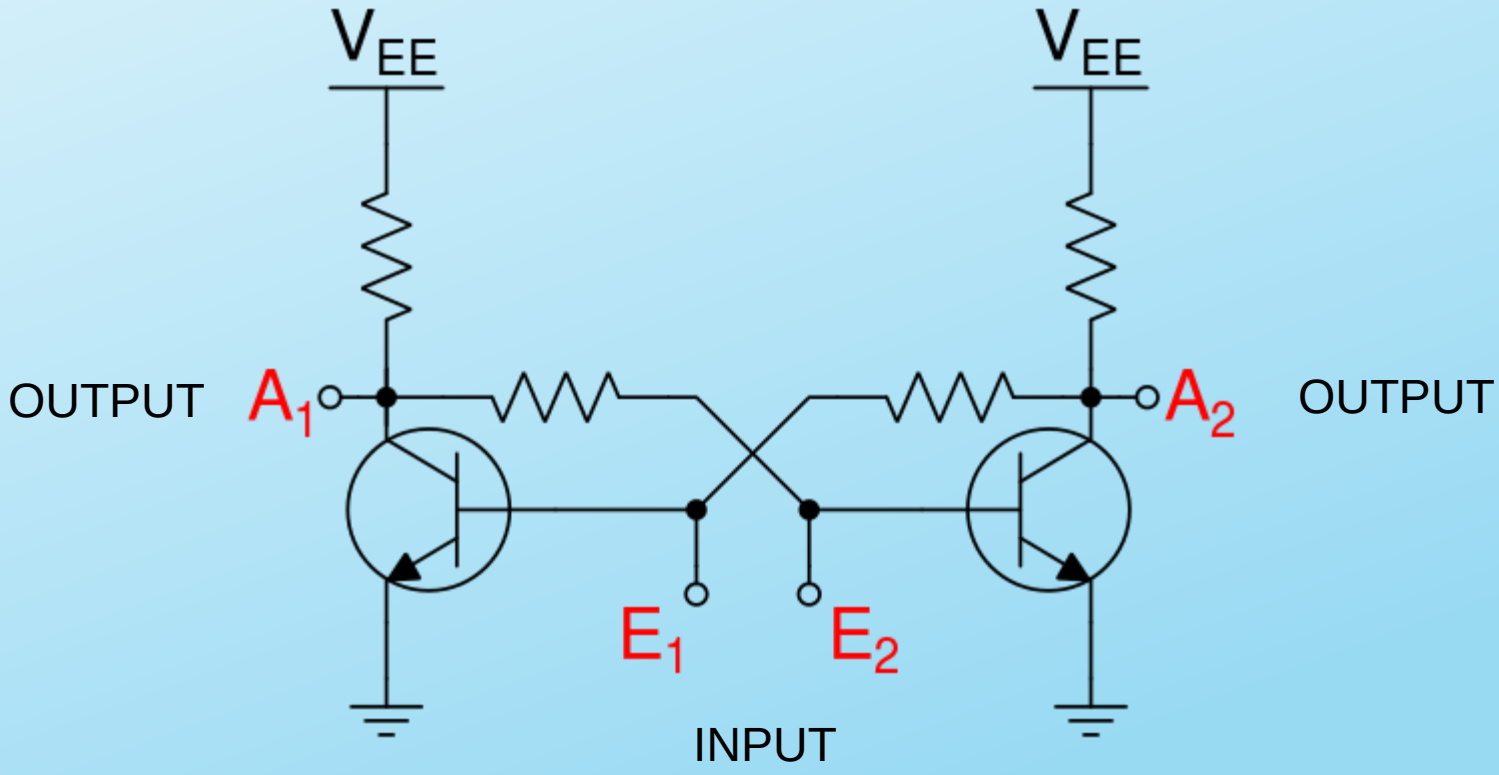


BLOCURI DE MEMORIE ELECTRONICA

CEA MAI SIMPLA ARHITECTURA DE MEMORIE RAM SCALABILA

Circuite elementare de memorie

- Circuitul bistabil



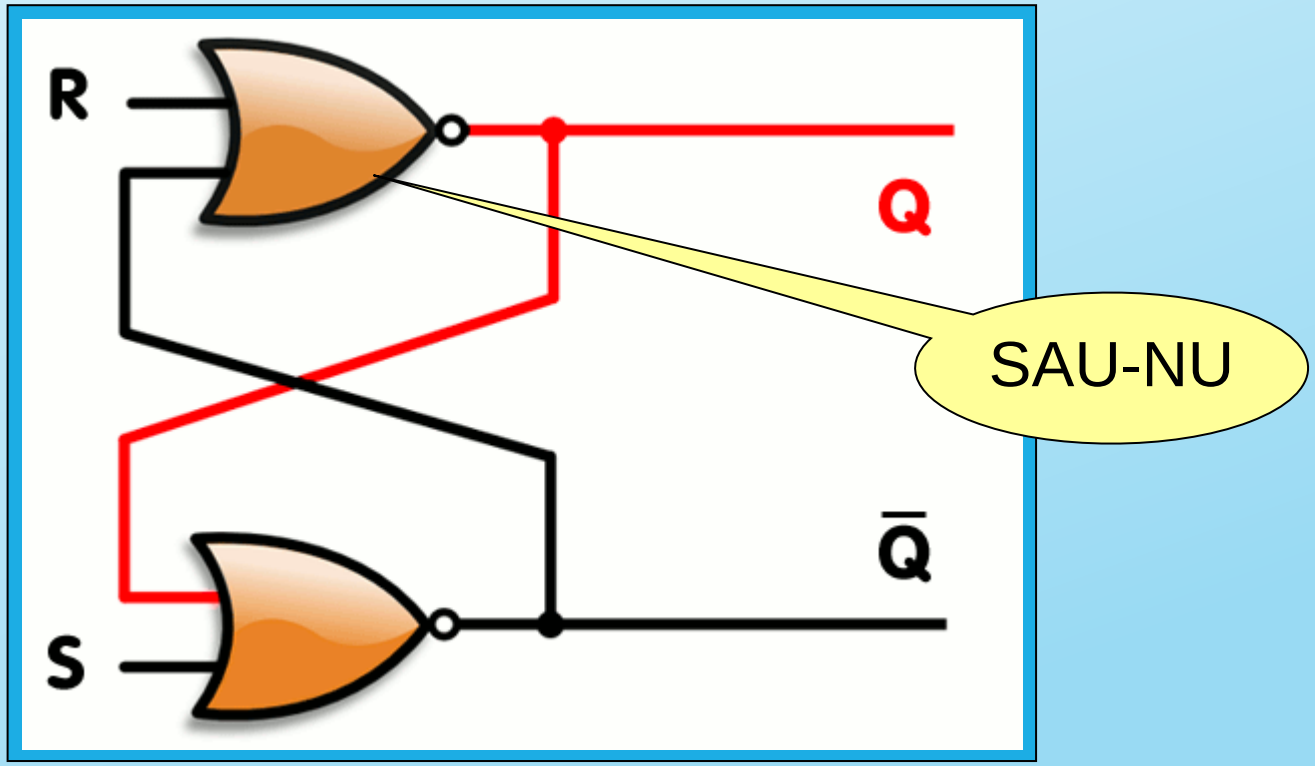
Exemplu de circuit cu tranzistori bipolari

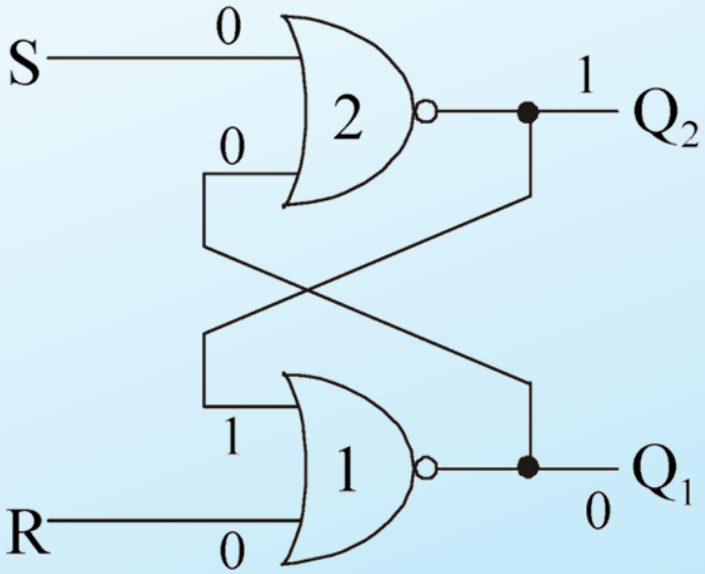
Schema logica echivalenta

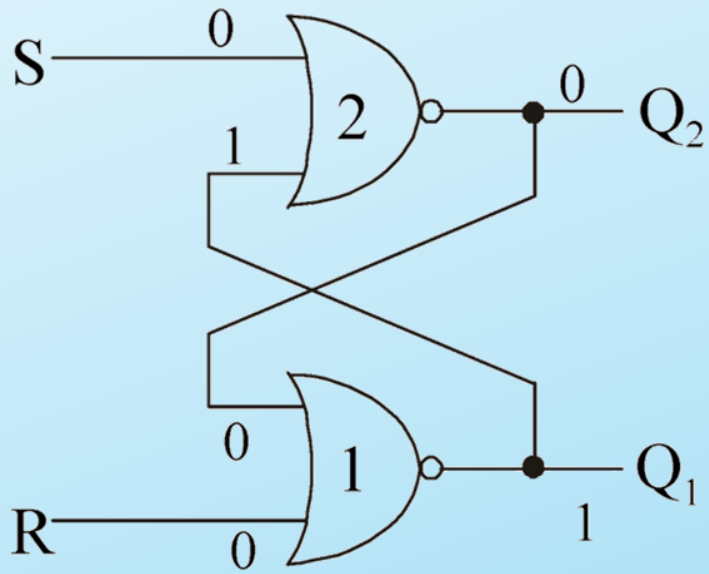
INPUT:

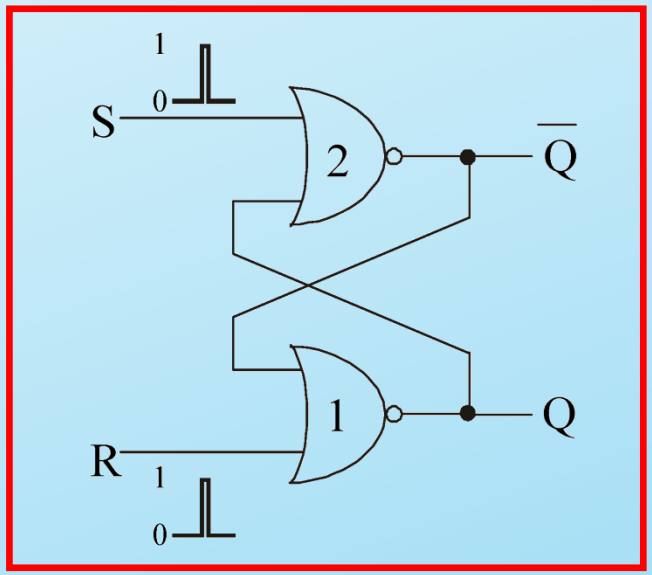
S – SET

R -RESET

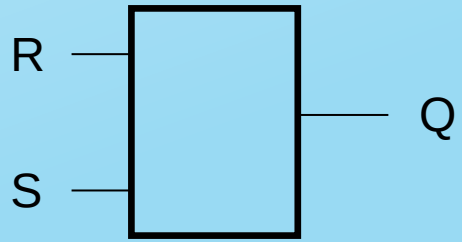








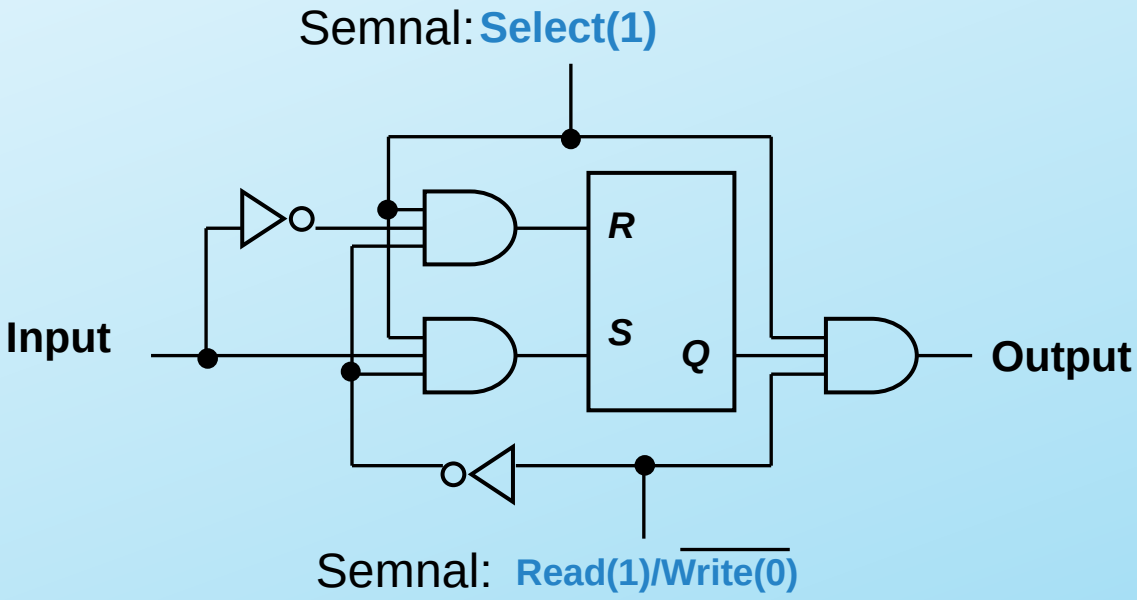
- Un impuls pozitiv pe S aduce iesirea Q1 in starea 1
- Un impuls pozitiv pe R aduce iesirea Q1 in starea 0



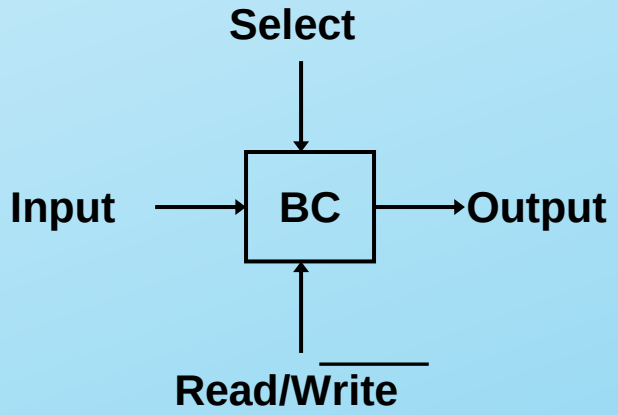
Echivalentul mecanic al memoriei

CELULA DE MEMORIE SRAM DE 1 bit

Diagrama logica pentru **celula de 1 bit**



Logic diagram



Block diagram

Matrice de celule de memorie 4x3

(4 locatii de 3 biti)

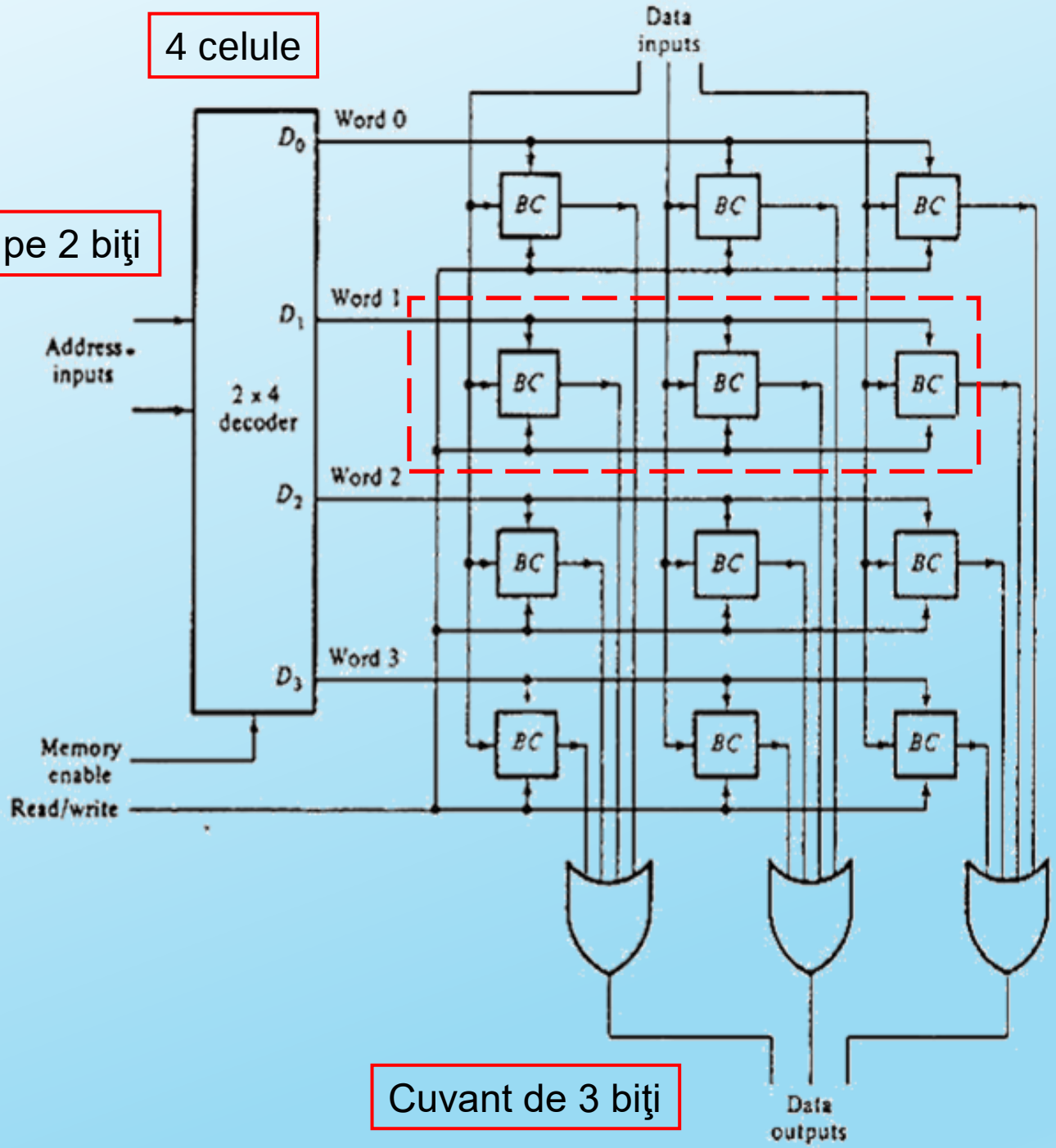
4x3 RAM

Biți din cuvant transferați in paralel

Cuvinte transferate succesiv (funcție de adresa)

4 celule

Adrese pe 2 biţi



Cuvant de 3 biţi

informaţia de adresa se transforma in semnal de selecţie

Bloc de memorie: 1K x 8-bit RAM (chip)

- 1K= 1024 cuvinte=2^{10}

pentru 1024 cuvinte este nevoie de o dimensiune de adresa de 10 biti

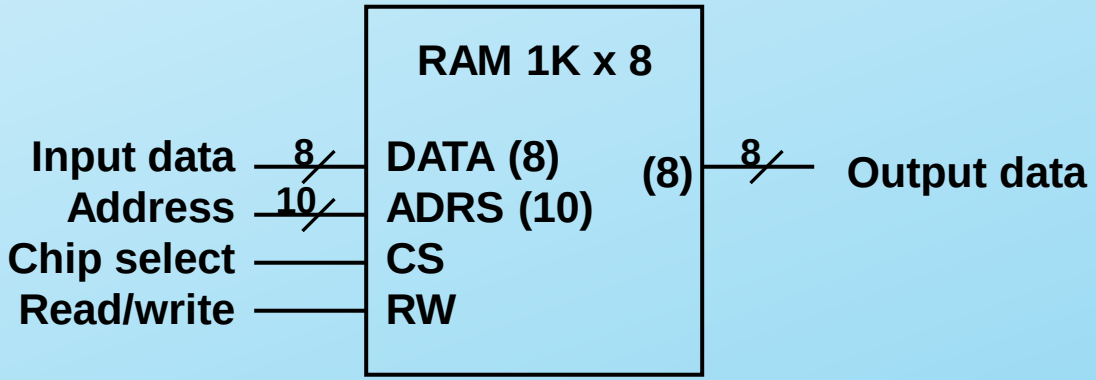
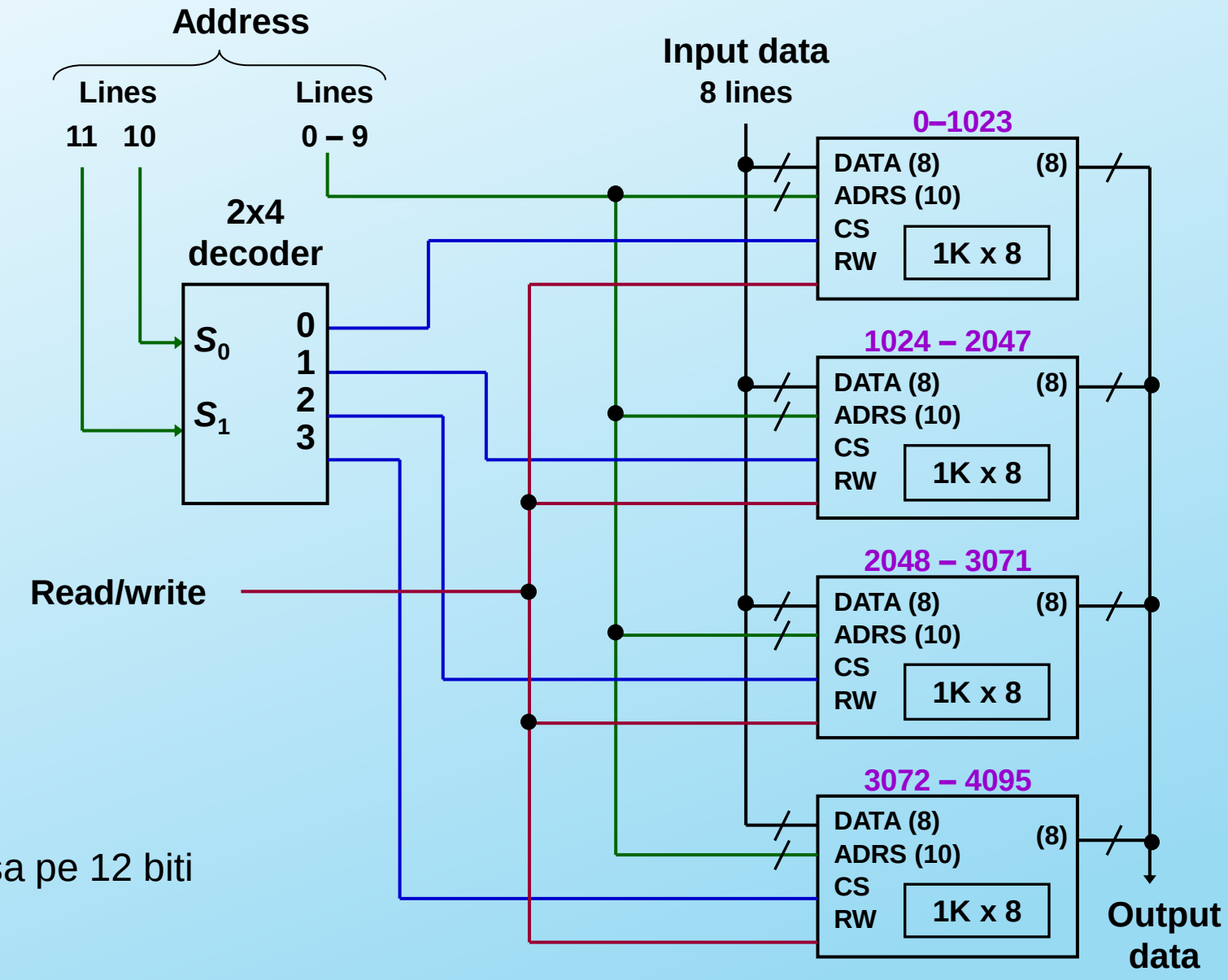


Diagrama bloc a unui chip RAM de 1K x 8b

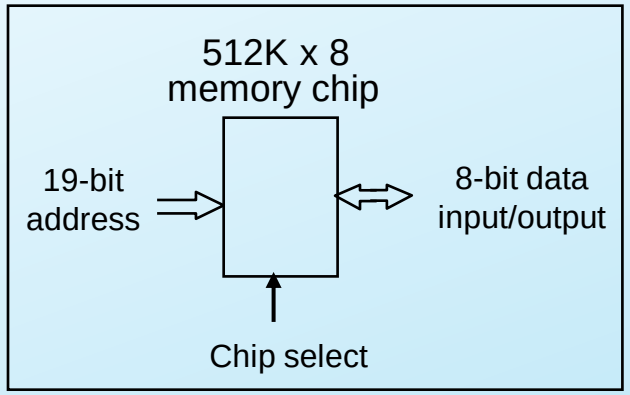


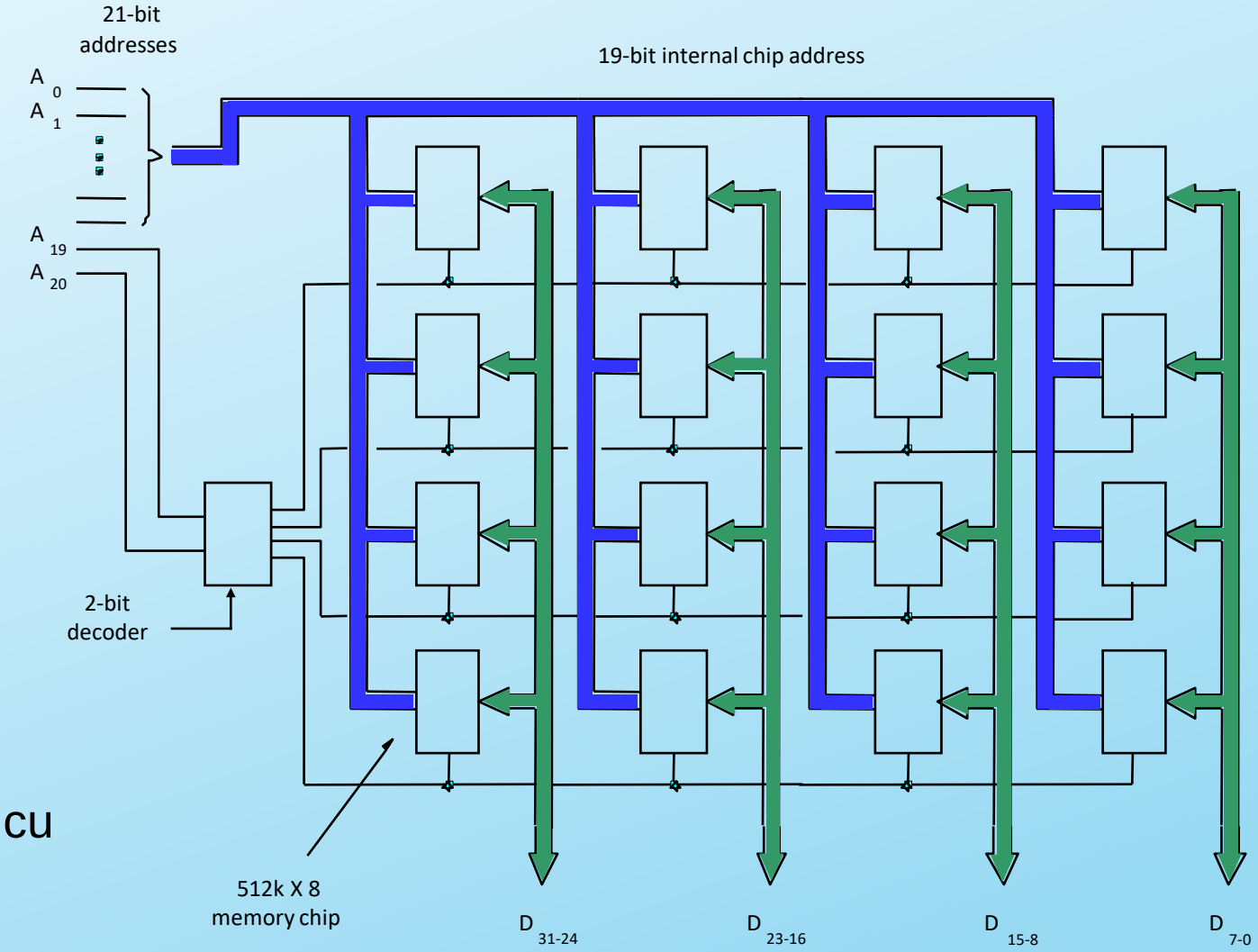
Bloc 4Kx8b RAM

in acest caz adresa este scrisa pe 12 biti

Blocurile OR de colectare sunt omis pentru simplificarea desenului

Tema: redesenati schema, incluzand si blocurile de colectare





Alt exemplu:
Modul de memorie de **2M × 32b** asamblat cu 512K × 8b static memory chips.

Semnalul: Read/Write este omis

Tema: redesenati schema, incluzand toate blocurile si semnalele omis

TEMA

Desenati schema unui modul de memorie de 2G × 64b, folosind cipuri de memorie de 512M × **32b**