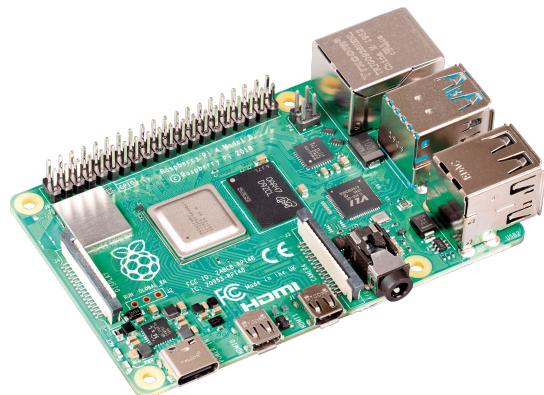


Writing a bare metal GPU driver for the Raspberry PI 4

Darius ENGLER

July 9, 2022



Introduction

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 - A kernel-space driver (for communicating with the hardware) e.g. linux

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 - Basic communication with the GPU

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 - Basic communication with the GPU
 - Running (compute) shaders

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 - A user-space driver (the opengl / vulkan implementation) e.g. mesa
- What's our goal?
 - Basic communication with the GPU
 - Running (compute) shaders
 - Rendering a 3D scene on the GPU

Motivation

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- Learn more about modern GPU

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- alternative for linux/mesa

Hardware overview

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- BCM2711 SoC

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 - QPU

Communicating with the GPU

Communicating with the GPU

- Mailbox interface managed by VCOS

Communicating with the GPU

- Mailbox interface managed by VCOS
- MMIO Registers

Mailbox interface

Mailbox interface

- Documented

Mailbox interface

- Documented
- Plenty of examples online

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Execute Code

- Tag: 0x00030010
- Request:
 - Length: 28
 - Value:
 - u32: function pointer
 - u32: r0
 - u32: r1
 - u32: r2
 - u32: r3
 - u32: r4
 - u32: r5
- Response:
 - Length: 4
 - Value:
 - u32: r0

Calls the function at given (bus) address and with arguments given. E.g. $r0 = fn(r0, r1, r2, r3, r4, r5)$; It blocks until call completes. The (GPU) instruction cache is implicitly flushed. Setting the lsb of function pointer address will suppress the instruction cache flush if you know the buffer hasn't changed since last execution.

<https://github.com/raspberrypi/firmware/wiki/Mailbox-property-interface#execute-code>

MMIO Registers

MMIO Registers

arch/arm/boot/dts/bcm2711-rpi-ds.dtsi

```
compatible = "brcm,2711-v3d";
reg =
    <0x7ec00000  0x0  0x4000>,
    <0x7ec04000  0x0  0x4000>;
reg-names = "hub", "core0";
```

MMIO Registers

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compatible = "brcm,2711-v3d";
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    <0x7ec04000 0x0 0x4000>;
reg-names = "hub", "core0";
```

drivers/gpu/drm/v3d/v3d_regs.h

#define V3D_HUB_AXICFG	0x00000
# define V3D_HUB_AXICFG_MAX_LEN_MASK	V3D_MASK(3, 0)
# define V3D_HUB_AXICFG_MAX_LEN_SHIFT	0
#define V3D_HUB_UIFCFG	0x00004
#define V3D_HUB_IDENT0	0x00008
#define V3D_HUB_IDENT1	0x0000c
# define V3D_HUB_IDENT1_WITH_MS0	BIT(19)
# define V3D_HUB_IDENT1_WITH_TSY	BIT(18)
# define V3D_HUB_IDENT1_WITH_TFU	BIT(17)
# define V3D_HUB_IDENT1_WITH_L3C	BIT(16)
# define V3D_HUB_IDENT1_NHOSTS_MASK	V3D_MASK(15, 12)
# define V3D_HUB_IDENT1_NHOSTS_SHIFT	12
# define V3D_HUB_IDENT1_NCORES_MASK	V3D_MASK(11, 8)
# define V3D_HUB_IDENT1_NCORES_SHIFT	8
# define V3D_HUB_IDENT1_REV_MASK	V3D_MASK(7, 4)
# define V3D_HUB_IDENT1_REV_SHIFT	4
# define V3D_HUB_IDENT1_TVER_MASK	V3D_MASK(3, 0)
# define V3D_HUB_IDENT1_TVER_SHIFT	0

MMIO Registers

MMIO Registers

V3D_HUB_IDENT0 : 0x42554856 ("VHUB")

MMIO Registers

V3D_HUB_IDENT0 : 0x42554856 ("VHUB")

*V3D_HUB_IDENT0 =

MMIO Registers

V3D_HUB_IDENT0 : 0x42554856 ("VHUB")

*V3D_HUB_IDENT0 = **0xDEADBEEF**

MMIO Registers

V3D_HUB_IDENT0 : 0x42554856 ("VHUB")

*V3D_HUB_IDENT0 = 0xDEADBEEF

<https://forums.raspberrypi.com/viewtopic.php?f=72&t=35966>

3. Back on the ARM side I started to trawl thru the Linux sources to see how they turn on the V3D, after a day of work I had managed to crash the BUS of the V3D enough so that instead of showing me 0xDEADBEEF, it crashed the R-Pi with any read from V3D peripheral region of memory only, possibly making it into the same state as my bootcode.bin demo.

4. I had noticed from my **Tags Channel** demo <https://github.com/PeterLemon/Raspberry...agsChannel> that in bare metal the V3D is in an "Enabled" state, but the frequency is set to zero, so I forced the clock frequency of the V3D to 250MHz using (250 * 1000 * 1000) which I had found in Linux sources. I then tried reading the V3D registers but still got 0xDEADBEEF...

5. Finally I remembered that **Herman H Hermitage** had done a Fast Fourier Transform demo using the QPU and I started to look at the sources... I found that he used 2 new totally undocumented **Mailbox Property Interface** tags, namely 0x30011 = Execute_QPU, & 0x30012 = Enable_QPU. So I ran the tag "Enable_QPU" using 1 as my data, to set it to enable, and then tried reading the V3D registers and magically it kicks it into place!

This is really neat as my main V3D initialization is 2 simple concatenated tags of: (A) Set V3D Clock To 250Mhz, (B) Enable The QPU =D
A massive thankyou to **Herman H Hermitage**, without your help I would not have got it to work!!

I hope you guys like this, as it is a stepping stone to fully alpha blended textured shaded 2D & 3D GFX in bare metal on the Raspberry Pi, which will make the homebrew scene on this wonderful HW explode!

For my next V3D demo, I will try to show you guys howto run **Control Lists**, so we can use OpenGL ES style functions to draw HW GFX to the screen =D

P.S We need to put those 2 new QPU Mailbox Property Tags onto some wiki or document, as they were so hard to find, and they are very important.

Logging register accesses

Logging register accesses

```
1 static inline u32 v3d_readl_wrapper(void* addr, const char* name, const char* file, int line)
2 {
3     printk("v3d-test: V3D_READ() : %s(0x%016llx) in %s:%d", name, (u64)addr, file, line);
4     return readl(addr);
5 }
6
7 static inline void v3d_writel_wrapper(u32 val, void* addr, const char* name, const char* file, int line)
8 {
9     printk("v3d-test: V3D_WRITE(0x%x) : %s(0x%016llx) in %s:%d", val, name, (u64)addr, file, line);
10    writel(val, addr);
11 }
12
13 #define V3D_READ(offset) v3d_readl_wrapper(v3d->hub_regs + offset, #offset, __FILE__, __LINE__)
14 #define V3D_WRITE(offset, val) v3d_writel_wrapper(val, v3d->hub_regs + offset, #offset, __FILE__, __LINE__)
15
16 #define V3D_BRIDGE_READ(offset) v3d_readl_wrapper(v3d->bridge_regs + offset, #offset, __FILE__, __LINE__)
17 #define V3D_BRIDGE_WRITE(offset, val) v3d_writel_wrapper(val, v3d->bridge_regs + offset, #offset, __FILE__, __LINE__)
18
19 #define V3D_GCA_READ(offset) v3d_readl_wrapper(v3d->gca_regs + offset, #offset, __FILE__, __LINE__)
20 #define V3D_GCA_WRITE(offset, val) v3d_writel_wrapper(val, v3d->gca_regs + offset, #offset, __FILE__, __LINE__)
21
22 #define V3D_CORE_READ(core, offset) v3d_readl_wrapper(v3d->core_regs[core] + offset, #offset, __FILE__, __LINE__)
23 #define V3D_CORE_WRITE(core, offset, val) v3d_writel_wrapper(val, v3d->core_regs[core] + offset, #offset, __FILE__, __LINE__)
```

Logging register accesses

```
1 static inline u32 v3d_readl_wrapper(void* addr, const char* name, const char* file, int line)
2 {
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4     return readl(addr);
5 }
6
7 static inline void v3d_writel_wrapper(u32 val, void* addr, const char* name, const char* file, int line)
8 {
9     printk("v3d-test: V3D_WRITE(0x%08X) : %s(0x%016llx) in %s:%d", val, name, (u64)addr, file, line);
10    writel(val, addr);
11 }
12
13 #define V3D_READ(offset) v3d_readl_wrapper(v3d->hub_regs + offset, #offset, __FILE__, __LINE__)
14 #define V3D_WRITE(offset, val) v3d_writel_wrapper(val, v3d->hub_regs + offset, #offset, __FILE__, __LINE__)
15
16 #define V3D_BRIDGE_READ(offset) v3d_readl_wrapper(v3d->bridge_regs + offset, #offset, __FILE__, __LINE__)
17 #define V3D_BRIDGE_WRITE(offset, val) v3d_writel_wrapper(val, v3d->bridge_regs + offset, #offset, __FILE__, __LINE__)
18
19 #define V3D_GCA_READ(offset) v3d_readl_wrapper(v3d->gca_regs + offset, #offset, __FILE__, __LINE__)
20 #define V3D_GCA_WRITE(offset, val) v3d_writel_wrapper(val, v3d->gca_regs + offset, #offset, __FILE__, __LINE__)
21
22 #define V3D_CORE_READ(core, offset) v3d_readl_wrapper(v3d->core_regs[core] + offset, #offset, __FILE__, __LINE__)
23 #define V3D_CORE_WRITE(core, offset, val) v3d_writel_wrapper(val, v3d->core_regs[core] + offset, #offset, __FILE__, __LINE__)
```

\$ dmesg | grep "v3d"

```
...
[ 1.873515] v3d-mbox: tag=RPI_FIRMWARE_SET_GPIO_STATE(0x00038041), size=0x8, buf=8400000000000000
[ 1.881719] v3d-mbox: tag=RPI_FIRMWARE_GET_CLOCK_STATE(0x00030001), size=0x12, buf=0E0000000000000000000000
[ 1.881789] v3d-mbox: tag=RPI_FIRMWARE_GET_CLOCK_STATE(0x00030001), size=0x12, buf=0D0000000000000000000000
[ 1.884571] v3d-mbox: tag=RPI_FIRMWARE_GET_CLOCK_STATE(0x00030001), size=0x12, buf=0B0000000000000000000000
[ 1.887295] v3d-mbox: tag=RPI_FIRMWARE_GET_CLOCK_STATE(0x00030001), size=0x12, buf=050000000000000000000000
[ 1.889991] v3d-mbox: tag=RPI_FIRMWARE_GET_CLOCK_STATE(0x00030001), size=0x12, buf=040000000000000000000000
[ 1.892633] v3d-mbox: tag=RPI_FIRMWARE_GET_CLOCK_STATE(0x00030001), size=0x12, buf=030000000000000000000000
[ 1.943423] v3d-mbox: tag=RPI_FIRMWARE_SET_GPIO_STATE(0x00038041), size=0x8, buf=840000001000000
[ 19.801280] v3d-test: V3D_READ() : V3D_MMU_DEBUG_INFO(0xFFFFFFF011C99238) in drivers/gpu/drm/v3d/v3d_drv.c:266
[ 19.801304] v3d-test: V3D_READ() : V3D_HUB_IDENT1(0xFFFFFFF011C9800C) in drivers/gpu/drm/v3d/v3d_drv.c:271
[ 19.801378] v3d-mbox: tag=RPI_FIRMWARE_GET_CLOCK_RATE(0x00030002), size=0x12, buf=050000000000000000000000
[ 19.806450] v3d-test: V3D_WRITE(0x0) : V3D_CTL_L2TFLSTA(0xFFFFFFF011CA8034) in drivers/gpu/drm/v3d/v3d_gem.c:78
[ 19.806472] v3d-test: V3D_WRITE(0xFFFFFFFF) : V3D_CTL_L2TFLEND(0xFFFFFFF011CA8038) in drivers/gpu/drm/v3d/v3d_gem.c:79
[ 19.806489] v3d-test: V3D_WRITE(0x1B600) : V3D_MMU_PT_PA_BASE(0xFFFFFFF011C99204) in drivers/gpu/drm/v3d/v3d_mmu.c:71
[ 19.806504] v3d-test: V3D_WRITE(0x60D0C01) : V3D_MMU_CTL(0xFFFFFFF011C99200) in drivers/gpu/drm/v3d/v3d_mmu.c:72
[ 19.806518] v3d-test: V3D_WRITE(0x8006373C) : V3D_MMU_ILLEGAL_ADDR(0xFFFFFFF011C99230) in drivers/gpu/drm/v3d/v3d_mmu.c:81
...
```

MMIO Registers

MMIO Registers

```
1 void v3d_test_ident0(void)
2 {
3     u32* addr = ioremap(0xFEC00000, 0x4000);
4     if (addr)
5         printk("v3d-ident0: 0x%08X", addr[2]);
6     else
7         printk("v3d-error: ioremap failed");
8 }
```

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6     else
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8 }
```

drivers/soc/bcm/bcm2835-power.c

```
1 printk("bcm2835_asb_power_on 6");
2 v3d_test_ident0();
3
4 ret = bcm2835_asb_enable(power, asb_s_reg);
5 if (ret) {
6     dev_err(power->dev, "Failed to enable ASB slave for %s\n",
7             pd->base.name);
8     goto err_disable_asb_master;
9 }
10
11 printk("bcm2835_asb_power_on 7");
12 v3d_test_ident0();
```

MMIO Registers

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1 void v3d_test_ident0(void)
2 {
3     u32* addr = ioremap(0xFEC00000, 0x4000);
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6     else
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8 }
```

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4 ret = bcm2835_asb_enable(power, asb_s_reg);
5 if (ret) {
6     dev_err(power->dev, "Failed to enable ASB slave for %s\n",
7             pd->base.name);
8     goto err_disable_asb_master;
9 }
10
11 printk("bcm2835_asb_power_on 7");
12 v3d_test_ident0();
```

```
[    8.803038] bcm2835_asb_power_on 6
[    8.803059] v3d-ident0: 0xDEADBEEF
[    8.803069] bcm2835_asb_power_on 7
[    8.803105] v3d-ident0: 0x42554856
```

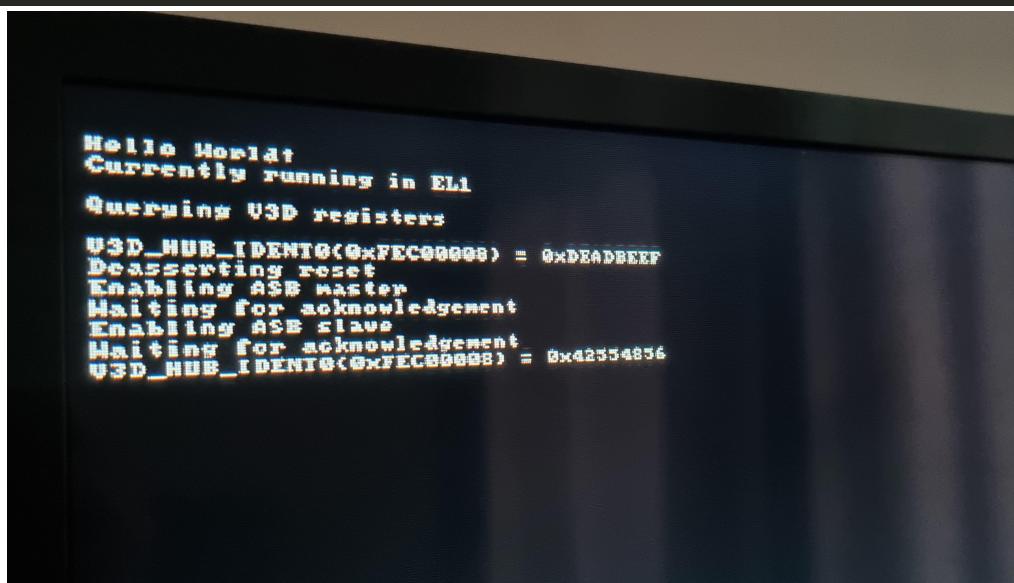
MMIO Registers

MMIO Registers

```
1 static constexpr u32 PM_V3DRSTN      = bit(6);
2 static constexpr u32 PM_PASSWORD     = 0x5A000000;
3 static constexpr u32 ASB_REQ_STOP    = bit(0);
4 static constexpr u32 ASB_ACK         = bit(1);
5 static constexpr u32 ASB_EMPTY       = bit(2);
6 static constexpr u32 ASB_FULL        = bit(3);
7
8 // Deasserting reset
9 MMIO::write(MMIO::PM_GRAFX, MMIO::read(MMIO::PM_GRAFX) | PM_PASSWORD | PM_V3DRSTN);
10
11 // Enabling ASB master
12 MMIO::write(MMIO::ASB_V3D_M_CTRL, PM_PASSWORD | (MMIO::read(MMIO::ASB_V3D_M_CTRL) & ~ASB_REQ_STOP));
13 // Waiting for acknowledgement
14 while (MMIO::read(MMIO::ASB_V3D_M_CTRL) & ASB_ACK);
15
16 // Enabling ASB slave
17 MMIO::write(MMIO::ASB_V3D_S_CTRL, PM_PASSWORD | (MMIO::read(MMIO::ASB_V3D_S_CTRL) & ~ASB_REQ_STOP));
18 // Waiting for acknowledgement
19 while (MMIO::read(MMIO::ASB_V3D_S_CTRL) & ASB_ACK);
```

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13 // Waiting for acknowledgement
14 while (MMIO::read(MMIO::ASB_V3D_M_CTRL) & ASB_ACK);
15
16 // Enabling ASB slave
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18 // Waiting for acknowledgement
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```



GPU Tasks

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 - Takes command lists

GPU Tasks

- CSD (compute shader dispatch)
 - takes code buffer, uniform buffer
 - executes code
- TFU (Texture Formatter Unit)
 - takes source/destination image & format
 - Texture blitting
- Binner/Render
 - Takes command lists
 - Renders commands

CSD Task

CSD Task

```
Hello World!
Currently running in EL1
Testing GPU
code address: 0x3e512000
uniform address: 0x3e5120c0

CSD Status: num active : 0; num completed : 0;
Launching V3D CSD Task
CSD Status: num active : 1; num completed : 0;
Waiting 1 sec...
CSD Status: num active : 0; num completed : 1;
Flushing cache...

Code buffer:
: 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
-----
00000000 : 00 00 00 BB 86 71 80 3D 01 F0 92 B6 81 31 E0 3D
00000010 : 0C 90 83 7C 81 31 E0 3D 03 F0 83 B6 80 31 E0 3D
00000020 : 08 80 83 7C 80 31 E0 3D 03 10 FC B6 01 30 E0 3D
00000030 : 04 80 83 7C 80 31 E0 3D 00 10 00 B6 81 31 00 3C
00000040 : 07 90 83 B6 81 31 E0 3D 00 20 00 B6 82 31 00 3C
00000050 : 00 20 81 B6 8B 31 00 3C 40 60 03 B6 8C 31 00 3C
00000060 : 00 50 81 BB 86 31 00 3C 00 40 81 BB 92 31 20 3C
00000070 : 00 00 00 BB 86 31 00 3C 00 00 00 BB 86 31 00 3C
00000080 : 00 00 00 BB 86 31 20 3C 00 00 00 BB 86 31 20 3C
00000090 : 00 00 00 BB 86 31 00 3C 00 00 00 BB 86 31 00 3C
000000A0 : 00 00 00 BB 86 31 20 3C 00 00 00 BB 86 31 00 3C
000000B0 : 00 00 00 BB 86 31 00 3C 00 00 00 BB 86 31 00 3C

Uniform buffer:
: 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
-----
00000000 : C4 20 51 3E 37 13 00 00

Uniform return value : 0x00001337
```

Binning? Rendering?

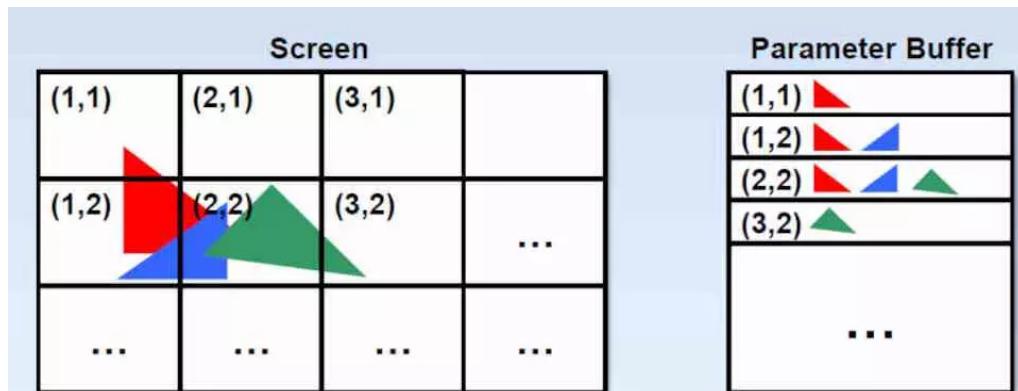
Binning? Rendering?

- The VideoCore VI is a Tile Renderer!

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Binning

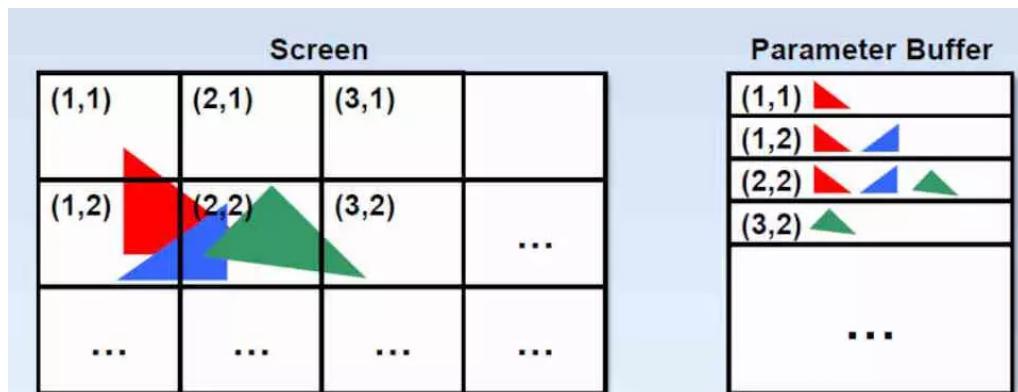


<https://itigic.com/tile-rendering-architecture-of-very-low-consumption-gpus/>

Binning? Rendering?

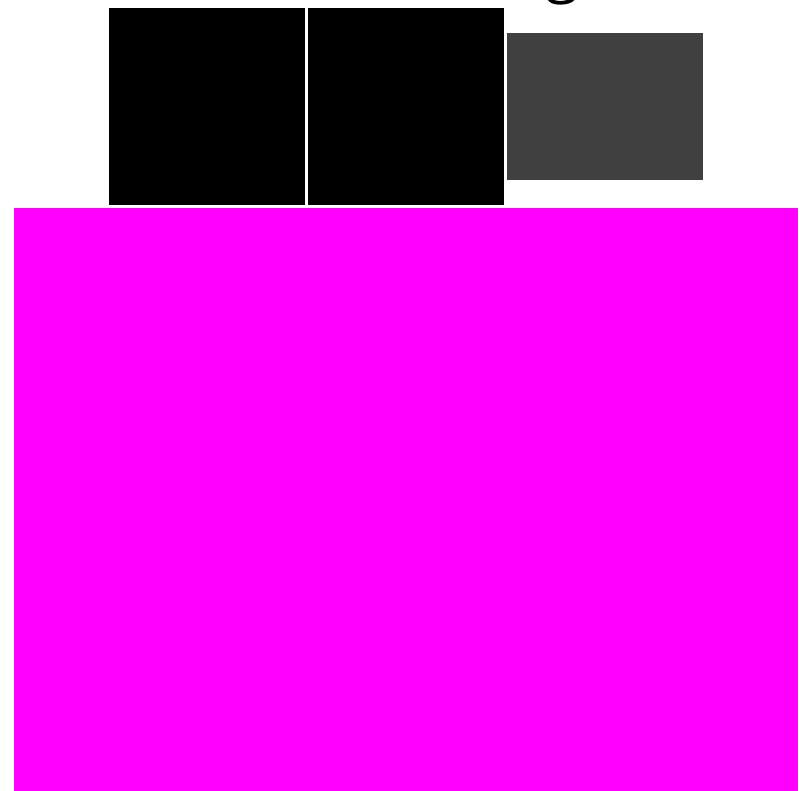
- The VideoCore VI is a Tile Renderer!

Binning



<https://itigic.com/tile-rendering-architecture-of-very-low-consumption-gpus/>

Rendering



<https://developer.samsung.com/galaxy-gamedev/resources/articles/gpu-framebuffer.html>

Figuring out the command list format

Figuring out the command list format

```
1 <struct name="GL Shader State Record" min_ver="41">
2 <field name="Point size in shaded vertex data" size="1" start="0" type="bool"/>
3 <field name="Enable clipping" size="1" start="1" type="bool"/>
4
5 <field name="Vertex ID read by coordinate shader" size="1" start="2" type="bool"/>
6 <field name="Instance ID read by coordinate shader" size="1" start="3" type="bool"/>
7 <field name="Base Instance ID read by coordinate shader" size="1" start="4" type="bool"/>
8 <field name="Vertex ID read by vertex shader" size="1" start="5" type="bool"/>
9 <field name="Instance ID read by vertex shader" size="1" start="6" type="bool"/>
10 <field name="Base Instance ID read by vertex shader" size="1" start="7" type="bool"/>
11
12 <field name="Fragment shader does Z writes" size="1" start="8" type="bool"/>
13 <field name="Turn off early-z test" size="1" start="9" type="bool"/>
14 <field name="Coordinate shader has separate input and output VPM blocks" size="1" start="10" type="bool"/>
15 <field name="Vertex shader has separate input and output VPM blocks" size="1" start="11" type="bool"/>
16 <field name="Fragment shader uses real pixel centre W in addition to centroid W2" size="1" start="12" type="bool"/>
17 <field name="Enable Sample Rate Shading" size="1" start="13" type="bool"/>
18 <field name="Any shader reads hardware-written Primitive ID" size="1" start="14" type="bool"/>
19 <field name="Insert Primitive ID as first varying to fragment shader" size="1" start="15" type="bool"/>
20 <field name="Turn off scoreboard" size="1" start="16" type="bool"/>
21 <field name="Do scoreboard wait on first thread switch" size="1" start="17" type="bool"/>
22 <field name="Disable implicit point/line varyings" size="1" start="18" type="bool"/>
23 <field name="No prim pack" size="1" start="19" type="bool"/>
24
25 <field name="Number of varyings in Fragment Shader" size="8" start="3b" type="uint"/>
26
27 <field name="Coordinate Shader output VPM segment size" size="4" start="4b" type="uint"/>
28 <field name="Min Coord Shader output segments required in play in addition to VCM cache size" size="4" start="36" type="uint"/>
29
30 <field name="Coordinate Shader input VPM segment size" size="4" start="5b" type="uint"/>
31 <field name="Min Coord Shader input segments required in play" size="4" start="44" type="uint" minus_one="true"/>
32
33 <field name="Vertex Shader output VPM segment size" size="4" start="6b" type="uint"/>
34 <field name="Min Vertex Shader output segments required in play in addition to VCM cache size" size="4" start="52" type="uint"/>
35
36 <field name="Vertex Shader input VPM segment size" size="4" start="7b" type="uint"/>
37 <field name="Min Vertex Shader input segments required in play" size="4" start="60" type="uint" minus_one="true"/>
38
```

Tracing GPU communication

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- wrap MMIO registers access macros

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Buffer Objects

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Buffer Objects

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```
***** BCL *****  
78 00 00 00 00 7F 07 37 04 TILE_BINNING_MODE_CFG  
13 FLUSH_VCD_CACHE  
5C 00 00 00 00 OCCLUSION_QUERY_COUNTER  
06 START_TILE_BINNING  
04 FLUSH
```

```
***** INDIRECT *****  
7D TILE_COORDINATES_IMPLICIT  
1A END_OF_LOADS  
38 02 PRIM_LIST_FORMAT  
15 00 BRANCH_TO_IMPLICIT_TILE_LIST  
1D 00 B0 11 00 E0 01 00 00 00 00 06 00 STORE_TILE_BUFFER_GENERAL  
19 03 CLEAR_TILE_BUFFERS  
1B END_OF_TILE_MARKER  
12 RETURN_FROM_SUB_LIST
```

```
***** RCL *****  
79 00 80 07 38 04 00 01 00 TILE_RENDERING_MODE_CFG_COMMON  
79 03 FF 00 00 FF 00 00 00 TILE_RENDERING_MODE_CFG_CLEAR_COLORS_PART1  
79 81 00 00 00 00 00 00 00 TILE_RENDERING_MODE_CFG_COLOR  
79 02 00 00 00 00 00 00 00 TILE_RENDERING_MODE_CFG_ZS_CLEAR_VALUES  
7E 04 TILE_LIST_INITIAL_BLOCK_SIZE  
7B 00 00 C8 00 MULTICORE_RENDERING_TILE_LIST_SET_BASE  
7A 01 01 0F 09 1E 10 01 00 MULTICORE_RENDERING_SUPERTILE_CFG  
  
7C 00 00 00 TILE_COORDINATES  
1A END_OF_LOADS  
1D 08 00 00 00 00 00 00 00 00 00 00 00 00 STORE_TILE_BUFFER_GENERAL  
19 03 CLEAR_TILE_BUFFERS  
1B END_OF_TILE_MARKER  
7C 00 00 00 TILE_COORDINATES  
1A END_OF_LOADS  
1D 08 00 00 00 00 00 00 00 00 00 00 00 00 STORE_TILE_BUFFER_GENERAL  
1B END_OF_TILE_MARKER  
  
13 FLUSH_VCD_CACHE  
14 00 00 D6 00 17 00 D6 00 START_ADDRESS_OF_GENERIC_TILE_LIST(00D60000-00D60017)  
17 00 00 SUPERTILE_COORDINATES  
17 01 00 SUPERTILE_COORDINATES  
...  
17 0D 08 SUPERTILE_COORDINATES  
17 0E 08 SUPERTILE_COORDINATES  
0D END_OF_RENDERING
```

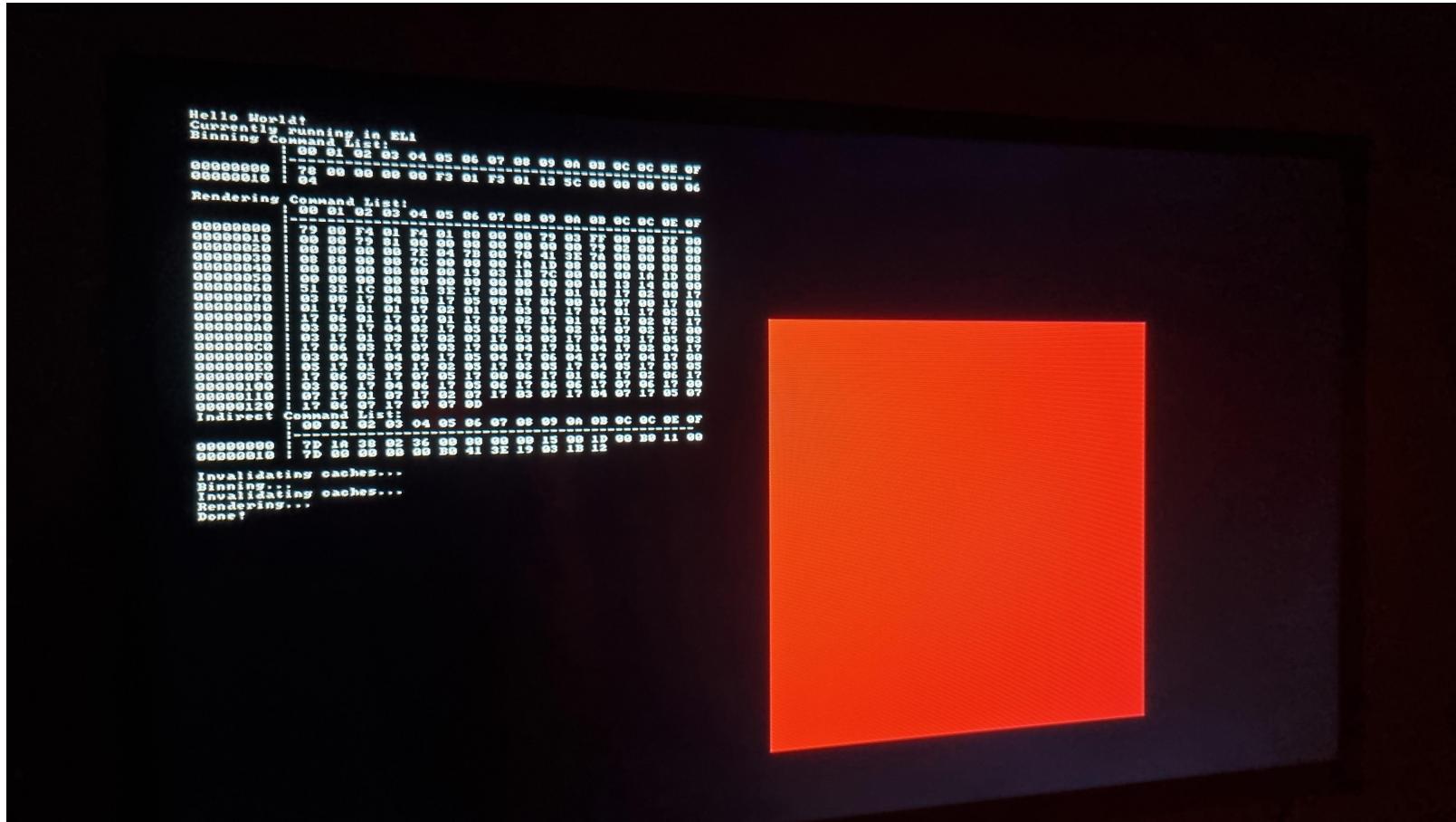
Putting everything together

Putting everything together

```
1 /* ===== BCL ===== */
2 {
3     bcl << TileBinningModeCfg(0, 0, 1, 0, false, false, width, height);
4     bcl << OP_FLUSH_VCD_CACHE;
5     bcl << OcclusionQueryCounter(0);
6     bcl << OP_START_TILE_BINNING;
7
8     bcl << ClipWindow(0, 0, width, height);
9     bcl << CfgBits(true, true, true, false, 0, 0, false, 7, false, false, true, false, false, false, false);
10    bcl << PointSize(1.0f);
11    bcl << LineWidth(1.0f);
12    bcl << ClipperXYScaling((width / 2) * 256.f, (height / 2) * -256.f);
13    bcl << ClipperZScaleAndOffset(.5f, .5f);
14    bcl << ClipperZMinMaxClippingPlanes(0.f, 1.f);
15    bcl << ViewportOffset(width / 2, height / 2, 0, 0);
16    bcl << ColorWriteMasks(0);
17    bcl << BlendConstantColor(0, 0, 0, 0);
18    bcl << OP_ZERO_ALL_FLAT_SHADE_FLAGS;
19    bcl << OP_ZERO_ALL_NON_PERSPECTIVE_FLAGS;
20    bcl << OP_ZERO_ALL_CENTROID_FLAGS;
21    bcl << TransformFeedbackSpecs(0, false);
22    bcl << OcclusionQueryCounter(0);
23    bcl << SampleState(0xF, 1.0f);
24    bcl << VcmCacheSize(4, 4);
25
26    bcl << GlShaderState(shaderStateRecordAddr, attrCount);
27    // mode=4 (triangle)
28    bcl << VertexArrayPrims(4, vertexCount, 0);
29
30    // bcl epilogue
31    bcl << OP_FLUSH;
32 }
33
34 /* ===== RCL ===== */
35 {
36     // must be first
37     rcl << TileRenderingModeCfgCommon(1, width, height, 0, false, false, 0, false, 2, false);
38     rcl << TileRenderingModeCfgClearColorColorsPart1(0, 0xFF101010, 0x00000000);
39     rcl << TileRenderingModeCfgColor(0, 2, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0);
40     // must be last
41     rcl << TileRenderingModeCfgZSClearValues(0, 1.0f);
42     rcl << TileListInitialBlockSize(0, true);
43
44     u32 superTileW;
45     u32 superTileH;
46     u32 frameWSupertile;
47     u32 frameHSupertile;
48     getSuperTiles(superTileW, superTileH, frameWSupertile, frameHSupertile, tilesX, tilesY);
```

First Render!

First Render!



Actual Geometry

We need shaders

```
1 GLShaderStateRecord shader{};
2 shader.enable_clipping = true;
3 shader.fragment_shader_uses_real_pixel_centre_w_in_addition_to_centroid_w2 = true;
4 shader.disable_implicit_point_line_varyings = true;
5 shader.number_of_varyings_in_fragment_shader = 4; // 4 component color
6 shader.coordinate_shader_output_vpm_segment_size = 1;
7 shader.coordinate_shader_input_vpm_segment_size = 1;
8 shader.vertex_shader_output_vpm_segment_size = 1;
9 shader.vertex_shader_input_vpm_segment_size = 1;
10 shader.address_of_default_attribute_values = defaultAttrAddr;
11
12 shader.fragment_shader_code_address = fragShaderAddr >> 3;
13 shader.fragment_shader_uniforms_address = fragUnifAddr;
14 shader.fragment_shader_4_way_threadable = true;
15 shader.fragment_shader_start_in_final_thread_section = false;
16 shader.fragment_shader_propagate_nans = true;
17
18 shader.vertex_shader_code_address = vtxShaderAddr >> 3;
19 shader.vertex_shader_uniforms_address = vtxUnifAddr;
20 shader.vertex_shader_4_way_threadable = true;
21 shader.vertex_shader_start_in_final_thread_section = true;
22 shader.vertex_shader_propagate_nans = true;
23
24 shader.coordinate_shader_code_address = coordShaderAddr >> 3;
25 shader.coordinate_shader_uniforms_address = coordUnifAddr;
26 shader.coordinate_shader_4_way_threadable = true;
27 shader.coordinate_shader_start_in_final_thread_section = true;
28 shader.coordinate_shader_propagate_nans = true;
29 indirect << shader;
```

and attributes

```
1 // positions
2 GlShaderStateAttributeRecord posAttr{};
3 posAttr.address = posAttrAddr;
4 posAttr.number_of_values_read_by_vertex_shader = 3;
5 posAttr.number_of_values_read_by_coordinate_shader = 3;
6 posAttr.instance_divisor = 0;
7 posAttr.stride = 3 * sizeof(f32);
8 posAttr.maximum_index = 0xFFFFFFF;
9 posAttr.vec_size = 3;
10 posAttr.type = 2; // ATTRIBUTE_FLOAT
11
12 // colors
13 GlShaderStateAttributeRecord colorAttr;
14 colorAttr.address = colorAttrAddr;
15 colorAttr.number_of_values_read_by_vertex_shader = 4;
16 colorAttr.number_of_values_read_by_coordinate_shader = 0;
17 colorAttr.instance_divisor = 0;
18 colorAttr.stride = 4 * sizeof(u8);
19 colorAttr.maximum_index = 0xFFFFFFF;
20 colorAttr.type = 4; // ATTRIBUTE_BYTE
21 colorAttr.normalized_int_type = true;
22 indirect << colorAttr;
```

Coordinate shaders?

```
1 #version 300 es
2 layout (location = 0) in vec3 position;
3 layout (location = 1) in vec3 normal;
4 layout (location = 2) in vec4 color;
5
6 uniform mat4 u_model;
7 uniform mat4 u_view;
8 uniform mat4 u_proj;
9
10 out vec4 v_color;
11 out vec3 v_normal;
12
13 void main()
14 {
15     v_color = color;
16     v_normal = mat3(transpose(inverse(u_model))) * normal;
17     gl_Position = u_proj * u_view * u_model * vec4(position, 1.0);
18 }
```

Coordinate shaders?

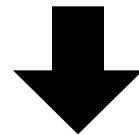
```
1 #version 300 es
2 layout (location = 0) in vec3 position;
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14 {
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17     gl_Position = u_proj * u_view * u_model * vec4(position, 1.0);
18 }
```

Coordinate shaders?

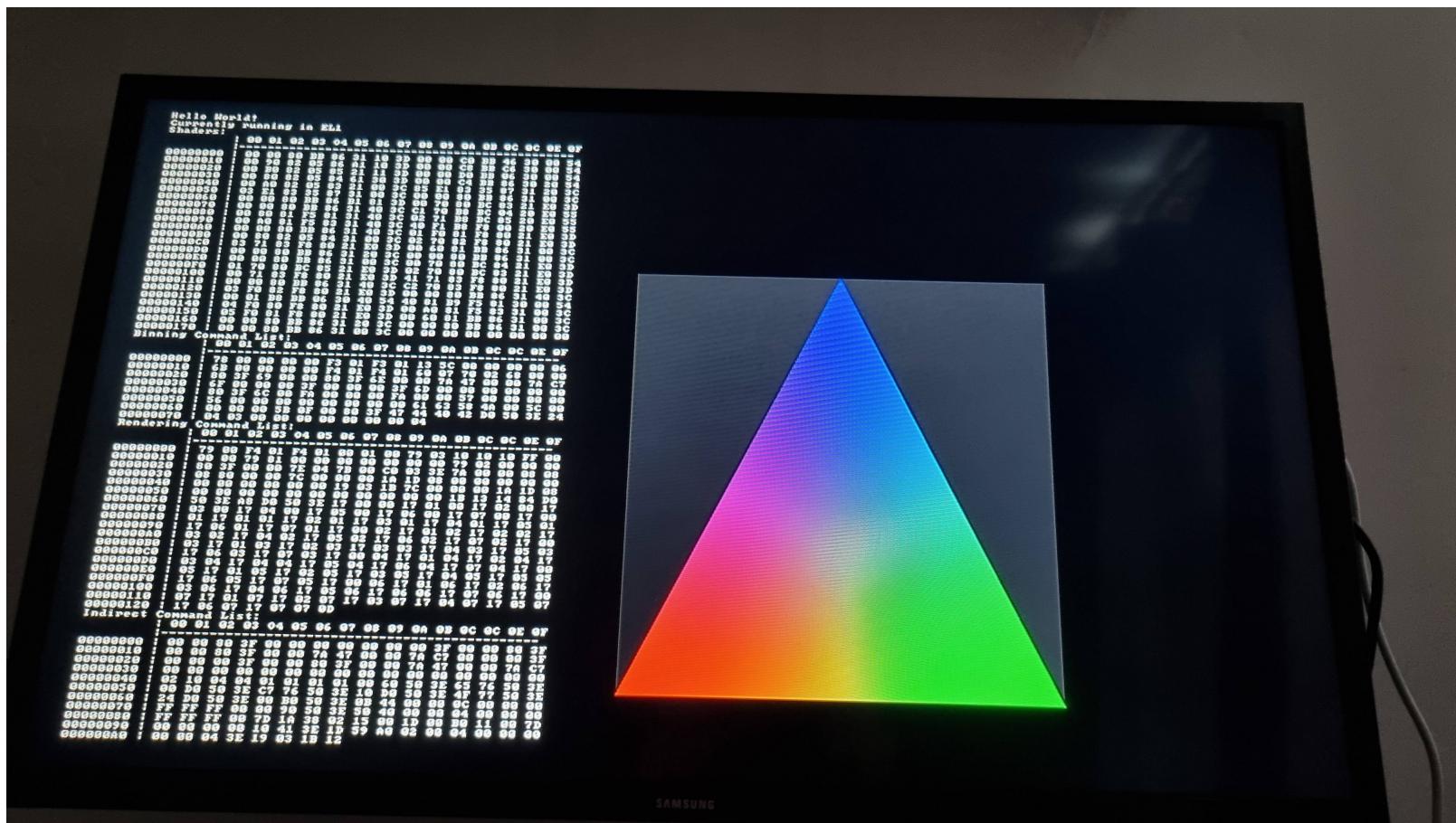
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```



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11 }
```

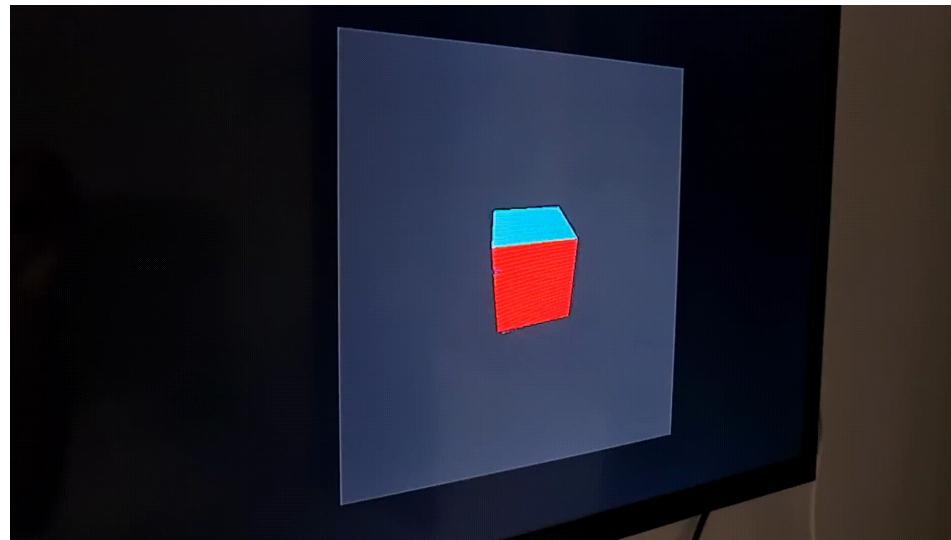
First Triangle!

First Triangle!

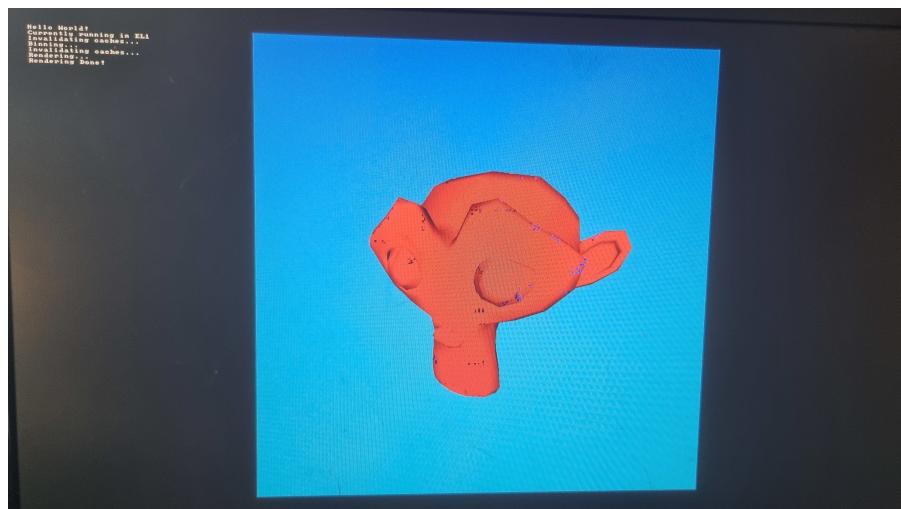
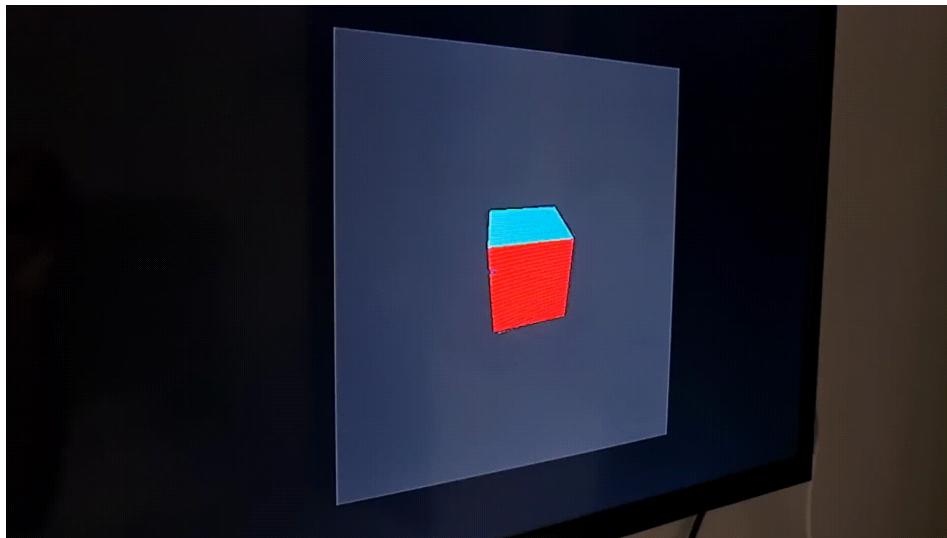


More complex scenes

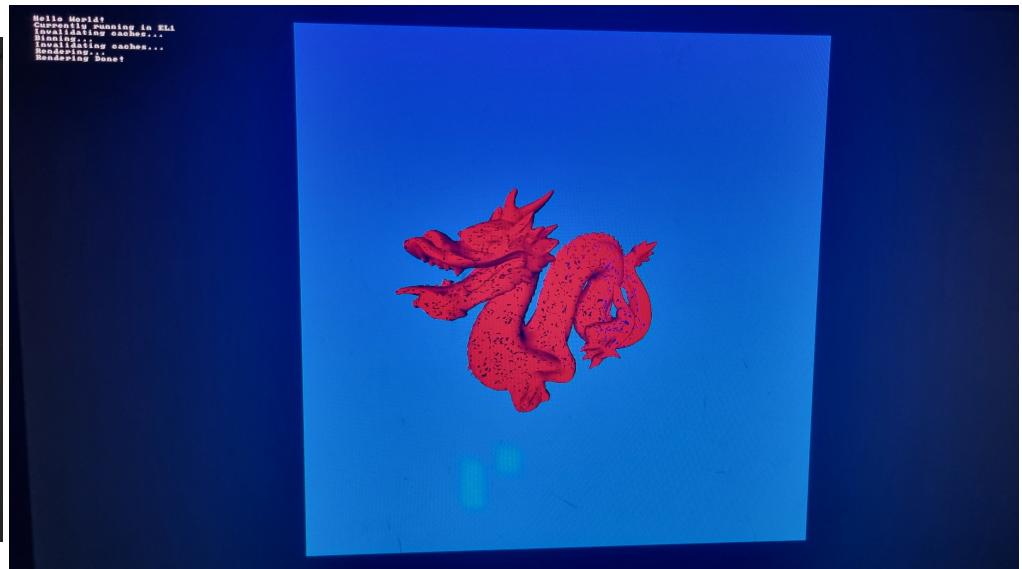
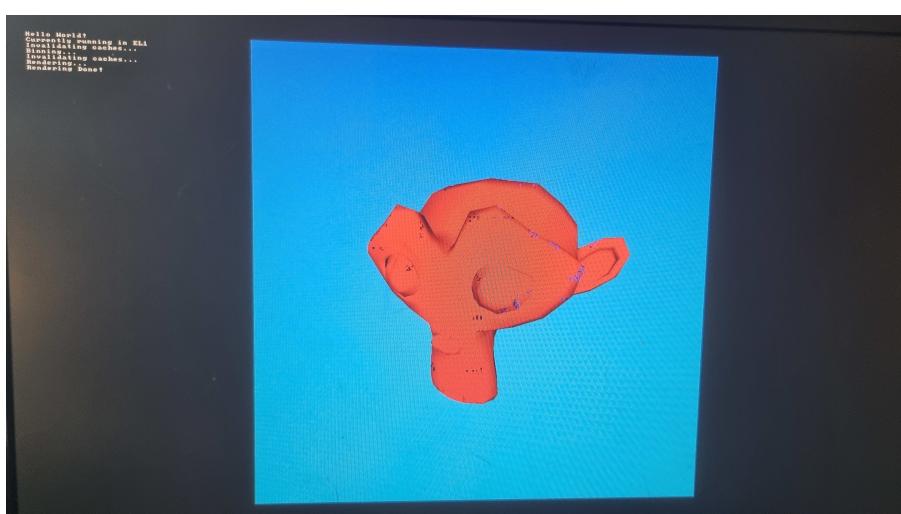
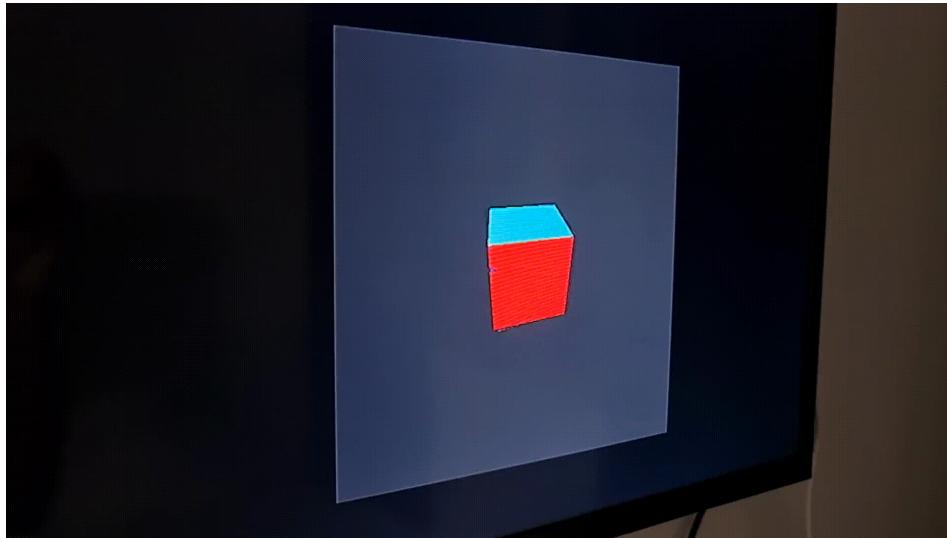
More complex scenes



More complex scenes



More complex scenes



Mini OpenGL API

Mini OpenGL API

<https://webgl2fundamentals.org/webgl/lessons/resources/webgl-state-diagram.html>

The screenshot displays the WebGL State Diagram tool interface, which visualizes the OpenGL state stack. It includes several panels:

- global state**: Shows common state like VIEWPORT (0, 0, 300, 150), CURRENT_PROGRAM (prg), and ACTIVE_TEXTURE (TEXTURE3). It also lists Texture Units (2D, CUBE_MAP, 3D, 2D_ARRAY, SAMPLER) and clear states.
- program[prg]**: Displays attached shaders, attribute info (position, normal, texcoord), transform feedback varyings, uniforms (projection, modelView, diffuseMult, lightDir, diffuse, decal), and state (LINK_STATUS: true).
- vertex array[cubeVertexArray]**: Shows attributes (position, normal, texture, texCoord) and state (ELEMENT_ARRAY_BUFFER_BINDING: null, indexBuffer: null).
- canvas**: A preview window showing three cubes with textures and lighting.
- Code Editor**: A code editor pane containing JavaScript code for rendering the cubes, using matrices and WebGL functions like `uniformMatrix4fv`, `drawElements`, and `uniform4fv`.

Mini OpenGL API

```
1 gl.clearColor(0.06f, 0.06f, 0.06f, 1.0f);
2 gl.clearStencil(0.0f);
3 gl.clearDepth(1.0f);
4
5 u32 positionLoc = gl.getAttribLocation(prg, "position");
6 u32 colorLoc = gl.getAttribLocation(prg, "color");
7
8 u32 triangleVAO = gl.createVertexArray();
9 gl.bindVertexArray(triangleVAO);
10
11 u32 positionBuffer = gl.createBuffer();
12 gl.bindBuffer(GL_ARRAY_BUFFER, positionBuffer);
13 gl.bufferData(GL_ARRAY_BUFFER, sizeof(g_PosAttrBuff), g_PosAttrBuff, GL_STATIC_DRAW);
14
15 u32 colorBuffer = gl.createBuffer();
16 gl.bindBuffer(GL_ARRAY_BUFFER, colorBuffer);
17 gl.bufferData(GL_ARRAY_BUFFER, sizeof(g_ColorAttrBuff), g_ColorAttrBuff, GL_STATIC_DRAW);
18
19
20 gl.enableVertexAttribArray(positionLoc);
21 gl.bindBuffer(GL_ARRAY_BUFFER, positionBuffer);
22 gl.vertexAttribPointer(
23     positionLoc,
24     3,           // 2 values per vertex shader iteration
25     GL_FLOAT,   // data is 32bit floats
26     false,       // don't normalize
27     0,           // stride (0 = auto)
28     0           // offset into buffer
29 );
30
31 gl.bindBuffer(GL_ARRAY_BUFFER, colorBuffer);
32 gl.enableVertexAttribArray(colorLoc);
33 gl.vertexAttribPointer(
34     colorLoc,
35     4,           // 4 values per vertex shader iteration
36     GL_UNSIGNED_BYTE, // data is 8bit unsigned bytes
37     true,        // do normalize
38     0,           // stride (0 = auto)
39     0           // offset into buffer
40 );
41
42 gl.useProgram(prg);
43 gl.drawArrays(GL_TRIANGLES, 0, 3);
```

Conclusion

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- Managed to write a driver that renders basic scenes

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- Progress was non-linear

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- Managed to write a driver that renders basic scenes
- Progress was non-linear
- Command lists are closer to graphics API than expected

TODO:

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- Support texture samplers

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- Reverse engineer Tile allocation / TSDA (Tile State Data Array)

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- handle GPU interrupt
- Write a SPIR-V => QPU compiler

Questions?