Lecture 4a: Robust Analog Circuit Sizing Under Process Variations

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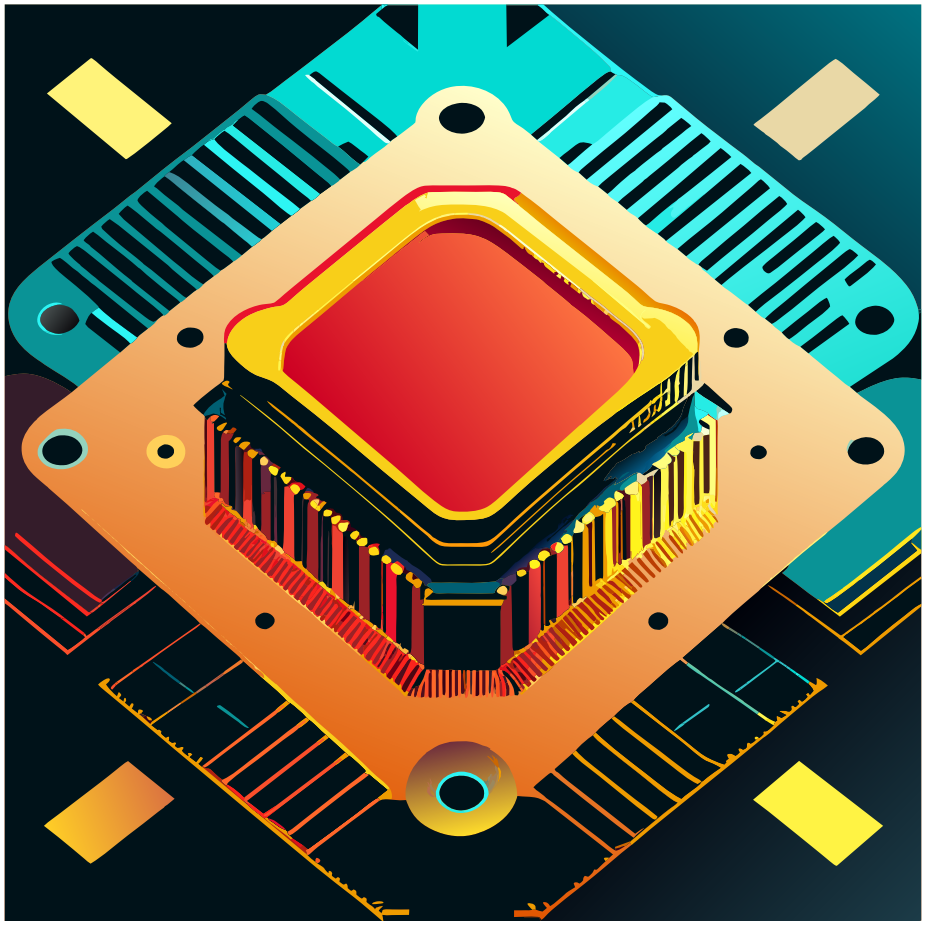

Figure 1: image

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Keywords

- Analog circuit
- Design for robustness
- Worst-case scenarios
- Affine arithmetic
- Convex programming
- Geometric programming
- Posynomial (Positive + polynomial)
- Ellipsoid method

Overview

- Challenges of 20nm Analog Design
- Design for variability
- Design for robustness
- Analog circuit sizing problem formulation
- Robust geometric programming
- Affine arithmetic for worst case scenarios
- Design examples

Introduction

Table 1: Fab, process, mask, and design costs are much higher at 20nm (IBS, May 2011)

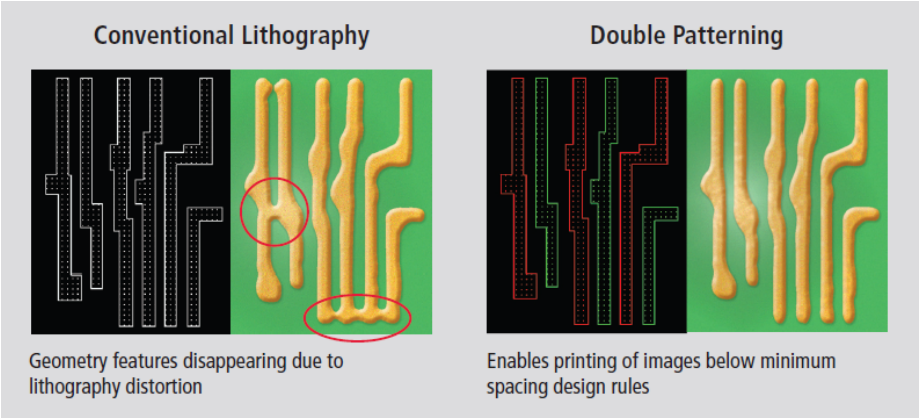
Costs	28nm	20nm
Fab Costs	3B	4B - 7B
Process R&D	1.2B	2.1B - 3B
Mask Costs	2M - 3M	5M - 8M
Design Costs	50M - 90M	120M - 500M

Challenges at 20 nm

- Double-patterning aware
- Layout-dependent effects

- New local interconnect layers
- >5,000 design rules
- Device variation and sensitivity
- New type of transistor - FinFET

Double Patterning



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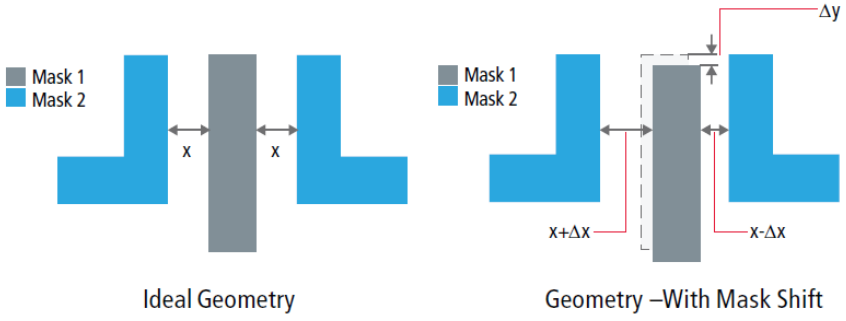
Overlay Error (Mask Shift)

- Parasitic matching becomes very challenging



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Layout-Dependent Effects

Layout-Dependent Effects	> 40nm	At 40nm	>= 28nm
Well Proximity Effect (WPE)	x	x	x
Poly Spacing Effect (PSE)		x	x
Length of Diffusion (LOD)	x	x	x
OD to OD Spacing Effect (OSE)		x	x

New Local Interconnect Layers

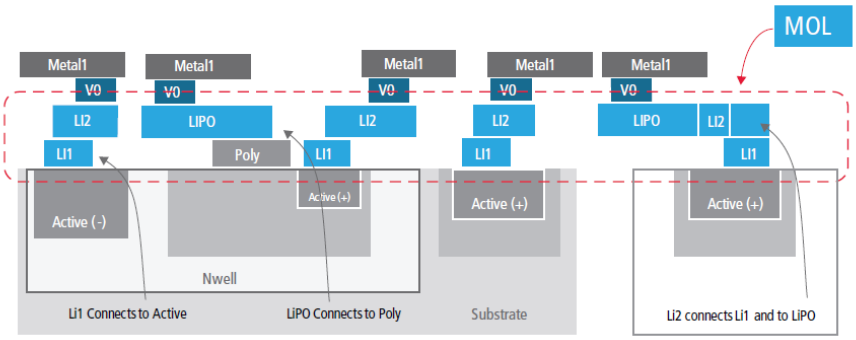

Figure 4: img

New Transistor Type: FinFET

Design for Robustness

- Process variations must be included in the specification.

Basic Design Flow

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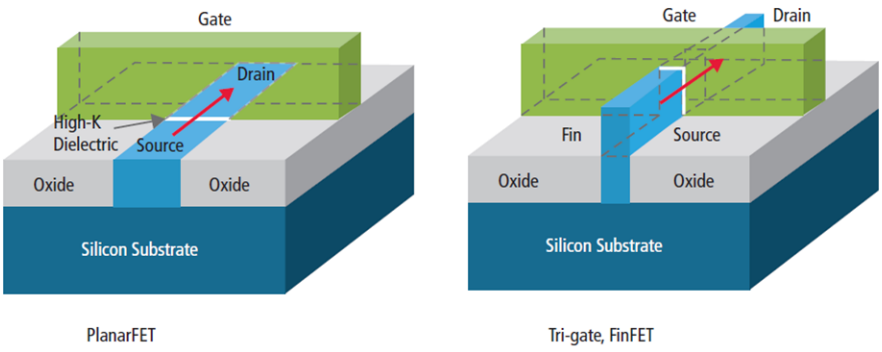

Figure 5: Width is discrete. You can add 2 fins or 3 fins, but not 2.75 fins.

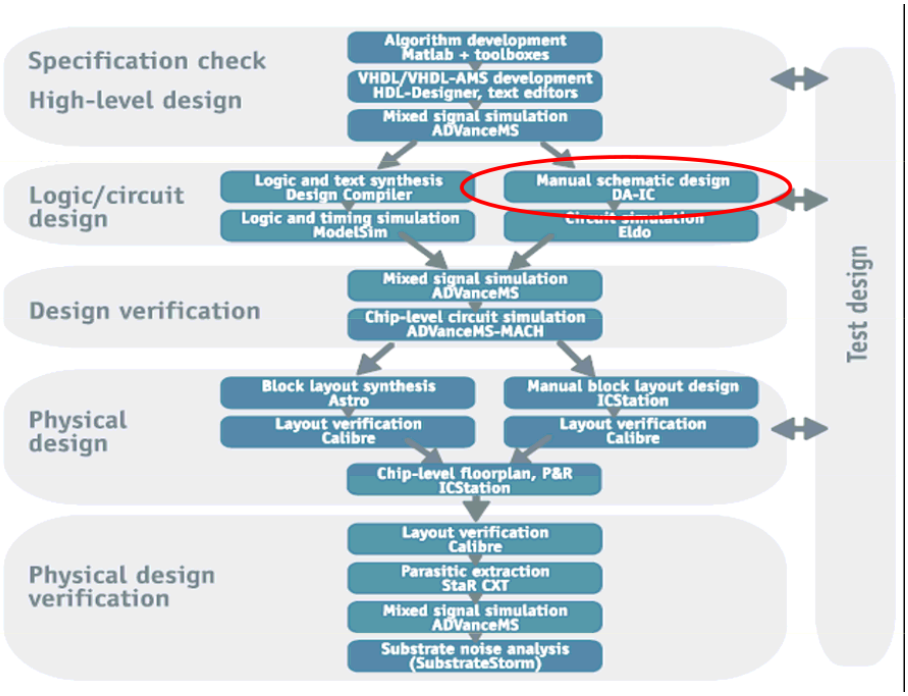

Figure 6: img

Top-down Design Phases

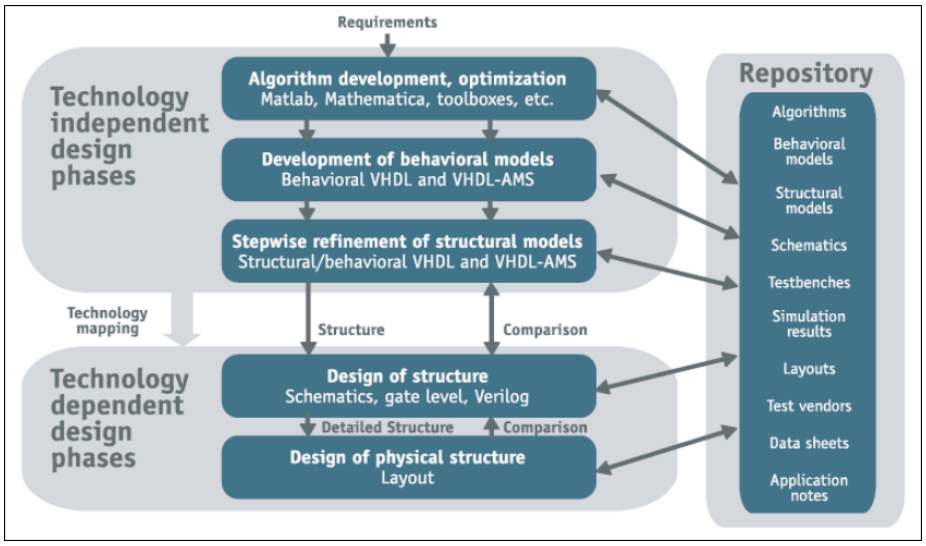

Figure 7: img

Basic Flow of Analog Synthesis

Analog Circuit Sizing Problem

- Problem definition:
  - Given a circuit topology, a set of specification requirements and technology, find the values of design variables that meet the specifications and optimize the circuit performance.
- Difficulties:
  - High degrees of freedom
  - Performance is sensitive to variations

Main Approaches in CAD

- Knowledge-based
  - Rely on circuit understanding, design heuristics

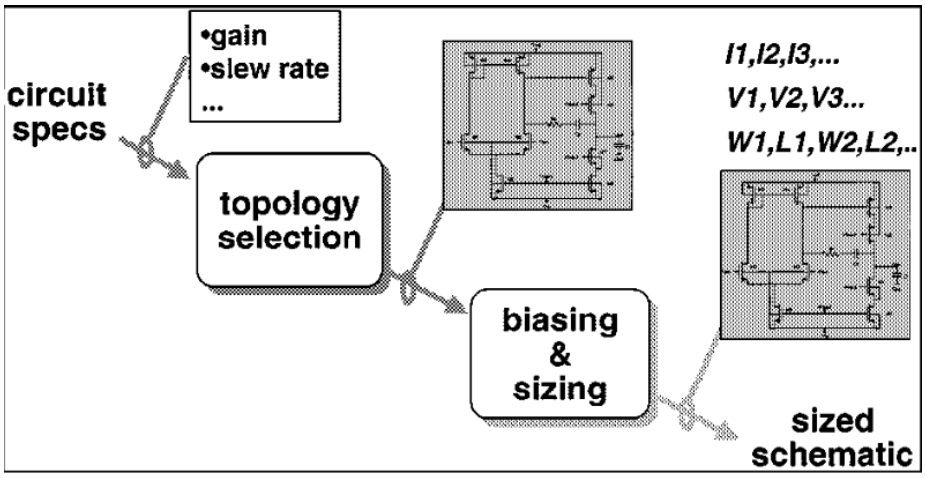

Figure 8: img

- Optimization based
  - **Equation based**
    - Establish circuit equations and use numerical solvers
  - Simulation based
    - Rely on circuit simulation

In practice, you mix and match of them whenever appropriate.

Geometric Programming

- In recent years, techniques of using geometric programming (GP) are emerging.
- In this lecture, we present a new idea of solving robust GP problems using **ellipsoid method** and **affine arithmetic**.