Low Power Latch Based Design with Smart Retiming

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***Abstract*— Flip-flops and latches are two options to construct pipelines in digital integrated circuits (ICs). In this paper, the implications for converting a flip-flop based design to a latch-based design are investigated by performing timing and power analysis. Design flows are also proposed to convert a flip-flop based design to a latch-based design as well as a latch/flip-flop-mixed design. With a new retiming strategy, the optimum operating condition is identified for both the latch based design and the mixed design, where the maximum time borrowing or performance enhancement can be obtained. Compared to the flip-flop based design, 48% and 45% frequency boosting are achieved by the latch based design and the mixed design, respectively. While maintaining the same performance as the flip-flop based design with the aid of supply voltage scaling, the latch based design and the mixed design reduce the power consumption by 21% and 16%, respectively, in an industrial 28-nm FDSOI CMOS technology.**

***Index Terms*—Latch, flip-flop, voltage scaling, time borrowing, power consumption.**

I. Introduction

Portable/wearable devices and Internet-of-Things (IoT) applications are ubiquitous nowadays. As the heart of those devices, intelligent integrated circuits (ICs) play a pivotal role in the applications. ICs in mobile or IoT applications are either powered by battery with limited volume or scavenge energy from surrounding environment. The power/energy consumption requirement for those ICs is therefore rigid. Innovative ultra-low power/energy circuit design techniques are highly desired for ICs in mobile or IoT applications. In digital circuits, sequential circuits are essential for pipelining, synchronization, and intermediate data storage. Sequential circuits as well as the driving clock distribution network account for up to ∼70% of the total power consumption in high-performance as well as ultra-low power ICs [1–4].

Synchronous digital circuits are typically implemented using edge sensitive flip-flops (FF). The design, verification, and test of digital circuits that are designed using flip-flops are well supported by commercial electronic design automation (EDA) tools. An important feature of flip-flop based digital circuit is that the maximum achievable operating frequency of the circuit depends on the propagation delay of the longest path in the pipeline stage. Flip-flop based design method is therefore a worst-case design method. This feature also represents an important drawback of flip-flop based design, especially in high-performance circuits where clock skew and jitter tend to dominate the clock cycle [5]. The advantage of flip-flop based design is its resilience against duty cycle jitter.

Alternatively, latches are seldomly used in digital design as EDA tools have limited support for latch based (LB) design. The verification and test of latch based design are not trivial, either [6]. Latches are however smaller, faster, and more energy efficient as compared to flip-flops. Latches allow designers to exploit clock skew scheduling to improve cycle time. Designers use latches mainly to reduce the sequencing overhead in high-performance processors [7]. Latches provide flexibility of distributing timing budget between neighboring stages such that time borrowing is possible [4], [5], [7–9], thereby further enhancing the speed of the circuit. Latch based designs however have longer hold time requirement compared to flip-flop based designs.

There are a few investigations of latch based design in the literature. In [10], flip-flop based designs of FIR filter, shift register (SR), and multiply and accumulate (MAC) unit are converted to latch based designs. Up to 45% of energy savings is achieved by the latch based designs as compared to flip-flop based designs in sub-threshold region. Similar work is introduced in [11] with the implementation of latch based FIR filter. Compared to the conventional flip-flop based filter, this latch based filter reduces the energy consumption by more than 25%. In [12], an ARM Cortex-M3 is converted to latch based design to eliminate the timing margins by using Bubble Razor, which unfortunately consumes more power compared to the original flip-flop based design. In [13], a latch based 32-bit icyflex2 processor is implemented, showing minimum energy consumption per operation as low as 17.1 pJ/cycle at 19 kHz and 0.37 V.

In this paper, timing and power analysis is performed for both flip-flop based and latch based designs. The trade-offs for converting a flip-flop based design to a latch based design are formulated. Design flows of converting a flip-flop based design to a latch based design as well as a latch/flip-flop-mixed design are proposed. Based on a smart retiming strategy, the optimum operating condition for the latch based as well as the latch/flip-flop-mixed design is identified for achieving the maximum time borrowing, and hence the highest power savings by scaling supply voltage.

This paper is organized as follows. In Section II, the timing requirement and power consumption for flip-flop and latch based designs are formulated. The flows for converting any flip-flop based design to latch based design and latch/flip-flop-mixed design for the maximum power savings are proposed in Section III. In Section III, we elaborate the smart retiming strategy for latch based design. In Section IV, the evaluation of latch based design is presented. The

experimental results for the latch based design and latch/flip-flop-mixed design are presented by using ARM Cortex-M0 as the test circuit. Finally, conclusions are drawn in Section V.

II. Timing and Power Analysis for Synchronous Designs

Power dissipation in digital CMOS circuits has two major components: dynamic switching power consumption and leakage power consumption. The dynamic power consumption is the major component in designs operating in the super-threshold voltage region, while leakage power consumption plays a critical role in designs operating in the idle mode for most of the time or in ultra-low voltage region. Without loss of generality, we ignore the power dissipation by short circuit current in the analysis. The power dissipation of a digital circuit is

$$\begin{aligned} P &= P_{dynamic} + P_{leakage} \\ &= \alpha C_L V_{dd}^2 f + I_{leakage} V_{dd} \end{aligned} \tag{1}$$

$P_{dynamic}$ is the dynamic power consumption, where C_L is the loading capacitance, f is the clock frequency, and α is the activity factor. $P_{leakage}$ is the leakage power consumption. $I_{leakage}$ is the leakage current which consists of sub-threshold, gate, and substrate junction leakage currents. The timing-driven power analysis of flip-flop based and latch based designs is performed in this section. More attention is paid to the dynamic power consumption in this work.

The flip-flop based and latch based pipeline structures are shown in Fig. 1. Latch based design has twice the number of pipeline stages compared to the flip-flop based design. The combinational logic in a single pipeline stage of the flip-flop based design is divided into two latch pipeline stages, assuming both designs target similar operating frequencies. In this work, we try to relate the time borrowing property in latch based design to the power consumption of the circuit. According to Fig. 1, the setup timing constraint for flip-flop based design in terms of equivalent logical depth (assuming $L_{DF1} = L_{DF2}$), setup time (T_{SU}), clock skew (T_{SKEW}), and clock period (T_{CLKF}) is

$$T_{CLKF} \geq \tau_g L_{DF1} + T_{CQ} + T_{SU} - T_{SKEW}, \tag{2}$$

where T_{CQ} is the clock-to-Q propagation delay. τ_g is the equivalent single gate delay. It is highly possible that $L_{DF1} \neq L_{DF2}$ (assuming $L_{DF1} \geq L_{DF2}$). The maximum operating frequency is decided by the timing critical path. The power consumption of a flip-flop based design is

$$P_{dynamic-f} = \frac{\alpha_f C_f V_{dd}^2}{\tau_g L_{DF1} + T_{CQ} + T_{SU} - T_{SKEW}}. \tag{3}$$

For the latch based design, where each flip-flop is split into one positive latch and one negative latch, the clock period (T_{CLKL}) can be written in terms of equivalent logical depth ($L_{DL} = L_{DL1} + L_{DL2} + L_{DL3} + L_{DL4} = L_{DF1} + L_{DF2}$).

$$\begin{aligned} 2T_{CLKL} \geq\ & \tau_g L_{DL1} + T_{DQ-} + \tau_g L_{DL2} + T_{DQ+} \\ & + \tau_g L_{DL3} + T_{DQ-} + \tau_g L_{DL4} + T_{DQ+} + T_{SU} \\ & - T_{SKEW}. \end{aligned} \tag{4}$$

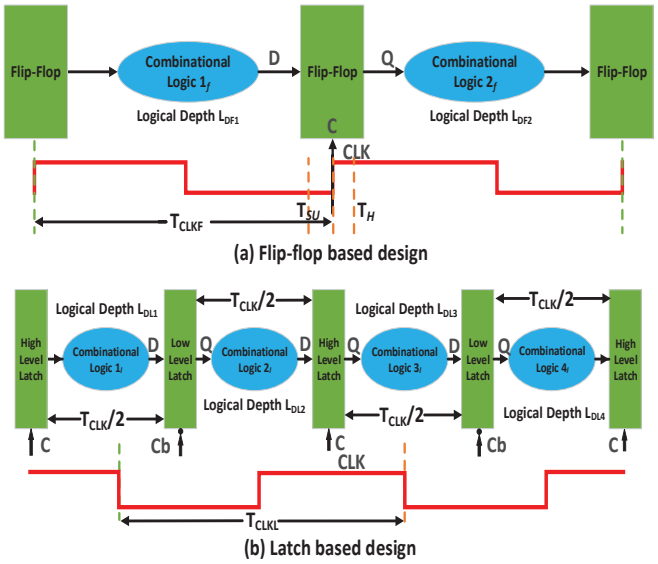

Fig. 1. Flip-flop based and latch based pipeline structures.

$$T_{CLKL} \geq \frac{\tau_g L_{DL}}{2} + \frac{4T_{DQL}}{2} + \frac{T_{SU}}{2} - \frac{T_{SKEW}}{2}, \tag{5}$$

where T_{DQL} ($T_{DQL} = T_{DQ+} = T_{DQ-}$) is the D-to-Q propagation delay of a latch. For latch based design, because of time borrowing, different pipeline stages can share the available timing slack. Therefore, latch based designs have the chance to operate at higher frequencies ($T_{CLKF} > T_{CLKL}$) compared to flip-flop based designs. (5) is for the case of two pipeline stages. If there are K pipeline stages, the clock period can be written as

$$T_{CLKL} \geq \frac{\tau_g L_{DL}}{K} + 2T_{DQL} + \frac{T_{SU}}{K} - \frac{T_{SKEW}}{K}. \tag{6}$$

From (6), the latch based design for any pipelined circuit displays advantage over flip-flop based design in terms of skew tolerance. The time which can be borrowed from the neighboring stage in a latch based design is

$$T_{borrow} \leq \frac{T_{CLKL}}{2} - T_{SU}. \tag{7}$$

For pipelined circuits, the time borrowing can be accumulative from the first stage to the last stage, thereby resulting in shorter clock period. The power consumption of a latch based design is

$$P_{dynamic-l} = \frac{\alpha_l C_l V_{dd}^2}{\frac{\tau_g L_{DL}}{K} + 2T_{DQL} + \frac{T_{SU}}{K} - \frac{T_{SKEW}}{K}}. \tag{8}$$

Since the frequency is higher for latch based design, we can scale the supply voltage to get the same frequency as flip-flop based design. For accessing the scaled voltage, we can express the critical path delay in terms of logical depth and equivalent gate delay. The flip-flop/latch delay, setup time, and skew can be modeled in terms of certain number of equivalent gate delays. So we can write $\tau_g L_{DF1} + T_{CQ} + T_{SU} - T_{SKEW} = N_f \tau_g$ for flip-flop based and $\frac{\tau_g L_{DL}}{K} + 2T_{DQL} + \frac{T_{SU}}{K} - \frac{T_{SKEW}}{K} = N_l \tau_g$ for latch based designs. Therefore, the power

consumption of the flip-flop based and latch based designs can be rewritten as

$$P_{dynamic-f} = \frac{\alpha_f C_f V_{dd}^2}{N_f \tau_g}. \quad (9)$$

$$P_{dynamic-l} = \frac{\alpha_l C_l V_{dd}^2}{N_l \tau_g}. \quad (10)$$

The equivalent gate delay is

$$\tau_g = \frac{kC_g V_{dd}}{(V_{gs} - V_{th})^a}, \quad (11)$$

where k and a are technology parameters. C_g is the total gate capacitance of a CMOS logic gate. For CMOS logic, $V_{gs} = V_{dd}$. For a latch based design to attain the same frequency as flip-flop based design, the scaled voltage (V_{ddl}) can be expressed in terms of the supply voltage of flip-flop based design (V_{ddf}) as

$$N_l \tau_{g-Vddl} = N_f \tau_{g-Vddf}. \quad (12)$$

$$N_l \frac{V_{ddl}}{(V_{ddl} - V_{th})^a} = N_f \frac{V_{ddf}}{(V_{ddf} - V_{th})^a}. \quad (13)$$

It can be estimated from (13) how much voltage can be scaled for the latch based design. The power consumption ratio between the latch based and flip-flop based designs for the same operating frequency at different supply voltages is

$$\frac{P_{dynamic-l}}{P_{dynamic-f}} = \frac{\alpha_l C_l V_{ddl}^2}{\alpha_f C_f V_{ddf}^2}. \quad (14)$$

The trade-off of converting a flip-flop based design to a latch based design can be conceived from (14). The factors effecting the power consumption in a latch based design are activity factor and load capacitance which change during the conversion.

III. Latch Based Design

The method to convert a flip-flop based design to a latch based design is investigated in this section. The experiments that are performed in this section are based on an industrial 28-nm FDSOI CMOS technology. The standard cell libraries with regular threshold voltage transistors are used.

A. Replacing Flip-Flops by Back-to-Back Connected Latches

Latches typically consume lower power compared to flip-flops while displaying speed advantage. This is also confirmed by the available data in the 28-nm FDSOI library that is used in this work. There are therefore chances to achieve power savings by simply replacing flip-flops with back-to-back connected latches in a digital circuit. This transformation shows power savings of 7% for an ARM Cortex-M0 as shown in Fig. 2. Cadence RTL Compiler is used for logic synthesis while Cadence Innovus Digital Implementation System is used for the backend physical design (placement and routing). A custom Python script is used to replace all the flip-flops in the design by back-to-back connected latches after the logic synthesis. In the back-to-back connected latch based design, 18 clock buffers are required in the clock tree for driving twice the number of sequential elements compared to 10 clock buffers for the flip-flop based design. The clock tree power consumption is therefore increased from 14% of the total power consumption to 33% after the conversion to back-to-back connected latch based design. The maximum frequency that can be achieved by the flip-flop based design and back-to-back connected latch based design is the same as there is no time borrowing. By re-positioning the latches, there are chances to achieve higher performance by enabling time borrowing.

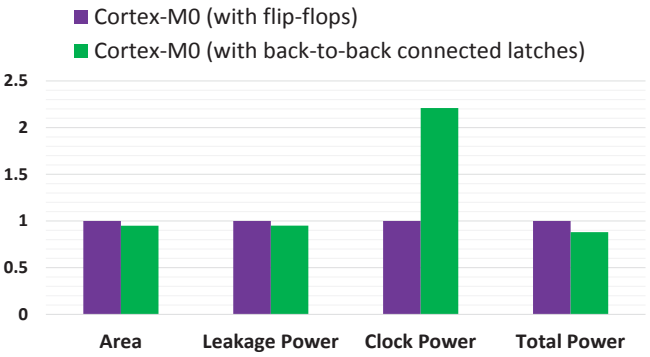

Fig. 2. Comparison between the flip-flop based design and back-to-back connected latch based design for an ARM Cortex-M0 after backend physical design. All data are normalized to the data of the flip-flop based Cortex-M0.

B. The Basic Flow for Converting a Flip-Flop Based Design to Latch Based Design

For converting a flip-flop based design to latch based design, the flip-flops need to be split into master and slave latches and then retimed by using the commercial retiming tools. The commercial tools take the advantage of time borrowing property of latches and divide the combinational logic equally between the master and slave latches. Cadence RTL Compiler is used for this purpose in this work. RTL Compiler does not support the retiming of latch based designs, but does support the retiming of flip-flop based designs. Therefore, a work-around method is used to convert a flip-flop based design to a latch based design [8]. In the work-around strategy, the design is synthesized with a clock period T. Each flip-flop is replaced by two flip-flops. Then, the whole design is retimed at twice the synthesis frequency (clock period T/2). Since replacing a flip-flop by two flip-flops, the number of pipeline stages is doubled in the design. By balancing/splitting the combinational logic in the original pipeline stages of flip-flop based design, the design with each flip-flop replaced by two flip-flops should be able to achieve twice the frequency. After retiming the circuit, the flip-flops are converted into negative and positive level-sensitive latches alternatively. After replacement with latches, the circuit is optimized for the required time period (T). Note that this process does not change the functionality of circuit. The generic design flow for the proposed method is shown in Fig. 3.

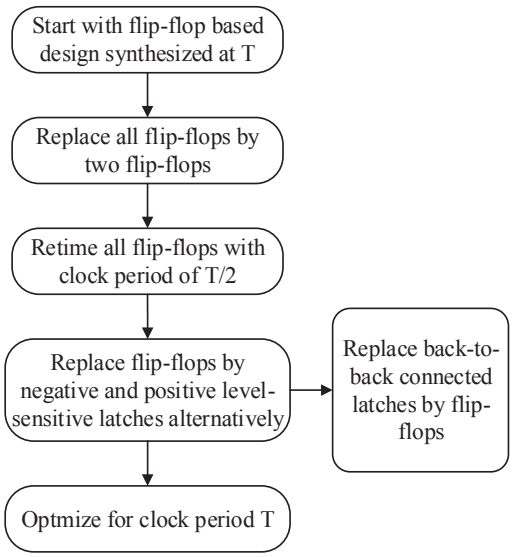

Fig. 3. The flow for converting flip-flop based design to latch based design.

C. New Retiming Strategy for Converting a Flip-Flop Based Design to Latch Based Design

While converting a flip-flop based design to a latch based design, there is a trade-off among the synthesis/retiming frequency, area, and timing slack, as illustrated in Fig. 4. When the frequency constraint is critical, the synthesis tool applies architecture change and over-sizing of gates to meet the timing (area increases) until it's impossible to meet the timing constraint. Sweeping the frequency from the point of timing slack 0 to the point when it's impossible to meet the timing is a large range. Therefore, to choose an optimum point for synthesis/retiming while converting a flip-flop based design to latch based design is an optimization problem. The optimization target in this work is for the maximum time borrowing. From (13) and (14), with more borrowed time, there could be wider supply voltage scaling for larger power savings. Note that for latch based design, the activity factor is affected by the operating frequency as well due to glitches.

After replacing all the flip-flops by two flip-flops for a design synthesized at a relaxed frequency (slack $>>0$ ns) and retiming with clock constraint T/2, the combinational logic doesn't move properly as the retiming constraint is relaxed. Alternatively, when the synthesis frequency is relatively high, retiming results in relatively balanced pipeline stages. During this process of splitting logic between flip-flops, the synthesis tool adds additional flip-flops to maintain the functionality for branching of logic. The number of latches and gates after retiming and converting the initial flip-flop based design with different synthesis frequencies to latch based design is shown in Table I. As listed in Table I, when the circuit is synthesized/retimed at higher frequency, the number of latches added to divide the logic during retiming is large.

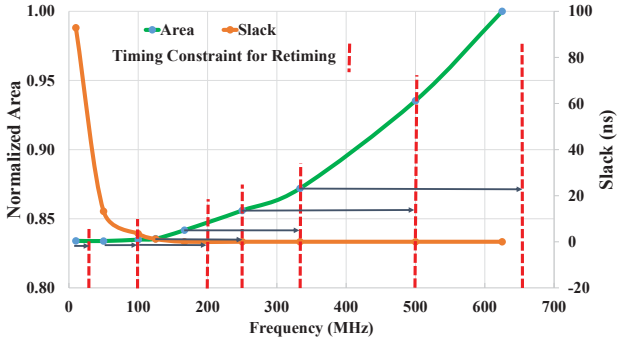

Fig. 4. Illustration of the trade-off among the synthesis/retming frequency, area, and timing slack for a latch based Cortex-M0.

TABLE I
COMPARISON OF GATE COUNT, NUMBER OF LATCHES, AND SLACK AFTER RETIMING AT DIFFERENT FREQUENCIES

Cortex-M0	Synthesis/ Retiming (R) Frequency	Gate Count	Flip-flop / latch number	Slack / Frequency
FF design	100 MHz	7147	841	3.5 ns / 153 MHz
LB design	R=200 MHz	7327	1732	4.4 ns / 178 MHz
FF design	125 MHz	7166	841	1.2 ns / 147 MHz
LB design	R=250 MHz	7422	1847	3.2 ns / 208 MHz
FF design	166.7 MHz	7284	841	0 ns / 166.7 MHz
LB design	R=333 MHz	7661	1986	1.1 ns / 204 MHz
FF design	250 MHz	7455	841	0 ns / 250 MHz
LB design	R=500 MHz	7819	2062	0 ns / 250 MHz
FF design	333 MHz	7594	841	0 ns / 333 MHz
LB design	R=666 MHz	8212	2220	0.2 ns / 357 MHz
FF design	500 MHz	8117	841	0 ns / 500 MHz
LB design	R=1 GHz	8634	2202	0 ns / 500 MHz

The optimum operating condition for latch based design which provides the maximum power savings could also be identified in Table I. The circuit that is synthesized at 125 MHz has the maximum time borrowing capability, improving the performance by 41%, as compared to the flip-flop based design. The results in Table I are based on the simulation after logic synthesis. The comparison of power consumption is to be done after physical design, which will be shown in Section IV.

From the logic synthesis results in Table I, synthesizing and retiming the flip-flop based design to convert to latch based design at relatively high frequencies or relaxed frequencies lead to no performance improvement. There is an optimum frequency where the maximum performance enhancement or the largest power savings can be achieved for the latch based design compared to the flip-flop based design. As illustrated in Fig. 4, the optimum point is close to the point where the slope of area versus frequency plot is 1. By performing a few experiments, a small range that covers the optimum point can be identified. Afterwards, a sweep of the frequency within this small range can be performed to capture the optimum frequency that provides the largest timing borrowing, and hence the highest power

savings compared to the flip-flop based design.

While retiming the design where one flip-flop is replaced by two flip-flops, the division of logic depends on the number of gates between two stages. If there are limited logic gates in one stage, then the retiming does not work and eventually the latches remain back-to-back connected. We convert the back-to-back connected latches back to flip-flops. This results in a mixed design where latches are on the timing critical paths while flip-flops are on the non-critical paths. The number of latches and flip-flops in the mixed design (with Cortex-M0 as the test circuit) after the physical design is listed in Table II. While converting the latch based design synthesized at 100 MHz (achieved by retiming at 200 MHz) to a mixed design with flip-flops and latches, the mixed design has 819 flip-flops and 80 latches. This shows that retiming at relaxed frequencies doesn't divide the logic among the latches efficiently, and hence the design has very limited performance enhancement as compared to the design synthesized at 100 MHz. For the design synthesized at 500 MHz and converted to latch based design by retiming at 1 GHz, the latch based design has 2202 latches which is 2.6X of the flip-flops in the flip-flop based design. Alternatively, the mixed design that is synthesized at 500 MHz has 164 flip-flops and 1854 latches. This shows that the design is pushed for more duplicate paths and hence more latches are used due to the tight timing constraints. The latch based design synthesized at 125 MHz and converted to a mixed design has balanced result, showing 613 flip-flops and 618 latches. In this mixed design, indeed the latches are on the critical paths and flip-flops are on the relaxed paths.

The choice between latch based and mixed based designs is design dependent. In latch based designs, clock gating is not trivial. If the designer intends to take advantage of clock gating, the mixed design strategy is preferred. Furthermore, note that the efficiency of the retiming strategy is the highest at an optimum operating frequency point. If the operating frequency is too high or too low, then the advantage of the mixed latch based design diminishes.

IV. Evaluation of Latch Based Design

The purely latch based design and the mixed design with both latches and flip-flops are evaluated and compared with the flip-flop based design in this section. The experimental results are based on the industrial 28-nm FDSOI CMOS technology. The worst-case corner is considered while evaluating the performance and power consumption of different designs. The ARM Cortex-M0 is used as the test circuit. The comparison of the latch based design, the mixed design, and the flip-flop based design is shown in Table II. Note that the switching power consumption in Table II is the power consumed by the interconnects and the primary ports of the standard cells while the internal power consumption is the power consumed by the internal part of the standard cells. As listed in Table II, the latch based design converted from the flip-flop based design synthesized at 125 MHz and retimed at 250 MHz has 48% improvement in frequency compared to the flip-flop based design. The improvement in frequency can be used to scale the supply voltage for power savings. The supply voltage of the latch based design is scaled to 0.80 V to achieve the same frequency (145 MHz) as the flip-flop based design at 0.90 V. With supply voltage scaling, 21% power savings are achieved by the latch based design as compared to the flip-flop based design for the same performance. Furthermore, as listed in Table III, the supply voltage scaling leads to 47% leakage power reduction with the latch based design compared to the flip-flop based design. It is interesting to note that the switching power consumption for the latch based design is higher than the flip-flop based design even after scaling the supply voltage. The latch based design has higher switching power consumption because of more instances, nets, glitch propagation, and complex clock tree network as listed in Table II. The number of clock tree buffers in the latch based design clock tree is 21, whereas the flip-flop based design has 10 clock tree buffers. In the latch based design, it is observed that when the design is operated at 145 MHz and 0.80 V, because of time borrowing the glitches from one stage can propagate to the next stage. The glitch propagation from one stage to another stage results in more switching of the latches as well as the combinational logic. Flip-flops act as the filter of glitches [14]. To reduce the number of instances, nets, and glitches, the back-to-back connected latches are converted back to flip-flops. As listed in Table II, the latch/flip-flop-mixed design synthesized at 125 MHz and retimed at 250 MHz has 45% improvement in frequency compared to the flip-flop based design. The latch/flip-flop-mixed design also achieves 16% power savings after scaling the supply voltage to 0.80 V as compared to the flip-flop based design at 0.90 V, as listed in Table III. Although the power savings for the mixed-design is lower as compared to the latch based design, the mixed design serves as an important trade-off between the purely flip-flop based design and the purely latch based design. With the mixed design where flip-flops also exist, other lower techniques such as clock gating can be easily applied to the flip-flops. Alternatively, clock gating for latches is not trivial. Note that for fair comparison, no clock gating is applied for any of the designs that are evaluated in this paper. Furthermore, whether clock gating is feasible or not and the effect of clock gating is heavily application dependent.

V. Conclusion

In this paper, the insight in terms of timing and power consumption for converting a flip-flop based design to a latch based design is revealed. Flows of converting a flip-flop based design to a latch based design as well as a latch/flip-flop-mixed design are proposed. Based on a smart retiming strategy, the optimum operating condition for the latch based as well as the mixed design is identified for achieving the maximum time borrowing and the highest power savings. By trading the performance enhancement with supply voltage scaling, 21% and 16% power savings are achieved by the latch based design and the mixed design, respectively, as compared to the flip-flop based design in a 28-nm FDSOI CMOS technology.

TABLE II

COMPARISON OF GATE COUNT, NUMBER OF FLIP-FLOPS/LATCHES, AND SLACK AFTER RETIMING AT DIFFERENT FREQUENCIES FOR CORTEX-M0 AFTER BACKEND PHYSICAL DESIGN. SIGN-OFF CONDITION: CORNER=SLOW, V_{DD}=0.90 V, T=-40°C

Cortex-M0	Synthesis/ Retime (R) Frequency	Gate Count	Number of flip-flop/ latch	Slack (ns)/ Max Frequency(MHz)	Area (μm^2)	Leakage Power (nW)	Internal Power (μW)	Switching Power (μW)	Total Power (μW)	Clock Power (μW/%)
FF design	100 MHz	7275	841 / -	3.4 ns / 151 MHz	8209	67	384	257	641	103 / 16%
LB design	R=200 MHz	7504	- / 1732	4 ns / 166 MHz	7903	69	243	374	618	241 / 39%
Mixed	100 MHz	6833	819 / 80	4 ns / 166 MHz	8355	74	401	276	677	115 / 17%
FF design	125 MHz	7308	841 / -	1.3 ns / 149 MHz	8210	66	474	322	796	128 / 16%
LB design	R=250 MHz	7576	- / 1847	3.5 ns / 222 MHz	8020	70	315	482	798	319 / 40%
Mixed	125 MHz	7135	613 / 618	3.4 ns / 217 MHz	8425	76	462	392	855	194 / 23%
FF design	166.7 MHz	7418	841 / -	0.3 ns / 175 MHz	8266	68	627	416	1044	172 / 16%
LB design	R=333 MHz	7777	- / 1986	1.4 ns / 217 MHz	8148	74	449	672	1122	477 / 42%
Mixed	166.7 MHz	7625	178 / 1578	1.4 ns / 217 MHz	8158	73	474	629	1104	405 / 36%
FF design	250 MHz	7615	841 / -	0.2 ns / 263 MHz	8400	69	983	669	1653	267 / 16%
LB design	R=500 MHz	7944	- / 2062	0.1 ns / 256 MHz	8287	76	645	1020	1665	693 / 41%
Mixed	250 MHz	7909	193 / 1661	0.1 ns / 256 MHz	8457	77	769	960	1730	658 / 38%
FF design	333 MHz	7740	841 / -	0 ns / 333 MHz	8465	72	1300	855	2155	350 / 16%
LB design	R=666 MHz	8308	- / 2220	0.1 ns / 345 MHz	8592	79	974	1459	2433	1067 / 44%
Mixed	333 MHz	8152	149 / 1880	0 ns / 333 MHz	8661	78	1057	1370	2427	969 / 40%
FF design	500 MHz	8303	841 / -	0 ns / 500 MHz	8831	82	1939	1353	3293	522 / 16%
LB design	R=1GHz	8776	- / 2202	0 ns / 500 MHz	8812	84	1464	2274	3691	1536 / 42%
Mixed	500 MHz	8658	164 / 1854	0 ns / 500 MHz	8929	88	1576	2094	3671	1416 / 38%

TABLE III

COMPARISON OF POWER CONSUMPTION BY SCALING VOLTAGE FOR CORTEX-M0 AFTER BACKEND PHYSICAL DESIGN. CORNER=SLOW, T=-40°C

Cortex-M0	Slack / Max Frequency at 0.90 V	Voltage	Simulation Frequency	Leakage Power (nW)	Internal Power (μW)	Switching Power (μW)	Total Power (μW)
FF design	1.3 ns / 149 MHz	0.90 V	145 MHz	66	550	373	923
LB design	3.5 ns / 222 MHz	0.80 V	145 MHz	35	289	438	727
Mixed	3.4 ns / 217 MHz	0.80 V	145 MHz	37	420	352	772

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