Lecture 1b: DFM For Dummies

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Faster, smaller & smarter

Figure 1: iPhoneX

Silicon Gold Rush?

Current Transistor

- High-K dielectrics, Metal Gate (HKMG)
- “3D” gate

Lithography

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Figure 2: SMIC

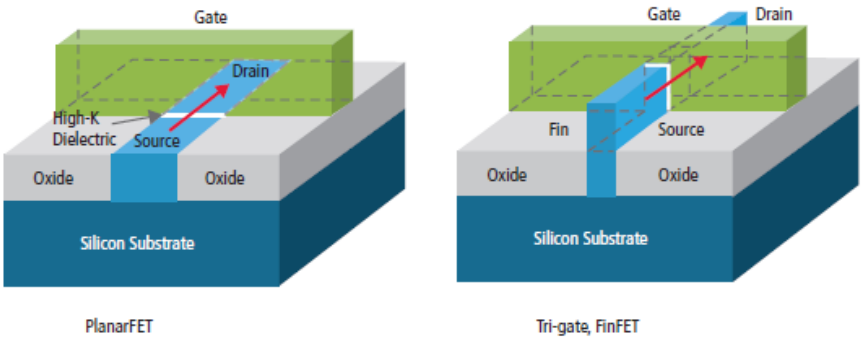

Figure 3: FinFET

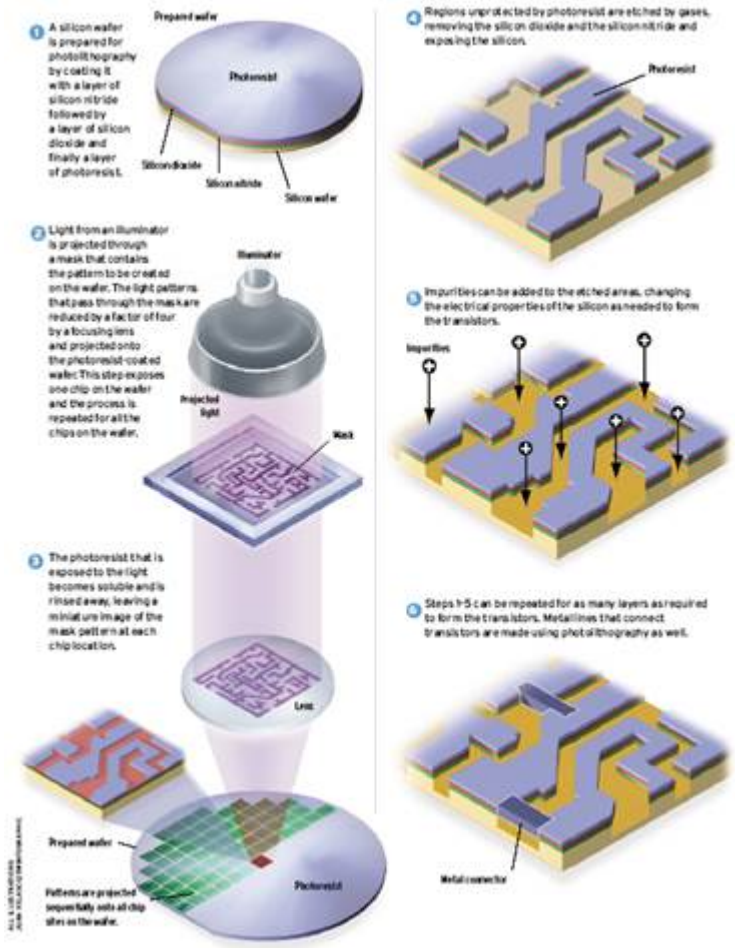

Figure 4: Lithography

- Photo-resist coating
- Illumination
- Exposure
- Etching
- Impurities Doping
- Metal connection

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Process-Design Gap

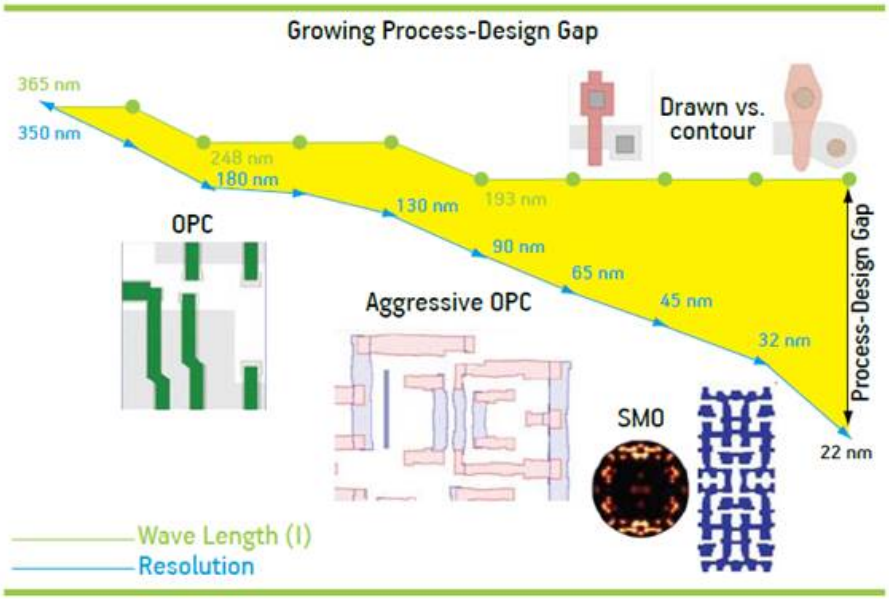

Figure 5: Process-Design Gap

Problem Visualization

Chemical Mechanical Polishing

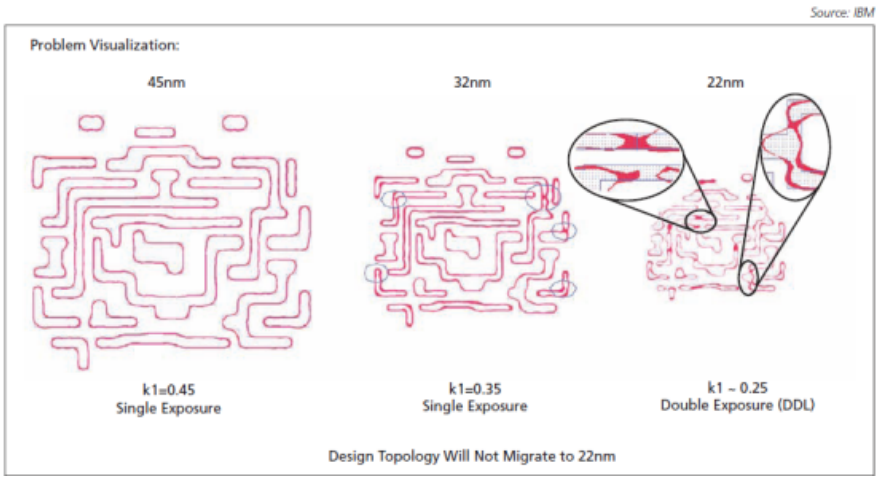

Figure 6: ibm

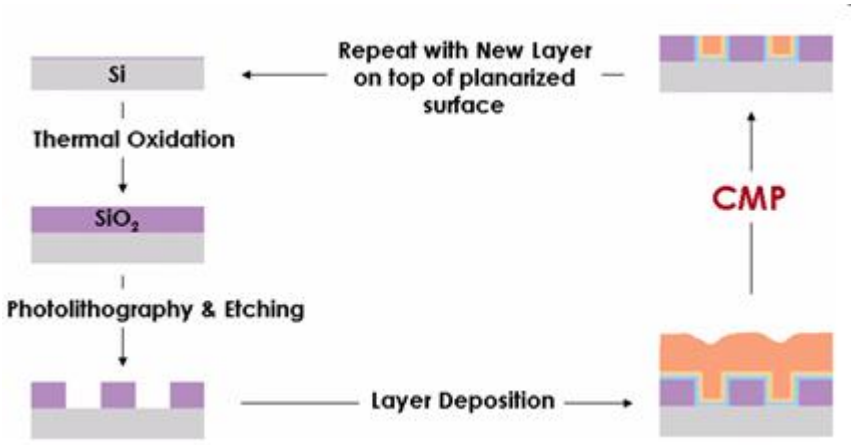

Figure 7: CMP

ECP & CMP

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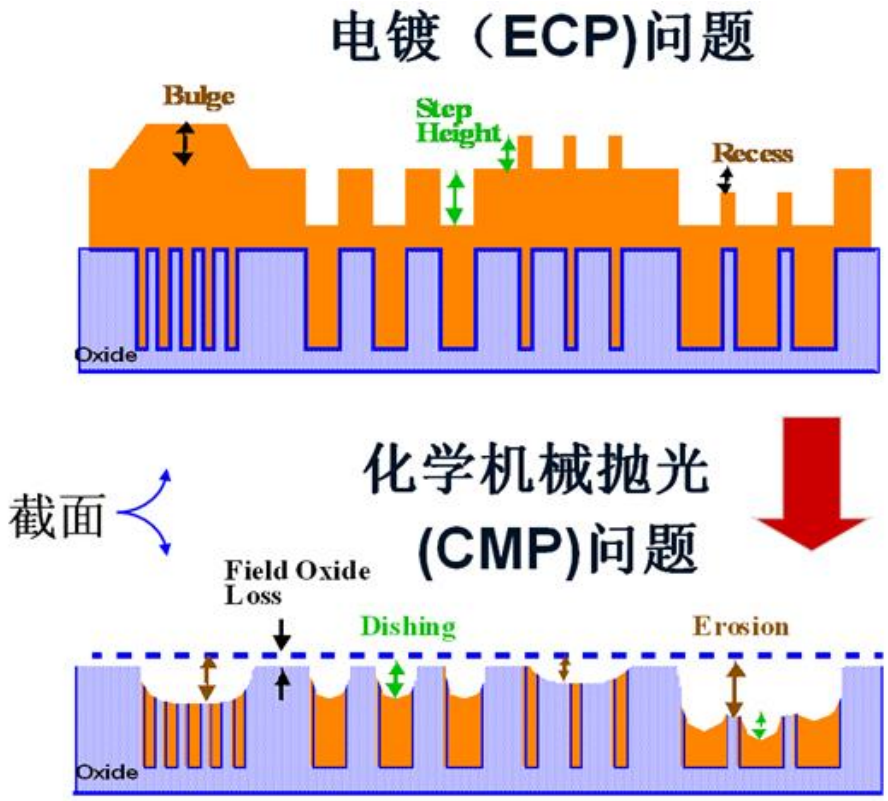

Figure 8: ECP

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Process Variation

Total Thickness Variation Per Node

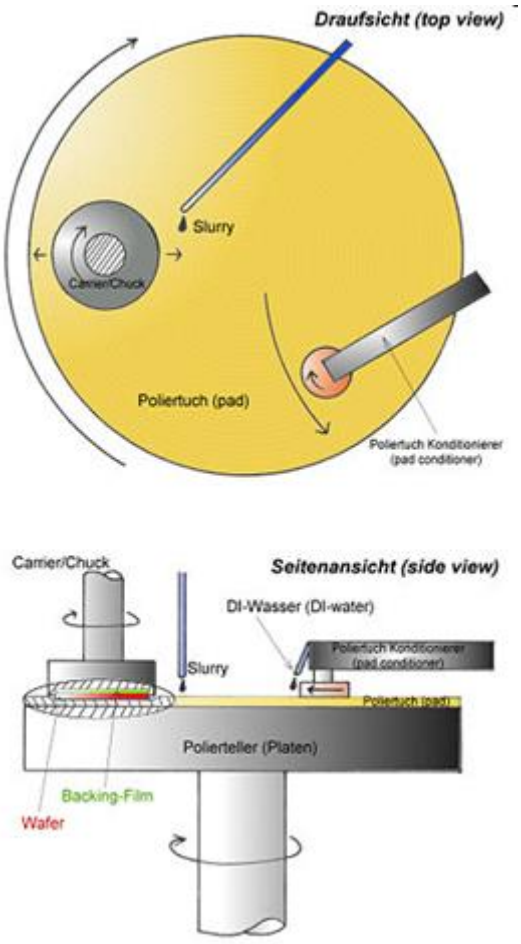
Draufsicht (top view)
Slurry
Carrier/Chuck
Poliertuch (pad)
Poliertuch Konditionierer
(pad conditioner)
Carrier/Chuck
Seitenansicht (side view)
DI-Wasser (DI-water)
Slurry
Poliertuch Konditionierer
(pad conditioner)
Poliertuch (pad)
Polierteller (Platen)
Backing-Film
Wafer

Figure 9: CMP

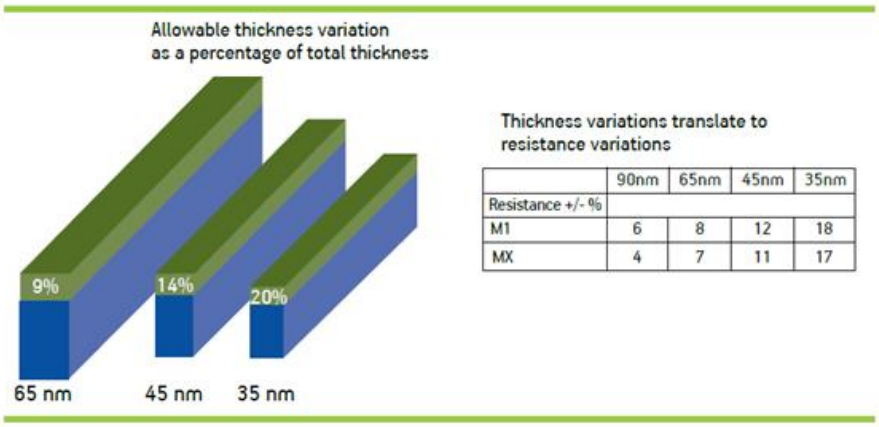

Figure 10: Thickness Variation

"Slippery Fish" at 45nm

- Process variation, impacting yield and performance
- More restricted design rules (RDRs)
  - +3 or more rules at 45nm
  - +100 or more rules at 32nm
  - +250 or more rules at 22nm
- More rules implies larger die size, lower performance
- 10nm is not sci-fiction due to FinFET technology

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DFM

What is DFM?

- Design for money?
- Design for Manufacturing
- Design for Manufacturability
  - Refer to a group of challenges less than 130nm
  - The engineering practice of designing integrated circuits (ICs) to optimize their manufacturing ease and production cost given performance, power and reliability requirements
  - A set of techniques to modify the design of ICs to improve their functional yield, parametric yield or their reliability

Why is it important?

- Achieving high-yielding designs in the state-of-the-art VLSI technology is extremely challenging due to the miniaturization and complexity of leading-edge products
- The manufacturing process becomes more sensitive to variations and defects, which can degrade the quality and functionality of the chips
- DFM can help to address various manufacturing issues, such as lithography hotspots, CMP dishing and erosion, antenna effects, electromigration, stress effects, layout-dependent effects and more

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How is it applied?

- DFM can be applied to various aspects of IC design, such as circuit design, logic design, layout design, verification and testing
- Each aspect has its own specific DFM guidelines and best practices that designers should follow to ensure manufacturability
- For example, some general DFM guidelines for layout design are:
  - Use regular and uniform layout structures
  - Avoid narrow or long metal wires
  - Avoid acute angles or jogs in wires
  - Avoid isolated or floating features
  - Use dummy fill to improve planarity and density uniformity
  - Use recommended design rules and constraints from foundries

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What are the benefits?

- By applying DFM techniques in the physical design stage of IC development, designers can:
  - Reduce the number of design iterations
  - Improve the collaboration with foundries
  - Enhance the product performance and functionality
  - Achieve faster time to market and lower production costs

DFM Market Share 2008

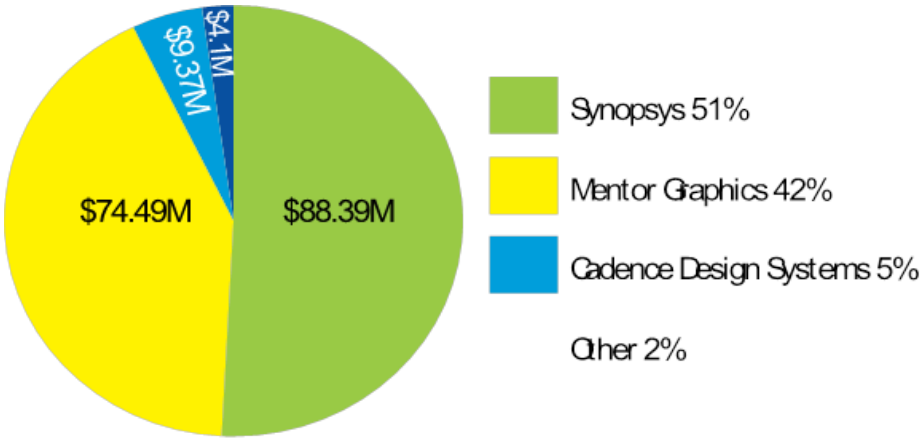
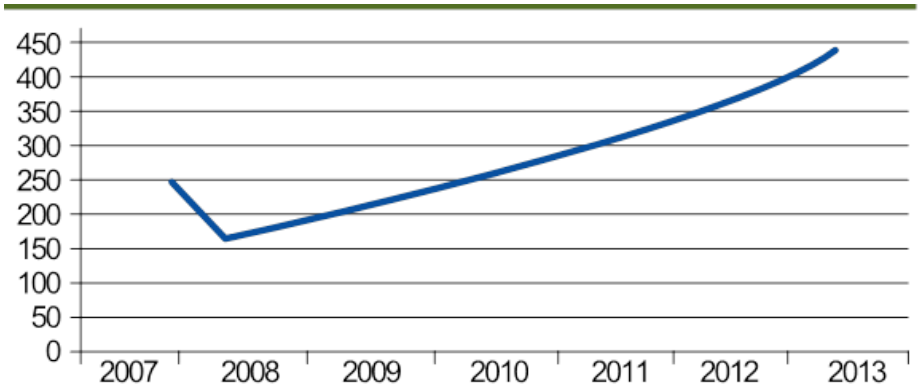


Figure 11: Market Share



	2007	2008	2009	2010	2011	2012	2013
RET	$208	$131	$144	$158	$174	$192	$211
DFY	$37	$46	$62	$84	$115	$156	$212
Total DRM	$246	$176	$206	$243	$289	$347	$423

Figure 12: forecast

DFM Forecast 2009 in $M

Increasing Importance of DFM

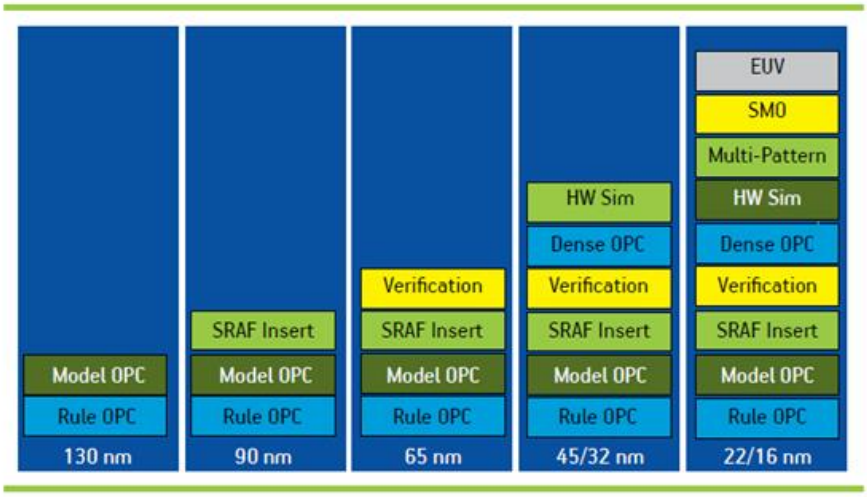


Figure 13: trend

DFM Analysis and Verification

- Critical area analysis
- CMP modeling
- Statistical timing analysis
- Pattern matching
- Lithography simulation
- Lithographic hotspot verification

2D Pattern Matching in DRC+

Contour Based Extraction

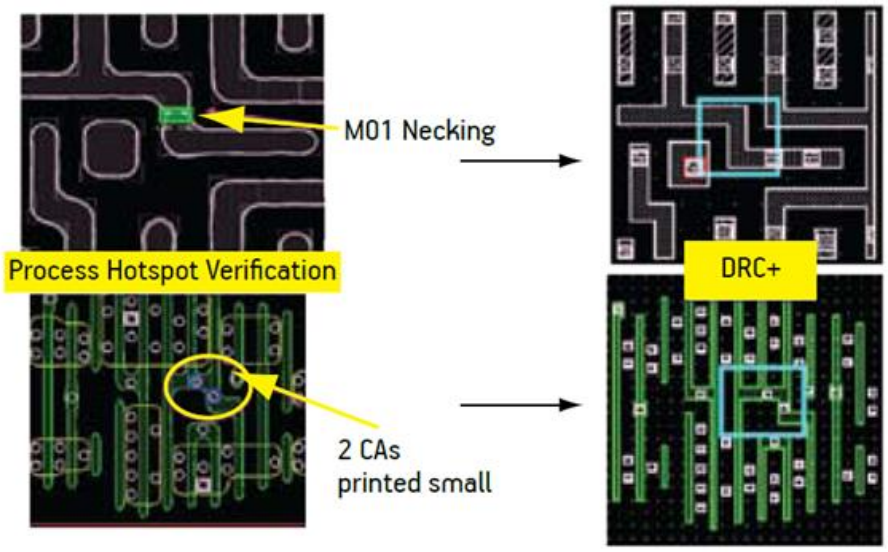


Figure 14: DRC+

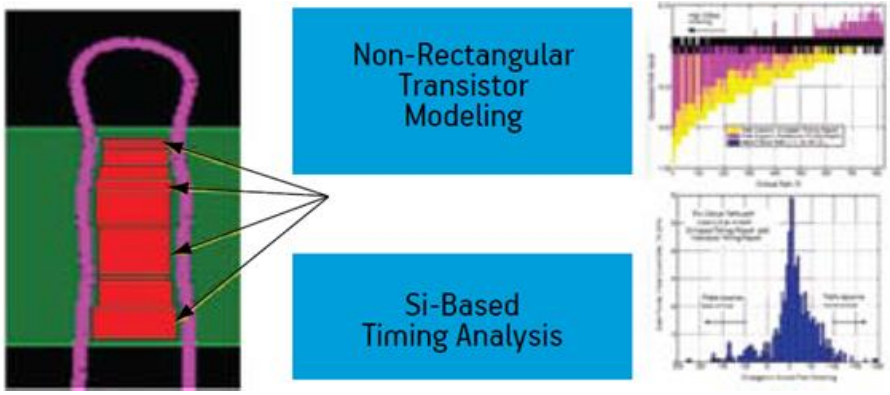


Figure 15: contour

DFM Enhancement and Optimization

- Wire spreading
- Dummy Filling
- Redundant Via Insertion
- Optical proximity correlation (OPC)
- Phase Shift Masking (PSM)
- Double/Triple/Multiple Patterning
- Statistical timing and power optimization

Dummy Filling

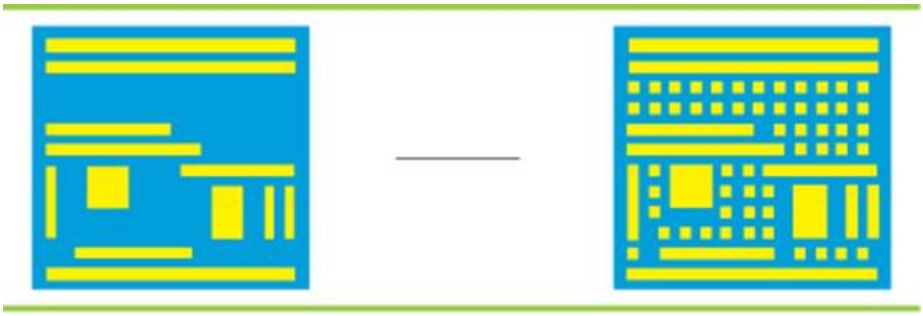


Figure 16: filling

"Smart" Filling

Redundant Via Insertion

- Also known as double via insertion.
- Post-routing RVI (many EDA tools already have this feature)
- Considering RVI during routing

Looks good, right?

But actually only few people are using this!

Why?

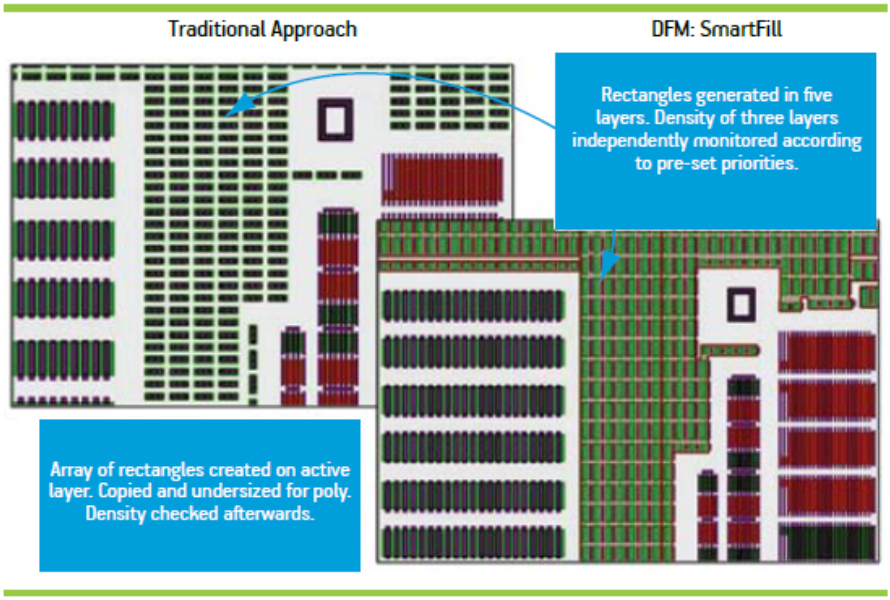


Figure 17: "Smart" Filling

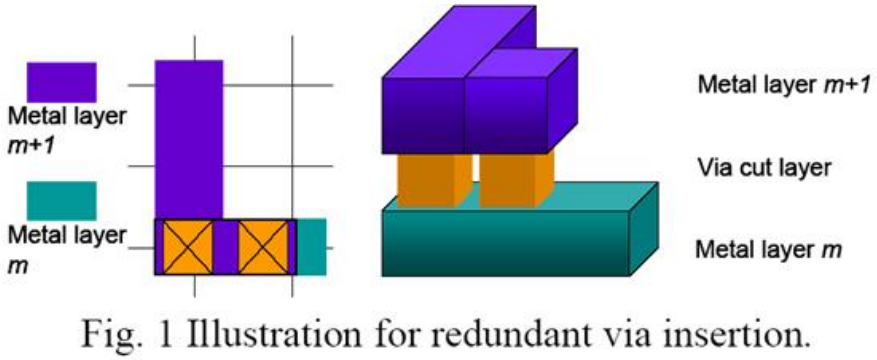
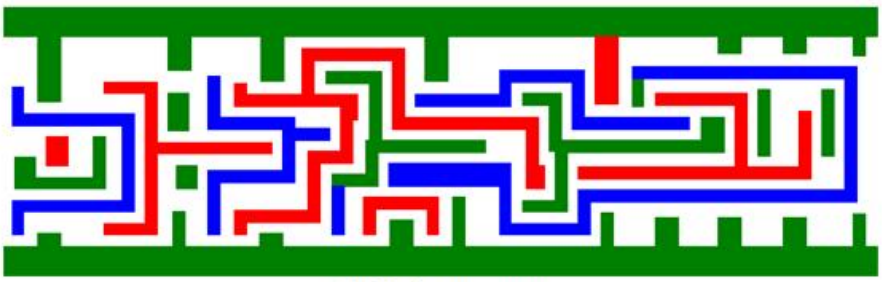


Fig. 1 Illustration for redundant via insertion.

Figure 18: RVI

Multiple Patterning (MPL)

- Instead of exposing the photoresist layer once under one mask, MPL exposes it twice by splitting the mask into "k" parts, each with features less dense.



(b) Triple patterning

Figure 19: MPL

What are the challenges of DFM?

- DFM is not a fixed set of rules, but rather a flexible and evolving methodology that depends on the product requirements, the manufacturing technology and the industry standards
- DFM can also be combined with other design methodologies, such as DFT, DFR, DFLP and DFS, to create a holistic approach to product development
- DFM requires strong capabilities in research, supply chain, talent, IP protection and government policies

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Course Structure

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- Describe the DFM problems that arise from.
- Abstract the problems in mathematical forms
- Describe the algorithms that solve the problems
- Discuss the alternative algorithms and possible improvement.
- Discuss if the algorithms can be applied to other area.
- Only describe the key idea in lectures. Details are left for paper reading if necessary.

Not covered

- Algorithms for 3D problems
- Packaging
- Machine Learning/AI Based algorithm