BUS COMMUNICATION — CHAPTER 2

This section describes the HP-71 system bus structure, protocol, and timing. Also included is a description of the bus commands, device addressing, and the power down and wake up characteristics.

2.1 Bus Structure

The HP-71 bus consists of 8 lines including:

- 4 BUS[0:3] - data lines, driven by the CPU or system devices.
- 1 *STROBE (*STR) - driven by the CPU.
- 1 *COMMAND-DATA (*CD) - usually driven by the CPU.
- 1 VDD
- 1 GROUND

Plug-ins may have two additional lines:

- 1 DAISYIN - (DIN) input to device
- 1 DAISYOUT - (DOUT) output from device, may be tied to next device's DIN

NOTE : A '*' before a signal name denotes negative true logic.

2.1.1 General Protocol

*STR is driven by the CPU and serves to synchronize all bus transfers. It is not a true system clock since it can remain inactive for several cycles while the CPU is performing internal manipulations. All address, data, and bus commands are transferred on the BUS[0:3]. The BUS[0:3] is driven during *STR low by either the CPU or the device the CPU is accessing. This data is latched either by the CPU during *STR low or by the receiving device on the rising edge of *STR.

All bus operations are initiated by the CPU. The CPU starts a specific transfer on the bus by driving the *CD line low before *STR goes low. While *CD and *STR are low the CPU drives a bus command on the BUS[0:3] and all devices in the system latch the command on the rising edge of *STR. This strobe is referred to as

a command strobe. The bus command issued during a command strobe specifies the operation that is to be performed on each succeeding *STR until another bus command is issued. At all times when data or address is being transferred *CD is held high. A strobe issued while *CD is high is referred to as a a data strobe.

2.1.2 Bus Commands

The bus commands are:

0	NOP	All devices ignore *STR until a new command is loaded.
1	ID	The unconfigured device that has its DAISY-IN high sends its 5-nibble ID on the following data strobes, starting with the low- order nibble of the ID.
2	PC READ	(PC)->BUS or read using the Program Counter (PC). The device addressed by its program counter sends data pointed to by its local program counter on each following data strobe and all devices increment their local program counters once each data strobe. A dummy strobe immediately follows the issuance of this bus command (see subsection 2.1.4).
3	DP READ	(DP)->BUS or read using the Data Pointer (DP). The device addressed by its data pointer sends data pointed to by its local data pointer on each following data strobe and all devices increment their local data pointers once each data strobe. A dummy strobe immediately follows the issuance of this bus command (see subsection 2.1.4).
4	PC WRITE	BUS->(PC) or write using PC. The device addressed by its program counter loads the data on the following data strobes into the location pointed to by its local program counter and all devices increment their local program counter once each data strobe.
5	DP WRITE	BUS->(DP) or write using DP. The device addressed by its data pointer loads the data on the following data strobes into the location pointed to by its local data pointer and all devices increment their local data pointer once each data strobe.

6	LOAD PC	BUS->PC or load PC. All devices load the data on following 5 data strobes into their local program counter, starting with the low-order nibble. After all 5 nibbles are transferred the command code is automatically changed to a 2, PC READ (see subsection 2.1.3).
7	LOAD DP	BUS->DP or load DP. All devices load the data on following 5 data strobes into their local data pointer, starting with the low-order nibble. After all 5 nibbles are transferred the command code is automatically changed to a 3, DP READ (see subsection 2.1.3).
8	CONFIGURE	The unconfigured device that has its DAISY-IN high loads the following 5 data nibbles into its configuration register starting with the low-order nibble.
9	UNCONFIGURE	The device currently addressed by its data pointer unconfigures itself. The device then responds to CONFIGURE and ID bus commands only. The local data pointers must be loaded immediately preceding an unconfigure command.
A	POLL	All chips that require service pull one data line high during the next *STR low (see section 2.5).
B	Reserved	
C	BUSCC	The device currently addressed by its local data pointer performs a specific operation as defined by the individual device.
D	Reserved	
E	SHUTDOWN	When the CPU has received a SHUTDN instruction it issues this command and turns off its oscillator. Each device responds based on its own special requirements to this command (see section 2.4).
F	RESET	All devices reset their configuration flags (if applicable) and perform other local resets based on their own special requirements.

2.1.3 Command Auto-Switch

There exists one special case in which all devices change their current bus command. This is called 'auto-switch' and occurs following the load of either the PC or the DP. On the rising edge of *STR after the 5th nibble of address has been loaded all devices clear bit 2 of their command latch changing the bus command from either a LOAD PC to PC READ or LOAD DP to DP READ.

2.1.4 Dummy Strobe

Immediately following a PC READ bus command, a DP READ bus command, and a command auto-switch the CPU issues a 'dummy strobe'. This dummy strobe appears as a data strobe except that no data is transferred during this period and devices do not increment their local address registers. The dummy strobe provides memory devices a full strobe cycle for the first access and therefore allows data pipelining.

2.2 Addressing

Each device on the HP-71 bus has two 20-bit address registers; a local program counter (PC) and a local data pointer (DP). Each device is also either hard addressed at a specific address (hard configured) or capable of being dynamically located within the address space (soft configured). A device only responds to data reads and writes if its local address register (PC or DP depending on the read or write command) is within its configured address space.

The HP-71 operating system allows soft configured devices to have address spaces ranging in size from 8 bytes to 128K bytes. All devices are configured such that the upper-order bits of the local address register can be compared with the upper-order bits of the device's configuration register (hard or soft). If these bits are identical, the device has an address match and will respond to read and write commands (and the unconfigure and BUSCC commands if applicable). Each device with a given address space size compares a given number of the upper-order bits of address. For example, a device with an address space size of 1K bytes or 2K nibbles requires 11 bits of address leaving the upper 9 bits for its configuration register.

2.2.1 Soft Configuration

A soft configured device powers up unconfigured. When unconfigured a device responds only to the ID and CONFIGURE commands and drives its DAISYOUT low. A device's ID code is used to identify the device before it is configured. If a soft configured device is unconfigured and has its DAISYIN line high, it sources its 5-nibble ID code starting with the low-order nibble on the 5 data strobes immediately following the issuance of an ID command (no dummy strobe is issued).

The 5-nibble ID code contains information on the device type and the address space required by the device as defined below:

NIBBLE 0 : Determines the size of the address space and is interpreted differently for memory and memory mapped I/O.

Nib 0	Memory Size	MM I/O space
F	1K nibble	16 nibbles
E	2	32
D	4	64
C	8	128
B	16	256
A	32	512
9	64 (max RAM)	1K
8	128	2K
7	256 (max)	4K
6	-	8K
7	-	16K (max)

NIBBLE 1 : Reserved for future use.

NIBBLE 2 : Device type--

0 : RAM
1 : ROM
2-E : Assorted memory types
F : Memory-mapped I/O

NIBBLE 3 : Device class--

Memory : unassigned

Memory-mapped I/O - 0 : HP-IL mailbox
1-F : unassigned

NIBBLE 4 : bits 0-1 : unassigned
bit 2 : Last chip in sequence.
Always assumed high for MM I/O.
bit 3 : Last chip in module.

Since the BUS[0:3] is precharged low before each strobe, the CPU will read an ID of all zeros if all devices are configured (or are unconfigured but have DAISYIN low). For more information on how the operating system handles configuration see the HP-71 Software IDS Volume 1.

A soft configured device is assigned its address configuration by the CONFIGURE command. If an unconfigured device has its

DAISYIN line high, it loads the configuration address that is issued on the 5 data strobes immediately following the CONFIGURE command (low-order nibble first) into its configuration register. A device may actually latch only the number of high-order bits it requires as determined by its address space size.

After being configured a device no longer responds to either an ID or CONFIGURE command. A configured device drives DAISYOUT to the same logic level as DAISYIN. The DAISYOUT of one device may be tied to the DAISYIN of second device. In this way many devices may be daisy-chained together in a way that they can be configured one at a time to different addresses. After being configured a device waits until the next command strobe to set its configuration flag in order to delay DAISYOUT so that the next device on the daisy-chain will not be configured simultaneously.

A device may be unconfigured by either a RESET or UNCONFIGURE bus command. The bus RESET command unconfigures all soft configured devices in the system. A device responds to an UNCONFIGURE command by clearing its configuration flag if the DP is within its address configuration.

2.2.2 Hard Configuration

A hard configured device powers-up configured to a specific address. It will not respond to an ID, CONFIGURE, or UNCONFIGURE command and a bus RESET will not affect its configuration. If the device has a DAISYOUT, it is always driven to the same logic level as its DAISYIN.

2.3 Data Transfer

All information that is transferred from the CPU to other devices in the system (commands, addresses, and data) is latched from the BUS[0:3] on the rising edge of *STR. Data that is transferred from system devices to the CPU is latched off the BUS[0:3] after the falling edge of *STR (timed internally on the CPU).

The CPU loads all devices' local address registers by issuing a LOAD PC or LOAD DP bus command followed by 5 data strobes of address, least significant nibble first. After the last nibble of address has been loaded all devices auto-switch to a PC READ or DP READ bus command. The CPU may then read the contents of that address location by issuing one dummy strobe followed by 1 to 16 data strobes during which the CPU latches the BUS[0:3] data. The

CPU may read without first loading the local address registers by issuing a PC READ or DP READ, followed by a dummy strobe, followed by 1 to 16 data strobes. The CPU precharges the BUS[0:3] low each cycle before *STR goes low. Therefore if no device responds the CPU reads zeros.

The CPU writes the contents of a specific addressed location similarly. It is not required to load the local address registers immediately before issuing a PC WRITE or DP WRITE command. The write command is followed by 1 to 16 data strobes during which the addressed device latches the BUS[0:3] data.

All devices increment their local address registers once each data strobe during read and write operations. It is possible for a read or write operation to begin in one device and cross the address boundary into another device. Future controllers on the HP-71 bus may read and write more than 16 nibbles at a time.

Two other types of data transfers are ID, which is simply a 5-nibble read with no address load or dummy strobe, and CONFIGURE, which is a 5-nibble write with no address load. Both these data transfers require that a device be unconfigured and that the DAISYIN line be high. POLL is a unique read and is discussed in section 2.5.

2.4 Power down; Wake up

The HP-71 system can be shutdown under software control. The CPU executes a SHUTDN instruction by issuing a SHUTDOWN bus command and on the ensuing cycle stopping the system clock (*STR) and its own oscillator. While in shutdown mode all data stored in RAM and CPU resident memory is preserved. The CPU is brought out of shutdown mode by either pulling an Input Register line high, or by driving *CD low.

*CD is driven low to wake up the CPU primarily by a device in the system that needs service while the system is in shutdown mode. If a device wakes up the CPU and the CPU shuts down without satisfying its service request the device will not wake up the CPU again until its service request has been satisfied and it needs service again. This avoids a situation where the operating system does not know how to handle a device's service request and cannot shutdown. For more information on power down and wake up see section 3.5.

2.5 Service Poll

If a device needs service while the CPU is operating it must wait until the CPU executes a service request instruction (SREQ), or, if it has the capability, interrupt the CPU using IR14 (available at all ports). The SREQ instruction causes the CPU to issue a POLL bus command followed by one data strobe during which the CPU latches the BUS[0:3] data in the manner of a usual read. A device may respond to the service POLL by pulling one of the BUS[0:3] lines high. Since the CPU precharges the BUS[0:3] low every cycle before *STR goes low the data read by the CPU is a binary OR of all devices' responses.

The following HP-71 chips can wake-up the CPU and can respond to a service POLL on the BUS[0:3] line shown:

Device	Bus line	Reason for Service Request
Display Driver	BUS[0]	Timer underflow.
HP-IL chip	BUS[1]	Data Avail; Interrupt; Pwr-on Reset; Loop Service Request.
Card Reader	BUS[2]	FIFO servicing; Error condition.

ROM CHIP — CHAPTER 6

The 1LG7 ROM is designed to support the 1LF2 CPU and future processors that operated on the HP-71 bus. The ROM core consists of 128K bits of memory arranged as 32,768 four-bit nibbles.

6.1 Pin Designations

The pins of the 1LG7 ROM chip are as follows:

PIN	FUNCTION
VDD	Power Supply.
GND	System Ground.
BUS[0:3]	System bus.
*STR	*STROBE
*CD	*COMMAND-DATA
OD	OUTPUT DISABLE - when driven high, the ROM tri-states the BUS[0:3]; OD is passively pulled low on-chip by an internal resister.
DIN	Daisy chain input.
DOUT	Daisy chain output.

In the HP-71 system, the OD pins of the 4 system ROMs are tied together. This signal is available at PORT1, and with special hardware, at PORT3 and the HP-IL port. By pulling the OD line high, all 4 system ROMs are effectively removed from the bus.

6.2 Bus Commands

The 1LG7 ROM can be either hard or soft configured and has no service request capability. The ROM responds to the bus commands

described in section 2.1.2 with the following exceptions:

1	ID	If hard configured : same as NOP.
4	PC WRITE	The ROM increments its local program counter once each data strobe. No write is performed.
5	DP WRITE	The ROM increments its local data pointer once each data strobe. No write is performed.
8	CONFIGURE	If hard configured : same as NOP.
9	UNCONFIGURE	If hard configured : same as NOP.
A	POLL	Same as NOP.
C	BUSCC	Same as NOP.
E	SHUTDOWN	Same as NOP.
F	RESET	If hard configured : same as NOP.

The ROM's ID code is hard programmed (if soft configured). Generally, the ID code will be either 0010A, for one ROM of a multiple ROM set, or 8010A for an individual ROM or the last ROM of a multiple ROM set.

6.3 Addressing

The 32K nibbles of ROM require 15 bits of address space, leaving 5 bits of configuration address. The chip is selected when the upper 5 bits of the PC or DP (whichever is active) match the 5 bits stored in its configuration register and its configuration flag is set. The chip uses the remaining 15 bits to address its memory.

The ROM chip is manufactured in both soft and hard configured options (see section 2.2). In the hard configured option the 5 bits of the configuration register as well as the configuration flag are mask programmed to configure the ROM chip to a fixed address. The HP-71 operating system is stored in 4 mainframe ROMs configured as follows:

	ROM0	ROM1	ROM2	ROM3
Starting addr =	00000	08000	10000	18000
Ending addr =	07FFF	0FFFF	17FFF	1FFFF

Some plug-in ROMs are soft configured. In the soft configured option, the configuration register latchs the configuration address under software control as described in section 2.2.1.

RAM CHIP — CHAPTER 7

The 1LG8 RAM is designed to support the 1LF2 CPU and future processors that operate on the HP-71 bus. The RAM core consists of 8K bits of static memory arranged as 2048 four-bit nibbles.

7.1 Pin Designations

The pins of the 1LG8 RAM chip are identical to the pins of the 1LG7 ROM chip (see section 6.1) with the following addition:

ID	If tied high on the hybrid PC board (last chip) the most significant bit of the most significant nibble of the 5-nibble ID code will be set to a 1.

7.2 Bus Commands

The 1LG8 RAM is soft configured and has no service request capability. It responds to the bus commands as described in section 2.1.2 with the following exceptions:

A	POLL	Same as NOP.
C	BUSCC	Same as NOP.
E	SHUTDOWN	Same as NOP.

The RAM ID code is n000E, where n=0 if the ID pin is tied low and n=8 if the ID pin is tied high. The ID pin is tied high only on the last chip of the 4-chip hybrid.

7.3 Addressing

The 2K nibbles of RAM require 11 bits of address space, leaving 9 bits of configuration address. The chip is selected when the upper 9 bits of the PC or DP (whichever is active) match the 9 bits stored in its configuration register and its configuration flag is

set. The chip then uses the remaining 11 bits to address its memory. As an example of addressing, if a 4-chip RAM hybrid has been configured contiguously starting at 30000 hex, the following would apply:

		RAM0	RAM1	RAM2	RAM3
Starting addr	=	30000	30800	31000	31800
Ending addr	=	307FF	30FFF	317FF	31FFF

SYSTEM DIAGRAMS	CHAPTER 8

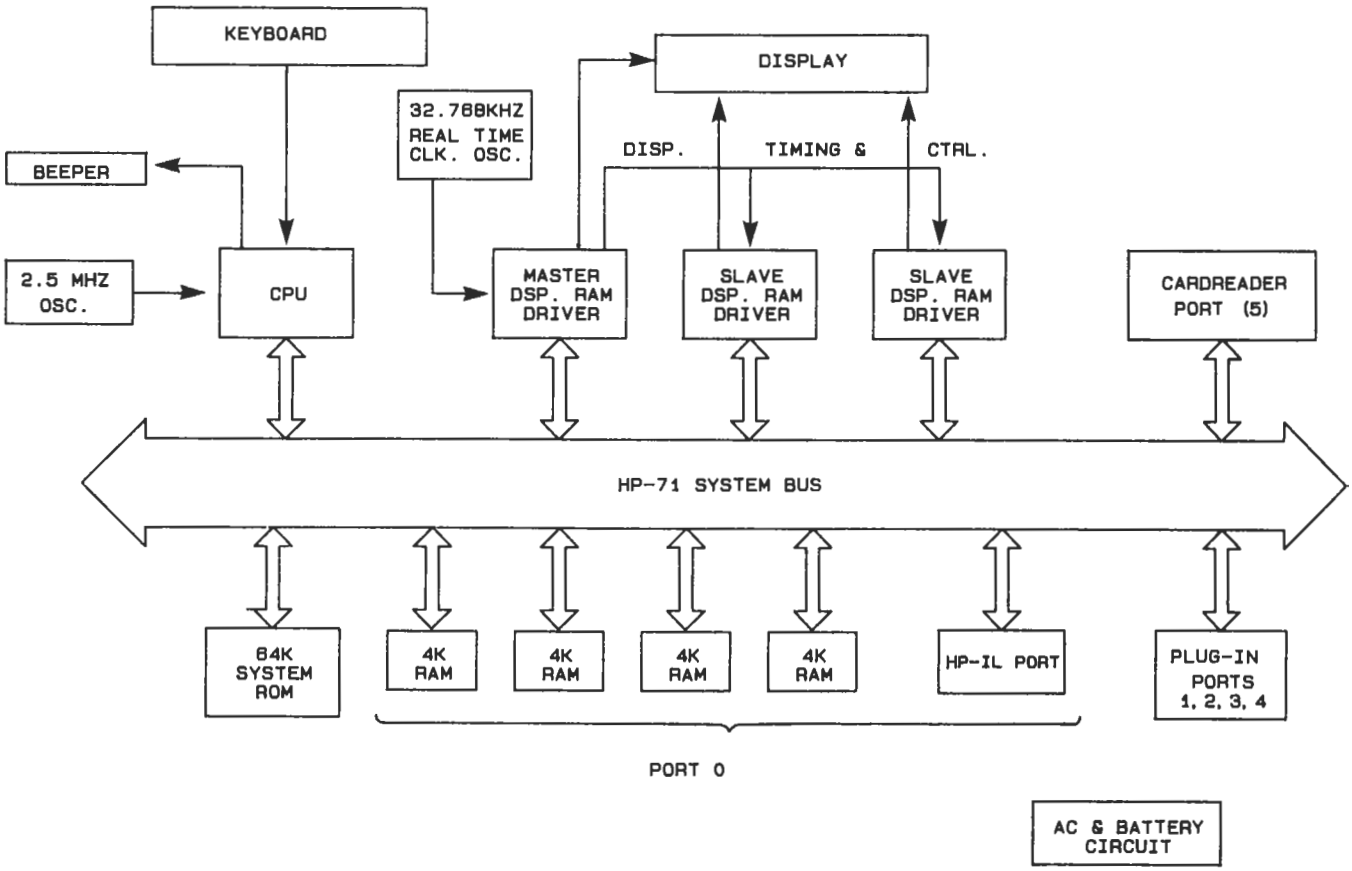

Figure 8-1. System Block Diagram

SYSTEM ELECTRICAL SPECIFICATION	CHAPTER 9

IC ABSOLUTE MAXIMUM RATINGS:

Supply Voltage Vdd	Vss + 7.5V
Maximum Voltage at any Input or Output	Vdd + 0.3V
Minimum Voltage at any Input or Output	Vss - 0.3V
Operating Free-Air Temperature	0C to +45C
Storage Temperature	-40C to +55C
Humidity	0 to 95% RH

TEST CONDITIONS: Test conditions are such that the following parameters are guaranteed for Vdd = 4.25V to 6.5V and Temperature = 0C to 45C unless a different supply voltage or temperature is noted.

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Vss	Ground	0.0	0.0	0.0	V	
Vdd	Supply voltage	4.25	-	6.5	V	
Iddop	Idd operating current	-	-	15.0	mA	Display on, CPU running, T0=1.5uS.
Iddls	Idd light sleep current	-	-	0.5	mA	Display on, CPU shutdown.
Iddds	Idd deep sleep current	-	-	50	uA	Display off CPU shutdown.

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
POWER SUPPLY						
Vac	AC adapter input voltage	9.0	-	14.0	V	See Note 1.
Vreg	AC adapter voltage at Vdd	5.6	-	6.5	VDC	
Iac	AC adapter current drain	-	-	30	mADC	Over mainframe requirements.
Vbat	Battery voltage at Vdd	4.25	-	6.0	VDC	Unregulated.
Ibat	Battery current drain	-	-	100	mADC	Over mainframe requirements.
BUS PARAMETERS						
Vih	Input logic level '1'	Vdd-.65	-	-	V	
Vil	Input logic level '0'	-	-	Vss+.65	V	
Voh	Output logic level '1'	Vdd-.5	-	-	V	
Vol	Output logic level '0'	-	-	Vss+.5	V	
Cout	Output capacitance drive capability (surplus)					
	BUS0-3	50	-	-	pF	See Notes 2 & 3.
	*CD,*STR	50	-	-	pF	See Notes 2 & 3.
	DIN	10	-	-	pF	With no pulldown, See Note 4.
	DIN	50	-	-	pF	With Rpd = 50Kohm, See Note 4.

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Ioh	High level output source current capability					
	BUS0-3	1.0	-	-	mADC	See Note 3.
	*CD,*STR	1.0	-	-	mADC	See Note 3.
	DIN	100	-	-	uADC	
Iol	Low level output sink current capability					
	BUS0-3	1.0	-	-	mADC	See Note 3.
	*CD,*STR	1.0	-	-	mADC	See Note 3.
	DIN	2	-	-	uADC	
Cin	Input capacitance loading					
	BUS0-3	-	-	300	pF	See Note 2.
	*CD,*STR	-	-	250	pF	See Note 2.
	*INT	-	-	1200	pF	
	IR14	-	-	250	pF	
	HALT	-	-	250	pF	
	OD	-	-	.012	uF	
Iih	High level input current loading					
	BUS0-3	-	-	50	uADC	Internal pulldown
	*CD	-	0.0	-	uADC	Internal pullup
	*STR	-	0.0	-	uADC	Internal pullup
	*INT	-	0.0	-	uADC	10K pullup
	IR14	-	-	50	uADC	Internal pulldown
	HALT	-	-	1.0	mADC	10K pulldown
	OD	-	-	50	uADC	Internal pulldown

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Iil	Low level input current loading					
	BUS0-3	-	0.0	-	uADC	Internal pulldown
	*CD	-	-	50	uADC	Internal pullup
	*STR	-	-	50	uADC	Internal pullup
	*INT	-	-	1.0	mADC	10K pullup
	IR14	-	0.0	-	uADC	Internal pulldown
	HALT	-	0.0	-	uADC	10K pulldown
	OD	-	0.0	-	uADC	Internal pulldown
BUS TIMING PARAMETERS						
T0	*STR cycle time	1.0	-	-	us	Current HP-71's operate at 600KHz to 650KHz, future HP-71's will run at up to 1MHz.
Tpwl	*STR low	0.5	-	-	us	
Tpwh	*STR high	0.5	-	-	us	
Tdwc	Data-in valid to *STR high	200	-	-	ns	Command cycle
Tdwd	Data-in valid to *STR high	100	-	-	ns	Write cycle
Tdh	*STR high to data-in invalid	100	-	-	ns	
Tacc	*STR low to data-out valid	-	-	200	ns	BUS precharged low
Toh	*STR high to data-out tristated	20	-	100	ns	

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Tc1	*CD low to *STR low	30	-	-	ns	
Tc2	*STR high to *CD high	50	-	-	ns	
Tc3	*CD high to *STR low	100	-	-	ns	
Tr	Rise time					
	*STR	-	-	100	nS	
	*CD	-	-	100	nS	
	BUS0-3	-	-	100	nS	
Tf	Fall time					
	*STR	-	-	100	nS	
	*CD	-	-	100	nS	
	BUS0-3	-	-	100	nS	

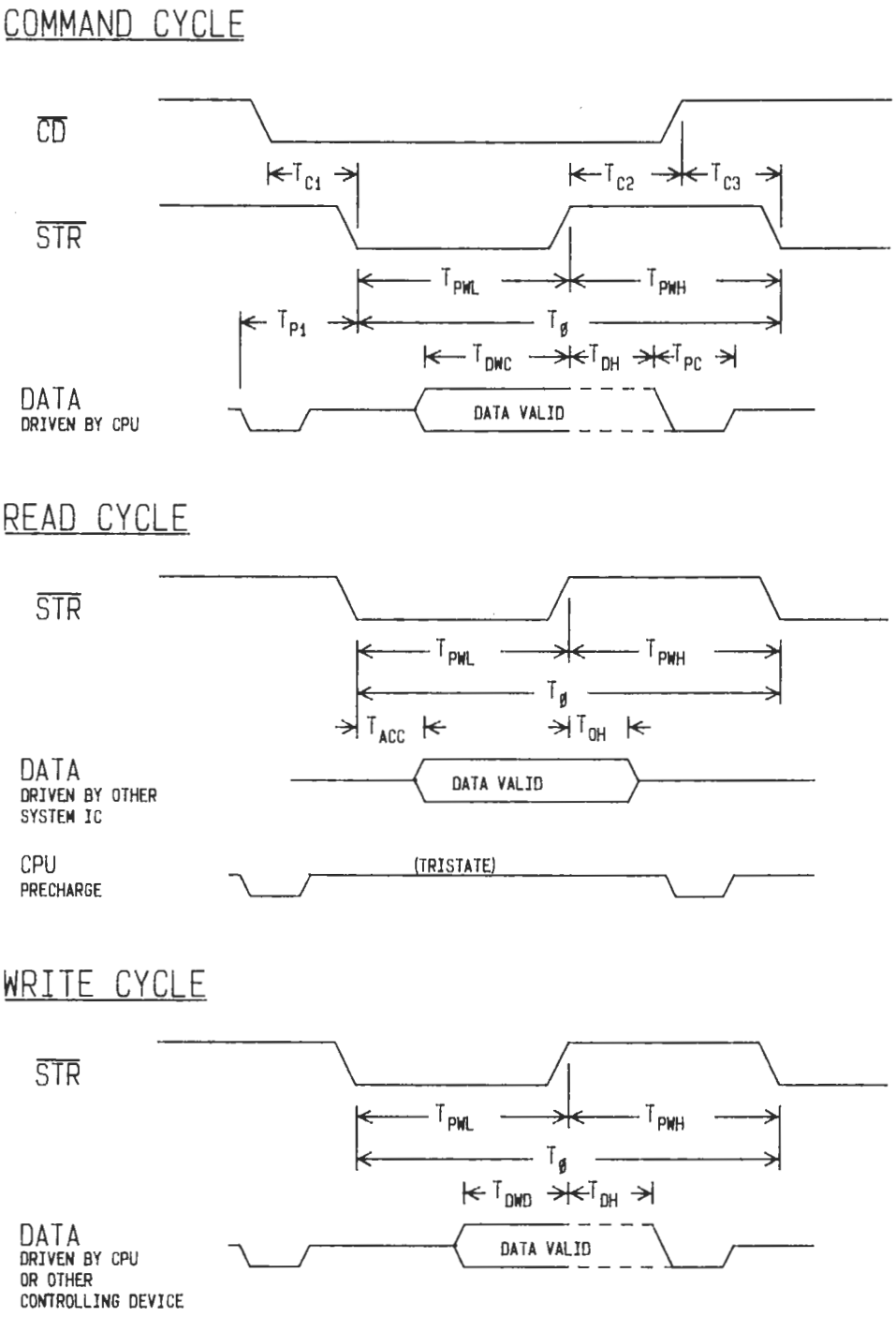

Figure 9-1. Bus Timing Relationships

SYM	PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
Fclk	Display *CLK frequency	-	512	-	Hz	+- 40 PPM Real time base.
LOW BATTERY INDICATION						
Vlbi	Low battery trip point	4.3	-	4.5	V	Low battery bit high when Vdd < Vlbi.
Vdta	Vlbi - Very low battery trip point	.08	-	.12	V	Very low battery bit high when Vdd < Vlbi-Vdta.

NOTES :

1) The values specified for Vac limit the peak voltage that may be applied between the 2 AC adapter input pins. This voltage may be either an AC peak voltage or a DC voltage. If a voltage less than 9.0V is applied the unit's batteries may be discharged. This minimum value for Vac (9.0V) can be reduced to 7.5V if the batteries are removed from the unit.

2) The values specified under Cout and Cin for BUS0-3, *CD, and *STR allow for 100pF loading by plug-in modules. This can be broken down as:

   a) RAM or ROM modules = 20pF x 4
   b) HP-IL module = 12pF
   c) Card reader module = 8pF

   A HP-71B with no plug-in modules could drive 100pF more than specified and would load these lines 100pF less than specified.

3) Reduce Cout (output capacitance drive capability) by 25 pF/mA of the larger of Ioh and Iol (high level source and low level sink current capability) required of BUS0-3, *CD, and/or *STR. Under no condition should the minimum current capability specified for Ioh and Iol be exceeded.

4) The DIN lines of the I/O ports are driven by the CPU output register (OR). The OR lines are also used to form the keyboard matrix and therefore excessive loading of a DIN line will prevent proper keyboard operation. The maximum capacitive loading of a DIN line may be increased to 50pF if a pulldown resistor, Rpd, of 50 Kohm (+-10%) is tied from DIN to ground. For most of the time when the HP-71 is turned on all lines of the OR are high and thus Rpd will draw current. When the HP-71 is shut off the operating system sets OR0 high and all other OR lines low. OR0 drives the DIN line of Port 1.