Document Number: FXOS8700CQ
Rev. 1, 06/2012

RoHS

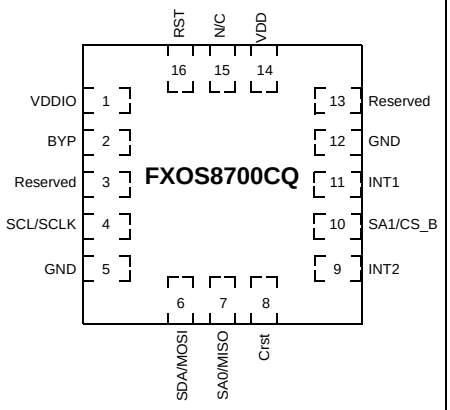
6-Axis Xtrinsic Sensor with Integrated Linear Accelerometer and Magnetometer

FXOS8700CQ

16 LEAD QFN
3 mm by 3 mm by 1.2 mm

FXOS8700CQ is a small, low-power 6-axis linear accelerometer and magnetometer combined into a single package. The device features a selectable digital I^2C or SPI serial interface with 14-bit accelerometer and 16-bit magnetometer resolution along with smart-embedded functions. FXOS8700CQ has dynamically selectable acceleration full scales of ±2g/±4g/±8g and a fixed magnetic measurement range of ±1200 µT. Output Data Rates (ODR) from 1.563 Hz to 800 Hz are selectable by the user for each sensor. Interleaved magnetic and acceleration data is available at ODR rates of up to 400 Hz. FXOS8700CQ is available in a plastic QFN package and it is guaranteed to operate over the extended temperature range of -40°C to +85°C.

Top View



Pin Connections

Features

- 1.95V to 3.6V VDD supply voltage, 1.62V to 3.6 VDDIO voltage
- ±2g/±4g/±8g dynamically selectable acceleration full-scale range
- ±1200 µT magnetic sensor full-scale range
- Output Data Rates (ODR) from 1.563 Hz to 800 Hz for each sensor, and up to 400 Hz when operated in hybrid mode with both sensors active
- Low noise: < 150 µg/√Hz acceleration, < 1 µT rms magnetic
- 14-bit resolution for acceleration measurements
- 16-bit resolution for magnetic measurements
- Footprint compatible with Xtrinsic MMA8451, 2, 3
- Embedded programmable acceleration event functions:
  - Freefall and Motion Detection
  - Transient Detection
  - Vector-Magnitude Change Detection
  - Pulse and Tap Detection (Single and Double)
  - Orientation Detection (Portrait/Landscape)
- Embedded programmable magnetic event functions:
  - Threshold Detection
  - Vector-Magnitude Change Detection
  - Autonomous Magnetic Min/Max Detection
  - Autonomous Hard-Iron Calibration
- Programmable automatic ODR change using Auto-Wake and return to Sleep functions to save power. This function works with both magnetic and acceleration event interrupt sources.
- 32-sample FIFO for acceleration data only
- Integrated accelerometer and magnetometer self-test functions

Target Markets

- Smart phones, tablets, personal navigation devices, robotics, UAVs, and wrist watches with embedded electronic compass (eCompass) function.
- Medical applications: patient monitoring, fall detection, and rehabilitation

This document contains information on a new product. Specifications and information herein are subject to change without notice.

freescale Xtrinsic

Applications

- eCompass in mobile devices
- User interface (menu scrolling by orientation change, tap detection for button replacement)
- Orientation detection (portrait/landscape: up/down, left/right, back/front position identification)
- Augmented Reality (AR), gaming, and real-time activity analysis (pedometry, freefall and drop detection for hard disk drives and other devices)
- Power management for mobile devices using inertial and magnetic event detection
- Shock and vibration monitoring (mechatronic compensation, shipping and warranty usage logging)

ORDERING INFORMATION			
Part Number	**Temperature Range**	**Package Description**	**Shipping**
FXOS8700CQR1	-40°C to +85°C	QFN	Tape and Reel

Related Documentation

The FXOS8700CQdevice features and operations are described in a variety of reference manuals, user guides, and application notes. To find the most-current versions of these documents:

1. Go to the Freescale homepage at:

   http://www.freescale.com/

2. In the Keyword search box at the top of the page, enter the device number FXOS8700CQ.

In the Refine Your Result pane on the left, click on the Documentation link.

Contents

1 Block Diagram

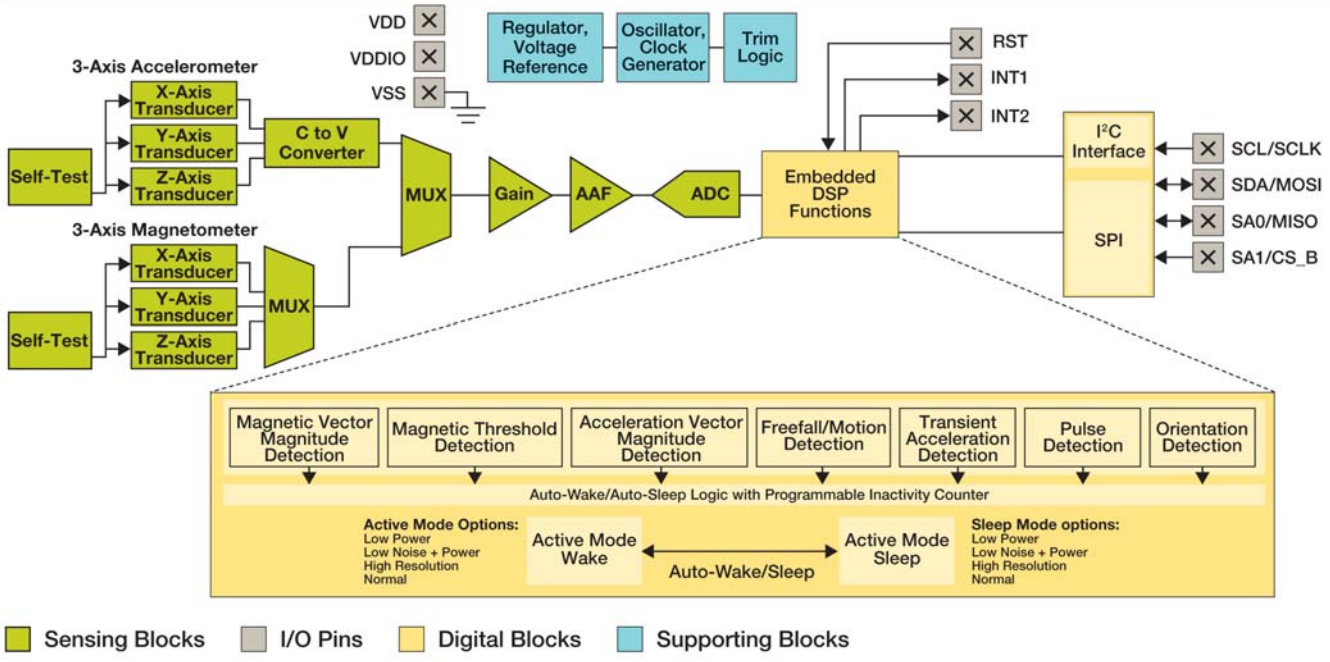
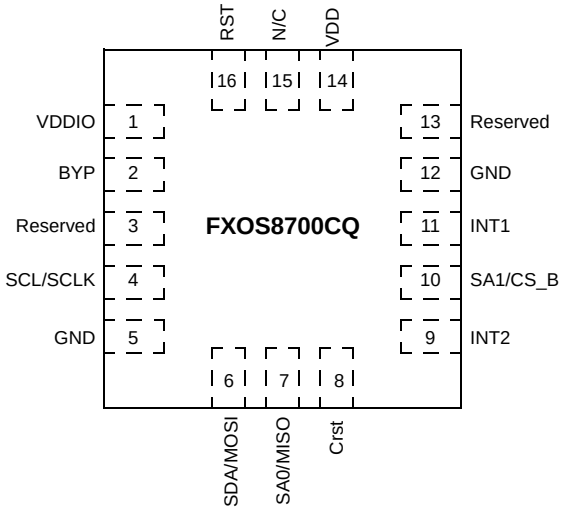


Figure 1. Block diagram

2 Pin Description



Top View
16 Lead QFN-COL
3 mm by 3 mm by 1.2 mm

Figure 2. Pinout diagram

Table 1. Pin Description

Pin	Name	Function
1	VDDIO	Interface power supply
2	BYP	Internal regulator output bypass capacitor connection
3	Reserved	Test reserved, connect to GND
4	SCL/SCLK	I^2C Serial Clock/SPI Clock
5	GND	Ground
6	SDA/MOSI	I^2C Serial Data/SPI Master Out, Slave In
7	SA0/MISO	I^2C address selection bit 0[(1)]/SPI Master In, Slave Out
8	Crst	Magnetic reset cap
9	INT2	Interrupt 2
10	SA1/CS_B	I^2C address selection bit 1[(1)]/SPI Chip Select (active low)
11	INT1	Interrupt 1
12	GND	Ground
13	Reserved	Test reserved, connect to GND
14	VDD	Power supply
15	N/C	Internally not connected
16	RST	Reset input, active high. Connect to GND if unused

1. See Table 9 for I^2C address options selectable using the SA0 and SA1 pins.

Device power is supplied through the VDD pin. Power supply decoupling capacitors (100 nF ceramic plus 4.7 µF bulk) should be placed as close as possible to pin 14 of the device. The digital interface supply voltage (VDDIO) should be decoupled with a 100 nF ceramic capacitor placed as close as possible to pin 1 of the device.

The digital control signals SCL, SDA, SA0, SA1, and RST are not tolerant of voltages more than VDDIO + 0.3V. If VDDIO is removed, these pins will clamp any logic signals through their internal ESD protection diodes.

The function and timing of the two interrupt pins (INT1 and INT2) are user programmable through the I^{2}C/SPI interface. The SDA and SCL I^{2}C connections are open drain and therefore require a pullup resistor as shown in the application diagram in Figure 3. The INT1 and INT2 pins may also be configured for open-drain operation. If they are configured for open drain, external pullup resistors are required.

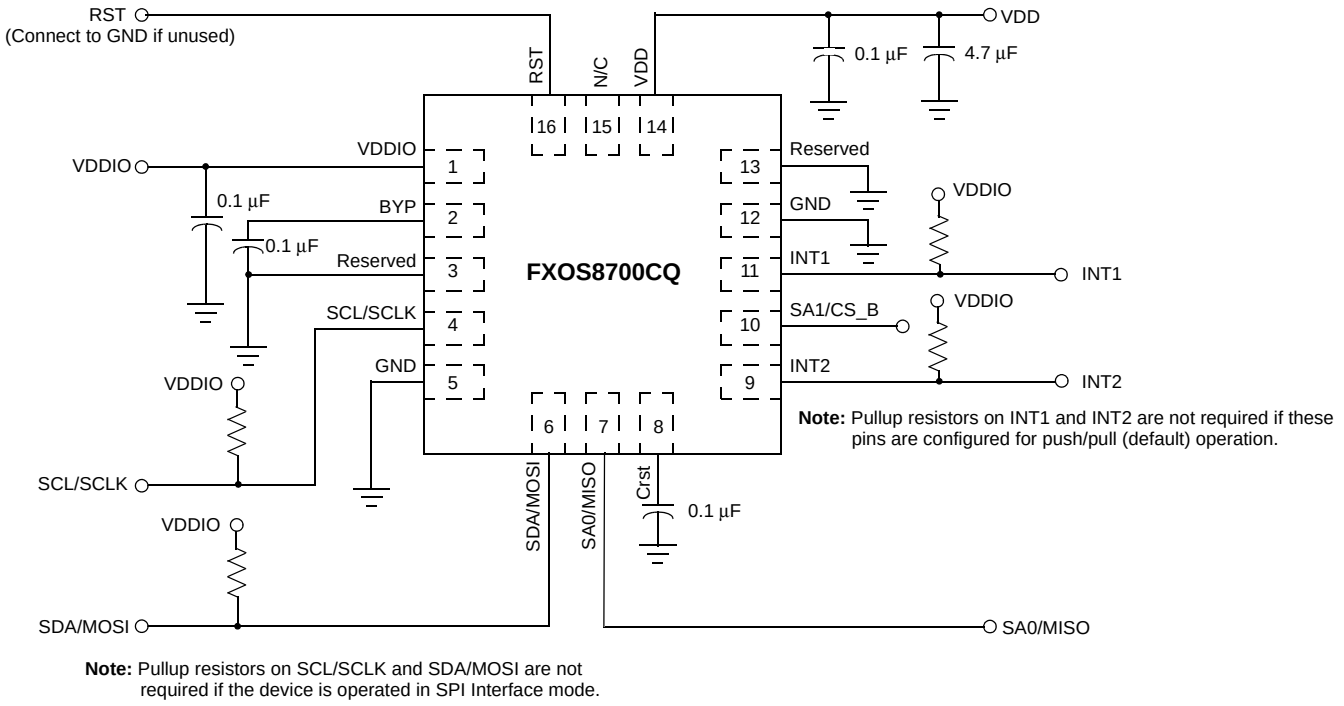


Figure 3. Electrical connection

2.1 Soldering information

The QFN package is compliant with the RoHS standards. Please refer to Freescale application note AN4077 for more information.

2.2 Orientation

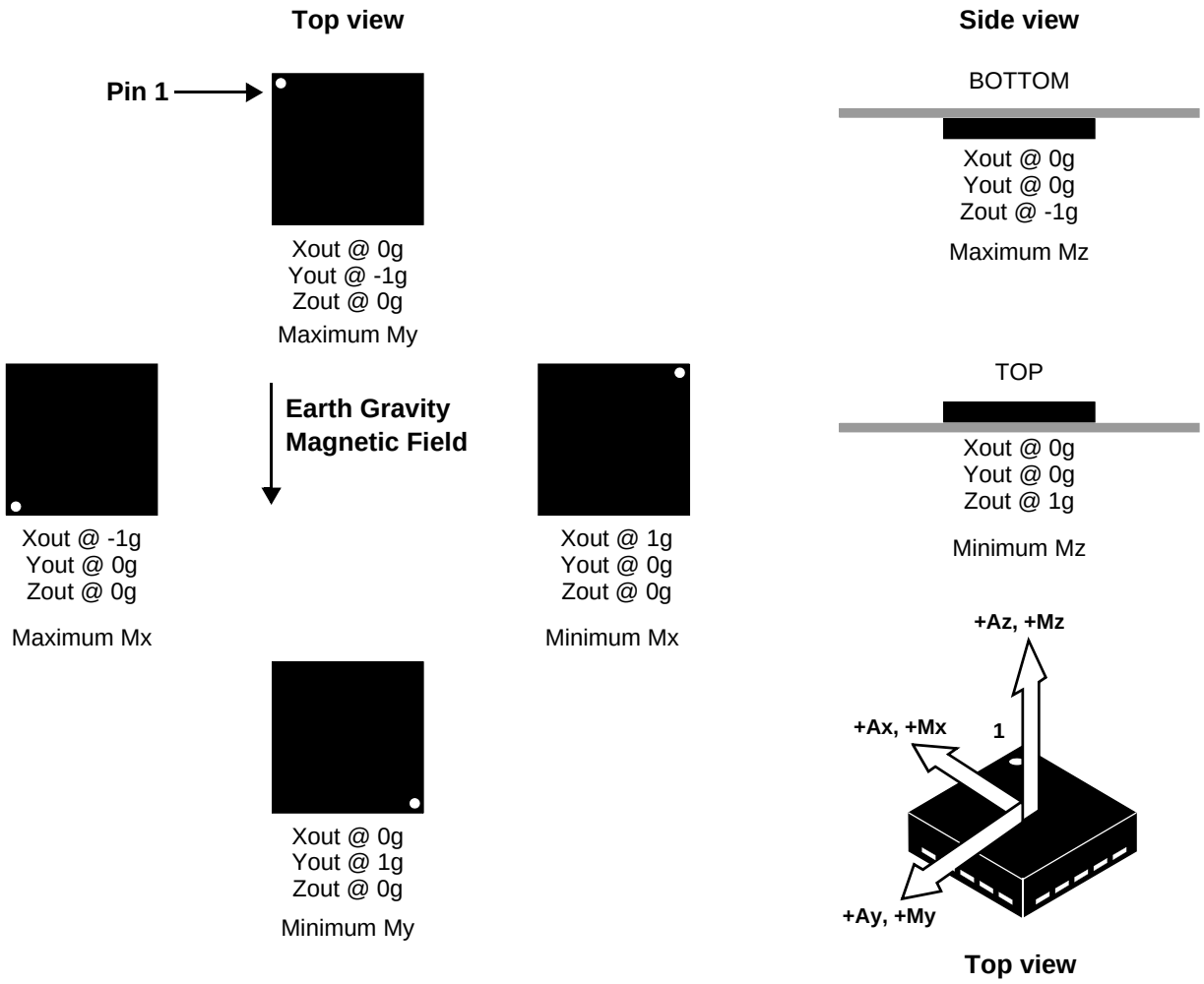


Figure 4. Product orientation and axis orientation

3 Terminology

3.1 Sensitivity

Sensitivity is represented in mg/LSB for the accelerometer and μT/LSB for the magnetometer. The magnetometer sensitivity is fixed at 0.1 μT/LSB. The accelerometer sensitivity changes with the full-scale range selected by the user. Accelerometer sensitivity is 0.244 mg/LSB in 2g mode, 0.488 mg/LSB in 4g mode, and 0.976 mg/LSB in 8g mode.

3.2 Zero-g and Zero-Flux offset

For the accelerometer, zero-g offset (TyOff) describes the deviation of the output values from the ideal values when the sensor is stationary. With an accelerometer stationary on a level horizontal surface, the ideal output is 0g for the X and Y axes, and 1g for the Z-axis. The deviation of each axes output from the ideal value is called zero-g offset. Offset is to some extent a result of stress on the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. For the magnetometer, zero-flux offset describes the deviation of the output signal from zero when the device is shielded from external magnetic field sources (i.e. inside a zero-gauss chamber).

3.3 Self-Test

Self-Test can be used to verify the accelerometer and magnetometer transducer functionality without the need for an external acceleration or magnetic field stimulus. When the accelerometer self-test is activated, an electrostatic actuation force is applied to the sensor, simulating a small acceleration. In this case the sensor X, Y, Z outputs will exhibit a change in DC levels related to the selected full-scale range (sensitivity). When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic self-test force. When self-test is activated for the magnetometer, an internal magnetic field is generated along the X, Y and Z axes. The sensor response will be the sum of the ambient magnetic field and the self-test induced field.

4 Device Characteristics

4.1 Mechanical characteristics (accelerometer)

Table 2. Mechanical characteristics @ VDD = 2.5V, VDDIO = 1.8V T = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
FS	Measurement range[1]	±2g mode		±2		g
		±4g mode		±4		
		±8g mode		±8		
So	Sensitivity	±2g mode		4096		LSB/g
				0.244		mg/LSB
		±4g mode		2048		LSB/g
				0.488		mg/LSB
		±8g mode		1024		LSB/g
				0.976		mg/LSB
TCSo[1]	Sensitivity change with temperature	±2g, ±4g, ±8g modes		±0.008		%/°C
Soa	Sensitivity accuracy[2]			±1		%
TyOff	Zero-g level offset accuracy[3]	±2g, ±4g, ±8g modes		±20		mg
TyOffPBM	Zero-g level offset accuracy post-board mount[4]	±2g, ±4g, ±8g modes		±30		mg
TCOff	Zero-g level change versus temperature	-40°C to 85°C[1]		±0.15		mg/°C
NL	Nonlinearity Best-fit straight line	Over ±2g range normal mode Over ±1g range low-noise mode		TBD		%FS
Vst	Self-Test output change[5] X Y Z	Set to ±4g mode		+181 +255 +1680		LSB
	ODR accuracy, 2 MHz clock			±2		%
BW	Output-data bandwidth		ODR/3		ODR/2	Hz
Noise	Output-noise density	ODR = 400 Hz, normal mode		126		µg/√Hz
Noise	Output-noise density low-noise mode[1]	ODR = 400 Hz, normal mode		99		µg/√Hz
Top	Operating temperature range		-40		+85	°C

1. Dynamic range is limited to ±4g when in the low-noise mode.
2. Sensitivity remains in spec as stated, but changing the oversampling mode to low power causes a 3% sensitivity shift. This behavior is also seen when changing from 800 Hz ODR to any other ODR in the normal, low-noise + low-power, or high-resolution modes.
3. Before board mount.
4. Post-board mount offset specifications are based on an 8-layer PCB.
5. Self-test is only exercised along one direction for each sensitive axis.

4.2 Magnetic characteristics (magnetometer)

Table 3. Magnetic characteristics @ VDD = 2.5V, VDDIO = 1.8V T = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
FS	Measurement range		±1200			µT
So	Sensitivity			0.1		µT/LSB
Tc	Sensitivity change versus temperature			±0.1		%/°C
	Zero-flux offset accuracy[1]			±1		µT
Tco	Zero-flux offset change with temperature			0.8 (XY) 2.4 (Z)		µT/°C
	Hysteresis[2]			±1		%FS
NL	Nonlinearity[3] Best-fit straight line			TBD		%FS
	Temperature sensor repeatability[4]			1		°C
	Temperature sensor sensitivity			0.96		°C/LSB
Noise	Magnetometer output noise	ODR = 800 Hz, OS = 2		1.7 (XY) 2.5 (Z)		µT/rms
		ODR = 400 Hz, OS = 4		1.2 (XY) 1.8 (Z)		
		ODR = 200 Hz, OS = 8		0.85 (XY) 1.3 (Z)		
		ODR = 100 Hz, OS = 16		0.6 (XY) 0.9 (Z)		
		ODR = 50 Hz, OS = 32		0.42 (XY) 0.6 (Z)		
		ODR = 12.5 Hz, OS = 128		0.3 (XY) 0.44 (Z)		
		ODR = 6.25 Hz, OS = 256		0.23 (XY) 0.33 (Z)		
		ODR = 1.56 Hz, OS = 1024		0.21 (XY) 0.3 (Z)		
Vst	Self-Test output change[1]	X-axis	20	-1320	TBD	LSB
		Y-axis	20	+1300	TBD	LSB
		Z-axis	20	100	TBD	LSB
BW	Output data bandwidth		ODR/3		ODR/2	Hz
Top	Operating temperature range		-40		+85	°C

1. After m-cell has been trimmed.
2. Hysteresis is measured by sweeping the applied magnetic field from -1500 µT to 1500 µT and then back to -1500 µT. The difference in the two readings at -1500 µT divided by the swept field range is the hysteresis figure, expressed in % of the full-scale range (FS).
3. Over a ±300 µT sliding window within the full-scale range.
4. Verified by characterization.

4.3 Hybrid characteristics

Table 4. Hybrid characteristics @ VDD = 2.5V, VDDIO = 1.8V T = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Maximum output data rate in hybrid mode			400		Hz
Top	Operating temperature range		-40		+85	°C

4.4 Electrical characteristics

Table 5. Electrical characteristics @ VDD = 2.5V, VDDIO = 1.8V T = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VDD	Supply voltage		1.95	2.5	3.6	V
VDDIO	Interface supply voltage		1.62	1.8	3.6	V
I_{dd}LP	Low-power acceleration mode	ODR = 12.5 Hz		8		µA
		ODR = 100 Hz		35		
		ODR = 400 Hz		130		
I_{dd}	Normal acceleration mode	ODR = 50 Hz		35		µA
		ODR = 200 Hz		130		
		ODR = 800 Hz		240		
I_{dd}	Hybrid mode	ODR = 200 Hz g-cell OS = 4 m-cell OS = 2		440		µA
		ODR = 100 Hz g-cell OS = 4 m-cell OS = 2		240		
		ODR = 25 Hz g-cell OS = 4 m-cell OS = 2		80		
I_{dd}	Magnetic mode	ODR = 400 Hz, OS = 2		575		µA
		ODR = 12.5 Hz, OS = 2		40		
Idd Boot	Current during boot sequence, 0.9 mS max duration using recommended regulator bypass capacitor	VDD = 2.5V			3	mA
Cap, Cres	Value of capacitors on BYP pin and magnetic reset pins	-40°C to 85°C	75	100	470	nF
IddSTBY	Standby mode current @ 25°C	Standby mode		2		µA
IddSTBY	Standby mode current over-temperature range	Standby mode			16	µA
VIH	Digital high-level input voltage RST pin			1.04		V
VIL	Digital low-level input voltage RST pin			0.68		V
VIH	Digital high-level input voltage SCL, SDA, SA0, SA1		0.75*VDDIO			V
VIL	Digital low-level input voltage SCL, SDA, SA0, SA1				0.3*VDDIO	V
VOH	High-level output voltage INT1, INT2	I_O = 500 µA	0.9*VDDIO			V
VOL	Low-level output voltage INT1, INT2	I_O = 500 µA			0.1*VDDIO	V
VOLS	Low-level output voltage SDA	I_O = 500 µA			0.1*VDDIO	V

Table 5. Electrical characteristics @ VDD = 2.5V, VDDIO = 1.8V T = 25°C unless otherwise noted.

	SCL, SDA pin leakage	25°C		1.0		nA
		-40°C to 85°C		4.0		
	SCL, SDA pin capacitance			3		pf
BW	3 dB signal bandwidth	Magnetic or acceleration mode		ODR/3		Hz
BW	Signal bandwidth	Hybrid mode		ODR/6		Hz
	Power-on ramp time		0.001		1000	mSec
BT	Boot time(1)			900	1000	µs
	Turn-on time(2)				2/ODR + 1	ms
	Turn-on time(3)				2/ODR + 2	ms
Top	Operating temperature range		-40		+85	°C

1. Time from VDDIO on and VDD > VDD min until I^2C ready for operation.
2. Time to obtain valid data from Standby mode to Active mode.
3. Time to obtain valid data from power-down condition.

4.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 6. Maximum ratings

Rating	Symbol	Value	Unit
Maximum acceleration (all axes, 100 µs)	g_{max}	5,000	g
Supply voltage, IO voltage	VDD	-0.3 to +3.6	V
Input voltage on any control pin (SA0/MISO, SA1/CS_B, SCL/SCLK, SDA/MOSI, RST)	Vin	-0.3 to VDDIO + 0.3	V
Drop-Test height	D_{drop}	1.8	M
Maximum exposed magnetic field without perming (sensor characteristics may be restored using the magnetic reset de-gauss function)		10,000	µT
Maximum exposed field without permanent damage		0.1	T
Storage temperature range	T_{STG}	-40 to +125	°C

Table 7. ESD and latchup protection characteristics

Rating	Symbol	Value	Unit
Human Body Model	HBM	±2000	V
Machine Model	MM	±200	V
Charge Device Model	CDM	±500	V
Latchup current at T = 85°C		±100	mA

This device is sensitive to ESD, improper handling can cause permanent damage to the part.

5 Digital Interfaces

5.1 I²C interface characteristics

Table 8. I²C slave timing values(1)

Parameter	Symbol	I²C Fast Mode		Unit
		Min	Max	
SCL Clock Frequency	f_{SCL}	0	400	kHz
Bus Free Time between STOP and START condition	t_{BUF}	1.3		µs
(Repeated) START Hold Time	$t_{HD;STA}$	0.6		µs
(Repeated) START Setup Time	$t_{SU;STA}$	0.6		µs
STOP Condition Setup Time	$t_{SU;STO}$	0.6		µs
SDA Data Hold Time	$t_{HD;DAT}$	0.05	0.9(2)	µs
SDA Valid Time(3)	$t_{VD;DAT}$		0.9(2)	µs
SDA Valid Acknowledge Time(4)	$t_{VD;ACK}$		0.9(2)	µs
SDA Setup Time	$t_{SU;DAT}$	100		ns
SCL Clock Low Time	t_{LOW}	1.3		µs
SCL Clock High Time	t_{HIGH}	0.6		µs
SDA and SCL Rise Time	t_r	20 + 0.1 C_b(5)	300	ns
SDA and SCL Fall Time	t_f	20 + 0.1 C_b(5)	300	ns
Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter	t_{SP}	0	50	ns

1. All values referred to VIH (min) and VIL (max) levels.
2. This device does not stretch the LOW period (t_{LOW}) of the SCL signal.
3. $t_{VD;DAT}$ = time for Data signal from SCL LOW to SDA output.
4. $t_{VD;ACK}$ = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
5. C_b = total capacitance of one bus line in pF.

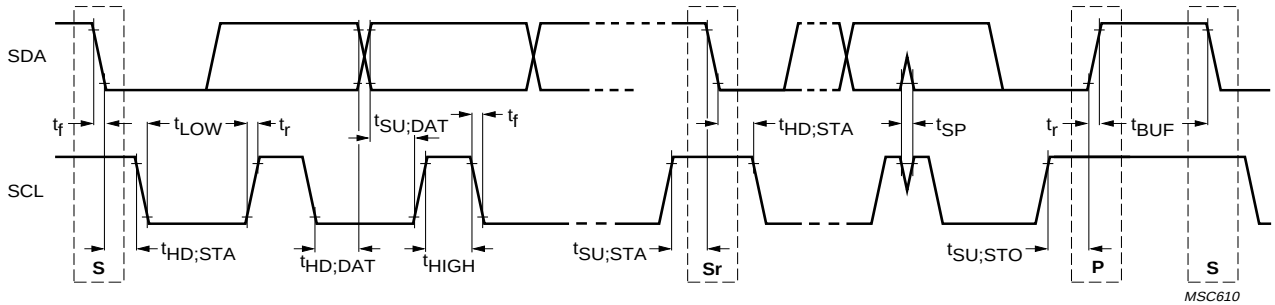


Figure 5. I²C slave timing diagram

5.1.1 General I²C operation

There are two signals associated with the I²C bus: the Serial Clock Line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to VDDIO are required for SDA and SCL. When the bus is free both the lines are high. The I²C interface is compliant with fast mode (400 kHz), and normal mode (100 kHz) I²C standards. Operation at frequencies higher than 400 kHz is possible, but depends on several factors including the pullup resistor values, and total bus capacitance (trace + device capacitance). See Table 8 for more information.

A transaction on the bus is started through a start condition (ST) signal, which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After the ST signal has been transmitted by the master, the bus is considered busy. The next byte of data transmitted contains the slave address in the first seven bits, and the eighth bit, the read/write bit, indicates whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after the ST condition with its own address. If they match, the device considers itself addressed by the master. The 9th clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching. Not all receiver devices support clock stretching. Not all master devices recognize clock stretching. This part does not use clock stretching.

A low to high transition on the SDA line while the SCL line is high is defined as a stop condition (SP) signal. A write or burst write is always terminated by the master issuing the SP signal. A master should properly terminate a read by not acknowledging a byte at the appropriate time in the protocol. A master may also issue a repeated start signal (SR) during a transfer

The slave addresses that may be assigned to the FXOS8700CQ part are 0x1C, 0x1D, 0x1E, or 0x1F. The selection is made by the logic level of the SA1 and SA0 inputs. Consult the factory for alternate address programming options.

Table 9. I²C slave address

SA1	SA0	Slave address*
0	0	0x1E
0	1	0x1D
1	0	0x1C
1	1	0x1F

* Preproduction parts have the I²C address of 0x1C, 0x1D, 0x1E and 0x1F respectively.

5.1.2 I²C Read/Write operations

Single byte read

The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address, with the R/W bit set to “0” for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to read and the FXOS8700CQ sends an acknowledgement. The master (or MCU) transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to “1” for a read from the previously selected register. The FXOS8700CQ then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

Multiple byte read

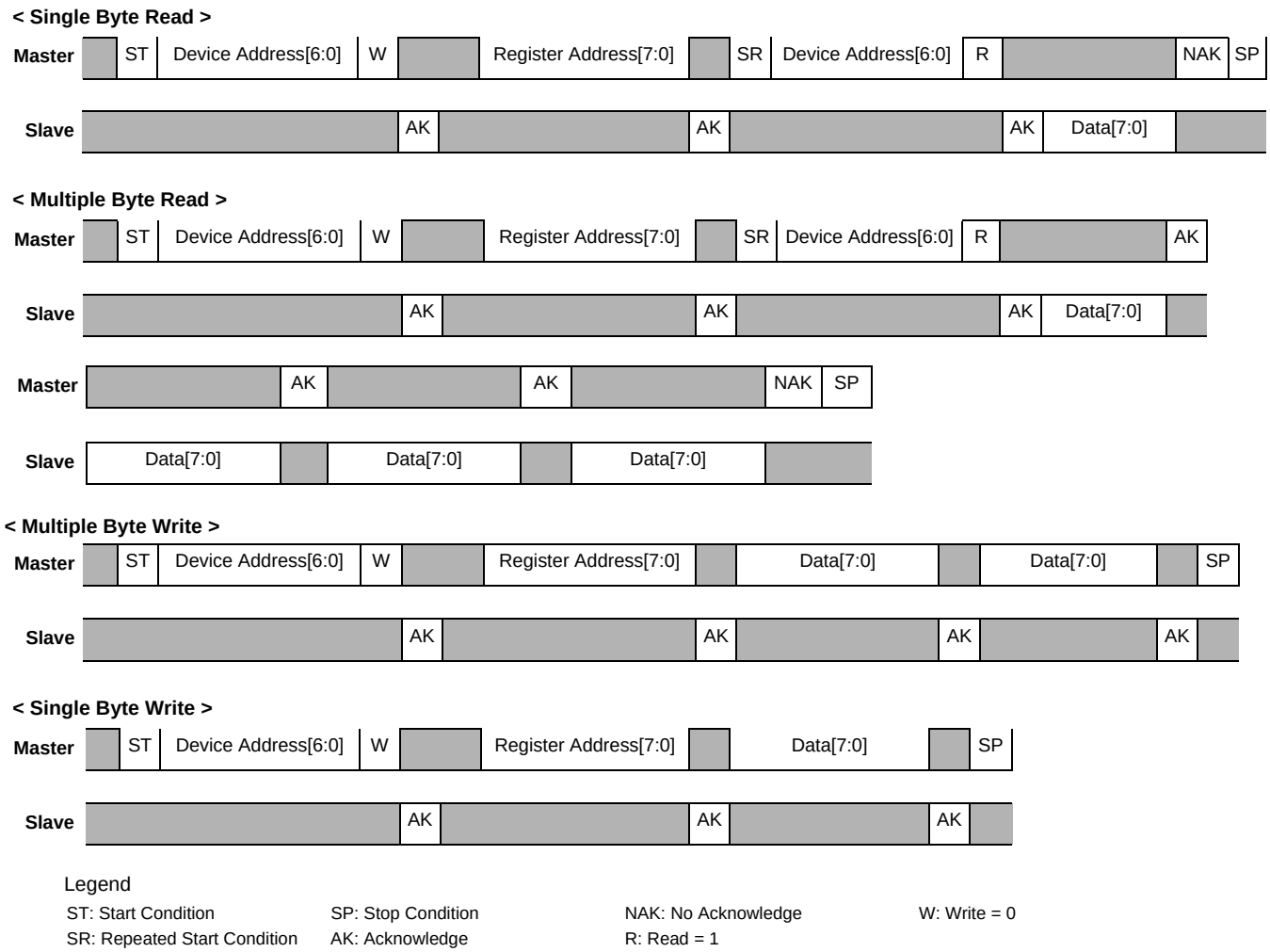
When performing a multi-byte or “burst” read, the FXOS8700CQ automatically increments the register address read pointer after a read command is received. Therefore, after following the steps of a single byte read, multiple bytes of data can be read from sequential registers after each FXOS8700CQ acknowledgment (AK) is received until a no acknowledge (NAK) occurs from the master followed by a stop condition (SP) signaling an end of transmission.

Single byte write

To start a write command, the master transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address with the R/W bit set to “0” for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to write to, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the 8-bit data to write to the designated register and the FXOS8700CQ sends an acknowledgement that it has received the data. Since this transmission is complete, the master transmits a stop condition (SP) to end the data transfer. The data sent to the FXOS8700CQ is now stored in the appropriate register.

Multiple byte write

The FXOS8700CQ automatically increments the register address write pointer after a write command is received. Therefore, after following the steps of a single byte write, multiple bytes of data can be written to sequential registers after each FXOS8700CQ acknowledgment (ACK) is received.



Legend

ST: Start Condition	SP: Stop Condition	NAK: No Acknowledge	W: Write = 0
SR: Repeated Start Condition	AK: Acknowledge	R: Read = 1	

Figure 6. I^{2}C timing diagram

5.2 SPI Interface characteristics

SPI interface is a classical master/slave serial port. The FXOS8700CQ is always considered as the slave and thus is never initiating the communication.

Table 10 and Figure 7 describe the timing requirements for the SPI system.

Table 10. SPI timing

Function	Symbol	Min	Max	Unit
Operating Frequency	O*f*	—	1	MHz
SCLK Period	tSCLK	1000	—	ns
SCLK High time	tCLKH	500	—	ns
SCLK Low time	tCLKL	500	—	ns
CS_B lead time	tSCS	65	—	ns
CS_B lag time	tHCS	65	—	ns
MOSI data setup time	tSET	25	—	ns
MOSI data hold time	tHOLD	75	—	ns
MISO data valid (after SCLK low edge)	tDDLY	—	500	ns
Width CS High	tWCS	TBD	—	ns

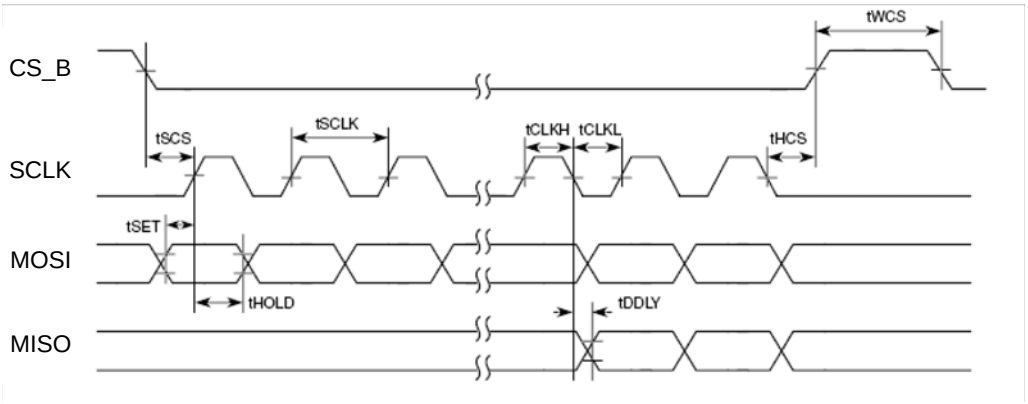


Figure 7. SPI Timing Diagram

5.2.1 General SPI operation

The CS_B pin is driven low at the start of a SPI transaction, held low for the duration of the transaction, and driven high after the transaction is complete. During a transaction the master toggles the SPI clock (SCLK) and transmits data on the MOSI pin.

A write operation is initiated by transmitting a 1 for the R/W bit. Then the 8-bit register address, ADDR[7:0] is encoded in the first and second serialized bytes. Data to be written starts in the third serialized byte. The order of the bits is as follows:

R/W,ADDR[6],ADDR[5],ADDR[4],ADDR[3],ADDR[2],ADDR[1],ADDR[0],

ADDR[7],X,X,X,X,X,X,X,

DATA[7],DATA[6],DATA[5],DATA[4],DATA[3],DATA[2],DATA[1],DATA[0].

Multiple bytes of DATA may be transmitted. The X indicates a bit that is ignored by the part. The register address is auto-incremented so that the next clock edges will latch the data for the next register. When desired, the rising edge on CS_B stops the SPI communication.

The FXOS8700CQ SPI configuration is as follows:

- Polarity: rising/falling
- Phase: sample/setup
- Order: MSB first

5.2.2 SPI READ/WRITE operations

A READ operation is initiated by transmitting a 0 for the R/W bit. Then the 8-bit register address, ADDR[7:0] is encoded in the first and second serialized bytes. Subsequent bits are ignored by the part. The read data is deserialized from the MISO pin.

Similarly a WRITE operation is initiated by transmitting a 1 for the R/W bit. After the first and second serialized bytes multiple data bytes can be transmitted into consecutive registers, starting from the indicated register address in ADDR[7:0].

An SPI transaction is started by asserting the CS_B pin (high-to-low transition), and ended by deasserting the CS_B pin (low-to-high transition).

R/W bit followed by ADDR [6:0]	ADDR[7] followed by 7 “don’t care” bits	Data0*	Data1	—	Datan

* Data bytes must be transmitted to the slave (FXOS8700CQ) via MOSI pin by the master when R/W = 1. Data bytes will be transmitted by the slave (FXOS8700CQ) to the master via MISO pin when R/W = 0. The first 2 bytes are always transmitted by the master via MOSI pin. i.e. a transaction is always initiated by master.

Figure 8. SPI single-burst READ/WRITE transaction diagram

The registers embedded inside the FXOS8700CQ are accessed through either an I^2C, or a SPI serial interface. To enable either interface the VDDIO line must be connected to the interface supply voltage. If VDD is not present and VDDIO is present FXOS8700CQ is in shutdown mode and communications on the interface are ignored. If VDDIO is held high, VDD can be powered off and the communications pins will be in a high impedance state. This will allow communications to continue on the bus with other devices.

Table 11. Serial interface pin descriptions

Pin Name	Pin Description
VDDIO	Digital interface power
SA1/CS_B	I^2C second least significant bit of device address/SPI chip select
SCL/SCLK	I^2C/SPI serial clock
SDA/MOSI	I^2C serial data/SPI master serial data out slave serial data in
SA0/MISO	I^2C least significant bit of the device address/SPI master serial data in slave out

5.2.3 I^2C/SPI auto detection

Table 12. I^2C/SPI auto detection

SA0	Slave address
GND	I^2C
VDDIO	I^2C
Floating	SPI

It is possible to factory-trim parts such that the part always uses either I^2C or SPI communication protocol. When this trim is not in place the device will operate in either I^2C or SPI interface mode based on the state of the SA0 pin during power up or when exiting reset. Once set for I^2C or SPI operation the device will remain in I^2C or SPI mode until the device is reset.

5.2.4 Power supply sequencing and I^2C/SPI mode auto detection

This component does not have any specific power supply sequencing requirements between VDD and VDDIO voltage supplies to ensure normal operation. To ensure correct operation of the I^2C/SPI auto-detection function, VDDIO should be applied before or at the same time as VDD. If this order cannot be maintained, the user should either toggle the RST line or power cycle the VDD rail in order to force the auto-detect function to restart and correctly identify the desired interface. Please consult the factory for further options if necessary.

6 Modes of Operation

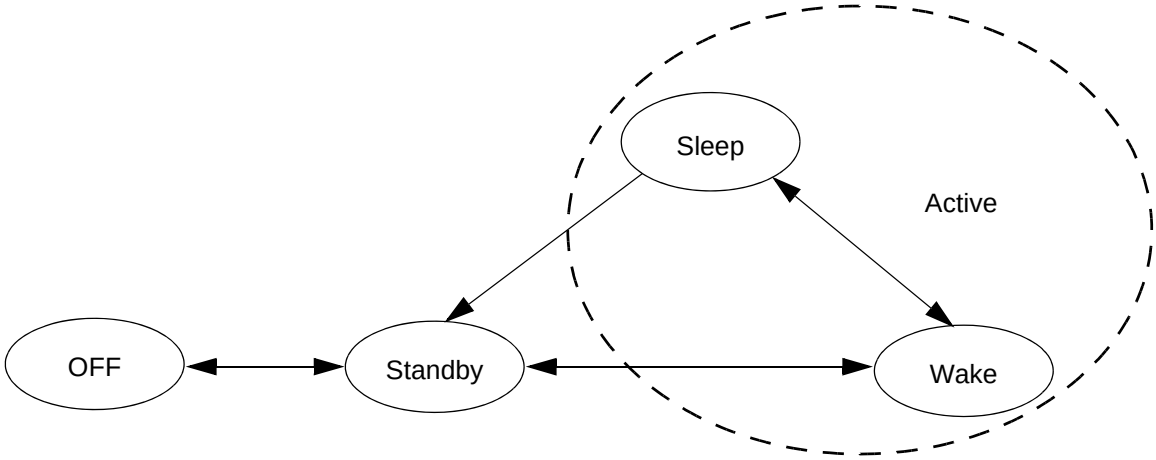


Figure 9. FXOS8700CQ power mode transition diagram

Table 13. Mode of operation description

Mode	I^2C/SPI Bus state	VDD	VDDIO	Function description
OFF	Powered down	<1.8 V	VDDIO can be > VDD	The device is powered off. All analog and digital blocks are shutdown. I^2C bus inhibited.
Standby	I^2C/SPI communication with FXOS8700CQ is possible	ON	VDDIO = High VDD = High Active bit is cleared	Only digital blocks are enabled. Analog subsystem is disabled. Internal clocks disabled.
Active (Wake/Sleep)	I^2C/SPI communication with FXOS8700CQ is possible	ON	VDDIO = High VDD = High Active bit is set	All blocks are enabled (digital and analog).

All register contents are preserved when transitioning from Active to Standby mode. Some registers are reset when transitioning from Standby to Active. These are all noted in the device memory map register table. The Sleep and Wake modes are active modes. For more information on how to use the Sleep and Wake modes and configuring the device to transition between them, please refer to Section 7, “Embedded Functionality” or Freescale application note AN4074.

7 Embedded Functionality

FXOS8700CQ is a low-power, digital output 6-axis sensor with both I^2C and SPI interfaces. Extensive embedded functionality is provided to detect inertial and magnetic events at low-power, with the ability to notify the host processor of an event via either of the two programmable interrupt pins. The embedded functionality includes:

- 8-bit or 14-bit accelerometer data which includes high-pass filtered data, and 8 or 16-bit magnetometer data
- Four different oversampling options for the accelerometer output data, and eight for the magnetometer. The oversampling settings allow the end user to optimize the resolution versus power trade-off in a given application.
- A low-noise accelerometer mode that functions independently of the oversampling modes for even higher resolution
- Low-power auto-wake/sleep function for conserving power in portable battery powered applications
- Accelerometer pulse detection circuit which can be used to detect directional single and double taps
- Accelerometer directional motion and freefall event detection with programmable threshold and debounce time
- Acceleration transient detection with programmable threshold and debounce time. Transient detection can employ either a high-pass filter or use the difference between reference and current sample values.
- Orientation detection with programmable hysteresis for smooth transitions between portrait/landscape orientations
- Accelerometer vector magnitude change event detection with programmable reference, threshold, and debounce time values
- Magnetic threshold event detection with programmable reference, threshold, and debounce time
- Magnetometer vector magnitude change event detection with programmable reference, threshold and debounce time values
- Magnetic min/max detection circuit which can also be used for autonomous calibration of magnetic hard-iron offset

Many different configurations of the above functions are possible to suit the needs of the end application. Separate application notes are available to further explain the different configuration settings and potential use cases.

7.1 Factory calibration

FXOS8700CQ's integrated accelerometer and magnetometer sensors are factory calibrated for sensitivity and offset on each axis. The trim values are stored in Non-Volatile Memory (NVM). On power-up, the trim parameters are read from NVM and applied to the internal compensation circuitry. After mounting the device to the PCB, the user may further adjust the accelerometer and magnetometer offsets through the OFF_X/Y/Z and M_OFF_X/Y/Z registers, respectively. For more information on device calibration, refer to Freescale application note, AN4069.

7.2 8-bit or 14-bit accelerometer data

The measured acceleration data is stored in the OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB registers as 2's complement 14-bit numbers. The most significant 8-bits of each axis are stored in the OUT_X, Y, Z_MSB registers, so applications needing only 8-bit results simply read these three registers and ignore the OUT_X,Y, Z_LSB registers. To do this, the *f_read* mode bit in CTRL_REG1 must be set.

When the full-scale range is set to 2g, the measurement range is -2g to +1.999g, and each count corresponds to 0.244 mg at ±14-bits resolution. When the full-scale is set to 8g, the measurement range is -8g to +7.996g, and each count corresponds to 0.976 mg. The resolution is reduced by a factor of 64 if only the 8-bit results are used ([*f_read*] = 1). For further information on the different data formats and modes, please refer to Freescale application note AN4076.

7.3 Accelerometer low-power modes versus high-resolution modes

FXOS8700CQ can be optimized for lower power or for higher resolution of the accelerometer output data. High resolution is achieved by setting the lnoise bit in register 0x2A. This improves the resolution (by lowering the noise), but be aware that the dynamic range becomes limited to ±4g when this bit is set. This will affect all internal embedded functions (scaling of thresholds, etc.) and reduce noise. Another method for improving the resolution of the data is through oversampling. One of the oversampling schemes of the output data can activated when CTRL_REG2[*mods*] = 0b10 which will improve the resolution of the output data without affecting other internal embedded functions or limiting the dynamic range.

There is a trade-off between low power and high resolution. Low power can be achieved when the oversampling rate is reduced. When CTRL_REG2[*mods*] = 0b10, the lowest power is achieved, at the expense of higher noise. In general, the lower the selected ODR and OSR, the lower the power consumption. For more information on how to configure the device in low-power or high-resolution modes and understand the benefits and trade-offs, please refer to Freescale application note AN4075.

7.4 Auto-Wake/Sleep mode

FXOS8700CQ can be configured to transition between sample rates (with their respective current consumptions) based on the status of the embedded interrupt event generators in the device. The advantage of using the Auto-Wake/Sleep is that the system can automatically transition to a higher sample rate (higher current consumption) when needed but spends the majority of the time in the Sleep mode (lower current) when the device does not require higher sampling rates. Auto-Wake refers to the device being triggered by one of the interrupt event functions to transition to a higher sample rate. This may also interrupt the processor to transition from a sleep mode to a higher power mode.

Sleep mode occurs when none of the enabled interrupt event functions has detected an interrupt within the user defined time-out period. The device will then transition to the specified lower sample rate. It may also alert the processor to go into a lower power mode to save power during this period of inactivity. Please refer to AN4074 for more detailed information on configuring the Auto-Wake/Sleep function.

7.5 Hybrid mode

FXOS8700CQ uses a single common Analog-to-Digital Converter (ADC) for both the accelerometer and magnetometer. When operating in hybrid mode (M_CTRL_REG1[m_hms] = 2'b11), both the accelerometer and magnetometer sensors are actively measured by the ADC at an ODR equal to one half of the setting made in CTRL_REG1[dr] when operating in accelerometer-only mode (M_CTRL_REG1[m_hms] = 2'b00 (default)) or magnetometer-only mode (M_CTRL_REG1[m_hms] = 2'b01). While the ODR is common to both sensors when operating in hybrid mode, the OSR settings for each sensor are independent and may be set via CTRL_REG2[mods] for the accelerometer and M_CTRL_REG1[m_os] for the magnetometer, respectively.

7.6 Accelerometer Freefall and Motion event detection

FXOS8700CQ integrates a programmable threshold based acceleration detection function capable of detecting either motion or freefall events depending upon the configuration. For further details and examples on using the embedded freefall and motion detection functions, please refer to Freescale application note AN4070.

7.6.1 Freefall detection

The detection of "Freefall" involves the monitoring of the X, Y, and Z axes for the condition where the acceleration magnitude is **below** a user specified threshold for a user definable amount of time. Typically, the usable threshold ranges are between ±100 mg and ±500 mg.

7.6.2 Motion detection

Motion detection is often used to alert the main processor that the device is currently in use. When the acceleration exceeds a set threshold for a set amount of time, the motion interrupt is asserted. A motion can be a fast moving shake or a slow moving tilt. This will depend on the threshold and timing values configured for the event. The motion detection function can analyze static acceleration changes or faster jolts. The timing value is set by a configurable debounce counter. The debounce counter acts like a filter to indicate whether the condition exists for longer than a set amount of time (i.e., 100 ms or longer). There is also directional data available in the source register to detect the direction of the motion that generated the interrupt. This is useful for applications such as directional shake or flick detection, and can also assist gesture detection algorithms by indicating that a motion gesture has started.

7.7 Transient detection

FXOS8700CQ integrates an acceleration transient detection function that incorporates a high-pass filter. Acceleration data goes through the high-pass filter, eliminating the DC tilt offset and low frequency acceleration changes. The high-pass filter cutoff can be set by the user to four different frequencies which are dependent on the selected Output Data Rate (ODR). A higher cutoff frequency ensures that DC and slowly changing acceleration data will be filtered out, allowing only the higher frequencies to pass. The transient detection feature can be used in the same manner as the motion detection by bypassing the high-pass filter. There is an option in the configuration register to do this. This adds more flexibility to cover the various customer use cases.

Many applications use the accelerometer's static acceleration readings (i.e., tilt) which measure the change in acceleration due to gravity only. These functions benefit from acceleration data being filtered with a low-pass filter where high-frequency data is considered noise. However, there are many functions where the accelerometer must analyze dynamic acceleration. Functions such as tap, flick, shake and step counting are based on the analysis of the change in the dynamic acceleration. The transient detection function can be routed to either interrupt pin through bit 5 in CTRL_REG5 register (0x2E). Registers 0x1D – 0x20 and 0x79 – 0x7C are the dedicated transient detection configuration registers. The source register contains directional data to determine the direction of the transient acceleration, either positive or negative. For further information of the embedded transient detection function along with specific application examples and recommended configuration settings, please refer to Freescale application note AN4071.

7.8 Pulse detection

FXOS8700CQ has embedded single/double and directional pulse detection. This function employs several timers for programming the pulse width time and the latency between pulses. The detection thresholds are independently programmable for each axis. The acceleration data input to the pulse detection circuit can be put through both high and low-pass filters, allowing for greater flexibility in discriminating between pulse and tap events. The PULSE_SRC register provides information on the axis, direction (polarity), and single/double event status for the detected pulse or tap. For more information on how to configure the device for pulse detection, please refer to Freescale application note AN4072.

7.9 Orientation detection

FXOS8700CQ has an embedded orientation detection algorithm with the ability to detect all six orientations. The transition angles and hysteresis are programmable, allowing for a smooth transition between portrait and landscape orientations.

The angle at which the device no longer detects the orientation change is referred to as the “Z-lockout angle”. The device operates down to 29° from the flat position. All angles are accurate to ±2°.

For further information on the orientation detection function refer to Freescale application note, AN4068.

7.10 Acceleration Vector Magnitude detection

FXOS8700CQ incorporates an acceleration vector magnitude change detection block that can be configured to generate an interrupt when the acceleration magnitude exceeds a pre-set threshold for a programmed debounce time. The function can be configured to operate in absolute or relative modes, and can also act as a wake to sleep/sleep to wake source. This function is useful for detecting acceleration transients when operated in absolute mode, or for detecting changes in orientation when operated in relative mode.

7.11 Magnetic Vector Magnitude detection

FXOS8700CQ incorporates a magnetic vector magnitude change detection block that can be configured to generate an interrupt when the magnetic field magnitude exceeds a pre-set threshold for a programmed debounce time. The function can be configured to operate in absolute or relative modes, and can also act as a wake to sleep/sleep to wake source.

7.12 Magnetic Threshold detection

FXOS8700CQ incorporates a magnetic threshold event detection block that can be configured to generate an interrupt when the magnetic field on the enabled axes is above or below a programmed threshold.

Two logic combinations are possible for the detection: all of the enabled axes below their respective thresholds (AND condition), or any of the enabled axes above their respective thresholds (OR condition). Even detection may be filtered using a dedicated debounce counter to avoid spurious event detection. The thresholds for each axis are individually programmable and the function can also act as a wake to sleep/sleep to wake source.

7.13 Magnetic Min/Max detection (autonomous calibration)

FXOS8700CQ incorporates a magnetic min/max detection circuit that can be used to automatically track the minimum and maximum field values measured on each of the X, Y, and Z axes. The stored minimum and maximum values may optionally be used to determine the magnetic hard-iron compensation and load the offset registers with the appropriate correction values.

8 Register Map

Table 14. Register Address Map

Name	Type	Register Address	Auto-Increment Address				Default Hex Value	Comment	
			STATUS[*f_mode*] = 00, CTRL_REG1[*f_read*] = 0	STATUS[*f_mode*] > 00, CTRL_REG1[*f_read*] = 0	STATUS[*f_mode*] = 00, CTRL_REG1[*f_read*] = 1	STATUS[*f_mode*] > 00, CTRL_REG1[*f_read*] = 1			
STATUS[1][2]	R	0x00	0x01				0x00	Real-time data-ready status or FIFO status (DR_STATUS or F_STATUS)	
OUT_X_MSB[1][2]	R	0x01	0x02	0x01	0x03	0x01	Data	[7:0] are 8 MSBs of 14-bit sample.	Root pointer to XYZ FIFO data.
OUT_X_LSB[1][2]	R	0x02	0x03		0x00		Data	[7:2] are 6 LSBs of 14-bit real-time sample	
OUT_Y_MSB[1][2]	R	0x03	0x04		0x05	0x00	Data	[7:0] are 8 MSBs of 14-bit real-time sample	
OUT_Y_LSB[1][2]	R	0x04	0x05		0x00		Data	[7:2] are 6 LSBs of 14-bit real-time sample	
OUT_Z_MSB[1][2]	R	0x05	0x06		M_CTRL_REG2[*hyb_autoinc_mode*] = 0 → 0x00, M_CTRL_REG2[*hyb_autoinc_mode*] = 1 → 0x33		Data	[7:0] are 8 MSBs of 14-bit real-time sample	
OUT_Z_LSB[1][2]	R	0x06	M_CTRL_REG2[*hyb_autoinc_mode*] = 0 → 0x00, M_CTRL_REG2[*hyb_autoinc_mode*] = 1 → 0x33				Data	[7:2] are 6 LSBs of 14-bit real-time sample	
Reserved	R	0x07 - 0x08	0x00				0x00	Reserved, reads return 0x00	
F_SETUP[1][3]	R/W	0x09	0x0A				0x00	FIFO setup	
TRIG_CFG	R/W	0x0A	0x0B				0x00	FIFO event trigger configuration register	
SYSMOD[1][2]	R	0x0B	0x0C				Output	Current system mode	
INT_SOURCE[1][2]	R	0x0C	0x0D				Output	Interrupt status	
WHO_AM_I[1]	R	0x0D	0x0E				0xC7	Device ID	
XYZ_DATA_CFG[1][4]	R/W	0x0E	0x0F				0x00	Acceleration dynamic range and filter enable settings	
HP_FILTER_CUTOFF[1][4]	R/W	0x0F	0x10				0x00	Pulse detection high-pass and low-pass filter enable bits. High-pass filter cutoff frequency selection	
PL_STATUS[1][2]	R	0x10	0x11				0x00	Landscape/Portrait orientation status	
PL_CFG[1][4]	R/W	0x11	0x12				0x83	Landscape/Portrait configuration	
PL_COUNT[1][3]	R/W	0x12	0x13				0x00	Landscape/Portrait debounce counter	
PL_BF_ZCOMP[1][4]	R/W	0x13	0x14				0x00	Back/Front Trip angle threshold	
PL_THS_REG[1][4]	R/W	0x14	0x15				0x1A	Portrait to Landscape Trip Threshold angle and hysteresis settings	
A_FFMT_CFG[1][4]	R/W	0x15	0x16				0x00	Freefall/Motion function configuration	
A_FFMT_SRC[1][2]	R	0x16	0x17				0x00	Freefall/Motion event source register	
A_FFMT_THS[1][3]	R/W	0x17	0x18				0x00	Freefall/Motion threshold register	
A_FFMT_COUNT[1][3]	R/W	0x18	0x19				0x00	Freefall/Motion debounce counter	

Table 14. Register Address Map

Reserved	R/W	0x19-0x1C		—	Reserved, reads return 0x00
TRANSIENT_CFG[1][4]	R/W	0x1D	0x1A	0x00	Transient function configuration
TRANSIENT_SRC[1][2]	R	0x1E	0x1B	0x00	Transient event status register
TRANSIENT_THS[1][3]	R/W	0x1F	0x1C	0x00	Transient event threshold
TRANSIENT_COUNT[1][3]	R/W	0x20	0x1D	0x00	Transient debounce counter
PULSE_CFG[1][4]	R/W	0x21	0x22	0x00	Pulse function configuration
PULSE_SRC[1][2]	R	0x22	0x23	0x00	Pulse function source register
PULSE_THSX[1][3]	R/W	0x23	0x24	0x00	X-axis pulse threshold
PULSE_THSY[1][3]	R/W	0x24	0x25	0x00	Y-axis pulse threshold
PULSE_THSZ[1][3]	R/W	0x25	0x26	0x00	Z-axis pulse threshold
PULSE_TMLT[1][4]	R/W	0x26	0x27	0x00	Time limit for pulse detection
PULSE_LTCY[1][4]	R/W	0x27	0x28	0x00	Latency time for second pulse detection
PULSE_WIND[1][4]	R/W	0x28	0x29	0x00	Window time for second pulse detection
ASLP_COUNT[1][4]	R/W	0x29	0x2A	0x00	In activity counter setting for Auto-Sleep
CTRL_REG1[1][4]	R/W	0x2A	0x2B	0x00	System ODR, accelerometer OSR, operating mode
CTRL_REG2[1][4]	R/W	0x2B	0x2C	0x00	Self-Test, Reset, accelerometer OSR and Sleep mode settings
CTRL_REG3[1][4]	R/W	0x2C	0x2D	0x00	Sleep mode interrupt wake enable, interrupt polarity, push-pull/open-drain configuration
CTRL_REG4[1][4]	R/W	0x2D	0x2E	0x00	Interrupt enable register
CTRL_REG5[1][4]	R/W	0x2E	0x2F	0x00	Interrupt pin (INT1/INT2) map
OFF_X[1][4]	R/W	0x2F	0x30	0x00	X-axis accelerometer offset adjust
OFF_Y[1][4]	R/W	0x30	0x31	0x00	Y-axis accelerometer offset adjust
OFF_Z[1][4]	R/W	0x31	0x0D	0x00	Z-axis accelerometer offset adjust
M_DR_STATUS	R	0x32		0x00	Magnetic data ready
M_OUT_X_MSB[1][5]	R	0x33		Data	MSB of 16-bit magnetic data for X-axis
M_OUT_X_LSB[1][5]	R	0x34		Data	LSB of 16-bit magnetic data for X-axis
M_OUT_Y_MSB[1][5]	R	0x35		Data	MSB of 16-bit magnetic data for Y-axis
M_OUT_Y_LSB[1][5]	R	0x36		Data	LSB of 16-bit magnetic data for Y-axis
M_OUT_Z_MSB[1][5]	R	0x37		Data	MSB of 16-bit magnetic data for Z-axis
M_OUT_Z_LSB[1][5]	R	0x38		Data	LSB of 16-bit magnetic data for Z-axis

Table 14. Register Address Map

CMP_X_MSB[1][5]	R	0x39		Data	Bits [13:8] of integrated X-axis accerleration data
CMP_X_LSB[1][5]	R	0x3A		Data	Bits [7:0] of integrated X-axis accerleration data
CMP_Y_MSB[1][5]	R	0x3B		Data	Bits [13:8] of integrated Y-axis accerleration data
CMP_Y_LSB[1][5]	R	0x3C		Data	Bits [7:0] of integrated Y-axis accerleration data
CMP_Z_MSB[1][5]	R	0x3D		Data	Bits [13:8] of integrated Z-axis accerleration data
CMP_Z_LSB[1][5]	R	0x3E		Data	Bits [7:0] of integrated Z-axis accerleration data
M_OFF_X_MSB[6]	R/W	0x3F		0x00	MSB of magnetometer of X-axis offset
M_OFF_X_LSB[6]	R/W	0x40		0x00	LSB of magnetometer of X-axis offset
M_OFF_Y_MSB[6]	R/W	0x41		0x00	MSB of magnetometer of Y-axis offset
M_OFF_Y_LSB[6]	R/W	0x42		0x00	LSB of magnetometer of Y-axis offset
M_OFF_Z_MSB[6]	R/W	0x43		0x00	MSB of magnetometer of Z-axis offset
M_OFF_Z_LSB[6]	R/W	0x44		0x00	LSB of magnetometer of Z-axis offset
MAX_X_MSB[1][6]	R	0x45		Data	Magnetometer X-axis maximum value MSB
MAX_X_LSB[1][6]	R	0x46		Data	Magnetometer X-axis maximum value LSB
MAX_Y_MSB[1][6]	R	0x47		Data	Magnetometer Y-axis maximum value MSB
MAX_Y_LSB[1][6]	R	0x48		Data	Magnetometer Y-axis maximum value LSB
MAX_Z_MSB[1][6]	R	0x49		Data	Magnetometer Z-axis maximum value MSB
MAX_Z_LSB[1][6]	R	0x4A		Data	Magnetometer Z-axis maximum value LSB
MIN_X_MSB[1][6]	R	0x4B		Data	Magnetometer X-axis minimum value MSB
MIN_X_LSB[1][6]	R	0x4C		Data	Magnetometer X-axis minimum value LSB
MIN_Y_MSB[1][6]	R	0x4D		Data	Magnetometer Y-axis minimum value MSB
MIN_Y_LSB[1][6]	R	0x4E		Data	Magnetometer Y-axis minimum value LSB
MIN_Z_MSB[1][6]	R	0x4F		Data	Magnetometer Z-axis minimum value MSB
MIN_Z_LSB[1][6]	R	0x50		Data	Magnetometer Z-axis minimum value LSB
TEMP[1]	R	0x51		Data	Device temperature, valid range of -128 to 127° C
M_THS_CFG[1][4]	R/W	0x52		0x00	Magnetic threshold detection function configuration
M_THS_SRC[1][2]	R	0x53		Data	Magnetic threshold event source register

Table 14. Register Address Map

M_THS_X_MSB[1]	R/W	0x54		0x00	X-axis magnetic threshold MSB
M_THS_X_LSB[1]	R/W	0x55		0x00	X-axis magnetic threshold LSB
M_THS_Y_MSB[1]	R/W	0x56		0x00	Y-axis magnetic threshold MSB
M_THS_Y_LSB[1]	R/W	0x57		0x00	Y-axis magnetic threshold LSB
M_THS_Z_MSB[1]	R/W	0x58		0x00	Z-axis magnetic threshold MSB
M_THS_Z_LSB[1]	R/W	0x59		0x00	Z-axis magnetic threshold LSB
M_THS_COUNT[1][3]	R/W	0x5A		0x00	Magnetic threshold debounce counter
M_CTRL_REG1	R/W	0x5B		0x00	Control for magnetic sensor functions
M_CTRL_REG2	R/W	0x5C		0x00	Control for magnetic sensor functions
M_CTRL_REG3	R/W	0x5D		0x00	Control for magnetic sensor functions
M_INT_SRC	R	0x5E		0x00	Magnetic interrupt source
A_VECM_CFG	R/W	0x5F		0x00	Acceleration vector magnitude configuration register
A_VECM_THS_MSB	R/W	0x60		0x00	Acceleration vector magnitude threshold MSB
A_VECM_THS_LSB	R/W	0x61		0x00	Acceleration vector magnitude threshold LSB
A_VECM_CNT	R/W	0x62		0x00	Acceleration vector magnitude debounce count
A_VECM_INITX_MSB	R/W	0x63		0x00	Acceleration vector magnitude X-axis reference value MSB
A_VECM_INITX_LSB	R/W	0x64		0x00	Acceleration vector magnitude X-axis reference value LSB
A_VECM_INITY_MSB	R/W	0x65		0x00	Acceleration vector magnitude Y-axis reference value MSB
A_VECM_INITY_LSB	R/W	0x66		0x00	Acceleration vector magnitude Y-axis reference value LSB
A_VECM_INITZ_MSB	R/W	0x67		0x00	Acceleration vector magnitude Z-axis reference value MSB
A_VECM_INITZ_LSB	R/W	0x68		0x00	Acceleration vector magnitude Z-axis reference value LSB
M_VECM_CFG	R/W	0x69		0x00	Magnetic vector magnitude configuration register
M_VECM_THS_MSB	R/W	0x6A		0x00	Magnetic vector magnitude threshold MSB
M_VECM_THS_LSB	R/W	0x6B		0x00	Magnetic vector magnitude threshold LSB

Table 14. Register Address Map

M_VECM_CNT	R/W	0x6C		0x00	Magnetic vector magnitude debounce count
M_VECM_INITX_MSB	R/W	0x6D		0x00	Magnetic vector magnitude reference value X-axis MSB
M_VECM_INITX_LSB	R/W	0x6E		0x00	Magnetic vector magnitude reference value X-axis LSB
M_VECM_INITY_MSB	R/W	0x6F		0x00	Magnetic vector magnitude reference value Y-axis MSB
M_VECM_INITY_LSB	R/W	0x70		0x00	Magnetic vector magnitude reference value Y-axis LSB
M_VECM_INITZ_MSB	R/W	0x71		0x00	Magnetic vector magnitude reference value Z-axis MSB
M_VECM_INITZ_LSB	R/W	0x72		0x00	Magnetic vector magnitude reference value Z-axis LSB
A_FFMT_THS_X_MSB	R/W	0x73		0x00	X-axis FMT threshold MSB
A_FFMT_THS_X_LSB	R/W	0x74		0x00	X-axis FFMT threshold LSB
A_FFMT_THS_Y_MSB	R/W	0x75		0x00	Y-axis FFMT threshold MSB
A_FFMT_THS_Y_LSB	R/W	0x76		0x00	Y-axis FFMT threshold LSB
A_FFMT_THS_Z_MSB	R/W	0x77		0x00	Z-axis FFMT threshold MSB
A_FFMT_THS_Z_LSB	R/W	0x78		0x00	Z-axis FFMT threshold LSB
Reserved (do not modify)		0x7D		—	Reserved. Reads return 0x00.

1. Register contents are preserved when transitioning from Active to Standby mode.
2. Register contents are reset when transitioning from Standby to Active mode.
3. Register contents can be modified anytime in Standby or Active mode. A write to this register will cause a reset of the corresponding internal system debounce counter.
4. Modification of this register's contents can only occur when device is in Standby mode, except the FS[1:0] bit fields in CTRL_REG1 register. Hybrid auto-increment mode may be used to read out acceleration and magnetic data from registers x1-x6 using a burst read transaction. When M_CTRL_REG2[*hyb_autoinc_mode*] = 1, the user may do a burst read of 12 bytes starting from OUT_X_MSB (address 0x1) to read out both the current accelerometer and magnetometer data in one contiguous operation.
5. To ensure that valid data is read from these registers, the user must first read the M_OUT_X_MSB register in either burst or single-read mode. Reading of the M_OUT_X_MSB register triggers the update of the M_OUT_X/Y/Z registers with the current time-aligned output data.
6. To ensure that valid data is read from these registers, the user must first read the MSB register of each register pair in either burst or single-read mode. Reading of the LSB register without first reading the MSB register will result in invalid data.

NOTE

Auto-increment addresses which are not a simple increment are highlighted in bold. The auto-increment addressing is only enabled when registers are read using burst read mode when configured for I^2C or SPI. The auto-increment address is cleared in I^2C mode when a stop condition is detected. In SPI mode there is no stop condition and the address is not cleared.

9 Registers by Functional Blocks

9.1 Device configuration

9.1.1 STATUS (0x00) register

DR_STATUS or F_STATUS							
0	0	0	0	0	0	0	0

Figure 10. STATUS register

Table 15. STATUS Description

Field	Description
F_SETUP[*f_mode*] = 0b00	register 0x00 → DR_STATUS
F_SETUP[*f_mode*] > 0b00	register 0x00 → F_STATUS

The STATUS register aliases allow for the contiguous burst read of both status and current acceleration sample/FIFO data using the auto incrementing mechanism in both 8 and 14-bit modes.

9.1.2 DR_STATUS (0x00) register

Data-Ready Status when STATUS = 0x00

This STATUS register provides the acquisition status information on a per-sample basis, and reflects real-time updates to the OUTX, OUTY, and OUTZ registers.

When the FIFO subsystem data output register driver is disabled (F_SETUP[*f_mode*] = 0b00), this register indicates the real-time status information of the X, Y, and Z sample data.

zyxow	zow	yor	xor	zyxdr	zdr	ydr	xdr
0	0	0	0	0	0	0	0

Figure 11. DR_STATUS register

Table 16. DR_STATUS description

Field	Description
zyxow	*zyxow* is set to 1 whenever new data is acquired before completing the retrieval of the previous set. This event occurs when the content of at least one acceleration data register (i.e. OUTX, OUTY, and OUTZ) has been overwritten. *zyxow* is cleared when the high-bytes of the acceleration data (OUTX_MSB, OUTY_MSB, and OUTZ_MSB) are read. X, Y, Z-axis data overwrite. 0: No data overwrite has occurred 1: Previous X, Y, Z data was overwritten by new X, Y, Z data before it was completely read
zow	*zow* is set to 1 whenever a new Z-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. zow is cleared anytime OUTZ_MSB register is read. Z-axis data overwrite. 0: No data overwrite has occurred 1: Previous Z-axis data was overwritten by new Z-axis data before it was read
yow	*yow* is set to 1 whenever a new Y-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. yow is cleared anytime OUTY_MSB register is read. Y-axis data overwrite. 0: No data overwrite has occurred 1: Previous Y-axis data was overwritten by new Y-axis data before it was read

Table 16. DR_STATUS description

xow	*xow* is set to 1 whenever a new X-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. xow is cleared anytime OUTX_MSB register is read. X-axis data overwrite. 0: No data overwrite has occurred 1: Previous X-axis data was overwritten by new X-axis data before it was read
zyxdr	*zyxdr* signals that a new acquisition for any of the enabled channels is available. *zyxdr* is cleared when the high-bytes of the acceleration data (OUTX_MSB, OUTY_MSB, OUTZ_MSB) are read. X, Y, Z-axis new data ready. 0: No new set of data ready 1: New set of data is ready
zdr	*zdr* is set to 1 whenever a new Z-axis data acquisition is completed. *zdr* is cleared anytime the OUTZ_MSB register is read. Z-axis new data available. 0: No new Z-axis data is ready 1: New Z-axis data is ready
ydr	*ydr* is set to 1 whenever a new Y-axis data acquisition is completed. *ydr* is cleared anytime the OUTY_MSB register is read. Y-axis new data available. Default value: 0 0: No new Y-axis data ready 1: New Y-axis data is ready
xdr	*xdr* is set to 1 whenever a new X-axis data acquisition is completed. *xdr* is cleared anytime the OUTX_MSB register is read. X-axis new data available. Default value: 0 0: No new X-axis data ready 1: New X-axis data is ready

9.1.3 F_STATUS (0x00) register

FIFO Status when STATUS > 0x00.

If the FIFO subsystem data output register driver is enabled, the status register indicates the current status information of the FIFO subsystem.

f_ovf	f_wmrk_flag	f_cnt[5:0]
0	0	0

Figure 12. F_STATUS register

Table 17. FIFO flag event descriptions

f_ovf	f_wmrk_flag	Event description
0	X	No FIFO overflow events detected.
1	X	FIFO overflow event detected.
X	0	No FIFO watermark event detected.
X	1	A FIFO Watermark event was detected indicating that a FIFO sample count greater than watermark value has been reached. If F_SETUP[*f_mode*] = 0b11, a FIFO trigger event was detected

The *f_ovf* and *f_wmrk_flag* flags remain asserted while the event source is still active, but the user can clear the FIFO interrupt bit flag in the interrupt source register (INT_SOURCE) by reading the F_STATUS register. In this case, the INT_SOURCE[*src_fifo*] bit will be set again when the next data sample enters the FIFO.

Therefore the *f_ovf* bit flag will remain asserted while the FIFO has overflowed and the *f_wmrk_flag* bit flag will remain asserted while the *f_cnt* value is equal to or greater than then *f_wmrk* value.

Table 18. FIFO sample count bit description

Field	Description
f_cnt[5:0]	These bits indicate the number of acceleration samples currently stored in the FIFO buffer. Count 0b000000 indicates that the FIFO is empty. FIFO sample counter. Default value 0b000000. (0b000001 to 0b100000 indicates 1 to 32 samples stored in FIFO

9.1.4 TRIG_CFG (0x0A) register

FIFO trigger configuration register. After the interrupt flag of the enabled event in TRIG_CFG is set, the FIFO (when configured in Trigger mode) is gated at the time of the interrupt event preventing the further collection of data samples. This allows the host processor to analyze the data leading up to the event detection (up to 32 samples). For detailed information on how to utilize the FIFO and the various trigger events, please see AN4073 available on the Freescale website.

—	—	trig_trans	trig_lndprt	trig_pulse	tria_ffmt	trig_a_vecm	—
0	0	0	0	0	0	0	0

Figure 13. TRIG_CFG register

Table 19. TRIG_CFG bit descriptions

Field	Description
trig_trans	Transient interrupt FIFO trigger enable.
trig_lndprt	Landscape/Portrait orientation interrupt FIFO trigger enable.
trig_pulse	Pulse interrupt FIFO trigger enable
tria_ffmt	Freefall/motion interrupt FIFO trigger enable
trig_a_vecm	Acceleration vector magnitude FIFO trigger enable.

9.1.5 SYSMOD (0x0B) register

fgerr	fgt[4:0]	sysmod[1:0]

Figure 14. SYSMOD register

Table 20. SYSMOD bit description

Field	Description
fgerr	FIFO gate error. Default value: 0. 0: No FIFO gate error detected. 1: FIFO gate error was detected. Emptying the FIFO buffer clears the *fgerr* bit in the SYSMOD register. See CTRL_REG3 [Interrupt CTRL register] (0x2C) for more information on configuring the FIFO Gate function.
fgt[4:0]	Number of ODR time units since *fgerr* was asserted. Reset when *fgerr* is cleared
sysmod[1:0]	System mode. Default value: 0. 00: Standby mode 01: Wake mode 10: Sleep mode

The system mode register indicates the current device operating mode. Applications using the Auto-Sleep/Auto-Wake mechanism should use this register to synchronize their application with the device operating mode. The system mode register also indicates the status of the FIFO gate error flag and the time elapsed since the FIFO gate error flag was asserted.

9.1.6 INT_SOURCE (0x0C) register

Interrupt source register. The bits that are set (logic ‘1’) indicate which function has asserted its interrupt and conversely bits that are cleared (logic ‘0’) indicate which function has not asserted its interrupt. Additional interrupt flags for magnetic interrupt events are located in the M_INT_SRC register (0x5E).

Reading the INT_SOURCE register does not clear any interrupt status bits (except src_a_vecm, see below); the respective interrupt flag bits are reset by reading the appropriate interrupt source register for the function that generated the interrupt.

src_aslp	src_fifo	src_trans	src_lndprt	src_pulse	src_ffmt	src_a_vecm	src_drdy

Figure 15. INT_SOURCE register

Table 21. INT_SOURCE bit descriptions

Field	Description
src_aslp	Auto-Sleep/Wake interrupt status bit: logic ‘1’ indicates that an interrupt event that can cause a Wake to Sleep or Sleep to Wake system mode transition has occurred and logic ‘0’ indicates that no Wake to Sleep or Sleep to Wake system mode transition interrupt event has occurred. The “Wake-to-Sleep” transition occurs when a period of inactivity that exceeds the user specified time limit (ASLP_COUNT) has been detected, thus causing the system to transition to a user specified low ODR setting. A “Sleep-to-Wake” transition occurs when the user specified interrupt event has awakened the system, thus causing the system to transition to the user specified higher ODR setting. Reading the SYSMOD register will clear the *src_aslp* bit.
src_fifo	FIFO interrupt status bit: logic ‘1’ indicates that a FIFO interrupt event such as an overflow or watermark (F_STATUS[*f_cnt*] = F_STATUS[*f_wmrk*]) event has occurred and logic ‘0’ indicates that no FIFO interrupt event has occurred. This bit is cleared by reading the F_STATUS register.
src_trans	Transient interrupt status bit: logic ‘1’ indicates that an acceleration transient value greater than user specified threshold has occurred. and logic ‘0’ indicates that no transient event has occurred. This bit is asserted whenever TRANSIENT_SRC[*ea*] is asserted and the functional block interrupt has been enabled. This bit is cleared by reading the TRANSIENT_SRC register.
src_lndprt	Landscape/Portrait orientation interrupt status bit: logic ‘1’ indicates that an interrupt was generated due to a change in the device orientation status and logic ‘0’ indicates that no change in orientation status was detected. This bit is asserted whenever PL_STATUS[*newlp*] is asserted and the functional block interrupt has been enabled. This bit is cleared by reading the PL_STATUS register.
src_pulse	Pulse interrupt status bit: logic ‘1’ indicates that an interrupt was generated due to single and/or double pulse event and logic ‘0’ indicates that no pulse event was detected. This bit is asserted whenever PULSE_SRC[*ea*] is asserted and the functional block interrupt has been enabled. This bit is cleared by reading the PULSE_SRC register.
src_ffmt	Freefall/motion interrupt status bit: logic ‘1’ indicates that the freefall/motion function interrupt is active and logic ‘0’ indicates that no freefall or motion event was detected. This bit is asserted whenever PULSE_SRC[*ea*] is asserted and the functional block interrupt has been enabled. This bit is cleared by reading the A_FFMT_SRC register.
src_a_vecm	Accelerometer vector magnitude interrupt status bit: logic ‘1’ indicates that an interrupt was generated due to acceleration vector magnitude function and logic ‘0’ indicates that no interrupt has been generated. This bit is cleared by reading this register (INT_SOURCE).
src_drdy	Data-ready interrupt status bit. In acceleration only mode this bit indicates that new accelerometer data is available to read. In magnetometer only mode, *src_drdy* indicates that new magnetic data is available to be read. In hybrid mode, this bit signals that new acceleration and/or magnetic data is available. The *src_drdy* interrupt is cleared by reading out the acceleration data in accelerometer only mode and by reading out the magnetic data in magnetometer only or hybrid modes. In hybrid mode and with M_CTRL_REG2[*hyb_autoinc_mode*] = 1, all of the sensor data can be read out in a 12 byte burst read starting at register 0x01 (OUT_X_MSB).

9.1.7 WHO_AM_I (0x0D) register

who_am_i[7:0]
0xC7

Figure 16. WHO_AM_I register

Device identification register. This register contains the device identifier which is set to 0xC4 for preproduction devices and 0xC7 for production devices.

9.1.8 CTRL_REG1 (0x2A) register

Note: Except for Standby mode selection, the device must be in Standby mode to change any of the fields within CTRL_REG1 (0x2A).

aslp_rate[1:0]	dr[2:0]	lnoise	f_read	active
0	0b001	0	0	0

Figure 17. CTRL_REG1 register

Table 22. CTRL_REG1 bit descriptions

Field	Description
aslp_rate[1:0]	Configures the auto-wake sample frequency when the device is in Sleep mode. See Table 22 for more information.
dr[2:0]	Output Data Rate (ODR) selection. See Table 23 for more information.
lnoise	Reduced noise and full-scale range mode (analog gain times 2). 0: Normal mode 1: Reduced noise mode; Note that the FSR setting is restricted to a ±4g in this mode (lnoise = 1).
f_read	Fast-read mode: Data format is limited to the 8-bit MSB for both magnetometer and accelerometer output data. The address pointer will skip over the LSB addresses for each axes sample data when performing a burst read operation. 0: Normal mode 1: Fast-read mode
active	Standby/Active. 0: Standby mode 1: Active mode

Table 23. Sleep mode poll rate description

aslp_rate1	aslp_rate0	Frequency (Hz)
0	0	50
0	1	12.5
1	0	6.25
1	1	1.56

It is important to note that when the device is in Auto-Sleep mode, the system ODR and data rate for all the system functional blocks is overridden by the sleep data rate set by the aslp_rate field. When hybrid mode is enabled, the frequency is one-half of what is shown in Table 22. For example, with aslp_rate = 0b00 the frequency is 25 Hz.

Table 24 shows the various system output data rates (ODR) that may be selected using the dr[2:0] bits. The selected ODR is reduced by a factor of two when the device is operated in hybrid mode.

Table 24. System Output Data Rate selection

dr2	dr1	dr0	ODR accelerometer or magnetometer only modes (Hz)	Period accelerometer or magnetometer only modes (ms)	ODR hybrid mode (Hz)	Period hybrid mode (ms)
0	0	0	800.0	1.25	400	2.5
0	0	1	400.0	2.5	200	5
0	1	0	200.0	5	100	10
0	1	1	100.0	10	50	20
1	0	0	50.0	20	25	80
1	0	1	12.5	80	6.25	160
1	1	0	6.3	160	3.15	320
1	1	1	1.6	640	0.8	1280

The *active* bit selects between Standby mode and Active mode. The default value is 0 (Standby mode) on reset.

The *lnoise* bit selects between normal full dynamic range mode and a high sensitivity, low-noise mode. In low-noise mode the maximum signal that can be measured is ±4g. Note: Any thresholds set above 4g will not be reached.

The *f_read* bit selects between normal and fast-read modes where the auto-increment counter will also skip over the LSB data bytes when *f_read* = 1. Data read from the FIFO will also skip over the LSB data, reducing the data acquisition time. In hybrid mode and with M_CTRL_REG2[*hyb_autoinc_mode*] = 1, all of the sensor data MSB's can be read out with a single 6-byte burst read starting at the OUT_X_MSB register. Note: The *f_read* bit can only be changed while F_SETUP[*f_mode*] = 0

9.1.9 CTRL_REG2 (0x2B) register

st	rst	—	smods[1:0]	slpe	mods[1:0]
0	0	0	0	0	0

Figure 18. CTRL_REG2 register

Table 25. CTRL_REG2 bit descriptions

Field	Description
st	The *st* bit activates the accelerometer self-test function. When *st* is set to 1, an output change will occur to the device outputs thus allowing the host application to check the functionality of the entire measurement signal chain. Self-Test Enable: 0: Self-Test disabled 1: Self-Test enabled.
rst	The *rst* bit is used to initiate a software reset. The reset mechanism can be enabled in both Standby and Active modes. When the *rst* bit is set, the boot mechanism resets all functional block registers and loads the respective internal registers with their default values. After setting the *rst* bit, the system will automatically transition to Standby mode. Therefore, if the system was already in Standby mode, the reboot process will immediately begin; else if the system was in Active mode the boot mechanism will automatically transition the system from Active mode to Standby mode, only then can the reboot process begin. A system reset can also be initiated by pulsing the external RST pin high. The I^2C and SPI communication systems are also reset to avoid corrupted data transactions. The host application should allow 1 ms between issuing a software (setting *rst* bit) or hardware (pulsing RST pin) reset and attempting communications with the device over the I^2C or SPI interfaces. At the end of the boot process the *rst* bit is deasserted to 0. Reading this bit will always return a value of 0. 0: Device reset disabled 1: Device reset enabled.
smods[1:0]	Sleep mode power scheme selection. See Table 25 for more information.
slpe[(1)]	Auto-Sleep mode enable: 0: Auto-Sleep is not enabled 1: Auto-Sleep is enabled.
mods[1:0]	Accelerometer OSR selection. This setting, along with the ODR selection determines the Active mode power and RMS noise for acceleration measurements. See Table 25 for more information.

1. When SLPE = 1, a transition between Sleep mode and Wake mode results in a FIFO flush and a reset of internal functional block counters. All functional block status information is preserved except where otherwise stated. For further information, refer to the CRTL_REG3 register description (FIFO_GATE bit).

Table 26. CTRL_REG2[mods] oversampling modes

(s)mods1	(s)mods0	Power mode
0	0	Normal
0	1	Low Noise, Low Power
1	0	High Resolution
1	1	Low Power

Table 27. Current Consumption versus Oversampling

Mode	Normal		Low noise, Low power		High resolution		Low power	
ODR	Current μA	OS ratio	Current μA	OS ratio	Current μA	OS ratio	Current μA	OS ratio
1.5625	37	128	8	32	245	1024	7	16
6.25	37	32	11	8	245	256	9	4
12.5	37	16	14	4	245	128	11	2
50	37	4	37	4	245	32	22	2
100	67	4	67	4	245	16	37	2
200	126	4	126	4	245	8	67	2
400	245	4	245	4	245	4	126	2
800	245	2	245	2	245	2	245	2

9.1.10 CTRL_REG3 [Interrupt Control Register] (0x2C) register

fifo_gate	wake_trans	wake_lndprt	wake_pulse	wake_ffmt	wake_en_a_vecm	ipol	pp_od
0	0	0	0	0	0	0	0

Figure 19. CTRL_REG3 register

Table 28. CTRL_REG3 bit descriptions

Field	Description
fifo_gate	0: FIFO gate is bypassed. FIFO is flushed upon the system mode transitioning from Wake-to-Sleep mode or from Sleep-to-Wake mode. 1: The FIFO input buffer is blocked when transitioning from “Wake-to-Sleep” mode or from “Sleep-to-Wake” mode until the FIFO is flushed.(1) Although the system transitions from “Wake-to-Sleep” or from “Sleep-to-Wake” the contents of the FIFO buffer are preserved, new data samples are ignored until the FIFO is emptied by the host application. If the FIFO_GATE bit is set to logic ‘1’ and the FIFO buffer is not emptied before the arrival of the next sample, then the SYSMOD[*fgerr*] will be asserted. The SYSMOD[*fgerr*] bit remains asserted as long as the FIFO buffer remains un-emptied. Emptying the FIFO buffer clears the SYS_MOD[*fgerr*] register.
wake_tran	0: Transient function is disabled in Sleep mode 1: Transient function is enabled in Sleep mode and can generate an interrupt to wake the system
wake_lndprt	0: Orientation function is disabled Sleep mode. 1: Orientation function is enabled in Sleep mode and can generate an interrupt to wake the system
wake_pulse	0: Pulse function is disabled in Sleep mode 1: Pulse function is enabled in Sleep mode and can generate an interrupt to wake the system
wake_ffmt	0: Freefall/motion function is disabled in Sleep mode 1: Freefall/motion function is enabled in Sleep mode and can generate an interrupt to wake the system
wake_en_a_vecm	0: Acceleration vector magnitude function is disabled in Sleep mode 1: Acceleration vector magnitude function is enabled in Sleep mode and can generate an interrupt to wake the system

Table 28. CTRL_REG3 bit descriptions

ipol	The *ipol* The bit selects the logic polarity of the interrupt signals output on the INT1 and INT2 pins. INT1/INT2 interrupt logic polarity: 0: Active low (default) 1: Active high
pp_od	INT1/INT2 push-pull or open-drain output mode selection. The open-drain configuration can be used for connecting multiple interrupt signals on the same interrupt line but will require an external pullup resistor to function correctly. 0: Push-pull (default) 1: Open-drain

1. The FIFO contents are flushed whenever the system ODR changes in order to prevent the mixing of FIFO data from different time domains.

The wake enable bits for the magnetic threshold and magnetic vector magnitude functions are located in registers 0x52 (MAG_THS_CFG) and 0x69 (M_VECM_CFG), respectively.

9.1.11 CTRL_REG4 [Interrupt Enable Register] (0x2D) register

int_en_aslp	int_en_fifo	int_en_trans	int_en_lndprt	int_en_pulse	int_en_ffmt	int_en_a_vecm	int_en_drdy
0	0	0	0	0	0	0	0

Figure 20. CTRL_REG4 register

Table 29. Interrupt Enable Register bit descriptions

Field	Description
int_en_aslp	Sleep interrupt enable 0: Auto-Sleep/Wake interrupt disabled 1: Auto-Sleep/Wake interrupt enabled
int_en_fifo	FIFO interrupt enable 0: FIFO interrupt disabled 1: FIFO interrupt enabled
int_en_trans	Transient interrupt enable 0: Transient interrupt disabled 1: Transient interrupt enabled
int_en_lndprt	Orientation interrupt enable 0: Orientation (Landscape/Portrait) interrupt disabled 1: Orientation (Landscape/Portrait) interrupt enabled
int_en_pulse	Pulse interrupt enable 0: Pulse detection interrupt disabled 1: Pulse detection interrupt enabled
int_en_ffmt	Freefall/motion interrupt enable 0: Freefall/motion interrupt disabled 1: Freefall/motion interrupt enabled
int_en_a_vecm	Acceleration vector magnitude interrupt enable 0: Acceleration vector magnitude interrupt disabled 1: Acceleration vector magnitude interrupt enabled
int_en_drdy	Data-ready interrupt enable 0: Data-ready interrupt disabled 1: Data-ready interrupt enabled

The corresponding functional block interrupt enable bit allows the functional block to route its event detection flag to the system's interrupt controller. The interrupt controller routes the enabled interrupt signals to either the INT1 or INT2 pins depending on the settings made in CTRL_REG5. Please note that the interrupt enable bits for the magnetic threshold and vector magnitude interrupts are located in registers 0x52 (MAG_THS_CFG), and 0x69 (M_VECM_CFG), respectively.

9.1.12 CTRL_REG5 [Interrupt Routing Configuration Register] (0x2E) register

int_cfg_aslp	int_cfg_fifo	int_cfg_trans	int_cfg_lndprt	int_cfg_pulse	int_cfg_ffmt	int_cfg_a_vecm	int_cfg_drdy
0	0	0	0	0	0	0	0

Figure 21. CTRL_REG5 register

Table 30. Interrupt Routing Configuration bit descriptions

Field	Description
int_cfg_aslp	Sleep interrupt routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
int_cfg_fifo	FIFO interrupt routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
int_cfg_trans	Transient detection interrupt routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
int_cfg_lndprt	Orientation detection interrupt routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
int_cfg_pulse	Pulse detection interrupt routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
int_cfg_ffmt	Freefall/motion detection interrupt routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin
int_cfg_a_vecm	Acceleration vector magnitude interrupt routing 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin.
int_cfg_drdy	INT1/INT2 configuration. 0: Interrupt is routed to INT2 pin 1: Interrupt is routed to INT1 pin.

Please note that the routing configuration for the magnetic threshold interrupt is controlled by *m_ths_int_cfg* bit located in register 0x52 (MAG_THS_CFG), and the magnetic vector magnitude function routing is controlled by *m_vecm_int_cfg* bit in register 0x69 (M_VECM_CFG).

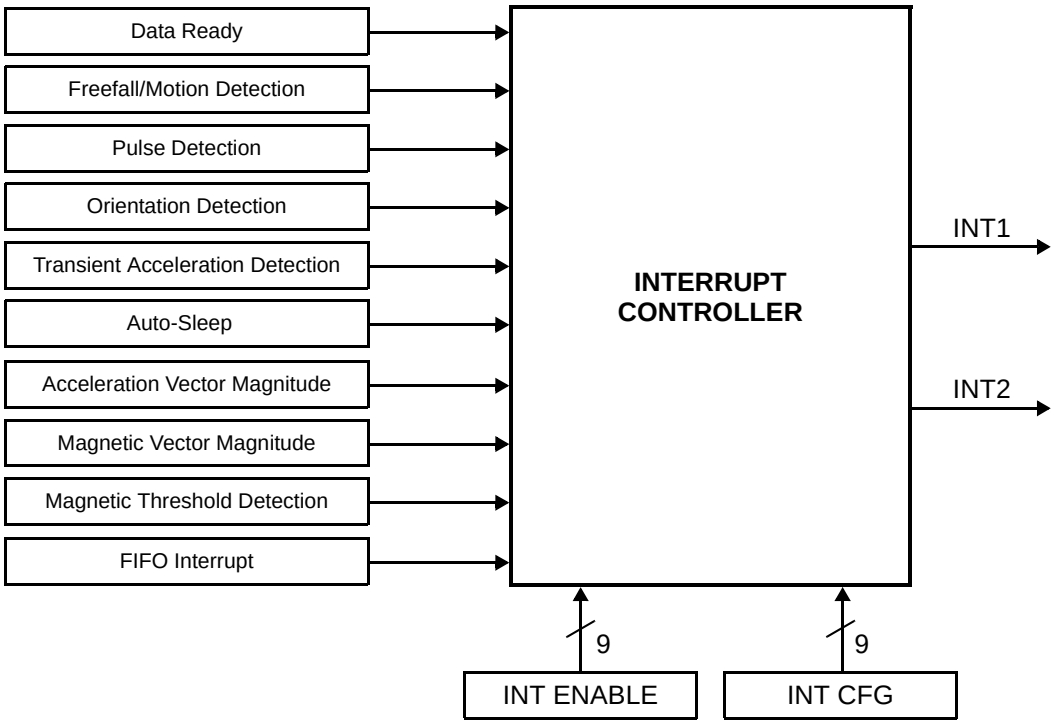


Figure 22. Interrupt controller block diagram

The system's interrupt controller uses the corresponding bit field in the CTRL_REG5 register to determine the routing for the INT1 and INT2 interrupt pins. For example, if the *int_cfg_drdy* bit value is logic '0' the functional block's interrupt is routed to INT2, and if the bit value is logic '1' then the interrupt is routed to INT1. All interrupt signals routed to either INT1 or INT2 are logically ored together as illustrated in Figure 23, thus one or more functional blocks can assert an interrupt pin simultaneously; therefore a host application responding to an interrupt should read the INT_SOURCE register to determine the appropriate sources of the interrupt(s).

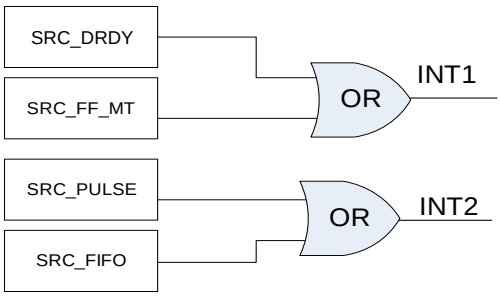


Figure 23. INT1/INT2 PIN Control Logic

9.2 Auto-Sleep trigger

9.2.1 ASLP_COUNT (0x29) register

The ASLP_COUNT register sets the minimum time period of event flag inactivity required to initiate a change from the current active mode ODR value specified in CTRL_REG1[*dr*] to the Sleep mode ODR value specified in CTRL_REG1[*aslp_rate*], provided that CTRL_REG2[*slpe*] = 1.

See Table 32 for functional blocks that may be monitored for inactivity in order to trigger the return-to-sleep event.

aslp_cnt[7:0]
0b00000000

Figure 24. ASLP_COUNT register

Table 31. ASLP_COUNT bit description

Field	Description
aslp_cnt[7:0]	See Table 31 for details

Table 32. ASLP_COUNT relationship with ODR

Output Data Rate (ODR)	Duration (s)	ODR time step (ms)	ASLP_COUNT step (ms)
800	0 to 81	1.25	320
400	0 to 81	2.5	320
200	0 to 81	5	320
100	0 to 81	10	320
50	0 to 81	20	320
12.5	0 to 81	80	320
6.25	0 to 81	160	320
1.56	0 to 163	640	640

Please note that when the device is operated in hybrid mode, the effective ODR is half of what is selected in CTRL_REG1[*dr*]. For example, with ODR = 800 Hz and the device set to hybrid mode, the ASLP_COUNT time step becomes 640 ms.

Table 33. Sleep/Wake mode gates and triggers

Interrupt source	Event restarts time and delays Return-to-Sleep	Event will Wake-from-Sleep
SRC_FIFO	Yes	No
SRC_TRANS	Yes	Yes
SRC_LNDPRT	Yes	Yes
SRC_PULSE	Yes	Yes
SRC_FFMT	Yes	Yes
SRC_ASLP	No*	No*
SRC_Mag	Yes	Yes
SRC_DRDY	No	No
SRC_AVECM	Yes	Yes
SRC_MVECM	Yes	Yes
SRC_MTHS	Yes	Yes

* If the FIFO_GATE bit is set to logic '1', the assertion of the SRC_ASLP interrupt does not prevent the system from transitioning to Sleep or from Wake mode; instead it prevents the FIFO buffer from accepting new sample data until the host application flushes the FIFO buffer.

The interrupt sources listed in Table 33 affect the auto-sleep, return to sleep and wake from sleep mechanism only if they have been previously enabled. The functional block event flags that are bypassed while the system is in Auto-Sleep mode are temporary disabled *(see CTRL_REG3 register for more information)* and are automatically re-enabled when the device returns from Auto-Sleep mode (i.e. wakes up), except for the data ready function.

If any of the interrupt sources listed under the Return-to-Sleep column is asserted before the sleep counter reaches the value specified in ASLP_COUNT, then all sleep mode transitions are terminated and the internal sleep counter is reset. If none of the interrupts listed under the Return-to-Sleep column are asserted within the time limit specified by the ASLP_COUNT register, the system will transition to the Sleep mode and use the ODR value specified in CTRL_REG1[*aslp_rate*].

If any of the interrupt sources listed under the “Wake-from-Sleep” column is asserted, then the system will transition out of the low sample rate Auto-Sleep mode to the user specified fast sample rate provided the user specified wake event function is enabled in register CTRL_REG3.

If the Auto-Sleep interrupt is enabled, a transition from Active mode to Sleep mode and vice-versa will generate an interrupt.

If CTRL_REG3[*fifo_gate*] = 1, transitioning to Auto-Sleep mode will preserve the FIFO contents, set SYSMOD[*fgerr*] (FIFO Gate error), and stop new acquisitions. The system will wait for the FIFO buffer to be emptied by the host application before new samples can be acquired.

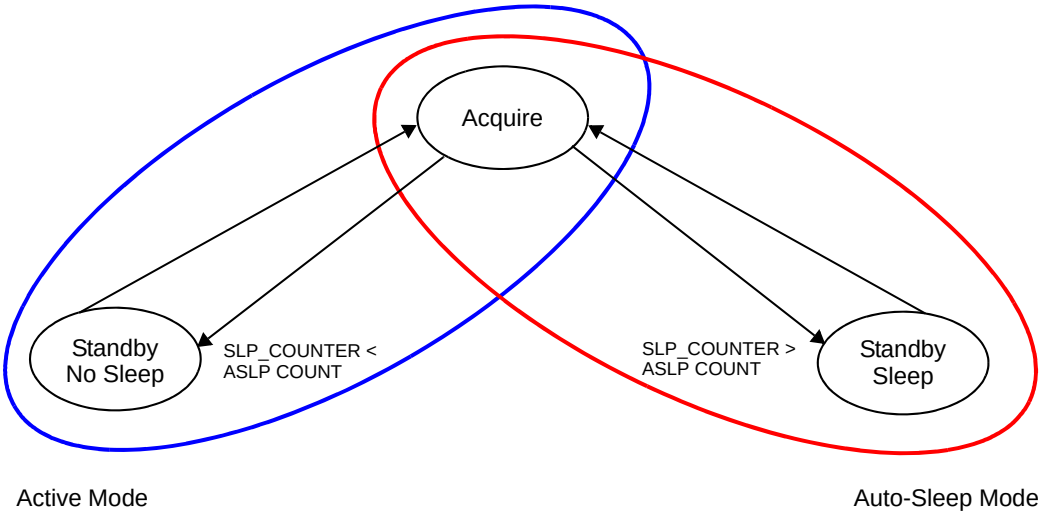


Figure 25. Auto-Sleep state transition diagram

9.3 Temperature

9.3.1 TEMP (0x51) register

8-bit 2’s compliment sensor temperature value with 0.96°C/LSB resolution. Temperature data is only valid between -40°C and 125°C.

die_temperature[7:0]

Figure 26. TEMP register

9.4 Accelerometer output data registers

9.4.1 OUT_X_MSB (0x01), OUT_X_LSB (0x02), OUT_Y_MSB (0x03), OUT_Y_LSB (0x04), OUT_Z_MSB (0x05), OUT_Z_LSB (0x06) registers

These registers contain the X-axis, Y-axis, and Z-axis 14-bit left-justified sample data expressed as 2's complement numbers.

The sample data output registers store the current sample data if the FIFO buffer function is disabled, but if the FIFO buffer function is enabled the sample data output registers then point to the head of the FIFO buffer which contains up to the previous 32 X, Y, and Z data samples.

The data is read out in the following order: Xmsb, Xlsb, Ymsb, Ylsb, Zmsb, Zlsb for CTRL_REG1[*f_read*] = 0, and Xmsb, Ymsb, Zmsb for CTRL_REG1[*f_read*] = 1. If the device is operating in hybrid mode and M_CTRL_REG2[*hyb_autoinc_mode*] = 1, The data read out order is acceleration Xmsb, Xlsb, Ymsb, Ylsb, Zmsb, and Zlsb followed by magnetic data Xmsb, Xlsb, Ymsb, Ylsb, Zmsb, Zlsb. Similarly, for CTRL_REG1[*f_read*] = 1, only the MSB's of the acceleration and magnetic data are read out in the same axis order.

If the CTRL_REG1[*f_read*] bit is set, auto increment will skip over the LSB registers. This will shorten the data acquisition from 7 bytes to 4 bytes, If the LSB registers are directly addressed, the LSB information can still be read regardless of the CTRL_REG1[*f_read*] register setting.

If the FIFO data output register driver is enabled (F_SETUP[*f_mode*] > 00), register 0x01 points to the head of the FIFO buffer, while registers 0x02, 0x03, 0x04, 0x05, 0x06 return a value of zero when read directly.

The DR_STATUS registers, OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB are stored in the auto-incrementing address range of 0x00 to 0x06, allowing all of the acceleration data to be read in a single burst read of 6 bytes starting at the OUT_X_MSB register. If the device is operating in hybrid mode and M_CTRL_REG2[*hyb_autoinc_mode*] = 1, the magnetometer data can also be read out in the same axis and endian order by executing a burst read of 12 bytes starting at register OUT_X_MSB.

xd[13:6]

Figure 27. OUT_X_MSB register

xd[5:0]	—	—

Figure 28. OUT_X_LSB register

yd[13:6]

Figure 29. OUT_Y_MSB register

yd[5:0]	—	—

Figure 30. OUT_Y_LSB register

zd[13:6]

Figure 31. OUT_Z_MSB register

zd[5:0]	—	—

Figure 32. OUT_Z_LSB register

9.5 Accelerometer FIFO

9.5.1 F_SETUP (0x09) register

f_mode[1:0]	f_wmrk[5:0]
0	0

Figure 33. F_SETUP register

Table 34. F_SETUP bit descriptions

Field	Description
f_mode[1:0](1)(2)(3)	FIFO buffer operating mode. **00:** FIFO is disabled. **01:** FIFO contains the most recent samples when overflowed (circular buffer). Oldest sample is discarded to be replaced by new sample. **10:** FIFO stops accepting new samples when overflowed. **11:** FIFO trigger mode. The FIFO is flushed whenever the FIFO is disabled, during an automatic ODR change (Auto-Wake/Sleep), or on a transition from Standby mode to Active mode. Disabling the FIFO (*f_mode* = 0b00) resets the F_STATUS[*f_ovf*], F_STATUS[*f_wmrk_flag*], F_STATUS[*f_cnt*] status flags to zero. A FIFO overflow event (i.e. F_STATUS[*f_cnt]* = 32) will assert the F_STATUS[*f_ovf*] flag.
f_wmrk[5:0](2)	FIFO sample count watermark. These bits set the number of FIFO samples required to trigger a watermark interrupt. A FIFO watermark event flag F_STATUS[*f_wmk_flag*] is raised when FIFO sample count F_STATUS[*f_cnt]* value is equal to or greater than the *f_ wmrk* watermark. Setting the *f_wmrk* to 0b000000 will disable the FIFO watermark event flag generation. This field is also used to set the number of pre-trigger samples in trigger mode (*f_mode* = 0b11).

1. This bit field can be written in Active mode.
2. This bit field can be written in Standby mode.
3. The FIFO mode (*f_mode*) cannot be switched between operational modes (01, 10 and 11).

A FIFO sample count exceeding the watermark event does not stop the FIFO from accepting new data.

The FIFO update rate is dictated by the selected system ODR. In Active mode the ODR is set by CTRL_REG1[*dr*] and when Auto-Sleep is active, the ODR is set by CTRL_REG1[*aslp_rate*] bit fields.

When data is read from the FIFO buffer, the oldest sample data in the buffer is returned and also deleted from the front of the FIFO, while the FIFO sample count is decremented by one. It is assumed that the host application will use the I^2C or SPI burst read transactions to dump the FIFO contents. If the FIFO X, Y, and Z data is not completely read in one burst read transaction, the next read will start at the next FIFO location X-axis data. If the Y or Z data is not read out in the same burst transaction as the X-axis data, it will be lost.

In Trigger mode, the FIFO is operated as a circular buffer and will contain up to the 32 most recent acceleration data samples. The oldest sample is discarded and replaced by the current sample, until a FIFO trigger event occurs. After a trigger event occurs, the FIFO will continue to accept samples only until overflowed, after which point the newest sample data is discarded. For more information on using the FIFO buffer and the various FIFO operating modes, please refer to Freescale application note AN4073.

9.6 Accelerometer sensor data configuration

9.6.1 XYZ_DATA_CFG (0x0E) register

The XYZ_DATA_CFG register is used to configure the desired acceleration full-scale range, and also to select whether the output data is passed through the high-pass filter.

—	—	—	hpf_out	—	—	fs[1:0]
0	0	0	0	0	0	0

Figure 34. XYZ_DATA_CFG register

Table 35. XYZ_DATA_CFG bit descriptions

Field	Description
hpf_out	Enable high-pass filter on acceleration output data 1: Output data is high-pass filtered 0: High-pass filter is disabled.
fs[1:0]	Accelerometer full-scale range selection. See Table 35

Table 36.

fs[1]	fs[0]	Full-Scale range
0	0	±0.244 mg/LSB
0	1	±0.488 mg/LSB
1	0	±0.976 mg/LSB
1	1	Reserved

9.7 Accelerometer High-Pass filter

9.7.1 HP_FILTER_CUTOFF (0x0F) register

High-pass filter cutoff frequency setting register.

—	—	pulse_hpf_byp	pulse_lpf_en	—	—	sel[1:0]
0	0	0	0	0	0	0

Figure 35. HP_FILTER_CUTOFF register

Table 37. HP_FILTER_CUTOFF bit descriptions

Field	Description
pulse_hpf_byp	Bypass high-pass filter for pulse processing function 0: HPF enabled for pulse processing 1: HPF bypassed for pulse processing
pulse_lpf_en	Enable low-pass filter for pulse processing function 0: LPF disabled for pulse processing 1: LPF enabled for pulse processing
sel[1:0]	HPF cutoff frequency selection See Table 37.

Table 38. HP_FILTER_CUTOFF

High-Pass cutoff frequency (Hz)								
ODR (Hz)	sel = 0b00				sel = 0b01			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	16	16	16	16	8	8	8	8
400	16	16	16	8	8	8	8	4
200	8	8	16	4	4	4	8	2
100	4	4	16	2	2	2	8	1
50	2	2	16	1	1	1	8	0.5
12.5	2	0.5	16	0.25	1	0.25	8	0.125
6.25	2	0.25	16	0.125	1	0.125	8	0.063
1.56	2	0.063	16	0.031	1	0.031	8	0.016
ODR (Hz)	sel = 0b10				sel = 0b11			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	4	4	4	4	2	2	2	2
400	4	4	4	2	2	2	2	1
200	2	2	4	1	1	1	2	0.5
100	1	1	4	0.5	0.5	0.5	2	0.25
50	0.5	0.5	4	0.25	0.25	0.25	2	0.125

Table 38. HP_FILTER_CUTOFF

12.5	0.5	0.125	4	0.063	0.25	0.063	2	0.031
6.25	0.5	0.063	4	0.031	0.25	0.031	2	0.016
1.56	0.5	0.016	4	0.008	0.25	0.008	2	0.004

Please note that when the part is operated in hybrid mode, the ODR is reduced by a factor of two, which also affects the filter cutoff frequency. For example, an ODR setting of 400 Hz in accelerometer only mode with HP_FILTER_CUTOFF[*sel*] = 0b10 sets the cutoff frequency at 4 Hz. If the part is operated in Hybrid mode, the effective ODR becomes 200 Hz and the cutoff frequency is now 2 Hz for the same ODR and HP_FILTER_CUTOFF[*sel*] settings.

9.8 Portrait/Landscape Detection

The FXOS8700CQ is capable of detecting six orientations: Landscape Left, Landscape Right, Portrait Up, and Portrait Down with Z-lockout feature as well as Face Up and Face Down orientation as shown in Figures 36**,** 37 and 38. For more details on the meaning of the different user configurable settings and for example code, please refer to Freescale application note AN4068.

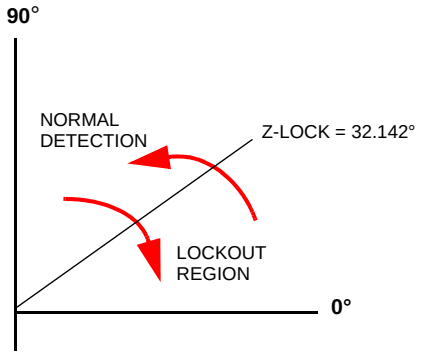


Figure 36. Illustration of Z-tilt angle lockout transition

.

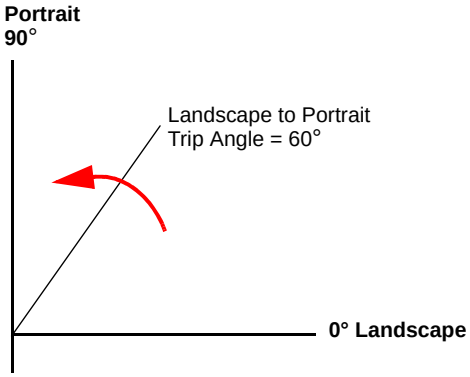


Figure 37. Illustration of landscape to portrait transition

.

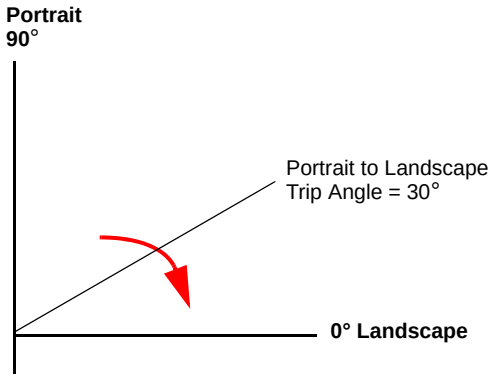


Figure 38. Illustration of portrait to landscape transition

9.8.1 PL_STATUS (0x10) register

This status register can be read to get updated information on any change in orientation by reading bit 7, or the specifics of the orientation by reading the other bits. For further understanding of Portrait Up, Portrait Down, Landscape Left, Landscape Right, Back and Front orientations please refer to Figure 38. The interrupt is cleared when reading the PL_STATUS register.

newlp	lo	—	—	—	lapo[1:0]	bafro
0	0	0	0	0	0	0

Figure 39. PL_STATUS register

Table 39. PL_STATUS bit descriptions

Field	Description
newlp	Landscape/Portrait status change flag. 0: No change 1: BAFRO and/or LAPO and/or Z-tilt lockout value has changed
lo	Z-tilt angle lockout. 0: Lockout condition has not been detected. 1: Z-tilt lockout trip angle has been exceeded. Lockout condition has been detected.
bafro	Back or front orientation. 0: Front: equipment is in the front facing orientation. 1: Back: equipment is in the back facing orientation.
lapo[1:0](1)	Landscape/Portrait orientation. 00: Portrait up: equipment standing vertically in the normal orientation 01: Portrait down: equipment standing vertically in the inverted orientation 10: Landscape right: equipment is in landscape mode to the right 11: Landscape left: equipment is in landscape mode to the left.

1. The default power up state is bafro(Undefined), lapo(Undefined), and no lockout for orientation function.

The *newlp* bit is set to 1 after the first orientation detection after a Standby to Active transition, and whenever a change in *lo*, *bafro*, or *lapo* occurs. The *newlp* bit is cleared anytime the PL_STATUS register is read. *lapo, bafro* and *lo* continue to change when *newlp* is set. The current orientation is locked if the absolute value of the acceleration experienced on any of the three axes is greater than 1.25g.

9.8.2 PL_CFG (0x11) register

This register enables the Portrait/Landscape function and sets the behavior of the debounce counter.

dbcntm	pl_en	—	—	—	—	—	—
1	0	0	0	0	0	1	1

Figure 40. PL_CFG register

Table 40. PL_CFG bit descriptions

Field	Description
dbcntm	Debounce counter mode selection. 0: Decrements debounce whenever condition of interest is no longer valid. 1: Clears counter whenever condition of interest is no longer valid.
pl_en	Portrait/Landscape detection enable. 0: Portrait/Landscape detection is disabled. 1: Portrait/Landscape detection is enabled.

9.8.3 PL_COUNT (0x12) register

This register sets the debounce count for the orientation state transition. The minimum debounce latency is determined by the system ODR value and the value of the PL_COUNT register. Any change to the system ODR or a transition from Active to Standby (or vice-versa) resets the internal landscape/portrait internal debounce counters. When the device is operated in hybrid mode, the effective ODR will be half of what is selected by the user, which will also affect the debounce time. For example, if an ODR of 400 Hz is selected and the part is also in hybrid mode, the effective ODR is 200 HZ, and the effective debounce time step is 5 ms instead of 2.5 ms

dbnce[7:0]
0

Figure 41. PL_COUNT register

Table 41. PL_Count Relationship with the ODR

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	40.8	0.638	40.8	20	160	2.5	160
1.56	5.1	163	0.638	163	20	640	2.5	640

9.8.4 PL_BF_ZCOMP (0x13) register

Back/Front and Z-tilt angle compensation register

bkfr[1:0]	—	—	—	zlock[2:0]
0	0	0	0	0b010

Figure 42. PL_BF_ZCOMP register

Table 42. PL_BF_ZCOMP bit descriptions

Field	Description
zlock[2:0]	Z-lock angle threshold. range is from 13° to 44°. Step size is approximately 4°. See Table 42 for more information. Default value: **00** ≥ **13°**. Maximum value: **07** ≥ **44°**.
bkfr[1:0]	Back/front trip angle threshold. See Table 43 for more information. Default: 10 ≥ ±75°. Step size is 5°. Range: ±(65° to 80°).

Table 43. Z-Lockout Angle definitions

zlock	Resultant angle (min) for positions between Landscape and Portrait	Resultant angle (max) for ideal Landscape or Portrait
0x00	13.6	14.5
0x01	17.1	18.2
0x02	20.7	22.0
0x03	24.4	25.9
0x04	28.1	30.0
0x05	32.0	34.2
0x06	36.1	38.7
0x07	40.4	43.4

Table 44. Back/Front Orientation definitions

bkfr	Back → Front Transition	Front → Back Transition
00	Z < 80° or Z > 280°	Z > 100° and Z < 260°
01	Z < 75° or Z > 285°	Z > 105° and Z < 255°
10	Z < 70° or Z > 290°	Z > 110° and Z < 250°
11	Z < 65° or Z > 295°	Z > 115° and Z < 245°

9.8.5 PL_THS_REG (0x14) register

Portrait to landscape trip threshold registers.

pl_ths[4:0]	hys[2:0]
0b00011	0b010

Figure 43. PL_THS_REG register

Table 45. Threshold angle lookup table

Threshold angle (approx.)	5-bit register value
15	0x07
20	0x09
30	0x0C
35	0x0D
40	0x0F
45	0x10
55	0x13
60	0x14
70	0x17
75	0x19

Table 46. Trip angles versus hysteresis settings

Hysteresis register value	Landscape to Portrait trip angle	Portrait to Landscape trip angle
0	45	45
1	49	41
2	52	38
3	56	34
4	59	31
5	62	28
6	66	24
7	69	21

Table 47. Portrait/Landscape orientation definitions

Position	Description
PU	y ~ -1g, x ~ 0
PD	y ~ +1g, x ~ 0
LR	y ~ 0, x ~ +1g
LL	y ~ 0, x ~ -1g

9.9 Freefall and Motion detection

The freefall/motion detection block can be configured to detect low-g (freefall) or high-g (motion) events utilizing the A_FFMT_CFG[*a_ffmt_oae*] bit.

In low-g detect mode (A_FFMT_CFG[*a_ffmt_oae*] = 0) a low-g condition will need to occur on all enabled axes (ex. X, Y and Z) for the A_FFMT_SRC[*a_ffmt_ea*] bit to be affected. And, in high-g detect mode (A_FFMT_CFG[*a_ffmt_oae*] = 1) a high-g condition occurring in any of the enabled axes (ex. X, Y or Z) will suffice to affect the A_FFMT_SRC [*a_ffmt_ea*] bit.

The detection threshold(s) are programed in register 0x17 (A_FFMT_THS) for common threshold operation, and 0x73-0x78 (A_FFMT_THS_X/Y/Z) for individual axis threshold operation.

A_FFMT_CFG[*a_ffmt_ele*] bit determines the behavior of A_FFMT_SRC[*a_ffmt_ea*] bit in response to the desired acceleration event (low-g/high-g). When A_FFMT_CFG[*a_ffmt_ele*] = 1, the freefall or motion event is latched and the A_FFMT_SRC[a_ffmt_ea] flag can only be cleared by reading the A_FFMT_SRC register. When A_FFMT_CFG[*a_ffmt_ele*] = 0, freefall or motion events are not latched, and the A_FFMT_SRC[*a_ffmt_ea*] bit reflects the real-time status of the event detection.

A_FFMT_THS[*a_ffmt_dbcntm*] bit determines the debounce filtering behavior of the logic which sets the A_FFMT_SRC[*a_ffmt_ea*] bit. See Figure 55 for details.

It is possible to enable/disable each axis used in the freefall/motion detection function by configuring bits A_FFMT_CFG[*a_ffmt_xefe*], A_FFMT_CFG[*a_ffmt_yefe*], and A_FFMT_CFG[*a_ffmt_zefe*].

The freefall/motion detection function has the option to use a common 7-bit unsigned threshold for each of the X, Y, Z axes, or individual unsigned 13-bit thresholds for each axis. When A_FFMT_THS_X_MSB[*a_ffmt_ths_xyz_en*] = 0, the 7-bit threshold value stored in register 0x17 is used as a common 7-bit threshold for the X, Y, and Z axes. When *a_ffmt_ths_xyz_en* = 1, each axis may be programmed with an individual 13-bit threshold (stored in the A_FFMT_X/Y/Z MSB and LSB registers).

9.9.1 A_FFMT_CFG (0x15) register

Freefall/motion configuration register.

a_ffmt_ele	a_ffmt_oae	a_ffmt_zefe	a_ffmt_yefe	a_ffmt_xefe	—	—	—
0	0	0	0	0	0	0	0

Figure 44. A_FFMT_CFG register

Table 48. A_FFMT_CFG bit descriptions

Field	Description
a_ffmt_ele	*a_ffmt_ele* denotes whether the enabled event flag will be latched in the A_FFMT_SRC register or the event flag status in the A_FFMT_SRC will indicate the real-time status of the event. If *a_ffmt_ele* bit is set to a logic '1', then the event flags are frozen when the *a_ffmt_ea* bit gets set, and are cleared by reading the A_FFMT_SRC source register. Default value: 0 0: Event flag latch disabled 1: Event flag latch enabled
a_ffmt_oae	*a_ffmt_oae* bit allows the selection between motion (logical OR combination of high-g X, Y, Z-axis event flags) and freefall (logical AND combination of low-g X, Y, Z-axis event flags) detection. Motion detect/freefall detect logic selection. Default value: 0 (freefall flag) 0: Freefall flag(Logical AND combination of low-g X, Y, Z-axis event flags) 1: Motion flag (Logical OR combination of high-g X, Y, Z event flags)
a_ffmt_zefe	*a_ffmt_zefe* enables the detection of a high or low-g event when the measured acceleration data on Z-axis is above/below the threshold set in the A_FFMT_THS register. If the *a_ffmt_ele* bit is set to logic '1' in the A_FFMT_CFG register, new event flags are blocked from updating the A_FFMT_SRC register. Default value: 0 0: Event detection disabled 1: Raise event flag on measured Z-axis acceleration above/below threshold.
a_ffmt_yefe	*a_ffmt_yefe* enables the detection of a high or low-g event when the measured acceleration data on Y-axis is above/below the threshold set in the A_FFMT_THS register. If the *a_ffmt_ele* bit is set to logic '1' in the A_FFMT_CFG register, new event flags are blocked from updating the A_FFMT_SRC register. Default value: 0 0: Event detection disabled 1: Raise event flag on measured Y-axis acceleration above/below threshold.
a_ffmt_xefe	*a_ffmt_xefe* enables the detection of a high or low-g event when the measured acceleration data on X-axis is above/below the threshold set in the A_FFMT_THS register. If the *a_ffmt_ele* bit is set to logic '1' in the A_FFMT_CFG register, new event flags are blocked from updating the A_FFMT_SRC register. Default value: 0 0: Event detection disabled 1: Raise event flag on measured X-axis acceleration above/below threshold.

9.9.2 A_FFMT_SRC (0x16) register

Freefall/motion source register. Read-only register.

This register keeps track of the acceleration event which is triggering (or has triggered, in case of A_FFMT_CFG[*a_ffmt_ele*] = 1) the event flag. In particular A_FFMT_SRC[*a_ffmt_ea*] is set to a logic '1' when the logical combination of acceleration event flags specified in A_FFMT_CFG register is true. This bit is used in combination with the values in CTRL_REG4[*int_en_ffmt*] and CTRL_REG5[*int_cfg_ffmt*] register bits to generate the freefall/motion interrupts.

a_ffmt_ea	—	a_ffmt_zhe	a_ffmt_zhp	a_ffmt_yhe	a_ffmt_yhp	a_ffmt_xhe	a_ffmt_xhp
0	0	0	0	0	0	0	0

Figure 45. A_FFMT_SRC register

Table 49. A_FFMT_SRC bit descriptions

Field	Description
a_ffmt_ea	Event active flag. Default value: 0 0: No event flag has been asserted 1: One or more event flag has been asserted. See the description of the A_FFMT_CFG[*a_ffmt_oae*] bit to determine the effect of the 3-axis event flags on the *a_ffmt_ea* bit.
a_ffmt_zhe	Z-high event flag. Default value: 0 0: Event detected 1: Z-high event has been detected This bit always reads zero if the *a_ffmt_zefe* control bit is set to zero

Table 49. A_FFMT_SRC bit descriptions

a_ffmt_zhp	Z-high event polarity flag. Default value: 0 0: Z event was positive g 1: Z event was negative g This bit read always zero if the *a_ffmt_zefe* control bit is set to zero
a_ffmt_yhe	Y-high event flag. Default value: 0 0: No event detected 1: Y-high event has been detected This bit read always zero if the *a_ffmt_yefe* control bit is set to zero
a_ffmt_yhp	Y-high event polarity flag. Default value: 0 0: Y event detected was positive g 1: Y event was negative g This bit always reads zero if the *a_ffmt_yefe* control bit is set to zero
a_ffmt_xhe	X-high event flag. Default value: 0 0: No event detected 1: X-high event has been detected This bit always reads zero if the *a_ffmt_xefe* control bit is set to zero
a_ffmt_xhp	X-high event polarity flag. Default value: 0 0: X event was positive g 1: X event was negative g This bit always reads zero if the *a_ffmt_xefe* control bit is set to zero

9.9.3 A_FFMT_THS (0x17), A_FFMT_ THS_X_MSB (0x73), A_FFMT_THS_X_LSB (0x74), A_FFMT_THS_Y_MSB (0x75), A_FFMT_THS_Y_LSB (0x76), A_FFMT_THS_Z_MSB (0x77), A_FFMT_THS_Z_LSB (0x78) registers

Freefall/motion detection threshold registers.

a_ffmt_dbcntm	ths[6:0]
0	0b0000000

Figure 46. A_FFMT_THS (0x17) register

Table 50. A_FFMT_THS (0x17) bit descriptions

Field	Description
a_ffmt_dbcntm	The ASIC uses *a_ffmt_dbcntm* to set the acceleration FFMT debounce counter clear mode independent of the value of the *a_ffmt_ths_xyz_en*. *a_ffmt_dbcntm* bit configures the way in which the debounce counter is reset when the inertial event of interest is momentarily not true. When *a_ffmt_dbcntm* bit is a logic '1', the debounce counter is cleared to 0 whenever the inertial event of interest is no longer true (part b, Figure 55) while if the *a_ffmt_dbcntm* bit is set to logic '0' the debounce counter is decremented by 1 whenever the inertial event of interest in longer true (part c, Figure 55) until the debounce counter reaches 0 or the inertial event of interest become active. The decrementing of the debounce counter acts to filter out irregular spurious events which might impede the correct detection of inertial events.
ths[6:0]	Freefall/motion detection threshold: default value: 0b0000000. Resolution is fixed at 63 mg/LSB.

a_ffmt_ths_xyz_en	a_ffmt_ths_x[12:6]
0	0b0000000

Figure 47. A_FFMT_THS_X_MSB (0x73) register

Table 51. A_FFMT_THS_X_MSB (0x73) bit descriptions

Field	Description
a_ffmt_ths_xyz_en	For *a_ffmt_ths_xyz_en* = 0 the ASIC uses the *ffmt_ths*[6:0] value located in register x17[6:0] as a common threshold for the X, Y, and Z-axis acceleration detection. The common unsigned 7-bit acceleration threshold has a fixed resolution of 63 mg/LSB, with a range of 0-127 counts. For *a_ffmt_ths_xyz_en* = 1 the ASIC ignores the common 7-bit G_FFMT_THS value located in register x17 when executing the FFMT function, and the following independent threshold values are used for each axis: A_FFMT_THS_X_MSB and A_FFMT_THS_X_LSB are used for the X-axis acceleration threshold, A_FFMT_THS_Y_MSB and A_FFMT_THS_Y_LSB for the Y-axis acceleration threshold, A_FFMT_THS_Z_MSB and A_FFMT_THS_Z_LSB for the Z-axis acceleration threshold. The A_FFMT_THS_X/Y/Z thresholds are 13-bit unsigned values that have the same resolution as the accelerometer output data determined by XYZ_DATA_CFG fs [1:0]. The *a_ffmt_ths_xyz_en* and *a_ffmt_trans_ths_en* bits must not be enabled simultaneously.
a_ffmt_ths_x[12:6]	7-bit MSB of X-axis acceleration threshold

a_ffmt_ths_x[5:0]	—	—
0b000000	0	0

Figure 48. A_FFMT_THS_X_LSB (0x74) register

a_ffmt_trans_ths_en	a_ffmt_ths_y[12:6]
0	0b0000000

Figure 49. A_FFMT_THS_Y_MSB (0x75) register

Table 52. A_FFMT_THS_X_MSB (0x73) bit descriptions

Field	Description
a_ffmt_trans_ths_en	For *a_ffmt_trans_ths_en* =0 the ASIC uses the *tr_ths[6:0]* value located in TRANSIENT_THS (0x1F) register as a common threshold for the X, Y, and Z-axis transient acceleration detection. The common unsigned 7-bit transient acceleration threshold has a fixed resolution of 63 mg/LSB with a range of 0-127 counts. For *a_ffmt_trans_ths_en* = 1 the ASIC ignores the common 7-bit *tr_ths[6:0]* value located in register x1F when executing the transient acceleration function, and the following independent threshold values are used for each axis: A_FFMT_THS_X_MSB and A_FFMT_THS_X_LSB are used for the X-axis transient acceleration threshold, A_FFMT_THS_Y_MSB and A_FFMT_THS_Y_LSB for the Y-axis transient acceleration threshold, A_FFMT_THS_Z_MSB and A_FFMT_THS_Z_LSB for the Z-axis transient acceleration threshold. The A_FFMT_THS_X/Y/Z thresholds are 13-bit unsigned values that have the same resolution as the accelerometer output data determined by XYZ_DATA_CFG fs [1:0]. The *a_ffmt_ths_xyz_en* and *a_ffmt_trans_ths_en* bits must not be enabled simultaneously
a_ffmt_ths_y[12:6]	7-bit MSB of Y-axis acceleration threshold

a_ffmt_ths_y[5:0]	—	—
0b000000	0	0

Figure 50. A_FFMT_THS_Y_LSB (0x76) register

—	a_ffmt_ths_z[12:6]
0	0b0000000

Figure 51. A_FFMT_THS_Z_MSB (0x77) register

a_ffmt_ths_z[5:0]	—	—
0b000000	0	0

Figure 52. A_FFMT_THS_Z_LSB (0x78) register

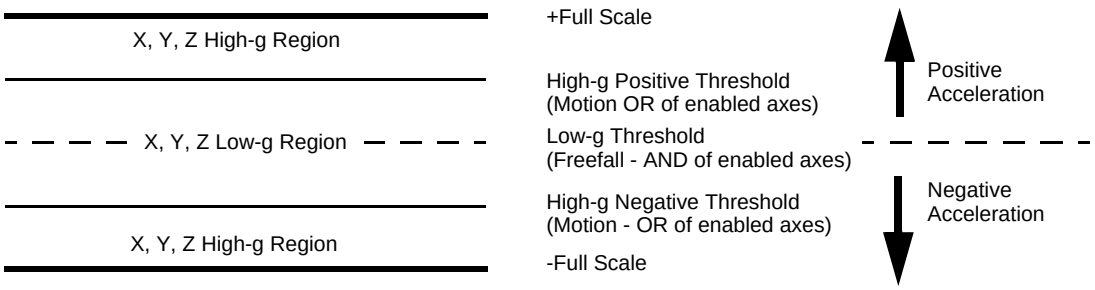


Figure 53. A_FFMT_THS high and low-g level

A_FFMT_THS contains the unsigned 7-bit threshold value used by the freefall/motion detection functional block and is used to detect either low-g (freefall) or high-g (motion) events depending on the setting of G_FFMT_CFG[*f_ffmt_oae*]. If *g_ffmt_oae* = 0, the event is detected when the absolute value of all the enabled axes are below the threshold value. When *g_ffmt_oae* = 1, the event is detected when the absolute value of any of the enabled axes is above the threshold value (see Figure 53 for an illustration of the freefall/motion event detection thresholds). If A_FFMT_THS_X_MSB[*a_ffmt_ths_xyz_en*] = 1, the behavior is identical, except that each axis may be programmed with an individual 13-bit threshold (stored in the A_FFMT_X/Y/Z MSB and LSB registers).

9.9.4 A_FFMT_COUNT (0x18) register

Debounce count register for freefall/motion detection events

This register sets the number of debounce counts for acceleration sample data matching the user programmed conditions for either a freefall or motion detection event required before the interrupt is triggered.

a_ffmt_count[7:0]
0b00000000

Figure 54. A_FFMT_COUNT register

Table 53. A_FFMT_COUNT bit description

Field	Description
a_ffmt_count[7:0]	*a_ffmt_count* defines the minimum number of debounce sample counts required for the detection of a freefall or motion event. A_FFMT_THS[*ffmt_dbcntm*] determines the behavior of the counter when the condition of interest is momentarily not true.

When the internal debounce counter reaches the A_FFMT_COUNT value a freefall/motion event flag is set. The debounce counter will never increase beyond the A_FFMT_COUNT value. The time step used for the debounce sample count depends on the ODR chosen (see Table 53). When the device is operated in hybrid mode, the effective ODR is half of what is selected in CTRL_REG1. This has the effect of doubling the time-step values shown in Table 53.

Table 54. A_FFMT_COUNT relationship with the ODR

High-Pass cutoff frequency (Hz)								
ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	LP
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	40.8	0.638	40.8	20	160	2.5	160
1.56	5.1	163	0.638	163	20	640	2.5	640

For example, an ODR of 100 Hz and a A_ FFMT_COUNT value of 15 would result in minimum debounce response time of 150 ms. If the device is operated in hybrid mode, the effective debounce response time will be 300 ms for the same settings.

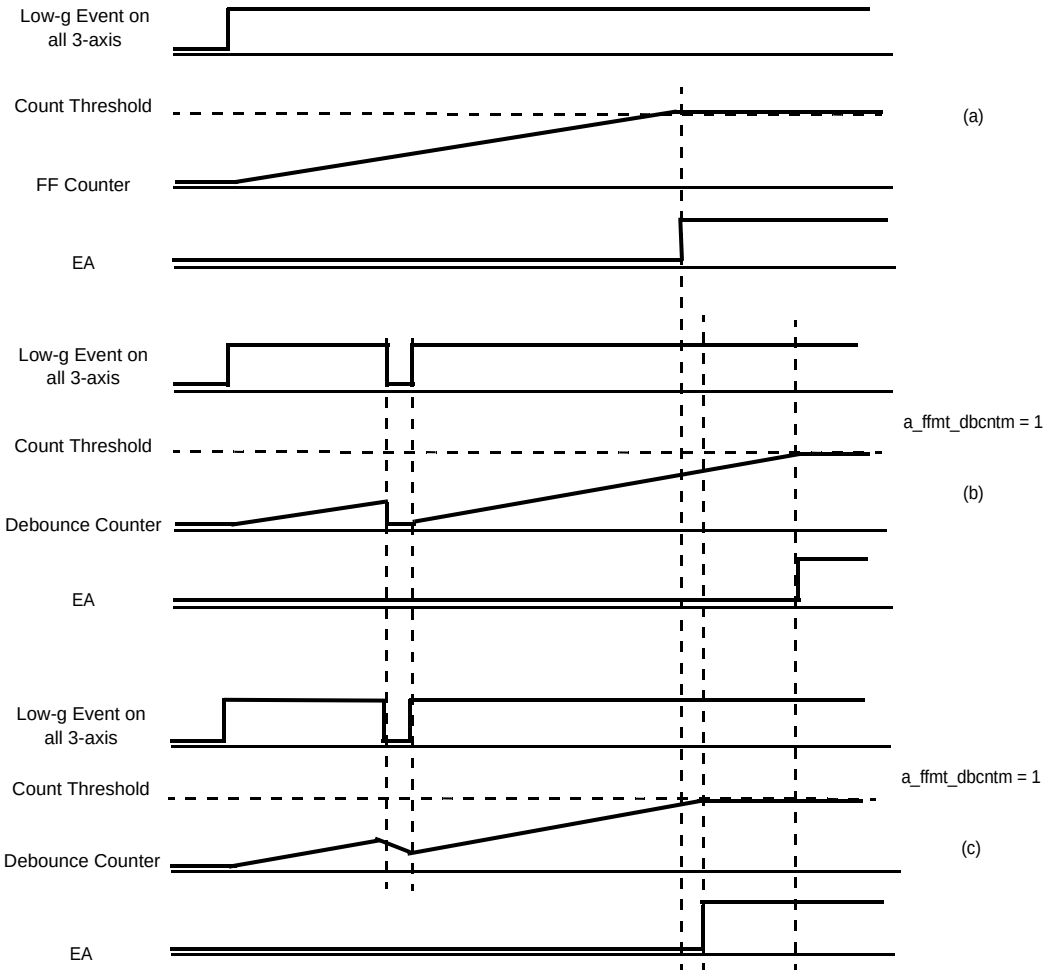


Figure 55. Behavior of the A_FFMT debounce counter in relation to the a_ffmt_dbcntm setting

9.10 Accelerometer vector magnitude function

The accelerometer vector magnitude function is an inertial event detection function available to assist host software algorithms in detecting motion events.

If $\sqrt{(a\_x\_out - a\_x\_ref)^2 + (a\_y\_out - a\_y\_ref)^2 + (a\_z\_out - a\_z\_ref)^2}$ > A_VECM_THS for a time period greater than the value stored in A_VECM_CNT, the vector magnitude change event flag is triggered.

a_x_out, a_y_out, and a_z_out are the current accelerometer output values, and a_x_ref, a_y_ref, and a_z_ref are the reference values stored internally in the ASIC for each axis or in A_VECM_INIT_X/Y/Z registers if A_VECM_CFG[*a_vecm_initm*] is set.

Please note that the x_ref, y_ref, and z_ref values are not directly visible to the host application through the register interface. Please refer to Freescale application note 4458.

9.10.1 A_VECM_CFG (0x5F) register

—	a_vecm_ele	a_vecm_initm	a_vecm_updm	a_vecm_en	—	—	—
0	0	0	0	0	0	0	0

Figure 56. A_VECM_CFG register

Table 55. A_VECM_CFG bit descriptions

Field	Description
a_vecm_ele	Control bit *a_vecm_ele* defines the event latch enable mode. Event latching is disabled for *a_vecm_ele* = 0. In this case, the vector magnitude interrupt flag is in updated real-time and is cleared when the condition for triggering the interrupt is no longer true. The setting and clearing of the event flag is controlled by the A_VECM_CNT register's programmed debounce time. For *a_vecm_ele* = 1, the interrupt flag is latched in and held until the host application reads the INT_SOURCE register (0x0C).
a_vecm_initm	Control bit *a_vecm_initm* defines how the initial reference values (x_ref, y_ref, and z_ref) are chosen. For *a_vecm_initm* = 0 the function uses the current x/y/z accelerometer output data at the time when the vector magnitude function is enabled. For *a_vecm_initm* = 1 the function uses the data from A_VECM_INIT_X/Y/Z registers as the initial reference values.
a_vecm_updm	Control bit *a_vecm_updm* defines how the reference values are updated once the vector magnitude function has been triggered. For *a_vecm_updm* = 0, the function updates the reference value with the current x, y, and z accelerometer output data values. For *a_vecm_updm* = 1, the function does not update the reference values when the interrupt is triggered. Instead the function continues to use the reference values that were loaded when the function was enabled. If both *a_vecm_initm* and *a_vecm_updm* are set to logic '1', the host software can manually update the reference values in real time by writing to the A_VECM_INITX,Y,Z registers.
a_vecm_en	The accelerometer vector magnitude function is enabled by setting *a_vecm_en* = 1, and disabled by clearing this bit (default). The reference values are loaded with either the current X/Y/Z acceleration values or the values stored in the A_VECM_INIT_X/Y/Z registers, depending on the state of the *a_vecm_initm* bit. **Note:** The vector magnitude function will only perform correctly up to a maximum ODR of 400 Hz.

9.10.2 A_VECM_THS_MSB (0x60) register

a_vecm_dbcntm	—	—	a_vecm_ths[12:8]
0	0	0	0b00000

Figure 57. A_VECM_THS_MSB register

Table 56. A_VECM_THS_MSB bit descriptions

Field	Description
a_vecm_dbcntm	Control bit *a_vecm_dbcntm* defines how the debounce timer is reset when the condition for triggering the interrupt is no longer true. When *a_vecm_dbcntm* = 0 the debounce counter is decremented by 1 when the vector magnitude result is below the programmed threshold value. When *a_vecm_dbcntm* = 1 the debounce counter is cleared when the vector magnitude result is below the programmed threshold value.
a_vecm_ths[12:8]	Five MSBs of the 13-bit unsigned A_VECM_THS value. The resolution is equal to the selected accelerometer resolution set in XYZ_DATA_CFG[*fs*]

9.10.3 A_VECM_THS_LSB (0x61) register

a_vecm_ths[7:0]
0b00000000

Figure 58. A_VECM_THS_LSB register

9.10.4 A_VECM_CNT (0x62) register

a_vecm_cnt[7:0]
0b00000000

Figure 59. A_VECM_CNT register

Table 57. A_VECM_CNT bit description

Field	Description
a_vecm_cnt[7:0]	Vector magnitude function debounce count value.

The debounce timer period is determined by the ODR selected in CTRL_REG1. For example, in accelerometer only mode with an ODR of 100 Hz and *a_vecm_cnt* = 15, the debounce time is set at 150 ms. When operating in hybrid mode, the effective ODR is reduced by a factor of two, making the debounce time 300 ms for this example.

Table 58. A_VECM_CNT relationship with selected ODR and power mode

ODR (Hz)	Max time range (s)				Time Step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.318	0.318	0.318	0.318	1.25	1.25	1.25	1.25
400	0.318	0.318	0.318	0.638	1.25	1.25	1.25	2.5
200	0.638	0.638	0.318	1.276	2.5	2.5	1.25	5
100	1.276	1.276	0.318	2.56	5	5	1.25	10
50	2.56	2.56	0.318	5.1	10	10	1.25	20
12.5	2.56	10.2	0.318	20.4	10	40	1.25	80
6.25	2.56	20.4	0.318	40.8	10	80	1.25	160
1.56	2.56	81.6	0.318	163.2	10	320	1.25	640

9.10.5 A_VECM_INITX_MSB (0x63) register

—	—	a_vecm_initx[13:8]
0	0	0b000000

Figure 60. A_VECM_INITX_MSB register

Table 59. A_VECM_INITX_MSB bit description

Field	Description
a_vecm_initx[13:8]	Most significant 6 bits of the signed 14-bit initial X-axis value to be used as ref_x when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

9.10.6 A_VECM_INITX_LSB (0x64) register

a_vecm_initx[7:0]
0b00000000

Figure 61. A_VECM_INITX_LSB register

Table 60. A_VECM_INITX_LSB bit description

Field	Description
a_vecm_initx[7:0]	LSB of the signed 14-bit initial X-axis value to be used as ref_x when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

9.10.7 A_VECM_INITY_MSB (0x65) register

—	—	a_vecm_inity[13:8]
0	0	0b000000

Figure 62. A_VECM_INITY_MSB register

Table 61. A_VECM_INITY_MSB bit description

Field	Description
a_vecm_inity[13:8]	Most significant 6 bits of the signed 14-bit initial Y-axis value to be used as ref_y when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

9.10.8 A_VECM_INITY_LSB (0x66) register

a_vecm_inity[7:0]

Figure 63. A_VECM_INITY_LSB register

Table 62. A_VECM_INITY_LSB bit description

Field	Description
a_vecm_inity[7:0]	LSB of the signed 14-bit initial Y-axis value to be used as ref_y when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

9.10.9 A_VECM_INITZ_MSB (0x67) register

—	—	a_vecm_initz[13:8]
0	0	0b000000

Figure 64. A_VECM_INITZ_MSB register

Table 63. A_VECM_INITZ_MSB bit description

Field	Description
a_vecm_initz[13:8]	Most significant 6 bits of the signed 14-bit initial Z-axis value to be used as ref_z when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

9.10.10 A_VECM_INITZ_LSB (0x68) register

a_vecm_initz[7:0]
0b00000000

Figure 65. A_VECM_INITZ_LSB register

Table 64. A_VECM_INITZ_LSB bit description

Field	Description
a_vecm_initz[7:0]	LSB of the signed 14-bit initial Z-axis value to be used as ref_z when A_VECM_CFG[*a_vecm_initm*] = 1. The resolution is determined by the settings made in XYZ_DATA_CFG[*fs*], and is equal to the accelerometer resolution.

9.11 Transient (AC) acceleration detection

The transient detection function is similar to the freefall/motion detection function with the exception that a high-pass filter can be used to eliminate the DC offset from the acceleration data. There is an option to disable the high pass filter, which causes the transient detection function to work in a similar manner to the motion detection function.

The transient detection function can be configured to signal an interrupt when the high-pass filtered acceleration delta values for any of the enabled axes exceeds the threshold programmed in TRANSIENT_THS for the debounce time programmed in TRANSIENT_COUNT. For more information on how to use and configure the transient detection function please refer to Freescale application note AN4461.

9.11.1 TRANSIENT_CFG (0x1D) register

—	—	—	tran_ele	tran_zefe	tran_yefe	tran_xefe	tran_hpf_byp
0	0	0	0	0	0	0	0

Figure 66. TRANSIENT_ CFG register

Table 65. TRANSIENT_ CFG bit descriptions

Field	Description
tran_ele	Transient event flag latch enable. Default value: 0 0: Event flag latch disabled: the transient interrupt flag reflects the real-time status of the function. 1: Event flag latch enabled: the transient interrupt event flag is latched and a read of the TRANSIENT_SRC register is required to clear the event flag.
tran_zefe	Z-axis transient event flag enable. Default value: 0 0: Z-axis event detection disabled 1: Z-axis event detection enabled. Raise event flag on Z-axis acceleration value greater than threshold.
tran_yefe	Y-axis transient event flag enable. Default value: 0 0: Y-axis event detection disabled 1: Y-axis event detection enabled. Raise event flag on Y-axis acceleration value greater than threshold.
tran_xefe	X-axis transient event flag enable. Default value: 0 0: X-axis event detection disabled 1: X-axis event detection enabled. Raise event flag on X-axis acceleration value greater than threshold.
tran_hpf_byp	Transient function high-pass filter bypass. Default value: 0 0: High-pass filter is applied to accelerometer data input to the transient function. 1: High-pass filter is not applied to accelerometer data input to the transient function.

9.11.2 TRANSIENT_SRC (0x1E) register

Transient event flag source register. This register provides the event status of the enabled axes and polarity (directional) information.

—	tran_ea	tran_zef	tran_zpol	tran_yef	tran_ypol	tran_xef	trans_xpol
0	0	0	0	0	0	0	0

Figure 67. TRANSIENT_ CFG register

Table 66. TRANSIENT_SRC bit descriptions

Field	Description
tran_ea	Transient event active flag. Default value: 0 0: No transient event active flag has been asserted. 1: One or more transient event active flags has been asserted.
tran_zef	Z-axis transient event active flag. Default value: 0 0: Z-axis event flag is not active. 1: Z-axis event flag is active; Z-axis acceleration has exceeded the programmed threshold for the debounce time specified in TRANS_COUNT.
tran_zpol	Z-axis event flag polarity. 0: Z-axis event was above positive threshold value. 1: Z-axis event was below negative threshold value.
tran_yef	Y-axis transient event active flag. Default value: 0 0: Y-axis event flag is not active. 1: Y-axis event flag is active; Y-axis acceleration has exceeded the programmed threshold for the debounce time specified in TRANS_COUNT.
tran_ypol	Y-axis event flag polarity. 0: Y-axis event was above positive threshold value. 1: Y-axis event was below negative threshold value.
tran_xef	X-axis transient event active flag. Default value: 0 0: X-axis event flag is not active. 1: X-axis event flag is active; X-axis acceleration has exceeded the programmed threshold for the debounce time specified in TRANS_COUNT.
tran_xpol	X-axis event flag polarity. 0: X-axis event was above positive threshold value. 1: X-axis event was below negative threshold value.

When TRANSIENT_CFG[*tran_ele*] = 1, the TRANSIENT_SRC event flag(s) and polarity bits are latched when the interrupt event is triggered, allowing the host application to determine which event flag(s) originally triggered the interrupt. When TRANSIENT_CFG[*tran_ele*] = 0, events which occur after the event that originally triggered the interrupt will update the flag and polarity bits, but once set, the flags can only be cleared by reading the TRANSIENT_SRC register.

9.11.3 TRANSIENT_THS (0x1F) register

The TRANSIENT_THS register determines the debounce counter behavior and also sets the transient event detection threshold.It is possible to use A_FFMT_THS_X/Y/Z MSB and LSB registers to set transient acceleration thresholds for individual axes via *a_ffmt_trans_ths_en* bit in A_FFMT_THS_Y_MSB register. Please see Section 9.9.3 for more details.

tr_dbcntm	tr_ths[6:0]
0	0b0000000

Figure 68. TRANSIENT_THS register

Table 67. TRANSIENT_THS bit descriptions

Field	Description
tr_dbcntm	Debounce counter mode selection. 0: Decrements debounce counter when the transient event condition is not true during the current ODR period. 1: Clears debounce counter when the transient event condition is not true during the current ODR period.
tr_ths[6:0]	Transient event threshold. This register has a resolution of 63mg/LSB regardless of the full-scale range setting made in XYZ_DATA_CFG[*fs*]. If CTRL_REG1[*lnoise*] = 1, the maximum acceleration measurement range is ±4g.

The tr_ths[6:0] value is a 7-bit unsigned number, with a fixed resolution of 63 mg/LSB corresponding to a ±8g measurement range. The resolution does not change with the full-scale range setting made in XYZ_DATA_CFG[fs]. If CTRL_REG1[*lnoise*] = 1, the measurement range is fixed at ±4g, regardless of the settings made in XYZ_DATA_CFG.

9.11.4 TRANSIENT_COUNT (0x20) register

The TRANSIENT_COUNT register sets the minimum number of debounce counts needed to trigger the transient event interrupt flag when the measured acceleration value exceeds the threshold set in TRANSIENT_THS for any of the enabled axes.

tr_count[7:0]
0b00000000

Figure 69. TRANSIENT_COUNT register

Table 68. TRANSIENT_COUNT bit description

Field	Description
tr_count[7:0)	Transient function debounce count value.

The time step for the transient detection debounce counter is set by the value of the system ODR and power mode as shown in Table 68. When the device is operated in hybrid mode, the effective ODR is half of what is selected in CTRL_REG1, which also doubles the time-step values shown in Table 68.

Table 69. TRANSIENT_COUNT relationship with the ODR

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20
12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	40.8	0.638	40.8	20	160	2.5	160
1.56	5.1	163	0.638	163	20	640	2.5	640

An ODR of 100 Hz and a TRANSIENT_COUNT value of 15 would result in minimum debounce response time of 150 ms. When the device is operated in hybrid mode, these settings would result in an effective debounce time of 300 ms.

9.12 Pulse detection

9.12.1 PULSE_CFG (0x21) register

This register configures the pulse event detection function.

pls_dpa	pls_ele	pls_zdpefe	pls_zspefe	pls_ydpefe	pls_yspefe	pls_xdpefe	pls_xspefe
0	0	0	0	0	0	0	0

Figure 70. PULSE_CFG register

Table 70. PULSE_CFG bit descriptions

Field	Description
pls_dpa	Double pulse abort. 0: Double pulse detection is not aborted if the start of a pulse is detected during the time period specified by the PULSE_LTCY register. 1: Setting the *pls_dpa* bit momentarily suspends the double tap detection if the start of a pulse is detected during the time period specified by the PULSE_LTCY register and the pulse ends before the end of the time period specified by the PULSE_LTCY register.
pls_ele	Pulse event flag latch enable. When enabled, a read of the PULSE_SRC register is needed to clear the event flag. 0: Event flag latch disabled 1: Event flag latch enabled
pls_zdpefe	Event flag enable on double pulse event on Z-axis. 0: Event detection disabled 1: Raise event flag on detection of double pulse event on Z-axis
pls_zspefe	Event flag enable on single pulse event on Z-axis. 0: Event detection disabled 1: Raise event flag on detection of single pulse event on Z-axis
pls_ydpefe	Event flag enable on double pulse event on Y-axis. 0: Event detection disabled 1: Raise event flag on detection of double pulse event on Y-axis
pls_yspefe	Event flag enable on single pulse event on Y-axis. 0: Event detection disabled 1: Raise event flag on detection of single pulse event on Z-axis.
pls_xdpefe	Event flag enable on double pulse event on X-axis. 0: Event detection disabled 1: Raise event flag on detection of double pulse event on X-axis.

Table 70. PULSE_CFG bit descriptions

pls_xspefe	Event flag enable on single pulse event on X-axis. 0: Event detection disabled 1: Raise event flag on detection of single pulse event on X-axis.

9.12.2 PULSE_SRC (0x22) register

This register indicates the status bit for the pulse detection function.

pls_src_ea	pls_src_axz	pls_src_axy	pls_src_axx	pls_src_dpe	pls_src_polz	pls_src_poly	pls_src_polx

Figure 71. PULSE_SRC register

Table 71. PULSE_SRC bit descriptions

Field	Description
pls_src_ea	Event active flag. 0: No interrupt has been generated 1: One or more interrupt events have been generated
pls_src_axz	Z-axis event flag. 0: No interrupt. 1: Z-axis event has occurred
pls_src_axy	Y-axis event flag. 0: No interrupt. 1: Y-axis event has occurred
pls_src_axx	X-axis event flag. 0: No interrupt. 1: X-axis event has occurred.
pls_src_dpe	Double pulse on first event. 0: Single pulse event triggered interrupt. 1: Double pulse event triggered interrupt.
pls_src_polz	Pulse polarity of Z-axis event. 0: Pulse event that triggered interrupt was positive. 1: Pulse event that triggered interrupt was negative.
pls_src_poly	Pulse polarity of Y-axis event. 0: Pulse event that triggered interrupt was positive. 1: Pulse event that triggered interrupt was negative.
pls_src_polx	Pulse polarity of X-axis event. 0: Pulse event that triggered interrupt was positive. 1: Pulse event that triggered interrupt was negative.

9.12.3 PULSE_THSX (0x23) register

—	pls_thsx[6:0]
0	0b0000000

Figure 72. PULSE_THSX register

Table 72. PULSE_THSX bit description

Field	Description
pls_thsx[6:0]	Pulse threshold for X-axis.

The PULSE_THSX, PULSE_THSY and PULSE_THSZ registers define the thresholds used by the system to start the pulse event detection procedure. Threshold values for each axis are unsigned 7-bit numbers with a fixed resolution of 0.063g/LSB,

corresponding to an 8g acceleration full-scale range. The full-scale range is fixed at 8g for the pulse detection function, regardless of the settings made in XYZ_DATA_CFG[*fs*].

9.12.4 PULSE_THSY (0x24) register

—	pls_thsy[6:0]
0	0b0000000

Figure 73. PULSE_THSY register

Table 73. PULSE_THSY bit description

Field	Description
pls_thsy[6:0]	Pulse threshold for Y-axis.

9.12.5 PULSE_THSZ (0x25) register

—	pls_thsz[6:0]
0	0b0000000

Figure 74. PULSE_THSZ register

Table 74. PULSE_THSZ bit description

Field	Description
pls_thsz[6:0]	Pulse threshold for Z-axis.

9.12.6 PULSE_TMLT (0x26) register

pls_tmlt[7:0]
0b00000000

Figure 75. PULSE_TMLT register

Table 75. PULSE_TMLT bit description

Field	Description
pls_tmlt[7:0]	*pls_tmlt[7:0]* defines the maximum time interval that can elapse between the start of the acceleration on the selected channel exceeding the specified threshold and the end when the channel acceleration goes back below the specified threshold.

Minimum time step for the pulse time limit is defined in Tables 75 and 76. Maximum time for a given ODR is “Minimum time step x 255”.

Table 76. Time step for pulse time limit LPF_EN = 1

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.319	0.319	0.319	0.319	1.25	1.25	1.25	1.25
400	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
200	1.28	1.28	0.638	1.28	5	5	2.5	5
100	2.55	2.55	0.638	2.55	10	10	2.5	10
50	5.1	5.1	0.638	5.1	20	20	2.5	20

Table 76. Time step for pulse time limit LPF_EN = 1

12.5	5.1	20.4	0.638	20.4	20	80	2.5	80
6.25	5.1	40.8	0.638	40.8	20	160	2.5	160
1.56	5.1	163	0.638	163	20	640	2.5	640

Table 77. Time step for PULSE time limit LPF_EN = 0

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.159	0.159	0.159	0.159	0.625	0.625	0.625	0.625
400	0.159	0.159	0.159	0.319	0.625	0.625	0.625	1.25
200	0.319	0.319	0.159	0.638	1.25	1.25	0.625	2.5
100	0.638	0.638	0.159	1.28	2.5	2.5	0.625	5
50	1.28	1.28	0.159	2.55	5	5	0.625	10
12.5	1.28	5.1	0.159	10.2	5	20	0.625	40
6.25	1.28	10.2	0.159	20.4	5	40	0.625	80
1.56	1.28	40.8	0.159	81.6	5	160	0.625	320

Therefore an ODR setting of 400 Hz with normal power mode would result in a maximum pulse time limit of (0.625 ms * 255) ≥ 159 ms.

9.12.7 PULSE_LTCY (0x27) register

pls_ltcy[7:0]
0b00000000

Figure 76. PULSE_LTCY register

Table 78. PULSE_LTCY bit description

Field	Description
pls_ltcy[7:0]	*pls_ltcy*[7:0] defines the time interval that starts after the first pulse detection where the pulse detection function ignores the start of a new pulse.

Minimum time step for the pulse latency is defined in Tables 78 and 79. Maximum time is “(time step @ ODR and power mode) x 255”.

Table 79. Time step for PULSE latency @ ODR and power mode LPF_EN = 1

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
400	1.276	1.276	1.276	1.276	5	5	5	5
200	2.56	2.56	1.276	2.56	10	10	5	10
100	5.1	5.1	1.276	5.1	20	20	5	20
50	10.2	10.2	1.276	10.2	40	40	5	40
12.5	10.2	40.8	1.276	40.8	40	160	5	160
6.25	10.2	81.6	1.276	81.6	40	320	5	320
1.56	10.2	326	1.276	326	40	1280	5	1280

Table 80. Time step for PULSE Latency @ ODR and power mode LPE_EN = 0

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.318	0.318	0.318	0.318	1.25	1.25	1.25	1.25
400	0.318	0.318	0.318	0.638	1.25	1.25	1.25	2.5
200	0.638	0.638	0.318	1.276	2.5	2.5	1.25	5
100	1.276	1.276	0.318	2.56	5	5	1.25	10
50	2.56	2.56	0.318	5.1	10	10	1.25	20
12.5	2.56	10.2	0.318	20.4	10	40	1.25	80
6.25	2.56	20.4	0.318	40.8	10	80	1.25	160
1.56	2.56	81.6	0.318	163.2	10	320	1.25	640

9.12.8 PULSE_WIND (0x28) register

pls_wind[7:0]
0b00000000

Figure 77. PULSE_WIND register

Table 81. PULSE_WIND bit description

Field	Description
pls_wind[7:0]	*pls_wind*[7:0] defines the maximum interval of time that can elapse after the end of the latency interval in which the start of the second pulse event must be detected provided the device has been configured for double pulse detection. The detected second pulse width must be shorter than the time limit constraint specified by the PULSE_TMLT register, but the end of the double pulse need not finish within the time specified by the PULSE_WIND register.

The time step for the pulse window counter varies with the selected ODR and power modes as defined in Tables 81 and 82. The maximum time value is equal to (time step @ ODR and power mode) x 255. Please note that when the device is operated in hybrid mode, the effective ODR is half of what is selected in CTRL_REG1, which will double the time step value from what is shown in Table 81 and Table 82.

Table 82. Time step for PULSE detection window @ ODR and power mode LPF_EN = 1

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.638	0.638	0.638	0.638	2.5	2.5	2.5	2.5
400	1.276	1.276	1.276	1.276	5	5	5	5
200	2.56	2.56	1.276	2.56	10	10	5	10
100	5.1	5.1	1.276	5.1	20	20	5	20
50	10.2	10.2	1.276	10.2	40	40	5	40
12.5	10.2	40.8	1.276	40.8	40	160	5	160
6.25	10.2	81.6	1.276	81.6	40	320	5	320
1.56	10.2	326	1.276	326	40	1280	5	1280

Table 83. Time step for PULSE detection window @ ODR and power mode LPF_EN = 1

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	0.318	0.318	0.318	0.318	1.25	1.25	1.25	1.25
400	0.318	0.318	0.318	0.638	1.25	1.25	1.25	2.5
200	0.638	0.638	0.318	1.276	2.5	2.5	1.25	5
100	1.276	1.276	0.318	2.56	5	5	1.25	10
50	2.56	2.56	0.318	5.1	10	10	1.25	20
12.5	2.56	10.2	0.318	20.4	10	40	1.25	80
6.25	2.56	20.4	0.318	40.8	10	80	1.25	160
1.56	2.56	81.6	0.318	163.2	10	320	1.25	640

9.13 Accelerometer offset correction

The 8-bit 2's complement offset correction registers are used to realign the zero-g position of the X, Y, and Z axes after device board mount. The resolution of the offset registers is 2 mg per LSB, with an effective offset adjustment range of -256 mg to +254 mg for each axis.

For more information on how to calibrate the 0g offset, please refer to Freescale application note AN4069.

9.13.1 OFF_X (0x2F) register

Figure 78. OFF_X register

off_x[7:0]
0b00000000

Table 84. OFF_X bit description

Field	Description
off_x[7:0]	X-axis offset correction value expressed as an 8-bit 2's complement number.

9.13.2 OFF_Y (0x30) register

off_y[7:0]
0b00000000

Figure 79. OFF_Y register

Table 85. OFF_Y bit description

Field	Description
off_y[7:0]	Y-axis offset correction value expressed as an 8-bit 2's complement number.

9.13.3 OFF_Z (0x31) register

off_z[7:0]
0b00000000

Figure 80. OFF_Z register

Table 86. OFF_Z bit description

Field	Description
off_z[7:0]	Z-axis offset correction value expressed as an 8-bit 2's complement number.

9.14 Magnetometer data registers

9.14.1 M_DR_STATUS (0x32) register

Magnetic data ready status register.

This register indicates the real-time status information of the X, Y, and Z magnetic sample data.

xyzow	zow	yow	xow	xyzdr	zdr	ydr	xdr
0	0	0	0	0	0	0	0

Figure 81. M_DR_STATUS register

Table 87. M_DR_STATUS bit descriptions

Field	Description
zyxow	*zyxow* is set to one whenever new magnetic data is acquired before completing the retrieval of the previous data set. This event occurs when the content of at least one magnetometer output data register (i.e. M_OUT_X/Y/Z) has been overwritten. *zyxow* is cleared when the most significant bytes of the magnetometer data (M_OUT_X_MSB, M_OUT_Y_MSB, and M_OUT_Z_MSB) are read. X, Y, Z-axis data overwrite: 0: No data overwrite has occurred 1: Previous X, Y, Z magnetic data was overwritten by new X, Y, Z data before it was completely read
zow	*zow* is set to 1 whenever a new Z-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. *zow* is cleared anytime the M_OUT_Z_MSB register is read. Z-axis data overwrite: 0: No data overwrite has occurred 1: Previous Z-axis magnetic data was overwritten by new Z-axis data before it was read
yow	*yow* is set to 1 whenever a new Y-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. *yow* is cleared anytime M_OUT_Y_MSB register is read. Y-axis data overwrite: 0: No data overwrite has occurred 1: Previous Y-axis magnetic data was overwritten by new Y-axis data before it was read
xow	*xow* is set to 1 whenever a new X-axis acquisition is completed before the retrieval of the previous data. When this occurs the previous data is overwritten. *xow* is cleared anytime the M_OUT_X_MSB register is read. X-axis data overwrite: 0: No data overwrite has occurred 1: Previous X-axis magnetic data was overwritten by new X-axis data before it was read
zyxdr	*zyxdr* signals that a new acquisition for the X, Y, and Z axes magnetic data is available. *zyxdr* is cleared when the most significant bytes of the magnetometer data (M_OUT_X_MSB, M_OUT_Y_MSB, and M_OUT_Z_MSB) are read. X, Y, Z new data available: 0: No new set of X, Y, Z magnetic data is available 1: A new set of X, Y, Z magnetic data is available
zdr	*zdr* is set to 1 whenever a new Z-axis data acquisition is completed. *zdr* is cleared anytime the M_OUT_Z_MSB register is read. Z-axis new data available: 0: No new Z-axis magnetic data is available 1: New Z-axis magnetic data is available
ydr	*ydr* is set to 1 whenever a new Y-axis data acquisition is completed. *ydr* is cleared anytime the M_OUT_Y_MSB register is read. Y-axis new data available: 0: No new Y-axis magnetic data is available 1: New Y-axis magnetic data is available

Table 87. M_DR_STATUS bit descriptions

xdr	*xdr* is set to 1 whenever a new X-axis data acquisition is completed. *xdr* is cleared anytime the M_OUT_X_MSB register is read. X-axis new data available: 0: No new X-axis magnetic data is available. 1: New X-axis magnetic data is available

9.14.2 M_OUT_X_MSB (0x33), M_OUT_X_LSB (0x34), M_OUT_Y_MSB (0x35), M_OUT_Y_LSB (0x36), M_OUT_Z_MSB (0x37), M_OUT_Z_LSB (0x38) registers

X-axis, Y-axis, and Z-axis 16-bit magnetic output data expressed as 2's complement numbers, with a resolution of 0.1 μT/LSB.

m_out_x[15:8]

Figure 82. M_OUT_X_MSB (0x33) register

m_out_x[7:0]

Figure 83. M_OUT_X_LSB (0x34) register

m_out_y[15:8]

Figure 84. M_OUT_Y_MSB (0x35) register

m_out_y[7:0]

Figure 85. M_OUT_Y_LSB (0x36) register

m_out_z[15:8]

Figure 86. M_OUT_Z_MSB (0x37) register

m_out_z[7:0]

Figure 87. M_OUT_Z_LSB (0x38) register

9.14.3 CMP_X_MSB (0x39), CMP_X_LSB (0x3A), CMP_Y_MSB (0x3B), CMP_Y_LSB (0x3C), CMP_Z_MSB (0x3D), CMP_Z_LSB (0x3E) registers

These registers contain the 2’s complement 14-bit decimated acceleration values, and are time aligned with the magnetometer sample data. The decimation is controlled by the ODR (CTRL_REG1 dr[2:0]) and the magnetometer OSR (M_CTRL_REG1 m_os[2:0]) settings.These registers allow the host application to acquire a complete set of time-aligned magnetic and acceleration data with the same oversampling ratio applied to each axis. Note that unlike the acceleration data available in the OUT_X/Y/Z registers located at addresses x1-x6, the data in the CMP_X/Y/Z registers is right justified.

—	—	cmp_x[13:8]

Figure 88. CMP_X_MSB (0x39) register

cmp_x[7:0]

Figure 89. CMP_X_LSB (0x3A) register

—	—	cmp_y[13:8]

Figure 90. CMP_Y_MSB (0x3B) register

cmp_y[7:0]

Figure 91. CMP_Y_LSB (0x3C) register

—	—	cmp_z[13:8]

Figure 92. CMP_Z_MSB (0x3D) register

cmp_z[7:0]

Figure 93. CMP_Z_LSB (0x3E) register

9.14.4 MAX_X_MSB (0x45), MAX_X_LSB (0x46), MAX_Y_MSB (0x47), MAX_Y_LSB (0x48), MAX_Z_MSB (0x49), MAX_Z_LSB (0x4A) registers

The magnetometer MAX_X/Y/Z registers are 16-bit 2's complement format with a resolution of 0.1 µT/LSB. The registers are read/write and along with the MIN_X/Y/Z registers are used to calculate the magnetic offset for each axis using the equation (MAX_X/Y/Z + MIN_X/Y/Z) /2 when M_CTRL_REG2[*maxmin_dis*] = 0 (default).

When M_CTRL_REG1[*m_acal*] = 1 (default 0), the MAG_OFF_X/Y/Z registers are automatically updated with the calculated offset values at the end of every measurement cycle (ODR period).

On a POR, or after setting M_CTRL_REG2[*maxmin_rst*] = 1, the MAX_X/Y/Z registers are loaded with the hex value 0x8000 (negative full scale).

The host application may write to the MAX_X/Y/Z registers to change the currently used maximum values for each axis, however, when M_CTRL_REG1[*maxmin_dis*] = 0 (default), the system will overwrite these values when it updates the MAX_X/Y/Z registers at the end of the next measurement cycle (ODR period).

max_x[15:8]
0b00000000

Figure 94. MAX_X_MSB register

max_x[7:0]
0b00000000

Figure 95. MAX_X_LSB register

max_y[15:8]
0b00000000

Figure 96. MAX_Y_MSB register

max_y[7:0]
0b00000000

Figure 97. MAX_Y_LSB register

max_z[15:8]
0b00000000

Figure 98. MAX_Z_MSB register

max_z[7:0]
0b00000000

Figure 99. MAX_Z_LSB register

9.14.5 MIN_X_MSB (0x4B), MIN_X_LSB (0x4C), MIN_Y_MSB (0x4D), MIN_Y_LSB (0x4E), MIN_Z_MSB (0x4F), MIN_Z_LSB (0x50) registers

The magnetometer MIN_X/Y/Z registers are 16-bit 2's complement format with a resolution of 0.1 µT/LSB. The registers are read/write and along with the MAX_X/Y/Z registers are used to calculate the magnetic offset for each axis using the equation (MAX_X/Y/Z + MIN_X/Y/Z) /2 when M_CTRL_REG2[*maxmin_dis*] = 0 (default).

When M_CTRL_REG1[*m_acal*] = 1 (default 0), the MAG_OFF_X/Y/Z registers are automatically updated with the calculated offset values at the end of every measurement cycle (ODR period).

On a POR, or after setting M_CTRL_REG2[*maxmin_rst*] = 1, the MIN_X/Y/Z registers are loaded with the hex value 0x7FFF (positive full scale). The host application may write to the MIN_X/Y/Z registers to change the currently used minimum values for each axis, however, when M_CTRL_REG1[*maxmin_dis*] = 0 (default), the system will overwrite these values when it updates the MIN_X/Y/Z registers at the end of the next measurement cycle (ODR period).

min_x[15:8]
0b00000000

Figure 100. MIN_X_MSB register

min_x[7:0]
0b00000000

Figure 101. MIN_X_LSB register

min_y[15:8]
0b00000000

Figure 102. MIN_Y_MSB register

min_y[7:0]
0b00000000

Figure 103. MIN_Y_LSB register

min_z[15:8]
0b00000000

Figure 104. MIN_Z_MSB register

min_z[7:0]
0b00000000

Figure 105. MIN_Z_LSB register

9.15 Magnetometer offset correction

9.15.1 M_OFF_X_MSB (0x3F), M_OFF_X_LSB (0x40),M_OFF_Y_MSB (0x41),M_OFF_Y_LSB (0x42), M_OFF_Z_MSB (0x43), M_OFF_Z_LSB (0x44) registers

The zero-field output for each axis can be adjusted by writing to these registers. The user must set M_CTRL_REG3[*m_raw*] = 0 (default) for the values in these registers to have any effect on the magnetic output data.

Each offset register is 16-bit, 2's complement format with a resolution of 0.1 μT/LSB.

m_off_x[15:8]
0b00000000

Figure 106. M_OFF_X_MSB register

m_off_x[7:0]
0b00000000

Figure 107. M_OFF_X_LSB register

m_off_y[15:8]
0b00000000

Figure 108. M_OFF_Y_MSB register

m_off_y[7:0]
0b00000000

Figure 109. M_OFF_Y_LSB register

m_off_z[15:8]
0b00000000

Figure 110. M_OFF_Z_MSB register

m_off_z[7:0]
0b00000000

Figure 111. M_OFF_Z_LSB register

9.16 Magnetometer threshold function

The magnetometer threshold function works in a similar manner to the freefall/motion detection module but uses magnetic data for the event detection instead of acceleration data. The *m_ths_oae* bit setting determines the logic used to evaluate the threshold detection function for the enabled axes. With *m_ths_oae* = 0, the magnetic sample data for each enabled axis must be below the threshold values specified in the MAG_THS_X/Y/Z registers for the time period specified in MAG_THS_COUNT before the event flag is triggered. For *m_ths_oae* = 1, any of the enabled axes must be above the threshold values specified in the MAG_THS_X/Y/Z registers for the time period specified in MAG_THS_COUNT before the event flag is triggered.

9.16.1 M_THS_CFG (0x52) register

Magnetic field threshold detection configuration register.

m_ths_ele	m_ths_oae	m_ths_zefe	m_ths_yefe	m_ths_xefe	m_ths_wake_en	m_ths_int_en	m_ths_int_cfg
0	0	0	0	0	0	0	0

Figure 112. M_THS_CFG register

Table 88. M_THS_CFG bit descriptions

Field	Description
m_ths_ele	Magnetic threshold event latch enable. 0: Event flag latch disabled. Magnetic threshold events are not latched, and the event flag will change state with the real-time status of the event detection logic. 1: Event flag latch enabled. Magnetic threshold events are latched and the event flag can only be cleared by reading the M_THS_SRC register.
m_ths_oae	Magnetic threshold event logic selection. 0: Logical “AND” of enabled axes X, Y, and Z below threshold flags is used to detect the event. 1: Logical “OR” of enabled axes X, Y, and Z above threshold flags is used to detect the event.
m_ths_zefe	Event flag enable on Z-axis. Default value: 0 0: Z-axis event detection disabled 1: Raise event flag on measured magnetic field value above/below preset threshold for Z-axis
m_ths_yefe	Event flag enable on Y-axis. Default value: 0 0: Y-axis event detection disabled 1: Raise event flag on measured magnetic field value above/below preset threshold for Y-axis
m_ths_xefe	Event flag enable on X-axis. Default value: 0 0: X-axis event detection disabled 1: Raise event flag on measured magnetic field value above/below preset threshold for X-axis
m_ths_wake_en	0: The system excludes the magnetic threshold event flag when evaluating the Auto-Sleep/Wake function. 1: The system includes the magnetic threshold event flag when evaluating the Auto-Sleep/Wake function.
m_ths_int_en	0: Magnetic threshold interrupt is disabled. 1: Magnetic threshold interrupt is enabled.
m_ths_int_cfg	0: Magnetic threshold event flag is output on INT2 pin (logically OR'd with other INT2 interrupt events) 1: Magnetic threshold event flag is output on INT1 pin (logically OR'd with other INT1 interrupt events)

The unsigned 15-bit M_THS_X/Y/Z registers hold the threshold used for magnetic event detection. With M_THS_CFG [m_ths_oae] = 0, the event is detected when all of the enabled axes are below or equal to their respective threshold values (AND condition). With M_THS_CFG [m_ths_oae] = 1, the event is detected when any of the enabled axes is above or equal to their respective threshold value (OR condition). The thresholds for each axis are applied after the magnetic data has been adjusted by the offset values stored in the M_OFF_X/Y/Z registers when M_CTRL_REG3[*m_raw*] = 0.

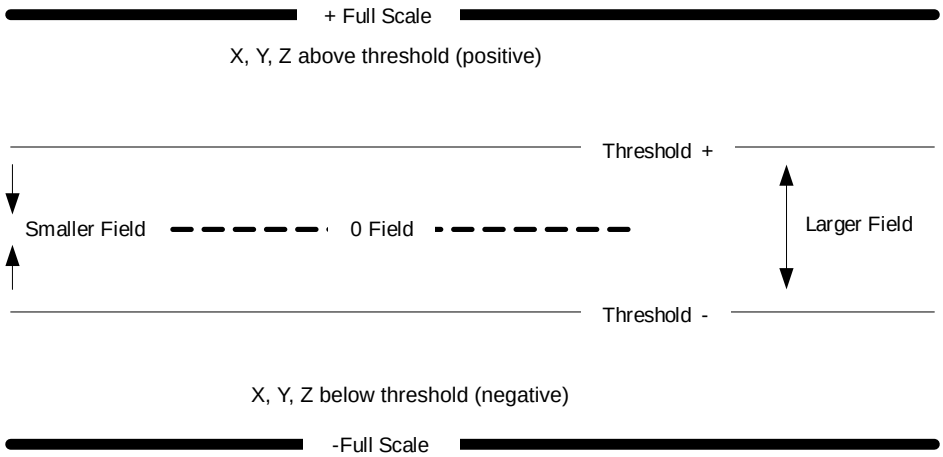


Figure 113. Illustration of magnetic threshold detection

9.16.2 M_THS_SRC (0x53) register

Magnetic threshold interrupt source register.

This register keeps track of the magnetic threshold event which is triggering (or has triggered, when M_THS_CFG[*m_ths_ele*] = 1) the event flag. In particular, if M_THS_SRC[*m_ths_ea*] is set to a logic '1' then the logical combination of magnetic event flags specified in M_THS_CFG is true.

m_ths_ea	—	m_ths_zhe	m_ths_zhp	m_ths_yhe	m_ths_yhp	m_ths_xhe	m_ths_xhp
0	0	0	0	0	0	0	0

Figure 114. M_THS_SRC register

Table 89. M_THS_SRC bit descriptions

Field	Description
m_ths_ea	Event active flag. 0: No event flag has been asserted 1: One or more event flag(s) has been asserted.
m_ths_zhe	Z-high event flag. 0: No event detected 1: Z-high event has been detected This bit always reads zero if the *m_ths_zefe* control bit is set to zero
m_ths_zhp	Z-high event polarity flag. 0: Z event detected was positive polarity 1: Z event detected was negative polarity This bit always reads zero if the *m_ths_zefe* control bit is set to zero
m_ths_yhe	Y-high event flag. 0: No event detected 1: Y-high event has been detected This bit always reads zero if the *m_ths_yefe* control bit is set to zero
m_ths_yhp	Y-high event polarity flag. 0: Y event detected was positive polarity 1: Y event detected was negative polarity This bit always reads zero if the m_ths_*yefe* control bit is set to zero
m_ths_xhe	X-high event flag. 0: No event detected 1: X-high event has been detected This bit always reads zero if the m_ths_*xefe* control bit is set to zero

Table 89. M_THS_SRC bit descriptions

m_ths_xhp	X-high event polarity flag. 0: X event detected was positive polarity 1: X event detected was negative polarity. This bit always reads zero if the *m_ths_xefe* control bit is set to zero

9.16.3 M_THS_X_MSB (0x54), M_THS_X_LSB (0x55), M_THS_Y_MSB (0x56), M_THS_Y_LSB (0x57), M_THS_Z_MSB (0x58), M_THS_Z_LSB (0x59) registers

The M_THS_X/Y/Z registers contain the unsigned 15-bit magnetic thresholds used by the magnetic threshold function. Each register has a resolution of 0.1 μT/LSB. The thresholds are evaluated after the magnetic data has been adjusted by the offset value stored in the M_OFF_X/Y/Z registers when M_CTRL_REG3[*m_raw*] = 0.

m_ths_dbcntm	m_ths_x[14:8]
0	0b0000000

Figure 115. M_THS_X_MSB register

Table 90. M_THS_X_MSB bit descriptions

Field	Description
m_ths_dbcntm	The *m_ths_dbcntm* bit configures the way in which the debounce counter is reset when the magnetic event of interest is momentarily not true. When *m_ths_dbcntm* = 1, the debounce counter is cleared to 0 whenever the magnetic event of interest is no longer true. When *m_ths_dbcntm* = 0, the debounce counter is decremented by 1 whenever the magnetic event of interest is no longer true.
m_ths_x[14:8]	Upper 7 bits of the 15-bit unsigned X-axis magnetic threshold.

m_ths_x[7:0]
0b00000000

Figure 116. M_THS_X_LSB register

—	m_ths_y[14:8]
0	0b0000000

Figure 117. M_THS_Y_MSB register

m_ths_y[7:0]
0b00000000

Figure 118. M_THS_Y_LSB register

N/A	m_ths_z[14:8]
0	0b0000000

Figure 119. M_THS_Z_MSB register

m_ths_z[7:0]
0b00000000

Figure 120. M_THS_Z_LSB register

9.16.4 M_THS_COUNT (0x5A) register

This register sets the number of debounce sample counts required before a magnetic threshold event is triggered.The behavior of the debounce counter is controlled by M_THS_X_MSB [*m_ths_dbcntm*].

m_ths_cnt[7:0]
0b00000000

Figure 121. M_THS_COUNT register

Table 91. M_THS_COUNT bit description

Field	Description
m_ths_cnt[7:0]	Magnetic threshold debounce count value.

When the internal debounce counter reaches the M_THS_COUNT value a magnetic event flag is set. The debounce counter will never increase beyond the M_THS_COUNT value. The time step used for the debounce sample count depends on the chosen ODR. When hybrid mode is enabled, the effective ODR is reduced by a factor of two, which increases the debounce counter time step by a factor of two from what is shown in Table 91.

Table 92. M_THS_COUNT relationship with the ODR This table needs to be re-done for this function. Ask design during review

ODR (Hz)	Max time range (s)				Time step (ms)			
	Normal	LPLN	High resolution	Low power	Normal	LPLN	High resolution	Low power
800	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
400	N/A	N/A	N/A	0.638	N/A	N/A	N/A	2.5
200	1.28	1.28	N/A	1.28	5	5	N/A	5
100	2.55	2.55	N/A	2.55	10	10	N/A	10
50	5.1	5.1	N/A	5.1	20	20	N/A	20
12.5	5.1	20.4	N/A	20.4	20	80	N/A	80
6.25	5.1	40.8	N/A	40.8	20	160	N/A	160
1.56	5.1	163	N/A	163	20	640	N/A	640

For example, an ODR of 100 Hz and a M_THS_COUNT value of 15 would result in a debounce response time of 150 ms. In hybrid mode, the same settings would result in a debounce response time of 300 ms.

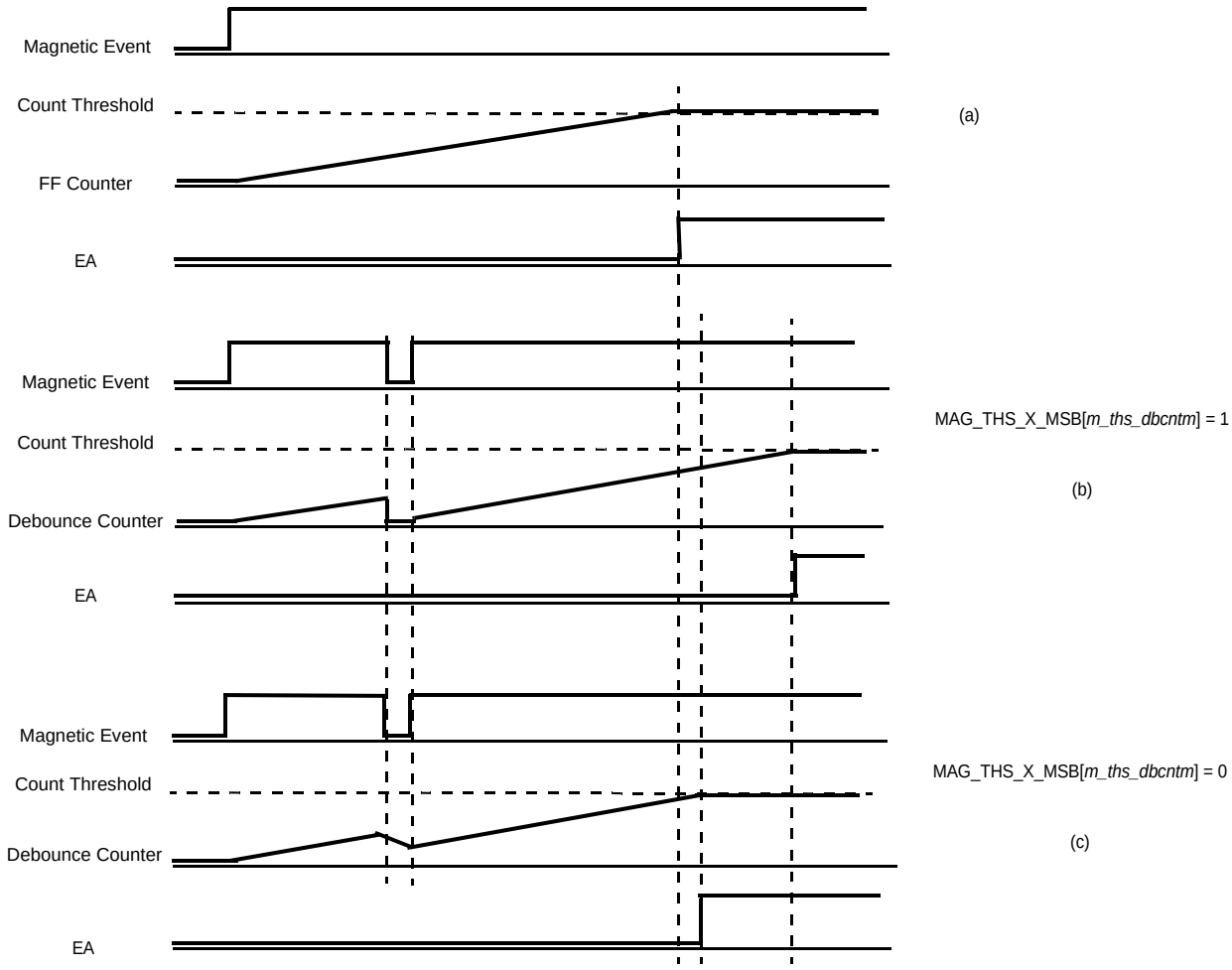


Figure 122. DBCNTM bit function

9.17 Magnetometer control registers

9.17.1 M_CTRL_REG1 (0x5B) register

m_acal	m_rst	m_ost	m_os[2:0]	m_hms[1:0]
0	0	0	0b000	0b00

Figure 123. M_CTRL_REG1 register

Table 93. M_CTRL_REG1 bit descriptions

Field	Description
m_acal	Magnetic hard-iron offset auto-calibration enable: 0: Auto-calibration feature disabled 1: Auto-calibration feature is enabled; the ASIC uses the maximum and minimum magnetic data to determine the hard iron offset value. The M_OFF_X/Y/Z registers are automatically loaded with (MAX_X/Y/Z + MIN_X/Y/Z)/2 for each axis at the end of every ODR cycle.
m_rst	One-shot magnetic reset de-gauss control bit: 0: No magnetic sensor reset is active 1: One-shot magnetic reset is enabled, hardware cleared when complete.

Table 93. M_CTRL_REG1 bit descriptions

m_ost	One-shot magnetic measurement mode: 0: No action taken, or one-shot measurement complete. 1: If device is in Active mode no action is taken. If device is in Standby mode, take one set of magnetic measurements, clear this bit, and return to Standby mode.
m_os[2:0]	Oversample ratio (OSR) for magnetometer data (see Table 95).
m_hms[1:0]	00 = Only accelerometer sensor is active 01 = Only magnetometer sensor is active 11 = Hybrid mode, both accelerometer and magnetometer sensors are active(1)

1. When operating in hybrid mode, the effective ODR for each sensor is half of the frequency selected in the CTRL_REG1[*dr*] and CTRL_REG1[*aslp_rate*] bit fields.

The *m_os*[2:0] OSR setting along with the system ODR value set in CTRL_REG1 sets the magnetic output data update rate.

When *m_hms*[1:0] = 2'b11, magnetic output data is available in registers M_OUT_X_MSB (0x33), M_OUT_X_LSB (0x34), M_OUT_Y_MSB (0x35), M_OUT_Y_LSB (0x36), M_OUT_Z_MSB (0x37), and M_OUT_Z_LSB (0x38) along with the time synchronized accelerometer data in CMP_X_MSB (0x39), CMP_X_LSB (0x3A), CMP_Y_MSB (0x3B), CMP_Y_LSB (0x3C), CMP_Z_MSB (0x3D), and CMP_Z_LSB (0x3E).

9.17.2 M_CTRL_REG2 (0x5C) register

—	—	hyb_autoinc_mode	m_maxmin_dis	m_maxmin_dis_ths	m_maxmin_rst	m_rst_cnt[1:0]
0	0	0	0	0	0	0b00

Figure 124. M_CTRL_REG2 register

Table 94. M_CTRL_REG2 bit descriptions

Field	Description
hyb_autoinc_mode	With *hyb_autoinc_mode* = 1 and fast-read mode is disabled (CTRL_REG1 [*f_read*] = 0), the register address will automatically advance to register x33 (M_OUT_X_MSB) after reading register x06 (OUT_Z_LSB) in burst-read mode. For *hyb_autoinc_mode* = 1 and fast read mode enabled (CTRL_REG1[*f_read* = 1) the register address will automatically advance to register x33 (M_OUT_X_MSB) after reading register x05 (OUT_Z_MSB) during a burst-read mode. Please refer to the register map auto-increment address column for further information.
m_maxmin_dis	Magnetic measurement max/min detection function disable: 0: Magnetic min/max detection function is enabled (default). 1: Magnetic min/max detection function is disabled. When enabled, the magnetic min/max detection function will update the MAX_X/Y/Z and MIN_X/Y/Z registers at the end of each ODR cycle with the maximum and minimum magnetic measurements from each axis. This is used along with the auto-cal feature (M_CTRL_REG1[*m_acal*] = 1) as a hardware based hard-iron offset compensation function.
m_maxmin_dis_ths	Magnetic measurement min/max detection function disable via magnetic threshold event trigger: 0: No impact to magnetic min/max detection function on a magnetic threshold event 1: Magnetic min/max detection function is disabled when magnetic threshold event is triggered
m_maxmin_rst	Magnetic measurement min/max detection function reset: 0: No reset sequence is active 1: Setting this bit resets the MIN_X/Y/Z and MAX_X/Y/Z registers to 0x7FFF and 0x8000, respectively (positive and negative full-scale values).This bit is automatically cleared after the reset is completed.
m_rst_cnt[1:0]	Magnetic auto-reset de-gauss frequency: 00: Automatic magnetic reset at the beginning of each ODR cycle (default). 01: Automatic magnetic reset every 16 ODR cycles. 10: Automatic magnetic reset every 512 ODR cycles. 11: Automatic magnetic reset is disabled. Magnetic reset only occurs automatically on a transition from Standby to Active mode, or can be triggered manually by setting M_CTRL_REG1 [*m_rst*] = 1

9.17.3 M_CTRL_REG3 (0x5D) register

m_raw	m_aslp_os[2:0]	m_ths_xyz_update	m_st_z	m_st_xy[1:0]
0	0b000	0	0	0b00

Figure 125. M_CTRL_REG3 register

Table 95. M_CTRL_REG3 bit descriptions

Field	Description
m_raw	Magnetic measurement RAW mode enable: 0: Values stored in the M_OFF_X/Y/Z registers are applied to the magnetic sample data. This bit must be cleared in order for the automatic hard-iron compensation function to have any effect. 1: Values stored in M_OFF_X/Y/Z are not applied to the magnetic sample data; automatic hard-iron compensation function does not have any effect on the output data.
m_aslp_os[2:0]	Defines magnetometer OSR in Auto-Sleep mode. See Table 95.
m_ths_xyz_update	This control bit defines which reference values are updated when the magnetic threshold event detection function triggers. 0: X, Y and Z reference values are all updated when the function triggers on any of the X, Y, or Z axes. 1: Only the reference value for the axis that triggered the detection event is updated.
m_st_z	Enables Z-axis magnetic self-test function when set to 1.
m_st_xy[1:0]	Enables both X and Y axes magnetic self-test function simultaneously when set to a value greater than 2'b00. X and Y magnetic self-test is disabled when this field is set to 2'b00.

Table 96. M-cell OSR versus ODR

ODR (Hz)	OSR = 0	OSR = 1	OSR = 2	OSR = 3	OSR = 4	OSR = 5	OSR = 6	OSR = 7
1.56	16	16	32	64	128	256	512	1024
6.25	4	4	8	16	32	64	128	256
12.5	2	2	4	8	16	32	64	128
50	2	2	2	2	4	8	16	32
100	2	2	2	2	2	4	8	16
200	2	2	2	2	2	2	4	8
400	2	2	2	2	2	2	2	4
800	2	2	2	2	2	2	2	2

9.17.4 M_INT_SRC (0x5E) register

—	—	—	—	—	src_m_ths	src_m_vecm	src_m_drdy
0	0	0	0	0	0	0	0

Figure 126. M_INT_SRC register

Table 97. M_INT_SRC bit description

Field	Description
src_m_ths	Magnetic threshold interrupt flag: 0: Magnetic threshold event has not been detected. 1: Magnetic threshold event has been detected.
src_m_vecm	Magnetic vector magnitude interrupt flag: 0: Magnetic vector magnitude change event has not been detected. 1: Magnetic vector magnitude change event has been detected.

Table 97. M_INT_SRC bit description

src_m_drdy	Magnetic data-ready interrupt flag: 0: No new magnetic data is available. 1: New magnetic data is available.

9.17.5 Magnetometer Vector Magnitude Function

The magnetometer vector magnitude function will generate an interrupt when $\sqrt{(m\_x\_out - m\_x\_ref)^2 + (m\_y\_out - m\_y\_ref)^2 + (m\_z\_out - m\_z\_ref)^2}$ > M_VECM_THS value and t > M_VECM_CNT value. Where m_x_out, m_y_out, and m_z_out are the current decimated magnetometer output values, and m_x_ref, m_y_ref, and m_z_ref are the internally latched reference values. The user may program the M_VECM_THS and M_VECM_CNT registers to establish the conditions needed to detect a magnetic vector magnitude change event. Depending on the values chosen for the reference values, this function may be configured to detect a magnetic field magnitude that is above a preset threshold (with reference values = 0), or a change in magnitude between two magnetic vectors greater than the preset threshold (with reference values non-zero). Please note x_ref, y_ref, z_ref are stored internally and are not observable by the user through the register interface. Please refer to Freescale application note AN4458.

9.17.6 M_VECM_CFG (0x69) register

—	m_vecm_ele	m_vecm_initm	m_vecm_updm	m_vecm_en	m_vecm_wake_en	m_vecm_init_en	m_vecm_init_cfg
0	0	0	0	0	0	0	0

Figure 127. M_VECM_CFG register

Table 98. M_VECM_CFG bit descriptions

Field	Description
m_vecm_ele	Magnetic vector magnitude event latch enable: 0: Event latch disabled 1: Event latch enabled With event latching enabled, the *src_m_vecm* interrupt flag may only be cleared by reading the M_INT_SRC register. With event latching disabled, the *src_m_vecm* interrupt flag is updated in real time and may be cleared by the ASIC prior to the user reading the flag.
m_vecm_initm	Magnetic vector magnitude initialization mode: 0: The ASIC uses the current magnetic output data as the initial reference values at the time the *m_vecm_en* bit is set. 1: The ASIC uses the data stored in the M_VECM_X/Y/Z_INIT registers as the initial reference values at the time the *m_vecm_en* bit is set.
m_vecm_updm	Magnetic vector magnitude reference value update mode: 0: The function updates the reference values with the current X/Y/Z magnetic data when the event is triggered. 1: The function does not update the reference values when the event is triggered. *Setting m_vecm_initm* = 1 and *m_vecm_updm* = 1 allows the user to manually update the reference values using the M_VECM_INIT_X/Y/Z registers in real time when the function is enabled.
m_vecm_en	Magnetic vector magnitude function enable: 0: Function is disabled. 1: Function is enabled, the ASIC will update the internal *m_x/y/z_ref* registers with either the current magnetic output data or the values stored in the M_VECM_INIT_X/Y/Z registers depending on the state of *m_vecm_initm*. **Note:** The magnetic vector magnitude function will only function correctly up to a maximum ODR of 400 Hz.
m_vecm_wake_en	Magnetic vector magnitude wake enable: 0: The system excludes the *src_m_vecm* event flag when evaluating the Auto-Sleep function. 1: The system includes the *src_m_vecm* event flag when evaluating the Auto-Sleep function.
m_vecm_int_en	Magnetic vector magnitude interrupt enable: 0: Magnetic vector magnitude interrupt is disabled. 1: Magnetic vector magnitude interrupt is enabled.
m_vecm_init_cfg	Magnetic vector magnitude interrupt configuration: 0: Magnetic vector magnitude interrupt is output on INT2 pin. 1: Magnetic vector magnitude interrupt is output on INT1 pin.

9.17.7 M_VECM_THS_MSB (0x6A) register

m_vecm_dbcntm	m_vecm_ths[14:8]
0	0b0000000

Figure 128. M_VECM_THS_MSB register

Table 99. M_VECM_THS_MSB bit descriptions

Field	Description
m_vecm_dbcntm	Magnetic vector magnitude debounce counter mode selection: 0: The debounce counter is decremented by 1 whenever the current vector magnitude result is below the threshold set in M_VECM_THS. 1: The debounce counter is cleared whenever the current vector magnitude result is below the threshold set in M_VECM_THS.
m_vecm_ths[14:8]	Seven most significant bits of 15-bit unsigned magnetic vector magnitude threshold. Resolution is 0.1 μT/LSB.

9.17.8 M_VECM_THS_LSB (0x6B) register

m_vecm_ths[7:0]
0b00000000

Figure 129. M_VECM_THS_LSB register

9.17.9 M_VECM_CNT (0x6C) register

m_vecm_cnt[7:0]
0b00000000

Figure 130. M_VECM_CNT register

Table 100. M_VECM_CNT bit description

Field	Description
m_vecm_cnt[7:0]	Magnetic vector magnitude debounce count value. The debounce timer count period is set by the current ODR. For example, with M_VECM_CNT = 15 and an ODR of 100 Hz selected, the debounce is set to 150 ms. When operating in hybrid mode, the effective ODR is reduced by a factor of two, making the debounce time for this example 300 ms.

9.17.10 M_VECM_INITX_MSB (0x6D) register

m_vecm_initx[15:8]
0b00000000

Figure 131. M_VECM_INITX_MSB register

Table 101. M_VECM_INITX_MSB bit description

Field	Description
m_vecm_initx[15:8]	MSB of signed 16-bit initial X-axis value used by the magnetic vector magnitude function when M_VECM_CFG[*m_vecm_initm*] = 1.

9.17.11 M_VECM_INITX_LSB (0x6E) register

m_vecm_initx[7:0]
0b00000000

Figure 132. M_VECM_INITX_LSB register

Table 102. M_VECM_INITX_LSB bit description

Field	Description
m_vecm_initx[7:0]	LSB of signed 16-bit initial X-axis value used by the magnetic vector magnitude function when M_VECM_CFG[*m_vecm_initm*] = 1.

9.17.12 M_VECM_INITY_MSB (0x6F) register

m_vecm_inity[15:8]
0b00000000

Figure 133. M_VECM_INITY_MSB register

Table 103. M_VECM_INITY_MSB bit description

Field	Description
m_vecm_inity[15:8]	MSB of signed 16-bit initial Y-axis value used by the magnetic vector magnitude function when M_VECM_CFG[*m_vecm_initm*] = 1.

9.17.13 M_VECM_INITY_LSB (0x70) register

m_vecm_inity[7:0]
0b00000000

Figure 134. M_VECM_INITY_LSB register

Table 104. M_VECM_INITY_LSB bit description

Field	Description
m_vecm_inity[7:0]	LSB of signed 16-bit initial Y-axis value used by the magnetic vector magnitude function when M_VECM_CFG[*m_vecm_initm*] = 1.

9.17.14 M_VECM_INITZ_MSB (0x71) register

m_vecm_initz[15:8]
0b00000000

Figure 135. M_VECM_INITZ_MSB register

Table 105. M_VECM_INITZ_MSB bit description

Field	Description
m_vecm_initz[15:8]	MSB of signed 16-bit initial Z-axis value used by the magnetic vector magnitude function when M_VECM_CFG[*m_vecm_initm*] = 1.

9.17.15 M_VECM_INITZ_LSB (0x72) register

m_vecm_initz[7:0]
0b00000000

Figure 136. M_VECM_INITZ_LSB register

Table 106. M_VECM_INITZ_LSB bit description

Field	Description
m_vecm_initz[7:0]	LSB of signed 16-bit initial Z-axis value used by the magnetic vector magnitude function when M_VECM_CFG[*m_vecm_initm*] = 1.

10 Mounting Guidelines for the Quad Flat No Lead (QFN) Package

Printed Circuit Board (PCB) layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the PCB and the package. With the correct footprint, the packages will self-align when subjected to a solder reflow process.

These guidelines are for soldering and mounting the Quad Flat No-Lead (QFN) package inertial sensors to PCBs. The purpose is to minimize the stress on the package after board mounting. The FXOS8700CQ uses the QFN package platform. This section describes suggested methods of soldering these devices to the PCB for consumer applications.

10.1 Overview of soldering considerations

Information provided here is based on experiments executed on QFN devices. They do not represent exact conditions present at a customer site. Hence, information herein should be used for guidance only and process and design optimizations are recommended to develop an application specific solution. It should be noted that with the proper PCB footprint and solder stencil designs, the package will self-align during the solder reflow process.

10.2 Halogen content

This package is designed to be Halogen Free, exceeding most industry and customer standards. Halogen Free means that no homogeneous material within the assembly package shall contain chlorine (Cl) in excess of 700 ppm or 0.07% weight/weight or bromine (Br) in excess of 900 ppm or 0.09% weight/weight.

10.3 PCB mounting recommendations

1. The PCB land should be designed with Non-Solder Mask Defined (NSMD) as shown in Figure 138 and Figure 139
2. No additional via pattern underneath package.
3. PCB land pad is 0.8 mm by 0.3 mm as shown in Figure 138 and Figure 139.
4. Solder mask opening = PCB land pad edge + 0.113 mm larger all around.
5. Stencil opening = PCB land pad -0.015 mm smaller all around = 0.77 mm by 0.27 mm.
6. Stencil thickness is 100 or 125 µm.
7. Do not place any components or vias at a distance less than 2 mm from the package land area. This may cause additional package stress if it is too close to the package land area.
8. Signal traces connected to pads are as symmetric as possible. Put dummy traces on NC pads in order to have same length of exposed trace for all pads.
9. Use a standard pick and place process and equipment. Do not use a hand soldering process.
10. Do not use a screw down or stacking to fix the PCB into an enclosure because this could bend the PCB, putting stress on the package.
11. The PCB should be rated for the multiple lead-free reflow condition with max 260°C temperature.
12. No copper traces on top layer of PCB under the package. This will cause planarity issues with board mount. Freescale QFN sensors are compliant with Restrictions on Hazardous Substances (RoHS), having halide-free molding compound (green) and lead-free terminations. These terminations are compatible with tin-lead (Sn-Pb) as well as tin-silver-copper (Sn-Ag-Cu) solder paste soldering processes. Reflow profiles applicable to those processes can be used successfully for soldering the devices.

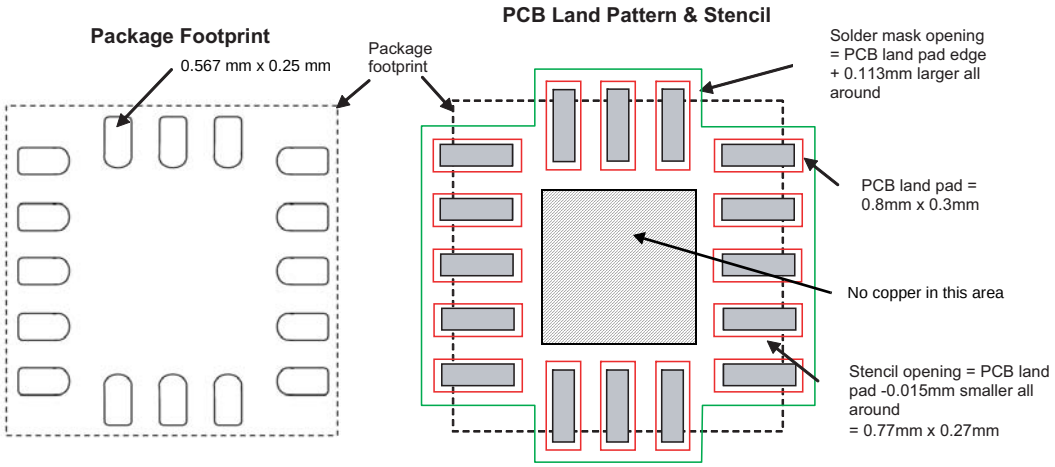


Figure 137. Recommended PCB land pattern, solder mask, and stencil opening near package footprint

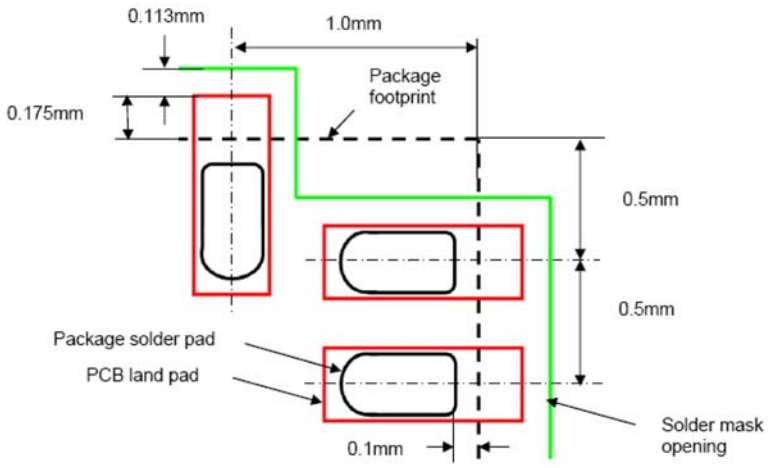
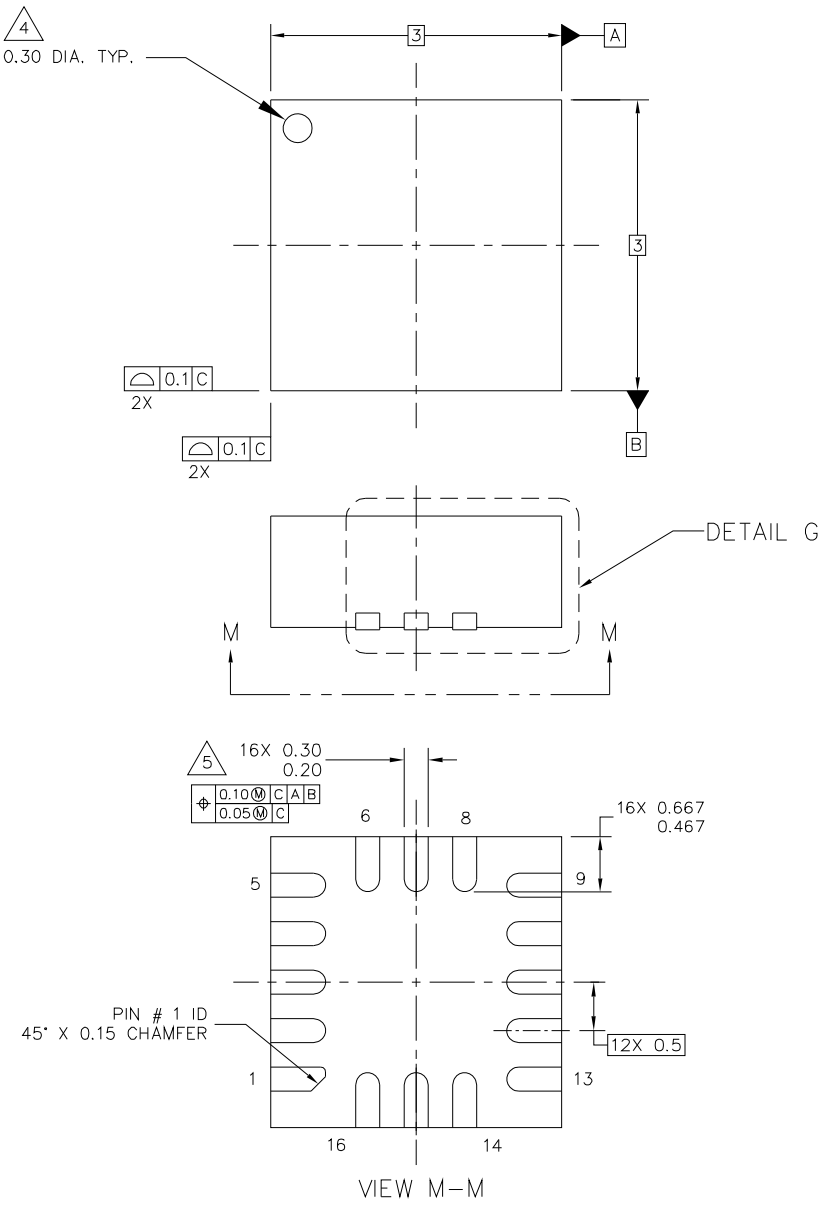


Figure 138. Detailed dimensions

11 Package



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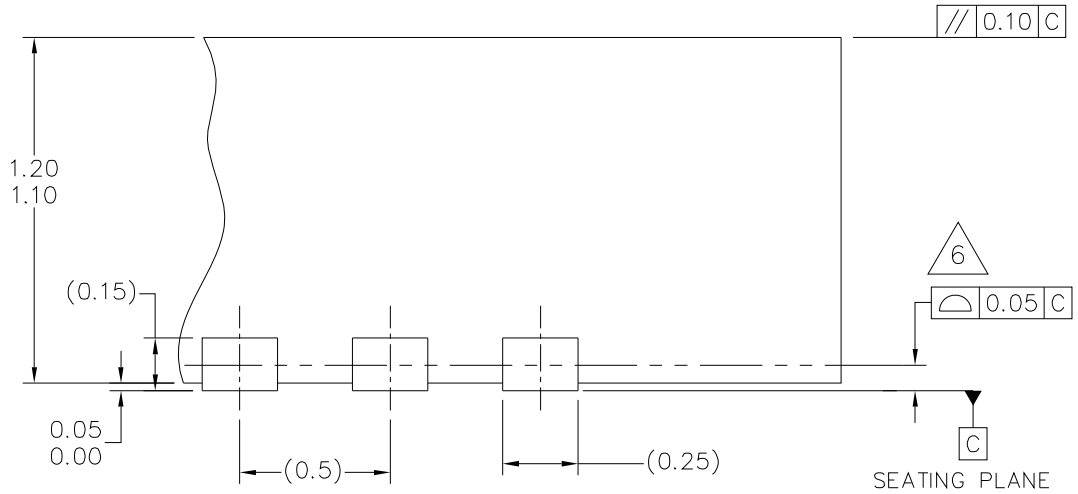
	CASE NUMBER: 2188–01	02 MAR 2011
	STANDARD: NON JEDEC	

CASE 2188-01
ISSUE O
16 LEAD QFN



DETAIL G

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	CASE NUMBER: 2188-01	02 MAR 2011
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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THIS IS NON JEDEC REGISTERED PACKAGE.
4. PIN #1 ID ON TOP WILL BE LASER MARKED.
5. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THIS DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
6. COPLANARITY APPLIES TO LEADS AND ALL OTHER BOTTOM SURFACE METALLIZATION.
7. MIN. METAL GAP SHOULD BE 0.2MM.

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	CASE NUMBER: 2188–01	02 MAR 2011
	STANDARD: NON JEDEC	

CASE 2188-01
ISSUE O
16 LEAD QFN

Table 107. Revision history

Revision number	Revision date	Description of changes
0.1	05/2012	• Corrected Figure 1 and updated Figure 4 to include acceleration values.
0.2	05/2012	• Added Autonomous sub-bullets to first page. • Table 2: Changed Cross-axis Max value to ±0.5 and Die-to-package alignment error Max value to ±2. • Table 13: WHO_AM_I register, Default Hex Value numbers changed from 0xC4/0xC7 to 0xC7 removed Note 4 and 5. • Section 9.1.7, WHO_AM_I register changed register numbers in Figure 16 from 0xC4/0xC7 to 0xC7
0.3	05/2012	• Table 2: Changed Nonlinearity values to TBD. Added Test Conditions for Noise rows. • Table 3: Added Min values for Self-test output change for X-axis and Y-axis rows. • Table 5: Updated ODR values for Low-power acceleration mode, Normal-acceleration mode, Hybrid mode and Magnetic mode. Added max value for IddSTBY, Standby mode; added Typ values for VIH and VIL, all previously TBD. Added Typ value for 25° SCL, SDA pin leakage. • Added Section 7.5, Hybrid mode. • Table 13:. Deleted registers 0x79, 0x7A, 0x7B and 0x7C, • Table 50: Updated a_ffmt_ths_xyz_en description. • Table 51: Updated a_ffmt_trans_ths_en description. • Updated descriptive paragraph for Section 9.11.3. • Updated descriptive paragraph for Section 9.11.4.
1	06/2012	• Changed title of document. • Table 3: updated Note 2. Tco spec updated, Hysteresis value updated, Updated Noise values for ODR = 6.25 Hz, OS = 256 and ODR = 1.56 Hz, OS = 1024. Updated Vst X-axis Typ value from -1500 to -1320 and Z-axis from TBD to 100. • Table 4: Removed first 2 rows, X, Y, Z inertial alignment parameters and Typ values. • Table 8: Added SCL, SDA pin leakage Typ value 4 nA, added SCL, SDA pin capacitance 3 pf. • Replace Table 8 with updated parameters. • Updated section 5.2 SPI interface characteristics. • Table 94: updated m_st_xy[1:0] bit description.

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