

Colloquium: Advances in automation of quantum dot devices control

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Arrays of quantum dots (QDs) are a promising candidate system to realize scalable, coupled qubits systems and serve as a fundamental building block for quantum computers. In such semiconductor quantum systems, devices now have tens of individual electrostatic and dynamical voltages that must be carefully set to localize the system into the single-electron regime and to realize good qubit operational performance. The mapping of requisite dot locations and charges to gate voltages presents a challenging classical control problem. With an increasing number of QD qubits, the relevant parameter space grows sufficiently to make heuristic control unfeasible. In recent years, there has been a considerable effort to automate device control that combines script-based algorithms with machine learning (ML) techniques. In this Colloquium, we present a comprehensive overview of the recent progress in automation of QD device control, with a particular emphasis on silicon- and GaAs-based QDs formed in two-dimensional electron gases. Combining physics-based modeling with modern numerical optimization and ML has proven quite effective in yielding efficient, scalable control. Further integration of theoretical, computational, and experimental efforts with computer science and ML holds tremendous potential in advancing semiconductor and other platforms for quantum computing.

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I. QUANTUM DOT DEVICES: HISTORY AND OVERVIEW

The electron is the simplest natural quantum bit. It is spin-1/2 and comes with an electric charge, enabling trapping and moving of the particle, much like an ion. Furthermore, Kramer’s theorem provides an assurance that this simple structure is maintained even in the complex environment of a condensed matter system, specifically the spin-1/2 property. This means that one can leverage the vast array of condensed matter and solid state research and the corresponding industry that has developed around the control of electrons, particularly in the case of semiconductors. Quantum dots (QDs) are one such approach for isolating and controlling single electrons using semiconductor physics (Hanson *et al.*, 2007; Loss and DiVincenzo, 1998; van der Wiel *et al.*, 2002; Zwanenburg *et al.*, 2013).

Interest in QDs goes well beyond quantum computing, from direct current (DC) standard to low-power logic to thermometry at low temperatures (Likharev, 1999). Working at the single-electron level with both orbital and spin coherence represents the edge of the possible in semiconductors, and thus quantum computing with semiconductor QDs has proven to be a fruitful domain

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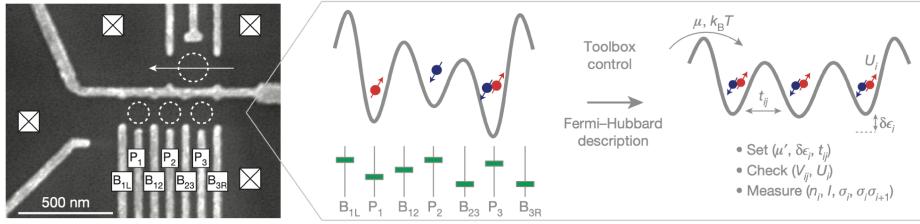


FIG. 1 Electron micrograph of a gate-defined triple QD array in GaAs (left). The bottom three dashed circles indicate the qubit QD array while the single dashed circle with an arrow indicates the sensing dot channel. The goal of tuning QD devices (right): setting a desired Hamiltonian through the efficient control of voltages applied to all gates to enable fine control of QD qubits. The final form maps to (variants of) the Hubbard model, where the parameters of detuning, charge interaction, and tunneling are all controlled by gate voltages. From Hensgens *et al.* (2017).

to develop new techniques and uses of isolated electronic systems, while maintaining their promise as a pathway to quantum computing (Watson *et al.*, 2018).

Unfortunately, the difficulty of working with such systems—where fabrication tolerances are tight, impurities punishing, and material considerations vast—has meant that only a few groups around the world have succeeded in advancing the limit of QD performance. Surprisingly, many of the fabrication and materials challenges have been surmounted with engineering and by a practice of sharing results and even materials and samples throughout the academic community. The biggest remaining challenge is reducing the difficulty of arranging the depletion and accumulation of electrons in a nano-scale semiconductor system such that the right number of isolated islands (QDs) with the right number of electrons (charge state) in the right connection network (topology) is realized every time the system is cooled down and initiated.

This task is surprisingly hard. A typical gate-based semiconductor QD uses between four and six local depletion and/or accumulation gates to form a single island, see Fig. 1. If one seeks to build an array of such devices in close proximity—such that individual electrons can coherently tunnel between islands as is necessary for most quantum computing implementations—the number of gates scales as some polynomial in at least the square root of the number of QDs, and typically scales linearly.

In order to reach a stable few-electron configuration, early experiments set the input voltages heuristically. However, such an approach does not scale well with growing array sizes and is susceptible to random errors. Moreover, since the parameter space exploration strongly relies on intuition and experience, such tuning may result in only an acceptable rather than an optimal state. Finally, the size of the relevant space of parameters that need to be adjusted with an increasing number of QD qubits makes heuristic control even more challenging. As a result, there has been great interest in exploring the potential of machine learning (ML) to solve the auto-tuning problem.

Let us now consider the specific challenges of bringing a device into the desired operating regime. An essential ingredient on any tuning procedure is determining the ‘state’ of the device (topology, number of charges, parameters such as tunneling rates, etc.). However, measuring these devices is non-trivial. In general, the field has progressed by exploratory measurement of electrical currents through nearby circuits. These techniques rely upon the variable conductance of the underlying semiconductor, which in turn depends upon the local electric field produced, e.g., by nearby electrical gates and by electrons that are trapped in QDs themselves. The probe systems must be nearby as screening of the electric field from nearby metallic regions reduces long-range coupling, and corresponding current flows are generally small (in the nanoampere range).

These current-flow approaches more commonly use an auxiliary QD or quantum point contact to act as a sensor of the local electric field, and are sufficiently sensitive to measure the change in the local potential landscape to the addition or subtraction of a single nearby charge (Simmons *et al.*, 2007). Their ability to work independent of coupling of the QDs in the main device (by use of virtual gates, below) provides substantial engineering simplicity in creating and tuning QD devices.

In addition to charge-based measurement, there are two other measurement techniques. The first was more common in the earlier era of the field: directly measuring the current flow through the QD of interest (Hendrickx *et al.*, 2020; Maurand *et al.*, 2016). This relies upon finding degeneracies between all the relevant charge configurations in the QDs such that electrons can freely flow from a source to a drain. However, these are not as useful for tuning to the single-electron regime, as the current flow through the devices typically get small as one approaches that regime, and tuning to these degeneracy points becomes increasingly challenging as the number of devices in series increases. Nonetheless, some ML-based auto-tuning techniques operate directly on current flow data (van Esbroeck *et al.*, 2020).

Finally, there are some new directions in measuring

devices that may have merit for future ML efforts. Of particular interest is the addition of circuit quantum electrodynamic techniques to the toolbox, in which the local response of the QD system to an applied microwave or radio frequency field causes the field to have a phase shift; in essence, the QD system acts as a (variable) capacitor in some resonant circuit (Crippa *et al.*, 2019; Mi *et al.*, 2017a). Thus, even though no current flows through the QDs, one can directly measure the local properties about the response of energy levels to the applied fields. This has shown promise outside the ML space for “tuning”, as it enables estimating other properties such as valley degeneracy in silicon devices (Mi *et al.*, 2017b).

This Colloquium begins with an overview of QD qubits, followed by a discussion of the Hubbard model representation of the QD system and a high-level overview of the QD tuning sub-processes that take a system from room temperature to quantum operation. Several key metaproblems related to scalability and tuning in the presence of imperfections are also discussed. The concept and methods of tuning QD devices are presented in Sec. III. Section IV concludes the Colloquium with a summary and outlook, including some interesting questions related to scaling up and “on-chip” implementations of the auto-tuning systems.

II. QUANTUM DOT DEVICES TODAY

QD qubits are systems in which the internal quantum-mechanical degrees of freedom of a QD system are manipulated in order to perform qubit operations. There are three main types of QD qubits in semiconducting QDs: *charge qubits*, *spin qubits*, and *composite qubits* (such as singlet-triplet, ‘exchange-only’, or hybrid qubits). For charge qubits, the logical states of the system are defined by different charge occupations of adjacent tunnel coupled QD (Gorman *et al.*, 2005; Kim *et al.*, 2015; Petersson *et al.*, 2010). In spin qubits, the different individual spin configurations of the same charge configuration define the logical states, with up and down defined relative to a uniform external magnetic field (DiVincenzo *et al.*, 2000a; Loss and DiVincenzo, 1998). Finally, for composite qubits, the logical states of the qubit are defined by symmetry operations on spin configurations resulting from having two, three, or even four electrons distributed between two, three, or four QDs (Cao *et al.*, 2016; DiVincenzo *et al.*, 2000b; Petta *et al.*, 2005; Russ and Burkard, 2017; Shi *et al.*, 2012; Wu *et al.*, 2014); again, the qubit is encoded in spin degrees of freedom, though these are representations of the symmetric group rather than the Kramer’s doublet. In all cases, the critical task of getting a QD system into a regime in which qubits can be realized has mostly common features, with only minor changes at the final stage of tuning to distinguish between the different qubit types.

In many respects, this paper is focused on developing the tools to get one to a regime in which the above qubit types can be reliably realized. From a systems engineering perspective, a useful intermediate representation of the system is the (multi-band) Hubbard model, in which individual quantum dots labeled with index i are allowed to have zero, one, or two electrons on them at a time, with fermionic annihilation operator $c_{i,\sigma}$, with $\sigma = \pm 1/2$ the spin. Writing it out, we have

$$H = - \sum_{ij} t_{ij} c_{i,\sigma}^\dagger c_{j,\sigma} + \sum_i (n_i - \epsilon_i) U_{ij} (n_j - \epsilon_j) + H_B \quad (1)$$

where the first sum is over quantum dots that are tunnel coupled with tunneling energy t_{ij} to each other. The second term incorporates both charge offsets due to gate voltages ϵ_i and also the inverse capacitance matrix $\sim U_{ij}$ which determines the lowest energy charge configuration. The last term H_B is the magnetic field Hamiltonian for the spins only, and typically includes both a uniform component and a local (gradient) component. Thus the automated procedures can attempt to directly extract the functional dependence of the tunneling (t_{ij}) and capacitance (U_{ij}) terms on the device parameters such as gate voltages, as well as further voltage dependencies in ϵ_i .

To get to this Hubbard abstraction, we now consider a typical gate-defined QD device in GaAs, shown in Fig. 1. The different metal gate electrodes are intended to serve different functions in forming and controlling the QD qubits by depleting or accumulating electrons in the semiconductor underneath the gates. The so-called “finger” gates, named for their resemblance to fingers on a hand, control the tunnel coupling with the reservoirs Γ_i (controlled by B_{1L}, B_{3R}), the inter-dot tunnel couplings t_{ij} (controlled by $B_{i,i+1}$, $i = 1, 2$), and are used to set the electron number in each dot by changing the local electrostatic potential (controlled by P_i , $i = 1, 2, 3$). However, in practice, each gate influences the other parameters as well (cross-talk), as we will discuss. In the typical setting, one of the quantum dot regions is separated out from the others (top area of Fig. 1) and is used as a local probe of the electrostatic environment, thus measuring changes in the number of nearby charges. This measurement system allows assessment of the rest of the device and provides a helpful abstraction from currents and conductances.

Once the measurement dot is operational, throughout tuning and calibration, the state of the device is assessed via a series of one-dimensional (1D) sweeps of a particular gate, see Fig. 2(a)(i, iii), or two-dimensional (2D) scans in the space of two gates of interest, see Fig. 2(a)(ii, iv). The signal in those plots represent either the flow of current through pairs of ohmic contacts to leads and the direct transport current through the QD, e.g., before tuning up the measurement dot, or the current through the charge sensor. The latter type of measurement is necessary to resolve electron tunneling in real time.

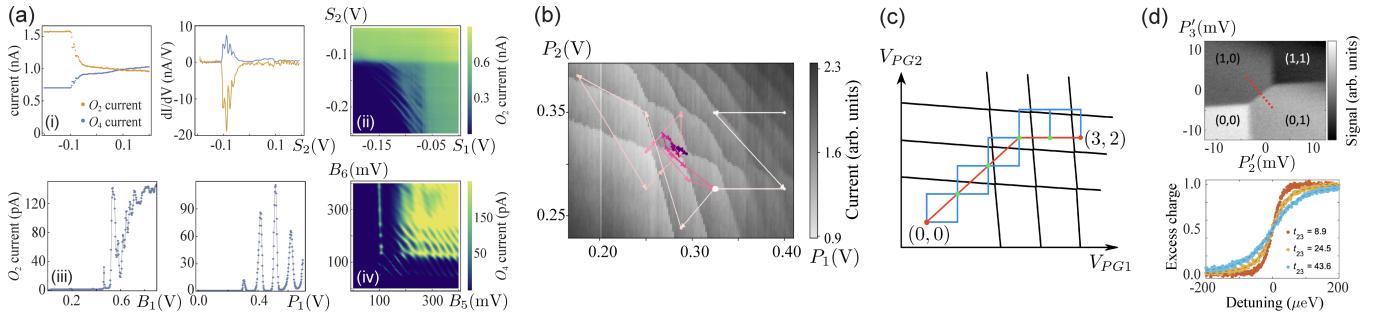


FIG. 2 The auto-tuning flow. (a) Sample plots used in the bootstrapping phase described in Sec. III.A. (i) Pinch-off measurement (left) and the numerical derivative of the measurement (right) for the central screening gate used to divide the 2DEG into two half-planes. Current through both the qubit and sensor side of the QD system is measured as the gate is swept to negative voltages. (ii) Example triangle plot of the qubit dot channel. The large rectangular regions to the right and top represent current flow underneath two screening gates. (iii) A series of pinch-off curves for finger gates showing Coulomb blockade oscillations. (iv) The so-called “wall-wall” plot in the space of the two barriers defining the sensor. From McJunkin (2021). (b) Visualization of a state tuning run in the the space of two plunger gates, with arrows and the intensity of the color indicating the progress of the autotuner. From Zwolak *et al.* (2020b). (c) A cartoon of a possible path (red line) connecting the (0,0) and the (3,2) charge state. From Durrer *et al.* (2020). (d) (top) Charge stability diagram in the space of virtual gates with a red dotted line indicating the inter-dot detuning axis. (bottom) Excess charge extracted from a fit to the sensing dot signal as a function of detuning along the dotted line for three different t_{23} . From Hsiao *et al.* (2020).

The complete process of tuning an unknown QD device can be divided into a sequence of distinct phases shown in Fig. 2. There have been numerous attempts at automating each of those phases, as we discuss in Sec. III. Here, we present a high level overview of what each of those phases encompasses and the desired output for each.

Bootstrapping. Bootstrapping (or initialization) is a pre-tuning process that involves cooling the device down, making local sensing systems operational, and bringing the main device regime into an appropriate parameter range for taking data (i.e., measurement setup). This might include bringing charge sensors into operation and preparing a 1D channel where dots are going to be formed in the two-dimensional electron gas (2DEG). Finally, bootstrapping can build a “sandbox” of acceptable parameter variations by checking the finger gates for response and pinch-off voltages and determining the safety ranges for coarse tuning.

Coarse tuning. Coarse tuning is a process of finding a range of gate voltages where the device is in a particular global configuration corresponding to a set of charge islands (QDs) with an understanding of their connectivity, i.e., which island is tunnel coupled to which. In simple devices, this corresponds to an estimate, e.g., of no dot, single dot, or double dot regimes. As such, it can be thought of as defining the device topology in the state space. At the end of this phase, the QD device should be in a stable global configuration of known topology. This topology is the output of the coarse tuning process.

Establishing controllability. Ideally, changing voltages on

a single gate would affect only the parameter it is designed to control (e.g., the electrochemical potential of a specific QD or the tunnel barrier between two adjacent QDs). However, the capacitive cross-talk between the various gate electrodes—i.e., a situation in which a signal on one gate causes a smaller version of the same signal on an adjacent gate because of the capacitance between them—makes it difficult (if not impossible) to vary just a single parameter without affecting the others. One way to compensate for the capacitive cross-talk is to implement so-called virtual gates, that is linear combinations of multiple QD gate voltages chosen to address only a single electrochemical potential or tunnel barrier. Virtual gates are the output of the establishing controllability phase.

Charge state tuning. While at the end of the coarse tuning phase the device is in a definitive global state (i.e., single or double QD), the number of charges on the dots is at this point unknown. Since each QD qubit type requires a specific charge configuration, the goal of charge state tuning is to bring the QD device to a specific charge configuration, i.e., the specified number of charges (typically 1 to 3) on the specified islands.

Fine tuning. The final, fine tuning phase of calibrating QD devices focuses on adjusting the inter-dot tunnel coupling, which directly translates to control over the exchange coupling. This is necessary for realizing the various proposals for charge- and spin-based qubits. The output of the fine tuning system should, ideally, be a range of parameters that enable high fidelity quantum gates on the quantum

bits stored within each dot or multi-dot qubit.

Beyond these elements, there are several key metaproblems to be addressed by future work. The most prominent is related to the ability to scale QD devices. Specifically, to what extent can we take a tuning system for one of the above tasks, and while holding a portion of the QD device tuned, tune up a different portion of the device? For example, in a long array of QDs, one might first tune up a nearby charge sensor. Then one might tune a double QD.

What if one seeks to add another QD to the chain? This inductive tuning problem has been shown to work experimentally (Volk *et al.*, 2019), but theoretically there are substantial open questions about the ability to rapidly and reliably tune a large 1D array. As an example of why this is challenging, it is often the case in higher dimensional arrays for there to be charge configurations that are lower in energy than the current configuration but that the device does not reach due to metastability—that is, there is no easy way for an electron at, say, the edge of the QD device to make its way to the relevant QD near the center of the device to let the system relax to its true charge ground state. This metastability in turn can lead to hysteresis when tuning QD devices.

A second key metaproblem is how such tuning systems behave in the presence of real world imperfections. From the efficiency standpoint, it would be beneficial to determine whether the devices in a wafer are suitable for tuning prior to the wiring and cool-down. This is particularly important for high-throughput production, where individual wafers may contain hundreds or even thousands of devices. A path towards automated lithographic quality assessment of QD devices has recently been put forward by Mei *et al.* (2021). The proposed control system relays on convolutional neural networks (CNN) applied to scanning electron microscope (SEM) micrographs collected in-line to assess the device usability based on detection of certain fabrication defects (e.g., particle contamination, proper exposure). However, while this is an important step towards streamlining QD devices fabrication quality control, there is a number of other imperfections need to be accounted for. These include variations in a single QD device over time, between cool-downs, and between changes in the control systems and other aspects of the integrated experimental system. This naturally fits into an online learning model, in which the running experiment is continually changing. At the same time, the practical capabilities that subsystems that are pretrained provide may need adaptation or replacement once these concerns are integrated.

Put simply, tuning up a multi-thousand QD device can only be accomplished if the systems can be solved semi-independently (using recursive or inductive solutions). It must be done repeatably, in the presence of expected noise, respond appropriately to unexpected events, and

quickly enough to maintain its final state before going “out of tune.” A large scale system achieving these tasks is the main target for future research in this direction.

As a concluding note for this section, there are a variety of ways to trap individual electrons in a semiconductor system. In this work, we focus on devices where the electric field plays a key role in accumulating or depleting regions of a semiconductor, all the way down to the single-electron level. This encompasses a large variety of different technologies and materials. In many cases, these systems have qualitative similarities. However, there are both large and subtle differences that can make “porting” a tuning method from one material (e.g., GaAs) to another (such as silicon-based QD) more complex or even likely to fail. For example, in fine tuning, silicon devices have valley degeneracy and a large effective electron mass, leading to substantially different behavior in the 0.1 meV energy scales of orbital and related physics. As another example, devices with electrons close to oxide interfaces are known to have a large probability of so-called spurious dots, in which an impurity or defect causes the formation of a charge trap which can impact the controllability and measurability of the QDs. Finally, differences in noise, dielectric properties, and gate geometries mean that each application of a tuning method must generally be targeted towards both a specific material and a specific approach to QD formation. In what follows, we focus on silicon- and GaAs-based quantum dots formed in 2DEGs, but note that many of these techniques can be generalized, with the above proviso.

III. TOWARDS FULL AUTOMATION OF DEVICE CONTROL

The tuning process is an essential, albeit repetitive, step for initialization of QD-based qubits. Historically, tuning of QD devices has been performed manually based on heuristics, experimental intuition, and informed guesses. Such techniques, however, present practical difficulties in implementation when the number of gates increases beyond a modest number. Moreover, they require extensive training of each new researcher involved which is time consuming and thus significantly affects the pace at which new discoveries can be made. It has, thus, become apparent that a manual approach to finding suitable gate voltages to electrostatically confine the necessary number of electrons is unfeasible. Large-scale quantum processors require fully autonomous tuning processes that can be parallelized for practical applications.

There have been several attempts at automation of the various steps of the tuning process over the past decade. The initial script-based approaches rely on appealingly intuitive and relatively easy to implement conventional algorithms. They typically involve a combination of techniques from regression analysis, pattern matching, and

quantum control theory. However, the defects and variations in the local composition of the heterostructure as well as fabrication variances which disorder the background potential energy make semi-automated control challenging. The random disorder that must be compensated for by different gate voltages when defining quantum dots further impedes the script-based tuning process. None of the proposed approaches to date fully eliminates the need for human intervention, as the decision of how to adjust gate voltages, based on the automatically obtained quantitative dot parameters and qualitative output, remains heuristic. More importantly, these approaches are typically calibrated to a particular device architecture (or even a specific device), are susceptible to noise, and do not transfer well to other devices (Baart *et al.*, 2016).

More recently, researchers began to take advantage of the tools provided by the field of artificial intelligence and, more specifically, supervised and unsupervised ML. ML is a branch of computer science that focuses on the use of data and various specially designed algorithms to imitate the way humans learn. Throughout training, an ML algorithm learns or, in some applications, discovers patterns in data without being explicitly programmed about the characteristic features of those patterns. Thus, if provided with proper training data, ML-enhanced methods have the flexibility of being applicable to various devices without any adjustments or re-training. By learning from the data, ML algorithms are more adjustable to new devices than script-based methods. However, ML models typically require large labeled datasets for training and often lack information on the reliability of the ML prediction (Darulová *et al.*, 2021; Zwolak *et al.*, 2018).

While the problem of estimating and tuning systems is generically challenging, QD-based devices do benefit from having a variety of distinct problems and means of estimation that are sufficiently mature to enable application of specific ML techniques to various sub-problems without requiring a holistic solution. However, there may be some benefits to considering a holistic approach, particularly in low information settings as considered in (Moon *et al.*, 2020).

In the following sections, we describe advances in QD auto-tuning, focusing on five main phases of the tuning process discussed in Sec. I. In general, all techniques used for automation follow one of the two main schools of thought: computer-supported, script-based gate control and ML-driven methods.

A. Bootstrapping and sandboxing quantum dot device

The mobility of electrons (or holes) as well as (many-body) interactions between an isolated spin trapped in a QD and the sea of nearby spins in the 2DEG are often

strongly dependent on a variety of parameters. Of particular relevance for observing quantum coherent behavior is the overall temperature of the device, as charge-phonon coupling prevents coherent behavior at moderate temperatures and more interesting (and necessary) effects such as resolution of excited electronic states in an individual QD become impossible for temperatures well above the energy regime of interest. Thus in general, the weaker the interaction, the colder the 2DEG has to be in order to observe it. For example, the smallest energy splitting in silicon QDs—the valley splitting—is typically 10 to 300 μeV for Si/Si_xGe_{1-x} (Borselli *et al.*, 2011; Simmons *et al.*, 2010) and about 300-800 μeV for SiMOS (Yang *et al.*, 2013), which is very small compared to room temperature (1 Kelvin is 87 μeV). Cooling the device down is the first step of the bootstrapping phase. The usual technique for cooling 2DEG samples to the temperature required for an experiment is to use a Helium-3 cryostat or more commonly a dilution refrigerator. Once the sample is sufficiently cooled, pre-tuning and functionality testing can begin.

At a basic physical level, the underlying semiconductor chip will have a variety of reasonable ranges of voltages that can be applied, which is often determined ahead of time in a probe state or, in the case of an industrial lab, can be engineered. This allowed range is designed to prevent undesired effects including electrostatic breakdown, leakage of current across the barriers, and other similar effects. Thus a basic level of device protection must be assured by providing limits that the control systems will respect. However, there is a much narrower range of desired operation than that restricted by pure physical damage. Determining this range is one of the goals of bootstrapping.

Depending on the device type, there are two additional goals: (i) assuring that a 1D transport channel is formed in the 2DEG (not applicable to, e.g., nanowire QDs) and (ii) properly calibrating the charge sensor (not applicable to devices that do not use charge sensors, though this will typically have to be replaced with other constraints for either electrodynamic or current-based readout).

As an example, let us consider silicon QDs in devices with an overlapping gates architecture, which require both (i) and (ii). In these devices, the active region for forming dots is provided by a 2DEG formed at the interface between layered semiconductor structures (heterostructures), where the free electrons are confined to a planar region so thin that they behave as if they were truly two-dimensional. An example false-color SEM of a sample device with the overlapping gates architecture is shown in Fig. 3. The functionality testing of such devices begins with establishing the so-called “global turn-on”, that is, determining the voltage level at which a 2DEG is uniformly accumulated underneath the gates (McJunkin, 2021). This is achieved by synchronously increasing the voltage applied to all gates (initially set to 0 V) while

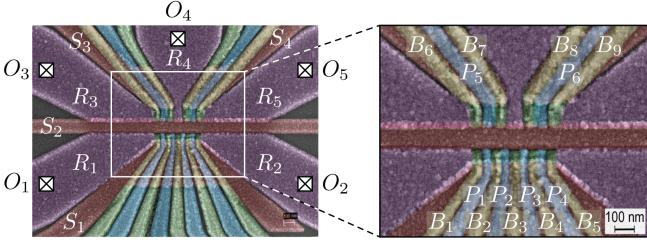


FIG. 3 A false-color SEM of a Si/SiGe quadruple QD device. This gate architecture is used as an example when discussing the autotuning process. All gates and voltage sources are labeled with standard names: screening (S), reservoir (R), plunger (P), barrier (B), and ohmic (O). The upper channel of this device with two QDs is used as a charge sensor for the lower channel dots. Adapted from McJunkin (2021).

simultaneously measuring current through appropriate pairs of ohmics. The level at which sufficient conductance is observed indicates the turn-on voltage.

The next step for this device is to assure that two 1D channels are formed within the 2DEG: one where the qubit QDs will be formed and the other to host the charge sensing dots. This is achieved by properly adjusting the screening (S_i , $i = 1, \dots, 4$, in Fig. 3) and reservoir (R_i , $i = 1, \dots, 5$) gates. First, the 2DEG has to be divided into two separate planes (current paths) by depleting electrons under the central screening gate (S_2 in Fig. 3; see also pinch-off curves in Fig. 2(a)(i)). To ensure sufficient accumulation and uniformity of the 2DEG, it might be desirable to re-adjust the turn-on for each side separately. Then, since the current through QDs has to be controlled at the single-electron level, it is important to verify that reservoir gates are not over-(or under-) accumulated. This is done by testing the “pinch-off” of each reservoir, that is finding the voltage level that cuts off the current through the device.

The next step involves calibrating the remaining screening gates to form two narrow conduction channels on each side of the device. By pinching-off an appropriate set of screening gates (e.g., S_1 and S_2 for the qubit channel in Fig. 3; see also Fig. 2(a)(ii)) and then setting the voltages on them significantly below the pinch-off, it is guaranteed that the 2DEG under those gates is depleted. Thus, if a current flow is observed when voltage is simultaneously increased at all relevant finger gates (i.e., gates B_i for $i = 1, \dots, 5$ and P_j for $j = 1, \dots, 4$ for the qubit channel), it can be safely assumed (for the overlapping gates design) that the 2DEG is accumulated only in the narrow passage between the screening gates.

Once the 1D channel is formed, the quality assessment and characterization of finger gates can begin. This process serves two purposes: (i) if a given gate does not pinch-off the current, it might be an indication that the gate is defective or broken and thus the devices should not be further calibrated and (ii) the pinch-off values for

each individual gate can be used as a guide when setting up the voltages needed to form dots. Two pinch-off curves showing Coulomb blockade oscillations in properly working finger gates are depicted in Fig. 2(a)(iii). As we already mentioned, voltages applied to the finger gates generally have to compensate for the disordered potential landscape resulting from various fabrication defects. Since the disorder is largely random and varies between devices, the optimal voltage for each gate has to be determined not only for each new device but might also be necessary between cooldowns of the same device. During the functionality testing step, all gates are checked and the optimal voltages are determined.

Typically, all of the bootstrapping steps are performed through a sequential analysis of 1D measurements of transport through the device as a function of gate voltages. As such, it is well suited for automation. One way to achieve this goal in the context of gate-defined QD devices is to combine physics-informed fitting and thresholds to inform the selection or relative voltage ranges as well as consecutive adjustments (Baart *et al.*, 2016; McJunkin, 2021). An approach to characterizing gates involving fitting and binary classification has also been proposed (Darulová *et al.*, 2020). Here, a set of parameters defining a hyperbolic-tangent-based fit to the 1D measurements is extracted and used to define, among other things, the pinch-off, transition, and saturation regions for each gate. A subset of these parameters is then used as a proxy for measurement quality (classified as good or bad) as well as to define the voltage range for subsequent coarse tuning. However, this approach is applicable mainly where not much variability in the pinch-off curves between the gates is expected. This is commonly seen in GaAs devices, while it is much less often observed in silicon devices. An automated analysis of the pinch-off curves for a device with an overlapping gates architecture is significantly more difficult as Coulomb blockade oscillations become present in the transport measurement. Thus, while these measurements can still be used to determine the pinch-off, a more nuanced analysis of the oscillations might be desirable to, e.g., determine the transition width of the pinch-off curve.

The final step of bootstrapping is calibration of the charge sensor, that is, finding a set of voltages applied to the sensing dot gates that maximizes sensitivity of the conductance through the dot to changes in the local electrostatic potential. This is typically done through an analysis of a 2D plot in the space of the two barriers defining the sensor starting with both barriers gates set slightly below their respective pinch off values and sweeping until saturation (as determined by the pinch off width) (Baart *et al.*, 2016; Botzem *et al.*, 2018; McJunkin, 2021). The resulting plot (so called “wall-wall” plot, see Fig. 2(a)(iv)) should reveal Coulomb blockade oscillations indicating the voltage range where the tunneling through the dot is finite, as indicated by the

characteristic diagonal lines. There are numerous edge detection techniques that can be deployed to identify the position and extract locations of those lines. Alternatively, a series of 1D sweeps of one of the barrier gates (from below the pinch off to saturation) while keeping the other barrier fixed slightly above its pinch off level should also reveal the oscillation pattern. Either method should produce voltages for setting the barriers for the charge sensor plunger sweep. This final 1D measurement from the plunger pinch off until saturation should reveal strong Coulomb blockade oscillations indicating this tuning is sufficient for operation as a charge sensor. The best charge sensitivity is achieved by choosing a voltage combination where the slope of the Coulomb peak is steepest.

B. Coarse tuning: Setting device topology

Once the two 1D channels are formed and the charge sensor is ready, the next step in the tuning process is setting the QD device up in a stable global configuration of known topology in the state space with a known number of charge islands. The coarse tuning phase is a process of finding a range of gate voltages for all the finger gates on the qubit side of the QD device that set the device in a particular global configuration. For simple devices, this corresponds to bringing the device into a single or double dot state, preferably in the few electron regime.

1. Topology of single QD devices

The process of tuning to a single QD state is quite similar to that of tuning a charge sensor: finding pinch off levels for all gates defining the QD, followed by calibration of barriers, and then sweeping the plunger gate. The Coulomb peak oscillations present in the resulting plot correspond to discrete charge transitions through the QD, indicating that a single QD has been formed. Depending on QD device type and architecture, tuning to a double QD state may involve adjusting the plunger gate until the single dot separates into two charge islands or tuning the adjacent set of gates to a single QD followed by fine-tuning of the cross-talk between the two neighboring QDs. At each step, the state of the device is determined based on visual inspection of the data. The various possible states manifest themselves as different shapes formed by electron transition lines, e.g., sets of parallel lines and honeycombs for the single and double QD states, respectively. Moreover, the orientations of those lines with respect to the measurement direction in the gate voltage space allows determination of the actual location of the charge island as, e.g., left, central, or right single QD.

Both script-based (Lapointe-Major *et al.*, 2020) and ML-enhanced (Czischek *et al.*, 2021) automated tuning

protocols that combine signal processing and adaptive measurement sequence derived from heuristics have been investigated for single silicon metal-oxide-semiconductor (SiMOS) QD devices. The sequence of measurements implemented in these algorithms is designed to mimic a typical manual tuning process, that is, adjusting voltages on gates defining the QD until transition lines become visible. The proposed algorithms involve an analysis of a series of images, each capturing a small sub-region in the voltage space, for a presence of lines. If no transitions are detected, both gate voltages are being simultaneously decreased by a fixed amount, creating a diagonal series of measurements until either a transition line is detected or a consecutive adjustment of voltages would surpass a safety restriction. Once a transition line is detected, the charge tuning stage is initiated, as we discuss in Sec. III.D.

2. Topology of double QD devices

A first computer-automated approach to tuning double-QD devices was proposed by Baart *et al.* (2016), where a GaAs quadruple-QD device was used to demonstrate an algorithm combining various image processing techniques to bring the device to a double QD in a single-electron regime. Here, the expected voltage ranges necessary to observe the Coulomb oscillations are determined by first fitting a tetragon to the area corresponding to large current in 2D barrier-barrier scans, followed by applying a Gabor filter to identify the center of the specific location where Coulomb peaks were formed. The resulting gate voltages serve as a starting point to form two independent single QDs. To form a double QD, a heuristic-based formula accounting for the capacitive coupling of the gates to the dots is used to determine the correct scan range. Finally, a pattern matching with a reference template containing expected geometry of the transition lines crossing is used to confirm reaching a double-QD regime. However, while in principle only prior knowledge of the gate design and the pinch-off value of the single gate shared by all QD is necessary to initiate this algorithm, in practice the consecutive steps rely on substantial knowledge about the device (e.g., a voltage required for the plunger gate to create a single QD, a suitable scan range for 2D scans, or the expected relative orientation of the transition lines in the crossing template). This makes the proposed tuning method not easily adaptable to new and unknown QD devices.

ML as a path toward scalable automation of tuning QD devices was suggested for the first time in the context of coarse tuning by Kalantre *et al.* (2017). In the proposed auto-tuning framework, the laborious tasks of a visual inspection and analysis of 2D measurements by a trained expert is replaced with an ML system—specifically a CNN—trained to quantify the captured

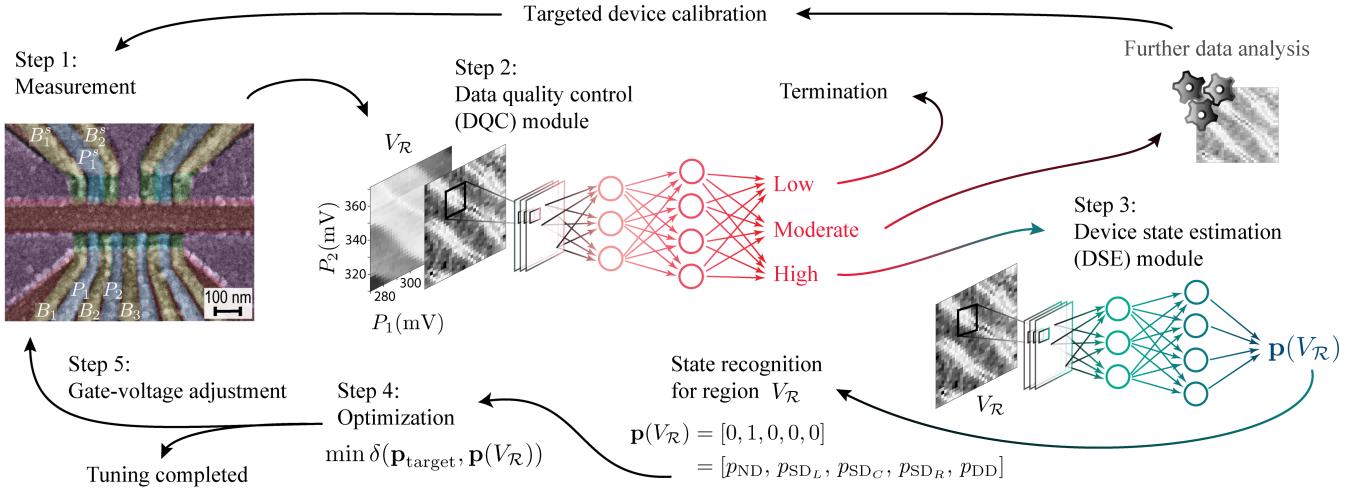


FIG. 4 Visualization of the coarse-tuning loop. The data processing step introduced in Zwolak *et al.* (2020b) is replaced with Step 2: Data quality control (DQC) module followed by state assessment and optimization for high quality scan, additional data analysis and targeted device recalibration for moderate quality scan, or the autotuning loop termination for low quality class. Adapted from Zwolak *et al.* (2020b) and Ziegler *et al.* (2021).

state of the device. The prediction vector returned by the CNN classifier—the “state vector”—represents the probability of each possible state being present within a given measurement. For the case of a double QD system this would be

$$\mathbf{p}(V_R) = [p_{ND}, p_{SD_L}, p_{SD_C}, p_{SD_R}, p_{DD}], \quad (2)$$

where \$V_R\$ denotes the measured scan, ND indicates that no QDs formed, SD_L, SD_C, and SD_R denote the left, central, and right single QD, respectively, and DD denotes the double-QD state.

Once properly trained, the ML classifier is integrated with a classical optimization algorithm to control the QD device and navigate the voltage space by minimizing the distance function $\delta(\mathbf{p}_{\text{target}}, \mathbf{p}(V_R))$ between the predicted $\mathbf{p}(V_R)$ and target $\mathbf{p}_{\text{target}}$ state vectors, as shown in Fig. 4. This auto-tuning framework was originally validated off-line, using premeasured experimental scans capturing a large range of gate voltages (Kalantre *et al.*, 2017) and then deployed on-line (*i.e.*, *in situ*) to tune a double QD in real time (Zwolak *et al.*, 2020b). However, while the tests showed a lot of promise, with a success rate of 85.7 % over 14 different on-line tuning runs of the same device, the experimental implementation required device-specific data processing to ensure compatibility with the CNN model trained on simplistic noiseless synthetic data. Still, when data was unusually noisy due to, e.g., instability of the charge sensor, the data processing was insufficient, resulting in the CNN returning an incorrect state vector and, ultimately, tuning failure.

To prevent failures due to low quality data, Ziegler *et al.* (2021) has recently proposed to replace the data processing step from the original auto-tuning framework with a data quality control (DQC) module. In the revised

framework, the DQC acts as a “gatekeeper” system to ensure that only reliable data is processed by the state classifier (DSE module), see inset in Fig. 4. Data assessed to be of lower quality triggers one of two alternative actions: additional data analysis followed by targeted device recalibration (for data classified as “moderate” quality) or tuning termination (for “low” quality data). Preliminary work in this space suggests that experimental noise and imperfections do not prevent the two-module ML system from operating as intended. While the updated system is yet to be tested experimentally, replacing the device-dependent processing with quality assessments seems to be a step in the right direction. Still, there are questions in ensuring both repeatability and reliability for ML-driven automation that remain open.

An alternative approach to tuning device topology for double QDs in GaAs that also relies on ML has been proposed by Darulová *et al.* (2020). Here, a sequential script-based protocol is set in place to adjust individual gates (or sets of gates), depending on the outcome of the ML module applied to a large 2D scan. The limits of the 2D scan are determined based on the voltage ranges (*i.e.*, the pinch-off levels and the “widths” of pinch-off curves) established during bootstrapping, as described in Sec. III.A. Once measured, the large 2D scan is segmented into small adjacent segments and each is analyzed independently by three binary classifiers trained to determine the dot regime (single or double QD) as well as its quality (good or bad). Then, depending on the outcome and the tuning goal, a scripted series of gate adjustments is executed. The algorithm stops when at least one segment of the charge diagram is classified as the desired dot regime. An overall 80 % success rate for tuning to a double QD state is reported for *in situ* test using a set

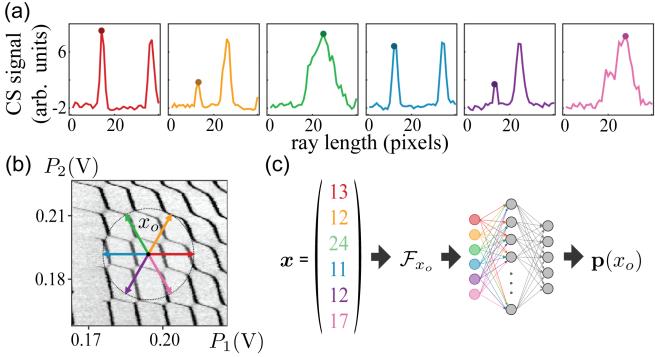


FIG. 5 (a) The processed charge sensor (CS) signal for six evenly distributed rays originating from a fixed point x_o in a double QD state. In each scan, the position of a transition line nearest to point x_o —that is, the “critical feature” along a given ray—is marked with a dot. (b) The distribution of rays overlaying a 2D measured scan. (c) Visualization of the ray-based fingerprinting framework. A vector of critical features is processed to produce a “point fingerprint” \mathcal{F}_{x_o} . The latter is then analyzed by a DNN classifier, resulting in a predicted state vector $\mathbf{p}(x_o)$ quantifying the current state of the device at the point x_o . Adapted from Zwolak *et al.* (2021).

of five double QD devices (from a single fabrication run) over two thermal runs.

3. Setting topology with rays

As we already mentioned, different configurations of the transition lines visible in a scan represent different states of the QD devices. Thus, while the qualitative information about the state of the device is fully encoded in the shape and orientation of those lines, the majority of the data points in any 2D scan contain background noise, which is irrelevant for setting device topology. In fact, it has been shown that the CNN model trained to estimate the QD device’s state (the DSE module in Fig. 4) learns to “ignore” all of the points measured between transition lines (Ziegler *et al.*, 2021). One way to reduce the number of unnecessary data points collected during measurement is to employ the ray-based classification (RBC) framework developed for classifying simple high-dimensional geometrical structures (Zwolak *et al.*, 2020a).

Rather than using a full 2D scan capturing a small region of the voltage space, the RBC framework relies on a collection of evenly distributed 1D sweeps (called “rays”) measured from a single point $x_o = (P_1, \dots, P_N)$ in multiple directions in the N -dimensional voltage space to assess the relative position of transition lines surrounding x_o (see Fig. 5(b) for an example of a sample point in double QD state with six evenly distributed rays). The resulting vector of distances to the nearest transition lines encodes qualitative information about the voltage space around x_o , effectively “fingerprinting” the neighborhood of x_o in the voltage space. The state of the device near

point x_o is determined using the point fingerprint and a simple deep neural network (DNN) trained using simulated fingerprints data.

The RBC framework has been tested using simulated data for the case of two and three QDs (Zwolak *et al.*, 2020a). It has also been implemented experimentally (both off-line and *in situ*) (Zwolak *et al.*, 2021) and shown performance on par with the more-data-demanding CNN-based classification (Zwolak *et al.*, 2020b) while requiring up to 70 % fewer measurement points. The off-line tuning success rate of 78.7 % is also comparable to that reported for tuning using on 2D scans (74.6 %; see Table I in Zwolak *et al.* (2020b)) even though tuning employing RBC was initiated significantly further from the target area than tuning based on a 2D scan, with initial points sampled uniformly over a region encompassing approximately 18 and 9 electron transitions, respectively. Importantly, the RBC framework naturally extends to classifying convex polytopes in higher dimensions (Weber *et al.*, 2021) which makes it an appealing measurement-cost-effective solution for differentiating between states of multi-QD devices.

The RBC not only reduces the amount of data that needs to be collected, but also can be implemented in an online or active learning setting, where data is acquired sequentially. In fact, an extension of the RBC framework to estimate the faces of the convex polytopes defined by state transitions has recently been proposed (Krause *et al.*, 2021). Here, a set of critical features measured in random directions from a fixed point x_o in the voltage space combined with an algorithm for learning convex polytopes from data with a margin (Gottlieb *et al.*, 2021) are used to approximate a candidate polytope whose faces intersect these points. Using an active learning strategy, the polytope estimate is iteratively refined based on a consecutive set of ray-based measurements targeting the vertices of the predicted polytope until either all faces are correctly located or the computation time runs out. The results for double QD system show that the algorithm can reliably find the facets of the polytope, including small facets with sizes on the order of the measurement precision, see Fig. 6(b).

While the extension of the RBC framework to approximate the enclosing polytope is interesting, there are a number of questions about its practical implication that remain open. For example, it is not clear what is the advantage of finding all of facets over simply estimating the general class a given polytope belongs to (as originally proposed) for the purpose of tuning to a specific charge state. Moreover, assigning the specific transitions to a given face, e.g., [2,0] or [2, 1] in Fig. 6(b), relies on the assumptions that the exact current state of the devices is already known, which in practice is usually not the case when tuning QD devices. Rather, the exact charge state of the QD device is typically calibrated once the QD topology is set, as we discuss in Sec. III.D.

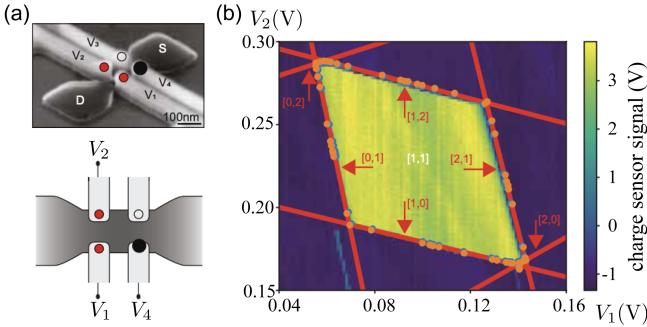


FIG. 6 (a) A micrograph (top) and a schematic (bottom) of a foundry-fabricated silicon QD device used to test the algorithm for polytope estimation (Ansaldi *et al.*, 2020). The two red dots indicate gates used to form the qubit QDs and the black dot indicate the sensor QD. (b) A 2D map of the sensor signal as a function of the control voltages V_1 and V_2 illustrating the convex polytope of the device shown in (a), with yellow pixels indicating the $[1, 1]$ state. The algorithm proposed in Krause *et al.* (2021) estimates state transitions to other states (red lines), based on a number of point pairs (x^+, x^-) (blue and orange dots) obtained via ray-based measurements. From Krause *et al.* (2021).

C. Establishing controllability

Once the device topology is defined, the intuitive next step would be to finely calibrate the device to a specific charge configuration. As we already mentioned, voltages applied to the finger gates shape the overall potential affecting electrons in the 2DEG. Ideally, changing voltages on a single gate would affect only a single parameter that the given gate is designed to control (e.g., the electrochemical potential of a specific QD or the tunnel barrier between two adjacent QDs). However, due to the capacitive cross-talk between the various gate electrodes changing the gate voltages defining one QD affects, at least to some degree, the potential of all nearby QDs. Thus, with the growing size of QD arrays, the task of setting the charge configuration becomes increasingly challenging.

The plunger and barrier gates collectively affect the overall potential profile μ , dot-specific single-particle energy detuning (i.e., the energy difference between the two QDs) of individual QDs $\delta\epsilon_i$, the tunnel couplings between QDs t_{ij} , and tunnel rates between the most outer QDs and reservoirs Γ_i . One way to compensate for the capacitive cross-talk between gates is to enable orthogonal control of the QDs potential by implementing so-called “virtual gates”. It is well known that linear combinations of gate voltage changes can be mapped onto onsite energy differences (Oosterkamp *et al.*, 1998). Virtual gates—the desired output of the establishing controllability phase—are linear combinations of multiple QD gate voltages chosen in such a way that only a single electrochemical potential or tunnel barrier is addressed (Hensgens, 2018; Hensgens *et al.*, 2017; Perron *et al.*, 2015).

The effect of shifting any given physical gate on the electrochemical potentials of all other gates is typically expressed via matrix of cross-capacitance couplings \mathbf{C} . The cross-capacitance matrix can be established by finding the slopes of transition lines in 2D images measured by fixing one of the gates as a reference, and then sweeping all of the remaining gates (one at a time) against the reference gate. Alternatively, one can use the relative magnitude of a shift of steps in 1D traces of the sensing dot conductance due to changing nearby dot occupation. A visualization of the cross-capacitance matrix for a three-QD device with one QD sensor is shown in Fig. 7(a). The entries of each row in this matrix show how the physical gate voltages affect each virtual gate, with a clearly visible fall-off in gating strength with distance. Virtual gates \mathbf{G}_{virt} obtained by inverting the matrix \mathbf{C} orthogonalize the voltage gate parameter space \mathbf{G} and enable control of each gate independently, without worrying about unwanted influence on the remaining dot energies (Hensgens, 2018):

$$\mathbf{G}^{\text{virt}} = \mathbf{C}^{-1} \mathbf{G}, \quad (3)$$

where $\mathbf{G} = [D_0, P_1, \dots, P_N, B_1, \dots, B_M]^T$ is a vector of physical gates defining qubit and sensor dots and \mathbf{G}^{virt} is a vector of corresponding virtual gates. Figure 7(b)

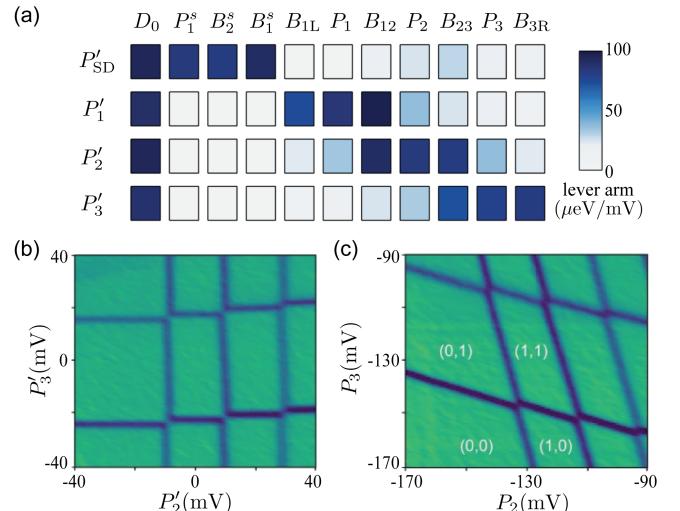


FIG. 7 (a) Visualization of the cross-capacitance matrix for a device shown in Fig. 1. The entries of each row show how the virtual plunger value (and hence the electrochemical potential) of a QD is influenced by other gate voltages. The rows for virtual barrier gates are omitted for simplicity. Gates defining the sensing dots (P_1^s , B_1^s , and B_2^s) are also included. Adapted from Hensgens (2018). (b) Charge stability diagram of a double QD in the single electron regime recorded as a function of the virtual plungers P'_2 and P'_3 . (c) Charge stability diagram of the same double QD in the physical gates space: The gradient of the charge sensor response (in arbitrary units) as a function of the plunger gate voltages P_2 and P_3 . From Volk *et al.* (2019).

shows a sample double QD charge stability diagram measured in the virtual gate space. For comparison, the same state measured in the physical gates space without correcting the cross-capacitance is shown in Fig. 7(c).

By enabling targeted control of specific QDs, virtual gates can be used to fill a QD array with electrons into a desired charge configuration. However, in the original proposal, the virtual gates did not account for the cross-talk on the tunnel barriers, which is necessary for fine-tuning QDs to work as qubits. In other words, applying voltage on gate B'_{ij} would not only affect t_{ij} , but also nearby tunnel couplings. To correct this limitation, two proposals for a redefinition of virtual gates that compensate for the cross-talk on tunnel couplings have recently been put forward (Hsiao *et al.*, 2020; Qiao *et al.*, 2020). Both proposed corrections rely on an assumption that t_{ij} can be approximated as an exponential function of a linear combination the physical gates:

$$t_{ij} = t_0 \exp(\Delta_{ij}) + \gamma_{ij}, \quad (4)$$

where t_0 and γ_{ij} are fit parameters, and Δ_{ij} is a linear combination of either the originally proposed virtual gates P'_k and B'_{kl} (Hsiao *et al.*, 2020), i.e.,

$$\Delta_{ij} = \sum_k \alpha_k^{ij} P'_k + \sum_{kl} \beta_{kl}^{ij} B'_{kl} \quad (5)$$

with α_k^{ij} and β_{kl}^{ij} derived from experimental data or the physical barrier gates (Qiao *et al.*, 2020), i.e.,

$$\Delta_{ij} = \sum_k \lambda_{ij} B_{ij}, \quad (6)$$

with λ_{ij} established based on a combination of simulations and experimental data analysis. We note that the parameters used in fitting likely depend substantially upon the topology and number of electrons in a given dot and dot array, and thus are only reliable as part of the fine-tuning process. Hsiao *et al.* (2020) redefines virtual gates using ratios of the α_k^{ij} and β_{kl}^{ij} coefficients from Eq. (5). Qiao *et al.* (2020), on the other hand, finds the required virtual barrier-gate voltages necessary to achieve target exchange coupling values by inverting Eq. (4). In either case, the resulting virtual barrier gates enable orthogonal control of the tunnel couplings over a wide range of tunnel coupling values, as shown for quadruple QDs in both Hsiao *et al.* (2020) and Qiao *et al.* (2020).

An alternative approach to correcting for the nonlinear and nonlocal dependence of exchange couplings on the barrier-gate voltages has also been proposed and demonstrated by Qiao *et al.* (2020). The model developed to define the virtual gates relies on the Heitler-London (HL) expression for exchange coupling between two spins (de Sousa *et al.*, 2001). However, solving nonlinear equations defining the HL-based model numerically can be susceptible to errors. Moreover, this model requires a

priori knowledge of the QD confinement potential which makes it less desirable for practical applications.

The utility of virtual gates has been shown in a number of multi-QD experiments, from showing controlled filling of an array of eight QDs using the “n+1 method” (Volk *et al.*, 2019) and tunable coupling between single electrons in a SiMOS (Eenink *et al.*, 2019) to demonstrating shuttling of a single charge through a 9-QDs charge stability space (Mills *et al.*, 2019b) and transferring single-spin eigenstates and entangled states via coherent SWAP gates between neighbouring pairs of spins in a four-qubit array (Kandel *et al.*, 2019). Adding the orthogonal control over tunnel couplings enabled generation of a Heisenberg spin chain and demonstration of two-, three-, and four-spin exchange oscillation (Qiao *et al.*, 2020).

D. Charge tuning

The coarse tuning algorithms, discussed in Sec. III.B, terminate once a target state—e.g., single- or double-QD state—is reached. However, the particular charge configuration of the system remains unknown at that point. At the same time, various quantum dot qubit realizations—hybrid qubits (Shi *et al.*, 2012), resonant exchange qubits (Medford *et al.*, 2013), or quadrupolar exchange-only qubits (Russ *et al.*, 2018)—require a specific number of electrons.

Depending on the QD qubit type, the required number of electrons is typically one to three per site. The goal of the charge tuning phase is to set the devices into a specific charge configuration. The charge sensor measurement does not provide the exact number of charges sensed but only the overall direction of change. The process of determining the charge configuration of a QD device—at least for the single- and double-QD cases—typically involves counting of the transition lines while emptying QD of all electrons, one at a time. To date, all proposals for automating the charge tuning have the same underlying strategy that is comprised of two phases: (i) emptying the QD of all electrons and (ii) re-loading the desired number of electrons on each QD.

The two algorithms proposed for single QD devices discussed in Sec. III.B implement this exact strategy. Starting at the transition detected either via image processing (Lapointe-Major *et al.*, 2020) or using ML-driven methods (Czischek *et al.*, 2021), gate voltages are adjusted to move towards neighbouring lines until no more transitions can be found. At that point (the so-called “reference point”), the QD is considered emptied and a re-loading phase begins. The latter involves adjusting gate voltages in the opposite direction until the first transition line is detected at which time the device is declared to be in a single electron regime, as depicted in Fig. 8(a). The ML-driven algorithm has a very high success rate for emptying the single QD device at about 98 %. However,

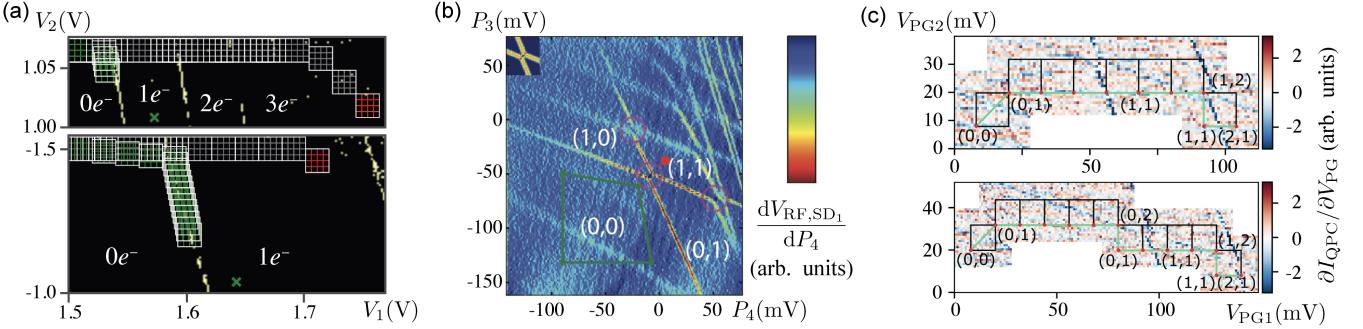


FIG. 8 (a) Visualization of the patch shifting algorithm proposed by Czischek *et al.* (2021) on two stability diagrams. Red grid indicates the starting points (see also Sec.III.B), the shifting path towards the empty reference point is shown in gray, and green denotes the shifting path towards the single-electron regime, with the green cross indicating the final position. After detecting the transition line from the empty reference point a jump to the lower right is performed to ensure ending up in the single-electron regime. From Czischek *et al.* (2021). (b) A sample double QD charge stability diagram showing three good matches to the reference crossings of charging lines template (inset), marked with purple circles. The occupancy of each dot is denoted by (n,m) and indicated the number of electrons in the left and right dot, respectively. The single-electron regime is found by verifying that no other charging lines are observed for more negative gate voltages with respect to the most bottom-left detected cross (green regions). From Baart *et al.* (2016). (c) Visualization of two successful runs of the ML-driven autotuner for tuning from $(0,0)$ to $(2,1)$ state. The boxes in black denote the patches used to determine the position of a next scan. From Durrer *et al.* (2020).

the reported 53 % success rate for re-loading a single electron back on the dot is rather low, which the authors attribute to interruptions in transition lines caused by the experimental measuring procedure. To mitigate the risk of the shifting algorithm hitting a gap in the transition lines, Czischek *et al.* (2021) propose to use arrays of K by K adjacent patches, as shown in Fig. 8(a), and show that the success rate, which seems to depend strongly on the array size, peaks for $K = 4$ at 75 %.

For double QD devices, the process of counting lines is more complicated as it is necessary to keep track of not only the total number of electrons but also which dot a given electron belongs to. A first automation proposal for double-QD devices to single-electron regime has been put forward by Baart *et al.* (2016). Starting at the most bottom-left crossing detected via the pattern matching algorithm described in Sec. III.B, the single-electron regime is found by verifying that no other prominent charging lines are observed when gate voltages are made more negative, as shown in Fig. 8(b). At that point, the algorithm sets both plunger voltages slightly above where the most bottom-left crossing was matched to enter the single-electron regime.

An alternative, ML-driven approach to the charge-state tuning, demonstrated using a GaAs triple QD device operated in the double-DQ mode, has been proposed by Durrer *et al.* (2020). The starting point for the charge-tuning algorithm is a well-defined double QD state with an unknown charge state (n_i, m_i) , where n_i and m_i denote the unknown initial number of charges on each QD, which is precisely the end-point of the coarse tuning phase discussed in Sec. III.B. Then, a two-stage algorithm for tuning the double QD device

to a pre-selected charge configuration (n, m) follows the unloading-re-loading strategy. Both stages involve a series of measurements in the space of the plunger gates, each followed by a CNN analysis of the measured scan and appropriate voltage adjustments rooted in heuristics. The measurement analysis is carried out by two specialized CNNs, each pre-trained using about 10^5 images sampled from large experimentally measured stability diagrams manually labeled with the position and orientation of the charge transition lines, with additional charge stability diagrams obtained by applying multiple augmentations to the experimental scans.

For the first (unloading) phase, a small, low-resolution scan (6 to 9 mV-per-pixel) is analyzed by a binary CNN classifier for the presence of transition lines. The size of the scans is chosen to assure that even within the voltage range with largest line spacing between consecutive transitions two transition lines can be captured. The algorithm follows a fixed path, decreasing both plunger gate voltages whenever at least one line is detected. Once a “no lines” class is identified, the depleting step terminates and a $(0,0)$ reference point charge state is assumed. At this point the second (re-loading) phase, aimed at loading electrons back to achieve the desired charge state, is automatically initiated.

The second algorithm also follows a pre-defined, though admittedly more nuanced, path. In particular, as long as both QDs need more electrons, both plunger gate voltages are increased by a fixed amount. Once at least one of the dots reaches the desired number of electrons, the direction of consecutive steps depends on which of the dots needs to be loaded (resulting in increasing of the voltage only on the relevant plunger gate) and whether

any undesirable transition lines are encountered for a dot that was previously tuned (resulting in decreasing voltage on the appropriate plunger gate). Two paths for the re-loading phase are shown in Fig. 8(c), where the device is tuned to a (2, 1) charge state. A separate CNN trained to recognize the presence and orientation of the detected transition lines from small high-resolution scans (1 mV-per-pixel) is used in this phase. This time the size of scans is chosen to assure that at most one transition line can be captured.

This charge-tuning algorithm has been validated experimentally using two double QD systems within the same triple QD device in GaAs. With the target state chosen randomly from a set of four possible configurations, an overall tuning success rate of 56.9 % has been reported for on-line tuning, with individual success rates for the unloading and re-loading phases being 90 % and 63 %, respectively. The majority of errors for the second phase stemmed from the low signal-to-noise ratio resulting in the CNN missing transition lines present in the data and ending up adding too many electrons. This work presents an important step toward autonomous QD calibration by enabling automated transition to fine-tuning discussed in Sec. III.E.

E. Fine-tuning

Once the quantum dot system is in the desired configuration—topology, charge, and controllability—there remains a significant additional step before the system can be used as a collection of quantum bits. These efforts entail fine-tuning of the parameters to enable treating the system in an abstract manner. There are two main aspects to fine-tuning. One is ensuring that the system is behaving close to the qubit regime. The second is ensuring that qubit performance and controllability can be achieved. Finally, fine-tuning also begins the process of mapping experimental analog parameters to those of bits, and thus represents a transition in what information is revealed or gained by experiments.

One critical challenge for ensuring qubit behavior is making certain that charge transitions occur only when desired. For example, during manipulation of electron spins as quantum bits, tunneling of the electron into a nearby Fermi sea would destroy coherence and would be considered a “leakage” error, in which case the qubit itself has been lost (Elzerman *et al.*, 2004b). Thus, a crucial aspect of fine-tuning is understanding and setting the tunneling (and co-tunneling) rates of QDs to nearby reservoirs. This becomes non-trivial when the additional requirement of being able to also reset or refill the QD from such reservoirs is imposed, as occurs in, e.g., a variety of qubit preparation and readout schemes.

Several groups have investigated means of automated estimation of tunneling to leads, including via estima-

tion of gate-dependent co-tunneling rates and by observation of charge loss and reset dynamics (Botzem *et al.*, 2018). These approaches take advantage of charge-based measurement, such as that provided by a nearby QD or quantum point contact in use as a charge sensor. However, rather than working (effectively) in a low frequency or DC domain, they instead use time dynamics. Analogous to estimating the time constant of an RC filter or the ring-down of a mechanical resonator, observation and fitting of such curves adds an additional depth to the challenge. This depth could be addressed in an automated manner via, e.g., ML techniques for processing time-domain signals, but so far remains untreated.

Another challenge arises when the topology and charge number is correct, but the tunneling rates to leads cannot get to the regime of interest, which may arise, for example, from pinch-off of a barrier. In that setting, returning to the coarse tuning mode with a new starting point may enable finding a different regime of parameter space which does not have such problems. However, no generic restart method has been proposed or implemented yet in experiment.

Finally, additional errors can occur in certain materials, such as silicon and SiGe QDs. In those devices, in addition to the spin and orbital physics of the QDs, there is also a valley degeneracy which plays the role of a pseudospin. This degeneracy is typically lifted due to various interface effects or disorder in a QD device. In practice, many groups work to ensure that QDs have valley splitting well in excess of the temperature and of the Larmor precession period of the spin degrees of freedom, such that it effectively can be neglected. However, for automated tuning, valley splitting must be estimated using, e.g., tunneling spectroscopy (Dodson *et al.*, 2021; Elzerman *et al.*, 2004a; Shi *et al.*, 2012; Zajac *et al.*, 2016).

The techniques above are designed to ensure that the QD system has appropriate means of resetting spins and does not “leak out” of the desired physical subspace—typically that of spin-1/2 or combinations of spin-1/2 electrons. However, operation on the spins or qubits (for composite spin systems) still requires substantial calibration.

One key parameter is the tunneling energy between two adjacent QDs, which determines the exchange interaction and forms the core of two-qubit gates, and for multi-electron qubits, single qubit gates as well. This parameter can be estimated both via more traditional gate voltage sweeps, and by more complex time-domain investigations. It does lead to a challenge for automated tuning, as often the rate is exponentially sensitive to applied voltages. Moreover, due to finite screening of nearby gate voltages, the tunneling energy has substantial interdependencies with other gates.

In one of the first works addressing automated control and adjustment of tunneling rates, a script-based method was developed that leveraged the virtual gates

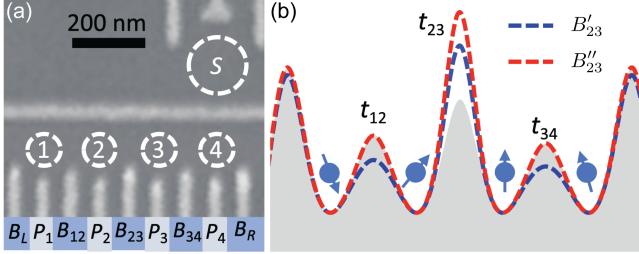


FIG. 9 (a) Electron micrograph (left) of a quadruple QD array in GaAs. (b) Schematics illustrating the influence of changes in virtual gates on the potential landscape of a quadruple QD. The grey area denotes the original landscape, the blue dashed line indicates the landscape when virtual gates are defined as proposed by Hensgens (2018), and the red dashed line indicates the landscape when virtual gates also compensate for the cross-talk on tunnel couplings. As can be seen, although B'_{23} keeps the dot potentials fixed while controlling the inter-dot tunnel coupling t_{23} , it also influences t_{12} and t_{34} . In contrast, B''_{23} does not affect the other two inter-dot tunnel couplings. From Hsiao *et al.* (2020).

concept (van Diepen *et al.*, 2018). In that effort, two different means of extracting the tunnel coupling are considered, both with low frequency measurements (width of the charge transition) and with high frequency measurements (photon-assisted tunneling). The benefit of the latter technique is the ability to measure beyond the thermal limit of linewidth, a crucial necessity for estimating small parameters even in a dilution refrigerator setting.

Fortunately, the use of virtual gates, as described in Sec. III.B, can help with isolating control of the tunneling rate (Hsiao *et al.*, 2020; Qiao *et al.*, 2020). The schematic in Fig. 9(b) depicts the effect of changes in the virtual gates (linear combinations of voltages applied to physical gates) on the potential landscape of the quadruple QD shown in Fig. 9(a). Changing voltage on virtual gate B''_{23} affects the target inter-dot tunnel coupling, as indicated with the red dashed line.

A different approach for handling estimation of parameters is to use template matching. In this approach, particular shapes and characteristics of data traces are assumed, and optimization occurs via fitting real data to a set of templates and extracting effective model parameters through this mechanism (Mills *et al.*, 2019a). A related set of techniques has also been leveraged to estimate, and tune, parameters in tunneling that lead to so-called bias triangles, using auto encoders to reduce the effective information coming from the experimental system to a significantly smaller feature space (van Esbroeck *et al.*, 2020). A key open question in fine tuning remains in determining how much actual experimental information should be extracted at each step. Experimental images are expensive (in time) to take, and thus reduced data acquisition is desired where possible. The

success of auto-encoders suggest that there exists a latent data space which would require substantially fewer experimental data points to populate.

As the tunneling rate becomes set, additional spin parameters must then be extracted, and in some cases, tuned. These include both the Zeeman splitting (Larmor precession frequency) and, where appropriate, estimates of the magnetic field gradient seen in each QD. In some sense, the goal of the physics-domain fine tuning is often to populate parameters in an effective model of the QD system. We note that the capacitive model used for virtual gates already provides a good starting point for this model.

Other, more phenomenological models such as the charge transition width (a proxy for tunnel coupling) and lead tunnel rates can be fit using data. If these estimates and their derivatives can be tracked, it becomes relatively straightforward to search parameter space efficiently. Unfortunately, tracking derivatives using finite differences becomes expensive in terms of data acquisition. In Teske *et al.* (2019) this complexity was removed by use of a Kalman filter to enable effective characterization of the gradients, enabling tuning in an efficient (in time and memory) control system.

So far, measurement methods have generally yielded relatively direct information regarding, e.g., changes in charge as a gate voltage is moved. However, future work must address the transition from a physics model description, such as the Hubbard model, and quantum gate performance. This effort, fortunately, need not directly rely upon experimental systems, as modeling of the system from a physics perspective is relatively straightforward given the observed connection between actual gate voltages and model parameters. However, a general solution of finding good quantum gates given this connection remains to be investigated.

IV. OUTLOOK: SOLVING THE METAPROBLEMS AND PATHS FORWARD

So far, we have considered the scenario in which the number of QDs and the number of gates to be manipulated—as well as the number of readout systems—is kept relatively small. The path to scaling up spin qubit systems through these automated approaches remains quite open, but is also quite opaque. Thus we now consider several metaproblems that will require substantial effort before scale-up can be achieved. For simplicity, we focus on the two most pressing today: efficiently adding additional QDs to a tuned system (scale-up) and moving key aspects of the ML systems closer to the dots themselves (reducing fan-out).

A. Scaling: inductive and in situ

On the scale-up problem, we have already seen that moving from physical gates to virtual gates is a significant benefit for controllability and fine tuning. Consider now a 1D array of gates on a nominal nanowire that could be used to form N QDs in series, with a nearby set of charge sensors. What approach can we use to “add” an additional QD to the array if we have already tuned up the first k dots and developed their virtual gate representation? Put simply, we can attempt to add the next QD holding the k dot system solved and “resolving” the k th dot in conjunction with the next dot in the line, thus mapping the system to a double QD tuning problem, but now starting with virtual gates for the k th dot such that cross-talk to the $k-1$ dots is close to zero. This inductive approach has not yet been tried in experiment, but could be a promising path forward.

A different approach would instead be to tune each pair of dots (e.g., 1 and 2; 2 and 3; etc.), while leveraging virtual gates from all the prior solutions. Then one can hope that the full solution is close to the tuned system. Many QD experiments with large arrays have used variations of this “in situ” approach to refine the range of acceptable parameters for searching for dots. One advantage of this approach is the ability to keep both the left and right dots in contact with the Fermi sea, making charge trapping and other hysteretic effects negligible.

In both cases, the assumed 1D nature of the physical layout provides substantial simplifications. More complicated is the loading of a two dimensional array of QDs, though both approaches may also find success in that setting. We do not anticipate that a fully computerized system is yet available that can explore this space efficiently; that is, the path forward today remains adapting practice in the lab to ML systems for solving key sub-problems first, then looking at generalizations.

B. Toward “on-chip” implementations

Finally, with the noisy intermediate-scale quantum (NISQ) technology era on the horizon (Preskill, 2018), it is important to consider the practical aspect of implementing autonomous control. Present day devices in which quantum bits are stored and processed require classical electronics to measure and control the qubits as well as conventional computer software to control and program these electronics. Since each qubit must be controlled and measured separately, it is necessary for the classical control system to scale along with the number of qubits, which at present represents a great engineering challenge (Geck *et al.*, 2019; Vandersypen *et al.*, 2017).

Placing the qubit control and analysis electronics in the immediate vicinity of the qubits in the cryostat either on the same chip or through chip-to-chip interconnection

technology poses serious constraints in terms of sizing and energy requirements. Thus, computational requirements and power consumption should also be considered when designing the autotuning system, enabling miniaturization of the control elements on low-power hardware a significant step towards “on-chip” autotuning. This issue has recently been discussed in the context of identification of charge state transition lines in two-dimensional stability diagrams, an important component in many of the autotuning proposals (Czischek *et al.*, 2021; Zwolak *et al.*, 2021).

Czischek *et al.* (2021) have recently shown that an extremely small feed-forward neural network (FFNN) with just a single hidden layer can be trained to detect charge-state transitions in single QD stability diagrams. Using a dataset of 800 synthetic stability diagrams (Genest, 2020), they train a binary classifier with only 10 hidden neurons to differentiate between the small patches with and without transition lines and report testing accuracy of 96 % on patches sampled from experimental data. The FFNN classifier lies at the core of a “shifting algorithm” they propose to tune single QD devices to the single-electron regime (see Sec. III.B and Sec. III.D).

An alternative approach to miniaturizing ML models has been proposed by Zwolak *et al.* (2021). Here, by replacing the traditional 2D scans and a CNN-based classifier with a series of 1D rays and encoding the state of the device via fingerprints (see Sec. III.B), the total number of parameters defining the ML model used for state assessment was reduced by two orders of magnitude compared to a CNN model (1.2×10^4 vs. 2.2×10^6 parameters, see Zwolak *et al.* (2020b)). While this number is still fairly high, it has been noted that the size and complexity of the DNN can be further reduced by at least an order of magnitude (Zwolak *et al.*, 2020a). Importantly, the RBC does not require any significant data processing, which further improves the computational efficiency of this approach and makes it an appealing candidate for the “on-chip” implementation on miniaturized hardware with low power consumption (Sebastian *et al.*, 2020).

C. Conclusions

With these provisos in mind, we hope the reader has seen that there is a tremendous set of tools that are being explored and leveraged to make QD systems substantially easier to operate and more reliable in their execution. Whether material science and fabrication obviate the need for this automation remains a question of engineering; we suspect that automated systems of this nature will be of critical importance for enabling ever-more complex experiments for the foreseeable future.

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