# *Cyclone V GX Starter Kit*

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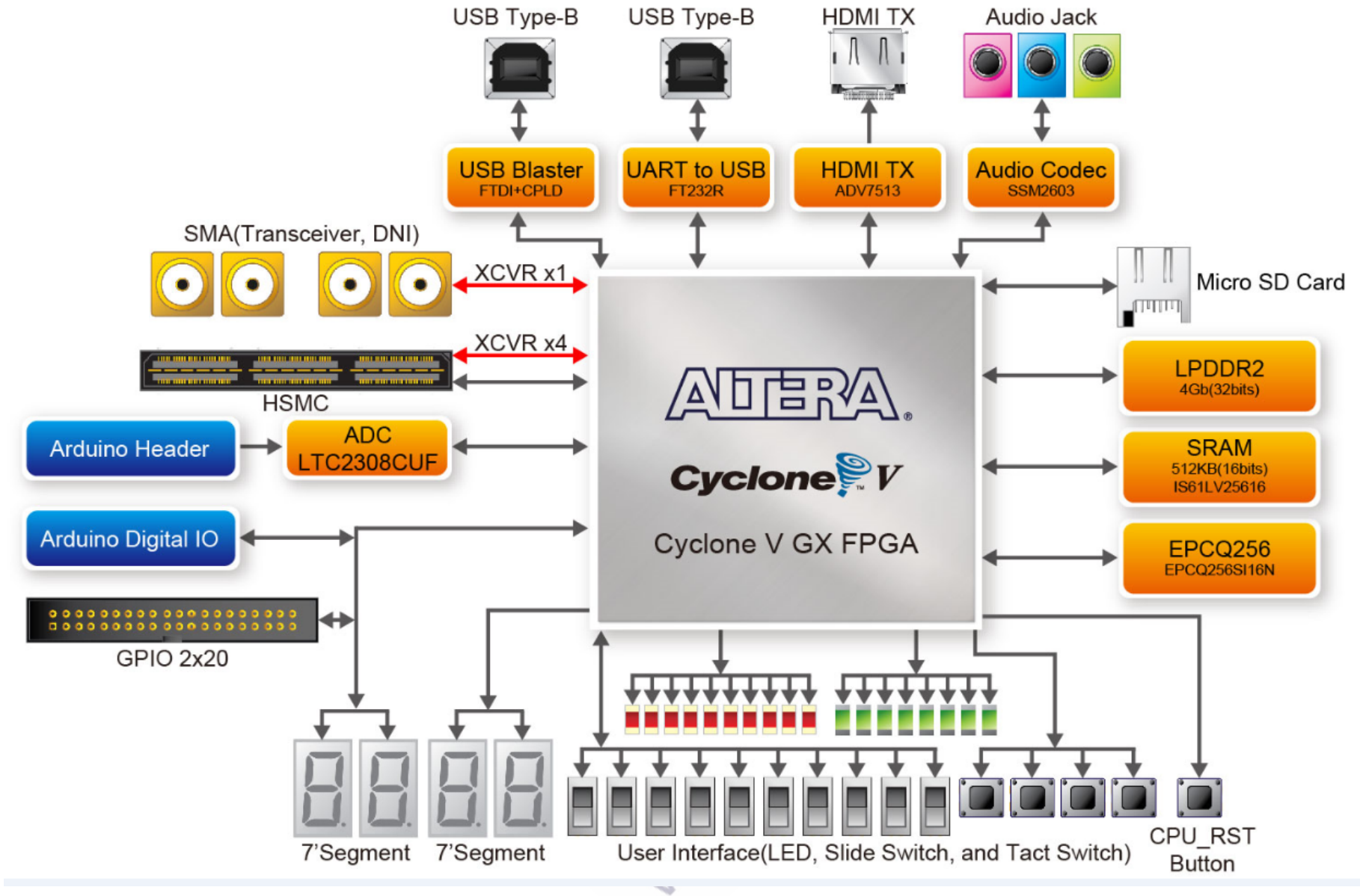


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## CYCLONE V GX BANK 3

**Bank 3B** VCCIO = 1.2V

| | | | | | |
|---|---|---|---|---|---|
| | T9 | IO_3B/DIFFIO_TX_B9P/DQ2B | IO_3B/DIFFIO_TX_B17P/DQ3B | V10 | SW6 |
| GND | U9 | IO_3B/DIFFIO_TX_B9N/GND | IO_3B/DIFFIO_TX_B17N/GND | V9 | GND |
| SW4 | W11 | IO_3B/DIFFIO_RX_B10P/DQ2B | IO_3B/DIFFIO_RX_B18P/DQ3B | AD8 | |
| SW8 | Y11 | IO_3B/DIFFIO_RX_B10N/DQ2B | IO_3B/DIFFIO_RX_B18N/DQ3B | AE8 | |
| DDR2LP_CS_n0 | R11 | IO_3B/DIFFIO_RX_B11P/DQS2B/B_CSN_0 | IO_3B/DIFFIO_RX_B19P/DQS3B/B_CK | N10 | DDR2LP_CK_p |
| DDR2LP_CS_n1 | T11 | IO_3B/DIFFIO_RX_B11N/DQSN2B/B_CSN_1 | IO_3B/DIFFIO_RX_B19N/DQSN3B/B_CKN | P10 | DDR2LP_CK_n |
| SW5 | AB10 | IO_3B/DIFFIO_TX_B12P | IO_3B/DIFFIO_TX_B20P/B_CA_6 | AE9 | DDR2LP_CA6 |
| SW7 | AC10 | IO_3B/DIFFIO_TX_B12N/DQ2B | IO_3B/DIFFIO_TX_B20N/DQ3B/B_CA_7 | AF9 | DDR2LP_CA7 |
| SW0 | AC9 | IO_3B/DIFFIO_TX_B13P/DQ2B | | | |
| SW3 | AC8 | IO_3B/DIFFIO_TX_B13N/DQ2B | | | |
| DDR2LP_CA8 | AB12 | IO_3B/DIFFIO_RX_B14P/DQ2B/B_CA_8 | IO_3B/DIFFIO_RX_B22P/DQ3B/B_CA_4 | U10 | DDR2LP_CA4 |
| DDR2LP_CA9 | AB11 | IO_3B/DIFFIO_RX_B14N/DQ2B/B_CA_9 | IO_3B/DIFFIO_RX_B22N/DQ3B/B_CA_5 | U11 | DDR2LP_CA5 |
| ADC_SDO | W10 | IO_3B/DIFFIO_TX_B16P/DQ2B | IO_3B/DIFFIO_TX_B24P/DQ3B/B_CA_0 | AE6 | DDR2LP_CA0 |
| ADC_SDI | Y10 | IO_3B/DIFFIO_TX_B16N/DQ2B | IO_3B/DIFFIO_TX_B24N/DQ3B/B_CA_1 | AF6 | DDR2LP_CA1 |

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### LPDDR2 Interface

7,11 DDR2LP_CA[9..0]
11 DDR2LP_CK_p
11 DDR2LP_CK_n
11 DDR2LP_CKE[1..0]
11 DDR2LP_CS_n[1..0]
11 DDR2LP_DM[3..0]
11 DDR2LP_DQ[31..0]
11 DDR2LP_DQS_p[3..0]
11 DDR2LP_DQS_n[3..0]

### SWITCH

18 SW[9..0]

### 7-SEGMENT

19 HEX0_D[6..0]
19 HEX1_D[6..0]

### ADC Interface

16 ADC_CONVST
16 ADC_SCK
16 ADC_SDO
16 ADC_SDI

R181
240
DDR2LP_OCT_RZQ AE11

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## CYCLONE V GX BANK 4

**Bank 4A** VCCIO = 1.2V

IO_4A/RZQ_0/DIFFIO_TX_B25N

| | | | | | |
|---|---|---|---|---|---|
| DDR2LP_DQ2 | AD11 | IO_4A/DIFFIO_TX_B25P/DQ4B/B_DQ_2 | IO_4A/DIFFIO_TX_B41P/DQ6B/B_DQ_18 | AC18 | DDR2LP_DQ18 |
| | | | IO_4A/DIFFIO_TX_B41N/GND | AD18 | GND |
| DDR2LP_DQ1 | Y14 | IO_4A/DIFFIO_RX_B26P/DQ4B/B_DQ_1 | IO_4A/DIFFIO_RX_B42P/DQ6B/B_DQ_17 | AD17 | DDR2LP_DQ17 |
| DDR2LP_DQ0 | AA14 | IO_4A/DIFFIO_RX_B26N/DQ4B/B_DQ_0 | IO_4A/DIFFIO_RX_B42N/DQ6B/B_DQ_16 | AD16 | DDR2LP_DQ16 |
| DDR2LP_DQS_p0 | V13 | IO_4A/DIFFIO_RX_B27P/DQS4B/B_DQS_0 | IO_4A/DIFFIO_RX_B43P/DQS6B/B_DQS_2 | V15 | DDR2LP_DQS_p2 |
| DDR2LP_DQS_n0 | W13 | IO_4A/DIFFIO_RX_B27N/DQSN4B/B_DQSN_0 | IO_4A/DIFFIO_RX_B43N/DQSN6B/B_DQSN_2 | W15 | DDR2LP_DQS_n2 |
| SW2 | AD13 | IO_4A/DIFFIO_TX_B28P/B_ODT_0 | IO_4A/DIFFIO_TX_B44P/B_RESETN | AE19 | SW9 |
| DDR2LP_DQ3 | AD12 | IO_4A/DIFFIO_TX_B28N/DQ4B/B_DQ_3 | IO_4A/DIFFIO_TX_B44N/DQ6B/B_DQ_19 | AF19 | DDR2LP_DQ19 |
| DDR2LP_DQ6 | AD10 | IO_4A/DIFFIO_TX_B29P/DQ4B/B_DQ_6 | IO_4A/DIFFIO_TX_B45P/DQ6B/B_DQ_22 | AF21 | DDR2LP_DQ22 |
| SW1 | AE10 | IO_4A/DIFFIO_TX_B29N/DQ4B/B_ODT_1 | IO_4A/DIFFIO_TX_B45N/DQ6B/GND | AF22 | GND |
| DDR2LP_DQ5 | W12 | IO_4A/DIFFIO_RX_B30P/DQ4B/B_DQ_5 | IO_4A/DIFFIO_RX_B46P/DQ6B/B_DQ_21 | AB17 | DDR2LP_DQ21 |
| DDR2LP_DQ4 | Y13 | IO_4A/DIFFIO_RX_B30N/DQ4B/B_DQ_4 | IO_4A/DIFFIO_RX_B46N/DQ6B/B_DQ_20 | AC17 | DDR2LP_DQ20 |
| | | | IO_4A/DIFFIO_RX_B47P/GND | T17 | GND |
| | | | IO_4A/DIFFIO_RX_B47N/GND | U17 | GND |
| DDR2LP_DM0 | AF11 | IO_4A/DIFFIO_TX_B32P/DQ4B/B_DM_0 | IO_4A/DIFFIO_TX_B48P/DQ6B/B_DM_2 | AE20 | DDR2LP_DM2 |
| DDR2LP_DQ7 | AF12 | IO_4A/DIFFIO_TX_B32N/DQ4B/B_DQ_7 | IO_4A/DIFFIO_TX_B48N/DQ6B/B_DQ_23 | AE21 | DDR2LP_DQ23 |
| DDR2LP_DQ10 | AC14 | IO_4A/DIFFIO_TX_B33P/DQ5B/B_DQ_10 | IO_4A/DIFFIO_TX_B49P/DQ7B/B_DQ_26 | AC20 | DDR2LP_DQ26 |
| GND | AC13 | IO_4A/DIFFIO_TX_B33N/GND | IO_4A/DIFFIO_TX_B49N/GND | AD20 | GND |
| DDR2LP_DQ9 | AB15 | IO_4A/DIFFIO_RX_B34P/DQ5B/B_DQ_9 | IO_4A/DIFFIO_RX_B50P/DQ7B/B_DQ_25 | AE16 | DDR2LP_DQ25 |
| DDR2LP_DQ8 | AC15 | IO_4A/DIFFIO_RX_B34N/DQ5B/B_DQ_8 | IO_4A/DIFFIO_RX_B50N/DQ7B/B_DQ_24 | AE15 | DDR2LP_DQ24 |
| DDR2LP_DQS_p1 | U14 | IO_4A/DIFFIO_RX_B35P/DQS5B/B_DQS_1 | IO_4A/DIFFIO_RX_B51P/DQS7B/B_DQS_3 | W16 | DDR2LP_DQS_p3 |
| DDR2LP_DQS_n1 | V14 | IO_4A/DIFFIO_RX_B35N/DQSN5B/B_DQSN_1 | IO_4A/DIFFIO_RX_B51N/DQSN7B/B_DQSN_3 | W17 | DDR2LP_DQS_n3 |
| DDR2LP_CKE1 | AE13 | IO_4A/DIFFIO_TX_B36P/B_CKE_1 | IO_4A/DIFFIO_TX_B52P/GND | AD22 | GND |
| DDR2LP_DQ11 | AF13 | IO_4A/DIFFIO_TX_B36N/DQ5B/B_DQ_11 | IO_4A/DIFFIO_TX_B52N/DQ7B/B_DQ_27 | AD21 | DDR2LP_DQ27 |
| DDR2LP_DQ14 | AE14 | IO_4A/DIFFIO_TX_B37P/DQ5B/B_DQ_14 | IO_4A/DIFFIO_TX_B53P/DQ7B/B_DQ_30 | AD23 | DDR2LP_DQ30 |
| DDR2LP_CKE0 | AF14 | IO_4A/DIFFIO_TX_B37N/DQ5B/B_CKE_0 | IO_4A/DIFFIO_TX_B53N/DQ7B/GND | AE23 | GND |
| DDR2LP_DQ13 | AA16 | IO_4A/DIFFIO_RX_B38P/DQ5B/B_DQ_13 | IO_4A/DIFFIO_RX_B54P/DQ7B/B_DQ_29 | AF17 | DDR2LP_DQ29 |
| DDR2LP_DQ12 | AB16 | IO_4A/DIFFIO_RX_B38N/DQ5B/B_DQ_12 | IO_4A/DIFFIO_RX_B54N/DQ7B/B_DQ_28 | AF16 | DDR2LP_DQ28 |
| | | | IO_4A/DIFFIO_RX_B55P/GND | U15 | GND |
| | | | IO_4A/DIFFIO_RX_B55N/GND | U16 | GND |
| DDR2LP_DM1 | AE18 | IO_4A/DIFFIO_TX_B40P/DQ5B/B_DM_1 | IO_4A/DIFFIO_TX_B56P/DQ7B/B_DM_3 | AE24 | DDR2LP_DM3 |
| DDR2LP_DQ15 | AF18 | IO_4A/DIFFIO_TX_B40N/DQ5B/B_DQ_15 | IO_4A/DIFFIO_TX_B56N/DQ7B/B_DQ_31 | AF23 | DDR2LP_DQ31 |
| | | | IO_4A/DIFFIO_TX_B57P/DQ8B/B_DQ_34 | AE25 | HEX1_D4 |
| | | | IO_4A/DIFFIO_TX_B57N/GND | AF24 | HEX1_D6 |
| | | | IO_4A/DIFFIO_RX_B58P/DQ8B/B_DQ_33 | Y18 | HEX0_D6 |
| | | | IO_4A/DIFFIO_RX_B58N/DQ8B/B_DQ_32 | AA18 | HEX1_D0 |
| | | | IO_4A/DIFFIO_RX_B59P/DQS8B/B_DQS_4 | V18 | HEX0_D1 |
| | | | IO_4A/DIFFIO_RX_B59N/DQSN8B/B_DQSN_4 | V17 | HEX0_D2 |
| | | | IO_4A/DIFFIO_TX_B60P/GND | AD26 | HEX1_D1 |
| | | | IO_4A/DIFFIO_TX_B60N/DQ8B/B_DQ_35 | AE26 | HEX1_D3 |
| | | | IO_4A/DIFFIO_TX_B61P/DQ8B/B_DQ_38 | AB19 | HEX1_D2 |
| | | | IO_4A/DIFFIO_TX_B61N/DQ8B/GND | AC19 | HEX1_D5 |
| | | | IO_4A/DIFFIO_RX_B62P/DQ8B/B_DQ_37 | Y20 | HEX0_D4 |
| | | | IO_4A/DIFFIO_RX_B62N/DQ8B/B_DQ_36 | Y19 | HEX0_D5 |
| | | | IO_4A/DIFFIO_RX_B63P/GND | V19 | HEX0_D0 |
| | | | IO_4A/DIFFIO_RX_B63N/GND | W18 | HEX0_D3 |
| | | | IO_4A/DIFFIO_TX_B64P/DQ8B/B_DM_4 | AB22 | ADC_CONVST |
| | | | IO_4A/DIFFIO_TX_B64N/DQ8B/B_DQ_39 | AA21 | ADC_SCK |

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| B | FPGA BANK 3 & 4 | B |

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## CYCLONE V GX BANK 5

VCCIO = 3.3V

### Bank 5A

| | | |
|---|---|---|
| GPIO35 | AC22 | IO_5A/RZQ_1/DIFFIO_TX_R1P/DQ1R |
| GPIO28 | W20 | IO_5A/DIFFIO_RX_R4P/DQ1R |
| GPIO27 | W21 | IO_5A/DIFFIO_RX_R4N/DQ1R |
| GPIO30 | Y23 | IO_5A/DIFFIO_TX_R7P/DQ1R |
| GPIO29 | Y24 | IO_5A/DIFFIO_TX_R7N |
| GPIO9 | T19 | IO_5A/DIFFIO_RX_R8P/DQ1R |
| GPIO24 | U20 | IO_5A/DIFFIO_RX_R8N/DQ1R |

### Bank 5B

VCCIO = 3.3V

| | | |
|---|---|---|
| IO_5B/DIFFIO_TX_R10P/DQ2R | V23 | HDMI_TX_D0 |
| IO_5B/DIFFIO_TX_R10N/DQ2R | V24 | HDMI_TX_D4 |
| IO_5B/DIFFIO_RX_R11P/DQ2R | T23 | HDMI_TX_D7 |
| IO_5B/DIFFIO_RX_R11N/DQ2R | T24 | HDMI_TX_D8 |
| IO_5B/DIFFIO_TX_R12P/DQ2R | AA24 | HDMI_TX_D20 |
| IO_5B/DIFFIO_TX_R12N/DQ2R | AB25 | HDMI_TX_D21 |
| IO_5B/DIFFIO_RX_R13P/DQS2R | R23 | HDMI_TX_D10 |
| IO_5B/DIFFIO_RX_R13N/DQSN2R | P23 | HDMI_TX_D13 |
| IO_5B/DIFFIO_TX_R14P | AD25 | HDMI_TX_D23 |
| IO_5B/DIFFIO_TX_R14N/DQ2R | AC25 | HDMI_TX_D22 |
| IO_5B/DIFFIO_RX_R15P/DQ2R | R24 | HDMI_TX_D17 |
| IO_5B/DIFFIO_RX_R15N/DQ2R | R25 | HDMI_TX_D11 |
| IO_5B/DIFFIO_TX_R16P/DQ2R | U24 | HDMI_TX_D6 |
| IO_5B/DIFFIO_TX_R16N | V25 | HDMI_TX_D5 |
| IO_5B/DIFFIO_TX_R18P/DQ3R | AB26 | HDMI_TX_D19 |
| IO_5B/DIFFIO_TX_R18N/DQ3R | AA26 | HDMI_TX_D1 |
| IO_5B/DIFFIO_RX_R19P/DQ3R | T26 | HDMI_TX_D9 |
| IO_5B/DIFFIO_RX_R19N/DQ3R | R26 | HDMI_TX_D18 |
| IO_5B/DIFFIO_RX_R21P/DQS3R | P21 | HDMI_TX_D16 |
| IO_5B/DIFFIO_RX_R21N/DQSN3R | P22 | HDMI_TX_D12 |
| IO_5B/DIFFIO_TX_R22P | W25 | HDMI_TX_D2 |
| IO_5B/DIFFIO_TX_R22N/DQ3R | W26 | HDMI_TX_D3 |
| IO_5B/DIFFIO_RX_R23P/DQ3R | N25 | HDMI_TX_D14 |
| IO_5B/DIFFIO_RX_R23N/DQ3R | P26 | HDMI_TX_D15 |
| IO_5B/DIFFIO_TX_R24P/DQ3R | U25 | HDMI_TX_VS |
| IO_5B/DIFFIO_TX_R24N | U26 | HDMI_TX_HS |

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## CYCLONE V GX BANK 6

### Bank 6A

VCCIO = 3.3V

| | | |
|---|---|---|
| SRAM_A14 | J25 | IO_6A/DIFFIO_TX_R26P/DQ4R |
| SRAM_A15 | J26 | IO_6A/DIFFIO_TX_R26N/DQ4R |
| SRAM_A16 | N24 | IO_6A/DIFFIO_RX_R27P/DQ4R |
| SRAM_A17 | M24 | IO_6A/DIFFIO_RX_R27N/DQ4R |
| SRAM_CE_n | N23 | IO_6A/DIFFIO_RX_R29P/DQS4R |
| SRAM_OE_n | M22 | IO_6A/DIFFIO_RX_R29N/DQSN4R |
| SRAM_WE_n | G25 | IO_6A/DIFFIO_TX_R30P |
| SRAM_LB_n | H25 | IO_6A/DIFFIO_TX_R30N/DQ4R |
| SRAM_UB_n | M25 | IO_6A/DIFFIO_RX_R31P/DQ4R |
| GPIO5 | M26 | IO_6A/DIFFIO_RX_R31N/DQ4R |
| GPIO1 | D26 | IO_6A/DIFFIO_TX_R32P/DQ4R |
| GPIO3 | E26 | IO_6A/DIFFIO_TX_R32N |
| SRAM_D0 | E24 | IO_6A/DIFFIO_TX_R34P/DQ5R |
| SRAM_D1 | E25 | IO_6A/DIFFIO_TX_R34N/DQ5R |
| SRAM_D2 | K24 | IO_6A/DIFFIO_RX_R35P/DQ5R |
| SRAM_D3 | K23 | IO_6A/DIFFIO_RX_R35N/DQ5R |
| SRAM_D4 | F24 | IO_6A/DIFFIO_TX_R36P/DQ5R |
| SRAM_D5 | G24 | IO_6A/DIFFIO_TX_R36N/DQ5R |
| SRAM_D6 | L23 | IO_6A/DIFFIO_RX_R37P/DQS5R |
| SRAM_D7 | L24 | IO_6A/DIFFIO_RX_R37N/DQSN5R |
| SRAM_D8 | H23 | IO_6A/DIFFIO_TX_R38P |
| SRAM_D9 | H24 | IO_6A/DIFFIO_TX_R38N/DQ5R |
| SRAM_D10 | H22 | IO_6A/DIFFIO_RX_R39P/DQ5R |
| SRAM_D11 | J23 | IO_6A/DIFFIO_RX_R39N/DQ5R |
| SRAM_D12 | F23 | IO_6A/DIFFIO_TX_R40P/DQ5R |
| SRAM_D13 | G22 | IO_6A/DIFFIO_TX_R40N |
| SRAM_D14 | L22 | IO_6A/DIFFIO_RX_R41P |
| SRAM_D15 | K21 | IO_6A/DIFFIO_RX_R41N |
| | | IO_6A/DIFFIO_TX_R42P/DQ6R |
| | | IO_6A/DIFFIO_TX_R42N/DQ6R |
| | | IO_6A/DIFFIO_RX_R43P/DQ6R |
| | | IO_6A/DIFFIO_RX_R43N/DQ6R |
| | | IO_6A/DIFFIO_TX_R44P/DQ6R |
| | | IO_6A/DIFFIO_TX_R44N/DQ6R |
| | | IO_6A/DIFFIO_RX_R45P/DQS6R |
| | | IO_6A/DIFFIO_RX_R45N/DQSN6R |
| | | IO_6A/DIFFIO_TX_R46P |
| | | IO_6A/DIFFIO_TX_R46N/DQ6R |
| | | IO_6A/DIFFIO_RX_R47P/DQ6R |
| | | IO_6A/DIFFIO_RX_R47N/DQ6R |
| | | IO_6A/DIFFIO_TX_R48P/DQ6R |
| | | IO_6A/DIFFIO_TX_R48N |

| | | |
|---|---|---|
| B25 | SRAM_A0 | |
| B26 | SRAM_A1 | |
| H19 | SRAM_A2 | |
| H20 | SRAM_A3 | |
| D25 | SRAM_A4 | |
| C25 | SRAM_A5 | |
| J20 | SRAM_A6 | |
| J21 | SRAM_A7 | |
| D22 | SRAM_A8 | |
| E23 | SRAM_A9 | |
| G20 | SRAM_A10 | |
| F21 | SRAM_A11 | |
| E21 | SRAM_A12 | |
| F22 | SRAM_A13 | |

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### HDMI TX

| | |
|---|---|
| 14 | HDMI_TX_D[23..0] |
| 14 | HDMI_TX_VS |
| 14 | HDMI_TX_HS |

### SRAM

| | |
|---|---|
| 12 | SRAM_A[17..0] |
| 12 | SRAM_D[15..0] |
| 12 | SRAM_CE_n |
| 12 | SRAM_OE_n |
| 12 | SRAM_WE_n |
| 12 | SRAM_LB_n |
| 12 | SRAM_UB_n |

### GPIO

| | |
|---|---|
| 7,8,17,19 | GPIO[35..0] |

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| Size | Document Number | Rev |
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| B | FPGA BANK 5 & 6 | B |

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## CYCLONE V GX BANK 7

**Bank 7A** VCCIO = 2.5V

| | | | |
|---|---|---|---|
| HSMC_D2 | D12 | IO_7A/RZQ_2/DIFFIO_TX_T40N | |
| HSMC_RX_p4 | H15 | IO_7A/DIFFIO_RX_T1P/GND | |
| HSMC_RX_n4 | J16 | IO_7A/DIFFIO_RX_T1N/GND | |
| HSMC_TX_p11 | C23 | IO_7A/DIFFIO_TX_T2P/DQ1T/T_DM_4 | IO_7A/DIFFIO_TX_T18P/DQ3T/T_DM_2 |
| HSMC_TX_n11 | C22 | IO_7A/DIFFIO_TX_T2N/DQ1T/T_DQ_39 | IO_7A/DIFFIO_TX_T18N/DQ3T/T_DQ_23 |
| HSMC_RX_p16 | B24 | IO_7A/DIFFIO_RX_T3P/DQ1T/T_DQ_37 | IO_7A/DIFFIO_RX_T19P/DQ3T/T_DQ_21 |
| HSMC_RX_n16 | A24 | IO_7A/DIFFIO_RX_T3N/DQ1T/T_DQ_36 | IO_7A/DIFFIO_RX_T19N/DQ3T/T_DQ_20 |
| HSMC_TX_p13 | A23 | IO_7A/DIFFIO_TX_T4P/DQ1T/T_DQ_38 | IO_7A/DIFFIO_TX_T20P/DQ3T/T_DQ_22 |
| HSMC_TX_n13 | A22 | IO_7A/DIFFIO_TX_T4N/DQ1T/GND | IO_7A/DIFFIO_TX_T20N/DQ3T/GND |
| HSMC_RX_p2 | H18 | IO_7A/DIFFIO_RX_T5P/DQS1T/T_DQS_4 | IO_7A/DIFFIO_RX_T21P/DQS3T/T_DQS_2 |
| HSMC_RX_n2 | H17 | IO_7A/DIFFIO_RX_T5N/DQSN1T/T_DQSN_4 | IO_7A/DIFFIO_RX_T21N/DQSN3T/T_DQSN_2 |
| HSMC_TX_p7 | B22 | IO_7A/DIFFIO_TX_T6P/GND | IO_7A/DIFFIO_TX_T22P/T_RESETN |
| HSMC_TX_n7 | A21 | IO_7A/DIFFIO_TX_T6N/DQ1T/T_DQ_35 | IO_7A/DIFFIO_TX_T22N/DQ3T/T_DQ_19 |
| HSMC_RX_p15 | D21 | IO_7A/DIFFIO_RX_T7P/DQ1T/T_DQ_33 | IO_7A/DIFFIO_RX_T23P/DQ3T/T_DQ_17 |
| HSMC_RX_n15 | D20 | IO_7A/DIFFIO_RX_T7N/DQ1T/T_DQ_32 | IO_7A/DIFFIO_RX_T23N/DQ3T/T_DQ_16 |
| HSMC_TX_p16 | B21 | IO_7A/DIFFIO_TX_T8P/DQ1T/T_DQ_34 | IO_7A/DIFFIO_TX_T24P/DQ3T/T_DQ_18 |
| HSMC_TX_n16 | B20 | IO_7A/DIFFIO_TX_T8N/GND | IO_7A/DIFFIO_TX_T24N/GND |
| HSMC_RX_p6 | G16 | IO_7A/DIFFIO_RX_T9P/GND | |
| HSMC_RX_n6 | G17 | IO_7A/DIFFIO_RX_T9N/GND | |
| HSMC_TX_p5 | C20 | IO_7A/DIFFIO_TX_T10P/DQ2T/T_DM_3 | IO_7A/DIFFIO_TX_T26P/DQ4T/T_DM_1 |
| HSMC_TX_n5 | B19 | IO_7A/DIFFIO_TX_T10N/DQ2T/T_DQ_31 | IO_7A/DIFFIO_TX_T26N/DQ4T/T_DQ_15 |
| HSMC_RX_p14 | E20 | IO_7A/DIFFIO_RX_T11P/DQ2T/T_DQ_29 | IO_7A/DIFFIO_RX_T27P/DQ4T/T_DQ_13 |
| HSMC_RX_n14 | E19 | IO_7A/DIFFIO_RX_T11N/DQ2T/T_DQ_28 | IO_7A/DIFFIO_RX_T27N/DQ4T/T_DQ_12 |
| HSMC_TX_p15 | C19 | IO_7A/DIFFIO_TX_T12P/DQ2T/T_DQ_30 | IO_7A/DIFFIO_TX_T28P/DQ4T/T_DQ_14 |
| HSMC_TX_n15 | C18 | IO_7A/DIFFIO_TX_T12N/DQ2T/GND | IO_7A/DIFFIO_TX_T28N/DQ4T/T_CKE_0 |
| HSMC_RX_p5 | J12 | IO_7A/DIFFIO_RX_T13P/DQS2T/T_DQS_3 | IO_7A/DIFFIO_RX_T29P/DQS4T/T_DQS_1 |
| HSMC_RX_n5 | J11 | IO_7A/DIFFIO_RX_T13N/DQSN2T/T_DQSN_3 | IO_7A/DIFFIO_RX_T29N/DQSN4T/T_DQSN_1 |
| HSMC_CLKOUT_p1 | A19 | IO_7A/DIFFIO_TX_T14P/GND | IO_7A/DIFFIO_TX_T30P/T_CKE_1 |
| HSMC_CLKOUT_n1 | A18 | IO_7A/DIFFIO_TX_T14N/DQ2T/T_DQ_27 | IO_7A/DIFFIO_TX_T30N/DQ4T/T_DQ_11 |
| HSMC_RX_p13 | D18 | IO_7A/DIFFIO_RX_T15P/DQ2T/T_DQ_25 | IO_7A/DIFFIO_RX_T31P/DQ4T/T_DQ_9 |
| HSMC_RX_n13 | D17 | IO_7A/DIFFIO_RX_T15N/DQ2T/T_DQ_24 | IO_7A/DIFFIO_RX_T31N/DQ4T/T_DQ_8 |
| HSMC_CLKOUT_p2 | A17 | IO_7A/DIFFIO_TX_T16P/DQ2T/T_DQ_26 | IO_7A/DIFFIO_TX_T32P/DQ4T/T_DQ_10 |
| HSMC_CLKOUT_n2 | A16 | IO_7A/DIFFIO_TX_T16N/GND | IO_7A/DIFFIO_TX_T32N/GND |
| HSMC_D1 | H14 | IO_7A/DIFFIO_RX_T17P/GND | |
| HSMC_D3 | H13 | IO_7A/DIFFIO_RX_T17N/GND | |
| | | IO_7A/DIFFIO_TX_T34P/DQ5T/T_DM_0 | |
| | | IO_7A/DIFFIO_TX_T34N/DQ5T/T_DQ_7 | |
| | | IO_7A/DIFFIO_RX_T35P/DQ5T/T_DQ_5 | |
| | | IO_7A/DIFFIO_RX_T35N/DQ5T/T_DQ_4 | |
| | | IO_7A/DIFFIO_TX_T36P/DQ5T/T_DQ_6 | |
| | | IO_7A/DIFFIO_TX_T36N/DQ5T/T_ODT_1 | |
| | | IO_7A/DIFFIO_RX_T37P/DQS5T/T_DQS_0 | |
| | | IO_7A/DIFFIO_RX_T37N/DQSN5T/T_DQSN_0 | |
| | | IO_7A/DIFFIO_TX_T38P/T_ODT_0 | |
| | | IO_7A/DIFFIO_TX_T38N/DQ5T/T_DQ_3 | |
| | | IO_7A/DIFFIO_RX_T39P/DQ5T/T_DQ_1 | |
| | | IO_7A/DIFFIO_RX_T39N/DQ5T/T_DQ_0 | |
| | | IO_7A/DIFFIO_TX_T40P/DQ5T/T_DQ_2 | |

| | | | |
|---|---|---|---|
| C17 | HSMC_TX_p14 | | |
| B17 | HSMC_TX_n14 | | |
| E18 | HSMC_RX_p8 | | |
| F18 | HSMC_RX_n8 | | |
| A14 | HSMC_TX_p12 | | |
| B14 | HSMC_TX_n12 | | |
| L12 | HSMC_RX_p3 | | |
| K11 | HSMC_RX_n3 | | |
| B15 | HSMC_TX_p6 | | |
| C15 | HSMC_TX_n6 | | |
| C14 | HSMC_RX_p11 | | |
| D15 | HSMC_RX_n11 | | |
| A8 | HSMC_TX_p9 | | |
| A9 | HSMC_TX_n9 | | |
| C9 | HSMC_TX_p1 | | |
| B9 | HSMC_TX_n1 | | |
| E16 | HSMC_RX_p12 | | |
| D16 | HSMC_RX_n12 | | |
| D10 | HSMC_TX_p2 | | |
| C10 | HSMC_TX_n2 | | |
| N12 | HSMC_RX_p0 | | |
| M12 | HSMC_RX_n0 | | |
| B10 | HSMC_TX_p4 | | |
| A11 | HSMC_TX_n4 | | |
| F16 | HSMC_RX_p9 | | |
| E15 | HSMC_RX_n9 | | |
| E10 | HSMC_TX_p0 | | |
| E11 | HSMC_TX_n0 | | |
| B12 | HSMC_TX_p10 | | |
| A13 | HSMC_TX_n10 | | |
| G12 | HSMC_RX_p7 | | |
| F12 | HSMC_RX_n7 | | |
| A12 | HSMC_TX_p3 | | |
| B11 | HSMC_TX_n3 | | |
| M11 | HSMC_RX_p1 | | |
| L11 | HSMC_RX_n1 | | |
| C13 | HSMC_TX_p8 | | |
| C12 | HSMC_TX_n8 | | |
| E13 | HSMC_RX_p10 | | |
| D13 | HSMC_RX_n10 | | |
| D11 | HSMC_D0 | | |

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## CYCLONE V GX BANK 8

**Bank 8A** VCCIO = 2.5V

| | | | |
|---|---|---|---|
| LEDG4 | A5 | IO_8A/DIFFIO_TX_T42P/DQ6T/T_CA_0 | IO_8A/DIFFIO_TX_T50P/DQ7T |
| LEDG5 | B6 | IO_8A/DIFFIO_TX_T42N/DQ6T/T_CA_1 | IO_8A/DIFFIO_TX_T50N/DQ7T |
| LEDG6 | H8 | IO_8A/DIFFIO_RX_T43P/DQ6T/T_CA_4 | IO_8A/DIFFIO_RX_T51P/DQ7T/T_CA_8 |
| LEDG7 | H9 | IO_8A/DIFFIO_RX_T43N/DQ6T/T_CA_5 | IO_8A/DIFFIO_RX_T51N/DQ7T/T_CA_9 |
| | | | IO_8A/DIFFIO_TX_T52P/DQ7T |
| | | | IO_8A/DIFFIO_TX_T52N/DQ7T |
| UART_RX | M9 | IO_8A/DIFFIO_RX_T45P/DQS6T/T_CK | IO_8A/DIFFIO_RX_T53P/DQS7T/T_CSN_0 |
| UART_TX | L9 | IO_8A/DIFFIO_RX_T45N/DQSN6T/T_CKN | IO_8A/DIFFIO_RX_T53N/DQSN7T/T_CSN_1 |
| AUD_XCK | D6 | IO_8A/DIFFIO_TX_T46P/T_CA_6 | IO_8A/DIFFIO_TX_T54P |
| AUD_BCLK | E6 | IO_8A/DIFFIO_TX_T46N/DQ6T/T_CA_7 | IO_8A/DIFFIO_TX_T54N/DQ7T |
| AUD_DACDAT | H10 | IO_8A/DIFFIO_RX_T47P/DQ6T | IO_8A/DIFFIO_RX_T55P/DQ7T |
| AUD_DACLRCK | G10 | IO_8A/DIFFIO_RX_T47N/DQ6T | IO_8A/DIFFIO_RX_T55N/DQ7T |
| AUD_ADCDAT | D7 | IO_8A/DIFFIO_TX_T48P/DQ6T | IO_8A/DIFFIO_TX_T56P/DQ7T |
| AUD_ADCLRCK | C7 | IO_8A/DIFFIO_TX_T48N/GND | IO_8A/DIFFIO_TX_T56N/GND |

| | | | |
|---|---|---|---|
| F6 | LEDR1 | | |
| G6 | LEDR2 | | |
| K8 | LEDR7 | | |
| J8 | LEDR4 | | |
| G7 | LEDR3 | | |
| F7 | LEDR0 | | |
| K10 | LEDR6 | | |
| J10 | LEDR9 | | |
| H7 | LEDR8 | | |
| J7 | LEDR5 | | |
| L7 | LEDG0 | | |
| K6 | LEDG1 | | |
| D8 | LEDG2 | | |
| E9 | LEDG3 | | |

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### Audio CODEC

| | |
|---|---|
| 13 | AUD_XCK |
| 13 | AUD_BCLK |
| 13 | AUD_DACDAT |
| 13 | AUD_DACLRCK |
| 13 | AUD_ADCDAT |
| 13 | AUD_ADCLRCK |

### LED

| | |
|---|---|
| 19 | LEDR[9..0] |
| 19 | LEDG[7..0] |

### UART to USB

| | |
|---|---|
| 20 | UART_RX |
| 20 | UART_TX |

### HSMC Interface

| | |
|---|---|
| 15 | HSMC_TX_p[16..0] |
| 15 | HSMC_TX_n[16..0] |
| 15 | HSMC_RX_p[16..0] |
| 15 | HSMC_RX_n[16..0] |
| 15 | HSMC_D[3..0] |

### HSMC Clock output

| | |
|---|---|
| 15 | HSMC_CLKOUT_p[2..1] |
| 15 | HSMC_CLKOUT_n[2..1] |

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Title: **Cyclone V GX Starter Kit**

| Size | Document Number | Rev |
|---|---|---|
| B | FPGA BANK 7 & 8 | B |

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## XCVR Reference Clock

7 REFCLK_p[1..0]

7 REFCLK_n[1..0]

## HSMC Transceiver

15 HSMC_GXB_TX_p[3..0]

15 HSMC_GXB_TX_n[3..0]

15 HSMC_GXB_RX_p[3..0]

15 HSMC_GXB_RX_n[3..0]

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### CYCLONE V GX Transceiver

#### GXB_L0

| | | | | | |
|---|---|---|---|---|---|
| HSMC_GXB_RX_p0 | AD2 | GXB_RX_L0P,GXB_REFCLK_L0P | GXB_TX_L0P | AE4 | HSMC_GXB_TX_p0 |
| HSMC_GXB_RX_n0 | AD1 | GXB_RX_L0N,GXB_REFCLK_L0N | GXB_TX_L0N | AE3 | HSMC_GXB_TX_n0 |
| HSMC_GXB_RX_p1 | AB2 | GXB_RX_L1P,GXB_REFCLK_L1P | GXB_TX_L1P | AC4 | HSMC_GXB_TX_p1 |
| HSMC_GXB_RX_n1 | AB1 | GXB_RX_L1N,GXB_REFCLK_L1N | GXB_TX_L1N | AC3 | HSMC_GXB_TX_n1 |
| HSMC_GXB_RX_p2 | Y2 | GXB_RX_L2P,GXB_REFCLK_L2P | GXB_TX_L2P | AA4 | HSMC_GXB_TX_p2 |
| HSMC_GXB_RX_n2 | Y1 | GXB_RX_L2N,GXB_REFCLK_L2N | GXB_TX_L2N | AA3 | HSMC_GXB_TX_n2 |
| REFCLK_p0 | V6 | REFCLK0LP | | | |
| REFCLK_n0 | W6 | REFCLK0LN | | | |

#### GXB_L1

| | | | | | |
|---|---|---|---|---|---|
| HSMC_GXB_RX_p3 | V2 | GXB_RX_L3P,GXB_REFCLK_L3P | GXB_TX_L3P | W4 | HSMC_GXB_TX_p3 |
| HSMC_GXB_RX_n3 | V1 | GXB_RX_L3N,GXB_REFCLK_L3N | GXB_TX_L3N | W3 | HSMC_GXB_TX_n3 |
| | T2 | GXB_RX_L4P,GXB_REFCLK_L4P | GXB_TX_L4P | P2 | |
| R196 0 | T1 | GXB_RX_L4N,GXB_REFCLK_L4N | GXB_TX_L4N | P1 | |
| SMA_GXB_RX_p | M2 | GXB_RX_L5P,GXB_REFCLK_L5P | GXB_TX_L5P | K2 | SMA_GXB_TX_p |
| SMA_GXB_RX_n | M1 | GXB_RX_L5N,GXB_REFCLK_L5N | GXB_TX_L5N | K1 | SMA_GXB_TX_n |
| REFCLK_p1 | N7 | REFCLK1LP | | | |
| REFCLK_n1 | P6 | REFCLK1LN | RREF_TL | B1 | R204 2K |

#### GXB_L2

| | | | | | |
|---|---|---|---|---|---|
| | H2 | GXB_RX_L6p,GXB_REFCLK_L6p | GXB_TX_L6p | G4 | |
| | H1 | GXB_RX_L6n,GXB_REFCLK_L6n | GXB_TX_L6n | G3 | |
| | F2 | GXB_RX_L7p,GXB_REFCLK_L7p | GXB_TX_L7p | E4 | |
| | F1 | GXB_RX_L7n,GXB_REFCLK_L7n | GXB_TX_L7n | E3 | |
| R199 0 | D2 | GXB_RX_L8p,GXB_REFCLK_L8p | GXB_TX_L8p | C4 | |
| | D1 | GXB_RX_L8n,GXB_REFCLK_L8n | GXB_TX_L8n | C3 | |
| | M6 | REFCLK2Lp | | | |
| R198 0 | L5 | REFCLK2Ln | | | |

**GXB L2 is C7 FPGA only**

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J12 SMA — C136 0.01u SMA_GXB_RX_p — DNI

J13 SMA — C137 0.01u SMA_GXB_RX_n — DNI

SMA_GXB_TX_p — J7 SMA — DNI

SMA_GXB_TX_n — J8 SMA — DNI

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Title: Cyclone V GX Starter Kit

Size B | Document Number: FPGA BANK Transceivers | Rev B

Date: Tuesday, August 20, 2013 | Sheet 6 of 23

## LPDDR2

11 DDR2LP_CA2
11 DDR2LP_CA3

## KEY

18 KEY[3..0]

## GPIO (CLOCK IN/OUT)

17 GPIO0
17 GPIO2
17 GPIO16
17 GPIO18

## HSMC Clock

15 HSMC_CLKOUT0
15 HSMC_CLKIN0
15 HSMC_CLKIN_p[2..1]
15 HSMC_CLKIN_n[2..1]

## XCVR Reference Clock

6 REFCLK_p[1..0]
6 REFCLK_n[1..0]

## HDMI TX

14 HDMI_TX_CLK
14 HDMI_TX_DE
14 HDMI_TX_INT

## GPIO

4,8,17,19 GPIO[35..0]

## I2C Interface

15 I2C_SDA
15 I2C_SCL

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# CYCLONE V GX Clock

| | | | | | |
|---|---|---|---|---|---|
| CLOCK_50_B3B | T13 | IO_3B/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B15P | **Bank 3B** VCCIO = 1.2V | AF7 | DDR2LP_CA2 |
| HDMI_TX_INT | T12 | IO_3B/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B15N | IO_3B/FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTP,FPLL_BL_FB/DIFFIO_TX_B21P/DQ3B/B_CA_2 | AF8 | DDR2LP_CA3 |
| KEY0 | P11 | IO_3B/CLK1P/DIFFIO_RX_B23P | IO_3B/FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTN/DIFFIO_TX_B21N/DQ3B/B_CA_3 | | |
| KEY1 | P12 | IO_3B/CLK1N/DIFFIO_RX_B23N | | | |
| CLOCK_125_p | U12 | IO_4A/CLK2P/DIFFIO_RX_B31P | **Bank 4A** VCCIO = 1.2V | | |
| CLOCK_125_n | V12 | IO_4A/CLK2N/DIFFIO_RX_B31N | | | |
| KEY2 | Y15 | IO_4A/CLK3P/DIFFIO_RX_B39P | | | |
| KEY3 | Y16 | IO_4A/CLK3N/DIFFIO_RX_B39N | | | |
| CLOCK_50_B5B | R20 | IO_5B/CLK6P/DIFFIO_RX_R17P | **Bank 5B** VCCIO = 3.3V | Y25 | HDMI_TX_CLK |
| GPIO7 | P20 | IO_5B/CLK6N/DIFFIO_RX_R17N | IO_5B/FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTP,FPLL_BR_FB/DIFFIO_TX_R20P/DQ3R | Y26 | HDMI_TX_DE |
| GPIO0 | T21 | IO_5B/CLK7P,FPLL_BR_FBP/DIFFIO_RX_R9P | IO_5B/FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTN/DIFFIO_TX_R20N/DQ3R | | |
| GPIO8 | T22 | IO_5B/CLK7N,FPLL_BR_FBN/DIFFIO_RX_R9N | | | |
| CLOCK_50_B6A | N20 | IO_6A/CLK5P/DIFFIO_RX_R25P | **Bank 6A** VCCIO = 3.3V | F26 | GPIO16 |
| GPIO6 | M21 | IO_6A/CLK5N/DIFFIO_RX_R25N | IO_6A/FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTP,FPLL_TR_FB/DIFFIO_TX_R28P/DQ4R | G26 | GPIO18 |
| GPIO2 | K25 | IO_6A/CLK4P,FPLL_TR_FBP/DIFFIO_RX_R33P | IO_6A/FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTN/DIFFIO_TX_R28N/DQ4R | | |
| GPIO4 | K26 | IO_6A/CLK4N,FPLL_TR_FBN/DIFFIO_RX_R33N | | | |
| CLOCK_50_B7A | H12 | IO_7A/CLK10P/DIFFIO_RX_T33P | **Bank 7A** VCCIO = 2.5V | | |
| I2C_SDA | G11 | IO_7A/CLK10N/DIFFIO_RX_T33N | | | |
| HSMC_CLKIN_p1 | G15 | IO_7A/CLK11P/DIFFIO_RX_T25P | | | |
| HSMC_CLKIN_n1 | G14 | IO_7A/CLK11N/DIFFIO_RX_T25N | | | |
| HSMC_CLKIN_p2 | L8 | IO_8A/CLK8P,FPLL_TL_FBP/DIFFIO_RX_T49P | **Bank 8A** VCCIO = 2.5V | A7 | HSMC_CLKOUT0 |
| HSMC_CLKIN_n2 | K9 | IO_8A/CLK8N,FPLL_TL_FBN/DIFFIO_RX_T49N | IO_8A/FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTP,FPLL_TL_FB/DIFFIO_TX_T44P/DQ6T/T_CA_2 | B7 | I2C_SCL |
| HSMC_CLKIN0 | N9 | IO_8A/CLK9P/DIFFIO_RX_T41P | IO_8A/FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTN/DIFFIO_TX_T44N/DQ6T/T_CA_3 | | |
| CLOCK_50_B8A | M10 | IO_8A/CLK9N/DIFFIO_RX_T41N | | | |

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R223 1K

CLOCK_125_p R188 100 CLOCK_125_n
HSMC_CLKIN_p1 R200 100 HSMC_CLKIN_n1
HSMC_CLKIN_p2 R197 100 HSMC_CLKIN_n2

VCC2P5: C264 0.1u 10V DNI, C263 0.1u 10V; C270 0.1u 10V, C267 0.1u 10V, C269 0.1u 10V, C268 0.1u 10V

C118 18p 50V DNI
C119 18p 50V DNI
Y1 25.00MHz

U20 SI5338

| | | | |
|---|---|---|---|
| CLKIN_P | 1 | VDD1 | 7 |
| CLKIN_N | 2 | VDD2 | 24 |
| CLKIN | 3 | VDDO3 | 11 |
| | | VDDO2 | 15 |
| I2C_LSB | 4 | VDDO1 | 16 |
| FDBK_P | 5 | VDDO0 | 20 |
| FDBK_N | 6 | INTR | 8 → SI5338_INTR |
| 2.5V CMOS | | CLK3B | 9 → PLL_50_OUT1 |
| | | CLK3A | 10 → PLL_50_OUT0 |
| 2.5V LVDS | | CLK2B | 13 → CLK_125_n1 |
| | | CLK2A | 14 → CLK_125_p1 |
| 2.5V LVDS | | CLK1B | 17 → CLK_125_n0 |
| | | CLK1A | 18 → CLK_125_p0 |
| 2.5V LVDS | | CLK0B | 21 → CLK_156_n0 |
| | | CLK0A | 22 → CLK_156_p0 |
| SCL | 12 | RSVD_GND | 23 |
| SDA | 19 | EPAD | 25 |

VCC2P5 VCC2P5
R214 1K DNI
R215 1K DNI
I2C_SCL R104 22 SI5338_SCL
I2C_SDA R105 22 SI5338_SDA

Default :
I2C Address 0xE0/E1

VCC2P5 R111 1K TP16

R110 0 CLOCK_50_B8A
R108 0 CLOCK_50_B7A
R101 0 CLOCK_125_n
R100 0 CLOCK_125_p

C110 0.1u 10V REFCLK_n0
C109 0.1u 10V REFCLK_p0
C113 0.1u 10V REFCLK_n1
C114 0.1u 10V REFCLK_p1

VCC3P3
R112 20K
C111 0.1u 10V
X2 50MHz (EN, VCC, GND, OUT)
OSC_50
R103 0 CLOCK_50_B5B
R102 0 CLOCK_50_B6A

VCC3P3 C106 0.1u 10V DNI
OSC_50
VCC3P3 VCC1P2 U18 SN74AVC1T45 DNI
CLOCK_50_B3B
VCC1P2 C107 0.1u 10V DNI

DIR = Low : B data to A bus

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Title: Cyclone V GX Starter Kit
Size B | Document Number: FPGA Clock | Rev B
Date: Friday, November 15, 2013 | Sheet 7 of 23

www.terasic.com

## USB Blaster

23 BST_TCK
23 BST_TMS
23 BST_TDI
23 BST_TDO

## CPU_RESET

17,18 CPU_RESET_n

## Micro SD Card

12 SD_CLK
12 SD_CMD
12 SD_DAT[3..0]

## GPIO

4,7,17,19 GPIO[35..0]

## HSMC JTAG

15 HSMC_JTAG_TCK
15 HSMC_JTAG_TMS
15 HSMC_JTAG_TDI
15 HSMC_JTAG_TDO

## EPCQ Interface

23 EPCQ_AS_DATA0
23 EPCQ_AS_DATA1
23 EPCQ_DCLK
23 EPCQ_nCSO

23 FPGA_CONF_DONE
23 FPGA_nCONFIG
23 FPGA_nCE

R175 0 DNI JTAG_FPGA_TCK
C165 33p 50V DNI
R51 1K
VCC3P3 VCC3P3
R54 1K
R56 1K
VCC3P3
R189 10K DNI
R191 0 DNI
C189 12p 50V DNI
R190 1K DNI

Design Note:
Optional termination resistor for DCLK

CAD Note:
Place near FPGA DCLK pin

U14-1

# CYCLONE V GX Configuration

### Bank 3A
VCCIO = 3.3V

TCK JTAG_FPGA_TCK Y5
TMS JTAG_FPGA_TMS R6
TDI JTAG_FPGA_TDI T6
TDO JTAG_FPGA_TDO V7
DCLK EPCQ_DCLK N8
AS_DATA0,ASDO/DATA0 EPCQ_AS_DATA0 AF5
AS_DATA1/DATA1 EPCQ_AS_DATA1 AD5
AS_DATA2/DATA2 EPCQ_AS_DATA2 AB5
AS_DATA3/DATA3 EPCQ_AS_DATA3 U6
nCSO/DATA4 EPCQ_nCSO Y6
IO_3A/DATA5/DIFFIO_TX_B2N SD_DAT0 U7
IO_3A/DATA6/DIFFIO_RX_B1N/DQ1B SD_DAT1 T7
IO_3A/DATA7/DIFFIO_TX_B2P/DQ1B SD_DAT2 V8
IO_3A/DATA8/DIFFIO_RX_B1P/DQ1B SD_DAT3 T8
IO_3A/DATA9/DIFFIO_TX_B4N/DQ1B SD_CLK AB6
IO_3A/DATA10/DIFFIO_RX_B3N/DQSN1B SD_CMD W8
IO_3A/DATA11/DIFFIO_TX_B4P GPIO21 AA6
IO_3A/DATA12/DIFFIO_RX_B3P/DQS1B GPIO17 Y9
IO_3A/DATA13/DIFFIO_TX_B6N/DQ1B GPIO20 AA7
IO_3A/DATA14/DIFFIO_RX_B5N/DQ1B GPIO15 R10
IO_3A/DATA15/DIFFIO_TX_B6P/DQ1B GPIO19 Y8
IO_3A/CLKUSR/DIFFIO_RX_B5P/DQ1B GPIO14 R9
IO_3A/DIFFIO_TX_B8P/DQ1B GPIO22 AD7

### Bank 5A
VCCIO = 3.3V

IO_5A/INIT_DONE/DIFFIO_RX_R2P U19 GPIO10
IO_5A/DEV_OE/DIFFIO_TX_R5P AC24 GPIO33
IO_5A/DEV_CLRN/DIFFIO_TX_R5N/DQ1R AB24 CPU_RESET_n
IO_5A/CRC_ERROR/DIFFIO_RX_R2N V20 GPIO26
IO_5A/nCEO/DIFFIO_TX_R3P/DQ1R AA22 GPIO32
IO_5A/nPERSTL0/DIFFIO_RX_R6P/DQS1R V22 GPIO25
IO_5A/CVP_CONFDONE/DIFFIO_TX_R3N/DQ1R AA23 GPIO31
IO_5A/nPERSTL1/DIFFIO_RX_R6N/DQSN1R U22 GPIO11
IO_5A/PR_REQUEST/DIFFIO_TX_R1N/DQ1R AC23 GPIO34
IO_3A/PR_READY/DIFFIO_TX_B8N/DQ1B AD6 GPIO23
IO_3A/PR_ERROR/DIFFIO_RX_B7P P8 GPIO12
IO_3A/PR_DONE/DIFFIO_RX_B7N R8 GPIO13

### Bank 9A

CONF_DONE FPGA_CONF_DONE A6
nSTATUS FPGA_nSTATUS B5
nCONFIG FPGA_nCONFIG F5
nCE FPGA_nCE D5
MSEL0 M7 MSEL0
MSEL1 L6 MSEL1
MSEL2 A2 MSEL2
MSEL3 K5 MSEL3
MSEL4 J5 MSEL4

5CGXFC5C6F27C7N

VCC3P3
RN22 10K
FPGA_CONF_DONE
FPGA_nSTATUS
FPGA_nCONFIG
FPGA_nCE

VCC3P3
R84 0
R82 0 DNI
R88 0 DNI
R79 0
R78 0 DNI
R85 0 DNI
R81 0
R87 0
R80 0 DNI
R77 0

MSEL Settings : MSEL[4:0] = 10010
Active serial (AS)(x1 and x4),
no compression, no security, fast POR

FPGA
HSMC

BST_TDI R177 0 DNI JTAG_FPGA_TDO — R173 0 DNI HSMC_JTAG_TDO
BST_TDO R53 0 JTAG_FPGA_TDI — R52 0 HSMC_JTAG_TDI
BST_TMS R55 0 JTAG_FPGA_TMS — R178 0 DNI HSMC_JTAG_TMS
BST_TCK R50 0 JTAG_FPGA_TCK — R176 0 HSMC_JTAG_TCK

LOW --> NC to/from COM = ON and NO to/from COM = OFF
HIGH --> NC to/from COM = OFF and NO to/from COM = ON

Logic 0 = pin 10 <--> pin 9 (HSMC Bypass)
Logic 1 = pin 10 <--> pin 2 (HSMC Enable)

VCC3P3
R27 10K
HSMC_JTAG_EN
HSMC_JTAG_TDO
JTAG_FPGA_TMS
XJ8 Jumper-2.54mm
JP2 HEADER 2 HSMC_DISABLE
Default Jumper Short

U3 TS5A23157
IN1 NO1 GND NO2 IN2 COM1 NC1 V+ NC2 COM2
1 2 3 4 5 10 9 8 7 6
BST_TDI
HSMC_JTAG_TDI R137 1K DNI VCC3P3
JTAG_FPGA_TDO -> JTAG_HSMC_TDI
VCC3P3
R136 1K VCC3P3
HSMC_JTAG_TMS
C131 0.1u 10V

JP2 HSMC JTAG Chain Enable / Disable

| | HSMC JTAG Chain Select |
|---|---|
| Open | Enable HSMC JTAG Chain |
| Short | Disable HSMC JTAG Chain |

VCC3P3
C164 0.1u 10V
U9 EPCQ256
NC01 NC02 NC03 NC04 NC05 NC06 NC07 NC08 VCC GND DATA0 DATA1 DATA2 DATA3 DCLK nCS
3 4 5 6 11 12 13 14 2 10 15 8 9 1 16 7
EPCQ_AS_DATA0
EPCQ_AS_DATA1
EPCQ_AS_DATA2
EPCQ_AS_DATA3
EPCQ_DCLK
EPCQ_nCSO
VCC3P3
R160 10K
R174 10K

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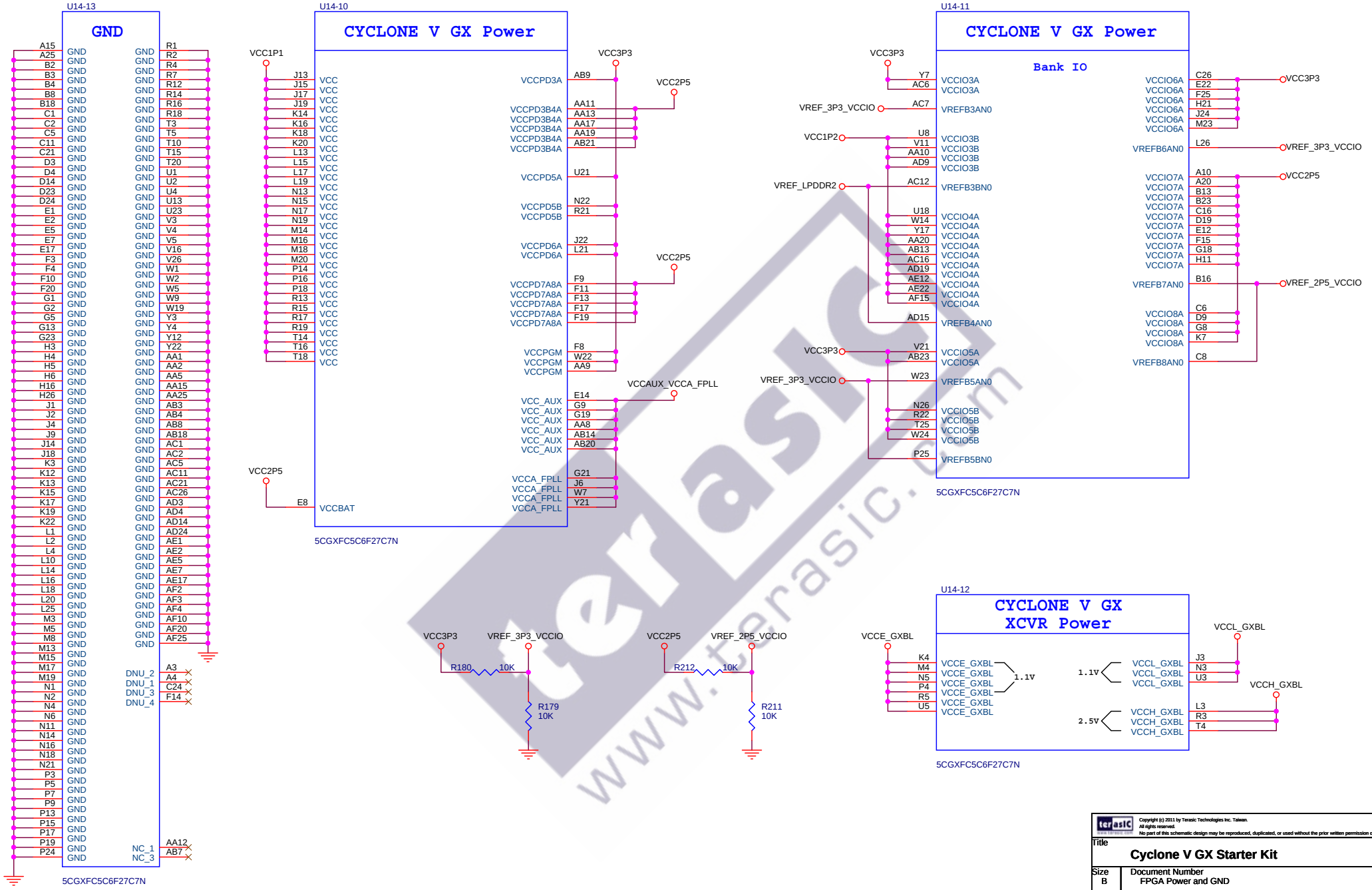
Title: Cyclone V GX Starter Kit
Size B | Document Number: FPGA Configuration and JTAG | Rev B
Date: Friday, November 15, 2013 | Sheet 8 of 23

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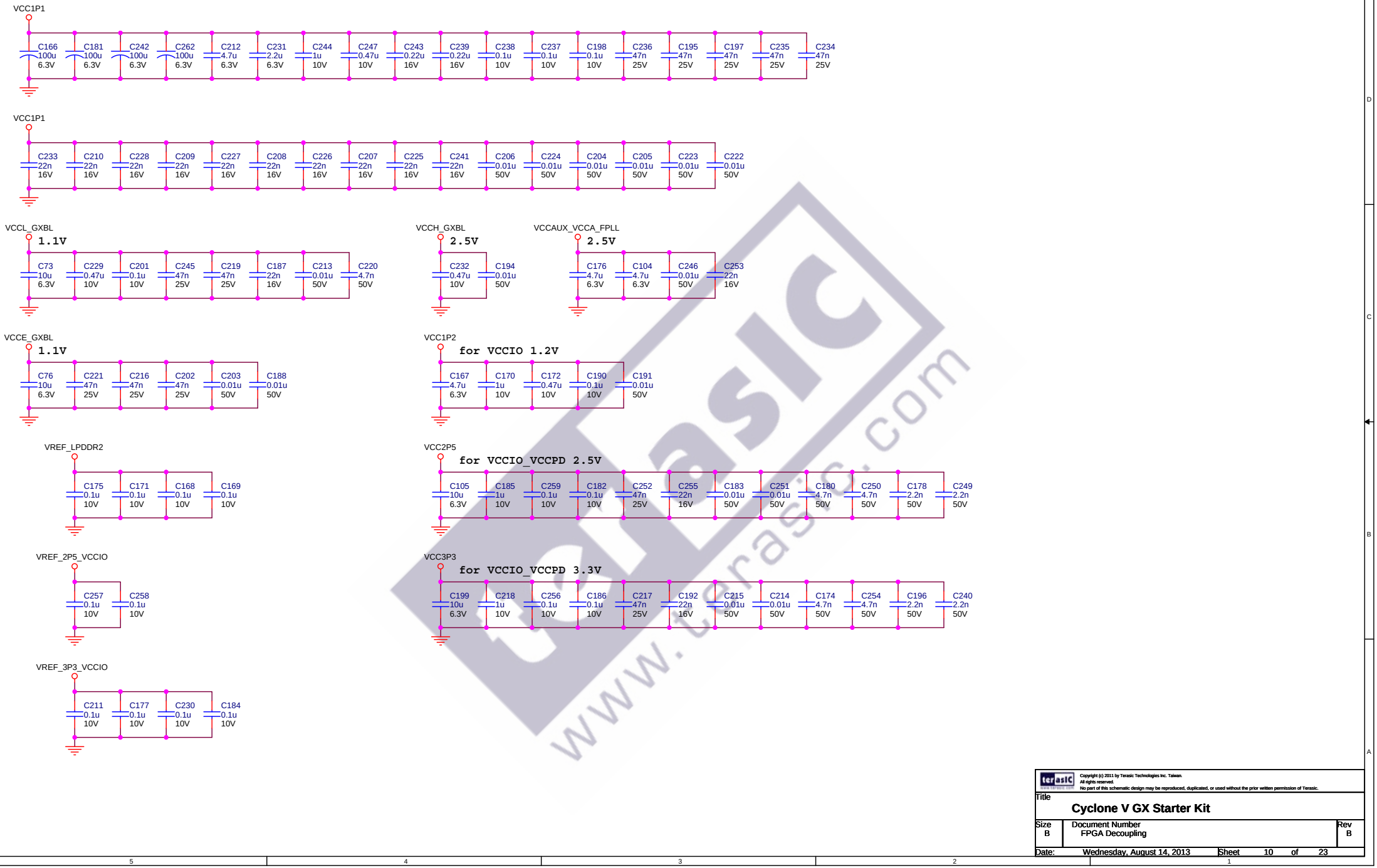
Title: **Cyclone V GX Starter Kit**

| Size | Document Number | Rev |
|---|---|---|
| B | FPGA Power and GND | B |

Date: Friday, November 15, 2013 Sheet 9 of 23

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Title: **Cyclone V GX Starter Kit**

| Size | Document Number | Rev |
|---|---|---|
| B | FPGA Decoupling | B |

Date: Wednesday, August 14, 2013 Sheet 10 of 23

# LPDDR2 SDRAM (16M X 32 X 8 banks x 1 die)

**LPDDR2 Interface**

3,7 DDR2LP_CA[9..0]
3 DDR2LP_CK_p
3 DDR2LP_CK_n
3 DDR2LP_CKE[1..0]
3 DDR2LP_CS_n[1..0]
3 DDR2LP_DM[3..0]
3 DDR2LP_DQ[31..0]
3 DDR2LP_DQS_p[3..0]
3 DDR2LP_DQS_n[3..0]

U8A

DDR2LP_CA0 AC6 CA0
DDR2LP_CA1 AB6 CA1
DDR2LP_CA2 AC7 CA2
DDR2LP_CA3 AB8 CA3
DDR2LP_CA4 AB9 CA4
DDR2LP_CA5 W1 CA5
DDR2LP_CA6 V2 CA6
DDR2LP_CA7 U1 CA7
DDR2LP_CA8 T2 CA8
DDR2LP_CA9 T1 CA9

DDR2LP_CK_p Y2 CK
DDR2LP_CK_n Y1 CK#

R169 4.7K DDR2LP_CKE0 AC3 CKE0
R168 4.7K DDR2LP_CKE1 AC4 CKE1
DNI

DDR2LP_CS_n0 AB3 CS#0
DDR2LP_CS_n1 AB4 CS#1

DDR2LP_DM0 N23 DM0
DDR2LP_DM1 L23 DM1
DDR2LP_DM2 AB20 DM2
DDR2LP_DM3 B20 DM3

R42 240 DDR2LP_ZQ0 P1 ZQ
R34 240 DDR2LP_ZQ1 AC11 NC/ZQ
DNI

A3 NC0
A4 NC1
A5 NC2
A6 NC3
A7 NC4
A8 NC5
A9 NC6
A10 NC7
B4 NC8
B6 NC9
B7 NC10
B9 NC11
D1 NC12
D2 NC13
E1 NC14
E2 NC15
F1 NC16
G1 NC17
G2 NC18
H1 NC19
H2 NC20
J1 NC21
K1 NC22
K2 NC23
L1 NC24
L2 NC25
M1 NC26
N1 NC27
AC10 NC28

place close to DDR2 chip
DDR2LP_CK_p R164 100 DDR2LP_CK_n
DNI

DQS0 R23 DDR2LP_DQS_p0
DQS#0 P22 DDR2LP_DQS_n0
DQS1 J22 DDR2LP_DQS_p1
DQS#1 K23 DDR2LP_DQS_n1
DQS2 AB18 DDR2LP_DQS_p2
DQS#2 AC19 DDR2LP_DQS_n2
DQS3 B18 DDR2LP_DQS_p3
DQS#3 A19 DDR2LP_DQS_n3

DQ0 AA23 DDR2LP_DQ0
DQ1 Y22 DDR2LP_DQ1
DQ2 W22 DDR2LP_DQ2
DQ3 W23 DDR2LP_DQ3
DQ4 V23 DDR2LP_DQ4
DQ5 U22 DDR2LP_DQ5
DQ6 T22 DDR2LP_DQ6
DQ7 T23 DDR2LP_DQ7
DQ8 H22 DDR2LP_DQ8
DQ9 H23 DDR2LP_DQ9
DQ10 G23 DDR2LP_DQ10
DQ11 F22 DDR2LP_DQ11
DQ12 E22 DDR2LP_DQ12
DQ13 E23 DDR2LP_DQ13
DQ14 D23 DDR2LP_DQ14
DQ15 C22 DDR2LP_DQ15
DQ16 AB12 DDR2LP_DQ16
DQ17 AC13 DDR2LP_DQ17
DQ18 AB14 DDR2LP_DQ18
DQ19 AC14 DDR2LP_DQ19
DQ20 AB15 DDR2LP_DQ20
DQ21 AC16 DDR2LP_DQ21
DQ22 AB17 DDR2LP_DQ22
DQ23 AC17 DDR2LP_DQ23
DQ24 B17 DDR2LP_DQ24
DQ25 A17 DDR2LP_DQ25
DQ26 A16 DDR2LP_DQ26
DQ27 B15 DDR2LP_DQ27
DQ28 B14 DDR2LP_DQ28
DQ29 A14 DDR2LP_DQ29
DQ30 A13 DDR2LP_DQ30
DQ31 B12 DDR2LP_DQ31

DNU0 A1
DNU1 A2
DNU2 A22
DNU3 A23
DNU4 B1
DNU5 B2
DNU6 B22
DNU7 B23
DNU8 AB1
DNU9 AB2
DNU10 AB22
DNU11 AB23
DNU12 AC1
DNU13 AC2
DNU14 AC22
DNU15 AC23

MT42L128M32D1LF-25WT

U8B

VCC1P8
A11 VDD1
A20 VDD1
B3 VDD1
N2 VDD1
N22 VDD1
AB5 VDD1
AC20 VDD1
VDD1

VCC1P2
B11 VDD2
B21 VDD2
C2 VDD2
L22 VDD2
R2 VDD2
AA2 VDD2
AB10 VDD2
AB21 VDD2
VDD2

A21 VSS
B10 VSS
C1 VSS
M2 VSS
M23 VSS
R1 VSS
AA1 VSS
AB11 VSS
AC5 VSS
AC21 VSS
AC9 VSS
B5 VSS/NC
B8 VSS/NC
F2 VSS/NC
J2 VSS/NC
VSS/NC

VREFCA P2
VREFDQ M22
DDR2LP_VREFCA
VREF_LPDDR2

VDDCA U2
VDDCA W2
VDDCA AC8

VDDQ B13
VDDQ B16
VDDQ B19
VDDQ D22
VDDQ G22
VDDQ K22
VDDQ R22
VDDQ V22
VDDQ AA22
VDDQ AB13
VDDQ AB16
VDDQ AB19
VDDQ

VSSCA V1
VSSCA AB7

VSSQ A12
VSSQ A15
VSSQ A18
VSSQ C23
VSSQ F23
VSSQ J23
VSSQ P23
VSSQ U23
VSSQ Y23
VSSQ AC12
VSSQ AC15
VSSQ AC18
VSSQ

MT42L128M32D1LF-25WT

VCC1P2
VREF_LPDDR2
R161 2.1K
R154 2.1K
C154 0.1u 10V
C160 0.1u 10V
R162 2.1K
R155 2.1K

Note:
Place resistors and Capacitor near LPDDR2 VREFCA and VREFDQ pins

Note:
Place decoupling caps near LPDDR2 power pins

VCC1P2
C155 10u 10V
C40 10u 10V
C159 4.7u 6.3V
C153 0.1u 10V
C145 0.1u 10V
C158 0.1u 10V
C146 22n 16V
C162 22n 16V
C161 0.01u 50V
C148 0.01u 50V
C156 4.7n 50V
C157 4.7n 50V
C151 2.2n 50V
C163 2.2n 50V

VCC1P8
C150 4.7u 6.3V
C147 0.1u 10V

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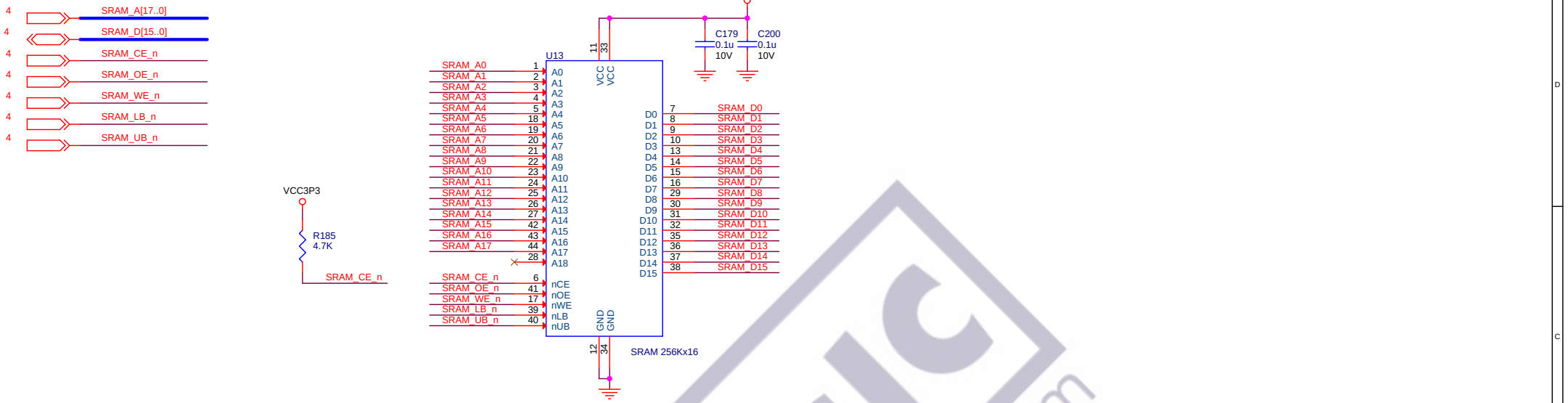
Title: **Cyclone V GX Starter Kit**

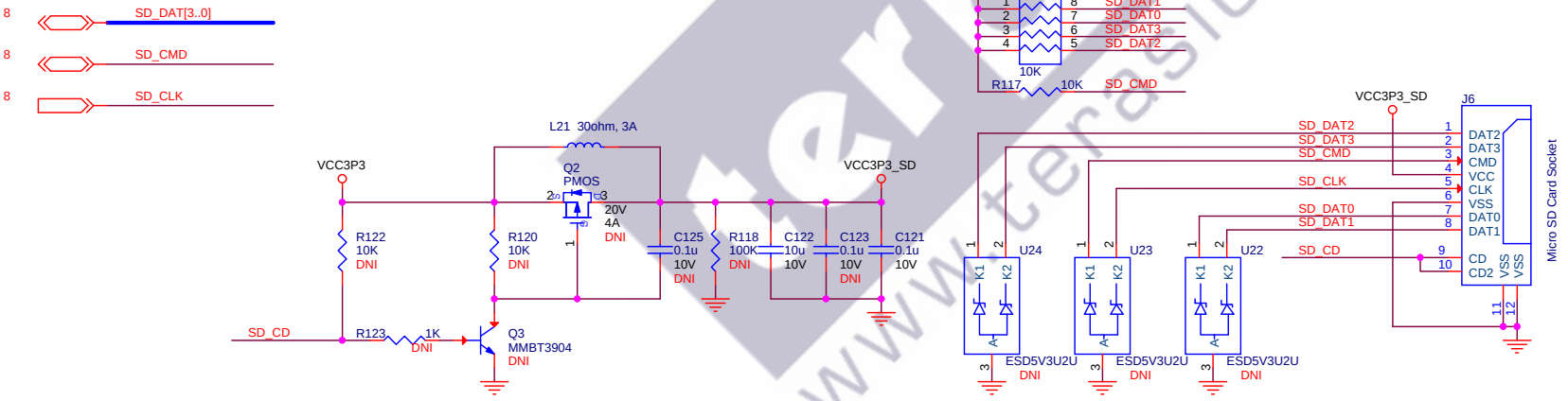
Size B | Document Number: LPDDR2 SDRAM | Rev B

Date: Wednesday, September 04, 2013 | Sheet 11 of 23

## SRAM




## Micro SD Card

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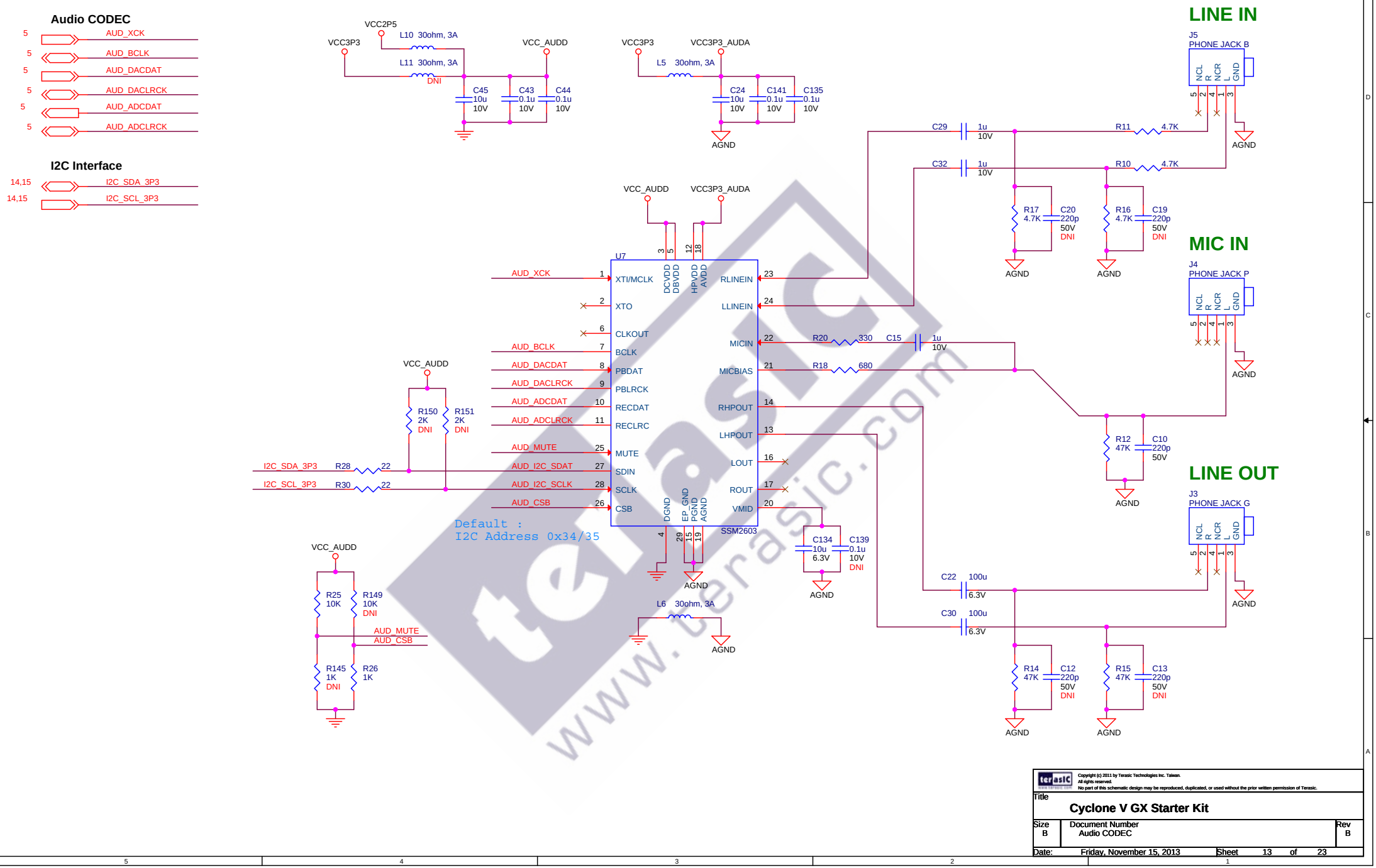
| | | |
|---|---|---|
| Title | Cyclone V GX Starter Kit | |
| Size B | Document Number SRAM and SD Card | Rev B |
| Date: Tuesday, August 20, 2013 | Sheet 12 of 23 | |


Audio CODEC
AUD_XCK
AUD_BCLK
AUD_DACDAT
AUD_DACLRCK
AUD_ADCDAT
AUD_ADCLRCK
I2C Interface
I2C_SDA_3P3
I2C_SCL_3P3
VCC2P5
L10 30ohm, 3A
L11 30ohm, 3A
DNI
VCC3P3
VCC_AUDD
C45 10u 10V
C43 0.1u 10V
C44 0.1u 10V
L5 30ohm, 3A
VCC3P3_AUDA
C24 10u 10V
C141 0.1u 10V
C135 0.1u 10V
AGND
U7
SSM2603
XTI/MCLK
XTO
CLKOUT
BCLK
PBDAT
PBLRCK
RECDAT
RECLRC
MUTE
SDIN
SCLK
CSB
DCVDD
DBVDD
HPVDD
AVDD
DGND
EP_GND
PGND
AGND
RLINEIN
LLINEIN
MICIN
MICBIAS
RHPOUT
LHPOUT
LOUT
ROUT
VMID
R150 2K DNI
R151 2K DNI
R28 22
R30 22
R25 10K
R149 10K DNI
R145 1K DNI
R26 1K
AUD_MUTE
AUD_CSB
L6 30ohm, 3A
C134 10u 6.3V
C139 0.1u 10V DNI
Default :
I2C Address 0x34/35
LINE IN
J5
PHONE JACK B
NCL
R
NCR
L
GND
C29 1u 10V
C32 1u 10V
R11 4.7K
R10 4.7K
R17 4.7K
C20 220p 50V DNI
R16 4.7K
C19 220p 50V DNI
MIC IN
J4
PHONE JACK P
R20 330
C15 1u 10V
R18 680
R12 47K
C10 220p 50V
LINE OUT
J3
PHONE JACK G
C22 100u 6.3V
C30 100u 6.3V
R14 47K
C12 220p 50V DNI
R15 47K
C13 220p 50V DNI
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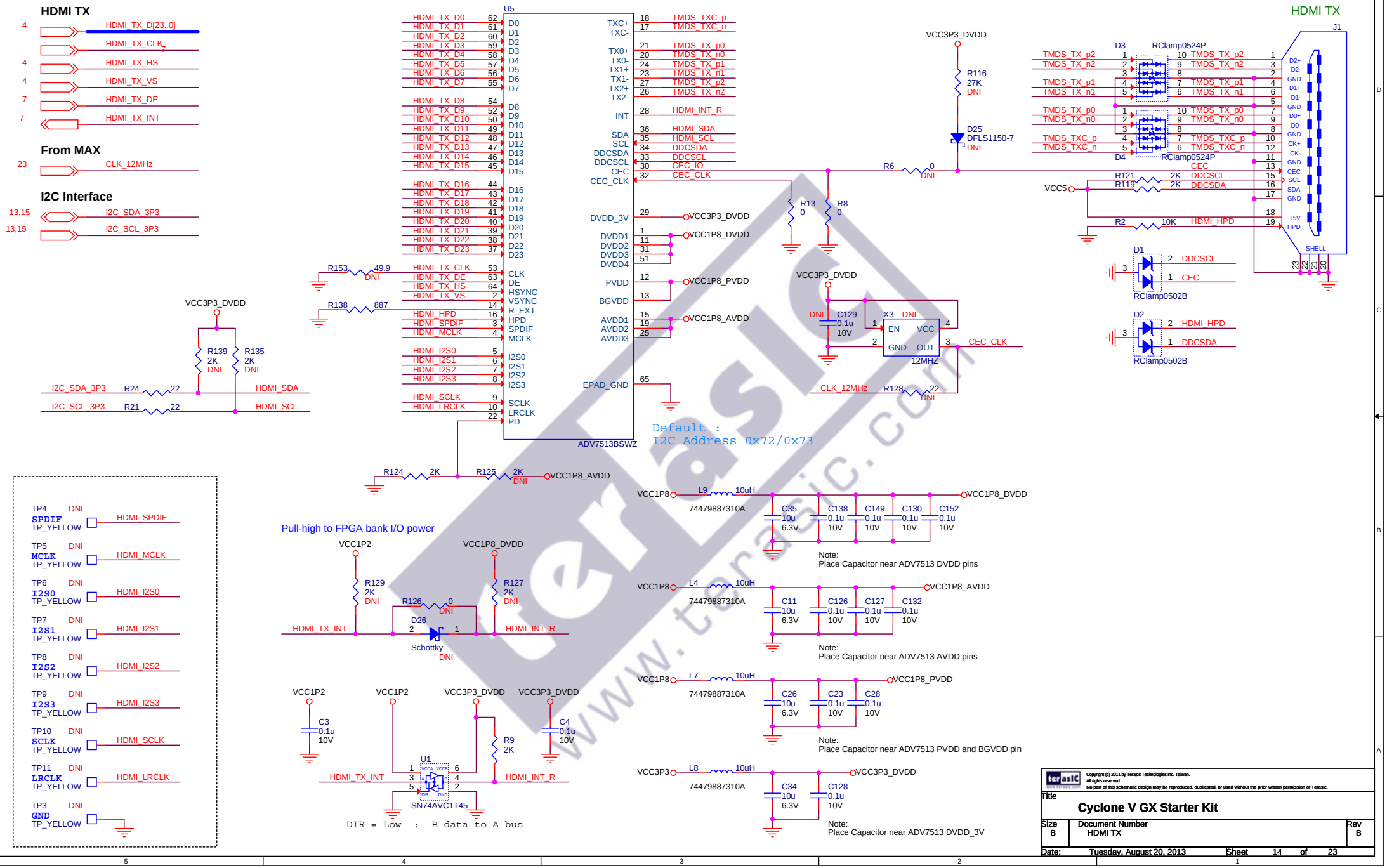
Title
Cyclone V GX Starter Kit
Size B
Document Number
Audio CODEC
Rev B
Date: Friday, November 15, 2013
Sheet 13 of 23


HDMI TX
HDMI_TX_D[23..0]
HDMI_TX_CLK
HDMI_TX_HS
HDMI_TX_VS
HDMI_TX_DE
HDMI_TX_INT
From MAX
CLK_12MHz
I2C Interface
I2C_SDA_3P3
I2C_SCL_3P3
U5
ADV7513BSWZ
HDMI_TX_D0
HDMI_TX_D1
HDMI_TX_D2
HDMI_TX_D3
HDMI_TX_D4
HDMI_TX_D5
HDMI_TX_D6
HDMI_TX_D7
HDMI_TX_D8
HDMI_TX_D9
HDMI_TX_D10
HDMI_TX_D11
HDMI_TX_D12
HDMI_TX_D13
HDMI_TX_D14
HDMI_TX_D15
HDMI_TX_D16
HDMI_TX_D17
HDMI_TX_D18
HDMI_TX_D19
HDMI_TX_D20
HDMI_TX_D21
HDMI_TX_D22
HDMI_TX_D23
HDMI_TX_CLK
HDMI_TX_DE
HDMI_TX_HS
HDMI_TX_VS
HDMI_HPD
HDMI_SPDIF
HDMI_MCLK
HDMI_I2S0
HDMI_I2S1
HDMI_I2S2
HDMI_I2S3
HDMI_SCLK
HDMI_LRCLK
TMDS_TXC_p
TMDS_TXC_n
TMDS_TX_p0
TMDS_TX_n0
TMDS_TX_p1
TMDS_TX_n1
TMDS_TX_p2
TMDS_TX_n2
HDMI_INT_R
HDMI_SDA
HDMI_SCL
DDCSDA
DDCSCL
CEC_IO
CEC_CLK
VCC3P3_DVDD
VCC1P8_DVDD
VCC1P8_PVDD
VCC1P8_AVDD
EPAD_GND
R153 49.9 DNI
R138 887
R139 2K DNI
R135 2K DNI
R24 22
R21 22
R124 2K
R125 2K DNI
R116 27K DNI
D25 DFLS1150-7 DNI
R6 0 DNI
R13 0
R8 0
R121 2K DDCSCL
R119 2K DDCSDA
R2 10K HDMI_HPD
D3 RClamp0524P
D4 RClamp0524P
D1 RClamp0502B
D2 RClamp0502B
J1
SHELL
C129 0.1u 10V DNI
X3 DNI
EN VCC GND OUT
12MHZ
CLK_12MHz
R128 22 DNI
Default :
I2C Address 0x72/0x73
Pull-high to FPGA bank I/O power
R129 2K DNI
R126 0 DNI
R127 2K DNI
D26
Schottky
DNI
C3 0.1u 10V
C4 0.1u 10V
R9 2K
U1
SN74AVC1T45
DIR = Low : B data to A bus
L9 10uH
74479887310A
C35 10u 6.3V
C138 0.1u 10V
C149 0.1u 10V
C130 0.1u 10V
C152 0.1u 10V
Note:
Place Capacitor near ADV7513 DVDD pins
L4 10uH
74479887310A
C11 10u 6.3V
C126 0.1u 10V
C127 0.1u 10V
C132 0.1u 10V
Note:
Place Capacitor near ADV7513 AVDD pins
L7 10uH
74479887310A
C26 10u 6.3V
C23 0.1u 10V
C28 0.1u 10V
Note:
Place Capacitor near ADV7513 PVDD and BGVDD pin
L8 10uH
74479887310A
C34 10u 6.3V
C128 0.1u 10V
Note:
Place Capacitor near ADV7513 DVDD_3V
TP4 DNI SPDIF TP_YELLOW
TP5 DNI MCLK TP_YELLOW
TP6 DNI I2S0 TP_YELLOW
TP7 DNI I2S1 TP_YELLOW
TP8 DNI I2S2 TP_YELLOW
TP9 DNI I2S3 TP_YELLOW
TP10 DNI SCLK TP_YELLOW
TP11 DNI LRCLK TP_YELLOW
TP3 DNI GND TP_YELLOW
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Title
Cyclone V GX Starter Kit
Size B
Document Number HDMI TX
Rev B
Date: Tuesday, August 20, 2013
Sheet 14 of 23

## HSMC Transceiver

6 HSMC_GXB_TX_p[3..0]
6 HSMC_GXB_TX_n[3..0]
6 HSMC_GXB_RX_p[3..0]
6 HSMC_GXB_RX_n[3..0]

## HSMC Interface

5 HSMC_TX_p[16..0]
5 HSMC_TX_n[16..0]
5 HSMC_RX_p[16..0]
5 HSMC_RX_n[16..0]
5 HSMC_D[3..0]

## HSMC Clock

7 HSMC_CLKOUT0
7 HSMC_CLKIN0
5 HSMC_CLKOUT_p[2..1]
5 HSMC_CLKOUT_n[2..1]
7 HSMC_CLKIN_p[2..1]
7 HSMC_CLKIN_n[2..1]

## HSMC JTAG

8 HSMC_JTAG_TCK
8 HSMC_JTAG_TMS
8 HSMC_JTAG_TDI
8 HSMC_JTAG_TDO

## I2C Interface

7 I2C_SDA
7 I2C_SCL
13,14 I2C_SDA_3P3
13,14 I2C_SCL_3P3

VCC12_HSMC
C248 22u 25V
C120 10u 35V
C266 0.1u 25V
VCC3P3_HSMC
C115 10u 6.3V
C265 0.1u 25V

VCC12
JP13 HEADER 2
VCC12_HSMC
VCC3P3
VCC3P3_HSMC
XJ1 Jumper-2.54mm
Default Jumper Open
TP1 Dummy Pin

I2C_SDA R186 22 HSMC_SDA
I2C_SCL R187 22 HSMC_SCL

VCC2P5 R171 2.2K
VCC2P5 R163 2.2K
DNI Q5 FDV305N
DNI Q4 FDV305N
VCC3P3 R165 2.2K DNI
VCC3P3 R158 2.2K DNI
I2C_SDA R166 0 I2C_SDA_3P3
I2C_SCL R159 0 I2C_SCL_3P3

J14

HSMC_GXB_TX_p3 R37 0 NET_HSMC_GXB_TX_p3
HSMC_GXB_TX_n3 R39 0 NET_HSMC_GXB_TX_n3
HSMC_GXB_TX_p2 R40 0 NET_HSMC_GXB_TX_p2
HSMC_GXB_TX_n2 R41 0 NET_HSMC_GXB_TX_n2
HSMC_GXB_TX_p1 R43 0 NET_HSMC_GXB_TX_p1
HSMC_GXB_TX_n1 R45 0 NET_HSMC_GXB_TX_n1
HSMC_GXB_TX_p0 R46 0 NET_HSMC_GXB_TX_p0
HSMC_GXB_TX_n0 R49 0 NET_HSMC_GXB_TX_n0

HSMC_SDA
HSMC_JTAG_TCK
HSMC_JTAG_TDO
HSMC_CLKOUT0
HSMC_SCL
HSMC_JTAG_TMS
HSMC_JTAG_TDI
HSMC_CLKIN0

VCC3P3_HSMC
VCC12_HSMC
TX_p TX_n RX_p RX_n

HSMC_D0 HSMC_D1
HSMC_D2 HSMC_D3
HSMC_TX_p0 HSMC_RX_p0
HSMC_TX_n0 HSMC_RX_n0
HSMC_TX_p1 HSMC_RX_p1
HSMC_TX_n1 HSMC_RX_n1
HSMC_TX_p2 HSMC_RX_p2
HSMC_TX_n2 HSMC_RX_n2
HSMC_TX_p3 HSMC_RX_p3
HSMC_TX_n3 HSMC_RX_n3
HSMC_TX_p4 HSMC_RX_p4
HSMC_TX_n4 HSMC_RX_n4
HSMC_TX_p5 HSMC_RX_p5
HSMC_TX_n5 HSMC_RX_n5
HSMC_TX_p6 HSMC_RX_p6
HSMC_TX_n6 HSMC_RX_n6
HSMC_TX_p7 HSMC_RX_p7
HSMC_TX_n7 HSMC_RX_n7
HSMC_CLKOUT_p1 HSMC_CLKIN_p1
HSMC_CLKOUT_n1 HSMC_CLKIN_n1
HSMC_TX_p8 HSMC_RX_p8
HSMC_TX_n8 HSMC_RX_n8
HSMC_TX_p9 HSMC_RX_p9
HSMC_TX_n9 HSMC_RX_n9
HSMC_TX_p10 HSMC_RX_p10
HSMC_TX_n10 HSMC_RX_n10
HSMC_TX_p11 HSMC_RX_p11
HSMC_TX_n11 HSMC_RX_n11
HSMC_TX_p12 HSMC_RX_p12
HSMC_TX_n12 HSMC_RX_n12
HSMC_TX_p13 HSMC_RX_p13
HSMC_TX_n13 HSMC_RX_n13
HSMC_TX_p14 HSMC_RX_p14
HSMC_TX_n14 HSMC_RX_n14
HSMC_TX_p15 HSMC_RX_p15
HSMC_TX_n15 HSMC_RX_n15
HSMC_TX_p16 HSMC_RX_p16
HSMC_TX_n16 HSMC_RX_n16
HSMC_CLKOUT_p2 HSMC_CLKIN_p2
HSMC_CLKOUT_n2 HSMC_CLKIN_n2
HSMC_PSNT_n

HSMC PORT

VCC3P3 R216 120 D23 LEDG HSMC_PSNT_n
VCC12_HSMC R218 4.7K D24 LEDB HSMC_12V

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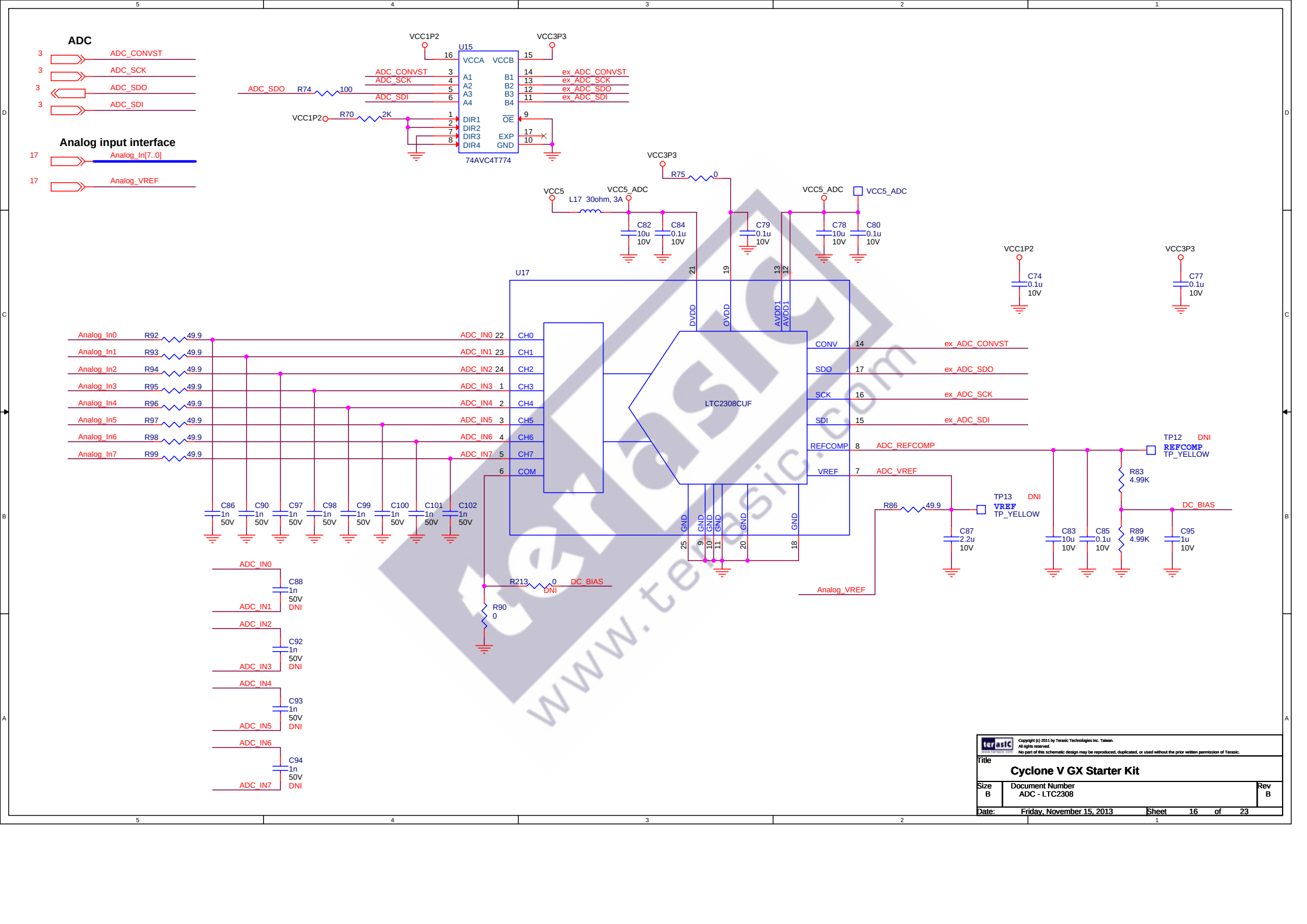
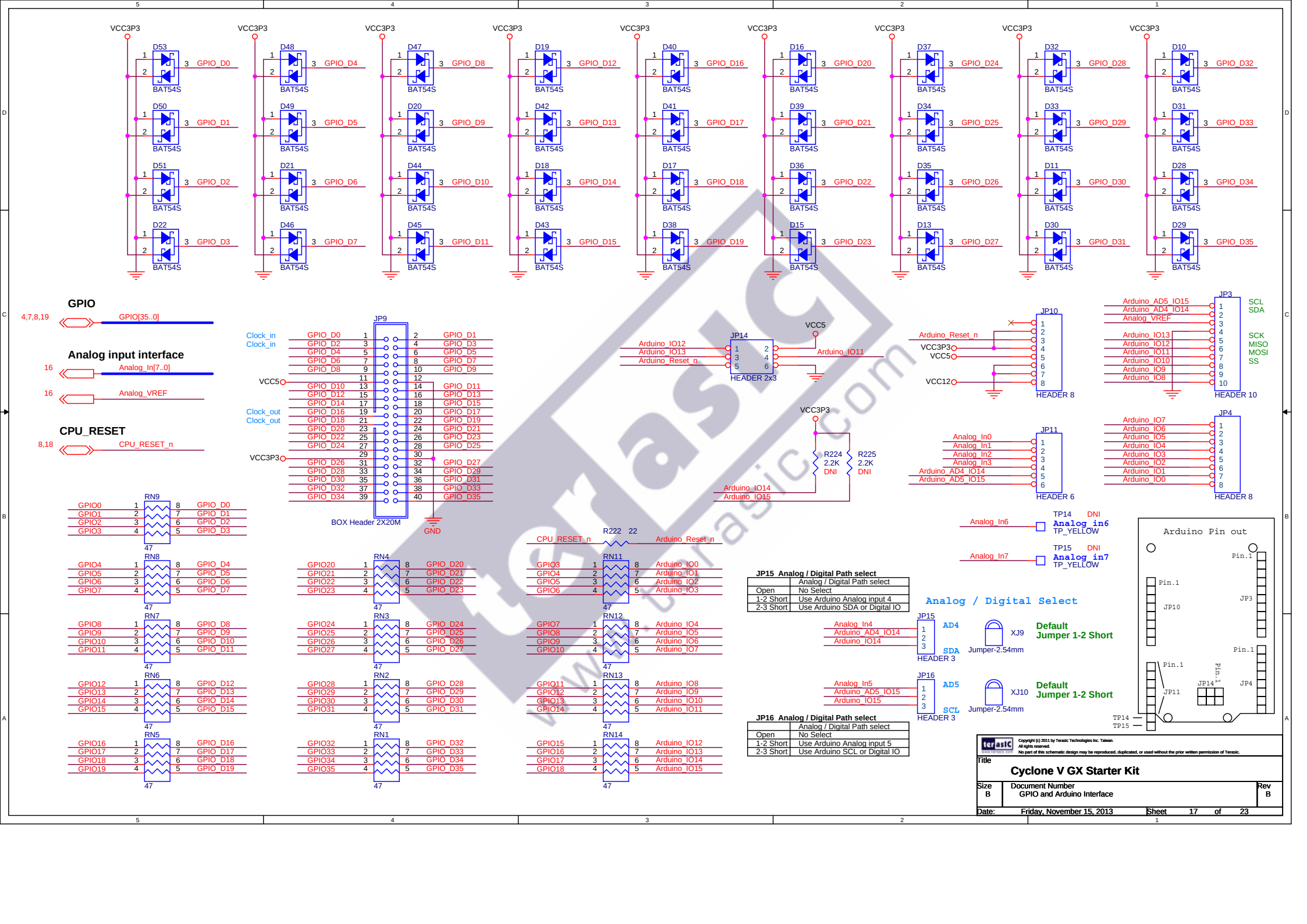
Title: Cyclone V GX Starter Kit
Size: Custom | Document Number: HSMC Interface | Rev: B
Date: Friday, November 15, 2013 | Sheet 15 of 23


ADC
ADC_CONVST
ADC_SCK
ADC_SDO
ADC_SDI
Analog input interface
Analog_In[7..0]
Analog_VREF
U15
74AVC4T774
VCC1P2
VCC3P3
R74 100
R70 2K
U17
LTC2308CUF
L17 30ohm, 3A
R75 0
R92 49.9
R93 49.9
R94 49.9
R95 49.9
R96 49.9
R97 49.9
R98 49.9
R99 49.9
R86 49.9
R213 0 DNI
R90 0
R83 4.99K
R89 4.99K
TP12 DNI REFCOMP TP_YELLOW
TP13 DNI VREF TP_YELLOW
DC_BIAS
Analog_VREF
Cyclone V GX Starter Kit
ADC - LTC2308
Friday, November 15, 2013
Sheet 16 of 23


VCC3P3
D53 D48 D47 D19 D40 D16 D37 D32 D10
D50 D49 D20 D42 D41 D39 D34 D33 D31
D51 D21 D44 D18 D17 D36 D35 D11 D28
D22 D46 D45 D43 D38 D15 D13 D30 D29
BAT54S
GPIO_D0 GPIO_D4 GPIO_D8 GPIO_D12 GPIO_D16 GPIO_D20 GPIO_D24 GPIO_D28 GPIO_D32
GPIO_D1 GPIO_D5 GPIO_D9 GPIO_D13 GPIO_D17 GPIO_D21 GPIO_D25 GPIO_D29 GPIO_D33
GPIO_D2 GPIO_D6 GPIO_D10 GPIO_D14 GPIO_D18 GPIO_D22 GPIO_D26 GPIO_D30 GPIO_D34
GPIO_D3 GPIO_D7 GPIO_D11 GPIO_D15 GPIO_D19 GPIO_D23 GPIO_D27 GPIO_D31 GPIO_D35
GPIO
4,7,8,19
GPIO[35..0]
Analog input interface
16
Analog_In[7..0]
16
Analog_VREF
CPU_RESET
8,18
CPU_RESET_n
JP9
Clock_in
Clock_in
Clock_out
Clock_out
VCC5
VCC3P3
GND
BOX Header 2X20M
JP14
HEADER 2x3
Arduino_IO12
Arduino_IO13
Arduino_Reset_n
Arduino_IO11
VCC5
JP10
HEADER 8
VCC3P3
VCC5
VCC12
JP3
HEADER 10
Arduino_AD5_IO15
Arduino_AD4_IO14
Analog_VREF
Arduino_IO13
Arduino_IO12
Arduino_IO11
Arduino_IO10
Arduino_IO9
Arduino_IO8
SCL
SDA
SCK
MISO
MOSI
SS
JP11
HEADER 6
Analog_In0
Analog_In1
Analog_In2
Analog_In3
Arduino_AD4_IO14
Arduino_AD5_IO15
JP4
HEADER 8
Arduino_IO7
Arduino_IO6
Arduino_IO5
Arduino_IO4
Arduino_IO3
Arduino_IO2
Arduino_IO1
Arduino_IO0
R224 2.2K DNI
R225 2.2K DNI
Arduino_IO14
Arduino_IO15
RN9 RN8 RN7 RN6 RN5
GPIO0 GPIO1 GPIO2 GPIO3
GPIO4 GPIO5 GPIO6 GPIO7
GPIO8 GPIO9 GPIO10 GPIO11
GPIO12 GPIO13 GPIO14 GPIO15
GPIO16 GPIO17 GPIO18 GPIO19
GPIO_D0 GPIO_D1 GPIO_D2 GPIO_D3
GPIO_D4 GPIO_D5 GPIO_D6 GPIO_D7
GPIO_D8 GPIO_D9 GPIO_D10 GPIO_D11
GPIO_D12 GPIO_D13 GPIO_D14 GPIO_D15
GPIO_D16 GPIO_D17 GPIO_D18 GPIO_D19
47
RN4 RN3 RN2 RN1
GPIO20 GPIO21 GPIO22 GPIO23
GPIO24 GPIO25 GPIO26 GPIO27
GPIO28 GPIO29 GPIO30 GPIO31
GPIO32 GPIO33 GPIO34 GPIO35
GPIO_D20 GPIO_D21 GPIO_D22 GPIO_D23
GPIO_D24 GPIO_D25 GPIO_D26 GPIO_D27
GPIO_D28 GPIO_D29 GPIO_D30 GPIO_D31
GPIO_D32 GPIO_D33 GPIO_D34 GPIO_D35
CPU_RESET_n
R222 22
Arduino_Reset_n
RN11 RN12 RN13 RN14
GPIO3 GPIO4 GPIO5 GPIO6
GPIO7 GPIO8 GPIO9 GPIO10
GPIO11 GPIO12 GPIO13 GPIO14
GPIO15 GPIO16 GPIO17 GPIO18
Arduino_IO0 Arduino_IO1 Arduino_IO2 Arduino_IO3
Arduino_IO4 Arduino_IO5 Arduino_IO6 Arduino_IO7
Arduino_IO8 Arduino_IO9 Arduino_IO10 Arduino_IO11
Arduino_IO12 Arduino_IO13 Arduino_IO14 Arduino_IO15
JP15 Analog / Digital Path select
Analog / Digital Path select
Open No Select
1-2 Short Use Arduino Analog input 4
2-3 Short Use Arduino SDA or Digital IO
JP16 Analog / Digital Path select
Analog / Digital Path select
Open No Select
1-2 Short Use Arduino Analog input 5
2-3 Short Use Arduino SCL or Digital IO
Analog / Digital Select
JP15
AD4
SDA
HEADER 3
Analog_In4
Arduino_AD4_IO14
Arduino_IO14
XJ9
Jumper-2.54mm
Default
Jumper 1-2 Short
JP16
AD5
SCL
HEADER 3
Analog_In5
Arduino_AD5_IO15
Arduino_IO15
XJ10
Jumper-2.54mm
Default
Jumper 1-2 Short
Analog_In6
TP14 DNI
Analog_in6
TP_YELLOW
Analog_In7
TP15 DNI
Analog_in7
TP_YELLOW
Arduino Pin out
Pin.1
JP10
JP3
JP11
JP14
JP4
TP14
TP15
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Title
Cyclone V GX Starter Kit
Size B
Document Number
GPIO and Arduino Interface
Rev B
Date: Friday, November 15, 2013
Sheet 17 of 23

KEY

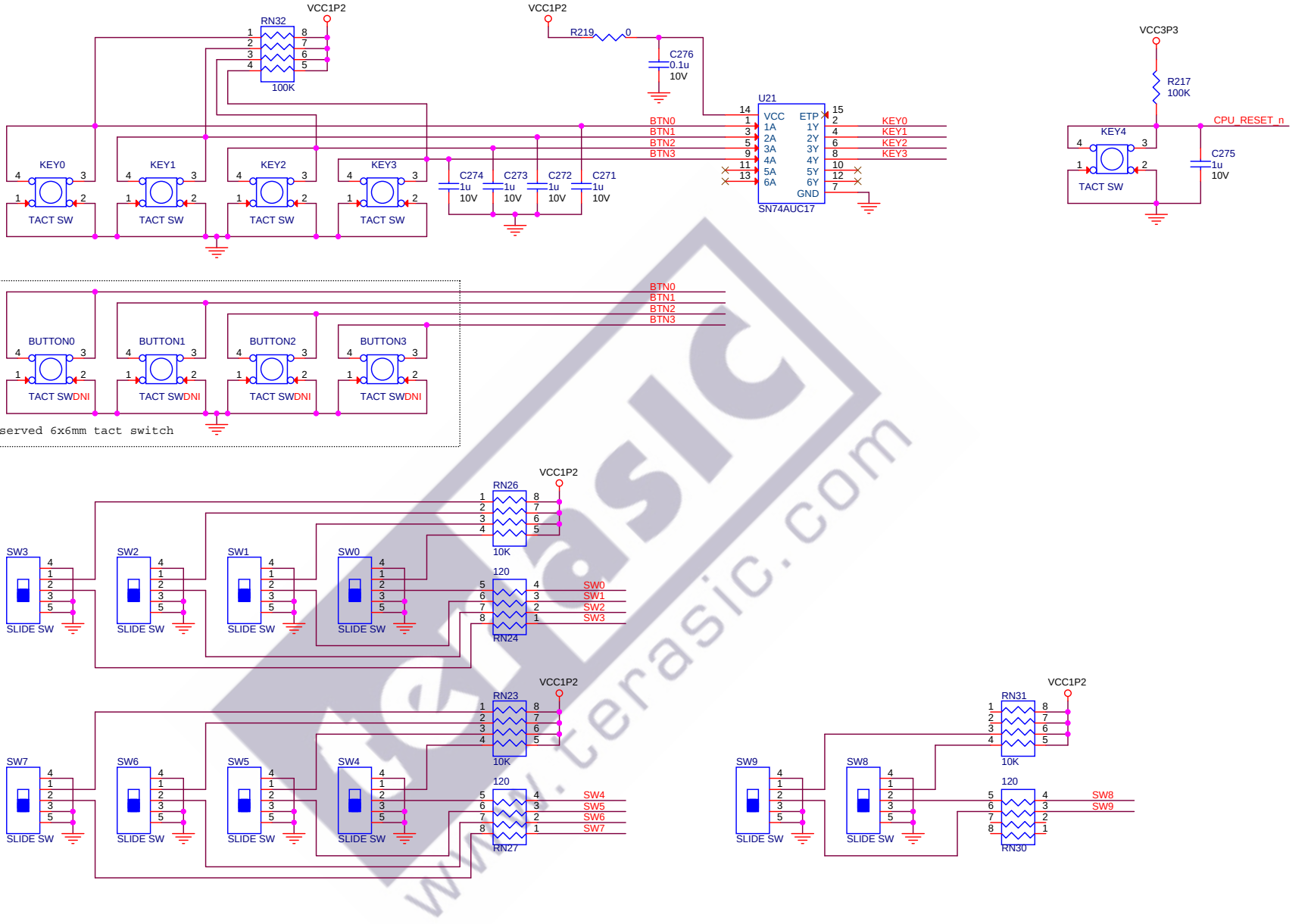
7 KEY[3..0]

CPU_RESET

8,17 CPU_RESET_n

SWITCH

3 SW[9..0]

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Title: **Cyclone V GX Starter Kit**

| Size | Document Number | Rev |
|---|---|---|
| B | Slide Switch and Tact switch | B |

Date: Friday, November 15, 2013 Sheet 18 of 23

## 7-Segment

3 HEX0_D[6..0]

3 HEX1_D[6..0]

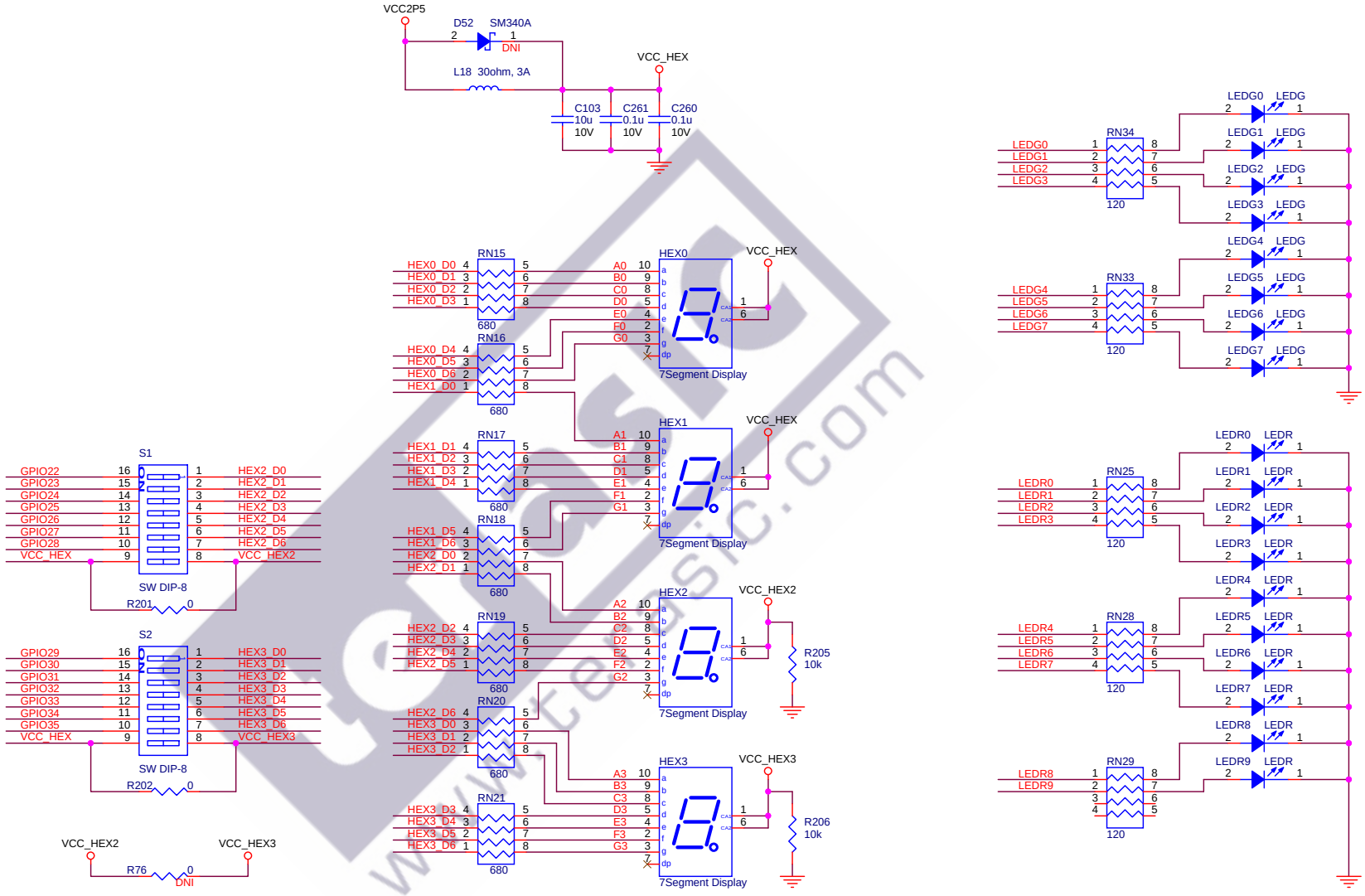
## 7-Segment (share GPIO[35..22])

4,8,17 GPIO[35..22]

## LED

5 LEDR[9..0]

5 LEDG[7..0]

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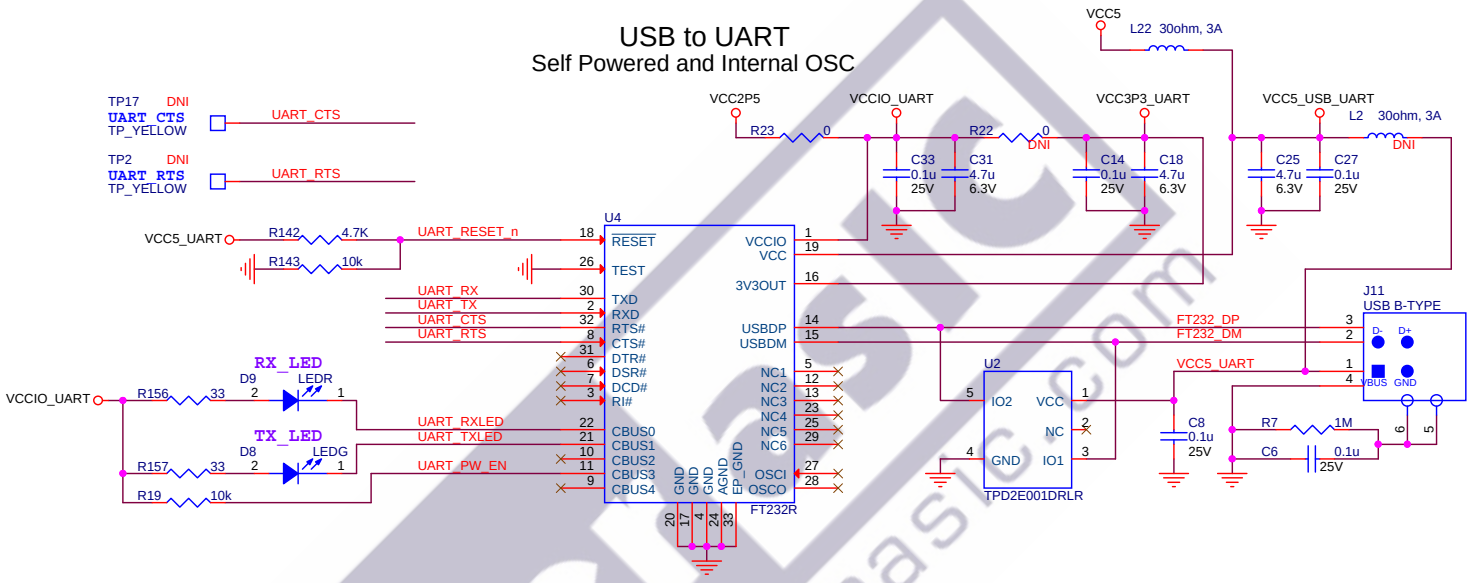
| | | |
|---|---|---|
| Title | Cyclone V GX Starter Kit | |
| Size B | Document Number 7-SEGMENTand LEDs | Rev B |
| Date: Friday, November 15, 2013 | Sheet 19 of 23 | |

UART

5 UART_RX

5 UART_TX

23 UART_RESET_n

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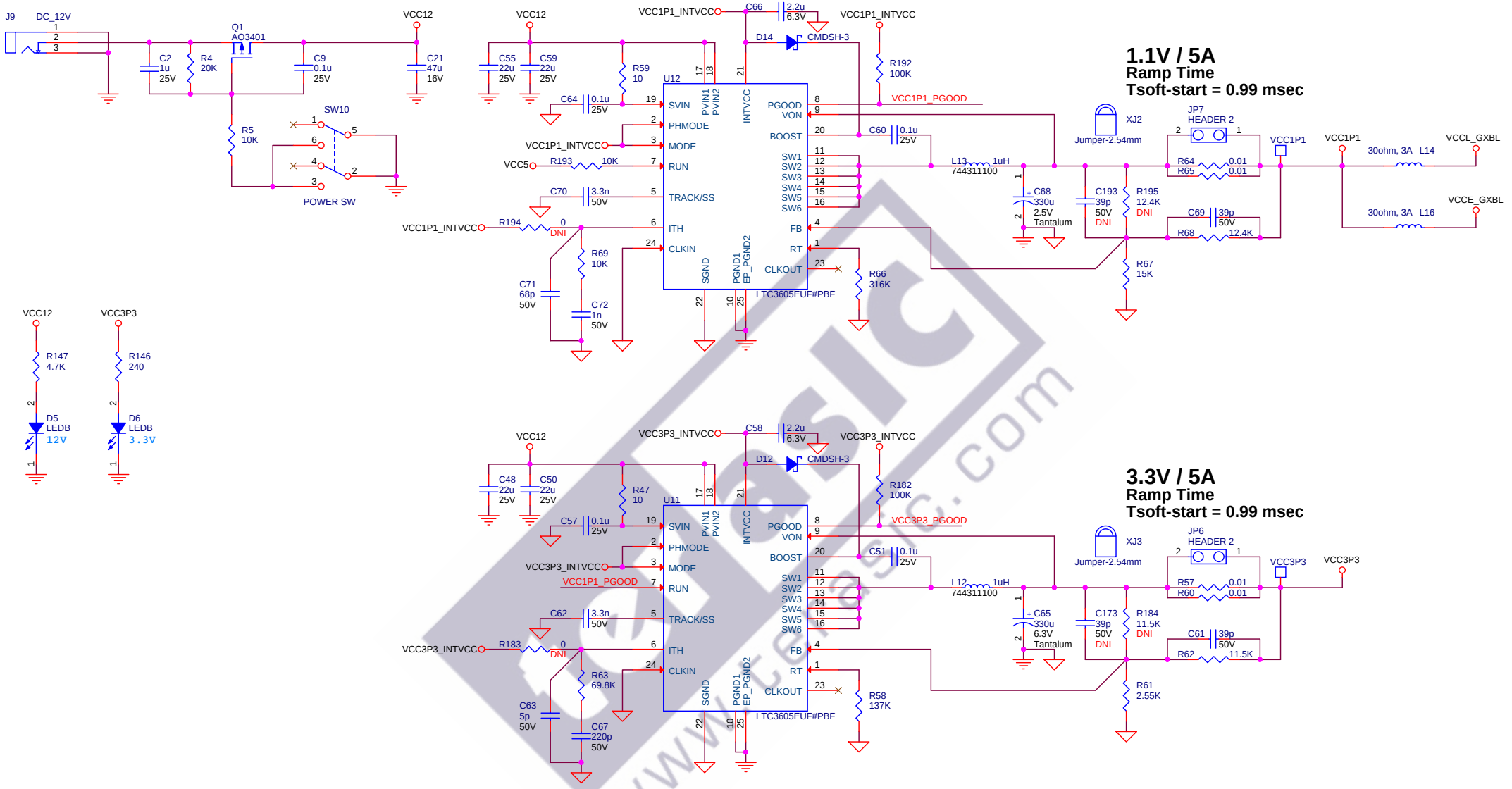
| | | |
|---|---|---|
| Title | Cyclone V GX Starter Kit | |
| Size B | Document Number UART to USB | Rev B |
| Date: Friday, November 15, 2013 | Sheet 20 of 23 | |

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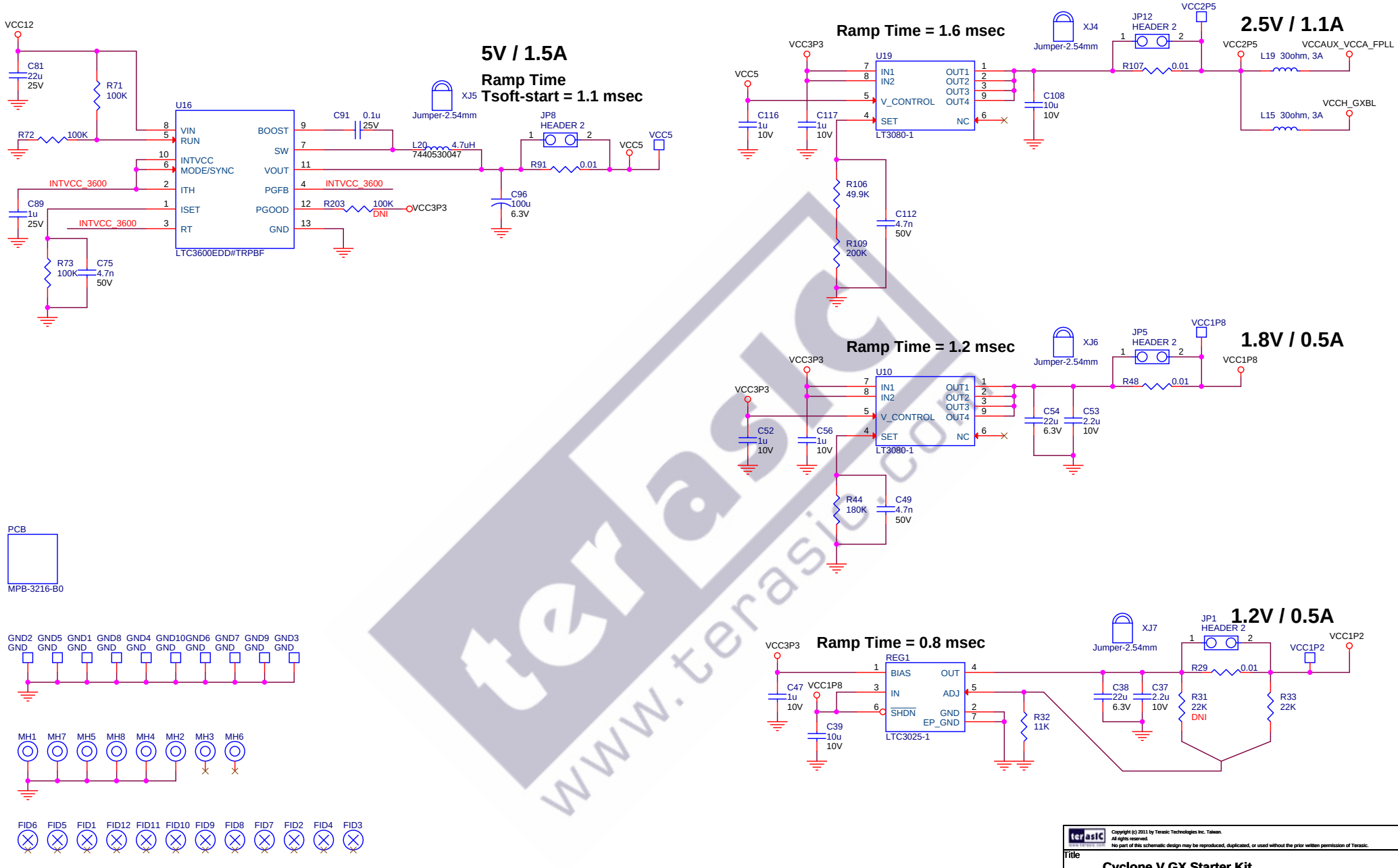
Title: **Cyclone V GX Starter Kit**

| Size | Document Number | Rev |
|---|---|---|
| B | Power - VCC1P1 & VCC3P3 | B |

Date: Friday, November 15, 2013 Sheet 21 of 23

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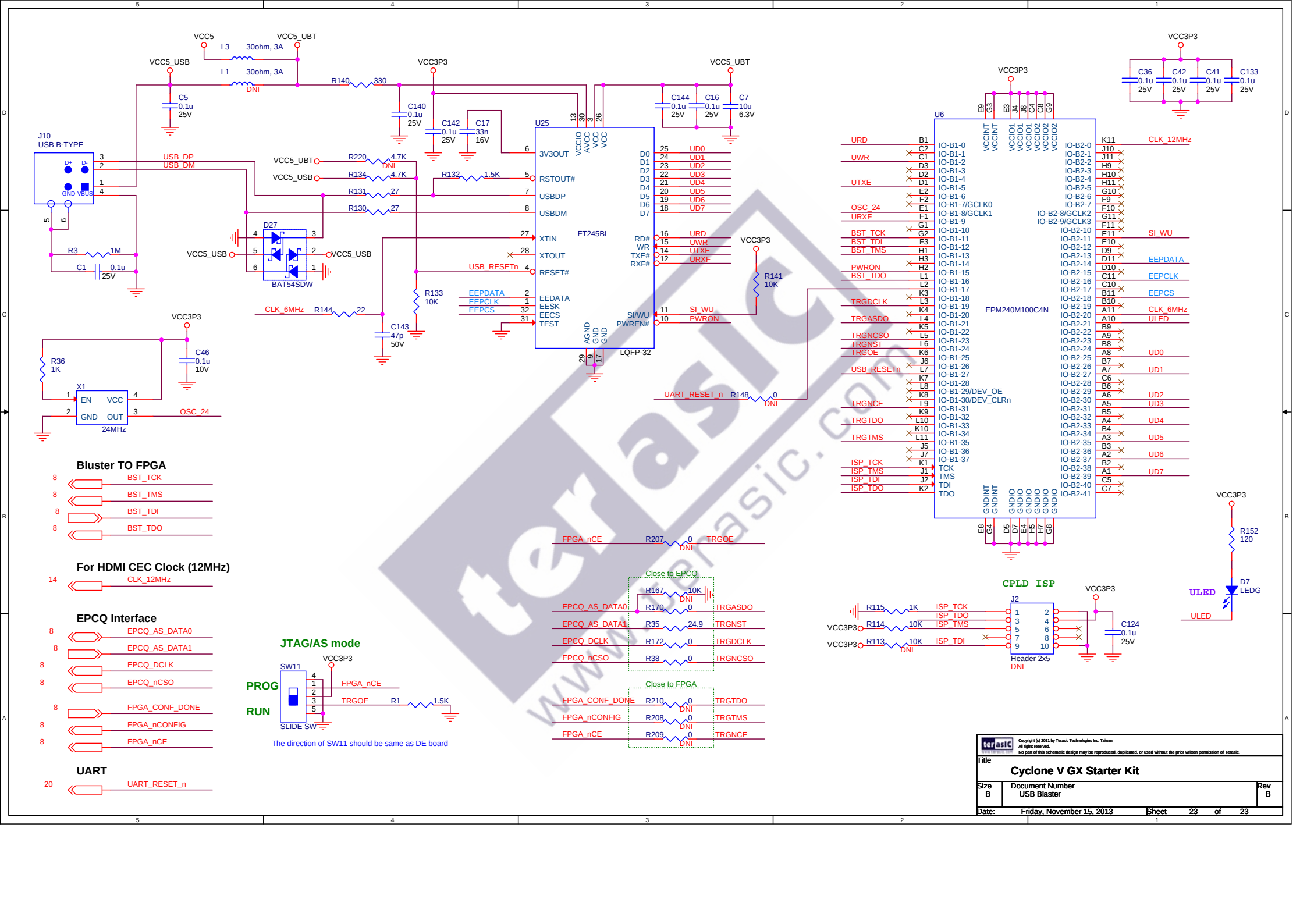
Title: **Cyclone V GX Starter Kit**

| Size | Document Number | Rev |
|---|---|---|
| B | Power - VCC5 & VCC1P2 & VCC1P8 & VCC2P5 | B |

Date: Wednesday, September 04, 2013 Sheet 22 of 23


VCC5
VCC5_UBT
L3 30ohm, 3A
L1 30ohm, 3A
VCC5_USB
VCC3P3
R140 330
DNI
C5 0.1u 25V
C140 0.1u 25V
C142 0.1u 25V
C17 33n 16V
C144 0.1u 25V
C16 0.1u 25V
C7 10u 6.3V
J10
USB B-TYPE
D+
D-
GND
VBUS
USB_DP
USB_DM
R3 1M
C1 0.1u 25V
R220 4.7K
DNI
R134 4.7K
R131 27
R130 27
R132 1.5K
D27
BAT54SDW
U25
3V3OUT
RSTOUT#
USBDP
USBDM
XTIN
XTOUT
RESET#
EEDATA
EESK
EECS
TEST
FT245BL
LQFP-32
D0
D1
D2
D3
D4
D5
D6
D7
UD0
UD1
UD2
UD3
UD4
UD5
UD6
UD7
RD#
WR
TXE#
RXF#
URD
UWR
UTXE
URXF
SI/WU
PWREN#
SI_WU
PWRON
USB_RESETn
EEPDATA
EEPCLK
EEPCS
CLK_6MHz
R144 22
C143 47p 50V
R133 10K
R141 10K
UART_RESET_n
R148 0
DNI
R36 1K
C46 0.1u 10V
X1
EN
VCC
GND
OUT
24MHz
OSC_24
U6
EPM240M100C4N
IO-B1-0
IO-B1-1
IO-B1-2
IO-B1-3
IO-B1-4
IO-B1-5
IO-B1-6
IO-B1-7/GCLK0
IO-B1-8/GCLK1
IO-B1-9
IO-B1-10
IO-B1-11
IO-B1-12
IO-B1-13
IO-B1-14
IO-B1-15
IO-B1-16
IO-B1-17
IO-B1-18
IO-B1-19
IO-B1-20
IO-B1-21
IO-B1-22
IO-B1-23
IO-B1-24
IO-B1-25
IO-B1-26
IO-B1-27
IO-B1-28
IO-B1-29/DEV_OE
IO-B1-30/DEV_CLRn
IO-B1-31
IO-B1-32
IO-B1-33
IO-B1-34
IO-B1-35
IO-B1-36
IO-B1-37
TCK
TMS
TDI
TDO
IO-B2-0
IO-B2-1
IO-B2-2
IO-B2-3
IO-B2-4
IO-B2-5
IO-B2-6
IO-B2-7
IO-B2-8/GCLK2
IO-B2-9/GCLK3
IO-B2-10
IO-B2-11
IO-B2-12
IO-B2-13
IO-B2-14
IO-B2-15
IO-B2-16
IO-B2-17
IO-B2-18
IO-B2-19
IO-B2-20
IO-B2-21
IO-B2-22
IO-B2-23
IO-B2-24
IO-B2-25
IO-B2-26
IO-B2-27
IO-B2-28
IO-B2-29
IO-B2-30
IO-B2-31
IO-B2-32
IO-B2-33
IO-B2-34
IO-B2-35
IO-B2-36
IO-B2-37
IO-B2-38
IO-B2-39
IO-B2-40
IO-B2-41
CLK_12MHz
SI_WU
EEPDATA
EEPCLK
EEPCS
CLK_6MHz
ULED
UD0
UD1
UD2
UD3
UD4
UD5
UD6
UD7
C36 0.1u 25V
C42 0.1u 25V
C41 0.1u 25V
C133 0.1u 25V
Bluster TO FPGA
BST_TCK
BST_TMS
BST_TDI
BST_TDO
For HDMI CEC Clock (12MHz)
CLK_12MHz
EPCQ Interface
EPCQ_AS_DATA0
EPCQ_AS_DATA1
EPCQ_DCLK
EPCQ_nCSO
FPGA_CONF_DONE
FPGA_nCONFIG
FPGA_nCE
UART
UART_RESET_n
JTAG/AS mode
SW11
PROG
RUN
SLIDE SW
FPGA_nCE
TRGOE
R1 1.5K
The direction of SW11 should be same as DE board
Close to EPCQ
R167 10K DNI
EPCQ_AS_DATA0
R170 0
TRGASDO
EPCQ_AS_DATA1
R35 24.9
TRGNST
EPCQ_DCLK
R172 0
TRGDCLK
EPCQ_nCSO
R38 0
TRGNCSO
Close to FPGA
FPGA_CONF_DONE
R210 0 DNI
TRGTDO
FPGA_nCONFIG
R208 0 DNI
TRGTMS
FPGA_nCE
R209 0 DNI
TRGNCE
FPGA_nCE
R207 0 DNI
TRGOE
CPLD ISP
J2
Header 2x5
DNI
R115 1K
R114 10K
R113 10K DNI
ISP_TCK
ISP_TDO
ISP_TMS
ISP_TDI
C124 0.1u 25V
R152 120
D7
LEDG
ULED
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Title
Cyclone V GX Starter Kit
Size B
Document Number
USB Blaster
Rev B
Date: Friday, November 15, 2013
Sheet 23 of 23