Device Specification Summary for Si5338C-B02268-GM

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I^{2}C-PROGRAMMABLE ANY-FREQUENCY, ANY-OUTPUT QUAD CLOCK GENERATOR

Input Type: CLKIN = Crystal, FDBK = OFF
Input Frequency: 25.000000000 MHz

Output Clock Configuration:
CLK0A/B: 156.250000000 MHz, 2.5V LVDS.
CLK1A/B: 125.000000000 MHz, 2.5V LVDS.
CLK2A/B: 125.000000000 MHz, 2.5V LVDS.
CLK3A/B: 50.000000000 MHz, 2.5V CMOS on A and B.

Output Enable Control

Enabled	Clock	Disable State
Enabled	CLK0A/B	StopLow
Enabled	CLK1A/B	StopLow
Enabled	CLK2A/B	StopLow
Enabled	CLK3A/B	StopLow

Default I2C address:
0x70 3.3V/2.5V

Spread Spectrum Profile:
Disabled

Frequency & Phase Adjust Configuration:

Clock	Initial Phase Offset (ns)	PINC Step Size (ns)
CLK0A/B	0.00	0.00
CLK1A/B	0.00	0.00
CLK2A/B	0.00	0.00
CLK3A/B	0.00	0.00

Device Pinout

Pin #	Description
1	CLKIN / XA
2	CLKINB / XB
3	CLKIN
4	I2C_LSB
5	FDBK
6	FDBKB
7	VDD
8	INTR
9	CLK3B
10	CLK3A
11	VDDO3
12	SCL
13	CLK2B
14	CLK2A
15	VDDO2
16	VDDO1
17	CLK1B
18	CLK1A
19	SDA
20	VDDO0
21	CLK0B
22	CLK0A
23	GND
24	VDD
PAD	PAD. Must be grounded for proper device operation.

This datasheet addendum is provided as supplemental information to the Si5338 datasheet available from www.silabs.com/timing.