SmartSens

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SC1035 Design and Application

V1.5

2014.11.05

table of Contents

Version History

version	And a description of the content	Owner / date
1.0	initial version.	Bill,20140829
1.1	1Update the table2-2The register $ 3416The instructions. its RNCValue {0x3415 [6: 4],0x3416}. 2Update the table2-2in0x3301,0x3304and0x3631Three registers Configuration. 3Update the table 2-3And Table 2-4inTIMING_VOFFSand TIMING_HOFFSTwo registers. 4Delete the table2-3And Table2-4All address bits0x50The beginning of the register, Register comprising WINDOW_MAN_EN,AVG_X_START, AVG_Y_START, AVG_X_WIDTH, AVG_Y_HEIGHT. 5Deleted table2-2The pair{3212,3213}Configuration. 6Deleted table 2-2The pair{3206,3207}Configuration, and added to the table 2-3 And Table2-4in. 7Update 2.3sectionPLLinstruction of. 8In Table 2-3And Table2-4Added 1280X960 @ 25fpsas well as 1280X960 @ 30fpsRegister configuration.	Bill,20140922
1.2	1,Update table2-5inPLLConfiguration register descriptions. 2, In Table2-3And Table2-4The increased output in each configuration pixel clock conditions frequency. 3,table2-2in$ 3631Configuration values from the register $ 3634To $ 3637. 4,in2.4Section increase BLCandRNC targetDescription With values. 5In Table2-6Added RNCTarget description.	Bill,20140927
1.3	1Update the table3-2The pairAECinstruction of. 2, Updated Figure 3-1The clerical error, the file"To" final. "	Bill,20140929

	3Modifying the 1-3IC in the note, the "± 0.1mm"The bias is changed to" ± 0.05mm. "	
1.4	1In Table2-2, The$ 3304Settings from $ 56To$ A0. 2In Table2-2Added {3907,3908}Register configuration.	Bill,20141009
1.5	1, In Table2-2Added 3e0fRegister configuration. 2,Change Table 2-3And Table 2-4inTIMING_HOFFSversus TIMING_VOFFSConfiguration (only for 1280x960Output).	Bill,20141105

1 Product Package basic information

SC1035Provide size 11.43mmX11.43mmofPLCC48Package.

1.1 Product Information Pin

table1-1Listed SC1035Signal description and the corresponding pin number.

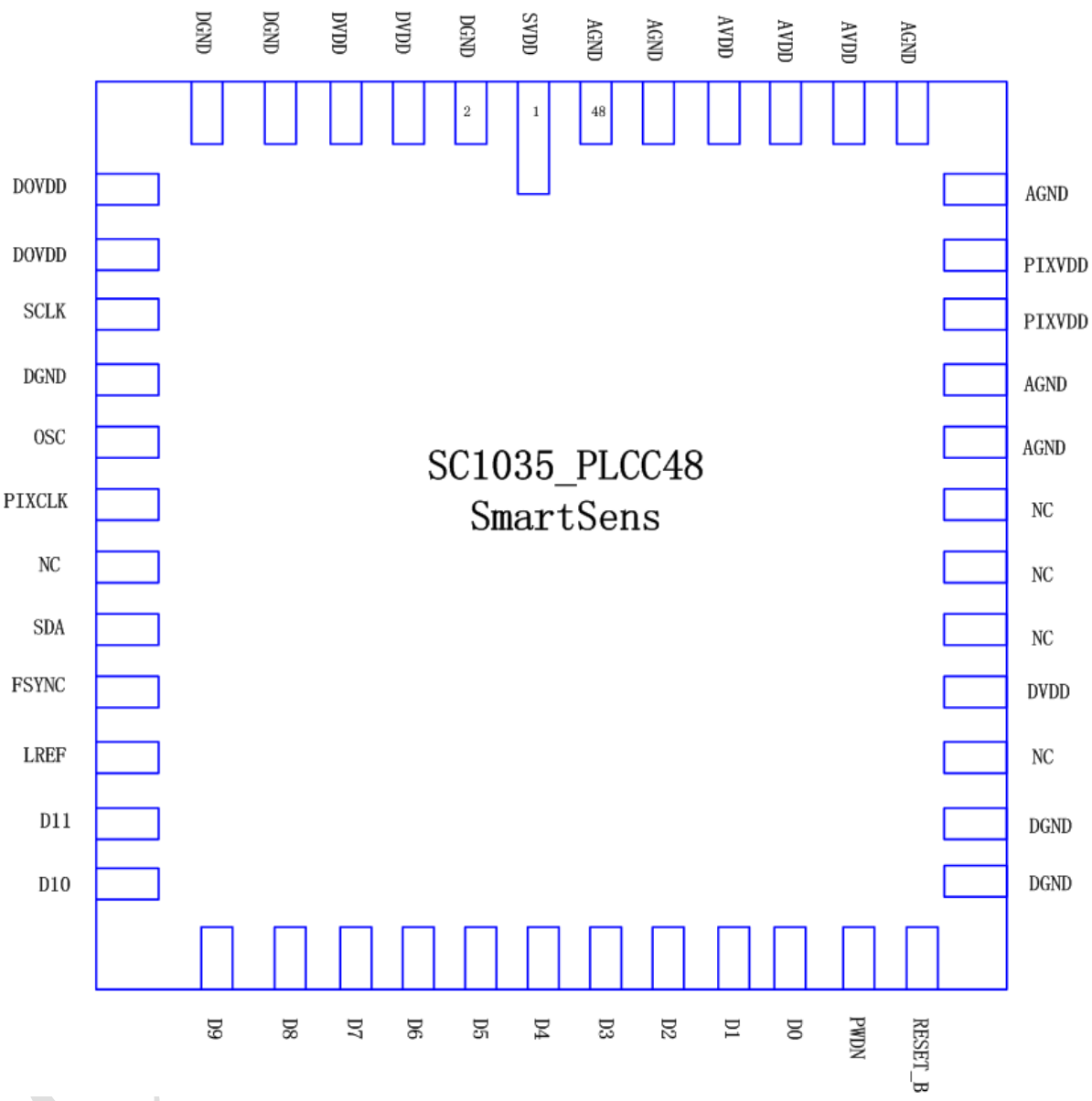
table1-1 Signal Description

Numbering	Signal names	Pin Type	description
1	SVDD	power supply	3.3VPixel signal acquisition module power supply
2	DGND	Ground	Digitally
3	DVDD	power supply	1.5VDigital Power
4	DVDD	power supply	1.5VDigital Power
5	DGND	Ground	Digitally
6	DGND	Ground	Digitally
7	DOVDD	power supply	1.8V / 3.3V IOpower supply
8	DOVDD	power supply	1.8V / 3.3V IOpower supply
9	SCL	enter	I2CInterface input clock line
10	DGND	Ground	Digitally
11	OSC	enter	System clock input
12	PIXCLK	Export	Pixel clock output
13	NC	N / A	not connected
14	SDA	I / O	I2CInterface cable (open drain)
15	FSYNC	I / O	Frame synchronization signal
16	LREF	I / O	Line synchronization signal
17	D11	Export	Parallel pixel data output [11]
18	D10	Export	Parallel pixel data output [10]
19	D9	Export	Parallel pixel data output [9]
20	D8	Export	Parallel pixel data output [8]
twenty one	D7	Export	Parallel pixel data output [7]

twenty two	D6	Export	Parallel pixel data output [6]
twenty three	D5	Export	Parallel pixel data output [5]
twenty four	D4	Export	Parallel pixel data output [4]
25	D3	Export	Parallel pixel data output [3]
26	D2	Export	Parallel pixel data output [2]
27	D1	Export	Parallel pixel data output [1]
28	D0	Export	Parallel pixel data output [0]
29	PWDN	enter	Power down signal input (built-in pull-down Resistance, high potential and effective)
30	RESET_B	enter	Reset input (built-in pull-up resistor, low Effective potential)
31	DGND	Ground	Digitally
32	DGND	Ground	Digitally
33	NC	N / A	not connected
34	DVDD	power supply	1.5VDigital Power
35	NC	N / A	not connected
36	NC	N / A	not connected
37	NC	N / A	not connected
38	AGND	Ground	Analog ground
39	AGND	Ground	Analog ground
40	PIXVDD	power supply	3.3VPixel power
41	PIXVDD	power supply	3.3VPixel power
42	AGND	Ground	Analog ground
43	AGND	Ground	Analog ground
44	AVDD	power supply	3.3VAnalog supply
45	AVDD	power supply	3.3VAnalog supply
46	AVDD	power supply	3.3VAnalog supply
47	AGND	Ground	Analog ground
48	AGND	Ground	Analog ground

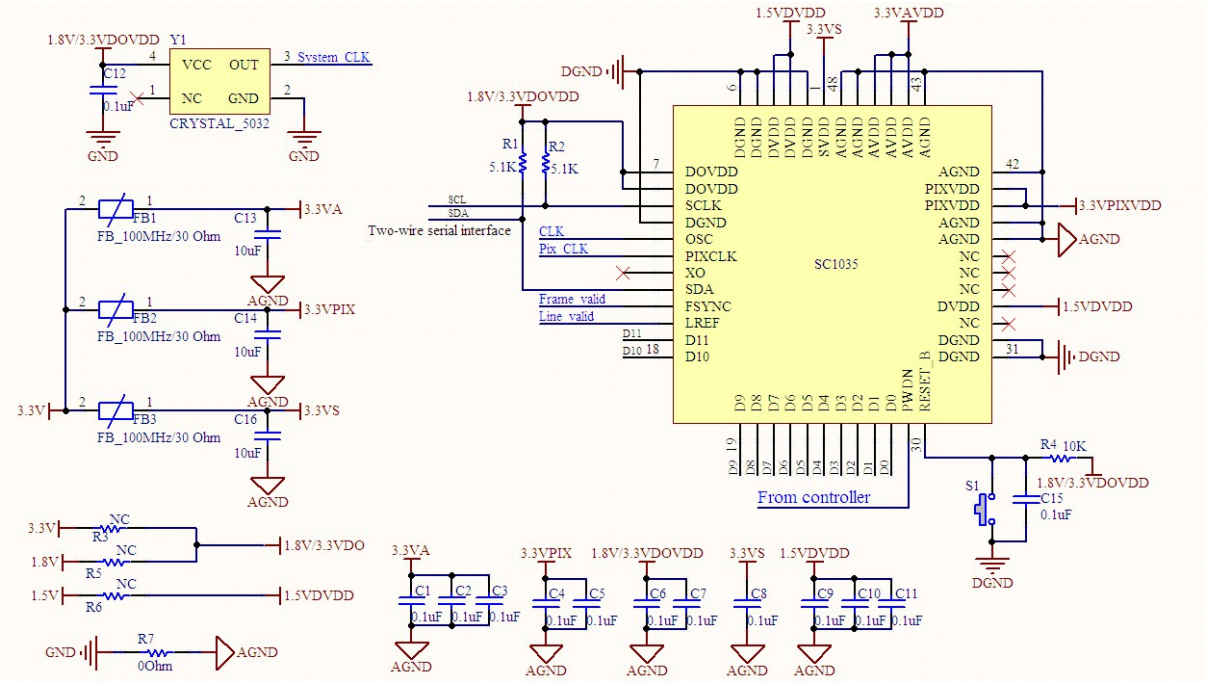
1.2 Product feet Bitmap

Top View



Map1-1 Pin Figure

1.3 Typical application circuit products



注释：1, Sysclk 可以采用有源晶振提供给OSC端口，也可以采用无源晶振双端接到OSC和XO两个管脚，晶振频率（6-27MHz）。

2, 3.3V,1.8V,1.5V,电压由外部LDO提供。参考型号AMS1117_3.3/1.8/1.5。

3, DVDD可以采用外部LDO提供，也可以采用内部供电。

4, DOVDD可以接1.8或者3.3V。

Map1-2 typical application

Note:SC1035 Chip sub Rd power: DOVDD = 1.8V ~ 3.3V,AVDD = 3.3V,SVDD = 3.3V, PIXVDD = 3.3V,DVDD = 1.5V(Default will be used internally LDOprovide1.5Vpower supply).

1.4 Notes module layout design

1.4.1 When designing modular power solutions Considerations

To obtain better image quality, SVDD,AVDD,PIXVDDYou must use isolated 3.3VPower supply.

DVDD It is the chip Core Voltage, which may be DVDDpin Directly 1.5VTo be through byDOVDD pin Input power, through the internal LDO produce1.5V Voltage (configure register).

1.4.2 Peripheral Application Notes

1. Design of the power module, should be placed as close to the chip input pin, the power line alignment The minimum width should be 0.1mm, Supply chip AVDD,SVDD,PIXVDDPower line As short as possible; and each power supply chip close to the pin, respectively, 0.1uF Filter Wave capacitance.

2. Design of the ground, the two routes AGND and DGND to take apart; linewidth reference ground
   At a minimum 0.1mm-0.15mm Between, under conditions that allow the wiring conditions should be widened

3. Each capacitor as close to the pins. And the
   alignment should be noted that after the first and
   then into the filter capacitor sensor; Filter
   capacitor is recommended omitted may affect the
   image quality;

4. When the power traces, regardless of the kind of power supply DVDD, AVDD and PIXVDD proposed to
   Separate alignment;

5. OSC, PIXCLK, FSYNC, LREF Preferably between ground shield trace or away;

6. SCL, SDA Traces should try to stay away from OSC, PIXCLK, D0, D1 (Low-frequency data
   pin), Land line or shield;

7. RESET_B (Reset), PWDN, AVDD Traces should also try to stay away from OSC, PIXCLK,
   D0-D7;

8. I2C Must be added when traces 5.1K (5.1K Recommended Value) Take pull-up resistor.

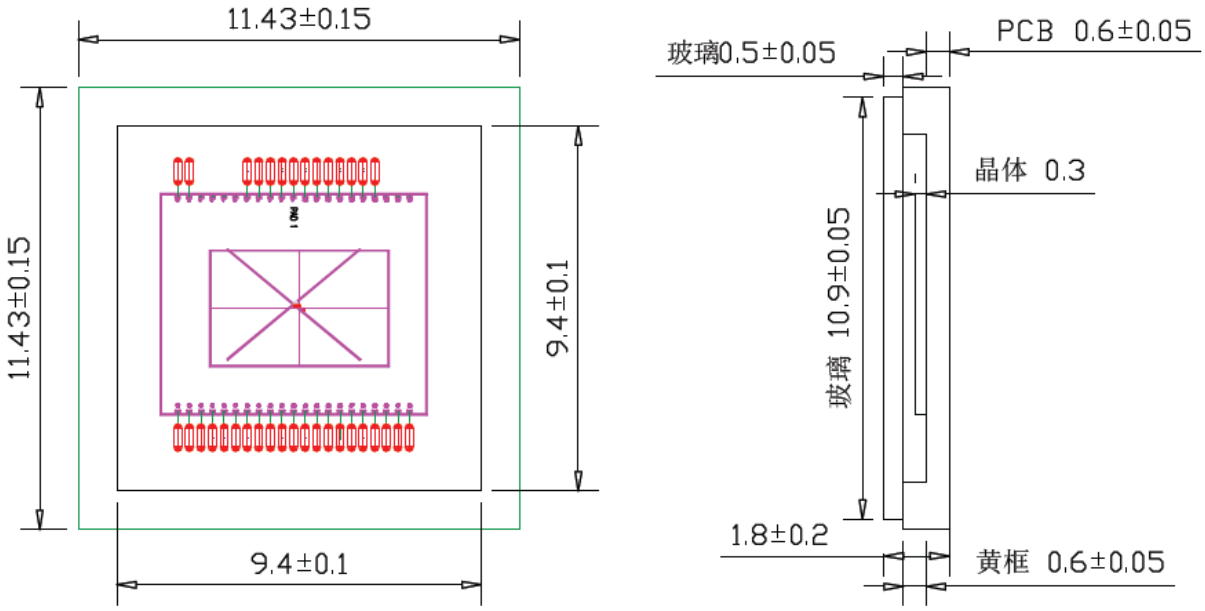
9. Chip NC Pin wiring is not connected directly to vacant;

10. Chip active crystal can be used directly by the OSC Input clock signal, but also by Chip directly
    CLOCK Signal as an input. If you want to use passive crystal scheme, and Separate contact.

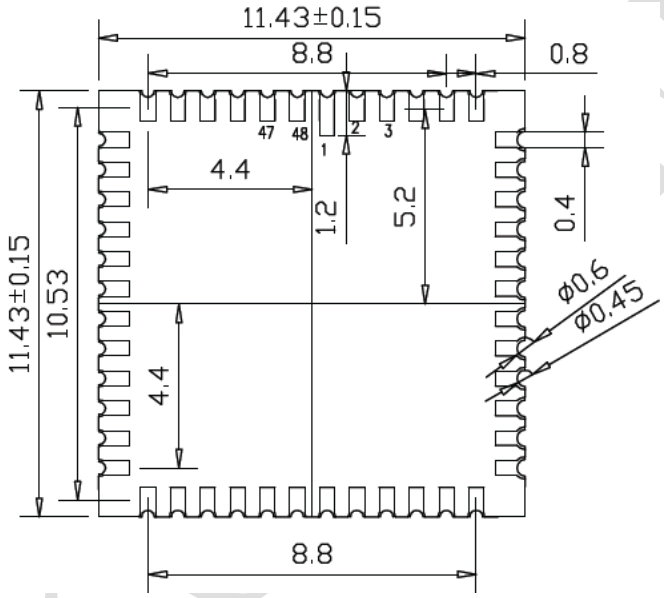
1.5 Package Dimensions Figure

SC1035 provide PLCC48 Package, package specific dimensions are as follows:

TOP VIEW SIDE VIEW



BOTTOM VIEW

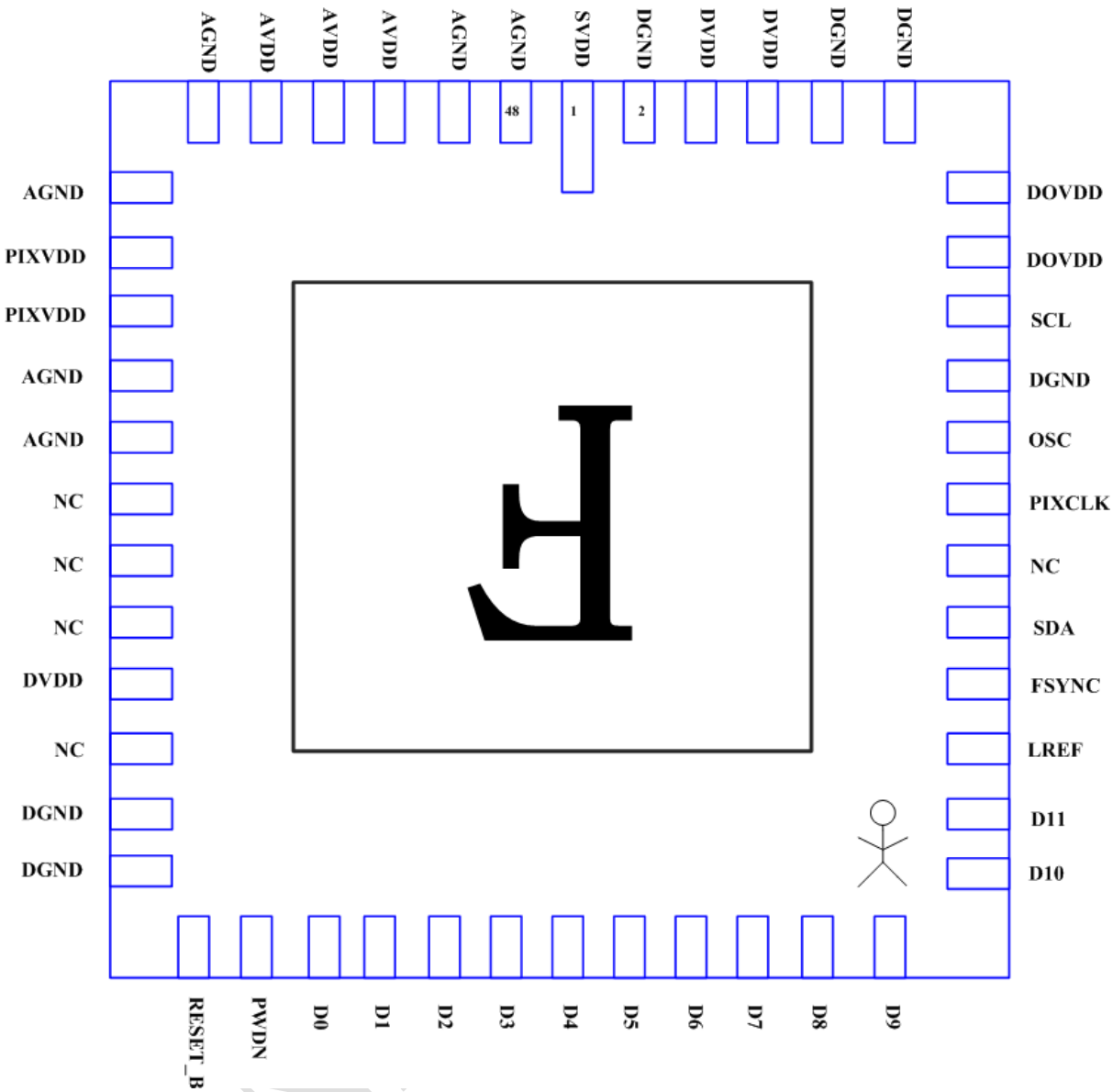


Map1-3 PLCC44Package Diagram (Unit: mm)

Note: The center of the photosensitive array package coincides with the range of allowable error.0.05mm

1.6 The imaging direction

The figure is a schematic view of the imaging direction.



Map1-4 A schematic view of the imaging direction (Bottom view)

2 Basic configuration register

Sc1035Register address 16bitRegister data bit width is 8bit.

2.1 Device Address

Sc1035Device address 7'h30,Save as 0x3008 [7:1]in.0x3008 [0]Read-write control bit. in Read operation,0x3008 [7:0] = 8'h61In the writing operation,0x3008 [7:0] = 8'h60.

table2-1 Address register

address	Register name	Defaults	read/write	description
0x3008	I2C SLAVE ID	8'h60	RW	Bit [7: 1]: I2C slave id

After the chip is properly powered, RESETComplete, you can pairRead and write operations.

2.2 The basic configuration of normal working hours

Need to pay attention to several issues:

1,$ 5000YesISPThe function control register, if you need to use anISPWemaed to close the corresponding interna Control bit.

2,$ 3416forRNC targetValue setting register, you can be adjusted as needed.

table2-2 Initialize the basic configuration

Register Name	Configuration	Special Note
$ 3000	$ 01	soft reset
$ 3003	$ 01	
$ 3400	$ 53	bit [0] rnc_en, 1 enable, 0 disable.

$ 3416	$ C0	RNC TARGET Chip data output 12bit Time, target Value is the {0x3415 [6: 4], 0x3416} These two register values; e.g. If only take high bits as data output, target value for {0x3415 [6: 4], 0x3416} These two register values Divided 4; If you just take the low 8 bits as data output, target Value {0x3415 [6: 4], 0x3416} Both send Register value divided by 16.
$ 3d08	$ 00	
$ 5000	$ 09	isp_ctrl: [0] awb_en, 1 enable, 0 disable. [3] awb_gain_en, 1 enable, 0 disable. (If needed awb Function, you need bit [3] and bit [1] Simultaneously enable) [7] lens_en, 1 enable, 0 disable.
$ 3e03	$ 00	open aec / agc bit <1: 0>
$ 3928	$ 00	
$ 3622	$ 2e	
$ 3630	$ 58	
$ 3612	$ 00	
$ 3632	$ 41	
$ 3635	$ 04	
$ 3500	$ 10	
$ 3631	$ 80	
$ 3620	$ 44	
$ 3633	$ 7c	
$ 3780	$ 0b	
$ 3300	$ 33	
$ 3301	$ 61	
$ 3302	$ 30	

$ 3303	$ 56
$ 3304	$ A0
$ 3305	$ 72
$ 331e	$ 56
{$ 321e, $ 321f}	$ 000a
$ 3216	$ 0a
$ 3115	$ 0a
$ 3332	$ 38
$ 5054	$ 82
{$ 3907,$ 3908}	$ 01c0
$ 3e0f	$ 14

Below are two tables smartsensThree common configuration register setting mode offers under.If you need it Configured his mode, and **smartsens** contact.-

table2-3 24MHzCrystal register configuration

Register Name	720p @ 25fps	720p @ 30fps	1280x960 @ 25fps	1280x960 @ 30fps	1280x960 @ 45fps
Output pixel clock frequency	36MHz	48MHz	45MHz	54MHz	81MHz
PLL_CTRL {0x3010,0x 3011}	$ 3146	$ 3146	$ 0916	$ 08e6	$ 1856
SC_REG04 0x 3004	$ 04	$ 03	$ 04	$ 04	$ 02
TIMING_HTS {0x 320c, 0x 320d}	$ 0708	$ 07d0	$ 0708	$ 0708	$ 0708
TIMING_VTS {0x 320e, 0x 320f}	$ 0320	$ 0320	$ 03e8	$ 03e8	$ 03e8
TIMING_HOFFS {0x3210,0x3211}	$ 0062	$ 0062	$ 0062	$ 0062	$ 0062

TIMING_VOFFS {0x3212,0x3213}	$ 000a	$ 000a	$ 0008	$ 0008	$ 0008
TIMING_X_OUTPUT_SIZE {0x 3208,0x 3209}	$ 0500	$ 0500	$ 0500	$ 0500	$ 0500
TIMING_Y_OUTPUT_SIZE {0x 320a, 0x 320b}	$ 02d0	$ 02d0	$ 03c0	$ 03c0	$ 03c0
TIMING_Y_START_ADDR {0x 3202,0x 3203}	$ 0078	$ 0078	$ 0008	$ 0008	$ 0008
TIMING_Y_END_ADDR {0x 3206,0x 3207}	$ 0367	$ 0367	$ 03cf	$ 03cf	$ 03cf

table2-4 27MHzCrystal register configuration

Register Name	720p @ 25fps	720p @ 30fps	1280x960 @ 25fps	1280x960 @ 30fps	1280x960 @ 45fps
Output pixel clock frequency	36MHz	48MHz	45MHz	54MHz	81MHz
PLL_CTRL {0x3010,0x 3011}	$ 2186	$ 2186	$ 0766	$ 0746	$ 11a6
SC_REG04 0x 3004	$ 04	$ 03	$ 04	$ 04	$ 02
TIMING_HTS {0x 320c, 0x 320d}	$ 0708	$ 07d0	$ 0708	$ 0708	$ 0708
TIMING_VTS {0x 320e, 0x 320f}	$ 0320	$ 0320	$ 03e8	$ 03e8	$ 03e8
TIMING_HOFFS {0x3210,0x3211}	$ 0062	$ 0062	$ 0062	$ 0062	$ 0062
TIMING_VOFFS {0x3212,0x3213}	$ 000a	$ 000a	$ 0008	$ 0008	$ 0008
TIMING_X_OUTPUT_SIZE {0x 3208,0x 3209}	$ 0500	$ 0500	$ 0500	$ 0500	$ 0500

TIMING_Y_OUTPUT_SIZE {0x 320a, 0x 320b}	$ 02d0	$02d0	$ 03c0	$03c0	$03c0
TIMING_Y_START_ADDR {0x 3202,0x 3203}}	$ 0078	$0078	$ 0008	$0008	$0008
TIMING_Y_END_ADDR {0x 3206,0x 3207}	$ 0367	$0367	$ 03cf	$03cf	$03cf

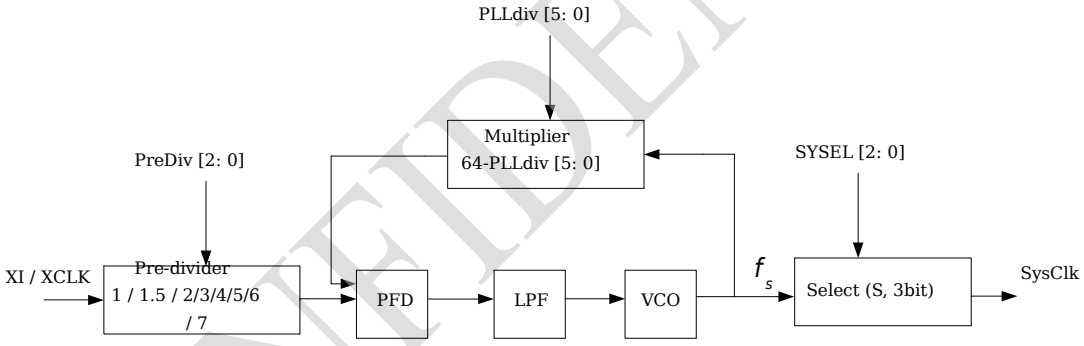
2.3 PLLConfiguration instructions

With the foregoing detailed configuration, PLL Make content only for

For details, interested customers can refer to.

SC1035 PLLAllows input clock frequency range 6 ~ 27MHz,among themVCOOutput frequency (f_s)of

Range of100MHzTo600MHz.PLLSchematics, and control registers in FIG. 2-1And Table2-5In the show.



Map2-1 PLLControl schematic

table2-5 PLLControl register

address	Register name	Defaults	read/write	description
0x3010		8'h20	RW	Bit [7]: BYPASS PLL Bit [6: 4]: SYSEL [2: 0] 000 ~ S = 0 001 ~ S = 1 010 ~ S = 2 ...... 111 ~ S = 7 Bit [3: 1]: PreDiv [2: 0] 000 ~ N = 1 001 ~ N = 1.5 010 ~ N = 2 011 ~ N = 3 ...... 111 ~ N = 7 Bit [0]: PLLDIV [5: 0]
0x3011		8'h86	RW	Bit [7: 3]: PLLDIV [4: 0] M = 64-PLLDIV [5: 0] Bit [2: 0]: Reserved

System clock frequency F_{sysclk} By type 2-1Calculated:

$$F_{sysclk} = F_{xclk} \times \frac{64 - M}{N \times (S + 1)} \quad (2\text{-}1)$$

Note: Arguments in a formula M, NandSIn FIG.2-1There are specific register instructions.

2.4 RNC BLC

The pixel array comprises a plurality of strips of black columns, to eliminate the line noise. This function is ca RNC. Pixel array comprises 64Article black reference columns that can provide data for the line noise cancellation algorithm. RNC Algorithm can refer to the black

□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□□

Are not the same. Taking into account the presence of color filters, you must use two channels to eliminate the line

Law) in a particular pixel to give a negative value, the result set 0.

Also includes an array of pixels black lines, black line which can compensate for the cancellation algorithm to pro

First subtract the black level data, BLC algorithm can estimate the black level compensation value from the black line dat

The value minus respective black level compensation value of the color channels. If some specific pixels, such redu

The negative, then the result set 0. By default, it will re-gain value after change BLC operating.

In the application process, **RNC** It is recommended to open (recommended configuration of the foregoing), the otherwise dark light bar

Member, the image quality is decreased, the dynamic RNC When the pause is turned on, the output image

The value {0x3415,0x3416} Two registers decision. Chip data output 12bit Time, target Value is the {0x3415,

0x3416} These two register values; if you just take the high 10bit as the target value {0x3415, 0x3416}

This value is divided by two registers, if you just take the high 8 bit target {0x3415, 0x3416}

16 .

Pixel array comprises 64 RNC Count

Method can estimate the noise travel from black reference column data. For the same line, the line noise is the sa

Noise row between rows different from each other. Taking into account the presence of color filters, you must use

If the cancellation algorithm (subtraction) to give a negative value in a particular pixel, then the result set 0.

when BLC versus RNC Open simultaneously (recommended), sensor Output data target by RNC target

($ 3415 [6: 4], $ 3416) Determined by BLC target value ($ 3907 [4: 0], $ 3908) Size, only decided to keep

Savings random row noise Space, if this space is too small will result in some cases (such as an analog open high

Gain) random noise It can not be completely saved in the final output image Not enough to eliminate completely. and so,

Suggest {$ 3907 [4: 0], $ 3908} set to $ 00c0 about.

If you need to shield RNC (Not recommended), open a BLC There the time RNC target invalid, sensor

Output target By value BLC target Decisions ($3907[4:0],$3908).

Its control registers are as follows:

2-6 RNC

Features		
RNC Enable	0x3400	Bit [0]: rnc_enable 0 ~ bypass blc 1~ RNC enable

□□	□□□□	□□
automaticRNC □□	0x3400	Bit [1]: rnc_auto_en 0 ~ manual mode 1 ~ auto mode
RNCChannel selection	0x3400	Bit [5]: one channel enable 0 ~ use 4 channel mode 1 ~ use 1 channel mode
RNC_manual00 □ B)	{0x3405 [4: 0], 0x3404}	RNC noise for B channel
RNC_manual01 □ GB □	{0x3407 [4: 0], 0x3406}	RNC noise for GB channel
RNC_manual10 □ GR □	{0x3409 [4: 0], 0x3408}	RNC noise for GR channel
RNC_manual11 □ R □	{0x340b [4: 0], 0x340a}	RNC noise for R channel
RNCTarget	{0x3415 [6: 4], 0x3416}	RNC TARGET Chip data output 12bit □□ target □□□ {0x3415 [6: 4], 0x3416}This Two register values; if you just take the high 10 □□□□□□□□□□ target □□ {0x3415[6:4], 0x3416}Both send Register value 4 □□□□□ by 8Place As a data output, target □□ {0x3415[6:4], 0x3416} □□□□ □□□□□ 16 □

□ 2-7 BLC □□□□□

□□	□□□□	□□
BLC □□	0x3900	Bit [0]: blc_enable 0~ bypass blc 1~ BLC enable

和和	和和和和	和和
BLC 和和和和	{0x3928 [0], 0x3905 [6]}	0x3928 [0]: 0 ~ use 8 channel offset mode 1 ~ use 4 channel offset mode 0x3905 [6]: one channel enable 0 ~ use 8 or 4 channel offset 1 ~ use one channel mode
BLC 和和和	{0x3907 [4: 0], 0x3908}	BLC target

3 AEC / AGCConfiguration instructions

AEC / AGC are based on the image brightness can be adjusted, AEC adjust exposure time, AGC Gain adjustme
, Final image brightness set to fall within the range of brightness threshold.

Sensor auto-exposure, auto-gain function, which aims to adapt to different lighting conditions, the output of F
Like normal display: to ensure that the picture is neither too exposed, it will not dim, as far as possible to suppress
ratio. Currently 0342 method used is this: the entire screen brightness averaging, the average set a threshold degr
Range when the output image screen when average within this range (via register control), that the image has bee
Otherwise, adjust the exposure time and gain, so that the output image brightness toward the threshold of the ran
When the value range is set to 400 ~ 600 (10bit data, corresponding to the 8bit data is divided by 4) between, thro
Exposure and gain, the average brightness of the final image will be at a value between 400 to 600.

In this process, sensor adjustment is not independent of the exposure time or gain. In order to achieve lower
Better signal to noise ratio, its regulatory principles: If the image is too dark, before the exposure time not yet reac
Benefits, until the exposure time until the limit is reached, if the case, the image is still dim, reach the set threshol
sensor began calling AGC. Need to be clearly pointed out that: Gain is on, it will lead directly to an average noise
Sound amplification exponentially; exposure time increased, help to improve the signal to noise ratio. Therefore, th
Exposure time priority, must be less than the gain is not open. Conversely, when the image is too bright, the priorit
Gain closes and the image is still too bright, will reduce the exposure time.

It is because of the automatic control of the AEC / AGC-control strategy, because the exposure time control pr
AEC can be used alone in a closed AGC, AGC can not be used alone but when closed AEC. For example: Close AEC
Open only when AGC, sensor regulation policy has not changed, still will first detect whether the exposure time ha
If at this time manually AEC, but has not reached a tune exposure limit exposure value, sensor will give priority to
Room, but this time the AEC has been ineffective, so there will be disorder automatic control, the screen will appe

Therefore, the exposure time and gain adjustment system is an interactive, when debugging, it should be take

□□□ AEC/AGC □□□□□□□□□□□□□□□□□□□□

□ 3-1 AGC □□□□□

items	DCG ($ 3E09 [7])	corse_gain ($ 3E09 [6: 4])	fine _gain ($ 3E09 [3: 0])		final_gain	gain_step	lsb_ste	p
			Register: 0	Gain: 1	1			
		Gain x1 □□□□□ 0	1	1.0588	1.0588	0.058830	.544012	
			2	1.1176	1.1176	0.058828	.937008	
			3	1.1765	1.1765	0.058827	.535062	
			4	1.2353	1.2353	0.058826	.179875	
			5	1.2941	1.2941	0.058824	.990341	
			6	1.3529	1.3529	0.058823	.904206	
			7	1.4118	1.4118	0.058822	.945885	
			8	1.4706	1.4706	0.058821	.991024	
			9	1.5294	1.5294	0.058821	.145547	
			a	1.5882	1.5882	0.058820	.362675	
			b	1.6471	1.6471	0.058819	.667901	
			c	1.7059	1.7059	0.058818	.957735	
			d	1.7647	1.7647	0.058818	.326061	
			e	1.8235	1.8235	0.058817	.735125	
			f	1.8824	1.8824	0.058917	.209414	
		Gain x2 Register: 1	0	1	2	0.1176	32.34	
			1	1.0588	2.1176	0.117630	.544012	
			2	1.1176	2.2352	0.117628	.937008	
			3	1.1765	2.353	0.117827	.535062	
			4	1.2353	2.4706	0.117626	.179875	
			5	1.2941	2.5882	0.117624	.990341	
			6	1.3529	2.7058	0.117623	.904206	
			7	1.4118	2.8236	0.117822	.945885	
			8	1.4706	2.9412	0.117621	.991024	
			9	1.5294	3.0588	0.117621	.145547	
			a	1.5882	3.1764	0.117620	.362675	
			b	1.6471	3.2942	0.117819	.667901	
			c	1.7059	3.4118	0.117618	.957735	
			d	1.7647	3.5294	0.117618	.326061	
			e	1.8235	3.647	0.117617	.735125	
	DCGX1 □□□□:0		f	1.8824	3.7648	0.117817	.209414	
		Gain x4 Register: 3	0	1	4	.2352	32.34	
			1	1.0588	4.2352	0.235230	.544012	
			2	1.1176	4.4704	0.235228	.937008	
			3	1.1765	4.706	0.235627	.535062	
			4	1.2353	4.9412	0.235226	.179875	
			5	1.2941	5.1764	0.235224	.990341	
			6	1.3529	5.4116	0.235223	.904206	
			7	1.4118	5.6472	0.235622	.945885	
			8	1.4706	5.8824	0.235221	.991024	
			9	1.5294	6.1176	0.235221	.145547	
			a	1.5882	6.3528	0.235220	.362675	
			b	1.6471	6.5884	0.235619	.667901	
			c	1.7059	6.8236	0.235218	.957735	
			d	1.7647	7.0588	0.235218	.326061	
			e	1.8235	7.294	0.235217	.735125	
			f	1.8824	7.5296	0.235617	.209414	
		Gain x8 Register values: 7	0	1	8	0.4704	32.34	
			1	1.0588	8.4704	0.470430	.544012	
			2	1.1176	8.9408	0.470428	.937008	
			3	1.1765	9.412	0.471227	.535062	
			4	1.2353	9.8824	0.470426	.179875	
			5	1.2941	10.3528	0.470424	.990341	
			6	1.3529	10.8232	0.470423	.904206	
			7	1.4118	11.2944	0.471222	.945885	
			8	1.4706	11.7648	0.470421	.991024	
			9	1.5294	12.2352	0.470421	.145547	
			a	1.5882	12.7056	0.470420	.362675	
			b	1.6471	13.1768	0.471219	.667901	
			c	1.7059	13.6472	0.470418	.957735	
			d	1.7647	14.1176	0.470418	.326061	
			e	1.8235	14.588	0.470417	.735125	
			f	1.8824	15.0592	0.471217	.209414	
	DCGx1.6 □□□□1	□□ x8 □□□□□ 7	4	1.235315.811840.7526426.179875				
			5	1.294116.564480.7526424.990341				
			6	1.352917.317120.7526423.904206				
			7	1.411818.071040.7539222.945885				
			8	1.470618.823680.7526421.991024				
			9	1.529419.576320.7526421.145547				
			a	1.588220.328960.7526420.362675				
			b	1.647121.082880.7539219.667901				
			c	1.705921.835520.7526418.957735				
			d	1.764722.588160.7526418.326061				
			e	1.8235	23.34080.7526417.735125			
			f	1.882424.094720.7539217.209414				

Note: 1, wherein, fine gain is calculated as: (64-2 * (15-N)) / 34 = (34 + 2 * N) / 34,

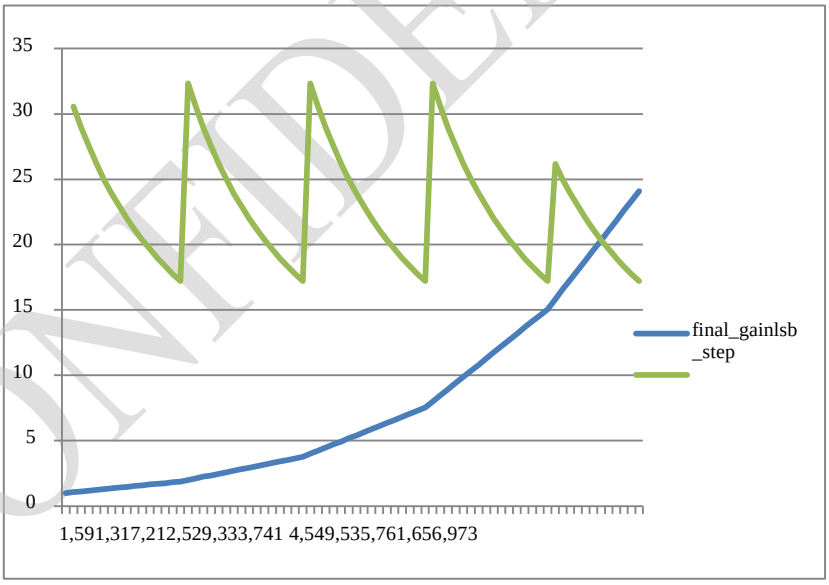
Where N is the register value, the maximum 15.

2, it is assumed to mean AEC to adjust the screen 550 (10bit).

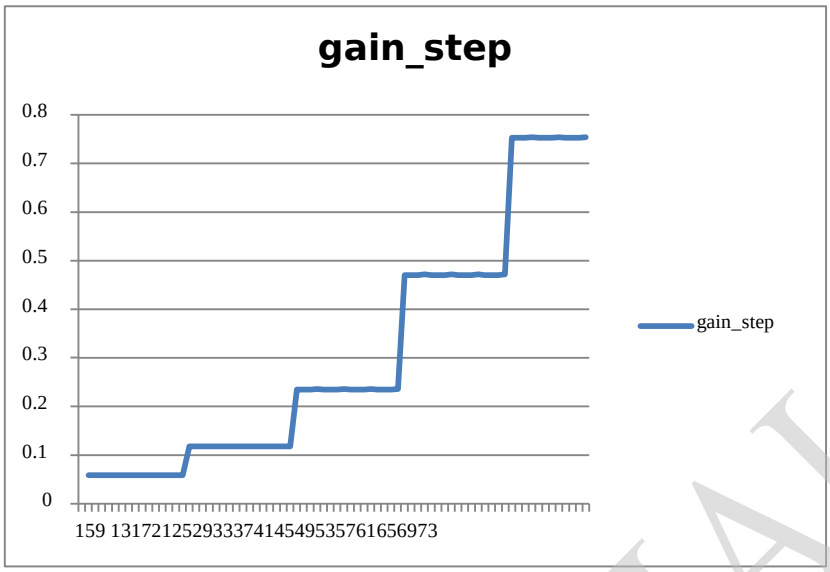
□ 3-2 AEC □□□□□

AEC	Line 1 minimum step	Line cycle time = X PIXCLK President	
	12bit controlled by the exposure time	8bit high as $ 3e01 of bit [7: 0] 4bit low as $ 3e02 of bit [7: 4]	Shall not exceed the maximum (a frame lengt -4 Degrees governor)
Auto AEC	Register 0x3e03	Bit [1]:AGC manual	0: auto enable 1: manual enable
	bit [1: 0]	Bit [0]:AEC manual	0:auto enable 1:manual enable

The following picture shows the two final gain and gain step change in the conditions of the various configura



□ 3-1 Final gainChanges under various configurations schematic



 3-2 Gain stepVarious changes in the configuration of a schematic