SmartSens

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SC1035 Datasheet

V1.2

2014.06.04

application

- car
- Security Monitoring
- Industrial Camera
- Door phone
- toy
- tablet
- MP4player
- MDIBaby monitors

characteristic

- Support for single-supply operation
- High photosensitivity
- Automatic exposure control
- 16xAnalog gain, 4xDigital Gain
- Level/Vertical windowing
- Automatic white balance control
- aperture/Gamma correction
- I2CRegister Programming Interface
- Output Interface
  - 12-bit DVP
- Low power consumption

Packaging Information

- SC1035CP48

  color48pin PLCCPackage

Key indicators (typ)

- 4μm×4μm 4T FSIPixel architecture
- Maximum image transmission rate:
  - 1280H×960V @ 45fps
  - 1200H×900V @ 50fps
  - 1280H×720V @ 60fps
- Dynamic Range70dB
- Optical Format1/2.8 "
- Output Interface12-bit Parallel Interface
- Output format:12-bit RAW RGB
- 0ºCRA
- Operating temperature range:-20ºC ~ +70ºC
- Optimum operating temperature range:0ºC ~ +50ºC
- Configure sensor slaveI2Cinterface
- voltage:
  - AVDD = PIXVDD = SVDD = 3.3V,

    DOVDD = 1.8V ~ 3.3V,

    DVDD = 1.5V(Internal support 1.5V

    regulatorpowered by)
- Image area: 5248μm×3904μm
- Package TypeLCC-48
- Package size:11.43mm×11.43mm

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Table Index

1 Signal Description

table1-1Listed SC1035Description of the image sensor signal and the corresponding pin number.

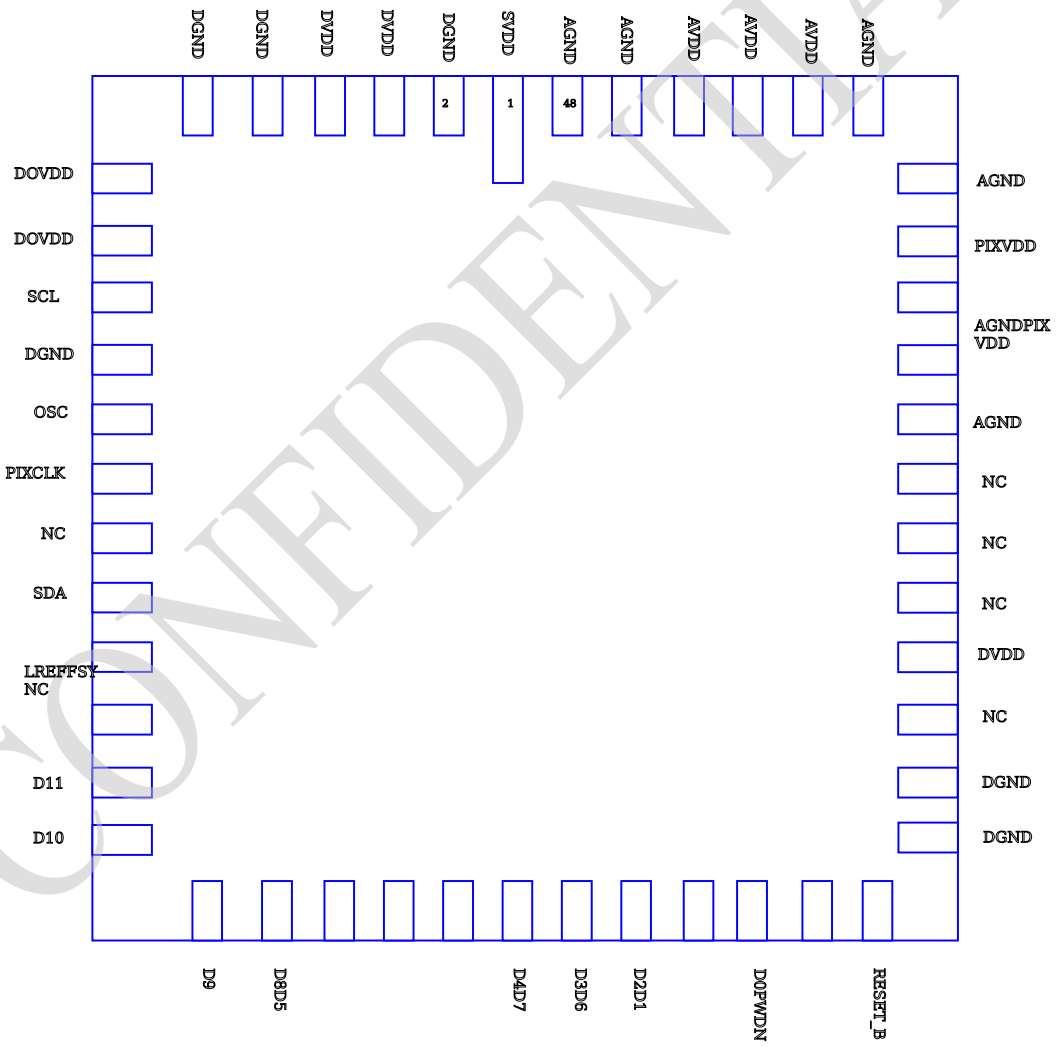
table1-1 Signal Description

Numbering	Signal names	Pin Type	description
1	SVDD	power supply	3.3VPixel array power supply
2	DGND	Ground	Digitally
3	DVDD	power supply	1.5VDigital Power
4	DVDD	power supply	1.5VDigital Power
5	DGND	Ground	Digitally
6	DGND	Ground	Digitally
7	DOVDD	power supply	1.8V / 3.3V IOpower supply
8	DOVDD	power supply	1.8V / 3.3V IOpower supply
9	SCL	enter	I2CInterface input clock line
10	DGND	Ground	Digitally
11	OSC	enter	System clock input
12	PIXCLK	I / O	Always input pixel
13	NC	N / A	not connected
14	SDA	I / O	I2CInterface cable (open drain)
15	FSYNC	I / O	Frame synchronization signal
16	LREF	I / O	Line synchronization signal
17	D11	Export	Parallel pixel data output[11]
18	D10	Export	Parallel pixel data output[10]
19	D9	Export	Parallel pixel data output[9]
20	D8	Export	Parallel pixel data output[8]

Numbering	Signal names	Pin Type	description
twenty one	D7	Export	Parallel pixel data output [7]
twenty two	D6	Export	Parallel pixel data output [6]
twenty three	D5	Export	Parallel pixel data output [5]
twenty four	D4	Export	Parallel pixel data output [4]
25	D3	Export	Parallel pixel data output [3]
26	D2	Export	Parallel pixel data output [2]
27	D1	Export	Parallel pixel data output [1]
28	D0	Export	Parallel pixel data output [0]
29	PWDN	enter	Power down signal input (built-in pull-down Resistance, high effective)
30	RESET_B	enter	Reset input (built-in pull-up resistor, low Bit effective)
31	DGND	Ground	Digitally
32	DGND	Ground	Digitally
33	NC	N / A	not connected
34	DVDD	power supply	1.5VDigital Power
35	NC	N / A	not connected
36	NC	N / A	not connected
37	NC	N / A	not connected
38	AGND	Ground	Analog ground
39	AGND	Ground	Analog ground
40	PIXVDD	power supply	3.3VPixel power
41	PIXVDD	power supply	3.3VPixel power
42	AGND	Ground	Analog ground
43	AGND	Ground	Analog ground
44	AVDD	power supply	3.3VAnalog supply

Numbering	Signal names	Pin Type	description
45	AVDD	power supply	3.3VAnalog supply
46	AVDD	power supply	3.3VAnalog supply
47	AGND	Ground	Analog ground
48	AGND	Ground	Analog ground

Top View



Map1-1 Pin Figure

2 System-level description

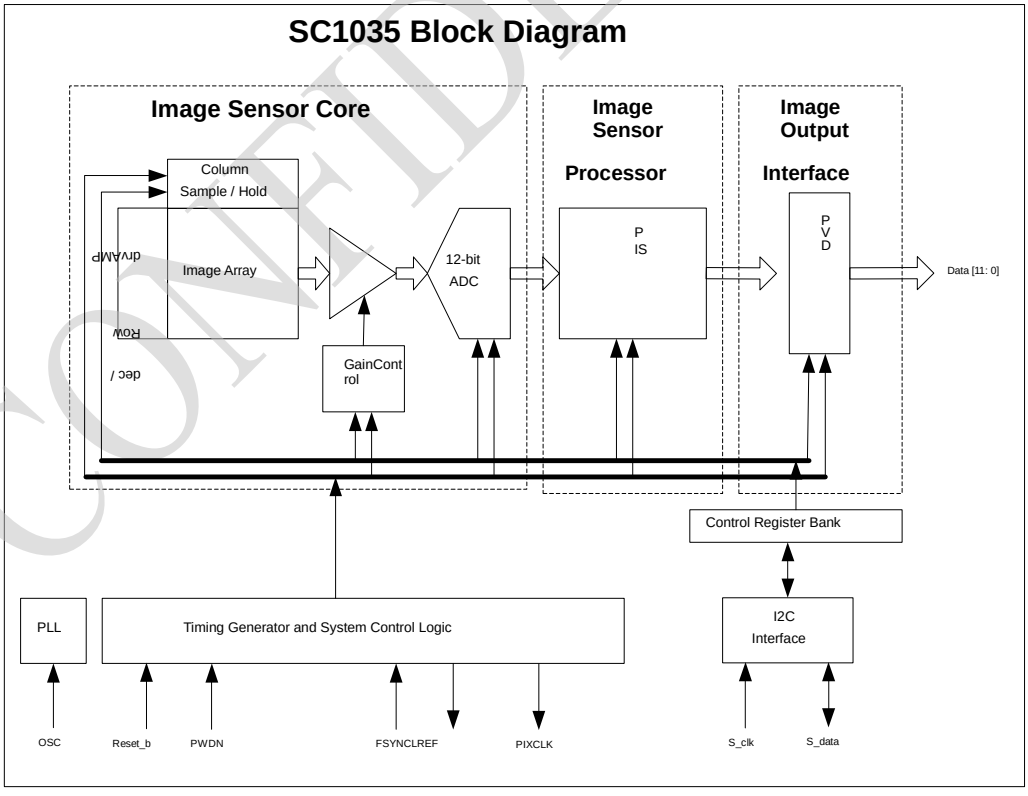
2.1 Outline

SC1035Is the most advanced camera field monitoring CMOSImage Sensor. stand by1280H×960V @ 45fps,1200H×900V @ 50fpsand1280H×720V @ 60fpsImage format. It outputs after the most radical thisISPAfter treatment rawFormat image. Effective pixel size 1280H960V. On-chip support complex operations - - Such as windowing, horizontal or vertical mirror and so on. Be configured through a simple two-wire serial port c

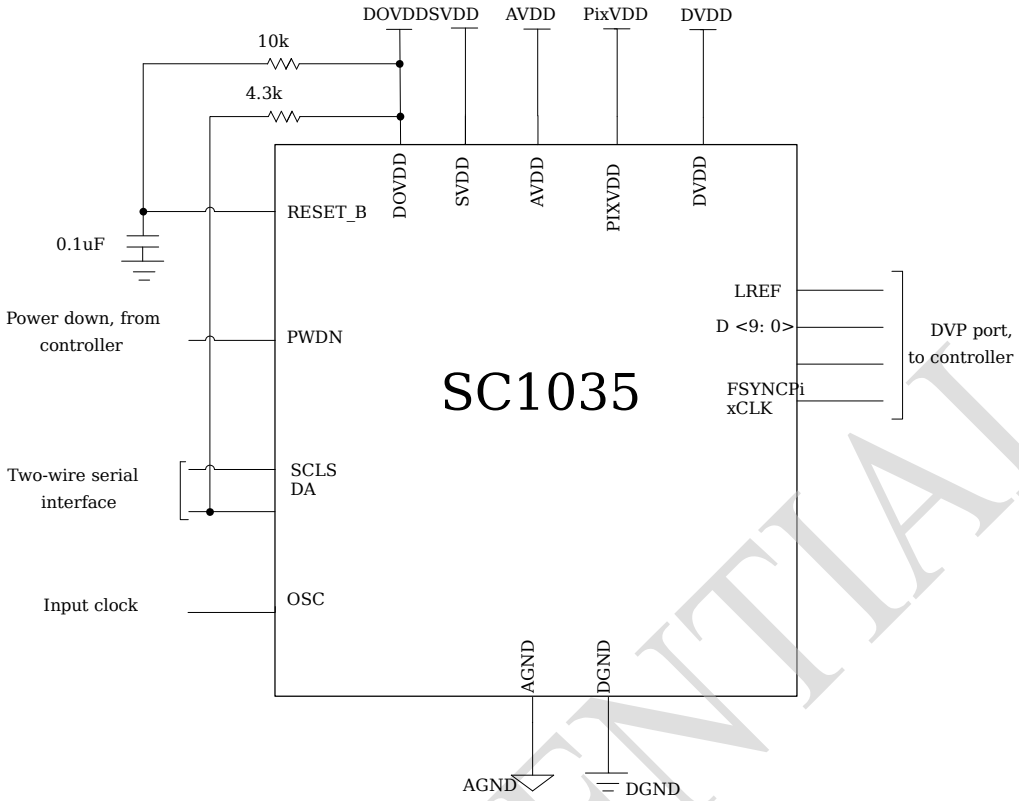
Can makeSC1035Work in the default mode, or configure their frame size, exposure time, gain and other similar Shall parameters. By default per 45the outputframe 1280H×960VSize image.

2.2 structure

SC1035It may be a fixed frame rate to generate pixel data stream, and with FSYNCAs a reference Test signal. Map2-1Shows SC1035Functional modules of the image sensor, and Map2-2Shows a typical application With examples.



Map2-1 SC1035block diagram

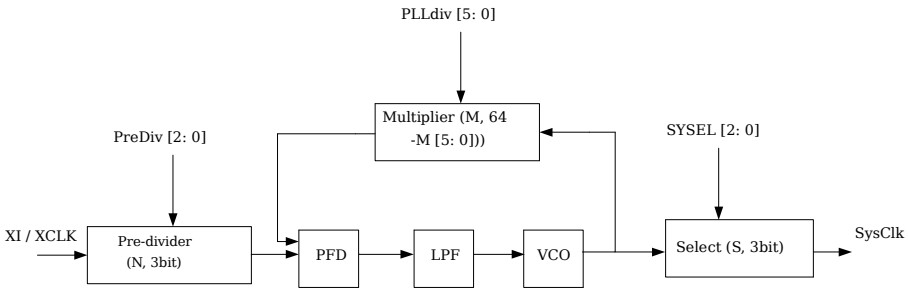


Map2-2 Typical Application Diagram

Note1: In order to obtain better image quality, DOVDD,SVDD,AVDD,PIXVDDmust use 3.3VIndependent power supply.

2.3 PLLcontrol

SC1035 PLLAllows input clock frequency range 6 ~ 27MHz,among theVCOFrequency maximum support 500MHz.PLLSchematics, and control registers are displayed in sum.



Map2-3 PLLControl schematic

table2-1 PLLControl register

address	Register name	Defaults	read/write	description
0x3010		8'h20	RW	Bit [7]: BYPASS PLL Bit [6: 4]: RESERVED Bit [3: 1]: PreDiv [2: 0] 000 ~ 1x 001 ~ 1.5x 010 ~ 2x 011 ~ 3x ..... 111 ~ 7x Bit [0]: PLLDIV [5: 0]
0x3011		8'h86	RW	Bit [7: 3]: PLLDIV [4: 0] Multiplier = 64-PLLDIV [5: 0] Bit [2: 0]: SYSEL [1: 0] 00 ~ 1x 01 ~ 4x 10 ~ 5x 11 ~ 6x

System clock frequency F_{sysclk} by formula 2-1 Calculated:

$$F_{sysclk} = F_{xclk} \times \frac{64 - M}{N \times (S + 1)} \quad (2\text{-}1)$$

2.4 Serial Register Interface (I²C)

SC1035 By standard 2-wire control register I2C Bus read and write. Its device address is 0x30.

Message Type: 16-bit address, 8-bit data and 7-bit device address

S	Slave Address	R / W	A	Sub Address [15: 8]	A	Sub Address [7: 0]	A	data	A / Ã	P

I2C read operation

S	Slave Address	0	A	Sub Address [15: 8]	A	Sub Address [7: 0]	A	Sr	Slave address	1	A	data	Ã	P

I2C writes

S	Slave Address	0	A	Sub Address [15: 8]	A	Sub Address [7: 0]	A	data	A / Ã	P

From slave to master S: START condition A: reply

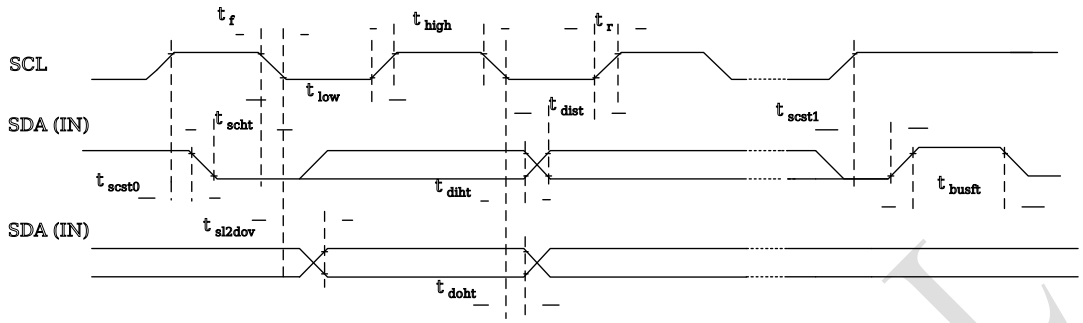
Master to slave P: Termination condition Ã: Reject reply

Depending on the direction of operation Sr: Repeated START condition

table 2-2 I2C Control register

address	Register name	Defaults	read/write	description
0x3008	I2C SLAVE ID	8'h60	RW	Bit [7: 1]: I2C slave id

I2C Timing



Map2-4 I2CInterface Timing

table2-3 I2CInterface Timing detailed parameters

symbol	parameter	Min	Typical value	Max	unit
f_{I2C}	Clock frequency	-	-	400	kHz
t_{low}	Clock Low Time	1.3	-	-	μs
t_{high}	Clock High Time	0.6	-	-	μs
t_{cl2dov}	SCLDown to the time interval between the output data is valid	0.1	-	0.9	μs
t_{busft}	An initial state before the next bus idle time	1.3	-	-	μs
t_{scht0}	START condition hold time	0.6	-	-	μs
t_{scst}	START condition setup time	0.6	-	-	μs
t_{diht}	Input Data Hold Time	0	-	-	μs
t_{dist}	Input data setup time	0.1	-	-	μs
t_{scst1}	Termination condition setup time	0.6	-	-	μs
$t_{f/}$ T_r	Fall than rise time	-	-	0.3	μs
t_{doht}	Output data hold time	0.05	-	-	μs

Note1: This is 400kHzMode I2CTiming.

2: Analyzing start rising or falling termination threshold is 10%, Analyzing rising or falling edge termination The initial threshold is 90%.

2.5 Power charging and power-off order

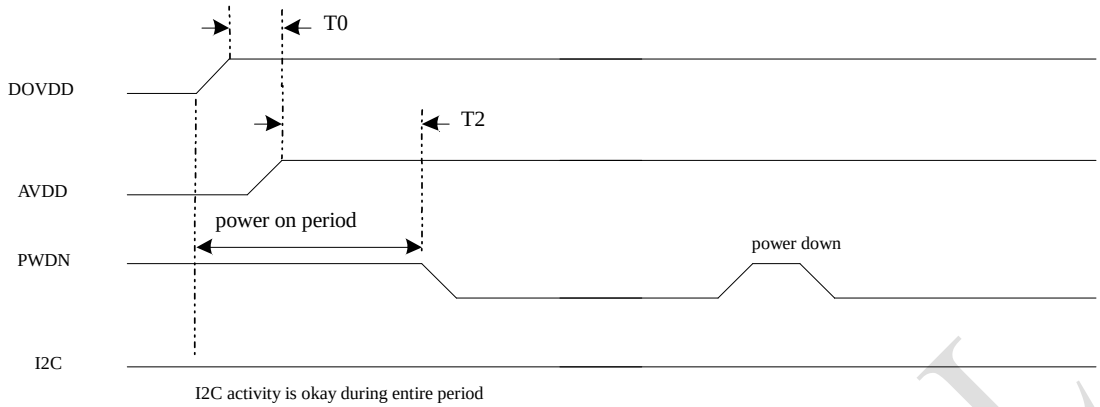
Based on different power configurations (I/O voltage, using built-in or external DVDD power supply), Electrification systems have some different requirements for power sequence. In order to I/O Port 1.8V Power supply, we recommend using the built-in DVDD Power supply. in case I/O Port 3.3V Power supply, due to the built-in DVDD There is a power supply High pressure drop may bring chip overheating. Therefore, 3.3V Power supply system, it is recommended to use an DVDD Power supply. In addition, as in this case results in a higher power-down current, it is necessary chip discomf use 3.3V I/O And an external power supply. PWDN When the power supply, turn off all power, including external supply.

2.5.1 When using the built-in power supply from the power DVDD Power Supply

Use the built-in DVDD Power supply, while the electrification time access, The following conditions must be met:

1. in case DOVDD and AVDDAt the same time open, you must ensure that DOVDD Before AVDD Prior to maintain stability;
2. PWDN Asynchronous trigger signal (no clock) and high effective;
3. During the electrification process must be PWDN signal, pulled
4. PWDN It must ensure that the electrification time has remained at a low level. AVDD Stable (low signal Room Interval of not less than 5ms);
5. RESET_B Asynchronous trigger signal status and effective;
6. During the electrification need to consider later RESET_B Signal is stable;
7. Master Clock, Clock In host access sensor I2C You must provide at least before the interval;
8. Hosts can access the entire period of bus (shared bus), In PWDN After the complex is given low Signal (reset signal PWDN Down 20ms Or after RESET_B Pulled 20ms After given), Host can access sensor I2C Bus to initialize the sensor.

DOVDD First pulled, then AVDD And the interval is less than 5ms;



Map2-5 InternalDVDDWhen the electric power supply from the order

Note1:T0≥0ms:DOVDDStability toAVDDStabilization delay.

2:T2≥5ms:AVDDStability to the sensor electrification between stable delay.

2.5.2 When using an external power supply electrification**DVDD**Power Supply

Using an external power supply, while the electrification time access, the following conditions must be met:

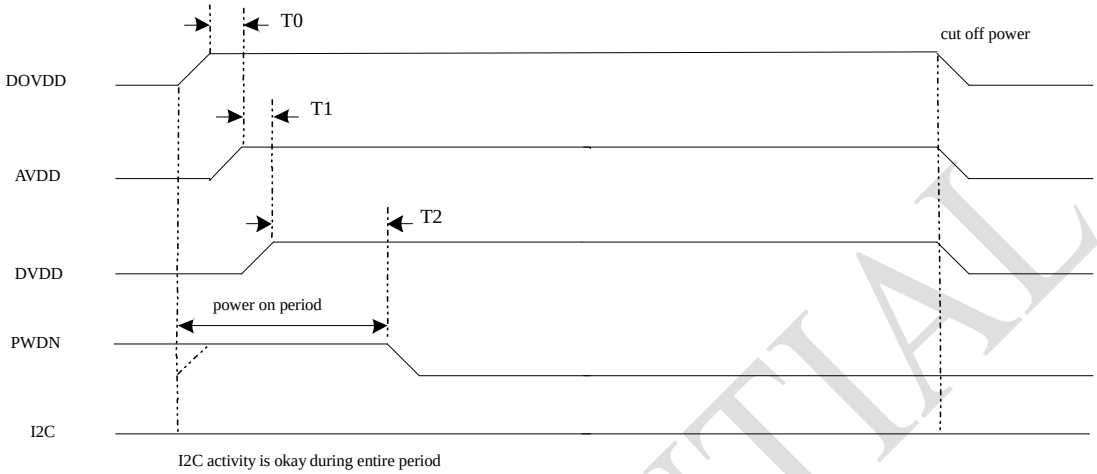
1. in caseDOVDDandAVDDAt the same time open, you must ensure that
2. in caseAVDDandDVDDAt the same time open, you must ensure that
3. PWDNAsynchronous trigger signal (no clock) and high effective;
4. PWDNIt must ensure that the electrification time has remained stable (low signal)

   Interval of not less than 5ms;
5. When not using the camera must be turned off all power (power-off mode is not recommended);
6. RESET_BAsynchronous trigger signal status and effective;
7. During the electrification need to consider later RESET_B Signal is stable;
8. Master Clock In host access sensor I2C You must provide at least 8 Time the clock interval;
9. Hosts can access the entire period I2C Bus (the electrical) In PWDN After the complex is given low

Signal (reset signal PWDNDown20msOr afterRESET_BPulled20msAfter given),

Host can access sensor I2CBus to initialize the sensor.

DOVDDFirst pulled, then AVDDAnd the interval is less than5ms



Map2-6 ExternalDVDDWhen the electric power supply from the order

Note1:T0≥0ms:DOVDDStability toAVDDStabilization delay.

2:T1≥0ms:AVDDStability toDVDDStabilization delay.

2:T2≥5ms:DVDDStability to the sensor electrification between stable delay.

2.6 Reset

SC1035Comprising a sensor RESET_BPin, grounding (DGND) Can be forced to complete the hard reset operating. Hard resetSC1035Register will clear all settings and reset to the default values. But can also pass PassI2CInterface register 0x3003ofBit [0]Set high to provide a soft reset function.

table2-4 Soft reset control register

address	Register name	Defaults	read/write	description
0x3003	Rst_pon	'B0	W	Bit [0]: rst soft

2.7 Power off and power-down mode

Sensor supply power off, all external power to be shut down, RESET_B, PWDN and OSC lead Feet should be low. And the power-down PWDN pin must be pulled.

2.8 Sleep Mode

Modify the appropriate register the sensor into sleep mode. In sleep mode, I2C Clock still kept jobs. You can still access the sensor registers.

table2-5 Sleep Mode Control Register

Features	Register name	description
Sleep Mode	0x3000	Bit [0]: manual stream enable Sleep = ~ Bit [0] or PWDN

3 The image sensor core functions

3.1 Mirroring and inversion

SC1035It provides mirroring mode and inversion mode. The former will reverse the data level sensor readout d

Who would reverse the vertical sensor readout order. Such asMap 3-1 FIG.

The original image Mirror Image Inverted image And inverted mirror image

Map3-1 Mirroring and inversion examples

table3-1 Mirroring and inversion mode control register

Features	Register name	description
Mirror Mode	0x321d	Bit [0]: mirror ctrl 0 ~ mirror off 1 ~ mirror on
Inverted mode	0x321c	Bit [6]: flip ctrl 0 ~ filp off 1 ~ flip on

3.2 Test Mode

To facilitate testing, SC1035It provides two test modes: incremental mode and the color bar pattern, such asMap 3-2 FIG.

Increment mode

Color bar pattern

Map3-2 Test Mode

table3-2 Test mode control register

Features	Register name	description
Increment mode	0x3781	Bit [1]: incremental pattern enable 0 ~ normal image 1 ~ incremental pattern
Color bar pattern	0x503d	Bit [7]: color bar test pattern 0 ~ disable 1 ~ enable

3.3 AEC / AGCalgorithm

3.3.1 Outline

AE image sensor control (AEC) And AGC (AGC) Function can be calculated together Suitable exposure time and gain, so as to adjust the brightness of the image to a certain range. In addition to the a You can also manually set the exposure time and gain. Such as table 3-3 of related registers

table3-3 AECControl register

Features	Register name	description
AECEnable	0x3e03	Bit [0]: AEC manual 0 ~ auto enable 1 ~ manual enable
AEC(Exposure time)	{0x3e01,0x3e02}	0x3e01 = AEC [15: 8] 0x3e02 = AEC [7: 0]
AEC(Gain)	{0x3e08 [0], 0x3e09}	Gain
Gain Enable	0x3e03	Bit [1]: AGC manual 0 ~ auto enable 1 ~ manual enable

3.3.2 Algorithm based on mean

Based on the mean AEC Algorithm uses register WPT(0x350f)andBPT(0x3510) To control the image brightness degree. Here, the register WPT(0x350f) Values represent high threshold, and register BPT(0x3510) The value table It shows low threshold. When the average YAVG(0x568a) Register target image WPT(0x350f)andBPT (0x3510Within) the scope, AECModule will maintain the current exposure; when YAVG(0x568a) Is greater than WPT (0x350f)Time,AECModule will reduce exposure. And when YAVG(0x568a) Value of less than BPT(0x3510) Time,AECModule will increase the exposure.

Accordingly, the register WPT(0x350f) Should be greater than the BPT(0x3510) Value. The difference between the two It can be controlled from the stability of the image.

3.3.3 Mean luminance (**YAVG**)

It offers two windowed modes: automatic window and sub-window mode. In automatic windowing (default) m YAVGThe output from the window by the input image size (Image size) To decide. In the sub-window mode (the register 0x5708 [0]Set1), The output from the register window AVG_X_START,AVG_X_WIDTH, AVG_Y_STARTandAVG_Y_HEIGHTDecision.

table3-4 YAVGControl register

Features	Register name	description
YAVGWindowing is enabled	0x5708	Bit [0]: win_man_en 0 ~ auto enable 1 ~ manual enable
AVG_X_START	{0x5700 [3: 0], 0x5701}	0x5700 [3: 0] = avg_x_start [11: 8] 0x5701 = avg_x_start [7: 0]
AVG_X_WIDTH	{0x5704 [3: 0], 0x5705}	0x5704 [3: 0] = avg_x_width [11: 8] 0x5705 = avg_x_width [7: 0]
AVG_Y_START	{0x5702 [3: 0], 0x5703}	0x5702 [3: 0] = avg_y_start [11: 8] 0x5703 = avg_y_start [7: 0]
AVG_Y_HEIGHT	{0x5706 [3: 0], 0x5707}	0x5706 [3: 0] = avg_y_width [11: 8] 0x5707 = avg_y_width [7: 0]

3.4 Black level correction

Pixel array comprises 8 Article black line. These black lines can provide data to compensate for the elimination algo
Must first subtract black level. BLC Algorithm can estimate the black level compensation value from the black line data.
Value minus the respective black level compensation value of the color channels. If some specific pixels, such redu
Negative, then the result is 0. By default, it will re-gain value after change BLCoperating.

Calculated by two modes: BLC And automaticBLC. In manual mode, the compensation value is specified by the
In automatic mode, the compensation value is calculated by a black line.

table3-5 BLCControl register

Features	Register name	description
BLCEnable	0x3900	Bit [0]: blc_enable 0 ~ bypass blc 1 ~ BLC enable
automaticBLCEnable	0x3902	Bit [6]: blc_auto_en 0 ~ manual mode 1 ~ auto mode
BLCChannel selection	{0x3928 [0], 0x3905 [6]}	0x3928 [0]: 0 ~ use 8 channel offset mode 1 ~ use 4 channel offset mode 0x3905 [6]: one channel enable 0 ~ use 8 or 4 channel offset 1 ~ use one channel mode
BLCTarget	{0x3907 [4: 0], 0x3908}	BLC target
BLC_manual00(B$_0$)	{0x3909 [4: 0], 0x390a}	BLC offset for B$_0$channel
BLC_manual01(GB$_0$)	{0x390b [4: 0], 0x390c}	BLC offset for GB$_0$channel
BLC_manual02(B$_1$)	{0x390d [4: 0], 0x390e}	BLC offset for B$_1$channel
BLC_manual03(GB$_1$)	{0x390f [4: 0], 0x3910}	BLC offset for GB$_1$channel
BLC_manual10(GR$_0$)	{0x3920 [4: 0], 0x3921}	BLC offset for GR$_0$channel
BLC_manual11(R$_0$)	{0x3922 [4: 0], 0x3923}	BLC offset for R$_0$channel
BLC_manual12(GR$_1$)	{0x3924 [4: 0], 0x3925}	BLC offset for GR$_1$channel
BLC_manual13(R$_1$)	{0x3926 [4: 0], 0x3927}	BLC offset for R$_1$channel

3.5 Digital Gain

After subtracting the black level, all the pixel values are multiplied by a digital gain value. By default, the sen

Before using the digital gain will be adjusted to the maximum analog gain.

table3-6 Digital gain control register

Features	Register name	description
Digital Gain	{0x3e08 [0], 0x3e09 [7]}	2'b01,2'b10: 2x dig gain 2'b11: 4x dig gain

3.6 Line noise canceling (**RNC**)

Pixel array comprises 64 effective black reference columns that can provide data for the line noise cancellation algorithm RNC. The

Method can estimate the noise travel from black reference column data. For the same line, the line noise is the same

Noise row between rows different from each other. Taking into account the presence of color filters, you must use

If the cancellation algorithm (subtraction) to give a negative value in a particular pixel, then the result set 0.

table3-7 RNCControl register

Features	Register name	description
RNCEnable	0x3400	Bit [0]: rnc_enable 0 ~ bypass blc 1 ~ RNC enable
automaticRNCEnable	0x3400	Bit [1]: rnc_auto_en 0 ~ manual mode 1 ~ auto mode
RNCChannel selection	0x3400	Bit [5]: one channel enable 0 ~ use 4 channel mode 1 ~ use 1 channel mode
RNC_manual00(B)	{0x3405 [4: 0], 0x3404}	RNC noise for B channel
RNC_manual01(GB)	{0x3407 [4: 0], 0x3406}	RNC noise for GB channel
RNC_manual10(GR)	{0x3409 [4: 0], 0x3408}	RNC noise for GR channel
RNC_manual11(R)	{0x340b [4: 0], 0x340a}	RNC noise for R channel

4 Digital image sensor function

4.1 ISPTop register

ISPPurpose top-level module: generate the necessary control signals.

table4-1 ISPTop register

Features	Register name	description
ISP_CTRL	0x5000	Bit [7]: LENC correnction enable 0 ~ disable 1 ~ enable Bit [4]: var_en Bit [3]: awb_gain_en Bit [0]: auto white balance enable 0 ~ disable 1 ~ enable

4.2 data synchronization

data synchronization SYNC)M odule two paths merge into a single data path.

table4-2 SYNCControl register

address	Register name	Defaults	read/write	description
0x3780	BLC_SYNC00	8'h10	RW	Bit [5: 0]: ASP delay cycles

address	Register name	Defaults	read/write	description
0x3781	BLC_SYNC01	8'h10	RW	Bit [7]: incremental pattern enable Bit [4]: r_raw1_swap_en Bit [3]: r_raw0_swap_en Bit [2]: rbule reverse Bit [1]: adc_g channel first enable Bit [0]: adclk_inv

4.3 Lens Correction

Lens Correction (LENC) The purpose of the module is to compensate for the distortion of light caused by the came

With respect to the lens (center) distortion, LENC module calculates the gain value at this point. Then in accordance with the

Gain for each pixel, and corrects the image data, in order to compensate for the distortion of the light.

table4-3 LENCControl register

address	Register name	Defaults	read/write	description
0x5000	ISP_CTRL00	8'h99	RW	Bit [7]: LENC correction enable 0 ~ disable 1 ~ enable

address	Register name	Defaults	read/write	description
0x5800	LENC_CTRL00	8'h90	RW	Bit [6]: no_delay 1 ~ sel data_i do lenc 0 ~ data_3d do lenc Bit [5]: debug mode Bit [4]: lenc_bias_en 1 ~ sub bias before do lenc 0 ~ use data_i do lenc Bit [1]: sel deltagain Bit [0]: sel_ra, if lenc enable select test mode
0x5801	LENC_RADIUS	8'h20	RW	Bit [7: 0]: lenc_radius
0x5802	LENC_XOFFSET	8'h20	RW	Bit [7: 0]: the horizontal start size
0x5803	LENC_YOFFSET	8'h10	RW	Bit [7: 0]: the vertical start size
0x5804	LENC_RGAIN	8'h80	RW	Bit [7: 0]: red color coefficient
0x5805	LENC_GGAIN	8'h80	RW	Bit [7: 0]: green color coefficient
0x5806	LENC_BGAIN	8'h80	RW	Bit [7: 0]: blue color coefficient
0x5807	LENC_CTRL07	8'h00	RW	Bit [7]: xy_offset_man_en Bit [5]: hskip_man_en Bit [4]: vskip_man_en Bit [3: 2]: r_hskip Bit [1: 0]: r_vskip
0x5808	LENC_XCNT	8'h2	RW	Bit [7: 2]: RESERVED Bit [1: 0]: xcnt [9: 8] horizontal center
0x5809	LENC_XCNT	8'h8a	RW	Bit [7: 0]: xcnt [7: 0]

address	Register name	Defaults	read/write	description
0x580a	LENC_YCNT	8'h1	RW	Bit [7: 2]: RESERVED Bit [1: 0]: ycnt [9: 8] vertical center
0x580b	LENC_YCNT	8'hf0	RW	Bit [7: 0]: ycnt [7: 0]

4.4 Auto White Balance

Auto White Balance(AWB) The purpose is to remove the false color image point, in order to identify the human eye Objects in the same image or video screen is displayed as a white object is AWB Module will ensure that white pixels in different Under the color temperature remains constant. Supports manual white balance and auto white balance. Automatic Simple automatic white balance and advanced automatic white balance. Advanced auto white balance color tempe Shade relative warmth and cold degrees.

table4-4 AWBControl register

address	Register name	Defaults	read/write	description
0x5000	ISP_CTRL00	8'h99	RW	Bit [3]: awb_gain_en Bit [0]: auto white balance enable 0 ~ disable 1 ~ enable
0x5180	AWB_CTRL00	8'h04	RW	Bit [7: 0]: stable_range
0x5181	AWB_CTRL01	8'h8	RW	Bit [7: 6]: stable_range
8x5182	AWB_CTRL02	8'h0	RW	Bit [0]: gain_man_en

4.5 VAR

VARThe purpose is to complete horizontal and vertical down-sampling.

table4-5 VARControl register

address	Register name	Defaults	read/write	description
0x5000	ISP_CTRL00	8'h99	RW	Bit [4]: var_en
0x5900	VAR_CTRL00	8'h01	RW	Bit [7]: b_avg_en Bit [6]: gb_avg_en Bit [5]: gr_avg_en Bit [4]: r_avg_en Bit [3]: debug_en Bit [2]: single_channel bypass Bit [1: 0]: addopt
0x5901	VAR_CTRL01	8'h0	RW	Bit [3: 2]: hskip Bit [1: 0]: vskip

4.6 Brightness mean calculation

Brightness mean calculation The purpose of the module is to calculate the brightness of the image data using the average Mean.

table4-6 YAVGControl register

address	Register name	Defaults	read/write	description
0x5680	AVG_XSTART	8'h00	RW	Bit [7: 4]: RESERVED Bit [3: 0]: r_avg x start [11: 8] horizontal start position for average window
0x5681	AVG_XSTART	8'h00	RW	Bit [7: 0]: r_avg x start [11: 8] horizontal start position for average window

address	Register name	Defaults	read/write	description
0x5682	AVG_YSTART	8'h00	RW	Bit [7: 4]: RESERVED Bit [3: 0]: r_avg y start [11: 8] vertical start position for average window
0x5683	AVG_YSTART	8'h00	RW	Bit [7: 0]: r_avg y start [11: 8] vertical start position for average window
0x5684	AVG_WIN_WIDTH	8'h10	RW	Bit [7: 4]: RESERVED Bit [3: 0]: r_win_width [11: 8] the width for average window
0x5685	AVG_WIN_WIDTH	8'ha0	RW	Bit [7: 0]: r_win_width [7: 0] the width for average window
0x5686	AVG_WIN_HEIGHT	8'h0c	RW	Bit [7: 4]: RESERVED Bit [3: 0]: r_win_height [11: 8] the height for average window
0x5687	AVG_WIN_HEIGHT	8'h67	RW	Bit [7: 0]: r_win_height [7: 0] the height for average window
0x5688	AVG_CTRL08	8'h2	RW	Bit [1]: avg_opt Bit [0]: win_man
0x568a	averge	-	RO	

5 The image sensor register list

5.1 SC

table5-1 SCControl register

address	Register name	Defaults	read/write	description
0x3000	SC_REG00	8'h01	RW	Bit [0]: manual stream enable Sleep = Bit [0] | p_pwdn_i | GPIO [0]
0x3001	SC_REG01	8'h00	RW	Bit [7]: rst avg Bit [6]: isp Bit [4]: rst blc Bit [3]: rst sync Bit [2]: rst sensor_ctrl Bit [1]: rst timing_ctrl Bit [0]: rst aec_pk
0x3002	SC_REG02	8'h00	RW	Bit [4]: rst channel gain Bit [3]: rst dvp_pre Bit [1]: rst data_pre Bit [0]: rst dvp
0x3004	SC_REG04	8'h02	RW	Bit [7]: sclk_sel_pad 1 ~ p_clk_i 0 ~ pll_sclk_i Bit [6]: r_sclk_div2_en Bit [4: 0]: sclk2x_div

address	Register name	Defaults	read/write	description
0x3005	SC_REG05	8'h22	RW	Bit [7: 4]: ppump_div 0/1 - ÷1 2 ~ ÷2 3 ~ ÷3 ... Bit [3: 0]: npump_div
0x3006	DIR_CTRL0	8'hff	RW	Bit [7]: c_vsync_o Bit [6]: c_pclk_o Bit [5]: c_href_o Bit [4]: c_fsin_o Bit [3: 0]: c_y_o [11: 8]
0x3007	DIR_CTRL1	8'hff	RW	Bit [7: 0]: c_y_o [7: 0]
0x3008	I2C_ID	8'h60	RW	I2C slave ID
0x3009	GPIO_CTRL	8'h00	RW	Bit [7: 4]: gpio_dir [3: 0] 0 ~ input 1 ~ output Bit [3: 0]: gpio_out [3: 0]
0x300a	SC_CTRL0A	8'h01	RW	Bit [0]: sys_rst_enable
0x3010	PLL_CTRL1	8'h20	RW	Bit [7: 6]: pll1_cp Bit [5: 0]: pll1_multiplier
0x3011	PLL_CTRL0	8'h86	RW	Bit [7]: pll1_bypass Bit [6: 4]: pll1_prediv Bi [3]: pll1_cp2 [2] Bit [2: 0]: pll1_sdiv
0x3080	GPIO_IN	-	RO	input of GPIO [3: 0]

5.2 SB CONTROL

table5-2 SBControl register

address	Register name	Defaults	read/write	description
0x2140	SB_SCCB_CTRL	8'h00	RW	Bit [7: 4]: RESERVED Bit [3]: r_sda_dly_en Bit [2: 0]: r_sda_dly
0x2141	SB_SCCB_OPT	8'h12	RW	Bit [7: 5]: RESERVED Bit [4]: en_ss_addr_inc Bit [3]: r_sda_byp_sync 0 ~ two clock stage sync for sda_i 1 ~ no sync for sda_i Bit [2]: r_scl_byp_sync 0 ~ two clock stage sync for scl_i 1 ~ no sync for scl_i Bit [1]: r_msk_glitch Bit [0]: r_msk_stop
0x2042	SB_SCCB_FILTER	8'h00	RW	Bit [7: 4]: r_sda_num Bit [3: 0]: r_scl_num

5.3 BLC SYNC

table5-3 BLC SYNCControl register

address	Register name	Defaults	read/write	description
0x3780	BLC_SYNC00	8'h01	RW	Bit [5: 0]: ASP delay cycles

address	Register name	Defaults	read/write	description
0x3781	BLC_SYNC01	8'h10	RW	Bit [7]: incremental pattern enable Bit [4]: r_raw1_swap_en Bit [3]: r_raw0_swap_en Bit [2]: rbule reverse Bit [1]: adc_g channel first enable Bit [0]: adclk_inv

5.4 CHANNEL GAIN

table5-4 CHANNEL GAINControl register

address	Register name	Defaults	read/write	description
0x3100	CHANNEL_GAIN00	8'h06	RW	Bit [5]: r_fpn_line_gain_en Bit [4]: r_row_same_gain_en Bit [3]: r_blue_sel Bit [2]: r_link_blank_gain_en Bit [1]: r_black_line_gain_en Bit [0]: r_channel_gain_en
0x3101	CHANNEL_GAIN01	8'h00	RW	Bit [7]: r_black_line_f_sel_o Bit [5]: r_fpn_line_f_en Bit [4]: r_fpn_rnc_en Bit [3]: r_fpn_awb_en Bit [2]: r_fpn_dpc_oned_en Bit [1]: r_fpn_lenc_en Bit [0]: r_fpn_blc_en
0x3102	R_B0_GAIN_H	8'h10	RW	r_b0_gain [12: 8]
0x3103	R_B0_GAIN_L	8'h00	RW	r_b0_gain [7: 0]

address	Register name	Defaults	read/write	description
0x3104	R_GB0_GAIN_H	8'h10	RW	r_gb0_gain [12: 8]
0x3105	R_GB0_GAIN_L	8'h00	RW	r_gb0_gain [7: 0]
0x3106	R_B1_GAIN_H	8'h10	RW	r_b1_gain [12: 8]
0x3107	R_B1_GAIN_L	8'h00	RW	r_b1_gain [7: 0]
0x3108	R_GB1_GAIN_H	8'h10	RW	r_gb1_gain [12: 8]
0x3109	R_GB1_GAIN_L	8'h00	RW	r_gb1_gain [7: 0]
0x310a	R_RG0_GAIN_H	8'h10	RW	r_rg0_gain [12: 8]
0x310b	R_RG0_GAIN_L	8'h00	RW	r_rg0_gain [7: 0]
0x310c	R_R0_GAIN_H	8'h10	RW	r_r0_gain [12: 8]
0x310d	R_R0_GAIN_L	8'h00	RW	r_r0_gain [7: 0]
0x310e	R_RG1_GAIN_H	8'h10	RW	r_rg1_gain [12: 8]
0x310f	R_RG1_GAIN_L	8'h00	RW	r_rg1_gain [7: 0]
0x3110	R_R1_GAIN_H	8'h10	RW	r_r1_gain [12: 8]
0x3111	R_R1_GAIN_L	8'h00	RW	r_r1_gain [7: 0]
0x3112	R_FPN_ROW_START_H	8'h00	RW	high byte of r_fpn_row_start
0x3113	R_FPN_ROW_START_L	8'h08	RW	low byte of r_fpn_row_start
0x3114	R_FPN_ROW_END_H	8'h00	RW	high byte of r_fpn_row_end
0x3115	R_FPN_ROW_END_L	8'h0c	RW	low byte of r_fpn_row_end
0x3116	R_FPN_COL_COUNT_H	8'h00	RW	high byte of r_fpn_col_count
0x3117	R_FPN_COL_COUNT_L	8'h64	RW	low byte of r_fpn_col_count

5.5 AEC

table5-5 AECControl register

address	Register name	Defaults	read/write	description
0x3500	AEC_CTRL00	8'h78	RW	Bit [7]: debug mode Bit [6]: less one line enable Bit [5]: band function enable Bit [4]: less 1 band enable Bit [3]: start selection Bit [2]: night mode Bit [1]: new balance function Bit [0]: freeze
0x3501	AEC_MIN_EXPOSURE	8'h01	RW	Bit [7: 0]: minimum exposure minimum exposure output limit
0x3502	AEC_MAX_EXPO_H (60Hz)	8'h3d	RW	Bit [7: 0]: maximum exposure [15: 8] 60Hz maximum exposure output limit
0x3503	AEC_MAX_EXPO_L (60Hz)	8'h80	RW	Bit [7: 0]: maximum exposure [7: 0] 60Hz maximum exposure output limit
0x3504	DEBUG MODE	8'h00	RW	

address	Register name	Defaults	read/write	description
0x3505	AEC_CTRL05	8'h30	RW	AEC system control 2 Bit [7]: debug mode Bit [6]: frame insert 0 ~ in night mode insert frame disable 1 ~ in night mode insert frame enable Bit [5]: step auto enable 0 ~ step manual mode 1 ~ step auto mode Bit [4: 0]: step auto ratlo in step auto mode ratle setting to adjust speed
0x3506	AEC_CTRL06	8'h10	RW	AEC system control 3 Bit [7: 5]: debug mode Bit [4: 0]: step manual setting 1 step manual increase mode fast step
0x3507	AEC_CTRL07	8'h18	RW	AEC system step register Bit [7: 4]: step manual setting 2 step manual slow step Bit [3: 0]: step manual setting 3 step manual fast step
0x3508	AEC_B50_STEP	8'h01	RW	50Hz band width Bit [7: 2]: debug mode Bit [1: 0]: b50 step [9: 8]

address	Register name	Defaults	read/write	description
0x3509	AEC_B50_STEP	8'h01	RW	50Hz band width Bit [7: 0]: b50 step [7: 0]
0x350a	AEC_B60_STEP	8'h01	RW	60Hz band width Bit [7: 2]: debug mode Bit [1: 0]: b60 step [9: 8]
0x350b	AEC_B60_STEP	8'h01	RW	60Hz band width Bit [7: 0]: b60 step [7: 0]
0x350c	AEC_CTRL0C	8'he4	RW	Bit [7: 4]: E1 max decimal line high limit zone Bit [3: 0]: E1 min decimal line low limit zone
0x350d	AEC_CTRL0D	8'h08	RW	60Hz max bands in one frame Bit [7: 6]: debug mode Bit [5: 0]: b60 max
0x350e	AEC_CTRL0E	8'h06	RW	50Hz max bands in one frame Bit [7: 6]: debug mode Bit [5: 0]: b50 max
0x350f	AEC_CTRL0F	8'h78	RW	stable range hig limit Bit [7: 0]: WPT
0x3510	AEC_CTRL10	8'h68	RW	stable range low limit Bit [7: 0]: BPT
0x3511	AEC_CTRL11	8'hd0	RW	stable manual mode fast zone high limit Bit [7: 0]: VPT high

address	Register name	Defaults	read/write	description
0x3513	AEC_CTRL13	8'h40	RW	Bit [7]: debug mode Bit [6]: pre_gain enable Bit [5: 0]: pre_gain_value
0x3514	AEC_MAX_EXPO_H (50Hz)	8'h0e	RW	50Hz maximum exposure output limit Bit [7: 4]: debug mode Bit [3: 0]: maximum exposure [11: 8]
0x3515	AEC_MAX_EXPO_L (50Hz)	8'h40	RW	50Hz maximum exposure output limit Bit [7: 0]: maximum exposure [7: 0]
0x3517	AEC_CTRL17	8'h01	RW	gain base when in night mode Bit [7: 2]: debug mode Bit [1: 0]: gain night threshold 00 to 00 01 to 10 10 to 30 11 to 70
0x3518	AEC_GAIN_CEILING	8'h03	RW	gain output top limit Bit [7: 3]: debug mode Bit [2: 0]: aec gain ceiling [9: 8] real gain format
0x3519	AEC_GAIN_CEILING	8'he0	RW	gain output top limit Bit [7: 0]: aec gain ceiling [7: 0] real gain format

address	Register name	Defaults	read/write	description
0x351a	AEC_DIFF_MIN	8'h04	RW	reserved default value for this register Bit [7: 0]: difference minimal
0x351b	AEC_CTRL1B	8'h78	RW	stable range high limit (go out) Bit [7: 0]: WPT2
0x351c	LED_ADD_ROW	8'h06	RW	exposure values added when strobe is on Bit [7: 0]: AEC LED add row [15: 8]
0x351d	LED_ADD_ROW	8'h18	RW	exposure values added when strobe is on Bit [7: 0]: AEC LED add row [7: 0]
0x351e	AEC_CTRL1E	8'h68	RW	stable range low limit (go out) Bit [7: 0]: BPT2
0x351f	AEC_CTRL1F	8'h40	RW	stable manual mode fast zone low limit Bit [7: 0]: VPT low
0x3520	AEC_CTRL20	8'h20	RW	Bit [7: 3]: debug mode Bit [2]: strbe option Bit [1: 0]: debug mode
0x3521	AEC_CTRL21	8'h78	RW	Bit [7]: debug mode Bit [6: 4]: strbe option Bit [3: 0]: debug mode
0x3522	AEC_CTRL25	8'h00	RW	Bit [7: 5]: debug mode Bit [4: 2]: freeze counter Bit [1: 0]: debug mode

5.6 AEC PK

table5-6 AEC PKControl register

address	Register name	Defaults	read/write	description
0x3e00	AEC_PK_EXPOSURE	8'h00	RW	exposure output Bit [7: 4]: debug mode Bit [3: 0]: exposure [19:16]
0x3e01	AEC_PK_EXPOSURE	8'h02	RW	exposure output Bit [7: 0]: exposure [15: 8]
0x3e02	AEC_PK_EXPOSURE	8'h00	RW	exposure output Bit [7: 0]: exposure [7: 0] lower four bits are a fraction of a line, do not use
0x3e03	AEC_PK_MANUAL	8'h00	RW	AEC manual mode control Bit [7: 2]: debug mode Bit [1]: AGC manual 0 ~ auto enable 1 ~ manual enable Bit [0]: AEC manual 0 ~ auto enable 1 ~ manual enable
0x3e08	AEC_PK_SNR_GAIN	8'h00	RW	SNR gain Bit [7: 2]: debug mode Bit [1: 0]: snr gain [9: 8]

address	Register name	Defaults	read/write	description
0x3e09	AEC_PK_SNR_GAIN	8'h10	RW	SNR gain Bit [7: 0]: snr gain [7: 0] Bit [3: 0] fine gain Bit [6: 4] sa1 gain
0x3e0a	AEC_PK_REAL_GAIN	8'h00	RW	real gain Bit [7: 2]: debug mode Bit [1: 0]: real gain [9: 8]
0x3e0b	AEC_PK_REAL_GAIN	8'h00	RW	real gain Bit [7: 0]: real gain [7: 0]
0x3e0c	AEC_PK_VTS	8'h00	RW	AEC VTS output Bit [7: 0]: VTS [15: 8]
0x3e0d	AEC_PK_VTS	8'h00	RW	AEC VTS output Bit [7: 0]: VTS [7: 0]
0x3e0e	AEC_PK_CTRL0E	8'h54	RW	Bit [7]: r_cexp_sel 1 ~ aec_expo 0 ~ aec_expo [15: 4] Bit [6]: r_dcg_auto_en Bit [5]: r_sa1_gain_overflowen Bit [4]: r_fine_gain_dcg_sel Bit [3: 0]: r_fine_gain_dcg_compensate

address	Register name	Defaults	read/write	description
0x3e0f	AEC_PK_CTRL0F	8'h10	RW	Bit [4]: r_dig_gain_sel1 1 ~ agc_adj [9: 0] 0 ~ else Bit [3]: r_dig_gain_sel2 1 ~ agc_adj [8: 7] 0 ~ {1'b0, agc_adj [8]} Bit [2]: r_blc_dig_gain_man_en Bit [1: 0]: the value manual dig gain

5.7 ANA REG

table5-7 ANA REGControl register

address	Register name	Defaults	read/write	description
0x3600	ADC	8'h54	RW	ADC [7: 0]
0x3601	ADC	8'h03	RW	ADC [15: 8]
0x3602	ADC	8'h2f	RW	ADC [23:16]
0x3603	ADC	8'h00	RW	ADC [32:24]
0x3610	ANALOG	8'h2c	RW	ANALOG [7: 0]
0x3611	ANALOG	8'h66	RW	ANALOG [15: 8]
0x3612	ANALOG	8'h80	RW	ANALOG [23:16]
0x3613	ANALOG	8'h88	RW	ANALOG [31:24]
0x3614	ANALOG	8'h08	RW	ANALOG [39:32]
0x3615	A_TEST	8'h00	RW	
0x3616	ANALOG6	8'h00	RW	
0x3617	ANALOG7	8'h00	RW	
0x3618	ANALOG8	8'h00	RW	

address	Register name	Defaults	read/write	description
0x3620	ARRAY	8'h88	RW	ARRAY [7: 0]
0x3621	ARRAY	8'h03	RW	ARRAY [15: 8]
0x3622	ARRAY	8'h00	RW	ARRAY [23:16]
0x3630	PWC	8'h80	RW	PWC [7: 0]
0x3631	PWC	8'h88	RW	PWC [15: 8]
0x3632	PWC	8'h40	RW	PWC [23:16]
0x3633	PWC	8'h64	RW	PWC [31:24]
0x3634	PWC	8'h91	RW	PWC [39:32]
0x3635	PWC	8'h80	RW	PWC [47:40]
0x3640	PAD_CTRL	8'h00	RW	

5.8 SENSOR CTRL

table5-8 SENSOR CTRLControl register

address	Register name	Defaults	read/write	description
0x3300	SENSOR_REG00	8'h56	RW	Bit [7: 4]: y_rst gap Bit [3: 0]: y_hblk gap
0x3301	SENSOR_REG01	8'h5d	RW	Bit [7: 4]: y_tx gap Bit [3: 0]: y_sig gap
0x3302	SENSOR_RSTGOLOW	8'h50	RW	rst go low point
0x3303	SENSOR_HLDWIDTH	8'h9a	RW	hblk / hsig width
0x3304	SENSOR_TXWIDTH	8'h9a	RW	tx width_sa
0x3305	SENSOR_REG05	8'hc3	RW	Bit [7: 4]: y_xlckb width Bit [2: 0]: y_rs gap
0x3306	SENSOR_REG06	8'h31	RW	chip debug

address	Register name	Defaults	read/write	description
0x3307	SENSOR_REG07	8'h03	RW	Bit [7]: r_vario Bit [6]: r_pvario4 Bit [5]: r_pvario2 Bit [4]: pre-pre-charge enable for long exposure Bit [3: 0]: long pre-pre-charge
0x3308	SENSOR_REG08	8'h00	RW	Bit [7]: rst_all_hi Bit [6]: sample rs_all_hi Bit [5]: sample rs_all_low Bit [4]: tx high enable Bit [3]: ptxlow Bit [2]: stxlow Bit [1: 0]: hld2s, hld switch 00～hblk, hsig 01～hblk, hblk 10～hsig, hsig 11～hsig, hblk

address	Register name	Defaults	read/write	description
0x3309	SENSOR_REG09	8'h28	RW	Bit [7]: r_rblue_pol Bit [6]: pre-pre-charge enable for short exposure Bit [5]: auto rstyz go low enable 1~rstyz go low when finish readout of one data line 0~rstyz go low control by 0x3712,0x3713 Bit [4]: RESERVED Bit [3]: adclk gate enable when rstyz is low Bit [2]: RESERVED Bit [1]: hsig always low Bit [0]: hblk always low
0x330a	SENSOR_REG0A	8'h00	RW	Bit [7]: tx always high Bit [6]: y_addr_o change delay one cycle Bit [5]: dkblc Bit [4]: rst keep low when sample Bit [3]: bitsw_pol Bit [2]: cbar Bit [1]: ptest Bit [0]: rst keep low after sample
0x330b	SENSOR_REG0B	8'h11	RW	Bit [7: 4]: prsdip Bit [3]: noxlckb Bit [2: 0]: srsdip

address	Register name	Defaults	read/write	description
0x330c	SENSOR_REG0C	8'h07	RW	Bit [7]: short_first_man_en Bit [6]: short_first_man Bit [5]: sa1en will go low between 2 samples Bit [4]: old fexp enable Bit [3]: btsw will go low between 2 samples Bit [2]: sa1_off_en Bit [1]: holdbs1_en Bit [0]: holdbs0_en
0x330d	SENSOR_REG0D	8'h00	RW	Bit [7]: array rblue fix Bit [6]: prs all high Bit [5]: prs all low Bit [4]: rstgolow when pchg Bit [3]: sa1en all high Bit [2]: sa1en all low Bit [1]: eq all high Bit [0]: eq1 all low
0x330e	SENSOR_REG0E	8'h00	RW	RESERVED
0x330f	SENSOR_REG0F	8'h40	RW	RESERVED
0x3310	SENSOR_REG10	8'h23	RW	Bit [4]: r_tx_same_width Bit [3: 0]: short ppchg lines
0x3312	SENSOR_RSTYZ_GOLOW	8'h00	RW	rstyz_golow [15: 8]
0x3313	SENSOR_RSTYZ_GOLOW	8'h20	RW	Bit [7: 0]: rstyz_golow [7: 0] Bit [0]: holdb_pol
0x3314	SENSOR_EQ_GOLOW	8'h08	RW	Eq go low

address	Register name	Defaults	read/write	description
0x3315	SENSOR_REG15	8'h04	RW	Bit [7]: btsw high sel 1~tc_cs = r_bl_hi 0~xlckb when sample Bit [6]: btsw fix enable Bit [5]: ck_ap delay one cycle go high Bit [4]: ck_ap delay one cycle go low Bit [3]: hld_pol Bit [2]: short pchg TX signal will go high when non-hdr mode Bit [1]: short sample TX signal will go high when non-hdr mode Bit [0]: short hold signal will go high when non-hdr mode
0x3316	SENSOR_STROBE_CTRL	8'h03	RW	Bit [2]: aec frame reverse Bit [1]: shadow canceling 1 line strobe mode Bit [0]: shadow cancel auto mode enable
0x3317	SENSOR_STROBE_WIDTH	8'h01	RW	Bit [7]: r_neg_vblankp1_sel Bit [3: 0]: r_stb_w
0x3318	SENSOR_STB_ST_MAN	8'h00	RW	Bit [7: 0]: shadow cancel manual strobe start line, high byte
0x3319	SENSOR_STB_ST_MAN	8'h00	RW	Bit [7: 0]: shadow cancel manual strobe start line, low byte

address	Register name	Defaults	read/write	description
0x331a	SENSOR_STB_END_MAN	8'h01	RW	Bit [7: 0]: shadow cancel manual strobe end line, high byte
0x331b	SENSOR_STB_END_MAN	8'h01	RW	Bit [7: 0]: shadow cancel manual strobe end line, low byte
0x331c	SENSOR_CTRL1C	8'h00	RW	
0x331d	SENSOR_BITSW_HI	8'h00	RW	Bit [7: 0]: bitsw_gohi [7: 0] Bit [1]: holdb enable when hsig Bit [0]: holdb enable when hblk
0x331e	SENSOR_TXWIDTH	8'h7a	RW	tx width_pchg
0x3331	SENSOR_CTRL31	8'h48	RW	Bit [7: 5]: r_blc_border_row_num Bit [4: 0]: r_blc_read_num
0x3332	SENSOR_CTRL32	8'hb8	RW	Bit [7]: r_yadd_adj_en Bit [6]: r_yadd_vflip_en Bit [5]: r_yadd_fpn_vflip_en Bit [4]: r_yadd_blc_vflip_en Bit [3: 0]: r_fpn_real_num
0x3340	SENSOR_STB_OK_START	8'h00	RO	high byte of good start line of shadow cancelling strobe
0x3341	SENSOR_STB_OK_START	8'h00	RO	low byte of good start line of shadow cancelling strobe
0x3342	SENSOR_STB_OK_END	8'h00	RO	high byte of good end line of shadow cancelling strobe
0x3343	SENSOR_STB_OK_END	8'h00	RO	low byte of good end line of shadow cancelling strobe

address	Register name	Defaults	read/write	description
0x3344	SENSOR_STB_EXP_WIDTH	8'h00	RO	high byte of shadow cancelling strobe width for each line
0x3345	SENSOR_STB_EXP_WIDTH	8'h00	RO	low byte of shadow cancelling strobe width for each line
0x3348	SENSOR_CTRL48	8'h00	RO	chip debug
0x3349	SENSOR_CTRL49	8'h00	RO	chip debug
0x334a	SENSOR_CTRL4A	8'h00	RO	chip debug
0x334b	SENSOR_CTRL4B	8'h00	RO	chip debug
0x334c	SENSOR_CTRL4C	8'h00	RO	chip debug
0x334d	SENSOR_CTRL4D	8'h00	RO	chip debug
0x334e	SENSOR_CTRL4E	8'h00	RO	chip debug
0x334f	SENSOR_CTRL4F	8'h00	RO	chip debug

5.9 TIMING CTRL

table5-9 TIMING_CTRLControl register

address	Register name	Defaults	read/write	description
0x3200	TIMING_X_START_ADDR	8'h00	RW	high byte of horizontal start address of ARRAY for readout
0x3201	TIMING_X_START_ADDR	8'h00	RW	low byte of horizontal start address of ARRAY for readout
0x3202	TIMING_Y_START_ADDR	8'h00	RW	high byte of vertical start address of ARRAY for readout
0x3203	TIMING_Y_START_ADDR	8'h00	RW	low byte of vertical start address of ARRAY for readout

address	Register name	Defaults	read/write	description
0x3204	TIMING_X_END_ADDR	8'h05	RW	high byte of horizontal end address of ARRAY for readout
0x3205	TIMING_X_END_ADDR	8'h67	RW	low byte of horizontal end address of ARRAY for readout
0x3206	TIMING_Y_END_ADDR	8'h03	RW	high byte of vertical end address of ARRAY for readout
0x3207	TIMING_Y_END_ADDR	8'hcf	RW	low byte of vertical end address of ARRAY for readout
0x3208	TIMING_X_OUTPUT_SIZE	8'h05	RW	high byte of DVP horizontal output size (pixel)
0x3209	TIMING_X_OUTPUT_SIZE	8'h00	RW	low byte of DVP horizontal output size (pixel)
0x320a	TIMING_Y_OUTPUT_SIZE	8'h03	RW	high byte of DVP vertical output size (pixel)
0x320b	TIMING_Y_OUTPUT_SIZE	8'he3	RW	low byte of DVP vertical output size (pixel)
0x320c	TIMING_HTS	8'h07	RW	high byte of horizontal total size
0x320d	TIMING_HTS	8'he0	RW	low byte of horizontal total size
0x320e	TIMING_VTS	8'h04	RW	high byte of vertical total size
0x320f	TIMING_VTS	8'h38	RW	low byte of vertical total size
0x3210	TIMING_HOFFS	8'h00	RW	high byte of win_hoffs
0x3211	TIMING_HOFFS	8'h10	RW	low byte of win_hoffs
0x3212	TIMING_VOFFS	8'h00	RW	high byte of win_voffs
0x3213	TIMING_VOFFS	8'h02	RW	low byte of win_voffs

address	Register name	Defaults	read/write	description
0x3215	TIMING_CTRL15	8'h80	RW	Bit [7]: black line href enable Bit [6]: FSIN interrupt enable Bit [5]: rip sof enable Bit [4]: horizontal crop manual enable Bit [2]: r_vts_double_opt_en Bit [1]: r_vts_double_en Bit [0]: r_vts_double_change_sel 1~asp_rd 0~tc_cs == 1 && tc_r == 0
0x3216	TIMING_CTRL16	8'h1a	RW	black lines number
0x3217	TIMING_CTRL17	8'h00	RW	Bit [7: 4]: tc_sof vertical start line number
0x3219	TIMING_CTRL19	8'h00	RW	
0x321c	TIMING_CTRL1C	8'h00	RW	Bit [7]: vflip to digital Bit [6]: vflip in array Bit [1]: vsub4 Bit [0]: vsub2
0x321d	TIMING_CTRL1D	8'h00	RW	Bit [7]: vflip black line Bit [6]: hdr_en Bit [1]: mirror to digital Bit [0]: mirror to array
0x321e	REGVS	8'h00	RW	high byte of the vref1 start row
0x321f	REGVS	8'h1a	RW	low byte of the vref1 start row

address	Register name	Defaults	read/write	description
0x3220	CORE_CTRL3	8'h00	RW	Bit [7]: r_debug_sof_sel 0～data_pre_sof 1～tc_sof_blc Bit [6]: r_dvp_href_in_sel 0～use normal rows 1～use href from dvp_pre that remove four rows Bit [5]: r_dvp_hsub2_man_en Bit [4]: r_f5060_sel Bit [3]: r_dvp_eof_sel 0～eof from isp 1～eof from dvp_pre Bit [2]: r_adclk1_neg_sel Bit [1]: r_adclk_inv Bit [0]: r_dvp_hsub2_man
0x3221	CORE_CTRL2	8'h01	RW	Bit [6: 3]: r_fine_gain_man Bit [2]: r_fine_gain_man_en Bit [1]: r_aec_agc_change Bit [0]: r_sa1_off_s [4]
0x3222	CORE_CTRL1	8'h00	RW	Bit [7: 4]: r_sa1_off_s [3: 0] Bit [3: 0]: r_sa1_off_l [4: 1]
0x3223	CORE_CTRL0	8'h02	RW	Bit [7]: r_sa1_off_l [0] Bit [2]: r_fmt_change for blc Bit [0]: fexp_sel for sensor ctrl
0x3232	TIMING_TC_CS_RST	8'h00	RW	timing control horizontal counter reset value, high byte

address	Register name	Defaults	read/write	description
0x3233	TIMING_TC_CS_RST	8'h00	RW	timing control horizontal counter reset value, low byte
0x3234	TIMING_TC_R_RST	8'h00	RW	timing control vertical counter reset value (vts-tc_r_rst), high byte
0x3235	TIMING_TC_R_RST	8'h00	RW	timing control vertical counter reset value (vts-tc_r_rst), low byte
0x3240	TIMING_TC_P_CNT	8'h00	RO	timing control pixel counter high byte
0x3241	TIMING_TC_P_CNT	8'h00	RO	timing control pixel counter low byte
0x3242	TIMING_TC_R_CNT	8'h00	RO	timing control line counter high byte
0x3243	TIMING_TC_R_CNT	8'h00	RO	timing control line counter low byte
0x3244	TIMING_GRP_STS	8'h00	RO	Bit [3]: group 3 hit, can be written to 0 Bit [2]: group 2 hit, can be written to 0 Bit [1]: group 1 hit, can be written to 0 Bit [0]: group 0 hit, can be written to 0
0x3248	TIMING_FRAME_CNT	8'h00	RO	timing control frame counter high byte

address	Register name	Defaults	read/write	description
0x3249	TIMING_FRAME_CNT	8'h00	RO	timing control frame counter low byte

5.10 BLC

table5-10 BLCControl register

address	Register name	Defaults	read/write	description
0x3209	BLC_CTRL00	8'h05	RW	Bit [3]: blackline_avg_frame Bit [2]: adc_11bit_mode Bit [1]: apply2blackline Bit [0]: blc_enable
0x3901	BLC_CTRL01	8'h00	RW	Bit [5: 0]: blc_start_line [5: 0]
0x3902	BLC_CTRL02	8'h45	RW	Bit [7]: format_change_en format_change_i from fmt will be effect when it is enable Bit [6]: blc_auto_en Bit [5: 0]: reset_frame_num
0x3903	BLC_CTRL03	8'h08	RW	Bit [7]: blc_redo_en 1~ trigger a blc redo N frames begin Bit [6]: freeze_enable Bit [5: 0]: manual_frame_num
0x3904	BLC_CTRL04	8'h08	RW	Bit [5: 0]: blc_line_num

address	Register name	Defaults	read/write	description
0x3905	BLC_CTRL05	8'h18	RW	Bit [7]: RESERVED Bit [6]: one_channel Bit [5]: one_line_mode Bit [4]: remove_none_imagedata Bit [3]: blc_man_1_en Bit [2]: blackline_bggr_man_en 1~bgbg / grgr fix 0~bgbg / gtgr is decided by rblue / hswap Bit [1]: blc_always_up_en 1~blc always update 0~normal freeze Bit [0]: agc_change_from_sys

address	Register name	Defaults	read/write	description
0x3906	BLC_CTRL06	8'h02	RW	Bit [7: 5]: RESERVED Bit [4: 3]: win_sel 00～full image 01～a window do not contain the first 16 pixels and the end 16 pixels 10～a window do not contain the first 1/16 image and the end 1 / 16image 11～a window do not contain the first 1/8 image and the end 1/8 image Bit [2: 0]: bypass_mode 000～bypass data_i after limit bits 001～bypass data_i [11: 0] 010～bypass data_i [12: 1] 011～bypass debug data bbrr 100～bypass debug data gggg
0x3907	TARGET	8'h00	RW	high byte of target
0x3908	TARGET	8'h40	RW	low byte of target
0x3909	BLC_MANUAL00	8'h00	RW	high byte of blc_manual00
0x390a	BLC_MANUAL00	8'h00	RW	low byte of blc_manual00
0x390b	BLC_MANUAL01	8'h00	RW	high byte of blc_manual01
0x390c	BLC_MANUAL01	8'h00	RW	low byte of blc_manual01
0x390d	BLC_MANUAL02	8'h00	RW	high byte of blc_manual02

address	Register name	Defaults	read/write	description
0x390e	BLC_MANUAL02	8'h00	RW	low byte of blc_manual02
0x390f	BLC_MANUAL03	8'h00	RW	high byte of blc_manual03
0x3910	BLC_MANUAL03	8'h00	RW	low byte of blc_manual03
0x3911	BLC_LEVEL00	-	RO	high byte of blc_level00
0x3912	BLC_LEVEL00	-	RO	low byte of blc_level00
0x3913	BLC_LEVEL01	-	RO	high byte of blc_level01
0x3914	BLC_LEVEL01	-	RO	low byte of blc_level01
0x3915	BLC_LEVEL10	-	RO	high byte of blc_level10
0x3916	BLC_LEVEL10	-	RO	low byte of blc_level10
0x3917	BLC_LEVEL11	-	RO	high byte of blc_level11
0x3918	BLC_LEVEL11	-	RO	low byte of blc_level11
0x391b	BLC_MAX	8'hff	RW	blc_man [7: 0]
0x391c	BLC_CTRL1C	8'h8f	RW	Bit [7]: stable_range_en Bit [6: 0]: stable_range if offset difference of two frames out of the stable range blc will work
0x391d	BLC_CTRL1D	8'h00	RW	Bit [7]: hswap_sync Bit [6]: hswap_blc Bit [5]: mirror_man_en Bit [4]: mirror_man Bit [3]: RESERVED Bit [2]: r_col_13_exchange_1 Bit [1]: r_col_02_exchange_1 Bit [0]: r_col_01_exchange_1

address	Register name	Defaults	read/write	description
0x391e	BLC_CTRL1E	8'h00	RW	Bit [7: 5]: RESERVED Bit [4]: hswap_sync_2 Bit [3]: RESERVED Bit [2]: r_col_13_exchange_2 Bit [1]: r_col_02_exchange_2 Bit [0]: r_col_01_exchange_2
0x3920	BLC_MANUAL10	8'h00	RW	high byte of blc_manual10
0x3921	BLC_MANUAL10	8'h00	RW	low byte of blc_manual10
0x3922	BLC_MANUAL11	8'h00	RW	high byte of blc_manual11
0x3923	BLC_MANUAL11	8'h00	RW	low byte of blc_manual11
0x3924	BLC_MANUAL12	8'h00	RW	high byte of blc_manual12
0x3925	BLC_MANUAL12	8'h00	RW	low byte of blc_manual12
0x3926	BLC_MANUAL13	8'h00	RW	high byte of blc_manual13
0x3927	BLC_MANUAL13	8'h00	RW	low byte of blc_manual13
0x3928	BLC_CTRL28	8'h01	RW	Bit [0]: r_blc_4channel_en
0x3929	BLC_LEVEL02	-	RO	high byte of blc_level02
0x392a	BLC_LEVEL02	-	RO	low byte of blc_level02
0x392b	BLC_LEVEL03	-	RO	high byte of blc_level03
0x392c	BLC_LEVEL03	-	RO	low byte of blc_level03
0x392d	BLC_LEVEL12	-	RO	high byte of blc_level12
0x392e	BLC_LEVEL12	-	RO	low byte of blc_level12
0x392f	BLC_LEVEL13	-	RO	high byte of blc_level13
0x3930	BLC_LEVEL13	-	RO	low byte of blc_level13

5.11 RNC

table5-11 RNCControl register

address	Register name	Defaults	read/write	description
0x3400	RNC_CTRL00	8'h05	RW	Bit [7]: hswap Bit [6]: r_blacklevel_on_channel Bit [5]: r_one_channel Bit [4]: r_remove_none_imagedata Bit [3]: r_apply2blackline Bit [2]: r_rnc_man_1_en Bit [1]: r_rnc_auto_en Bit [0]: r_rnc_en
0x3401	RNC_CTRL01	8'h07	RW	Bit [7: 6]: r_rnc_bypass_mode 00~ data_i [IM_DW-2: 0] do not care the high bit data_i [IM_DW-1]: data_i [IM_DW-1: 1] Bit [5]: dkc_channel_gain_en Bit [4]: dkc_blc_en Bit [3]: dkc_f_en_o Bit [2]: r_8channel Bit [1]: r_rnc_offset_sign Bit [0]: r_darkrow_f_auto
0x3402	RNC_CTRL02	8'h00	RW	r_rnc_start_col
0x3403	RNC_CTRL03	8'h40	RW	r_rnc_col_num

address	Register name	Defaults	read/write	description
0x3404	RNC_CTRL04	8'h00	RW	r_rnc_man00 [7: 0]
0x3405	RNC_CTRL05	8'h00	RW	Bit [4: 0]: r_rnc_man00 [12: 8]
0x3406	RNC_CTRL06	8'h00	RW	r_rnc_man01 [7: 0]
0x3407	RNC_CTRL07	8'h00	RW	Bit [4: 0]: r_rnc_man01 [12: 8]
0x3408	RNC_CTRL08	8'h00	RW	r_rnc_man02 [7: 0]
0x3409	RNC_CTRL09	8'h00	RW	Bit [4: 0]: r_rnc_man02 [12: 8]
0x340a	RNC_CTRL0A	8'h00	RW	r_rnc_man03 [7: 0]
0x340b	RNC_CTRL0B	8'h00	RW	Bit [4: 0]: r_rnc_man03 [12: 8]
0x340c	RNC_CTRL0C	8'h00	RW	r_rnc_man10 [7: 0]
0x340d	RNC_CTRL0D	8'h00	RW	Bit [4: 0]: r_rnc_man10 [12: 8]
0x340e	RNC_CTRL0E	8'h00	RW	r_rnc_man11 [7: 0]
0x340f	RNC_CTRL0F	8'h00	RW	Bit [4: 0]: r_rnc_man11 [12: 8]
0x3410	RNC_CTRL10	8'h00	RW	r_rnc_man12 [7: 0]
0x3411	RNC_CTRL11	8'h00	RW	Bit [4: 0]: r_rnc_man12 [12: 8]
0x3412	RNC_CTRL12	8'h00	RW	r_rnc_man13 [7: 0]
0x3413	RNC_CTRL13	8'h00	RW	Bit [4: 0]: r_rnc_man13 [12: 8]
0x3414	RNC_CTRL14	8'h00	RW	r_rnc_offset [7: 0]
0x3415	RNC_CTRL15	8'h00	RW	Bit [6: 4]: r_blacklevel_man [10: 8] Bit [2: 0]: r_rnc_offset [10: 8]
0x3416	RNC_CTRL16	8'hc0	RW	r_blacklevel_man [7: 0]

5.12 ISP PRE

table5-12 ISP PREControl register

address	Register name	Defaults	read/write	description
0x503d	ISP_CTRL61	8'h00	RW	Bit [7]: color bar test pattern enable 0~disable 1~enable Bit [6]: dmy_half Bit [5: 4]: color bar style Bit [3]: dmy_man Bit [2]: rolling Bit [1]: isp_test Bit [0]: squ_size
0x503e	ISP_CTRL62	8'h00	RW	Bit [6: 4]: rnd_seed Bit [3]: squ_bw Bit [2]: trans Bit [1: 0]: test_sel
0x5054	ISP_CTRL63	8'h92	RW	Bit [7]: r_vsize_in_sel 1: select calculate result 0: normal value Bit [6: 0]: r_fpn_num The number of fpn to calculate vsize

5.13 LENC

table5-13 LENCControl register

address	Register name	Defaults	read/write	description
0x5000	ISP_CTRL00	8'h99	RW	Bit [7]: LENC correction enable 0 ~ disable 1 ~ enable
0x5800	LENC_CTRL00	8'h90	RW	Bit [6]: no_delay 1 ~ sel data_i do lenc 0 ~ data_3d do lenc Bit [5]: debug mode Bit [4]: lenc_bias_en 1 ~ sub bias before do lenc 0 ~ use data_i do lenc Bit [1]: sel deltagain Bit [0]: sel_ra, if lenc enable select test mode
0x5801	LENC_RADIUS	8'h20	RW	Bit [7: 0]: lenc_radius
0x5802	LENC_XOFFSET	8'h20	RW	Bit [7: 0]: the horizontal start size
0x5803	LENC_YOFFSET	8'h10	RW	Bit [7: 0]: the vertical start size
0x5804	LENC_RGAIN	8'h80	RW	Bit [7: 0]: red color coefficient
0x5805	LENC_GGAIN	8'h80	RW	Bit [7: 0]: green color coefficient
0x5806	LENC_BGAIN	8'h80	RW	Bit [7: 0]: blue color coefficient

address	Register name	Defaults	read/write	description
0x5807	LENC_CTRL07	8'h00	RW	Bit [7]: xy_offset_man_en Bit [5]: hskip_man_en Bit [4]: vskip_man_en Bit [3: 2]: r_hskip Bit [1: 0]: r_vskip
0x5808	LENC_XCNT	8'h2	RW	Bit [7: 2]: RESERVED Bit [1: 0]: xcnt [9: 8] horizontal center
0x5809	LENC_XCNT	8'h8a	RW	Bit [7: 0]: xcnt [7: 0]
0x580a	LENC_YCNT	8'h1	RW	Bit [7: 2]: RESERVED Bit [1: 0]: ycnt [9: 8] vertical center
0x580b	LENC_YCNT	8'hf0	RW	Bit [7: 0]: ycnt [7: 0]

5.14 AWB

table5-14 AWBControl register

address	Register name	Defaults	read/write	description
0x5000	ISP_CTRL00	8'h99	RW	Bit [3]: awb_gain_en Bit [0]: auto white balance enable 0 ~ disable 1 ~ enable
0x5180	AWB_CTRL00	8'h04	RW	Bit [7: 0]: stable_range
0x5181	AWB_CTRL01	8'h8	RW	Bit [7: 6]: stable_range
8x5182	AWB_CTRL02	8'h0	RW	Bit [0]: gain_man_en

5.15 DPC ONED

□ 5-15 DPC ONED □□□□□

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0x5000	ISP_CTRL00	8’h99	RW	Bit [2]: wc_en white pixel cancellation Bit [1]: bc_en black pixel cancellation

5.16 WINDOW

□ 5-16 WINDOW □□□□□

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0x5700	WINDOW_XSTART	8'h00	RW	Bit [7: 4]: RESERVED Bit [3: 0]: r_x_start [11: 8] horizontal start position for window
0x5701	WINDOW_XSTART	8’h00	RW	Bit [7: 0]: r_x_start [7: 0] horizontal start position for window
0x5702	WINDOW_YSTART	8’h00	RW	Bit[7:4]: RESERVED Bit [3: 0]: r_y_start [11: 8] vertical start position for window
0x5703	WINDOW_YSTART	8’h00	RW	Bit [7: 0]: r_y_start [7: 0] vertical start position for window
0x5704	WINDOW_WIDTH	8'h03	RW	Bit[7:4]: RESERVED Bit [3: 0]: r_win_width [11: 8] the width for window

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0x5705	WINDOW_WIDTH	8'h20	RW	Bit [7: 0]: r_ win_width [7: 0] the width for window
0x5706	WINDOW_HEIGHT	8'h02	RW	Bit[7:4]: RESERVED Bit [3: 0]: r_win_height [11: 8] the height for window
0x5707	WINDOW_HEIGHT	8'h5c	RW	Bit [7: 0]: r_ win_ height [7: 0] the height for window
0x5708	WINDOW_MAN_EN	8’h00	RW	Bit [0]: win_man_en

5.17 VAR

□ 5-17 VAR □□□□□

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0x5000	ISP_CTRL00	8’h99	RW	Bit [4]: var_en
0x5900	VAR_CTRL00	8'h01	RW	Bit [7]: b_avg_en Bit [6]: gb_avg_en Bit [5]: gr_avg_en Bit [4]: r_avg_en Bit [3]: debug_en Bit [2]: single_channel bypass Bit [1: 0]: addopt
0x5901	VAR_CTRL01	8’h0	RW	Bit [3: 2]: hskip Bit[1:0]: vskip

5.18 YAVG

□ 5-18 YAVG □□□□□

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0x5680	AVG_XSTART	8'h00	RW	Bit[7:4]: RESERVED Bit [3: 0]: r_avg x start [11: 8] horizontal start position for average window
0x5681	AVG_XSTART	8'h00	RW	Bit [7: 0]: r_avg x start [11: 8] horizontal start position for average window
0x5682	AVG_YSTART	8'h00	RW	Bit[7:4]: RESERVED Bit [3: 0]: r_avg y start [11: 8] vertical start position for average window
0x5683	AVG_YSTART	8'h00	RW	Bit [7: 0]: r_avg y start [11: 8] vertical start position for average window
0x5684	AVG_WIN_WIDTH	8'h10	RW	Bit[7:4]: RESERVED Bit[3:0]: r_win_width[11:8] the width for average window
0x5685	AVG_WIN_WIDTH	8'ha0	RW	Bit [7: 0]: r_win_width [7: 0] the width for average window
0x5686	AVG_WIN_HEIGHT	8'h0c	RW	Bit[7:4]: RESERVED Bit[3:0]: r_win_height[11:8] the height for average window

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0x5687	AVG_WIN_HEIGHT	8'h67	RW	Bit [7: 0]: r_win_height [7: 0] the height for average window
0x5688	AVG_CTRL08	8'h2	RW	Bit [1]: avg_opt Bit [0]: win_man

5.19 DATA PRE

□ 5-19 DATA PRE □□□□□

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0x3f00	DATA_PRE_CTRL00	8’h00	RW	Bit [7: 3]: RESERVED Bit [2]: the switch of hsub_i Bit [1]: pclk inv en 1～enable 0～disable Bit [0]: data_pre en 1～enable 0～disable
0x3f01	DATA_PRE_CTRL01	8’h00	RW	RESERVED

5.20 DVP PRE

□ 5-20 DVP PRE □□□□□

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0x3f80	DVP_PRE_CTRL00	8’h00	RW	Bit [7]: r_hsync_sel Bit [6]: r_hsync_mod Bit [5: 4]: r_first_sel Bit [1]: r_hsync_sel2 Bit [0]: r_dvp_pre_en 1~enable 0~disable
0x3f81	DVP_PRE_CTRL01	8'h06	RW	Bit [7: 0]: r_hsync_st length of hsync posedge to href posedge
0x3f82	DVP_PRE_CTRL02	8’h06	RW	Bit [7: 0]: r_hsync_ed length of href negedge to hsync negedge
0x3f83	DVP_PRE_CTRL03	8'h30	RW	Bit [7: 0]: r_eof_dly length of eof posedge to href negedge

5.21 DVP

□ 5-21 DVP □□□□□

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0x3d00	DVP_MOD_SEL	8'h04	RW	Bit[7:4]: RESERVED Bit [3]: CCIR v select Bit [2]: CCIR f select Bit [1]: CCIR565 mode enable Bit [0]: HSYNC mode enable
0x3d01	DVP_VSYNC_WIDTH	8'h00	RW	VSYNC length, line count
0x3d02	DVP_HSYNVSY_ NEG_WIDTH	8'h00	RW	VSYNC length, pixel count high byte
0x3d03	DVP_HSYNVSY_ NEG_WIDTH	8'h01	RW	VSYNC length, pixel count low byte
0x3d04	DVP_VSYNC_MOD	8'h00	RW	Bit[7:4]: RESERVED Bit [3: 2]: r_vsyncout_sel Bit [1]: r_vsync3_mod Bit [0]: r_vsync2_mod
0x3d05	DVP_EOF_VSYNC_ DELAY	8'h00	RW	SOF / EOF negative edge to vsync positive edge high byte
0x3d06	DVP_EOF_VSYNC_ DELAY	8'h00	RW	SOF/EOF negative edge to vsync positive edge middle byte
0x3d07	DVP_EOF_VSYNC_ DELAY	8'h00	RW	SOF/EOF negative edge to vsync positive edge low byte

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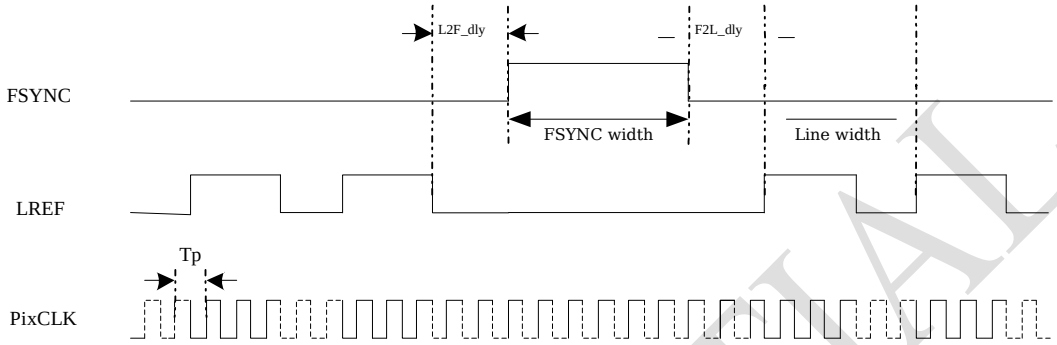
0x3d08	DVP_POL_CTRL	8'h01	RW	Bit [7]: CLK DDR mode enable Bit [6]: RESERVED Bit [5]: VSYNC gate clock enable Bit [4]: HREF gate clock enable Bit [3]: No first for FIFO Bit [2]: HREF polarity Bit [1]: VSYNC polarity Bit [0]: PCLK polarity / PCLK gate low enable
0x3d09	DVP_MOTO_ORDER	8'h00	RW	Bit [7]: fifo_bypass_mode Bit [6: 4]: data bit swap Bit [3]: bit test mode Bit [2]: bit test 10-bit Bit [1]: bit test 8-bit Bit [0]: bit test enable
0x3d0a	DVP_CTRL0A	8'h00	RW	Bit [4]: href_sel 1～hsync 0～href Bit [3: 0]: byp_sel for debug mode Bit [3]: debug mode en Bit [2: 0]: debug mode sel

6 Image sensor data output format and timing

SC1035Provides parallel video port(DVP), Output 10-bit Parallel data. Wherein each FSYNCpulse Red signal indicates the start of a new data.



Map6-1 DVPTiming

Note1:usually, L2F_dlyIt represents the last video cable falling FSYNCBetween the rising edge of the delay; F2L_dlyShowFSYNCFalling to between the first rising edge of the video SYNC Delay,default is a width Width of the video cable; a default width of the video line(Pixel clock cycle).

2: The above parameters can be modified by the register.

7 Electrical parameters

□ 7-1 Maximum Ratings

project	symbol	Ratings	unit	Remark
voltage (simulation 3.3V)	AVDD	4.5 -0.3 ~	V	
□□□□ (interface 3.3V □	DOVDD	-0.3~4.5	V	
□□□□ (digital 1.5V □	DVDD	2.0 -0.3 ~	V	
Input voltage		-0.3 ~ DOVDD + 0.3	V	
The output voltage		-0.3~DOVDD+0.3	V	
Operating temperature		-40 ~ + 85	ºC	
Storage temperature		-50 ~ + 120	ºC	
Performance guarantee temperature		-10 ~ + 65	ºC	

□ 7-2 DC Electrical Characteristics

□□	□□	Min	Typical values	Max	□□
power supply					
Supply voltage □□□ 3.3V □	AVDD	3.14	3.3	3.47	V
□□□□ □□□ 3.3V □	DOVDD	1.7	3.3	3.47	V
□□□□ □□□ 1.5V □	DVDD	1.43	1.5	1.57	V

□□	□□	□□□	□□□	□□□	□□
Effective current (Analog power)	I_{DD-A}	-	40	60	mA
A small current (IOpower supply)	I_{DD-IO}	—	30	45	mA
Digital input(Typical conditions: AVDD = 3.3V,DOVDD = 1.8 ~ 3.3V)					
Input low	V_{IL}	—	—	0.3×DOVDD	V
Input High	V_{IH}	0.7×DOVDD	—	—	V
Input capacitance	C_{IN}	—	—	10	pF
Digital Output(25pFStandard load)					
Output high	V_{OH}	0.9×DOVDD	—	—	V
Output low	V_{OL}	—	—	0.1×DOVDD	V
Serial interface input					
SCLandSDA □□□□□	V_{IL}	-0.5	0	0.3×DOVDD	V
SCL □ SDA □□□□□	V_{IH}	0.7×DOVDD	DOVDD	DOVDD + 0.5	V

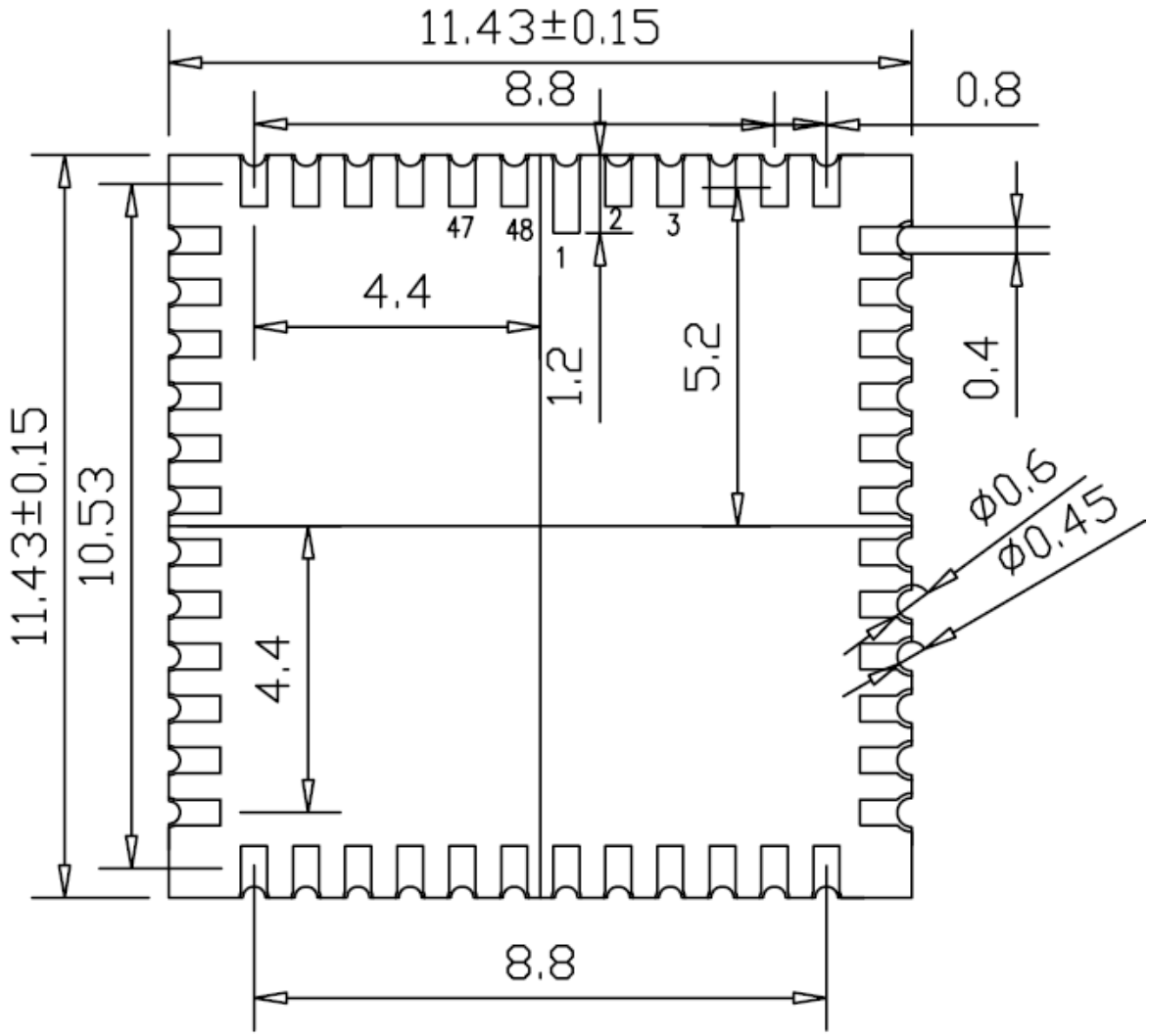
□ 7-3 AC Characteristics (TA = 25 ºC □ AVDD=3.3V □ DOVDD = 3.3V □

□□	□□	□□□	□□□	□□□	□□
AC parameters					
DC differential linearity error	DLE	—	<2	—	LSB
Soft reset setup time		—	—	1	ms
Change the resolution setting time		—	—	1	ms

□□	□□	□□□	□□□	□□□	□□
Configuration register set the time		—	—	300	ms
Oscillator and clock input					
Input clock frequency	F_{OSC}	—	6	—	MHz
Input clock rise /decline time		—	—	5	ns

8 Package

8.1 Package size



8-1 PLCC44Package Diagram (Unit: mm)

9 Optical parameters

9.1 Sensor array center

□ 9-1 □□□□□□□

□□	coordinate
Mold Center	(0,0)
Center of the array	(145μm, -105μm)

Note: The center of the array and the center of the package have a range of allowable error.

Version History

version	Explanation	chapter
1.0	initial version.	N / A
1.1	1.In the "key indicators" section to change the package types and package size. 2.change 表 1-1 为表 1-1The package information. 3.Update 表 8-1.	1.Change types of packages and key indicators. 2.Article1chapter. 3. 表 7 为表
1.2	1.increaseI2CInterface timing parameters(Table 2-3)and I2C Timing diagram(Figure 2-4)(表 2.Update application circuit. 3.Update package information. 4.for 表 9-1Annotated.	1. 表 2.4Section. 2. 表 2.2 为表 3. 表 1Chapter7 为表 4. 表 8 为表