DAC YF

PULSAR: QDI Synthesis Flow

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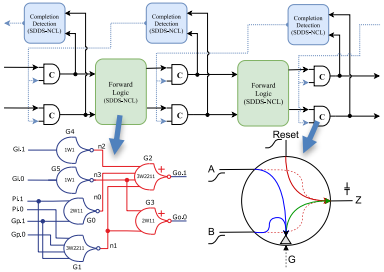
Introduction and Motivation

- Shift to asynchronous / GALS approaches
  - Clock/power domain crossing interconnection
- Quasi-delay-insensitive (QDI)
  - Resilient to variability, ageing, voltage scaling
- Specialised gates and EDA tools

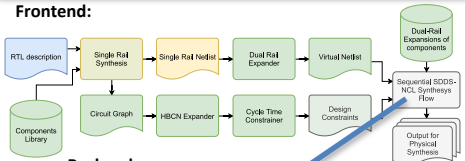
Pseudo-Synchronous SDDS-NCL

- Conventional synthesis tools (Cadence Genus)
- SDDS-NCL -> Combinational Logic
- Pseudo-Synchronous WCHB -> Sequential Logic

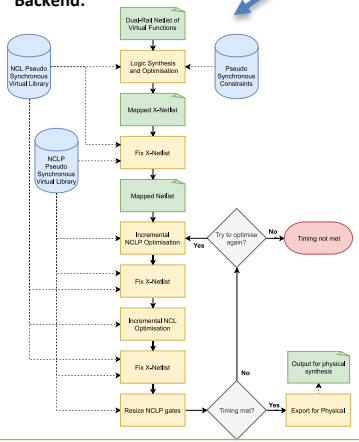


The Pulsar Flow

Frontend:

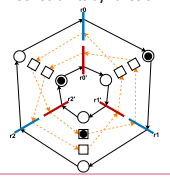


Backend:



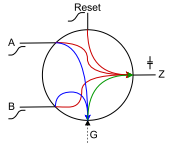
HBCN Timing Model

- Cycle time not obvious
- Constraints synthesis



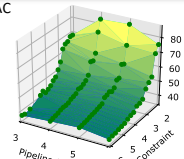
Pseudo-Latch

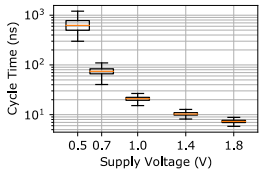
- Loop-Breakers for STA
- Original Arcs Preserved
- Delayed Simulation

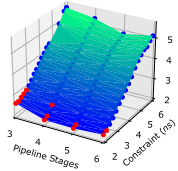


Experimental Results

- Results extracted from pipelined MAC
- Trade performance/area/power
- STA timing closure
  - Performance target
  - GALS applications
- Aggressive voltage-scaling
  - Circuit designed at 1.65v
  - Operates from 0.5v to 1.8v
- On-going silicon tape-out







References:

1. T. Moreira, M. P. A. Beerel, M. L. L. Sartori, and N. L. V. Calazans. **NCL Synthesis With Conventional EDA Tools: Technology Mapping and Optimization.** *ITCAS-I, 2018*
2. M. L. L. Sartori, R. N. Wuerdig, M. T. Moreira, and N. L. V. Calazans. **Pulsar: Constraining QDI Circuits Cycle Time Using Traditional EDA Tools.** *ASYNC, 2019*
3. M. L. L. Sartori, M. T. Moreira, and N. L. V. Calazans. **A Frontend using Traditional EDA Tools for the Pulsar QDI Design Flow**. *ASYNC, 2020*

Available at: https://github.com/marlls1989/pulsar