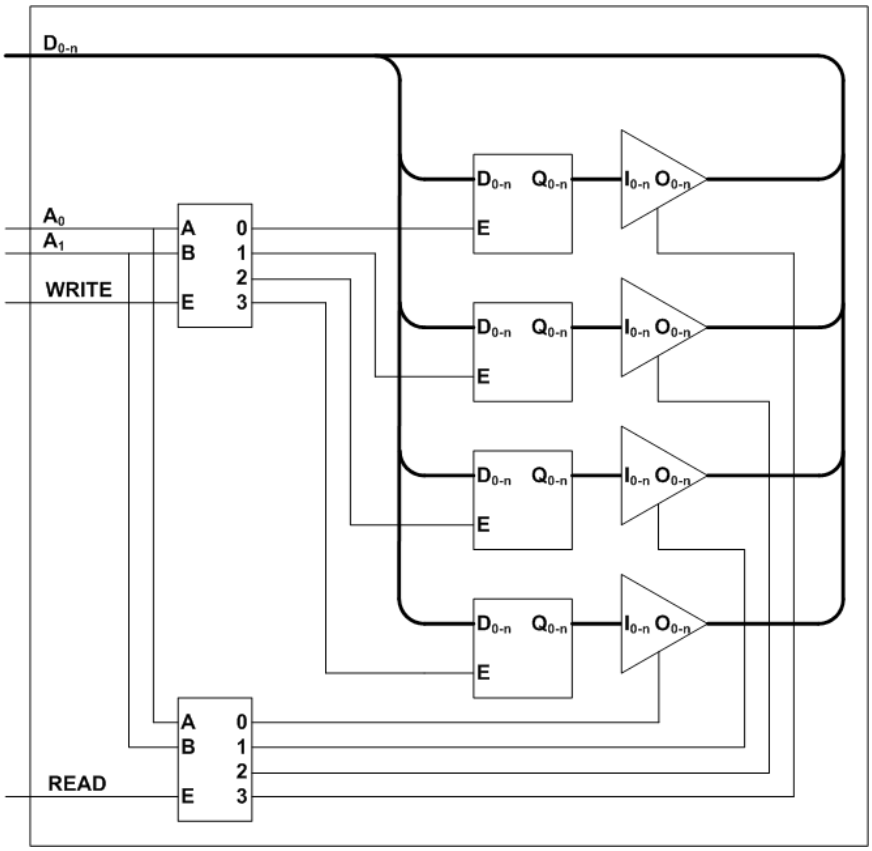
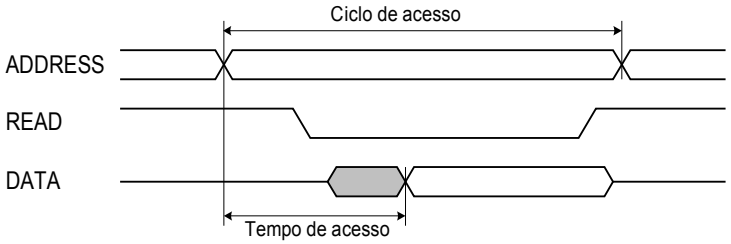
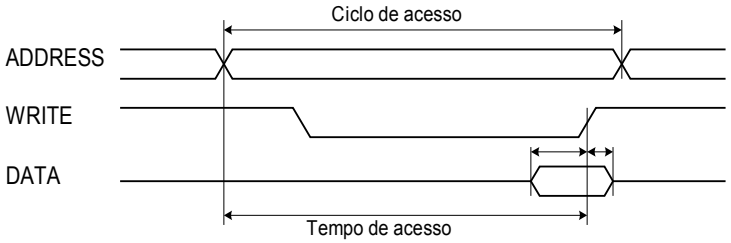
Memória estática

Modelo de construção interna

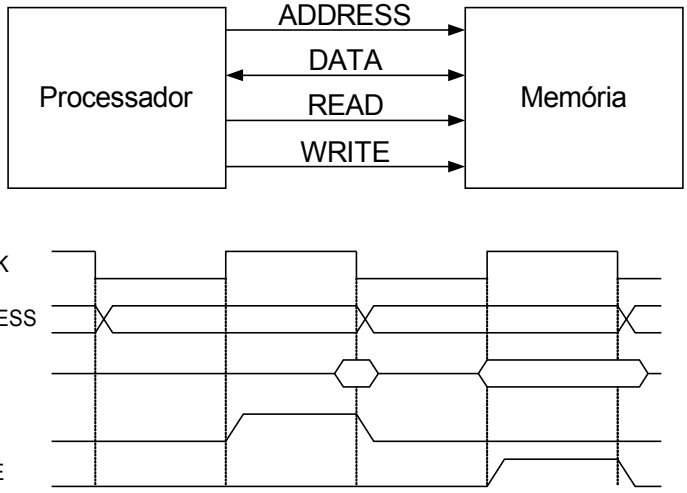


Ciclos de acesso

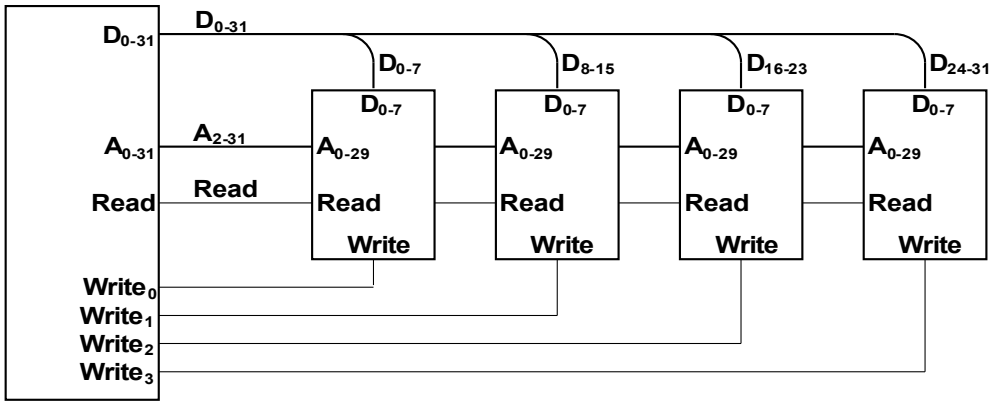




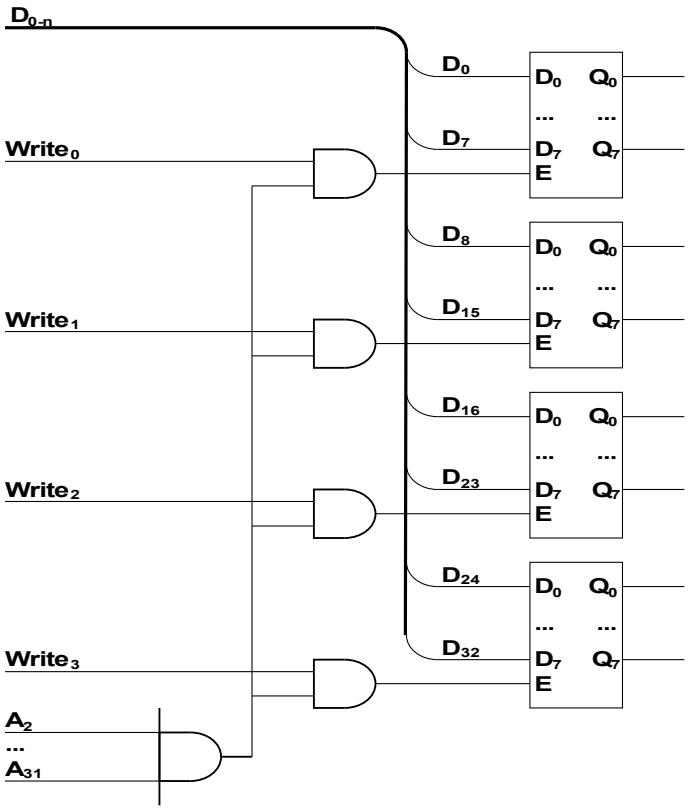
Modelo de interface processador memória



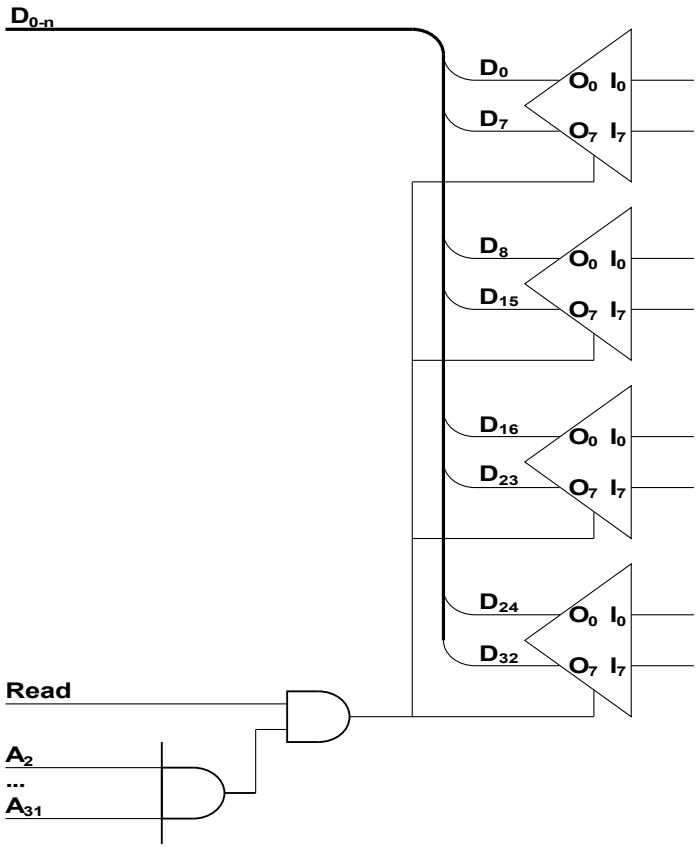
Organização da memória por bancos



Porto de saída



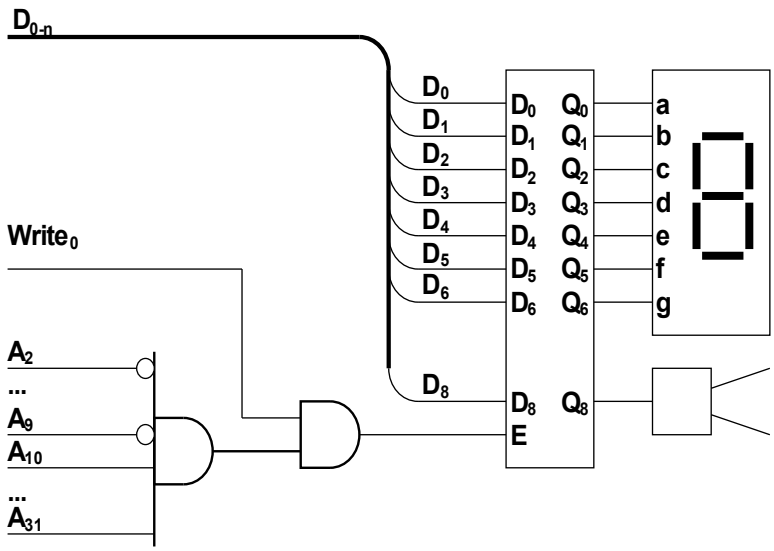
Porto de entrada



Exercício

Construir um porto de saída de 8 bits e ligar um *display* de 7 segmentos e um besouro. Considerar uma interface de processador com endereçamento ao nível do byte e com barramento de dados a 32 bits.

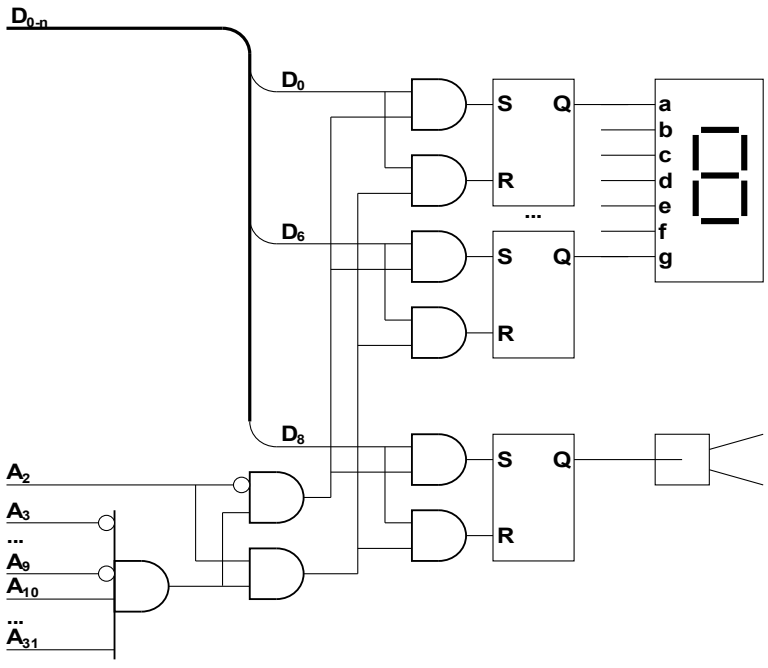
Solução com registadores do tipo D.




```
    .data
image:      .byte
table_7seg: .byte   0x3f,
0x4f
    .text
display_write:
    ldr     r1, =table_7seg
    ldr     r0, [r1, r0]
    ldr     r1, =image
    ldrb    r2, [r1]
    and     r2, r2, #0x80
    orr     r0, r0, r2
    strb    r0, [r1]
    ldr     r1, =0xfffffC00
    strb    r0, [r1]
    mov     pc, lr

buzzer_on_off:
    ldr     r1, =image
    ldrb    r2, [r1]
    and     r2, r2, #0x7f
    orr     r0, r2, lsl #7
    strb    r0, [r1]
    ldr     r1, =0xfffffC00
    strb    r0, [r1]
    mov     pc, lr
```

Solução com registadores do tipo S-R.




```
    .equ    SET, 0
    .equ    CLR, 1

display_write1:
    ldr     r1, =table_7seg
    ldr     r0, [r1, r0]
    ldr     r1, =0xfffffC00
    mov     r2, #0x7f
    strb    r2, [r1, #SET]
    strb    r0, [r1, #CLR]
    mov     pc, lr

buzzer_on_off1:
    ldr     r1, =0xfffffC00
    and     r0, r0, #1
    movs    r0, r0, lsl #7
    strneb  r0, [r1, #SET]
    streqb  r0, [r1, #CLR]
    mov     pc, lr
```

Mapa de memória do LPC2106

(em falta)

Portos de entrada/saída de utilização genérica do LPC2106

(General Purpose Input/output - GIPO)