CSIS 402: Computer Organization

Milestone 2

Team 74

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Timing Signals

T_0: AR <- PC
T_1: IR <- M[AR], PC <- PC + 1
T_2: D_0, ….. D_7 <- Decode IR(12-14), AR <- IR(0-11), I <- IR(15)

AND
D_0T_3: DR <- M[AR]
D_0T_4: AC <- DR ^ AC, SC <- 0

ADD
D_1T_3: DR <- M[AR]
D_1T_4: AC <- AC + DR, E <- C_{out}, SC <- 0

LDA
D_2T_3: DR <- M[AR]
D_2T_4: AC <- DR, SC <- 0

STA
D_3T_3: M[AR] <- AC, SC <- 0

BUN
D_4T_3: PC <- AR, SC <- 0

SUB
D_5T_3: DR <- M[AR]
D_5T_4: AC <- AC - DR, SC <- 0

INC
$D_7I'T_3b_5$: AC <- AC + 1, SC <- 0

SZA
$D_7I'T_3b_2$: If (AC = 0) then (PC <- PC + 1), SC <- 0

Controls Signals

WR_MEM = D_3T_3

READ_MEM = $T_1 + D_0T_3 + D_1T_3 + D_2T_3 + D_5T_3$

LD_AR = $T_0 + T_2$

LD_DR = $D_0T_3 + D_1T_3 + D_2T_3 + D_5T_3$

LD_AC = $D_0T_4 + D_1T_4 + D_2T_4 + D_5T_4 + D_7I'T_3b_5$

LD_PC = D_4T_3

LD_IR = T_1

INC_PC = $T_1 + D_7I'T_3b_2(AC = 0)$

CLR_SC = $D_0T_4 + D_1T_4 + D_2T_4 + D_3T_3 + D_4T_3 + D_5T_4 + D_7I'T_3$

BUS_SLCT	
000	$T_1 + D_0T_3 + D_1T_3 + D_2T_3 + D_5T_3$
001	D_4T_3
010	0
011	0
100	D_3T_3
101	T_0

110	T_2
111	0

ALU_SLCT	
0000	0
0001	D_1T_4
0010	0
0011	D_2T_4
0100	D_0T_4
0101	0
0110	0
0111	0
1000	D_5T_4
1001	$D_7I'T_3b_5$
1010	0
1011	0
1100	0
1101	0
1110	0
1111	0

ALU Data Sheet

0001	DR + AC
0010	DR - AC
0011	Transfer DR to AC
0100	DR and AC
0101	DR or AC
0110	DR xor AC
0111	Increment DR
1000	**AC - DR**
1001	**Increment AC**

Program

Program	Assembly

`int A, B, C, D; // variables`
 	
`if (A+B-C == 0)`
`{D = A && B;} //&& means ANDing`
`else`
`{D = A++;}`
	`ORG 0`
	`LDA A`
	`ADD B`
	`SUB C`
	`SZA`
	`BUN N1`
	`LDA B`
	`BUN N2`
	`N1, LDA A`
	`INC`
	`BUN N3`
	`N2, AND A`
	`N3, STA D`
	`A, DEC 2`
	`B, DEC 5`
	`C, DEC 7`
	`D, DEC 0`

Machine Code in Memory:

Address (HEX)	Memory Content (HEX)
0	200C
1	100D
2	500E
3	7004
4	4007
5	200D
6	400A
7	200C
8	7020
9	400B
A	000C
B	300F
C	0002
D	0005
E	0007
F	0000