# Performance Measures

Ch 7

# Control Structure Taxonomy

| | Synchronous | Asynchronous |
|---|---|---|
| **Globally Timed** | - Centralized clocked FSM generates all control signals<br>Easy to design but fixed size interval can be wasteful (no data-dependent timing) | - Central control unit tailors current time slice to current tasks<br>↳ large systems lead to very complicated timing generation |
| **Locally Timed** | - Start and finish signals generated by each major subsystem synchronously with global clock<br>↳ the best way to build large systems that have ind. timed components | - Each subsystem talks asynchronously Starts, generates asynchronous Finish (perhaps using local clock)<br>↳ extra work is worth it in special cases |

# Summary

**Latency (L)** = time it takes for given input to arrive at output

**Throughput** = rate at which new outputs appear

* For combinational circuits:

$$L = t_{PD}, \quad T = 1/L$$

## For K-pipelines ($K > 0$):

- always have registers on outputs
- K registers on **every** path from input to output
- inputs available shortly after clock $\uparrow$, outputs after $\uparrow K$
- $t_{CLK} = t_{PD,REG} + t_{PD}$ of slowest pipeline stage + $t_{SETUP}$
- $T = 1/t_{CLK}$
  - more throughput → split slowest pipeline stages
    - use replication/interleaving if no further split possible
- $L = K * t_{CLK} = K/T$
  - pipelined latency ≥ combinational latency