CH3 — CMOS

N-channel MOSFET : Physical View

↳ MOSFET ; metal-oxide-semiconductor
field effect transistors
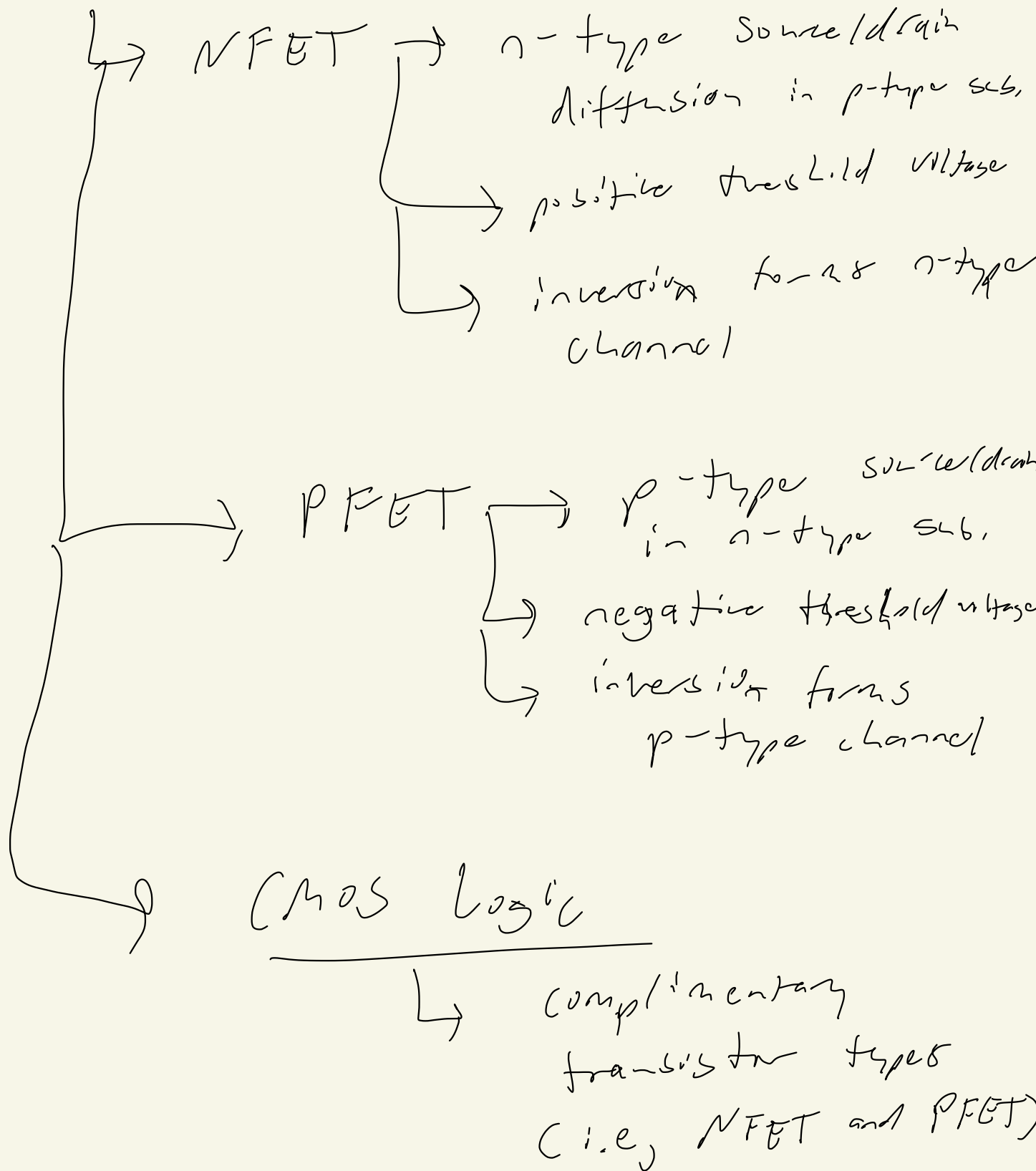
→ four-terminal voltage-controlled switches
↳ source   ↳ bulk
↳ gate   ↳ drains

→ current flows between the
diffusion terminals if the voltage is
large enough

↳ if not, the mosfet is off and the
diffusion terminals are not connected

N-channel MOSFET : Elec. View

↳ four terminals connect to
conductors that generate elec
fields in the channel region

↳ depend on the relative
voltages of each terminal

→ NFET → n-type source/drain diffusion in p-type sub.

→ positive threshold voltage

→ inversion forms n-type channel

→ PFET → p-type source/drain in n-type sub.

→ negative threshold voltage

→ inversion forms p-type channel

CMOS Logic

→ complimentary transistor types (i.e., NFET and PFET)

CMOS Recipe

- → Rule 1: only use NFETs in pulldown circuits

- → Rule 2: only use PFETs in pullup circuits

Complementary pullups/pulldowns

pullup	pulldown	F(inputs)
on	off	driven "1"
off	on	driven "0"
on	on	driven "X"
off	off	no connection

✳ memory is the load's capacitors charge

General CMOS Gate Recipe

Step 1: Figure out the pullup network that does what you want.

Step 2: Walk the hierarchy replacing nfets with pfets, series subnets with parallel subnets and parallel subnets with series subnets.

Combine pfet pullup network from step 1 with nfet pulldown network from step 2 to form a fully complementary CMOS gate.

CMOS Gates are Naturally Inverting

↳ All inputs 0

      ↳ nFETs off, pFETs on

         ↳ output must be 1

→ All inputs 1

      ↳ nFETs on, pFETs off

         ↳ output must be 0

Delays

↳ Propagation Delay (t_{PD})

      ↳ an upper bound on the delay from valid inputs to valid outputs

→ Contamination Delay (t_{CD})

      ↳ a lower bound on the delay from any invalid input to any invalid output

Acyclic Combination Circuit timing

- t_{CD} → min cumulative contamination delay over all paths from inputs to outputs

- t_{PD} → max cumulative propagation delay over all paths from inputs to outputs

Lenient Combinational Device

- output guaranteed to be valid when any combination of inputs sufficient to determine the output value has been valid for at least t_{PD}

- ✱ tolerates transitions and invalid levels on irrelevant inputs