Project Part 2 Lab Report: CprE 308

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1. Introduction

In this lab, we will explore several different types of memory page replacement algorithms and compare their effectiveness. More specifically, we will be dealing with FIFO (First In First Out), LRU (Least Recently Used), and the Clock algorithms. We have explained these paging algorithms in lecture, so we're now familiar with the concepts we will be implementing in this lab. After the completion of this lab, we should have a better understanding of how paging algorithms work and how to test their effectiveness.

2. Results/Output

Least Recently Used

```
matt@Matts-linux-box ~/Desktop/labs/project-B1 $
matt@Matts-linux-box ~/Desktop/labs/project-B1 $ ./mem_test 1 0

isu mmu.c:109: isu mmu_create(): created new MMU
matt@Matts-linux-box ~/Desktop/labs/project-B1 $ ./mem_test 1 1

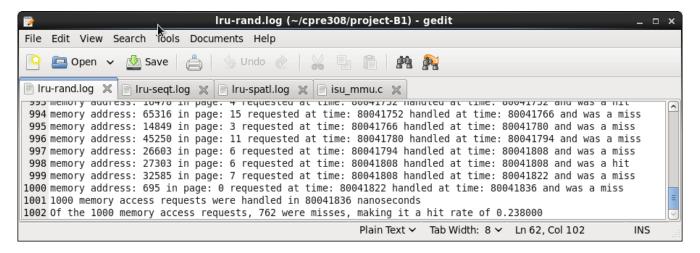
isu mmu.c:109: isu mmu_create(): created new MMU
matt@Matts-linux-box ~/Desktop/labs/project-B1 $ ./mem_test 1 2

isu mmu.c:109: isu mmu_create(): created new MMU
matt@Matts-linux-box ~/Desktop/labs/project-B1 $
```

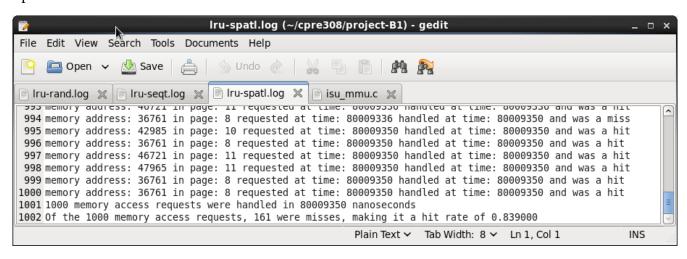
Sequential

```
Iru-seqt.log (~/cpre308/project-B1) - gedit
File Edit View Search Tools Documents Help
                 🔼 Open 🗸
🖹 Iru-rand.log 💥 📄 Iru-seqt.log 💥 📄 Iru-spatl.log 💥 📄 isu_mmu.c 💥
 ווופווו בככ uneiliory audicess. ע בווו page. ע requesteu at tilile. ווווים מטטסטטט nanuteu at tilile. מיסטסטטט anu was a iliss
994 memory address: 4096 in page: 1 requested at time: 80058670 handled at time: 80058684 and was a miss
 995 memory address: 8192 in page: 2 requested at time: 80058684 handled at time: 80058698 and was a miss
 996 memory address: 12288 in page: 3 requested at time: 80058698 handled at time: 80058712 and was a miss
997 memory address: 16384 in page: 4 requested at time: 80058712 handled at time: 80058726 and was a miss
998 memory address: 20480 in page: 5 requested at time: 80058726 handled at time: 80058740 and was a miss
999 memory address: 24576 in page: 6 requested at time: 80058740 handled at time: 80058754 and was a miss
1000 memory address: 28672 in page: 7 requested at time: 80058754 handled at time: 80058768 and was a miss
1001 1000 memory access requests were handled in 80058768 nanoseconds
1002 Of the 1000 memory access requests, 1000 were misses, making it a hit rate of 0.000000
                                                           Plain Text V Tab Width: 8 V Ln 978, Col 91
                                                                                                           INS
```

Random



Spatial



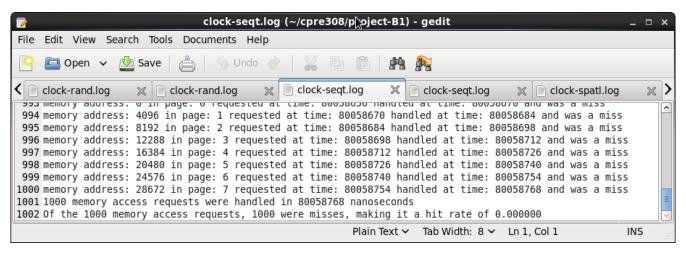
Are those the expected outputs/behavior? Which seems to perform the best over all the memory access patterns?

Yes, we expected a similar outcome. The least recently used algorithm performs best in the spatially located memory access pattern and worst in sequential memory access pattern. Sequential memory access pattern is the worst since once a page is accessed another time, all of the previous pages have been accessed, causing the algorithm to always page fault.

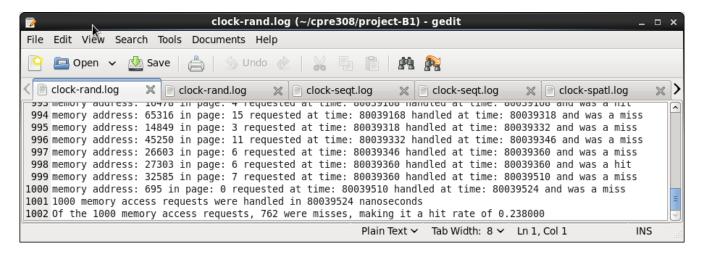
Clock Algorithm

```
bash-4.1$ ./mem_test 2 0
isu_mmu.c:109: isu_mmu_create(): created new MMU
bash-4.1$ ./mem_test 2 1
isu_mmu.c:109: isu_mmu_create(): created new MMU
bash-4.1$ ./mem_test 2 2
isu_mmu.c:109: isu_mmu_create(): created new MMU
```

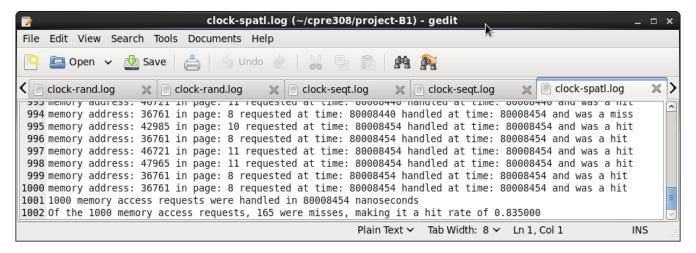
Sequential



Random



Spatial



Are those the expected outputs/behavior? Which seems to perform the best over all the memory access patterns?

Again the sequential was the worst, and spacial was the best. The results are very similar to the LRU algorithm above. We did have discrepancy between our results and the results in answers, but we were withing a reasonable difference, our results had 2 less page faults. Other than the discrepancy, our results were what we expected, similar to the LRU.

Going Further

After the page replacement algorithms have been implemented, it is recommended that the students play around with the size of L1 cache(or if desired, L2 cache, and RAM as well) and observe the difference in total time it took to handle all memory requests, and the difference in hit rate. Comment on what was experimented with and what observations were made in regards to the effects of changing the cache sizes.

Doubling the L1 size to 8 resulted in higher hit rates and lower running time for every algorithm. This intuitively makes sense, since there are more places to hold pages, more pages can be held in L1. Since there are more pages, there is a better probability for a page hit. Since a page fault takes longer than a page hit, if the hit rate increases the running time will decrease.

Doubling the L2 size seems to not affect the hit rate, but does decrease the running time.

Doubling the RAM size does not effect the hit rate or the running time.

3. Design Decision

Least Recently Used

We decided to keep it simple and use the code from the FIFO algorithm, but replace placement_time with access_time.

Clock Algorithm

To implement the clock algorithm we used a while loop which terminates when the page the hand is pointing to has a ref bit == 0. Then inside the while loop we set the current pages reference bit to 0 then advance the hand.

4. Issues

Most of our issues were implementing the clock algorithm. Our first problem was using the dirty bit in our algorithm, instead of the reference bit. This was a simple oversight, which was simple to fix. Another issue we ran into was we didn't increment our clock hand once we had found the replace index. This gave us some issues, since the output was very similar to the answers, but slightly off.

5. Conclusion

Overall, this lab was a success. We got to see the applications of paging algorithms and observe their effectiveness via test programs. We also gained more experience using Makefiles and compiling libraries. This lab gave us an insight into some of the core features of a real operating system, which helped give the lecture material some value.

6. Suggestions

We have no suggestions for this lab due to the well documented example files given and the straight-forward instructions given in the lab.