

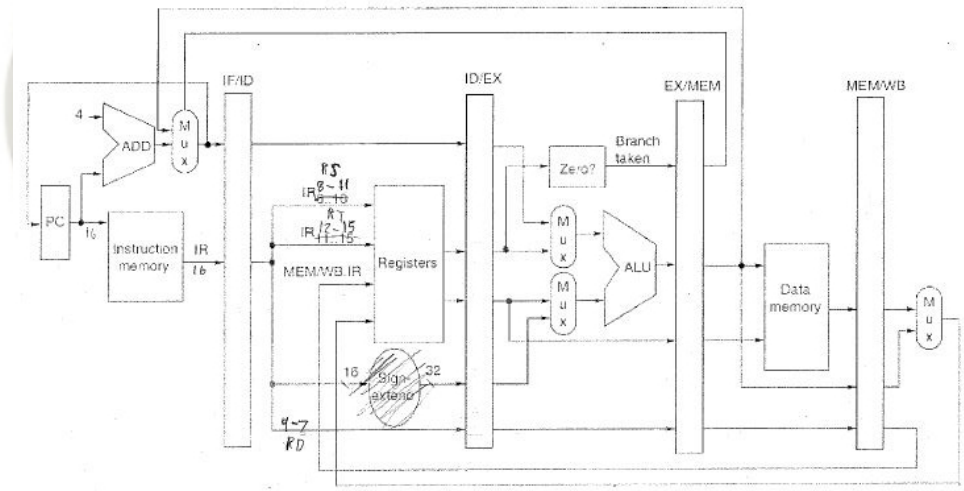

Deliverable 1: Design Specifications

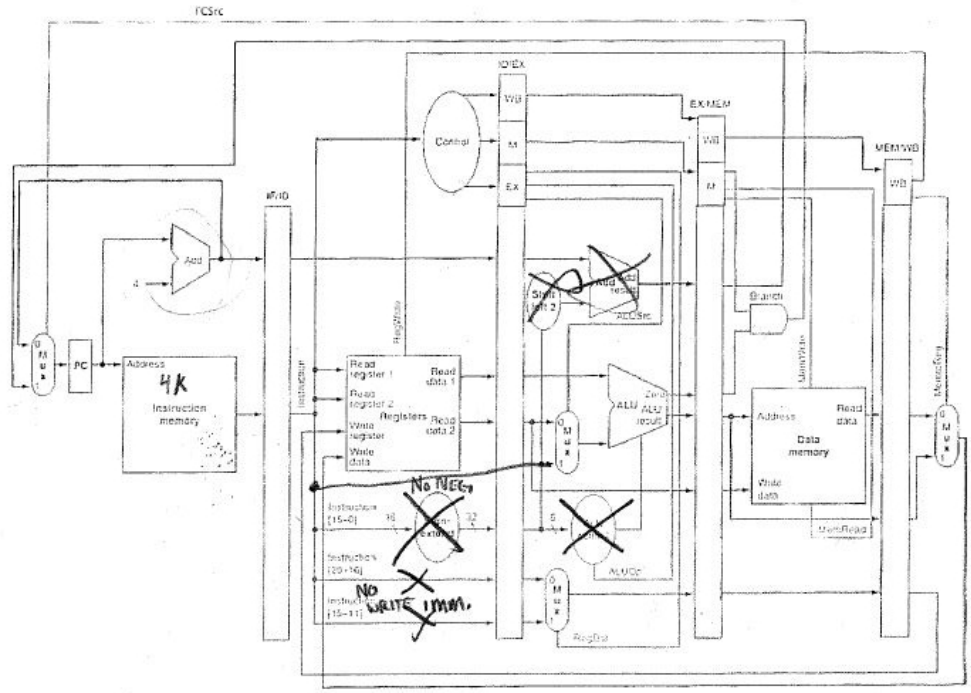
Team 3 - D.M.P.



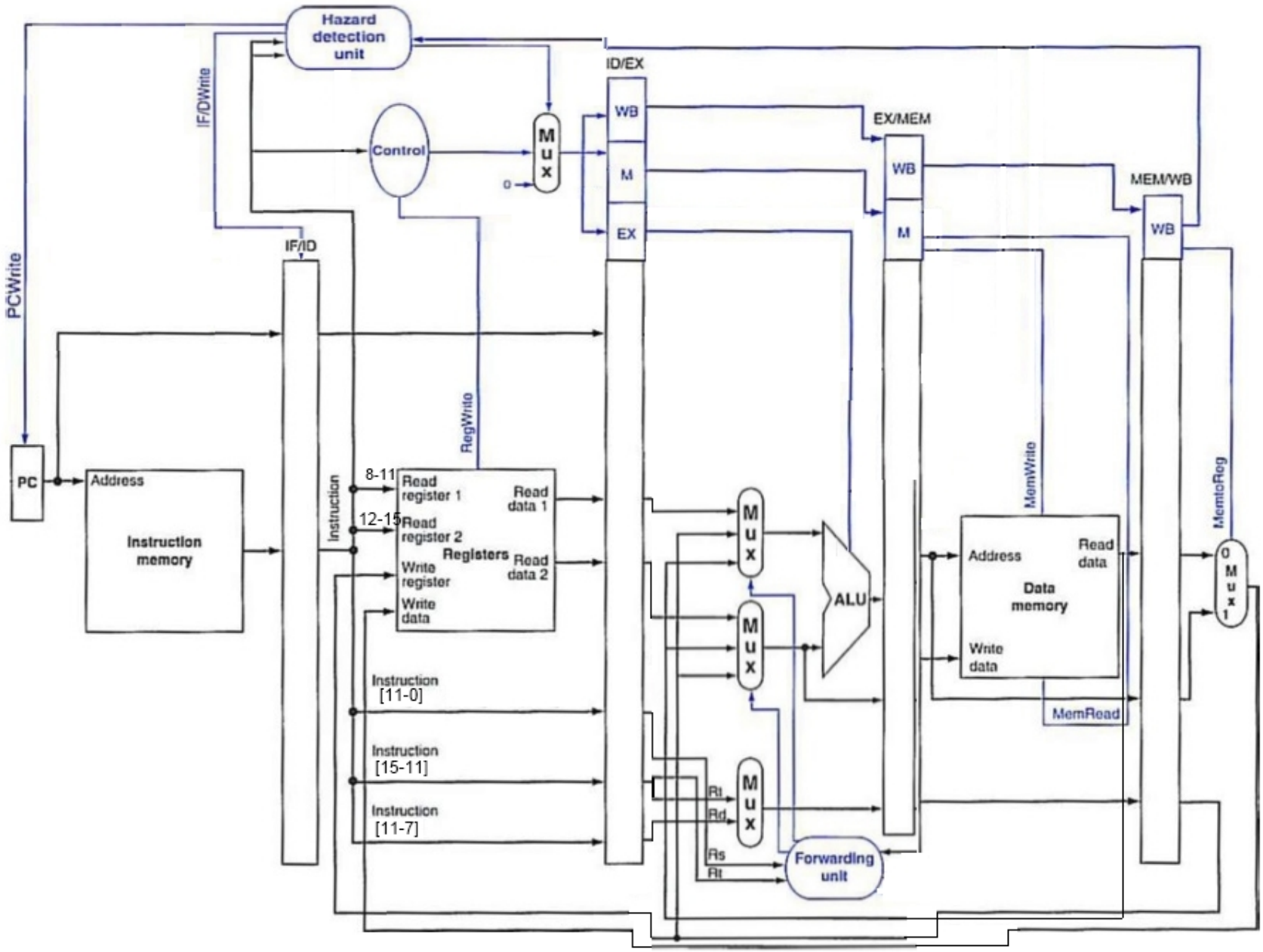

Hand Design Work

- Traced Current 32 bit Data Path
- Eliminate Sign Extend
- No Negative Numbers
- No Need for ALU control





Schematic


Hazard detection unit
IF/DWrite
PCWrite
Control
M u x
0
ID/EX
WB
M
EX
EX/MEM
WB
M
MEM/WB
WB
IF/ID
PC
Address
Instruction memory
Instruction
RegWrite
8-11
12-15
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
Instruction [11-0]
Instruction [15-11]
Instruction [11-7]
ALU
MemWrite
Address
Data memory
Read data
Write data
MemRead
MemtoReg
0 M u x 1
Rt
Rd
Rs
Rt
Forwarding unit

Components

Program Counter (x1)

- IN 16 bit next address
- IN Clock
- IN Power
- OUT 16 bit current address
- OUT Ground

ROM Instruction Fetch (x1)

- IN 16 bit current address
- IN Clock
- OUT 16 bit instruction
- OUT Ground




Components

16 Bit Adder(x1)

- IN 16 bit Operand A
- IN 16 bit Operand B
- OUT 16 bit Sum

2:1 Bit Control Mux(x4)

- IN 16 bit MUX A
- IN 16 bit MUX B
- IN 1 Control Bit
- OUT 16 bit MUX Result

Components

Hazard Detection Unit(x1)

- IN 16 bit Current Instruction
- IN 4 bit ID/EX RegisterRt
- IN 1 bit ID/EX MemRead
- OUT 1 bit Flush Mux

IF/ID Buffer(x1)

- IN 16 bit Current Address
- IN 16 bit Current Instruction
- IN Clock
- OUT 16 bit Current Address
- OUT 16 bit Current Instruction

Components

Register Unit(x1)

- IN 4 bit RD address
- IN 4 bit RS address
- IN 4 bit RT address
- IN 16 bit Write Back
- IN Clock
- OUT 16 bit ALU Operand A
- OUT 16 bit ALU Operand B

Control Unit(x1)

- IN 4 bit OpCode
- OUT 1 bit Jump MUX
- OUT 2 bit Forward MUX
- OUT 1 bit Write Back MUX
- OUT 1 bit ALU control
- OUT 1 bit Memory Read
- OUT 1 bit Memory Write

Components

ALU(x1)

- IN 1 bit ALU OpCode
- IN 16 bit ALU Operand A
- IN 16 bit ALU Operand B
- IN Clock
- OUT 16 bit ALU Sum
- OUT 1 bit Zero Flag

Forwarding Unit(x1)

- IN 4 bit RS Address
- IN 4 bit RT Address
- IN 4 bit RS Address
- IN 4 bit EX/MEM RegisterRtRd
- IN 4 bit MEM/WB RegisterRtRd
- IN 1 bit EX/MEM WB
- IN 1 bit MEM/WB WB
- OUT 2 bit ALU A Operand MUX
- OUT 2 bit ALU B Operand MUX

Components

EX/MEM Buffer

- IN 1 bit Write Back MUX
- IN 1 bit Memory Read
- IN 1 bit Memory Write
- IN 16 bit ALU Sum
- IN 1 bit ALU Zero
- IN 4 bit RdRt
- IN 16 bit ALU Operand B
- IN Clock

- OUT 1 bit Write Back MUX
- OUT 1 bit Memory Read
- OUT 1 bit Memory Write
- OUT 16 bit ALU Sum
- OUT 1 bit ALU Zero
- OUT 4 bit RdRt
- OUT 16 bit ALU Operand B




Components

Data Memory(x1)

- IN 16 bit Read/Write Input
- IN 16 bit Write Location
- OUT 16 bit Mem Read Value

MEM/WB Buffer(x1)

- IN 1 bit Write Back MUX
- IN 16 bit Read/Write Input
- IN 16 bit Mem Read Value
- IN 4 bit RdRt
- OUT 1 bit Write Back MUX
- OUT 16 bit Read/Write Input
- OUT 16 bit Mem Read Value
- OUT 4 bit RdRt

Next Steps

Get Real Work Done

- Assign Components to be created
- Start attaching the data path
- Revise current design

Begin Testing Phase

- Create low level Use Cases for components
- Consider real program support

Bibliography

1. "Digital Watches", Google Image Search http://www.google.com/search?client=safari&rls=en&q=digital+watches Images
2. Hennessy, John L., David A. Patterson, and Andrea C. Arpaci-Dusseau. *Computer Architecture: a Quantitative Approach*. Amsterdam: Morgan Kaufmann, 2007. Print.
3. Patterson, David A., and John L. Hennessy. *Computer Organization and Design: the Hardware/software Interface*. Amsterdam: Elsevier/Morgan Kaufmann, 2009. Print.