Waratah Seed Satellite Interface Control Document

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Revisions

	Version No.	Author	Change Log
19/07/2021	V1.0	XL , YH	First release
6/08/2021	V1.1	XL	Small tweaks on wording and project schedule
17/08/2021	V1.2	XL	Change of project schedule
23/08/2021	V1.3	IC, XL	Small tweaks on wording and project schedule
02/09/2021	V1.4	XL, IC	Minor changes to the UART connection description
02/09/2021	V1.5	XL, YH	1) Adjusted the stack to increase payload volume to 21.6mm 2) Updated WS-1 CAD in Figure 2
22/02/2022	V1.6	PO, XL	1) Updated electrical interface 2) Revised project schedule 3) Copyright
22/03/2022	V1.7	XL	Corrected the max. height for 0.5U, 0.75U and 1U in section 4.5.1
06/04/2022	V1.8	TK, PO	Adjusted Table 1 WS-1 Project Schedule

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1. Introduction and Scope

Waratah Seed is intended to be Australia's 1st Ride-Share satellite and the first NSW-built satellite (specifically a 6U CubeSat) focused on space industry & commercial applications. Waratah Seed is a pilot space qualification project to launch NSW-developed space technology into orbit to test and prove functionality. The project is focused on developing Australia's space sector, particularly NSW space industry.

The Waratah Seed project is led by the ARC Training Centre for CubeSats, Uncrewed Aerial Vehicles (UAV) and their Applications (CUAVA). CUAVA is funded by the Australian Research Council. Working with its academic, industry and government partners, its primary mission is to train the next generation of workers in advanced manufacturing, commercial space, and UAV applications. In doing so CUAVA will develop new instruments and technology to solve crucial problems, and develop a world-class Australian industry in CubeSats, UAVs, and related products. CUAVA has been in operation since December 2017, with headquarters at the University of Sydney. As well as CUAVA, the Waratah Seed partners are the Australian Centre for Space Engineering Research (ACSER) at University of New South Wales (UNSW), Saber Astronautics, Delta-V Space Hub, Macquarie University and the University of Technology Sydney (UTS).

The design of the Waratah Seed-1 (WS-1) Satellite bus is based on the 3U CUAVA-1 CubeSat bus, but with upgraded ADCS system and an additional high-speed communication system subject to requirements and contribution. This document is created to provide a concise overview of the various interfaces of WS-1 for payload developers. The satellite design is subject to changes due to payload requirements and budget constraints before the CDR stage without prior notice. It is recommended to reach out to the Waratah Seed engineering team after using this document to guide your initial payload design.

2. WS-1 Bus design

2.1. Bus design based on CUAVA-1 heritage

The satellite bus is mainly designed using commercial-off-the-shelf (COTS) products as listed in Table 1.

Table 2: WS-1 bus components

Subsystems/Functional components	Component Description	Source
On-board controller (OBC)	ISIS iOBC Onboard computer	https://www.isispace.nl/product/on-board-computer/
Full duplex UHF/VHF transceiver	ISIS.TrxVU full duplex radio	https://www.isispace.nl/product/cubesat-antenna-system-1u-3u/
Deployable VHF/ UHF antenna system	ISIS.deployable antenna system	https://www.isispace.nl/product/isis-uhf-downlink-vhf-uplink-full-duplex-transceiver/
Electrical power system (EPS) and battery pack	ISIS Compact EPS Type C (8 outputs and 4 battery pack, 45Whr)	https://www.isispace.nl/product/modular-electrical-power-system/
S-band communication system	Satlab SRS-4 Full-duplex High-speed S-band Transceiver	https://www.satlab.com/products/srs-4/
S-band Antenna	S-band patch antenna	https://www.iq-spacecom.com/products/antenna-s-band
Solar Panels	ISIS Modular Solar Panels (MSP) for 6U structure	https://www.isispace.nl/product/isis-cubesat-solar-panels/
Attitude Determination and Control system (ADCS)	CubeSpace CubeADCS 3-axis reaction wheels (1-3Deg pointing accuracy)	https://www.cubespace.co.za/products/integrated-adcs/3-axis/
Satellite Structure	ISIS 6U CubeSat Structure	https://www.isispace.nl/product/6-unit-cubesat-structure/
Payload OBC	In-house designed, can be customized subject to payload providers' requirement	Based on the Pocket Beagle opensource design: https://beagleboard.org/pocket
Flight Preparation Panel and debug interface panel	In-house designed, can be customized subject to payload providers' requirement	

Included in the above bus components is a high-speed communication system to increase the downlink bandwidth. The probable high-speed radio system is written above but is yet to be confirmed. If a payload has large data needs then these need to be communicated to the Waratah Seed team; meeting these needs may require additional financial contributions to be made by the payload team.

Optionally, we can add a star tracker to increase the pointing accuracy to 0.5-0.1 degree (subject to payload provider's requirements and contributions).

A system diagram, with assumed payloads, is shown in Figure 1.

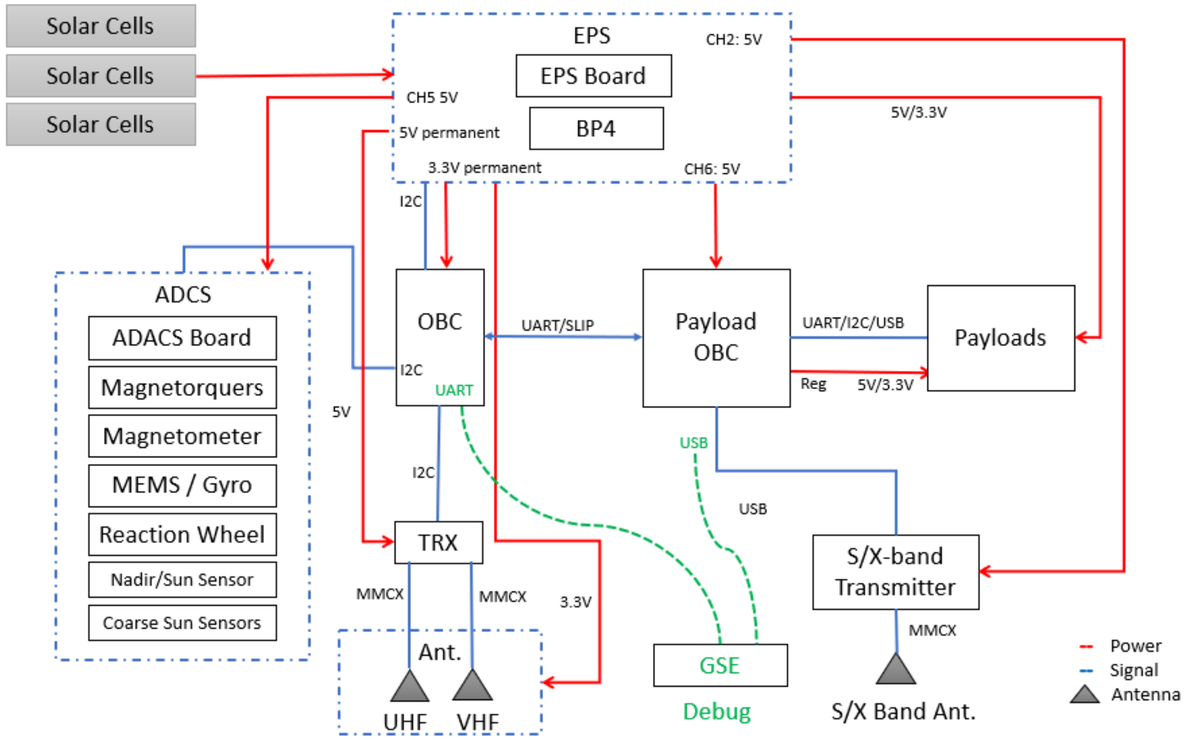


Figure 1: WS-1 system diagram

Note that most of the payloads shall be connected to the payload OBC rather than the satellite OBC unless specified otherwise. Both the satellite OBC and the payload OBC will be running a customized Linux (KubOS, as discussed in section 3). It is possible to have a second payload OBC if the number of the payloads is more than the payload OBC ports. The satellite OBC and the payload OBC(s) are connected via the Serial Line Internet Protocol (SLIP) interface as point-to-point ethernet connection(s). Each telecommand uplinked to the satellite radio(s) will be enveloped by a "space packet" (https://public.ccsds.org/Pubs/133x0b2e1.pdf), where the command ID, IP address, port number etc. are specified. When received by the satellite radio, the radio service will distribute the command to the correct payload service. For more details about the radio service, please refer to SW-1 Preliminary Design Review.

2.2. Bus capability Summary

CPU: 400MHz, 32-bit ARM9 CPU

RAM: 32MB SDRAM

SD-Card: 2 x 2GB

UHF/VHF data-rate: 9600bps

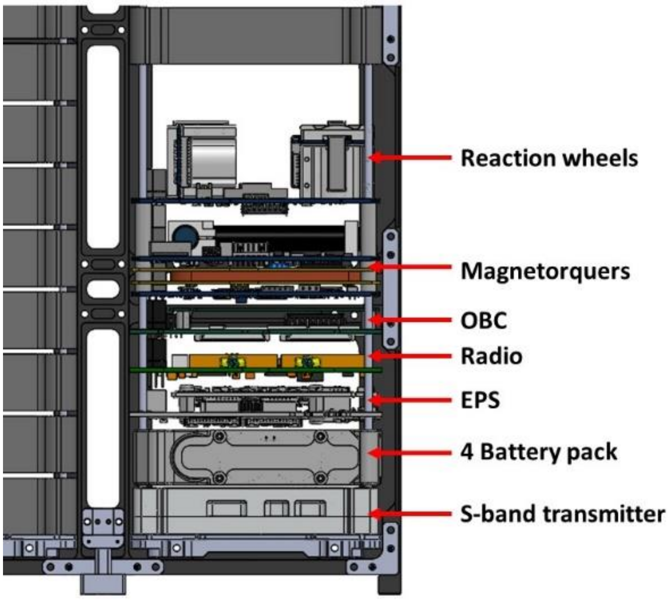
S-band (TBD): 4Mbps

Pointing accuracy: 1-3 Degree

Solar panel power: ~20W

EPS and battery: 6 configurable outputs (5V or 3.3V) with battery maximum depth of discharge 7.5Whr

Bus volume (without payload computer): approximately 1.5U as shown in Figure 3.



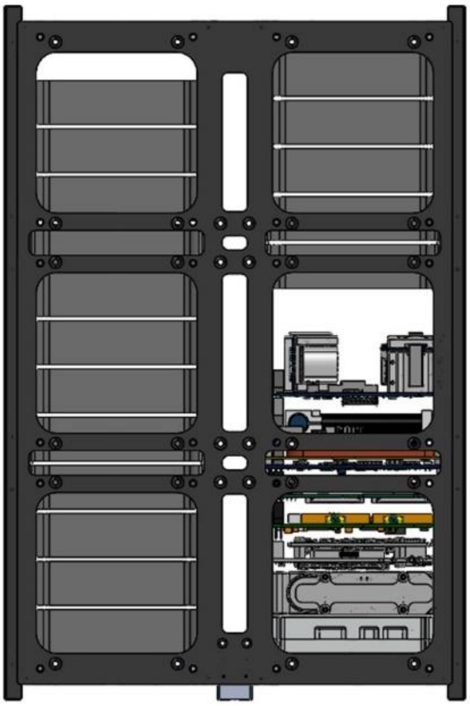


Figure 2: Waratah Seed Bus Design

2.3. Payload Computer Design

2.3.1. Payload Computer Design Overview

The payload computer design is still in progress. The design will be based on the Pocket Beagle design (https://github.com/beagleboard/pocketbeagle).

The payload computer will be connected to a 5V@2A power channel. It will include a power selection chip to select and deliver 5V@1A to up-to 12 payloads. It is recommended to use a Beaglebone Black or Pocket Beagle board to test the software interface during payload development. Depending on the number of payloads, it may be possible to add a second payload computer on the WS-1.

Before payload delivery, the Waratah Seed or CUAVA team will provide a payload computer to the payload team to test the software interface.

2.3.2. Payload Computer Communication interfaces

- UART (3 sets): 6pin picoblade connector. up to 500kbps (115.2kbps if using Serial Line Internet Protocol (SLIP)) LSB first, no parity, 8 data bits, 1 stop bit
- I2c (up to 6 devices): 6pin picoblade connector. 400kbps
- USB hosts (4 sets via a USB hub controller): Considering **TF38-22S-0.5SV (pin allocation TBD)**
- USB slave: Reserved for debug
- Ethernet port (1 set): Considering FPC or nano Dsub (**pin allocation TBD**).

3. WS-1 Software Design.

3.1. KubOS overview

The flight software is developed in-house by the CUAVA software team at the University of Sydney based on an open source embedded Linux named KubOS (Kubos, n.d.). KubOS is a package framework that runs directly on satellite hardware combining a customized Linux distribution, subsystem APIs, and core services. It provides some of the core functions for satellite developers such as File Transfer Protocol, mission scheduler etc.

Due to power constraints imposed by the ISIS OBC, we are designing a payload computer as discussed in Section 2. The payload computer(s) will also use the KubOS platform and will connect to the OBC via a point-to-point ethernet connection. The CUAVA team will provide the CROSS compiler for either of the computers and it is **NOT** necessary to design your software API and service again in the case that we want to relocate your payload from payload computer to the OBC.

The OBC software architecture is shown below.

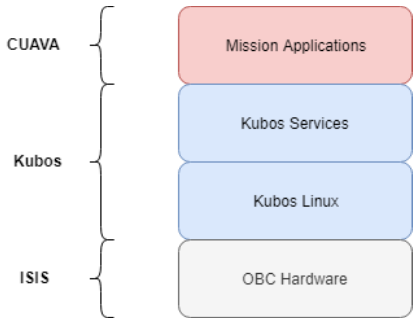


Figure 3 - Architecture Overview

- **Mission Applications:** Governs the behaviour of the satellite
- **Kubos Services:** Core and hardware services for interacting with the satellite, including services for mission specific bus components and payloads
- **Kubos Linux:** Custom Linux distribution designed for embedded devices
- **OBC Hardware: ISIS** on-board computer and in-house design payload computer

3.2. Kubos Core Services

Core services provide critical flight software capability but do not interact with hardware. The payload Concept of Operation (CONOP) will be based some of all of the below core services. They are developed by Kubos and currently include:

- Shell service (design by CUAVA)
- Telemetry database service
- File transfer service
- Process monitoring service
- Application service/registry
- Monitor service

3.3. Mission Applications

Handle all the onboard decision making and form the backbone of the satellite's operation. The payload service will be based some of all of the below mission applications. The applications can include but are not limited to:

- Bootup and initialisation
- Time management
- Command processing
- Telemetry processing
- Data storage

- Fault protection
- Payload operation, logging and monitoring

There are also some mission specific Applications heritage from the CUAVA-1 mission that can be used for payload CONOP design:

- Radio inhibit and antenna deployment application
- ADCS commissioning and detumbling application
- ADCS pointing application

3.4. Designing Payload API and Service

Each payload on the satellite will require its own software for operation that will interface with the mission application software. When the payload is delivered, it shall come with functional payload Application interface (API) and service for testing (we can NOT consider the payload as "delivered" without a working service), it is possible to deliver your payload Application(s) after the payload hardware is delivered and before the environmental testing.

In addition to the documentation provided by KubOS, the CUAVA team also has tips and guides in our group wiki and code template to assist your payload service software design. The Waratah Seed and CUAVA teams will also provide workshops to get your team started and support during your development process.

The services discussed above, together with the ground station terminal software forms the Mission Architecture as shown below:

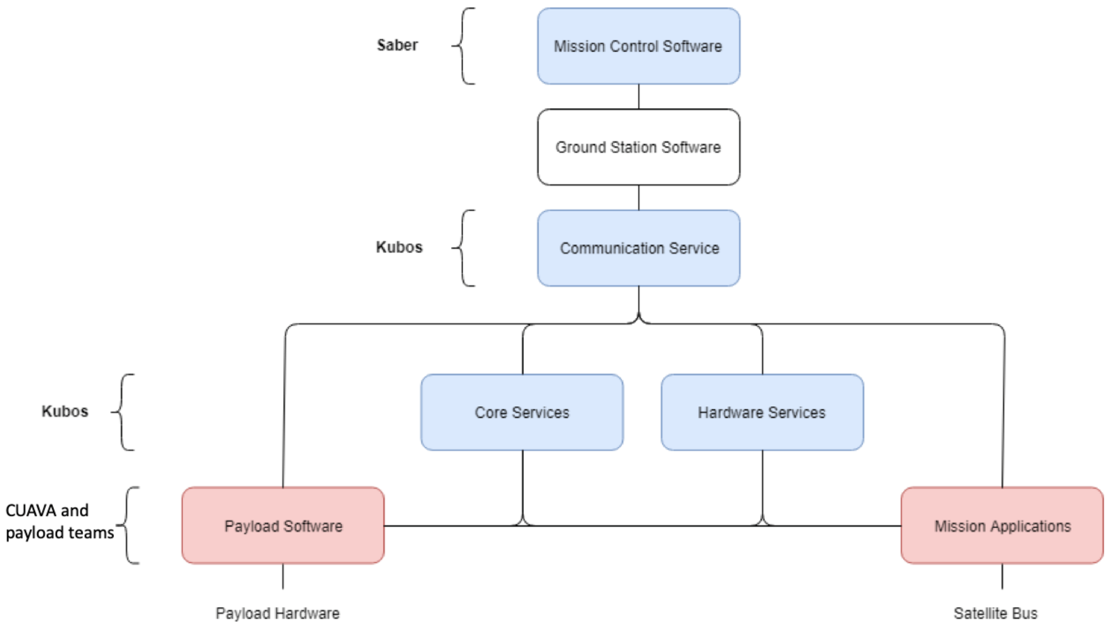


Figure 4 - Mission Architecture

4. Payload Interfaces

4.1. Electrical Interface

As mentioned in Section 2, **ALL** payloads shall be connected to the payload computer unless the Waratah Seed team specifies otherwise. The power will be delivered in the same connector with the communication bus from the payload computer. You can choose from UART, i2c interfaces (slave devices only), USB Host or Ethernet:

- UART (4 sets): 6pin picoblade connector. up to 500kbps (115.2kbps if using Serial Line Internet Protocol (SLIP)) LSB first, no parity, 8 data bits, 1 stop bit I2c (up to 6 devices)

Pin	Connection	Wire colour
1	GND	Blk
2	5V/3.3V	Red
3	RxD	Yellow
4	TxD	Orange
5	GND	Brown
6	5V/3.3V	Green

- i2c (Slave only): 6pin picoblade connector. Up to 400kbp, **pull up resister already exist on the payload computer.**

Pin	Connection	Wire color
1	GND	Blk
2	5V/3.3V	Red
3	SDA	Green
4	SCL	Brown
5	GND	Blue
6	5V/3.3V	White

- USB and ethernet connectors: please consult the Waratah Seed team for availability and pin allocations.

The allocation of the electrical interface allocation (especially for UARTs) will follow a first in first served principle and be subject to coordination between payload teams.

6-pin picoblade connector is recommended and should be easily accessible for integration/reintegration. For UART and i2C, and we generally encourage pin 1 to pin 1 connection. Please specify in your ICD if designed differently. Note that other connector types may introduce higher cabling cost.

4.2. Power budget

For a nominal ~500km SSO orbit, WS-1 payloads will have approximately 5.0 watt-hours (Whr) available per orbit. This may be improved depending on utilisation of ADCS and mission pointing requirements.

4.3. Power constraints

All payloads with size 0.5U or smaller shall restraint the power consumption below 5W@5V1A. For larger payloads with higher power consumption (up to 10W@5V2A), it is recommended to directly connect the payload to the PC104 stack and obtain power from EPS directly. There is a limited number of such 5V2A power channels and please consult the Waratah Seed team for availability.

4.4. PC104 interfaces

This section is intended for i2c payloads that connect directly to the PC104 stack. The ground pins are H2-30, H2-29 and H2-32. The power channels are from H1-48 to H1-51. Due to design constraints, the number of the power channels directly from the PC104 stack will be extremely limited. Please discuss with the Waratah Seed team prior to your final PCB board design.

Note that Vbat (H2-45/46, ~8V), permanent 3.3V (H2-27/28) and permanent 5V (H2-25/25) are **NOT** available to the payload teams.

	20		22	DRXD	24		26	5V	28	3.3V	30	GND	32	GND	34		36	
H2	19		21	DTXD	23		25	5V	27	3.3V	29	GND	31		33		35	
	20		22		24		26		28		30		32		34		36	
H1	19		21	I2C SCL	23	I2C SDA	25		27		29		31		33		35	

	38		40		42		44		46	VBAT	48		50	GPIO 24	52	GPIO 28
H2	37		39		41		43		45	VBAT	47		49		51	GPIO 26
	38		40		42		44		46	GPIO 23	48	3.3V OUT1	50	3.3V OUT2	52	3.3V OUT3
H1	37		39		41	I2C SDA	43	I2C SCL	45	GPIO 22	47	5V OUT1	49	5V OUT2	51	5V OUT3

4.5. Mechanical Design:

4.5.1. Standard mechanical interface

The WS-1 satellite follows the CubeSat mechanical interface. Each stack has 4 ribs connected by 4 threaded rods. The pictures below illustrate the integration process and a complete 1U stack.

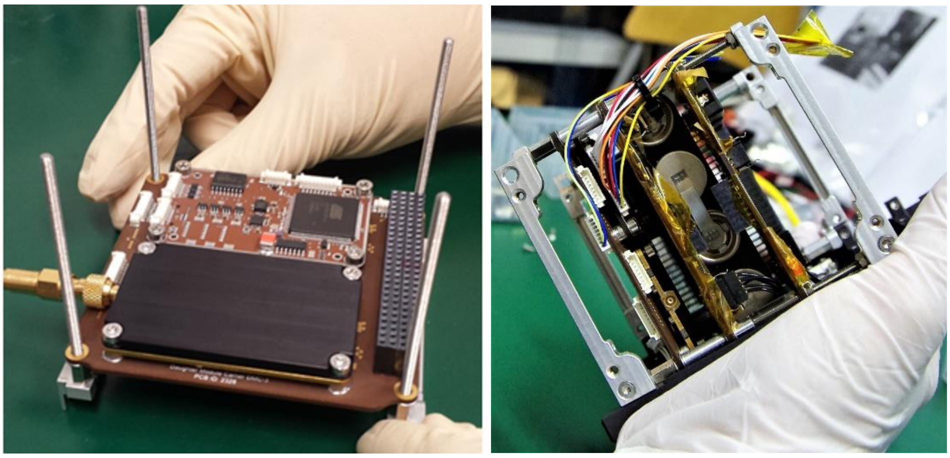
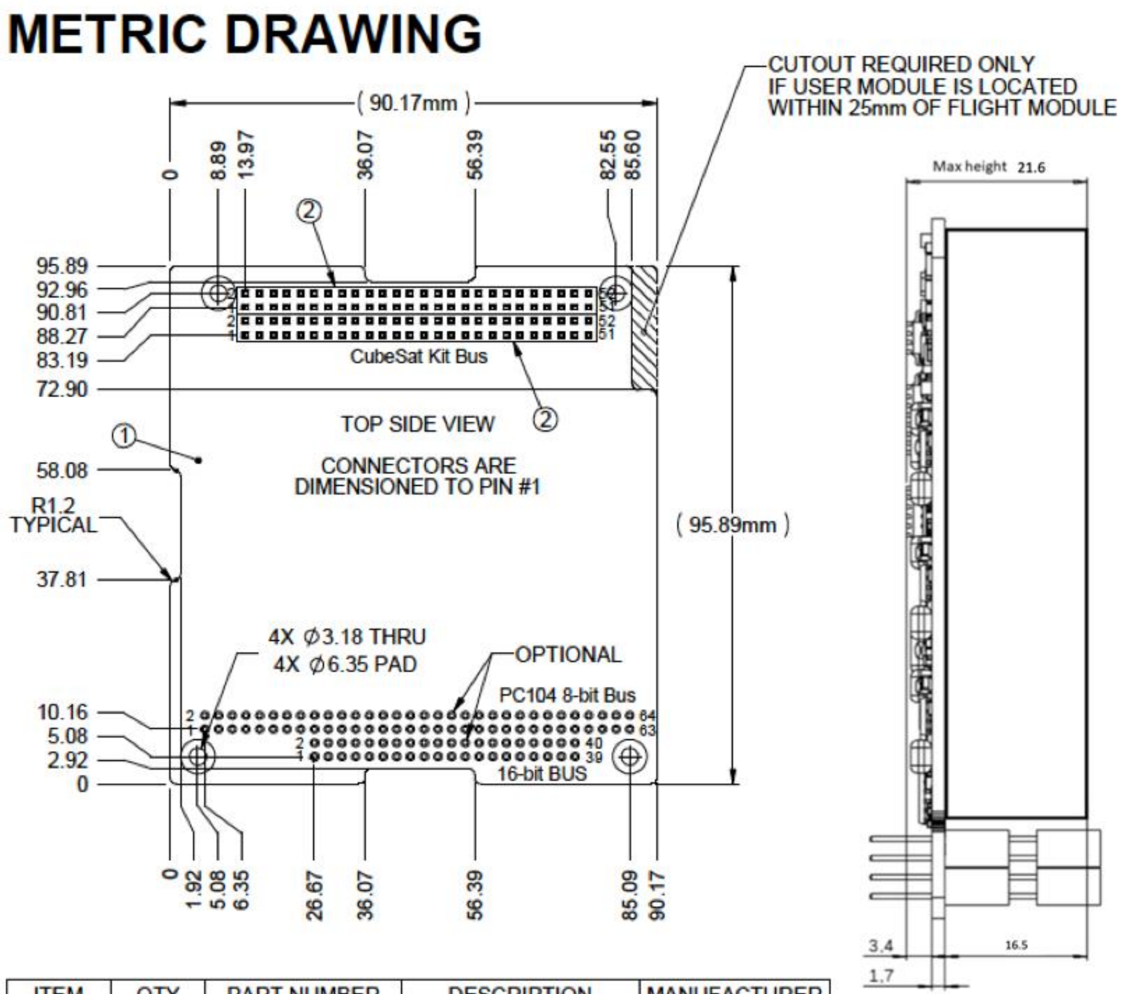


Figure 5 – Mechanical interface for PCB boards

For a standard 0.25U payload slot, the design should comply with the mechanical design as shown in Figure 6. Dimensions are given in mm. If your payload is selected, the Waratah Seed team will provide satellite CAD to guide your design. The mechanical interface (Metrics, mm) for the CubeSat standard PCB is shown in figure 6 (referenced the Pumpkin satellite CubeSat Kit PCB Specification). The imperial version of the drawing is attached in Annex 1.

Note that even if you are not using the PC104 stack for electrical interfaces, it is **recommended** to have it in place to increase the mechanical integrity of the stack. It is possible to have an alternative mechanical mounting design if the Waratah Seed team agrees following detailed discussions.



ITEM	QTY	PART NUMBER	DESCRIPTION	MANUFACTURER
1	1	PC104 Spec PCB	User	User
2	2	ESQ-126-39-G-D	2x26 Stack-Through	Samtec.com

NOTES:

1) Connectors shown are .10" x .10" spacing, .025" square pin.
2) Samtec part numbers listed are low insertion force versions.
3) In the case where a 25mm gap will exist above the User Slot an additional connector should be used to gap the extra 10mm distance, plugged into the main connector. Use part SSQ-1XX-22-G-D where "XX" is the # of contacts per row.

Figure 6 – WS-1 payload mechanical interface (measurements shown in mm) *

*** For a 0.5U, 0.75U, 1U payload slot, the maximum height is 45.2mm, 68.8mm and 92.4mm respectively (Pin header height shall change accordingly). For 0.5U and larger payload slots, it is possible to customize design the mechanical interface subjective to discussion with the Waratah Seed team.**

4.5.2. Customized mechanical interface for larger payloads

For 0.5U or larger payloads, it is possible to design a customized mounting structure. It is also possible, for larger payloads, to have apertures and to protrude outside the satellite structure for up to 6.5mm (subject to launcher's requirements). However, the location of the apertures, protrusions and customized structure designs will be subject to other design constraints (i.e. ADCS design, solar panel design etc.). If customized design is desired, please discuss with the Waratah Seed team as early as possible and certainly before 30th Dec 2021. Such customized design may also involve extra costs.

5. WS-1 Design Restrictions and suggestions

1) No battery or supercapacitor is allowed on the payload. The payload MCU will sync the time with the OBC when start/restarted if time-stamped payload operation is required.
2) Use Surface Mounting Components (SMC) where possible for better vibration and vacuum performance.
3) All mechanical design shall specify 10µm (or lower) as tolerance to the manufacturers
4) Conformal coating is welcomed for flight models
5) Please use NASA's outgassing data to guide your material selection: https://outgassing.nasa.gov/. CUAVA recommends the below glues and tapes based on our past missions:

- Thermal Tape: Sigraflex Foil F05010E or F05010TH or Cho-therm 1671
- Aluminium tape: 3M™ Aluminium Foil Tape 425 and 435 (425 has been tested in vacuum chamber).
- 3M Scotch-Weld 2216 Epoxy
- UHU 300 Epoxy
- Thread locker: Loctite 243 (Not included in the NASA database but widely used)

6. Qualification Testing/Flight Acceptance and Licencing

All WS-1 payloads shall complete a vibration test for sinusoidal and random vibration unless waived by the Waratah Seed engineering team. A recommended qualification level is shown in Table 2. **The acceptance test level will be updated once the launch vehicle is selected.**

Table 3 Recommended Acceptance test level (NASA GEVS Table 2.4-3).

Frequency (Hz)	ASD Level (g^2/Hz)
	Acceptance
20	0.013
20 – 50	+6dB/Oct
50 – 800	0.08
800 – 2000	-6dB/Oct
2000	0.013
Overall	10 G_{rms}
Duration (minutes/axis)	2

Thermal vacuum test is recommended but not mandatory. The Waratah Seed team reserves the right to require a thermal bakeout if a payload sensitive to outgassing (i.e. an optical payload) is selected for WS-1.

All payloads that generate RF signals (for both communication and non-communication purposes) must coordinate with the Waratah Seed team after selection to obtain frequencies coordination provided by International Amateur Radio Union (IARU), and International Telecommunication Union (ITU).

7. Project Schedule

We aim to deliver the WS-1 satellite by January 2023, with launch in April 2023. The Waratah Seed team needs to provide a 6-month notice (TBC) if we want to delay the launch. Also, the Waratah Seed team will need at least 4 months to assemble, integrate and test the WS-1 satellite prior to delivery. Please see Table 3 for the due dates for the delivery of Engineering Model (EM) and Flight Model (FM). It is not required to provide two payload models. The Service Agreement describes the conditions under which Waratah Seed may reject a payload without refund if the due dates are not or cannot be met.

The current schedule with estimated due dates is listed below.

Table 4 WS-1 Project Schedule

Milestone	Estimated Due Date
Interface Control Document	31st August 2021
Rideshare Payload Applications close	28th Sep 2021
Shortlisted applicants notified	5th October 2021
Private Pitch	19th October 2021
Public Pitch	9th November 2021
Written applications close	30th November 2021
Finalists and shortlist announced	10th December 2021
Preliminary Design Review (Payload Competition Winners)	28th February 2022
Preliminary Design Review (Commercial Clients)	30th April 2022
Payload EM delivery (Payload Competition Winners)	31st May 2022
Payload EM delivery (Commercial Clients)	30th June 2022
Payload EM functional and vibration Testing (up to payload team)	30th June 2022
Critical Design Review	31st July 2022
Payload FM delivery (Payload Competition Winners)	1st September 2022
Payload FM delivery (Commercial Clients)	1st October 2022
FM Satellite integration and Functional testing	31st October 2022
Environmental testing	30th November 2022
FRR and delivery	31st January 2023

Annex 1, Imperial (in) version of CubeSat Kit PCB specification (credit to Pumpkin Inc.)