curveTech

ID-35

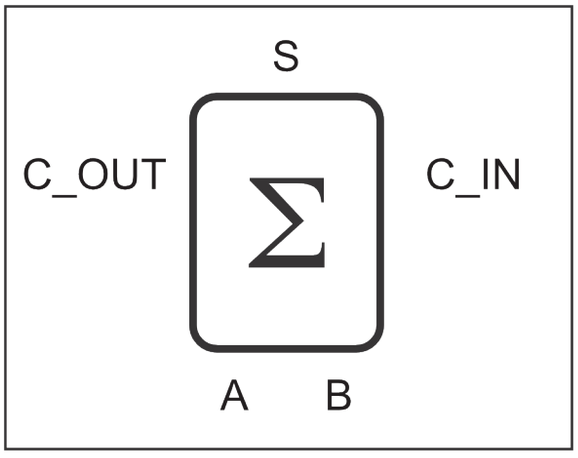
INTEGRATED DEVICES

ADDER

FULL SUMMATION UNIT

AN ADDER UNIT ADDS BINARY NUMBERS AND ACCOUNTS FOR VALUES CARRIED IN AS WELL AS OUT. A ONE-BIT FULL-SUMMATION UNIT ADDS THREE ONE-BIT NUMBERS, NOTATED HERE AS A, B, AND C_IN; A AND B ARE THE OPERANDS, AND C_IN IS A BIT CARRIED IN FROM THE PREVIOUS LESS-SIGNIFICANT STAGE. THE ADDER UNIT IS USUALLY A COMPONENT IN A CASCADE OF ADDER UNITS, WHICH ADD 8, 16, 32, ETC. BIT BINARY NUMBERS. THE CIRCUIT PRODUCES A TWO-BIT OUTPUT. OUTPUT CARRY AND SUM, REPRESENTED BY THE SIGNALS C_OUT AND S, WHERE THE SUM EQUALS 2*C_OUT + S

ADDER DIAGRAM



ADDER LOGIC TABLE

A	B	C_IN	S	C_OUT
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1

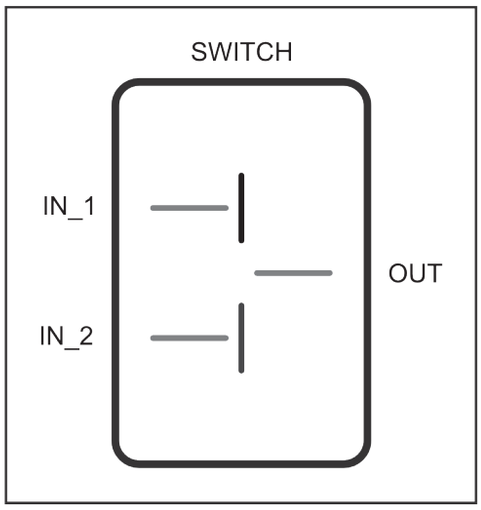
MULTIPLEXER / DEMULTIPLEXER

TRANSMISSION CHANNEL SWITCHING

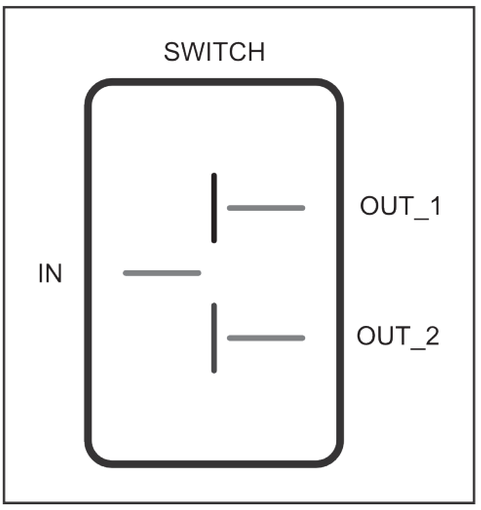
A MULTIPLEXER, IS A UNIT THAT SELECTS BETWEEN SEVERAL SIGNAL INPUT TRANSMISSION CHANNELS AND FORWARDS THE SELECTED INPUT TO A SINGLE OUTPUT CHANNEL. THE SELECTION IS DIRECTED BY A SEPARATE SIGNAL INPUTS KNOWN AS THE SWITCH. SIGNALS SENT TO THE SWITCH PORT WILL ADVANCE THE SELECTED INPUT CHANNEL BY ONE, WRAPPING UPON REACHING THE END. THE INPUT LINE SELECTION IS SHOWN BY THE ACTIVE LIGHT.

CONVERSELY, A DEMULTIPLEXER IS A DEVICE TAKING A SINGLE INPUT CHANNEL AND SELECTING SIGNALS OF THE OUTPUT OF THE COMPATIBLE MULTIPLEXER, WHICH IS CONNECTED TO THE SINGLE INPUT, AND A SHARED SWITCH SIGNAL. A MULTIPLEXER IS OFTEN USED WITH A COMPLEMENTARY DEMULTIPLEXER ON THE RECEIVING END.

2-1 MULTIPLEXER DIAGRAM



1-2 DEMULTIPLEXER DIAGRAM



SINGLE BIT MEMORY

SINGLE BIT STORAGE UNIT WITH WRITE AND FUNCTIONS

A SIGNAL BIT MEMORY UNIT IS DESIGNED TO HOLD A SIGNAL BIT STATE. INTERNAL STATE CAN BE MODIFIED USING THE EXTERNAL SIGANL INPUT PORTS, OR USING THE MANUAL BUTTONS ON THE FRONT OF THE UNIT. THE STATE CAN BE READ USING THE READ BUTTON OR SIGNAL INPUT PORT, WHICH WILL PRODUCE THE APPROPRIATE SIGNAL FROM THE SIGNAL OUTPUT PORT. INTERNAL STATE CAN BE DETERMINED USING THE STATUS LIGHT ON THE FRONT OF THE UNIT. ACTIVATING THE WRITE SIGANL INPUT PORT WILL CAUSE THE INTERNAL STATE TO MATCH THE STATE OF THE CURRENT SIGNAL INPUT LOCATED AT THE BOTTOM OF THE UNIT.

SIGNAL BIT MEMORY DIAGRAM