Lab Plan from now.

25/10/17 (Wed) --- 2 to 3 (Viva Exam) and 3.30 to 5.30 (Design Test) exact date and venue will be intimated two days prior

26/10/17 (Thurs) --- Discussion on SRAM-TCAM implementation on FPGA and verifying the outputs for Priority Enc. Design on FPGA.

01/11/17 (Wed) ---- Discussion on project and evaluation of SRAM-TCAM design on FPGA and also discussion on **UPDATE Engine Design** (Part of your final project, doesn't require day-day evaluation)

12/11/17 -- Optional lab. Can be used for doubts clarifications, pending day-day evaluations and compensation works evaluations.

13/11/17 -- Last day for finishing all your day-day evaluations with penalty. Experiments not evaluated by the end of this day will be considered as incomplete and given ***zero*** marks.

Important Deadlines:

1. *Report:* ***12/11/17 - 12 p.m, the deadline has been changed and please note it.***
2. Day to Day Evaluations: 13/11/17 – 5 p.m.
3. Final Project: 25/11/2017 -- COE Batch and Kurnool Students.

   26/11/2017 -- CED Batch.

Final project evaluations will be done post your exams and this has been decided upon receiving the request from majority of the students. If someone leaves before the 25/11/2017, they can meet me in prior and can fix their evaluation dates at your time of convenience ***before 24/11/17.***