Microchip Technology Inc.

Digital Compensator Design Tool Help File

Digital Compensator Design Tool Help Menu

Getting Started

The Digital Compensator Design Tool (DCDT) was developed to aid power supply engineers in the design of the digital controller, specifically those used for Switch Mode Power Supply (SMPS) applications. The DCDT Graphical User Interface (GUI) will request from the user all the pertinent information required to model the system, once that all the parameters are entered into the GUI the designer can use the built in tools such as Bode Plots, Nyquist, Step Response and Root Locus to evaluate the performance of the compensator and determine if it meets the desired performance, prior to the hardware implementation.

The DCDT tool was designed specifically for power supply applications and this supports Voltage Mode Control (Single-Loop System), Peak-Current Mode systems and Dual-Loop Systems* (such as Average Current Mode). The user can make the selection based on hardware topology requirements.

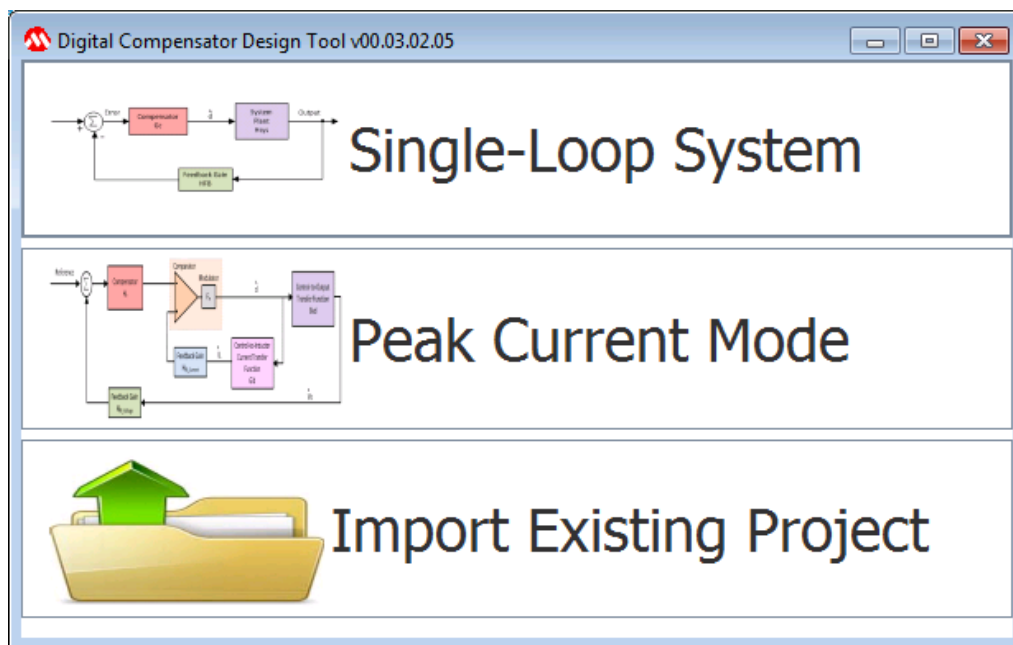Note *: Average Current Mode is in development and not implemented in this release of DCDT.

Figure 1 - DCDT Start-up Window

Single-Loop System

The Single-Loop System option is used when the power supply includes one compensator, with a single feedback loop. For example a voltage mode (VM) step-down or Buck converter, see Figure 2 below, where the output voltage is monitored via the feedback resistor divider network and compared against a reference/set-point voltage. Based on the measured error the compensator will calculate the PWM duty cycle to ensure that the output voltage is well regulated.

As an example, below is the simplified diagram of a voltage mode buck converter controlled by a Type III analog compensator, where the DCDT can calculate the Digital Compensator coefficients to represent the equivalent controller using a microcontroller.
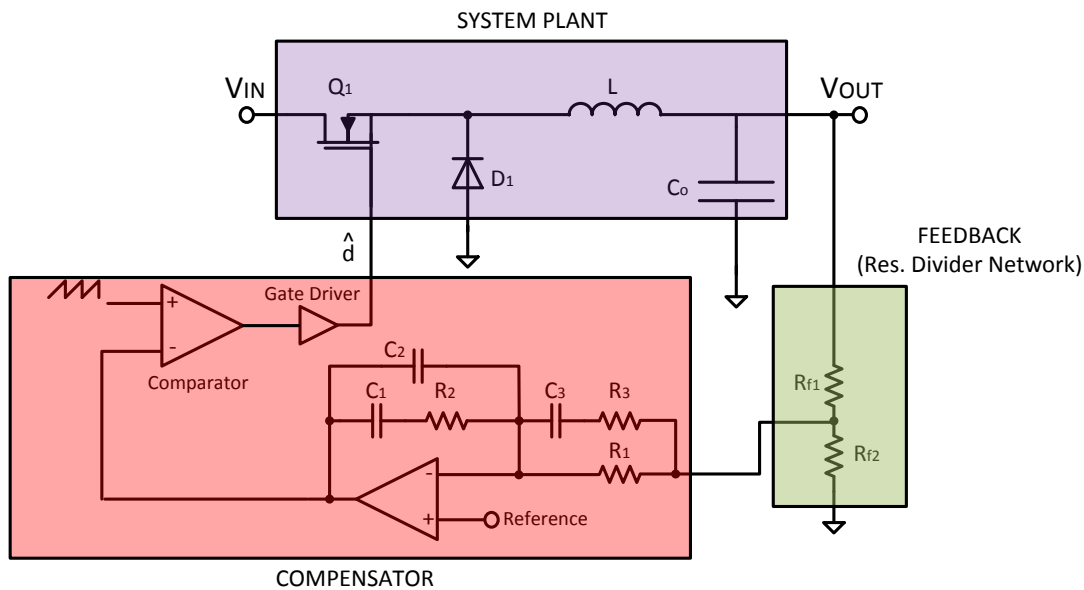

Figure 2 – Voltage Mode Buck Converter

The DCDT GUI will represent the system using the following block diagrams, where each block diagram will need to be defined by the user based on the hardware topology and design.

Figure 3 - DCDT Block Diagram for Single-Loop System

Peak-Current Mode Control

The Peak-Current Mode Control (PCMC) option allows the user to model and design the digital compensator required for this mode of control. The PCMC is characterized by having one compensator to monitor the outer Voltage-Loop and one analog comparator used to monitor the inner Current-loop. The advantages and disadvantages of the different control modes will not be discussed in this document and more information can be found in the Related Application Notes: section.

As an example, below is shown a step-down or Buck converter operated in Peak Current Mode, notice how this diagram is simplified and can be used to represent any power supply topology.

Figure 4 - Peak Current Mode controlled Buck Converter

The DCDT GUI will represent the system using the following block diagrams, where each block diagram will need to be defined by the user based on the hardware topology and design.
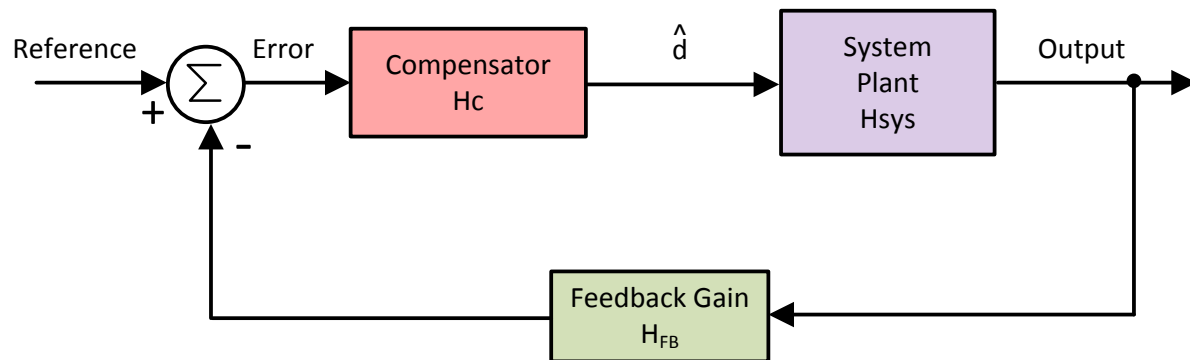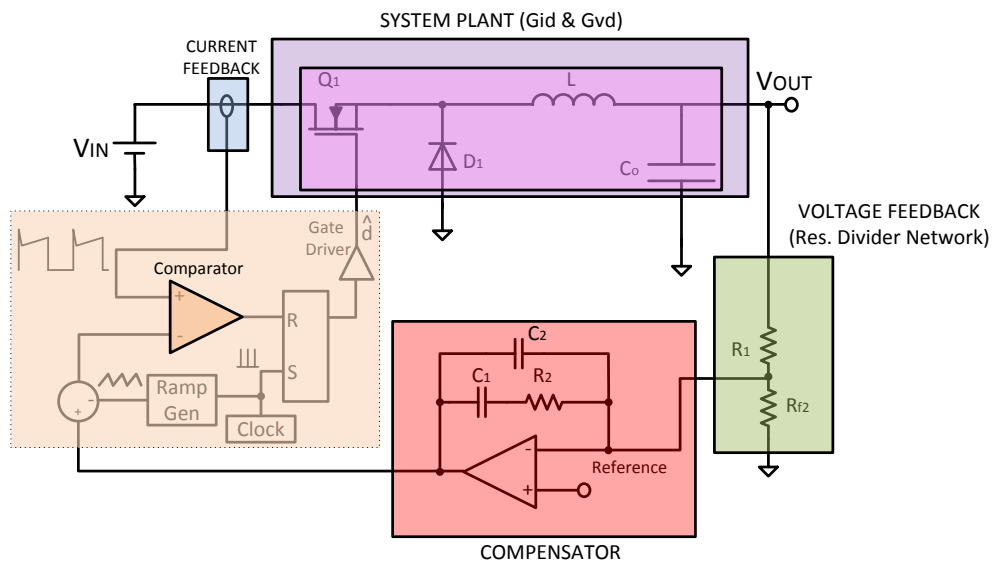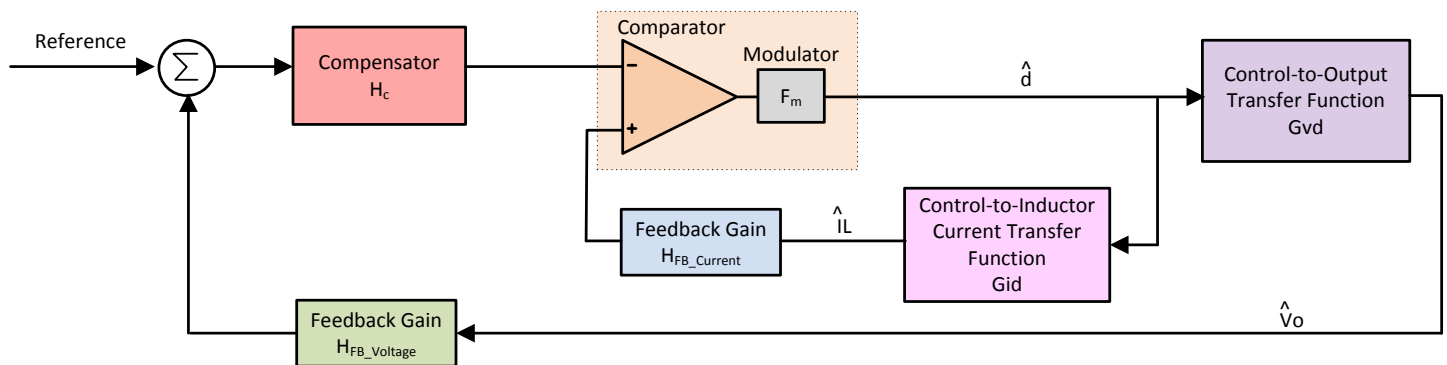

Figure 5 - DCDT Block Diagram for Peak Current Mode System

Import Existing Project

The Import Existing Project option will copy all the settings from a previously created DCDT Project into a new folder and allow the user to give a new name to the project.

New Project

When creating a new project the name and folder path are to be defined by the user, the DCDT GUI will use this folder as the active project path and all the generated GUI files will be saved in this location.

IMPORTANT: It is not possible to create two projects using the same folder path (Project Location) and the user must create an individual folder for each project.
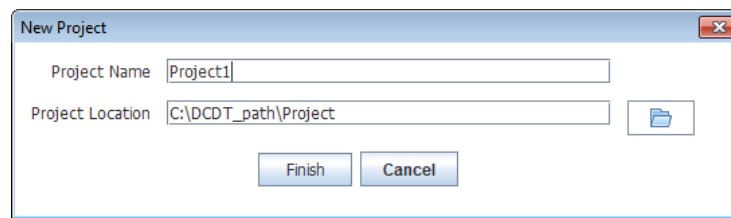
Figure 6 - New Project Name and Project Folder Location

Single-Loop System Block Diagram

Designing a Single-Loop System is a straight forward process, where the GUI will represent the power supply in three main blocks the Plant, Feedback and Compensator. The user must define each of the blocks and enter the information required by the GUI to compute the system Loop Gain and overall performance.

The tool does not require any specific order to be followed when defining the system blocks, but the following order is recommended as it will facilitate the compensator design:

1. Define the System or Plant information*
2. Define the Feedback
3. Design and optimize the Compensator

Note *: See the Related Application Notes: section for more information on how to extract the describing transfer functions from the specific hardware topologies.

Figure 7 - Single-Loop Block Diagram

Peak Current Mode System Block Diagram

Peak Current Mode systems are characterized by having two loops, an inner current loop and the outer voltage loop, the DCDT does not require any specific order to be followed when defining the system blocks, but the following order is recommended as it will facilitate the compensator design:

1. Define the Control to Inductor Current block (Gid)*
2. Define the Current Feedback
3. Provide information about the Comparator block
4. Define the Control to Output Voltage block (Gvd)*
5. Define the Voltage Feedback
6. Design and optimize the Compensator

Note *: See the Related Application Notes: section for more information on how to extract the describing transfer functions from the specific hardware topologies.
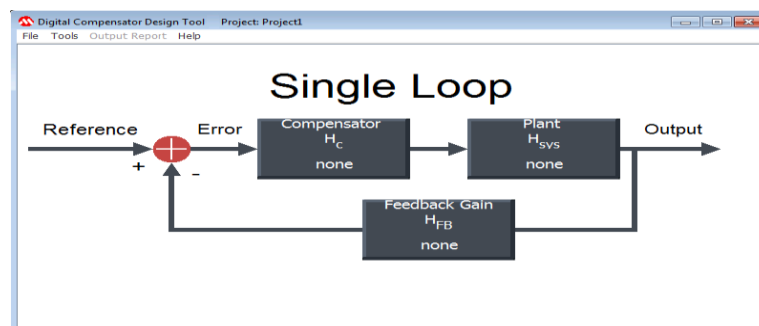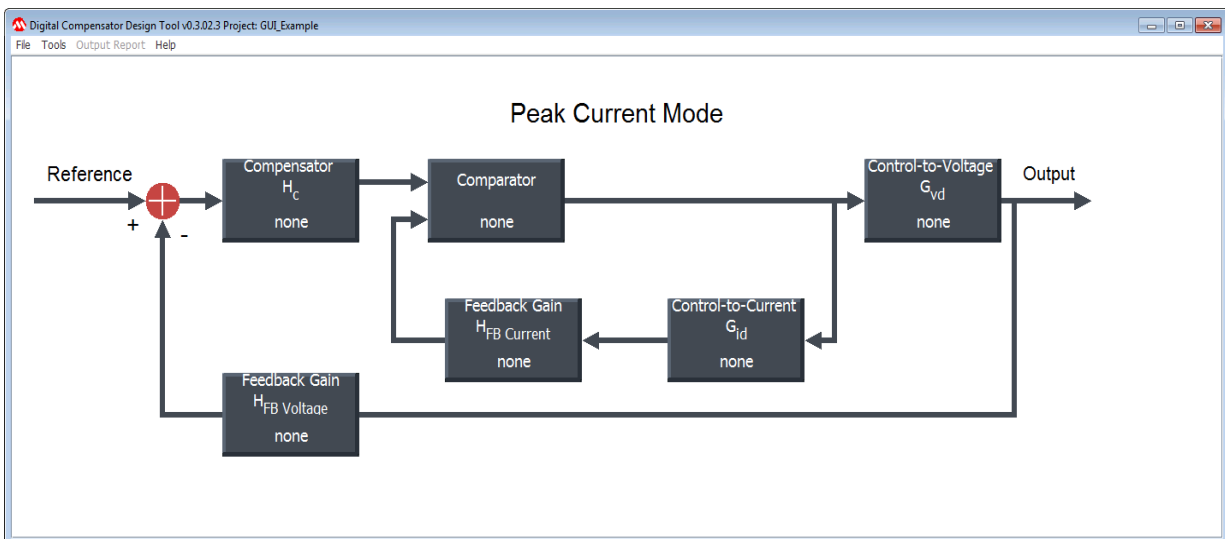

Figure 8 - Peak Current Mode System Block Diagram

Defining the System Plant

The System or Plant block defines the information about the power supply hardware that needs to be controlled, and because Microchip dsPIC® DSCs are well suited for many different power supply topologies the DCDT GUI gives the user the flexibility to define the plant using anyone of the three different methods, these are:

- Polynomial Transfer Function
- Pole Zero Transfer Function
- Import Plant Data
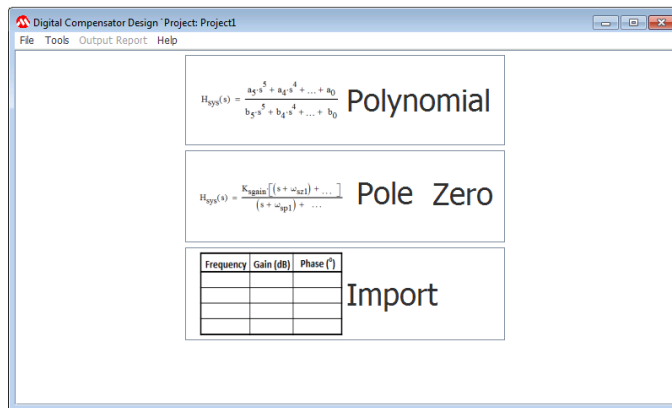
Figure 9 - Select Plant Entry Method

Plant in Polynomial Form

The User can enter the transfer function of the System or Plant by expressing this in a Polynomial form, where each of the polynomial coefficients is defined by the user.

Equation 1 - Polynomial Plant Transfer Function

$$H_{sys}(s) = \frac{a_5 \cdot s^5 + a_4 \cdot s^4 + a_3 \cdot s^3 + a_2 \cdot s^2 + a_1 \cdot s + a_0}{b_5 \cdot s^5 + b_4 \cdot s^4 + b_3 \cdot s^3 + b_2 \cdot s^2 + b_1 \cdot s + b_0}$$
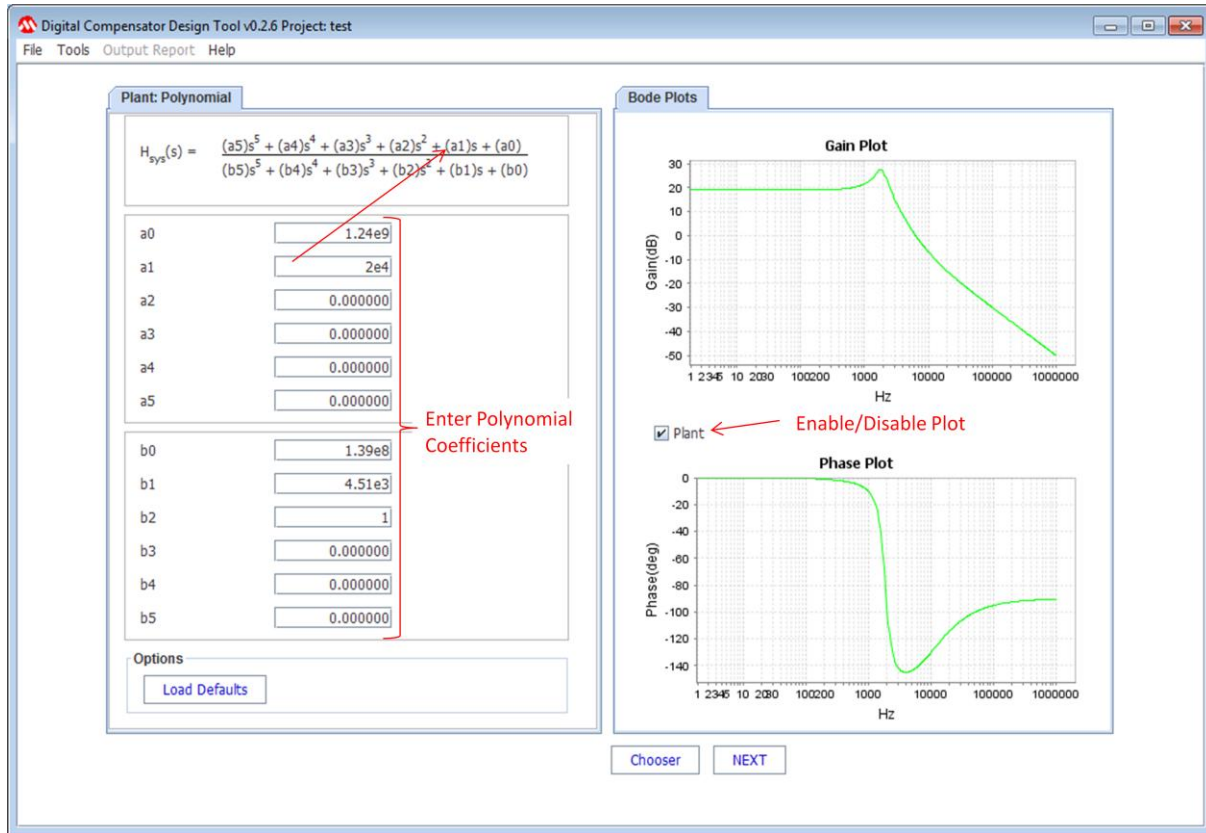
Figure 10 - Plant Polynomial Window

Plant in Pole Zero Form

The second method to enter the System Plant information is using the frequency domain Real Poles and Real Zeros, by entering the frequency location (in Hz) the GUI will compute the system transfer function and use this for all computations.

Equation 2 - Pole Zero Plant Transfer Function

$$H_{sys}(s) = \frac{K_{DC} \cdot (s + f_{z1}) \cdot (s + f_{z2}) \cdot (s + f_{z3}) \cdot (s + f_{z4}) \cdot (s + f_{z5})}{(s + f_{p1}) \cdot (s + f_{p2}) \cdot (s + f_{p3}) \cdot (s + f_{p4}) \cdot (s + f_{p5})}$$
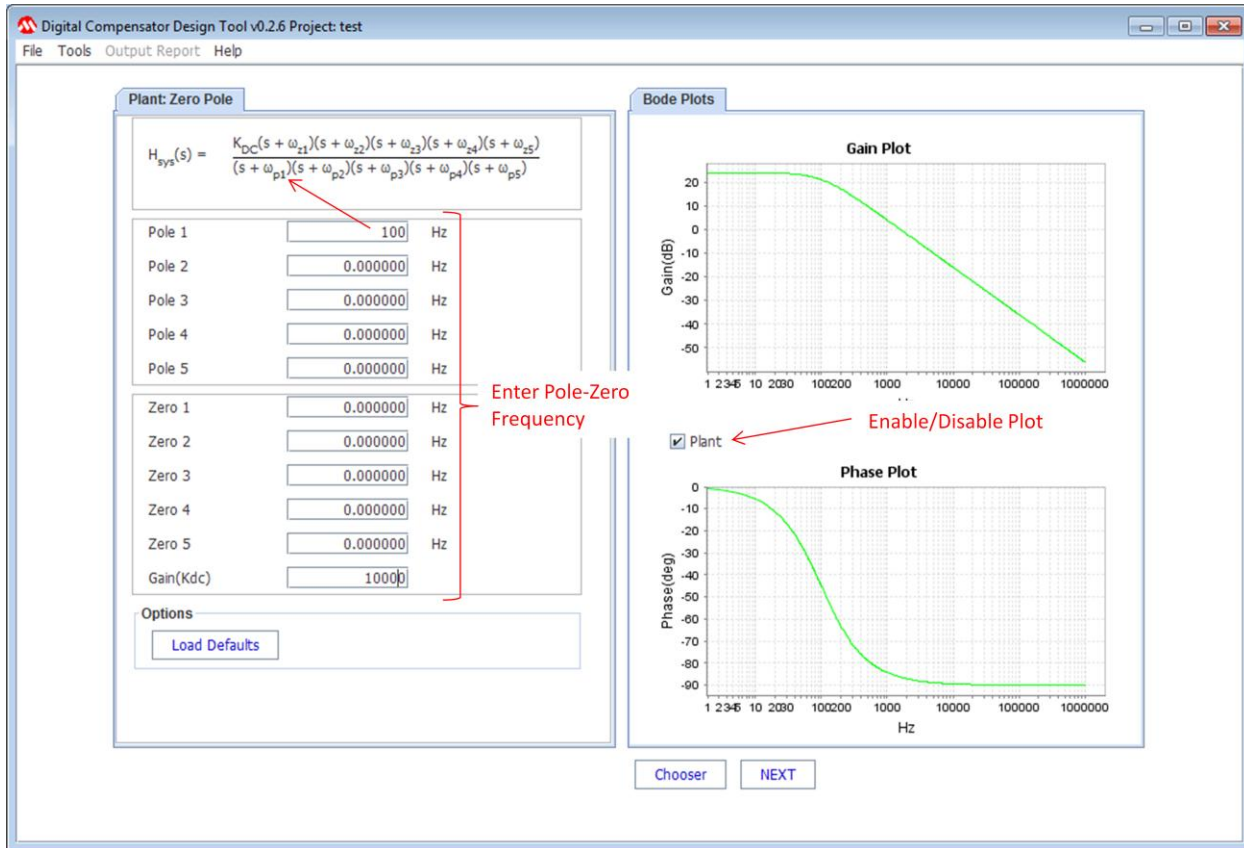
Figure 11 - Plant Pole-Zero Window

Plant Imported From

The third method to define the System Plant is by importing the Gain and Phase information as a data index using a Comma Separated Value (.CSV) file format. This allows the user to import the frequency response characteristics from real hardware measurements or data gathered using simulation tools.

The data to be imported must follow formatting guidelines:

- File must be saved as Comma Separated Values (.CSV)
- First Row will not be imported and is assumed to be the column name.
- The First Data Column will be the Frequency defined in Hertz (Hz).
- The second data column will be the Plant Gain magnitude defined in decibels (dB).
- The third data column will be the Plant Phase defined in degrees ($^{\circ}$)
- For good plant resolution it is suggested to have at least 10 data points per frequency decade, there is a maximum plant
- Frequency sweep data must be sequential and incrementally organized.

Table 1- Import Plant CSV Format Example

```
Frequency(Hz),Gain (dB),Phase (deg)
1.00E-01,35.41945333,-0.000382034
1.02E-01,35.41945333,-0.000389137
1.04E-01,35.41945333,-0.000396372
1.06E-01,35.41945333,-0.000403741
1.08E-01,35.41945333,-0.000411247
1.10E-01,35.41945333,-0.000418892
       .          .          .
       .          .          .
       .          .          .
5058246.62,-76.45228426,-95.43259287
5152286.446,-76.61369508,-95.3340156
```

Using the File Browser Menu locate the data file you and once the data is successfully imported this will be displayed inside the GUI window as shown in Figure 12- Import Plant Window below.
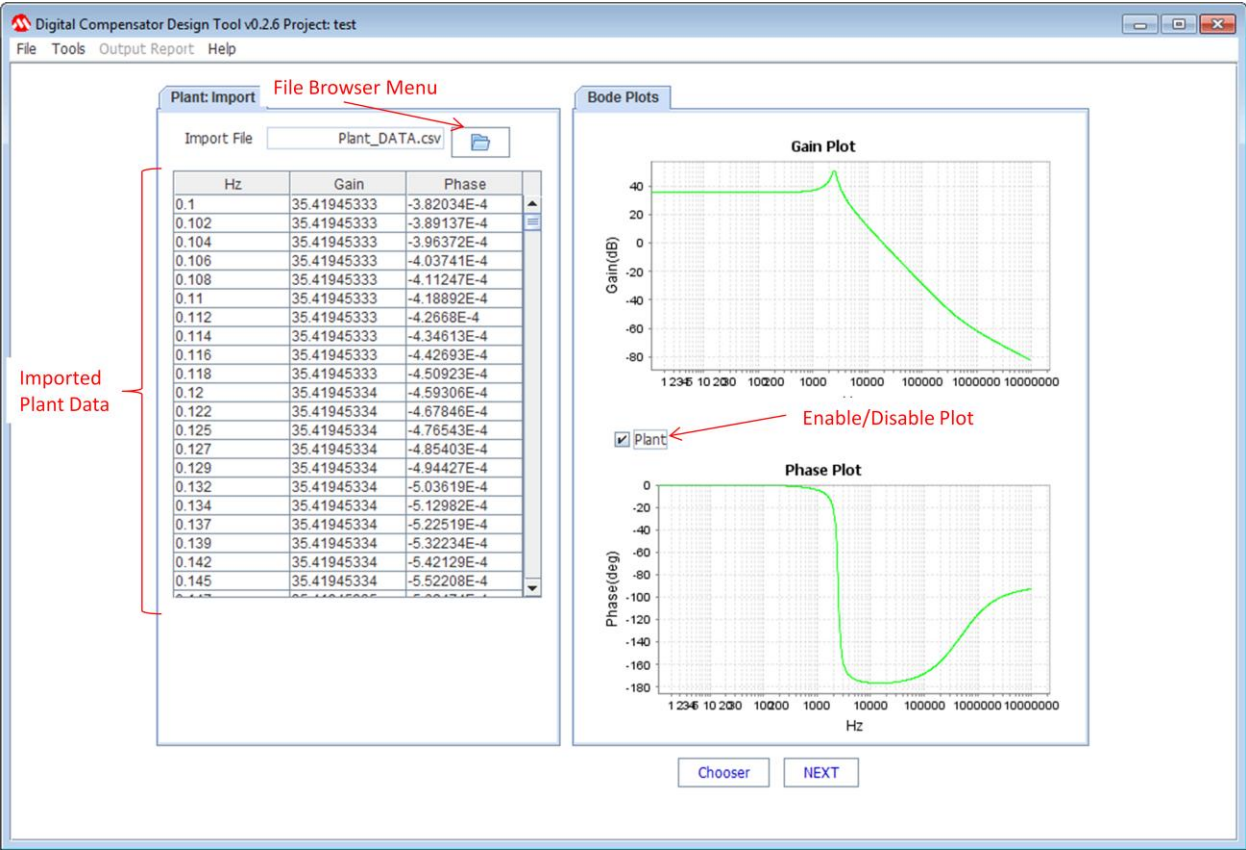

Figure 12- Import Plant Window

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Defining the Feedback

There are many different methods to measure a signal and these can vary from using a simple resistor divider network to more complex sensing circuits that use operational amplifiers or opto-isolators, for this reason and in order to accommodate for the various kinds of feedback networks, the GUI supports two different methods to define the Feedback used.

- Resistor-Capacitor Network
- Fixed Gain limited bandwidth sensor
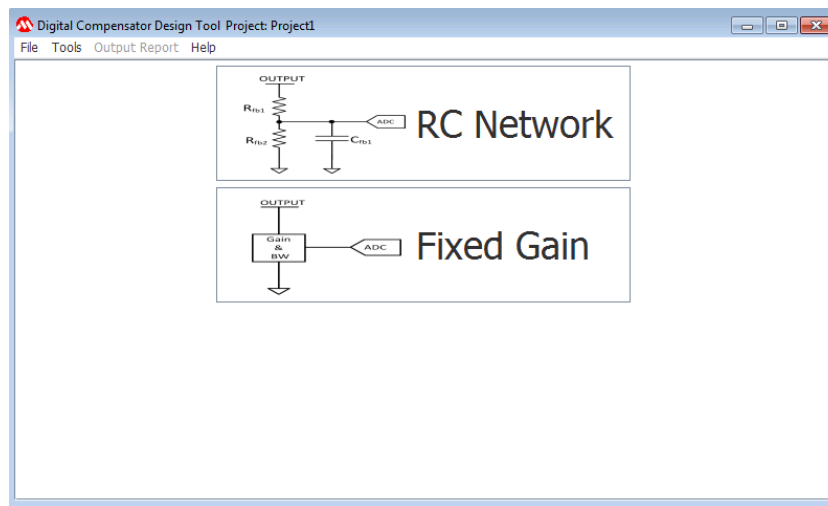
Figure 13 - Feedback Type Select Window

Resistor-Capacitor Feedback Network

Using the Resistor-Capacitor (RC) Feedback Network allows the user to enter specific resistor divider values and the capacitor used for the feedback. This network introduces an attenuation factor and also behaves as a low pass filter limiting signals beyond the frequency of interest.

In this window the user must also define the characteristics of the Analog-to-Digital Converter (ADC), the user should use the values defined in the specific dsPIC® DSC datasheet.

- **ADC Resolution**: This is determined by the dsPIC® DSC hardware and the number of bits of resolution of the ADC module.
- **ADC Latency**: This value needs to account for the delay introduced by the Sample&Hold and Conversion delay (for dsPIC33F family this is typically ~600ns)
- **ADC Operating Voltage**: This is the maximum voltage range of the ADC module

Note: For more information about ADC Module see the Family Datasheets and Reference Manual Documents section.

Figure 14 - RC Feedback Network Window

Fixed Gain Feedback Network

This Feedback option allows the user to define a constant gain with a limited bandwidth sensor. This enables the GUI to model the feedback system without having to model complex Op-amp based circuitry configurations.

In this window the user must also define the characteristics of the Analog to Digital Converter (ADC), the user should use the values defined in the specific dsPIC® DSC datasheet.

- **ADC Resolution**: This is determined by the dsPIC® DSC hardware and the number of bits of resolution of the ADC module.
- **ADC Latency**: This value needs to account for the delay introduced by the Sample&Hold and Conversion delay (for dsPIC33F family this is typically ~600ns)
- **ADC Operating Voltage**: This is the maximum voltage range of the ADC module

Note: For more information about ADC Module see the Family Datasheets and Reference Manual Documents section.
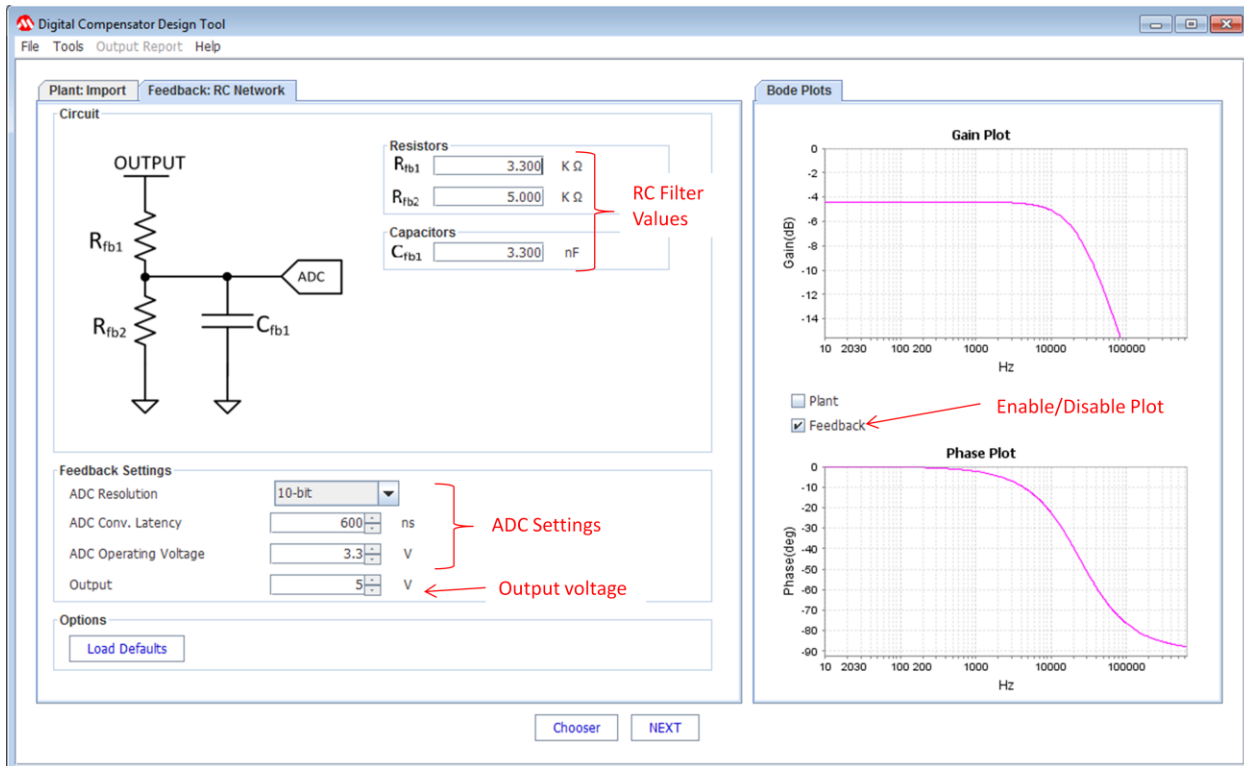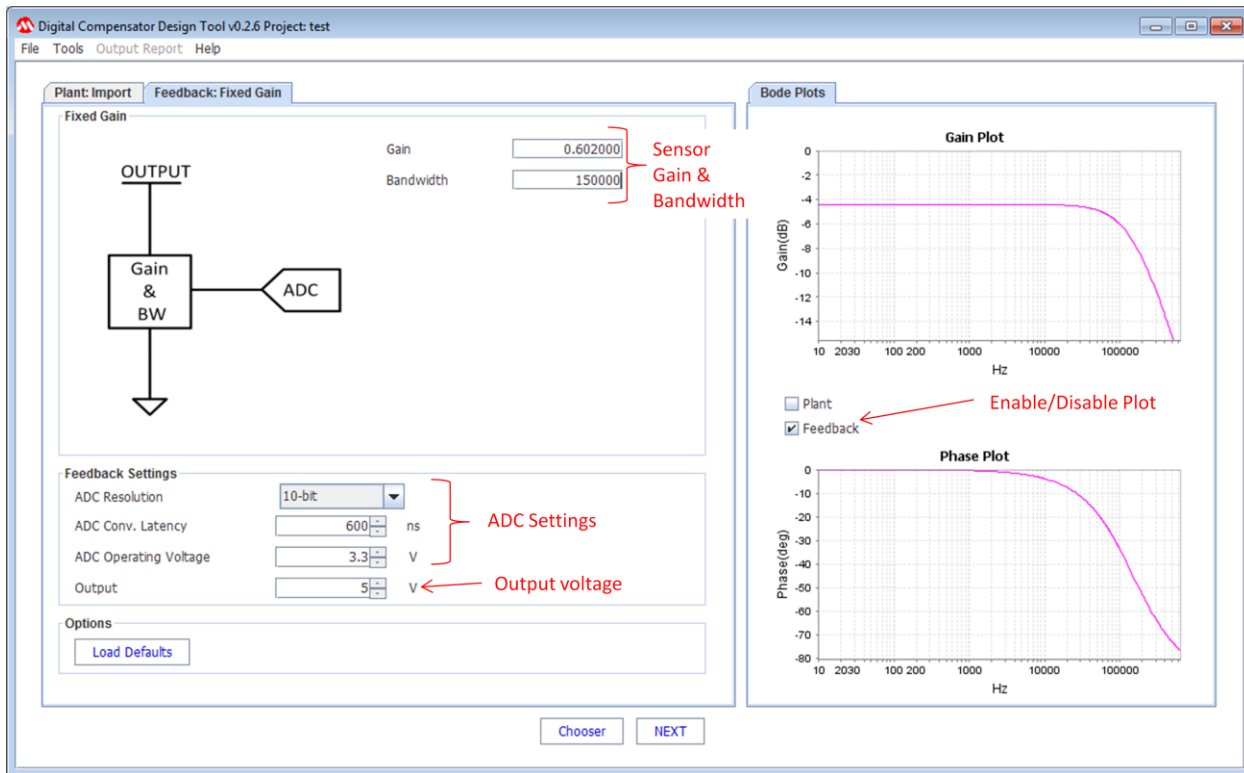
Figure 15 - Fixed Gain Feedback Window

Selecting the Compensator

The DCDT allows the user to select between different types of compensators and the user is encouraged to explore the different available options to determine the one that achieves the best overall system performance.

This DCDT GUI release version includes the following compensators types:

- Three- Pole, Three Zero (3P3Z) Compensator
- Two- Pole, Two Zero (2P2Z) Compensator
- Proportional Integral Derivative (PID) Compensator
- Analog Op-Amp Type III Compensator
- Analog Op-Amp Type II Compensator

The Compensator Select Window, shown in Figure 16 below, allows the user make a selection by clicking on the compensator of interest.
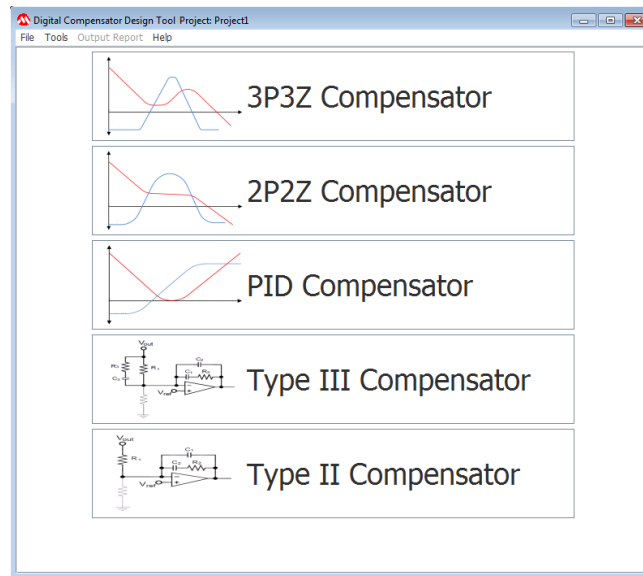
Figure 16 - Compensator Select Window

3P3Z Compensator:

The 3P3Z Compensator is the digital implementation of the analog type III controller, this is a filter which introduces a specific Gain and Phase boost into the system by considering three poles and two zeros, see Figure 17 - 3P3Z Compensator Phase and Gain Characteristics. The User must strategically select the frequency placement for each of the Poles and Zeros that will help achieve the desired system performance. In this figure the (-1) slope is the equivalent to -20dB/decade and the (+1) slope to +20dB/decade.
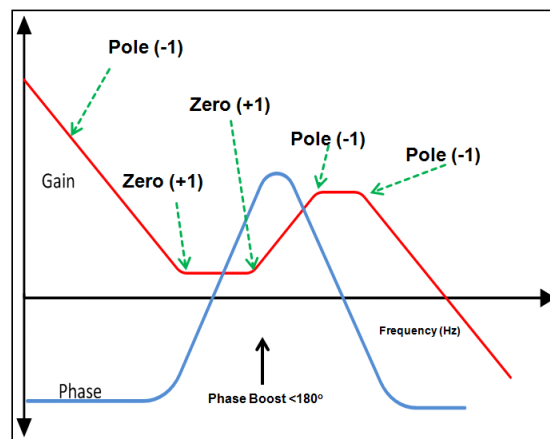
Figure 17 - 3P3Z Compensator Phase and Gain Characteristics

Equation 3 - 3P3Z Compensator Transfer Function

$$H_c(s) = K_{DC} \cdot \frac{\omega_{p0}}{s} \cdot \frac{\left(1 + \dfrac{s}{\omega_{z1}}\right)\left(1 + \dfrac{s}{\omega_{z2}}\right)}{\left(1 + \dfrac{s}{\omega_{p2}}\right)\left(1 + \dfrac{s}{\omega_{p3}}\right)}$$

The DCDT 3P3Z Compensator Design Window is shown in Figure 18, in this window the user must enter the specific information about the hardware configuration along with compensator settings, this includes:

- **Poles / Zero Frequency**: The location in the frequency domain where the pole or zero should be placed.

- **PWM Switching Frequency**: This is the operating frequency of the power switch (e.g., MOSFET) and this will be defined by the microcontroller Time Base Period Register.

- **PWM Sampling Ratio**: The DCDT will use this value to calculate the sampling frequency as a function of the PWM Switching Frequency
    - Sampling Frequency = (PWM Switching Frequency / PWM Sampling Ratio)
    - For example, use the Trigger # Output Divider bits to configure trigger event register and enable specific hardware sampling frequency, see *dsPIC33/PIC24 Family Reference Manual* for more details

- **PWM Maximum Resolution**: Depending on hardware configuration settings the PWM resolution will change, this value will be used to compute the PWM gain value, see *dsPIC33/PIC24 Family Reference Manual* for more details.

- **Computational Delay**: This is the time it takes for the microcontroller to execute the selected compensator mathematical algorithm, the DCDT will use the default values as defined in Table 2 of this document. It is important for the user to understand that this delay will not impact the calculated digital compensator coefficients, but it will have an impact on the overall system loop gain (closed-loop) phase margin.

- **Gate Drive Delay**: This is the delay associated with the hardware gate-driver + MOSFET delays, (see section on GUI default values). It is important for the user to understand that that this delay will not have an impact on the calculated digital compensator coefficients, but it will impact the overall system loop gain (closed-loop) phase margin.

- **Control Output Min/Max**: These are integer values that will be used as the absolute max/min clamping limits for the compensator output, this value clamps the value written to the target register and will have no effects to the internal compensator computations.

- **Load Defaults**: This button option will load the DCDT default values for the selected compensator (see section on GUI default values).

- **Use Radian Per Second:** Enabling this option allows the user to input the Poles and Zeros location using radians per second (Rad/sec) instead of using Hertz (Hz). It should be noted that no other parameters or bode plots would be represented in radians per second.

- **Enable Frequency Warp:** This feature will enable each of the Pole/Zero frequencies to be Pre-Warped to ensure correct placement when mapped in the s-plane and that is bounded by the Nyquist frequency ($F_{Nyquist}$ = Sampling Frequency /2) .

- **Use Complex Zeros:** By enabling this option, the tool enables the user to place a Complex-Conjugate pair of zeros, where the Frequency and Damping Ratio must be entered by the user.
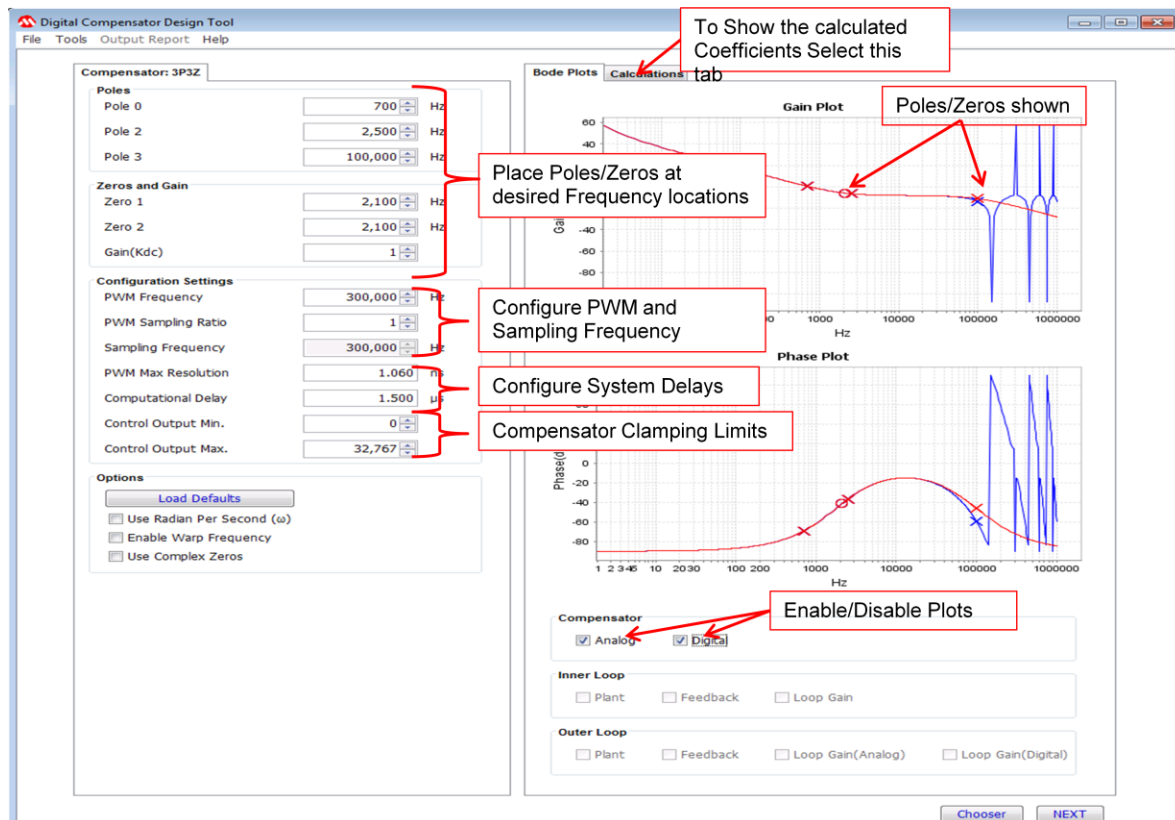

Figure 18 - 3P3Z Compensator Design Window

2P2Z Compensator:

The 2P2Z Compensator is the digital implementation of the analog type II controller, this is a filter which introduces a specific Gain and Phase boost into the system by considering two poles and one zero, see Figure 19 - 2P2Z Compensator Phase and Gain Characteristics. The User must strategically select the Frequency placement for each of the Poles and the Zero that will help achieve the desired system performance. In this figure the (-1) slope is the equivalent to -20dB/decade and the (+1) slope to +20dB/decade.
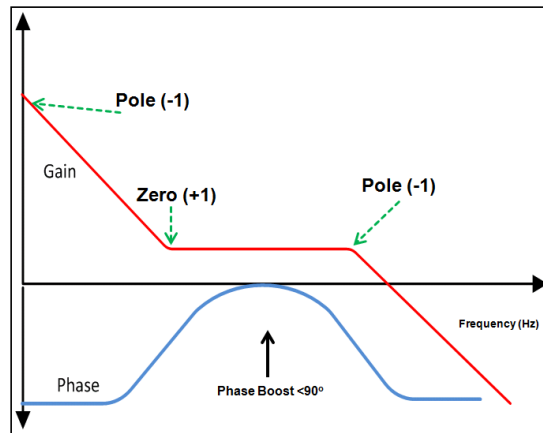
Figure 19 - 2P2Z Compensator Phase and Gain Characteristics

Equation 4 - 2P2Z Compensator Transfer Function below shows the mathematical transfer function for the 2P2Z Compensator:

Equation 4 - 2P2Z Compensator Transfer Function

$$H_c(s) = K_{DC} \cdot \frac{\omega_{p0}}{s} \cdot \frac{\left(1 + \dfrac{s}{\omega_{z1}}\right)}{\left(1 + \dfrac{s}{\omega_{p2}}\right)}$$

The 2P2Z Compensator Design Window is shown in Figure 20, in this window the user must enter the specific information about the hardware configuration along with compensator settings, this includes:

- **Poles / Zero Frequency**: The location in the frequency domain where the poles or zero should be placed.

- **PWM Switching Frequency**: This is the operating frequency of the power switch (e.g., MOSFET) and this will be defined by the microcontroller Time Base Period Register.

- **PWM Sampling Ratio**: The DCDT will use this value to calculate the sampling frequency as a function of the PWM Switching Frequency
    - o   Sampling Frequency = (PWM Switching Frequency / PWM Sampling Ratio)

- o For example, use the Trigger # Output Divider bits to configure trigger event register and enable specific hardware sampling frequency, see *dsPIC33/PIC24 Family Reference Manual* for more details

- **PWM Maximum Resolution**: Depending on hardware configuration settings the PWM resolution will change, this value will be used to compute the PWM gain value, see *dsPIC33/PIC24 Family Reference Manual* for more details.

- **Computational Delay**: This is the time it takes for the microcontroller to execute the selected compensator mathematical algorithm, the DCDT will use the default values as defined in Table 2 of this document. It is important for the user to understand that this delay will not impact the calculated digital compensator coefficients, but it will have an impact on the overall system loop gain (closed-loop) phase margin.

- **Gate Drive Delay**: This is the delay associated with the hardware gate-driver + MOSFET delays, (see section on GUI default values). It is important for the user to understand that that this delay will not have an impact on the calculated digital compensator coefficients, but it will impact the overall system loop gain (closed-loop) phase margin.

- **Control Output Min/Max**: These are integer values that will be used as the absolute max/min clamping limits for the compensator output, this value clamps the value written to the target register and will have no effects to the internal compensator computations.

- **Load Defaults**: This button option will load the DCDT default values for the selected compensator (see section on GUI default values).

- **Use Radian Per Second:** Enabling this option allows the user to input the Poles and Zeros location using radians per second (Rad/sec) instead of using Hertz (Hz). It should be noted that no other parameters or bode plots would be represented in radians per second.

- **Enable Frequency Warp:** This feature will enable each of the Pole/Zero frequencies to be Pre-Warped to ensure correct placement when mapped in the s-plane and that is bounded by the Nyquist frequency ($F_{Nyquist}$ = Sampling Frequency /2).
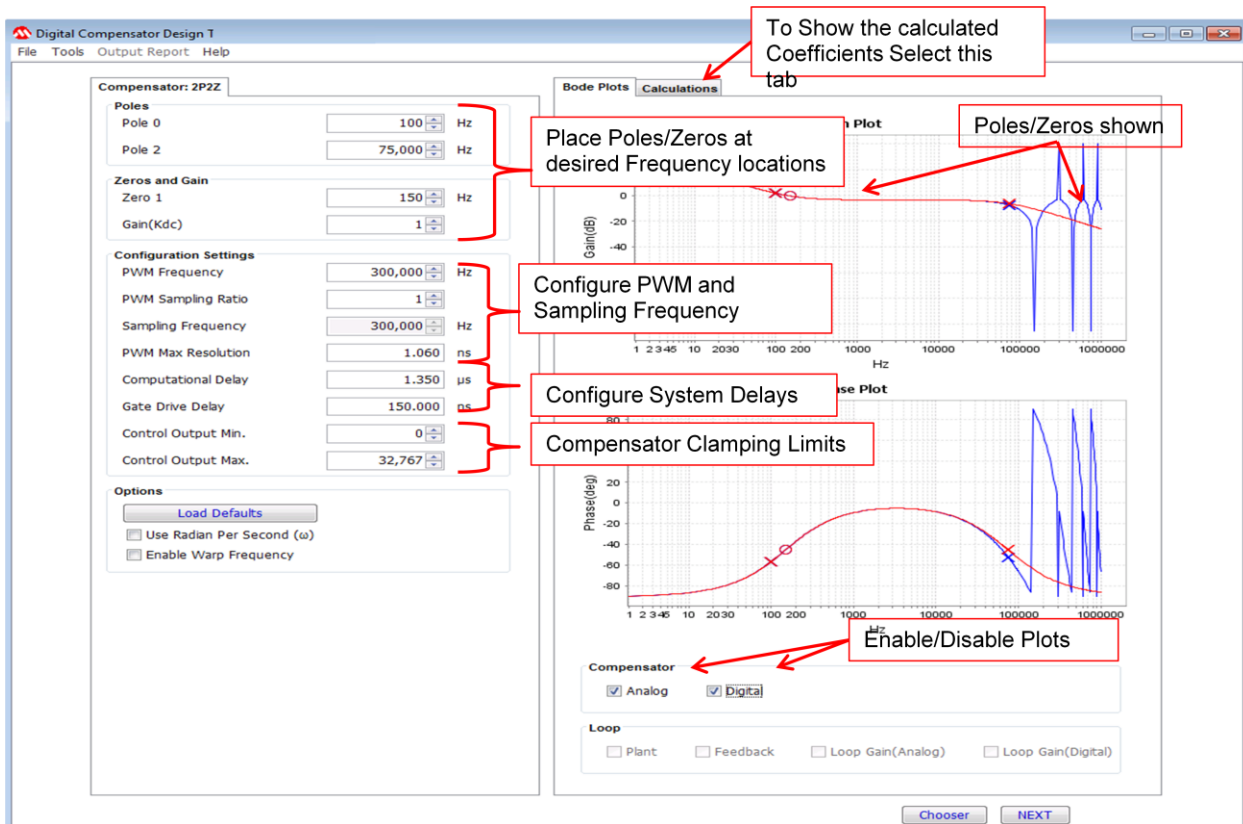
Figure 20- 2P2Z Compensator Design Window

PID Compensator:

The Proportional Integral Derivative (PID) compensator enables the user to optimize the frequency response of the filter by using three (3) gain coefficients, these are the Proportional Gain (Kp), Integral Gain (Ki) and Differential Gain (Kd). The user might also choose to tune this controller by selecting the placement frequency for the single pole and two zeros, see Figure 21 - PID Compensator Phase and Gain Characteristics shown below. In this figure the (-1) slope is the equivalent to -20dB/decade and the (+1) slope to +20dB/decade.
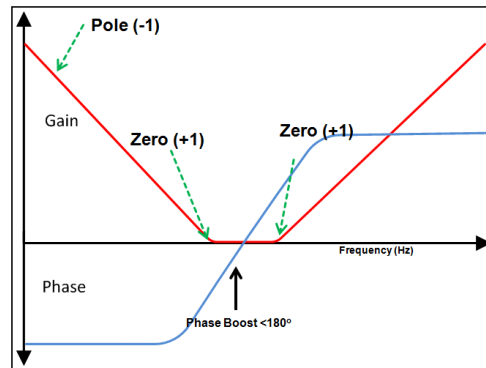

Figure 21 - PID Compensator Phase and Gain Characteristics

Equation 5 - PID Compensator Transfer Function is shown below.

Equation 5 - PID Compensator Transfer Function

$$H_{C(s)} = K_p + \frac{Ki}{s} + K_d s = \frac{K_p s + K_i + K_d s^2}{s}$$

The PID Compensator Design Window is shown in Figure 22 - PID Compensator Design Window in this window the user must enter the specific information about the hardware configuration along with compensator settings, this includes:

- **PID Gains:** User can define the gains for the Proportional, Integral and Derivative gains
- **Pole / Zeros Frequency**: Based on the PID Gains defined, the DCDT will calculate and display the Frequency location of the Pole (at origin) and the two Zeros of the compensator.
- **PWM Switching Frequency**: This is the operating frequency of the power switch (e.g., MOSFET) and this will be defined by the microcontroller Time Base Period Register.
- **PWM Sampling Ratio**: The DCDT will use this value to calculate the sampling frequency as a function of the PWM Switching Frequency
    - o Sampling Frequency = (PWM Switching Frequency / PWM Sampling Ratio)

- o For example, use the Trigger # Output Divider bits to configure trigger event register and enable specific hardware sampling frequency, see *dsPIC33/PIC24 Family Reference Manual* for more details
- **PWM Maximum Resolution**: Depending on hardware configuration settings the PWM resolution will change, this value will be used to compute the PWM gain value, see *dsPIC33/PIC24 Family Reference Manual* for more details.
- **Computational Delay**: This is the time it takes for the microcontroller to execute the selected compensator mathematical algorithm, the DCDT will use the default values as defined in Table 2 of this document. It is important for the user to understand that this delay will not impact the calculated digital compensator coefficients, but it will have an impact on the overall system loop gain (closed-loop) phase margin.
- **Gate Drive Delay**: This is the delay associated with the hardware gate-driver + MOSFET delays, (see section on GUI default values). It is important for the user to understand that that this delay will not have an impact on the calculated digital compensator coefficients, but it will impact the overall system loop gain (closed-loop) phase margin.
- **Control Output Min/Max**: These are integer values that will be used as the absolute max/min clamping limits for the compensator output, this value clamps the value written to the target register and will have no effects to the internal compensator computations.
- **Load Defaults**: This button option will load the DCDT default values for the selected compensator (see section on GUI default values).
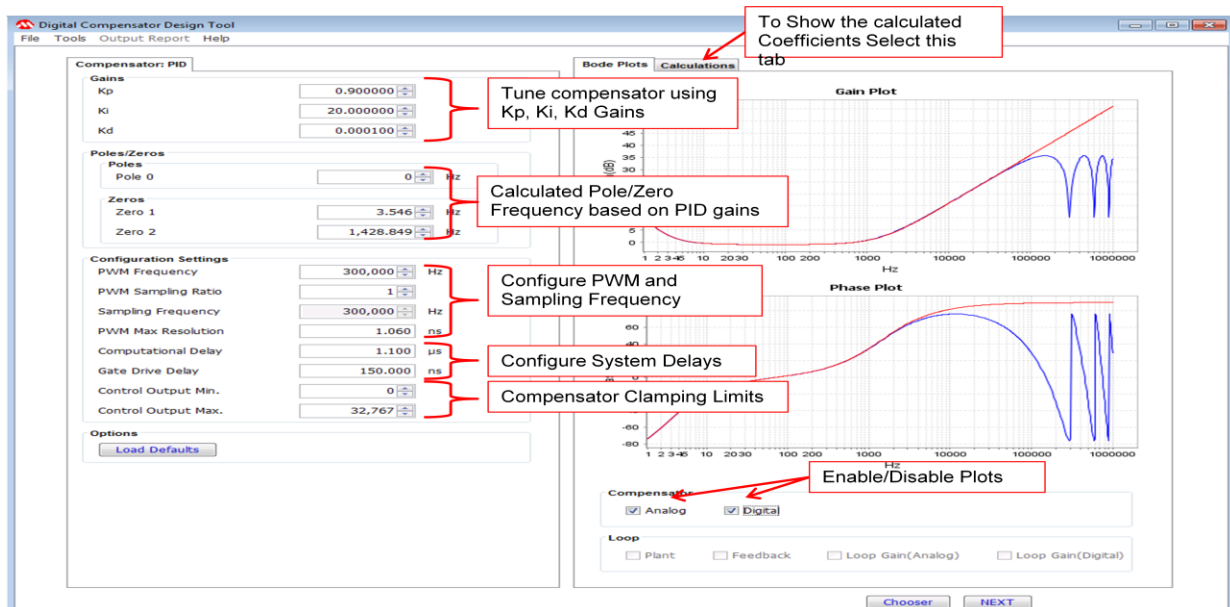

Figure 22 - PID Compensator Design Window

Type III Analog Compensator:

This compensator was designed to aid power supply designers transition a Type III Analog compensator that uses resistors, capacitors and one operational amplifier circuit (Figure 23 - Type III Analog Compensator Circuit) into a digital compensator to produce a specific frequency response filter. The user of the DCDT can enter the values of the resistors and capacitors and based on these values the DCDT will calculate the corresponding location of the compensator Poles and Zeros. The user can choose to generate the coefficients for the equivalent digital compensator or use these calculations as the starting point to further optimize the performance of the compensator.
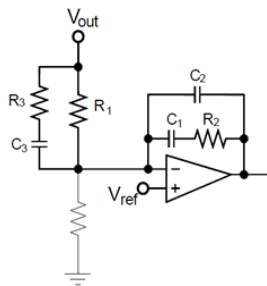

Figure 23 - Type III Analog Compensator Circuit

The Type III Analog Compensator Design Window is shown in Figure 24, in this window the user must enter the specific information about the hardware configuration along with compensator settings, this includes:

- **Resistor/Capacitor Values:** Define component values for the resistor and capacitors as shown on circuit diagram.
- **Pole / Zeros Frequency**: Based on the component values for the resistors and capacitors the DCDT will calculate the Frequency location of the Poles and the Zeros and displayed, if the user wants to optimize the compensator by adjusting the Pole/Zeros frequencies they must enable the "Pole/Zero" checkbox. The resistor and capacitor component values will not be recalculated based on the Pole/Zero frequency placement.
- **PWM Switching Frequency**: This is the operating frequency of the power switch (e.g., MOSFET) and this will be defined by the microcontroller Time Base Period Register.
- **PWM Sampling Ratio**: The DCDT will use this value to calculate the sampling frequency as a function of the PWM Switching Frequency
    - o Sampling Frequency = (PWM Switching Frequency / PWM Sampling Ratio)

- For example, use the Trigger # Output Divider bits to configure trigger event register and enable specific hardware sampling frequency, see *dsPIC33/PIC24 Family Reference Manual* for more details

- **PWM Maximum Resolution**: Depending on hardware configuration settings the PWM resolution will change, this value will be used to compute the PWM gain value, see *dsPIC33/PIC24 Family Reference Manual* for more details.

- **Computational Delay**: This is the time it takes for the microcontroller to execute the selected compensator mathematical algorithm, the DCDT will use the default values as defined in Table 2 of this document. It is important for the user to understand that this delay will not impact the calculated digital compensator coefficients, but it will have an impact on the overall system loop gain (closed-loop) phase margin.

- **Gate Drive Delay**: This is the delay associated with the hardware gate-driver + MOSFET delays, (see section on GUI default values). It is important for the user to understand that that this delay will not have an impact on the calculated digital compensator coefficients, but it will impact the overall system loop gain (closed-loop) phase margin.

- **Control Output Min/Max**: These are integer values that will be used as the absolute max/min clamping limits for the compensator output, this value clamps the value written to the target register and will have no effects to the internal compensator computations.

- **Load Defaults**: This button option will load the DCDT default values for the selected compensator (see section on GUI default values).

- **Use Radian Per Second:** Enabling this option allows the user to input the Poles and Zeros location using radians per second (Rad/sec) instead of using Hertz (Hz). It should be noted that no other parameters or bode plots would be represented in radians per second.

- **Enable Frequency Warp:** This feature will enable each of the Pole/Zero frequencies to be Pre-Warped to ensure correct placement when mapped in the s-plane and that is bounded by the Nyquist frequency ($F_{Nyquist}$ = Sampling Frequency /2).

- **Use Complex Zeros:** By enabling this option, the tool enables the user to place a Complex-Conjugate pair of zeros, where the Frequency and Damping Ratio must be entered by the user.
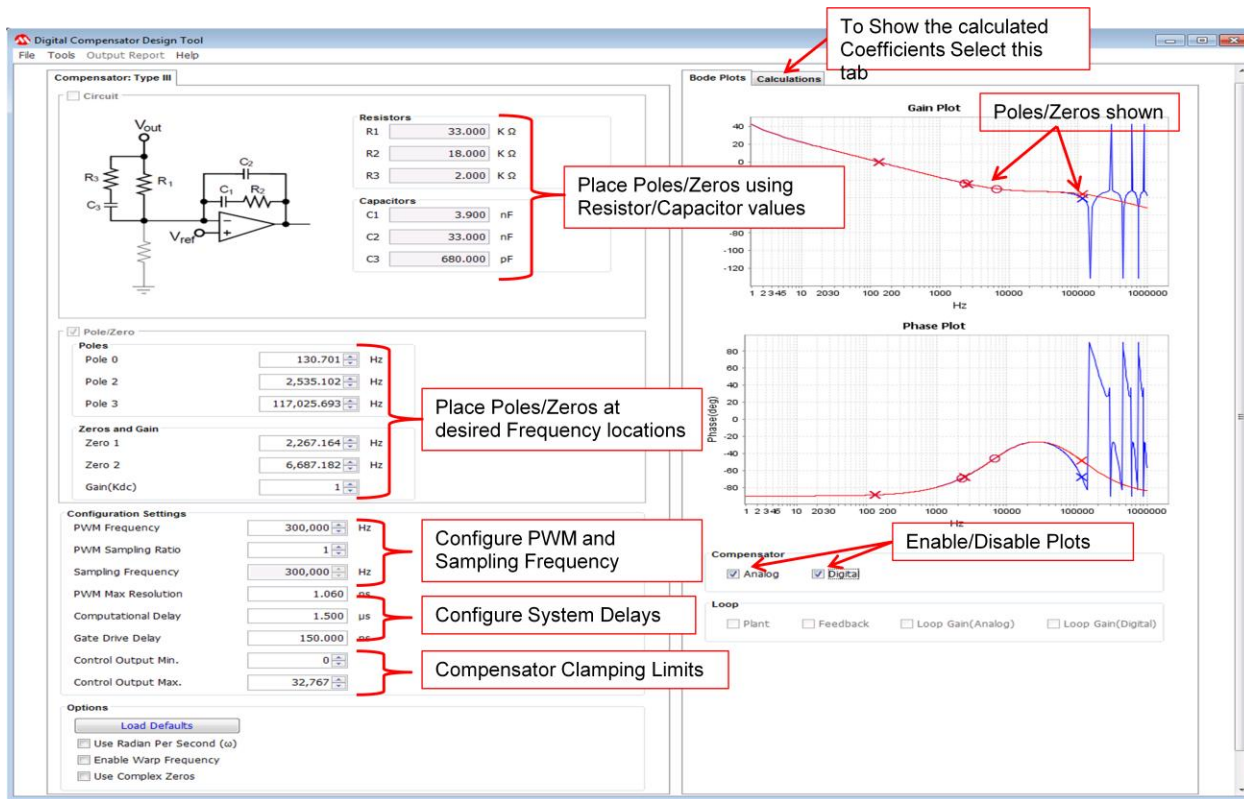
Figure 24 - Analog Type III Compensator Design Window

Type II Analog Compensator:

This compensator was designed to aid power supply designers transition a Type II Analog compensator that uses resistors, capacitors and one operational amplifier circuit (Figure 25 - Type II Analog Compensator Circuit) into a digital compensator to produce a specific frequency response filter. The user of the DCDT can enter the values of the resistors and capacitors and based on these values the DCDT will calculate the corresponding location of the compensator two Poles and one Zero. The user can choose to generate the coefficients for the equivalent digital compensator or use these calculations as the starting point to further optimize the performance of the compensator.
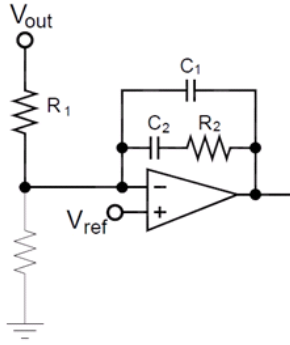
The Type II Analog Compensator Design Window is shown in Figure 26, in this window the user must enter the specific information about the hardware configuration along with compensator settings, this includes:

- **Resistor/Capacitor Values:** Define component values for the resistor and capacitors as shown on circuit diagram.

- **Pole / Zeros Frequency**: Based on the component values for the resistors and capacitors the DCDT will calculate the Frequency location of the Poles and the Zeros and displayed, if the user wants to optimize the compensator by adjusting the Pole/Zeros frequencies they must enable the "Pole/Zero" checkbox. The resistor and capacitor component values will not be recalculated based on the Pole/Zero frequency placement.

- **PWM Switching Frequency**: This is the operating frequency of the power switch (e.g., MOSFET) and this will be defined by the microcontroller Time Base Period Register.

- **PWM Sampling Ratio**: The DCDT will use this value to calculate the sampling frequency as a function of the PWM Switching Frequency

    o   Sampling Frequency = (PWM Switching Frequency / PWM Sampling Ratio)

    o   For example, use the Trigger # Output Divider bits to configure trigger event register and enable specific hardware sampling frequency, see *dsPIC33/PIC24 Family Reference Manual* for more details

- **PWM Maximum Resolution**: Depending on hardware configuration settings the PWM resolution will change, this value will be used to compute the PWM gain value, see *dsPIC33/PIC24 Family Reference Manual* for more details.

- **Computational Delay**: This is the time it takes for the microcontroller to execute the selected compensator mathematical algorithm, the DCDT will use the default values as defined in Table 2 of this document. It is important for the user to understand that this delay will not impact the calculated

digital compensator coefficients, but it will have an impact on the overall system loop gain (closed-loop) phase margin.

- **Gate Drive Delay**: This is the delay associated with the hardware gate-driver + MOSFET delays, (see section on GUI default values). It is important for the user to understand that that this delay will not have an impact on the calculated digital compensator coefficients, but it will impact the overall system loop gain (closed-loop) phase margin.

- **Control Output Min/Max**: These are integer values that will be used as the absolute max/min clamping limits for the compensator output, this value clamps the value written to the target register and will have no effects to the internal compensator computations.

- **Load Defaults**: This button option will load the DCDT default values for the selected compensator (see section on GUI default values).

- **Use Radian Per Second:** Enabling this option allows the user to input the Poles and Zeros location using radians per second (Rad/sec) instead of using Hertz (Hz). It should be noted that no other parameters or bode plots would be represented in radians per second.

- **Enable Frequency Warp:** This feature will enable each of the Pole/Zero frequencies to be Pre-Warped to ensure correct placement when mapped in the s-plane and that is bounded by the Nyquist frequency ($F_{Nyquist}$ = Sampling Frequency /2).
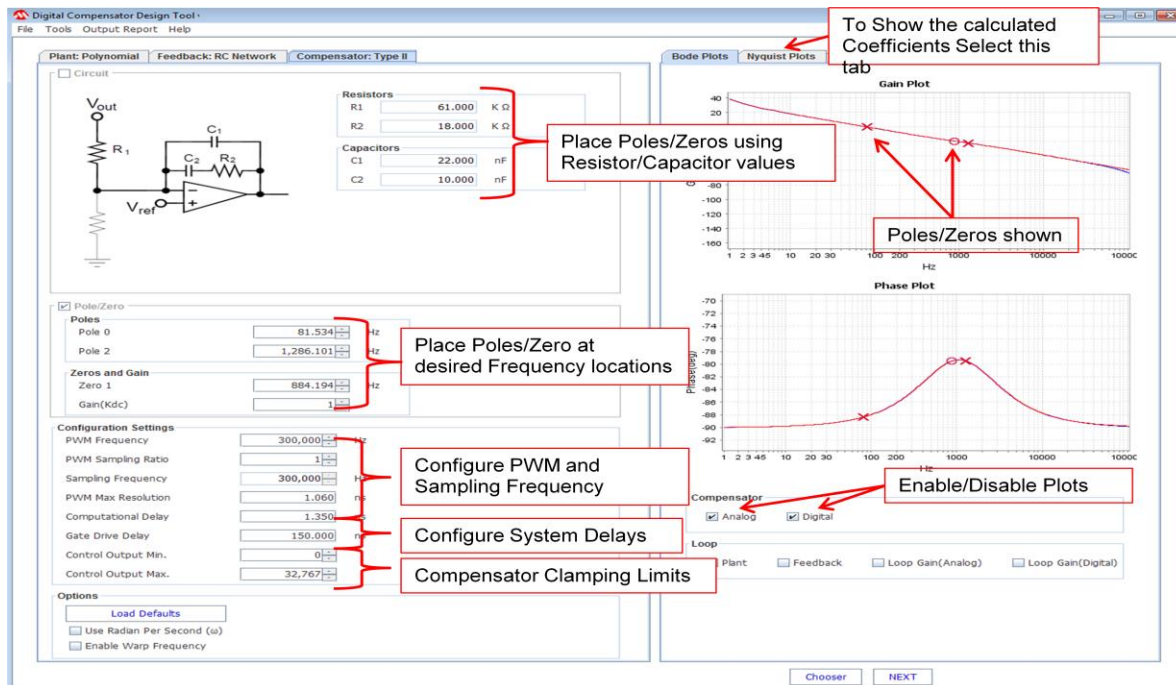

Figure 26 - Analog Type II Compensator Design Window

What Compensator type should I select?

Type II Analog and Digital 2P2Z Converter

These converter types are required when the Phase boost is less than 90° and the System-Plant dominant pole is of determined to be of the first-order, such in the case of a Current-Mode Buck converter where the dominant system pole is a function of the load resistance, times the output capacitance.

Type III Analog and Digital 3P3Z Converter

These converter types are required when the Phase boost is between 90° and <180° or when the System-Plant dominant pole is determined to be of the second-order, such in the case of a Voltage-Mode Buck converter where the dominant system pole is a function of the output inductor and the output capacitance.

PID Converter

This converter is considered to be an excellent compensator for different applications and it involves the tuning of three specific parameters Kp, Ki, Kd gain terms, these gains are used to modify the Phase boost and Gain margins of the loop-gain (closed-loop). This compensator allows the user the placement of the compensator Origin Pole and two Zeros.

IMPORTANT: Compensator Coefficients are computed based on specific hardware configuration settings, if these hardware settings change, the user must recalculate the compensator coefficients.

How are the Coefficients calculated?

The DCDT uses mathematical approximations, such as the Bilinear-Tustin Approximation and the Backward Euler Approximation (applies to PID compensator only) to calculate the coefficients for each of the supported compensators, by using these transformations it is possible to simplify the computations required to map the s-domain (continuous time domain) transfer function of our compensator into the z-domain (discrete time domain).

Equation 6 - Backward Euler Approximation

$$s = \frac{(z-1)}{T_s \cdot z}$$

Equation 7- Bilinear or Tustin Approximation

$$s = \frac{2}{T_s} \cdot \frac{(z-1)}{(z+1)}$$

Where:

Ts is the Sampling period

The GUI will display the calculated coefficients for the selected compensator and these will be shown in the Compensator Calculation Tab as shown in figure below.

| (a) | (b) |

Figure 27 - GUI Calculated Coefficients, (a) Floating Point Coefficients, (b) Normalized Coefficients

Once the coefficients are calculated these will be normalized and optimized for Fixed-Point math by the DCDT, and the hardware can implement these coefficients using Microchip's SMPS Control Library. This means that the User of the DCDT can focus on the placement of the compensator Poles / Zeros to meet the desired system performance and the tool will generate the digital equivalent coefficients that will represent the compensator using a digital controller such as the Microchip dsPIC33 "GS" family of devices.
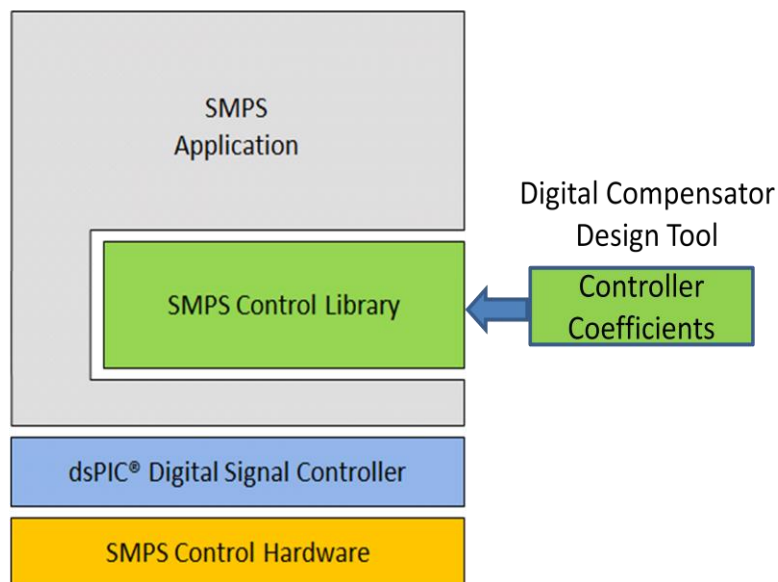

Figure 28 - Hardware & GUI Generated Coefficient Implementation

K$_{DC}$ Gain

The Compensator design windows and in Equation 3, 4 and 5 the variable K$_{DC}$ is shown, this variable represents a DC gain for the compensator. This variable is intended to introduce a DC gain offset to the compensator, without having to adjust the frequency location of the Pole/Zero placement of the compensator. The default value is set equal to one (1).

K$_{uC}$ Gain Calculation

In order to account for gains associated with the feedback sensing network, PWM and ADC modules, the DCDT will take into account the corresponding information provided to compute the K$_{uC}$ gain. This gain must be included at the time of generating the digital compensator coefficients of the header file (Output Report > Generate code Option). This gain will be automatically in introduced by enabling the "implement Kuc gain" check-box option, alternatively the user might manually enter this gain value using the K$_{DC}$ field.

Bode Plots

The DCDT allows the user to select the Bode plots that are to be displayed (e.g., Plant, Compensator, etc) as shown in Figure 29 below.
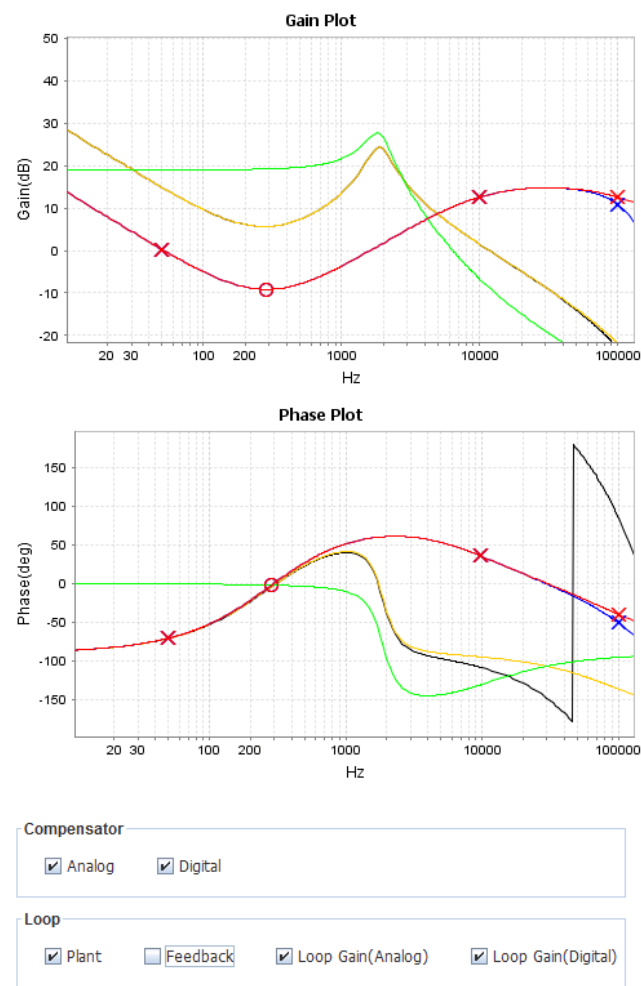

Figure 29 - Bode Plot Example

To Zoom-in in a specific area of the plot, use the Left-Mouse-Button, click into the bode plot and drag the mouse creating a rectangle in the zoom area of interest.

To restore the Bode Plot view, using the Left-Mouse-Button, click into the bode plot and drag from the right-to-left.

Nyquist Plot

The DCDT will compute the Nyquist Plot for the closed-loop system using the Digital Compensator selected. This plot can be used to evaluate the overall stability of the system by determining the number of encirclements of the point at (-1,0). Please review the Nyquist stability criterion for more details.
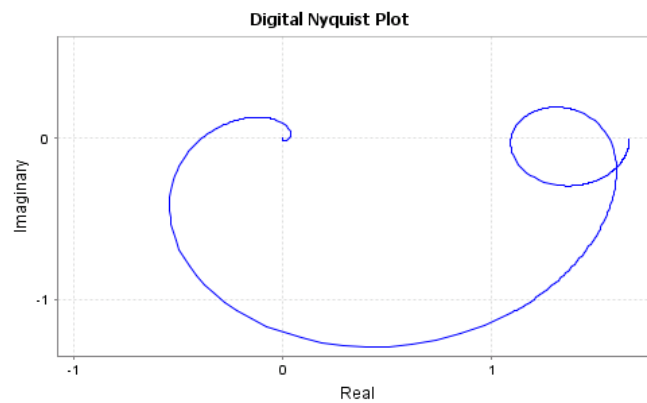

Figure 30 - Nyquist Plot

Root Locus Plot

The DCDT will compute the root locus plot of the closed loop system taking into account the digital compensator selected. This plot can be used to determine how the roots of the system or the close loop poles will change with variations to a free system variable (α). We can further clarify this by defining the compensator gain as K(s)=αK'(s) where the α is the term the DCDT will vary and use to perform the calculations for the plots.
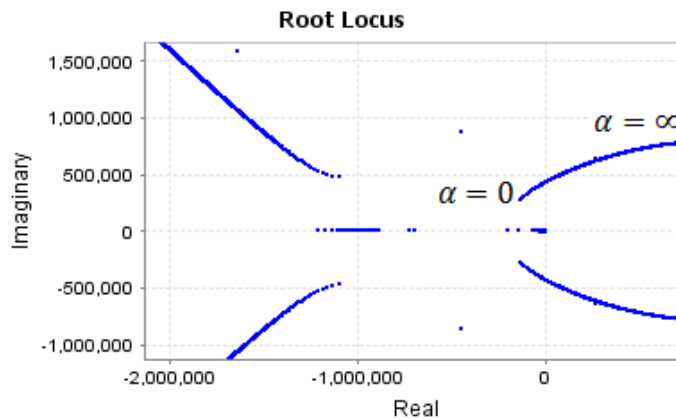

Figure 31 - Root Locus Plot

Generate Summary Report

Once all the required information is entered into the DCDT it will enable the user to generate a project summary report and a file that includes the calculated coefficients. The user can choose between the two options.
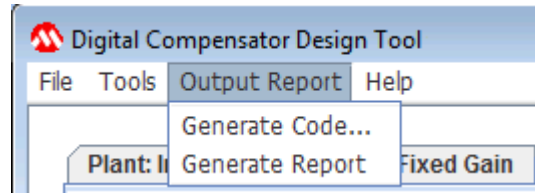

Figure 32 - Output Report File Menu

Generate Report: This menu option will create an HTML document that includes a summary of the active project and is intended for documentation purposes. The file will be saved in the same folder as defined in the Project Location (see Figure 6 - New Project Name and Project Folder Location

Note: The DCDT will only capture input information from the most recent window selections and this will be summarized in Figure 7 - Single-Loop Block Diagram.

Generate Code: This menu option will generate the Header source file that includes the #define declarations for the compensator coefficients that reflect the performance designed by the GUI. The code can be directly placed into the MPLAB® X IDE active project and that is programmed into the hardware.


```
// Compensator Coefficient Defines
#define BUCK_COMP_3P3Z_COEFF_A1        0x7FDF
#define BUCK_COMP_3P3Z_COEFF_A2        0xD986
#define BUCK_COMP_3P3Z_COEFF_A3        0xF059
#define BUCK_COMP_3P3Z_COEFF_B0        0x2033        Digital
#define BUCK_COMP_3P3Z_COEFF_B1        0xE1CA        Compensator
#define BUCK_COMP_3P3Z_COEFF_B2        0xDFD4        Coefficients
#define BUCK_COMP_3P3Z_COEFF_B3        0x1E3D
#define BUCK_COMP_3P3Z_POSTSCALER      0x6F17
#define BUCK_COMP_3P3Z_POSTSHIFT       0xFFFF
#define BUCK_FB_RC_Network_PRESHIFT    0x0005

// Compensator Clamp Limits
#define BUCK_COMP_3P3Z_MIN_CLAMP       0x0000        Compensator
#define BUCK_COMP_3P3Z_MAX_CLAMP       0x7FFF        Clamp Limits
```

Figure 33 - Digital Compensator Generated Coefficients

The generated source file will also include a summary of the user data and GUI settings and these are not shown on Figure 33 - Digital Compensator Generated Coefficients above.

DCDT Default Values

The DCDT GUI defines specific default values for many of the user entry-fields and these are to be used as a starting point or reference, based on a typical application, but the user is encouraged to measure and determine the actual values based on the hardware configuration settings.

The section below gives a quick overview of the default values and how these where selected.

- **PWM Switching Frequency**: 300 kHz is the default value used in all the different available compensators and this is a commonly used switching frequency in DC to DC converters.
- **PWM Sampling Ratio**: The DCDT default sampling ratio is one (1) configuring the sampling frequency equal to the switching frequency. Particular attention should be paid that the sampling frequency used allows the microcontroller enough time to executed control algorithm and any additional tasks the microcontroller is required to do (e.g., communication, fault monitoring, etc).
- **PWM Maximum Resolution**: The DCDT by default configures the PWM hardware for the maximum resolution for dsPIC33F devices of 1.06 ns. Depending on the hardware requirement the user should adjust this value.
- **Computational Delay**: The default compensator computational delays defined in the DCDT where determined form based on hardware measurements on a dsPIC33 device operating at 40 MHz CPU clock speed, these are to be used as examples and the user is encouraged to make time delay measurements in the specific hardware.

Table 2 - Compensator Default Delay

Compensator Type	Typical Compensator Delay (CPU at 50MHz)
PID	1.1 us
2P2Z (Type II)	1.35 us
3P3Z (Type III)	1.5 us

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Figure 34 - System Delays with 3P3Z Compensator shown below is an example of a voltage mode converter, where the sampling frequency is equals to the PWM switching frequency (Sampling Ratio = 1), this means that the ADC module will make a measurement of the output voltage once per PWM cycle. After the ADC has completed the conversion of the measurement, the ADC Interrupt Service Routine (ISR) will be called, inside of which the function call to the 3P3Z compensator will be executed and the new duty cycle will be written to the target PWM register.
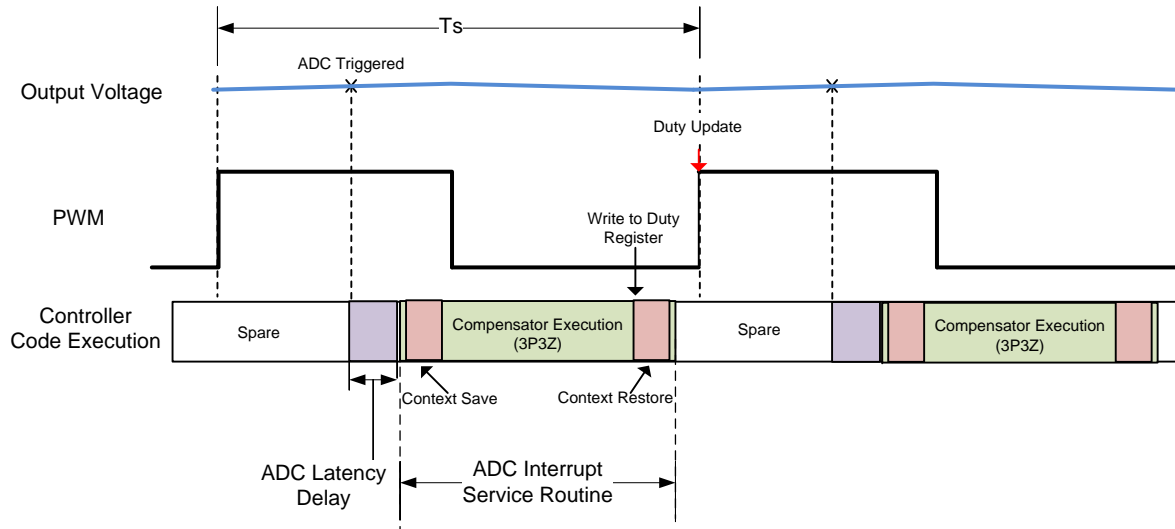

Figure 34 - System Delays with 3P3Z Compensator

- **Gate Drive Delay**: This is the delay associated with the gate-driver and the power switch (e.g., MOSFET) delays, these delays are often very small but should be taken into account when calculating overall system performance. For simplicity purposes this delay was not shown in Figure 34, and it is possible to measure this by using an oscilloscope at the output of the microcontroller PWM output to the time when the power switch (e.g., MOSFET drain terminal) is fully turned on.

    For example:

    Using Microchip MOSFET gate driver MCP14700, the datasheet specifies a Turn-On Propagation delay of 36 ns and the Turn-Off Propagation delay of 36 ns, rise and fall times of 10 ns for a total of 92 ns Gate Driver delays.

    Using Microchip High-Speed N-Channel Power MOSFET MCP87050, it defines the Turn-On Delay of 5 ns, Rise time of 18 ns, Turn-Off delay of 11 ns and Fall-time of 5 ns, for a total of 39 ns.

    Combining the gate driver and the MOSFET delays it equates to 131 ns.

Related Application Notes:

Switch Mode power Supply (SMPS) Topologies (Part I)
http://ww1.microchip.com/downloads/en/AppNotes/01114A.pdf

Switch Mode Power Supply (SMPS) Topologies (Part II)
http://ww1.microchip.com/downloads/en/AppNotes/01207B.pdf

Digital Compensator Design and Modeling Application Notes:

Family Datasheets and Reference Manual Documents

For device datasheets, family reference manuals and code examples please visit www.microchip.com/power,
and select Product Family "Full Digital Control / dsPIC33F SMPS & Digital Power Conversion Devices"