Cairo University
Faculty of Engineering
Computer Department

Project Specification

Logic Design
CMP 101
Spring 2017

1. Objectives

After this project, the student should be able to:

1. Design and implement a sequential logic circuit based on specifications.
2. Learn to use a simulation tool to test the design before implantation.

2. Project Description

The aim of the project is to build an IC tester to find the type of an IC of the following categories:

1. AND 7408
2. OR 7432
3. XOR 7486
4. NAND 7400

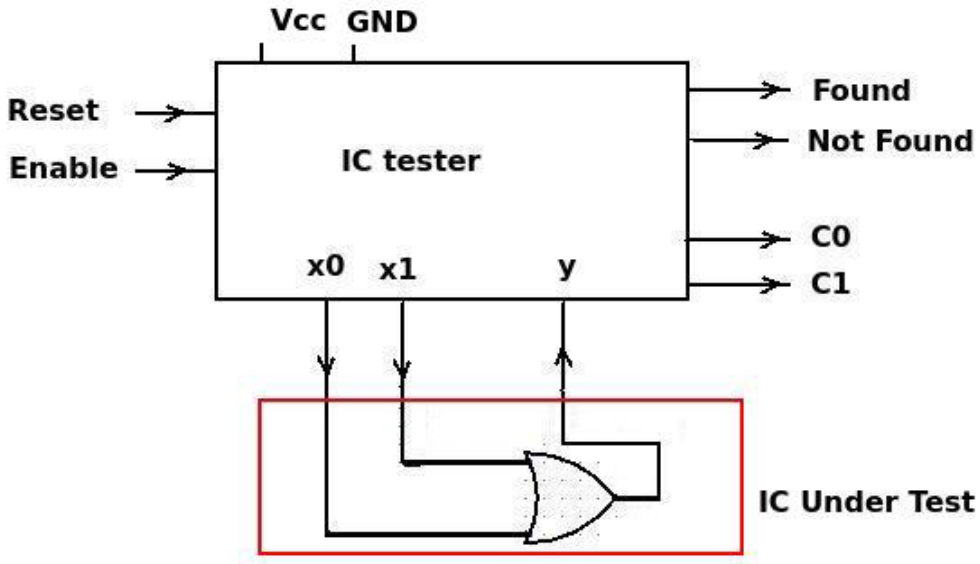

Figure 1. IC tester Block Diagram

The block diagram of the circuit is shown in Figure 1. The following are the specification of each input/output:

1. Input:
   a. Reset: An input for the circuit to reset its internal state.
   b. Enable: An input for the circuit to enable or disable it. So if enable the circuit start searching for the connected IC (IC Under Test).
   c. y0: is 4bit input that comes from the output of the IC under test.
2. Output:
   a. x1,x0: each are 4bit output that goes as input to the IC under test.
   b. Found: a signal that becomes high if the IC tester detect the type of the connected IC.
   c. Not Found: a signal that becomes high if the IC tester can not detect the type of the connected IC. i.e. not one of the 4 mentioned types.
   d. c1,c0: will contain the ID of the detected IC if Found is high and will contain don't care if Not Found is high. The IDs are {00,01,10,11} for the {AND, OR, XOR, NAND} respectively.

3. Circuit Architecture

The design of the IC tester based on the previous criteria is up to you. However, we propose the following design for better understanding to the problem and its solution.

System design procedure is a top down approach which means you have to think in the circuit as concrete blocks then you have to find the optimal design for each block independently. The proposed method is to save all the possible outputs of the known ICs in a table these known ICs are{AND, OR, XOR, NAND}. The size of this table should be 16 as the truth table of each IC is 4 rows. Then we have to iterate over all these possible outputs (i.e. using counter) and we can compare the saved output in the search table with the output of the IC under test if both values are then same we have to increment another counter that keep track the equality between the two values.

If the equality counter reaches 4 i.e. four possible saved outputs are the same as the four outputs of the IC under test then the Found signal should be high and c0,c1 signals should contains the ID of the found IC. Else if the IC under test is not in the search table then the Not Found signal

should be high. In both cases the search procedure should be paused. Note. we have to reset the equality counter each four iterations in order to begin the test for the next saved IC with the IC under test.

The proposed design contains five basic entities which are:

1. Search Table Circuit: The purpose of this circuit is to save all the possible outputs of the known ICs to our IC tester these known ICs are {AND, OR, XOR, NAND}.
2. Counter 1 Circuit: It's a four-bit counter that generate the iteration index for the search table in order to generate the save output.
3. Counter 1 Control Circuit: This circuit controls the counting of Counter 1 you should find the optimal design for this circuit to handle the following cases:
    a. When the IC under test not found then Counter 1 should be paused and Not Found signal should be high.
    b. When the IC under test is found then Counter 1 should be paused and Found signal should be high.
    c. When Enable is low Counter 1 should be paused.
    d. When Reset is high Counter 1 should reset.
4. Counter 2 Circuit: It's a four-bit counter that keeps track the equality between the output from the IC under test and the output from the search table.
5. Counter 2 Control Circuit: This circuit controls the counting of Counter 2 you should find the optimal design for this circuit to handle the following cases:
    a. When the output from the four gates in the IC under test is equal to the output from the search table then this counter should be enable to count else it should be paused.
    b. Each four iterations of Counter 1, Counter 2 should be reset.
    c. When Reset is high Counter 2 should reset.
    d. When the IC under test not found this counter should be paused.
    e. When the IC under test is found this counter should be paused.

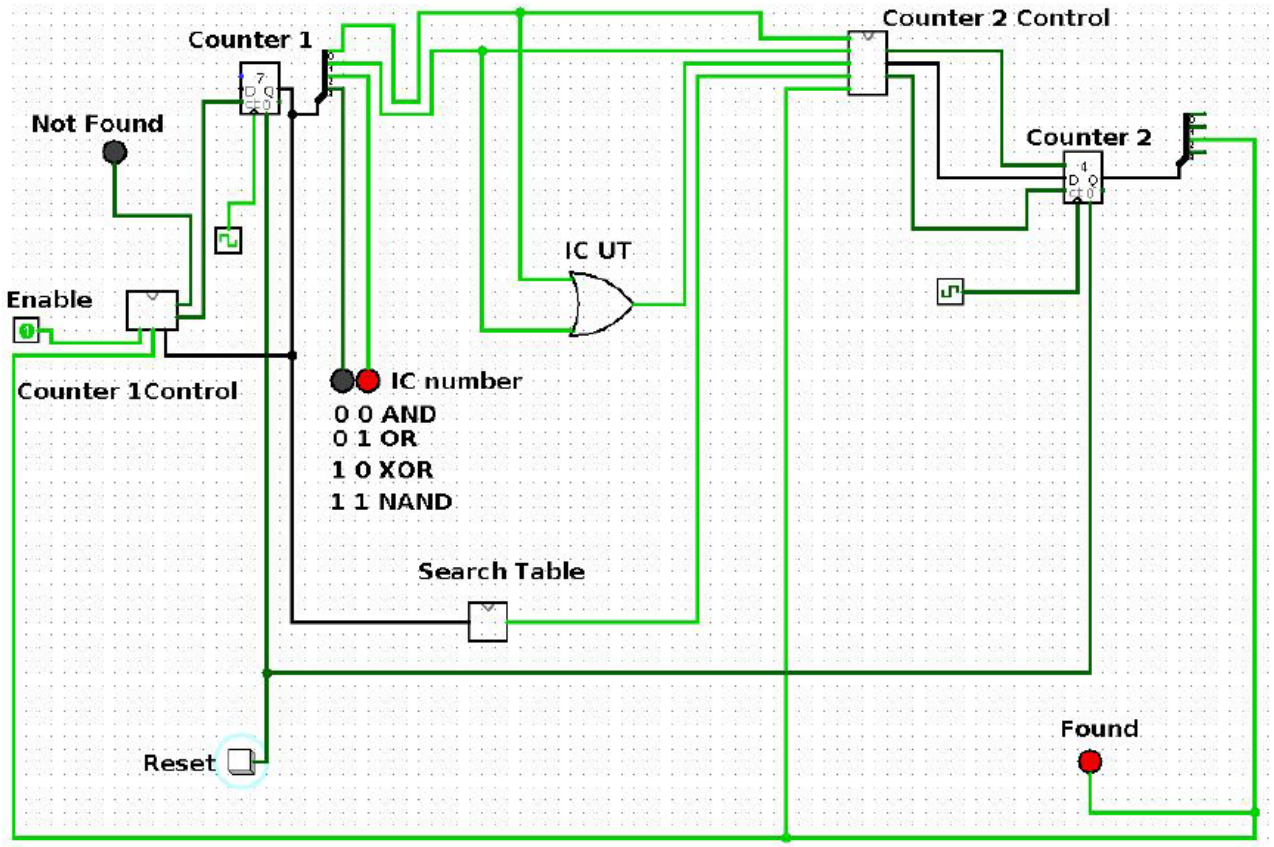

Figure 2: IC Tester Internal blocks

Figure 2 shows the internal blocks for the IC tester and the connections between them. You have to submit a design similar to the proposed one. And if you choose to submit a different design you should divided your design to basic blocks as we done earlier.

Important notes:

1. In this design Counter 1 and Counter 2 should operate on two different edges of the CLK.
2. You should test the four gates in the IC under test.

4. Project Delivery

- Groups should have 3-4 students.
- Delivery date: TBA
- You will be required to deliver a Design report (Hard Copy) that contains the following
- for each sub-circuit:
  - Detailed circuit diagram of the implementation.
  - A list of the used chips and components.
- Understanding of the project implementation by the group members (Individual grades)
- Do and present the circuit simulation on logisim tool.
- Do and present the hardware circuit on the bread board.
- Any changes in the project rules, criteria, or schedule will be announced before delivery by a sufficient time.
- Failure in any of the mentioned rules will lead to lose in your grades.

5. Grading Criteria

The distribution of the grade in this project will be as the following:

- Design report (20%): Detailed design report for your circuit and each block and the used components.
- Circuit Simulation (30%): Do and present the circuit simulation on logisim tool.
- Working Circuit on the bread board (50%): 10% for the control of Counter1, 10% for the control of Counter 2, 5% for the Search Table circuit. 25% for the integration.
- PCB circuit (Bonus 10%): Printed circuit board circuit is bonus.