Solutions to *The Art of Electronics 3rd Edition*

December 11, 2023

Contents

Solutions for Chapter 2

Exercise 2.1

In order to solve this problem, many assumptions must be made. Different people may assume slightly different values for parameters. This is OK. What is important is making good assumptions and checking our conclusions to make sure they are reasonable.

To solve for the current in the LED, let us assume we know the LED is red, so it follows the red LED curve from Figure 2.8 in the book. Let us also assume the transistor is acting like a closed switch, so the collector voltage of Q1 is close to 0 V. Let us also assume the LED is ON, so it's voltage is approximately $V_{\text{LED}} = 2\,\text{V}$. From the preceding assumptions, we can calculate that the LED current is

$$I_{\text{LED}} = \frac{3.3\,\text{V} - 2\,\text{V}}{330\,\Omega} = \frac{1.3\,\text{V}}{330\,\Omega} \approx 3.94\,\text{mA}$$

If we use Figure 2.8 (from the textbook) to check our numbers, we see that a current of 3.94 mA roughly correlates to an LED voltage of $V_{\text{LED}} = 1.7\,\text{V}$. We will run the same calculation again to reduce our error.

$$I^*_{\text{LED}} = \frac{3.3\,\text{V} - 1.7\,\text{V}}{330\,\Omega} = \frac{1.6\,\text{V}}{330\,\Omega} \approx \boxed{4.85\,\text{mA}}$$

In order to determine the minimum current gain required from our transistor, we must calculate the base current. Let us assume we know the base-emitter voltage $V_{\text{BE}} = 0.6\,\text{V}$. Therefore

$$I_{\text{B}} = \frac{3.3\,\text{V} - 0.6\,\text{V}}{10\,\text{k}\Omega} = 270\,\mu\text{A}$$

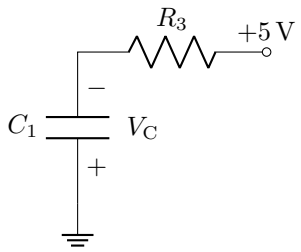
So the minimum current gain must be

$$\beta_{\text{min}} = \frac{I^*_{\text{LED}}}{I_{\text{B}}} \approx \frac{4.85\,\text{mA}}{270\,\mu\text{A}} \approx \boxed{18.0}$$

Exercise 2.2

When Q_1 goes is in saturation, the base voltage of Q_2 equals the opposite of the voltage on the capacitor C_1 at $t = 0\,\text{s}$, $V_0 = 4.4\,\text{V}$ and Q_2 is then cutoff. V_{out} will be equal to 5 V until Q_2 is brought in saturation again. This happens when its base voltage gets higher or equal to the Q_2 threshold voltage (0.6 V). As soon as Q_1 is brought in saturation, C_1 starts to discharge into the resistor R_3 and the equivalent circuit, valid until Q_2 is cutoff, is then:

Figure 1.1: Equivalent C_1 discharging circuit.



The time evolution of the voltage across the capacitor C_1 is given by:

$$V_\mathrm{C}(t) = (V_0 - V_\infty)\, e^{-\frac{t}{R_3 C_1}} + V_\infty$$

where V_∞ is the steady-state voltage on the capacitor C_1 end equals $-5\,\mathrm{V}$. Given the considerations above, we have that $V_C(t = T_\mathrm{pulse}) = -0.6\,\mathrm{V}$. Solving for t gives:

$$T_\mathrm{pulse} = -R_3 C_1 \ln\left(\frac{-0.6\,\mathrm{V} - V_\infty}{V_0 - V_\infty}\right) = \boxed{0.76 R_3 C_1 = 76\,\mu\mathrm{s}}$$

Exercise 2.3

The output voltage is now influenced by R_5 that goes in series with R_4, and by the V_BE of Q_3 which is equal to $0.6\,\mathrm{V}$ when the transistor is in saturation. Therefore:

$$V_\mathrm{out} = \frac{R_5}{R_5 + R_4}\,(5\,\mathrm{V} - 0.6\,\mathrm{V}) + 0.6\,\mathrm{V} = \boxed{4.79\,\mathrm{V}}$$

The minimum value of β of Q_3 can be obtained looking at the maximum value of the current flowing through the collector of Q_3, $I_\mathrm{c}^{\mathrm{Q_3}}$. As soon as Q_1 goes in saturation, the capacitor C_1 starts to discharge and its current is given by $C_1 dV_\mathrm{C}/dt$. With reference to the variables introduced in the previous exercise (2.2):

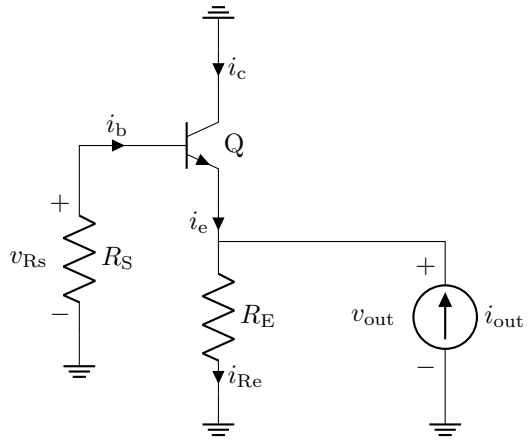
$$I_\mathrm{c}^{\mathrm{Q_3}}(t) = \frac{5\,\mathrm{V}}{R_2} - I_{\mathrm{C_1}}(t) = \frac{5\,\mathrm{V}}{R_2} + C_1 \frac{1}{R_3 C_1}\,(V_0 - V_\infty)\, e^{-\frac{t}{R_3 C_1}}$$

Therefore:

$$\beta_\mathrm{min} = \frac{I_\mathrm{c}^{\mathrm{Q_3}}(t)|_\mathrm{max}}{I_\mathrm{b}^{\mathrm{Q_3}}} = \frac{I_\mathrm{c}^{\mathrm{Q_3}}(t = 0\,\mathrm{s})}{I_\mathrm{b}^{\mathrm{Q_3}}} = \boxed{27}$$

Exercise 2.4

Figure 1.2: Emitter follower circuit used for computing the output resistance



Applying the KCL on the Q transistor:

$$i_e = i_b + i_c = i_b\,(\beta + 1)$$

The current flowing through the emitter resistor R_E is equal to:

$$i_{Re} = i_e + i_{out} = i_b\,(\beta + 1) + i_{out}$$

Since for the emitter follower $v_{Rs} = v_{out}$:

$$[i_b\,(\beta + 1) + i_{out}]\,R_E = v_{out}$$

Since:

$$i_b = -\frac{v_{Rs}}{R_S} = -\frac{v_{out}}{R_S}$$

we can write:

$$\left[-\frac{v_{out}}{R_S}\,(\beta + 1) + i_{out}\right] R_E = v_{out}$$

Therefore:

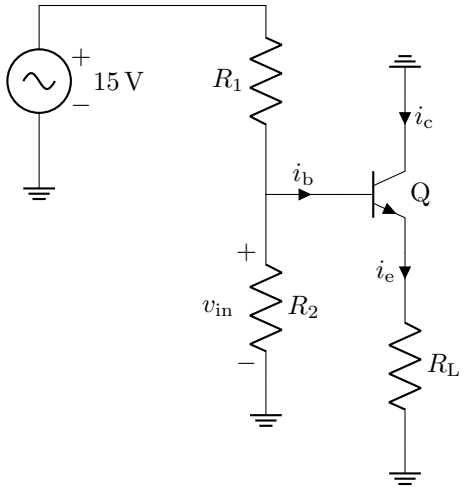
$$R_{out} = \frac{v_{out}}{i_{out}} = \frac{R_E R_S}{R_S + (\beta + 1)\,R_E}$$

If $R_E >> R_S/(\beta + 1)$:

$$\boxed{R_{out} \approx \frac{R_S}{(\beta + 1)}}$$

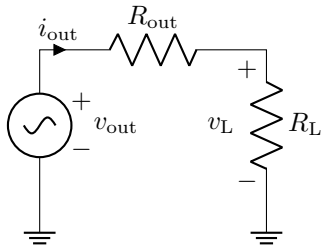
Exercise 2.5

Figure 1.3: Small signal circuit



In order to achieve a maximum voltage change of 5 % for a maximum current to the load (R_L) equal to 25 mA, we can make reference to the equivalent circuit of Figure 1.4:

Figure 1.4: Output equivalent circuit



obtaining:

$$\left.\frac{v_{out} - v_L}{v_{out}}\right|_{i_{out}=25\,mA} = 0.05$$

Since

$$v_{out} - R_{out}\, i_{out} = v_L$$

and for an emitter follower $v_{out} = v_{in} = 5\,V$ we can write:

$$\frac{R_{out}\, 25\,mA}{5\,V} = 0.05$$

obtaining the following condition on R_{out}:

$$R_{out} = \frac{0.05\, 5\,V}{25\,mA}$$

For the emitter follower configuration:

$$R_{\text{out}} = \frac{R_{\text{in}}}{\beta + 1}$$

and we see from the circuit of Figure 1.3 that R_{in} is given by the parallel between R_1 and R_2:

$$R_{\text{in}} = \frac{R_1 R_2}{R_1 + R_2}$$

In order to achieve $v_{\text{in}} = 5\,\text{V}$, the following condition must be verified for the values of R_1 and R_2:

$$\frac{R_2}{R_1 + R_2} = \frac{5\,\text{V}}{15\,\text{V}}$$

Assuming $\beta = 100$, we can finally obtain:

$$\boxed{R_1 = 30\,\Omega,\ R_2 = 15\,\Omega}$$

Exercise 2.6

The minimum current flowing through the R resistor has to be at least equal to the maximum current to the load plus the minimum current to the zener:

$$I_{\text{min,R}} = \frac{20\,\text{V} - 10\,\text{V}}{R} \geq 100\,\text{mA} + 10\,\text{mA}$$

Therefore:

$$R \leq \frac{10\,\text{V}}{110\,\text{mA}} = \boxed{91\,\Omega}$$

It follows that the maximum power to the zener, selecting $R = 91\,\Omega$, is equal to

$$P_{\text{max,z}} = \left(\frac{25\,\text{V} - 10\,\text{V}}{91\,\Omega} - 0\,\text{A}\right) 10\,\text{V} = \boxed{1.65\,\text{W}}$$

Exercise 2.7

With reference to figure 2.21 of the book, neglecting the current entering the ase of the transistor Q, in order to have at least 10 mA flowing through the zener, the resistor R should comply with the following condition:

$$\frac{20\,\text{V} - 10\,\text{V}}{R} \geq 10\,\text{mA}$$

which results in:

$$\boxed{R \leq 1\,\text{k}\Omega}$$

In order to avoid the transistor to be saturated, we want the collector-base voltage to be always higher than zero. This translates in:

$$R_{\text{C}} < R\frac{10\,\text{mA}}{100\,\text{mA}} = 100\,\Omega$$

Selecting a conservative value of R_{C} equal to $\boxed{20\,\Omega}$, we can compute the maximum power dissipated by the zener, $P_{\text{max,z}}$ and the transistor, $P_{\text{max,Q}}$ as:

$$P_{\text{max,z}} = \left(\frac{25\,\text{V} - 10\,\text{V}}{1\,\text{k}\Omega}\right) 10\,\text{V} = \boxed{0.15\,\text{W}}$$

$$P_{\mathrm{Q}} = (25\,\mathrm{V} - 20\,\Omega I_{\mathrm{load}})\, I_{\mathrm{load}}$$

The maximum power dissipated by the transistor is obtained for a collector current equal to 625 mA which is higher than the maximum load current. Therefore, in our case, the maximum power dissipated by Q will be obtained for $I_{\mathrm{load,max}} = 100\,\mathrm{mA}$:

$$P_{\mathrm{max,Q}} = (25\,\mathrm{V} - 20\,\Omega I_{\mathrm{load,max}})\, I_{\mathrm{load,max}} = \boxed{2.3\,\mathrm{W}}$$

Comparing the results with those of the previous exercise, we notice that the power disspated by the zener diode significantly decreased but we have an additional power dissipated by the transistor which is higher than the power that the zener diode dissipated in the circuit of the previous exercise. However this power can be decreased by increasing the value of R_{C}.

Exercise 2.8

In order to keep the emitter voltage V_{E} in the half range of the dc supply, considering the quiescent current of 5 mA we have:

$$V_{\mathrm{E}} = \frac{15\,\mathrm{V} - (-15\,\mathrm{V})}{2} = 15\,\mathrm{V}$$

and the emitter resistor R_{E}:

$$R_{\mathrm{E}} = \frac{15\,\mathrm{V}}{5\,\mathrm{mA}} = \boxed{3\,\mathrm{k\Omega}}$$

Since the imput impedance to the transistor, under the assumption of a load resistance much larger than the emitter resistance, is:

$$R_{\mathrm{in}} = \beta R_{\mathrm{E}} = 300\,\mathrm{k\Omega}$$

in order to have the 3 dB point below the lowest frequency of 20 Hz, the capacitor C_1 has to be:

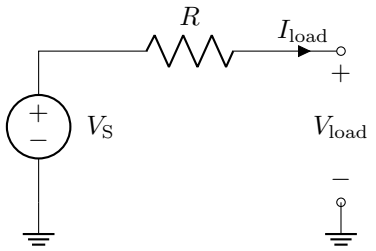
$$\frac{1}{R_{\mathrm{in}} C_1} \leq 20\,\mathrm{Hz}$$

meaning that:

$$\boxed{C_1 \geq 0.17\,\mu\mathrm{F}}$$

Exercise 2.9

Figure 1.5: Current source circuit



We want:

$$\frac{I_{\mathrm{load}}^{\mathrm{max}} - I_{\mathrm{load}}^{\mathrm{min}}}{I_{\mathrm{load}}^{\mathrm{max}}} = \frac{V_{\mathrm{S}} - 0\,\mathrm{V} - (V_{\mathrm{S}} - 10\,\mathrm{V})}{V_{\mathrm{S}} - 0\,\mathrm{V}} = 0.01$$

from which it follows:

$$\boxed{V_{\mathrm{S}} = 1\,\mathrm{kV}}$$

Exercise 2.10

With reference to Figure 1.5, we assume that I_{load} is equal to 10 mA if V_{load} is equal to 0 V, which means R_{load} is equal to 0 Ω. We can therfore calculate R as:

$$R = \frac{V_{\text{S}}}{10\,\text{mA}} = 100\,\text{k}\Omega$$

In this case we have:

$$\boxed{P_{\text{load}} = 0\,\text{W},\ P_{\text{R}} = I_{\text{load}}^2 R = 10\,\text{W}}$$

If $V_{\text{load}} = 10\,\text{V}$, from the condition of the previous exercise, we have:

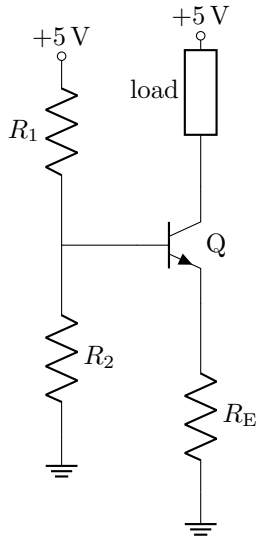
$$I_{\text{load}} = (1 - 0.01)10\,\text{mA} = 9.9\,\text{mA}$$

Therefore:

$$\boxed{P_{\text{load}} = 10\,\text{V} I_{\text{load}} = 0.1\,\text{W},\ P_{\text{R}} = I_{\text{load}}^2 R = 9.8\,\text{W}}$$

Exercise 2.11

Figure 1.6: Current sink



In order to have an emitter current equal to 5 mA, the following condition has to be verified:

$$\frac{R_2}{R_1 + R_2} 5\,\text{V} - 0.6\,\text{V} = R_{\text{E}} 5\,\text{mA}$$

Furthermore, the transistor shouldn't sensibly load the voltage divider, therefore:

$$\frac{R_1 R_2}{R_1 + R_2} << R_{\text{E}}\beta$$

Since we have a dc voltage of 5 V, we want the voltage on R_2 to be lower or equal to this value:

$$R_{\text{E}} 5\,\text{mA} + 0.6\,\text{V} \leq 5\,\text{V}$$

leading to:

$$R_\mathrm{E} \leq 880\,\Omega$$

A good guess value for R_E could be:

$$\boxed{R_\mathrm{E} = 200\,\Omega}$$

The base voltage will be given by:

$$V_\mathrm{B} = R_\mathrm{E} 5\,\mathrm{mA} + 0.6\,\mathrm{V} = 1.6\,\mathrm{V}$$

Selecting $\boxed{R_1 = 1\,\mathrm{k}\Omega}$ it is possible to compute R_2:

$$\boxed{R_2 = 470\,\Omega}$$

The impedance seen by the input of the transistor is equal to $320\,\Omega$ and the input impedance of the transistor, considering $\beta = 100$, is $R_\mathrm{E}\beta = 20\,\mathrm{k}\Omega$ with the former much lower than the latter. Finally, considering a maximum V_CE voltage of the transistor equal to $0.2\,\mathrm{V}$ before it saturates, we obtain the compliance voltage on the load as:

$$\boxed{V_\mathrm{comp} = 5\,\mathrm{V} - (0.2\,\mathrm{V} + R_\mathrm{E} 5\,\mathrm{mA}) = 3.8\,\mathrm{V}}$$

Exercise 2.12

The distortion is given by:

$$\frac{\Delta V_\mathrm{out}}{V_\mathrm{drop}} \frac{V_\mathrm{T}}{V_\mathrm{T} + I_\mathrm{E} R_\mathrm{E}}$$

therefore, if $R_\mathrm{E} = 0\,\Omega$ we obtain a predicted distortion equal to $\boxed{\frac{\Delta G}{G} = \frac{0.2\,\mathrm{V}}{5\,\mathrm{V}} = 0.04}$ in case of $0.1\,\mathrm{V}$ output amplitude and $\boxed{\frac{\Delta G}{G} = \frac{2\,\mathrm{V}}{5\,\mathrm{V}} = 0.4}$ in case of $1\,\mathrm{V}$ output amplitude. If $R_\mathrm{E} I_\mathrm{E} = 0.25\,\mathrm{V}$, $\frac{\Delta G}{G}$ equals to $\boxed{0.004}$ and $\boxed{0.04}$ for output voltage amplitudes equal to $0.1\,\mathrm{V}$ and $1\,\mathrm{V}$, respectively.

Exercise 2.13

If the transistor is biased at half V_cc, we have that the collector-emitter voltage will be equal to $V_\mathrm{CE} = V_\mathrm{cc} - I_\mathrm{C} R_\mathrm{C} = V_\mathrm{cc} - V_\mathrm{cc}/2 = V_\mathrm{cc}/2$ where I_C is the collector quiescent current and R_C is the collector resistor. The collector-base voltage will be therefore $V_\mathrm{CB} = V_\mathrm{cc}/2 - V_\mathrm{BE}$. In this case V_BE is supposed to be obtained by means of a voltage divider. If the temperature changes, approximately V_BE does not change and the collecotr current will increase by $9\,\%\,^\circ\mathrm{C}^{-1}$. This means that the collector current doubles for a temperature increase equal to $8\,^\circ\mathrm{C}$. In this case $R_\mathrm{C} I_\mathrm{C}$ becomes equal to $2V_\mathrm{cc}/2 = V_\mathrm{cc}$. As a consequence $\boxed{V_\mathrm{CB} = -V_\mathrm{BE} < 0 \text{ and the transistor goes in saturation.}}$

Exercise 2.14

The bias is arranged in order to have a collector current equal to $1\,\mathrm{mA}$. Indeed:

$$I_\mathrm{c} = \frac{0.775\,\mathrm{V} - 0.6\,\mathrm{V}}{175\,\Omega} = 1\,\mathrm{mA}$$

The base-emitter voltage decreases by $2.1\,\mathrm{mV}\,^\circ\mathrm{C}^{-1}$. Therefore, if the temperature increases by $20\,^\circ\mathrm{C}$, the collecotr current will become:

$$I_\mathrm{c} = \frac{0.775\,\mathrm{V} - 0.6\,\mathrm{V} - 0.0021\,\mathrm{V}\,^\circ\mathrm{C}^{-1}\,20\,^\circ\mathrm{C}}{175\,\Omega} = 0.76\,\mathrm{mA}$$

$\boxed{\text{It can be seen that the new collecotr current is about } 25\,\% \text{ lower than } 1\,\mathrm{mA}}$

Exercise 2.15

The voltage gain is given by:

$$G = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_{\text{C}}}{r_{\text{e}}} = \frac{I_{\text{C}} R_{\text{C}}}{V_{\text{T}}}$$

In order to achieve a voltage drop on R_{C} equal to half the V_{cc} voltage:

$$I_{\text{C}} R_{\text{C}} = \frac{1}{2} V_{\text{cc}}$$

and therefore:

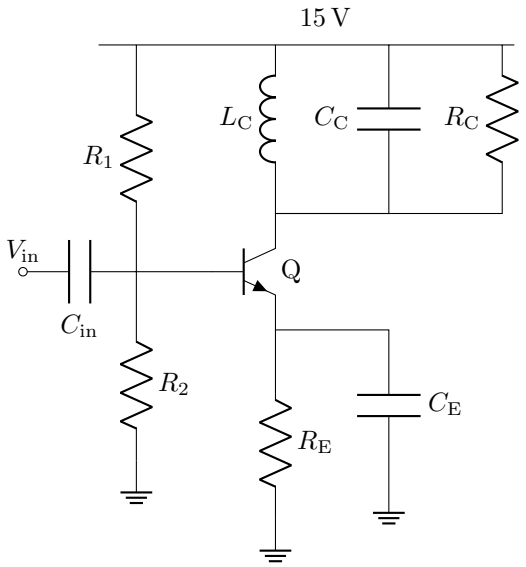
$$R_{\text{C}} = \frac{1}{2} \frac{V_{\text{cc}}}{I_{\text{C}}}$$

Substituting the R_{C} expression into the voltage gain:

$$\boxed{G = \frac{1}{2} \frac{V_{\text{cc}}}{V_{\text{T}}} = \frac{V_{\text{cc}}}{50\,\text{mV}} = 20 V_{\text{cc}}}$$

Exercise 2.16

Figure 1.7: Tuned common emitter amplifier



With reference to Figure 1.7, we start by choosing the emitter resistor R_{E}. We want its value to be large enough to have a voltage drop higher than V_{BE} in order to have a good stability of the quiescent current with the temperature. However we want the transistor to operate in the active region. Since at DC, the inductor behaves like a short circuit, we have that the collector voltage is equal to V_{cc}, therefore:

$$R_{\text{E}} I_{\text{E}}^{\text{Q}} < V_{\text{cc}} - 0.2\,\text{V}$$

and

$$R_{\text{E}} < \frac{V_{\text{cc}} - 0.2\,\text{V}}{I_{\text{E}}^{\text{Q}}} = 14.8\,\text{k}\Omega$$

where $I_{\mathrm{E}}^{\mathrm{Q}}$ is equal to about 1 mA. We choose:

$$\boxed{R_{\mathrm{E}} = 1\,\mathrm{k\Omega}}$$

In order to achieve a quiescent current equal to 1 mA, the base voltage has to be equal to:

$$V_{\mathrm{B}} = 0.6\,\mathrm{V} + R_{\mathrm{E}} I_{\mathrm{E}}^{\mathrm{Q}} = 1.6\,\mathrm{V}$$

Therefore, the ratio between R_1 and R_2 has to be equal to 8.4. Choosing the parallel resistance of R_1 and R_2 to be about one tenth of the transistor input resistance $\beta R_{\mathrm{E}} \approx 100\,\mathrm{k\Omega}$ we choose the following values for R_1 and R_2:

$$\boxed{R_1 = 84\,\mathrm{k\Omega}, \quad R_2 = 10\,\mathrm{k\Omega}}$$

The value of the capacitor C_{C} can be obtained forcing the parallel LC circuit to resonate at 100 kHz:

$$\frac{1}{2\pi}\sqrt{\frac{1}{L_{\mathrm{C}} C_{\mathrm{C}}}} = 100\,\mathrm{kHz}$$

Therefore:

$$\boxed{C_{\mathrm{C}} = 2.5\,\mathrm{nF}}$$

The value of the capacitor C_{E} can be selected imposing that the absolute value of the impedance of the parallel between R_{E} and C_{E} is lower than $r_{\mathrm{e}} = 25\,\Omega$ for a quiescent current of 1 mA. Doing the math we obtain:

$$C_{\mathrm{E}} > \frac{\sqrt{\frac{R_{\mathrm{E}}}{25\,\Omega}^2 - 1}}{\omega R_{\mathrm{E}}} = 63.6\,\mathrm{nF}$$

A value of C_{E} equal to 10 µF is conservative enough to maximise the AC gain:

$$\boxed{C_{\mathrm{E}} = 10\,\mu\mathrm{F}}$$

It remains to calculate the value of the input decoupling capacitor C_{in}. Its value can be obtained by forcing the cut-off frequency $1/R_{\mathrm{in}}$ to be below 100 kHz where

$$R_{\mathrm{eq}} = \beta r_{\mathrm{e}} || R_1 || R_2$$

where we neglected the emitter impedance which is verly low thanks to the C_{E} effect. We have therefore:

$$C_{\mathrm{in}} \geq 5\,\mathrm{nF}$$

Even in this case a conservative value for C_{in} can be:

$$\boxed{C_{\mathrm{in}} = 10\,\mu\mathrm{F}}$$

Exercise 2.17

In the following, the pedix B, C and E refer to base, collector and emitter. The apix Q1, Q2 and Q3 refer to the relevant transistors. Supposing all the transistors share the same β, the I_{P} current can be expressed as:

$$I_{\mathrm{P}} = I_{\mathrm{C}}^{\mathrm{Q1}} + I_{\mathrm{B}}^{\mathrm{Q3}} = \beta I_{\mathrm{B}}^{\mathrm{Q1}} + \frac{I_{\mathrm{C}}^{\mathrm{Q3}}}{\beta}$$

Since the base-emitter voltage of the transistor Q1 is the same of the transistor Q2, the base currents are the same. Therefore:

$$I_{\mathrm{B}}^{\mathrm{Q1}} + I_{\mathrm{B}}^{\mathrm{Q2}} = 2 I_{\mathrm{B}}^{\mathrm{Q1}} = I_{\mathrm{E}}^{\mathrm{Q3}} - I_{\mathrm{C}}^{\mathrm{Q1}} = \frac{\beta + 1}{\beta} I_{\mathrm{C}}^{\mathrm{Q3}} - \beta I_{\mathrm{B}}^{\mathrm{Q1}}$$

and then:

$$I_{\mathrm{B}}^{\mathrm{Q1}} = \frac{\beta + 1}{\beta(\beta + 2)} I_{\mathrm{C}}^{\mathrm{Q3}}$$

Substituting this expression into the first equation, it is possible to obtain the following expression for I_{P}:

$$I_{\mathrm{P}} = \left(1 + \frac{2}{\beta(\beta + 2)}\right) I_{\mathrm{C}}^{\mathrm{Q3}} \approx I_{\mathrm{C}}^{\mathrm{Q3}}$$

By comparing the above expression with that that typical of a basic current mirror:

$$I_{\mathrm{P}} = \left(1 + \frac{2}{\beta}\right) I_{\mathrm{C}}$$

one can see that the load current $I_{\mathrm{C}}^{\mathrm{Q3}}$ is much colser to the reference current I_{P} than for the basic current mirror. Indeed:

$$\frac{2}{\beta(\beta + 2)} << \frac{2}{\beta}$$

Exercise 2.18

For a grounded differential amplifier, the differential gain is:

$$G_{\mathrm{diff}} = \frac{R_{\mathrm{C}}}{2r_{\mathrm{e}}} = \frac{R_{\mathrm{C}} I_{\mathrm{C}}}{2V_{\mathrm{T}}} = V_{\mathrm{C}} 2V_t extT = \boxed{20V_{\mathrm{C}}}$$

where V_{C} is the voltage drop across the collector resistor R_{C}. Therefore, if $V_{\mathrm{C}} = 0.5V_{\mathrm{cc}}$:

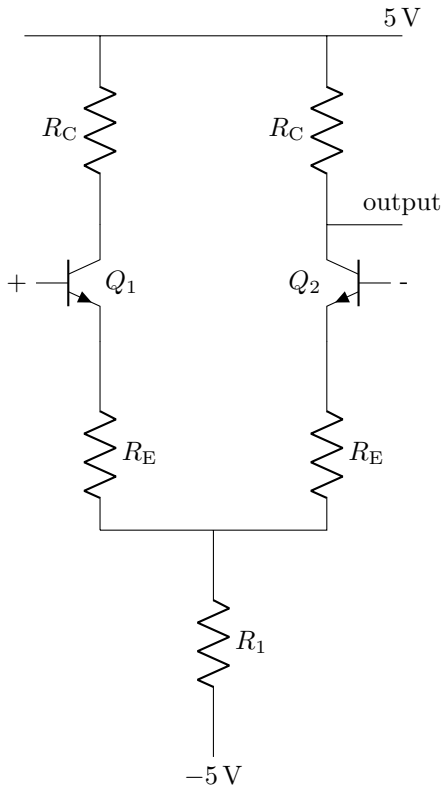
$$\boxed{G_{\mathrm{diff}} = 10V_{\mathrm{cc}}}$$

Following a similar argument:

$$\mathrm{CMRR} = \frac{R_1}{r_{\mathrm{e}}} = \frac{R_1 I_{\mathrm{C}}}{V_{\mathrm{T}}} = \frac{1}{2} V_1 V_{\mathrm{T}} = \boxed{20V_1}$$

where V_1 is the voltage drop across the R_1 resistor.

Figure 1.8: Tuned common emitter amplifier



For the differential, single-ended amplifier in Figure 1.8, the output impedance is equal to R_C. Therefore we have $\boxed{R_C = 10\,\mathrm{k\Omega}}$. Since we want the voltage drop on the collector resistor to be half of the V_{cc}:

$$\boxed{I_C = 2.5\,\mathrm{V}\,10\,\mathrm{k\Omega} = 250\,\mu\mathrm{A}}$$

Neglecting the voltage drop on the emitter resistor R_E, we can approximate the collector current as:

$$I_C \approx \frac{5\,\mathrm{V} - 0.6\,\mathrm{V}}{2R_1}$$

and therefore:

$$\boxed{R_1 = 2.8\,\mathrm{k\Omega}}$$

The value of R_E can then be obtained from the differential gain, considering that it is given by:

$$G_{\mathrm{diff}} = 25 = \frac{R_C}{2\,(r_e + R_E)}$$

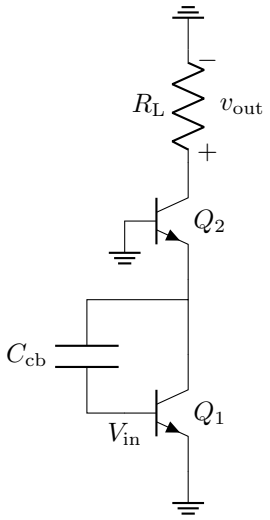
. Therefore, considering that $r_e = V_T/I_C = 100\,\Omega$:

$$\boxed{R_E = 100\,\Omega}$$

Exercise 2.19

As regards the differential amplifier in Figure 2.84 of the book, the AC voltage across the C_{CB} capacitor is equal to the voltage at the base of the transistor Q_1 without depending on the voltage gain. The voltage across the emitter resistor R_{E} is the input to a common base amplifier which does not have Miller effect.

Figure 1.9: Cascode amplifier



As regards the cascode configuration, one can make reference to Figure 1.9. Under the approximation that the collecotr current of the transistor Q_1 is equal to that of the transistor Q_2:

$$i_{\mathrm{C}}^{\mathrm{Q_1}} = i_{\mathrm{C}}^{\mathrm{Q_2}} = \frac{v_{\mathrm{in}}}{r_{\mathrm{e}}^{\mathrm{Q_1}}}$$

where $r_{\mathrm{e}}^{\mathrm{Q_1}}$ is the differential resistance of the Q_1 transistor. The output voltage will be:

$$v_{\mathrm{out}} = R_{\mathrm{L}} i_{\mathrm{C}}^{\mathrm{Q_2}}$$

The base-emitter AC voltage of the Q_2 transistor will be:

$$v_{\mathrm{BE}}^{\mathrm{Q_2}} = r_{\mathrm{e}}^{\mathrm{Q_2}} i_{\mathrm{C}}^{\mathrm{Q_2}}$$

where $r_{\mathrm{e}}^{\mathrm{Q_2}}$ is the differential resistance of the Q_2 transistor.
The voltage across the C_{CB} capacitor will be:

$$v_{\mathrm{CB}} = v_{\mathrm{in}} + v_{\mathrm{BE}}^{\mathrm{Q_2}} = v_{\mathrm{in}} + \frac{v_{\mathrm{in}} r_{\mathrm{e}}^{\mathrm{Q_2}}}{r_{\mathrm{e}}^{\mathrm{Q_1}}}$$

It follows that the amplitude of the current through the C_{CB} capacitor is:

$$I_{\mathrm{CB}} = \frac{v_{\mathrm{in}} \left(1 + \frac{r_{\mathrm{e}}^{\mathrm{Q_2}}}{r_{\mathrm{e}}^{\mathrm{Q_1}}}\right)}{X_{\mathrm{CB}}}$$

where X_{CB} is the capacitive reactance associated to the C_{CB} capacitor. The Miller capacitance $C_{\mathrm{CB}}^{\mathrm{M}}$ is therefore:

$$\boxed{C_{\mathrm{CB}}^{\mathrm{M}} = C_{\mathrm{CB}}\left(1 + \frac{r_{\mathrm{e}}^{\mathrm{Q}_2}}{r_{\mathrm{e}}^{\mathrm{Q}_1}}\right)}$$

and does not depend on the voltage gain of the cascode amplifier.

Exercise 2.20

The expression for the input impedance of the inverting amplifier is straightforward by considering that it is the series between the R_1 resistance with the input impedance of the transresistance amplifier. Therefore, the input impedance Z_{in} is:

$$\boxed{Z_{\mathrm{in}} = R_1 + R_{\mathrm{in}} || \frac{R_2}{1+A}}$$

The closed loop gain can also be obtained in a straightforward way starting by considering the input impedance of the operational amplifier, R_{in}, apporaching to infinity. In this case, all the current flowing in R_1 goes in R_2 making R_1 and R_2 in series. Therefore:

$$V_{\mathrm{out}} = vA$$

where v is the differential voltage of the operational amplifier and A is the open loop gain.
v is given by:

$$v = -[V_{\mathrm{in}} - (V_{\mathrm{in}} - V_{\mathrm{out}})B]$$

where B is defined as:

$$\frac{R_1}{R_1 + R_2}$$

The expression for the output voltage becomes:

$$V_{\mathrm{out}} = -A[V_{\mathrm{in}} - (V_{\mathrm{in}} - V_{\mathrm{out}})B]$$

and the closed loop gain is:

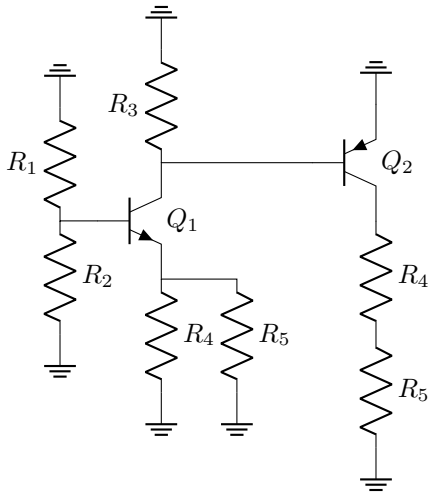
$$\boxed{G = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = -A\frac{1-B}{1+AB}}$$

Exercise 2.21

$$\boxed{G_{\mathrm{CL}} = \frac{-100j}{1 + -100j(0.1)} = 9.90 - 0.99j}$$

Exercise 2.22

Figure 1.10: Open loop small signal circuit



The feedback takes the voltage from the output of Q2 transistor and returns it to the input of the Q1 transistor through a voltage divider made of the resistors R_4 and R_5. The feedback is of *voltage-voltage* kind. In order to account ofr the feedback loading effect in opening the loop, the reference circuit is that of Figure 1.10. Considering a β of 100 for both Q1 and Q2, the open loop gain is:

$$G^{\mathrm{OL}} = \frac{-1}{r_{\mathrm{e}}^{\mathrm{Q_1}} + R_4||R_5} \left[R_3||r_{\mathrm{e}}^{\mathrm{Q_2}}\beta\right] \left[-\frac{R_4+R_5}{r_{\mathrm{e}}^{\mathrm{Q_2}}}\right] \approx \frac{1}{r_{\mathrm{e}}^{\mathrm{Q_1}} + R_4} \left[R_3||r_{\mathrm{e}}^{\mathrm{Q_2}}\beta\right] \left[\frac{R_5}{r_{\mathrm{e}}^{\mathrm{Q_2}}}\right]$$

Therfore, since $r_{\mathrm{e}}^{\mathrm{Q_1}} = r_{\mathrm{e}}^{\mathrm{Q_2}} = 25\,\Omega$:

$$\boxed{G^{\mathrm{OL}} \approx 200}$$

The feedback gain is:

$$B = \frac{R_4}{R_4+R_5} \approx \frac{R_4}{R_5} = 0.1$$

Therfore, the loop gain is:

$$\boxed{G^{\mathrm{OL}}B \approx 20}$$

The open loop output impedance is:

$$\boxed{Z_{\mathrm{out}}^{\mathrm{OL}} = R_4 + R_5 \approx R_5 = 10\,\mathrm{k}\Omega}$$

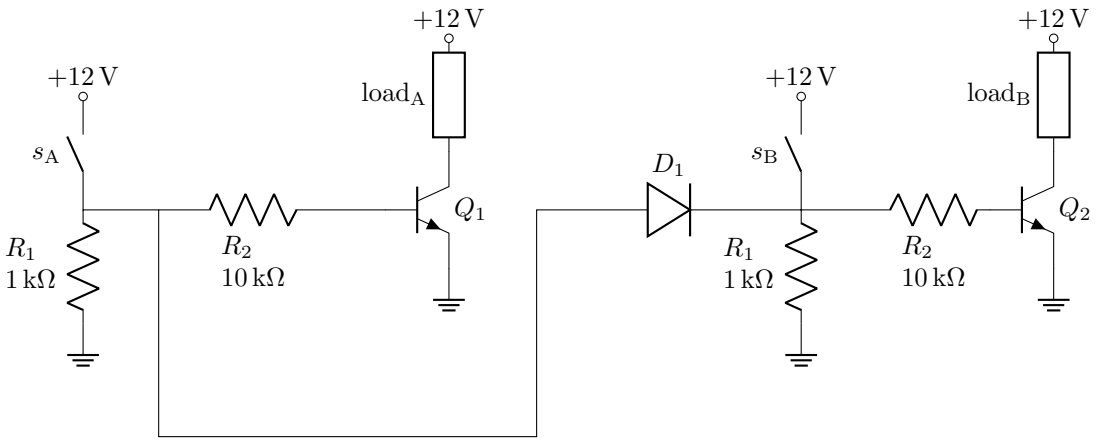
The closed loop parameters are therefore:

$$\boxed{G^{\mathrm{CL}} = \frac{G^{\mathrm{OL}}}{1+G^{\mathrm{OL}}B} \approx 9.5}$$

$$\boxed{Z_{\mathrm{out}}^{\mathrm{CL}} = \frac{Z_{\mathrm{out}}^{\mathrm{OL}}}{1+G^{\mathrm{OL}}B} \approx \frac{Z_{\mathrm{out}}^{\mathrm{OL}}}{G^{\mathrm{OL}}B} = 500}$$

Exercise 2.23

Figure 1.11: Solution



Let's suppose the loads are resistive with a resistance equal to 150 Ω and both the npn transistors have $\beta = 100$. When s_A and s_B are open, both $Q1$ and $Q2$ bases are to ground and no current flows into the loads.
If s_A is closed, the left terminals of the R_2 resistors are at 12 V (minus a diode voltage drop for the resistor connected at the Q_2 base). The base currents are therefore:

$$I_b = \frac{12\,\text{V} - 0.6\,\text{V}}{10\,\text{k}\Omega} = 1.14\,\text{mA}$$

Such a base current, with the considered β and load resistance, causes Q_1 and Q_2 to saturate. Therefore, the load current is:

$$I_l^A = I_l^B = \frac{12\,\text{V} - 0.2\,\text{V}}{150\,\Omega} = 79\,\text{mA}$$

When s_A is open and s_B is closed, D_1 is reverse biased and Q_1 is in cutoff region since no current flows into its base. However, 1.14 mA flows into the base of Q_2 which goes into saturation.

Exercise 2.24

(a) Under the assumption that β is very large, the load current I_{load} is given by:

$$I_{\text{load}} = I_C \approx I_E \left[\frac{V_{cc} R_2}{R_1 + R_2} - 0.6\,\text{V}\right] \frac{1}{R_E}$$

where $V_{CC} = 10\,\text{V}$, $R_1 = 8.2\,\text{k}\Omega$, $R_1 = 1.6\,\text{k}\Omega$ and $R_1 = 1.5\,\text{k}\Omega$. Therefore $\boxed{I_{\text{load}} = 0.7\,\text{mA}}$ Since for the transistor to work in active region it must hold:

$$V_{CE} = V_{CC} - V_{\text{load}} - V_E \geq 0.2\,\text{V}$$

since $V_E = I_E R_E \approx 1\,\text{V}$ the output compliance is given by:

$$\boxed{V_{\text{load}} \leq 8.8\,\text{V}}$$

(b) Removing the assumption that β is very large, has two effects. First, the emitter current and the collector currents are no more equal:

$$I_{\text{load}} = I_{\text{C}} = \beta \frac{1}{\beta + 1} I_{\text{E}}$$

Second, the R_1 and R_2 resistors are nomore in series since the bas current is no more negligible. The full expression for the emitter current can be obtained by considering that:

$$I_{\text{E}} = I_{\text{B}} + I_{\text{C}}$$
$$I_1 = I_{\text{B}} + I_2$$

where I_1 and I_2 are the currents flowing through R_1 and R_2,respectively, and I_{B} is the base current. Under this conditions, the emitter current is given by:

$$I_{\text{E}} = \frac{1}{R_{\text{E}}} \left[\frac{V_{\text{CC}} R_2}{R_1 + R_2} - 0.6\,\text{V} \right] \left[1 + \frac{R_2}{R_1(\beta + 1)} \left(1 - \frac{R_2}{R_1 + R_2} \right) \right]^{-1}$$

It follows:

$$\beta = 50 \quad I_{\text{E}} = 0.685\,\text{mA} \quad I_{\text{load}} = I_{\text{C}} = 0.67\,\text{mA}$$
$$\beta = 100 \quad I_{\text{E}} = 0.688\,\text{mA} \quad I_{\text{load}} = I_{\text{C}} = 0.68\,\text{mA}$$

(c) Here we consider again that β is very large. Being R_1 and R_2 in series, the base voltage does not change due to early effect and we can write:

$$\Delta I_{\text{E}} = -\frac{\Delta V_{\text{BE}}}{R_{\text{E}}} = \frac{0.0001 \Delta V_{\text{CE}}}{R_{\text{E}}}$$

Furthermore:

$$\Delta V_{\text{CE}} = -\Delta V_{\text{load}} - \Delta I_{\text{E}} R_{\text{E}}$$

Solving for ΔI_{E}:

$$\Delta I_{\text{load}} = \Delta I_C \approx \Delta I_{\text{E}} = \frac{-0.0001}{1.0001 R_{\text{E}}} \Delta V_{\text{load}}$$

For an output voltage within the output compliance ($\Delta V_{\text{load}} = 8.8\,\text{V}$):

$$\boxed{\Delta I_{\text{load}} = -66.7\,\text{nA}}$$

(d) V_{BE} varies by $-2.1\,\text{mV}\,^\circ\text{C}^{-1}$. With respect to the load current computed at the first point (a) ($I_{\text{load}} = 0.7\,\text{mA}$) it is easy to see that:

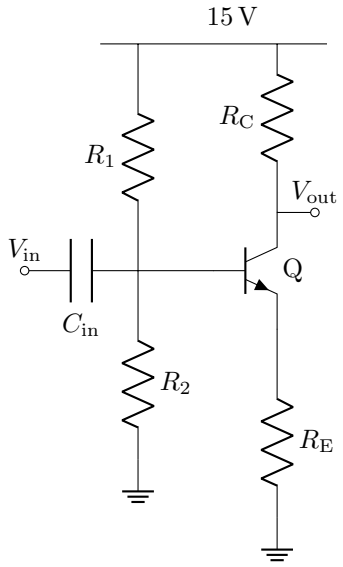
$$\boxed{\frac{\Delta I_{\text{load}}}{\Delta ^\circ\text{C}} = 0.2\,\%\,^\circ\text{C}^{-1}}$$

In order to account for the variation of β with temperature, we have to use the expression obtained in point b. In this case we obtain:

$$\boxed{\frac{\Delta I_{\text{load}}}{\Delta ^\circ\text{C}} = 0.21\,\%\,^\circ\text{C}^{-1}}$$

Exercise 2.25

Figure 1.12: Common emitter amplifier



The gain is approximately given by:

$$G = \frac{R_C}{R_E} = 15$$

Given a bias collector current of 0.5 mA, in order to have the bias collector voltage at $0.5V_{CC} = 7.5\,V$, the collector resistance has to be equal to:

$$\boxed{R_C = \frac{7.5\,V}{0.5\,mA} = 15\,k\Omega}$$

It follows that $\boxed{R_E = 1\,k\Omega}$ In order to have a bias collector current equal to 0.5 mA, the following condition must hold:

$$I_C \approx I_E = \frac{V_B - 0.6\,V}{R_E}$$

meaning that $V_B = 1.1\,V$ This defines the first out of three conditions on the value of the resistors R_1 and R_2:

$$V_{CC}\frac{R_2}{R_1 + R_2} = 1.1\,V \rightarrow R_1 = 12.64\,R_2$$

The second condition can be obtained by considering the maximum emitter voltage:

$$V_E^{MAX} = R_E I_E^{MAX} = 1\,k\Omega\,1\,mA = 1\,V$$

the minimum current flowig through R_1 is:

$$I_{R_1}^{MIN} = \frac{V_{CC} - 1.6\,V}{R_1} = \frac{13.4\,V}{R_1}$$

In order to properly drive the base of the transistor, this current has to be higher than the maximum base current:

$$\frac{13.4\,\mathrm{V}}{R_1} > \frac{1\,\mathrm{mA}}{\beta}$$

leading to the second condition:

$$R_1 < 1.34\,\mathrm{M\Omega}$$

Finally, the input impedance of the transistor should be much higher than the parallel impedance of R_1 and R_2:

$$\frac{R_1 R_2}{R_1 + R_2} << \beta R_\mathrm{E} = 100\,\mathrm{k\Omega}$$

Taking into account these conditions, we select the following values for R_1 and R_2:

$$\boxed{R_1 = 20.2\,\mathrm{k\Omega},\ R_2 = 1.6\,\mathrm{k\Omega}}$$

To be sure the 3 dB point is below the frequency of interest (100 Hz), the value of the input capacitor can be computed by:

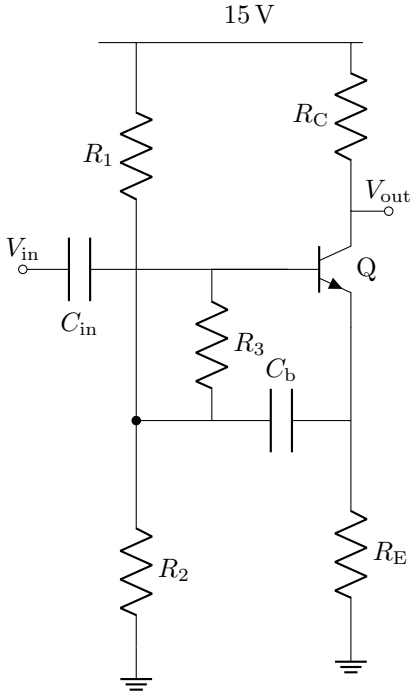
$$\frac{1}{1.5\,\mathrm{k\Omega}\, C_\mathrm{in}} < 2\pi 100\,\mathrm{Hz}$$

where 1.5 kΩ is the value of the parallel R_1 and R_2. From the previous expression one can obtain the value of the input capacitance C_in:

$$\boxed{C_\mathrm{in} > 1.06\,\mu\mathrm{F}}$$

Exercise 2.26

Figure 1.13: Bootstrapped common emitter amplifier



From a small signal perspective, the equivalent R_3 resistance is given by:

$$R_{\text{eq}} = \frac{R_3}{1 - A}$$

where A is the voltage gain of the emitter follower and it is given by:

$$\frac{R_{\text{E}} g_{\text{m}}}{1 + R_{\text{E}} g_{\text{m}}} = 0.95$$

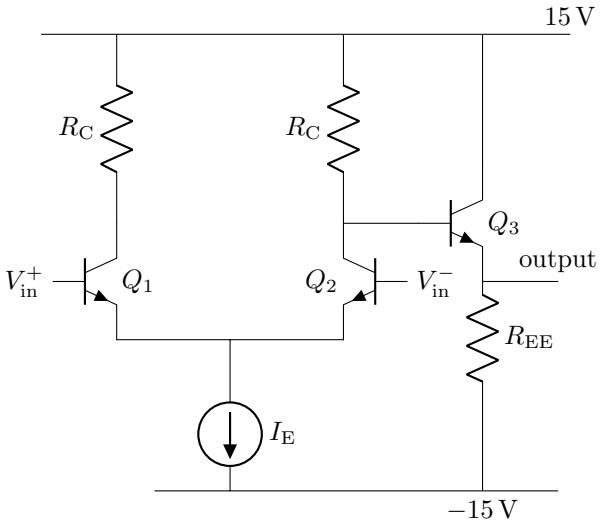
since $g_{\text{m}} = \frac{0.5\,\text{mA}}{25\,\text{mV}} = 0.02\,\text{S}$ Therefore $R_{\text{eq}} \approx 20 R_3$.
We can choose $\boxed{R_3 = 4.7\,\text{k}\Omega}$ to obtain a $R_{\text{eq}} = 94\,\text{k}\Omega$ The resistance seen by the C_{b} capacitor is equal to:

$$R_1 || R_2 || (R_{\text{eq}} + 100\,\text{k}\Omega) \approx 1.5\,\text{k}\Omega$$

Therefore we want the capacitive impedance of C_{b} at 100 Hz to be much lower than $1.5\,\text{k}\Omega$. Choosing a $\boxed{C_{\text{b}} = 10\,\mu\text{F}}$ should be enough.

Exercise 2.27

Figure 1.14: Differential pair and emitter follower



At DC, when $V_{\text{in}}^+ = V_{\text{in}}^- = 0\,\text{V}$ the current I_{E} is splitted equally between Q_1 and Q_2. Therefore, if the emitter current of both transistors has to be equal to 0.1 mA we have that $\boxed{I_{\text{E}} = 0.2\,\text{mA}}$ The differential gain G_{d} has to be equal to 50:

$$G_{\text{d}} = \frac{R_{\text{C}}}{2 r_{\text{E}}} = 50$$

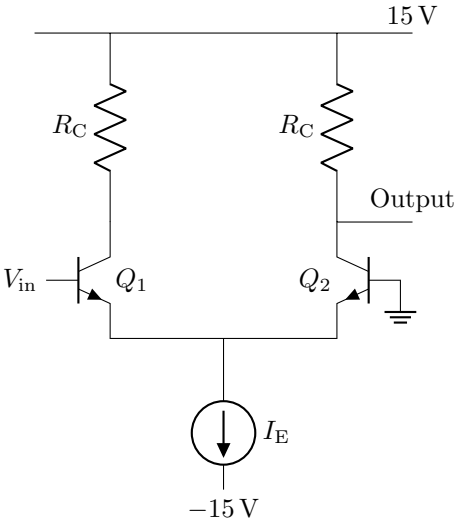
Since $R_{\text{E}} = 25\,\text{mV}/0.1\,\text{mA} = 250\,\Omega$, we have that $\boxed{R_{\text{C}} = 25\,\text{k}\Omega}$ If we also want the bias current of transistor Q_3 to be equal to 0.1 mA:

$$\boxed{R_{\text{EE}} = \frac{15\,\text{V} + 15\,\text{V} - 0.6\,\text{V} - R_{\text{C}}\,0.1\,\text{mA}}{0.1\,\text{mA}} \approx 270\,\text{k}\Omega}$$

As a final note, the differential pair is not degenerated. This led to a lower resistance R_{C} but to a higher resistance R_{EE} and a very small linearity region.

Exercise 2.28

Figure 1.15: Differential pair with current source emitter



(a)

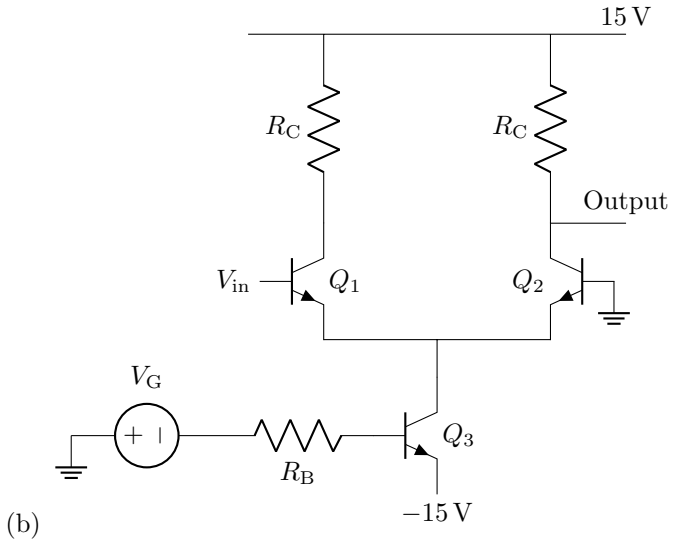
The quiscient current I_E will be equally divided among the two transistors Q_1 and Q_2. Therefore, in order to have a collector current equal to 100 µA, $\boxed{I_E = 200\,\mu A}$. The gain of the single ended input-output differential pair can be easily computed by considering that the equivalent resistance as seen from Q_2 emitter is equal to $r_E^{Q_2}$. Therefore, the gain will be equal to:

$$\boxed{G = \frac{R_C}{r_E^{Q_1} + r_E^{Q_2}} = \frac{R_C}{2r_E} = 20}$$

since:

$$r_E^{Q_1} = r_E^{Q_2} = r_E = \frac{25\,mV}{100\,\mu A} = 250\,\Omega$$

Figure 1.16: Differential pair with variable current emitter



In the circuit of Figure 1.16, the DC voltage V_G tunes the base current into the transistor Q_3 changing the quiescent current into the transistors Q_1 and Q_2. The value of the resistor R_B can be obtained by imposing that the maximum V_G voltage that doesn't saturate the transistors Q_1 and Q_2 is 10 V. By virtue of the V_{BE} of Q_2, the emitter of Q_1 and Q_2 is at -0.6 V with respect to ground. Therefore, the maximum collector current that doesn't cause Q_1 and Q_2 to saturate can be obtained as:

$$I_C^{\max} = \frac{15\,\text{V} + 0.6\,\text{V} - 0.2\,\text{V}}{R_C} = 1.54\,\text{mA}$$

The Q_3 maximum collector current will be twice I_C^{max}. Therefore, we have:

$$\beta \frac{15\,\text{V} - 10\,\text{V} - 0.6\,\text{V}}{R_B} = 2I_C^{\max}$$

which gives:

$$\boxed{R_B = 143\,\text{k}\Omega}$$

In order to compute the gain, first we have to compute the value of the quiescent collector current of Q_1 and Q_2. This will be equal to:

$$I_C^Q = \beta \frac{1}{2} \frac{15\,\text{V} - 0.6\,\text{V} - V_G}{R_B}$$

The gain will be equal to:

$$\boxed{G = \frac{1}{2} \frac{I_C^Q R_C}{25\,\text{mV}} \approx 70\,(14.4\,\text{V} - V_G)}$$

Exercise 2.29

(a) Since the quiescent point is equal to $0.5V_{CC}$, the quiescent collector current can be computed as:

$$I_C = \frac{1}{2} \frac{20\,\text{V}}{10\,\text{k}\Omega} = 1\,\text{mA}$$

Using the Ebers-Moll equation to derive the base quiescent voltage:

$$V_{\mathrm{BE}} = V_{\mathrm{T}} \ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}}\right) = 0.69\,\mathrm{V}$$

with a saturation current I_{S} equal to $1 \times 10^{-15}\,\mathrm{A}$, it is possible to estimate the value of the variable resistor R that leads to this voltage:

$$R = \frac{1\,\mathrm{k\Omega}\,0.69\,\mathrm{V}}{20\,\mathrm{V} - 0.69\,\mathrm{V}} = 35.8\,\Omega$$

The input impedance will be therefore the parralle between $1\,\mathrm{k\Omega}$, $35.8\,\Omega$ and $\beta\, r_{\mathrm{E}}$, being r_{E} the differential resistance of the transistor:

$$r_{\mathrm{E}} = \frac{I_{\mathrm{C}}}{V_{\mathrm{T}}} \approx 25\,\Omega$$

It follows that the input impedance Z_{in} is approximately equal to $34\,\Omega$

(b) The differential gain is equal to the ratio between the collector resistor and the differential resistor R_{E}. Therefore:

$$G = \frac{10\,\mathrm{k\Omega}}{25\,\Omega}$$

(c) Since the collector quiescent current approximately changes by $9\,\%\,^{\circ}\mathrm{C}^{-1}$, it is easily seen that its amount doubles for a temeprature change of $8\,^{\circ}\mathrm{C}$. This leads to a quiescent collector voltage equal to $20\,\mathrm{V}$ causing the transistor to saturate.

Exercise 2.30

The bias base current into Q_1 ($I_B^{Q_1}$) is the sum of the input bias current (from *input 1*: I^{I1}) and the collector current from the Q_4 transistor of the current mirror made of Q_4 and Q_3 ($I_C^{Q_4}$):

$$I_B^{Q_1} = I^{I1} + I_C^{Q_4}$$

Therrefore:

$$I^{I1} = I_B^{Q_1} - I_C^{Q_4}$$

Since Q_1 and Q_2 are beta matched, their base currents are the same since sharing the same collector current. The current mirror copies the base current of Q_2 on Q_4 and therefore $I_C^{Q_4} = I_B^{Q_1}$. It follows that:

$$I^{I1} = I_B^{Q_1} - I_C^{Q_4} = 0\,\mathrm{A}$$

In order for the circuit to operate correctly, all transistors have to work in active operation region. For this to be verified, the collector-base voltage has to be higher than zero for all transistors. Here the collector-base voltage of the transistor Q_1 is the critical one.

$$V_{\mathrm{CB}}^{Q_1} = -0.6\,\mathrm{V} - V_{\mathrm{CB}}^{Q_4}$$

$$V_{\mathrm{CE}}^{Q_4} = V_{\mathrm{E}} + 0.6\,\mathrm{V} - V_{\mathrm{M}}$$

where V_M is the bias voltage applied to the emitters of the current mirror.

$$V_{\mathrm{CB}}^{Q_4} = V_{\mathrm{CE}}^{Q_4} + 0.6\,\mathrm{V} = V_{\mathrm{E}} + 1.2\,\mathrm{V} - V_{\mathrm{M}}$$

By replacing the expression for $V_{\mathrm{CB}}^{Q_4}$ into that of $V_{\mathrm{CB}}^{Q_1}$ one finds:

$$V_{\mathrm{CB}}^{Q_1} = V_{\mathrm{M}} - V_{\mathrm{E}} - 1.8\,\mathrm{V}$$

If we want this to be higher than zero:

$$V_{\mathrm{M}} > V_{\mathrm{E}} + 1.8\,\mathrm{V}$$

$\boxed{V_{\mathrm{M}} = V_{\mathrm{E}} + 2\,\mathrm{V} \text{ is a quite safe value}}$