

Solutions to *The Art of Electronics 3rd Edition*

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# Solutions for Chapter 2

## Exercise 2.1

In order to solve this problem, many assumptions must be made. Different people may assume slightly different values for parameters. This is OK. What is important is making good assumptions and checking our conclusions to make sure they are reasonable.

To solve for the current in the LED, let us assume we know the LED is red, so it follows the red LED curve from Figure 2.8 in the book. Let us also assume the transistor is acting like a closed switch, so the collector voltage of Q1 is close to 0 V. Let us also assume the LED is ON, so its voltage is approximately  $V_{\text{LED}} = 2 \text{ V}$ . From the preceding assumptions, we can calculate that the LED current is

$$I_{\text{LED}} = \frac{3.3 \text{ V} - 2 \text{ V}}{330 \Omega} = \frac{1.3 \text{ V}}{330 \Omega} \approx 3.94 \text{ mA}$$

If we use Figure 2.8 (from the textbook) to check our numbers, we see that a current of 3.94 mA roughly correlates to an LED voltage of  $V_{\text{LED}} = 1.7 \text{ V}$ . We will run the same calculation again to reduce our error.

$$I_{\text{LED}}^* = \frac{3.3 \text{ V} - 1.7 \text{ V}}{330 \Omega} = \frac{1.6 \text{ V}}{330 \Omega} \approx \boxed{4.85 \text{ mA}}$$

In order to determine the minimum current gain required from our transistor, we must calculate the base current. Let us assume we know the base-emitter voltage  $V_{\text{BE}} = 0.6 \text{ V}$ . Therefore

$$I_{\text{B}} = \frac{3.3 \text{ V} - 0.6 \text{ V}}{10 \text{ k}\Omega} = 270 \mu\text{A}$$

So the minimum current gain must be

$$\beta_{\text{min}} = \frac{I_{\text{LED}}^*}{I_{\text{B}}} \approx \frac{4.85 \text{ mA}}{270 \mu\text{A}} \approx \boxed{18.0}$$

## Exercise 2.2

When  $Q_1$  goes is in saturation, the base voltage of  $Q_2$  equals the opposite of the voltage on the capacitor  $C_1$  at  $t = 0 \text{ s}$ ,  $V_0 = 4.4 \text{ V}$  and  $Q_2$  is then cutoff.  $V_{\text{out}}$  will be equal to 5 V until  $Q_2$  is brought in saturation again. This happens when its base voltage gets higher or equal to the  $Q_2$  threshold voltage (0.6 V). As soon as  $Q_1$  is brought in saturation,  $C_1$  starts to discharge into the resistor  $R_3$  and the equivalent circuit, valid until  $Q_2$  is cutoff, is then:

Figure 1.1: Equivalent  $C_1$  discharging circuit.

The time evolution of the voltage across the capacitor  $C_1$  is given by:

$$V_C(t) = (V_0 - V_\infty) e^{-\frac{t}{R_3 C_1}} + V_\infty$$

where  $V_\infty$  is the steady-state voltage on the capacitor  $C_1$  end equals  $-5\text{ V}$ . Given the considerations above, we have that  $V_C(t = T_{\text{pulse}}) = -0.6\text{ V}$ . Solving for  $t$  gives:

$$T_{\text{pulse}} = -R_3 C_1 \ln \left( \frac{-0.6\text{ V} - V_\infty}{V_0 - V_\infty} \right) = \boxed{0.76 R_3 C_1 = 76\text{ }\mu\text{s}}$$

### Exercise 2.3

The output voltage is now influenced by  $R_5$  that goes in series with  $R_4$ , and by the  $V_{\text{BE}}$  of  $Q_3$  which is equal to  $0.6\text{ V}$  when the transistor is in saturation. Therefore:

$$V_{\text{out}} = \frac{R_5}{R_5 + R_4} (5\text{ V} - 0.6\text{ V}) + 0.6\text{ V} = \boxed{4.79\text{ V}}$$

The minimum value of  $\beta$  of  $Q_3$  can be obtained looking at the maximum value of the current flowing through the collector of  $Q_3$ ,  $I_c^{Q_3}$ . As soon as  $Q_1$  goes in saturation, the capacitor  $C_1$  starts to discharge and its current is given by  $C_1 dV_C/dt$ . With reference to the variables introduced in the previous exercise (2.2):

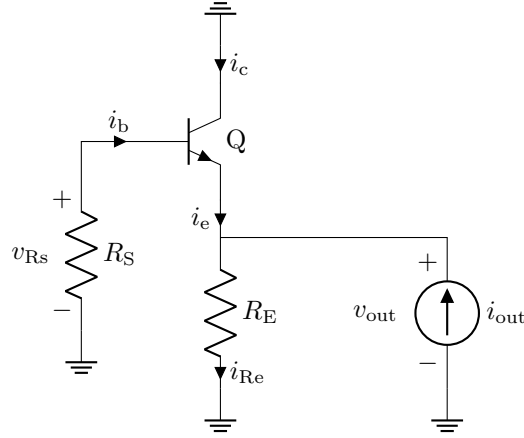
$$I_c^{Q_3}(t) = \frac{5\text{ V}}{R_2} - I_{C_1}(t) = \frac{5\text{ V}}{R_2} + C_1 \frac{1}{R_3 C_1} (V_0 - V_\infty) e^{-\frac{t}{R_3 C_1}}$$

Therefore:

$$\beta_{\min} = \frac{I_c^{Q_3}(t)|_{\max}}{I_b^{Q_3}} = \frac{I_c^{Q_3}(t=0\text{ s})}{I_b^{Q_3}} = \boxed{27}$$

## Exercise 2.4

Figure 1.2: Emitter follower circuit used for computing the output resistance



Applying the KCL on the Q transistor:

$$i_e = i_b + i_c = i_b (\beta + 1)$$

The current flowing through the emitter resistor  $R_E$  is equal to:

$$i_{Re} = i_e + i_{out} = i_b (\beta + 1) + i_{out}$$

Since for the emitter follower  $v_{Rs} = v_{out}$ :

$$[i_b (\beta + 1) + i_{out}] R_E = v_{out}$$

Since:

$$i_b = -\frac{v_{Rs}}{R_S} = -\frac{v_{out}}{R_S}$$

we can write:

$$\left[ -\frac{v_{out}}{R_S} (\beta + 1) + i_{out} \right] R_E = v_{out}$$

Therefore:

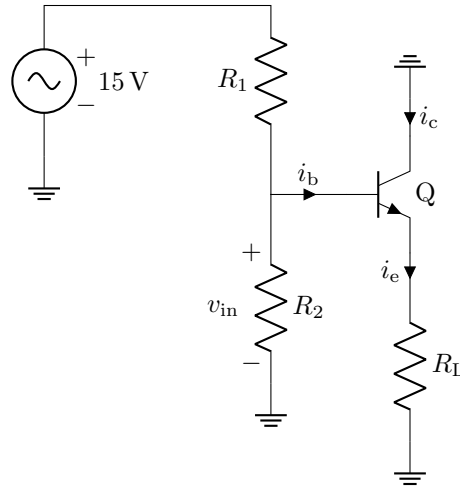
$$R_{out} = \frac{v_{out}}{i_{out}} = \frac{R_E R_S}{R_S + (\beta + 1) R_E}$$

If  $R_E \gg R_S/(\beta + 1)$ :

$$R_{out} \approx \frac{R_S}{(\beta + 1)}$$

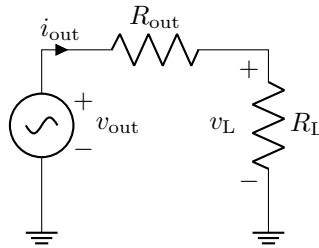
## Exercise 2.5

Figure 1.3: Small signal circuit



In order to achieve a maximum voltage change of 5% for a maximum current to the load ( $R_L$ ) equal to 25 mA, we can make reference to the equivalent circuit of Figure 1.4:

Figure 1.4: Output equivalent circuit



obtaining:

$$\left. \frac{v_{\text{out}} - v_L}{v_{\text{out}}} \right|_{i_{\text{out}}=25 \text{ mA}} = 0.05$$

Since

$$v_{\text{out}} - R_{\text{out}} i_{\text{out}} = v_L$$

and for an emitter follower  $v_{\text{out}} = v_{\text{in}} = 5 \text{ V}$  we can write:

$$\frac{R_{\text{out}} 25 \text{ mA}}{5 \text{ V}} = 0.05$$

obtaining the following condition on  $R_{\text{out}}$ :

$$R_{\text{out}} = \frac{0.05 \cdot 5 \text{ V}}{25 \text{ mA}}$$



For the emitter follower configuration:

$$R_{\text{out}} = \frac{R_{\text{in}}}{\beta + 1}$$

and we see from the circuit of Figure 1.3 that  $R_{\text{in}}$  is given by the parallel between  $R_1$  and  $R_2$ :

$$R_{\text{in}} = \frac{R_1 R_2}{R_1 + R_2}$$

In order to achieve  $v_{\text{in}} = 5 \text{ V}$ , the following condition must be verified for the values of  $R_1$  and  $R_2$ :

$$\frac{R_2}{R_1 + R_2} = \frac{5 \text{ V}}{15 \text{ V}}$$

Assuming  $\beta = 100$ , we can finally obtain:

$$\boxed{R_1 = 30 \Omega, R_2 = 15 \Omega}$$

## Exercise 2.6

The minimum current flowing through the  $R$  resistor has to be at least equal to the maximum current to the load plus the minimum current to the zener:

$$I_{\text{min},R} = \frac{20 \text{ V} - 10 \text{ V}}{R} \geq 100 \text{ mA} + 10 \text{ mA}$$

Therefore:

$$R \leq \frac{10 \text{ V}}{110 \text{ mA}} = \boxed{91 \Omega}$$

It follows that the maximum power to the zener, selecting  $R = 91 \Omega$ , is equal to

$$P_{\text{max},z} = \left( \frac{25 \text{ V} - 10 \text{ V}}{91 \Omega} - 0 \text{ A} \right) 10 \text{ V} = \boxed{1.65 \text{ W}}$$

## Exercise 2.7

With reference to figure 2.21 of the book, neglecting the current entering the base of the transistor  $Q$ , in order to have at least 10 mA flowing through the zener, the resistor  $R$  should comply with the following condition:

$$\frac{20 \text{ V} - 10 \text{ V}}{R} \geq 10 \text{ mA}$$

which results in:

$$\boxed{R \leq 1 \text{ k}\Omega}$$

In order to avoid the transistor to be saturated, we want the collector-base voltage to be always higher than zero. This translates in:

$$R_C < R \frac{10 \text{ mA}}{100 \text{ mA}} = 100 \Omega$$

Selecting a conservative value of  $R_C$  equal to  $\boxed{20 \Omega}$ , we can compute the maximum power dissipated by the zener,  $P_{\text{max},z}$  and the transistor,  $P_{\text{max},Q}$  as:

$$P_{\text{max},z} = \left( \frac{25 \text{ V} - 10 \text{ V}}{1 \text{ k}\Omega} \right) 10 \text{ V} = \boxed{0.15 \text{ W}}$$

$$P_Q = (25 \text{ V} - 20 \Omega I_{\text{load}}) I_{\text{load}}$$

The maximum power dissipated by the transistor is obtained for a collector current equal to 625 mA which is higher than the maximum load current. Therefore, in our case, the maximum power dissipated by  $Q$  will be obtained for  $I_{\text{load,max}} = 100 \text{ mA}$ :

$$P_{\text{max,Q}} = (25 \text{ V} - 20 \Omega I_{\text{load,max}}) I_{\text{load,max}} = \boxed{2.3 \text{ W}}$$

Comparing the results with those of the previous exercise, we notice that the power dissipated by the zener diode significantly decreased but we have an additional power dissipated by the transistor which is higher than the power that the zener diode dissipated in the circuit of the previous exercise. However this power can be decreased by increasing the value of  $R_C$ .

## Exercise 2.8

In order to keep the emitter voltage  $V_E$  in the half range of the dc supply, considering the quiescent current of 5 mA we have:

$$V_E = \frac{15 \text{ V} - (-15 \text{ V})}{2} = 15 \text{ V}$$

and the emitter resistor  $R_E$ :

$$R_E = \frac{15 \text{ V}}{5 \text{ mA}} = \boxed{3 \text{ k}\Omega}$$

Since the input impedance to the transistor, under the assumption of a load resistance much larger than the emitter resistance, is:

$$R_{\text{in}} = \beta R_E = 300 \text{ k}\Omega$$

in order to have the 3 dB point below the lowest frequency of 20 Hz, the capacitor  $C_1$  has to be:

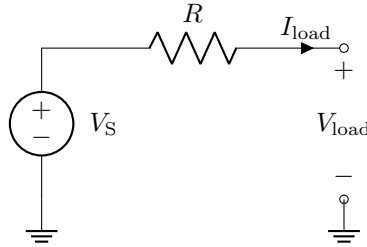
$$\frac{1}{R_{\text{in}} C_1} \leq 20 \text{ Hz}$$

meaning that:

$$\boxed{C_1 \geq 0.17 \mu\text{F}}$$

## Exercise 2.9

Figure 1.5: Current source circuit



We want:

$$\frac{I_{\text{load}}^{\text{max}} - I_{\text{load}}^{\text{min}}}{I_{\text{load}}^{\text{max}}} = \frac{V_S - 0 \text{ V} - (V_S - 10 \text{ V})}{V_S - 0 \text{ V}} = 0.01$$

from which it follows:

$$\boxed{V_S = 1 \text{ kV}}$$

## Exercise 2.10

With reference to Figure 1.5, we assume that  $I_{\text{load}}$  is equal to 10 mA if  $V_{\text{load}}$  is equal to 0 V, which means  $R_{\text{load}}$  is equal to 0  $\Omega$ . We can therefore calculate  $R$  as:

$$R = \frac{V_S}{10 \text{ mA}} = 100 \text{ k}\Omega$$

In this case we have:

$$P_{\text{load}} = 0 \text{ W}, P_R = I_{\text{load}}^2 R = 10 \text{ W}$$

If  $V_{\text{load}} = 10 \text{ V}$ , from the condition of the previous exercise, we have:

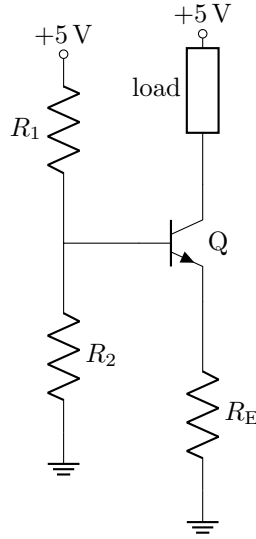
$$I_{\text{load}} = (1 - 0.01)10 \text{ mA} = 9.9 \text{ mA}$$

Therefore:

$$P_{\text{load}} = 10 \text{ V} I_{\text{load}} = 0.1 \text{ W}, P_R = I_{\text{load}}^2 R = 9.8 \text{ W}$$

## Exercise 2.11

Figure 1.6: Current sink



In order to have an emitter current equal to 5 mA, the following condition has to be verified:

$$\frac{R_2}{R_1 + R_2} 5 \text{ V} - 0.6 \text{ V} = R_E 5 \text{ mA}$$

Furthermore, the transistor shouldn't sensibly load the voltage divider, therefore:

$$\frac{R_1 R_2}{R_1 + R_2} \ll R_E \beta$$

Since we have a dc voltage of 5 V, we want the voltage on  $R_2$  to be lower or equal to this value:

$$R_E 5 \text{ mA} + 0.6 \text{ V} \leq 5 \text{ V}$$

leading to:

$$R_E \leq 880 \Omega$$

A good guess value for  $R_E$  could be:

$$R_E = 200 \Omega$$

The base voltage will be given by:

$$V_B = R_E 5 \text{ mA} + 0.6 \text{ V} = 1.6 \text{ V}$$

Selecting  $R_1 = 1 \text{ k}\Omega$  it is possible to compute  $R_2$ :

$$R_2 = 470 \Omega$$

The impedance seen by the input of the transistor is equal to  $320 \Omega$  and the input impedance of the transistor, considering  $\beta = 100$ , is  $R_E \beta = 20 \text{ k}\Omega$  with the former much lower than the latter. Finally, considering a maximum  $V_{CE}$  voltage of the transistor equal to  $0.2 \text{ V}$  before it saturates, we obtain the compliance voltage on the load as:

$$V_{\text{comp}} = 5 \text{ V} - (0.2 \text{ V} + R_E 5 \text{ mA}) = 3.8 \text{ V}$$

## Exercise 2.12

The distortion is given by:

$$\frac{\Delta V_{\text{out}}}{V_{\text{drop}}} \frac{V_T}{V_T + I_E R_E}$$

therefore, if  $R_E = 0 \Omega$  we obtain a predicted distortion equal to  $\frac{\Delta G}{G} = \frac{0.2 \text{ V}}{5 \text{ V}} = 0.04$  in case of  $0.1 \text{ V}$  output

amplitude and  $\frac{\Delta G}{G} = \frac{2 \text{ V}}{5 \text{ V}} = 0.4$  in case of  $1 \text{ V}$  output amplitude. If  $R_E I_E = 0.25 \text{ V}$ ,  $\frac{\Delta G}{G}$  equals to  $0.004$  and  $0.04$  for output voltage amplitudes equal to  $0.1 \text{ V}$  and  $1 \text{ V}$ , respectively.

## Exercise 2.13

If the transistor is biased at half  $V_{cc}$ , we have that the collector-emitter voltage will be equal to  $V_{CE} = V_{cc} - I_C R_C = V_{cc} - V_{cc}/2 = V_{cc}/2$  where  $I_C$  is the collector quiescent current and  $R_C$  is the collector resistor. The collector-base voltage will be therefore  $V_{CB} = V_{cc}/2 - V_{BE}$ . In this case  $V_{BE}$  is supposed to be obtained by means of a voltage divider. If the temperature changes, approximately  $V_{BE}$  does not change and the collector current will increase by  $9\% \text{ } ^\circ\text{C}^{-1}$ . This means that the collector current doubles for a temperature increase equal to  $8^\circ\text{C}$ . In this case  $R_C I_C$  becomes equal to  $2V_{cc}/2 = V_{cc}$ . As a consequence

$$V_{CB} = -V_{BE} < 0 \text{ and the transistor goes in saturation.}$$

## Exercise 2.14

The bias is arranged in order to have a collector current equal to  $1 \text{ mA}$ . Indeed:

$$I_c = \frac{0.775 \text{ V} - 0.6 \text{ V}}{175 \Omega} = 1 \text{ mA}$$

The base-emitter voltage decreases by  $2.1 \text{ mV } ^\circ\text{C}^{-1}$ . Therefore, if the temperature increases by  $20^\circ\text{C}$ , the collector current will become:

$$I_c = \frac{0.775 \text{ V} - 0.6 \text{ V} - 0.0021 \text{ V } ^\circ\text{C}^{-1} 20^\circ\text{C}}{175 \Omega} = 0.76 \text{ mA}$$

It can be seen that the new collector current is about  $25\%$  lower than  $1 \text{ mA}$

## Exercise 2.15

The voltage gain is given by:

$$G = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R_C}{r_e} = \frac{I_C R_C}{V_T}$$

In order to achieve a voltage drop on  $R_C$  equal to half the  $V_{cc}$  voltage:

$$I_C R_C = \frac{1}{2} V_{cc}$$

and therefore:

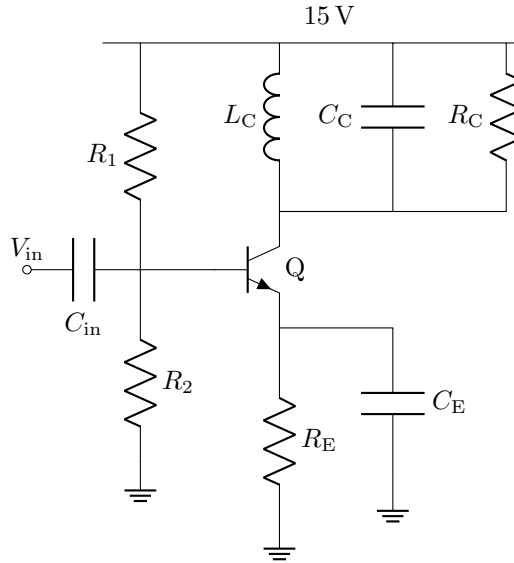
$$R_C = \frac{1}{2} \frac{V_{cc}}{I_C}$$

Substituting the  $R_C$  expression into the voltage gain:

$$G = \frac{1}{2} \frac{V_{cc}}{V_T} = \frac{V_{cc}}{50 \text{ mV}} = 20 V_{cc}$$

## Exercise 2.16

Figure 1.7: Tuned common emitter amplifier



With reference to Figure 1.7, we start by choosing the emitter resistor  $R_E$ . We want its value to be large enough to have a voltage drop higher than  $V_{BE}$  in order to have a good stability of the quiescent current with the temperature. However we want the transistor to operate in the active region. Since at DC, the inductor behaves like a short circuit, we have that the collector voltage is equal to  $V_{cc}$ , therefore:

$$R_E I_E^Q < V_{cc} - 0.2 \text{ V}$$

and

$$R_E < \frac{V_{cc} - 0.2 \text{ V}}{I_E^Q} = 14.8 \text{ k}\Omega$$

where  $I_E^Q$  is equal to about 1 mA. We choose:

$$R_E = 1 \text{ k}\Omega$$

In order to achieve a quiescent current equal to 1 mA, the base voltage has to be equal to:

$$V_B = 0.6 \text{ V} + R_E I_E^Q = 1.6 \text{ V}$$

Therefore, the ratio between  $R_1$  and  $R_2$  has to be equal to 8.4. Choosing the parallel resistance of  $R_1$  and  $R_2$  to be about one tenth of the transistor input resistance  $\beta R_E \approx 100 \text{ k}\Omega$  we choose the following values for  $R_1$  and  $R_2$ :

$$R_1 = 84 \text{ k}\Omega, \quad R_2 = 10 \text{ k}\Omega$$

The value of the capacitor  $C_C$  can be obtained forcing the parallel LC circuit to resonate at 100 kHz:

$$\frac{1}{2\pi} \sqrt{\frac{1}{L_C C_C}} = 100 \text{ kHz}$$

Therefore:

$$C_C = 2.5 \text{ nF}$$

The value of the capacitor  $C_E$  can be selected imposing that the absolute value of the impedance of the parallel between  $R_E$  and  $C_E$  is lower than  $r_e = 25 \Omega$  for a quiescent current of 1 mA. Doing the math we obtain:

$$C_E > \frac{\sqrt{\frac{R_E^2}{25 \Omega} - 1}}{\omega R_E} = 63.6 \text{ nF}$$

A value of  $C_E$  equal to 10  $\mu\text{F}$  is conservative enough to maximise the AC gain:

$$C_E = 10 \mu\text{F}$$

It remains to calculate the value of the input decoupling capacitor  $C_{in}$ . Its value can be obtained by forcing the cut-off frequency  $1/R_{in}$  to be below 100 kHz where

$$R_{eq} = \beta r_e || R_1 || R_2$$

where we neglected the emitter impedance which is verly low thanks to the  $C_E$  effect. We have therefore:

$$C_{in} \geq 5 \text{ nF}$$

Even in this case a conservative value for  $C_{in}$  can be:

$$C_{in} = 10 \mu\text{F}$$

## Exercise 2.17

In the following, the pedix B, C and E refer to base, collector and emitter. The apix Q1, Q2 and Q3 refer to the relevant transistors. Supposing all the transistors share the same  $\beta$ , the  $I_P$  current can be expressed as:

$$I_P = I_C^{Q1} + I_B^{Q3} = \beta I_B^{Q1} + \frac{I_C^{Q3}}{\beta}$$

Since the base-emitter voltage of the transistor Q1 is the same of the transistor Q2, the base currents are the same. Therefore:

$$I_B^{Q1} + I_B^{Q2} = 2I_B^{Q1} = I_E^{Q3} - I_C^{Q1} = \frac{\beta + 1}{\beta} I_C^{Q3} - \beta I_B^{Q1}$$

and then:

$$I_B^{Q1} = \frac{\beta + 1}{\beta(\beta + 2)} I_C^{Q3}$$

Substituting this expression into the first equation, it is possible to obtain the following expression for  $I_P$ :

$$I_P = \left(1 + \frac{2}{\beta(\beta + 2)}\right) I_C^{Q3} \approx I_C^{Q3}$$

By comparing the above expression with that that typical of a basic current mirror:

$$I_P = \left(1 + \frac{2}{\beta}\right) I_C$$

one can see that the load current  $I_C^{Q3}$  is much closer to the reference current  $I_P$  than for the basic current mirror. Indeed:

$$\frac{2}{\beta(\beta + 2)} \ll \frac{2}{\beta}$$

## Exercise 2.18

For a grounded differential amplifier, the differential gain is:

$$G_{\text{diff}} = \frac{R_C}{2r_e} = \frac{R_C I_C}{2V_T} = V_C 2V_{\text{ext}} T = \boxed{20V_C}$$

where  $V_C$  is the voltage drop across the collector resistor  $R_C$ . Therefore, if  $V_C = 0.5V_{\text{cc}}$ :

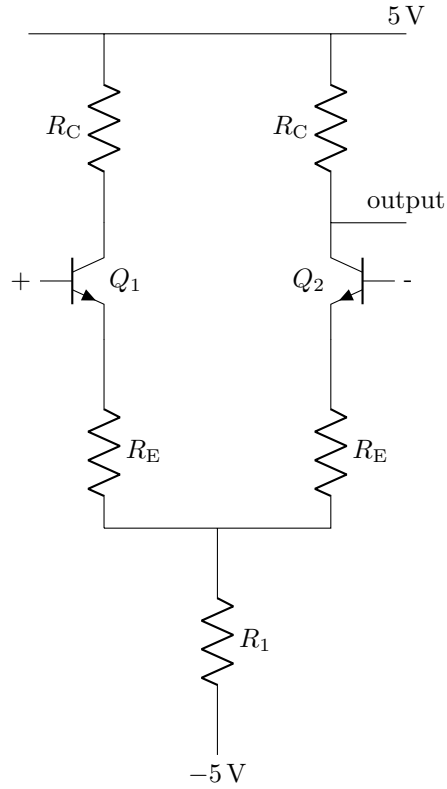
$$\boxed{G_{\text{diff}} = 10V_{\text{cc}}}$$

Following a similar argument:

$$\text{CMRR} = \frac{R_1}{r_e} = \frac{R_1 I_C}{V_T} = \frac{1}{2} V_1 V_T = \boxed{20V_1}$$

where  $V_1$  is the voltage drop across the  $R_1$  resistor.

Figure 1.8: Tuned common emitter amplifier



For the differential, single-ended amplifier in Figure 1.8, the output impedance is equal to  $R_C$ . Therefore we have  $R_C = 10\text{ k}\Omega$ . Since we want the voltage drop on the collector resistor to be half of the  $V_{cc}$ :

$$I_C = 2.5\text{ V} / 10\text{ k}\Omega = 250\text{ }\mu\text{A}$$

Neglecting the voltage drop on the emitter resistor  $R_E$ , we can approximate the collector current as:

$$I_C \approx \frac{5\text{ V} - 0.6\text{ V}}{2R_1}$$

and therefore:

$$R_1 = 2.8\text{ k}\Omega$$

The value of  $R_E$  can then be obtained from the differential gain, considering that it is given by:

$$G_{\text{diff}} = 25 = \frac{R_C}{2(r_e + R_E)}$$

. Therefore, considering that  $r_e = V_T / I_C = 100\text{ }\Omega$ :

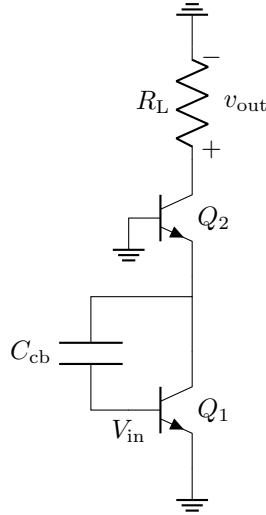
$$R_E = 100\text{ }\Omega$$



## Exercise 2.19

As regards the differential amplifier in Figure 2.84 of the book, the AC voltage across the  $C_{CB}$  capacitor is equal to the voltage at the base of the transistor  $Q_1$  without depending on the voltage gain. The voltage across the emitter resistor  $R_E$  is the input to a common base amplifier which does not have Miller effect.

Figure 1.9: Cascode amplifier



As regards the cascode configuration, one can make reference to Figure 1.9. Under the approximation that the collector current of the transistor  $Q_1$  is equal to that of the transistor  $Q_2$ :

$$i_C^{Q_1} = i_C^{Q_2} = \frac{v_{in}}{r_e^{Q_1}}$$

where  $r_e^{Q_1}$  is the differential resistance of the  $Q_1$  transistor. The output voltage will be:

$$v_{out} = R_L i_C^{Q_2}$$

The base-emitter AC voltage of the  $Q_2$  transistor will be:

$$v_{BE}^{Q_2} = r_e^{Q_2} i_C^{Q_2}$$

where  $r_e^{Q_2}$  is the differential resistance of the  $Q_2$  transistor.

The voltage across the  $C_{CB}$  capacitor will be:

$$v_{CB} = v_{in} + v_{BE}^{Q_2} = v_{in} + \frac{v_{in} r_e^{Q_2}}{r_e^{Q_1}}$$

It follows that the amplitude of the current through the  $C_{CB}$  capacitor is:

$$I_{CB} = \frac{v_{in} \left( 1 + \frac{r_e^{Q_2}}{r_e^{Q_1}} \right)}{X_{CB}}$$

where  $X_{CB}$  is the capacitive reactance associated to the  $C_{CB}$  capacitor. The Miller capacitance  $C_{CB}^M$  is therefore:

$$C_{CB}^M = C_{CB} \left( 1 + \frac{r_e^{Q_2}}{r_e^{Q_1}} \right)$$

and does not depend on the voltage gain of the cascode amplifier.

## Exercise 2.20

The expression for the input impedance of the inverting amplifier is straightforward by considering that it is the series between the  $R_1$  resistance with the input impedance of the transresistance amplifier. Therefore, the input impedance  $Z_{in}$  is:

$$Z_{in} = R_1 + R_{in} \parallel \frac{R_2}{1 + A}$$

The closed loop gain can also be obtained in a straightforward way starting by considering the input impedance of the operational amplifier,  $R_{in}$ , approaching to infinity. In this case, all the current flowing in  $R_1$  goes in  $R_2$  making  $R_1$  and  $R_2$  in series. Therefore:

$$V_{out} = vA$$

where  $v$  is the differential voltage of the operational amplifier and  $A$  is the open loop gain.  $v$  is given by:

$$v = -[V_{in} - (V_{in} - V_{out})B]$$

where  $B$  is defined as:

$$\frac{R_1}{R_1 + R_2}$$

The expression for the output voltage becomes:

$$V_{out} = -A[V_{in} - (V_{in} - V_{out})B]$$

and the closed loop gain is:

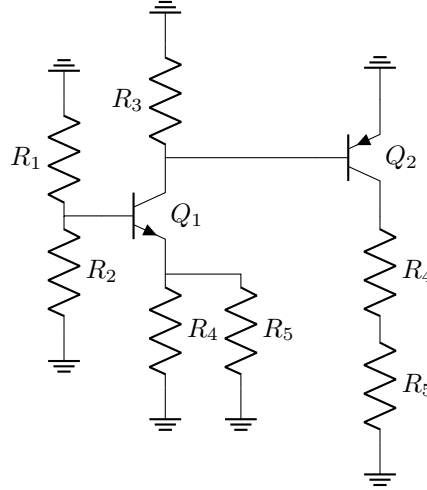
$$G = \frac{V_{out}}{V_{in}} = -A \frac{1 - B}{1 + AB}$$

## Exercise 2.21

$$G_{CL} = \frac{-100j}{1 + -100j(0.1)} = 9.90 - 0.99j$$

## Exercise 2.22

Figure 1.10: Open loop small signal circuit



The feedback takes the voltage from the output of Q2 transistor and returns it to the input of the Q1 transistor through a voltage divider made of the resistors  $R_4$  and  $R_5$ . The feedback is of *voltage-voltage* kind. In order to account for the feedback loading effect in opening the loop, the reference circuit is that of Figure 1.10. Considering a  $\beta$  of 100 for both Q1 and Q2, the open loop gain is:

$$G^{\text{OL}} = \frac{-1}{r_e^{\text{Q1}} + R_4 || R_5} [R_3 || r_e^{\text{Q2}} \beta] \left[ -\frac{R_4 + R_5}{r_e^{\text{Q2}}} \right] \approx \frac{1}{r_e^{\text{Q1}} + R_4} [R_3 || r_e^{\text{Q2}} \beta] \left[ \frac{R_5}{r_e^{\text{Q2}}} \right]$$

Therefore, since  $r_e^{\text{Q1}} = r_e^{\text{Q2}} = 25 \Omega$ :

$$G^{\text{OL}} \approx 200$$

The feedback gain is:

$$B = \frac{R_4}{R_4 + R_5} \approx \frac{R_4}{R_5} = 0.1$$

Therefore, the loop gain is:

$$G^{\text{OL}} B \approx 20$$

The open loop output impedance is:

$$Z_{\text{out}}^{\text{OL}} = R_4 + R_5 \approx R_5 = 10 \text{ k}\Omega$$

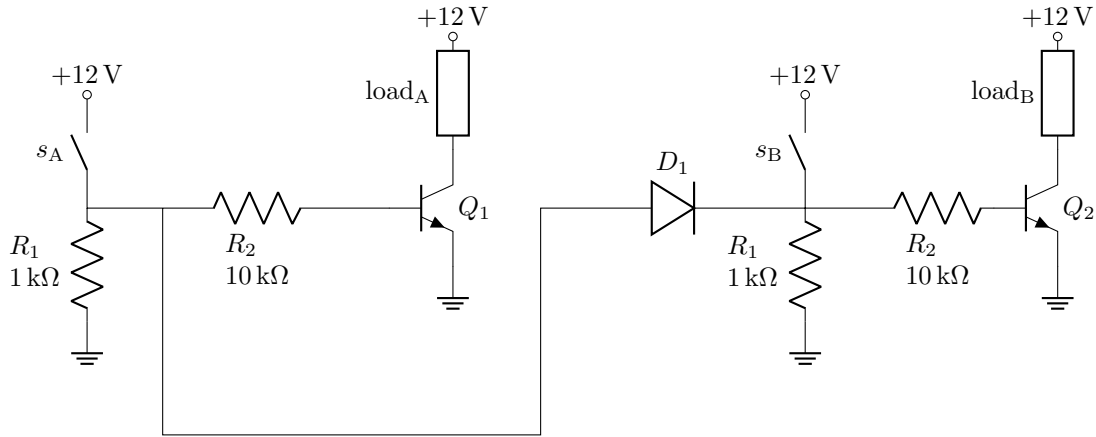
The closed loop parameters are therefore:

$$G^{\text{CL}} = \frac{G^{\text{OL}}}{1 + G^{\text{OL}} B} \approx 9.5$$

$$Z_{\text{out}}^{\text{CL}} = \frac{Z_{\text{out}}^{\text{OL}}}{1 + G^{\text{OL}} B} \approx \frac{Z_{\text{out}}^{\text{OL}}}{G^{\text{OL}} B} = 500$$

**Exercise 2.23**

Figure 1.11: Solution



Let's suppose the loads are resistive with a resistance equal to  $150\,\Omega$  and both the npn transistors have  $\beta = 100$ . When  $s_A$  and  $s_B$  are open, both  $Q_1$  and  $Q_2$  bases are to ground and no current flows into the loads.

If  $s_A$  is closed, the left terminals of the  $R_2$  resistors are at 12 V (minus a diode voltage drop for the resistor connected at the  $Q_2$  base). The base currents are therefore:

$$I_b = \frac{12\,\text{V} - 0.6\,\text{V}}{10\,\text{k}\Omega} = 1.14\,\text{mA}$$

Such a base current, with the considered  $\beta$  and load resistance, causes  $Q_1$  and  $Q_2$  to saturate. Therefore, the load current is:

$$I_1^A = I_1^B = \frac{12\,\text{V} - 0.2\,\text{V}}{150\,\Omega} = 79\,\text{mA}$$

When  $s_A$  is open and  $s_B$  is closed,  $D_1$  is reverse biased and  $Q_1$  is in cutoff region since no current flows into its base. However, 1.14 mA flows into the base of  $Q_2$  which goes into saturation.

Exercise 2.24 **TODO: write solution**

Exercise 2.25 **TODO: write solution**

Exercise 2.26 **TODO: write solution**

Exercise 2.27 **TODO: write solution**

Exercise 2.28 **TODO: write solution**

Exercise 2.29 **TODO: write solution**

Exercise 2.30 **TODO: write solution**