# Solutions to *The Art of Electronics 3rd Edition*

December 11, 2023

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# Solutions for Chapter 1

## Exercise 1.1

(a) $R = 5\,\mathrm{k\Omega} + 10\,\mathrm{k\Omega} = \boxed{15\,\mathrm{k\Omega}}$

(b) $R = \dfrac{R_1 R_2}{R_1 + R_2} = \dfrac{5\,\mathrm{k\Omega} \times 10\,\mathrm{k\Omega}}{5\,\mathrm{k\Omega} + 10\,\mathrm{k\Omega}} = \boxed{3.33\,\mathrm{k\Omega}}$

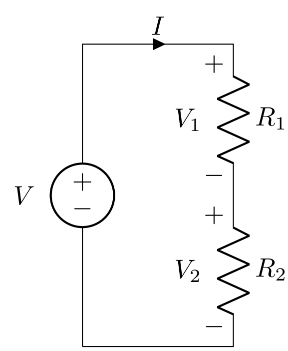
## Exercise 1.2

$$P = IV = \left(\frac{V}{R}\right) V = \frac{(12\,\mathrm{V})^2}{1\,\Omega} = \boxed{144\,\mathrm{W}}$$

## Exercise 1.3

Consider a simple series resistor circuit.

Figure 1.1: A basic series circuit.




By KVL and Ohm's law

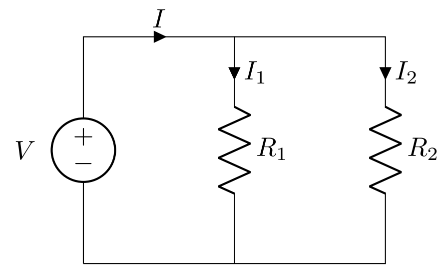
$$V = V_1 + V_2 = R_1 \cdot I + R_2 \cdot I = (R_1 + R_2) \cdot I = R \cdot I$$

where

$$\boxed{R = R_1 + R_2}$$

is the resistance of $R_1$ and $R_2$ in series. Now, consider a simple parallel resistor circuit.

Figure 1.2: A basic parallel circuit.




By KCL and Ohm's law

$$I = I_1 + I_2 = \frac{V}{R_1} + \frac{V}{R_2} = \left(\frac{1}{R_1} + \frac{1}{R_2}\right) \cdot V$$

solving for V as a function of I we get

$$V = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} \cdot I = \frac{R_1 R_2}{R_1 + R_2} \cdot I = R \cdot I$$

where

$$\boxed{R = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} = \frac{R_1 R_2}{R_1 + R_2}}$$

is the resistance of $R_1$ and $R_2$ in parallel.

## Exercise 1.4

We known that the resistance $R_{12}$[1] of two resistors $R_1$ and $R_2$ in parallel is given by

$$R_{12} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}}$$

Now, the resistance $R_{123}$ of three resistors $R_1$, $R_2$ and $R_3$ in parallel is equal to the resistance of two resistors $R_{12}$ (the resistance between $R_1$ and $R_2$ in parallel) and $R_3$ in parallel, then

$$R_{123} = \frac{1}{\frac{1}{R_{12}} + \frac{1}{R_3}} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

We will prove by induction that the resistance $R_{1\cdots n}$ of $n$ resistances $R_1, R_2, \ldots, R_n$ in parallel is given by

$$R_{1\cdots n} = \frac{1}{\sum_{i=1}^{n} \frac{1}{R_i}}$$

First, it's trivial to show that with $n = 1$ the equality holds. Now, we will assume that the equality is satisfied for $n = k$, that is

$$R_{1\cdots k} = \frac{1}{\sum_{i=1}^{k} \frac{1}{R_i}}$$

[1] Here we have only assigned a name to the resistance in parallel between $R_1$ and $R_2$.

Then, we must show that equality holds for $n = k+1$. Thus, the resistance $R_{1\cdots(k+1)}$ of $(k+1)$ resistances $R_1, R_2, \ldots, R_{k+1}$ in parallel is equal to the resistance of two resistors $R_{1\cdots k}$ and $R_{k+1}$ in parallel, then

$$R_{1\cdots(k+1)} = \frac{1}{\frac{1}{R_{1\cdots k}} + \frac{1}{R_{k+1}}} = \frac{1}{\sum_{i=1}^{k} \frac{1}{R_i} + \frac{1}{R_{k+1}}} = \frac{1}{\sum_{i=1}^{k+1} \frac{1}{R_i}}$$

where we have proved that equality holds for $n = k+1$. Finally, the resistance of $n$ resistors in parallel is given by

$$\boxed{R_{1\cdots n} = \frac{1}{\sum_{i=1}^{n} \frac{1}{R_i}} = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \ldots + \frac{1}{R_n}}}$$

## Exercise 1.5

Given that $P = \dfrac{V^2}{R}$, we know that the maximum voltage we can achieve is 15 V and the smallest resistance we can have across the resistor in question is 1 kΩ. Therefore, the maximum amount of power dissipated can be given by

$$P = \frac{V^2}{R} = \frac{(15\,\mathrm{V})^2}{1\,\mathrm{k\Omega}} = \boxed{0.225\,\mathrm{W}}$$

This is less than the 0.25 W power rating.

## Exercise 1.6

(a) The total current required by New York City that will flow through the cable is

$$I = \frac{P}{V} = \frac{1 \times 10^{10}\,\mathrm{W}}{115\,\mathrm{V}} = 86.96\,\mathrm{MA}$$

Therefore, the total power lost per foot of cable can be calculated by:

$$P = I^2 R = \left(86.96 \times 10^6\,\mathrm{A}\right)^2 \times \left(5 \times 10^{-8}\,\Omega/\mathrm{ft}\right) = \boxed{3.78 \times 10^8\,\mathrm{W/ft}}$$

(b) The length of cable over which all $1 \times 10^{10}$ W will be lost is:

$$L = \frac{1 \times 10^{10}\,\mathrm{W}}{3.78 \times 10^8\,\mathrm{W/ft}} = \boxed{26.45\,\mathrm{ft}}$$

(c) To calculate the heat dissipated by the cable, we can use the Stefan-Boltzmann equation $T = \sqrt[4]{\frac{P}{A\sigma}}$, with A corresponding to the cylindrical surface area of the 26.45 ft section of 1-foot diameter cable. Note that $\sigma$ is given in cm$^2$, so we will need to use consistent units.

$$A = \pi D L = \pi \times 30.48\,\mathrm{cm} \times 806.196\,\mathrm{cm} = 7.72 \times 10^4\,\mathrm{cm}^2$$

Therefore,

$$T = \sqrt[4]{\frac{P}{A\sigma}} = \sqrt[4]{\frac{1 \times 10^{10}\,\mathrm{W}}{7.72 \times 10^4\,\mathrm{cm}^2 \times 6 \times 10^{-12}\,\mathrm{W/K^4/cm^2}}} = \boxed{12{,}121\,\mathrm{K}}$$

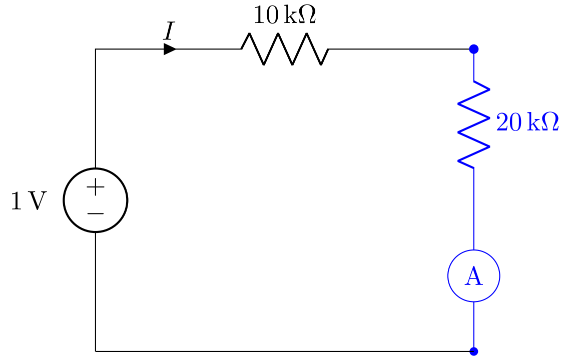
This is indeed a preposterous temperature, more than twice that at the surface of the Sun! The solution to this problem is that power should be transmitted along long distances at high voltage. This greatly reduces $I^2R$ losses. For example, a typical high voltage line voltage is 115 kV. At this voltage, the power loss per foot of cable is only 378 W per foot. Intuitively, we know that reducing current allows for lower power dissipation. We can deliver the same amount of power with a lower current by using a higher voltage.

## Exercise 1.7

A 20,000 $\Omega\,V^{-1}$ meter read, on its 1 V scale, puts a $20{,}000\,\Omega\,V^{-1} \cdot 1\,V = 20{,}000\,\Omega = 20\,k\Omega$ resistor in series with an ideal ammeter (ampere meter). Also, a voltage source with an internal resistance is equivalent to an ideal voltage source with its internal resistance in series.

(a) In the first question, we have the following circuit:

Figure 1.3: A voltage source with internal resistance and a 20,000 $\Omega\,V^{-1}$ meter read in its 1 V scale.

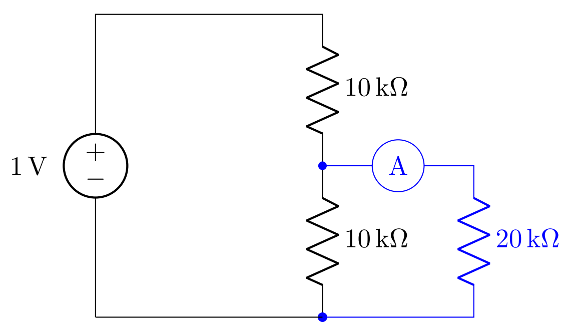



Then, we have that the current in the ideal ammeter and the voltage in the meter resistance are given by[2]

$$I = \frac{1\,V}{10\,k\Omega + 20\,k\Omega} = \boxed{0.0333\,mA} \quad \text{and} \quad V = 0.0333\,mA \times 20\,k\Omega = \boxed{0.666\,V}$$

(b) In the second question, we have the following circuit:

Figure 1.4: A $10\,k\Omega - 10\,k\Omega$ voltage divider and a 20,000 $\Omega\,V^{-1}$ meter read in its 1 V scale.




Now, we can to obtain the Thévenin equivalent circuit of circuit in Figure 1.4 with

$$R_{\mathrm{Th}} = \frac{10\,k\Omega \cdot 10\,k\Omega}{10\,k\Omega + 10\,k\Omega} = 5\,k\Omega$$

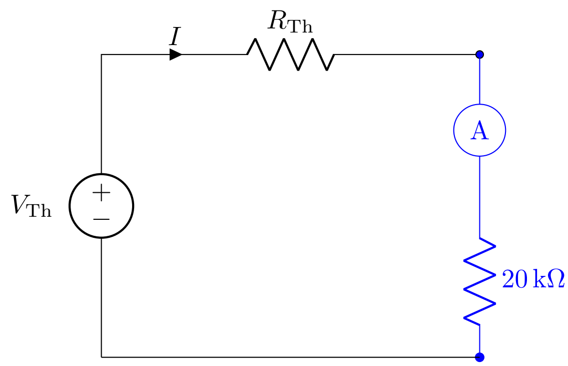
[2]When a meter only measures currents, it puts a resistance in series to measures the current through that resistance and internally converts that current into voltage to *measure voltages*.

and

$$V_{\mathrm{Th}} = 1\,\mathrm{V} \cdot \frac{10\,\mathrm{k\Omega}}{10\,\mathrm{k\Omega} + 10\,\mathrm{k\Omega}} = 0.5\,\mathrm{V}$$

Then, we have the following equivalent circuit:

Figure 1.5: Thévenin equivalent circuit of circuit in Figure 1.4.



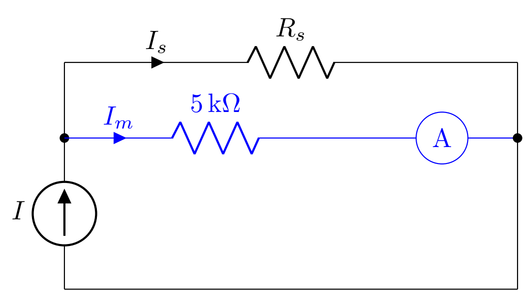

Finally, we have that the current in the ideal ammeter and the voltage in the meter resistance are given by

$$I = \frac{0.5\,\mathrm{V}}{5\,\mathrm{k\Omega} + 20\,\mathrm{k\Omega}} = \boxed{0.02\,\mathrm{mA}} \quad \text{and} \quad V = 0.02\,\mathrm{mA} \cdot 20\,\mathrm{k\Omega} = \boxed{0.4\,\mathrm{V}}$$

## Exercise 1.8

(a) In the first part, we have the following circuit:

Figure 1.6: 50 µA ammeter with 5 kΩ internal resistance (shown in blue) in parallel with shunt resistor.




We want to measure $I$ for 0-1 A, and the ideal ammeter measures up to $50\,\mu\mathrm{A}$. To find what shunt resistance $R_s$ allows us to do so, we set $I = 1\,\mathrm{A}$ and $I_m = 50\,\mu\mathrm{A}$. By KCL we know $I_s = 0.999950\,\mathrm{A}$. To determine $R_s$, we still need to find the voltage across it. We can find this voltage by doing

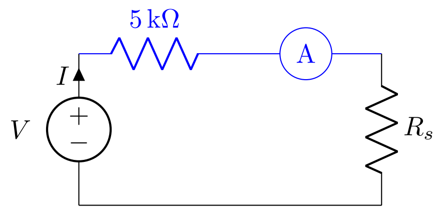
$$V = I_m R_m = 50\,\mu\mathrm{A} \cdot 5\,\mathrm{k\Omega} = 0.25\,\mathrm{V}$$

Then we simply do

$$R_s = \frac{V}{I_s} = \frac{0.25\,\mathrm{V}}{0.999950\,\mathrm{A}} = \boxed{0.25\,\Omega}$$

(b) In the second part, we have the following circuit:

Figure 1.7: $50\,\mu A$ ammeter with $5\,k\Omega$ internal resistance (shown in blue) with a series resistor.




We want to measure $V$ for 0-10 V, and the ideal ammeter measures up to $50\,\mu A$. To find the series resistance $R_s$, we set $V = 10\,V$ and $I = 50\,\mu A$. Then we solve

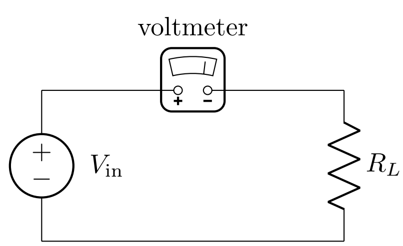
$$\frac{V}{I} = 5\,k\Omega + R_s$$

$$R_s = \frac{10\,V}{50\,\mu A} - 5\,k\Omega = \boxed{195\,k\Omega}$$

## Exercise 1.9

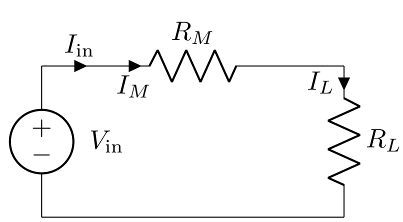
In order to measure resistance well above the range of your multimeter, you need to get creative. We will be using the multimeter in voltmeter mode. Lets start by connecting our DC voltage source, voltmeter, and the high-value resistor in series. (The reason for doing this will become clear later).

Figure 1.8: Connection of three components.




$V_{in}$ is our test voltage, and $R_L$ is our leakage resistance. We need to revise the model for our voltmeter.

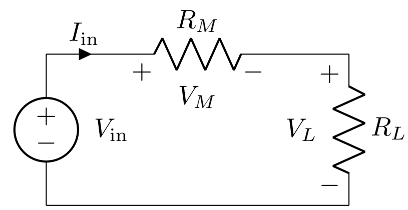
Figure 1.9: The voltmeter is now modeled as a resistor with value $R_M$.



The current flowing through our meter (modeled by the resistor $R_M$) is equal to the current flowing through the leakage resistor. This is also equal to the current supplied from our voltage source.

$$I_M = I_L = I_{\text{in}}$$

Figure 1.10: Voltage and current labels are added.




Notice: this test circuit is a **voltage divider**. When you use this technique, the voltmeter itself makes up half of the divider. The voltage across the leakage resistor cannot be measured directly, so we calculate it using Kirchhoff's Voltage Law by subtracting our voltmeter's reading from the voltage of our DC supply.

$$V_L = V_{\text{in}} - V_M$$

The current through the voltmeter's resistance is given by Ohm's Law.

$$I_M = \frac{V_M}{R_M}$$

The current through the leakage resistor is given by Ohm's Law.

$$I_L = \frac{V_L}{R_L}$$

We already determined that $I_M$ and $I_L$ are equal, so we can set the two previous expressions equal to each other.

$$I_M = I_L \Rightarrow \frac{V_M}{R_M} = \frac{V_L}{R_L}$$

We will rearrange the above equation to give an expression for $R_L$.

$$R_L = R_M \frac{V_L}{V_M}$$

Now we can substitute our first expression for $V_L$ into the previous equation to eliminate $V_M$ (the final unknown term).

$$R_L = R_M \frac{V_{\text{in}} - V_M}{V_M}$$

Rewriting the equation, the final result is

$$\boxed{R_L = R_M \left( \frac{V_{\text{in}}}{V_M} - 1 \right)}$$

To measure leakage current with a voltmeter, simply divide the meter's reading by the resistance of the meter. For example, if your $10\,\mathrm{M\Omega}$ voltmeter measures $0.023\,\mathrm{V}$, then $I_{leakage} = 23\,\mathrm{mV}/10\,\mathrm{M\Omega} = 2.3\,\mathrm{nA}$. The accuracy of such a measurement depends both on the accuracy of the voltage measurement, and the tolerance of the meter's resistance.

## Exercise 1.10

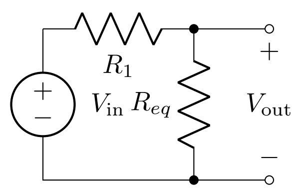
(a) With two equal-value resistors, the output voltage is half the input voltage.

$$V_{\text{out}} = \frac{1}{2}V_{\text{in}} = \frac{30\,\text{V}}{2} = \boxed{15\,\text{V}}$$

(b) To treat $R_2$ and $R_{\text{load}}$ as a single resistor, combine the two resistors which are in parallel to find that the combined (equivalent) resistance is $5\,\text{k}\Omega$. Now, we have a simple voltage divider with a $10\,\text{k}\Omega$ resistor in series with the $5\,\text{k}\Omega$ equivalent resistor. The output voltage is across this equivalent resistance. The output voltage is given by

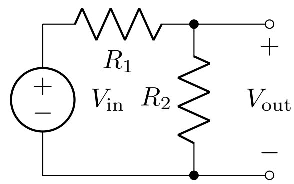
$$V_{\text{out}} = V_{\text{in}}\frac{5\,\text{k}\Omega}{10\,\text{k}\Omega + 5\,\text{k}\Omega} = \frac{30\,\text{V}}{3} = \boxed{10\,\text{V}}$$

Figure 1.11: Voltage divider with simplified equivalent resistance




(c) We can redraw the voltage divider circuit to make the "port" clearer.

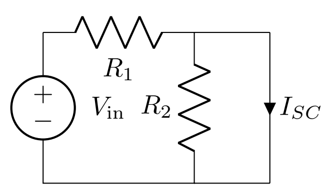
Figure 1.12: Voltage divider with port shown.




We can find $V_{\text{Th}}$ by leaving the ports open (open circuit) and measuring $V_{\text{out}}$, the voltage across $R_2$. This comes out to be half the input voltage when $R_1 = R_2$, so $V_{\text{out}} = 15\,\text{V}$. Thus $V_{\text{Th}} = \boxed{15\,\text{V}}$.

To find the Thévinen resistance, we need to find the short circuit current, $I_{SC}$. We short circuit the port and measure the current flowing through it.

Figure 1.13: Voltage divider with short circuit on the output.

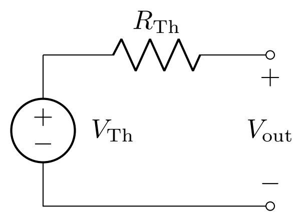


In this circuit, no current flows through $R_2$, flowing through the short instead. Thus we have $I_{SC} = \dfrac{V_{\text{in}}}{R_1}$. From this, we can find $R_{\text{Th}}$ from $R_{\text{Th}} = \dfrac{V_{\text{Th}}}{I_{SC}}$. This gives us

$$R_{\text{Th}} = \frac{V_{\text{Th}}}{I_{SC}} = \frac{V_{\text{Th}}}{V_{\text{in}}/R_1} = \frac{15\,\text{V}}{30\,\text{V}/10\,\text{k}\Omega} = \boxed{5\,\text{k}\Omega}$$

The Thévenin equivalent circuit takes the form shown below.

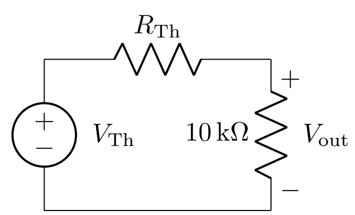
Figure 1.14: Thévenin equivalent circuit.




In terms of behavior at the ports, this circuit is equivalent to the circuit in Figure 1.11.

(d) We connect the $10\,\text{k}\Omega$ load to the port of the Thévenin equivalent circuit in Figure 1.14 to get the following circuit.

Figure 1.15: Thévenin equivalent circuit with $10\,\text{k}\Omega$ load.



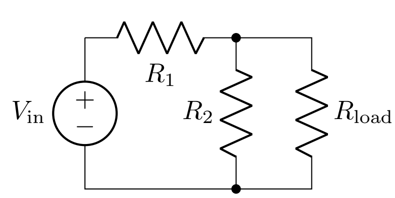

From here, we can find $V_{\text{out}}$, treating this circuit as a voltage divider.

$$V_{\text{out}} = \frac{10\,\text{k}\Omega}{R_{\text{Th}} + 10\,\text{k}\Omega} V_{\text{Th}} = \frac{10\,\text{k}\Omega}{5\,\text{k}\Omega + 10\,\text{k}\Omega} \cdot 15\,\text{V} = \boxed{10\,\text{V}}$$

This is the same answer we got in part (b).

(e) To find the power dissipated in each resistor, we return to the original three-resistor circuit.

Figure 1.16: Original voltage divider with $10\,\text{k}\Omega$ load attached.



From part (d), we know that the output voltage is 10V and that this is the voltage across the load resistor. Since $P = IV = \frac{V^2}{R}$, we find that the power through $R_{\text{load}}$ is

$$P_{\text{load}} = \frac{V^2}{R_{\text{load}}} = \frac{(10\,\text{V})^2}{10\,\text{k}\Omega} = \boxed{10\,\text{mW}}$$

Similarly, we know that the power across $R_2$ is the same since the voltage across $R_2$ is the same as the voltage across $R_{\text{load}}$. Thus we have

$$P_2 = \boxed{10\,\text{mW}}$$

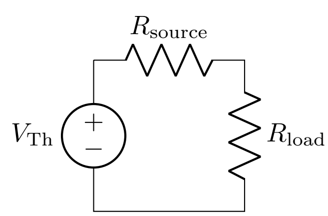
To find the power dissipated in $R_1$, we first have to find the voltage across it. From Kirchoff's loop rule, we know that the voltage around any closed loop in the circuit must be zero. We can choose the loop going through the voltage source, $R_1$, and $R_2$. The voltage supplied by the source is 30V. The voltage dropped across $R_2$ is 10V as discussed before. Thus the voltage dropped across $R_1$ must be $30\,\text{V} - 10\,\text{V} = 20\,\text{V}$. Now we know the voltage across and the resistance of $R_1$. We use the same formula as before to find the power dissipated.

$$P_1 = \frac{V^2}{R_1} = \frac{(20\,\text{V})^2}{10\,\text{k}\Omega} = \boxed{40\,\text{mW}}$$

## Exercise 1.11

Consider the following Thévenin circuit where $R_{\text{source}}$ is just another name for the Thévenin resistance, $R_{\text{Th}}$.

Figure 1.17: Standard Thévenin circuit with attached load.




We will first calculate the power dissipated in the load and then maximize it with calculus. We can find the power through a resistor using current and resistence since $P = IV = I(IR) = I^2R$. To find the total current flowing through the resistors, we find the equivalent resistance which is $R_{\text{source}} + R_{\text{load}}$. Thus the total current flowing is $I = \dfrac{V_{\text{Th}}}{R_{\text{source}} + R_{\text{load}}}$. The power dissipated in $R_{\text{load}}$ is thus

$$P_{\text{load}} = I^2 R_{\text{load}} = \frac{V_{\text{Th}}^2 R_{\text{load}}}{(R_{\text{source}} + R_{\text{load}})^2}$$

To maximize this function, we take the derivative and set it equal to 0.

$$\begin{aligned}\frac{dP_{\text{load}}}{dR_{\text{load}}} &= V_{\text{Th}} \frac{(R_{\text{source}} + R_{\text{load}})^2 - 2R_{\text{load}}(R_{\text{source}} + R_{\text{load}})}{(R_{\text{source}} + R_{\text{load}})^4} = 0 \\ &\implies R_{\text{source}} + R_{\text{load}} = 2R_{\text{load}} \\ &\implies R_{\text{source}} = R_{\text{load}}\end{aligned}$$

# Exercise 1.12

(a) Voltage ratio: $\frac{V_2}{V_1} = 10^{\text{dB}/20} = 10^{3/20} = \boxed{1.413}$

Power ratio: $\frac{P_2}{P_1} = 10^{\text{dB}/10} = 10^{3/10} = \boxed{1.995}$

(b) Voltage ratio: $\frac{V_2}{V_1} = 10^{\text{dB}/20} = 10^{6/20} = \boxed{1.995}$

Power ratio: $\frac{P_2}{P_1} = 10^{\text{dB}/10} = 10^{6/10} = \boxed{3.981}$

(c) Voltage ratio: $\frac{V_2}{V_1} = 10^{\text{dB}/20} = 10^{10/20} = \boxed{3.162}$

Power ratio: $\frac{P_2}{P_1} = 10^{\text{dB}/10} = 10^{10/10} = \boxed{10}$

(d) Voltage ratio: $\frac{V_2}{V_1} = 10^{\text{dB}/20} = 10^{20/20} = \boxed{10}$

Power ratio: $\frac{P_2}{P_1} = 10^{\text{dB}/10} = 10^{20/10} = \boxed{100}$

# Exercise 1.13

There are two important facts to notice from Exericse 1.12:

1. An increase of 3 dB corresponds to doubling the power
2. An increase of 10 dB corresponds to 10 times the power.

Using these two facts, we can fill in the table. Start from 10 dB. Fill in 7 dB, 4 dB, and 1 dB using fact 1. Then fill in 11 dB using fact 2. Then fill in 8 dB, 5 dB, and 2 dB using fact 1 and approximating 3.125 as $\pi$.

| dB | ratio($P/P_0$) |
|---|---|
| 0 | 1 |
| 1 | $\boxed{1.25}$ |
| 2 | $\boxed{\pi/2}$ |
| 3 | 2 |
| 4 | $\boxed{2.5}$ |
| 5 | $\boxed{3.125 \approx \pi}$ |
| 6 | 4 |
| 7 | $\boxed{5}$ |
| 8 | $\boxed{6.25}$ |
| 9 | 8 |
| 10 | 10 |
| 11 | $\boxed{12.5}$ |

## Exercise 1.14

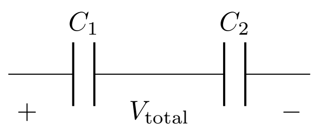
Recall the relationship between $I$, $V$, and $C$: $I = C\frac{dV}{dt}$. Now, we perform the integration:

$$\begin{aligned}
\int dU &= \int_{t_0}^{t_1} VI dt \\
U &= \int_{t_0}^{t_1} CV\frac{dV}{dt}dt \\
&= C\int_0^{V_f} V dV \\
U &= \frac{1}{2}CV_f^2
\end{aligned}$$

## Exercise 1.15

Consider the following two capacitors in series.

Figure 1.18: Two capacitors in series.




To prove the capacitance formula, we need to express the total capacitance of both of these capacitors in terms of the individual capacitances. From the definition of capacitance, we have

$$C_{\text{total}} = \frac{Q_{\text{total}}}{V_{\text{total}}}$$

Notice that $V_{\text{total}}$ is the sum of the voltages across $C_1$ and $C_2$. We can get each of these voltages using the definition of capacitance.

$$V_{\text{total}} = V_1 + V_2 = \frac{Q_1}{C_1} + \frac{Q_2}{C_2}$$

The key observation now is that because the right plate of $C_1$ is connected to the left plate of $C_2$, the charge stored on both plates must be of equal magnitude.[3]Therefore, we have $Q_1 = Q_2$. Let us call this charge stored $Q$ (i.e. $Q = Q_1 = Q_2$). Now, we know that the total charge stored is also $Q$.[4]Therefore, we know that $Q_{\text{total}} = Q$. Now, we have

$$C_{\text{total}} = \frac{Q_{\text{total}}}{V_{\text{total}}} = \frac{Q}{Q_1/C_1 + Q_2/C_2} = \frac{Q}{Q/C_1 + Q/C_2} = \frac{1}{1/C_1 + 1/C_2}$$

[4]If this were not true, then there would be a net charge on these two plates and the wire between them. Because we assume that the capacitors started out with no net charge and there is no way for charge to leave the middle wire or the two plates it connects, this is impossible.

[4]If you are having trouble seeing this, suppose we apply a positive voltage to the left plate of $C_1$ relative to the right plate of $C_2$. Suppose this causes the left plate of $C_1$ to charge to some charge $q$. We now must have a charge of $-q$ on the right plate of $C_1$ because $q$ units of charge are now pushed onto the left plate of $C_2$. Now the left of $C_2$ has $q$ units of charge which causes a corresponding $-q$ charge on the right side of $C_2$. Thus the overall total charge separated across these two capacitors is $q$.

## Exercise 1.16

Equation 1.21 gives us the relationship between the time and the voltage ($V_{\text{out}}$) across the capacitor while charging. To find the rise time, subtract the time it takes to reach 10% of the final value from the time it takes to reach 90% of the final value.

$$\begin{aligned} V_{\text{out}} &= 0.1V_f = V_f(1 - e^{-t_1/RC}) \\ 0.1 &= 1 - e^{-t_1/RC} \\ t_1 &= -RC\ln(0.9) \end{aligned}$$

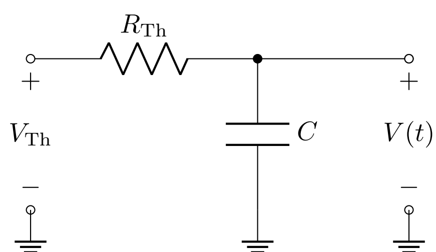
Similarly, we find that $t_2 = -RC\ln(0.1)$. Subtracting these two gives us

$$t_2 - t_1 = -RC(\ln(0.1) - \ln(0.9)) = 2.2RC$$

## Exercise 1.17

The voltage divider on the left side of the circuit can be replaced with the Thévenin equivalent circuit found Exercise 1.10 (c). Recall that $V_{\text{Th}} = \frac{1}{2}V_{\text{in}}$ and $R_{\text{Th}} = 5\,\text{k}\Omega$. This gives us the following circuit.

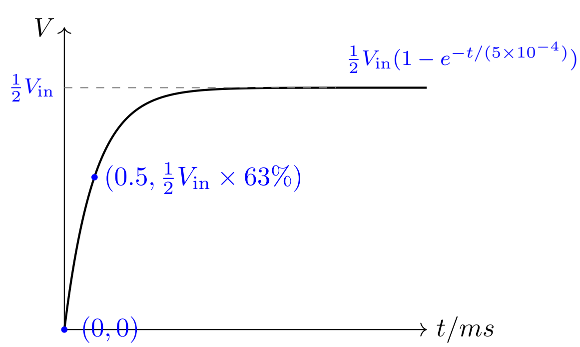
Figure 1.19: Thévenin equivalent circuit to Figure 1.36 from the textbook.




Now we have a simple RC circuit which we can apply Equation 1.21 to. The voltage across the capacitor is given by

$$V(t) = V_{\text{final}}(1 - e^{-t/RC}) = V_{\text{Th}}(1 - e^{-t/R_{\text{Th}}C} = \boxed{\frac{1}{2}V_{\text{in}}(1 - e^{-t/5\times10^{-4}})}$$

Figure 1.20: V(t) sketch.



## Exercise 1.18

From the capacitor equation in the previous paragraph, we have

$$V(t) = (I/C)t = (1\,\text{mA}/1\,\mu\text{F}) \times t = 10\,\text{V}$$

This gives us

$$\boxed{t = 0.01\,\text{s}}$$

## Exercise 1.19

Suppose a current $I$ is flowing through a loop of wire with cross-sectional area $A$. This induces a magnetic field $B$, and the flux $\Phi$ through the loop is

$$\Phi = BA$$

Now suppose the same current $I$ flows through a wire coiled into $n$ loops, each with the same cross-sectional area $A$. This induces a magnetic field of $n$ times the strength, $B_n = nB$. Since each loop has area $A$, the total cross-sectional area of the coil can be considered $A_n = nA$. Then the magnetic flux through the coil is

$$\Phi_n = B_n A_n = n^2 BA = n^2 \Phi$$

Since inductance is defined as flux through a coil divided by current through the flux, we can see that $\Phi_n = n^2\Phi$ implies $L \propto n^2$.

## Exercise 1.20

We can use the formula for the full-wave rectifier ripple voltage to find the capacitance.

$$\frac{I_{\text{load}}}{2fC} = \Delta V \leq 0.1\text{V}_{\text{p-p}}$$

The maximum load current is 10mA and assuming a standard wall outlet frequency of 60 Hz, we have

$$C \geq \frac{10\,\text{mA}}{2 \times 60\,\text{Hz} \times 0.1\,\text{V}} = \boxed{833\,\mu\text{F}}$$

Now we need to find the AC input voltage. The peak voltage after rectification must be 10 V (per the requirements). Since each phase of the AC signal must pass through 2 diode drops, we have to add this to find out what our AC peak-to-peak voltage must be. Thus we have

$$V_{\text{in,p-p}} = 10\,\text{V} + 2(0.6\,\text{V}) = \boxed{11.2\,\text{V}}$$

## Exercise 1.21

In order to calculate the minimum fuse rating for a time-varying current signal, one must calculate the RMS current of the signal - *not* the average current. This is because most fuses are designed to blow at a certain average power level, and average power is related to the average of the *square* of current.

Square waves are defined by two amplitudes. When one of those amplitudes is zero, the RMS value is given by the following equation:

$$I_{\text{RMS}} = \sqrt{\frac{I^2 + 0}{2}} = \sqrt{\frac{I^2}{2}} = \frac{I}{\sqrt{2}}$$

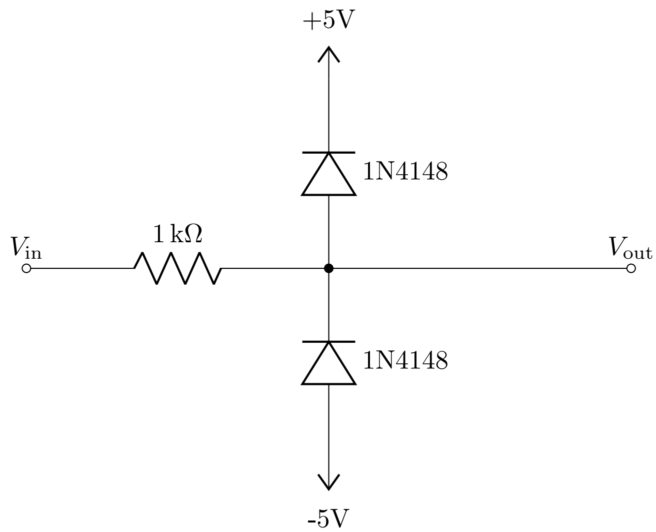
So in the case of a 0 to 2.0 A square wave with 50% duty cycle, the theoretical minimum current a fuse should be rated for is:

$$\frac{I}{\sqrt{2}} = \frac{2}{\sqrt{2}} = \boxed{\sqrt{2}A}$$

In this case, sizing a fuse for the *average* current (1 A) would too small by a factor of $\sqrt{2}$!

# Exercise 1.22

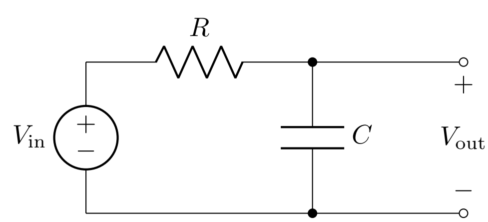
Figure 1.21: A symmetric 5.6 V clamping circuit.




# Exercise 1.23

For both low-pass and high-pass filters of the first-order, the **input** impedance is calculated by the series combination of impedances of both circuit elements. The **output** impedance is calculated as the parallel combination of the impedances of the two circuit elements.

Figure 1.22: Low-Pass Filter Driven by a Voltage Source.



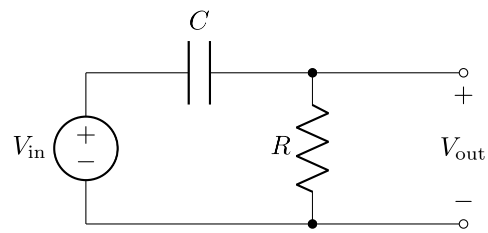

The minimum input impedance of a low-pass filter occurs at high frequency when the capacitor looks like a short circuit. This is true because this minimizes the impedance of the series-combination of impedances.

$$\boxed{Z_{\text{in,min}} = R + 0 = R}$$

The maximum output impedance a low-pass filter occurs at low frequency when the capacitor looks like an open circuit. This is true because this maximizes the impedance of the parallel-combination of impedances.

$$\boxed{Z_{\text{out,max}} = R \parallel \infty = R}$$

Figure 1.23: High-Pass Filter Driven by a Voltage Source.

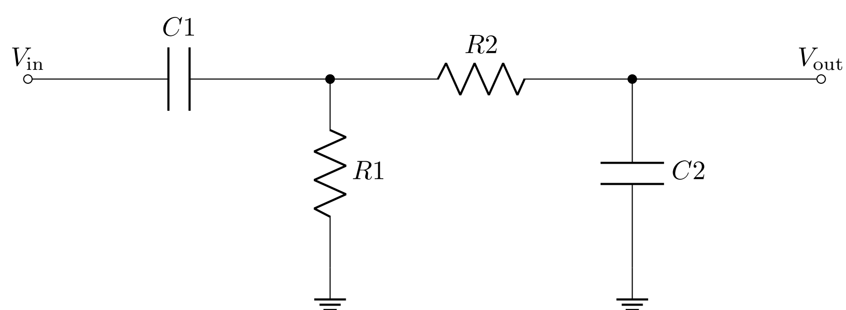



The reasoning for the high-pass filter is the same as for the low-pass filter. The circuit elements are swapped in their position, but the analysis is the same because: minimizing the input impedance is still a function of minimizing the series combination impedance; maximizing the output impedance is still a function of maximizing the parallel combination impedance.

## Exercise 1.24

As the question indicated, the bandpass filter is made of a highpass filter and lowpass filter as shown below.

Figure 1.24: Bandpass filter




For highpass and lowpass filters, we have

$$f_{3\text{dB}} = \frac{1}{2\pi * RC}$$

Given breakpoints, we can determine the resistors and capacitors values to meet the design requirements.

(a) Given $f_1 = 100\,\text{Hz}$ from the question:

$$R_1 * C_1 = \frac{1}{2\pi * 100\,\text{Hz}} = 1.6\,\text{ms}$$

Because the signal source output impedance is $100\,\Omega$, we select a value 10 times higher: $R_1 = 1\,\mathrm{k\Omega}$ then:

$$C_1 = \frac{1.6\,\mathrm{ms}}{1\,\mathrm{k\Omega}} = \boxed{1.6\,\mathrm{\mu F}}$$

(b) Given $f_2 = 10\,\mathrm{kHz}$ from the question:

$$R_2 * C_2 = \frac{1}{2\pi * 10\,\mathrm{kHz}} = 16\,\mathrm{\mu s}$$

Because the output impedance of the high-pass filter was approximately $1\,\mathrm{k\Omega}$, we select a value 10 times greater: $R_2 = 10\,\mathrm{k\Omega}$ then:

$$C_2 = \frac{16\,\mathrm{\mu s}}{10\,\mathrm{k\Omega}} = \boxed{1.6\,\mathrm{nF}}$$

# Exercise 1.25

(a) The impedance of 2 parallel capacitors is equal to the impedance of a single capacitor $C$ of value $C_1 + C_2$:

$$\mathbf{Z}_{\text{parallel}} = \frac{1}{\frac{1}{\mathbf{Z_1}} + \frac{1}{\mathbf{Z_2}}} = \frac{1}{j\omega C_1 + j\omega C_2} = \boxed{\frac{1}{j\omega(C_1 + C_2)}}$$

(b) The impedance of 2 series capacitors is equal to the impedance of a single capacitor $C$ of value $\frac{C_1C_2}{C_1+C_2}$:

$$\begin{aligned}
\mathbf{Z}_{\text{series}} &= \mathbf{Z_1} + \mathbf{Z_2} \\
&= \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} \\
&= \frac{1}{j\omega}\left(\frac{1}{C_1} + \frac{1}{C_2}\right) \\
&= \frac{1}{j\omega}\left(\frac{C_2}{C_1C_2} + \frac{C_1}{C_2C_1}\right) \\
&= \frac{1}{j\omega}\left(\frac{C_1 + C_2}{C_1C_2}\right) \\
&= \frac{1}{j\omega}\frac{1}{\left(\frac{C_1C_2}{C_1+C_2}\right)} \\
&= \boxed{\frac{1}{j\omega\left(\frac{C_1C_2}{C_1+C_2}\right)}}
\end{aligned}$$

# Exercise 1.26

$$Ae^{j\theta} = Be^{j\phi}Ce^{j\alpha} = BCe^{j(\phi+\alpha)}$$

Therefore, because $A$, $B$, and $C$ are all real numbers, $\theta$ must be equal to $(\phi + \alpha)$, so the exponentials on either side of the equation cancel.

$$Ae^{j\theta} = BCe^{j(\phi+\alpha)}$$

$$Ae^{j\theta} = BCe^{j\theta}$$

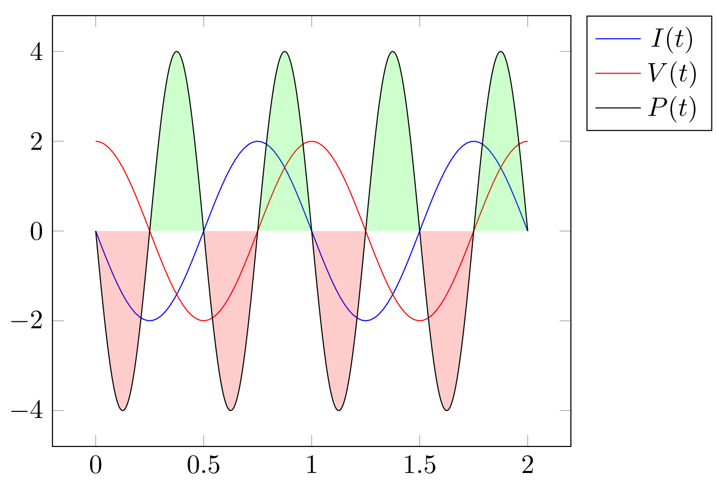
$$\boxed{A = BC}$$

## Exercise 1.27

We can solve this problem from two aproaches: analitically, or by inspecting the power waveform over a full cycle. First analytically:

$$\begin{aligned}
V(t) &= V_0 \cos(2\pi f t) && \text{Define the voltage} \\
I(t) &= I_0 \cos\left(2\pi f t + \tfrac{\pi}{2}\right) && \text{and current waveforms} \\
\\
P(t) &= V(t) \cdot I(t) \\
&= V_0 I_0 \cos(2\pi f t) \cos\left(2\pi f t + \tfrac{\pi}{2}\right) && \text{Using cosine multiplication rule} \\
&= V_0 I_0 \frac{\cos\left(4\pi f t + \frac{\pi}{2}\right) + \cancelto{0}{\cos\left(\frac{\pi}{2}\right)}}{2} && \text{we express the power waveform} \\
& && \text{as a sum of two cosines} \\
\\
P_{\text{av}} &= \frac{1}{T}\int_0^T V_0 I_0 \frac{\cos\left(4\pi f t + \frac{\pi}{2}\right)}{2} \mathrm{d}t && \text{From this point we take the integral} \\
&= \frac{V_0 I_0}{2T}\left[\frac{\sin\left(4\pi f t + \frac{\pi}{2}\right)}{4\pi f}\right]_{t=0}^{t=T} && \text{and evaluate over one cycle} \\
&= \frac{V_0 I_0}{8\pi} \underbrace{\left(\sin\left(4\pi + \tfrac{\pi}{2}\right) - \sin\left(\tfrac{\pi}{2}\right)\right)}_{1-1=0} = \boxed{0}
\end{aligned}$$

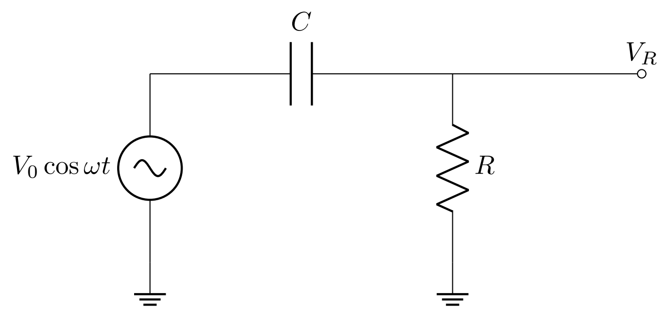
As an alternative method we can avoid the integration part by simply observing the power waveform over one full cycle considering $f = 1, I_0 = V_0 = 2$




From the plot it is clear that the red and green areas are equal and opposite and thus when integrating over a integer number of cycles the average power will be zero.

# Exercise 1.28

Figure 1.25: RC Circuit with AC Voltage Source




From discussions before this question, we know that

$$P = Re(VI^*) = \frac{V_0^2 R}{R^2 + (\frac{1}{\omega^2 C^2})} = \frac{V_0^2}{R} * \frac{(\omega RC)^2}{1 + (\omega RC)^2}$$

Since R and C are connected in series, we have

$$\frac{V_R}{V_0} = \frac{R}{R + \frac{1}{j\omega C}}$$

Thus, we can calculate the power consumed by the resistor in the following steps.

$$V_R = V_0 * \frac{j\omega RC}{1 + j\omega RC}$$

$$\frac{V_R^2}{R} = \frac{V_0^2}{R} * \frac{(\omega RC)^2}{1 + (\omega RC)^2}$$

We can see that it is equal to the real power delivered to the circuit. In another word, all the real power delivered to this circuit is consumed in the resistor.

# Exercise 1.29

(a) RLC series circuit

Since the resistor, inductor, and capacitor are in series, we can calculate the impedance of the circuit by adding individual impedance together.

$$Z = R + j\omega L - j\frac{1}{\omega C}$$

Given $C = \frac{1}{\omega^2 L}$,

$$Z = R + j\omega L - j\omega L = R$$

Thus, this reactive circuit can be treated as a resistive circuit when calculating the power factor, which is 1.

(b) RLC parallel circuit

Since all the components are in parallel, the invert of total impedance is the sum of inverts of all components' impedance

$$\frac{1}{Z} = \frac{1}{R} + \frac{1}{j\omega L} + j\omega C$$

Given $C = \frac{1}{\omega^2 L}$,

$$\frac{1}{Z} = \frac{1}{R} + \frac{1}{j\omega L} - \frac{1}{j\omega L} = \frac{1}{R}$$

Similarly, this show that this circuit can also be treated as a resistive circuit whoes power factor is 1.

## Exercise 1.30

$V_{\text{out}}$ is simply the voltage at the output of an impedance voltage divider. We know that $Z_R = R$ and $Z_C = \frac{1}{j\omega C}$. Thus we have

$$V_{\text{out}} = \frac{Z_C}{Z_R + Z_C} V_{\text{in}} = \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}} V_{\text{in}} = \frac{1}{1 + j\omega RC} V_{\text{in}}$$

The magnitude of this expression can be found by multiplying by the complex conjugate and taking the square root.

$$\sqrt{V_{\text{out}} V_{\text{out}}^*} = \frac{1}{\sqrt{1 + \omega^2 R^2 C^2}} V_{\text{in}}$$

## Exercise 1.31

From the frequency response of lowpass filter plotted on logarithmic axes, we know

$$\phi = -\arctan(\frac{f}{f_c})$$

Thus, when $f = 0.1 f_{3\text{dB}}$,

$$\phi = -\arctan(0.1) \approx -5.71^\circ \approx -6^\circ$$

Similarly, when $f = 10 f_{3\text{dB}}$,

$$\phi = -\arctan(10) \approx -84.29^\circ$$

The phase shift can also be expressed as $-(-90 - (-84.29)) \approx 5.71^\circ \approx 6^\circ$

In summary, for single-section $RC$ filters, the phase shift is $\approx 6^\circ$ from its asymptotic value at $0.1 f_{3\text{dB}}$ and $10 f_{3\text{dB}}$.

## Exercise 1.32

Given that the current is the same everywhere in series circuits, the axes also shows the relationships among voltages.

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{R}{hypotenuse}$$

By Pythagorean Theorem,

$$\frac{R}{hypotenuse} = \frac{R}{\sqrt{R^2 + (-j/\omega C)^2}} = \frac{R}{\sqrt{R^2 + \frac{1}{\omega^2 C^2}}}$$

Thus, $V_{\text{out}} = V_{\text{in}} * \frac{R}{\sqrt{R^2 + \frac{1}{\omega^2 C^2}}}$

## Exercise 1.33

For the lowpass filter, $V_{\text{out}}$ and $V_{\text{in}}$ have the following relationship.

$$V_{\text{out}} = V_{\text{in}} * \frac{1}{\sqrt{1+\omega^2 R^2 C^2}}$$

Given $V_{\text{out}} = \frac{1}{2}V_{\text{in}}$,

$$\frac{1}{\sqrt{1+\omega^2 R^2 C^2}} = \frac{1}{2}$$

Thus, solving for $\omega$

$$\frac{1}{1+\omega^2 R^2 C^2} = \frac{1}{4}$$
$$1+\omega^2 R^2 C^2 = 4$$
$$\omega^2 R^2 C^2 = 3$$
$$\omega = \frac{\sqrt{3}}{RC}$$

Since $f = \frac{\omega}{2\pi}$,

$$f = \frac{\sqrt{3}}{2\pi RC}$$

From previous calculation, we have $C = \frac{\sqrt{3}}{RC}$ From the phasor diagram for lowpass filter at $3dB$ point, we know that

$$\aleph = \arctan(\frac{\frac{-j}{\omega C}}{R}) = \arctan(-\frac{1}{\sqrt{3}}) = -30^\circ$$

Thus, the phase shift is

$$\phi = -90^\circ - (-30^\circ) = -60^\circ$$

## Exercise 1.34

From the phasor diagram, we can see that

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{C}{hypotenuse} = \frac{C}{\sqrt{R^2+C^2}}$$

pluging in $C = \frac{-j}{\omega C}$

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{\frac{-j}{\omega C}}{\sqrt{R^2+\frac{1}{\omega^2 C^2}}} = \frac{-j}{\omega C} * \frac{\omega C}{\sqrt{R^2\omega^2C^2+1}} = \frac{-j}{\sqrt{R^2\omega^2C^2+1}}$$

## Exercise 1.35

Resistor, inductor, and capacitor in series forms a voltage devider, so

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{Z_{\text{LC}}}{R+Z_{\text{LC}}}$$

Since the inductor and capacitor are in series and $\omega_0 = \frac{1}{\sqrt{LC}}$, which was derived from $f_0 = \frac{1}{2\pi\sqrt{LC}}$. We can write $Z_{\text{LC}}$ as following,

$$Z_{\text{LC}} = Z_{\text{L}} + Z_{\text{C}} = j\omega L + \frac{-j}{\omega C} = j(\omega L - \frac{1}{\omega C}) = jL(\frac{\omega^2-\omega_0^2}{\omega})$$

We can describe the response in the following conditions:

(a) When $f = f_0$, $\omega = \omega_0$ and $Z_{\text{LC}} = 0$. Thus, $\frac{V_{\text{out}}}{V_{\text{in}}} = 0$.

(b) When $f < f_0$, $\omega < \omega_0$ and $Z_{\text{C}} > Z_{\text{L}}$, which makes the circuit more capcitive. Thus, the circuit has a similar response as capacitors.

(c) When $f > f_0$, $\omega > \omega_0$ and $Z_{\text{L}} > Z_{\text{C}}$, which means the inductor has more impact on the general response of the whole circuit. Thus, the circuit responses more like inductors.

Thus, we see the response plot captured in Figure 1.109 from the textbook.

# Exercise 1.36

We can see from textbook Figure 1.122 that two SPDT switches can control the lamp independently. We need to explore wirings that allow DPDT switches to switch from two states. The following wire shows how to turn DPDT switches to work as described.

Figure 1.26: Wiring a DPDT switch to switch from two states

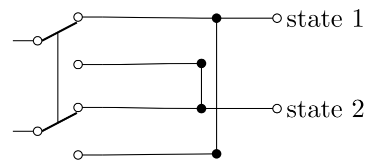
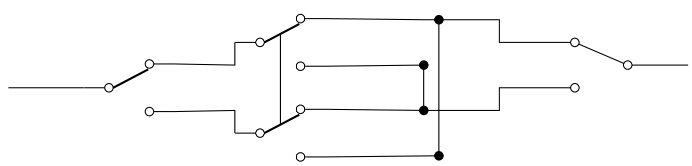


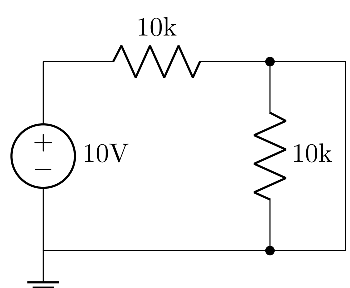

Figure 1.27: Generalization of "three-way" Switch Wiring with Two SPDT Switches And $N-2$ DPDT Switches



# Exercise 1.37

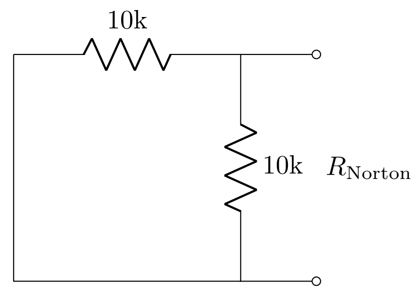
Recall that $I_{\text{Norton}} = I_{\text{short circuit the load}}$, so we can transform the circuit as shown below.

Figure 1.28: Circuit to find $I_{\text{Norton}}$



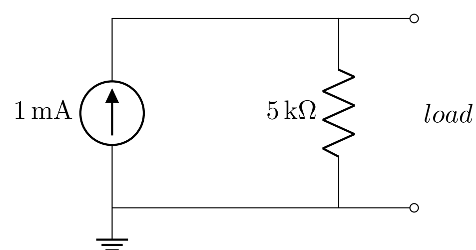
Then, $I_{\text{Norton}} = \frac{10\,\text{V}}{10\,\text{k}\Omega} = 1\,\text{mA}$ To find $R_{\text{Norton}}$, it's very similar to how we find $R$ in superposition where we remove all power sources. Then, the circuit is transformed as shown below.

Figure 1.29: Circuit to find $R_{\text{Norton}}$



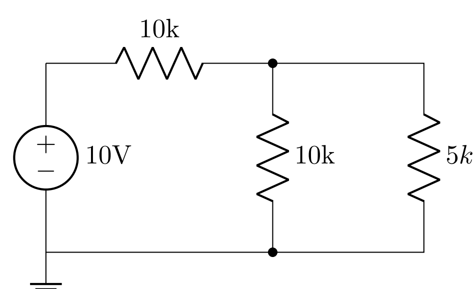

Based on the circuit, $R_{\text{Norton}} = \frac{1}{\frac{1}{10}+\frac{1}{10}} = 5\,\text{k}\Omega$ Thus, the Norton equivalent circuit is shown below.

Figure 1.30: Circuit to find $R_{\text{Norton}}$




When the $R_{\text{load}} = 5\,\text{k}\Omega$, $V_{\text{out}} = \frac{5\,\text{k}\Omega}{2} * 1\,\text{mA} = 2.5\,\text{V}$ And, the original circuit is as shown below.

Figure 1.31: Original Circuit with a $5\,\text{k}\Omega$ load




Thus, $V_{\text{out}} = \frac{V_{\text{in}} * \frac{1}{\frac{1}{10}+\frac{1}{5}}}{10+\frac{1}{\frac{1}{10}+\frac{1}{5}}} = 2.5\,\text{V}$

Finally, we showed that the Norton equivalent gives the same output voltage as the actual circuit when loaded by a $5k$ resistor.

## Exercise 1.38

Based on the circuit shown in this excercise, $V_{\text{Th}} = V_{\text{open}} = 0.5\,\text{mA} * 10\,\text{k}\Omega = 5\,\text{V}$

$I_{\text{short}} = 0.5\,\text{mA}$, so $R_{\text{Th}} = \frac{5\,\text{V}}{0.5\,\text{mA}} = 10\,\text{k}\Omega$

Similarly, we can find the Thévenin equivalent for the previous excercise.

$$V_{\text{Th}} = \frac{10\,\text{k}\Omega}{10+10} * V_{\text{in}} = 5\,\text{V}$$

$$I_{\text{short}} = \frac{10\,\text{V}}{10\,\text{k}\Omega} = 1\,\text{mA}$$

$$R_{\text{Th}} = \frac{5\,\text{V}}{1\,\text{mA}} = 5\,\text{k}\Omega$$

Since the $R_{\text{Th}}$ is different from the previous result, we can see that these Thévenin circuits are not the same.

## Exercise 1.39

Based on the filter behaviors, the "rumble filter" is essentially a high-pass filter.

Given $f_{3\text{dB}} = 10\,\text{Hz}$ from the question:

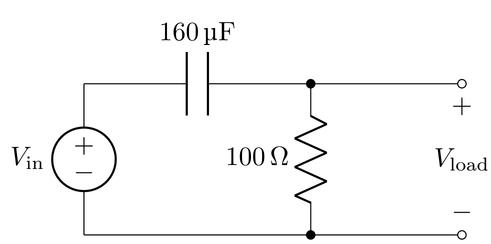
$$R * C = \frac{1}{2\pi * 10\,\text{Hz}} \approx 16\,\text{ms}$$

Since the load ($10\,\text{k}\Omega$ minimum) is in parallel with the reistor in the RC high-pass filer, we should select a relatively small resistor for the filter design so that the load doesn't affect the filter's performance significantly. We select a resistor: $R = \frac{10\,\text{k}\Omega}{100} = 100\,\Omega$ then:

$$C = \frac{16\,\text{ms}}{100\,\Omega} = 160\,\mu\text{F}$$

The filter design is shown below.

Figure 1.32: Rumble Filter




## Exercise 1.40

The "scratch filter" for audio signals is essentially a low-pass filter that filter out high-frequency sounds, such as scratches.

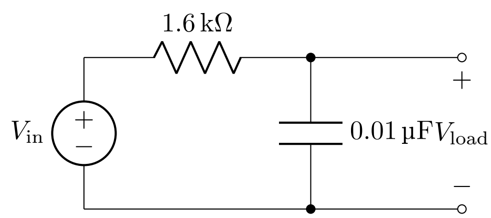
Given $f_{3\text{dB}} = 10\,\text{kHz}$ from the question:

$$R * C = \frac{1}{2\pi * 10\,\text{kHz}} = 0.016\,\text{ms}$$

Similar to the high-pass filter design in the previous question, we need to pick a low impedance capacitor so that the load doesn't affect the filter's performance significantly. We select a capacitor: $C = 0.01\,\mu\text{F}$ then:

$$R = \frac{1}{2\pi * 10000 * 0.01 * 0.000001} \approx 1.6\,\text{k}\Omega$$

Figure 1.33: Scratch Filter




## Exercise 1.41

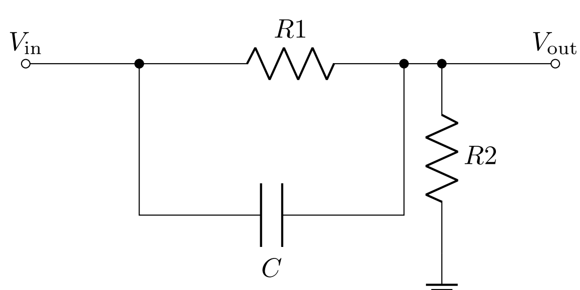
Since we need to design a filter using resitors and capcitors to produce the results as plotted, we need to think of RC circuits that we discussed before as building blocks for this problem.

Based on the plot, when $\omega < \omega_0$, the filter acts like a voltage divider and $\frac{V_{\text{out}}}{V_{\text{in}}} = 0.5$

When $\omega > \omega_0$, the filer looks like a high-pass filter.

We can combine voltage divider circuit and high-pass filter as shown below.

Figure 1.34: High-emphasis filter



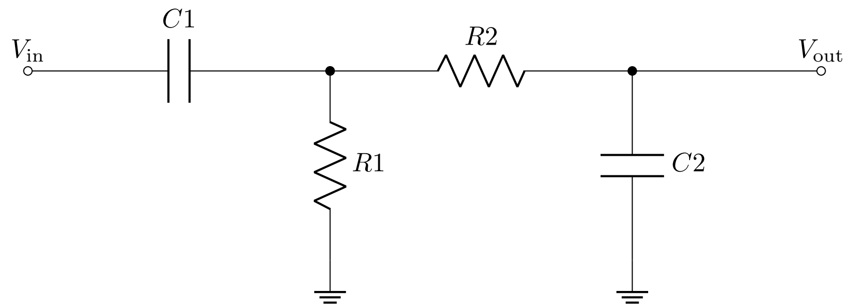

when $\omega < \omega_0$, the capacitor acts as if it's open, and the circuit is a voltage devider.

Given that $\frac{V_{\text{out}}}{V_{\text{in}}} = 0.5$, $R_1 = R_2 = R$

When $\omega > \omega_0$, the high frequency signals can pass the capacitor, but low frequency signals are blocked. We can find the capacitor value by treating the circuit as a high-pass filter. $f_{\text{3dB}} = \frac{1}{2\pi * RC}$ and $\omega = 2\pi * f_{\text{3dB}}$ so $C = \frac{R}{\omega_0}$

## Exercise 1.42

Figure 1.35: Bandpass filter




The bandpass filter is made of a high-pass filter and a low-pass filter. Thus, given $f_1$ and $f_2$, we have

$$f_1 = \frac{1}{2\pi * R_1 * C_1}$$

$$f_2 = \frac{1}{2\pi * R_2 * C_2}$$

As discussed in the session "Driving and loading RC filters" in the book, the assumptions are small input impedance compared to the load. We can set $R_1 = \frac{1}{10} * R_2$, and then

$$C_2 = \frac{1}{2\pi * f_2 R_2}$$

$$C_1 = \frac{1}{f_1 * 2\pi R_1} = \frac{1}{f_1 * 2\pi * 0.1 R_2} = \frac{5}{\pi R_2 f_1}$$

## Exercise 1.43

The circuit is the diode limiter discussed before (Figure 1.78 in the textbook), and the output is the same as the plots A and B in $Figure 1.79$. We need to find the characters of the output signal. Given that $f = 60\,\text{Hz}$

$$T = \frac{1}{f} = \frac{1}{60} \approx 17\,\text{ms}$$

$$\omega = 2\pi f = 120\pi$$

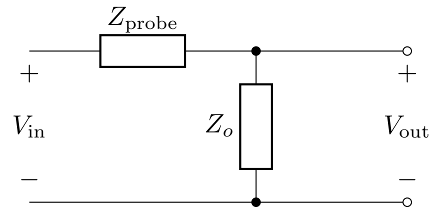
## Exercise 1.44

The equivalent capacitance of the oscilloscope and cable is

$$C_o = 100\,\text{pF} + 20\,\text{pF} = 120\,\text{pF}$$

The equivalent input impedance of the oscilloscope and the total capacitance is: $Z_o = \left(R_o \parallel \frac{1}{j\omega C_o}\right)$ where $R_o$ is the input resistance of the scope ($1\,\text{M}\Omega$). In order to reduce the voltage by a factor of 10, let us create a voltage divider between the probe tip and the equivalent scope-and-cable input impedance.

Figure 1.36: Basic Voltage Divider




In order to reduce the voltage by a factor of ten, our circuit must satisfy

$$V_{\text{out}} = \frac{V_{\text{in}}}{10}$$

We know that the output of a voltage divider is given by

$$V_{\text{out}} = V_{\text{in}} \frac{Z_{\text{out}}}{Z_{\text{out}} + Z_{\text{in}}}$$

When we equate the previous two expressions, it yields

$$\frac{V_{\text{in}}}{10} = V_{\text{in}} \frac{Z_o}{Z_o + Z_{\text{probe}}}$$

We may cancel $V_{\text{in}}$ from both sides of the equation and rearrange terms

$$Z_o + Z_{\text{probe}} = 10 Z_o$$

Subtract $Z_o$ from both sides to solve for the probe impedance:

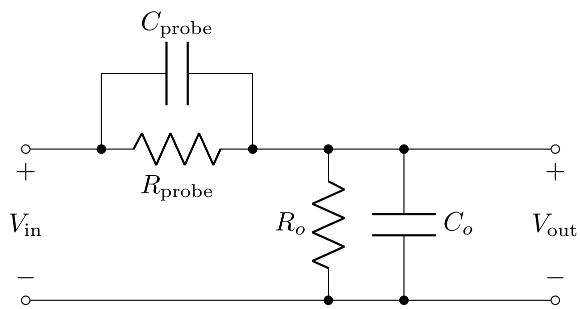
$$\begin{aligned} Z_{\text{probe}} &= 9 Z_o \\ &= 9 \left( R_o \parallel \frac{1}{j\omega C_o} \right) \\ &= 9 R_o \parallel \frac{9}{j\omega C_o} \\ &= 9 R_o \parallel \frac{1}{j\omega \left( \frac{1}{9} C_o \right)} \end{aligned}$$

So our “x10 probe” should be the parallel combination of a resistor and a capacitor. The resistor should be 9 times greater than the input resistance of the scope ($R_o$). The probe’s capacitor should be 9 times *smaller* than $C_o$ (the total capacitance of the cable and the oscilloscope).

$$R_{\text{probe}} = 9 R_o$$

$$C_{\text{probe}} = \frac{1}{9} C_o$$

Figure 1.37: x10 Probe




Many x10 probes implement $C_{\text{probe}}$ as a variable capacitor that the user may tune to very near one ninth the cable-plus-oscilloscope capacitance. This is sometimes referred to as “probe compensation”.

The input impedance of this x10 probe is

$$\begin{aligned} Z_{\text{in}} &= Z_{\text{probe}} + Z_o \\ &= 9R_o \parallel \frac{1}{j\omega\left(\frac{1}{9}C_o\right)} + \left(R_o \parallel \frac{1}{j\omega C_o}\right) \\ &= 9\left(R_o \parallel \frac{1}{j\omega C_o}\right) + \left(R_o \parallel \frac{1}{j\omega C_o}\right) \\ &= 10\left(R_o \parallel \frac{1}{j\omega C_o}\right) \\ Z_{\text{in}} &= \boxed{10Z_o} \end{aligned}$$

Finally, lets take a look at how the probe and the oscilloscope (working as a voltage divider) affect the output voltage as a function of the input voltage.

$$\begin{aligned} \frac{V_{\text{out}}}{V_{\text{in}}} &= \frac{Z_o}{Z_{\text{in}}} \\ &= \frac{R_o \parallel \frac{1}{j\omega C_o}}{10\left(R_o \parallel \frac{1}{j\omega C_o}\right)} \\ \frac{V_{\text{out}}}{V_{\text{in}}} &= \frac{1}{10} \end{aligned}$$

It is remarkable! The voltage transfer function of this circuit is *precisely* $\frac{1}{10}$. This circuit contains four passive components (two of them reactive) but **the transfer function does not depend on frequency**. Truly, the ancients were wise and knew many great things.

# Solutions for Chapter 2

## Exercise 2.1

In order to solve this problem, many assumptions must be made. Different people may assume slightly different values for parameters. This is OK. What is important is making good assumptions and checking our conclusions to make sure they are reasonable.

To solve for the current in the LED, let us assume we know the LED is red, so it follows the red LED curve from Figure 2.8 in the book. Let us also assume the transistor is acting like a closed switch, so the collector voltage of Q1 is close to 0 V. Let us also assume the LED is ON, so it's voltage is approximately $V_{\mathrm{LED}} = 2\,\mathrm{V}$. From the preceding assumptions, we can calculate that the LED current is

$$I_{\mathrm{LED}} = \frac{3.3\,\mathrm{V} - 2\,\mathrm{V}}{330\,\Omega} = \frac{1.3\,\mathrm{V}}{330\,\Omega} \approx 3.94\,\mathrm{mA}$$

If we use Figure 2.8 (from the textbook) to check our numbers, we see that a current of 3.94 mA roughly correlates to an LED voltage of $V_{\mathrm{LED}} = 1.7\,\mathrm{V}$. We will run the same calculation again to reduce our error.

$$I^*_{\mathrm{LED}} = \frac{3.3\,\mathrm{V} - 1.7\,\mathrm{V}}{330\,\Omega} = \frac{1.6\,\mathrm{V}}{330\,\Omega} \approx \boxed{4.85\,\mathrm{mA}}$$

In order to determine the minimum current gain required from our transistor, we must calculate the base current. Let us assume we know the base-emitter voltage $V_{\mathrm{BE}} = 0.6\,\mathrm{V}$. Therefore

$$I_{\mathrm{B}} = \frac{3.3\,\mathrm{V} - 0.6\,\mathrm{V}}{10\,\mathrm{k}\Omega} = 270\,\mu\mathrm{A}$$

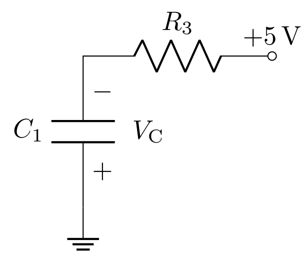
So the minimum current gain must be

$$\beta_{\mathrm{min}} = \frac{I^*_{\mathrm{LED}}}{I_{\mathrm{B}}} \approx \frac{4.85\,\mathrm{mA}}{270\,\mu\mathrm{A}} \approx \boxed{18.0}$$

## Exercise 2.2

When $Q_1$ goes is in saturation, the base voltage of $Q_2$ equals the opposite of the voltage on the capacitor $C_1$ at $t = 0\,\mathrm{s}$, $V_0 = 4.4\,\mathrm{V}$ and $Q_2$ is then cutoff. $V_{\mathrm{out}}$ will be equal to 5 V until $Q_2$ is brought in saturation again. This happens when its base voltage gets higher or equal to the $Q_2$ threshold voltage (0.6 V). As soon as $Q_1$ is brought in saturation, $C_1$ starts to discharge into the resistor $R_3$ and the equivalent circuit, valid until $Q_2$ is cutoff, is then:

Figure 2.1: Equivalent $C_1$ discharging circuit.




The time evolution of the voltage across the capacitor $C_1$ is given by:

$$V_{\mathrm{C}}(t) = (V_0 - V_\infty)\, e^{-\frac{t}{R_3 C_1}} + V_\infty$$

where $V_\infty$ is the steady-state voltage on the capacitor $C_1$ end equals $-5\,\mathrm{V}$. Given the considerations above, we have that $V_C(t = T_{\mathrm{pulse}}) = -0.6\,\mathrm{V}$. Solving for $t$ gives:

$$T_{\mathrm{pulse}} = -R_3 C_1 \ln\left(\frac{-0.6\,\mathrm{V} - V_\infty}{V_0 - V_\infty}\right) = \boxed{0.76 R_3 C_1 = 76\,\mathrm{\mu s}}$$

## Exercise 2.3

The output voltage is now influenced by $R_5$ that goes in series with $R_4$, and by the $V_{\mathrm{BE}}$ of $Q_3$ which is equal to $0.6\,\mathrm{V}$ when the transistor is in saturation. Therefore:

$$V_{\mathrm{out}} = \frac{R_5}{R_5 + R_4}\,(5\,\mathrm{V} - 0.6\,\mathrm{V}) + 0.6\,\mathrm{V} = \boxed{4.79\,\mathrm{V}}$$

The minimum value of $\beta$ of $Q_3$ can be obtained looking at the maximum value of the current flowing through the collector of $Q_3$, $I_{\mathrm{c}}^{\mathrm{Q_3}}$. As soon as $Q_1$ goes in saturation, the capacitor $C_1$ starts to discharge and its current is given by $C_1 dV_{\mathrm{C}}/dt$. With reference to the variables introduced in the previous exercise (2.2):

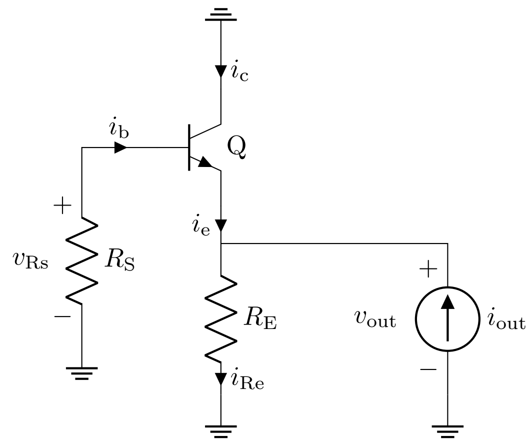
$$I_{\mathrm{c}}^{\mathrm{Q_3}}(t) = \frac{5\,\mathrm{V}}{R_2} - I_{\mathrm{C_1}}(t) = \frac{5\,\mathrm{V}}{R_2} + C_1 \frac{1}{R_3 C_1}\,(V_0 - V_\infty)\, e^{-\frac{t}{R_3 C_1}}$$

Therefore:

$$\beta_{\mathrm{min}} = \frac{I_{\mathrm{c}}^{\mathrm{Q_3}}(t)|_{\mathrm{max}}}{I_{\mathrm{b}}^{\mathrm{Q_3}}} = \frac{I_{\mathrm{c}}^{\mathrm{Q_3}}(t = 0\,\mathrm{s})}{I_{\mathrm{b}}^{\mathrm{Q_3}}} = \boxed{27}$$

# Exercise 2.4

Figure 2.2: Emitter follower circuit used for computing the output resistance




Applying the KCL on the Q transistor:

$$i_e = i_b + i_c = i_b\,(\beta + 1)$$

The current flowing through the emitter resistor $R_E$ is equal to:

$$i_{Re} = i_e + i_{out} = i_b\,(\beta + 1) + i_{out}$$

Since for the emitter follower $v_{Rs} = v_{out}$:

$$[i_b\,(\beta + 1) + i_{out}]\,R_E = v_{out}$$

Since:

$$i_b = -\frac{v_{Rs}}{R_S} = -\frac{v_{out}}{R_S}$$

we can write:

$$\left[-\frac{v_{out}}{R_S}\,(\beta + 1) + i_{out}\right] R_E = v_{out}$$

Therefore:

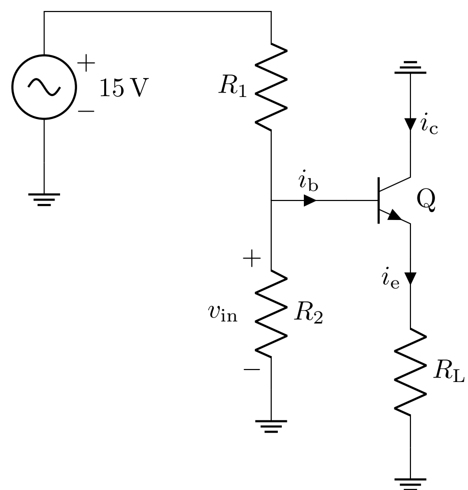
$$R_{out} = \frac{v_{out}}{i_{out}} = \frac{R_E R_S}{R_S + (\beta + 1)\,R_E}$$

If $R_E >> R_S/(\beta + 1)$:

$$\boxed{R_{out} \approx \frac{R_S}{(\beta + 1)}}$$

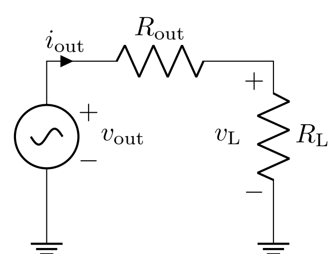
## Exercise 2.5

Figure 2.3: Small signal circuit




In order to achieve a maximum voltage change of 5 % for a maximum current to the load ($R_L$) equal to 25 mA, we can make reference to the equivalent circuit of Figure 2.4:

Figure 2.4: Output equivalent circuit




obtaining:

$$\left.\frac{v_{out} - v_L}{v_{out}}\right|_{i_{out}=25\,\mathrm{mA}} = 0.05$$

Since

$$v_{out} - R_{out}\, i_{out} = v_L$$

and for an emitter follower $v_{out} = v_{in} = 5\,\mathrm{V}$ we can write:

$$\frac{R_{out}\, 25\,\mathrm{mA}}{5\,\mathrm{V}} = 0.05$$

obtaining the following condition on $R_{out}$:

$$R_{out} = \frac{0.05\, 5\,\mathrm{V}}{25\,\mathrm{mA}}$$

For the emitter follower configuration:

$$R_{\rm out} = \frac{R_{\rm in}}{\beta + 1}$$

and we see from the circuit of Figure 2.3 that $R_{\rm in}$ is given by the parallel between $R_1$ and $R_2$:

$$R_{\rm in} = \frac{R_1\, R_2}{R_1 + R_2}$$

In order to achieve $v_{\rm in} = 5\,{\rm V}$, the following condition must be verified for the values of $R_1$ and $R_2$:

$$\frac{R_2}{R_1 + R_2} = \frac{5\,{\rm V}}{15\,{\rm V}}$$

Assuming $\beta = 100$, we can finally obtain:

$$\boxed{R_1 = 30\,\Omega,\ R_2 = 15\,\Omega}$$

## Exercise 2.6

The minimum current flowing through the $R$ resistor has to be at least equal to the maximum current to the load plus the minimum current to the zener:

$$I_{\rm min,R} = \frac{20\,{\rm V} - 10\,{\rm V}}{R} \geq 100\,{\rm mA} + 10\,{\rm mA}$$

Therefore:

$$R \leq \frac{10\,{\rm V}}{110\,{\rm mA}} = \boxed{91\,\Omega}$$

It follows that the maximum power to the zener, selecting $R = 91\,\Omega$, is equal to

$$P_{\rm max,z} = \left(\frac{25\,{\rm V} - 10\,{\rm V}}{91\,\Omega} - 0\,{\rm A}\right) 10\,{\rm V} = \boxed{1.65\,{\rm W}}$$

## Exercise 2.7

With reference to figure 2.21 of the book, neglecting the current entering the ase of the transistor $Q$, in order to have at least 10 mA flowing through the zener, the resistor $R$ should comply with the following condition:

$$\frac{20\,{\rm V} - 10\,{\rm V}}{R} \geq 10\,{\rm mA}$$

which results in:

$$\boxed{R \leq 1\,{\rm k}\Omega}$$

In order to avoid the transistor to be saturated, we want the collector-base voltage to be always higher than zero. This translates in:

$$R_{\rm C} < R\frac{10\,{\rm mA}}{100\,{\rm mA}} = 100\,\Omega$$

Selecting a conservative value of $R_{\rm C}$ equal to $\boxed{20\,\Omega}$, we can compute the maximum power dissipated by the zener, $P_{\rm max,z}$ and the transistor, $P_{\rm max,Q}$ as:

$$P_{\rm max,z} = \left(\frac{25\,{\rm V} - 10\,{\rm V}}{1\,{\rm k}\Omega}\right) 10\,{\rm V} = \boxed{0.15\,{\rm W}}$$

$$P_{\mathrm{Q}} = (25\,\mathrm{V} - 20\,\Omega I_{\mathrm{load}})\, I_{\mathrm{load}}$$

The maximum power dissipated by the transistor is obtained for a collector current equal to 625 mA which is higher than the maximum load current. Therefore, in our case, the maximum power dissipated by $Q$ will be obtained for $I_{\mathrm{load,max}} = 100\,\mathrm{mA}$:

$$P_{\mathrm{max,Q}} = (25\,\mathrm{V} - 20\,\Omega I_{\mathrm{load,max}})\, I_{\mathrm{load,max}} = \boxed{2.3\,\mathrm{W}}$$

Comparing the results with those of the previous exercise, we notice that the power disspated by the zener diode significantly decreased but we have an additional power dissipated by the transistor which is higher than the power that the zener diode dissipated in the circuit of the previous exercise. However this power can be decreased by increasing the value of $R_{\mathrm{C}}$.

## Exercise 2.8

In order to keep the emitter voltage $V_{\mathrm{E}}$ in the half range of the dc supply, considering the quiescent current of 5 mA we have:

$$V_{\mathrm{E}} = \frac{15\,\mathrm{V} - (-15\,\mathrm{V})}{2} = 15\,\mathrm{V}$$

and the emitter resistor $R_{\mathrm{E}}$:

$$R_{\mathrm{E}} = \frac{15\,\mathrm{V}}{5\,\mathrm{mA}} = \boxed{3\,\mathrm{k\Omega}}$$

Since the imput impedance to the transistor, under the assumption of a load resistance much larger than the emitter resistance, is:

$$R_{\mathrm{in}} = \beta R_{\mathrm{E}} = 300\,\mathrm{k\Omega}$$

in order to have the 3 dB point below the lowest frequency of 20 Hz, the capacitor $C_1$ has to be:

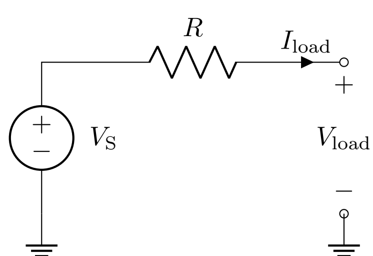
$$\frac{1}{R_{\mathrm{in}} C_1} \leq 20\,\mathrm{Hz}$$

meaning that:

$$\boxed{C_1 \geq 0.17\,\mathrm{\mu F}}$$

## Exercise 2.9

Figure 2.5: Current source circuit




We want:

$$\frac{I_{\mathrm{load}}^{\mathrm{max}} - I_{\mathrm{load}}^{\mathrm{min}}}{I_{\mathrm{load}}^{\mathrm{max}}} = \frac{V_{\mathrm{S}} - 0\,\mathrm{V} - (V_{\mathrm{S}} - 10\,\mathrm{V})}{V_{\mathrm{S}} - 0\,\mathrm{V}} = 0.01$$

from which it follows:

$$\boxed{V_{\mathrm{S}} = 1\,\mathrm{kV}}$$

## Exercise 2.10

With reference to Figure 2.5, we assume that $I_{\mathrm{load}}$ is equal to 10 mA if $V_{\mathrm{load}}$ is equal to 0 V, which means $R_{\mathrm{load}}$ is equal to 0 Ω. We can therfore calculate $R$ as:

$$R = \frac{V_{\mathrm{S}}}{10\,\mathrm{mA}} = 100\,\mathrm{k}\Omega$$

In this case we have:

$$\boxed{P_{\mathrm{load}} = 0\,\mathrm{W},\ P_{\mathrm{R}} = I_{\mathrm{load}}^2 R = 10\,\mathrm{W}}$$

If $V_{\mathrm{load}} = 10\,\mathrm{V}$, from the condition of the previous exercise, we have:

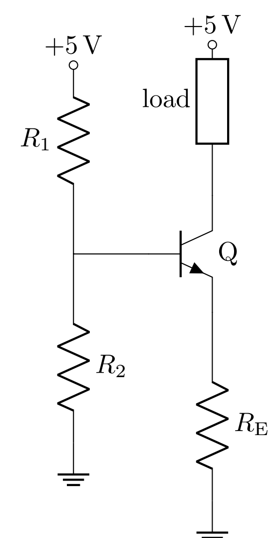
$$I_{\mathrm{load}} = (1 - 0.01)10\,\mathrm{mA} = 9.9\,\mathrm{mA}$$

Therefore:

$$\boxed{P_{\mathrm{load}} = 10\,\mathrm{V} I_{\mathrm{load}} = 0.1\,\mathrm{W},\ P_{\mathrm{R}} = I_{\mathrm{load}}^2 R = 9.8\,\mathrm{W}}$$

## Exercise 2.11

Figure 2.6: Current sink




In order to have an emitter current equal to 5 mA, the following condition has to be verified:

$$\frac{R_2}{R_1 + R_2} 5\,\mathrm{V} - 0.6\,\mathrm{V} = R_{\mathrm{E}} 5\,\mathrm{mA}$$

Furthermore, the transistor shouldn't sensibly load the voltage divider, therefore:

$$\frac{R_1 R_2}{R_1 + R_2} << R_{\mathrm{E}} \beta$$

Since we have a dc voltage of 5 V, we want the voltage on $R_2$ to be lower or equal to this value:

$$R_{\mathrm{E}} 5\,\mathrm{mA} + 0.6\,\mathrm{V} \leq 5\,\mathrm{V}$$

leading to:

$$R_{\mathrm{E}} \leq 880\,\Omega$$

A good guess value for $R_{\mathrm{E}}$ could be:

$$\boxed{R_{\mathrm{E}} = 200\,\Omega}$$

The base voltage will be given by:

$$V_{\mathrm{B}} = R_{\mathrm{E}} 5\,\mathrm{mA} + 0.6\,\mathrm{V} = 1.6\,\mathrm{V}$$

Selecting $\boxed{R_1 = 1\,\mathrm{k}\Omega}$ it is possible to compute $R_2$:

$$\boxed{R_2 = 470\,\Omega}$$

The impedance seen by the input of the transistor is equal to $320\,\Omega$ and the input impedance of the transistor, considering $\beta = 100$, is $R_{\mathrm{E}}\beta = 20\,\mathrm{k}\Omega$ with the former much lower than the latter. Finally, considering a maximum $V_{\mathrm{CE}}$ voltage of the transistor equal to $0.2\,\mathrm{V}$ before it saturates, we obtain the compliance voltage on the load as:

$$\boxed{V_{\mathrm{comp}} = 5\,\mathrm{V} - (0.2\,\mathrm{V} + R_{\mathrm{E}} 5\,\mathrm{mA}) = 3.8\,\mathrm{V}}$$

## Exercise 2.12

The distortion is given by:

$$\frac{\Delta V_{\mathrm{out}}}{V_{\mathrm{drop}}} \frac{V_{\mathrm{T}}}{V_{\mathrm{T}} + I_{\mathrm{E}} R_{\mathrm{E}}}$$

therefore, if $R_{\mathrm{E}} = 0\,\Omega$ we obtain a predicted distortion equal to $\boxed{\frac{\Delta G}{G} = \frac{0.2\,\mathrm{V}}{5\,\mathrm{V}} = 0.04}$ in case of $0.1\,\mathrm{V}$ output amplitude and $\boxed{\frac{\Delta G}{G} = \frac{2\,\mathrm{V}}{5\,\mathrm{V}} = 0.4}$ in case of $1\,\mathrm{V}$ output amplitude. If $R_{\mathrm{E}} I_{\mathrm{E}} = 0.25\,\mathrm{V}$, $\frac{\Delta G}{G}$ equals to $\boxed{0.004}$ and $\boxed{0.04}$ for output voltage amplitudes equal to $0.1\,\mathrm{V}$ and $1\,\mathrm{V}$, respectively.

## Exercise 2.13

If the transistor is biased at half $V_{\mathrm{cc}}$, we have that the collector-emitter voltage will be equal to $V_{\mathrm{CE}} = V_{\mathrm{cc}} - I_{\mathrm{C}} R_{\mathrm{C}} = V_{\mathrm{cc}} - V_{\mathrm{cc}}/2 = V_{\mathrm{cc}}/2$ where $I_{\mathrm{C}}$ is the collector quiescent current and $R_{\mathrm{C}}$ is the collector resistor. The collector-base voltage will be therefore $V_{\mathrm{CB}} = V_{\mathrm{cc}}/2 - V_{\mathrm{BE}}$. In this case $V_{\mathrm{BE}}$ is supposed to be obtained by means of a voltage divider. If the temperature changes, approximately $V_{\mathrm{BE}}$ does not change and the collecotr current will increase by $9\,\%\,°\mathrm{C}^{-1}$. This means that the collector current doubles for a temperature increase equal to $8\,°\mathrm{C}$. In this case $R_{\mathrm{C}} I_{\mathrm{C}}$ becomes equal to $2V_{\mathrm{cc}}/2 = V_{\mathrm{cc}}$. As a consequence $\boxed{V_{\mathrm{CB}} = -V_{\mathrm{BE}} < 0 \text{ and the transistor goes in saturation.}}$

## Exercise 2.14

The bias is arranged in order to have a collector current equal to $1\,\mathrm{mA}$. Indeed:

$$I_{\mathrm{c}} = \frac{0.775\,\mathrm{V} - 0.6\,\mathrm{V}}{175\,\Omega} = 1\,\mathrm{mA}$$

The base-emitter voltage decreases by $2.1\,\mathrm{mV}\,°\mathrm{C}^{-1}$. Therefore, if the temperature increases by $20\,°\mathrm{C}$, the collecotr current will become:

$$I_{\mathrm{c}} = \frac{0.775\,\mathrm{V} - 0.6\,\mathrm{V} - 0.0021\,\mathrm{V}\,°\mathrm{C}^{-1}\,20\,°\mathrm{C}}{175\,\Omega} = 0.76\,\mathrm{mA}$$

$\boxed{\text{It can be seen that the new collecotr current is about 25\,\% lower than 1\,mA}}$

## Exercise 2.15

The voltage gain is given by:

$$G = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = \frac{R_{\mathrm{C}}}{r_{\mathrm{e}}} = \frac{I_{\mathrm{C}} R_{\mathrm{C}}}{V_{\mathrm{T}}}$$

In order to achieve a voltage drop on $R_{\mathrm{C}}$ equal to half the $V_{\mathrm{cc}}$ voltage:

$$I_{\mathrm{C}} R_{\mathrm{C}} = \frac{1}{2} V_{\mathrm{cc}}$$

and therefore:

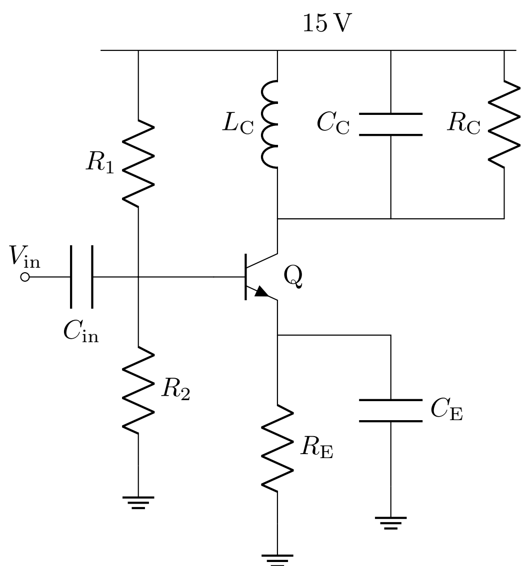
$$R_{\mathrm{C}} = \frac{1}{2} \frac{V_{\mathrm{cc}}}{I_{\mathrm{C}}}$$

Substituting the $R_{\mathrm{C}}$ expression into the voltage gain:

$$\boxed{G = \frac{1}{2} \frac{V_{\mathrm{cc}}}{V_{\mathrm{T}}} = \frac{V_{\mathrm{cc}}}{50\,\mathrm{mV}} = 20 V_{\mathrm{cc}}}$$

## Exercise 2.16

Figure 2.7: Tuned common emitter amplifier




With reference to Figure 2.7, we start by choosing the emitter resistor $R_{\mathrm{E}}$. We want its value to be large enough to have a voltage drop higher than $V_{\mathrm{BE}}$ in order to have a good stability of the quiescent current with the temperature. However we want the transistor to operate in the active region. Since at DC, the inductor behaves like a short circuit, we have that the collector voltage is equal to $V_{\mathrm{cc}}$, therefore:

$$R_{\mathrm{E}} I_{\mathrm{E}}^{\mathrm{Q}} < V_{\mathrm{cc}} - 0.2\,\mathrm{V}$$

and

$$R_{\mathrm{E}} < \frac{V_{\mathrm{cc}} - 0.2\,\mathrm{V}}{I_{\mathrm{E}}^{\mathrm{Q}}} = 14.8\,\mathrm{k\Omega}$$

where $I_{\mathrm{E}}^{\mathrm{Q}}$ is equal to about 1 mA. We choose:

$$\boxed{R_{\mathrm{E}} = 1\,\mathrm{k\Omega}}$$

In order to achieve a quiescent current equal to 1 mA, the base voltage has to be equal to:

$$V_{\mathrm{B}} = 0.6\,\mathrm{V} + R_{\mathrm{E}} I_{\mathrm{E}}^{\mathrm{Q}} = 1.6\,\mathrm{V}$$

Therefore, the ratio between $R_1$ and $R_2$ has to be equal to 8.4. Choosing the parallel resistance of $R_1$ and $R_2$ to be about one tenth of the transistor input resistance $\beta R_{\mathrm{E}} \approx 100\,\mathrm{k\Omega}$ we choose the following values for $R_1$ and $R_2$:

$$\boxed{R_1 = 84\,\mathrm{k\Omega}, \quad R_2 = 10\,\mathrm{k\Omega}}$$

The value of the capacitor $C_{\mathrm{C}}$ can be obtained forcing the parallel LC circuit to resonate at 100 kHz:

$$\frac{1}{2\pi}\sqrt{\frac{1}{L_{\mathrm{C}} C_{\mathrm{C}}}} = 100\,\mathrm{kHz}$$

Therefore:

$$\boxed{C_{\mathrm{C}} = 2.5\,\mathrm{nF}}$$

The value of the capacitor $C_{\mathrm{E}}$ can be selected imposing that the absolute value of the impedance of the parallel between $R_{\mathrm{E}}$ and $C_{\mathrm{E}}$ is lower than $r_{\mathrm{e}} = 25\,\Omega$ for a quiescent current of 1 mA. Doing the math we obtain:

$$C_{\mathrm{E}} > \frac{\sqrt{\frac{R_{\mathrm{E}}}{25\,\Omega}^2 - 1}}{\omega R_{\mathrm{E}}} = 63.6\,\mathrm{nF}$$

A value of $C_{\mathrm{E}}$ equal to 10 µF is conservative enough to maximise the AC gain:

$$\boxed{C_{\mathrm{E}} = 10\,\mathrm{\mu F}}$$

It remains to calculate the value of the input decoupling capacitor $C_{\mathrm{in}}$. Its value can be obtained by forcing the cut-off frequency $1/R_{\mathrm{in}}$ to be below 100 kHz where

$$R_{\mathrm{eq}} = \beta r_{\mathrm{e}} || R_1 || R_2$$

where we neglected the emitter impedance which is verly low thanks to the $C_{\mathrm{E}}$ effect. We have therefore:

$$C_{\mathrm{in}} \geq 5\,\mathrm{nF}$$

Even in this case a conservative value for $C_{\mathrm{in}}$ can be:

$$\boxed{C_{\mathrm{in}} = 10\,\mathrm{\mu F}}$$

## Exercise 2.17

In the following, the pedix B, C and E refer to base, collector and emitter. The apix Q1, Q2 and Q3 refer to the relevant transistors. Supposing all the transistors share the same $\beta$, the $I_{\mathrm{P}}$ currect can be expressed as:

$$I_{\mathrm{P}} = I_{\mathrm{C}}^{\mathrm{Q1}} + I_{\mathrm{B}}^{\mathrm{Q3}} = \beta I_{\mathrm{B}}^{\mathrm{Q1}} + \frac{I_{\mathrm{C}}^{\mathrm{Q3}}}{\beta}$$

Since the base-emitter voltage of the transistor Q1 is the same of the transistor Q2, the base currents are the same. Therefore:

$$I_{\mathrm{B}}^{\mathrm{Q1}} + I_{\mathrm{B}}^{\mathrm{Q2}} = 2 I_{\mathrm{B}}^{\mathrm{Q1}} = I_{\mathrm{E}}^{\mathrm{Q3}} - I_{\mathrm{C}}^{\mathrm{Q1}} = \frac{\beta + 1}{\beta} I_{\mathrm{C}}^{\mathrm{Q3}} - \beta I_{\mathrm{B}}^{\mathrm{Q1}}$$

and then:

$$I_{\mathrm{B}}^{\mathrm{Q1}} = \frac{\beta+1}{\beta(\beta+2)} I_{\mathrm{C}}^{\mathrm{Q3}}$$

Substituting this expression into the first equation, it is possible to obtain the following expression for $I_{\mathrm{P}}$:

$$I_{\mathrm{P}} = \left(1 + \frac{2}{\beta(\beta+2)}\right) I_{\mathrm{C}}^{\mathrm{Q3}} \approx I_{\mathrm{C}}^{\mathrm{Q3}}$$

By comparing the above expression with that that typical of a basic current mirror:

$$I_{\mathrm{P}} = \left(1 + \frac{2}{\beta}\right) I_{\mathrm{C}}$$

one can see that the load current $I_{\mathrm{C}}^{\mathrm{Q3}}$ is much colser to the reference current $I_{\mathrm{P}}$ than for the basic current mirror. Indeed:

$$\frac{2}{\beta(\beta+2)} << \frac{2}{\beta}$$

## Exercise 2.18

For a grounded differential amplifier, the differential gain is:

$$G_{\mathrm{diff}} = \frac{R_{\mathrm{C}}}{2r_{\mathrm{e}}} = \frac{R_{\mathrm{C}} I_{\mathrm{C}}}{2V_{\mathrm{T}}} = V_{\mathrm{C}} 2 V_t ext T = \boxed{20 V_{\mathrm{C}}}$$

where $V_{\mathrm{C}}$ is the voltage drop across the collector resistor $R_{\mathrm{C}}$. Therefore, if $V_{\mathrm{C}} = 0.5 V_{\mathrm{cc}}$:

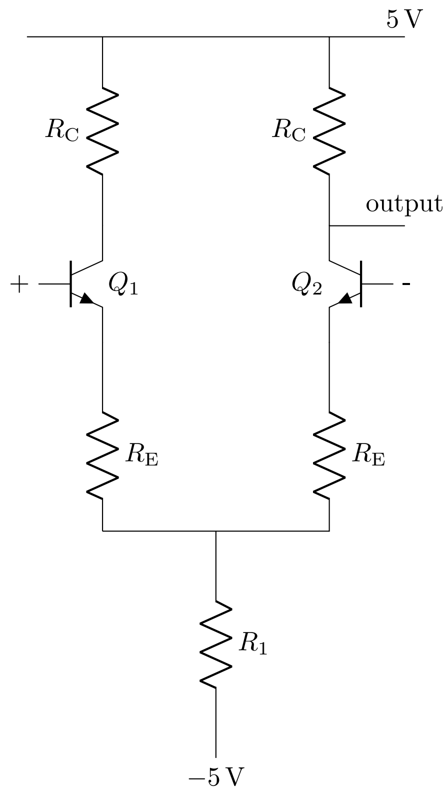
$$\boxed{G_{\mathrm{diff}} = 10 V_{\mathrm{cc}}}$$

Following a similar argument:

$$\mathrm{CMRR} = \frac{R_1}{r_{\mathrm{e}}} = \frac{R_1 I_{\mathrm{C}}}{V_{\mathrm{T}}} = \frac{1}{2} V_1 V_{\mathrm{T}} = \boxed{20 V_1}$$

where $V_1$ is the voltage drop across the $R_1$ resistor.

Figure 2.8: Tuned common emitter amplifier




For the differential, single-ended amplifier in Figure 2.8, the output impedance is equal to $R_C$. Therefore we have $\boxed{R_C = 10\,\mathrm{k\Omega}}$. Since we want the voltage drop on the collector resistor to be half of the $V_{cc}$:

$$\boxed{I_C = 2.5\,\mathrm{V}\,10\,\mathrm{k\Omega} = 250\,\mathrm{\mu A}}$$

Neglecting the voltage drop on the emitter resistor $R_E$, we can approximate the collector current as:

$$I_C \approx \frac{5\,\mathrm{V} - 0.6\,\mathrm{V}}{2R_1}$$

and therefore:

$$\boxed{R_1 = 2.8\,\mathrm{k\Omega}}$$

The value of $R_E$ can then be obtained from the differential gain, considering that it is given by:

$$G_{diff} = 25 = \frac{R_C}{2\,(r_e + R_E)}$$

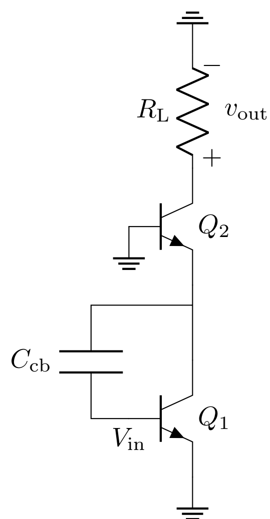
. Therefore, considering that $r_e = V_T/I_C = 100\,\Omega$:

$$\boxed{R_E = 100\,\Omega}$$

## Exercise 2.19

As regards the differential amplifier in Figure 2.84 of the book, the AC voltage across the $C_{\mathrm{CB}}$ capacitor is equal to the voltage at the base of the transistor $Q_1$ without depending on the voltage gain. The voltage across the emitter resistor $R_{\mathrm{E}}$ is the input to a common base amplifier which does not have Miller effect.

Figure 2.9: Cascode amplifier




As regards the cascode configuration, one can make reference to Figure 2.9. Under the approximation that the collecotr current of the transistor $Q_1$ is equal to that of the transistor $Q_2$:

$$i_{\mathrm{C}}^{\mathrm{Q}_1} = i_{\mathrm{C}}^{\mathrm{Q}_2} = \frac{v_{\mathrm{in}}}{r_{\mathrm{e}}^{\mathrm{Q}_1}}$$

where $r_{\mathrm{e}}^{\mathrm{Q}_1}$ is the differential resistance of the $Q_1$ transistor. The output voltage will be:

$$v_{\mathrm{out}} = R_{\mathrm{L}} i_{\mathrm{C}}^{\mathrm{Q}_2}$$

The base-emitter AC voltage of the $Q_2$ transistor will be:

$$v_{\mathrm{BE}}^{\mathrm{Q}_2} = r_{\mathrm{e}}^{\mathrm{Q}_2} i_{\mathrm{C}}^{\mathrm{Q}_2}$$

where $r_{\mathrm{e}}^{\mathrm{Q}_2}$ is the differential resistance of the $Q_2$ transistor.
The voltage across the $C_{\mathrm{CB}}$ capacitor will be:

$$v_{\mathrm{CB}} = v_{\mathrm{in}} + v_{\mathrm{BE}}^{\mathrm{Q}_2} = v_{\mathrm{in}} + \frac{v_{\mathrm{in}} r_{\mathrm{e}}^{\mathrm{Q}_2}}{r_{\mathrm{e}}^{\mathrm{Q}_1}}$$

It follows that the amplitude of the current through the $C_{\mathrm{CB}}$ capacitor is:

$$I_{\mathrm{CB}} = \frac{v_{\mathrm{in}} \left(1 + \frac{r_{\mathrm{e}}^{\mathrm{Q}_2}}{r_{\mathrm{e}}^{\mathrm{Q}_1}}\right)}{X_{\mathrm{CB}}}$$

where $X_{\mathrm{CB}}$ is the capacitive reactance associated to the $C_{\mathrm{CB}}$ capacitor. The Miller capacitance $C_{\mathrm{CB}}^{\mathrm{M}}$ is therefore:

$$\boxed{C_{\mathrm{CB}}^{\mathrm{M}} = C_{\mathrm{CB}}\left(1 + \frac{r_{\mathrm{e}}^{\mathrm{Q}_2}}{r_{\mathrm{e}}^{\mathrm{Q}_1}}\right)}$$

and does not depend on the voltage gain of the cascode amplifier.

# Exercise 2.20

The expression for the input impedance of the inverting amplifier is straightforward by considering that it is the series between the $R_1$ resistance with the input impedance of the transresistance amplifier. Therefore, the input impedance $Z_{\mathrm{in}}$ is:

$$\boxed{Z_{\mathrm{in}} = R_1 + R_{\mathrm{in}}||\frac{R_2}{1+A}}$$

The closed loop gain can also be obtained in a straightforward way starting by considering the input impedance of the operational amplifier, $R_{\mathrm{in}}$, apporaching to infinity. In this case, all the current flowing in $R_1$ goes in $R_2$ making $R_1$ and $R_2$ in series. Therefore:

$$V_{\mathrm{out}} = vA$$

where $v$ is the differential voltage of the operational amplifier and $A$ is the open loop gain.
$v$ is given by:

$$v = -[V_{\mathrm{in}} - (V_{\mathrm{in}} - V_{\mathrm{out}})B]$$

where $B$ is defined as:

$$\frac{R_1}{R_1 + R_2}$$

The expression for the output voltage becomes:

$$V_{\mathrm{out}} = -A[V_{\mathrm{in}} - (V_{\mathrm{in}} - V_{\mathrm{out}})B]$$

and the closed loop gain is:

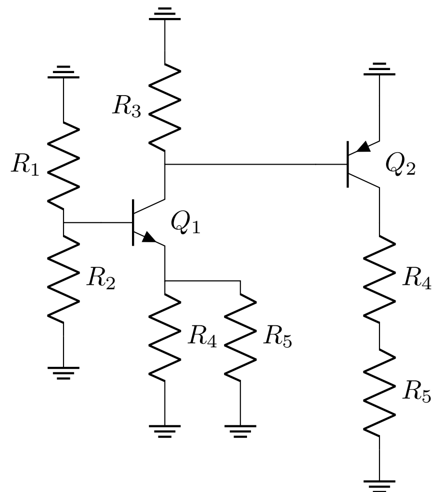
$$\boxed{G = \frac{V_{\mathrm{out}}}{V_{\mathrm{in}}} = -A\frac{1-B}{1+AB}}$$

# Exercise 2.21

$$\boxed{G_{\mathrm{CL}} = \frac{-100j}{1+-100j(0.1)} = 9.90 - 0.99j}$$

# Exercise 2.22

Figure 2.10: Open loop small signal circuit




The feedback takes the voltage from the output of Q2 transistor and returns it to the input of the Q1 transistor through a voltage divider made of the resistors $R_4$ and $R_5$. The feedback is of *voltage-voltage* kind. In order to account ofr the feedback loading effect in opening the loop, the reference circuit is that of Figure 2.10. Considering a $\beta$ of 100 for both Q1 and Q2, the open loop gain is:

$$G^{\text{OL}} = \frac{-1}{r_{\text{e}}^{\text{Q}_1} + R_4||R_5} \left[R_3||r_{\text{e}}^{\text{Q}_2}\beta\right] \left[-\frac{R_4 + R_5}{r_{\text{e}}^{\text{Q}_2}}\right] \approx \frac{1}{r_{\text{e}}^{\text{Q}_1} + R_4} \left[R_3||r_{\text{e}}^{\text{Q}_2}\beta\right] \left[\frac{R_5}{r_{\text{e}}^{\text{Q}_2}}\right]$$

Therfore, since $r_{\text{e}}^{\text{Q}_1} = r_{\text{e}}^{\text{Q}_2} = 25\,\Omega$:

$$\boxed{G^{\text{OL}} \approx 200}$$

The feedback gain is:

$$B = \frac{R_4}{R_4 + R_5} \approx \frac{R_4}{R_5} = 0.1$$

Therfore, the loop gain is:

$$\boxed{G^{\text{OL}}B \approx 20}$$

The open loop output impedance is:

$$\boxed{Z_{\text{out}}^{\text{OL}} = R_4 + R_5 \approx R_5 = 10\,\text{k}\Omega}$$

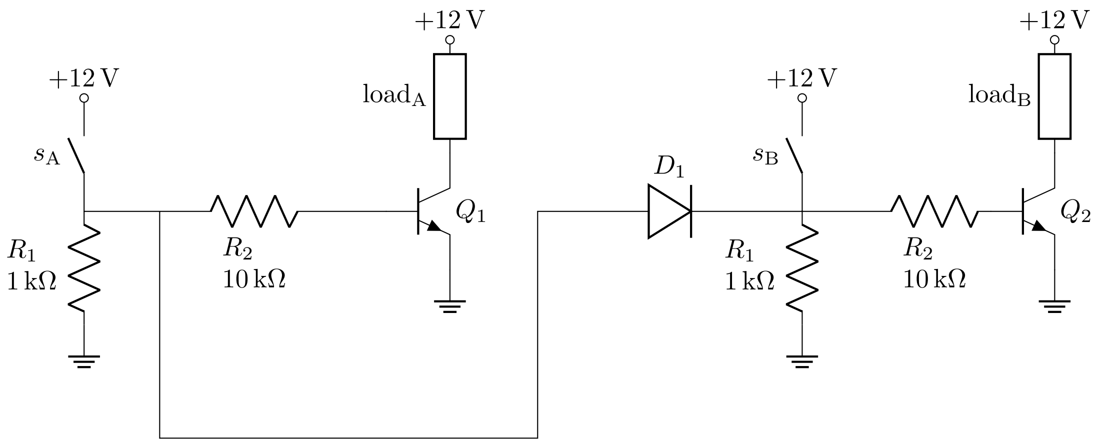
The closed loop parameters are therefore:

$$\boxed{G^{\text{CL}} = \frac{G^{\text{OL}}}{1 + G^{\text{OL}}B} \approx 9.5}$$

$$\boxed{Z_{\text{out}}^{\text{CL}} = \frac{Z_{\text{out}}^{\text{OL}}}{1 + G^{\text{OL}}B} \approx \frac{Z_{\text{out}}^{\text{OL}}}{G^{\text{OL}}B} = 500}$$

## Exercise 2.23

Figure 2.11: Solution




Let's suppose the loads are resistive with a resistance equal to $150\,\Omega$ and both the npn transistors have $\beta = 100$. When $s_\mathrm{A}$ and $s_\mathrm{B}$ are open, both $Q1$ and $Q2$ bases are to ground and no current flows into the loads.
If $s_\mathrm{A}$ is closed, the left terminals of the $R_2$ resistors are at 12 V (minus a diode voltage drop for the resistor connected at the $Q_2$ base). The base currents are therefore:

$$I_\mathrm{b} = \frac{12\,\mathrm{V} - 0.6\,\mathrm{V}}{10\,\mathrm{k}\Omega} = 1.14\,\mathrm{mA}$$

Such a base current, with the considered $\beta$ and load resistance, causes $Q_1$ and $Q_2$ to saturate. Therefore, the load current is:

$$I_\mathrm{l}^A = I_\mathrm{l}^B = \frac{12\,\mathrm{V} - 0.2\,\mathrm{V}}{150\,\Omega} = 79\,\mathrm{mA}$$

When $s_\mathrm{A}$ is open and $s_\mathrm{B}$ is closed, $D_1$ is reverse biased and $Q_1$ is in cutoff region since no current flows into its base. However, 1.14 mA flows into the base of $Q_2$ which goes into saturation.

## Exercise 2.24

(a) Under the assumption that $\beta$ is very large, the load current $I_\mathrm{load}$ is given by:

$$I_\mathrm{load} = I_\mathrm{C} \approx I_\mathrm{E}\left[\frac{V_\mathrm{cc}R_2}{R_1 + R_2} - 0.6\,\mathrm{V}\right]\frac{1}{R_\mathrm{E}}$$

where $V_\mathrm{CC} = 10\,\mathrm{V}$, $R_1 = 8.2\,\mathrm{k}\Omega$, $R_1 = 1.6\,\mathrm{k}\Omega$ and $R_1 = 1.5\,\mathrm{k}\Omega$. Therefore $\boxed{I_\mathrm{load} = 0.7\,\mathrm{mA}}$ Since for the transistor to work in active region it must hold:

$$V_\mathrm{CE} = V_\mathrm{CC} - V_\mathrm{load} - V_\mathrm{E} \geq 0.2\,\mathrm{V}$$

since $V_\mathrm{E} = I_\mathrm{E}R_\mathrm{E} \approx 1\,\mathrm{V}$ the output compliance is given by:

$$\boxed{V_\mathrm{load} \leq 8.8\,\mathrm{V}}$$

(b) Removing the assumption that $\beta$ is very large, has two effects. First, the emitter current and the collector currents are no more equal:

$$I_{\text{load}} = I_{\text{C}} = \beta \frac{1}{\beta + 1} I_{\text{E}}$$

Second, the $R_1$ and $R_2$ resistors are nomore in series since the bas current is no more negligible. The full expression for the emitter current can be obtained by considering that:

$$I_{\text{E}} = I_{\text{B}} + I_{\text{C}}$$
$$I_1 = I_{\text{B}} + I_2$$

where $I_1$ and $I_2$ are the currents flowing through $R_1$ and $R_2$,respectively, and $I_{\text{B}}$ is the base current. Under this conditions, the emitter current is given by:

$$I_{\text{E}} = \frac{1}{R_{\text{E}}} \left[ \frac{V_{\text{CC}} R_2}{R_1 + R_2} - 0.6\,\text{V} \right] \left[ 1 + \frac{R_2}{R_1(\beta + 1)} \left( 1 - \frac{R_2}{R_1 + R_2} \right) \right]^{-1}$$

It follows:

$$\beta = 50 \quad I_{\text{E}} = 0.685\,\text{mA} \quad I_{\text{load}} = I_{\text{C}} = 0.67\,\text{mA}$$
$$\beta = 100 \quad I_{\text{E}} = 0.688\,\text{mA} \quad I_{\text{load}} = I_{\text{C}} = 0.68\,\text{mA}$$

(c) Here we consider again that $\beta$ is very large. Being $R_1$ and $R_2$ in series, the base voltage does not change due to early effect and we can write:

$$\Delta I_{\text{E}} = -\frac{\Delta V_{\text{BE}}}{R_{\text{E}}} = \frac{0.0001 \Delta V_{\text{CE}}}{R_{\text{E}}}$$

Furthermore:

$$\Delta V_{\text{CE}} = -\Delta V_{\text{load}} - \Delta I_{\text{E}} R_{\text{E}}$$

Solving for $\Delta I_{\text{E}}$:

$$\Delta I_{\text{load}} = \Delta I_C \approx \Delta I_{\text{E}} = \frac{-0.0001}{1.0001 R_{\text{E}}} \Delta V_{\text{load}}$$

For an output voltage within the output compliance ($\Delta V_{\text{load}} = 8.8\,\text{V}$):

$$\boxed{\Delta I_{\text{load}} = -66.7\,\text{nA}}$$

(d) $V_{\text{BE}}$ varies by $-2.1\,\text{mV}\,{}^\circ\text{C}^{-1}$. With respect to the load current computed at the first point (a) ($I_{\text{load}} = 0.7\,\text{mA}$) it is easy to see that:

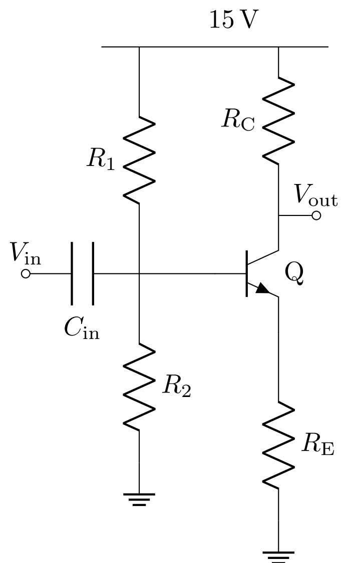
$$\boxed{\frac{\Delta I_{\text{load}}}{\Delta^\circ\text{C}} = 0.2\,\%\,{}^\circ\text{C}^{-1}}$$

In order to account for the variation of $\beta$ with temperature, we have to use the expression obtained in point b. In this case we obtain:

$$\boxed{\frac{\Delta I_{\text{load}}}{\Delta^\circ\text{C}} = 0.21\,\%\,{}^\circ\text{C}^{-1}}$$

## Exercise 2.25

Figure 2.12: Common emitter amplifier




The gain is approximately given by:

$$G = \frac{R_C}{R_E} = 15$$

Given a bias collector current of 0.5 mA, in order to have the bias collector voltage at $0.5V_{CC} = 7.5\,\mathrm{V}$, the collector resistance has to be equal to:

$$\boxed{R_C = \frac{7.5\,\mathrm{V}}{0.5\,\mathrm{mA}} = 15\,\mathrm{k\Omega}}$$

It follows that $\boxed{R_E = 1\,\mathrm{k\Omega}}$ In order to have a bias collector current equal to 0.5 mA, the following condition must hold:

$$I_C \approx I_E = \frac{V_B - 0.6\,\mathrm{V}}{R_E}$$

meaning that $V_B = 1.1\,\mathrm{V}$ This defines the first out of three conditions on the value of the resistors $R_1$ and $R_2$:

$$V_{CC}\frac{R_2}{R_1 + R_2} = 1.1\,\mathrm{V} \rightarrow R_1 = 12.64\,R_2$$

The second condition can be obtained by considering the maximum emitter voltage:

$$V_E^{MAX} = R_E I_E^{MAX} = 1\,\mathrm{k\Omega}\,1\,\mathrm{mA} = 1\,\mathrm{V}$$

the minimum current flowig through $R_1$ is:

$$I_{R_1}^{MIN} = \frac{V_{CC} - 1.6\,\mathrm{V}}{R_1} = \frac{13.4\,\mathrm{V}}{R_1}$$

In order to properly drive the base of the transistor, this current has to be higher than the maximum base current:

$$\frac{13.4\,\mathrm{V}}{R_1} > \frac{1\,\mathrm{mA}}{\beta}$$

leading to the second condition:

$$R_1 < 1.34\,\mathrm{M\Omega}$$

Finally, the input impedance of the transistor should be much higher than the parallel impedance of $R_1$ and $R_2$:

$$\frac{R_1 R_2}{R_1 + R_2} << \beta R_\mathrm{E} = 100\,\mathrm{k\Omega}$$

Taking into account these conditions, we select the following values for $R_1$ and $R_2$:

$$\boxed{R_1 = 20.2\,\mathrm{k\Omega},\ R_2 = 1.6\,\mathrm{k\Omega}}$$

To be sure the 3 dB point is below the frequency of interest (100 Hz), the value of the input capacitor can be computed by:

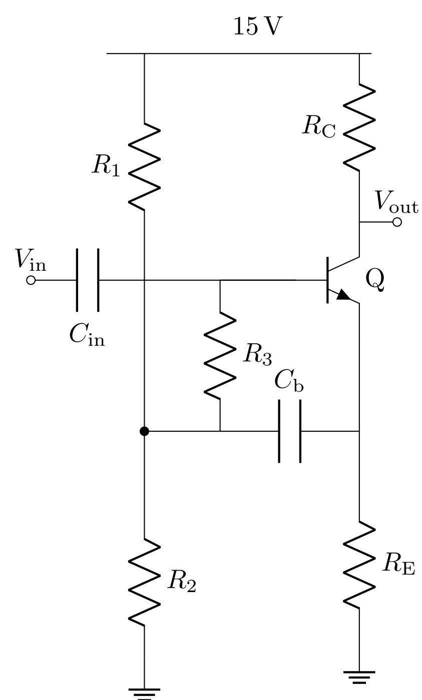
$$\frac{1}{1.5\,\mathrm{k\Omega}\, C_\mathrm{in}} < 2\pi 100\,\mathrm{Hz}$$

where $1.5\,\mathrm{k\Omega}$ is the value of the parallel $R_1$ and $R_2$. From the previous expression one can obtain the value of the input capacitance $C_\mathrm{in}$:

$$\boxed{C_\mathrm{in} > 1.06\,\mathrm{\mu F}}$$

## Exercise 2.26

Figure 2.13: Bootstrapped common emitter amplifier



From a small signal perspective, the equivalent $R_3$ resistance is given by:

$$R_{\mathrm{eq}} = \frac{R_3}{1-A}$$

where $A$ is the voltage gain of the emitter follower and it is given by:

$$\frac{R_{\mathrm{E}} g_{\mathrm{m}}}{1 + R_{\mathrm{E}} g_{\mathrm{m}}} = 0.95$$

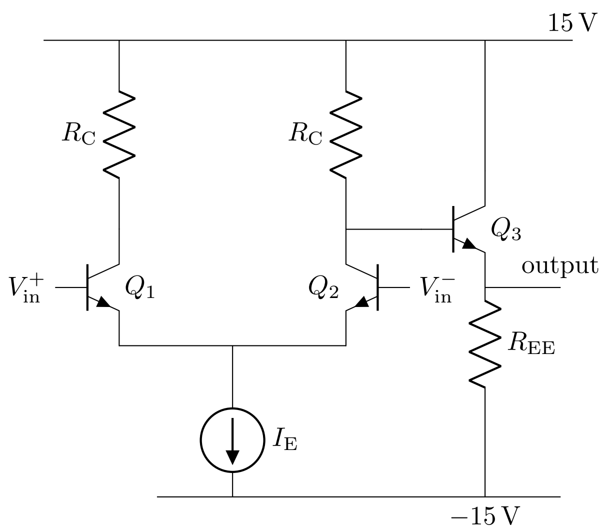
since $g_{\mathrm{m}} = \frac{0.5\,\mathrm{mA}}{25\,\mathrm{mV}} = 0.02\,\mathrm{S}$ Therefore $R_{\mathrm{eq}} \approx 20R_3$.
We can choose $\boxed{R_3 = 4.7\,\mathrm{k\Omega}}$ to obtain a $R_{\mathrm{eq}} = 94\,\mathrm{k\Omega}$ The resistance seen by the $C_{\mathrm{b}}$ capacitor is equal to:

$$R_1||R_2||(R_{\mathrm{eq}} + 100\,\mathrm{k\Omega}) \approx 1.5\,\mathrm{k\Omega}$$

Therefore we want the capacitive impedance of $C_{\mathrm{b}}$ at $100\,\mathrm{Hz}$ to be much lower than $1.5\,\mathrm{k\Omega}$. Choosing a $\boxed{C_{\mathrm{b}} = 10\,\mathrm{\mu F}}$ should be enough.

# Exercise 2.27

Figure 2.14: Differential pair and emitter follower




At DC, when $V_{\mathrm{in}}^+ = V_{\mathrm{in}}^- = 0\,\mathrm{V}$ the current $I_{\mathrm{E}}$ is splitted equally between $Q_1$ and $Q_2$. Therefore, if the emitter current of both transistors has to be equal to $0.1\,\mathrm{mA}$ we have that $\boxed{I_{\mathrm{E}} = 0.2\,\mathrm{mA}}$ The differential gain $G_{\mathrm{d}}$ has to be equal to 50:

$$G_{\mathrm{d}} = \frac{R_{\mathrm{C}}}{2r_{\mathrm{E}}} = 50$$

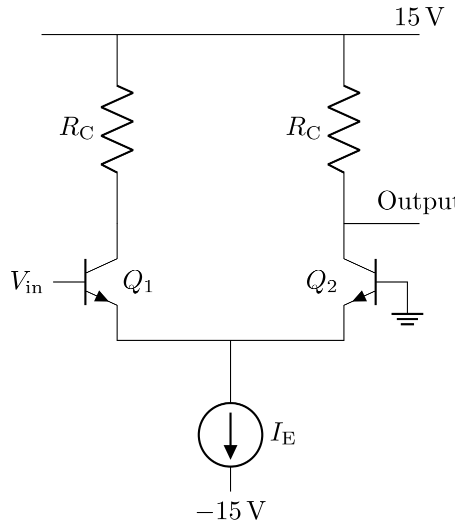
Since $R_{\mathrm{E}} = 25\,\mathrm{mV}/0.1\,\mathrm{mA} = 250\,\Omega$, we have that $\boxed{R_{\mathrm{C}} = 25\,\mathrm{k\Omega}}$ If we also want the bias current of transistor $Q_3$ to be equal to $0.1\,\mathrm{mA}$:

$$\boxed{R_{\mathrm{EE}} = \frac{15\,\mathrm{V} + 15\,\mathrm{V} - 0.6\,\mathrm{V} - R_{\mathrm{C}}\,0.1\,\mathrm{mA}}{0.1\,\mathrm{mA}} \approx 270\,\mathrm{k\Omega}}$$

As a final note, the differential pair is not degenerated. This led to a lower resistance $R_{\mathrm{C}}$ but to a higher resistance $R_{\mathrm{EE}}$ and a very small linearity region.

# Exercise 2.28

Figure 2.15: Differential pair with current source emitter




(a)

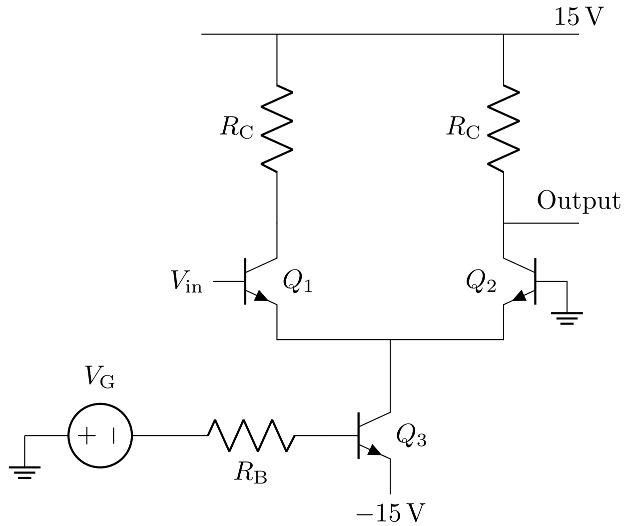
The quiscient current $I_E$ will be equally divided among the two transistors $Q_1$ and $Q_2$. Therefore, in order to have a collector current equal to 100 µA, $\boxed{I_E = 200\,\mu A}$. The gain of the single ended input-output differential pair can be easily computed by considering that the equivalent resistance as seen from $Q_2$ emitter is equal to $r_E^{Q_2}$. Therefore, the gain will be equal to:

$$\boxed{G = \frac{R_C}{r_E^{Q_1} + r_E^{Q_2}} = \frac{R_C}{2r_E} = 20}$$

since:

$$r_E^{Q_1} = r_E^{Q_2} = r_E = \frac{25\,\text{mV}}{100\,\mu\text{A}} = 250\,\Omega$$

Figure 2.16: Differential pair with variable current emitter




(b)

In the circuit of Figure 2.16, the DC voltage $V_G$ tunes the base current into the transistor $Q_3$ changing the quiescent current into the transistors $Q_1$ and $Q_2$. The value of the resistor $R_B$ can be obtained by imposing that the maximum $V_G$ voltage that doesn't saturate the transistors $Q_1$ and $Q_2$ is 10 V. By virtue of the $V_{BE}$ of $Q_2$, the emitter of $Q_1$ and $Q_2$ is at −0.6 V with respect to ground. Therefore, the maximum collector current that doesn't cause $Q_1$ and $Q_2$ to saturate can be obtained as:

$$I_C^{max} = \frac{15\,\mathrm{V} + 0.6\,\mathrm{V} - 0.2\,\mathrm{V}}{R_C} = 1.54\,\mathrm{mA}$$

The $Q_3$ maximum collector current will be twice $I_C^{max}$. Therefore, we have:

$$\beta \frac{15\,\mathrm{V} - 10\,\mathrm{V} - 0.6\,\mathrm{V}}{R_B} = 2I_C^{max}$$

which gives:

$$\boxed{R_B = 143\,\mathrm{k\Omega}}$$

In order to compute the gain, first we have to compute the value of the quiescent collector current of $Q_1$ and $Q_2$. This will be equal to:

$$I_C^Q = \beta \frac{1}{2} \frac{15\,\mathrm{V} - 0.6\,\mathrm{V} - V_G}{R_B}$$

The gain will be equal to:

$$\boxed{G = \frac{1}{2} \frac{I_C^Q R_C}{25\,\mathrm{mV}} \approx 70\,(14.4\,\mathrm{V} - V_G)}$$

## Exercise 2.29

(a) Since the quiescent point is equal to $0.5V_{CC}$, the quiescent collector current can be computed as:

$$I_C = \frac{1}{2} \frac{20\,\mathrm{V}}{10\,\mathrm{k\Omega}} = 1\,\mathrm{mA}$$

Using the Ebers-Moll equation to derive the base quiescent voltage:

$$V_{\mathrm{BE}} = V_{\mathrm{T}} \ln\left(\frac{I_{\mathrm{C}}}{I_{\mathrm{S}}}\right) = 0.69\,\mathrm{V}$$

with a saturation current $I_{\mathrm{S}}$ equal to $1 \times 10^{-15}$ A, it is possible to estimate the value of the variable resistor $R$ that leads to this voltage:

$$R = \frac{1\,\mathrm{k\Omega}\,0.69\,\mathrm{V}}{20\,\mathrm{V} - 0.69\,\mathrm{V}} = 35.8\,\Omega$$

The input impedance will be therefore the parralle between $1\,\mathrm{k\Omega}$, $35.8\,\Omega$ and $\beta\, r_{\mathrm{E}}$, being $r_{\mathrm{E}}$ the differential resistance of the transistor:

$$r_{\mathrm{E}} = \frac{I_{\mathrm{C}}}{V_{\mathrm{T}}} \approx 25\,\Omega$$

$\boxed{\text{It follows that the input impedance } Z_{\mathrm{in}} \text{ is approximately equal to } 34\,\Omega}$

(b) The differential gain is equal to the ratio between the collector resistor and the differential resistor $R_{\mathrm{E}}$. Therefore:

$$\boxed{G = \frac{10\,\mathrm{k\Omega}}{25\,\Omega}}$$

(c) Since the collector quiescent current approximately changes by $9\,\%\,{}^{\circ}\mathrm{C}^{-1}$, it is easily seen that its amount doubles for a temeprature change of $\boxed{8\,{}^{\circ}\mathrm{C}}$. This leads to a quiescent collector voltage equal to 20 V causing the transistor to saturate.

## Exercise 2.30

The bias base current into $Q_1$ ($I_B^{Q_1}$) is the sum of the input bias current (from *input 1*: $I^{I1}$) and the collector current from the $Q_4$ transistor of the current mirror made of $Q_4$ and $Q_3$ ($I_C^{Q_4}$):

$$I_B^{Q_1} = I^{I1} + I_C^{Q_4}$$

Therrefore:

$$I^{I1} = I_B^{Q_1} - I_C^{Q_4}$$

Since $Q_1$ and $Q_2$ are beta matched, their base currents are the same since sharing the same collector current. The current mirror copies the base current of $Q_2$ on $Q_4$ and therefore $I_C^{Q_4} = I_B^{Q_1}$. It follows that:

$$\boxed{I^{I1} = I_B^{Q_1} - I_C^{Q_4} = 0\,\mathrm{A}}$$

In order for the circuit to operate correctly, all transistors have to work in active operation region. For this to be verified, the collector-base voltage has to be higher than zero for all transistors. Here the collector-base voltage of the transistor $Q_1$ is the critical one.

$$V_{\mathrm{CB}}^{Q_1} = -0.6\,\mathrm{V} - V_{\mathrm{CB}}^{Q_4}$$

$$V_{\mathrm{CE}}^{Q_4} = V_{\mathrm{E}} + 0.6\,\mathrm{V} - V_{\mathrm{M}}$$

where $V_M$ is the bias voltage applied to the emitters of the current mirror.

$$V_{\mathrm{CB}}^{Q_4} = V_{\mathrm{CE}}^{Q_4} + 0.6\,\mathrm{V} = V_{\mathrm{E}} + 1.2\,\mathrm{V} - V_{\mathrm{M}}$$

By replacing the expression for $V_{\mathrm{CB}}^{Q_4}$ into that of $V_{\mathrm{CB}}^{Q_1}$ one finds:

$$V_{\mathrm{CB}}^{Q_1} = V_{\mathrm{M}} - V_{\mathrm{E}} - 1.8\,\mathrm{V}$$

If we want this to be higher than zero:

$$V_{\mathrm{M}} > V_{\mathrm{E}} + 1.8\,\mathrm{V}$$

$\boxed{V_{\mathrm{M}} = V_{\mathrm{E}} + 2\,\mathrm{V} \text{ is a quite safe value}}$