University of Canterbury

Power Electronics 1

ENEL371 - The Solar Car

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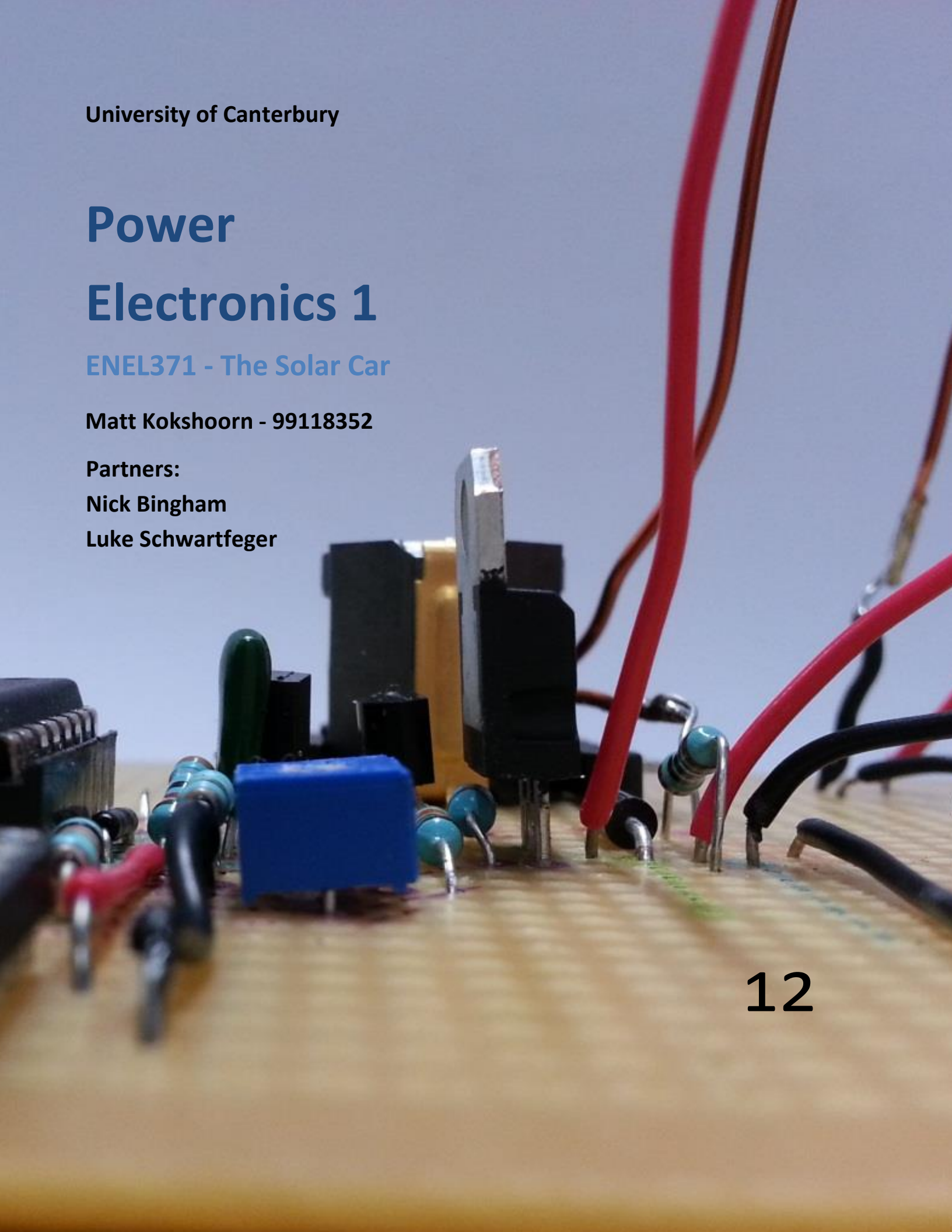

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Abstract

The aim of this project was interface a 10W Solar Panel with a low voltage DC Motor. Simply connecting the two will not work as the voltage and current characteristics do not meet the motor requirements. This system was implemented by means of a buck convertor and successfully achieved an efficiency of 82.6%. This report details the design process that has been undertaken to realize this buck convertor and the theory behind its operation.

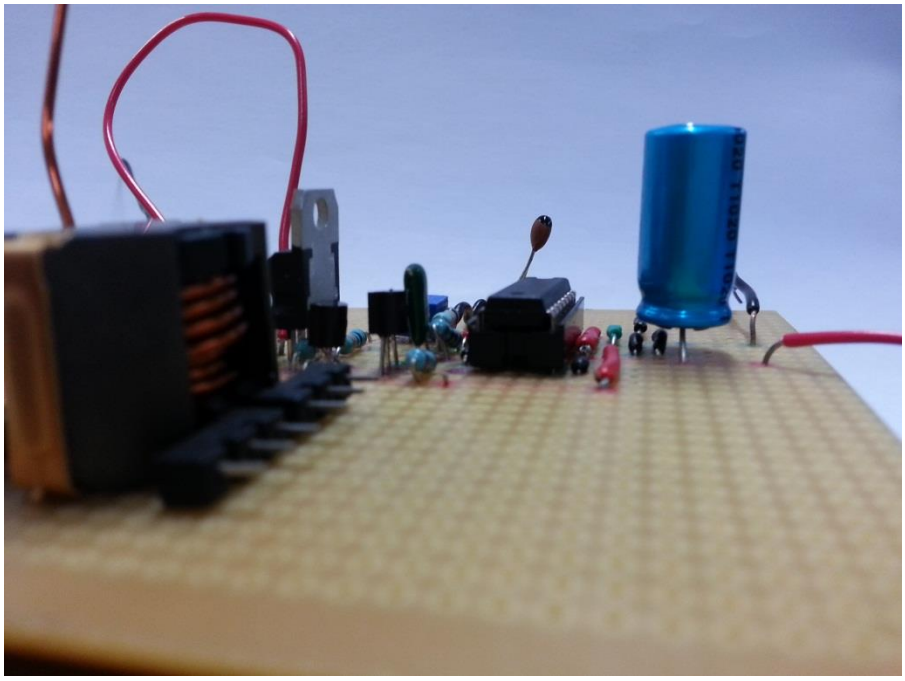

Figure 1 - Complete Buck Convertor Implementation

Contents

1) Introduction

The aim of this project was to develop the power electronics circuitry required for a model solar car. This involved the use a 10 Watt solar panel to run a small DC motor. Although the solar panel supplies sufficient power to run the motor, even at sub optimal levels of sunlight, simply connecting the motor to the panel will not subdue. This is because of the voltage and current characteristics of the 10 Watt supply. This supply is typically 15V with current of 0.3A. The motor requires specific voltage and current characteristics differing for startup and operation these are 2.5V at 1.7A and 1.6V respectively. To achieve this, the voltage from the panel must be stepped down.

In order to do this in a way that achieves a high efficiency and conserves power, the voltage needs to be stepped down using reactive components that do not dissipate energy. This allows power to be conserved by Equation 1 below. By this law, stepping down the voltage will cause the current to be stepped up. To realize this conversion, a power electronics circuit known as buck convertor must be utilized.

$$P = I\,V$$

Equation 1

To complicate things further, the voltage and current produced from the solar panel is not a set value and will instead fluctuate with changing light and load conditions. In order to maintain the desired output, an appropriate control mechanism will need to be employed to adjust the pulse width modulation (PWM) signal used in the buck convertor.

2) Theory

To successfully design an effective circuit for this project, the theory behind each module/component must be carefully considered.

a) Solar Panel

The panel used is a SOLAREX MSX-10 photovoltaic module. It is designed for DC loads with low energy requirements.

Technical Information

The PV module is described to generate direct current with a peak supply of 10 Watts. This power is described to be at a peak voltage and current of 17.5V at 0.57A respectively.

IV Characteristics

The module IV characteristics as described by the data sheet can be seen below in Figure 2

PV Characteristics

The PV characteristics of the panel are shown below in Figure 2.The MPPT (maximum power point) corresponds to the optimum operating region of the panel.

Temperature

It is also noteworthy that these values are subject to change with temperature as can be seen in Figure 2 .This effect is quantized have an approximate $-0.37\%/\ C^0$ effect on efficiency.

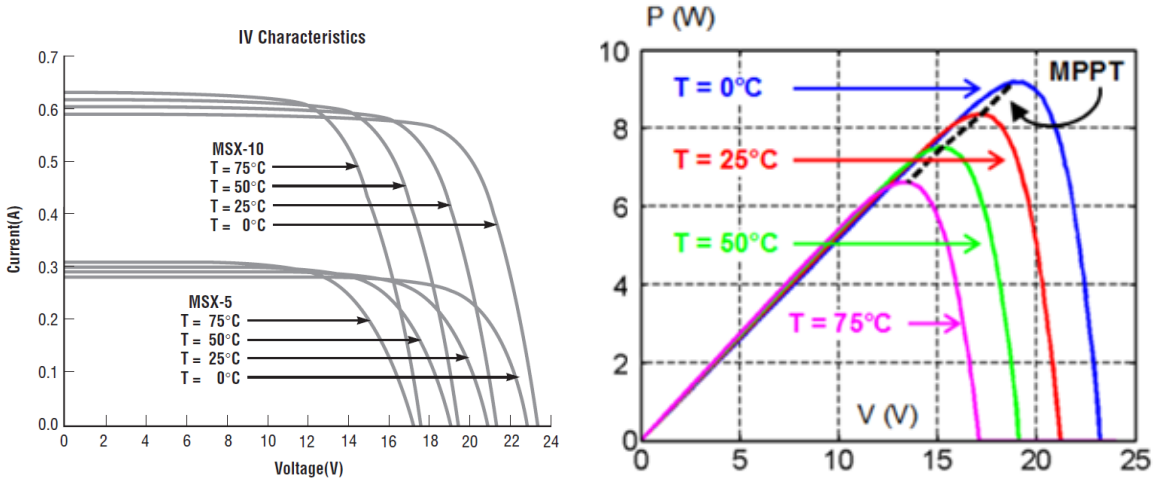

Figure 2 - Data Sheet IV Characteristics [1] (Left) and PV Characteristics (Right) of the SOLAREX MSX-10

b) DC Motor Model

The motor being used is a 15800rpm, 4.5-15V, DC permanent magnet motor. The motor will experience a larger mechanical load as it starts compared to once it is running. As result this will cause differing IV characteristics for each mode of operation. The motor requires current characteristics are as follows [2];

$$I_{Motor\ Starting} = 1.7A$$

$$I_{Motor\ Running} = 1.1A$$

c) Buck Converter

A buck convertor is to be used to achieve the required voltages and currents for the DC motor. A simple buck convertor circuit is shown below in Figure 3. A buck convertor is a step down convertor that typically boasts high efficiencies around 85% to 95%%. As a result of this voltage step down, the current is stepped up. The switching mechanism that controls the two paths of conduction is typically done by use of a power transistor and diode pair. The circuit operates in two modes of conduction known as the ON state and the OFF state. These states and their behaviour are explained on the following page in Figure 4 and Figure 5.

The buck convertor relies on the switching between two conduction states. The percentage of time the circuit spends in the ON state is known as the duty cycle and can be represented by k. Lower values of k correspond to having a reduced ON time with respect to the off time and thus a lower output voltage.

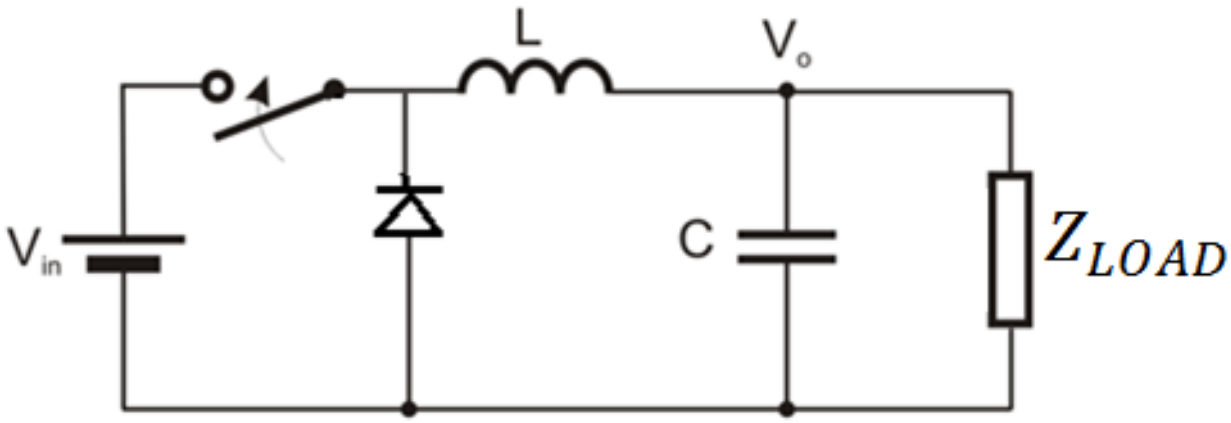

Figure 3 – Basic Buck Convertor Circuit

The On State

When the switch is closed the convertor is operating in the ON state, when this occurs current begins to ramp up through the inductor as the diode is reverse biased and is therefore non conducting. This can be seen below in Figure 4.

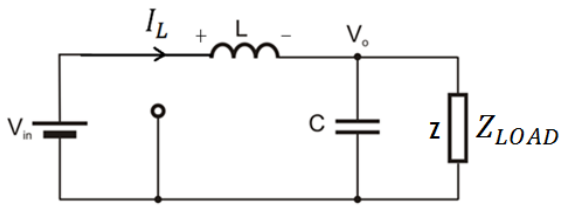

Figure 4 - Buck Convertor in ON State.

The inductor produces a voltage to oppose this change (assuming high inductance and switching frequency). Current flowing into the inductor as it opposes the current is stored in the form of a magnetic field during the ON state. The voltage over the inductor during this time can be described by Equation 2 below.

$$\boldsymbol{V_L = V_s - V_{Load} = L\frac{di}{dt}}$$

Equation 2

The Off State

When the switch is opened the convertor enters the off state and the diode become forward biased as can be seen in below in Figure 5. The energy previously stored in the inductor core is now used to continue driving current through the load. As the convertor remains in this state, the current/voltage slowly decreases as the energy supplied by the inductor is dissipated.

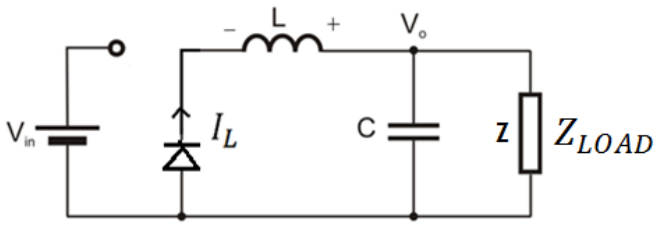

Figure 5 - Buck Convertor in OFF State

The voltage across the inductor in the OFF state can be described by Equation 3 below.

$$\boldsymbol{V_L = -V_{Load} = L\frac{di}{dt}}$$

Equation 3

In both the on and off state the capacitor is used to smooth the voltage on the load.

d) Power MOSFER and Gate Driver

The switching mechanism of the buck convertor previously described is required to be implemented using a STP22NF03L N - Channel power MOSFET. This is a gate voltage controlled component that is rated for a drain current of up to 22A [3].

In order to achieve a prompt switching response a gate driving circuit is also required. This is due to capacitive nature of the MOSFET gate causing V_{gs} to remain high for longer than required. Therefore the gate driving circuit needs to provide both a charging path from the supply voltage and a discharge path to ground. This will allow the MOSFET to switch on and off with minimal losses and delay [4] .

e) PWM

The duty cycle used to control the gate driver circuit and ultimately the buck convertor switching mechanism can be realized using PWM (pulse width modulation). The PWM signal is required to be generated using the Texas Instruments TL494 integrated circuit. The TL494 internal operation uses two locally generated signals that are compared to produce the PWM signal as can be seen below in Figure 6.

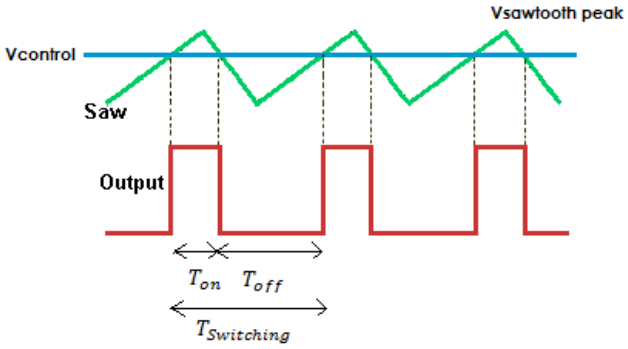

Figure 6 - PWM Generation Waveforms

The first of these is a high frequency saw tooth signal, $V_{sawtooth}$, and is essentially fed into the negative terminal of a comparator. This signal frequency corresponds to the PWM "switching frequency". The second signal, $V_{control}$, is a fraction of the locally generated 5V reference voltage. Feeding this into the positive terminal of the comparator causes it to be compared to the saw tooth signal and an output PWM signal produced. The duty cycle of this PWM signal, k , is then the amount of time the saw tooth signal spends greater than the reference voltage described below by Equation 4.

$$k = \frac{V_{control}}{V_{sawtooth\,Peak}} = \frac{T_{on}}{T_{on} + T_{off}} \,, 0 \leq k \leq 1$$

Equation 4

f) Control Circuit

In order to achieve the desired output voltage and current from the changing solar panel supply, the duty cycle of the PWM (determined by $V_{control}$) will need to change accordingly. To do this an appropriate control strategy must be implemented. This can be done using the TL494's built in error amplifier that operates as an integrator. The integrator takes the desired output voltage into the positive terminal and output load voltage into the negative terminal as shown below in Figure 7. The error between the two will accumulate and force the duty cycle to increase/decrease accordingly to minimize the error.

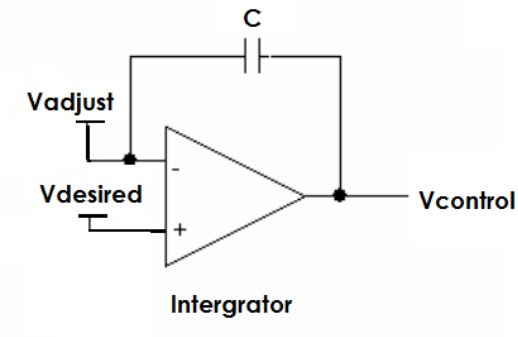

Figure 7 - Integrator Control Method

This concept can be extended to take a portion of the solar panel voltage as opposed to the load voltage. By tuning the ratio of voltage from the supply being fed into the integrator, the maximum power point (MPP) of the panel can be found and tracked. If the supply voltage shifts away from this point, as the load draws too much or too little current and therefore changes the supply voltage, the integrator will begin to accumulate error. This is seen when the portion of the tuned supply voltage (Red dot on in Figure 8) drifts away from the desired voltage. This causes an appropriate increase or decrease duty cycle in order to shift the system back into the MPP. This would be seen below as the red dots moving back towards the green dot (MPP).

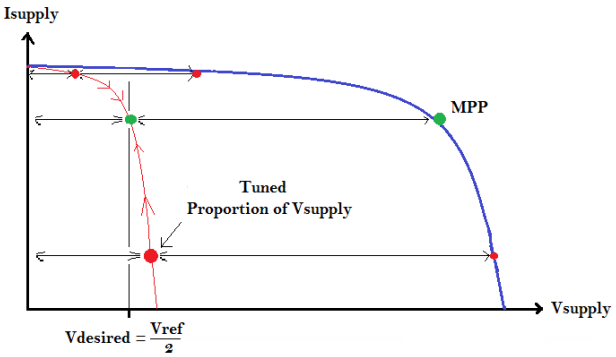

Figure 8 - Control Method to Keep Supply at MPP

3) Pre Design Testing

a) Solar Panel

To accurately design an effective power electronics module the current voltage and power characteristics of the solar panel were measured using an oscilloscope and a variable resistor. The results can be seen below in Figure 9.

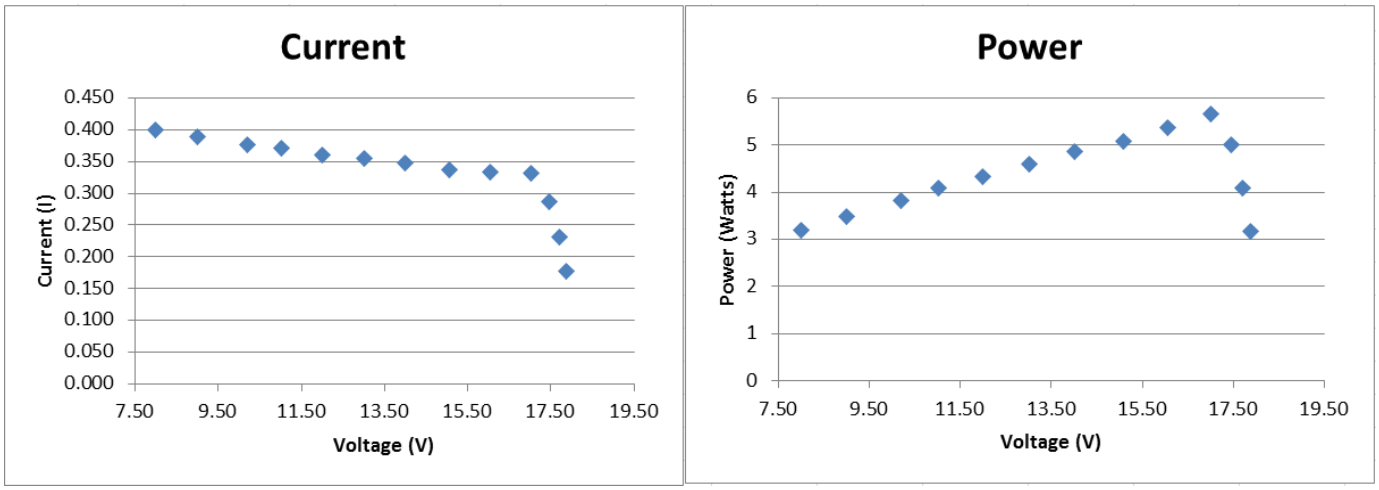

Figure 9 – Solar Panel IV Characteristics (Left) and Power Voltage Characteristics (Right)

The peak power can be observed to be approximately 6.75 W at a voltage of 17 V. This corresponds to a current of approximately 300mA.

b) Motor

Figure 10 shows the characteristics of the motor found by adjusting the voltage and observing the current.as would be expected power varies linearly with voltage increase.

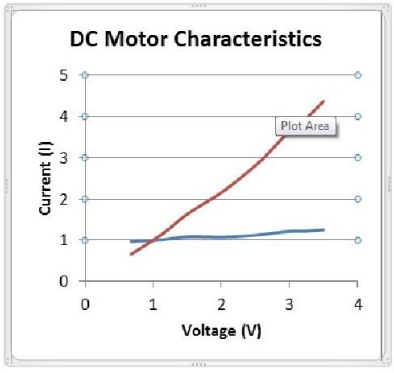

Figure 10 - DC Motor Characteristics, Current/Voltage (Blue) and Power (Red)

4) Design

The final convertor design comprises of three main circuit functional groups; the buck convertor itself, the gate driver and the PWM generation and control. To accurately assess the design, each circuit group must be considered.

a) Buck Convertor

The operation of the buck convertor is explained in Section 1)c). The buck convertor utilizes several components that contribute towards its functionality. The numerous design options that were considered when designing the buck convertor are described below.

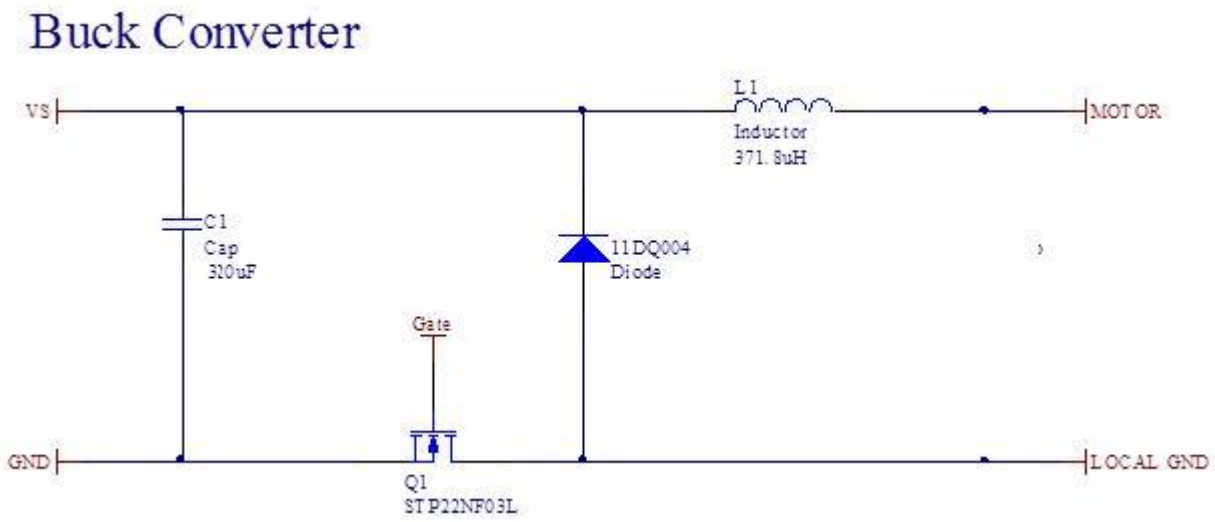

Figure 11 - Circuit Schematic of the Buck Convertor

Power MOSFET

As previously described the switching mechanism that was to be used was the STP22NF03L N - Channel power MOSFET. The design consideration surrounding this component was where to place it. The MOSFET can be placed between the capacitor and diode either on the positive rail or on the ground rail as can be seen above in Figure 11. In the end it was decided that is was best to place the MOSFET on the ground rail. This was selected as the MOSFET switching would depend on voltage to ground as opposed to being between the supply voltage and the gate. This will cause a more stable switching voltage as the ground reference is not going to change.

Inductor design

Ripple current, continuous/discontinuous conduction mode and inductor saturation are three important considerations that contribute to inductor design. The minimum inductance required to keep the buck convertor in continuous conduction mode can be found by considering the motor operating current of

1.1A at 2.5V. The minimum inductance can be described below in Equation 5 with $1mm^2$Copper winding used.

$$L_{min} = \frac{(1-k)V_O}{2f_S I_O} = 30.3\mu H$$

Equation 5

$$I_o = 1.1A\,, \quad V_o = 2.5V, \quad f_s = 32kHz, \quad k = \frac{2.5V}{15V} = 16.7\%$$

Current ripple is also a major consideration for inductor design. For our design it has been decided to limit current ripple to that below 20%, as this should be an acceptable level that does not impair motor operation. The minimum inductance required to do this can be calculated below using Equation 6.

$$\frac{I_{p-p}}{I_o} = \frac{V_O(1-k)}{I_o f_S L} = 0.2 \rightarrow \quad L_{\min} = \frac{V_O\,(1-k)}{0.2\,I_o f_S} = \ 295.8H$$

Equation 6

$$V_o = 2.5V, \quad f_s = 32kHz, \quad k = 16.7\%$$

The maximum inductance achievable with a specified core can also be determined below by Equation 7. This minimizes on weight from copper winding and thus reduces costs. This was not a particular issue for this project but is still a consideration.

$$L_{max} = \frac{NA_{core}B_{core}}{I_o}$$

Equation 7

The final inductance value was measure to be 371.8uH with 26 turns of copper windings. This was designed to be around 320 μH however when the core was clamped on it significantly increased the inductance by reducing the reluctance of the core's air gap. This was an acceptable increase as previous constraints on the inductor size have not been violated.

The final consideration of the inductor design was to then check that the core does not saturate. This can be calculated by Equation 8 below with further calculations in Appendix 3.

$$B_{peak} = \frac{\frac{\varphi_{ripple}}{2} + \varphi_{ave}}{A} \frac{\frac{(V_{panel} - V_O)k}{2Nf_S} + \frac{LI_O}{N}}{A} \ = \ 0.269\,T$$

Equation 8

The data sheet for the RM8/I core that was used requires a B_{peak} of less than 0.3 T. Therefore the inductor design upholds to the all constraints that have been discussed.

Freewheeling Diode

The freewheeling diode selected is 11DQ03. This diode has a low forward bias drop of 0.55V which aides efficiency. Additionally the diode has a reverse bias voltage of 30 V which is more than adequate to prevent conduction in the opposite direction. The alternative to a freewheeling diode would have been to use a second MOSFET running complimentary to the first. This would require extra protection to ensure that there is dead time between the two transistors and no shoot through current occurs as result of both being on at the same time. This would damage components and thus it was decided that the low loss characteristics of the 11DQ03 were suitable for this application.

Capacitor

No capacitor is required over the load as the switching frequency is significantly larger than the mechanical frequency of the motor. The DC motor will resulting still operate with ripple voltage. One of the circuit constraints is to keep the total capacitance of the circuit below 350 μF. By eliminating this need for this load capacitance, a large portion of the remaining capacitance can be placed over the supply to decouple noise and provide a more stable voltage.

b) Gate Driver

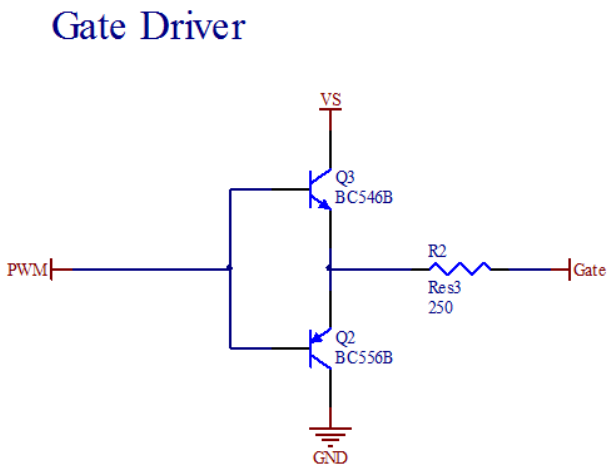

Figure 12 - Circuit Schematic of the Gate Driver

Operation

The circuit shown above in Figure 12 is known as totem pole gate driver. The two BJT's have maximum emitter currents of 100mA. When the PWM signal is low, the lower BJT and current is allowed to flow from the MOSFET gate through the resistor to ground. This decreases V_{gs} and therefore turns the N-MOSFET off. When the PWM signal is high, the upper BJT is switched on and current is allowed to flow into the MOSFET gate. This increases V_{gs} and therefore turns the N-MOSFET on. It is important to note that the two BJTs are complimentary and therefore are never simultaneously on.

Current Limiting Resistor

To ensure that the currents through the BJT's do not exceed the maximum emitter current of 100mA a 250 Ω resistor is placed on the input to the MOSFET. This caters for the highest supply voltage that could potentially occur of 21.4V limiting the maximum current to,

$$\frac{21.4V}{250\Omega} = 85.6mA$$

c) PWM Generation and Control Circuit

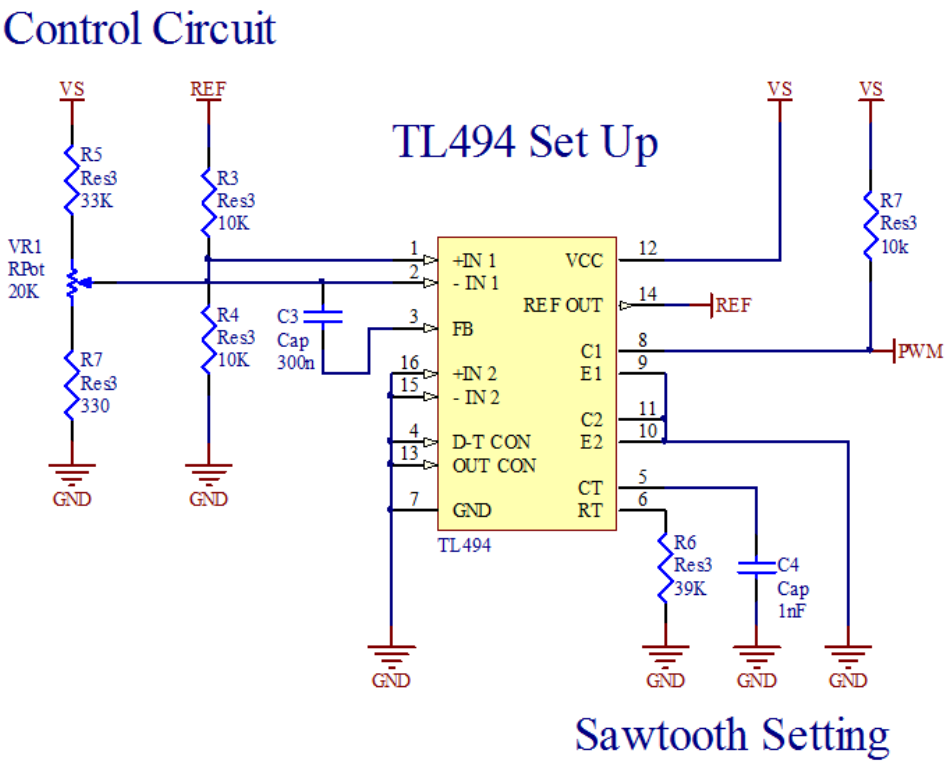

Figure 13 - Circuit Schematic of the PWM Generation and Control

PWM Signal

The PWM signal is generated using Texas Instrument's TL494 pulse width modulation control circuit. The operation of the PWM generation explained in section 1)e). The saw tooth frequency, f_s , is defined by the resistor R6 and the capacitor C4 shown above in Figure 13. The switching frequency was set to 32 kHz by setting the resistor to $39k\Omega$ and the capacitor to 1nF. These values were determined by use of the graph in Appendix 2.

The switching frequency had to be above 12.5 kHz, for the selected inductance; otherwise it would shift the inductor into saturation due to Equation 8. Therefore 32 kHz was selected as it is high enough to keep the inductor flux well below the 0.3 T thresholds.

The resistor R7 has been selected to limit current into the collector of the BJT within the TL494. The collector current needs to be below 200mA however should be lowered further to reduce losses. Therefore a $5k\Omega$ resistor is used to limit the current to 4.2mA.

The control circuit

The control circuit operation is explained in section 1)f) . The design consists of a 2.5V voltage being fed into the integrator positive terminal, a portion of the solar panel voltage being fed into the negative terminal and a feedback capacitor to define the integrating period.

The 2.5V control voltage is achieved by using two equally sized transistors in a voltage divider arrangement. This line to ground needed to be high resistance in order to limit current, therefore two $10k\Omega$ reisstors were used. This limits the current to be 0.25mA.

The portion of the supply voltage being fed into the negative terminal is achieved by R5, R7 and VR1. This resistor/variable resistor combination gives a range of possible voltages at the negative terminal given by Equation 9 below. This range was selected as, given a 15V supply voltage, it allows a voltage range from 5.7 V down to nearly 90mV. This gives a good variation that will allow the system to easily be tuned to the correct divider combination explained in section 1)f).

$$V_{negative} = [0.381, 0.006]\, V_s$$

Equation 9

These resistors also contribute towards the integrating time of the integrator given by Equation 10 below. The integrating frequency was required to be a factor of 100 times lower than the switching frequency, therefore should be approximately 320Hz or a time of 0.0003125 s. The resistance seen by the integrator is the Thevenin equivalent that ranges from 327Ω to $12k\Omega$. If we want an average time constant of 0.0003125 s we can use the average resistance. Thus the feedback capacitance can be calculated by,

$$\tau = RC$$

Equation 10

$$C = \frac{\tau}{R} = \frac{0.0003125}{6.453k\Omega} = 48.4\ \text{nF}$$

Equation 11

The remaining pins on the TL494 for were not used and therefore were grounded.

5) Simulations and Testing Results

To understand the characteristics and operation of the buck convertor several waveforms have been examined below. Overall our buck convertor has achieved an efficiency of 82.6%. The completed circuit can be seen below in Figure 14.

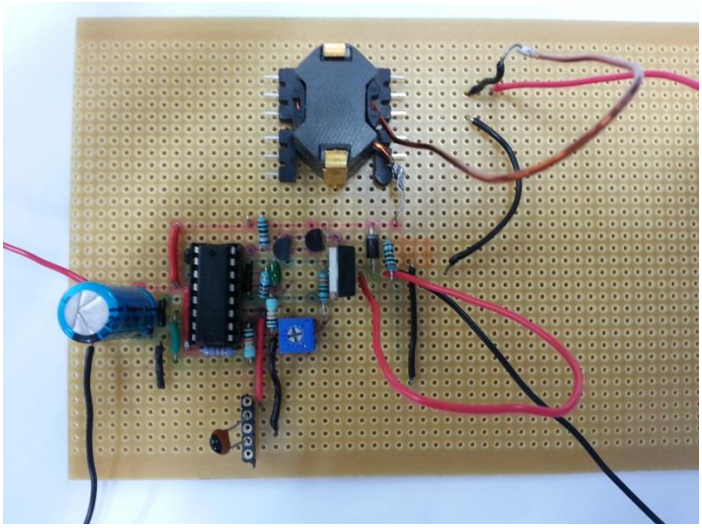

Figure 14 - Completed Buck Convertor Design on Vero Board

a) Saw tooth Waveform

Figure 15 shows the saw tooth waveform generated by the TL494 control chip. The signal was calculated to be 32 kHz which is very close to the actual reading of 32.2 kHz.

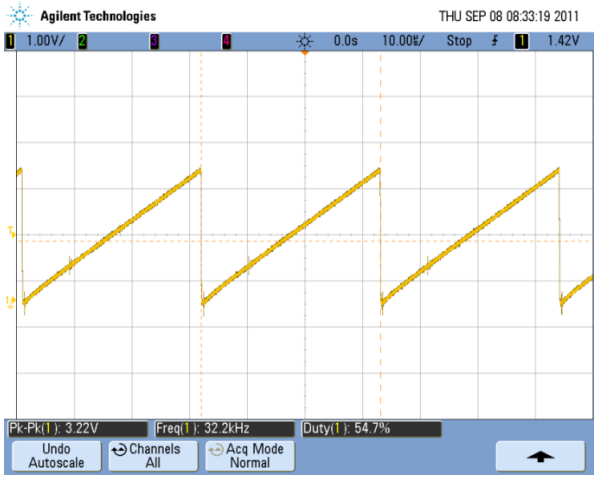

Figure 15 – Saw tooth Waveform Generated by TL494

b) PWM Waveform

Figure 16 shows the PWM waveform generated by the TL494 to be fed to the BJT gate driver network. As can be seen the frequency of the signal is 32.2 kHz, the same as the saw tooth waveform as is expected.

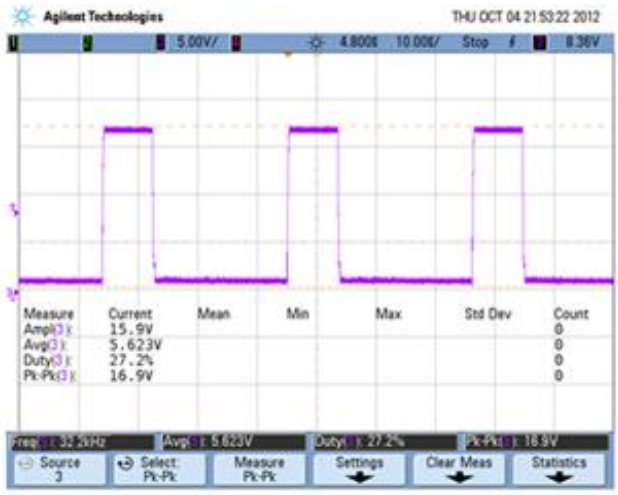

Figure 16 – PWM Waveform Output to Gate Drive

c) Voltage Ripple Waveform

Figure 17 shows the voltage ripple on the load. The ripple is very large however as discussed earlier, the electrical frequency is much higher than that of the mechanical load, so the voltage is not required to be smoothed.

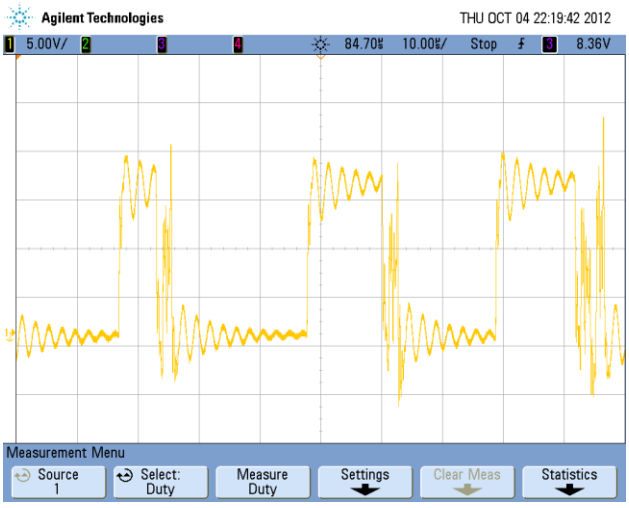

Figure 17 – Waveform Showing Voltage ripple on Load.

d) Current Ripple Waveform

Figure 18 shows the current through the inductor and the load. As can be seen as the buck convertor is supplying over 1A to the load from a 0.3A supply, meaning the buck convertor is operating correctly. The current ripple is measured to be 381mA. This corresponds to a ripple of 35%. This is significantly higher than our predicted 20%.

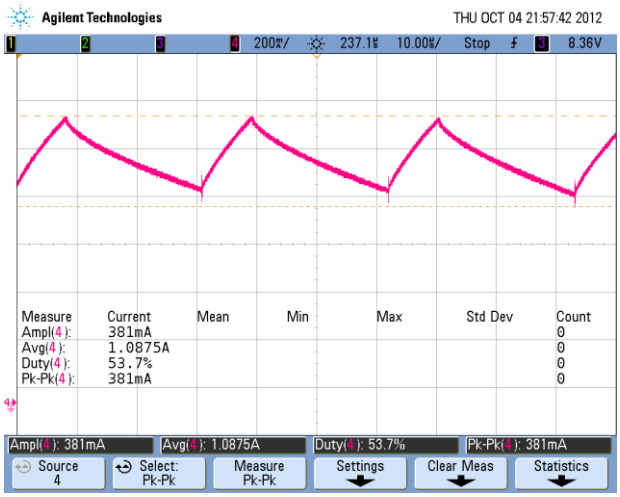

Figure 18 – Waveform Showing Inductor and Load Currents

e) Gate Voltage

Figure 19 shows the oscilloscope output of both the PWM waveform from the chip and the MOSFETS gate voltage. Without the gate driver one would expect that the gate voltage would slowly discharge as it has no immediate ground path. When the gate driver is implemented, the gate voltage can quickly discharge and therefore the MOSFET can quickly turn off.

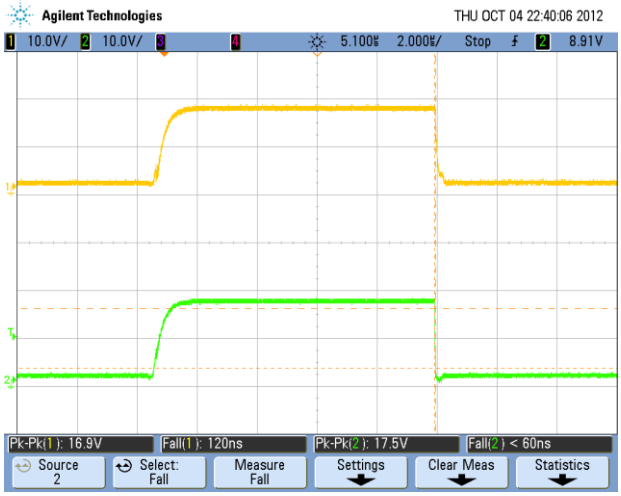

Figure 19 – Oscilloscope Capture of TL949 output (Bottom) and MOSFET gate voltage (top).

The capture above shows a significant improvement than when compared with that shown below in Figure 20 as a gate voltage without a gate driver.

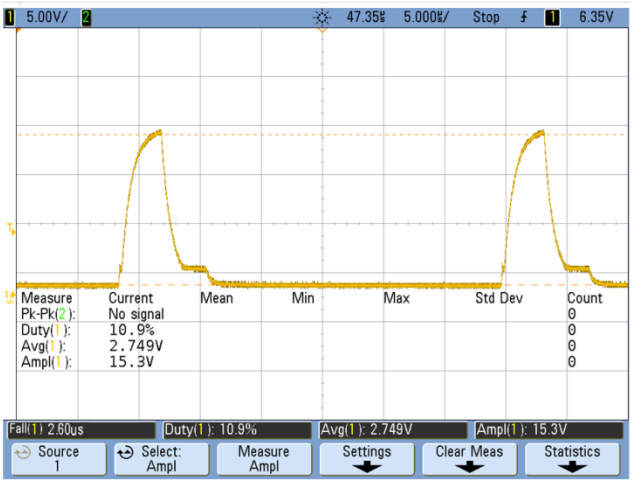

Figure 20 - Oscilloscope Capture of Gate Voltage without gate Driver Circuit

6) Discussion/Overall Operation

Overall the buck convertor operates successfully, however there are several areas that could be improved or are not operating as expected. These issues are discussed below.

Actual Operating Characteristics

The actual operating mode of the load when running at 82.6% efficiency is 4.25V at 0.81A. This differs from that expected of 1.1A at 2.4V. This is due to the load receiving 4W as opposed to the previously anticipated 3W.

Current Ripple

The current ripple is greater than the previously calculated 20% and instead 35%. This is due to the duty cycle and output voltage operating at higher values than predicted.

MPP Tuning

The tuning method for tracking the MPP works well once the point is found however finding this point can be a sensitive process. This could have been improved by reducing the voltage range in which the potentiometer outputs to the integrator. This would allow a more 'fine tuning' approach although would require consideration to over what voltage values this smaller range would lie.

Feedback Capacitor

The feedback capacitor for the integrator was calculated to be 48.4nF. In practice it was found that this capacitance was too large and as a result caused the system to responds too slowly. Instead a significantly different capacitor value of 2.2pF was found to be optimum for the design and therefore was used.

The reasoning behind why this value was so different is unclear. It is suspected that there could potentially be a fault somewhere in the circuit contributing to the integrating time constant either in terms of resistance or capacitance. This would cause the required capacitance to bring the time constant to 100 times greater than the switching period to differ from that calculated.

Resistor Changing

During the final stages of the design two resistors were changed that greatly increased the overall efficiency of the system. The first of these was the current limiting resistance from the gate driver into the gate of the MOSFET. This was originally planned to be $1k\Omega$. Upon closer inspection it was found that this was substantially increasing the time to complete transitional state change of the MOSFET. This contributed to losses as during this period the MOSFET is neither on nor off and instead is in the linear region, dissipating power as a resistor. By changing this resistor to 100Ω we greatly reduced the state changing time, and therefore increased the overall efficiency. Current limiting was not too much of an issue in this application as the current into the gate was over very short durations.

The second resistor that was changed was the current limiting resistor placed on the collector of the TL494, used to generate the PWM signal. This was originally 680Ω but was found to allow too much current being drawn from the panel and therefore reduced the efficiency. Since the only distinctive requirement of the minimum current allowed was the constraint that it still switches the gate driver BJT's, a large value of $10k\Omega$ was used to replace it.

The combination of these two resistor substitutions brought our system efficiency from 71.3% to our final value of 82.6%. This was a considerable efficiency increase that improved our overall design.

Non-inverting gate drive

A minor issue associated with the use of a non-inverting gate driver was identified that could be improved. This occurs in the non-inverting design as V_{BE} , and therefore the base current controlling the BJTs, is dependent on the voltage on the MOSFET gate. This voltage is subject to change and therefore it would be more beneficial to use the inverting design that utilises the supply and ground voltages as more stable references instead.

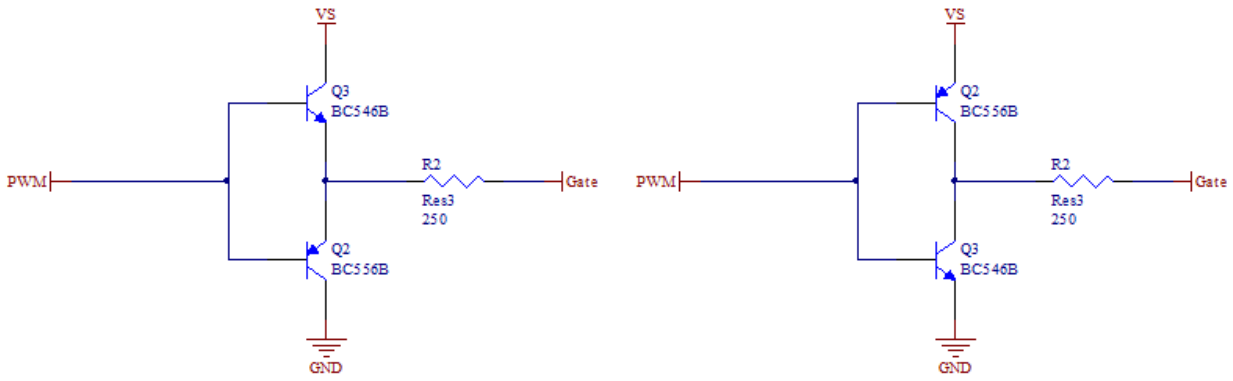

Figure 21 - Non-Inverting Gate Driver (Left) and Inverting Gate Driver (Right)

7) Conclusion

In conclusion we have produced buck convertor system that successfully powers the DC motor of a model solar car. The system is capable of running at a range of torques with varying input power. The ability to vary the operating point to the maximum power point allows the system to perform as required under a range of environmental lighting conditions.

Not every component usually included in a buck converter was needed for this application. The voltage smoothing capacitor was not included since the load was able to take small fluctuations in voltage without impeding performance. However, the inductor component which appears to be only a small part of the buck converter is quite vital. The design of this component itself had several sections which were not straight forward. The design is found to be 82.6% efficient when sourced by a supply of 15V.

8) Bibliography

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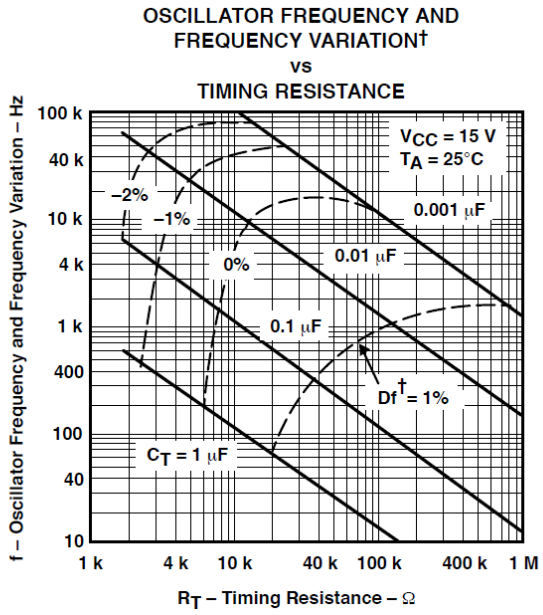
9) Appendix

Solar Panel Characteristics		
Voltage	Current	Power
8.00	0.399	3.192
9.01	0.388	3.49588
10.20	0.376	3.8352
11.02	0.371	4.08842
12.00	0.361	4.332
13.01	0.354	4.60554
14.00	0.347	4.858
15.07	0.337	5.07859
16.04	0.334	5.35736
17.01	0.332	5.64732
17.45	0.287	5.00815
17.70	0.231	4.0887
17.87	0.178	3.18086

Appendix 1 - Solar Panel Data



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Appendix 2 - Graph Used to Calculate f_s

$$B_{peak} = \frac{\frac{\varphi_{ripple}}{2} + \varphi_{ave}}{A}, \qquad \varphi_{ripple} = \frac{(V_{panel} - V_O)k}{N f_S}, \quad \varphi_{ave} = \frac{NI_O}{R} = \frac{LI_o}{N}$$

$$B_{peak} = \frac{\frac{(V_{panel} - V_O)k}{2N f_S} + \frac{LI_O}{N}}{A} = 0.269\,T$$

$$V_{panel} = 15V, \qquad V_o = 2.5V\,, \quad k = 16.7\%\,, \qquad I_o = 1.1A, \qquad f_s = 32kHz,$$
$$A = 6.3 \times 10^{-5}, \; N = 26\,, \qquad L = 371.8\mu H$$

Appendix 3 - Peak Flux Density Calculations