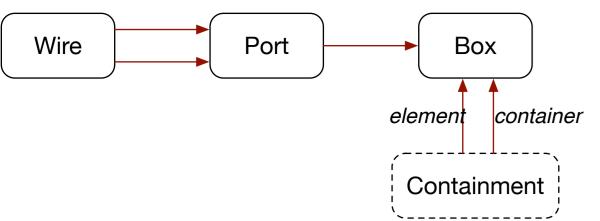
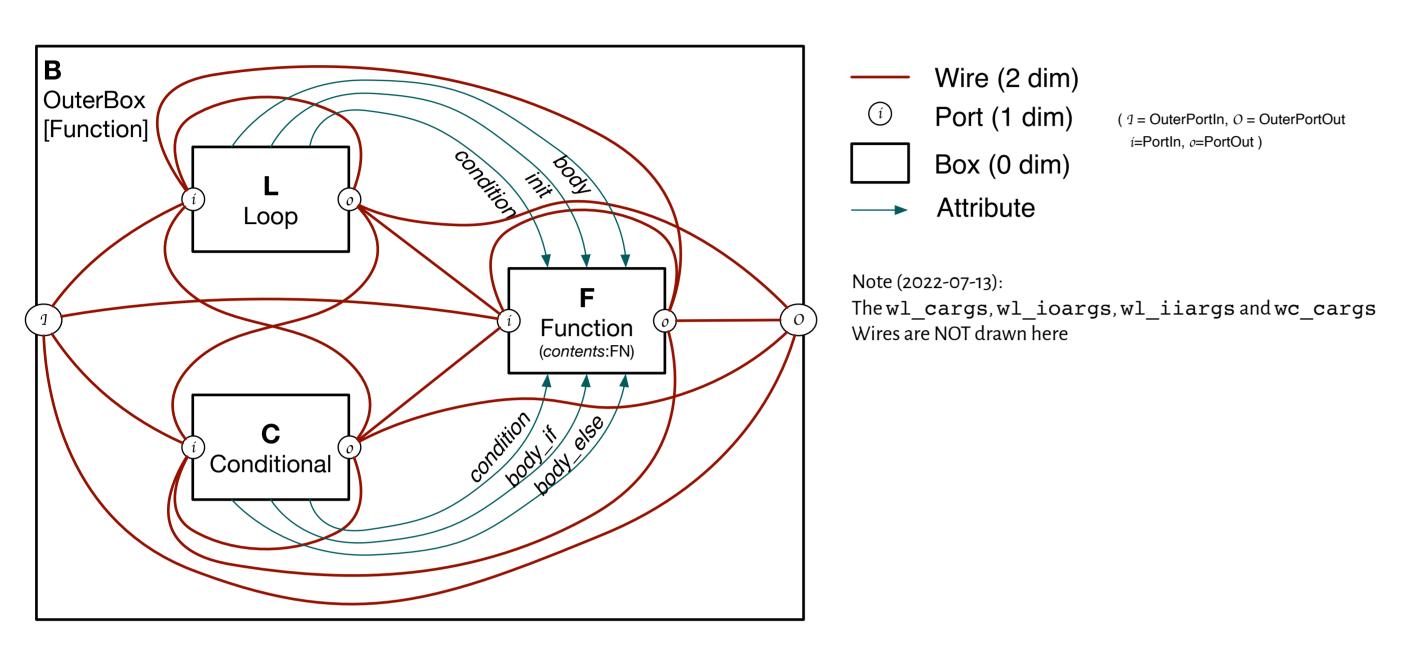
# GroMEt Base Schema G

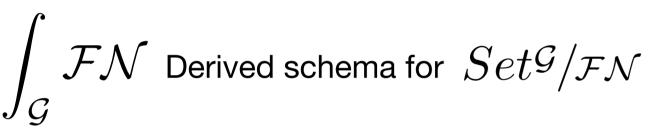


## GroMEt FunctionNetwork FN v0.1.1

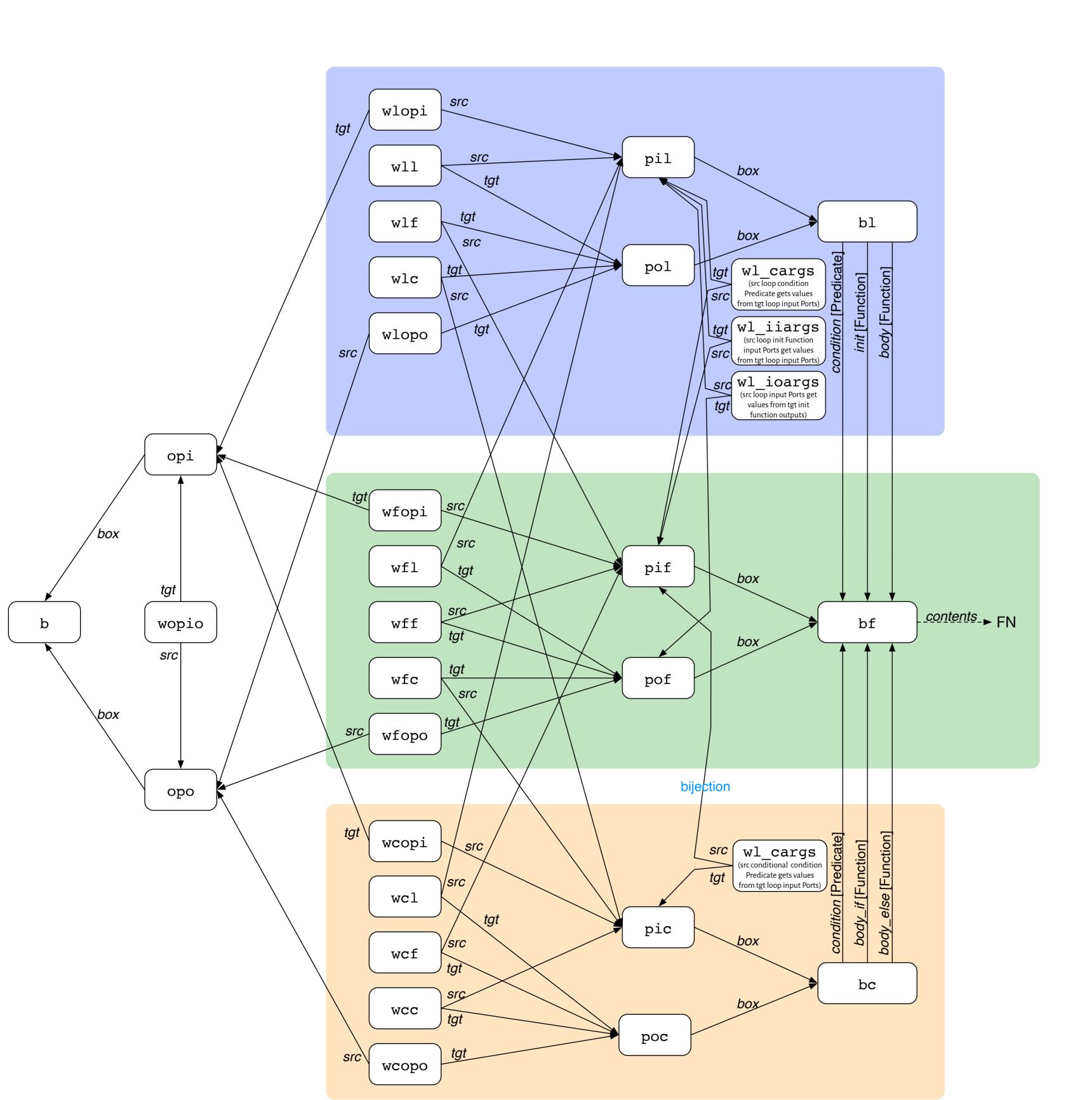
Instance of Base  $\mathcal{FN} \in Set^{\mathcal{G}}$ 

(Instance of Base Schema as a category-theoretic Wiring Diagram)





(Can be directly interpreted as an ER (Entity-Relation) database schema)



#### Box Types

Functions have their own hierarchy that will not be explicitly represented in the GroMEt export,

but instead represented by a function\_type (String) attribute associated with the Function Box.

The most general type is Function, which includes no constraints on number of input and output Ports.

When a box has FN contents, the Box type will be the type of the outer box of the FN.

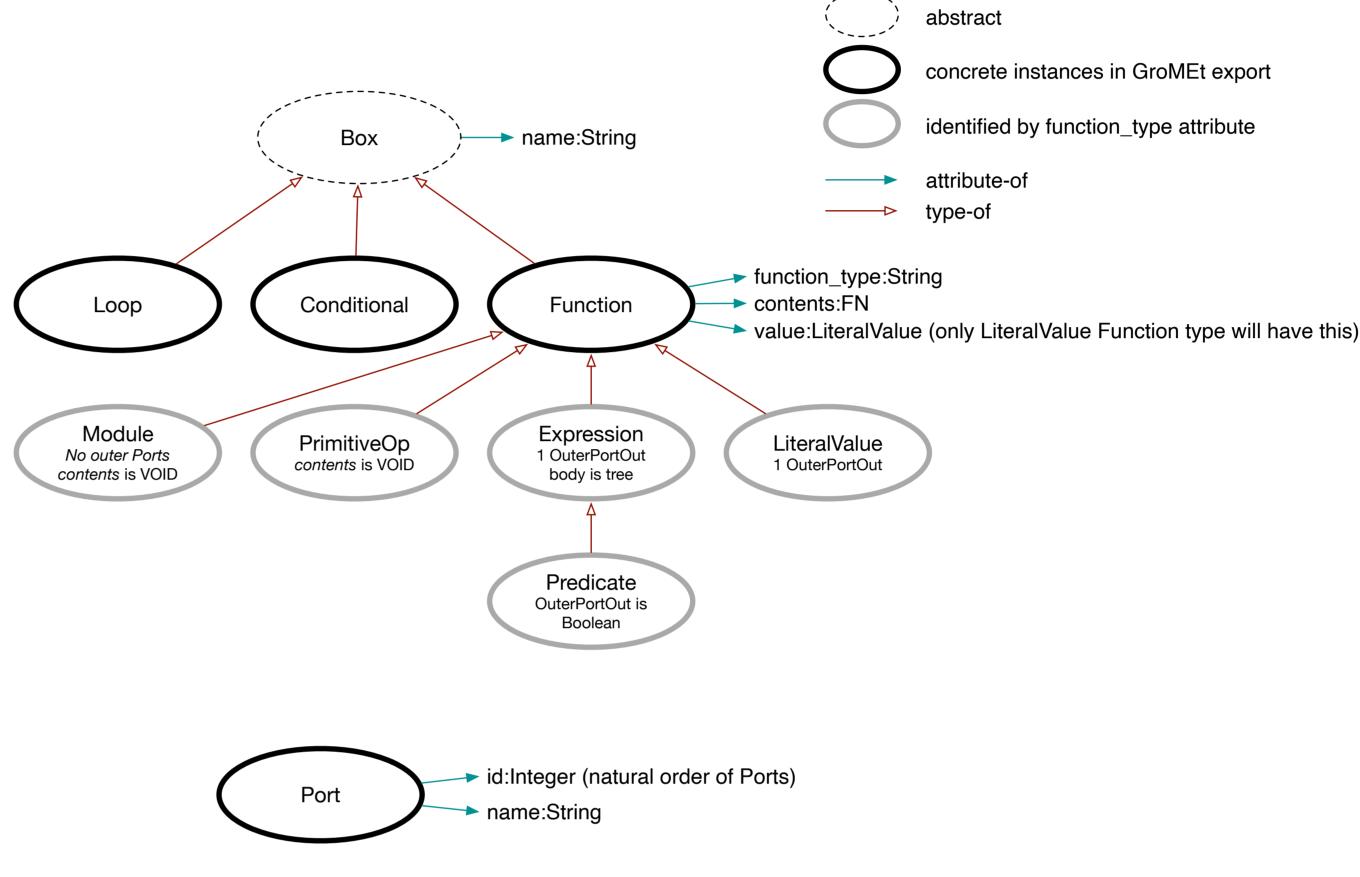
These structural constraints are not enforced by the schema but would need to be validated

These Box types will also have different attributes, as represented by the green arrows pointing at the attribute names:types.

The smaller text within the ovals describe some additional constraints imposed by a given type.

All child Box types inherit attributes of parents (even if hey don't use/fill them) as well as structural/contents constraints.

Module is special and only appears that the "top" level FN.



### Notes:

Naming Conventions: All type names start with their schema syntactic type:

op = OuterPort

opi = OuterPort Input Ports, opo = OuterPort Output Ports

p = Port

the next Port name letters:

i = in, o = out; followed by I = Loop, f = Function, c = Conditional

w = Wire

For 3-lettered Wire names, the last two letters are:

src -> tgt, with I = Loop, f = Function, c = Conditional b = Box

followed by I = Loop, f = Function, c = Conditional

#### Special Wire cases:

(1) wopio: Wire from OuterPortIn to OuterPortOut (i.e., passthrough)

(2) wl\_cargs and wc\_cargs represent a map (as Wires) from the arguments of the condition (cargs) Predicate (src) of the Loop or Conditional to the Portln's (tgt) of the Loop or Conditional Box.

Similarly, wl\_iiargs and wl\_ioargs represent a map from the input and output (respectively Ports of the loop init Function to the loop input Ports.

The background color patches group Ports, Wires and Boxes that are present depending on whether Function (green), Loop (blue) or Conditional (orange) is present.