4.4.3. CP15 c1 Control Register

Use the read/write Control Register to:

- prevent PC loads from changing the T bit
- select high-address or low-address vector locations
- enable the ITCM and DTCM
- select big-endian or little-endian operation
- enable the AHB write buffer
- enable fault checking of address alignment.

Access the Control Register with the instructions in Table 4.4.

Table 4.4. Control Register instructions

Instruction	Operation
`MRC p15, 0, <Rd>, c1, c0, 0`	Read Control Register
`MCR p15, 0, <Rd>, c1, c0, 0`	Write Control Register

Figure 4.4 shows the Control Register bit fields.

Figure 4.4. Control Register

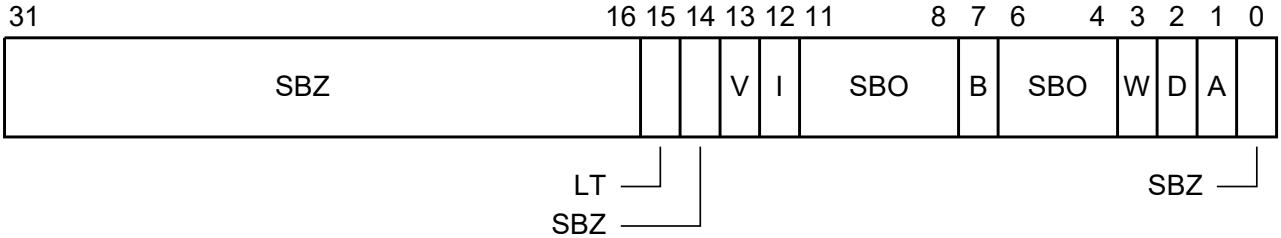

Table 4.5 describes the bit fields of the Control Register.

Table 4.5. Encoding of the Control Register

Bit	Name	Definition
[31:16]	-	Should Be Zero.
[15]	LT	Load Thumb disable bit: 1 = loading PC does not set T bit 0 = loading PC sets T bit. Reset clears the LT bit.
[14]	-	Should Be Zero.
[13]	V	Exception vector location bit: 1 = vector address range is `0xFFFF0000` to `0xFFFF001C` 0 = vector address range is `0x00000000` to `0x0000001C`. At Reset, the **VINITHI** pin determines the value of the V bit. You can write to V after Reset.

Bit	Name	Definition
[12]	I	ITCM enable bit: 1 = instruction accesses use ITCM interface 0 = instruction accesses use AHB interface. At Reset, the **INITRAM** pin determines the value of the I bit. You can write to I after Reset.
[11:8]	-	Should Be One.
[7]	B	Big-endian bit: 1 = big-endian memory mapping 0 = little-endian memory mapping. Reset clears the B bit.
[6:4]	-	Should Be One.
[3]	W	AHB write buffer enable bit: 1 = write buffer enabled 0 = write buffer disabled. Clearing the W bit causes AHB write buffer entries to complete as buffered writes. Reset clears W.
[2]	D	DTCM enable bit: 1 = data accesses use DTCM interface 0 = data accesses use AHB interface. At Reset, the **INITRAM** pin determines the value of the D bit.
[1]	A	Address alignment fault checking enable bit: 1 = fault checking of address alignment enabled 0 = fault checking of address alignment disabled. Reset clears the A bit.
[0]	-	Should Be Zero.