# **Michael Lerman**

2462 Booksin Ave, San Jose CA, 95125 408-564-9578 | michael\_lerman@yahoo.com

# SYSTEM ARCHITECT, INVENTOR OF NETMORY

#### **OBJECTIVE**

Seeking a role that can make a difference in the future.

My vision of the next generation computer and the internet, tells me that a revolution is around the corner. Computers will have an unlimited and persistent memory. These computers or devices will communicate faster. All this is achieved when those new computers consume only one fifth of the energy consumed in today's machines, and resulting in an amazingly longer battery life. I strongly believe that my invention NETMORY will reach this goal.

#### **EDUCATION**

# **Technion, Israel Institute of Technology**

Haifa, Israel

BSC - Bachelor of Science in Computer Engineering

#### **EXPERIENCE**

Xilinx San Jose , CA

Staff Debug/Diagnostic Engineer

2017-Now

Develop tools for debug and diagnosis of system function failures. Design and verification of DFx features with Vivado and Synopsys DVE on DSP device. Firmware DRAM memory and L2 cache test running out of On Chip Memory (OCM). Linux Shell Automation.

Milpitas, CA

Software Engineer - Senior

2014-2017

**Embedded Business Unit** 

SSD: developed tool based on a USB to SATA adapter using SCSI-ATA translation spec. Vendor specific accelerated command, firmware update, SSD performance. SD tool for measuring endurance, WAF (Write Amplification Factor) computed over the lifetime of the NAND device. SPI Secure Boot, ACRTM. Embedded Linux, Xilinx Zenq with the ARM Zedboard. Created a secure boot flow integrated in FSBL and Uboot. Created a tool for testing most secure features of an SPI device. Cryptographic hash mac, SHA256, key generation, root key, session key and digests. Linux Kernel: SPI protocol driver. Android with Snapdragon platform. Full Android build and ADB. BSP from Intrinsyc Open-Q 820.

INPHI Santa Clara, CA

Senior Staff Engineer

2013-2014

BIOS: Intel Memory Reference Code with AMI BIOS. DDR4, UEFI memory test, NVDIMM.

AMD Sunnyvale, CA

System Engineering - Manager

2000-2013

Bring up and validation. Developed JTAG based debug tools. Support Debug chipset debug features. EC (Embedded Controller) 8051 with the Keil RTOS and middleware. Supported ILA: an internal protocol analyzer for PCIe like bus.

**Hardware Debug Tools** 

#### **STMicroelectronics**

San Jose, CA

Manager System Solution

1994 - 2000

Managed a multi-disciplinary team. Developed hardware and software for a single chip PC & DVD device.

## **SKILLS**

# • Software development and hardware bring up

- x86 PC chipset system architecture
- o From the lowest level firmware and driver to the highest level Web UI
- o ARM: Xilinx Zynq embedded Linux with Zedboard
- Linux kernel and drivers (/dev/spidev and /dev/osal)
- UEFI x64 Shell application
- o Embedded firmware development for 8051 micro-controller with Keil
- o Scripting with various languages: Perl, Batch, PHP, Python
- C/C++/C# Visual Studio
- Windows and LINUX
- Timing Signal Analysis and Usage model
- Keysight LA and scope
- o LeCroy protocol analyzer for SATA/SAS, USB, and PCIe
- DDR3, DDR4, SPI, NAND, UFS, NVMe
- GIT and github

#### Full stack Web and Network development

- Frontend HTML, CSS, Javascript
- o Backend server side native CGI, PHP, Node.js
- o Databases: MySQL, SQlite, MSAccess.
- JAVA applet with JNI
- Socket network programming
- WAMP, LAMP
- PDF with TCPDF PDFTK
- Imaging with ImageMagick
- Data parsing, BNF, XML, XSLT, RegEx
- Graphing with D2, Chartis

#### Embedded

o Beaglebone, RaspberyPi, Freedom board, Zedboard

## Specialities

- o Nand SSD, Micro-SD
- NOR SPI
- Embedded Linux
- Secure boot
- JTAG
- Test automation
- Debug tools
- Web UI UX
- o Memory DRAM

#### PATENTS AND AWARDS

#### **Patents**

- NETMORY US9697114B2
  - A revolutionary new computer architecture for a non volatile and illimited system memory.
- SLEEP PROCESSOR: <u>US8683247B2</u>
  - Method and apparatus for controlling power supply to primary processor and portion of peripheral devices by controlling switches in a power/reset module embedded in secondary processor.
- AUTO-SLEEP ARRAY: <u>US8370669B2</u> MEMORY DEVICE HAVING A MEMORY SLEEP LOGIC AND METHODS THEREFORE.
- EASY FLASH: <u>US9870220B2</u>
  MEMORY FLASH APPARATUS AND METHOD FOR PROVIDING DEVICE UPGRADES OVER A STANDARD INTERFACE.

#### **Awards**

Spotlight Award on Aug 2010 for the outstanding contribution to the SB900 Bring up effort through the development of Register Explorer

### **OTHER**

## Languages

• French, English, Hebrew, Arabic

US and EU citizen