

# **FEATURES**

- eXpressDSP Digital Media (XDM IVIDDEC3) interface compliant.
- Validated on OMAP4 ES1.0 hardware platform
- VC1 Advanced Profile up to Level 3 is supported.
- Progressive, Interlaced field and Interlaced Frame types are supported
- Multiple slices decoding is supported
- Range reduction and Range mapping is supported
- Intensity compensations is supported
- Both RCV(RCV V1, RCV V2) and Elementary stream formats are supported
- Tested for compliance with VC1 SMPTE reference decoder version 7
- All features of Simple Profile, Main Profile and Advanced Profile are supported
- Supports all block type partitioned and prediction modes.
- Supports resolutions from all standard resolutions from QCIF to 1080p/1080i
- Picture width and height minimum 64x64 to maximum 1920x1088 pixel supported
- Performance measured for 1920x1088
  picture resolution for progressive as well
  interlace format in normal conditions means
  without erroneous conditions
- Supports YUV420 semi-planar Chroma format
- Supports multi-channel functionality

- Ability to plug in any multimedia frameworks (e.g. Codec engine, OpenMax, GStreamer etc)
- Independent of any Operating system (DSP/BIOS, Linux, windowCE, symbian etc)
- Error concealment is supported
- Graceful exit from codec under error conditions is supported
- · Cache aware decode library

## **DESCRIPTION**

VC1 is the Society of Motion Picture and Television Engineers (SMPTE) standardized video decoder.VC1 consists of three profiles namely, simple, main, and advanced. Simple and main profiles were developed for use in lower-bitrate networked computing environments. VC1 standard defines several profiles and levels that specify restrictions on the bit stream, and hence limits the capabilities needed to decode the bitstreams. This project is developed using Code Composer Studio version 4.2.0.09000 and code generation tools version 4.5.1.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners





# SPRS751- OCTOBER 2018

# **Performance Summary**

This section describes the performance of the VC1 Advanced Profile Decoder on IVAHD.

**Table 1. Configuration Table** 

CONFIGURATION	ID
VC1 Advanced profile level 0,1,2,3	VC1_DEC_001

Table 2. Cycles Information - Profiled on OMAP4 ES1.0 with Code Generation Tools 4.5.1

	PERFORMANCE STATISTICS (MEGA CYCLES PER SECOND) <sup>(1) (2)</sup>			
CONFIGURATION ID	TEST DESCRIPTION <sup>(3)</sup>	AVERAGE <sup>(4)</sup>	PEAK <sup>(5)</sup>	
	sa00040_progressive_frame_1920x1080_22mbps_30fps.vc1	222	226	
	sa00040_interlaced_frame_1920x1080_26mbps_30fps.vc1	211	222	
	sa00040_interlaced_field_1920x1080_27mbps_30fps.vc1	259	259	
VC1 DEC 001	SA20033_progressive_frame_1280x720_5mbps_IPP_30fps.vc1	105	112	
	SA10189_progressive_frame_720x480_3mbps_IPP_30fps.vc1			
		49	51	
	SA10210_interlaced_field_720x480_3mbps_IPP_30fps.vc1	61	61	
	tennis_p640x360_1mbps_IPPP_30fps.vc1	37	38	

- (1) Measured with OMAP4 ES1.0 having M3 @ 166 MHz, IVAHD @ 266 MHz and DDR @ 333 MHz. Also, M3 Code and codec Memtab request being in External Memory. All 2D image buffers of codec being in TILED\_8Bit Memory and Chroma 2D buffers of codec for YUV420 semi-planar output being in TILED\_16Bit Memory.
- (2) Peak MCPS measurements can vary by +/-5%. Peak is the maximum of first 30 frames.
- (3) Test cases have mixed variation and resolution as mentioned in test case name. Also, no latency from system process call and processing unit as frame (i.e., no sub-frame communication).
- (4) Based on average cycles for 1 second @ 30 fps.
- (5) Based on worst case cycles for high bit-rate frame decoding, in this scenario appropriate output buffering is required.

Table 3. Memory Statistics - Generated with Code Generation Tools Version 4.5.1

CONFIGURATION ID	RESOLUTION	PROGRAM DATA MEMORY TOTA				
					ТОТА	
			PERSISTENT	CONSTANT	STACK	L
VC1_DEC_001	1920 x 1088	14	16	595	2	627

<sup>&</sup>lt;sup>(1)</sup>All memory requirements are expressed in kilobytes (1K-byte = 1024 bytes).





SPRS751- OCTOBER 2018

### Table 4. Internal Data Memory Split-Up

	DATA MEMORY – INTERNAL <sup>(1)</sup>		
CONFIGURATION ID	SHARED		INSTANCE <sup>(2)</sup>
	CONSTANTS	SCRATCH	INSTANCE"
VC1_DEC_001	0	0	0

(1) I/O buffers are not included. Some of the instance memory buffers could be scratch.

#### **Notes**

- I/O buffers:
  - o Input buffer size = 2000 Kbytes (average case for a 1920x1088 picture resolution)
  - Output buffer size = 3800 Kbytes (average case for a 1920x1088 picture resolution)
- Total data memory for N non pre-emptive instances = Constants + Runtime Tables + Scratch + N \* (Instance + I/O buffers + Stack)
- Total data memory for N pre-emptive instances = Constants + Runtime Tables + N \* (Instance + I/O buffers + Stack + Scratch)
- Entire IVA-HD is considered as a resource for VC1 decoding process.

#### Reference

- SMPTE 421M VC1 compressed video bit-stream format and decoding process
- VC1 Advanced Profile Decoder on IVAHD User's Guide





SPRS751- OCTOBER 2018

# Glossary

TERM	DESCRIPTION
Constants	Elements that go into .const memory section
Scratch	Memory space that can be reused across different instances of the algorithm
Shared	Sum of Constants and Scratch
Instance	Persistent-memory that contains persistent information - allocated for each instance of the algorithm

# Acronyms

ACRONYM	DESCRIPTION
SMPTE	Society of motion picture and television engineering group
DCT	Discrete Cosine Transform
DSP	Digital Signal Processing
XDM	eXpressDSP Digital Media
HDTV	High Definition Television



#### IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications. Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have not been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of nondesignated products, TI will not be responsible for any failure to meet ISO/TS16949.

#### **Products**

Audio www.ti.com/audio **Amplifiers** amplifier.ti.com **Data Converters** dataconverter.ti.com **DLP® Products** www.dlp.com DSP dsp.ti.com Clocks and Timers www.ti.com/clocks Interface interface.ti.com Logic logic.ti.com Power Mgmt power.ti.com Microcontrollers microcontroller.ti.com www.ti-rfid.com www.ti.com/omap

**OMAP Applications Processors** Wireless Connectivity

### **Applications**

Automotive & Transportation www.ti.com/automotive Communications & Telecom Computers & Peripherals Consumer Electronics **Energy and Lighting** Industrial Medical Security Space, Avionics & Defense Video & Imaging

**TI E2E Community** www.ti.com/wirelessconnectivity

www.ti.com/communications www.ti.com/computers www.ti.com/consumer-apps www.ti.com/energyapps www.ti.com/industrial www.ti.com/medical www.ti.com/security

www.ti.com/space-avionics-defense www.ti.com/video

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright© 2014, Texas Instruments Incorporated