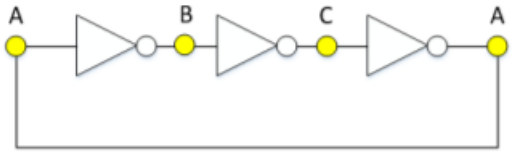
Experiment 1 – Clock and Periodic Signal Generation

Mohadeseh Azari,
810196404

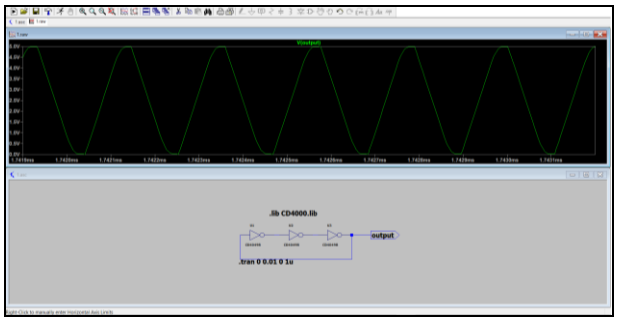
***Abstract*— part 1:one of the most important part in logic design is the clock. In this part we can see how to build a simple clock using not gate and to calculate the frequency of our clock; Also we learned about CD 4000 ICs and learn how to implement our circuits using Ltspice. Part 2: In this part we use our coding skills to build a clock in Verilog. As we've learned in previous part we can use a simple not gate to build our clock, so all we need to do is to see the digital output (not analogue) of the clock in ModelSim.part 3: In this part we will use Quartus components to synthesis our blocks with roughly close delays and use the ring oscillator and two counters to build a new clock (frequency divider). we will learn about 74 series ICs as well.**

***Keywords*— clock, frequency, delay**

I. RING OSCILLATOR

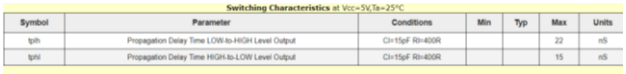


Ring Oscillator



Measuring the propagation delay

0.107µs (propagation delay)
2*Delay: propagation delay -> Delay: 17.834 ns



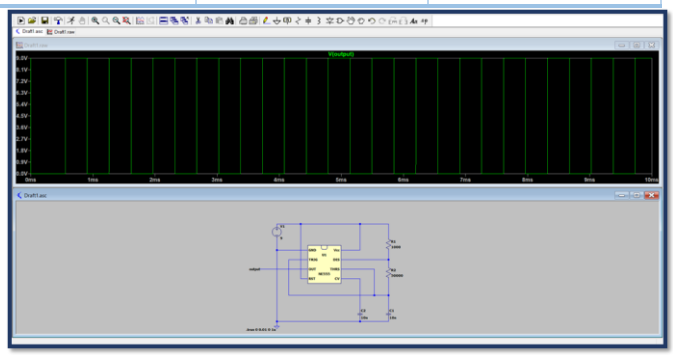
7404 TTL datasheet

Here we can see that 7404 datasheet delay is between (15,22) ns and our result is 17.834ns so it is roughly a good estimation.

II. LM555 TIMER

This IC has three mode

monostable	bistable	astable



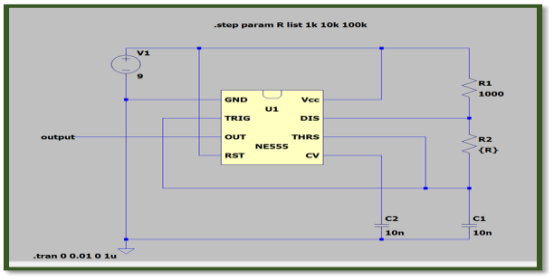
Since the 555 is running on 9V we are getting a square wave between 0 and 9 volts.

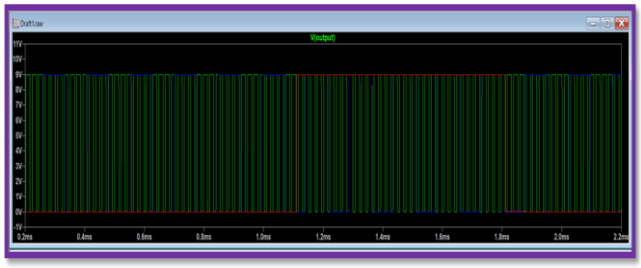
Calculation	Wave form
time period :0.6993ms	Time period:0.7ms
Frequency:1.430KHz	Frequency:1.4076KHz
Duty cycle:50.49%	Duty cycle:50%

$$T = 0{,}693 * (R_1 + 2R_2) * C$$

$$f = \frac{1}{T}$$

$$Duty\ cycle = \frac{R_1 + R_2}{R_1 + 2R_2}$$





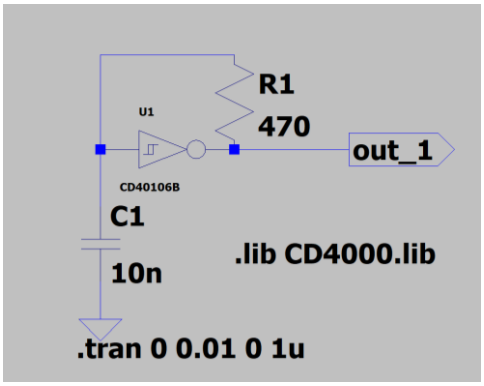
1Kohm	Calculation	Wave form
Period time	20.79µs	21.133µs
Frequency	48.10Khz	47.3177Khz
Duty cycle	0.67%	0.62%

10Kohm	Calculation	Wave form
Period time	145.53µs	146.83µs
Frequency	6.8714Khz	6.8103Khz
Duty cycle	52.38%	50%

100Kohm	Calculation	Wave form
Period time	1.3929ms	1.81ms
Frequency	717.911hz	552.4664hz
Duty cycle	50.24%	50%

The mathematical calculations have been attached to the file

III. Schmitt Trigger Oscillator



Schmitt inverter oscillator circuit

$$f = \frac{\alpha}{RC}$$

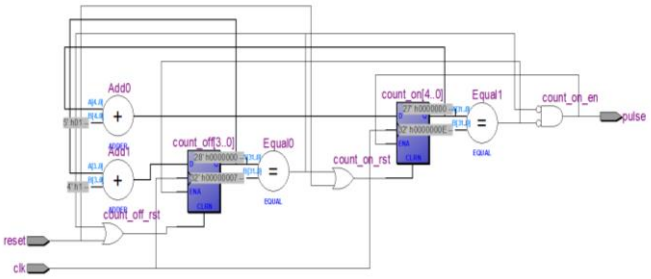
Resistance	**Frequency**	**Alfa**
470ohm	199.89Khz	0.9394
1Kohm	117.53Khz	1.1753
2.2Kohm	60.76Khz	1.3367

Mean = 1.15

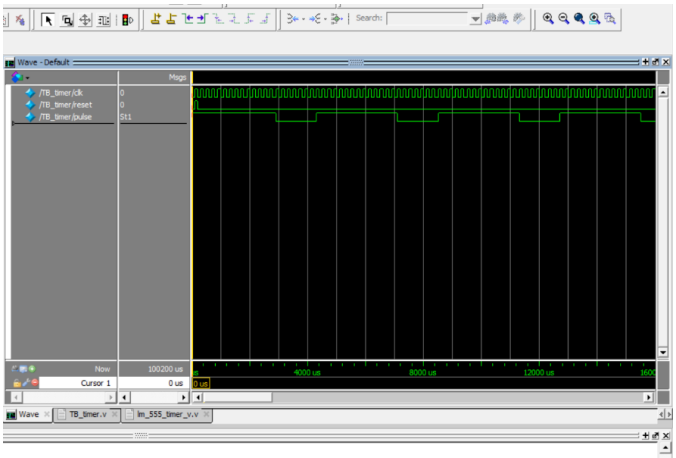
Alfa is a constant usually between 0.2-1

IV. Clock Generation using Verilog

The $clog2 function returns the ceiling of the logarithm to the base e (natural logarithm) rather than the ceiling of the logarithm to the base 2.



- First of all, it calculates the on duration and off duration based on their formula.
- After that we have to convert those values into binary.
- It continues to count up until this statement is true: ((count off! == off duration) & (count on! == on duration))
- If the count on en was 1 the pulse will rise and if the count off en is 1 the pulse will fall.
- If the reset was 1 the counter would restart the counting proses otherwise it would continue counting.

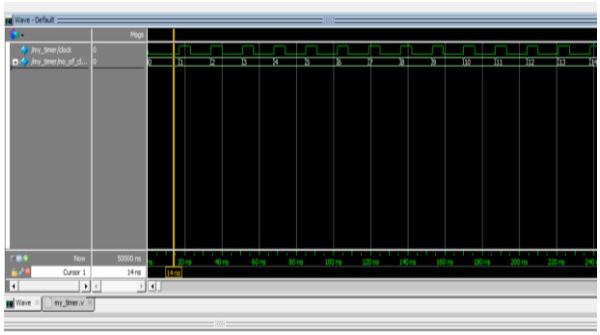


Resistance	Duty cycle(part2)	Part 1
1Kohm	65.43%	67%
10Kohm	52.71%	52.38%
100Kohm	50.25%	50.24%

Pulse_1 -> $\frac{2713}{4146}$ -> 65.43% duty cycle

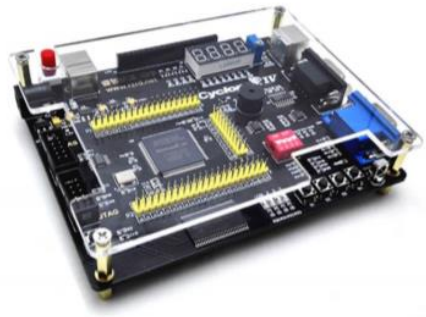
Pulse_10 -> $\frac{15361}{29138}$ -> 52.71% duty cycle

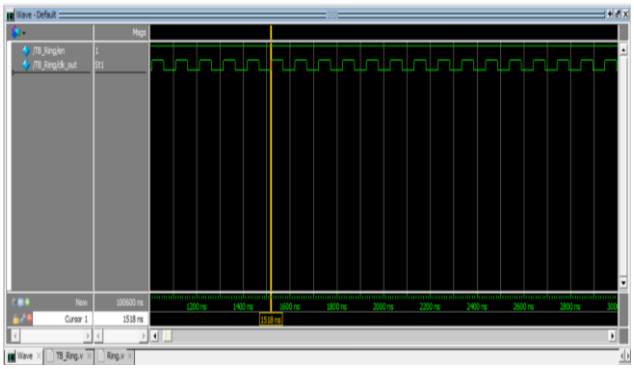
Pulse_100 -> $\frac{140000}{278600}$ -> 50.25% duty cycle



This is my timer with period time 17ns, 58.82 MHz is its frequency.

V. FPGA Design / Ring Oscillator

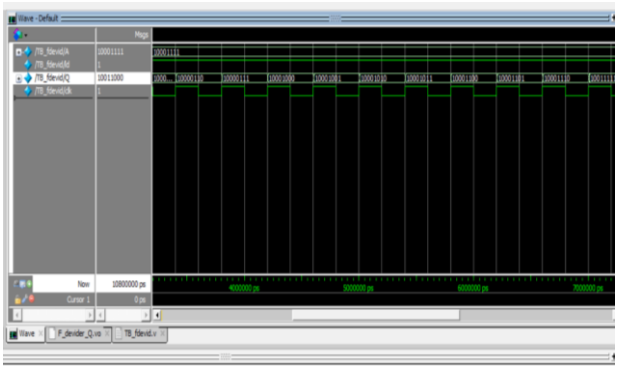




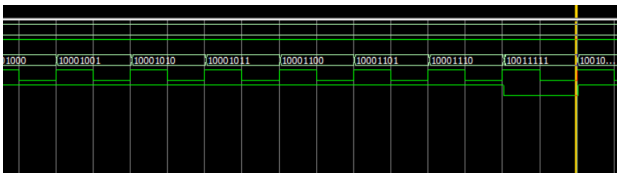
1415ns -> 1518ns: 103ns
Frequency: 9.7 MHz

My Verilog code give two parameters one for the number of inverter and the other one is the delay value of one inverter in ns.

VI. Synchronous Counter as Frequency Divider

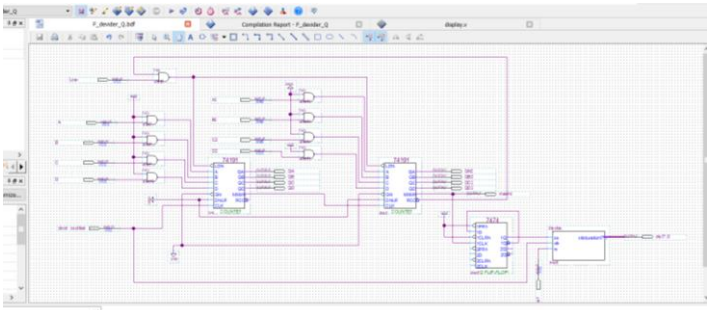


Frequency divider

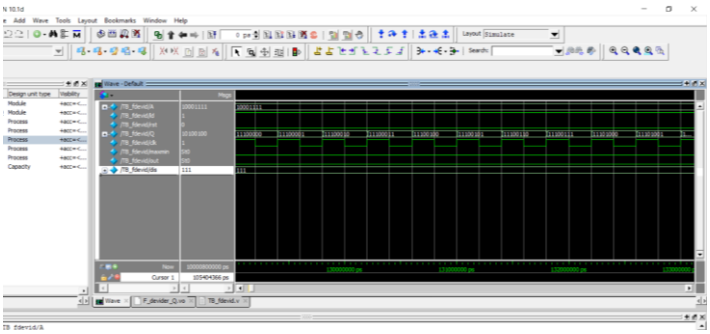


As a result, the frequency of frequency divider is less that the frequency of the Ring clock with the factor of 16.

VII. T Flip-Flop



Quartus design



Wave form

Here our duration is 111, so it means that it toggles 111 times and because our clock duration is 100000 ps or 100ns so its total duration will be 11100ns. so considering the frequency formula its frequency will be 90.09KHz and we know by using a frequency divider with initial value 113 so the remaining would be 143 (256). So the ring oscillator

frequency will be calculated to be 12.88 MHz and is roughly close to 9.7MHz.

VIII. CONCLUSION

we see in this lab that we can build clocks with different frequency and different duty cycle using lots of simple methods, using not gates, using timers, using frequency dividers. we can change their frequency, divide their frequency and easily used them as one of the most important parts in our logic design.