Monish Nene

ESD LAB2 Report

Things Learnt in Lab1

RS 232

Interrupts in MSP432 and 89C51

External and internal address Program memory access for 89C51

MAX232

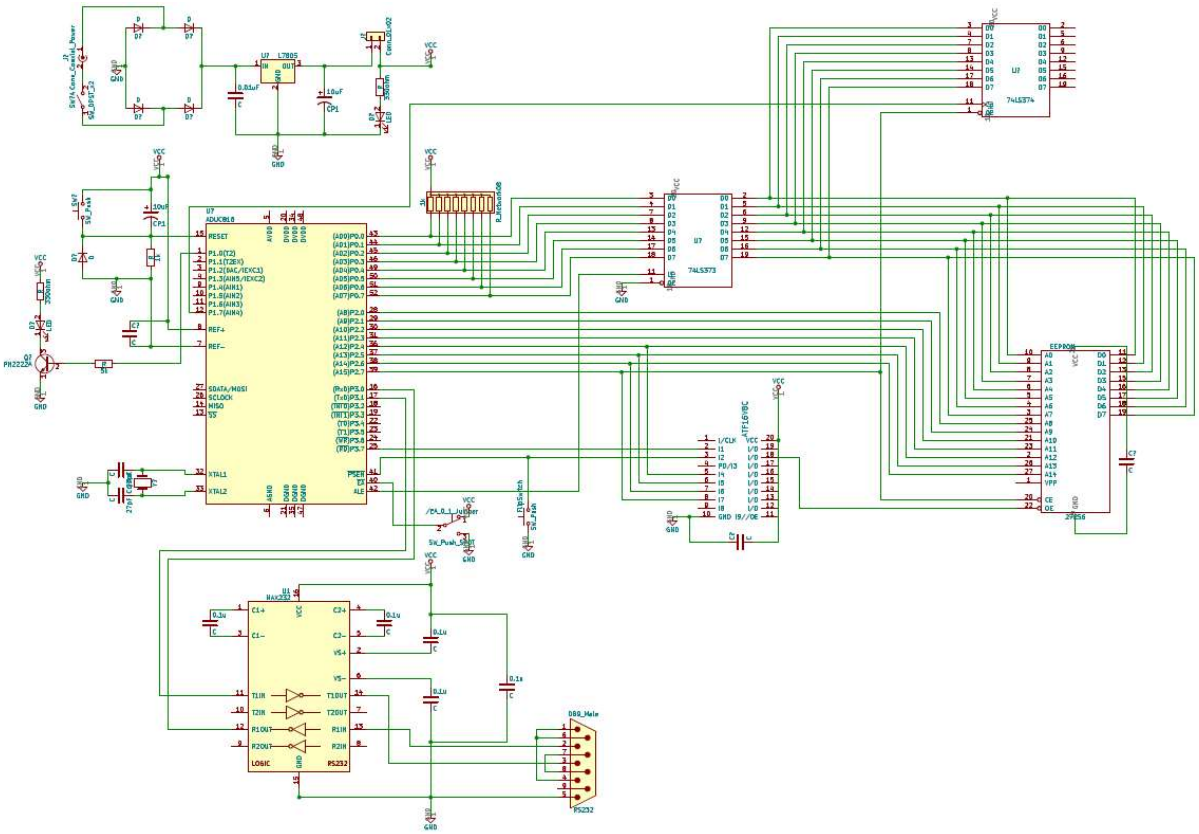
LOGIC Analysis

Toughest Thing to do

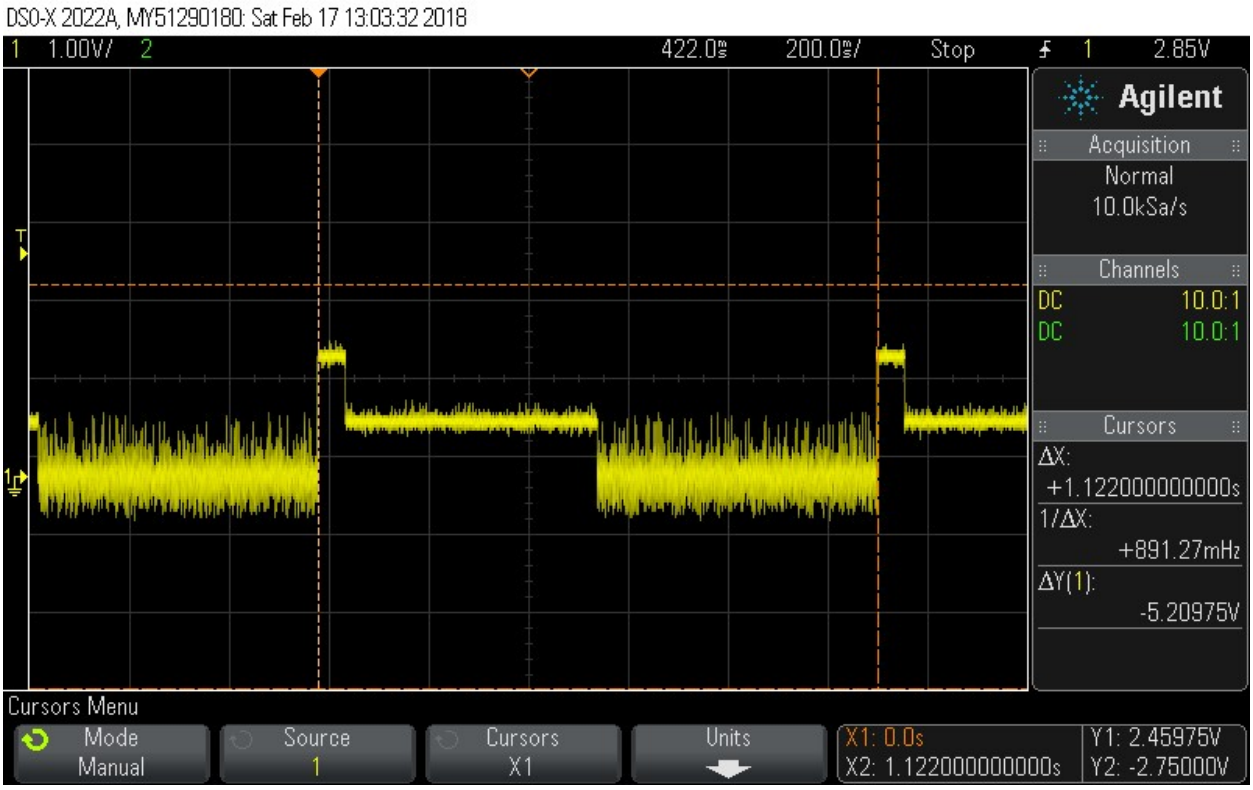
Interfacing 89C51 with EEPROM

Debugging Hardware

Schematic



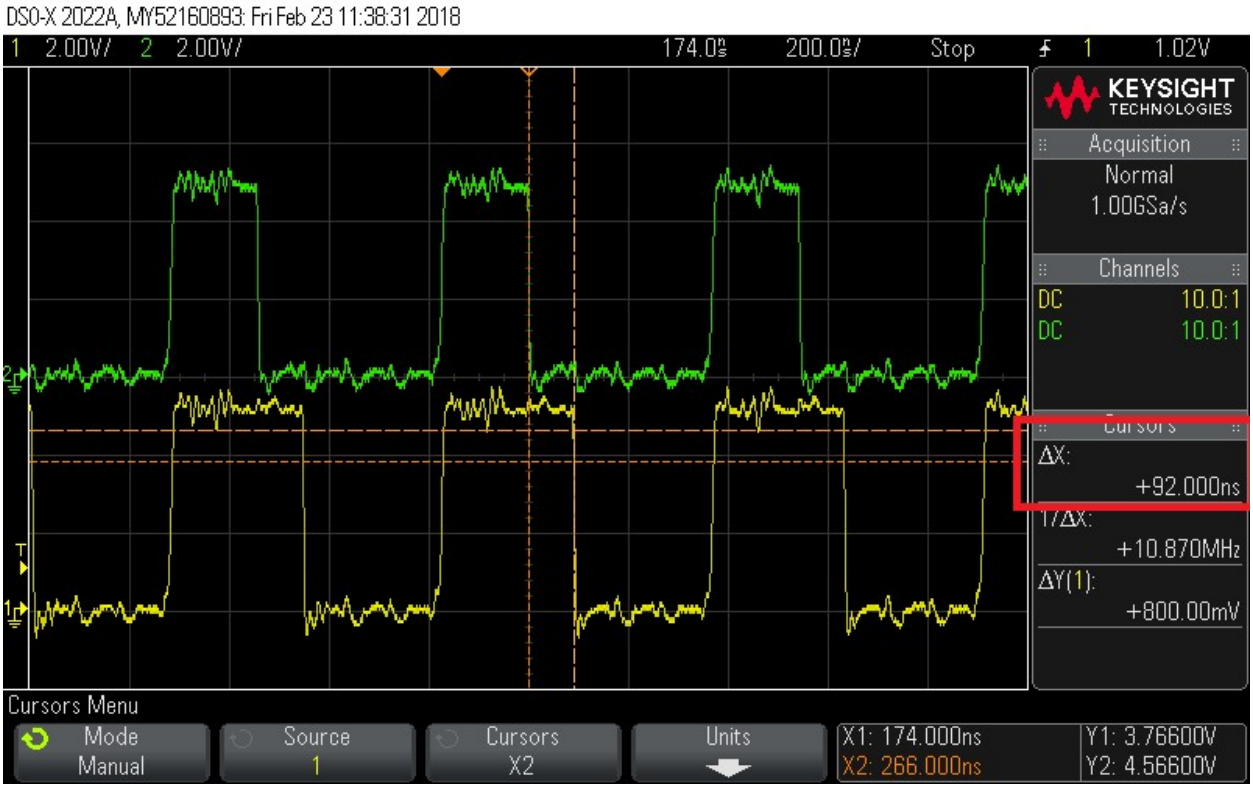
LED Waveform (period 1.122 S)



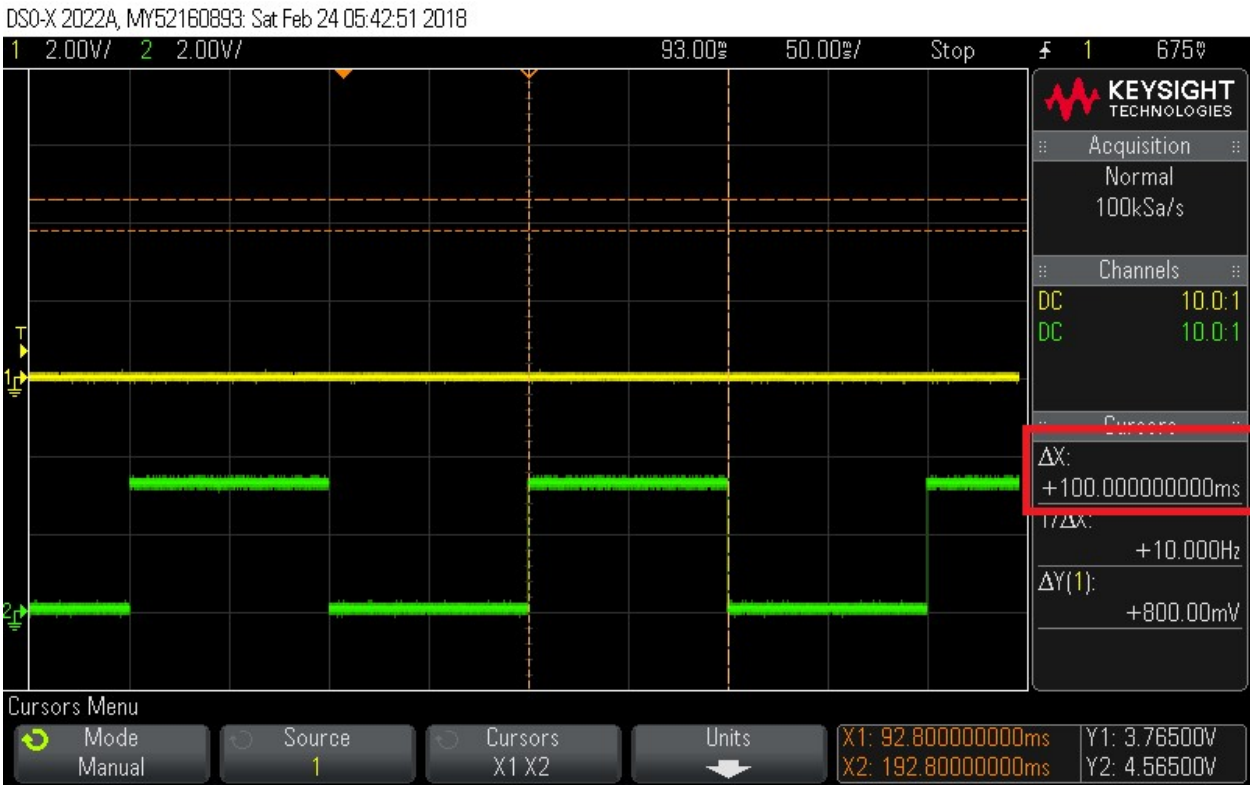
ISR Routine Cycles

	Cycles	Short Interrupt	Long Interrupt
ORG 000BH	0	0	0
INC R3	1	1	1
CPL P1.7	1	1	1
MOV A,R3	1	1	1
JNZ EXIT_ISR	2	2	2
CPL P1.0	1	0	1
MOV R3,#0F6H	1	0	1
CPL A	1	0	1
EXIT_ISR:	0	0	0
CPL P1.7	1	1	1
RETI	2	2	2
	Total Cycles =	8	11
	Ocsillator Cycles =	96	132
	Execution Time (uS)=	8.680555556	11.93576389

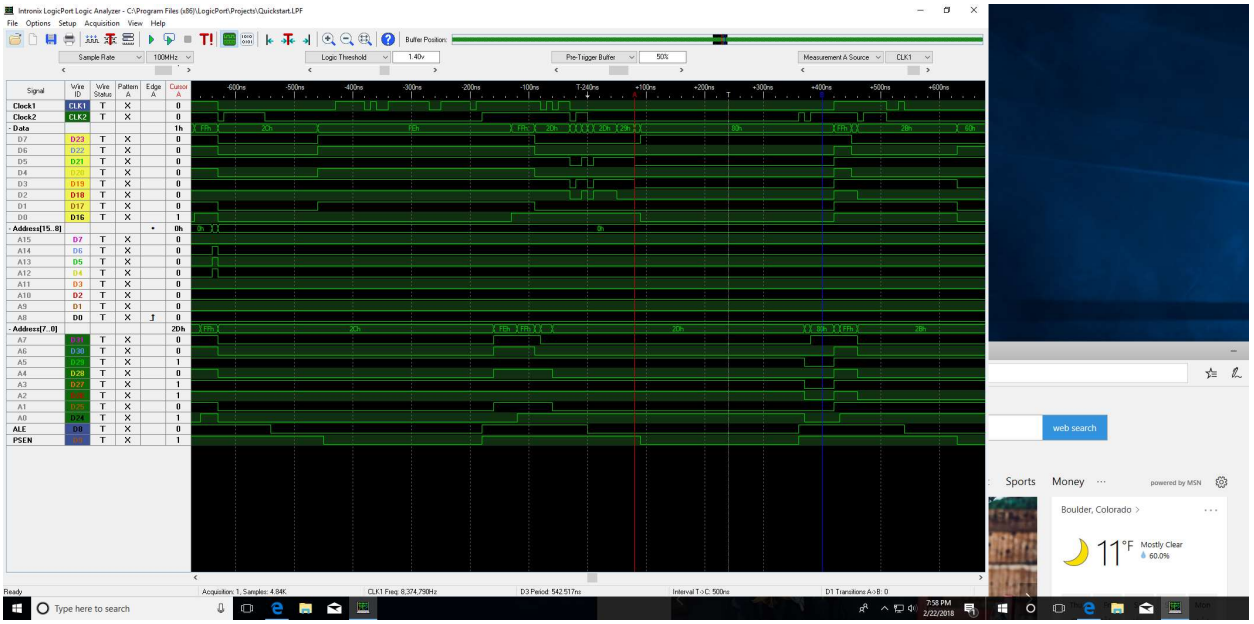
ALE_PSEN_TLL_PL 92ns



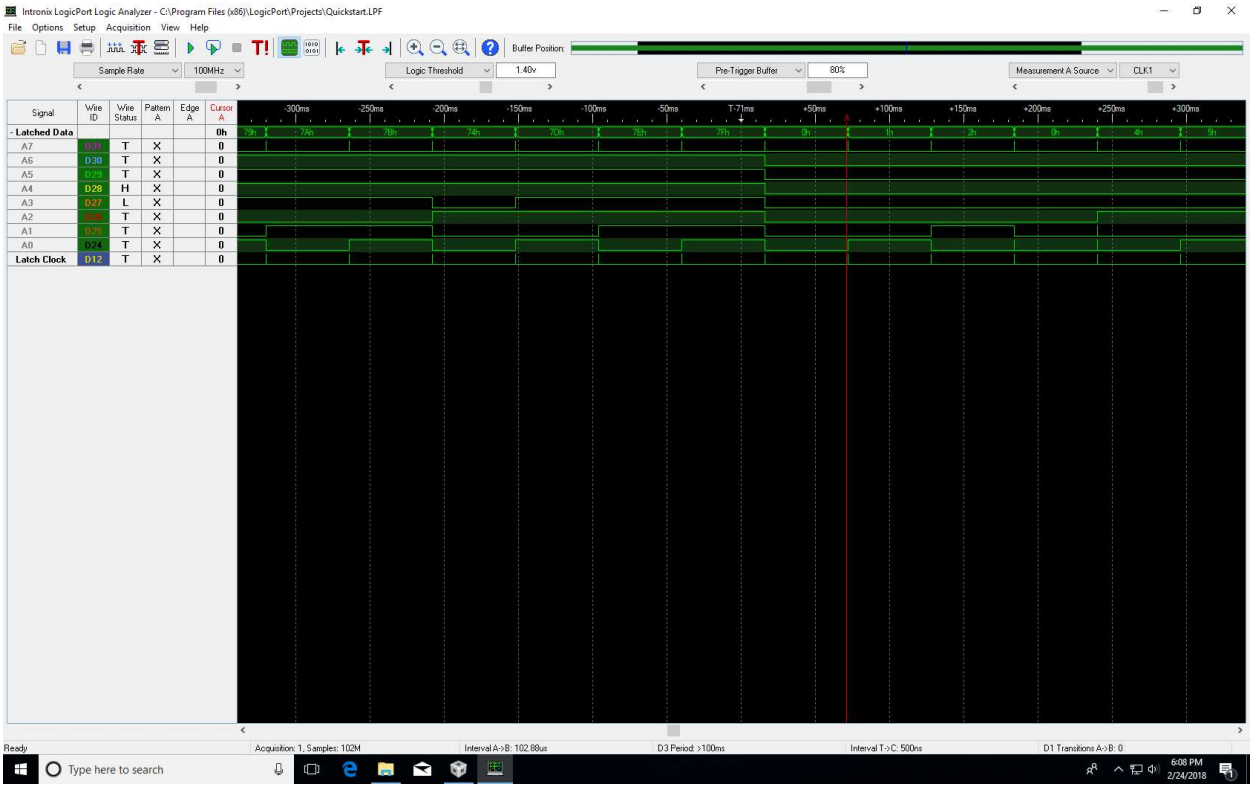
MSP_CODE_LED_INTERRUPT



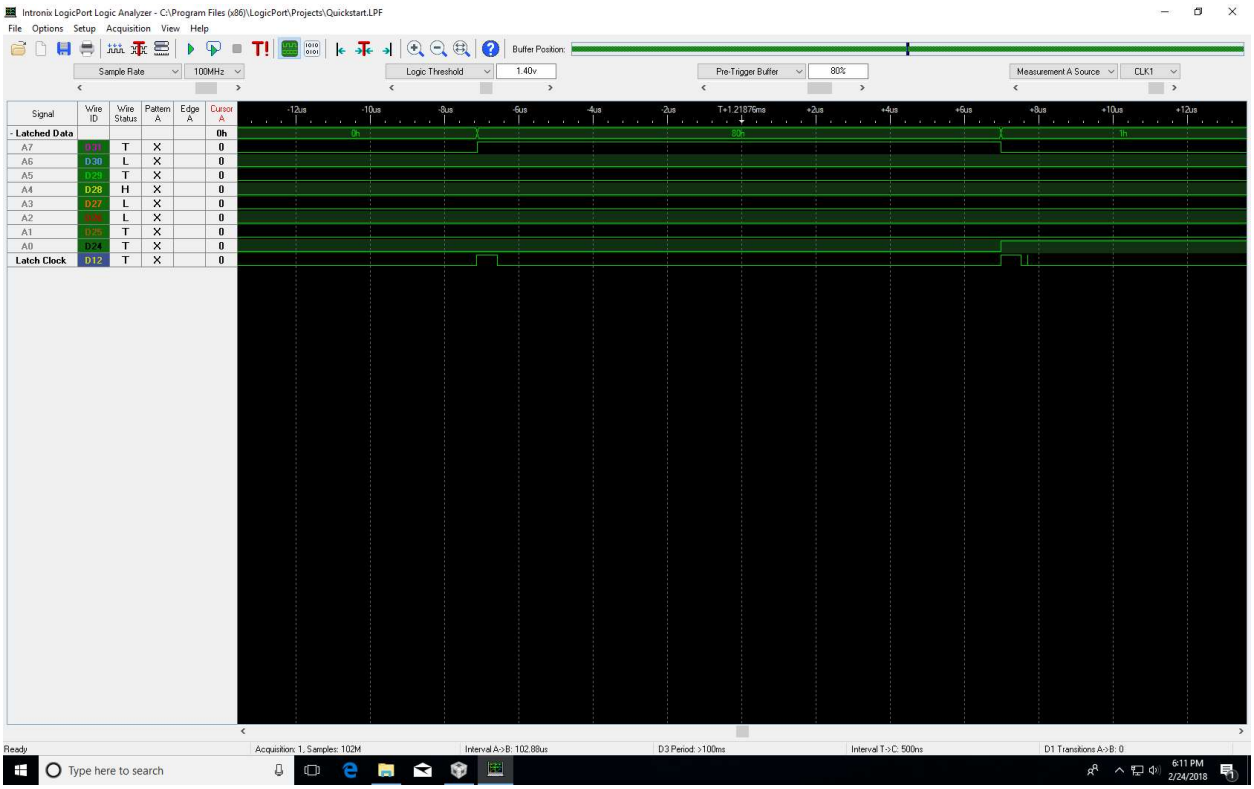
TLL-PL time 90ns



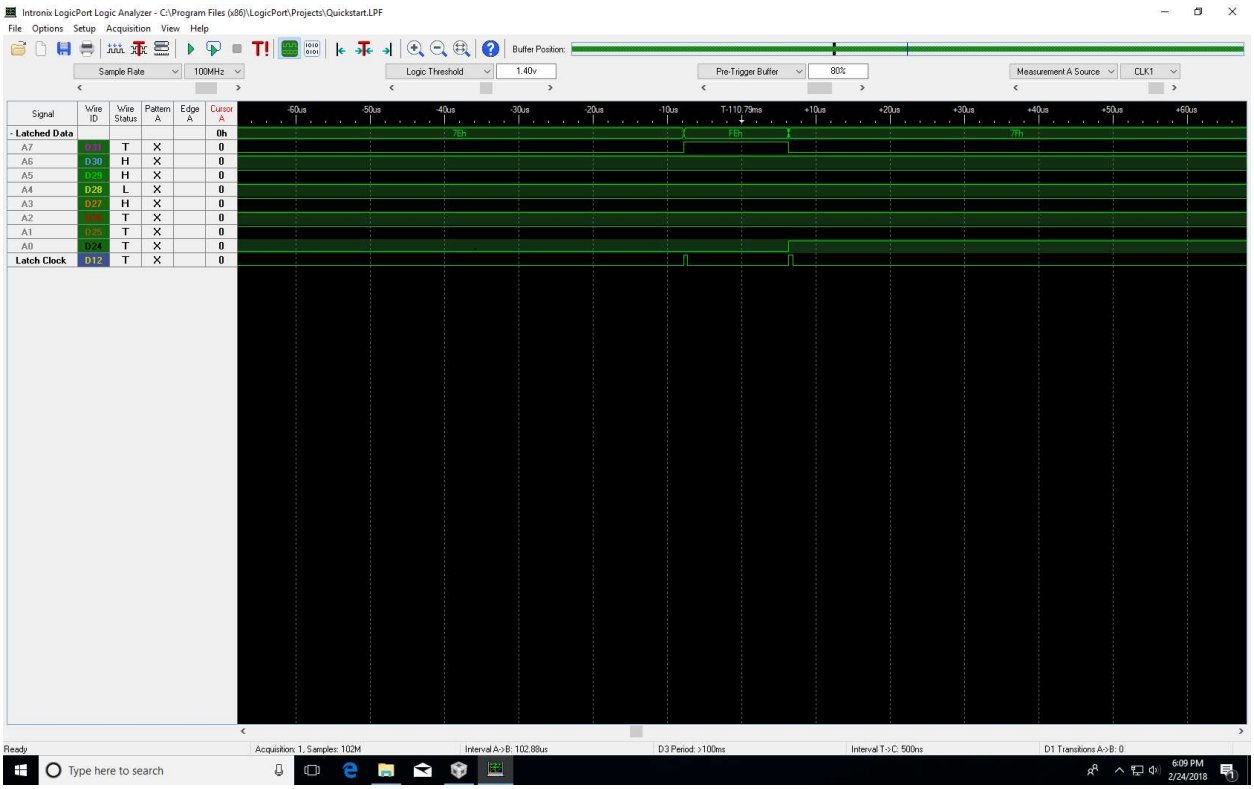
Data Latched (Supplemental)



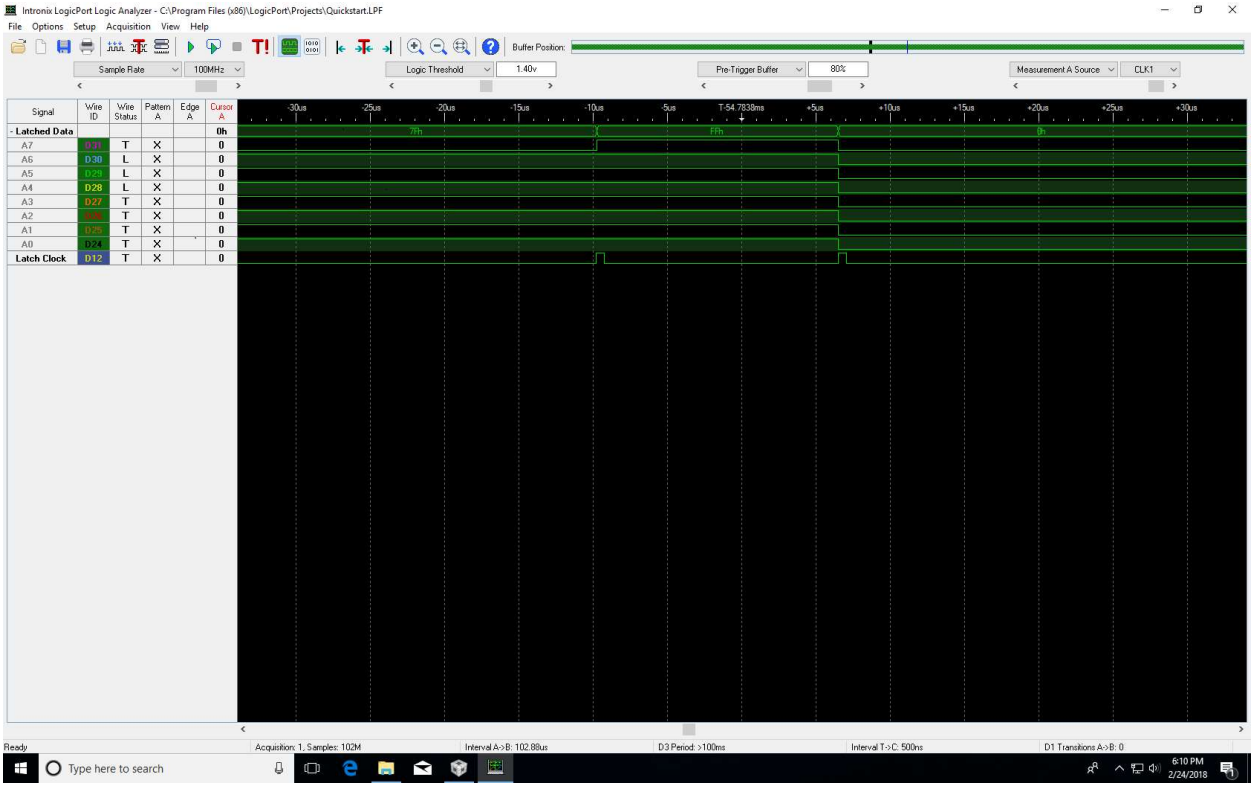
Data Latched 80h (Supplemental)



Data Latched FEh (Supplemental)



DATA Latched in ISR FF (Supplemental)



ECEN 5613 — **Embedded System Design** — Spring 2018

Lab #2 Signoff Sheet

You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by **Friday, February 16, 2018 (Part 1 Required Elements) and Friday, February 23, 2018 (Part 2 Required and Supplemental Elements)**.

Print your name below, sign the honor code pledge, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: Manish Nene

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: Manish

Signoff Checklist

Part 1 Required Elements

- ☑ Schematic of acceptable quality, correct memory map, SPLD .PLD file
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board
- ☑ NVRAM (as EPROM substitute), decode logic, and LED functional
- ☑ Understands device programmer.
- ☑ Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM.
- ☑ Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display.
- ☑ Shows and discusses logic analyzer screen captures:
- ☑ Assembly program and timer ISR functional:

TA signature and date 02/16/18

Part 2 Required and Supplemental Elements

- ☑ AT89C51RC2, RS-232, and FLIP functional
- ☑ 74LS374 debug port functional
- ☑ Understands timing analysis, setup/hold/propagation
- ☑ MSP432 code build process, basic LED program execution

TA signature and date 02/25/18

Instructor/TA Comments: ☐ ☐ ☐

FOR INSTRUCTOR USE ONLY Part 1 Elements	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑	☐	☐
Hardware physical implementation	☐	☐	☑	☐	☐
Part 1 Required Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☐	✓	☐
Overall Demo Quality (Part 1 Elements)	☐	☐	☐	✓	☐

FOR INSTRUCTOR USE ONLY Part 2 Elements	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☑	☐	☐
Hardware physical implementation	☐	☐	☑	☐	☐
Part 2 Required Elements functionality	☐	☐	☑	✓	☐
Supplemental Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☐	✓	☐
Overall Demo Quality (Part 2 Elements)	☐	☐	☐	✓	☐

NOTE: This signoff sheet should be the top/first sheet of your submission.