Cairo University

Computer Engineering Department

Faculty of Engineering

Third year

VLSI PROJECT

Home Automation System

Team#12 Members

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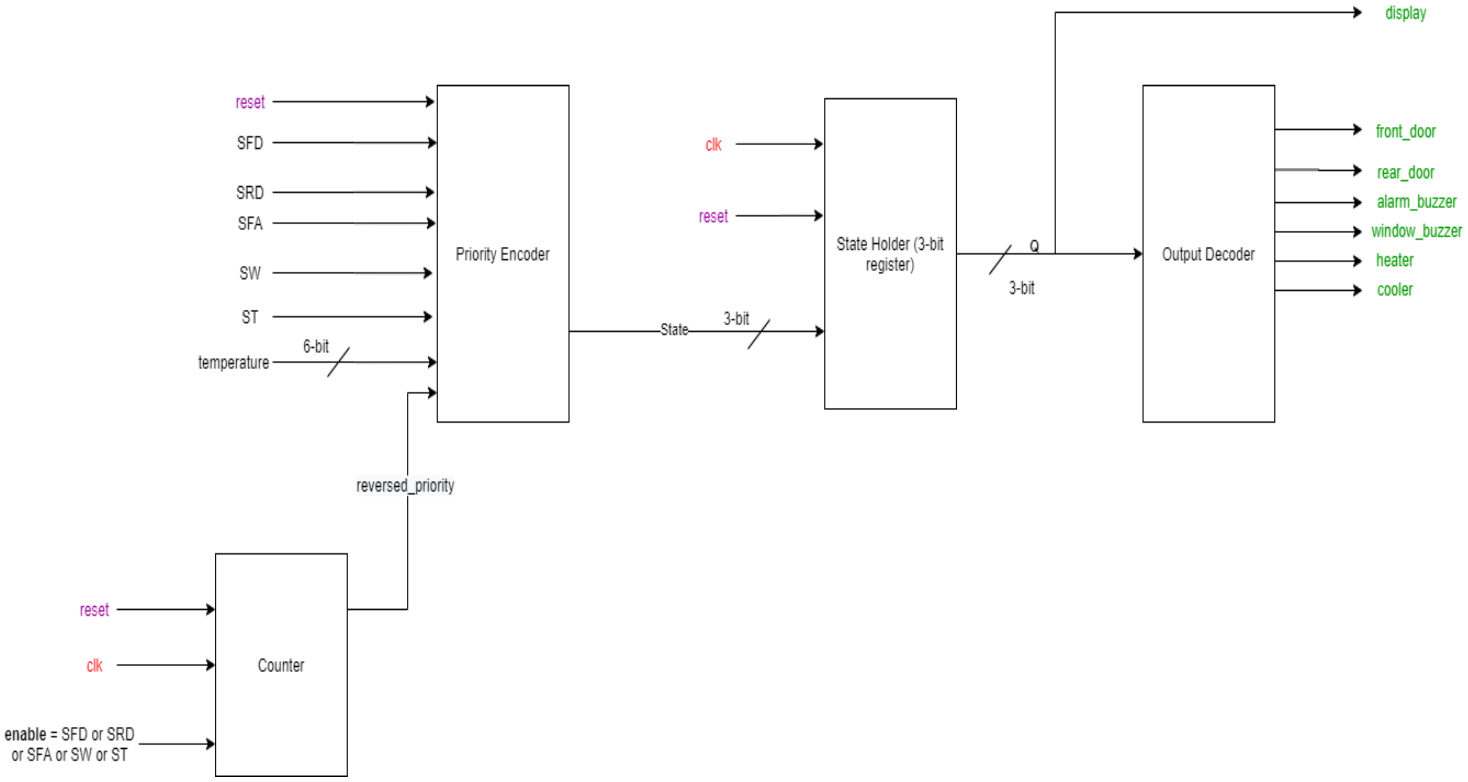
We have chosen design 2, as it handles starvation in a better way using dynamic priority and a sort of state machine.

Regarding the optimization parameters, design 2 utilize more area on the chip as it uses a larger design for the priority encoder and regarding the power, design 2 consumes more power due to the excessive load on the priority encoder and the frequent change of the state. Furthermore, slack value is higher as the register to output delay limits it.

Design 1

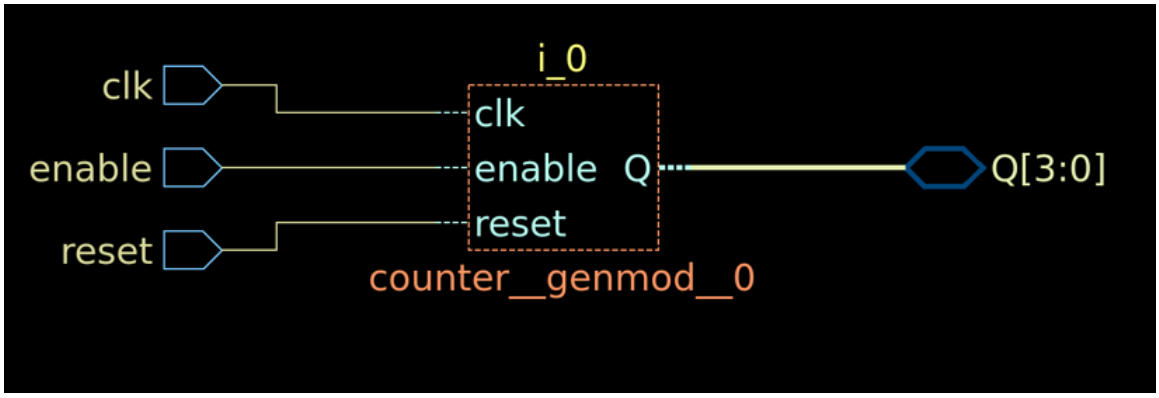
System Schematic:

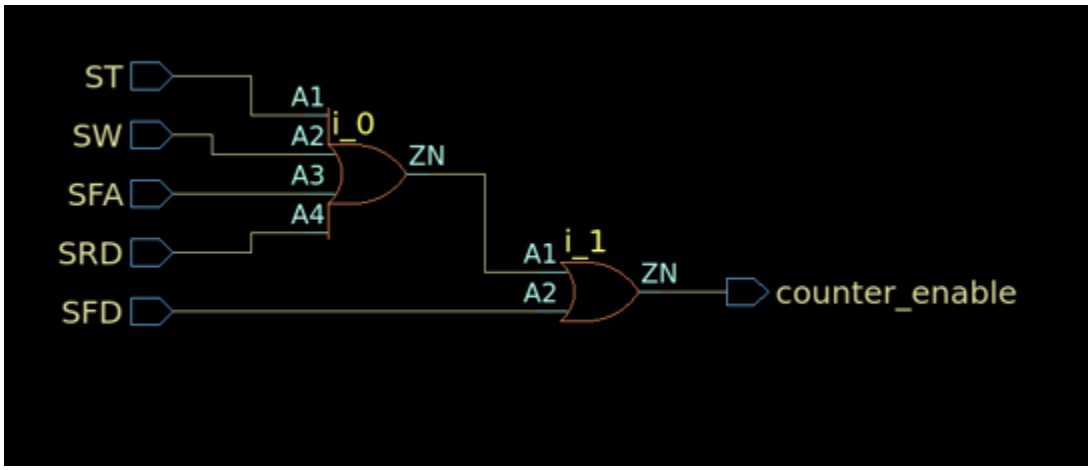


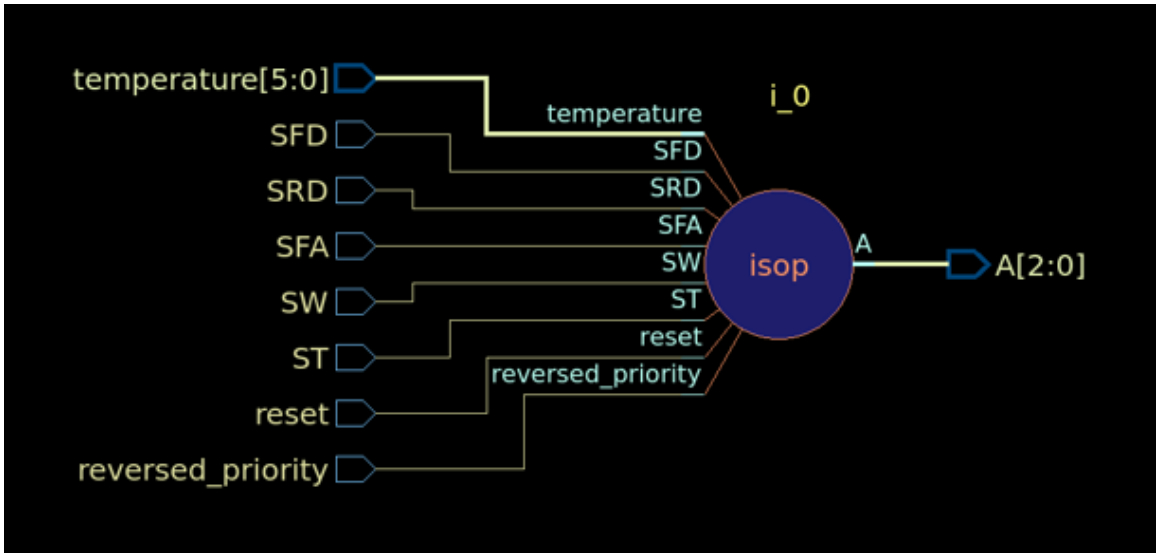
Description:

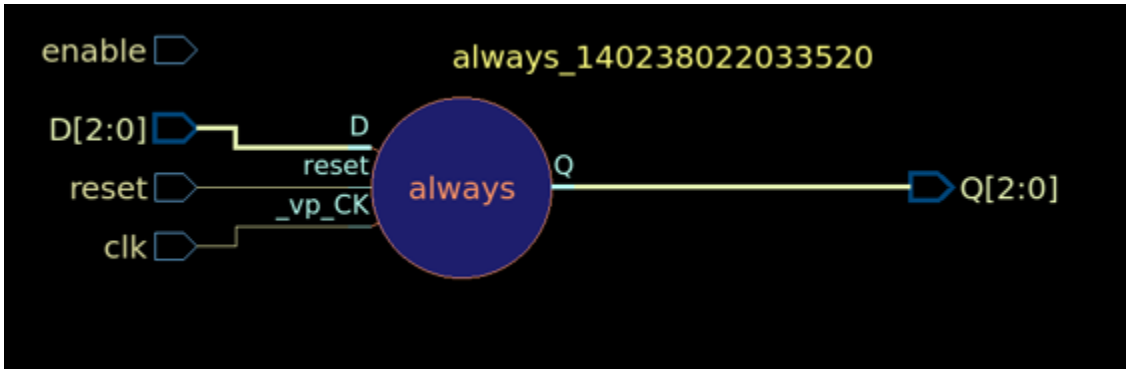
Every 6 clock cycles, the priority is completely reversed through the **reversed_priority** signal from the counter. The counter starts from 0 to 5 and then goes back to 0, it is increased by 1 in all cycles except if there is no active input, in that case the counter remains as it is for this cycle. The priority encoder outputs a code which represent the state of the system (which is the display output mentioned in the document). The register preserves the state so that any state should take at least 1 cycle. The output decoder maps the system state to the output signals.

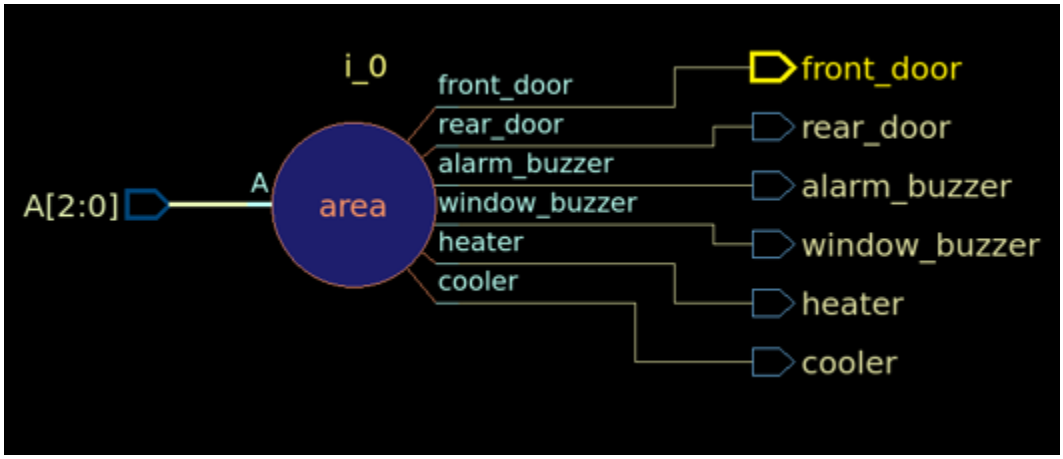
Schematic of the design after synthesis:

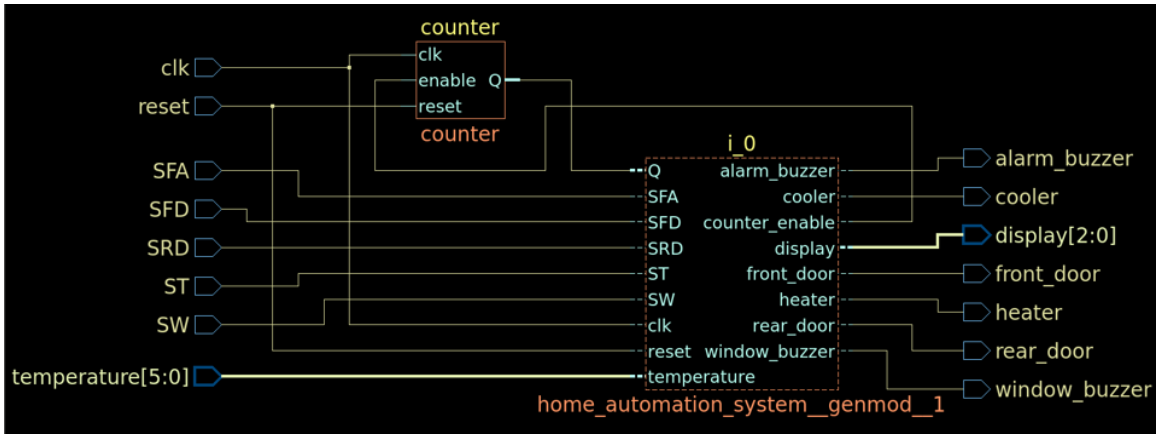


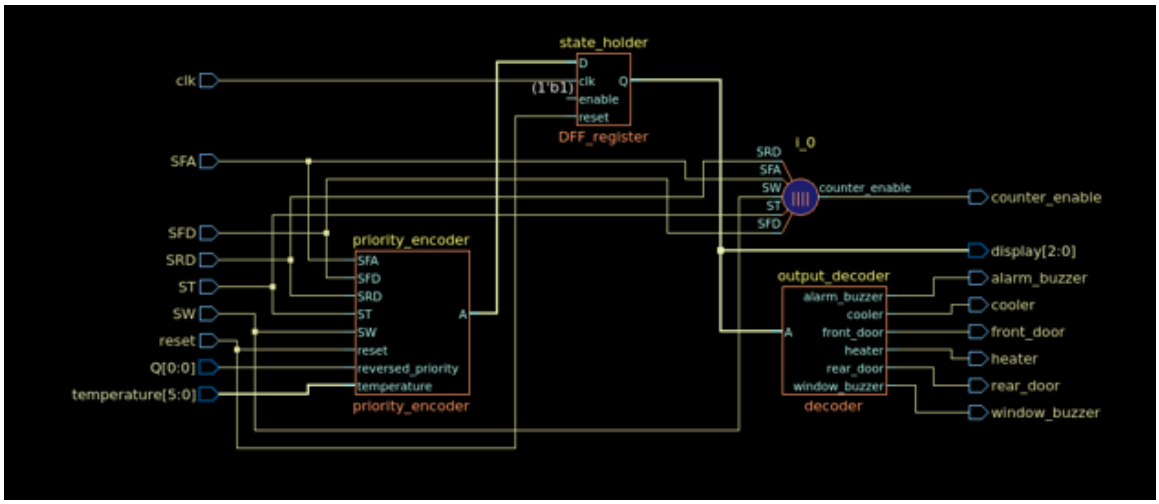



temperature[5:0]
SFD
SRD
SFA
SW
ST
reset
reversed_priority
i_0
temperature
SFD
SRD
SFA
SW
ST
reset
reversed_priority
isop
A
A[2:0]


enable
always_140238022033520
D[2:0]
reset
clk
D
reset
_vp_CK
always
Q
Q[2:0]

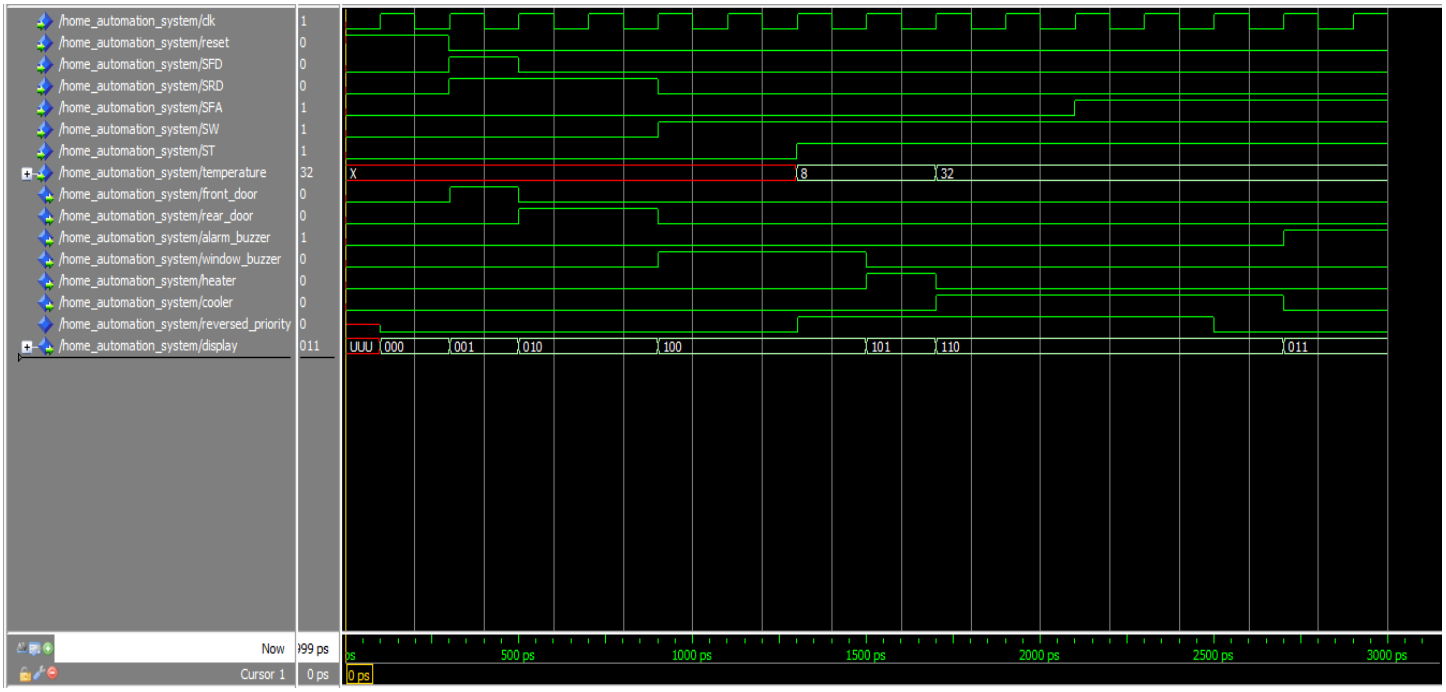

i_0
A[2:0]
A
area
front_door
rear_door
alarm_buzzer
window_buzzer
heater
cooler
front_door
rear_door
alarm_buzzer
window_buzzer
heater
cooler



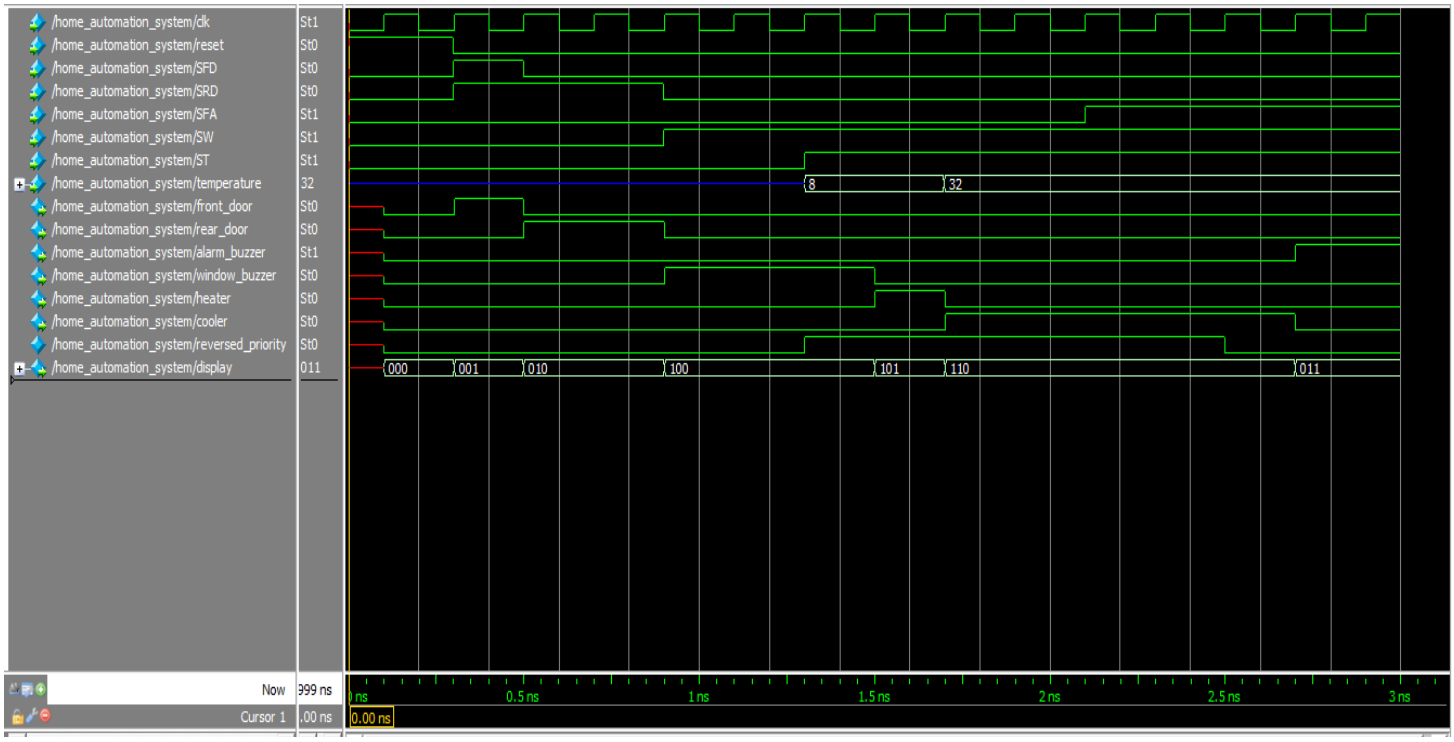


Note that the values of the temperature in the simulation are 49 and 73 not 8 and 32 because our design for the temperature register is that it ranges from 41F to 104F, so each value in the simulation must be added to 41 because it is our zero reference.

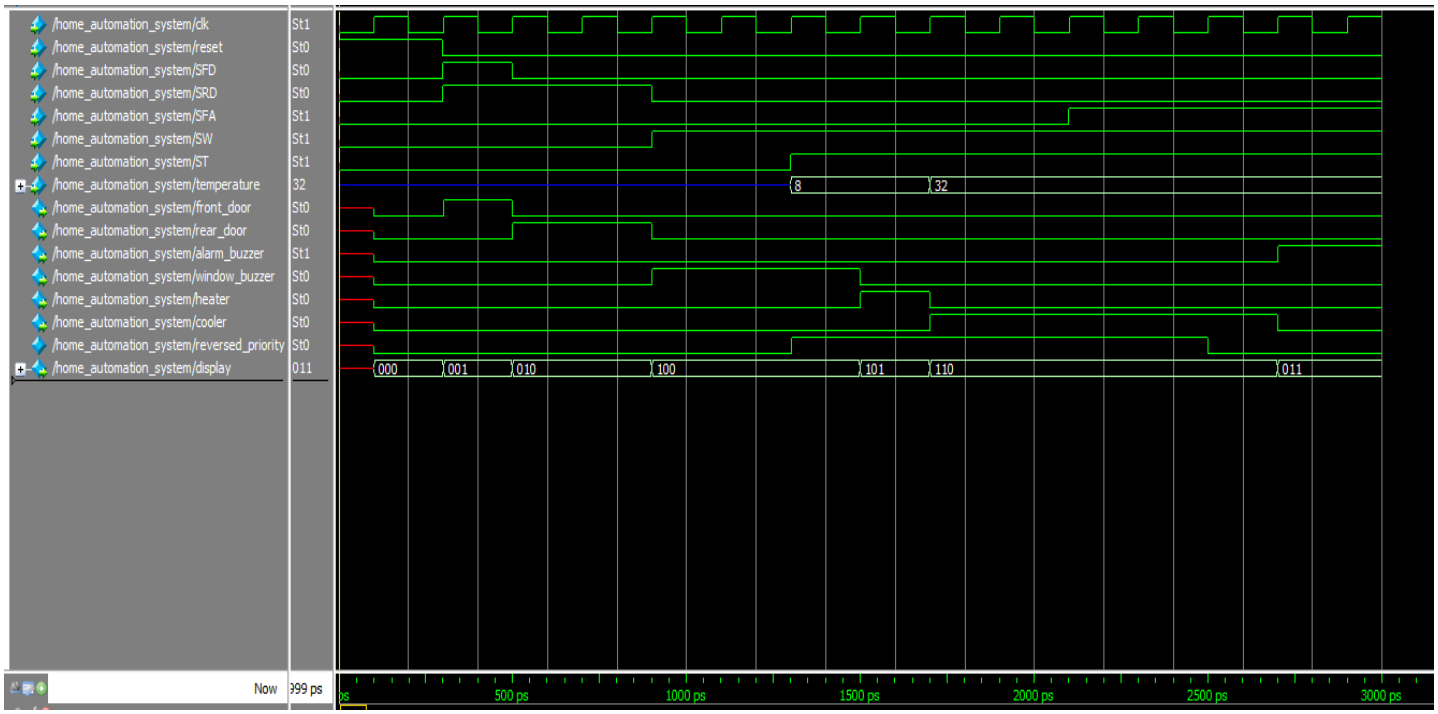
Pre-Synthesis Simulation:



Post-Synthesis Simulation:

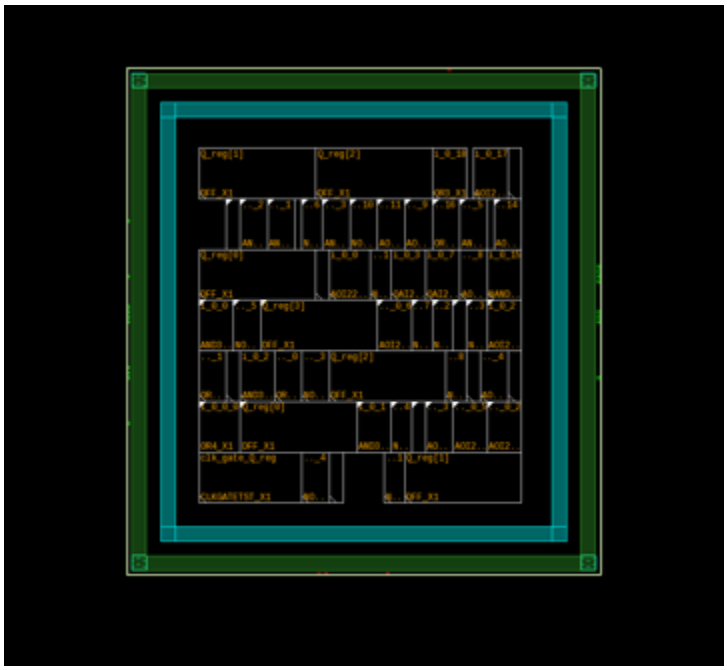


Post-Layout Simulation:

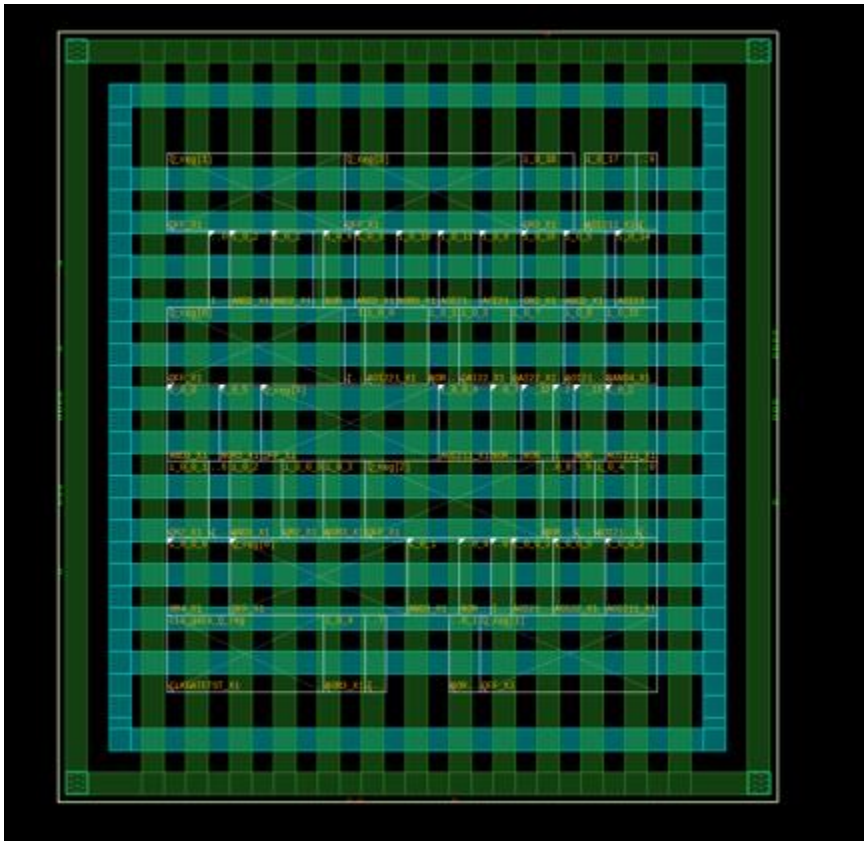


Chip Schematic:

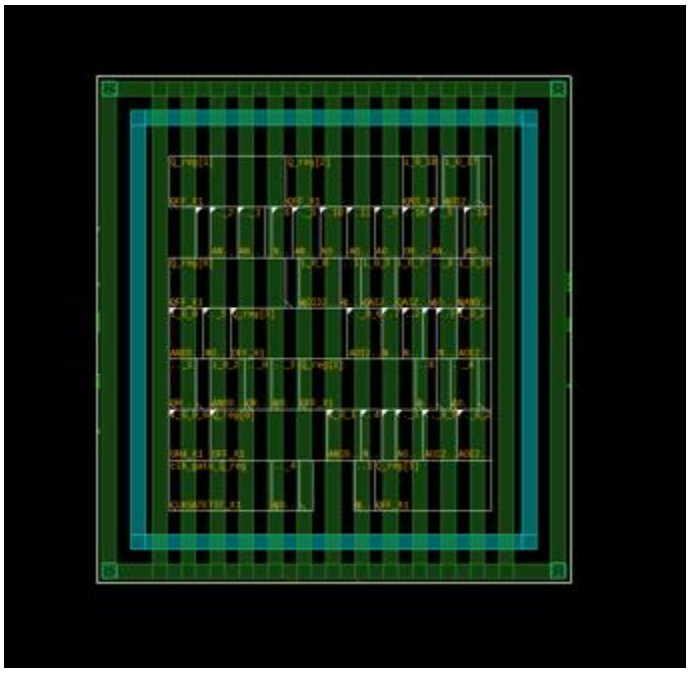
Power Grid:



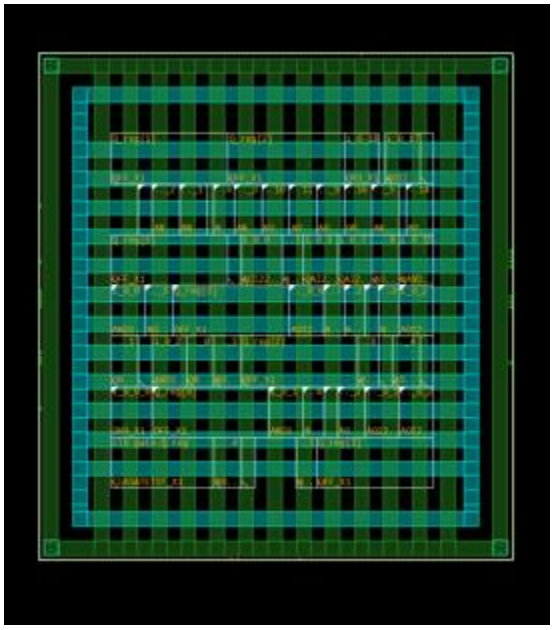
Routing:



Vdd Strips:



Vss Strips:



design.rpt file:

```
Report Physical info:
----------------------+--------------------+----------+------------
                      |                    |Area (squm)|Leakage (uW)
----------------------+--------------------+----------+------------
Design Name           |home_automation_system|          |
  Total Instances     |                  56|        84|       1.784
    Macros            |                   0|         0|       0.000
    Pads              |                   0|         0|       0.000
    Phys              |                   0|         0|       0.000
    Blackboxes        |                   0|         0|       0.000
    Cells             |                  56|        84|       1.784
      Buffers         |                   0|         0|       0.000
      Inverters       |                   9|         5|       0.129
      Clock-Gates     |                   1|         4|       0.059
      Combinational   |                  39|        44|       1.042
      Latches         |                   0|         0|       0.000
      FlipFlops       |                   7|        32|       0.554
       Single-Bit FF  |                   7|        32|       0.554
       Multi-Bit FF   |                   0|         0|       0.000
       Clock-Gated    |                   4|          |
       Bits           |                   7|        32|       0.554
         Load-Enabled |                   0|          |
         Clock-Gated  |                   4|          |
  Tristate Pin Count  |                   0|          |
Physical Info         |Placed              |          |
  Chip Size (mm x mm) |0.072 x 0.072       |      5160|
  Fixed Cell Area     |                    |         0|
    Phys Only         |                   0|         0|
  Placeable Area      |                    |       132|
  Movable Cell Area   |                    |        84|
  Utilization (%)     |                  63|          |
  Chip Utilization (%)|                  63|          |
  Total Wire Length (mm)|               0.806|          |
  Longest Wire (mm)   |                0.041|          |
  Average Wire (mm)   |                0.030|          |
----------------------+--------------------+----------+------------
```

path.rpt file:

```
Report Path Groups:
-----+-------+------+---------+---------
     | Path  |Weight|Critical |Worst
     | Group |      |Range(ps)|Slack(ps)
-----+-------+------+---------+---------
1    |default| 1.000|      0.0|    717.4
2    |I2R    | 1.000|      0.0|    676.9
3    |I2O    | 1.000|      0.0|<ill>
4    |R2O    | 1.000|      0.0|    689.5
-----+-------+------+---------+---------
```

power.rpt file:

Report Power (instances with prefix '*' are included in total) :

	Instance	Internal Power(uw)	Switching Power(uw)	Leakage Power(uw)	Total Power(uw)
1	*counter	22.111841	37.349838	0.641388	60.103069
2	*priority_encoder	16.324997	34.239510	0.577562	51.142063
3	*state_holder	6.935781	15.369468	0.326888	22.632137
4	*output_decoder	1.539435	5.220446	0.188646	6.948526
5	*i_0_0_0	0.364796	0.204921	0.026733	0.596451
6	*i_0_0_1	0.158072	0.113543	0.022695	0.294310
7					
8	*TOTAL	47.434925	92.497726	1.783913	141.716583

Clock period used in this design = 1ns = 1000ps

Score = 0.5 * Movable Cell Area in squm + 0.3 * (clock period in ps – worst slack in ps) + 0.2 * total power in uw = 167.2733166

Design 2

Algorithm:

Initially, the priority is normal (front door, rear door, fire alarm, window, temperature). Then in every cycle, the action with the highest priority in the previous cycle becomes the action with the least priority in the current cycle.

Example:

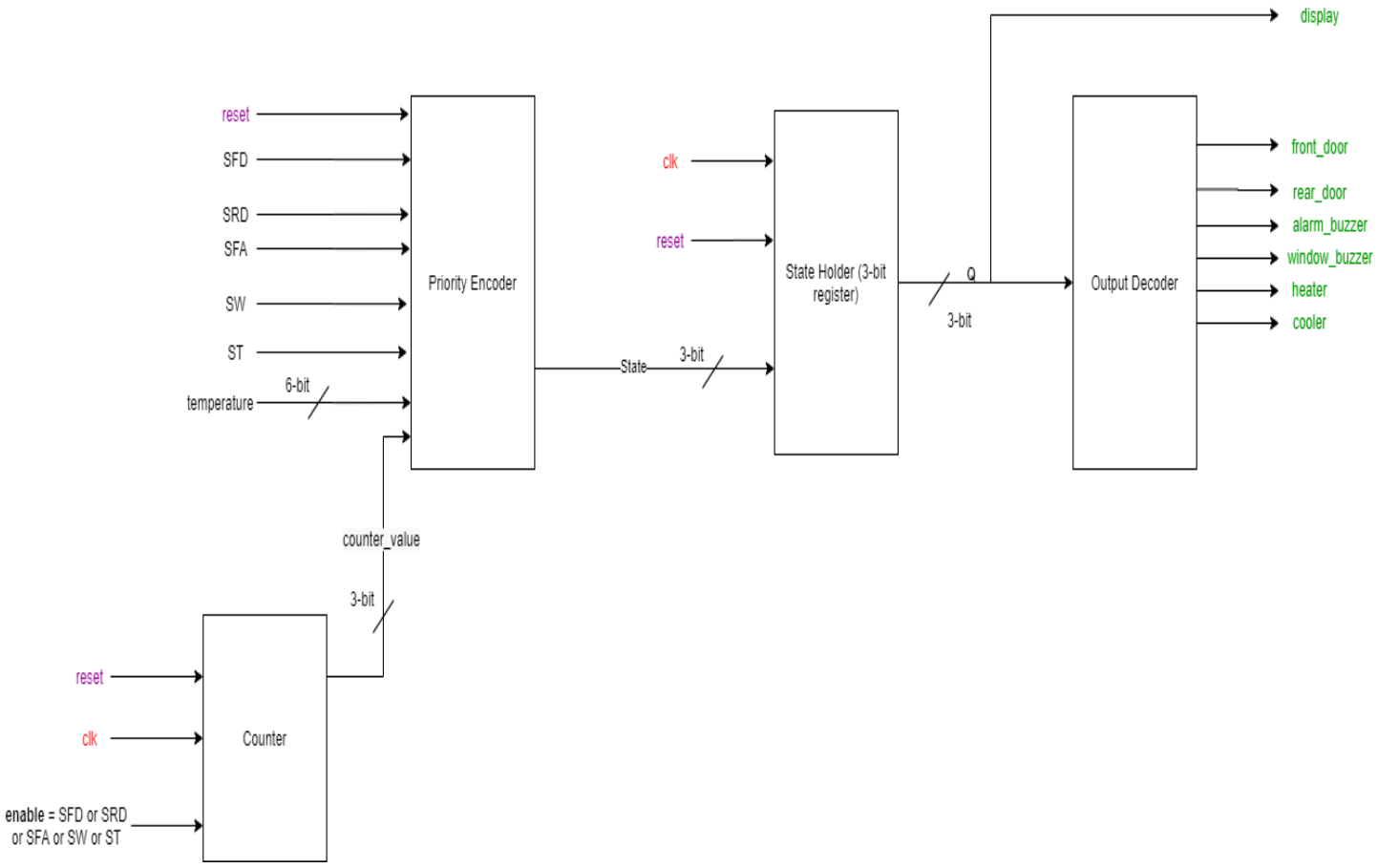
Cycle 1: front door, rear door, fire alarm, window, temperature

Cycle 2: rear door, fire alarm, window, temperature, front door

Cycle 3: fire alarm, window, temperature, front door, rear door

and so on.

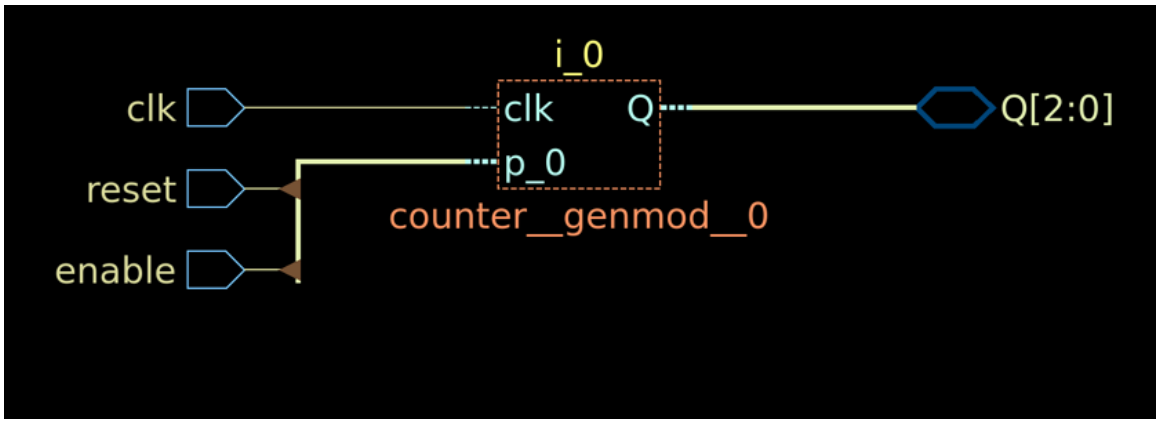
System Schematic:

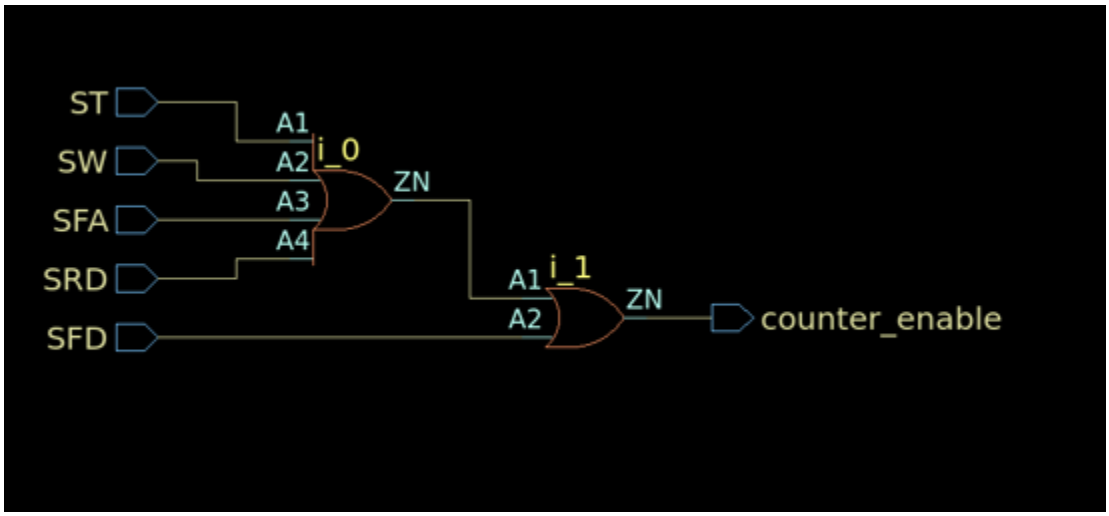


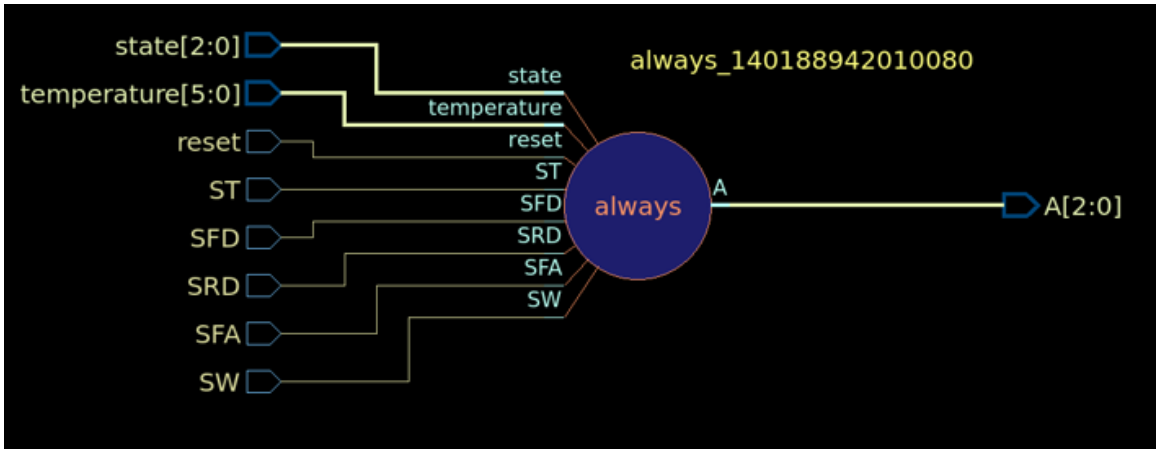
Description:

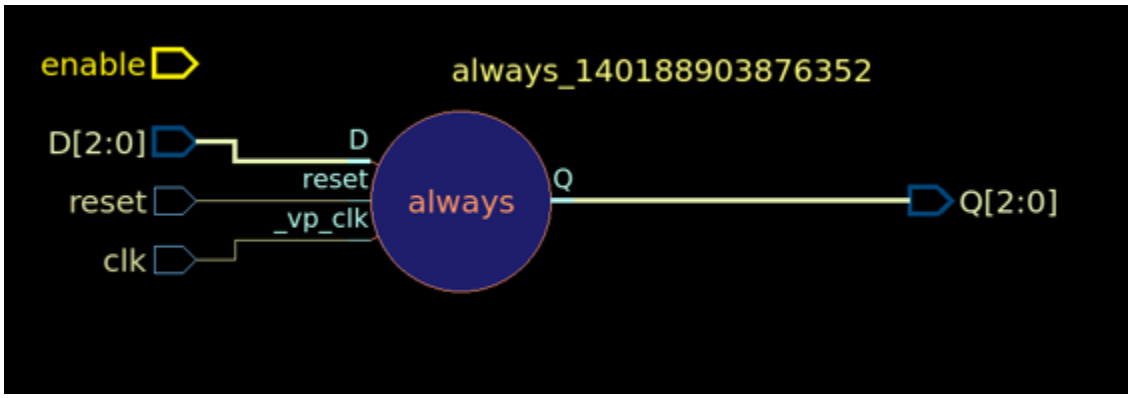
Every clock cycle, the priority encoder determines the state of the system according to the **counter_value** signal from the counter according to the previously discussed algorithm. The counter starts from 0 to 4 and then goes back to 0, it is increased by 1 in all cycles except if there is no active input, in that case the counter remains as it is for this cycle. The priority encoder outputs a code which represent the state of the system (which is the display output mentioned in the document). The register preserves the state so that any state should take at least 1 cycle. The output decoder maps the system state to the output signals.

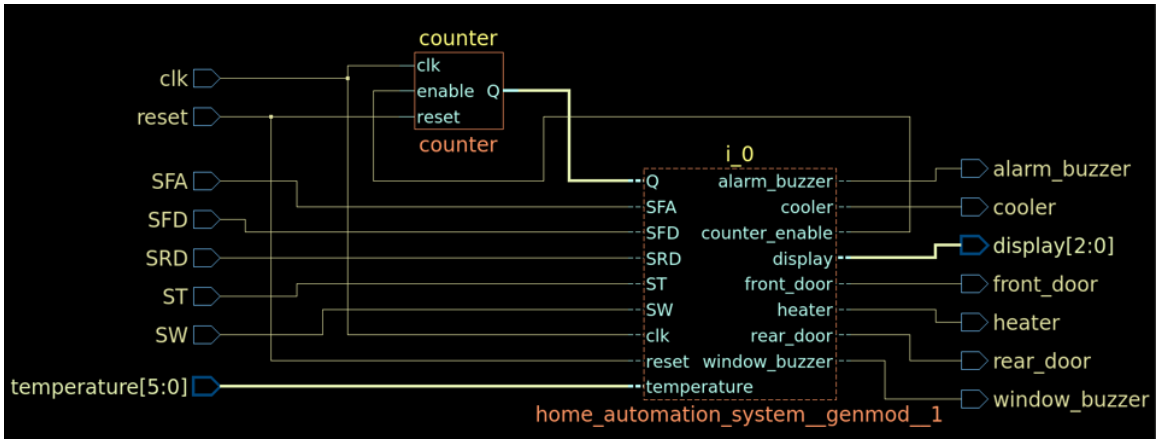
Schematic of the design after synthesis:

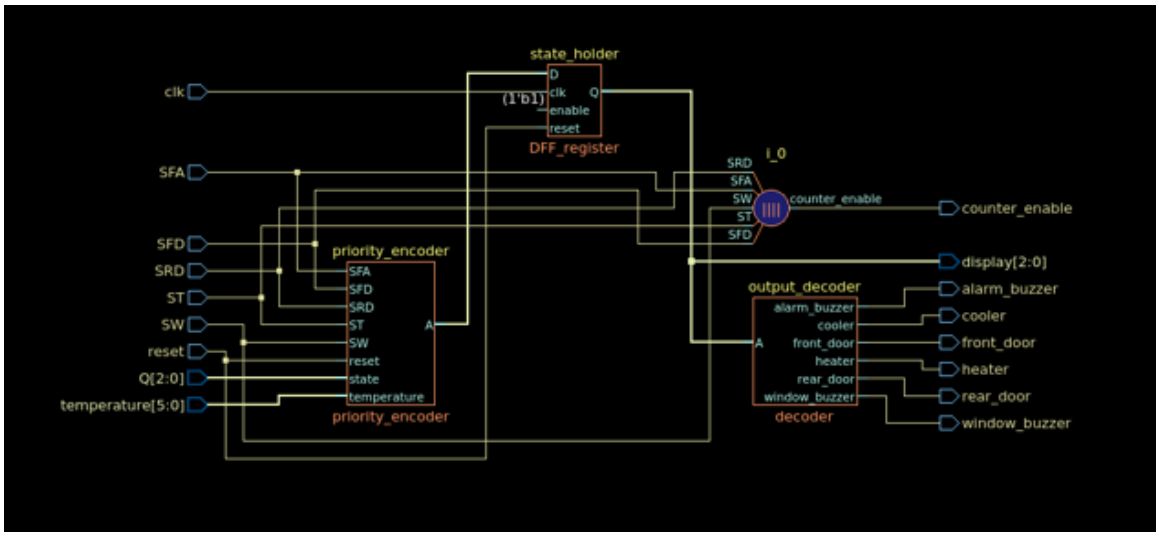




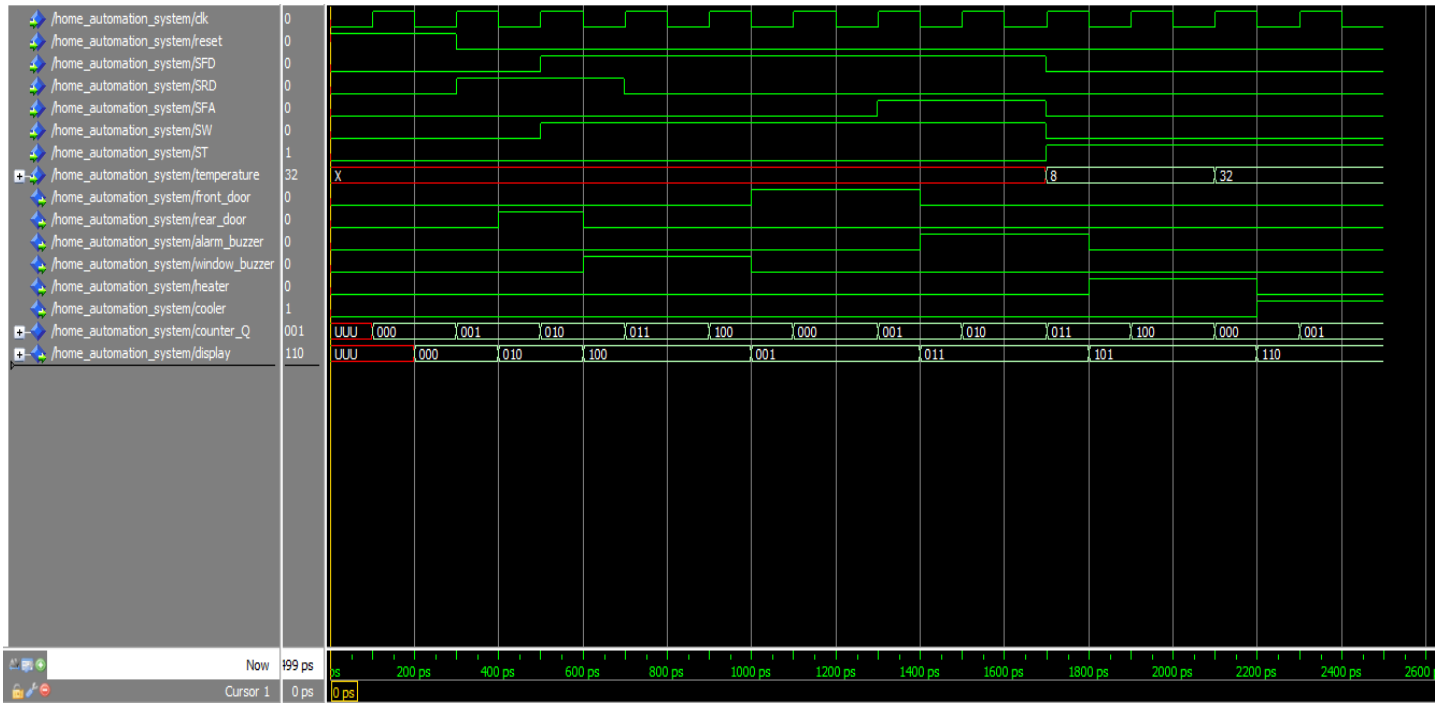

state[2:0]
temperature[5:0]
reset
ST
SFD
SRD
SFA
SW
always_140188942010080
state
temperature
reset
ST
SFD
SRD
SFA
SW
always
A
A[2:0]


enable
always_140188903876352
D[2:0]
reset
clk
D
reset
_vp_clk
always
Q
Q[2:0]

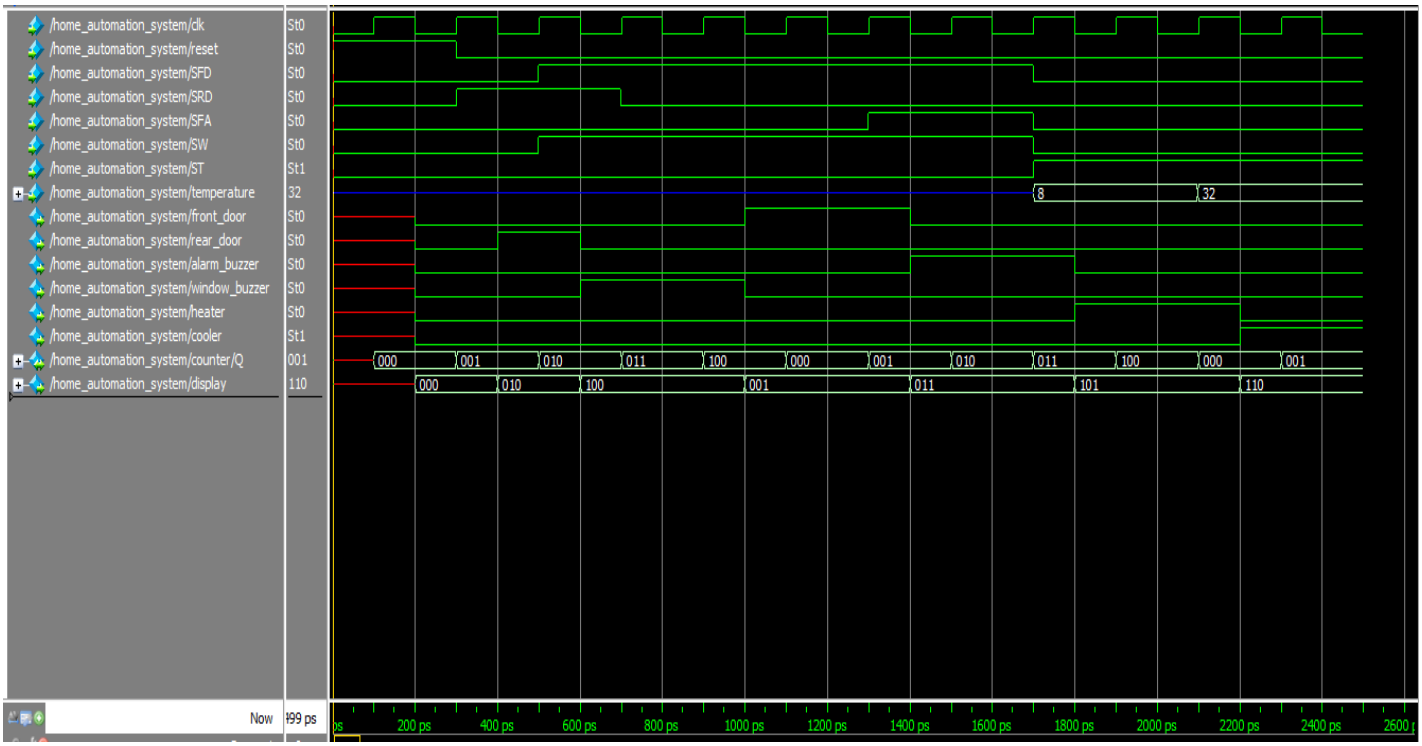

counter
clk
enable Q
reset
counter
clk
reset
SFA
SFD
SRD
ST
SW
temperature[5:0]
i_0
Q
SFA
SFD
SRD
ST
SW
clk
reset
temperature
alarm_buzzer
cooler
counter_enable
display
front_door
heater
rear_door
window_buzzer
home_automation_system__genmod__1
alarm_buzzer
cooler
display[2:0]
front_door
heater
rear_door
window_buzzer



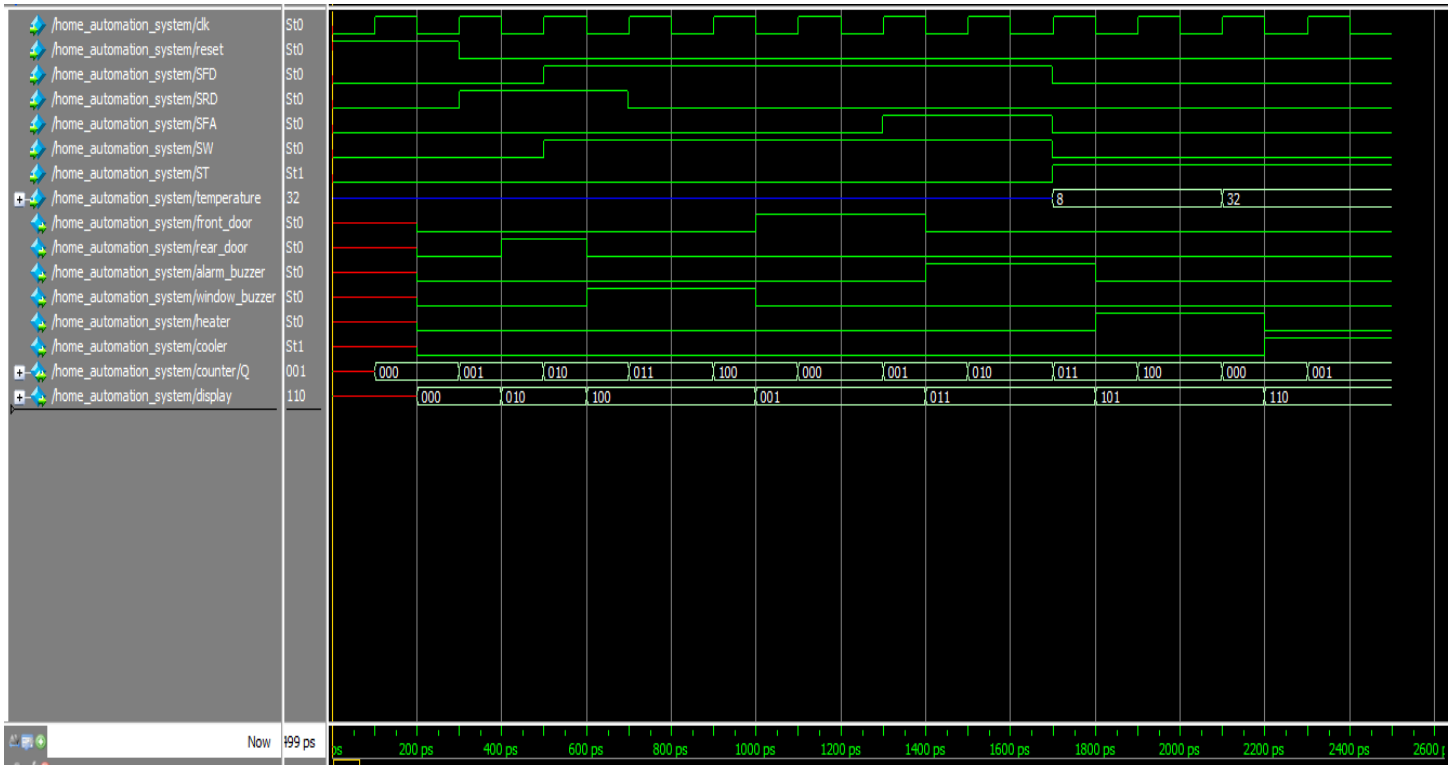
Pre-Synthesis Simulation:



Post-Synthesis Simulation:

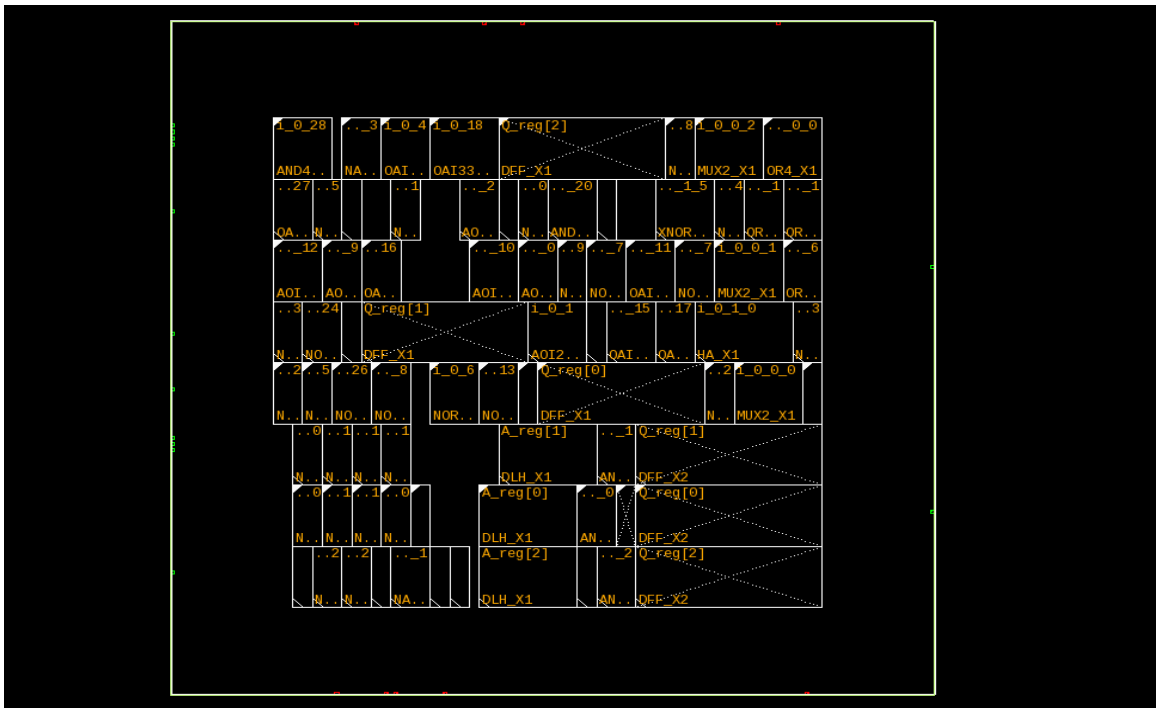


Post-Layout Simulation:

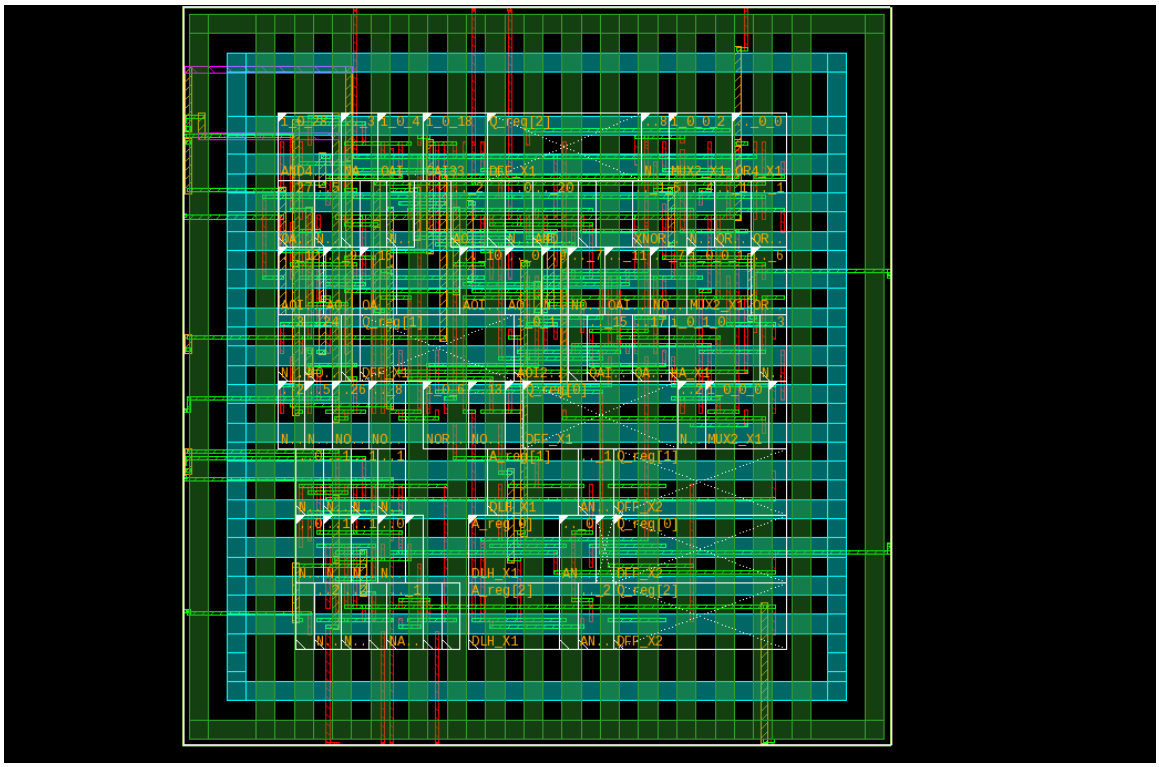


Chip Schematic:

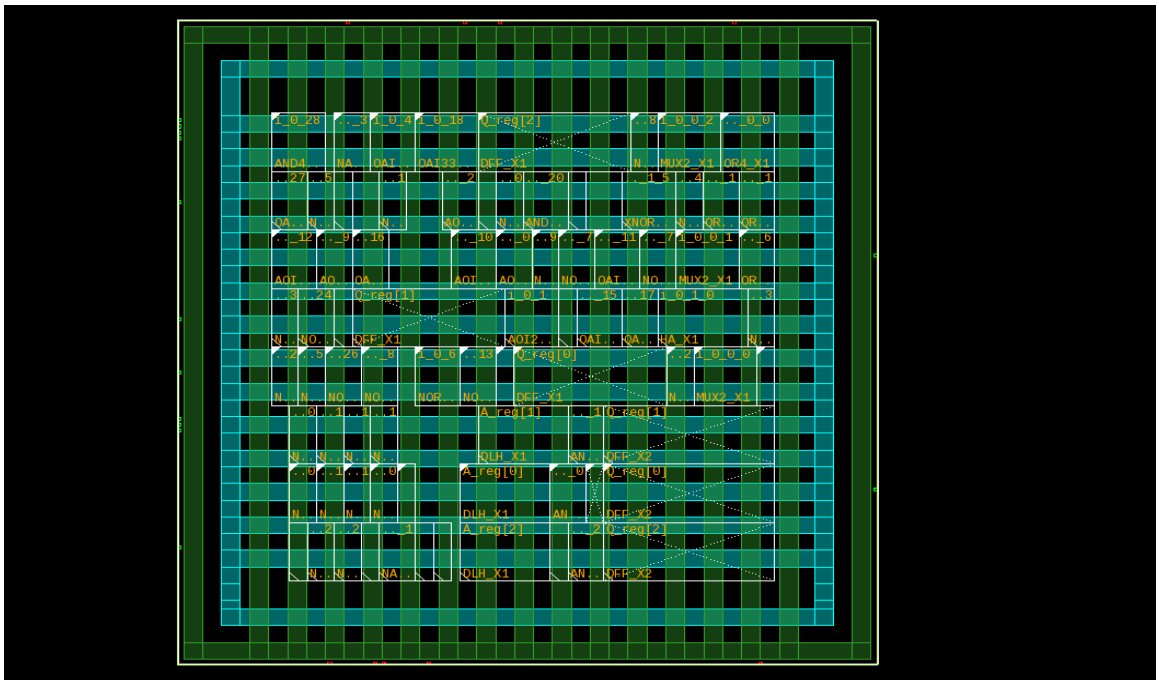
Floor Planning:



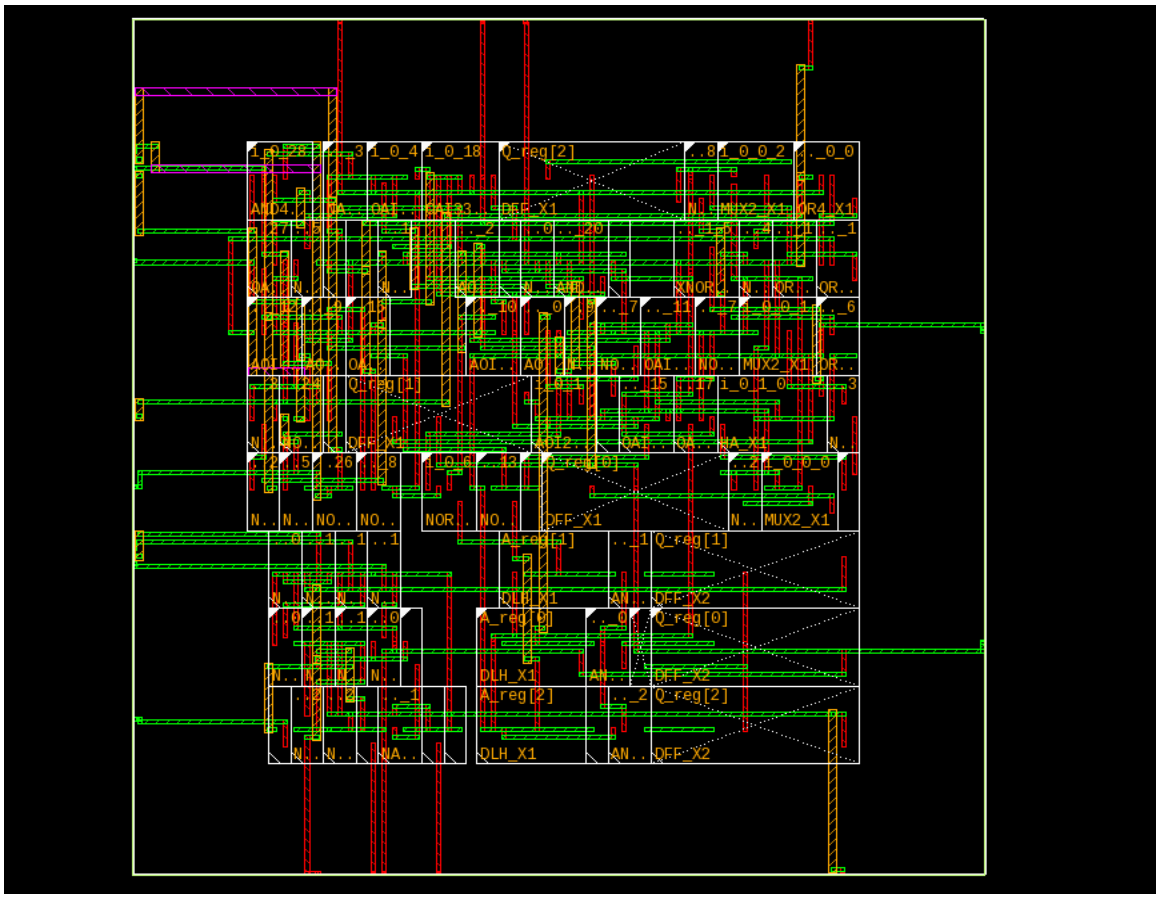
Power Grid with Routing:



Power Grid:



Routing:



design.rpt file:

```
Report Physical info:
----------------------+--------------------+----------+-----------
                      |                    |Area (squm)|Leakage (uW)
----------------------+--------------------+----------+-----------
Design Name           |home_automation_system|          |
  Total Instances     |                  72|       103|      2.172
    Macros            |                   0|         0|      0.000
    Pads              |                   0|         0|      0.000
    Phys              |                   0|         0|      0.000
    Blackboxes        |                   0|         0|      0.000
    Cells             |                  72|       103|      2.172
      Buffers         |                   0|         0|      0.000
      Inverters       |                  11|         6|      0.158
      Clock-Gates     |                   0|         0|      0.000
      Combinational   |                  52|        62|      1.417
      Latches         |                   3|         8|      0.123
      FlipFlops       |                   6|        27|      0.475
       Single-Bit FF  |                   6|        27|      0.475
       Multi-Bit FF   |                   0|         0|      0.000
       Clock-Gated    |                   0|          |
       Bits           |                   6|        27|      0.475
         Load-Enabled |                   0|          |
         Clock-Gated  |                   0|          |
  Tristate Pin Count  |                   0|          |
Physical Info         |Placed              |          |
  Chip Size (mm x mm) |0.073 x 0.073       |      5343|
  Fixed Cell Area     |                    |         0|
    Phys Only         |                   0|         0|
  Placeable Area      |                    |       163|
  Movable Cell Area   |                    |       103|
  Utilization (%)     |                  63|          |
  Chip Utilization (%)|                  63|          |
  Total Wire Length (mm)|               0.842|          |
  Longest Wire (mm)   |                0.044|          |
  Average Wire (mm)   |                0.032|          |
----------------------+--------------------+----------+-----------
```

path.rpt file:

```
Report Path Groups:
-----+-------+------+---------+---------
     | Path  |Weight|Critical |Worst
     | Group |      |Range(ps)|Slack(ps)
-----+-------+------+---------+---------
1    |default| 1.000|      0.0|<unc>
2    |I2R    | 1.000|      0.0|    489.4
3    |I2O    | 1.000|      0.0|<ill>
4    |R2O    | 1.000|      0.0|    238.9
-----+-------+------+---------+---------
```

time.rpt file (it is included to show the slack of the default path group):

```
Report for group default
--------------------------------------------------------------------------------------------------------------
Startpoint: counter/Q_reg[0]/Q
    (Clocked by sysclk R)
Endpoint: counter/Q_reg[1]/D
    (Clocked by sysclk R)
Path Group: default
Data required time: 968.3
    (Clock shift: 1000.0, minus Uncertainty: 0.0, plus Latency 0.0, minus Setup time: 31.7)
Data arrival time: 370.7
Slack: 597.6
Logic depth: 4
--------------------------------------------------------------------------------------------------------------
```

power.rpt file:

```
Report Power (instances with prefix '*' are included in total) :
-----+-----------------+--------------------+--------------------+------------------+-----------------
     | Instance        | Internal Power(uw) | Switching Power(uw) | Leakage Power(uw) | Total Power(uw)
-----+-----------------+--------------------+--------------------+------------------+-----------------
1    |*counter         |          12.970172|           32.886921|          0.610360|        46.467453
2    |*priority_encoder|          33.295689|           65.050598|          0.982816|        99.329102
3    |*state_holder    |          13.352933|           27.481203|          0.341241|        41.175377
4    |*output_decoder  |           2.937685|            9.588662|          0.188646|        12.714994
5    |*i_0_0_0         |           0.364796|            0.204921|          0.026733|         0.596451
6    |*i_0_0_1         |           0.167103|            0.277094|          0.022695|         0.466892
7    |                 |                   |                    |                  |
8    |*TOTAL           |          63.088379|          135.489395|          2.172491|       200.750275
-----+-----------------+--------------------+--------------------+------------------+-----------------
```

Clock period used in this design = 1ns = 1000ps

Score = 0.5 * Movable Cell Area in squm + 0.3 * (clock period in ps – worst slack in ps) + 0.2 * total power in uw = 319.980055