## SIMON FRASER UNIVERSITY

School of Mechatronic Systems Engineering MSE 352 Digital Logic and Microcontrollers Quiz II – Fall 2018



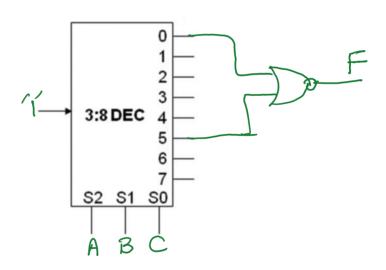
Student Full	Name:			
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Student Number :

- 1. Given the function  $W = (A \oplus C) + B$ ,
  - a) Fill in the truth-table below. (2 marks)

	Α	В	С	W
0=	0	_0_	0	0
	0	0	1	1
	0	1	0	1
	0	1	1	1 1
	1	0	0	1
カミ	1	_0_	1	0
	1	1	0	A
	1	1	1	1

b) Given the truth table of part (a), implement W using a single 3:8 decoder shown below and no more than a single 2-input NOR gate. (4 marks)



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2. On the following graph, inputs CLK and D are shown. They are inputs to both a D latch and a D flip-flop. CLK goes into the EN of the D latch. Write the output of the D latch as  $Q_{DL}$  on the graph. Then write the output of the D flip-flop as  $Q_{DFF}$  on the graph. Both outputs are initially 0 at the start of the graph, as shown. Do the two outputs differ, and if so, why?

the graph. Then write the output of the D flip-flop as  $Q_{DFF}$  on the graph. Both outputs are initially 0 at the start of the graph, as shown. Do the two outputs differ, and if so, why?

Either of the following answers are be a view to the following answers are be a view to the following answers.

1) If the FF is positive edge Sensitive

CLK

D

QDEF

2-If the D-FF is negative edge Sensitive.