

ANALOG IC DESIGN HIGH SPEED SERIAL LINKS (HSSL)



Team members

Transmitter	Receiver	Timing
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--	--	Mohamed Mansour El-Rayany

Introduction

- Why HSSL ?
- 10GBaseKR Standard
- System overview
 - Channel
 - Transmitter
 - Receiver
 - Timing system

Why HSSL?

- Many core system processors

→ Bandwidth increased to Tpbs

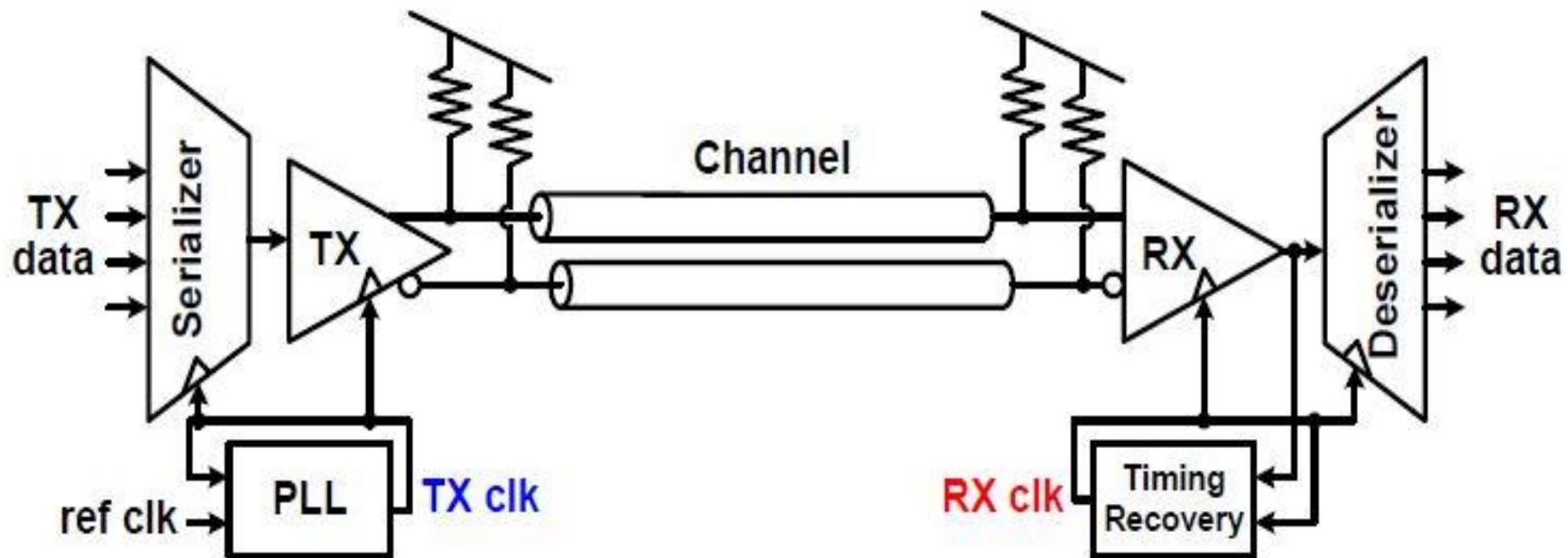
→ Limited number of pins

∴ HSSL

10GBaseKR Standard

10GBaseKR Standard			
	Transmitter		Receiver
Speed	10.3125 Gbps	Speed	10.3125 Gbps
Max. output diff. peak-peak	1.2V	Max. input diff. peak-peak	1.2V
Max. jitter	0.28 UI	Max Jitter	0.13 UI
Programmable Equalization (3-tap FIR)		AC coupling	
CM voltage limit	0 - 1.9		

System overview



Channel

- Limited channel bandwidth
- High frequency attenuation and dispersion
- Inter symbol interference (ISI)

Tx & Rx

□ Transmitter

- Serializer
- 3-Tap FIR

□ Receiver

- AFE
- ADC
- 3-Tap DFE & 2-tap FFE

Timing System

- Phase locked loop (PLL) at Tx side
- PLL at Rx side with CDR

TRANSMITTER

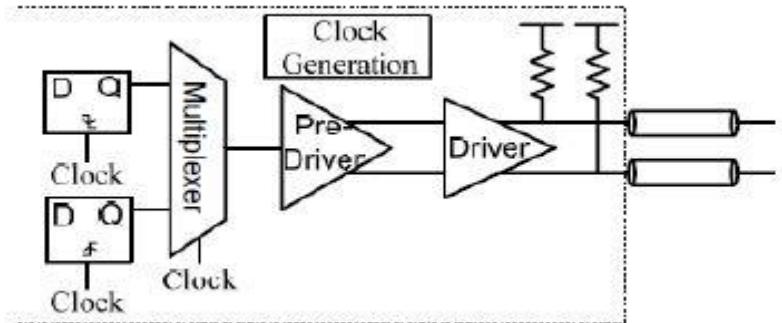


Transmitter system overview

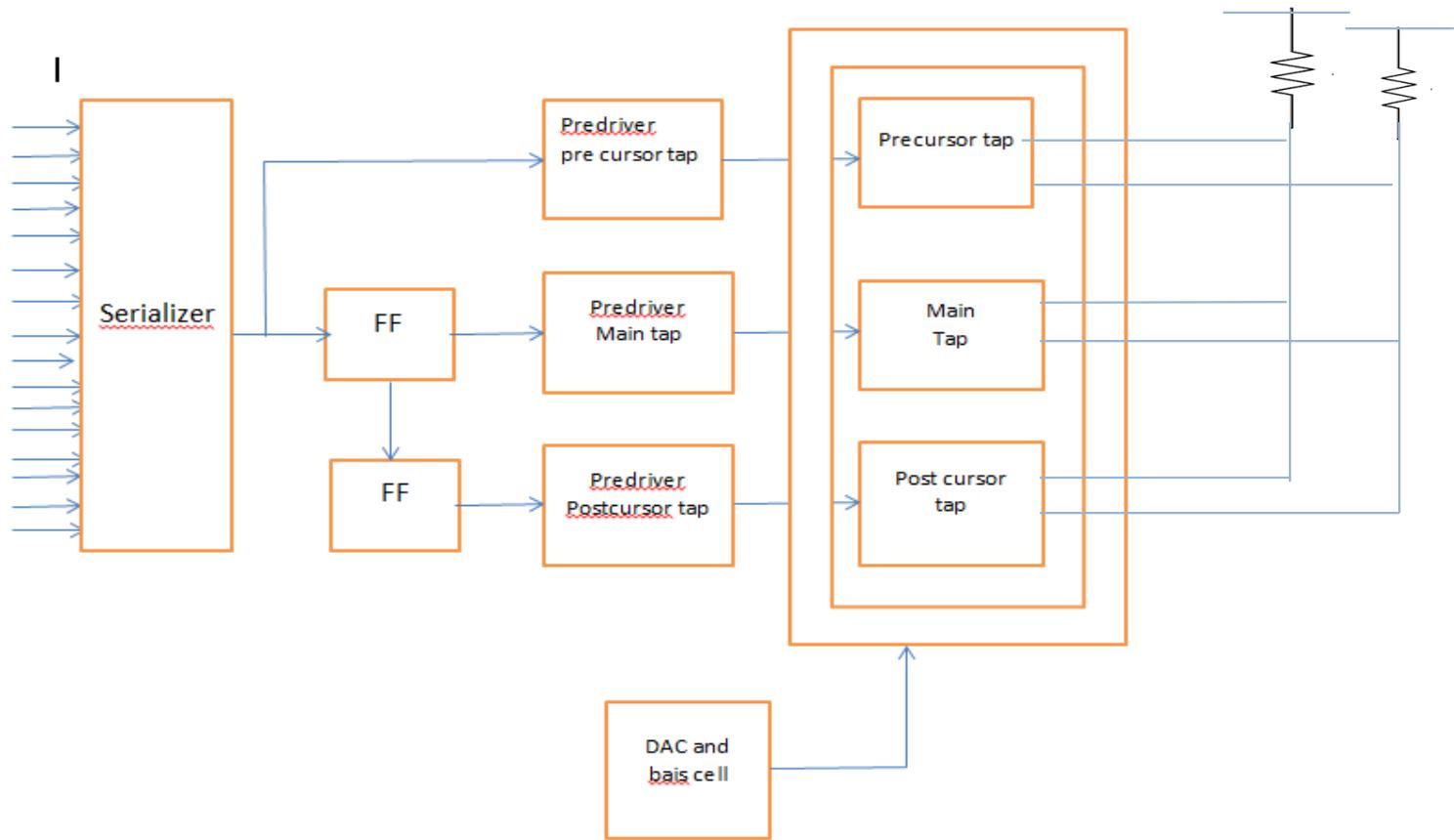
- Serializer.
- Three tap FIR equalizer.

Conceptual I/O Transmitter

- **Goals**
- High bit rate
- Low power consumption
- Low noise, free of unnecessary time-domain spikes.
- Low coupling to other links



System Overview



Multiplexer

Multiplexer

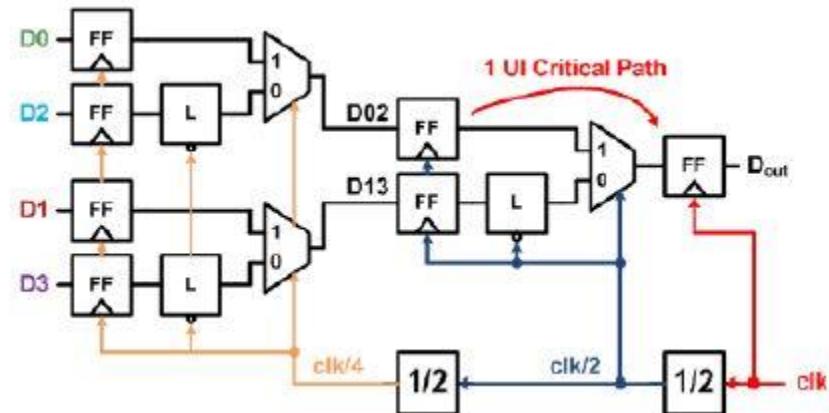
- Introduction.
- Different architectures.
- Topologies.
- Results.
- Power budget.
- Corner results.

Introduction

- High-speed links can be limited by both the channel and the circuits.
- Multiplexing circuitry also limits maximum data rate.

Different Architectures

- Full rate architecture.
- Advantages:
 - Relaxes duty cycle of the clock.
- Disadvantages:
 - Need to generate and distribute high speed clock.
 - Need to design high speed flip-flop.

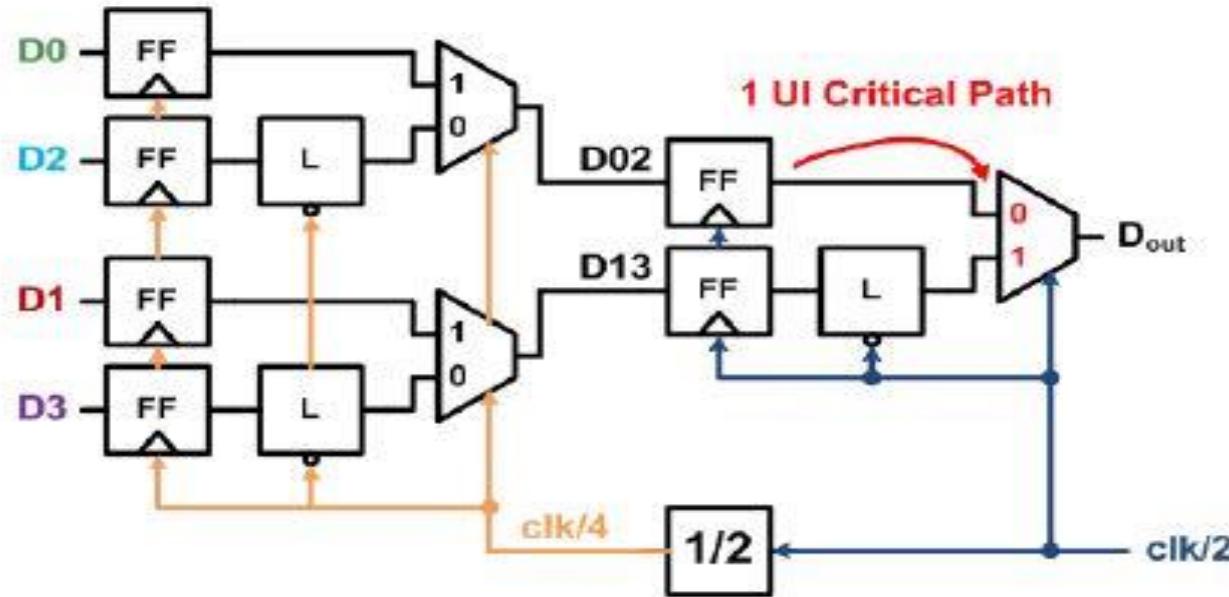


Half Rate Architecture

- Half-rate architecture uses 2 clock phases separated by 180° to mux data.
- Advantages:
 - eliminates high-speed clock and flip-flop.
- Disadvantages:
 - Output eye is sensitive to clock duty cycle..

Half Rate Architecture

Tree architecture

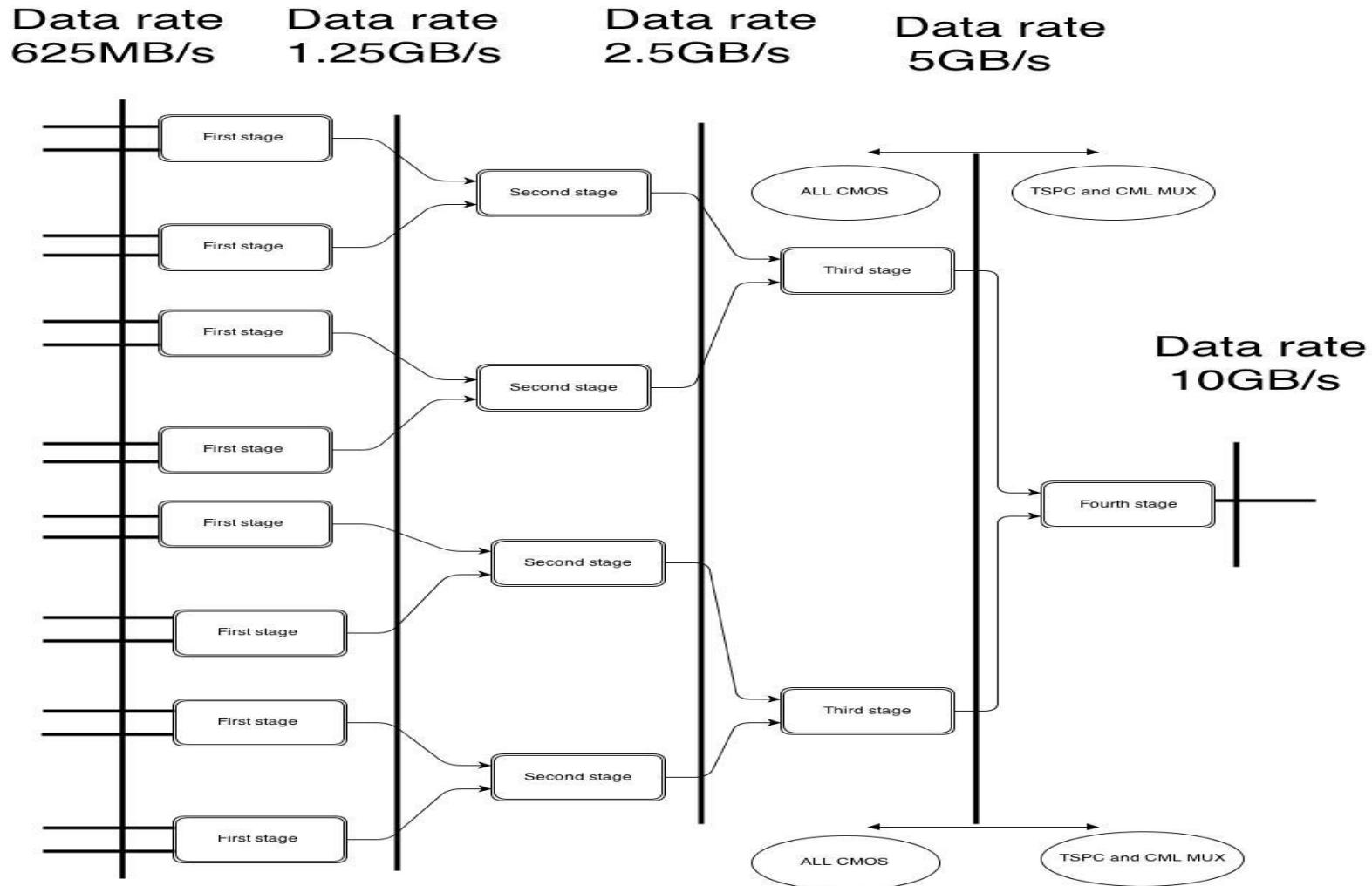


16:1 MUX with 4 stages based on 2_to_1 MUX

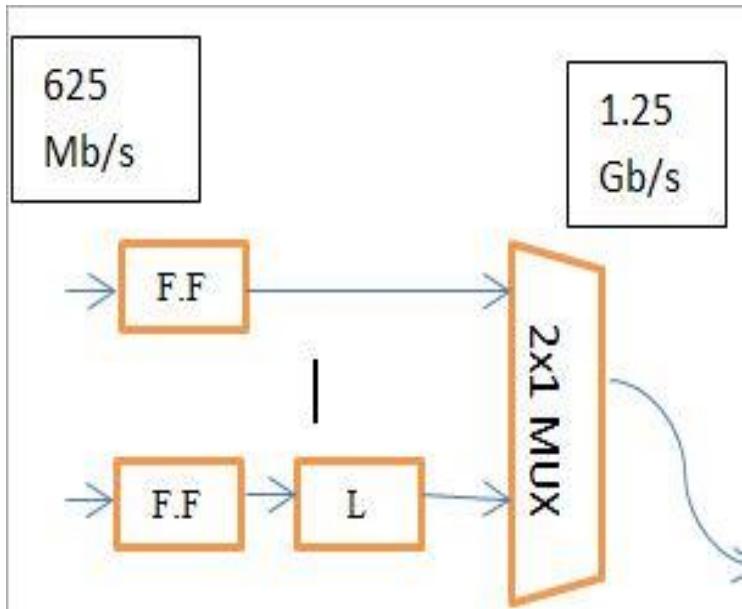
1/4-rate architecture

- 4-phase clock distribution spaced at 90° .
- 90° phase spacing and duty cycle critical for uniform output eye.
- Advantages:
 - Reduce the frequency of the clock .
- Disadvantages:
 - Increase multiplexing factor to allow for lower frequency clock distribution.

Tree Architecture

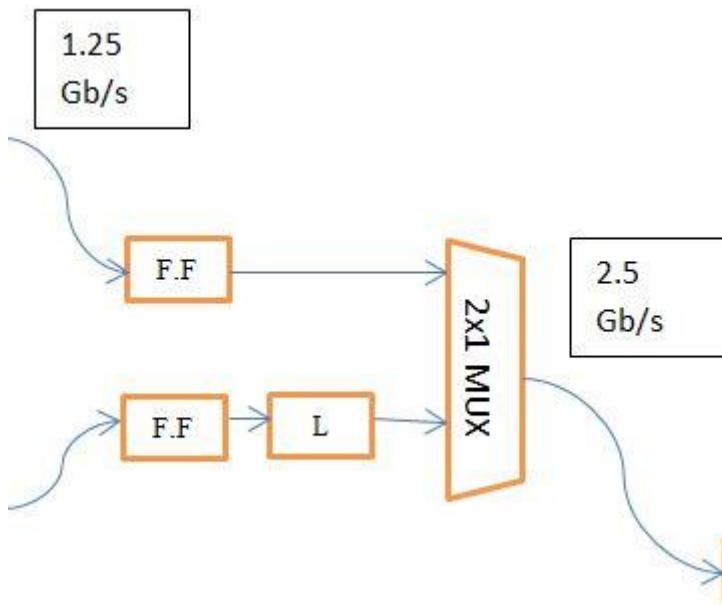


First Stage



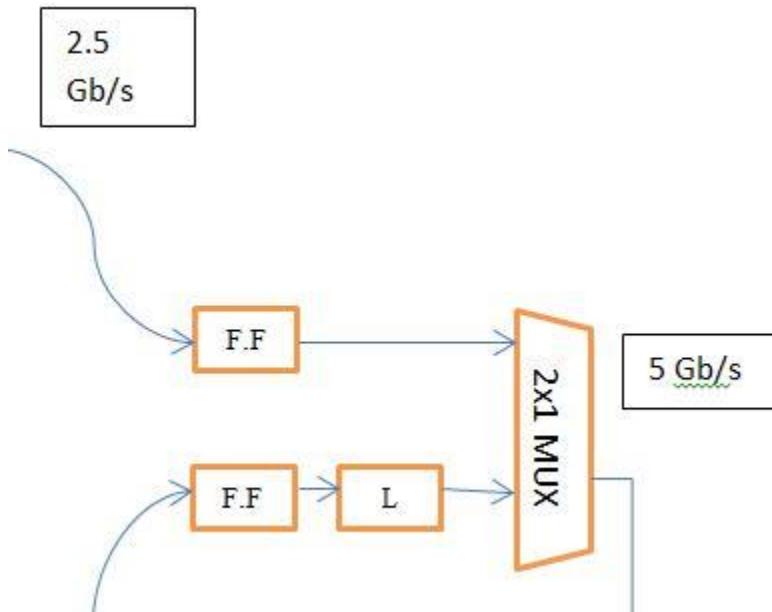
- Input data rate
625Mb/s.
- Output data rate
1.25Gb/s.
- The clock is 625MHz.
- All circuit implemented
in CMOS.

Second Stage



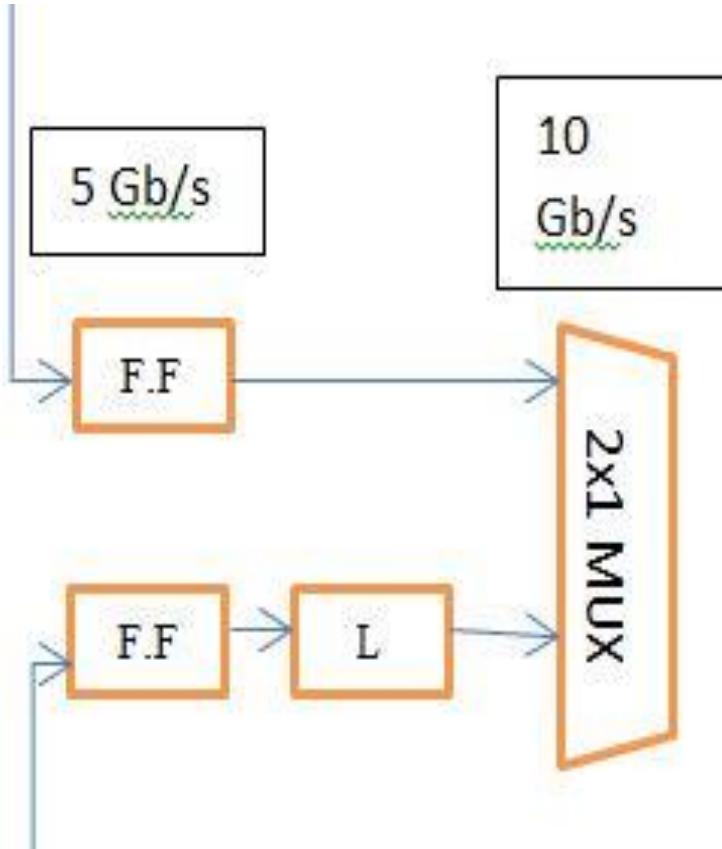
- Input data rate
1.25Gb/s.
- output data rate
2.5Gb/s.
- The clock is 1.25MHZ.
- All circuit implemented
in CMOS.

Third Stage



- Input data rate
2.5Gb/s.
- output data rate
5Gb/s.
- The clock is 2.5MHZ.
- All circuit implemented
in CMOS.

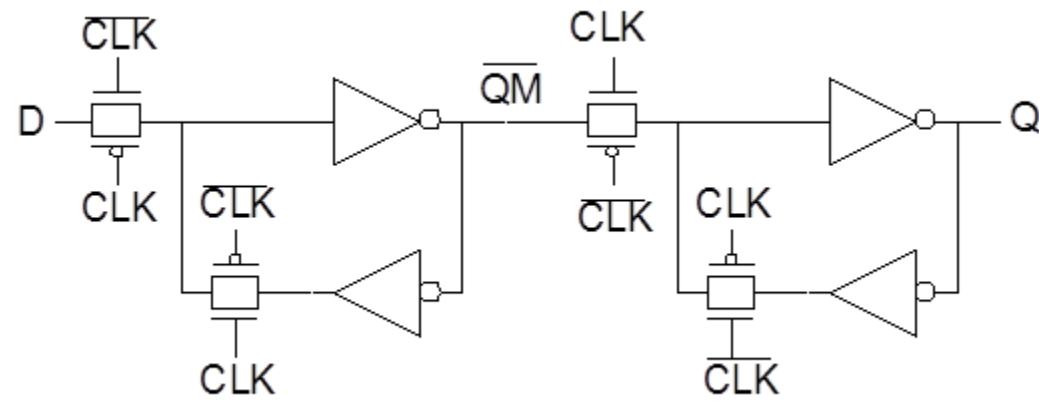
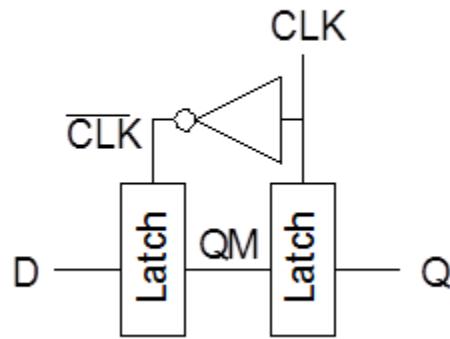
Fourth Stage



- Input data rate 5Gb/s.
- output data rate 10Gb/s.
- The clock is 5MHZ.
- Flip-Flop and Latch are implemented by TSPC.
- 2_1_mux is CML MUX.

Flip Flop

- Built from master and slave D latches



-

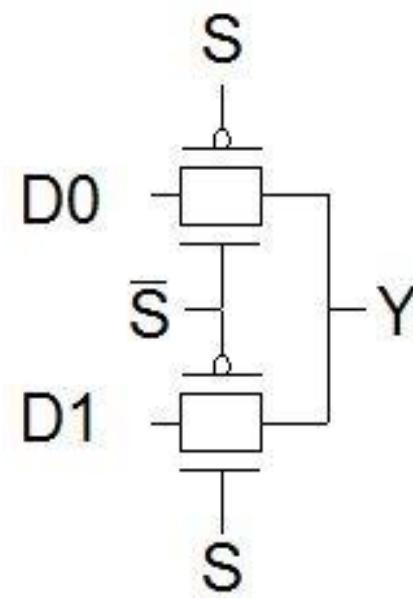
A “negative level-sensitive” latch

A “positive level-sensitive” latch

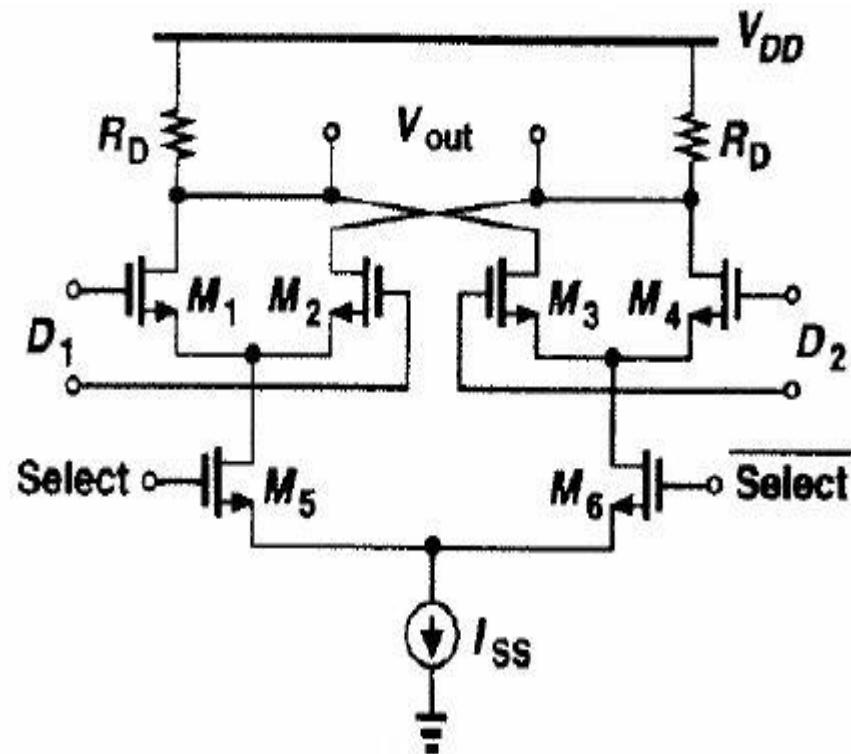
2:1 MUX

- No restoring mux uses two transmission gates.
 - Only 4 transistors

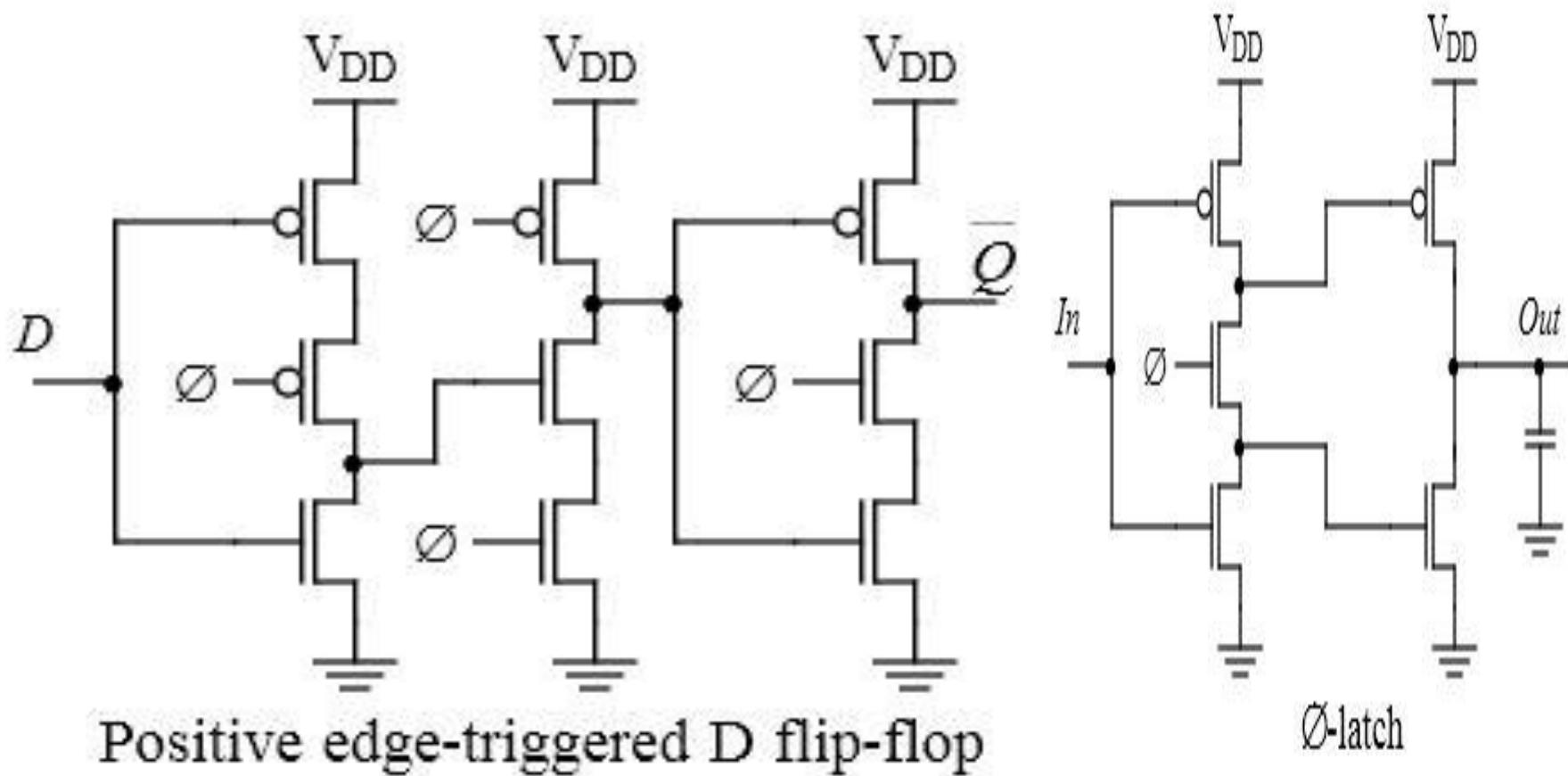
- More efficient.
- Low area.
- Low power.
- High speed than other
- CMOS.



CML MUX

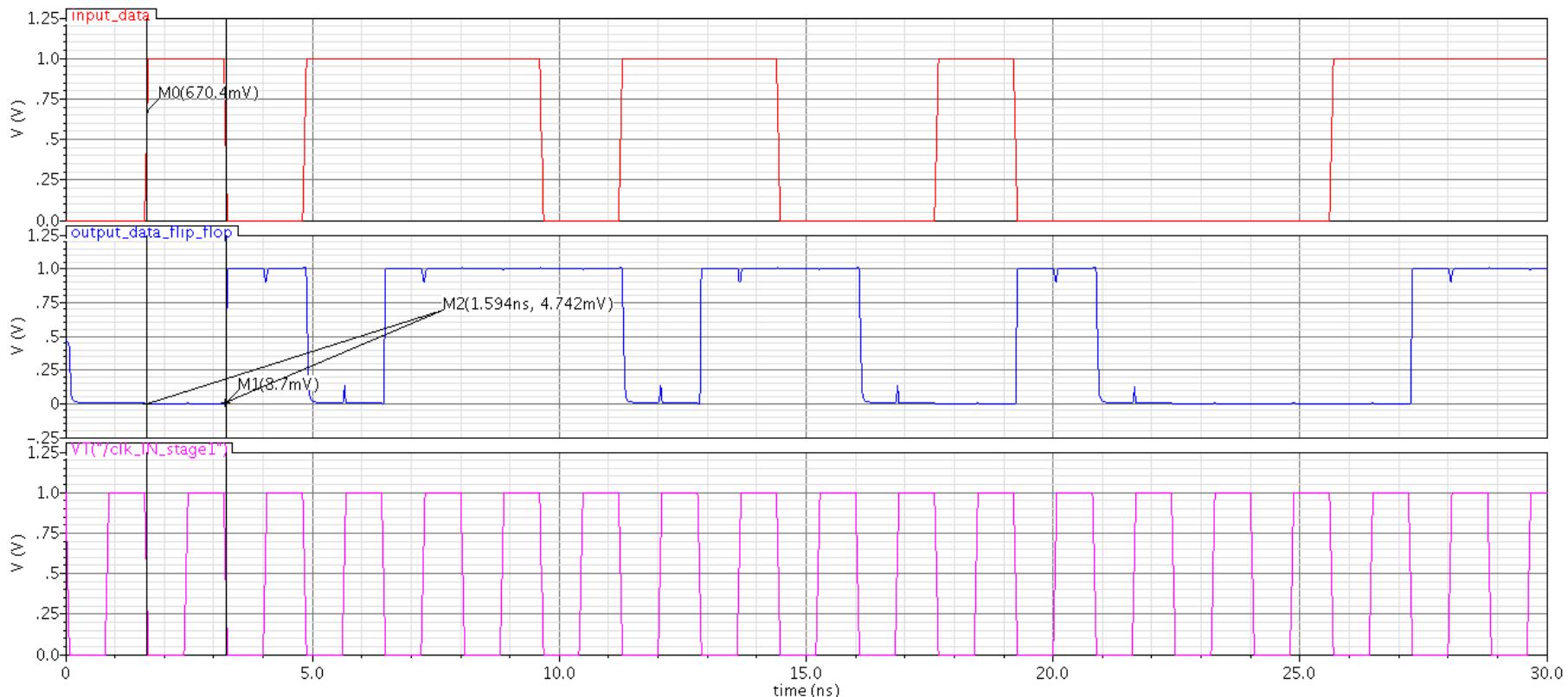


TSPC



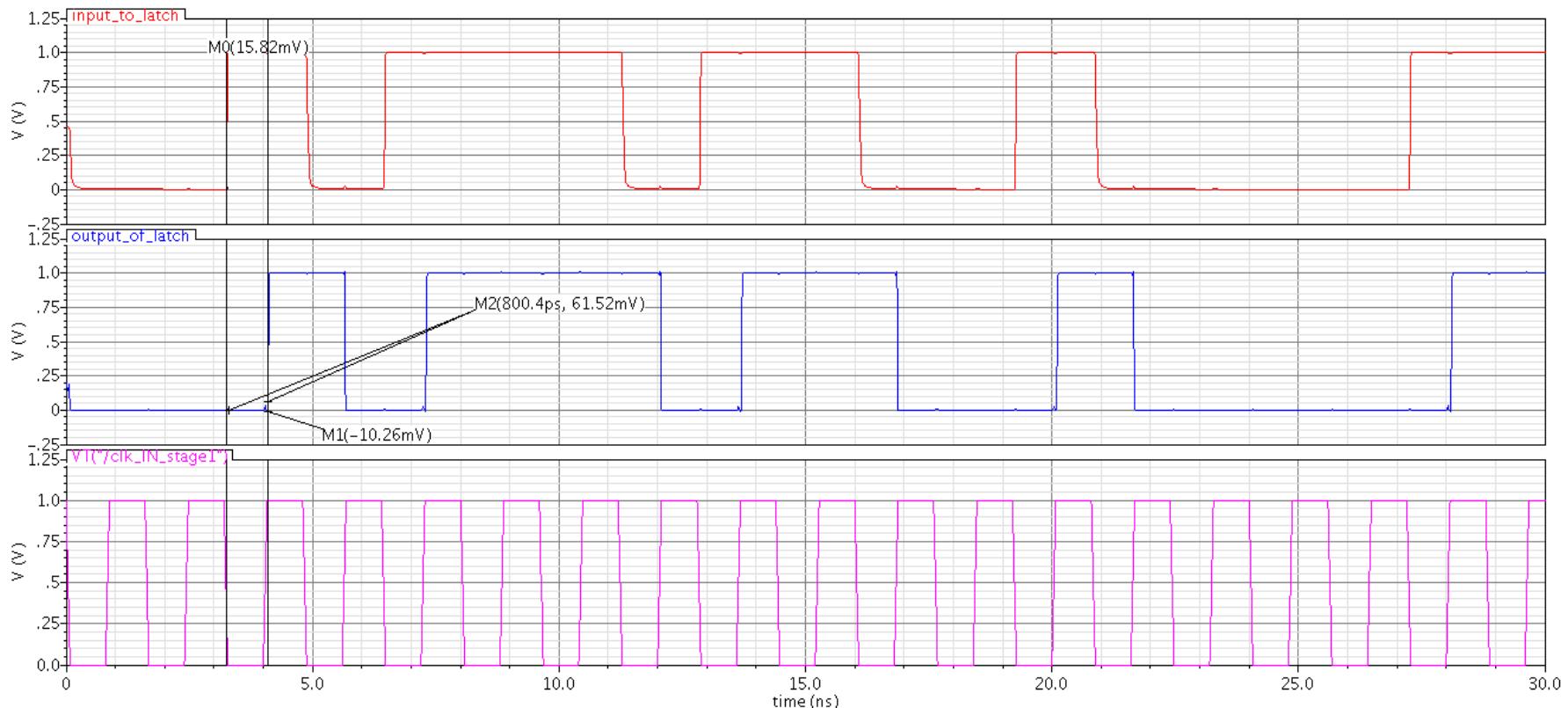
First Stage Result

□ Flip Flop



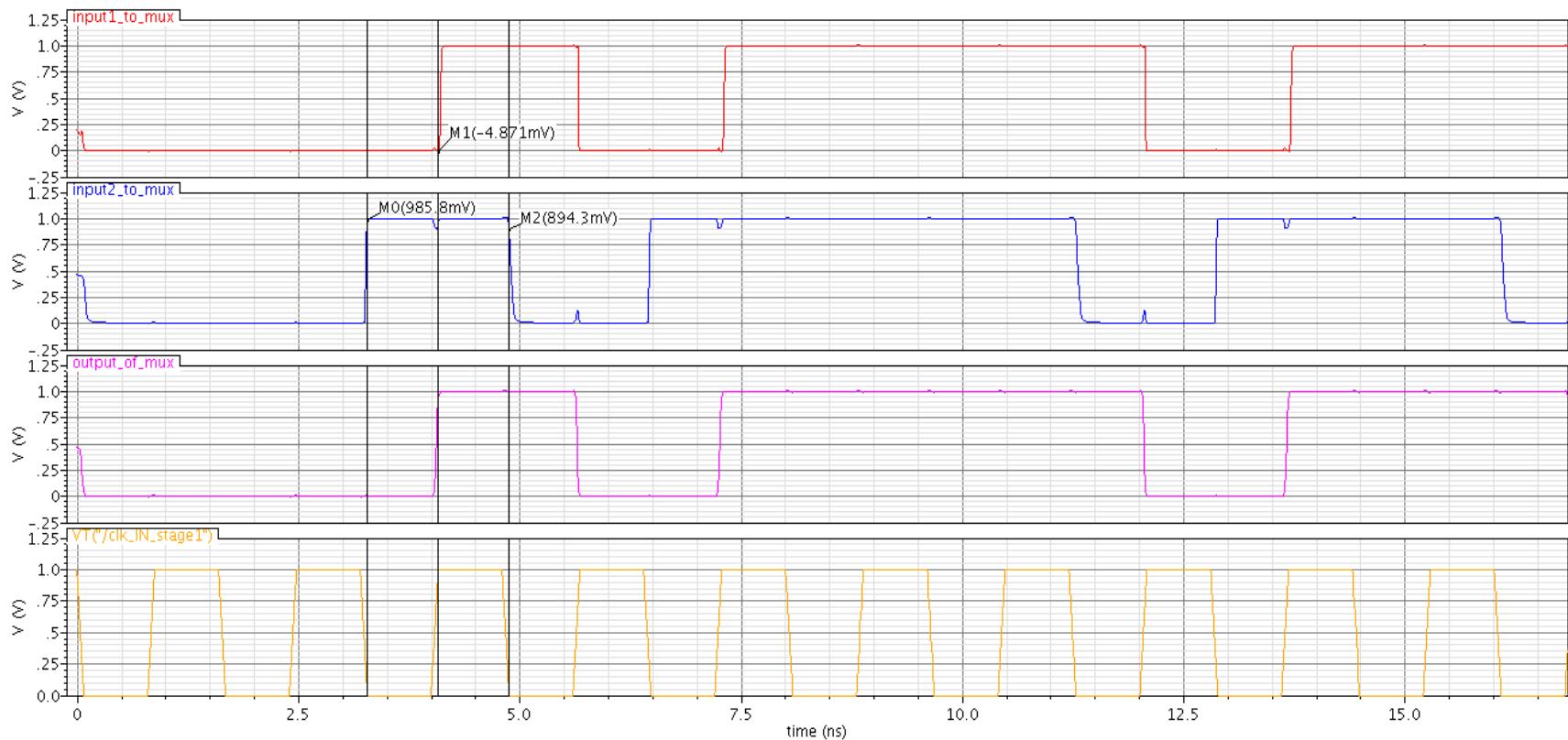
First Stage Result

□ D latch



First Stage Result

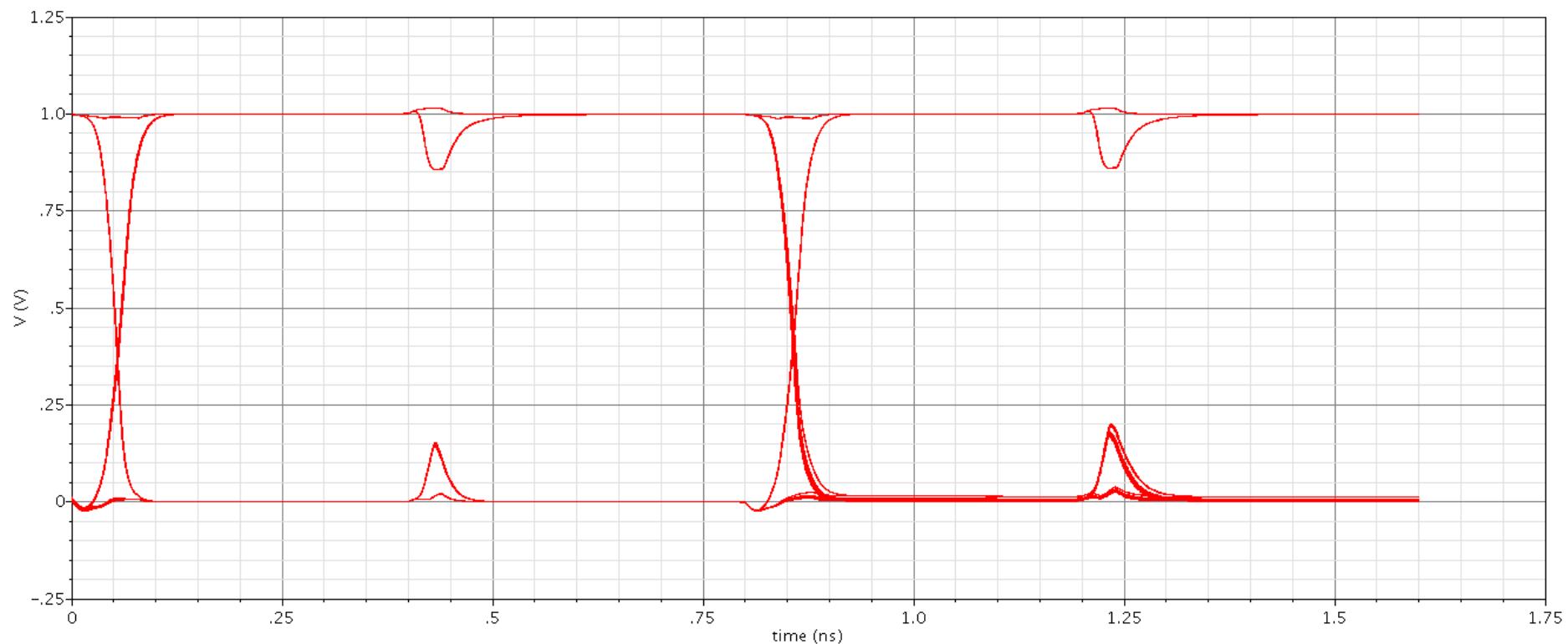
□ 2:1 MUX



First Stage Result

□ Eye diagram

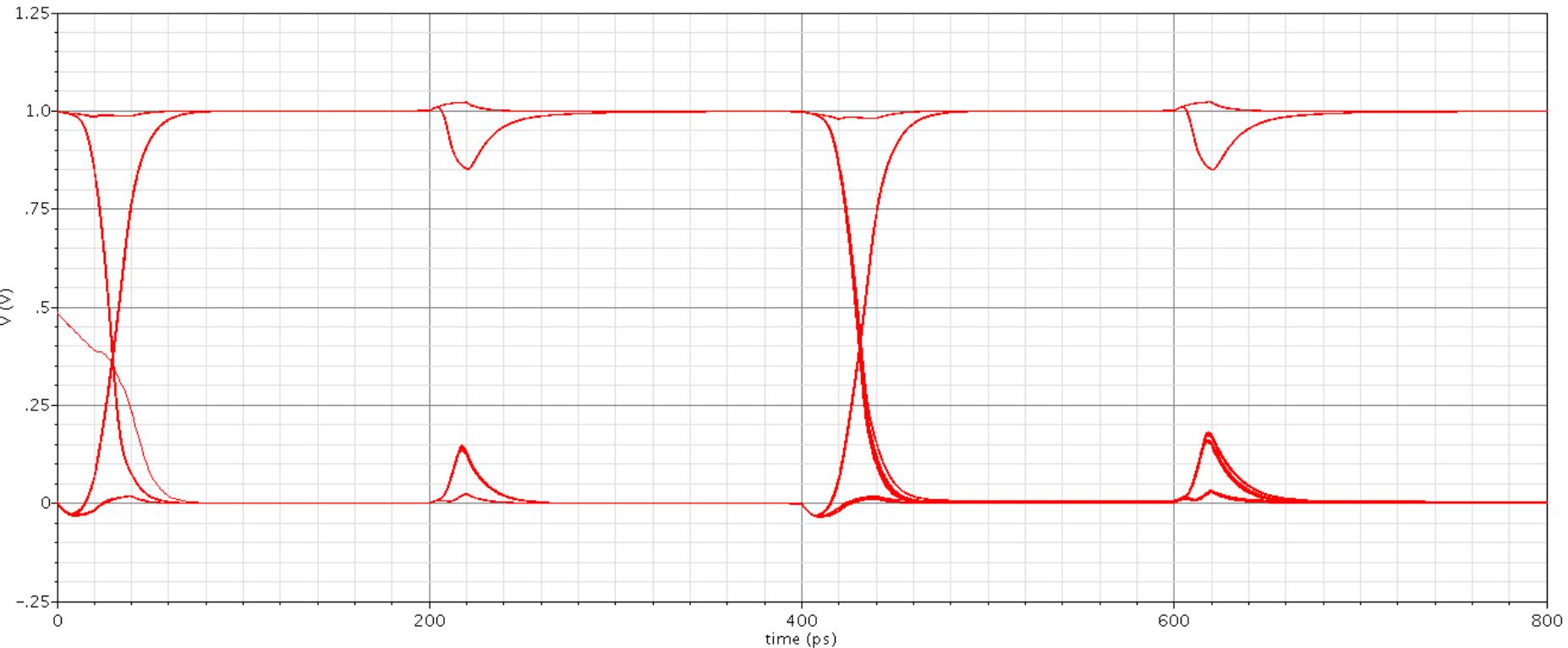
— eyeDiagram(VT("/net40") 0 1e-06 1.6e-09)



Second Stage Result

□ Eye diagram

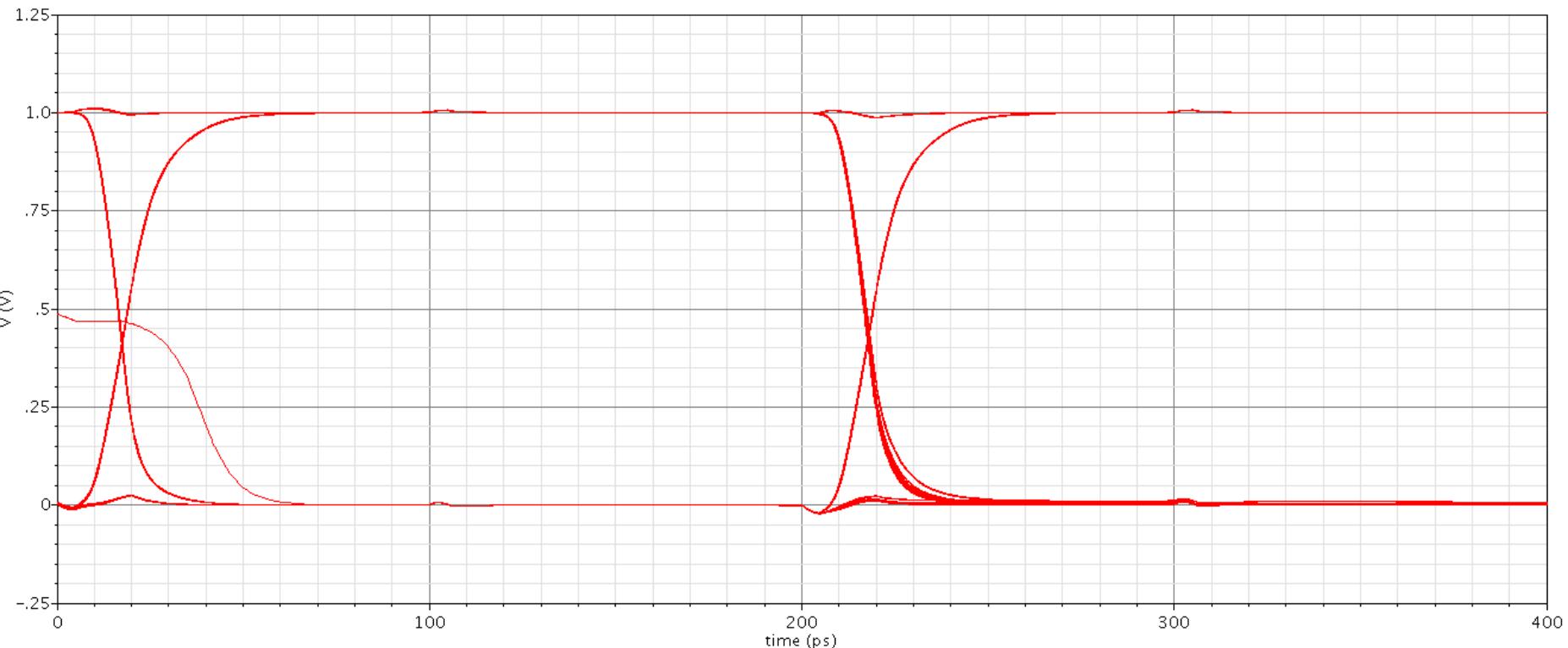
— eyeDiagram(VT("/net60") 0 1e-06 8e-10)



Third Stage Result

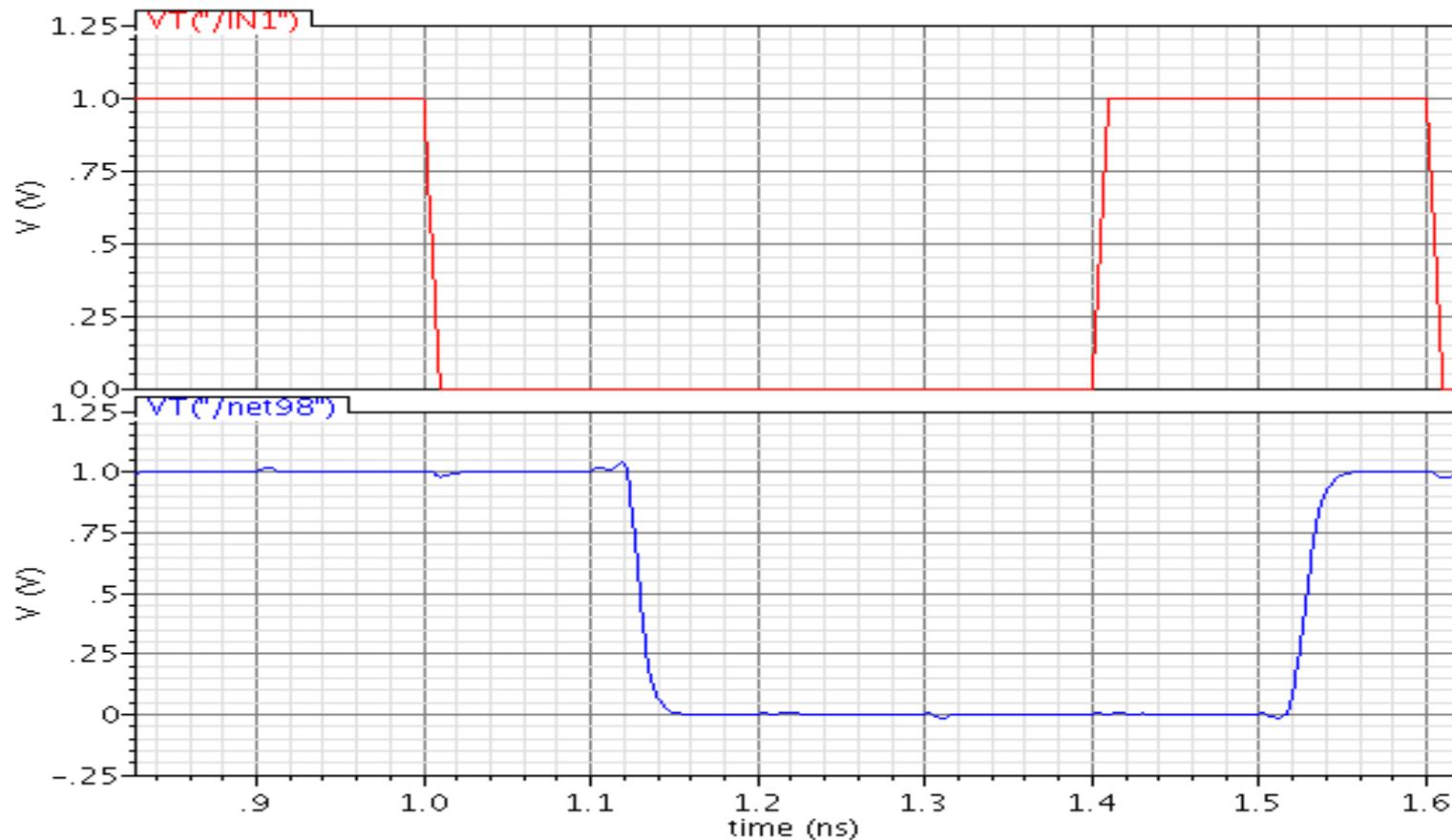
□ Eye diagram

— eyeDiagram(VT("/net70") 0 9e-07 4e-10)



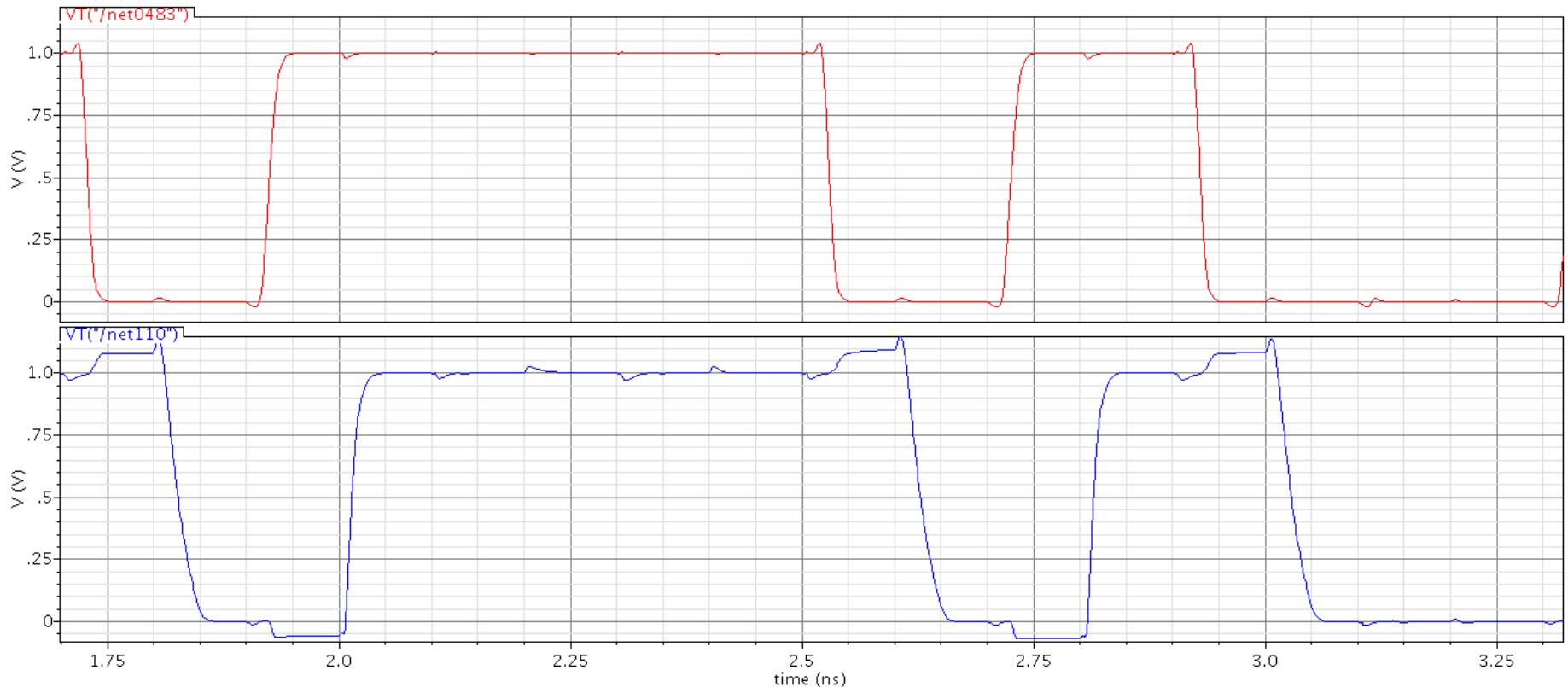
Fourth Stage Result

□ TSPC Flip Flop



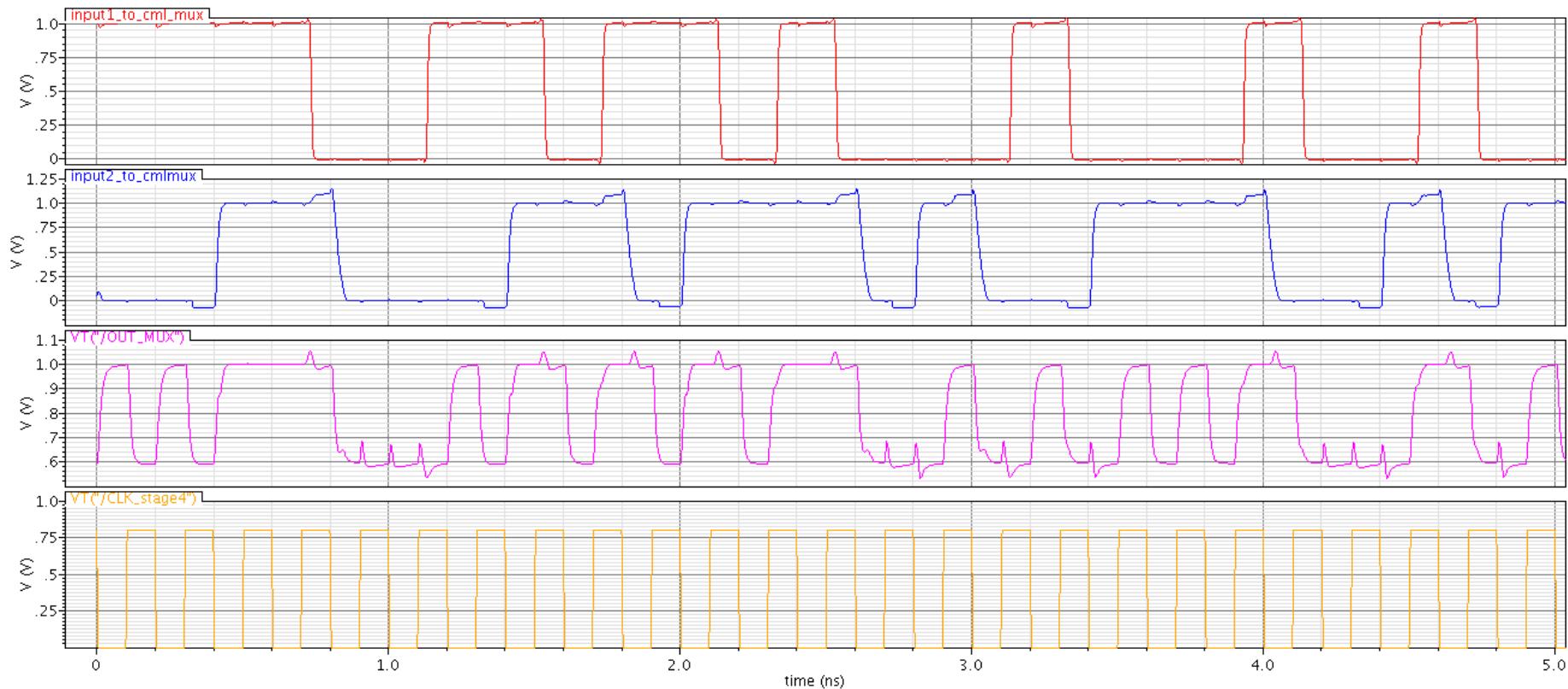
Fourth Stage Result

□ TSPC latch



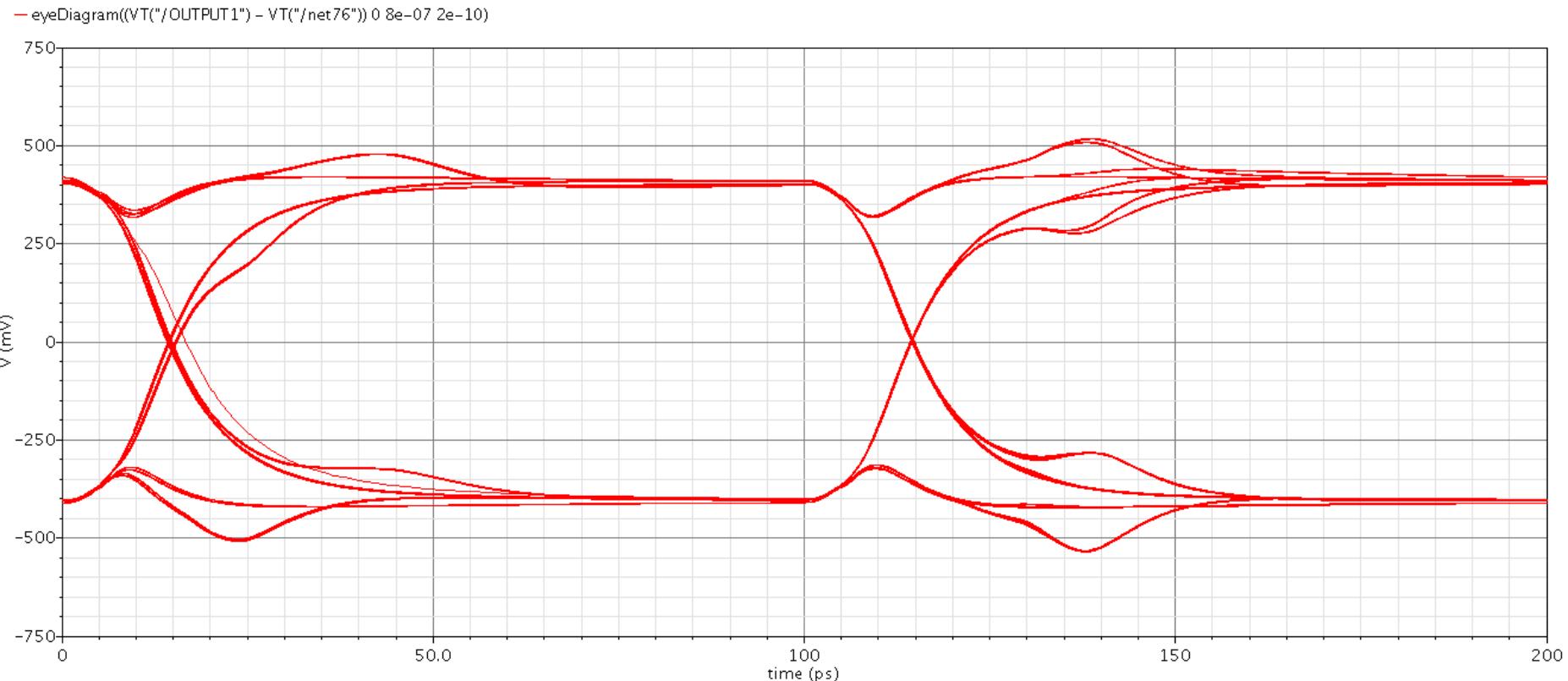
Fourth Stage Result

□ CML MUX



Fourth Stage Result

□ Eye diagram



Power budget

Stage	power
1-First stage	267.056 u watt
2-Second stage	885.57 u watt
3-Third stage	1.77625 m watt.
4-Fourth stage	2.5036 m watt.
5-Total power	11.7348m watt.

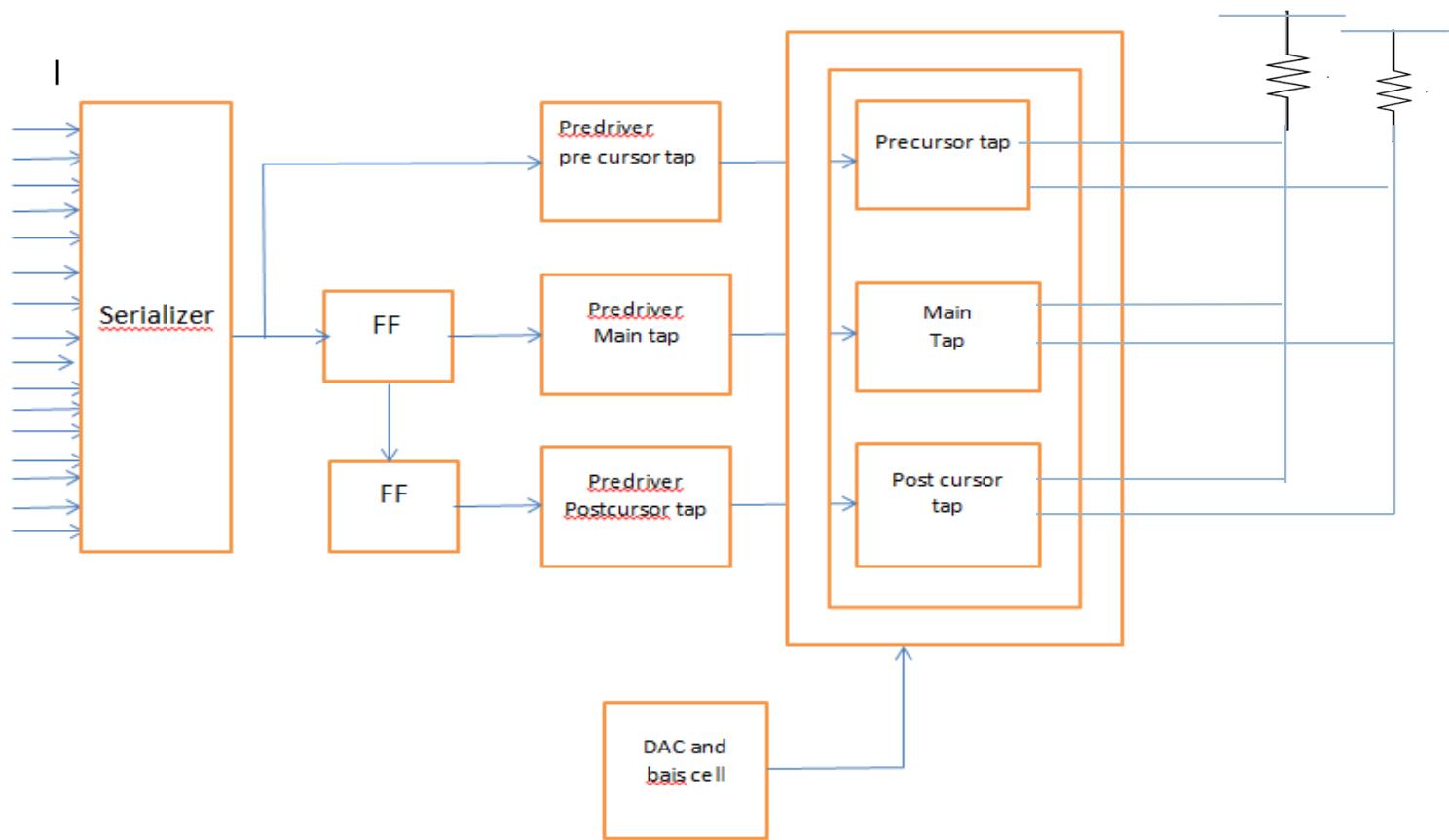
Corner Results

- Ss corner ,ff_res, high_temp
- MUX across this corner which is the worst corner and generate output swing 0.67 mV pp.

TRANSMITTER IN 10GBIT ETHERNET BASE-KR STANDARD

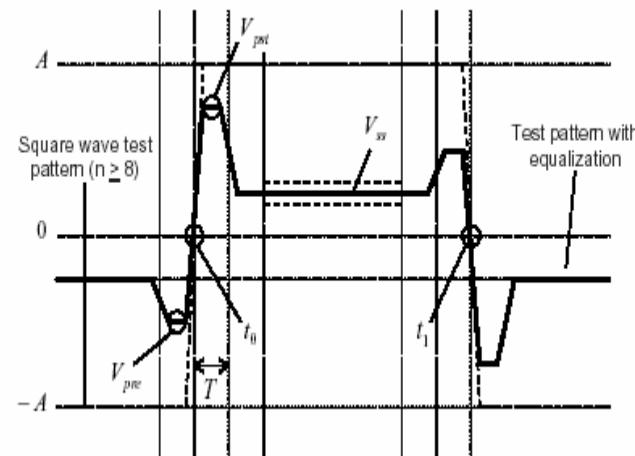
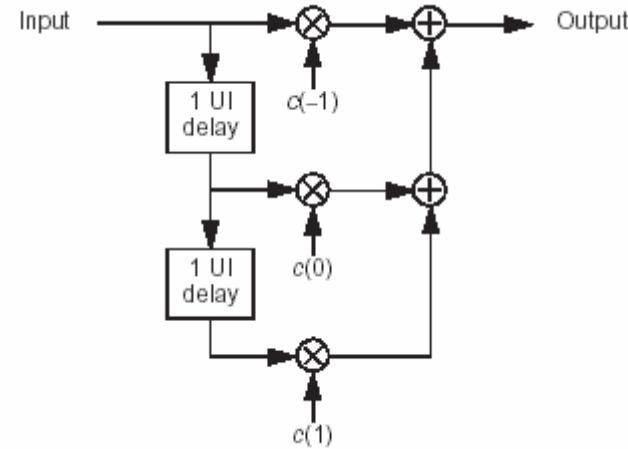


System Overview



3Tap Equalizer With programmable Cofficient

- $V_{pre} = [c(-1) - c(0) - c(1)]V$
- $V_{pst} = [c(-1) + c(0) - c(1)]V$
- $V_{ss} = [c(-1) + c(0) + c(1)]V$
- $A = [-c(-1) + c(0) - c(1)]V$
- C-1 has 8 settings from 0 to -0.175 with step size of at least 0.025.
- C1 has 8 settings from 0 to -0.375 with step size of at least 0.05.



Coefficient Range and Equivalent current

C(-1)	Pre-tap current	C(0)	Main-tap current	C(1)	Post-tap current
0	0mA	1	20mA	0	0mA
-0.025	0.5mA	0.925	18.5mA	-0.05	1mA
-0.05	1mA	0.85	17mA	-0.1	2mA
-0.075	1.5mA	0.775	15.5mA	-0.15	3mA
-0.1	2mA	0.7	14mA	-0.2	4mA
-0.125	2.5mA	0.625	12.5mA	-0.25	5mA
-0.15	3mA	0.55	11mA	-0.3	6mA
-0.175	3.5mA	0.475	9.5mA	-0.35	7mA

Range of coefficient

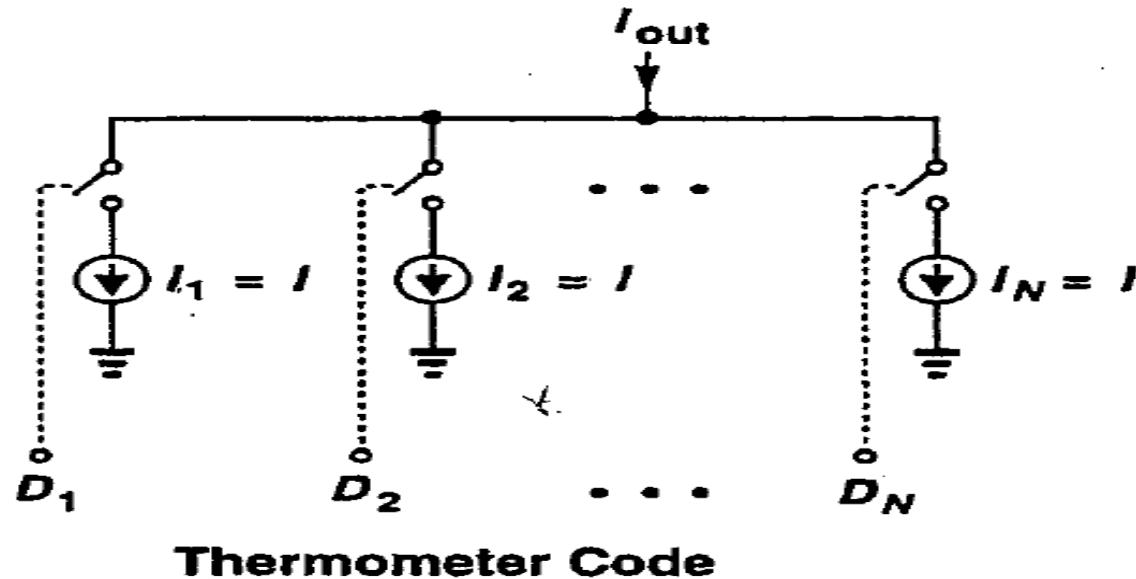
Equalizer has -26db of frequency peaking

- Attenuates DC at -26db and passes Nyquist frequency at 0dB

Digital to analog converter

□ Segmented current arrays

- All current sources are equal and controlled by thermometer code so that when digital input increases by 1 LSB , one additional current is switched to output.



current segmented arrays

Advantages

- Guarantee monotonicity: the transfer characteristics of such arrays is monotonic function of input .
- Cancel the glitches that lead to large DNL ,since it's controlled by thermometer coding .

Matching

- Analyze performance of mismatch on circuit :-

- Systematic Mismatch

ΔV_{DS}

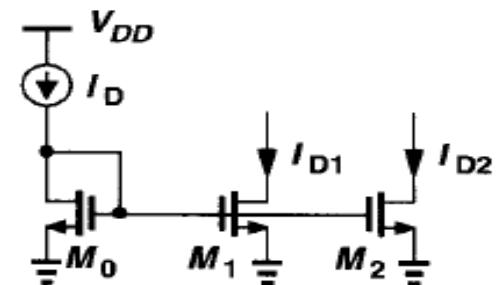
- Random Mismatch

$$I_d = \frac{I_{d1} + I_{d2}}{2}$$

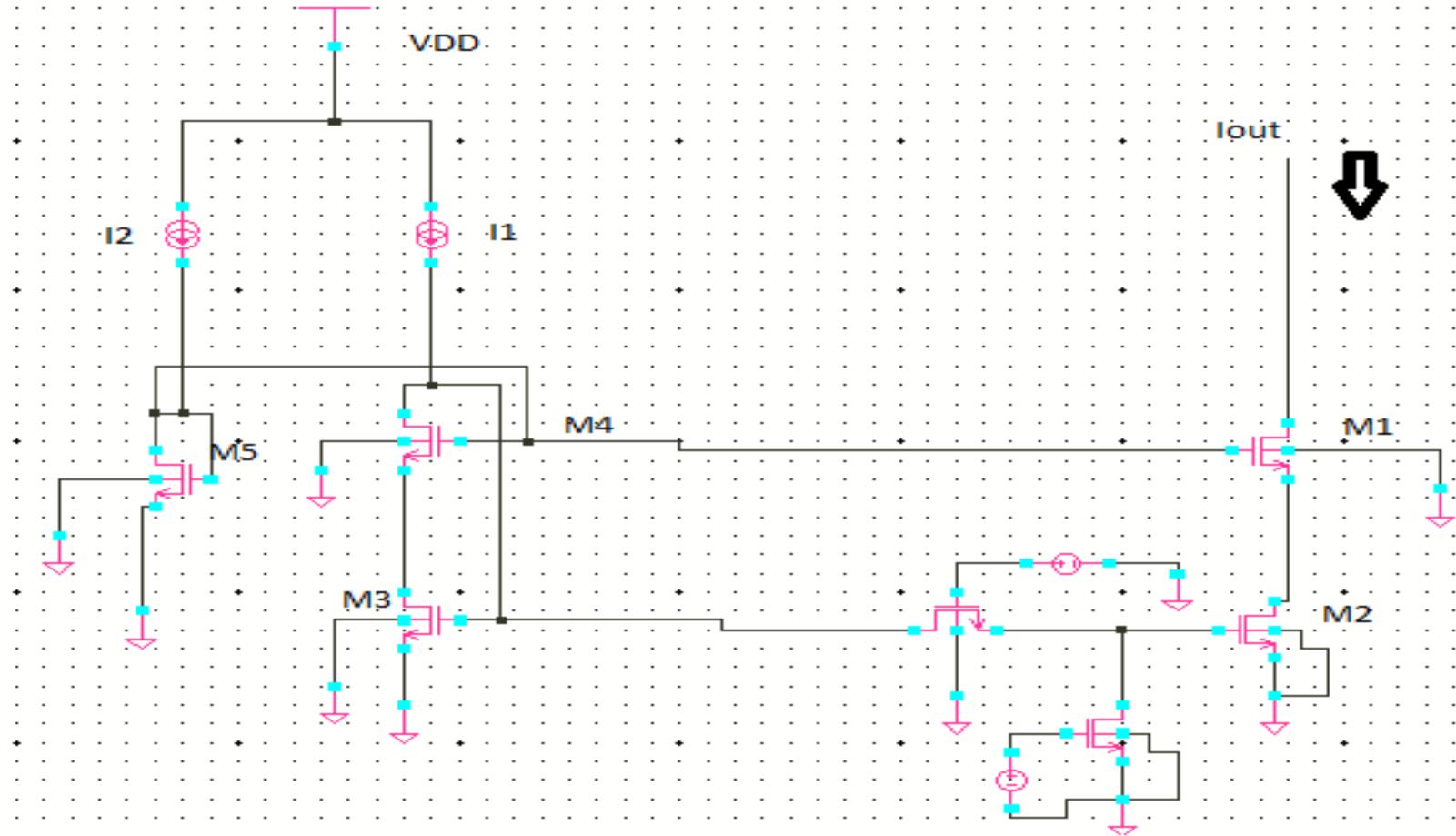
$$\frac{\Delta I_d}{I_d} = \frac{I_{d1} - I_{d2}}{I_d}$$

$$\frac{\Delta I_d}{I_d} = \frac{\Delta W/L}{W/L} + \frac{\Delta V_{th}}{V_{th}}$$

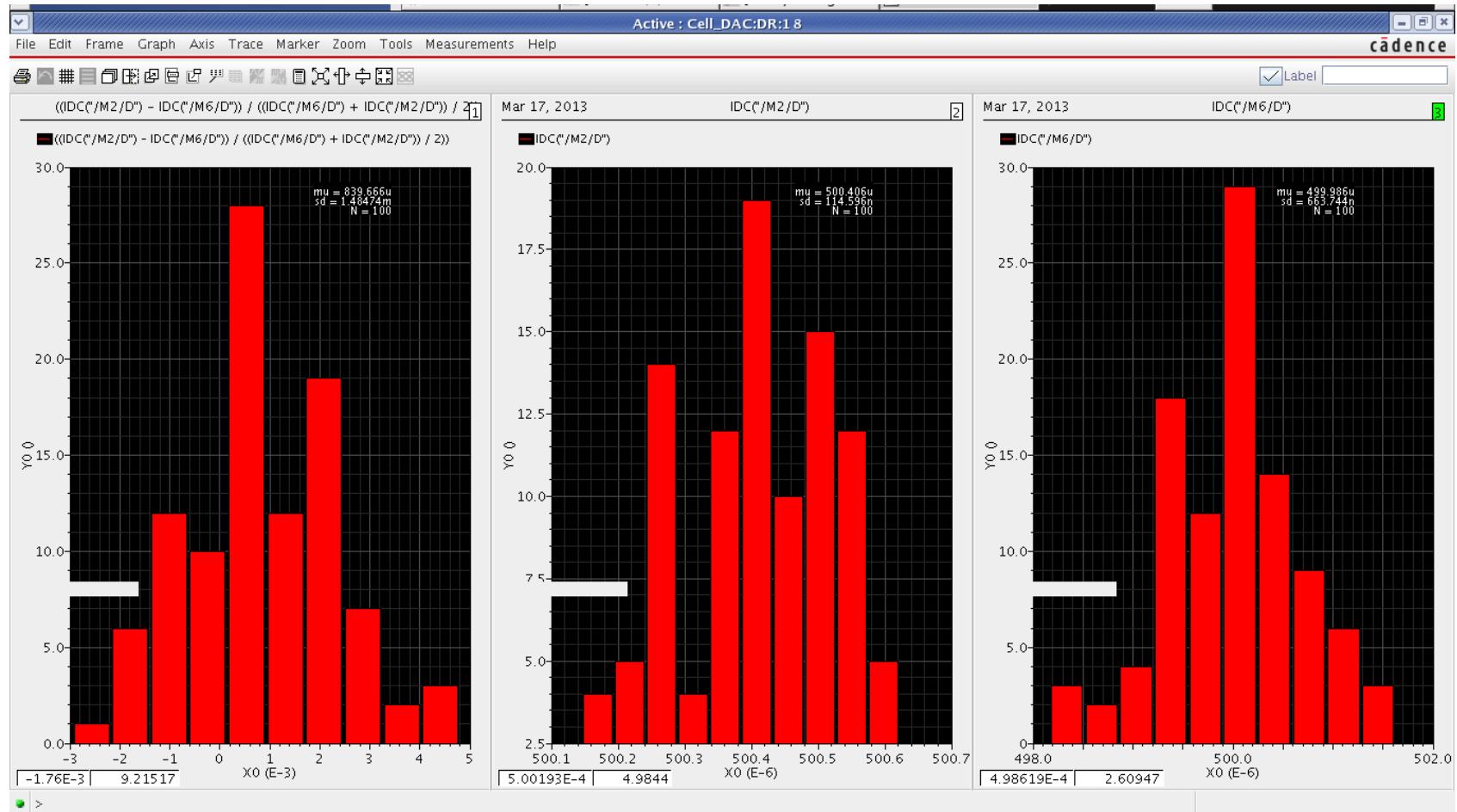
- Larger device area less mismatch effect
- Larger gate-overdrive less threshold mismatch



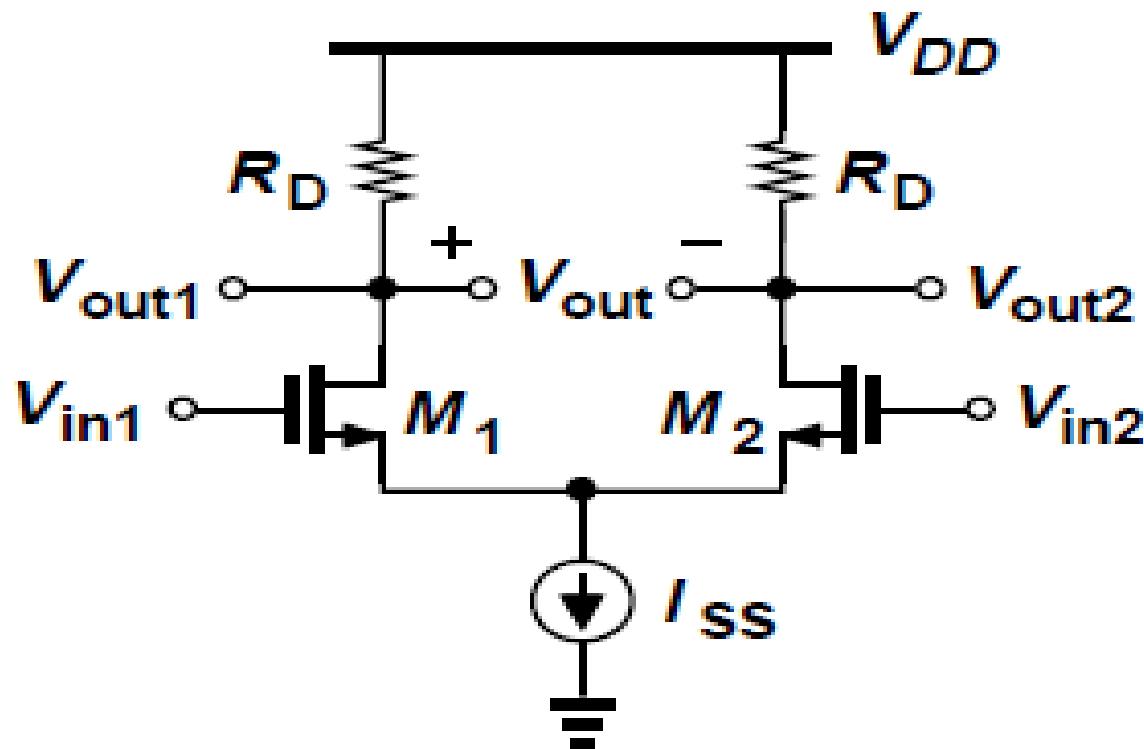
Cascode current mirror



Monte Carlo simulation

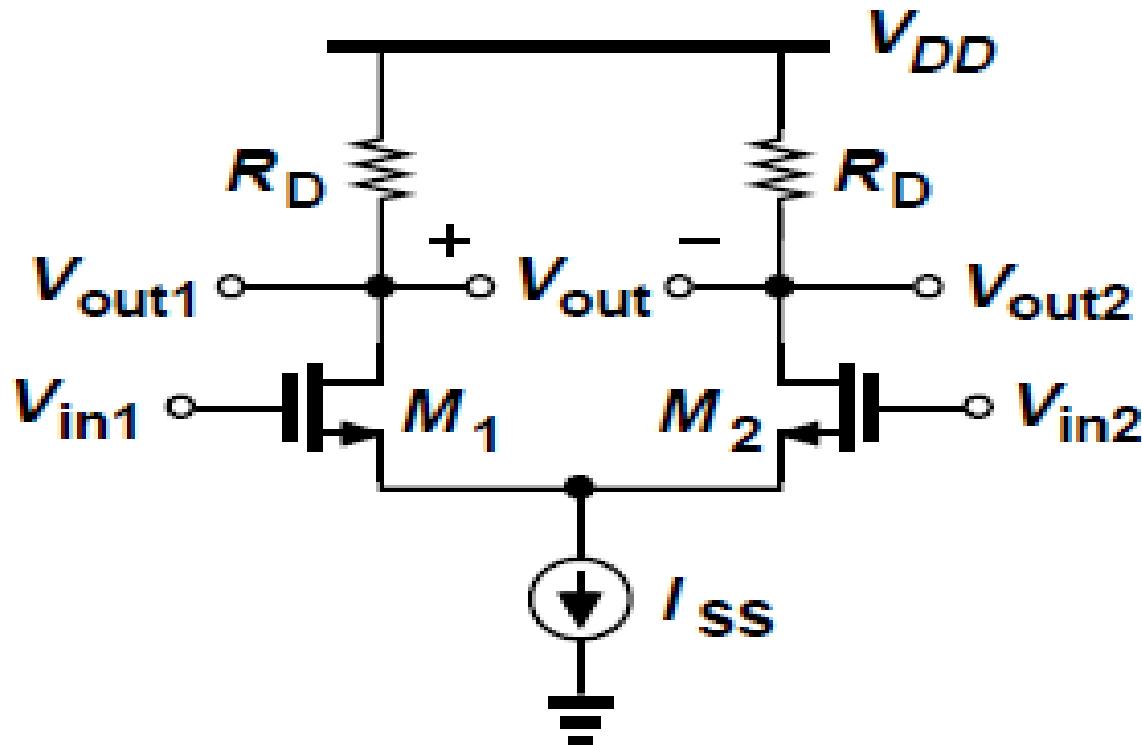


Drivers

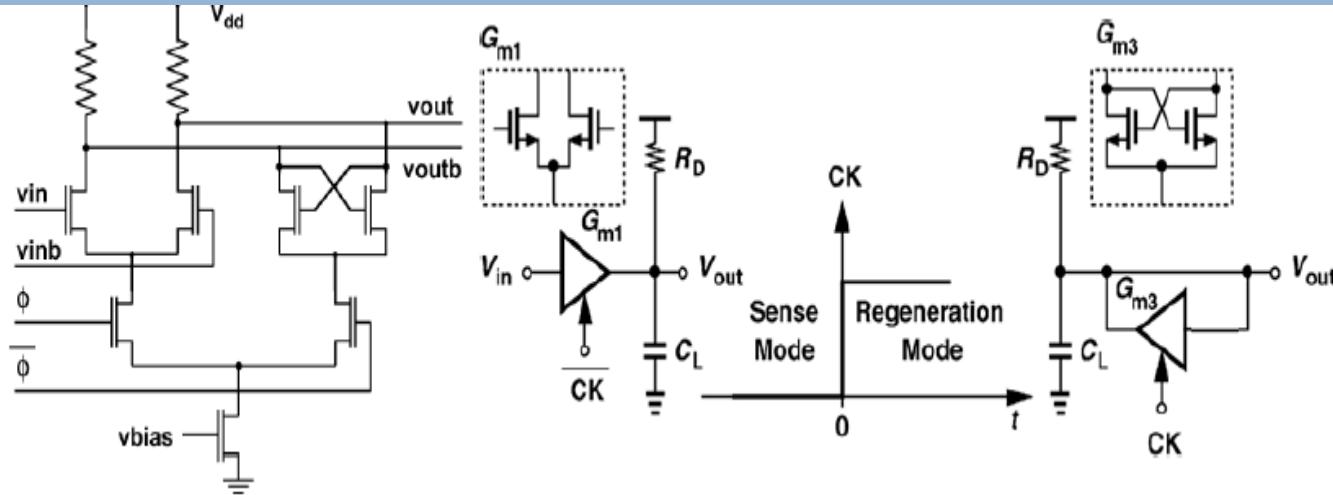


CML pre drivers

□ Capacitance driving



CML Latch Operation



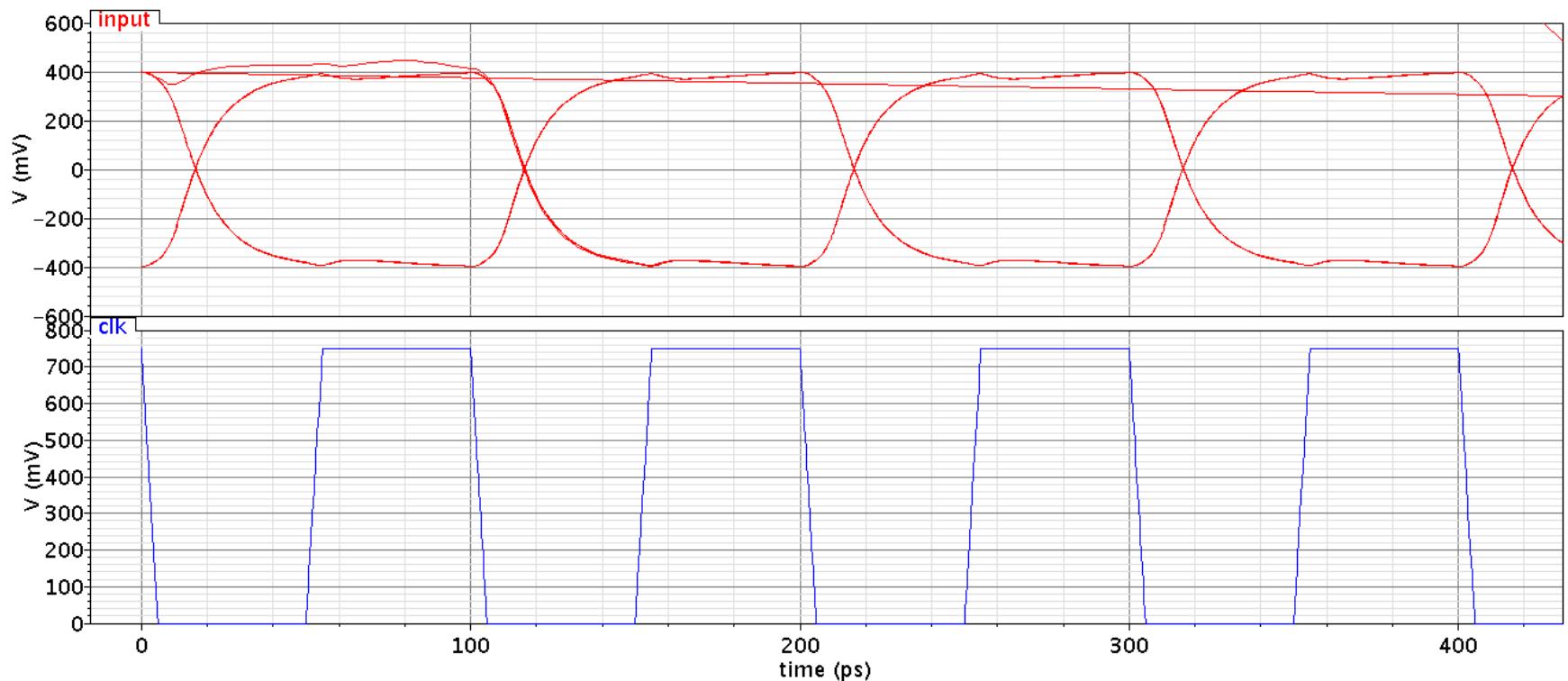
At the beginning of regeneration phase :

$$V_{out}(0) = g_m R_D v_{in}$$

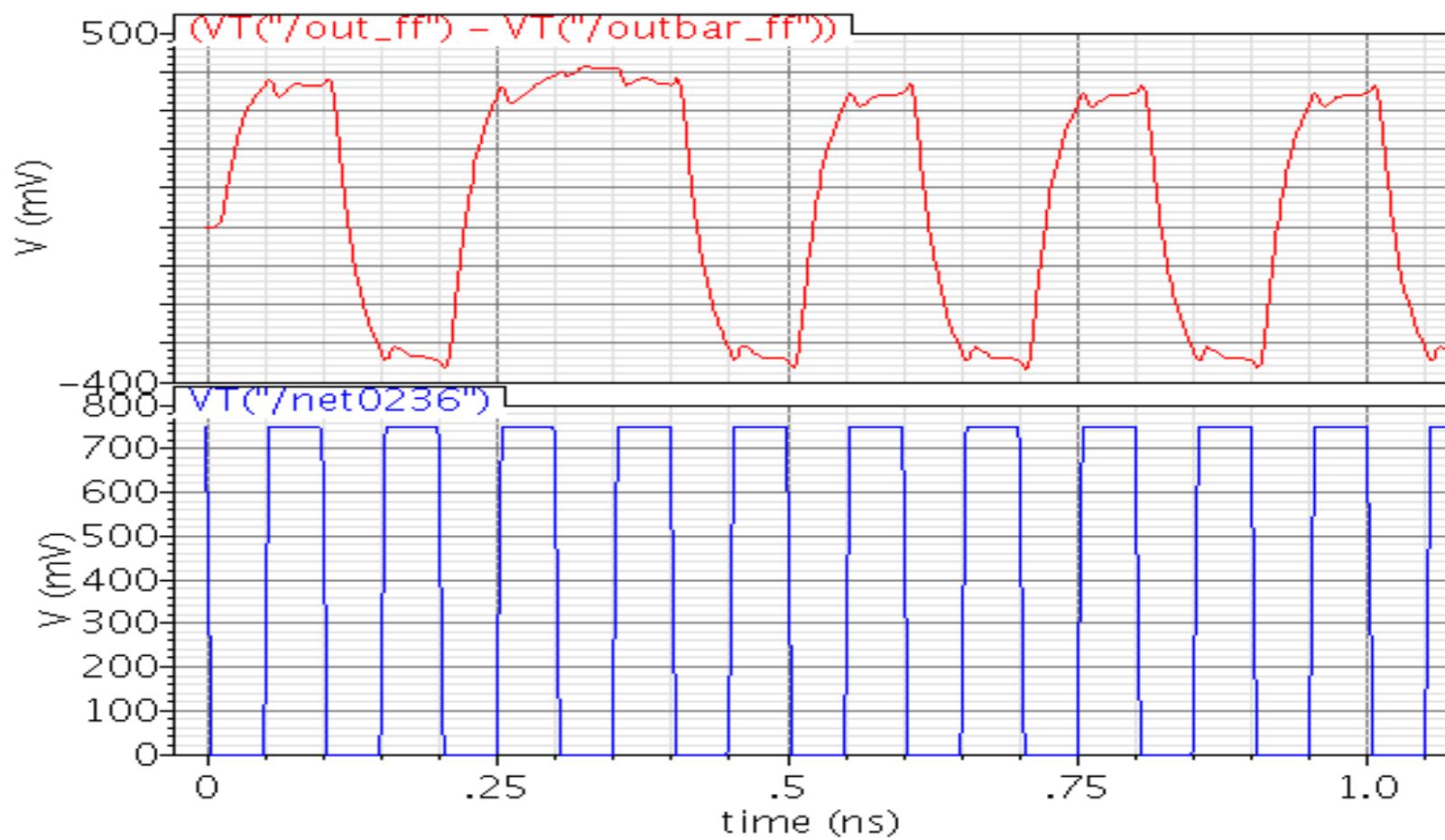
$$Gm3 V_{out} = \frac{V_{out}}{RD} + \frac{dv_{out}}{dt}$$

$$GM3 = Gm1 RD Vin \exp \frac{Gm3 t}{CL} \exp \frac{-t}{RD CL}$$

Setting & hold time

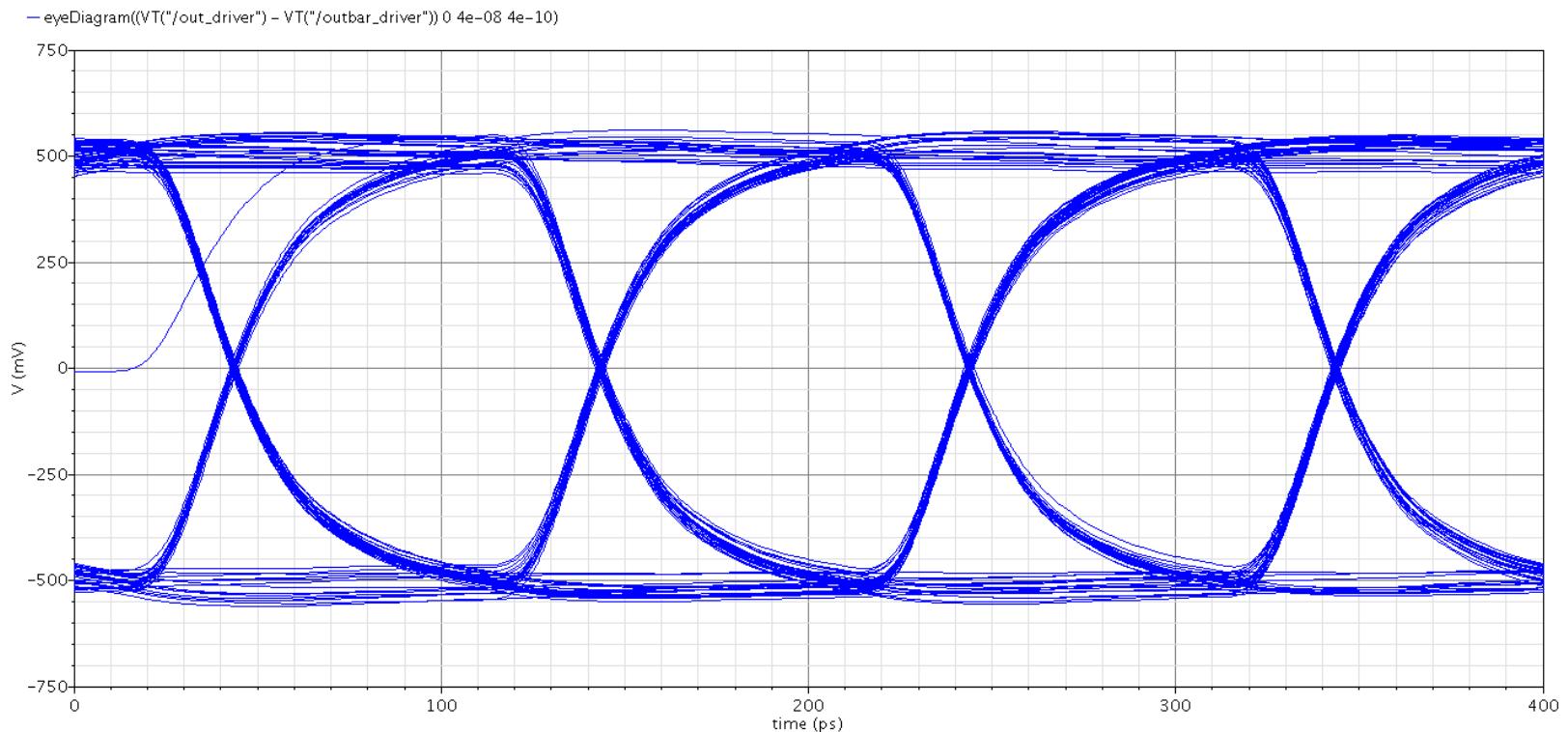


Flip flop output



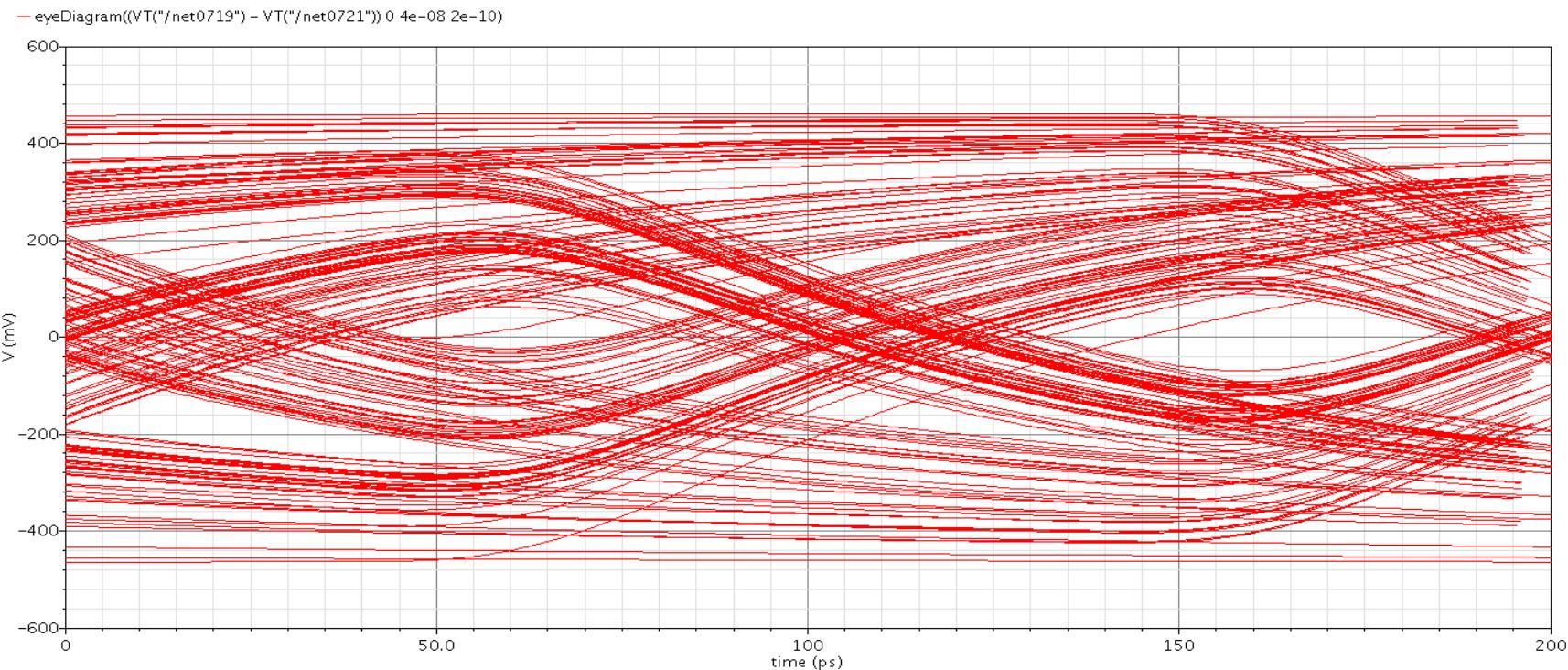
Transmitter output

□ Eye diagram without any Equalization



Transmitter output

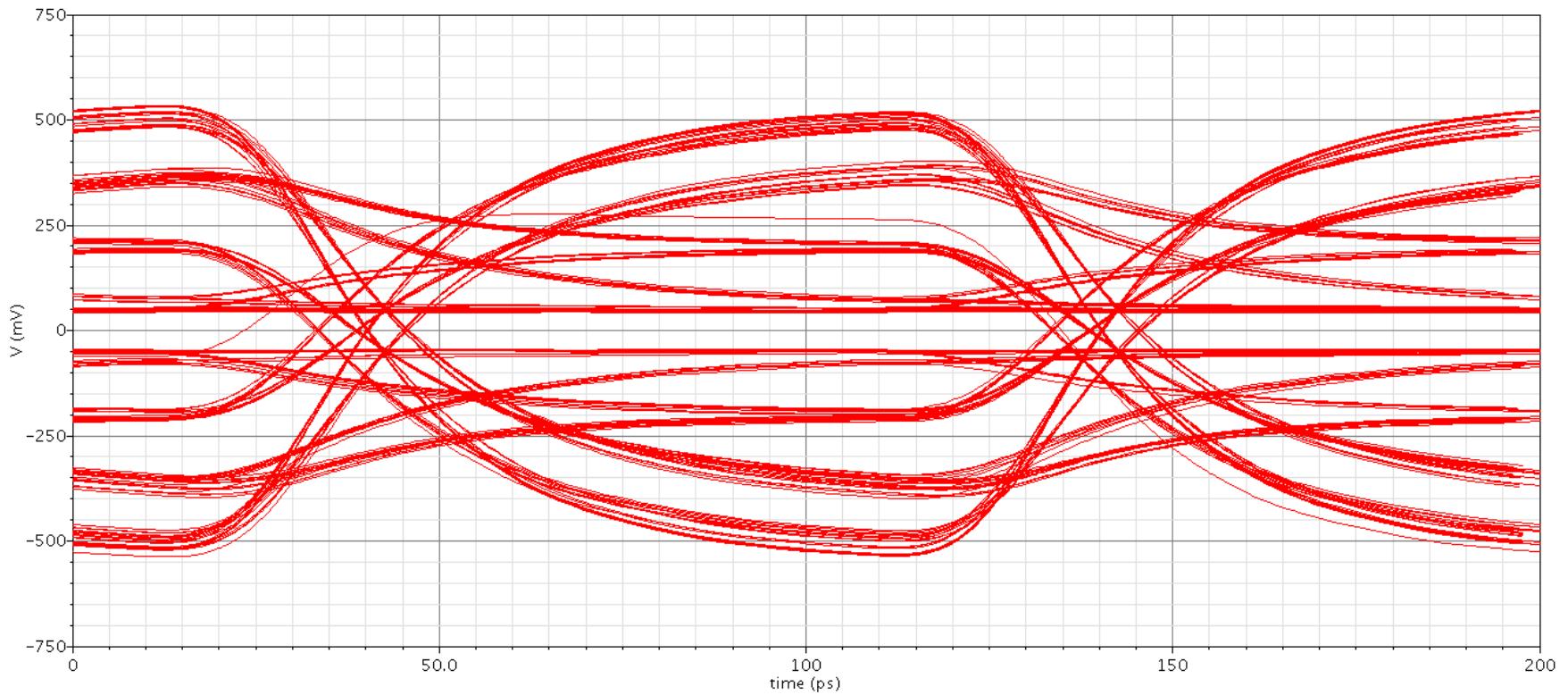
- Eye diagram after passing channel without Equalization



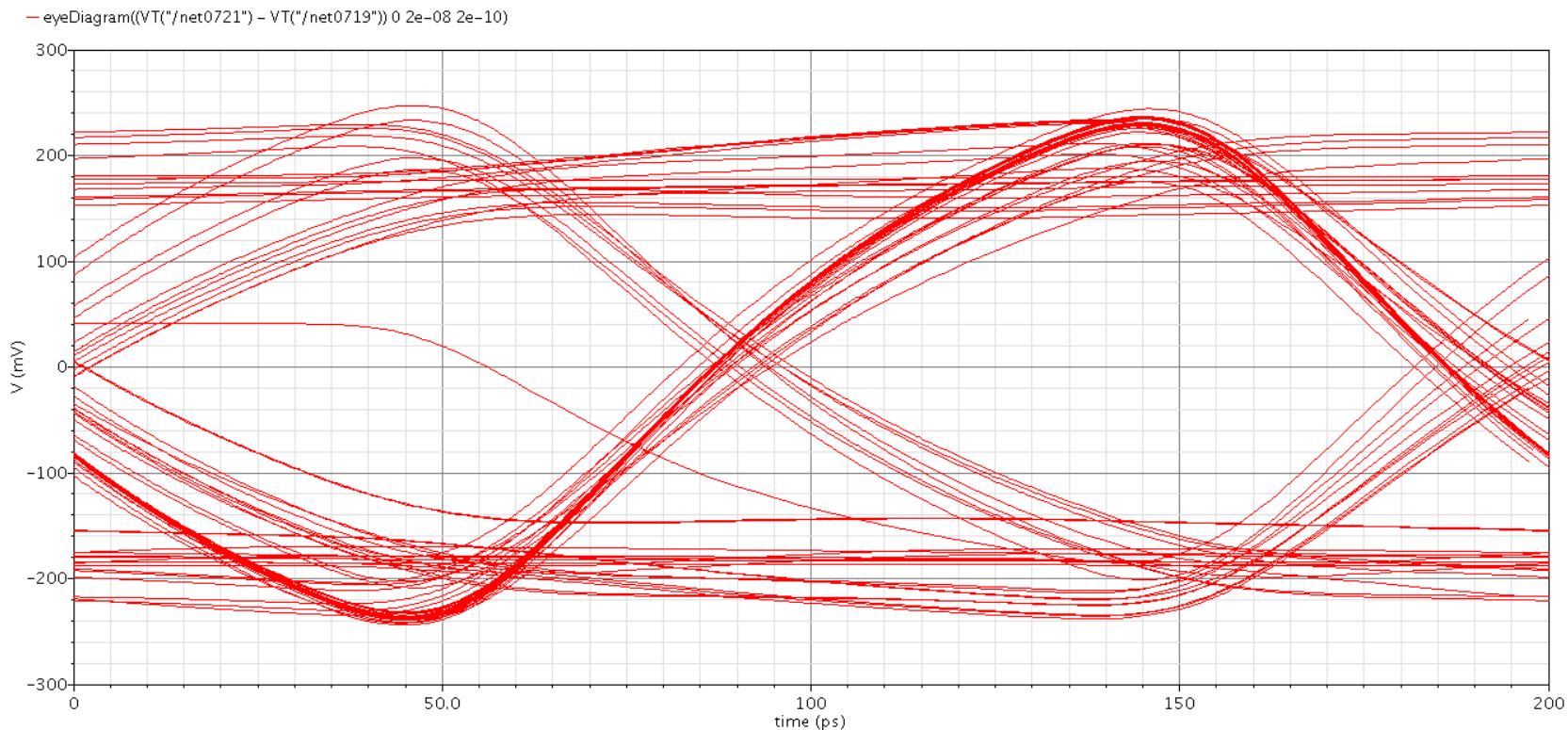
Transmitter output

□ Eye diagram at Tx with Equalization

— eyeDiagram((VT("/out_driver") - VT("/outbar_driver")) 0 4e-08 2e-10)



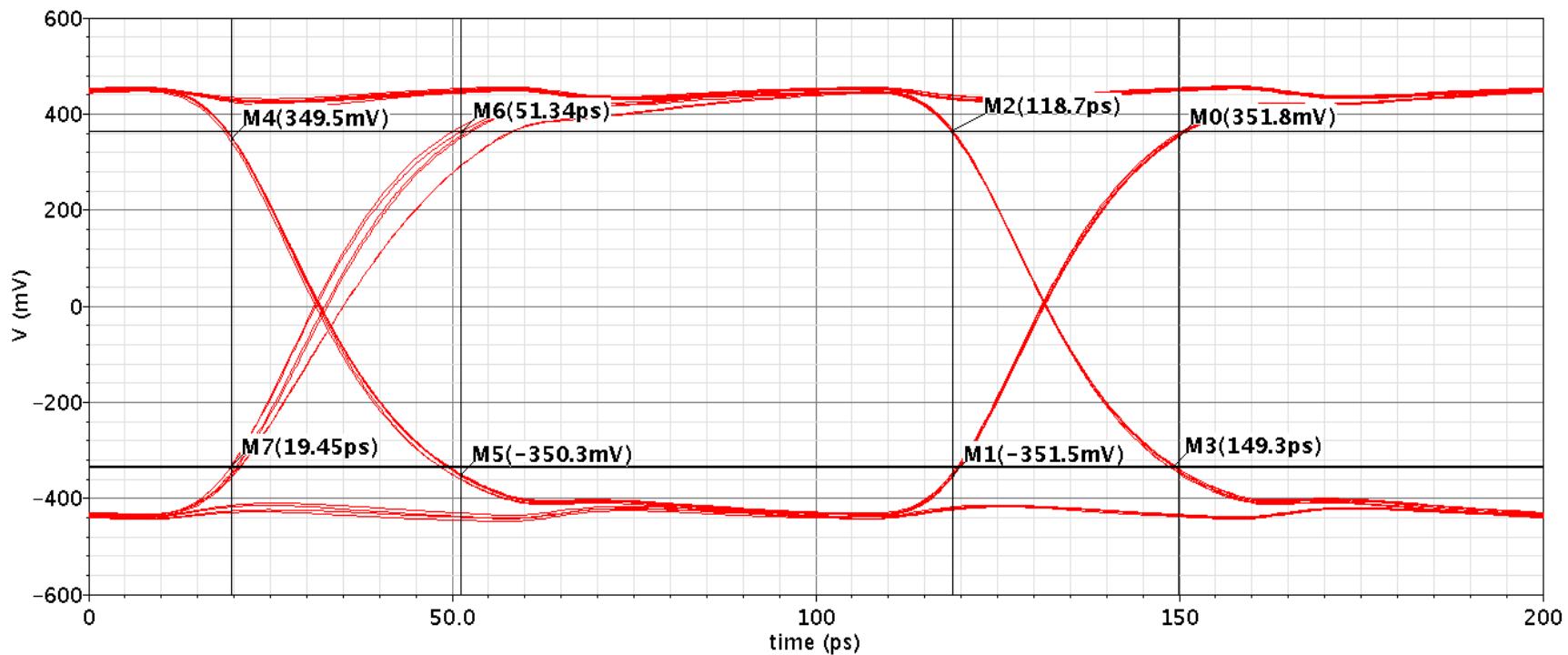
Transmitter output



Rise & Fall time

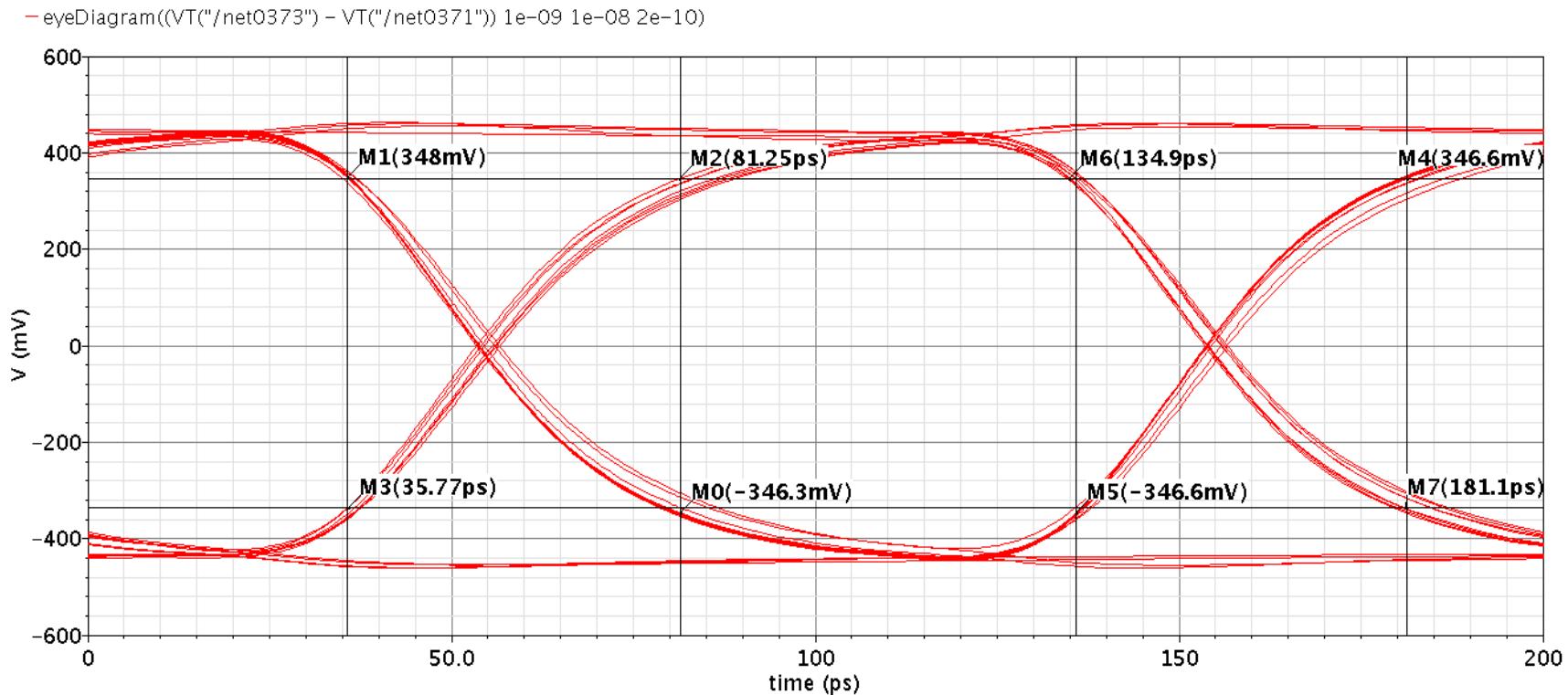
- Rise time is equal 30.7 ps.
- Fall time is equal 31.89 ps.
- at SS corner for transistor ff for resistor at temperature 80°C

- eyeDiagram((VT("/net0373") - VT("/net0371")) 1e-09 1e-08 2e-10)



Rise & Fall time 2

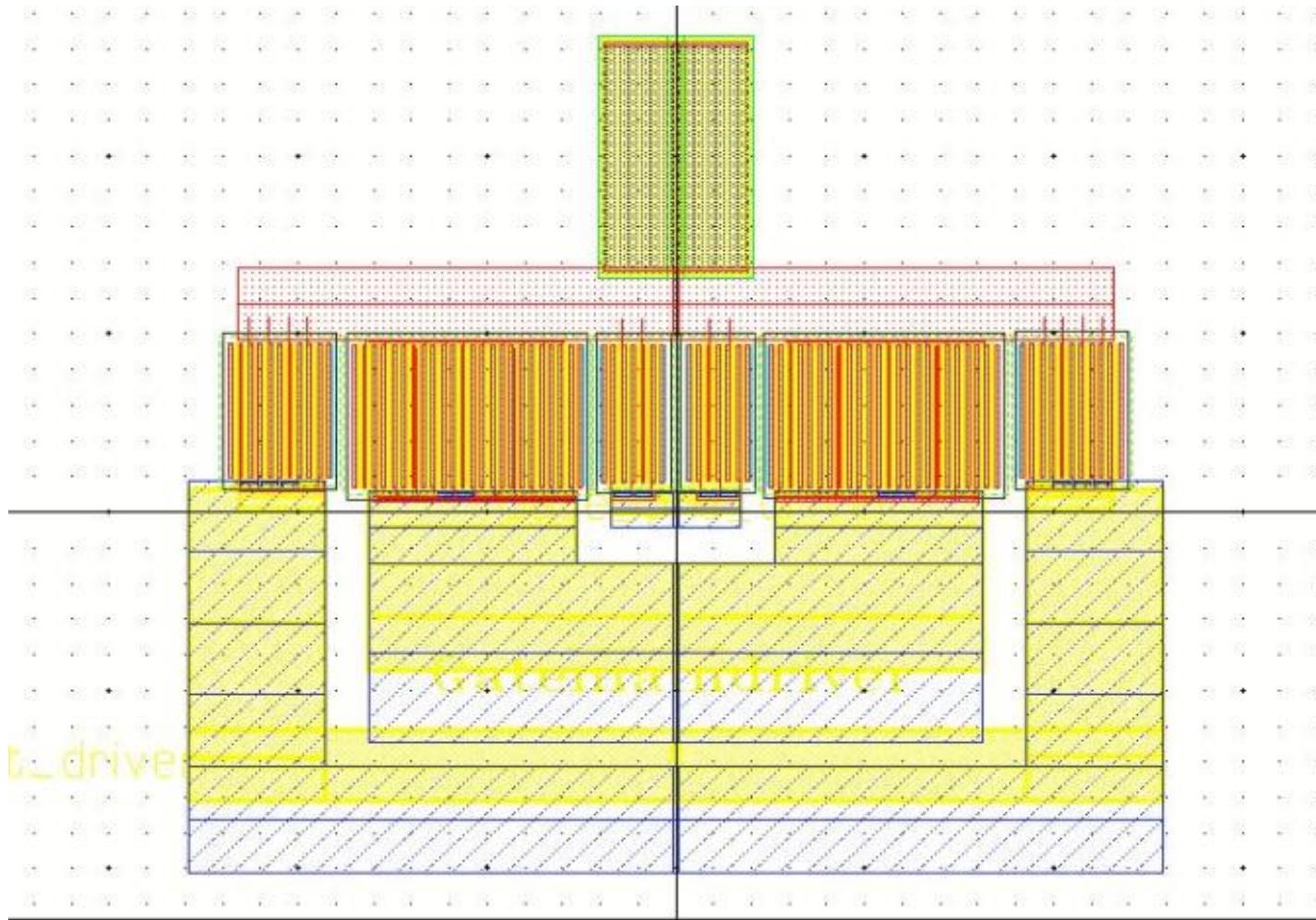
- Rise time is equal 46.2 ps.
- Fall time is equal 45.48 ps.
- at ff corner for transistor ss for resistor at temperature 0°C



Power budget

Type	Power consumption
1- MUX	1.5mW
2- Pre-driver	4.5mW
3-Flip-flop	2mW
3- Driver	20mW
4- Total power	28mW

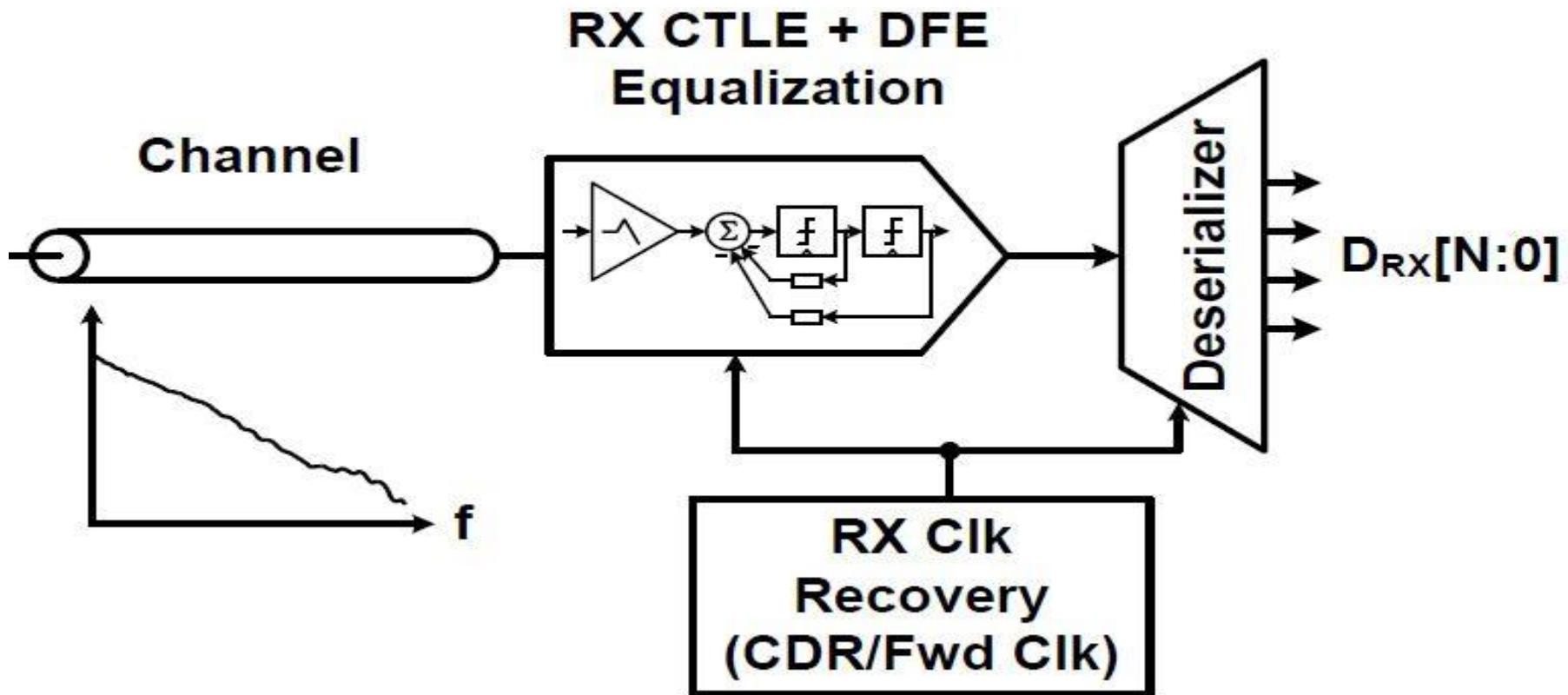
Drivers layout



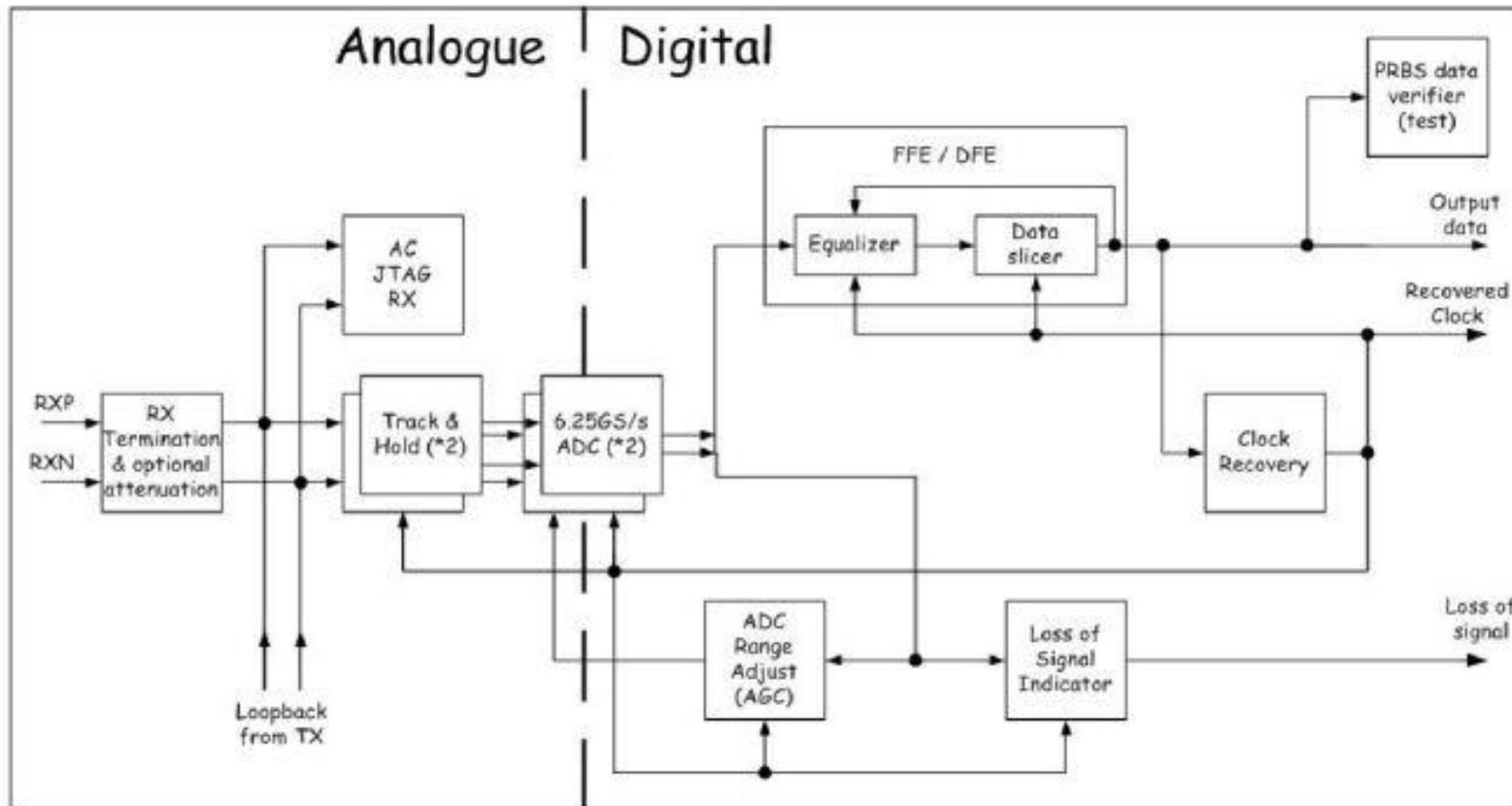
RECEIVER SYSTEM LEVEL OVERVIEW



RX system level conventional Architecture



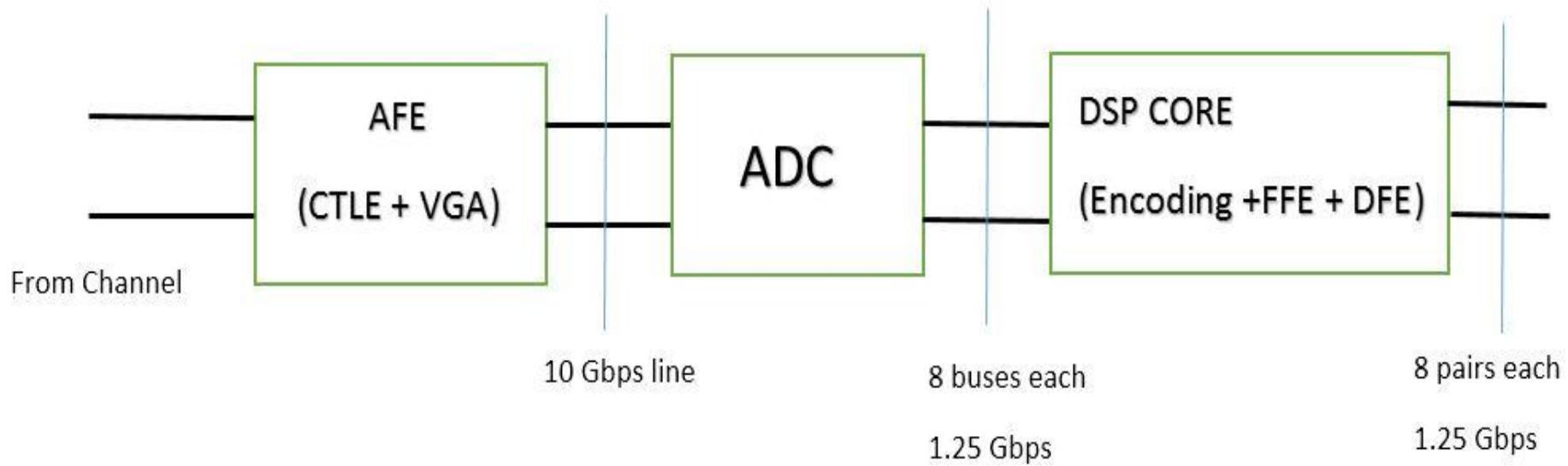
RX system level latest years & future trend



- 12.5GS/s 4.5-bit Flash ADC in 65nm CMOS
- 2-tap FFE & 5-tap DFE

[Harwood ISSCC 2007]

Our Rx System level



ANALOG FRONT END (AFE)

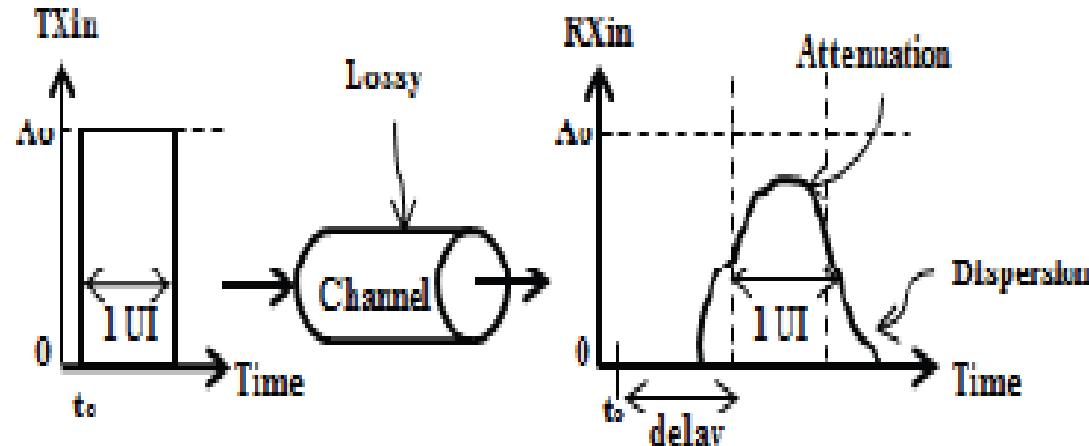


Contents

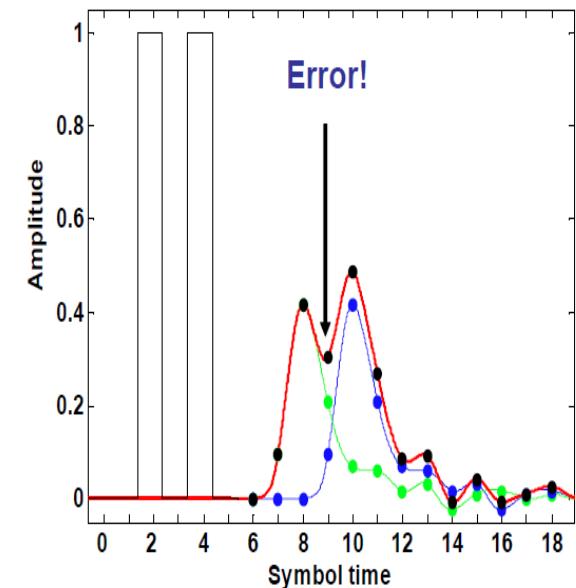
- Introduction
- Continuous Time Linear Equalizer (CTLE)
 - Design
 - Simulation Results
- Variable Gain Amplifier (VGA)
 - Design
 - Simulation Results

Introduction

- Received signals suffers from frequency dependent attenuation and dispersion caused by inter symbol interference (ISI)
- Dispersion due to skin effect and dielectric losses



. ISI effect in single pulse response.

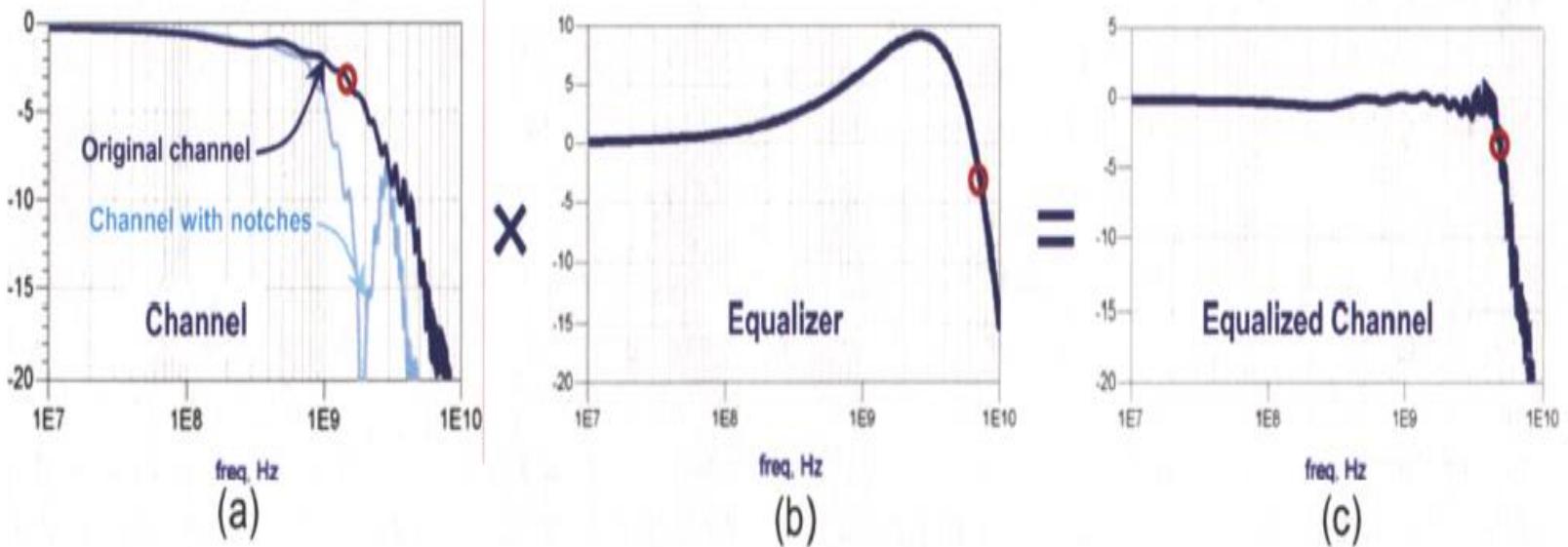


The effect of intersymbol interference

Continuous Time Linear Equalizer (CTLE)

- Equalizer acts as a high-pass filter to compensate for channel high frequency losses
- Passive linear Vs. Active linear equalizer
- First order Vs. Second order CTLE

CTLE



Frequency responses of (a) the channel, (b) the CTLE, and (c) the equalized channel. (● : -3 dB point.)

$$H_{ch}(s) = \frac{k_{ch}}{s + p_{ch}},$$

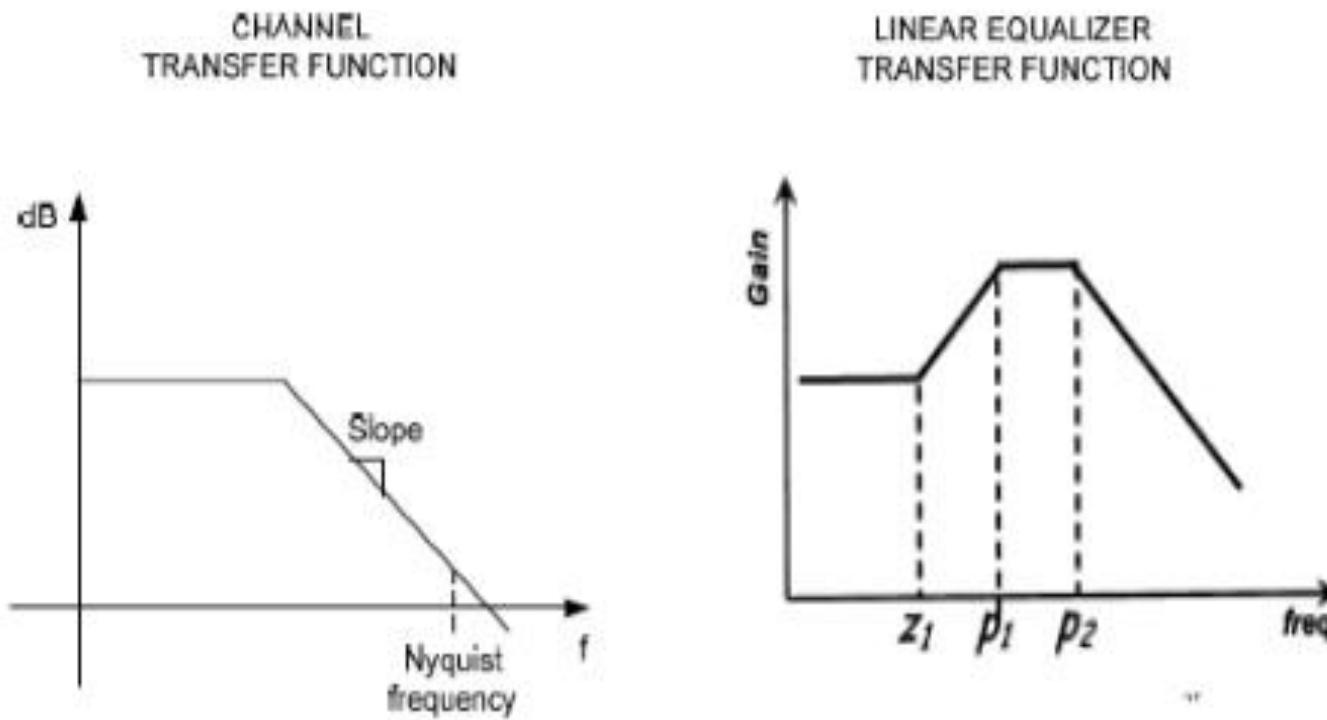
$$H_{CTLE}(s) = \frac{\tilde{k}_1(s + z_1)}{(s + p_1)(s + p_2)},$$

$$H_{EQ}(s) = \frac{k_1}{(s + p_1)(s + p_2)},$$

Channel
Equalized channel

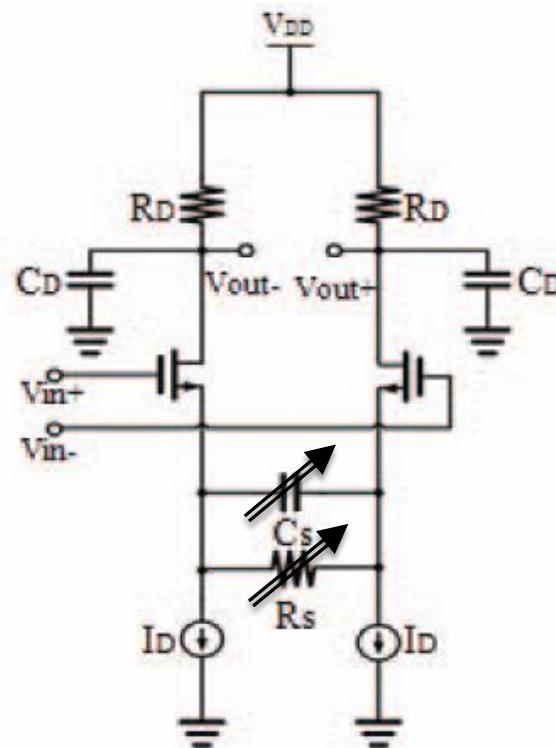
Equalizer

Concept of operation



Channel and linear equalizer transfer function.

Design

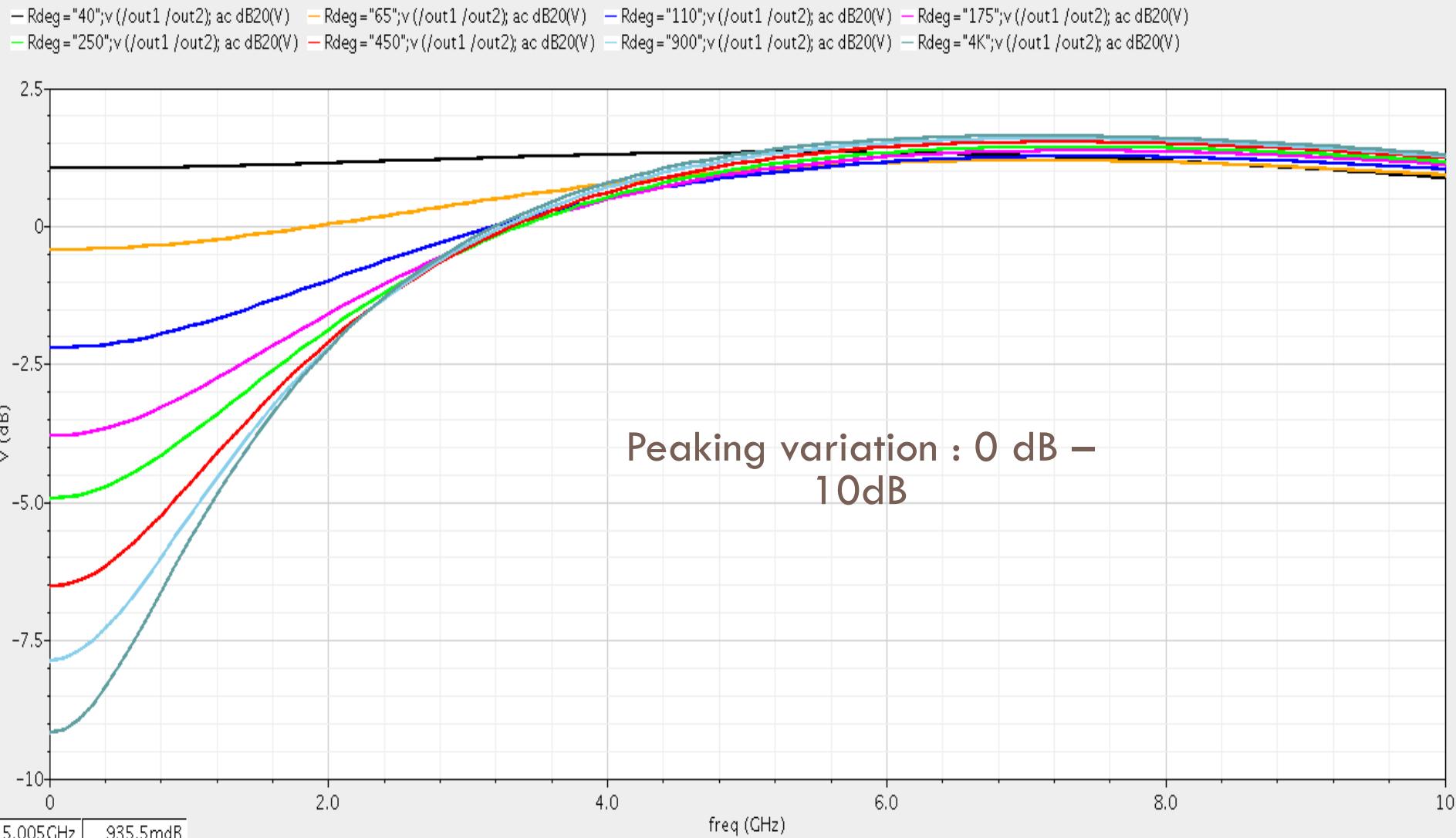


$$\omega_z = \frac{1}{R_s C_s}, \quad \omega_{R_i} = \frac{1}{R_i C_i}, \quad \text{and} \quad \omega_{R_f} = \frac{1 + g_m R_s / 2}{R_s C_s}.$$

Pros & Cons

- Pros
 - Low power and area
 - Cancel both precursor and long tail ISI
- Cons
 - Noise and cross talk are amplified
 - Very sensitive to PVT

Simulation results – AC-Response

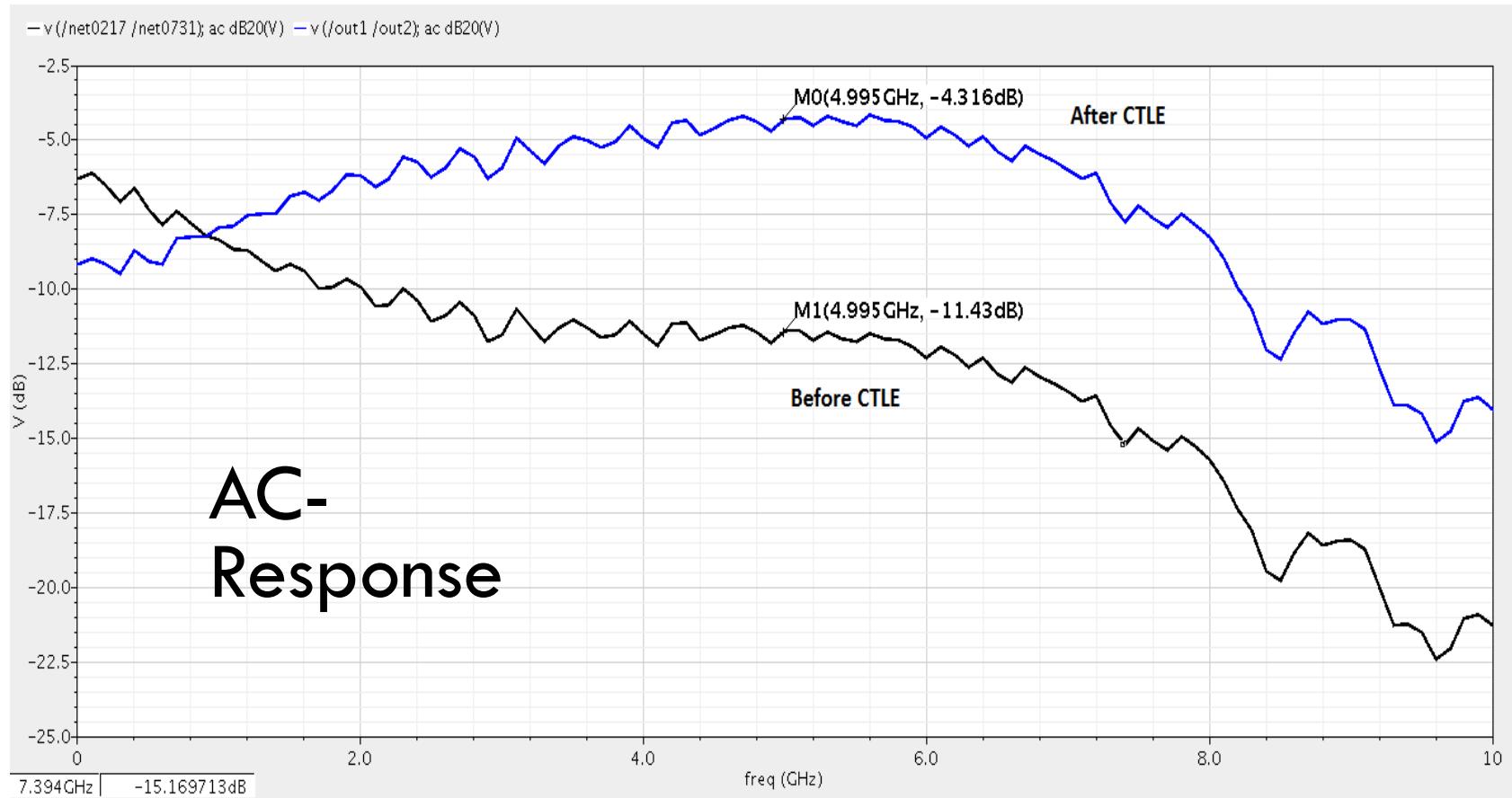


Peaking adaptation values

Rdeg (Ω)	Boosting (dB)
40	0
65	1.5
110	3
175	4.5
250	6
450	7.5
900	9
1.5K	10.5

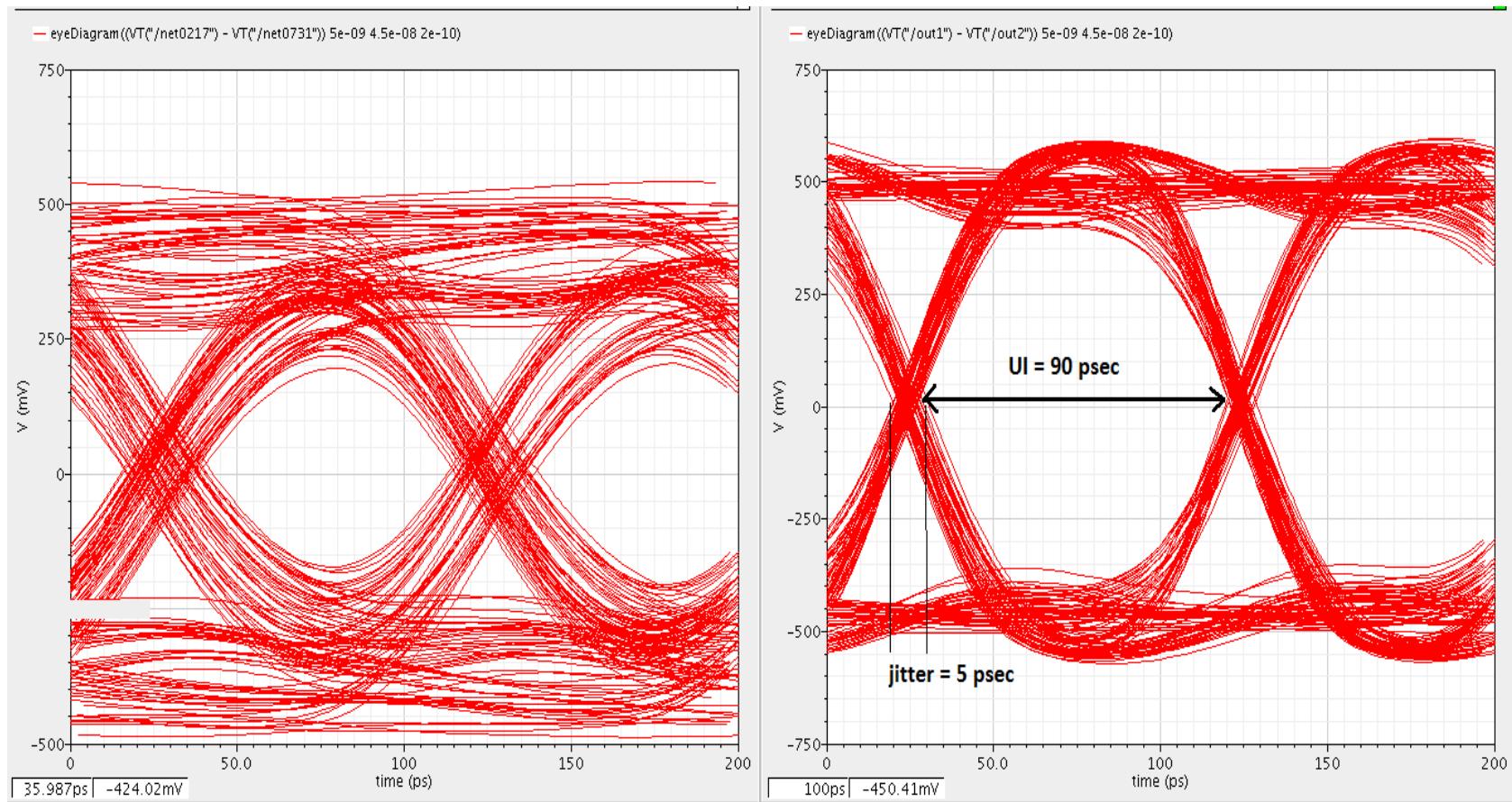
Simulation results – AC-Response (1)

- Typical back plane channel with $S_{21} = -5.3$ dB



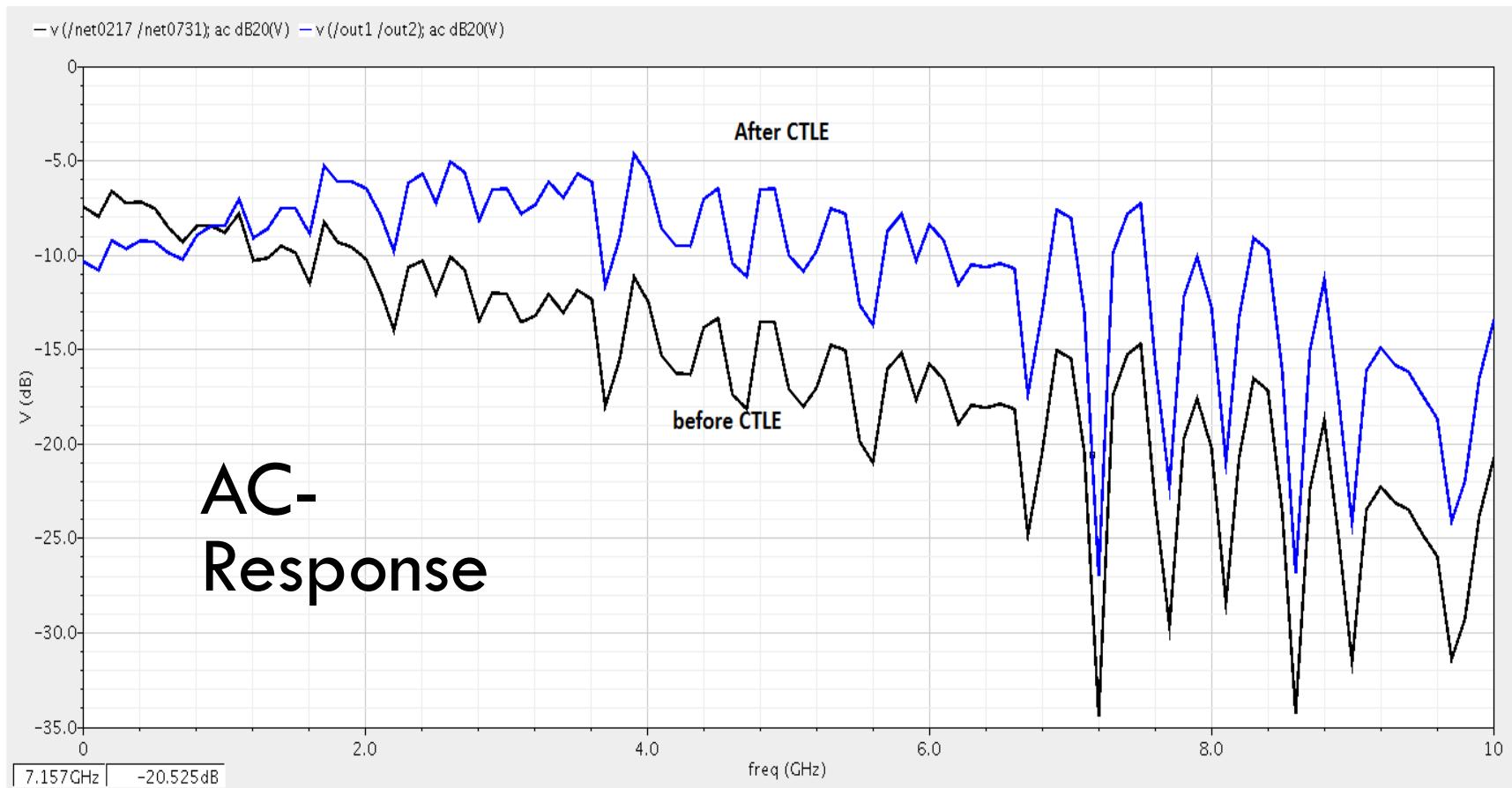
Simulation results – Eye diagram (1)

- Typical back plane channel with $S_{21} = -5.3$ dB



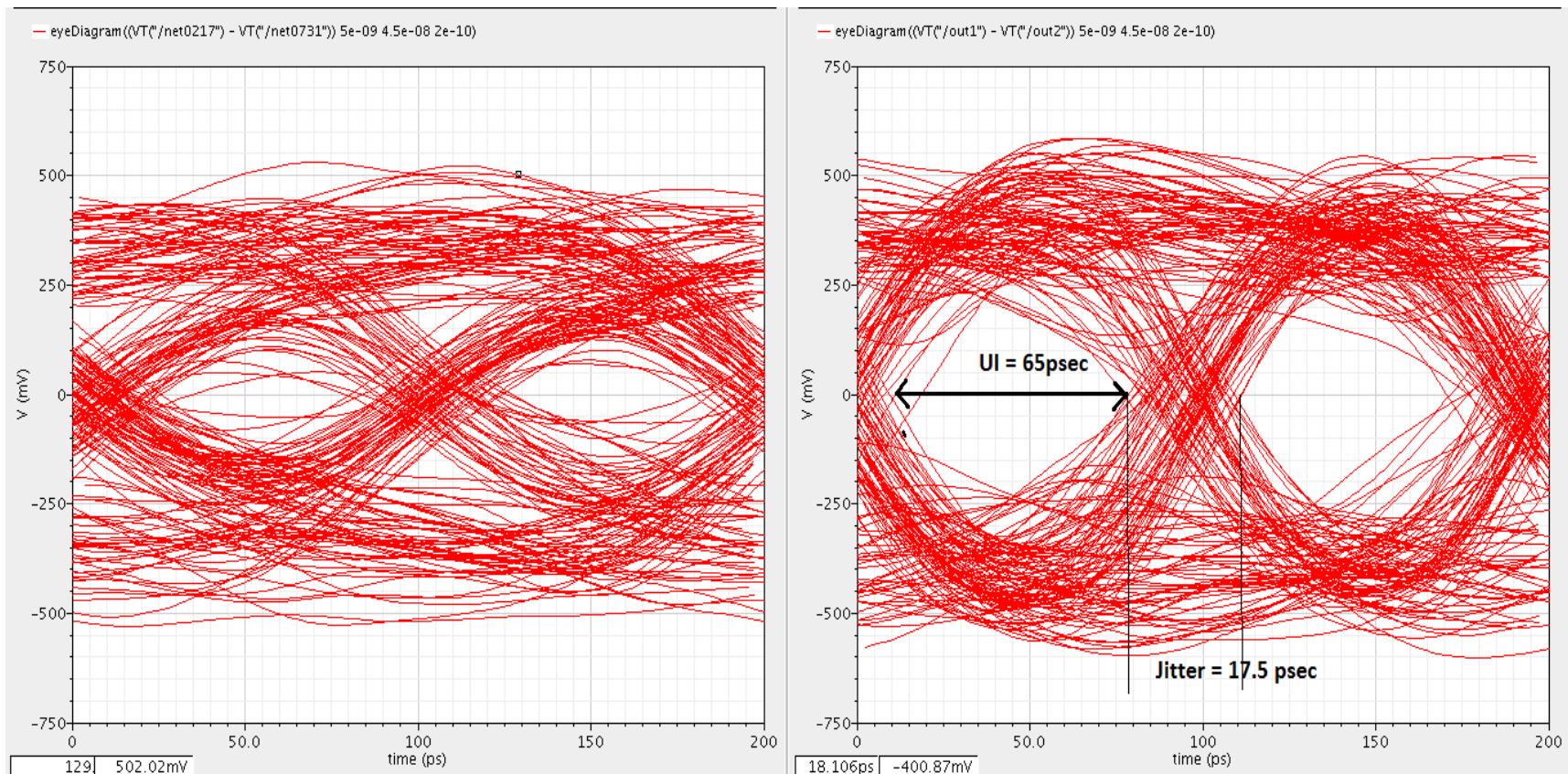
Simulation results – AC-Response (2)

- Typical back plane channel with $S_{21} = -9.5$ dB



Simulation results – Eye diagram (2)

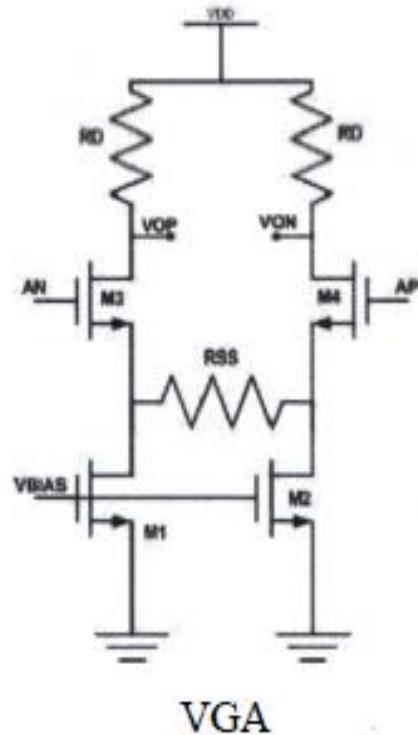
- Typical back plane channel with $S_{21} = -9.5$ dB



Variable Gain Amplifier (VGA)

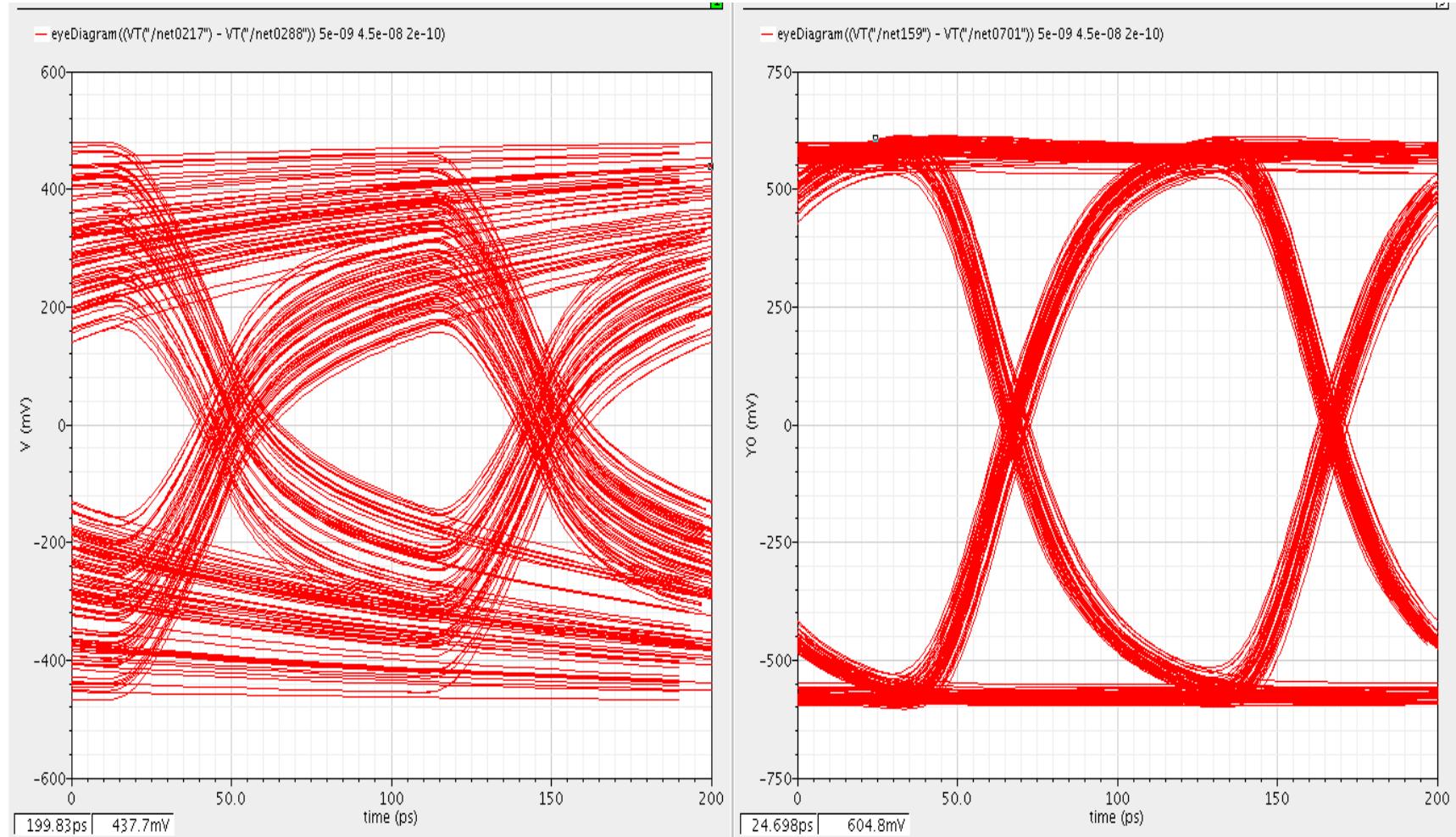
- Channel attenuates data
 - ∴ Received data must be amplified for operating the ADC
- Varying gain by varying the degeneration resistance to adjust the output swing at constant value = $1.2V_{p-p}$

Design



$$A = \frac{gm \cdot Rd}{1 + gm \left(\frac{Rs}{2} \right)}$$

Simulation results



Different gain adaptations

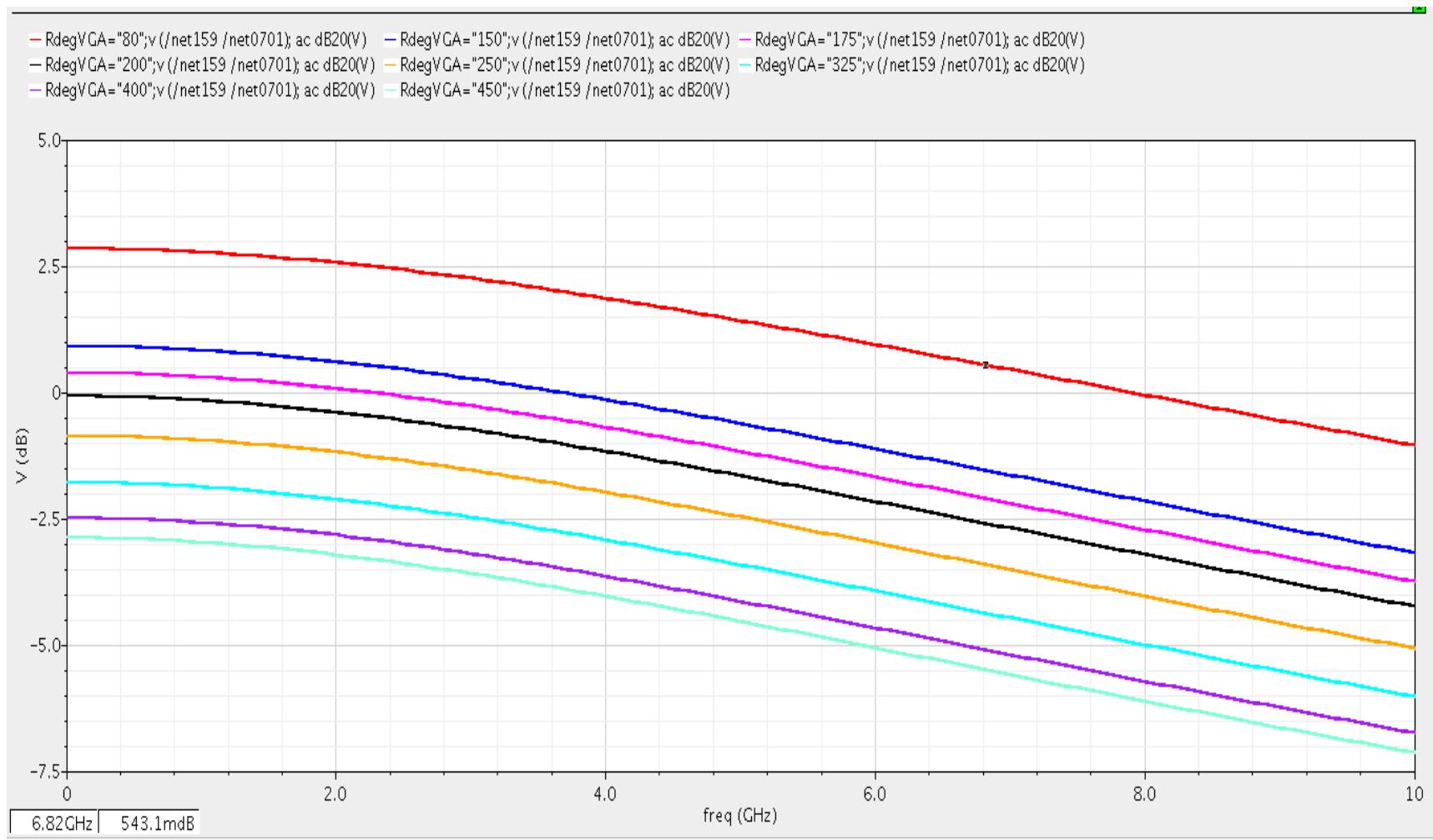


Table of specs

	Power Consumption	Range	Data Rate	Supply Voltage	Technology
CTLE	7.84 mW	0-10 dB	10 Gbps	1V	65nm
VGA	3.2 mW	0 – 5.5 dB			

Conclusion & Further work

- Conclusion
 - AFE of the Rx flatten the frequency response of the signal after being the channel effect, and amplifies the signal going to the ADC
- Further Work
 - Passing corners
 - Layout



Questions ?

LOW POWER , HIGH SPEED FLASH ADC



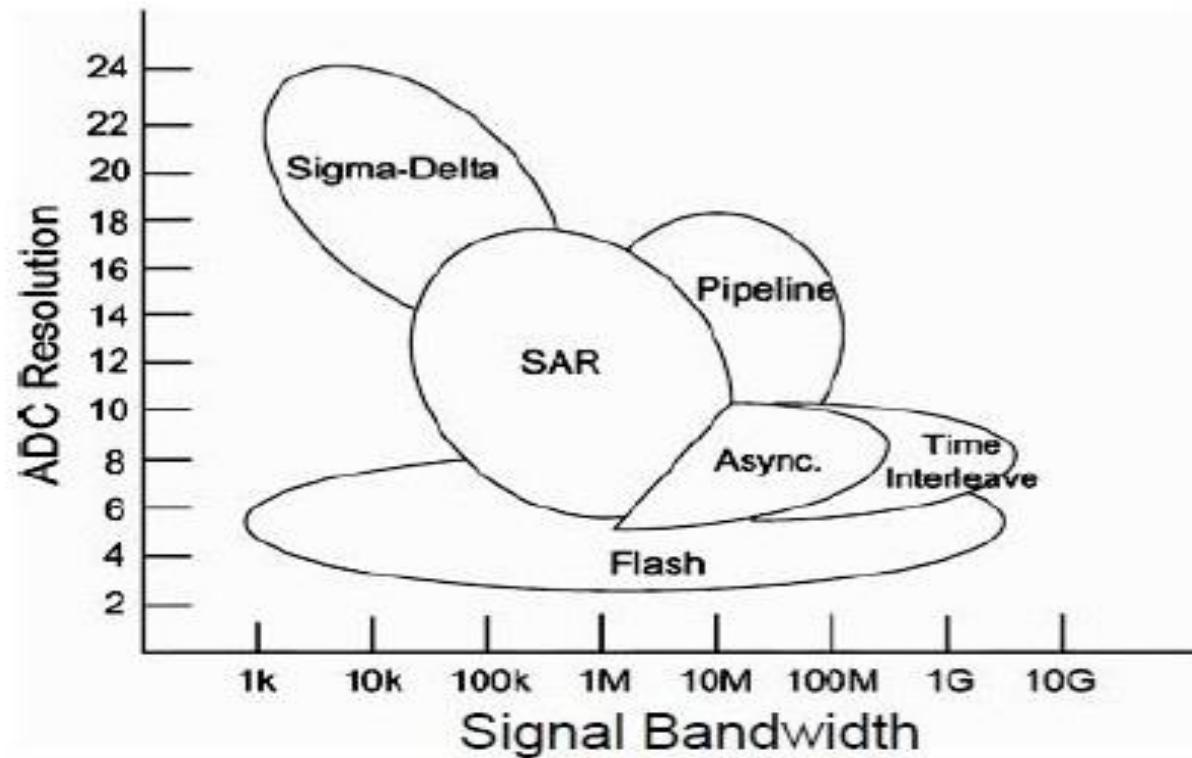
Overview

- ADC in Digital RX
 - Architecture
- System level design
 - Models
 - Expected Specs
- Circuits
 - Schematics
 - Specs
- Simulation Results
 - Waveforms
 - Corners
- Integration with CTLE and VGA
 - Waveforms

ADC Architecture

Most proper candidates:

Type	Resolution	Speed
Pipeline	High	Medium
Flash	Low	High
Folding	Medium	High



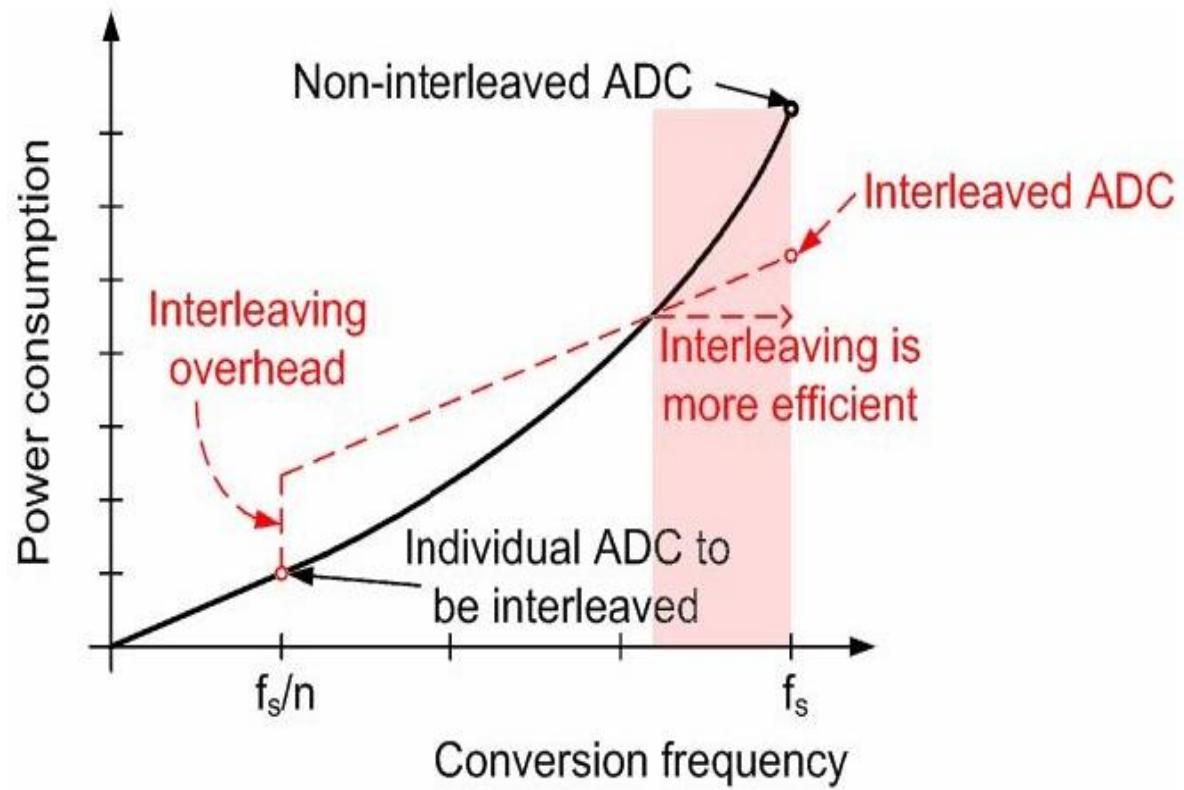
ADC Architecture: Time Interleaving

Pros:

- Lower sampling frequency
- Relax design of ADC components

Cons:

- Gain mismatch
- Offset mismatch
- Timing mismatch



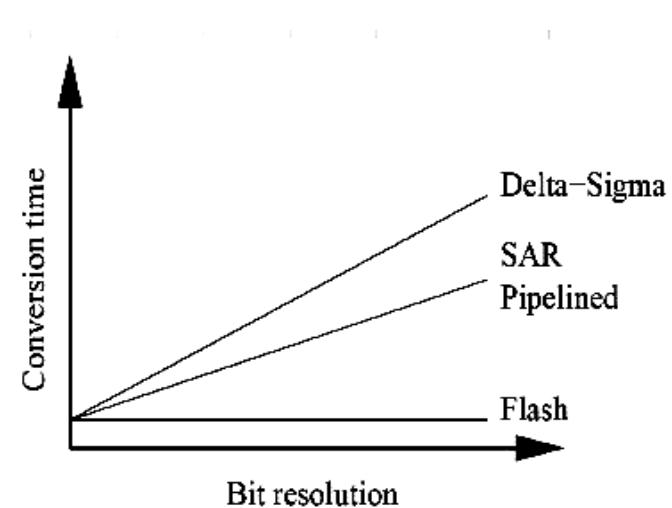
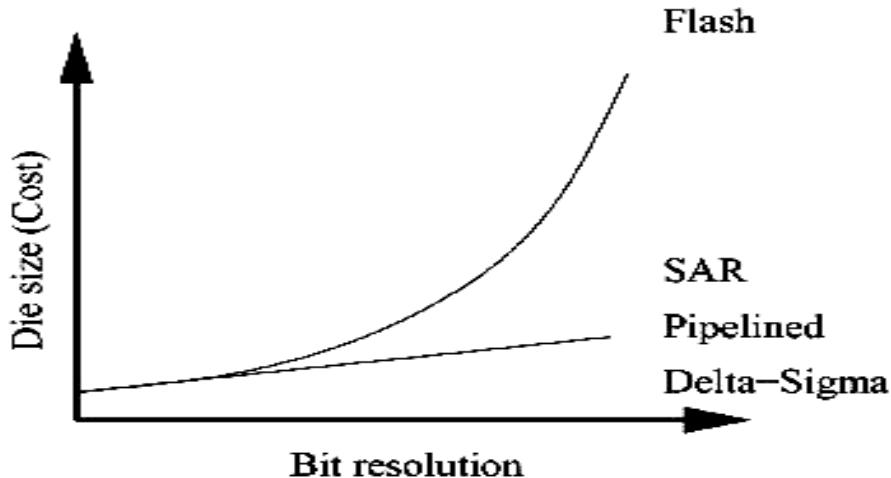
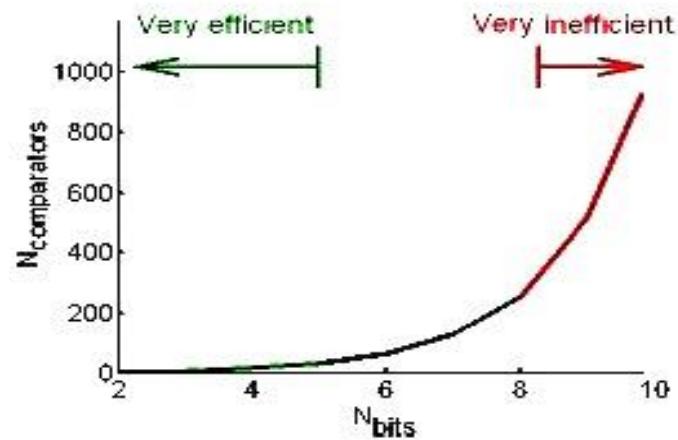
ADC Architecture: Flash ADC

Pros:

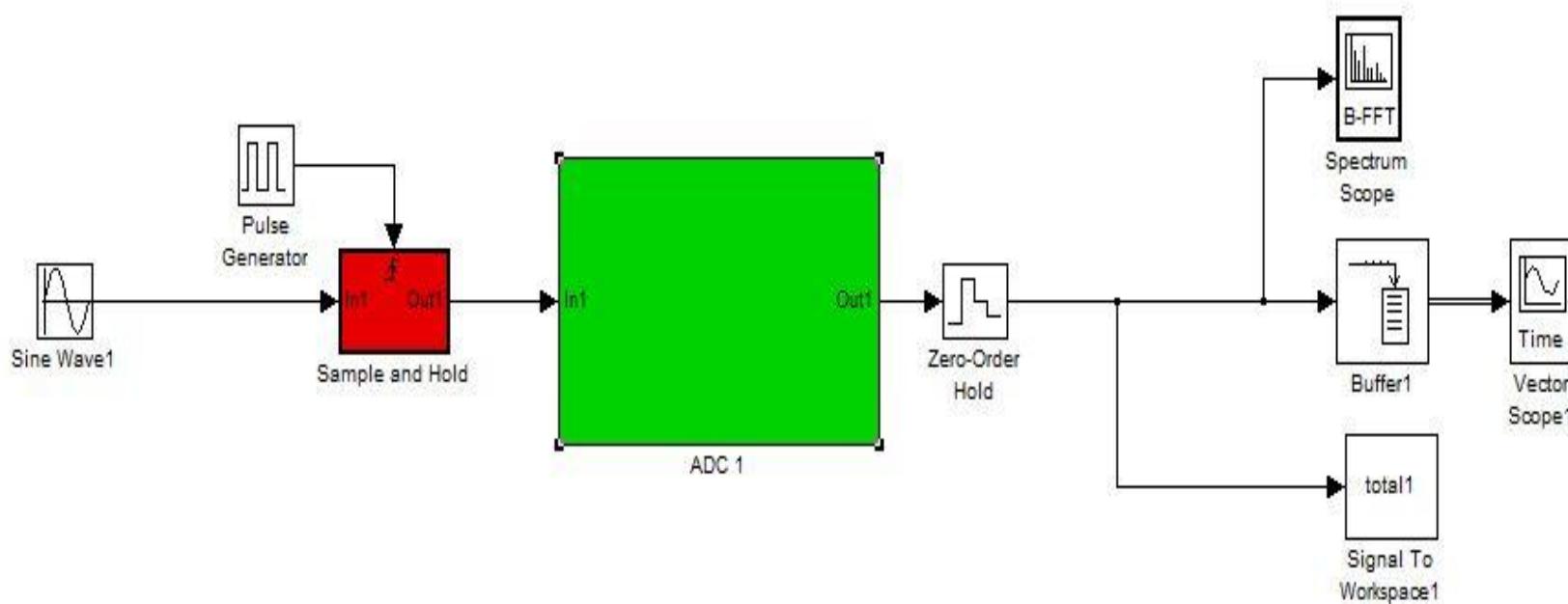
- Highest conversion speed.

Cons:

- Efficient only Up to 6 bits
- Large area
- High power

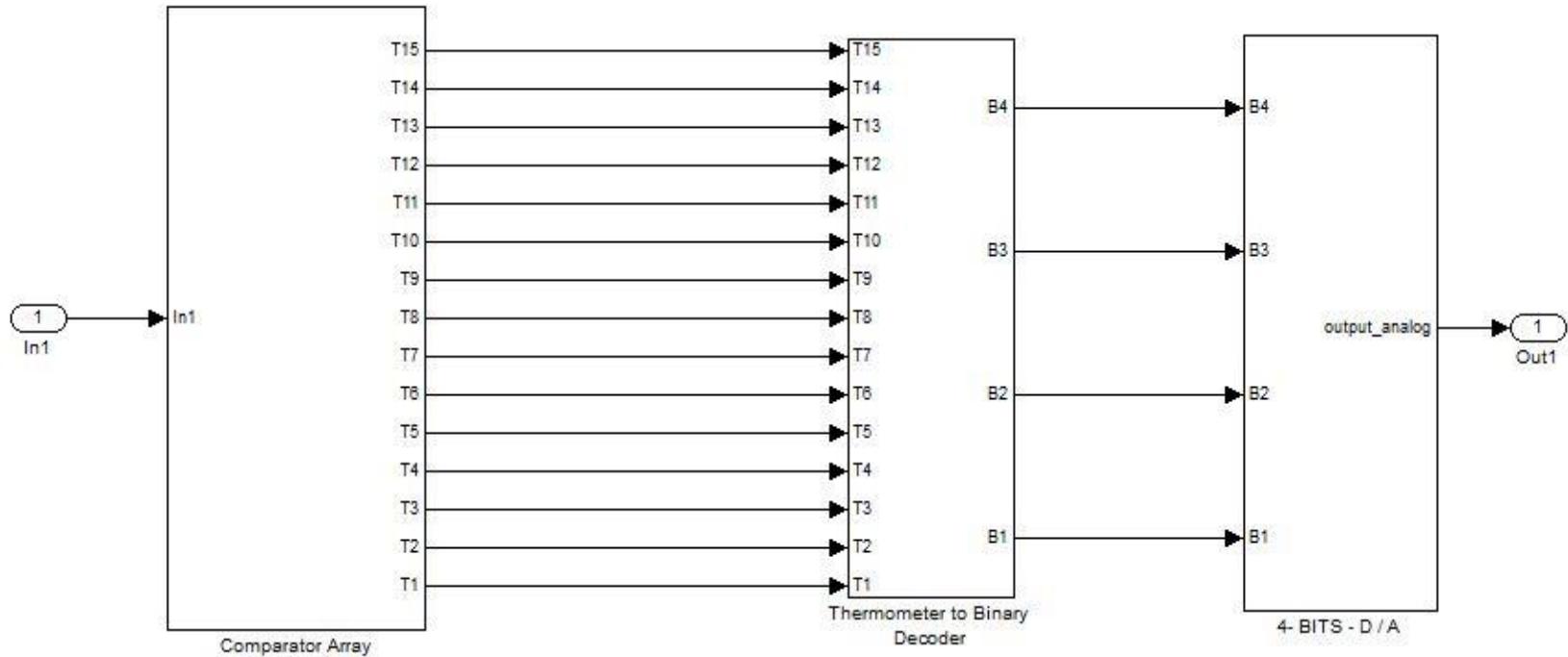


ADC System-Level Design

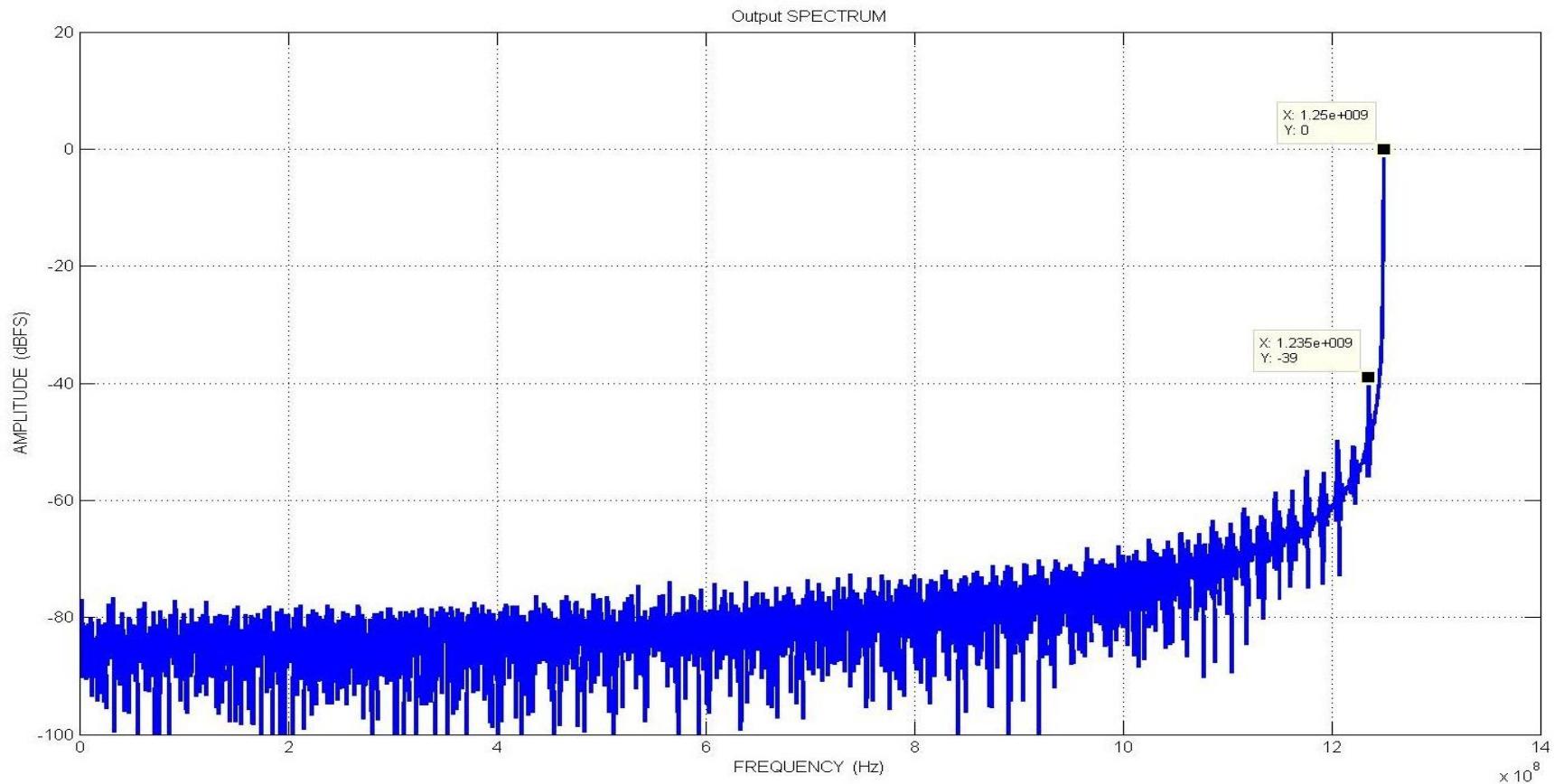


1st model

Sub-ADC model



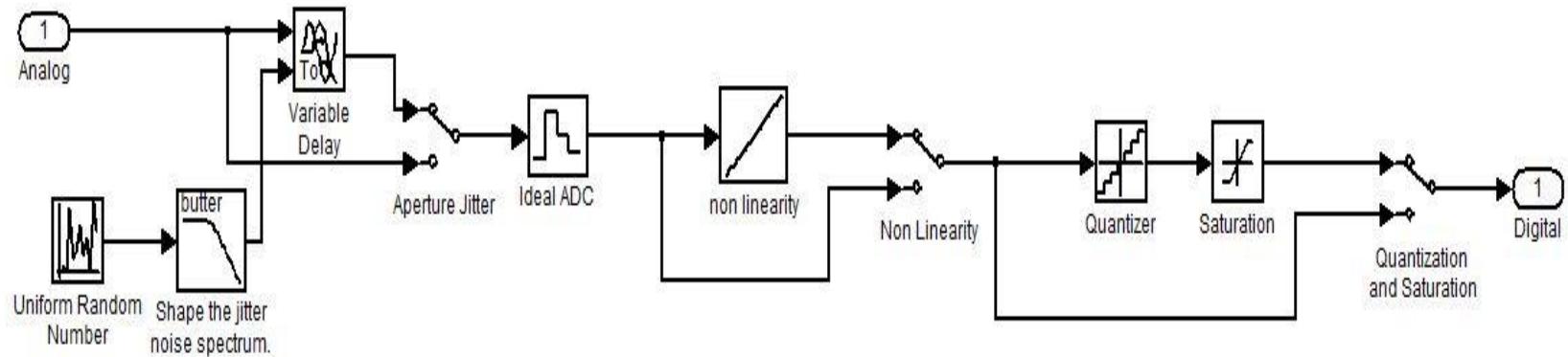
Dynamic performance: Output spectrum



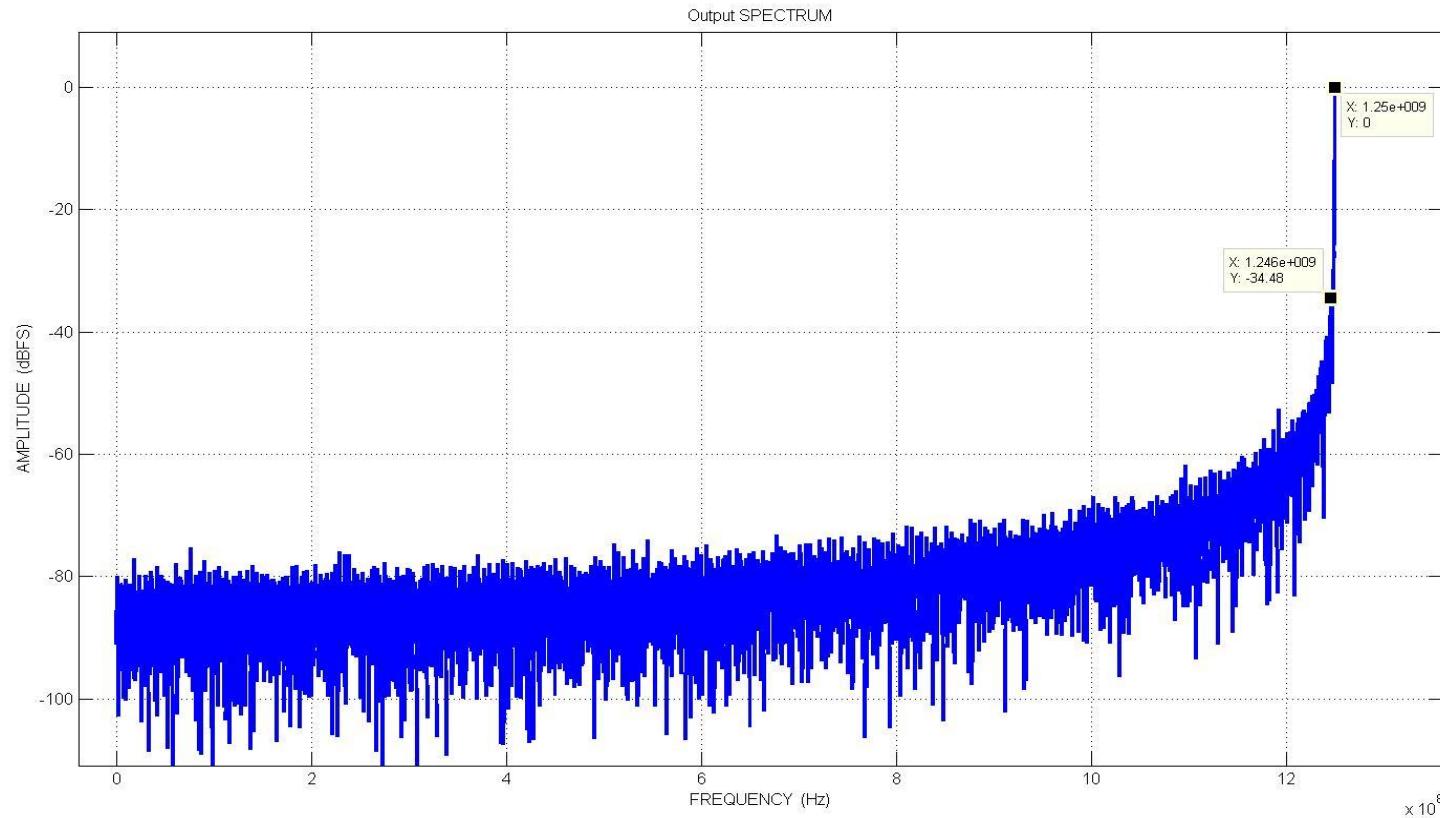
SFDR = 39dB for 1.25GHz input @ 2.5GS/s

2nd model

AMS-Library Modified Model

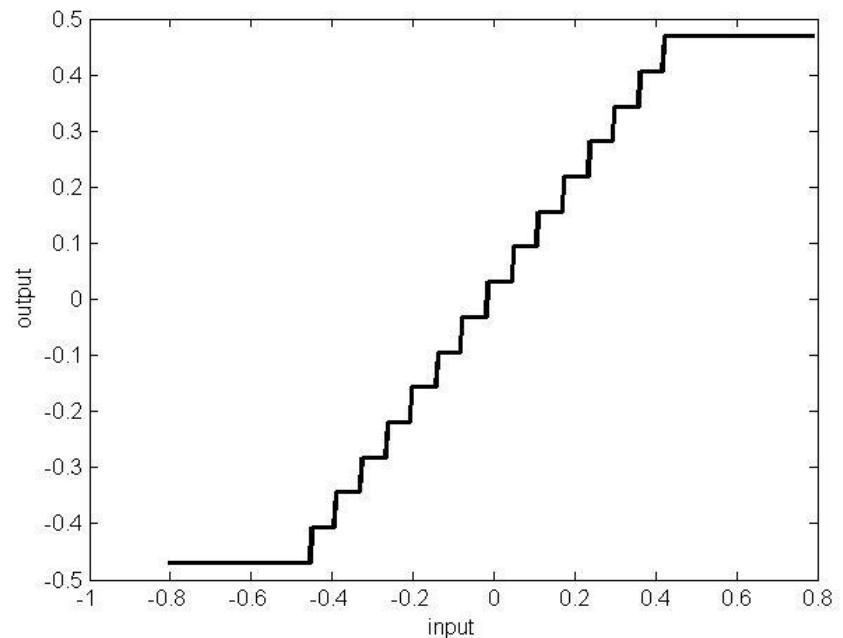
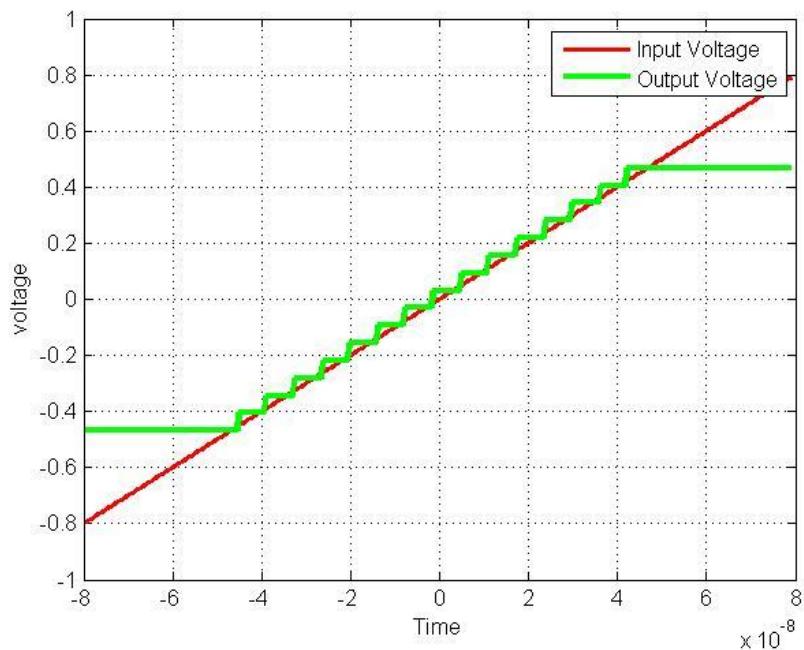


Dynamic performance for sub-ADC: Output spectrum

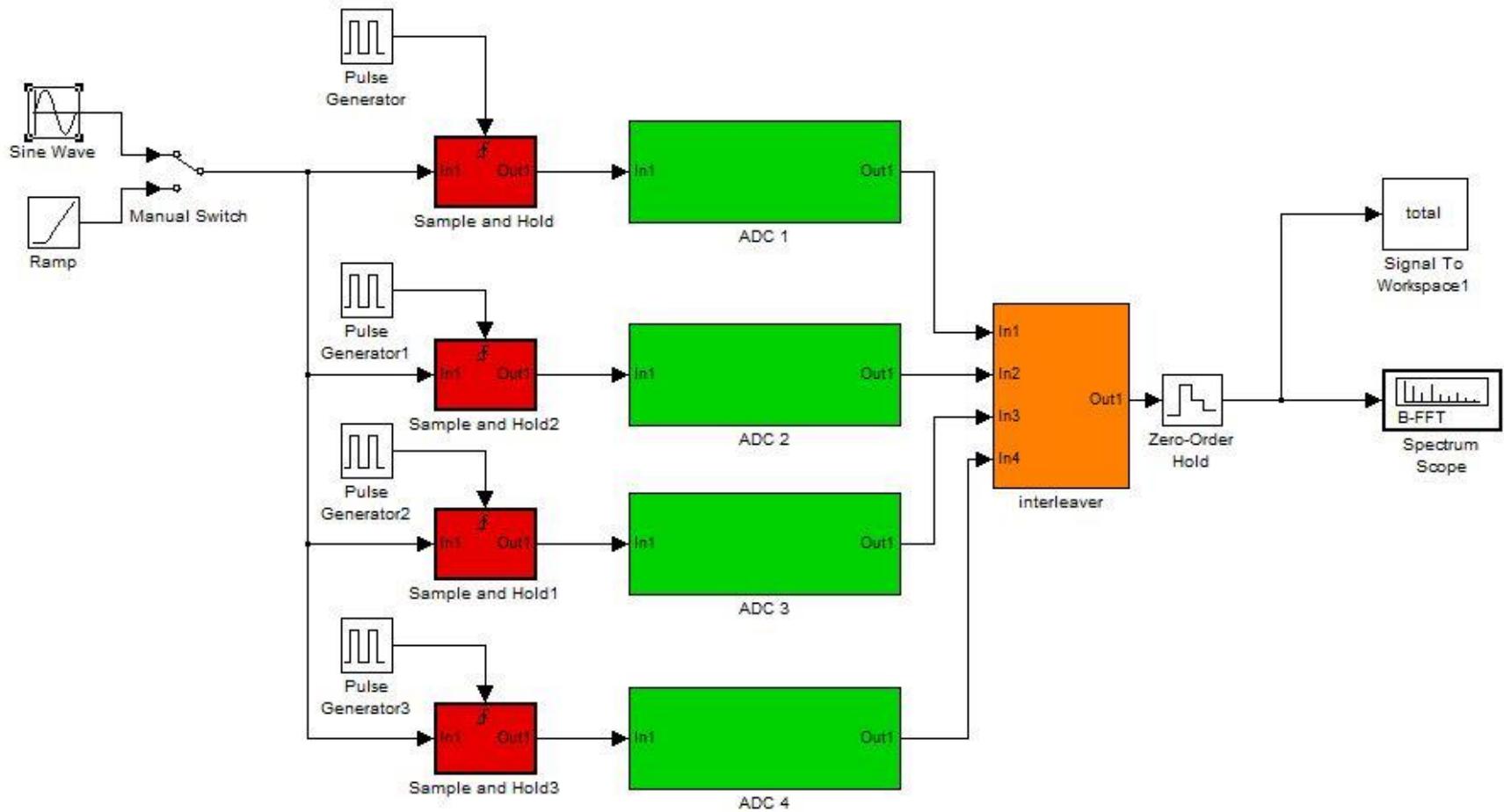


SFDR = 34.5dB for 1.25 GHz input @ 2.5GS/s

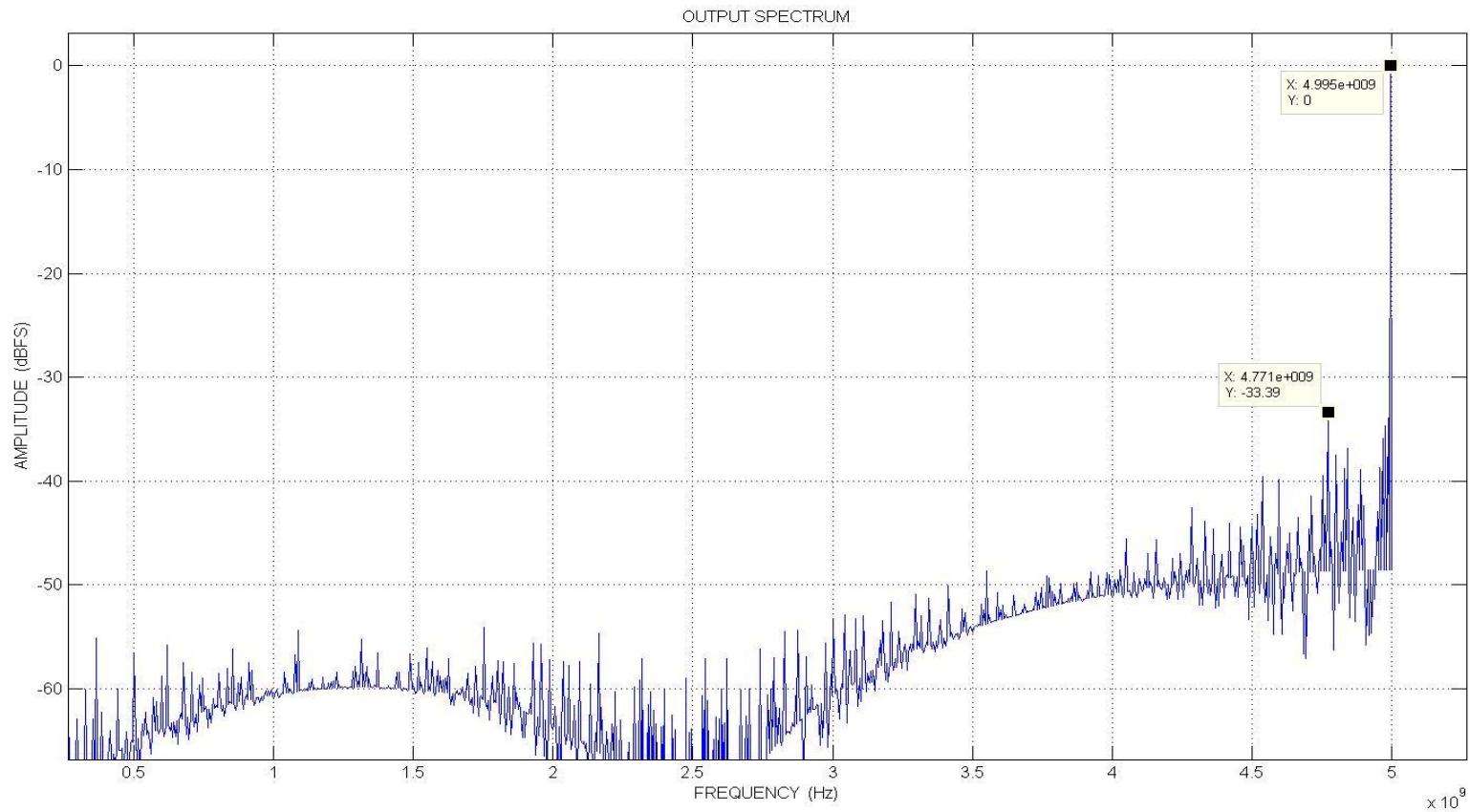
Static performance:



10 GS/s Interleaved ADC Model



Output spectrum for 5GHz input



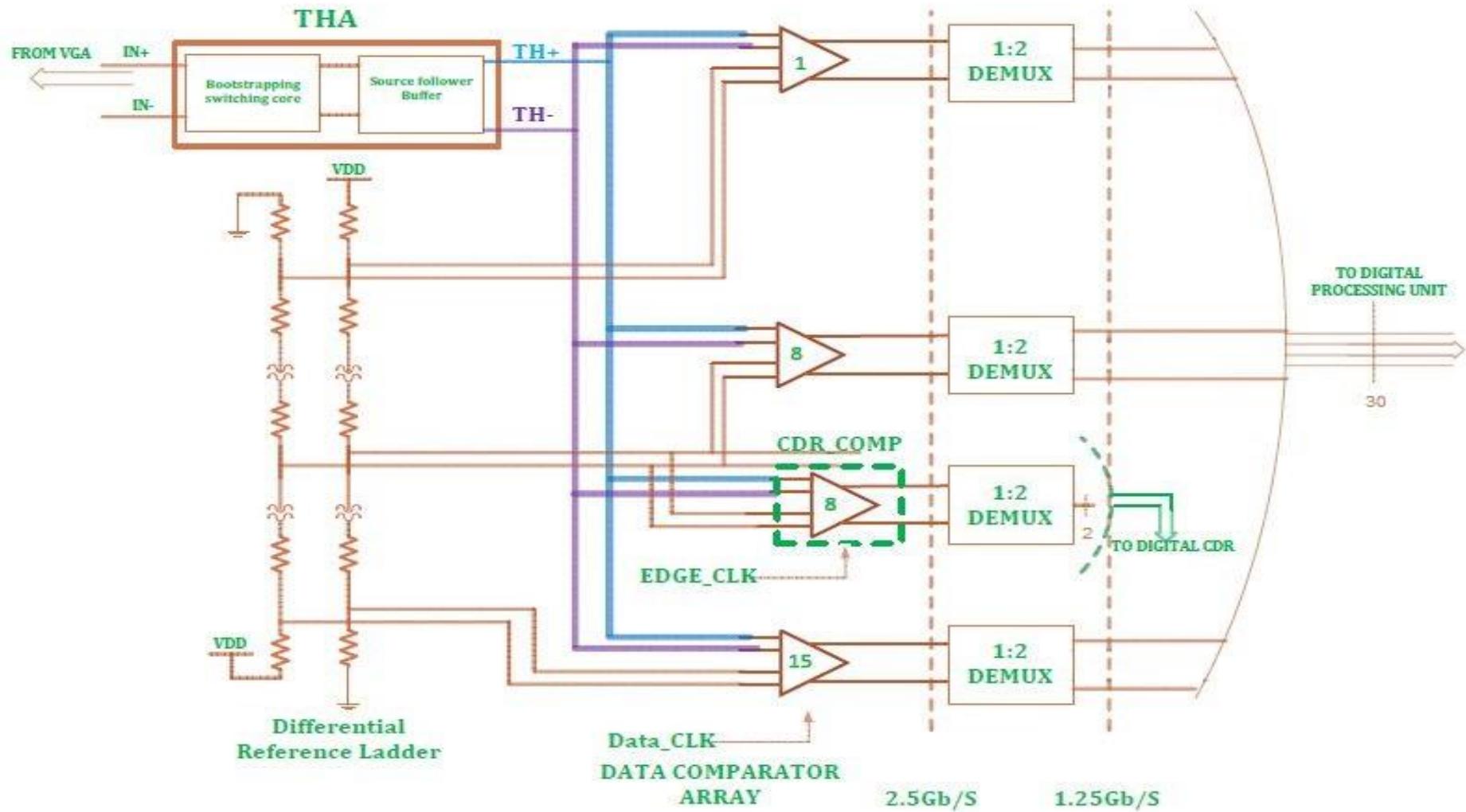
SFDR = 33.4dB for 5GHz input @ 10GS/s

Expected Specs

- ADC is expected to have the following specs at 5GHz input (Nyquist frequency):

Spec	Value
SNR_nominal	25.84 dB
SINAD	21.73 dB
SNR	22.46 dB
THD	-29.84 dB
SDR	29.84 dB
SFDR	33.4 dB
ENOB	3.32 bits

Circuits



Track and Hold Amplifier (THA)

Track and hold Circuit:

- Sampling Switch
- Buffer

TYPE	Open Loop	Closed Loop
Pros	<ul style="list-style-type: none">• High speed (90MHz - 10GHz)*• Unconditionally stable	<ul style="list-style-type: none">• More accurate – linearity on average (50dB - 78dB)*• Reduce charge injection
Cons	<ul style="list-style-type: none">• Pedestal error• Less accurate - Poor linearity (28dB - 63dB)*	<ul style="list-style-type: none">• Less Speed (\leq240MHz)*• Stability issue must be considered

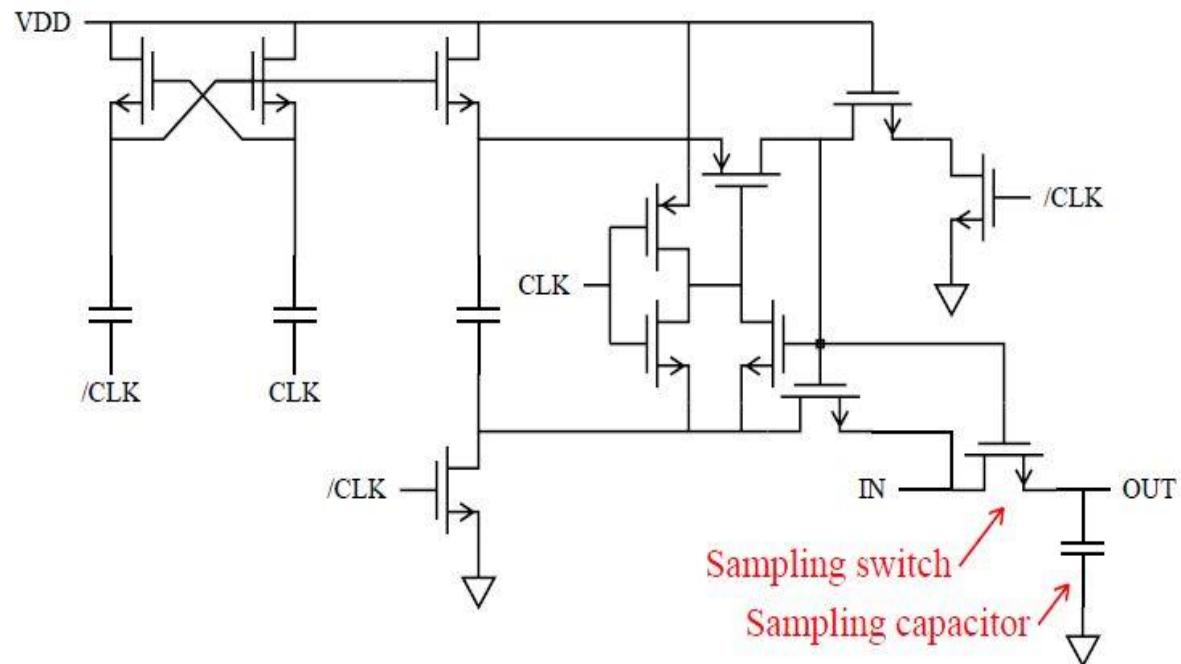
Open Loop Track and Hold Bootstrapped Sampling switch

Pros:

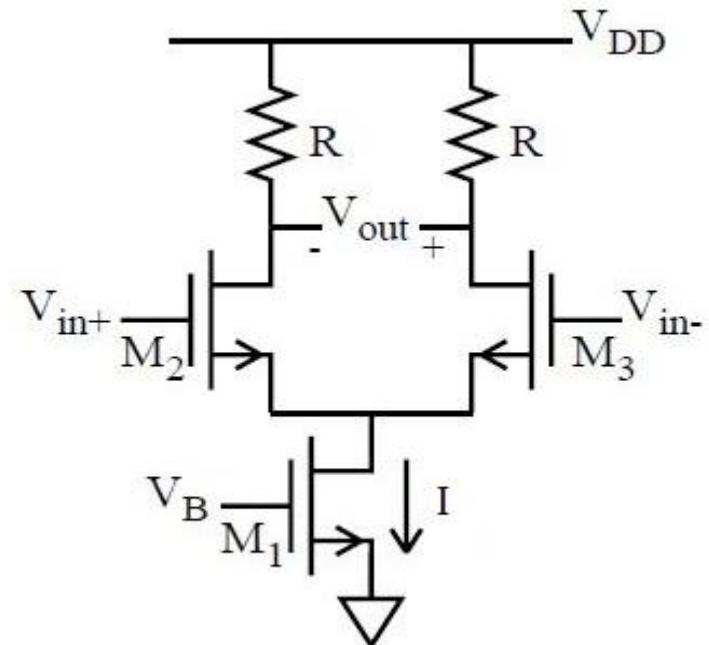
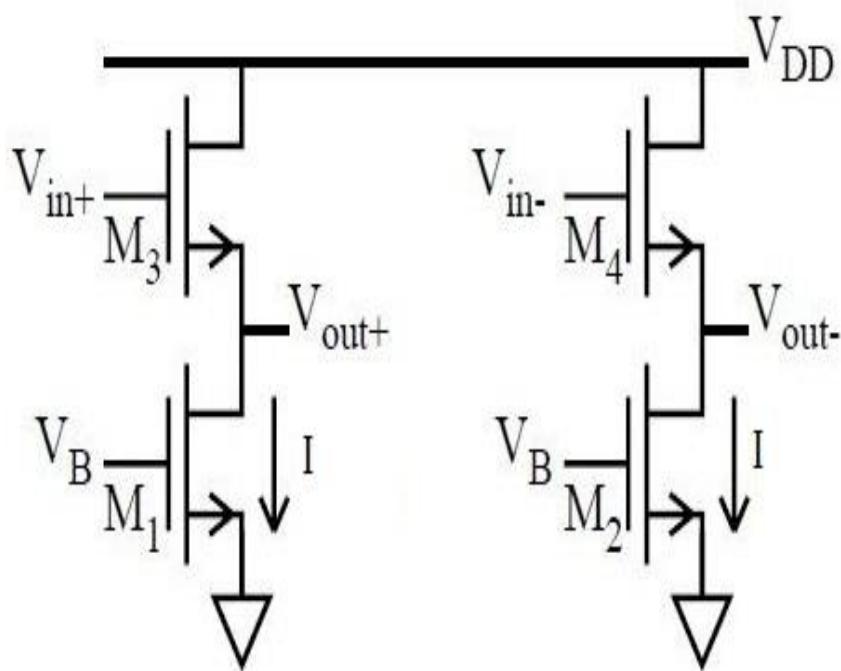
- Higher linearity
- Small switch size
- Less charge/clock injection

expense:

- Caps are large
- μW power consumption



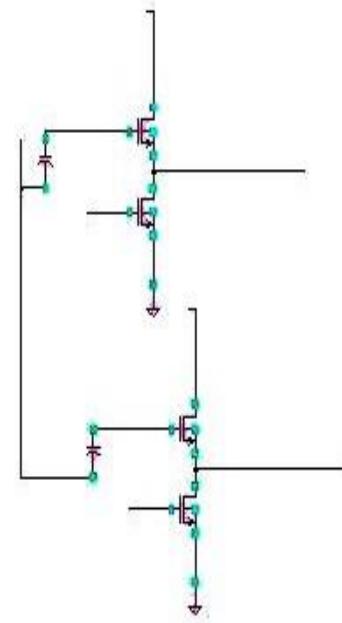
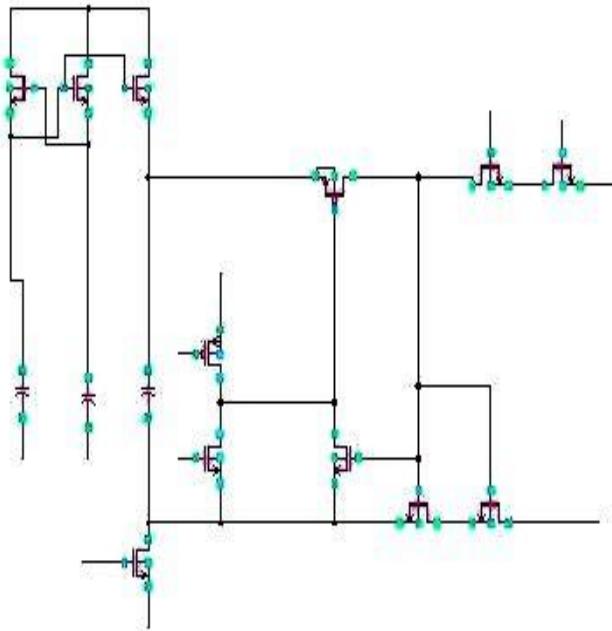
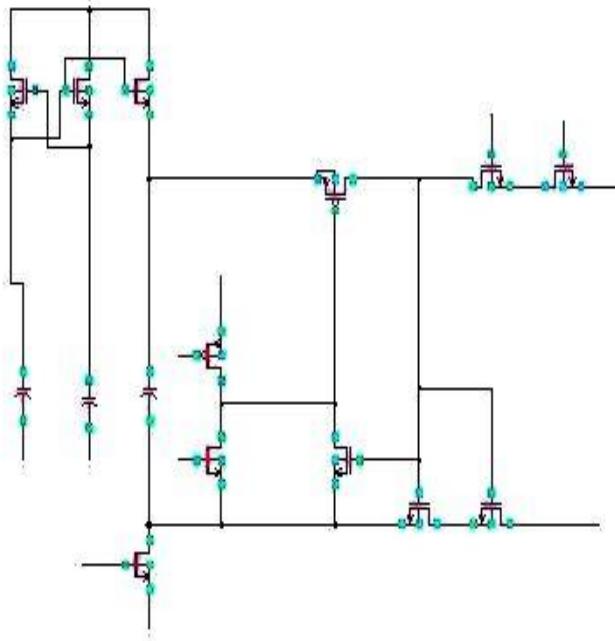
Open Loop Track and Hold Buffer Topologies



SF or DP ?

Topology	Source Follower	Differential Pair
Gain	Determined by second order effects	Determined by first order effects
Linearity	“Body effect – channel length mod.”	
Mismatch sensitivity	Low	High
Controllability		
Design freedom		

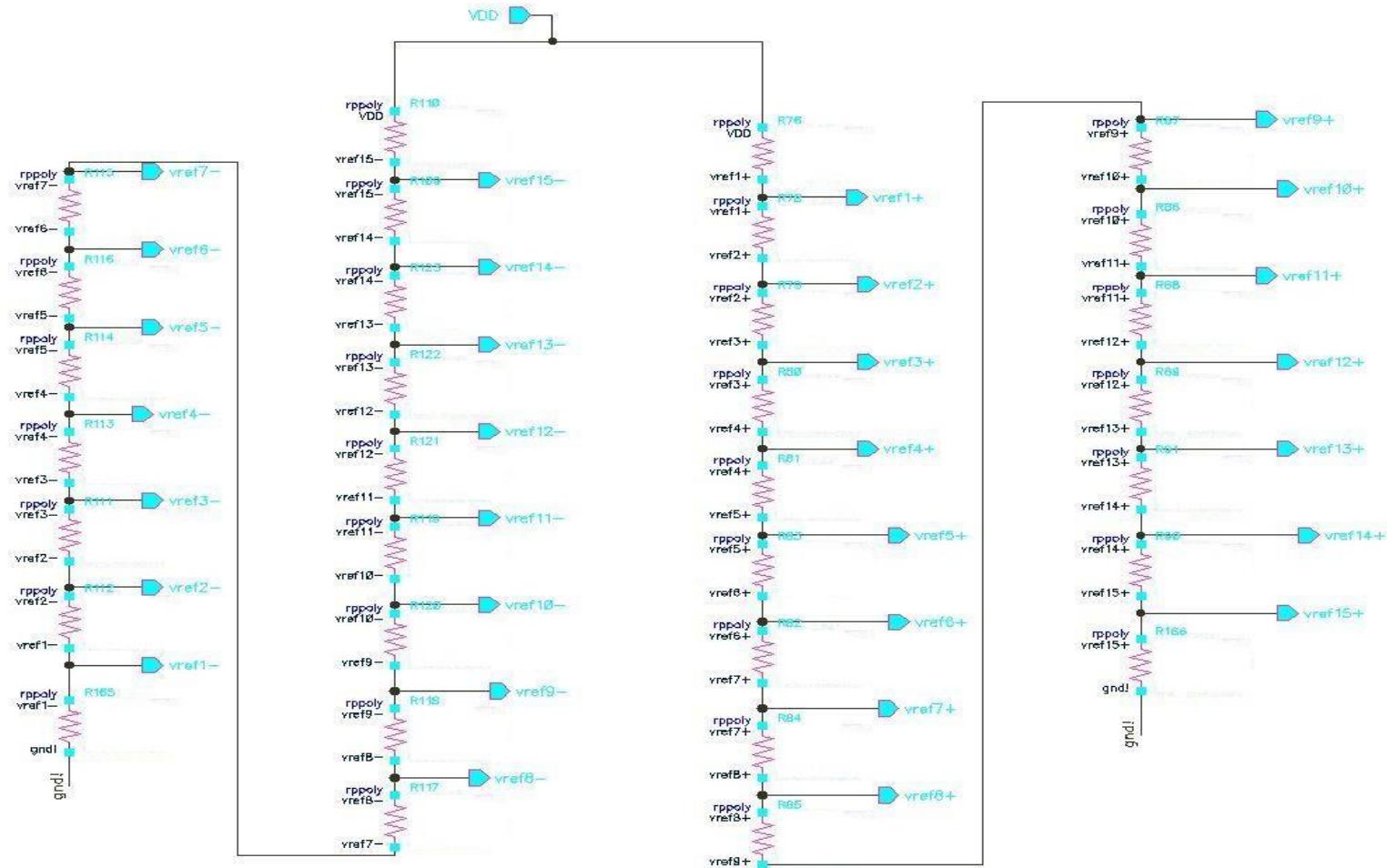
Designed THA



Reference Ladder

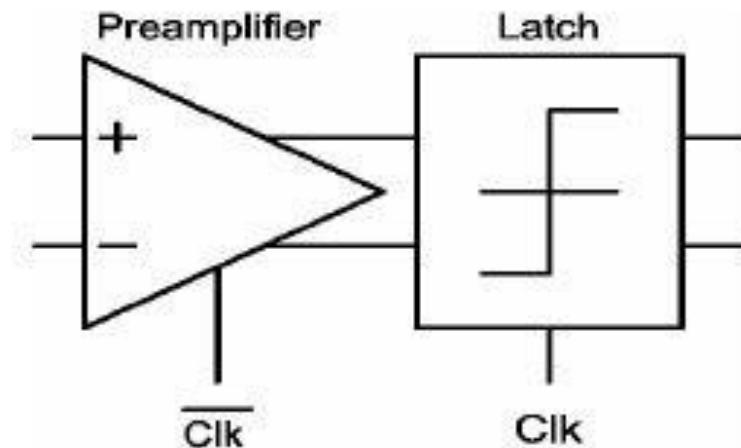
- To generate reference levels
- Stack of resistors in series “voltage divider rule”
- Alternatives:
 - Band-gap references
 - Adjustable references*

Differential Reference ladder

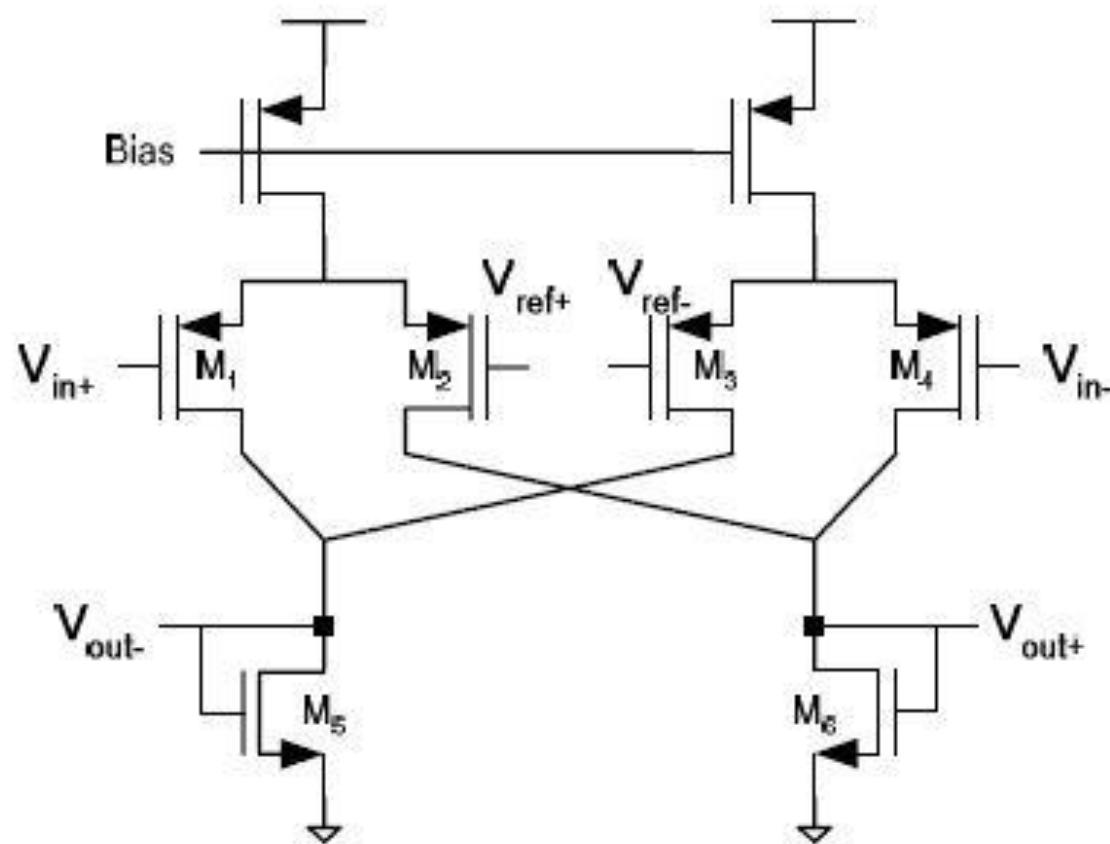


Comparator Design

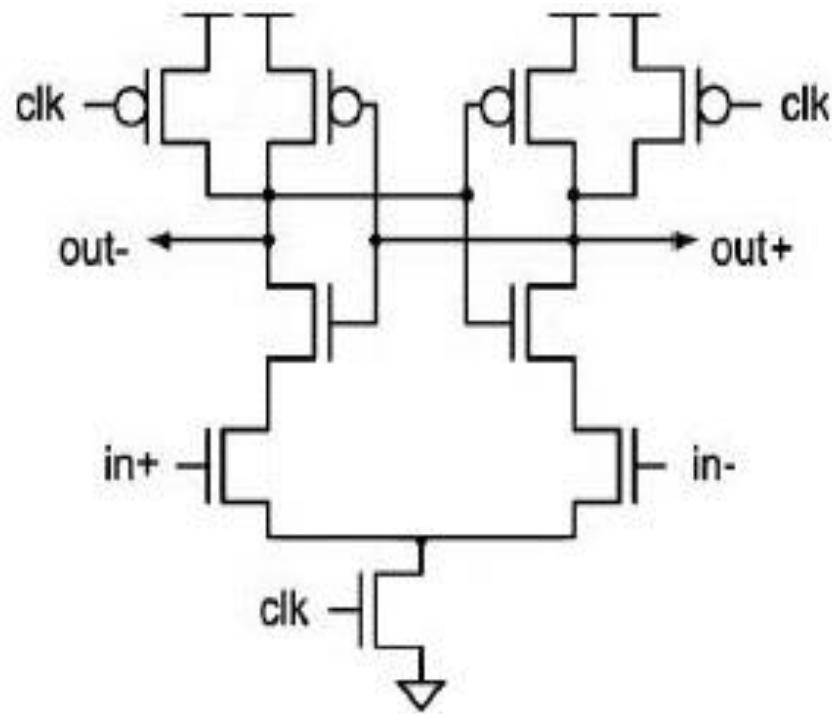
- Comparator consists of:
 - Pre-Amplifier
 - Regenerative latch



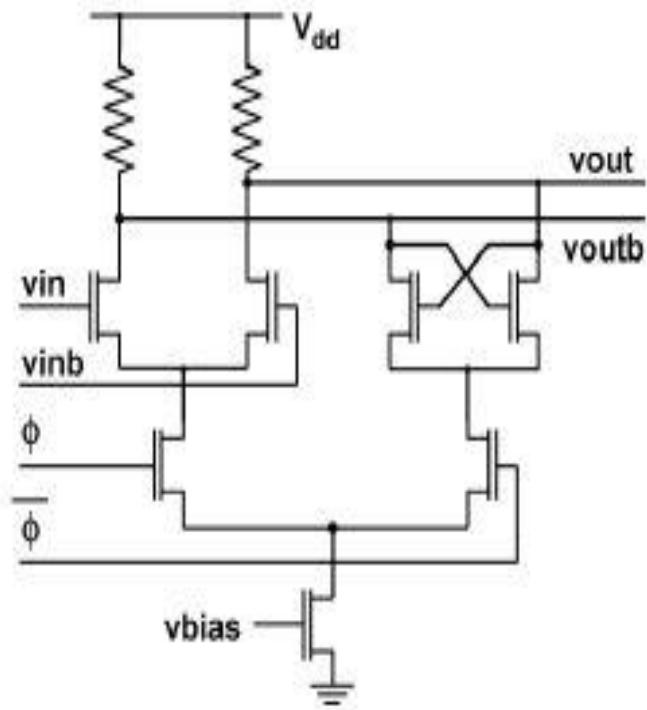
Pre-Amplifier Design



Regenerative Latch

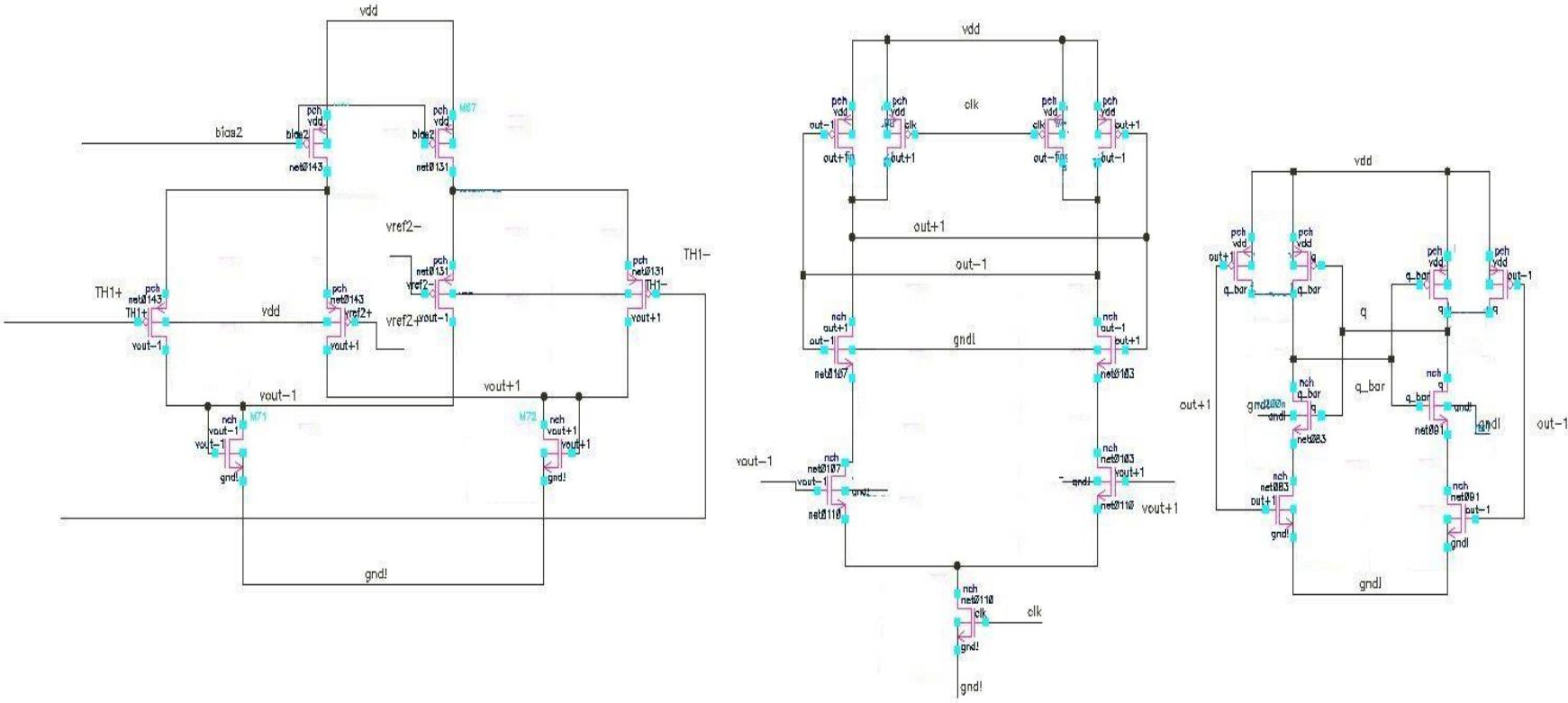


Strong-Arm Latch



CML latch

Designed Comparator



Circuit results (1):

□ THA measured specs:

Process	65 nm
Power supply	1 V
Signal range $v_{in,pp}$	1.2 V
Input common mode voltage	0.6 V
Output common mode voltage	0.3V
SFDR @ 1.25 GHz input	31 dB
Supported Load	300f F
Topology	Source follower
FOM_SFDR	34.21 fJ
Sampling frequency (fs)	2.5 GHz
Power consumption	2.44 mW

Circuit results (2):

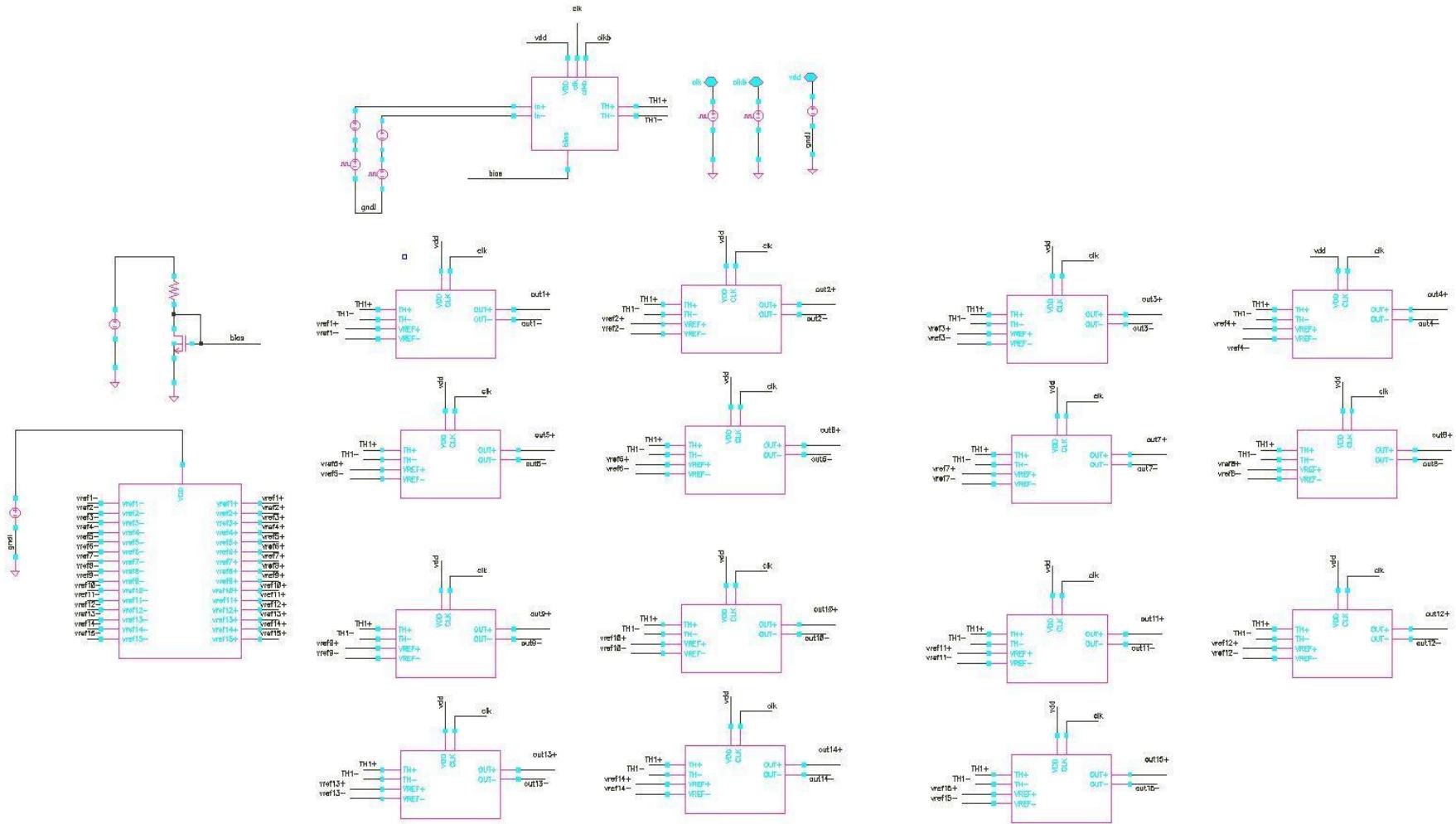
□ Reference ladder specs:

Power	16.83 mW
Single resistance value	4 ohm
Resistance Stack	116.7 ohm
systematic error in reference value	± 3.6 mV

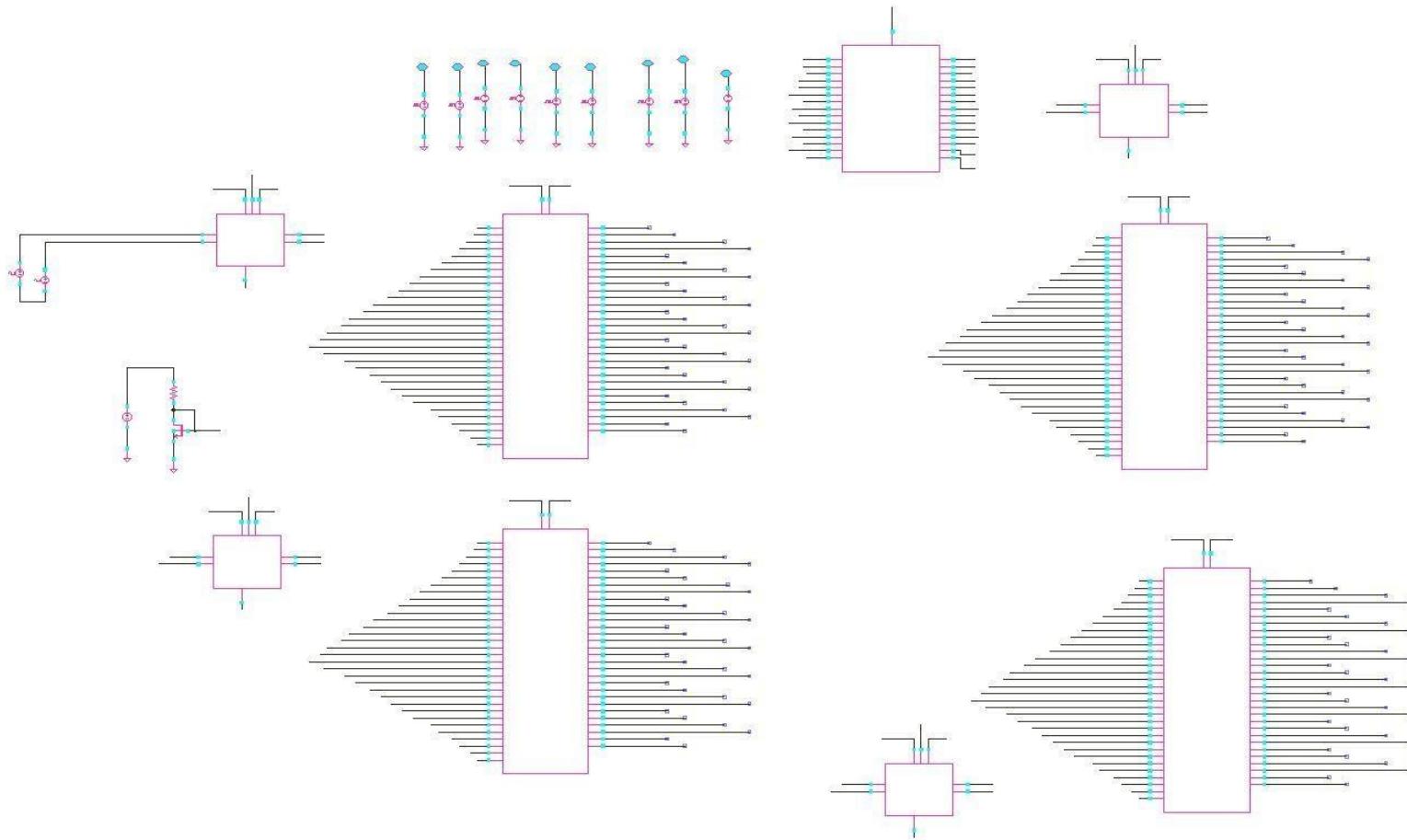
□ Comparator Specs:

Power	2 mW
Maximum systematic offset	13 mV
Delay	88.4 psec

Sub-ADC

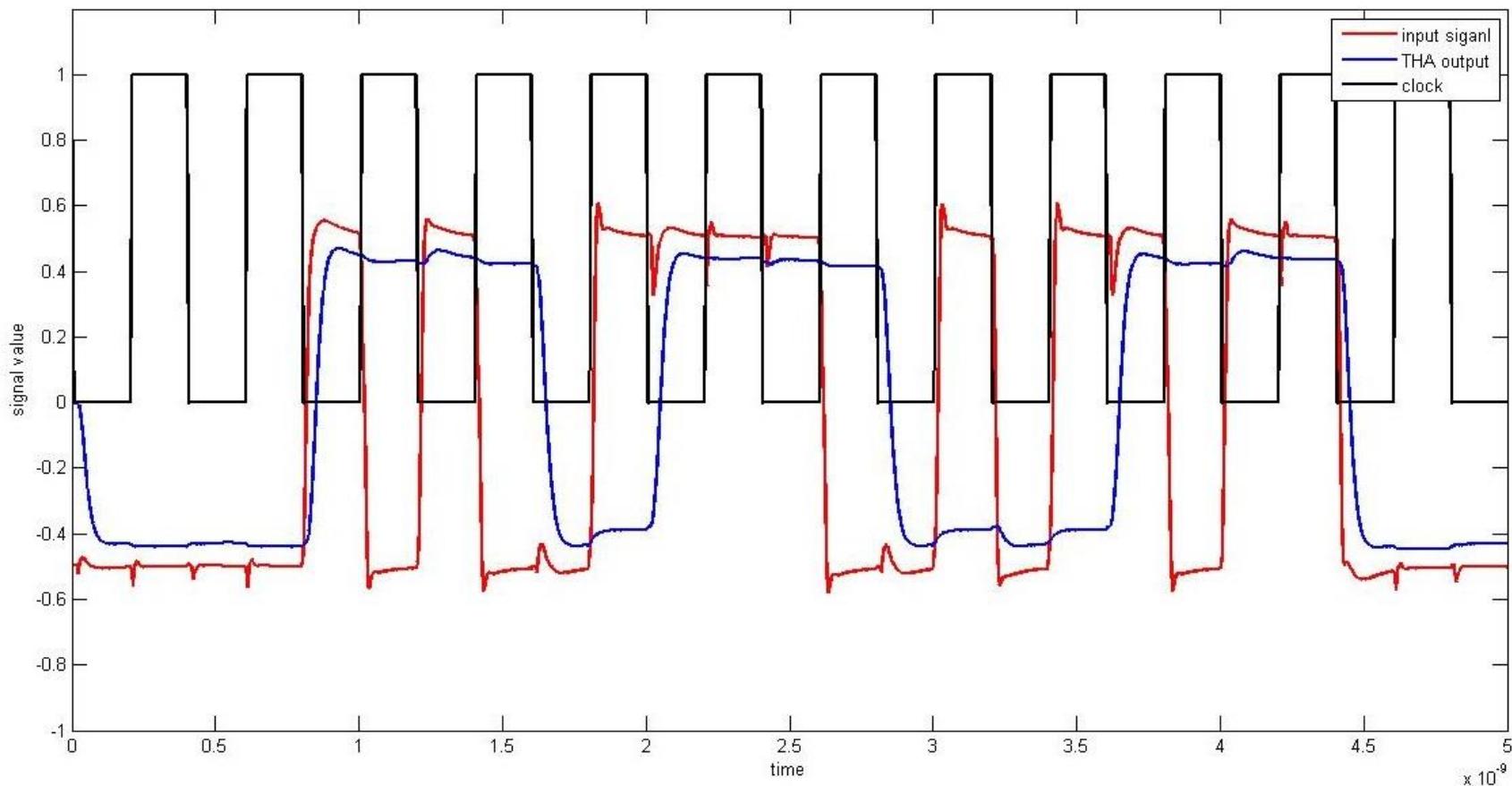


Full Flash ,Time Interleaved ADC



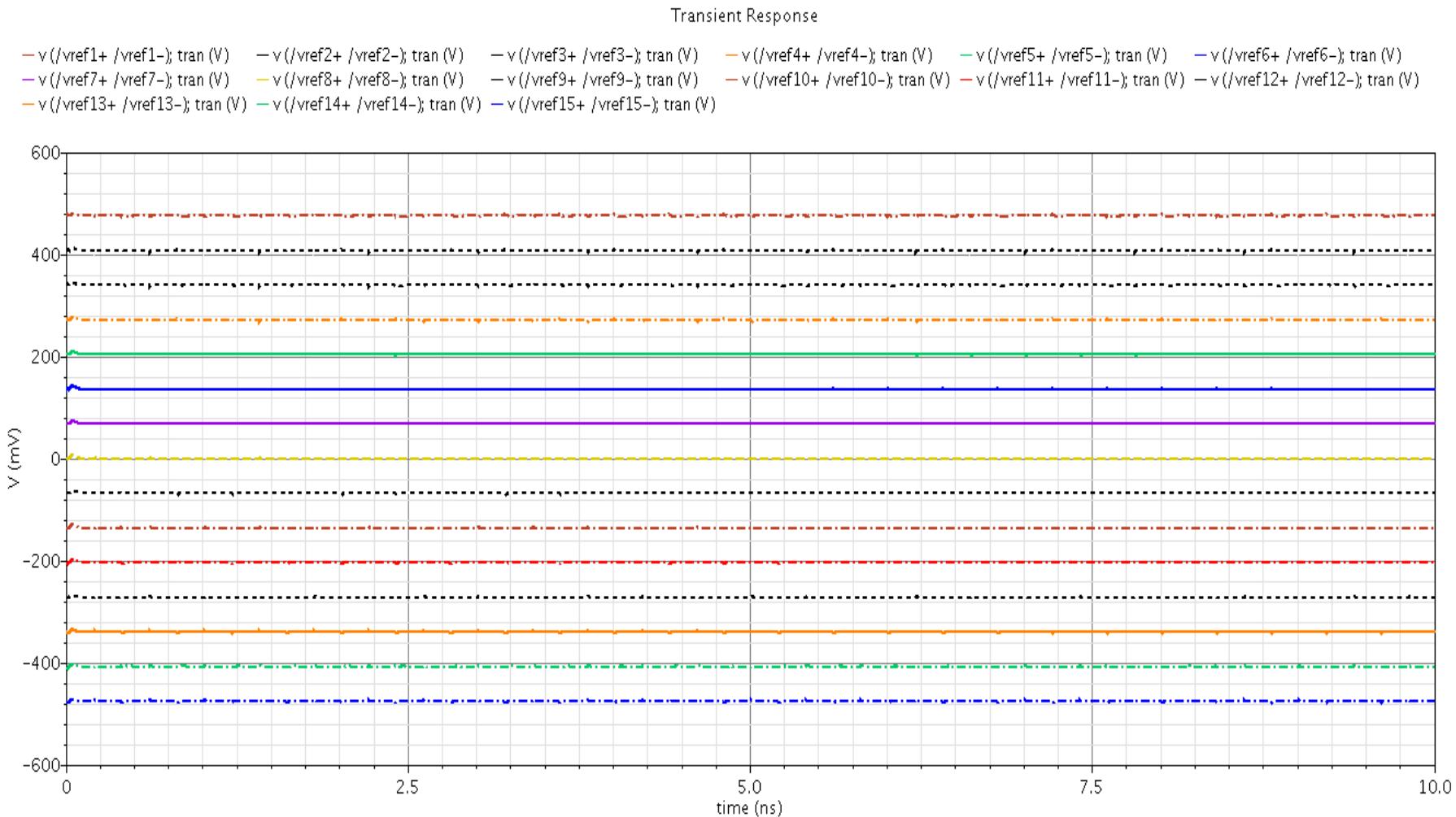
Simulation Results(1)

THA output for Random input stream



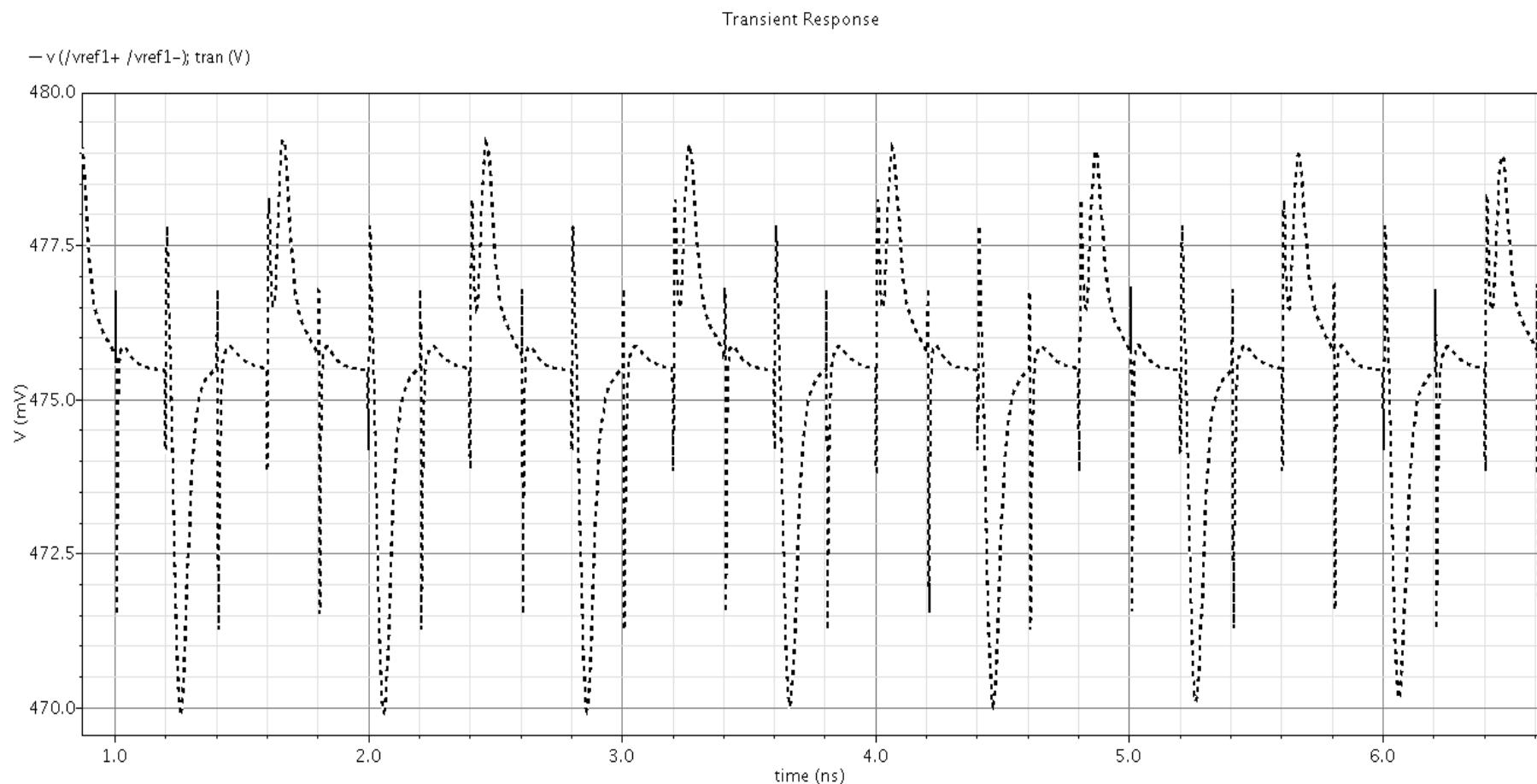
Simulation Results(2)

Reference levels for Comparators



Simulation Results(3)

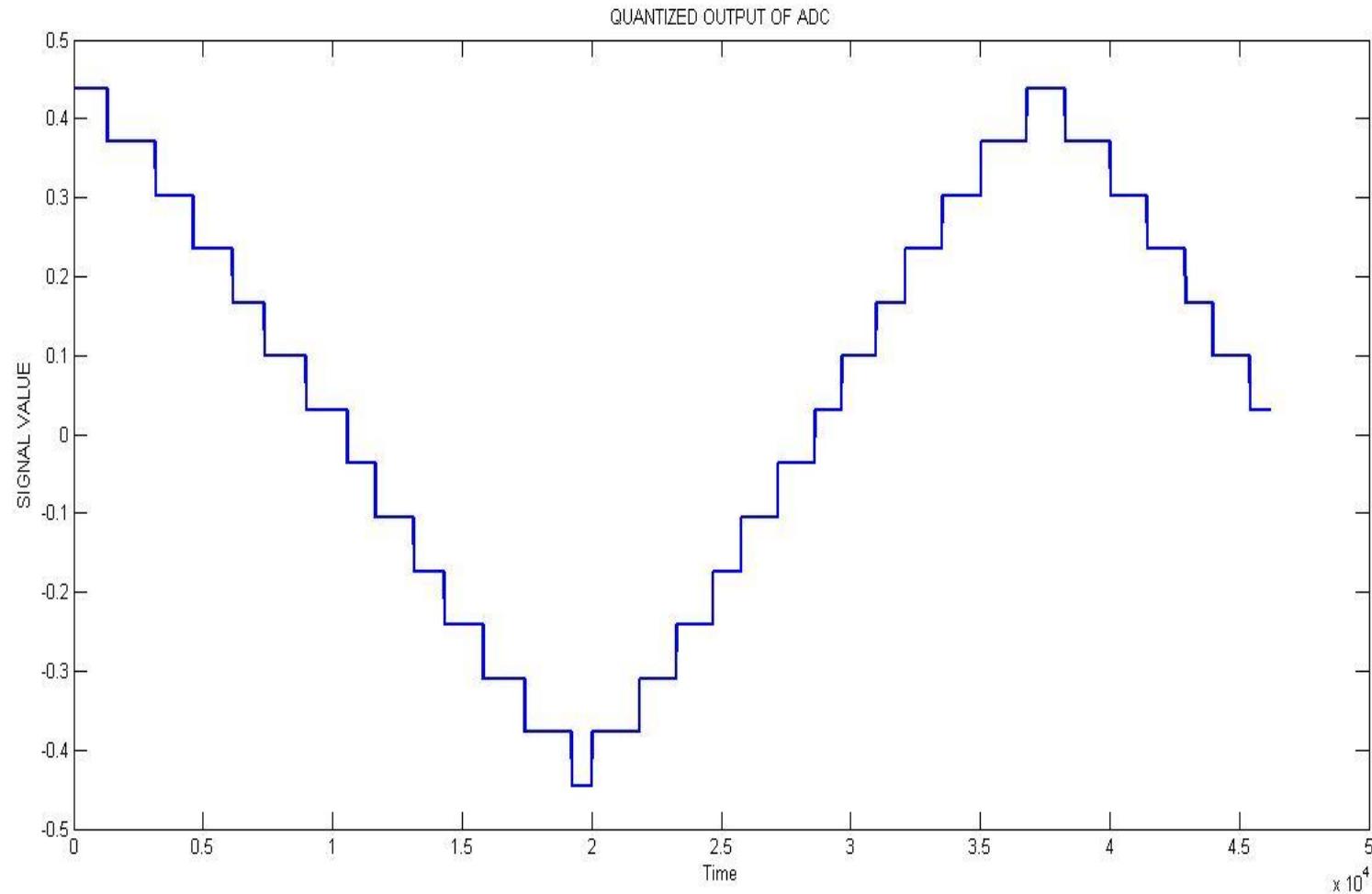
Single reference level, showing the effect of kickback noise and input feed-through



Simulation Results(4)

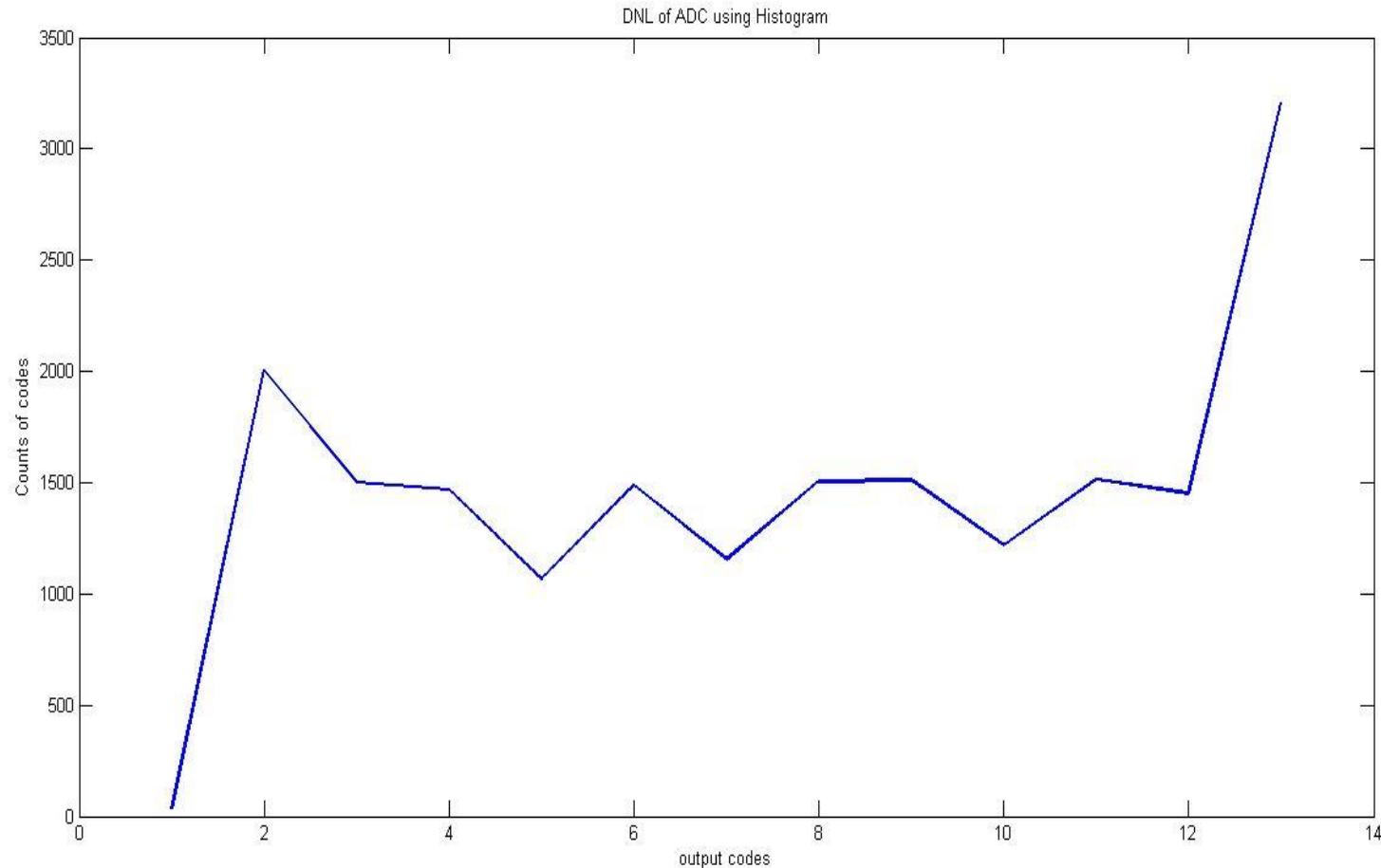
static performance

Analog output corresponding to output codes from the ADC



Simulation Results(5)

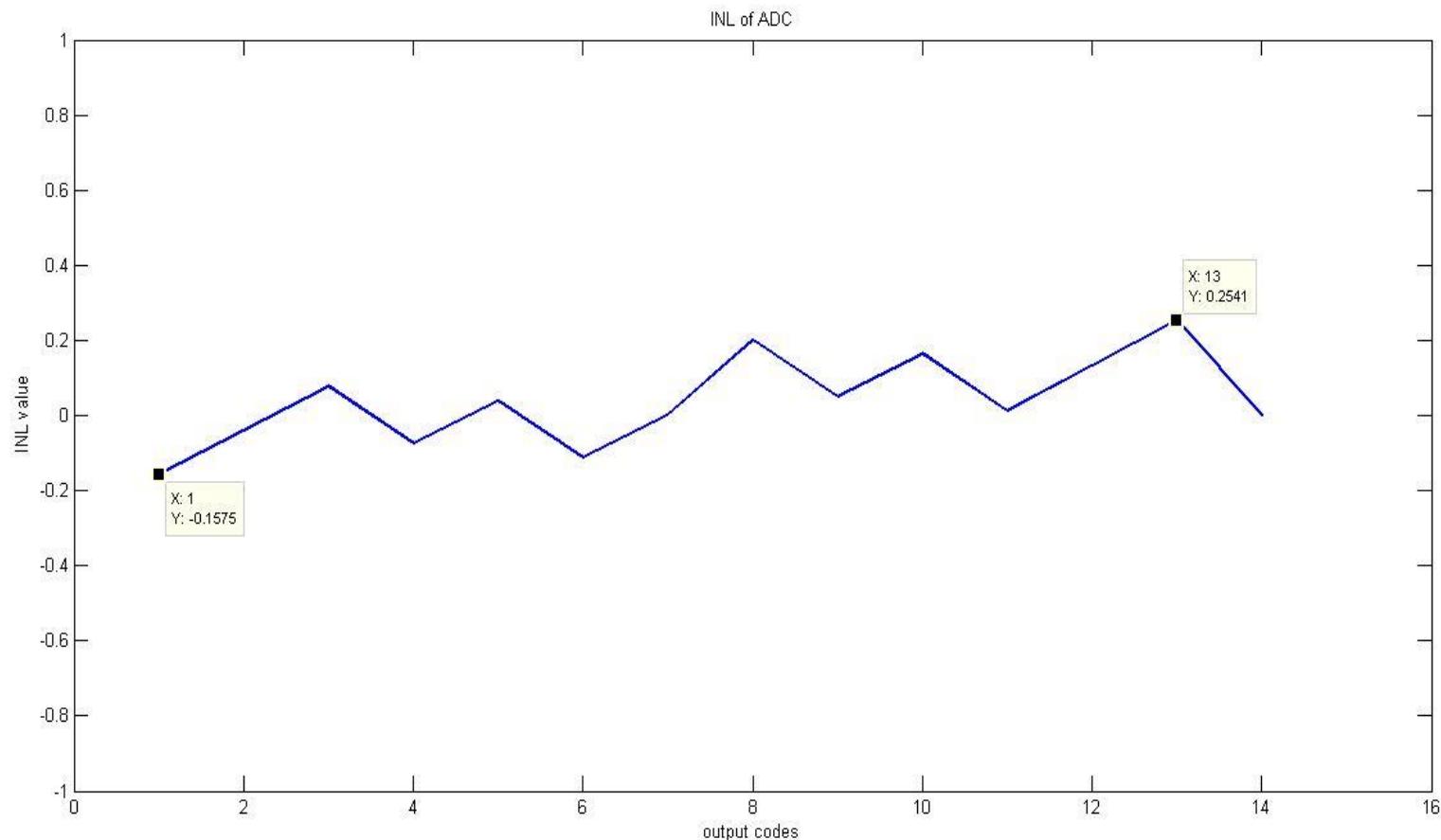
DNL -using histogram Method-



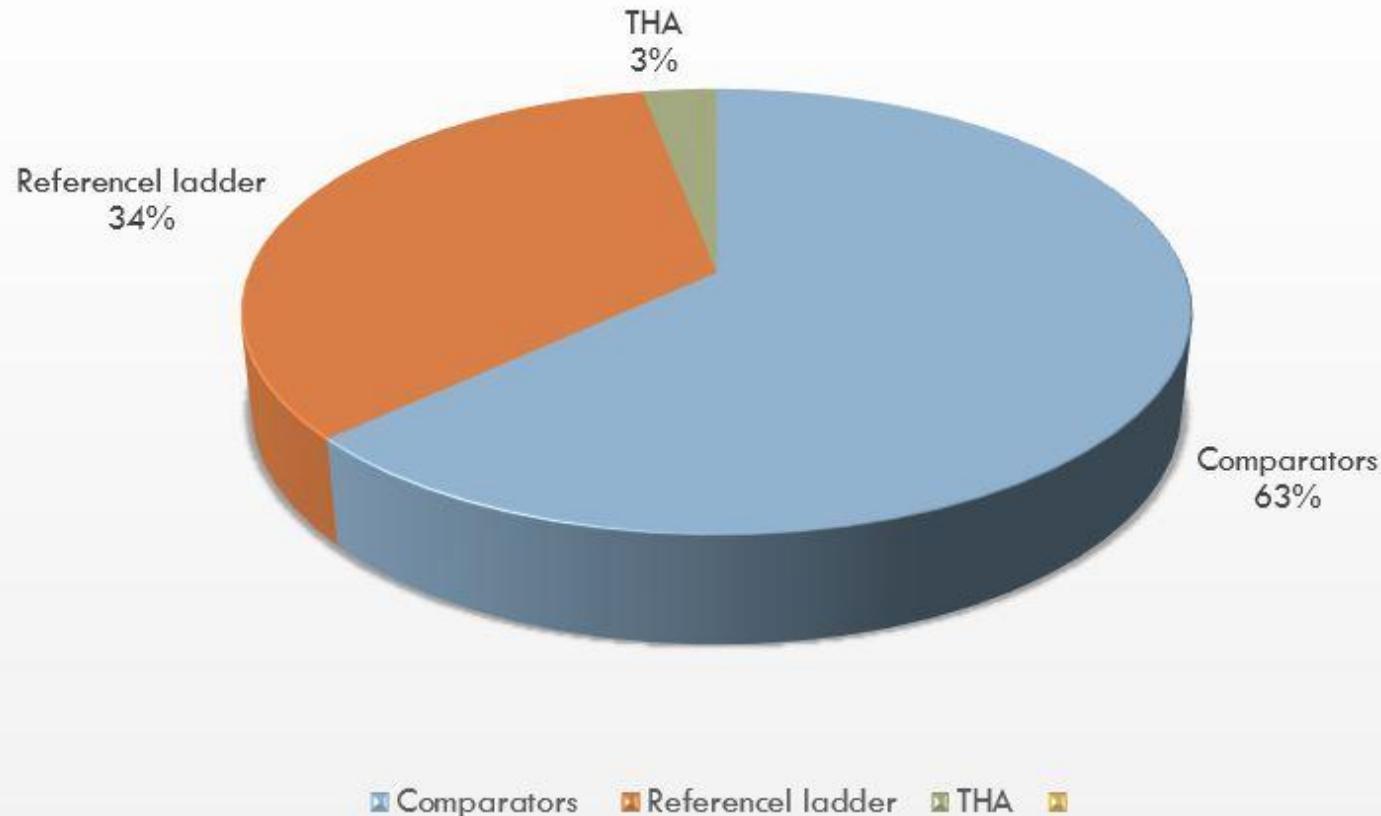
Simulation Results(6)

INL

INL = +0.25/ -0.16 → No mis-codes

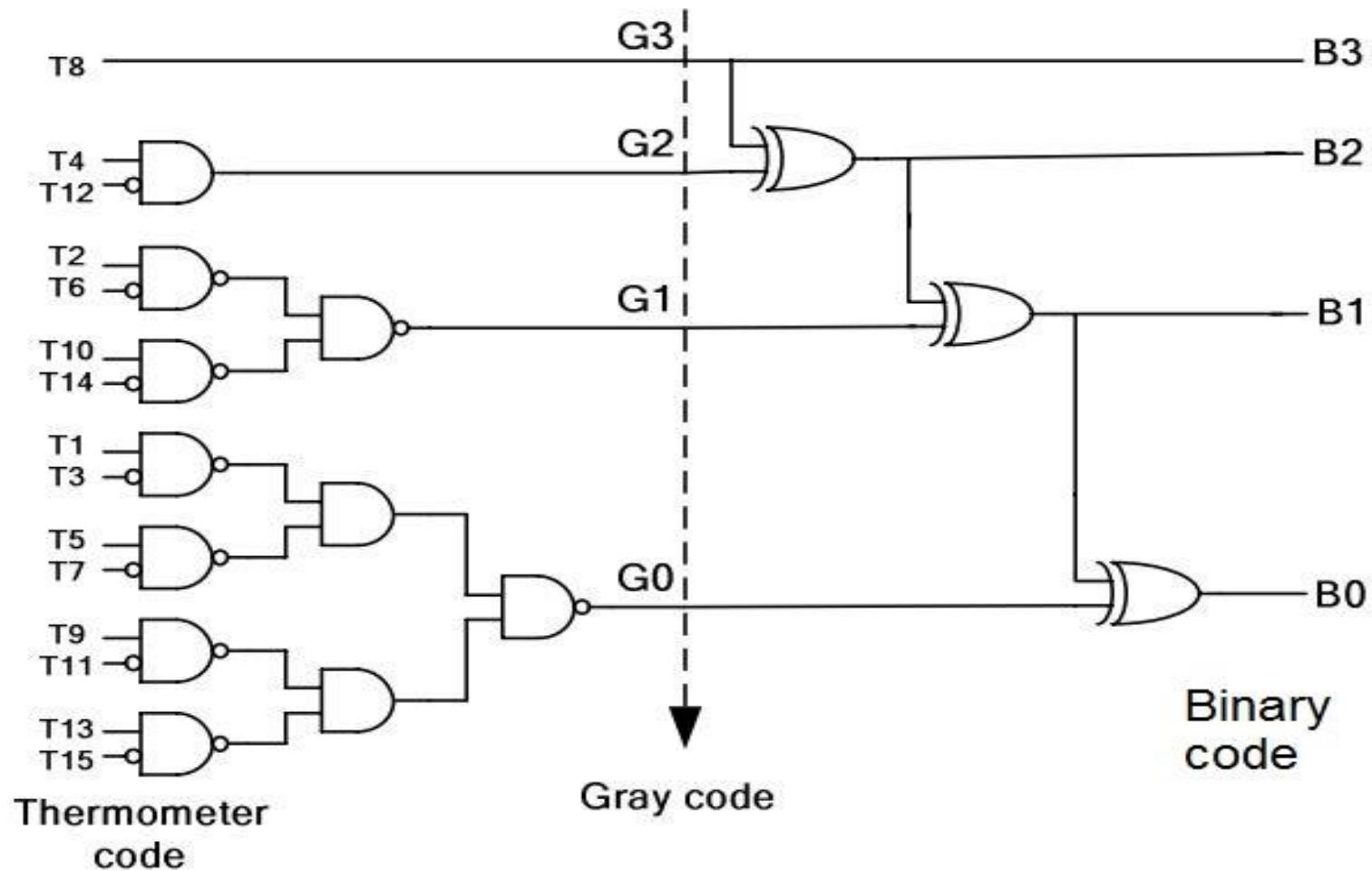


Power consumption distribution



Total consumed power per single ADC (2.5 GSps)= 49.6 mW

Thermometer to binary Decoder

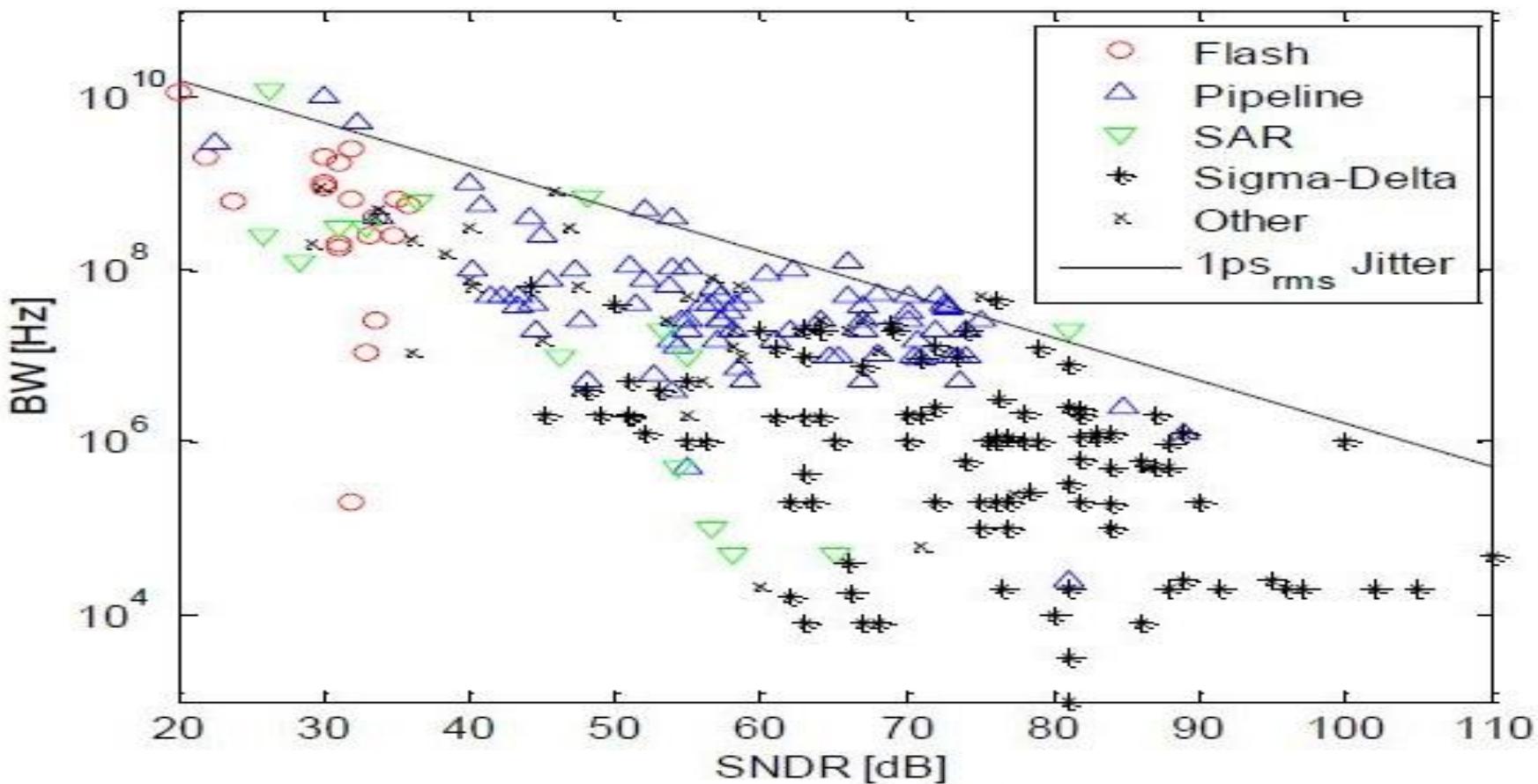


Final results

Total Power	158 mW
FSR (DR)	1 Vp-p
SNDR	20.42 dB
ENOB	3.1 bits
INL	+0.25 / -0.16
FOM	1.58 pJ/Conversion step
SFDR @ 5GHz	28 dB

Comparison with literature

ADC Performance Survey 1997-2013 (ISSCC & VLSI Symposium)



Future work

- Variable reference levels “digitally controlled by the equalizer”
- Offset cancellation circuit
- Digital calibration for the ADC



Questions ?

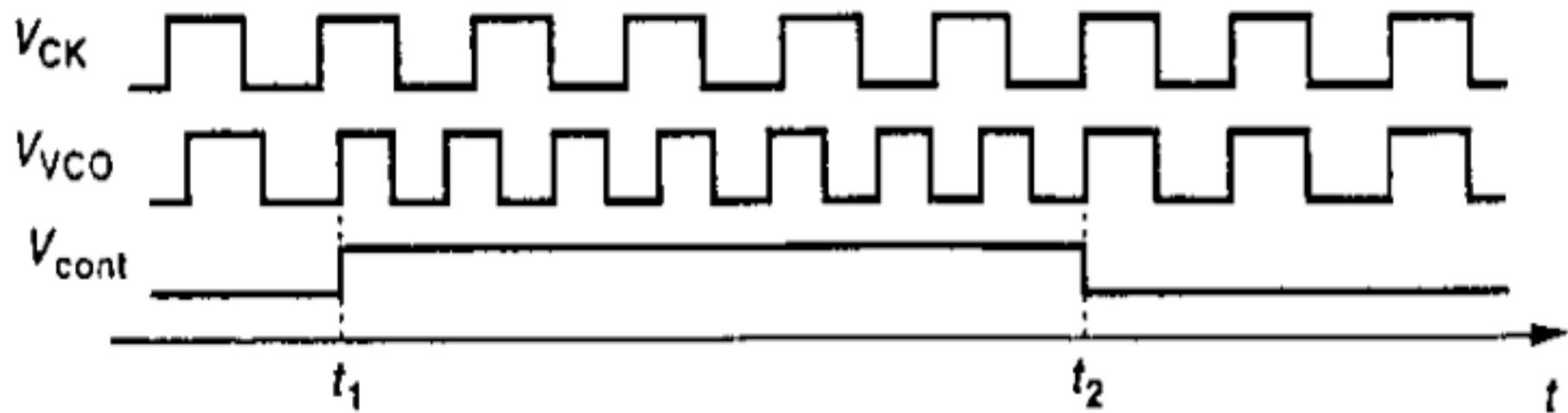
PLL SYSTEM



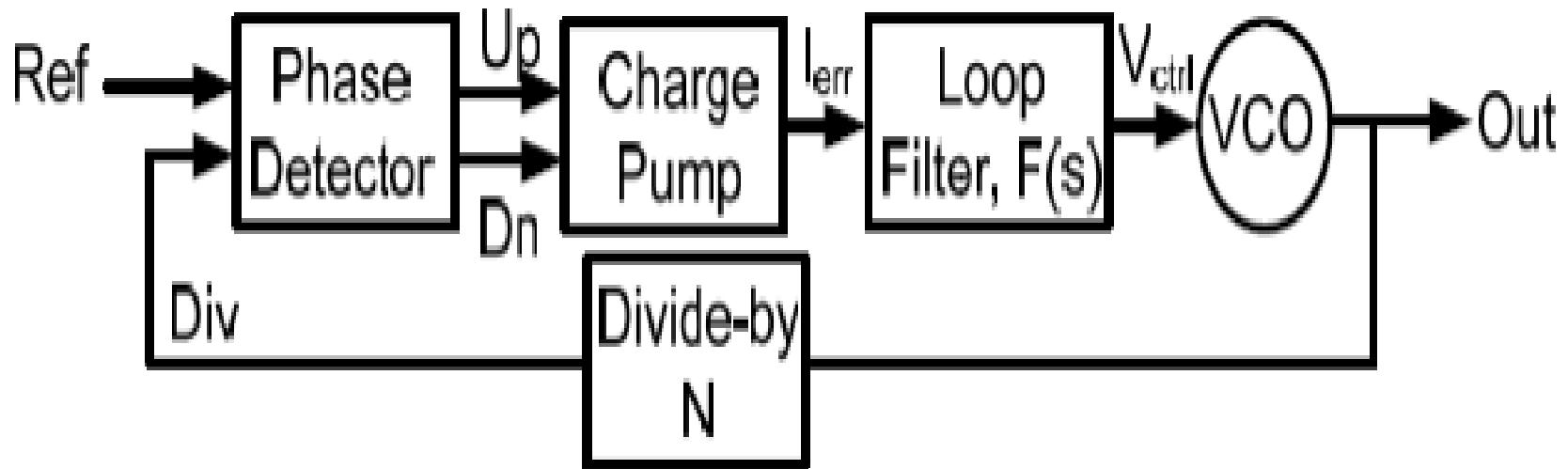
Overview

- What is PLL ?
- Block Diagram of PLL
- Targets and Specifications
- Simulations and results

What is PLL ?



Block Diagram of PLL

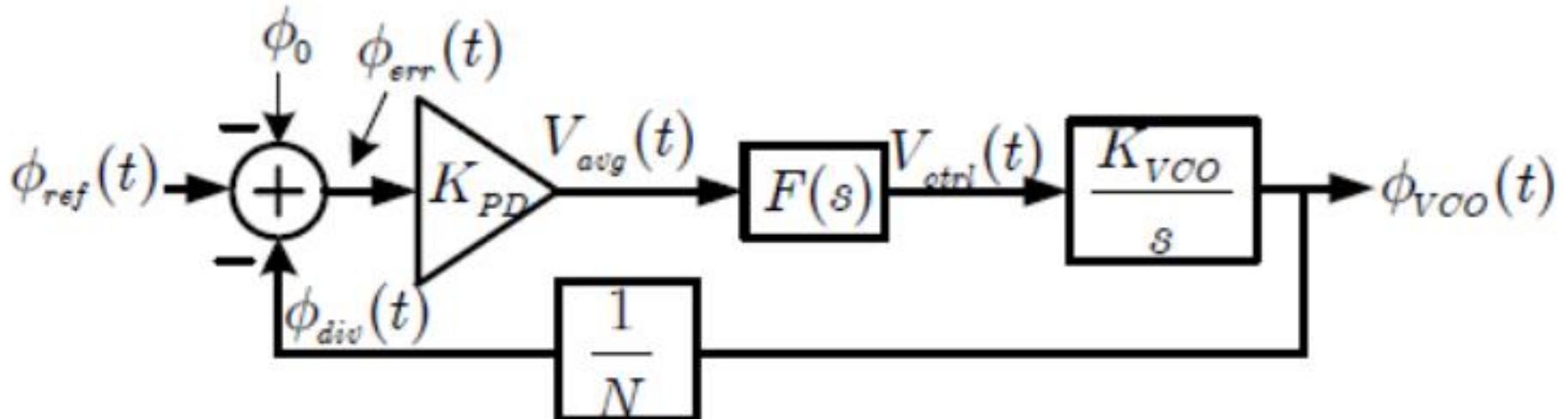


Targets & Specs

- Targets: Eliminating Frequency & Phase errors
- Specifications

Jitter	1ps
Phase Margin	60 degrees
K_{vco}	700MHz/V
I_{cp}	150 uA

Block Diagram



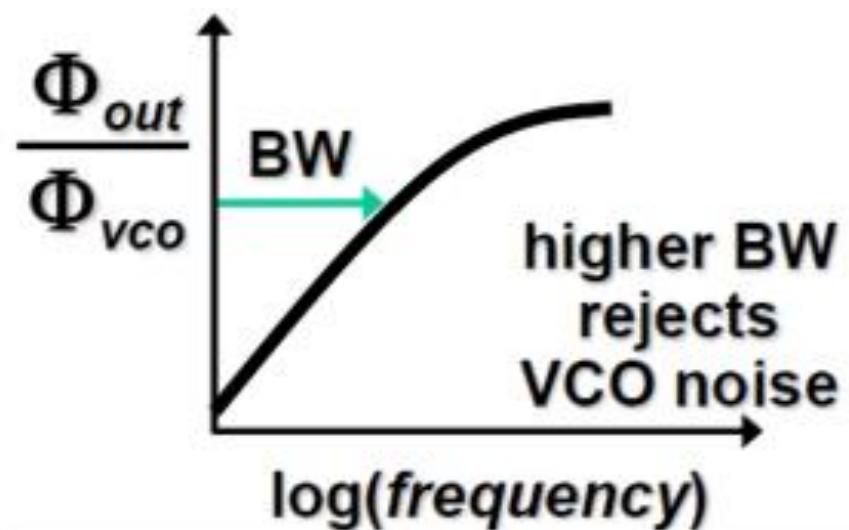
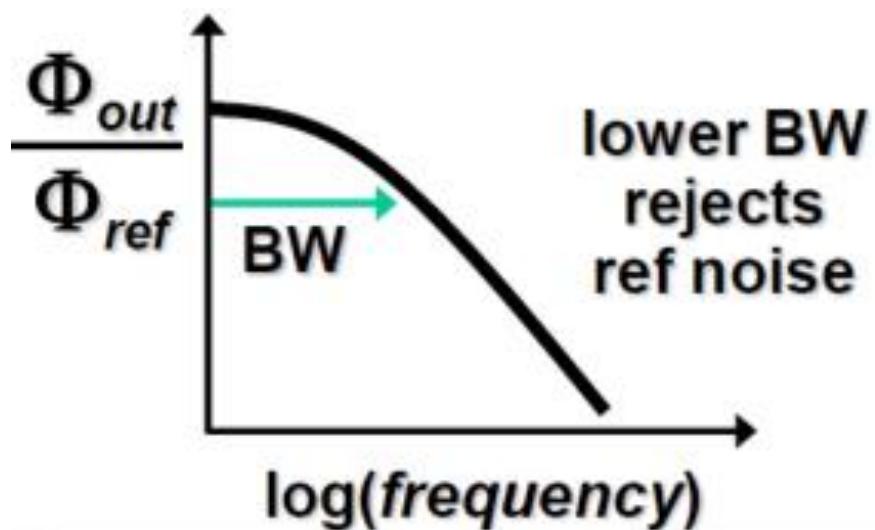
The transfer function of the system is given by:

$$A_\phi(s) = \frac{N(1+s\tau_2)}{1+s\tau_2 + \frac{s^2\tau_2}{K} + \frac{s^3\tau_2\tau_p}{K}}$$

where

$$k = \frac{b-1}{b} \frac{I_{cp} K_{VCO} R}{2\pi N}, \quad \tau_2 = RC_2, \quad \tau_p = R \frac{C_1 C_2}{C_1 + C_2} \quad \text{and} \quad b = 1 + \frac{C_2}{C_1}$$

Noise Performance in PLL



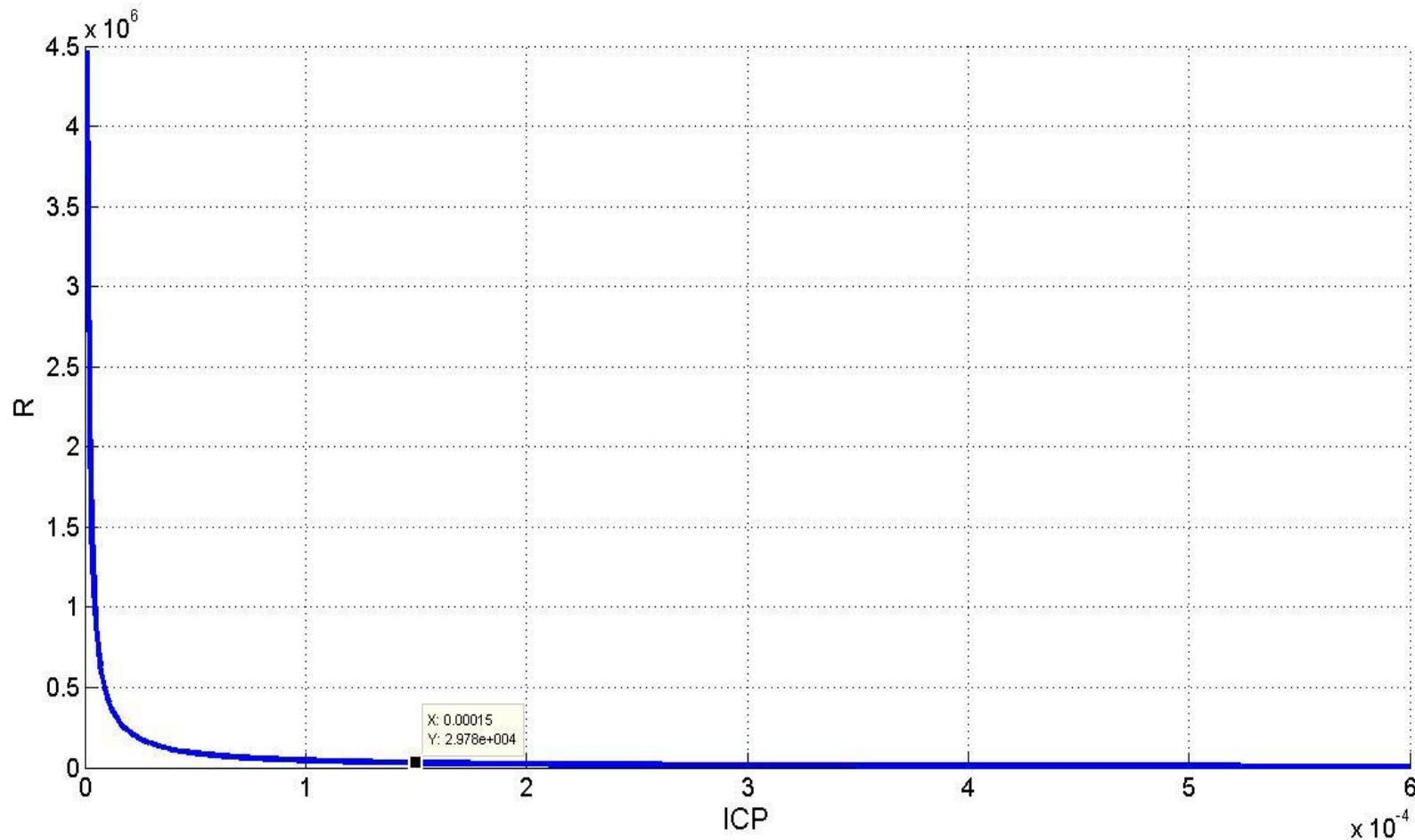
Simulations and Results

□ PLL Parameters

Parameter	Value
Reference Frequency	156.25 MHz
N	66
K_{vco}	700MHz/V
BW	7MHz
Phase margin	60 degrees
Peaking	< 2 dB

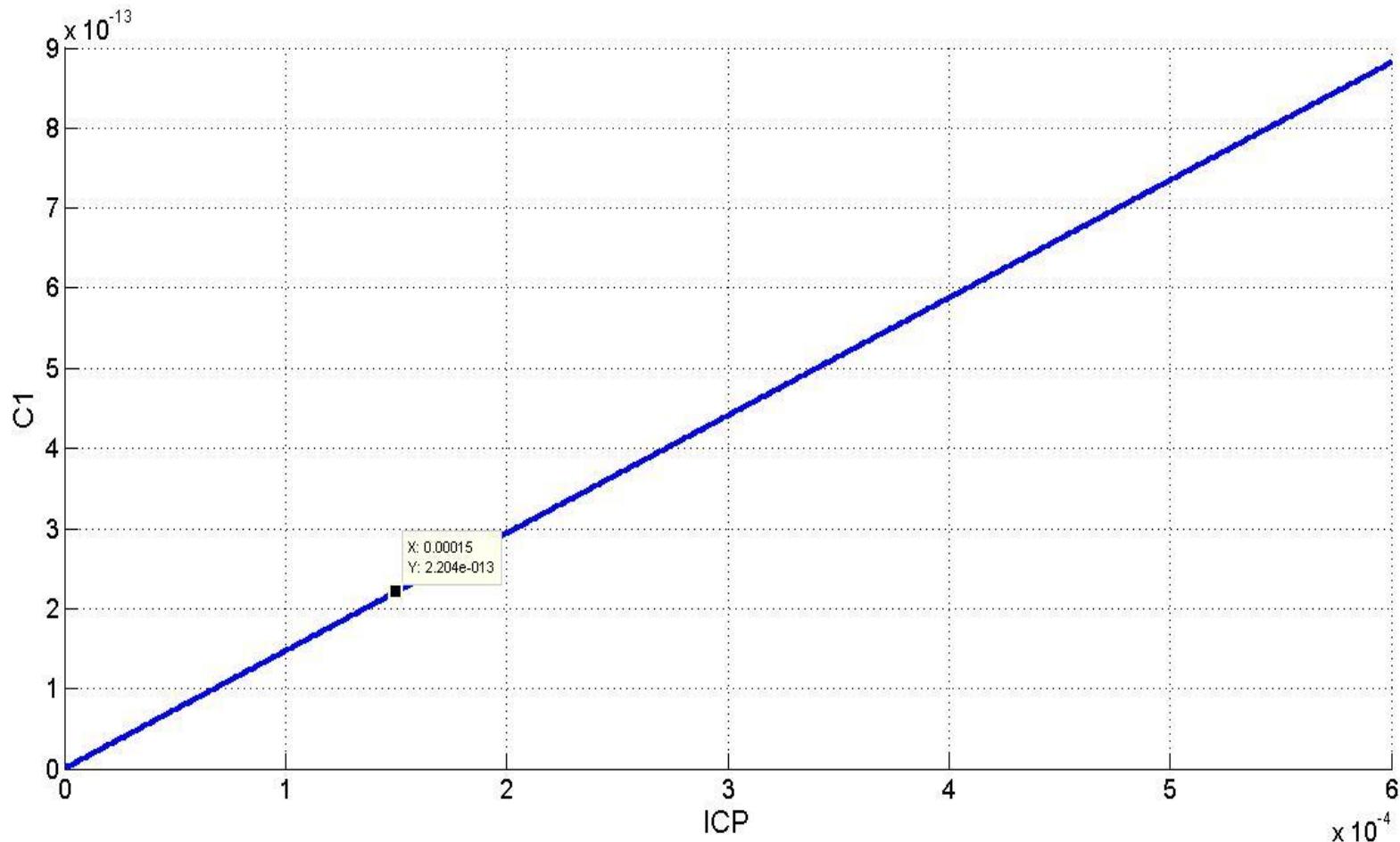
Simulations and Results

□ $R = 29.78\text{K}\Omega$



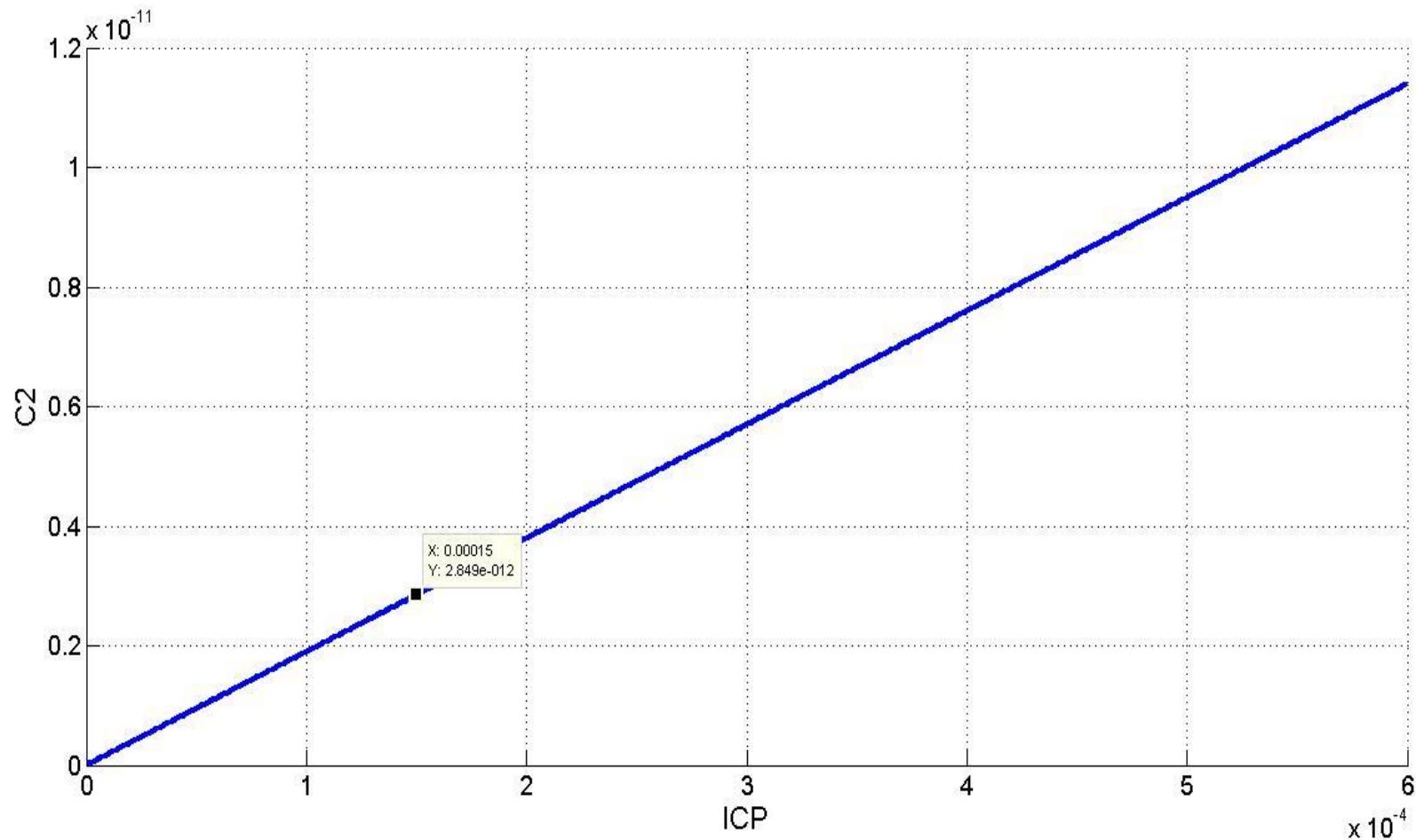
Simulations and Results

- $C_1 = 0.22\text{pF}$



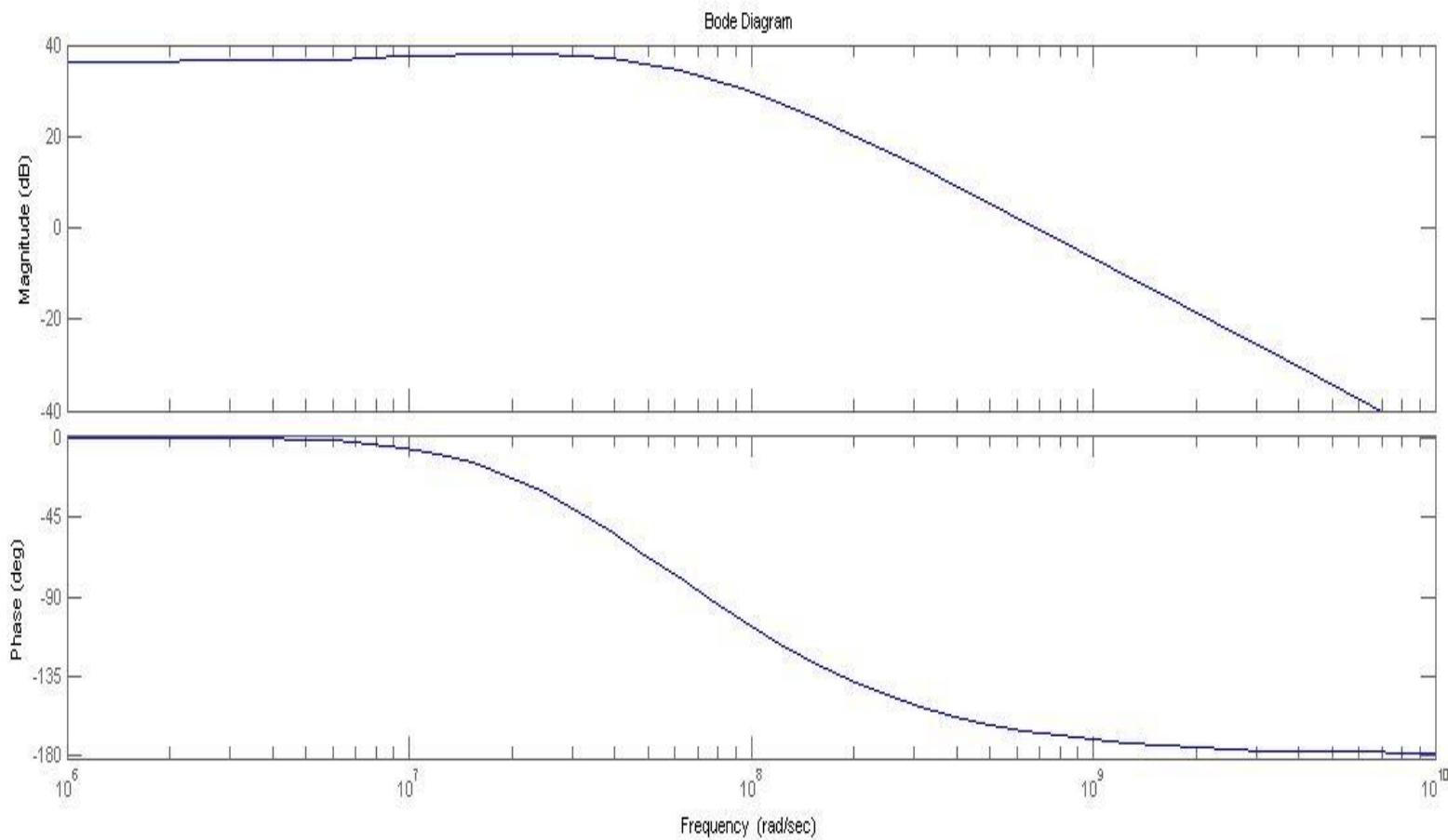
Simulations and Results

□ $C_2 = 2.85\text{pF}$



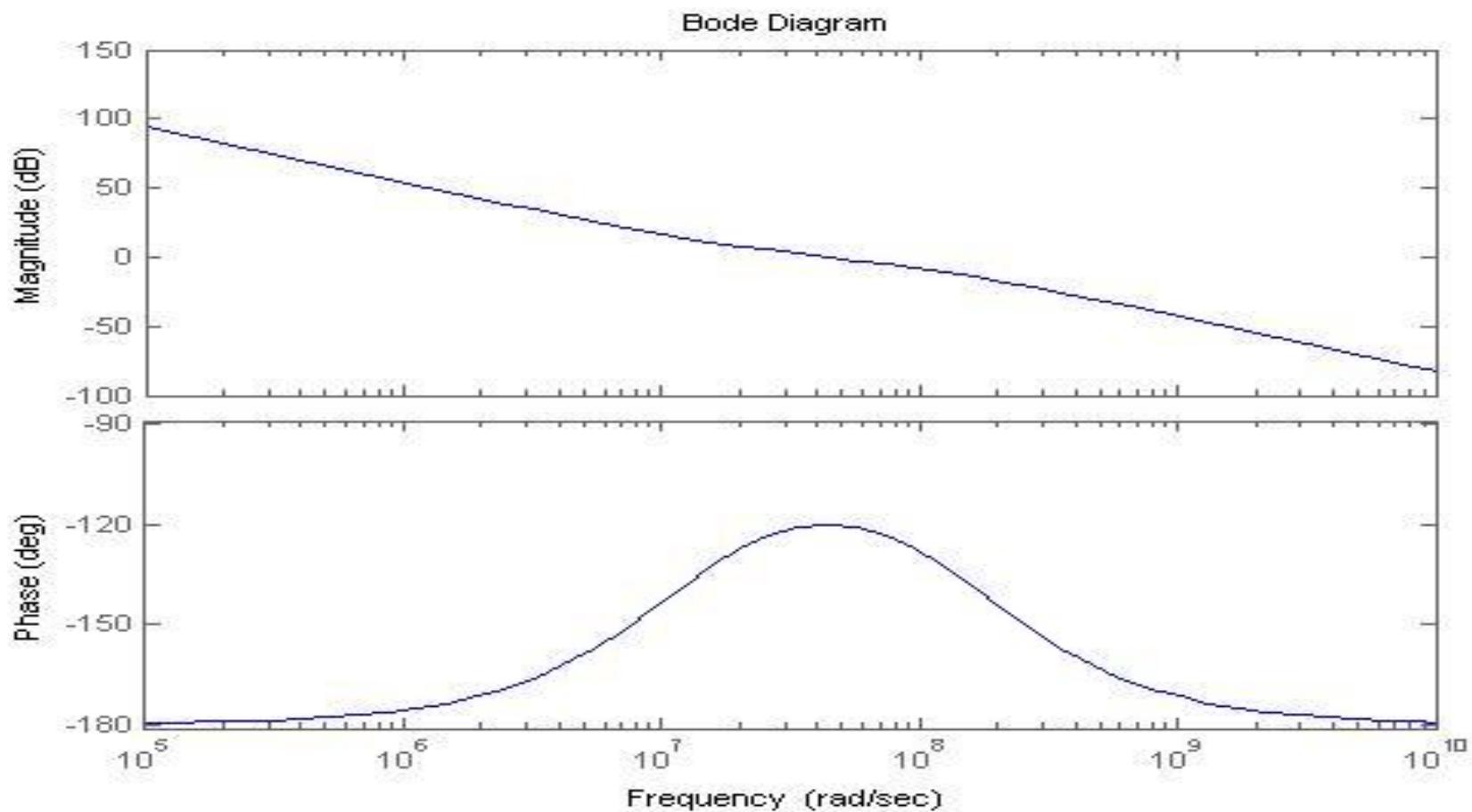
Simulations and Results

□ Closed Loop Transfer Function



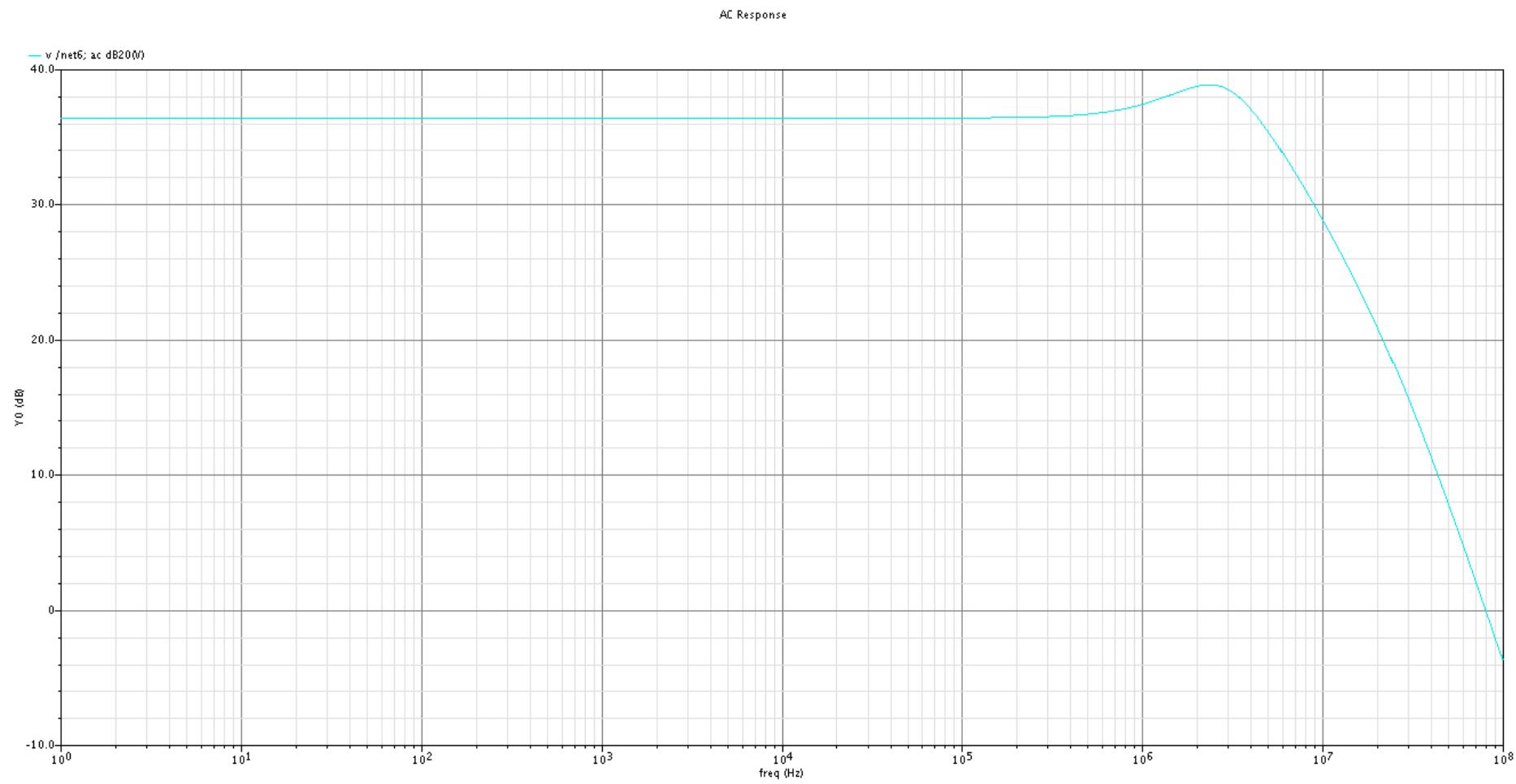
Simulations and Results

□ Open Loop Transfer Function



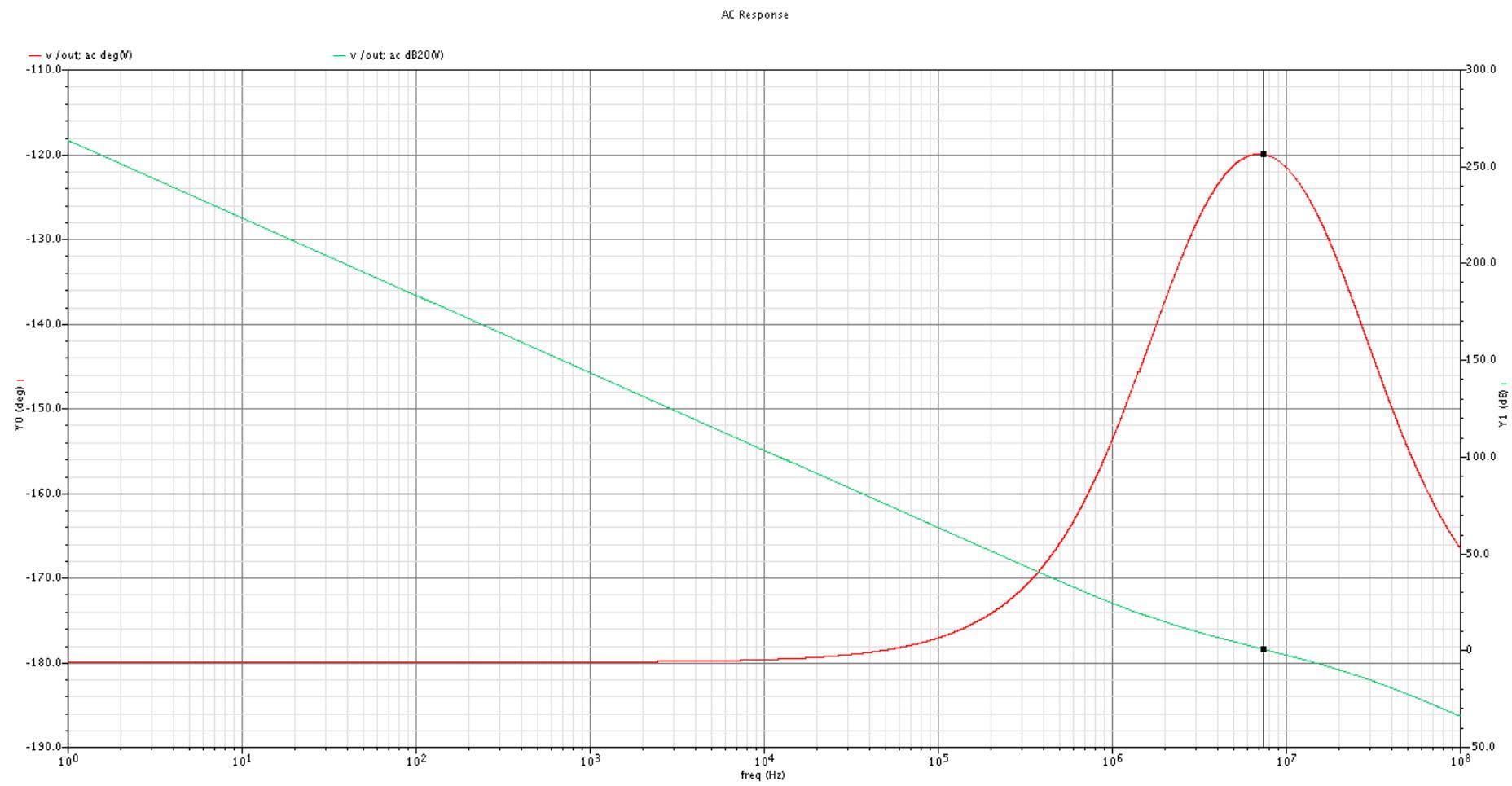
Simulations and Results

□ Closed Loop Transfer Function



Simulations and Results

□ Open Loop Transfer Function



Simulations and Results

Property	Value
C1	0.22pF
C2	2.85pF
R	29.78KΩ
Icp	150μA
Estimated rms Jitter*	47fs



Questions ?

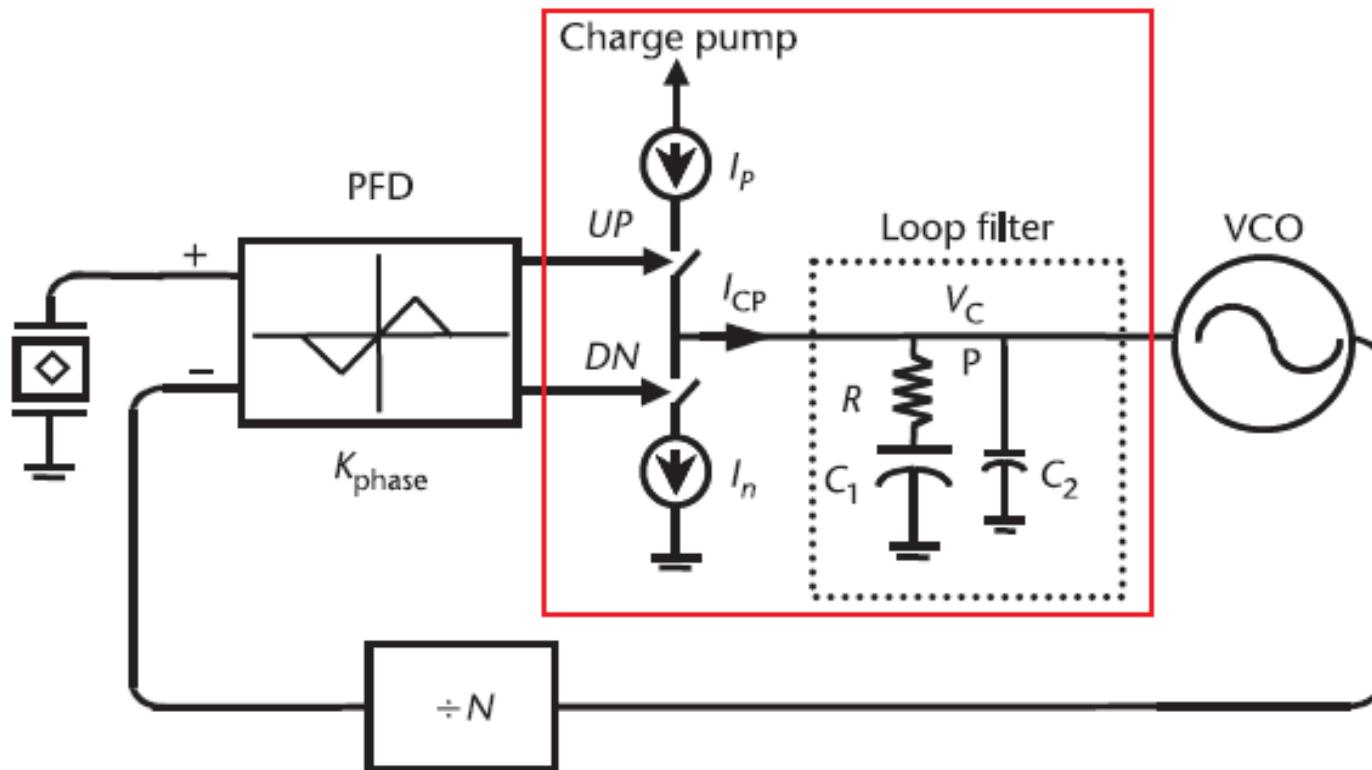
Charge Pump

Overview

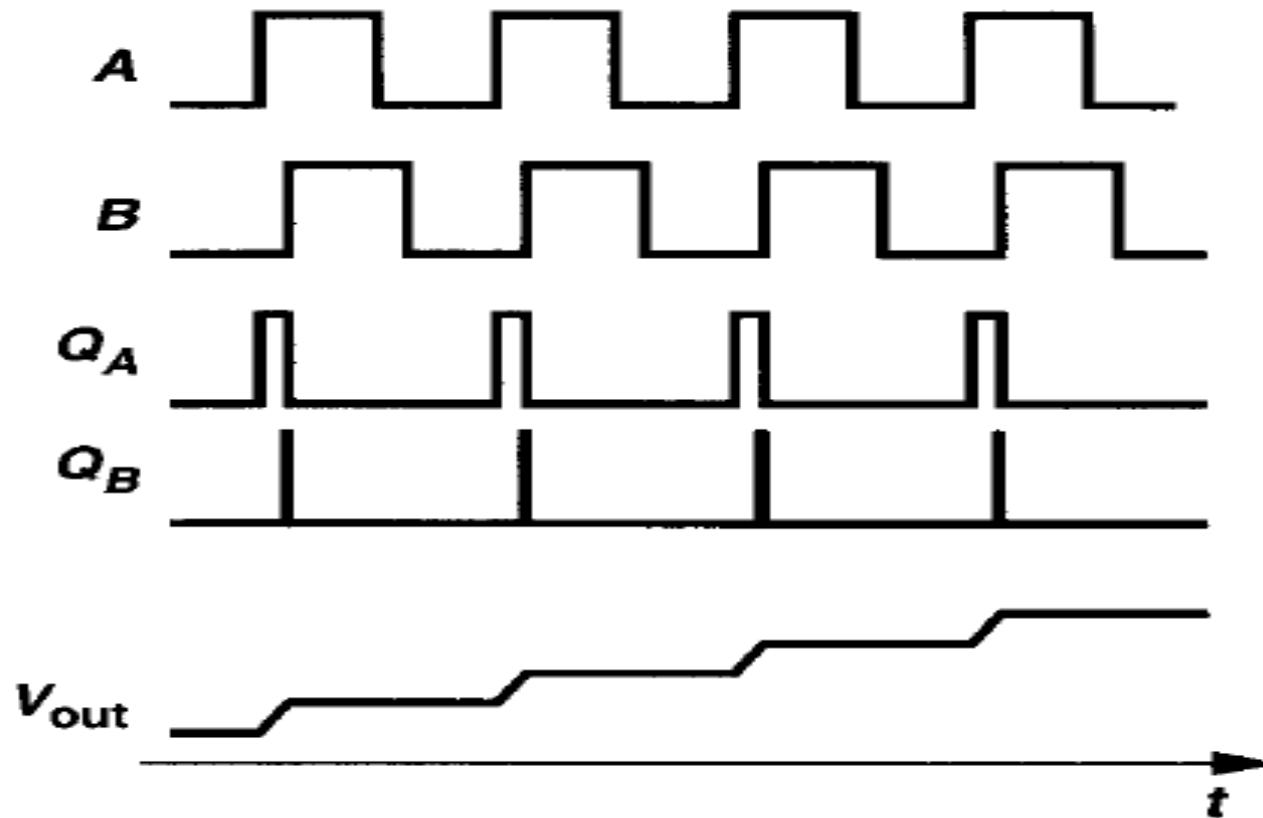
- Introduction
- Design Issues
- Different Topologies
- Phase Noise
- Corners Analysis

Introduction

□ UP & DOWN currents



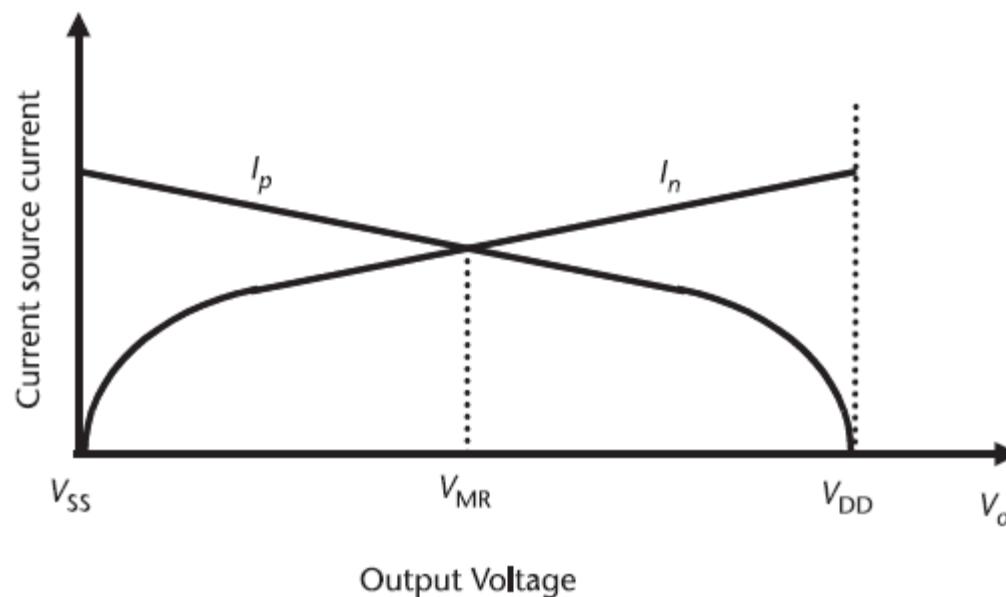
Introduction



Design Issues

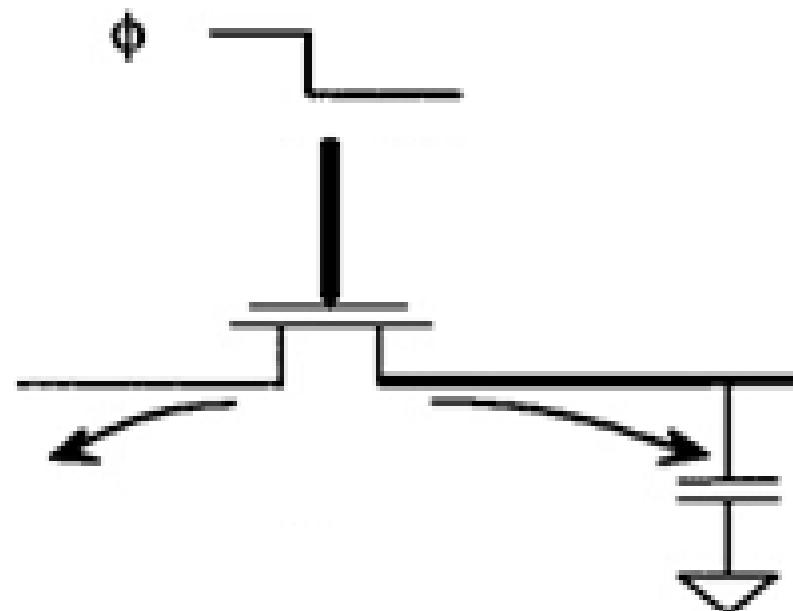
□ Current Mismatch

- $V_{DS,SAT}$
- Channel Length (L)



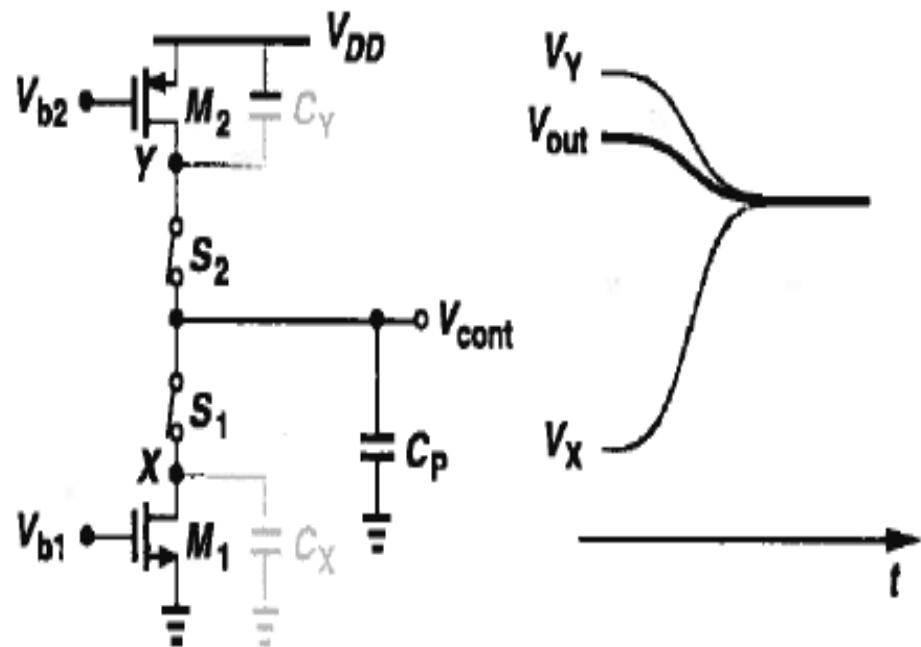
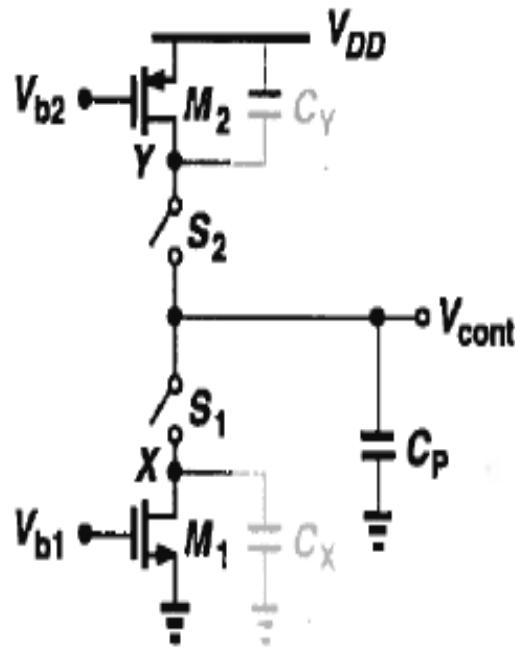
Design Issues

□ Charge Injection



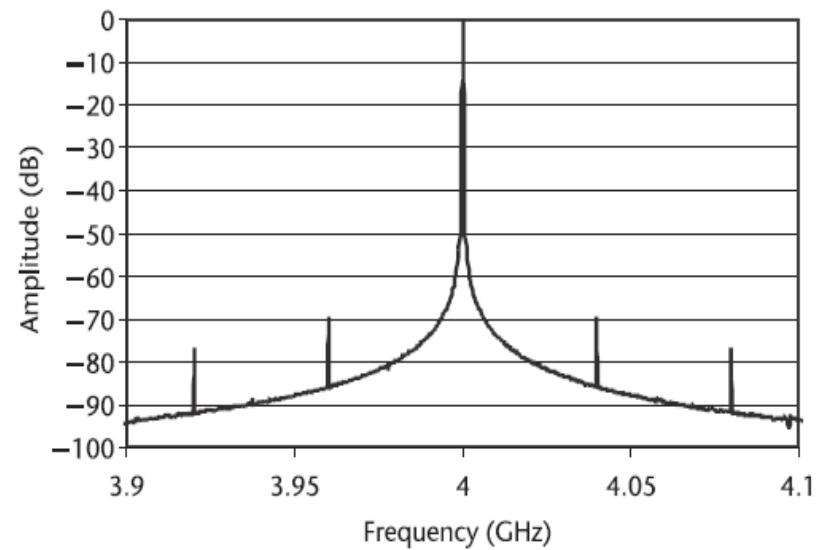
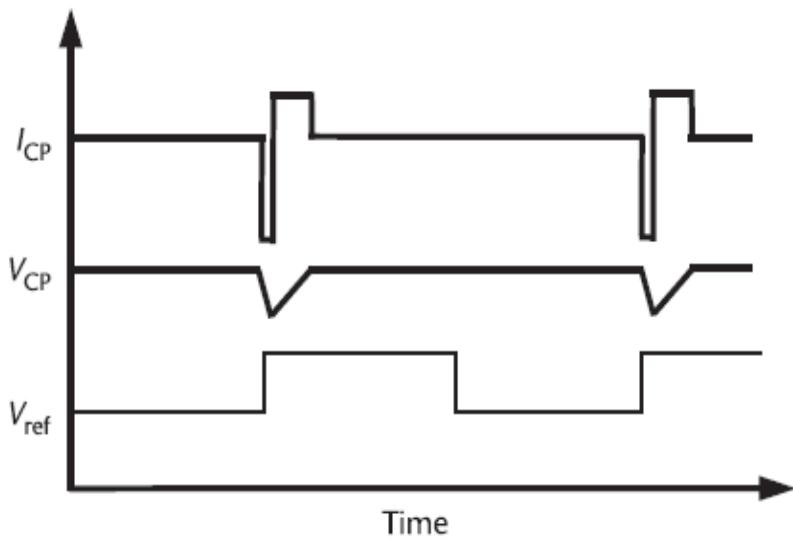
Design Issues

□ Charge Sharing

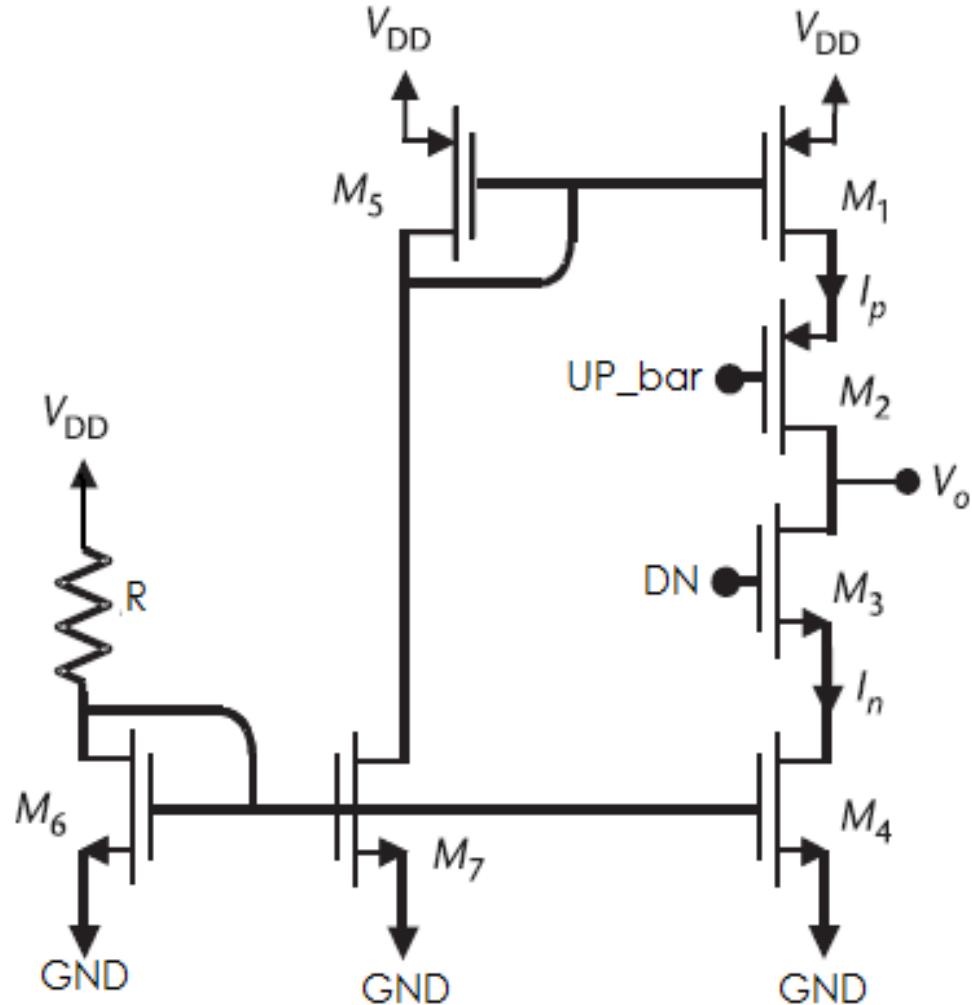


Design Issues

- Reference feed through
 - The reference feed through causes an AC signal on the control voltage at reference frequency.
 - Causes spurs in the output spectrum.



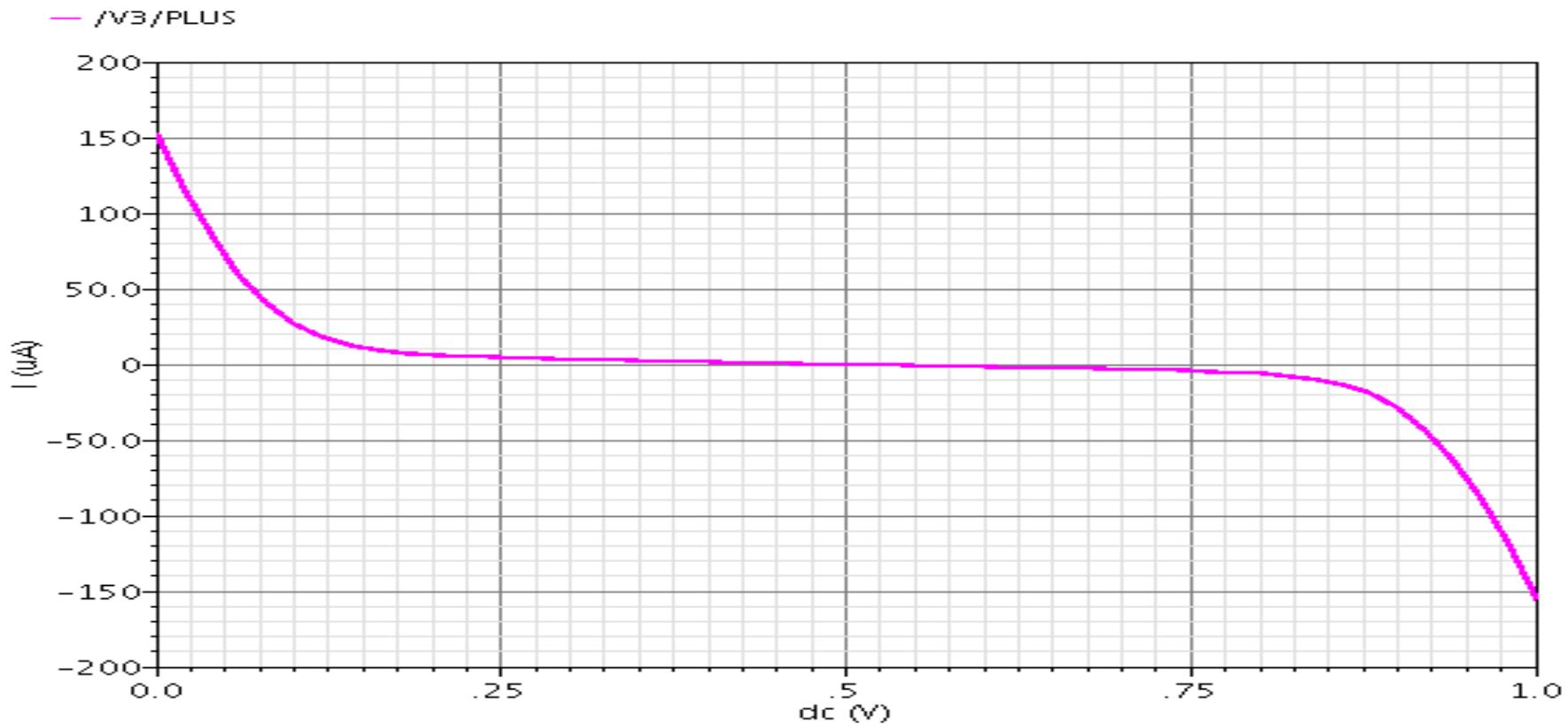
Topology 1



Topology 1

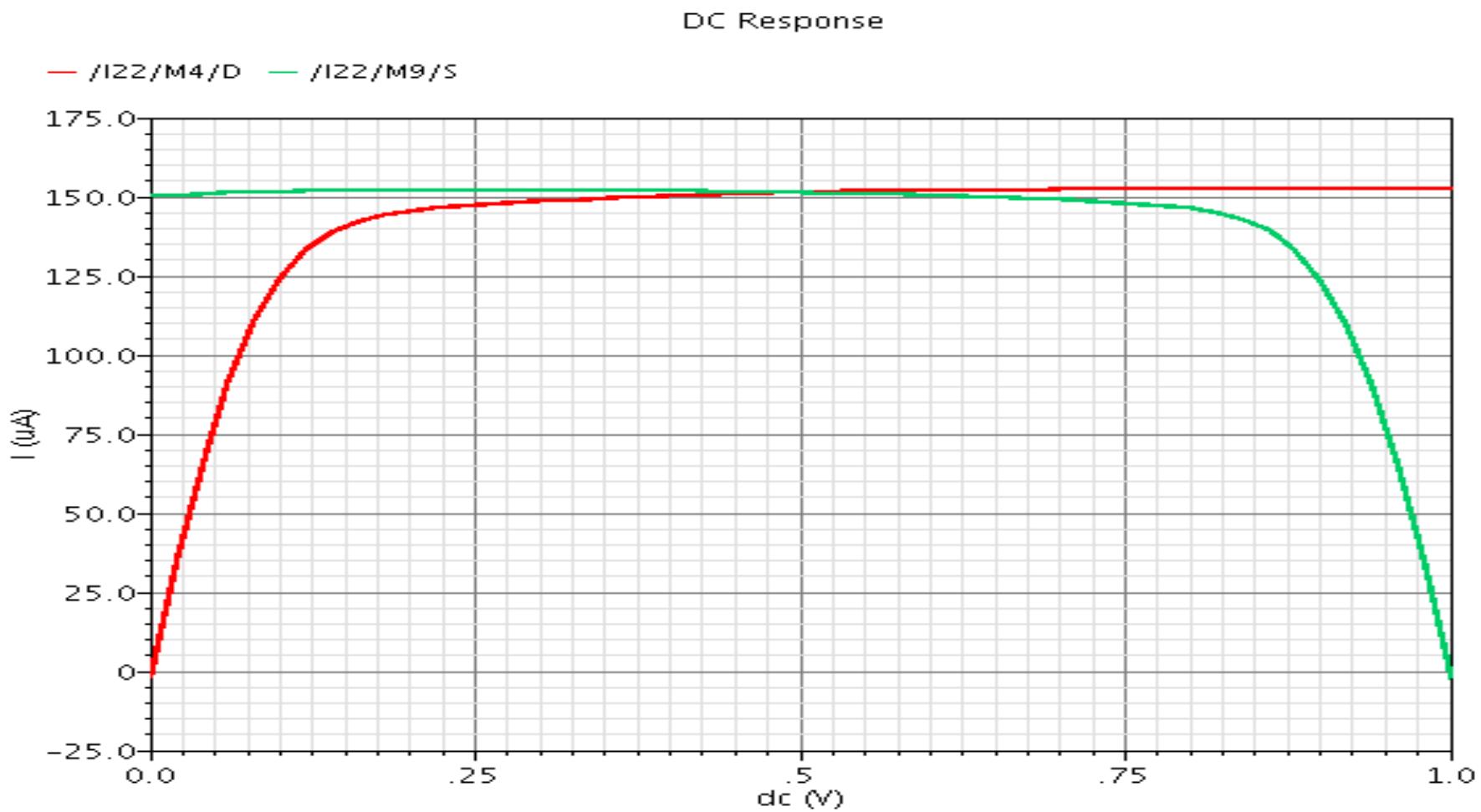
- Compliance Curve
 - 0.13v & 0.86v

DC Response



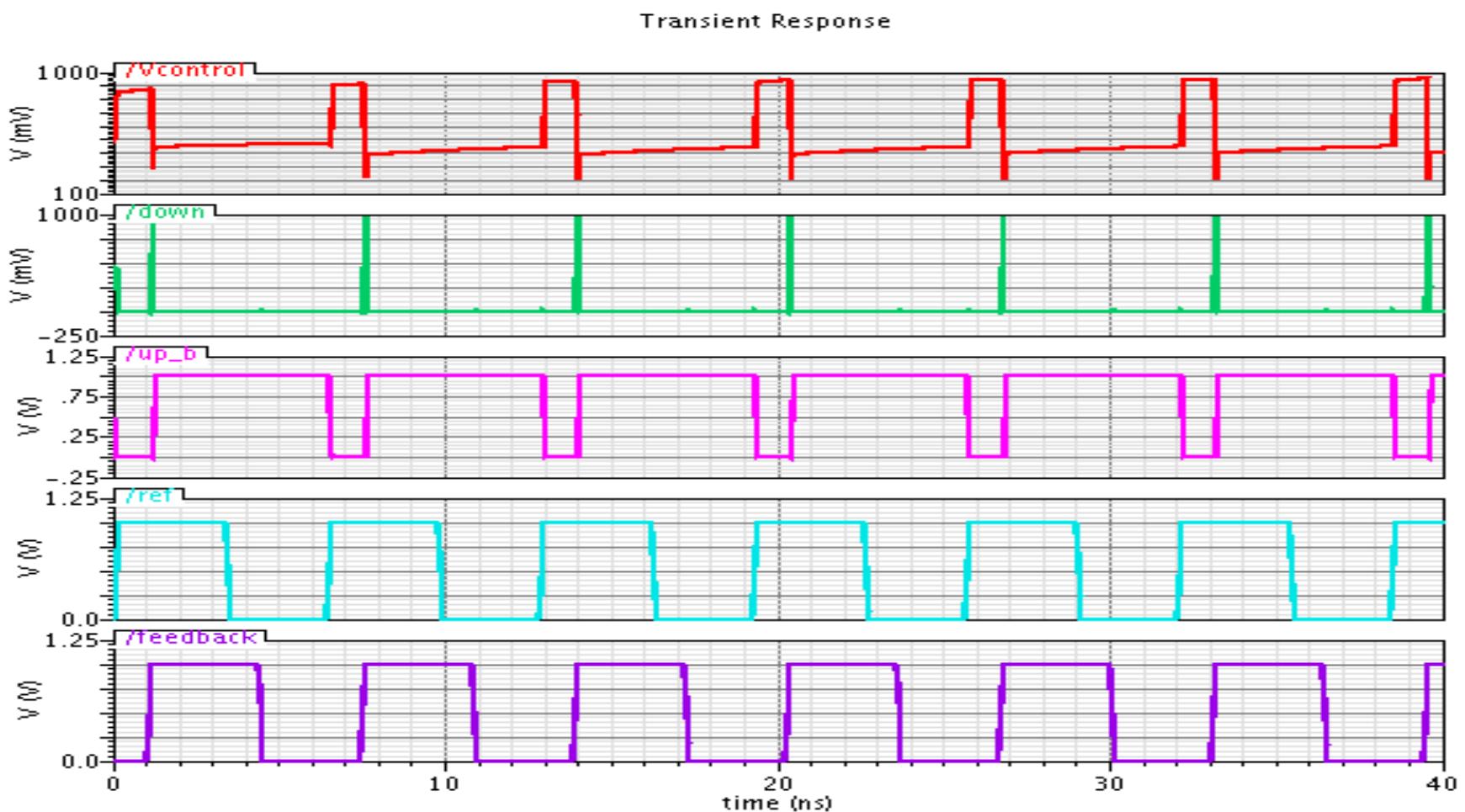
Topology 1

IDS Vs VDS



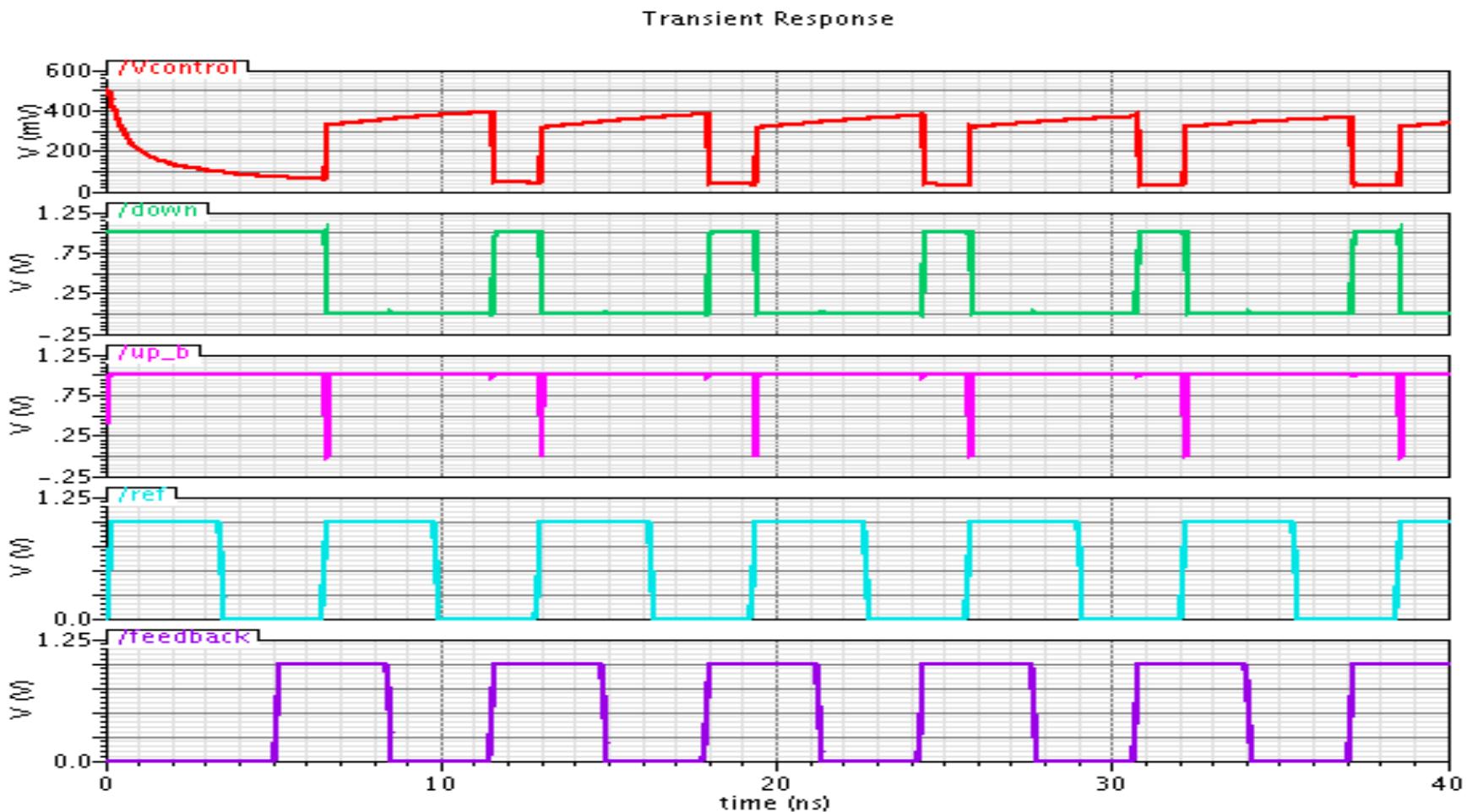
Topology 1

□ Transient Analysis (UP)

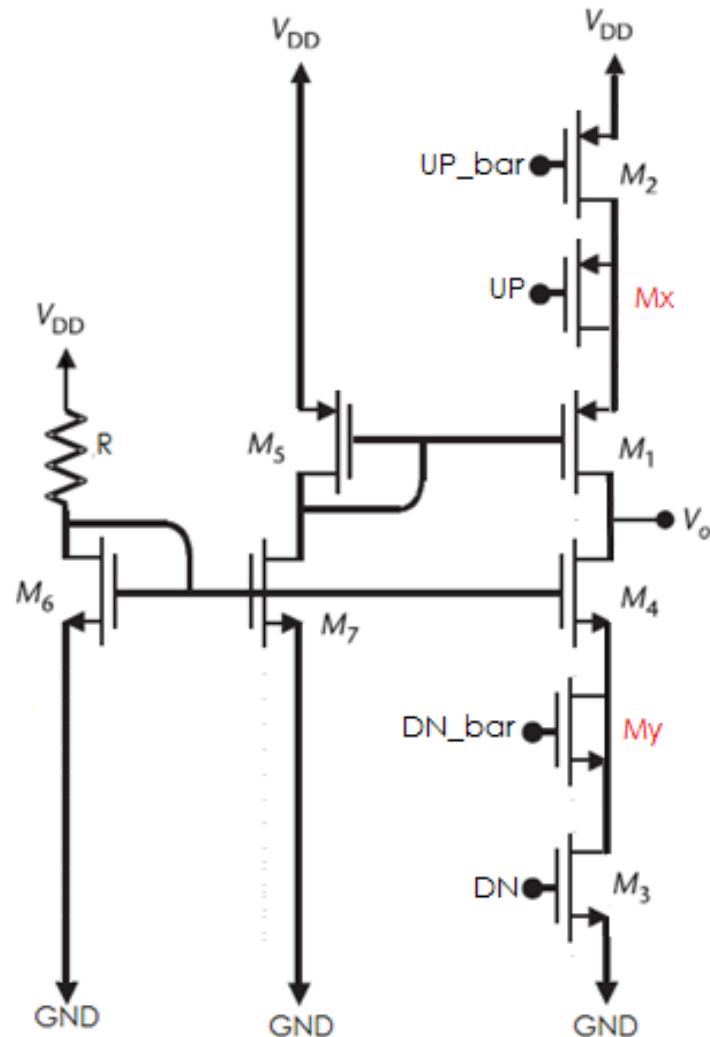


Topology 1

□ Transient Analysis (DOWN)

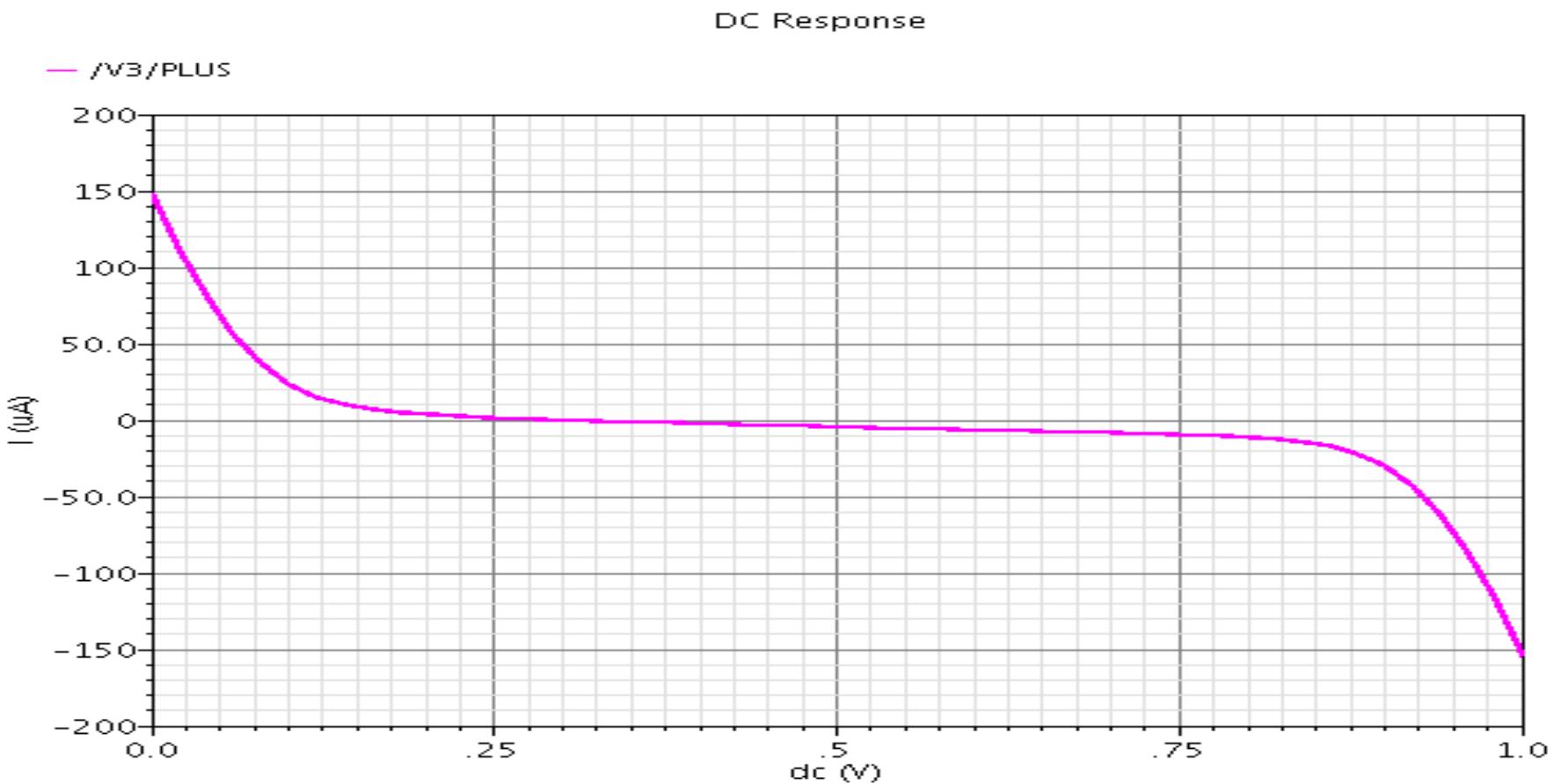


Topology 2



Topology 2

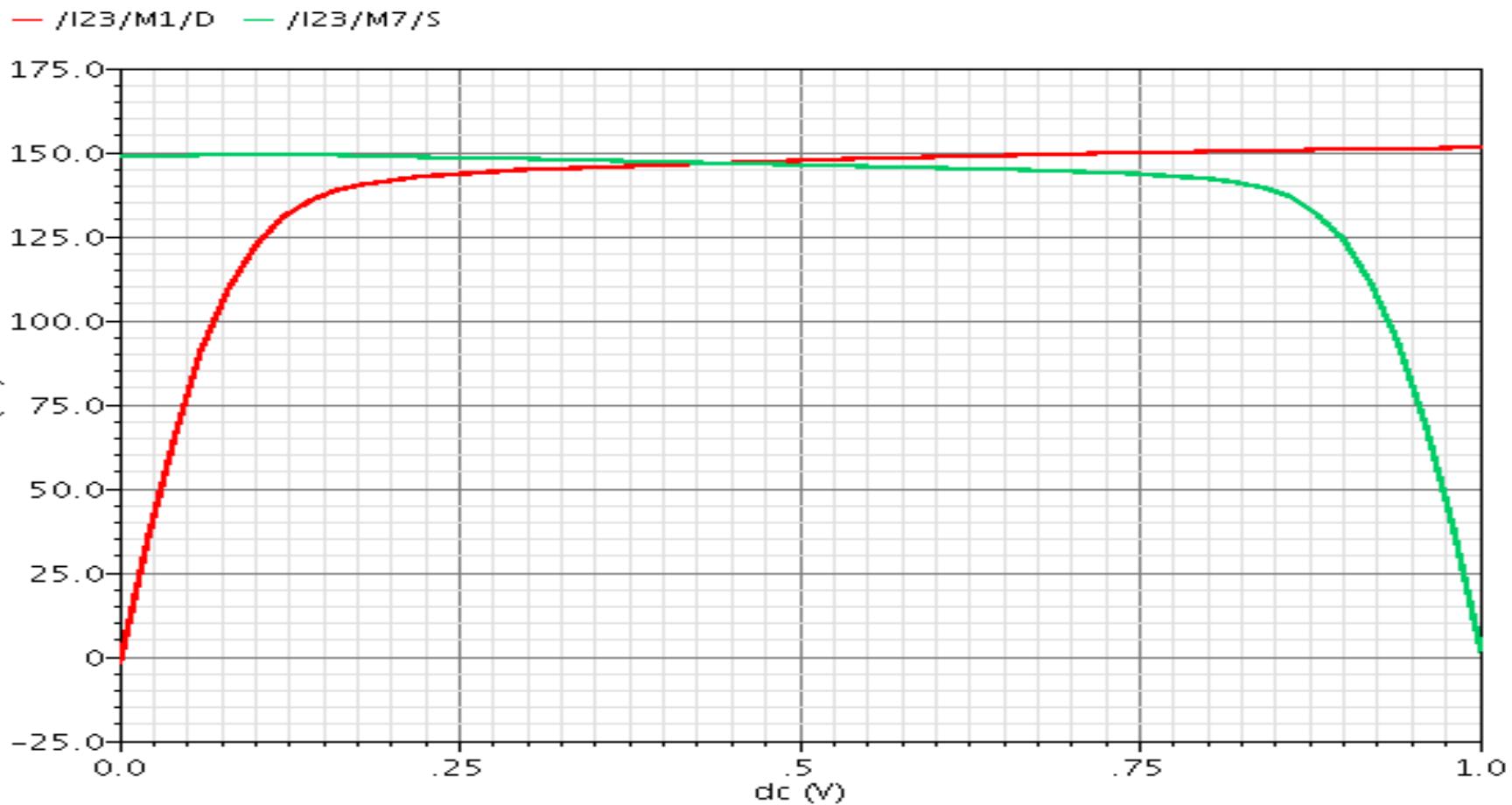
- Compliance Curve
 - 0.12v & 0.85v



Topology 2

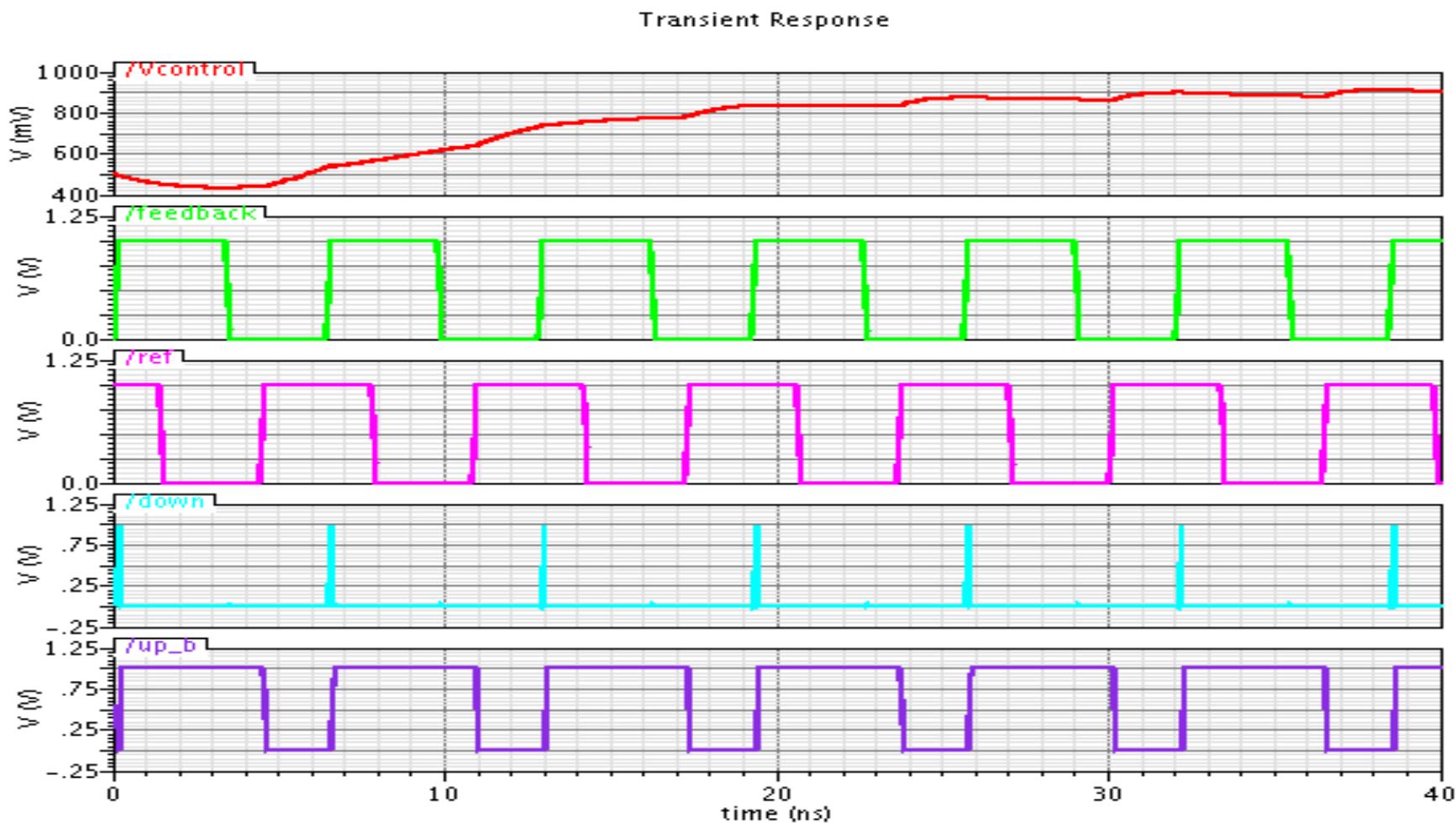
IDS Vs VDS

DC Response



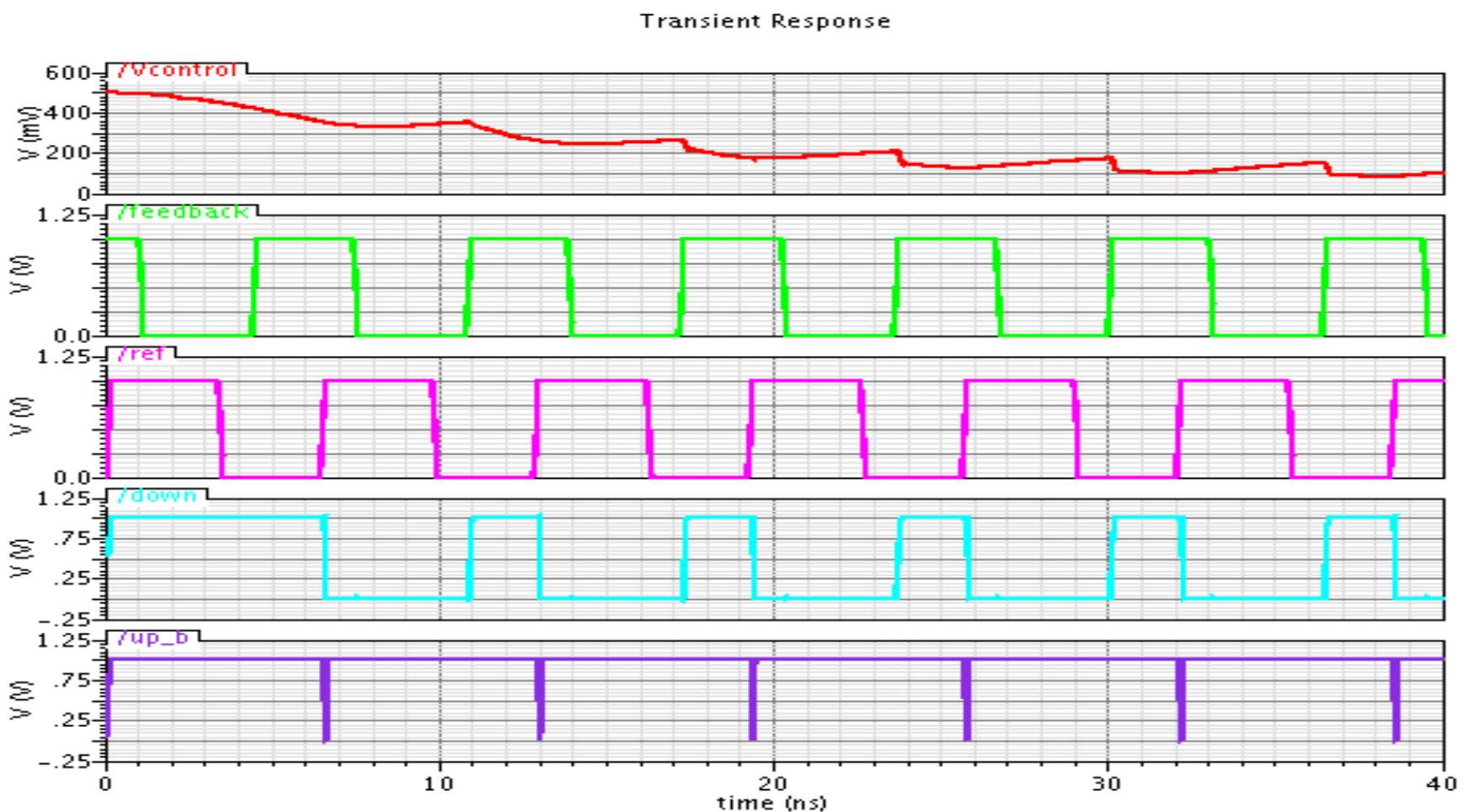
Topology 2

□ Transient Analysis (UP)

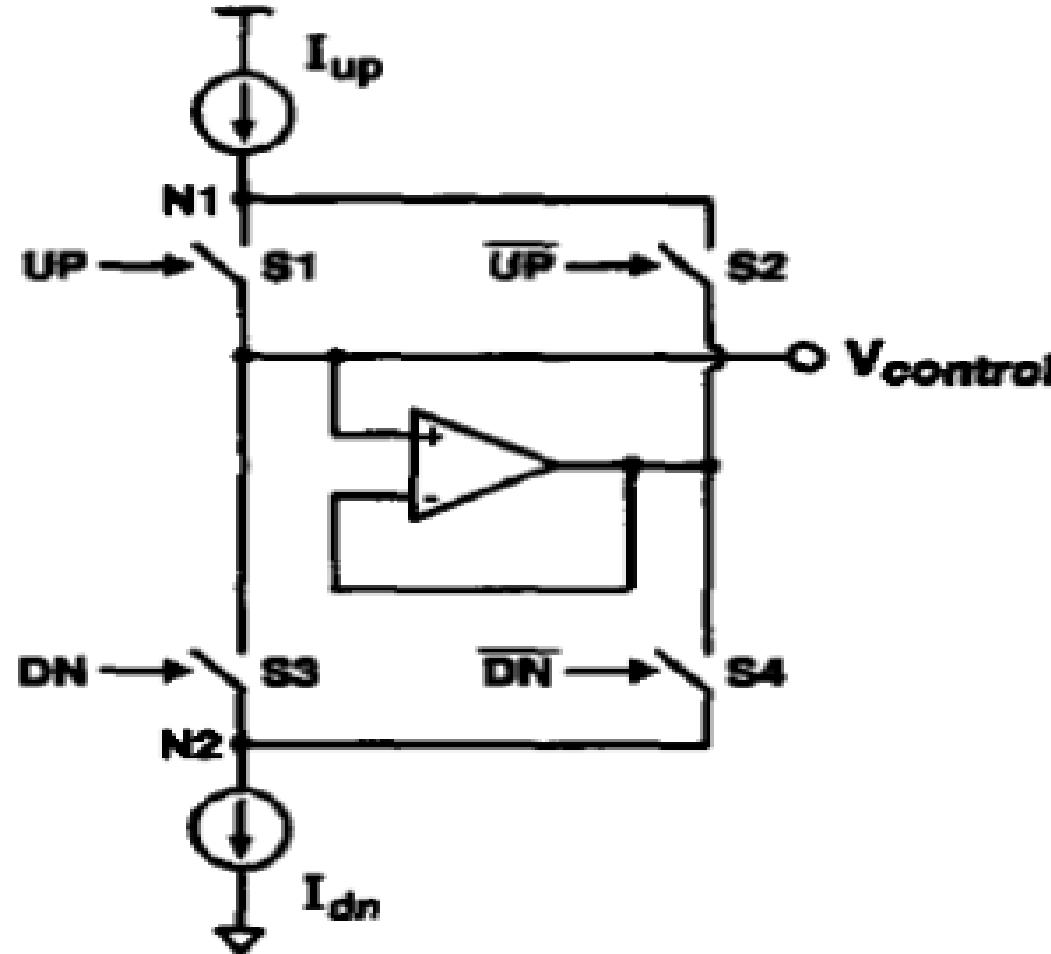


Topology 2

□ Transient Analysis (DOWN)



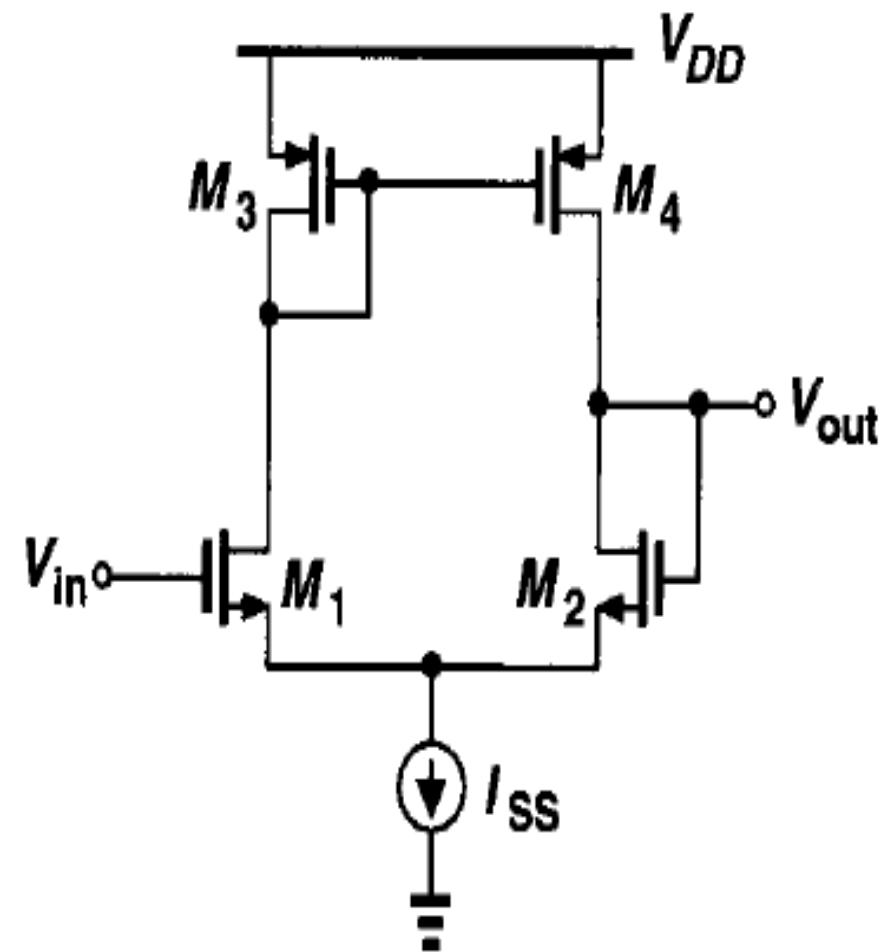
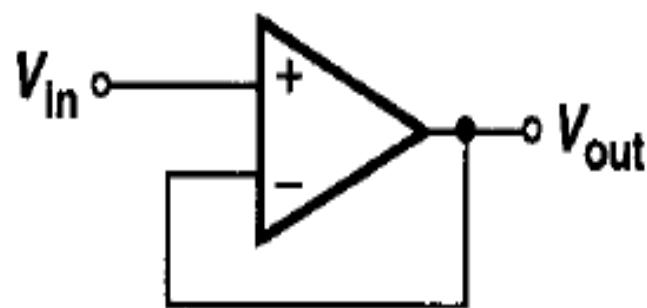
Topology 3



[Young JSSC 1992]

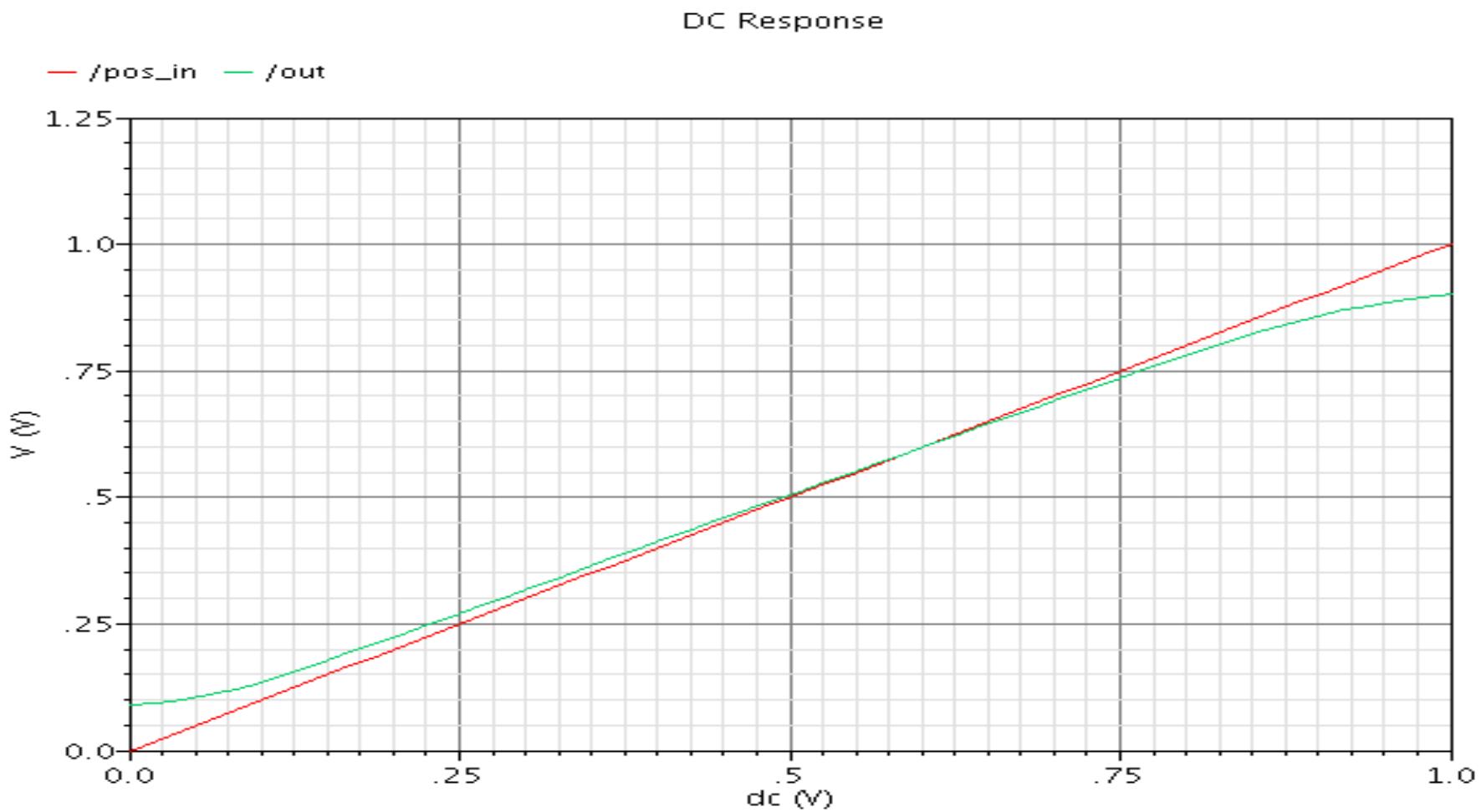
Topology 3

□ Unity Gain Buffer



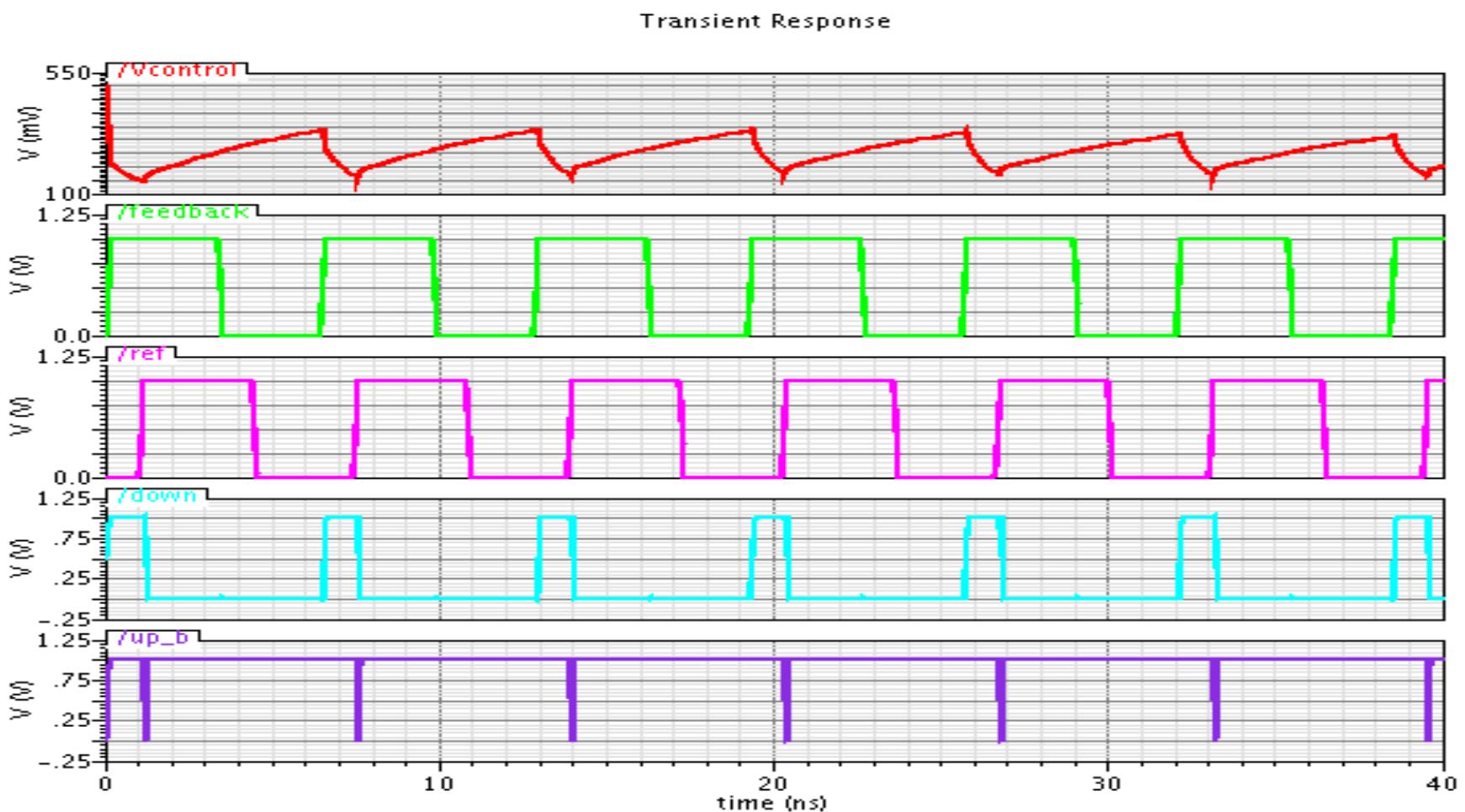
Topology 3

□ Unity Gain Buffer



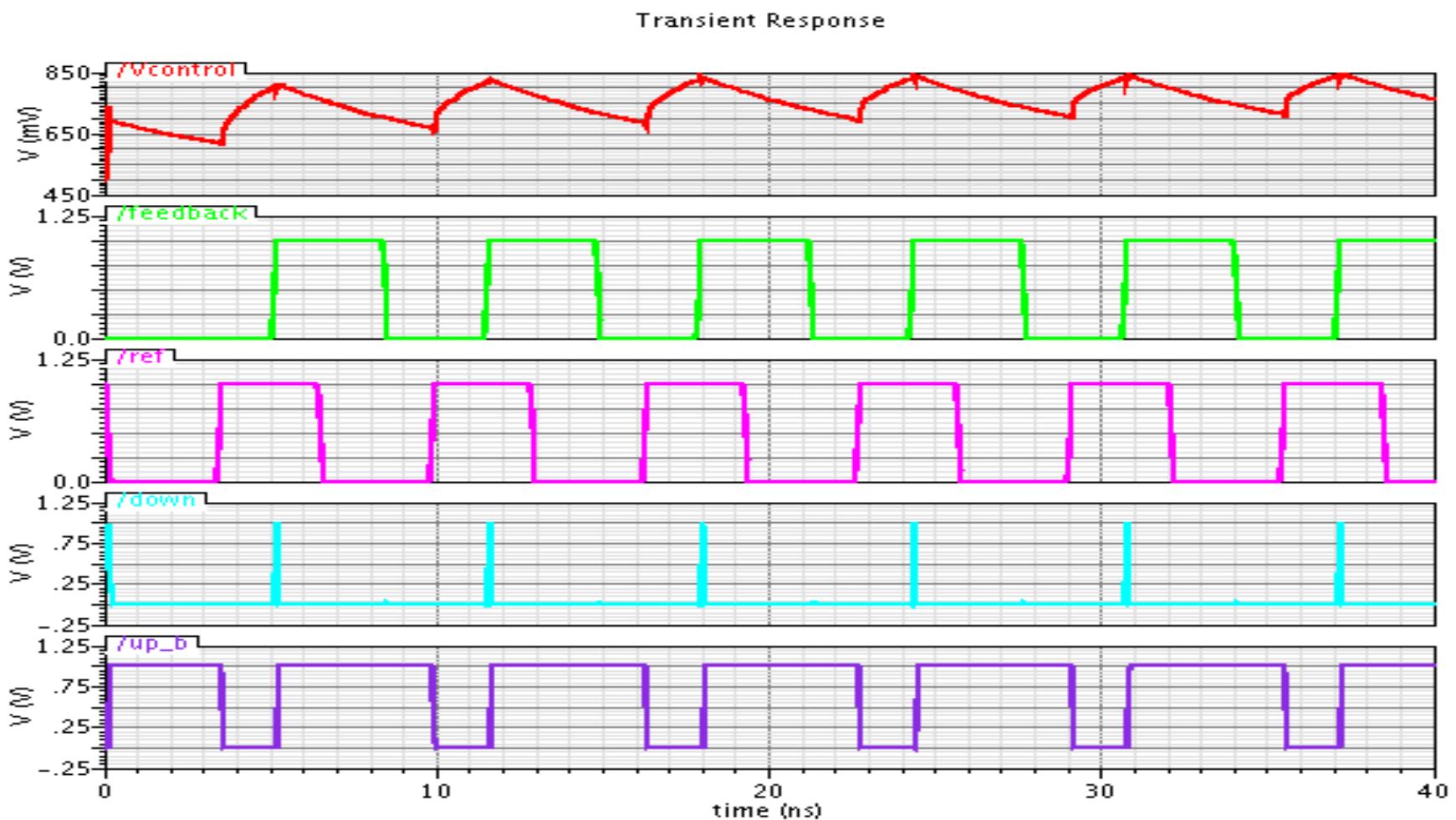
Topology 3

□ Transient Analysis (UP)



Topology 3

□ Transient Analysis (DOWN)



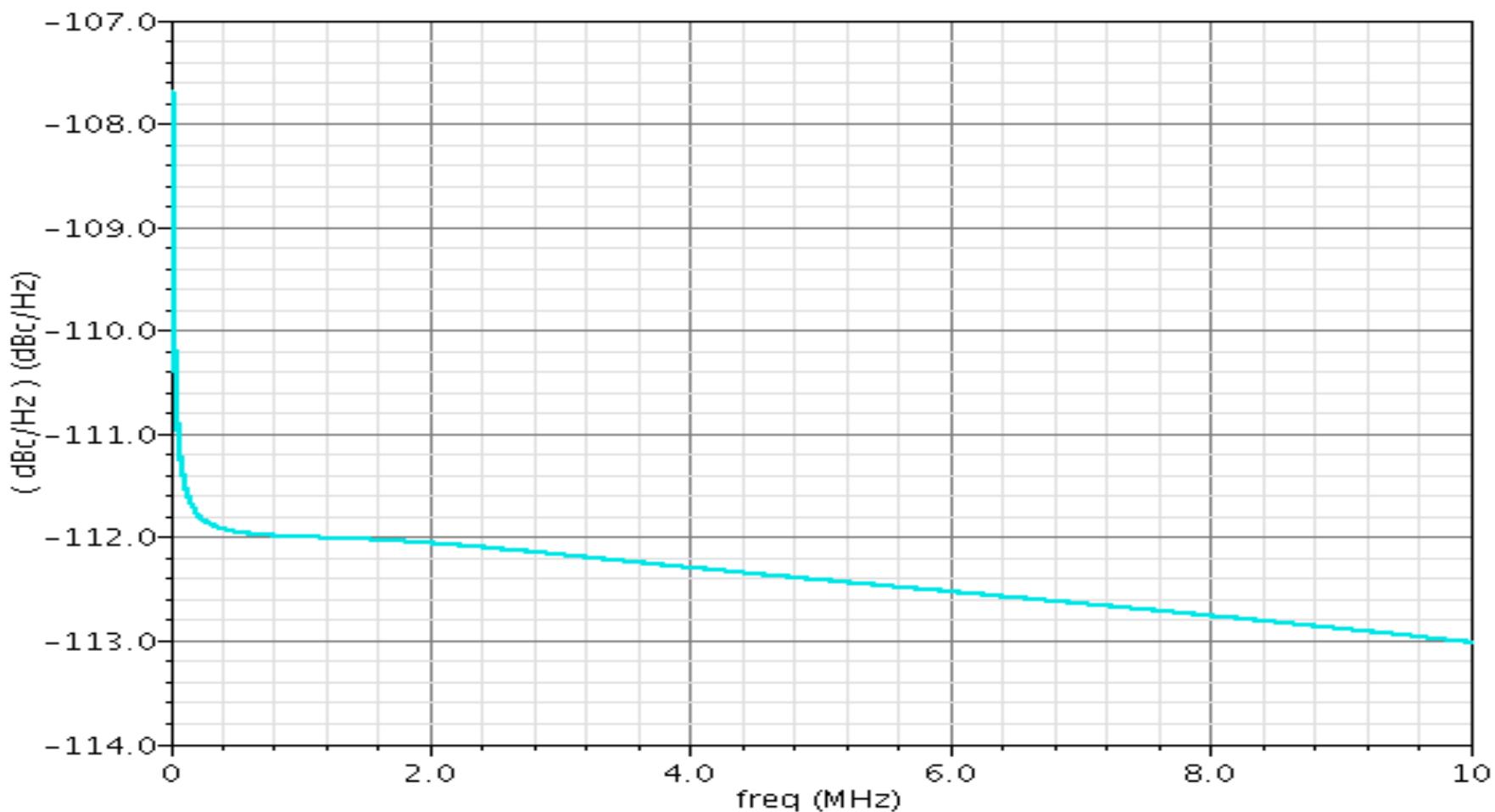
Topology Chosen

- Topology 2 was used because of:
 - Reduced charge sharing
 - Reduced charge injection
 - Least power (198.42 μW)

Phase Noise

Periodic Noise Response

— Phase Noise; dBc/Hz



Corners Analysis

- Compliance curve
 - 0.2v & 0.75v
- Phase Noise (at 10M)
 - -111dBc/Hz & -125 dBc/Hz



Questions ?

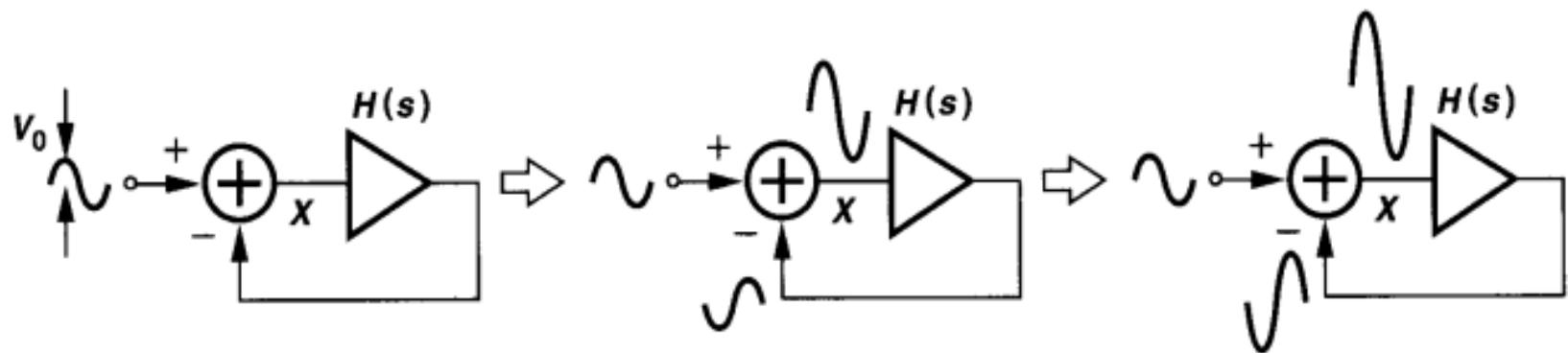
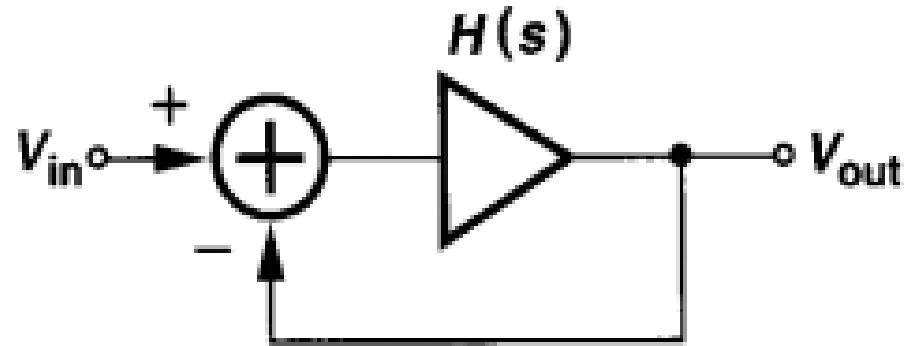
VOLTAGE Controlled oscillator (VCO)

Overview

- VCO basics
- Different Topologies
- LC VCO
 - Why LC ?
 - -GM vs Colpitts
 - -GM oscillator
 - CMOS vs NMOS and PMOS
- Simulation and results

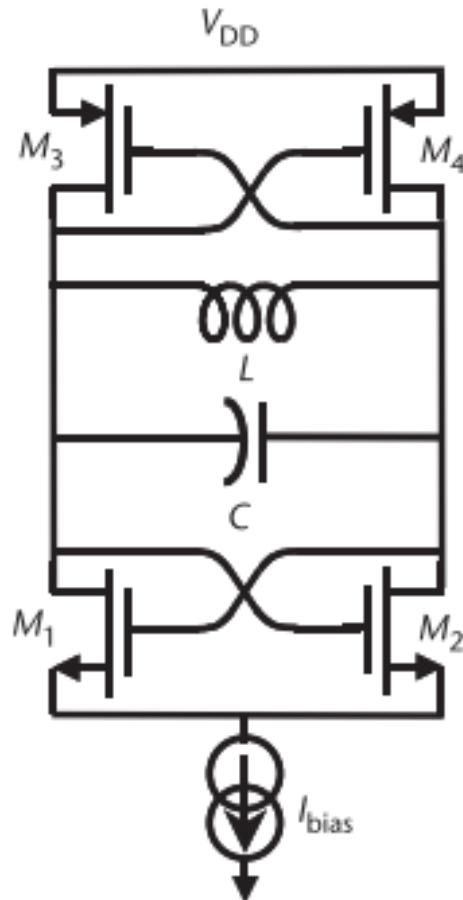
VCO Basics

- VCO is a feedback system.
- Positive feedback
- Barkhausen criterion

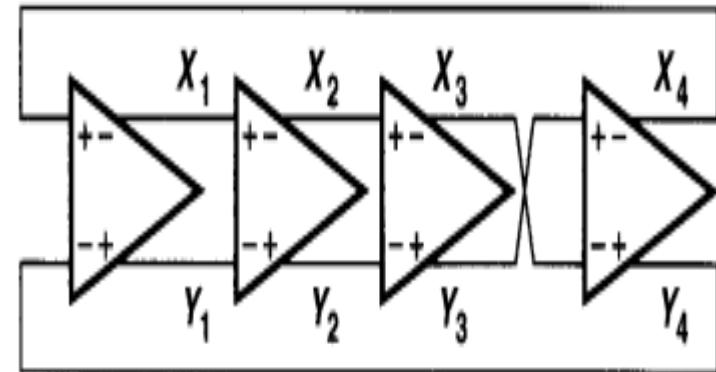


Different topologies

□ LC VCO



□ Ring VCO



Different topologies

	Ring Oscillator	LC Oscillator
Passive Devices	No Passive devices so it's easier to implement	Spiral inductors and varactors
Area	Smaller area	Larger area
Tuning Range	Large tuning range	Smaller tuning range
Frequency	High frequency	Much higher frequencies
Phase noise	Poor phase noise performance	Better phase noise performance
Power Consumption	Higher power consumption	Lower power consumption

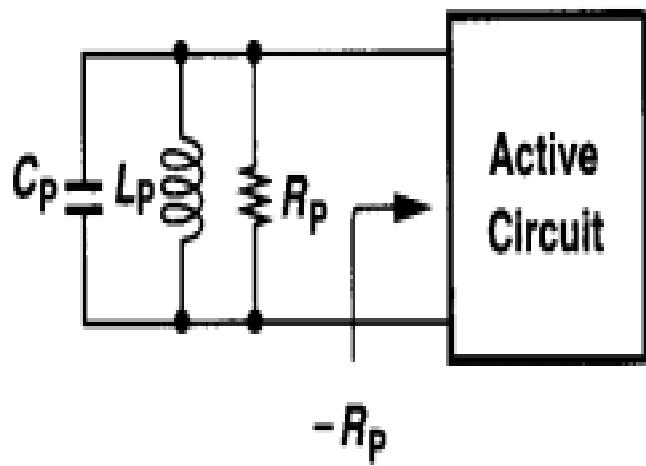
LC VCO

□ Why LC ?

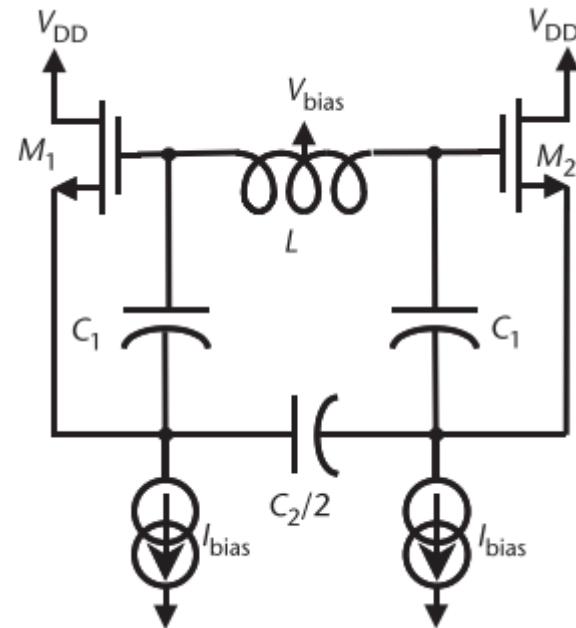
Since the required output jitter from the PLL is 1 ps rms, we have chosen to work with the LC VCO in order to achieve the lowest possible phase noise from the oscillator.

-GM oscillator vs Colpitts

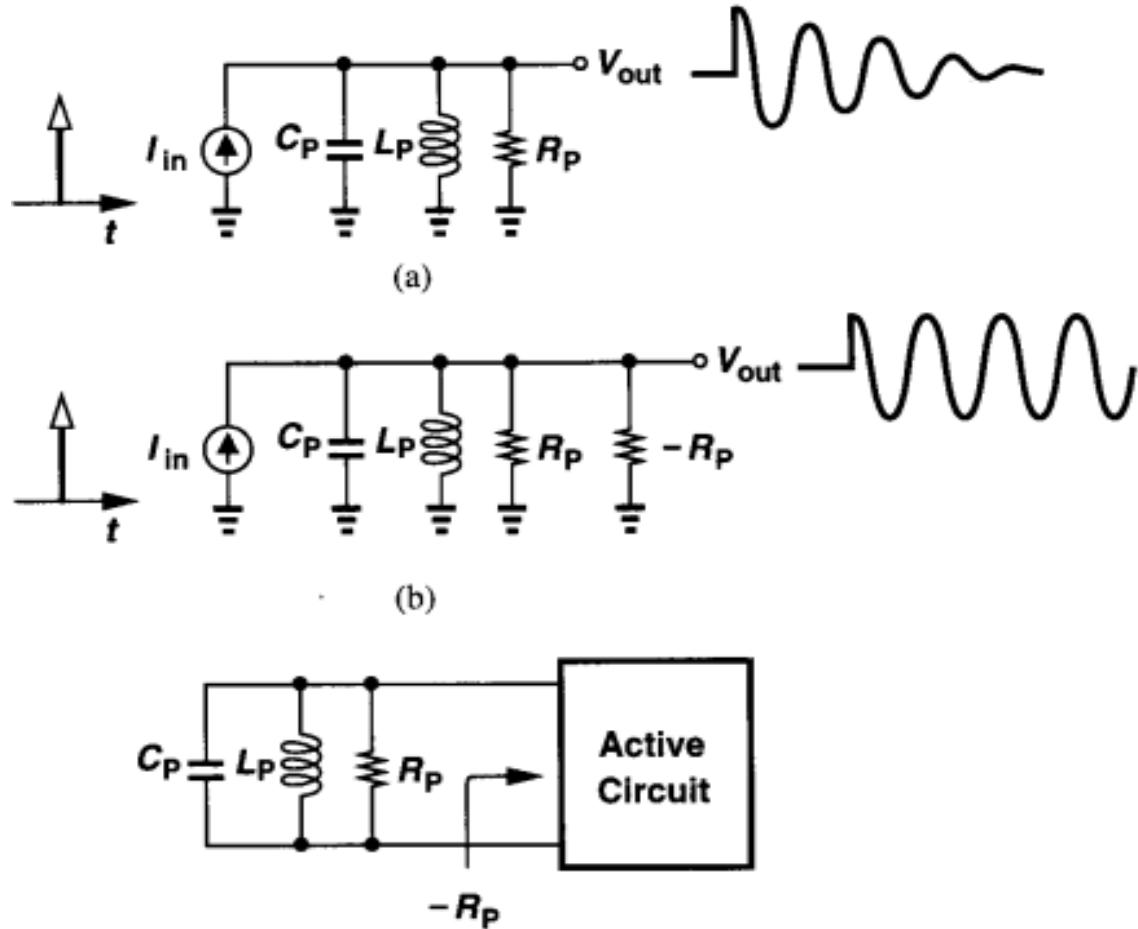
-GM VCO



Colpitts VCO

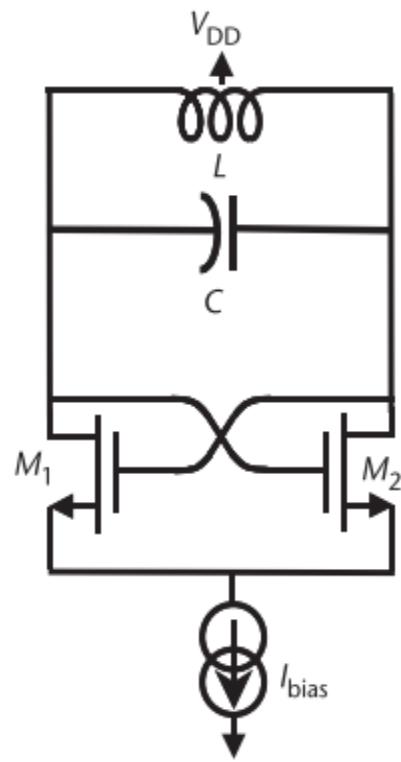


-GM oscillator

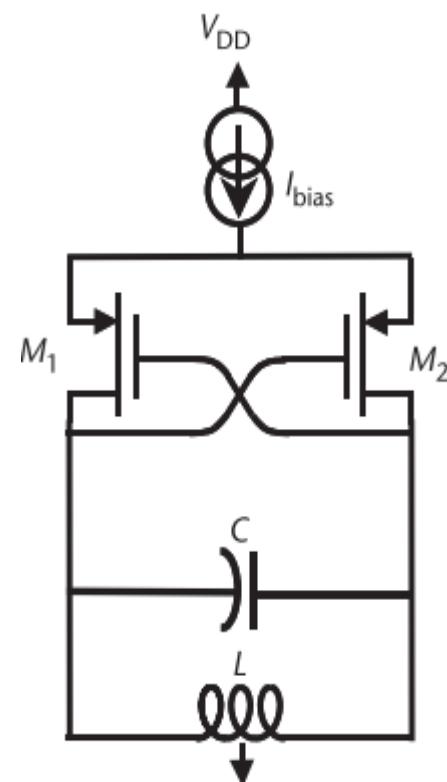


CMOS vs NMOS & PMOS

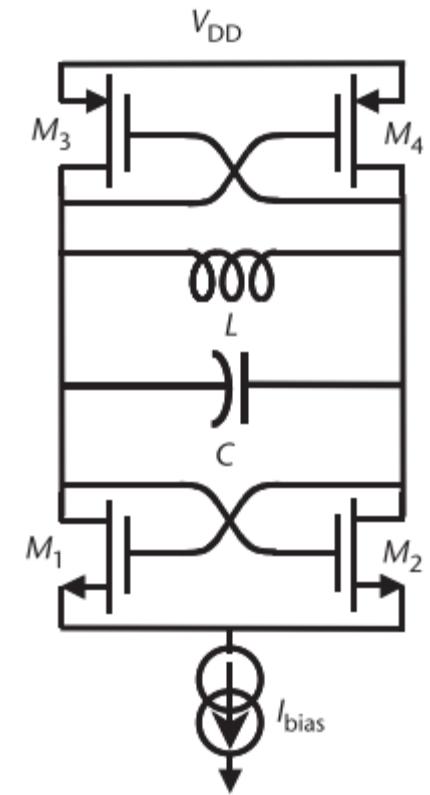
NMOS



PMOS

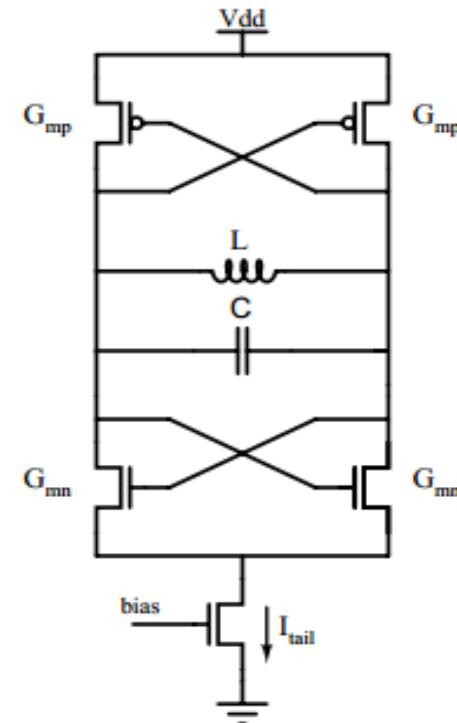
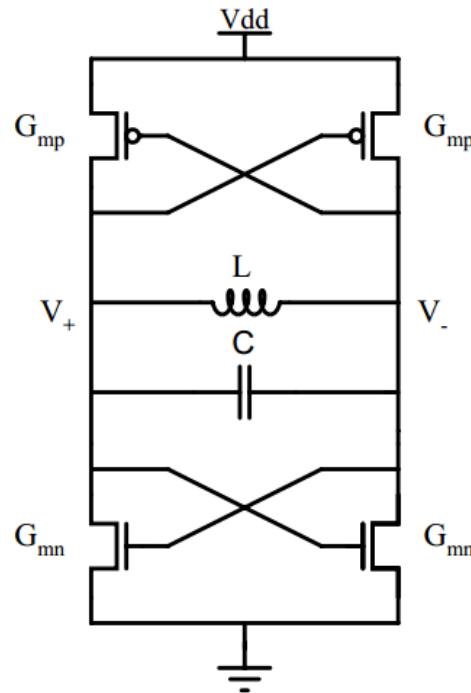


CMOS

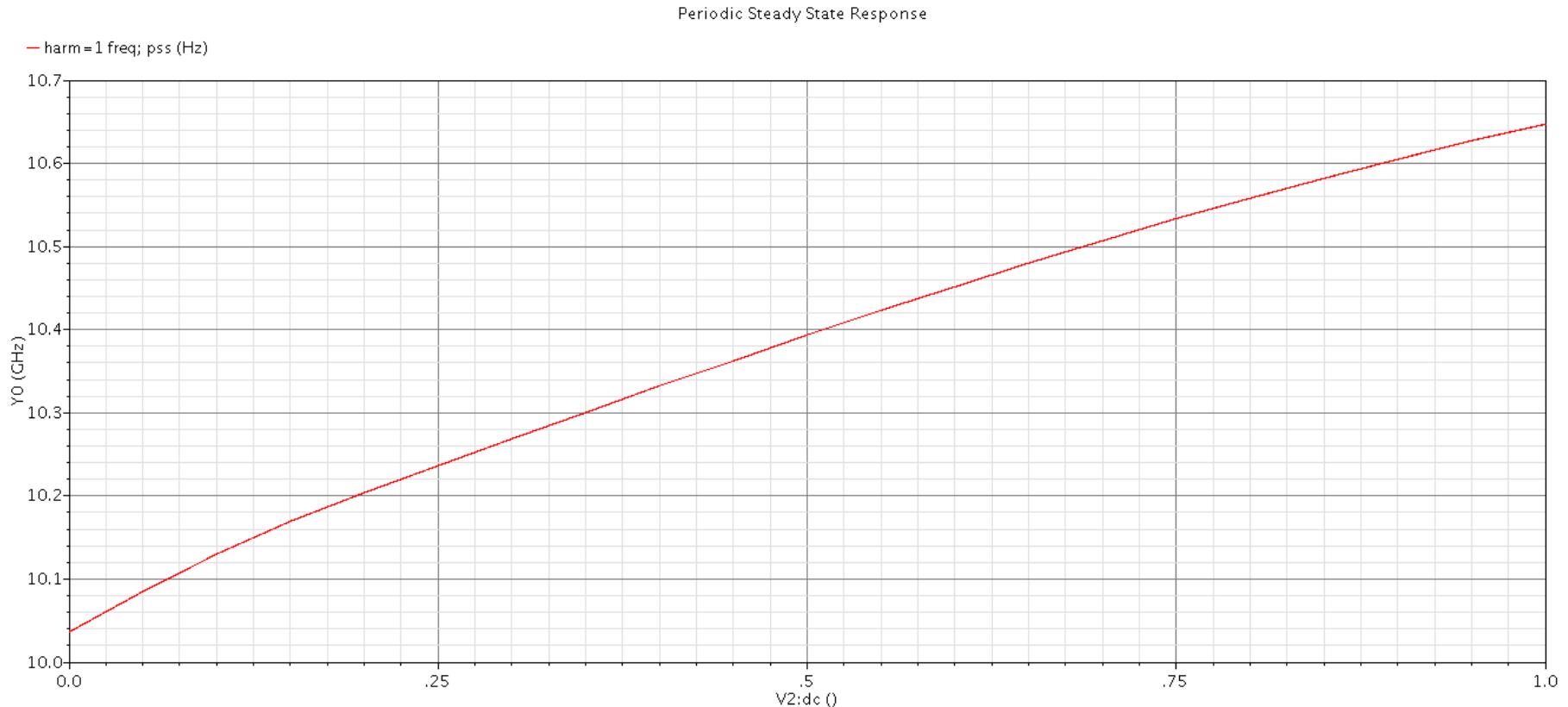


Current tail problem

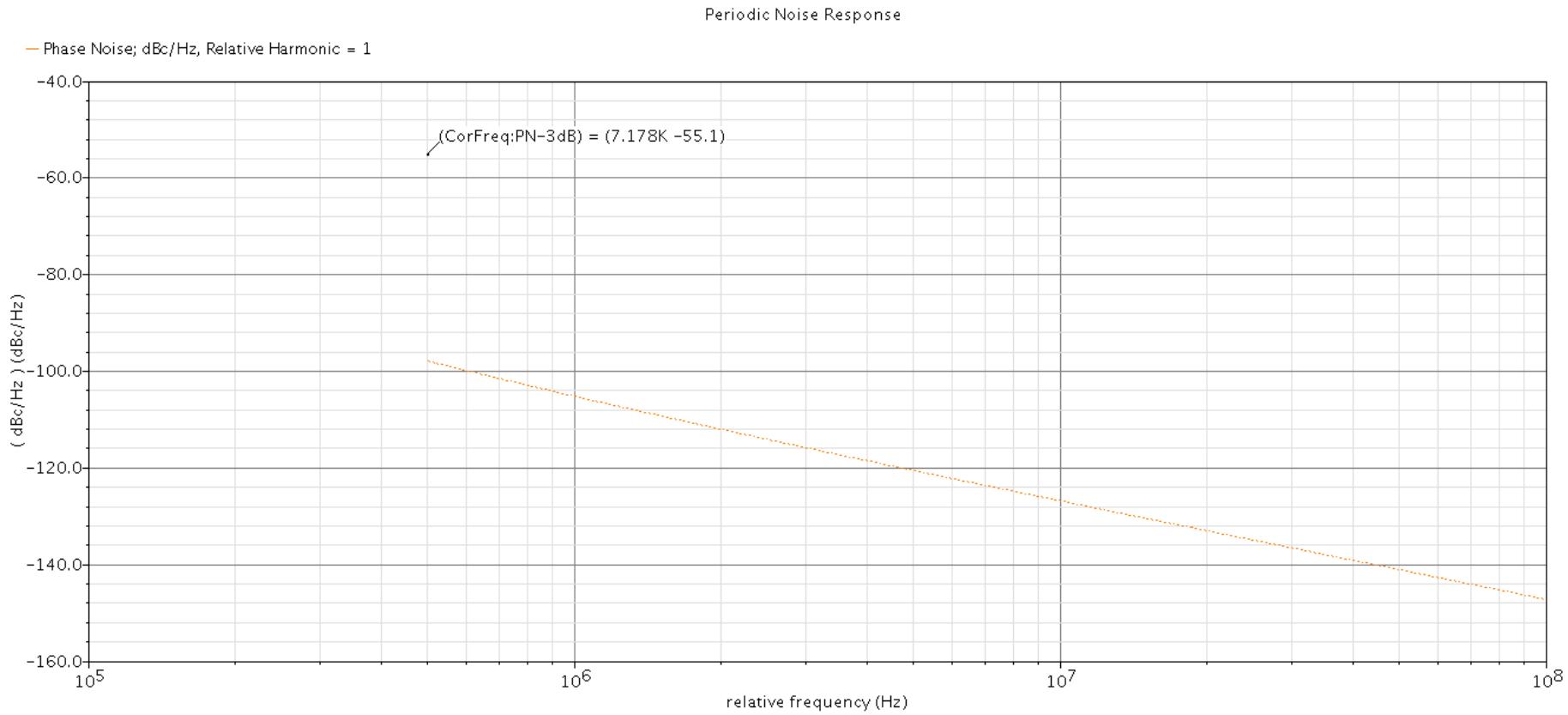
- Noise report indicated 20% of noise is from current source.
- On removing current source Phase noise is improved significantly.



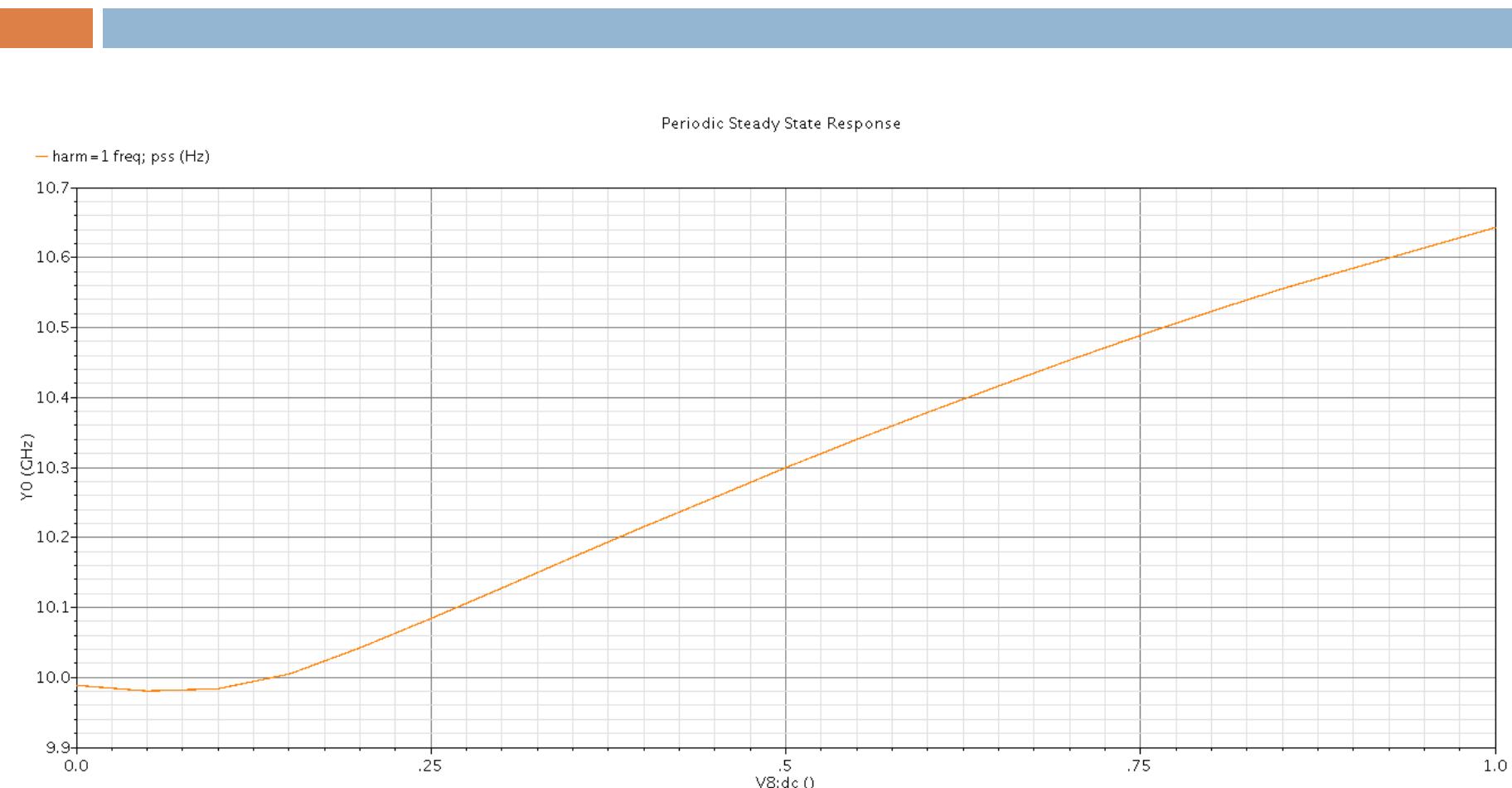
Performance with current source



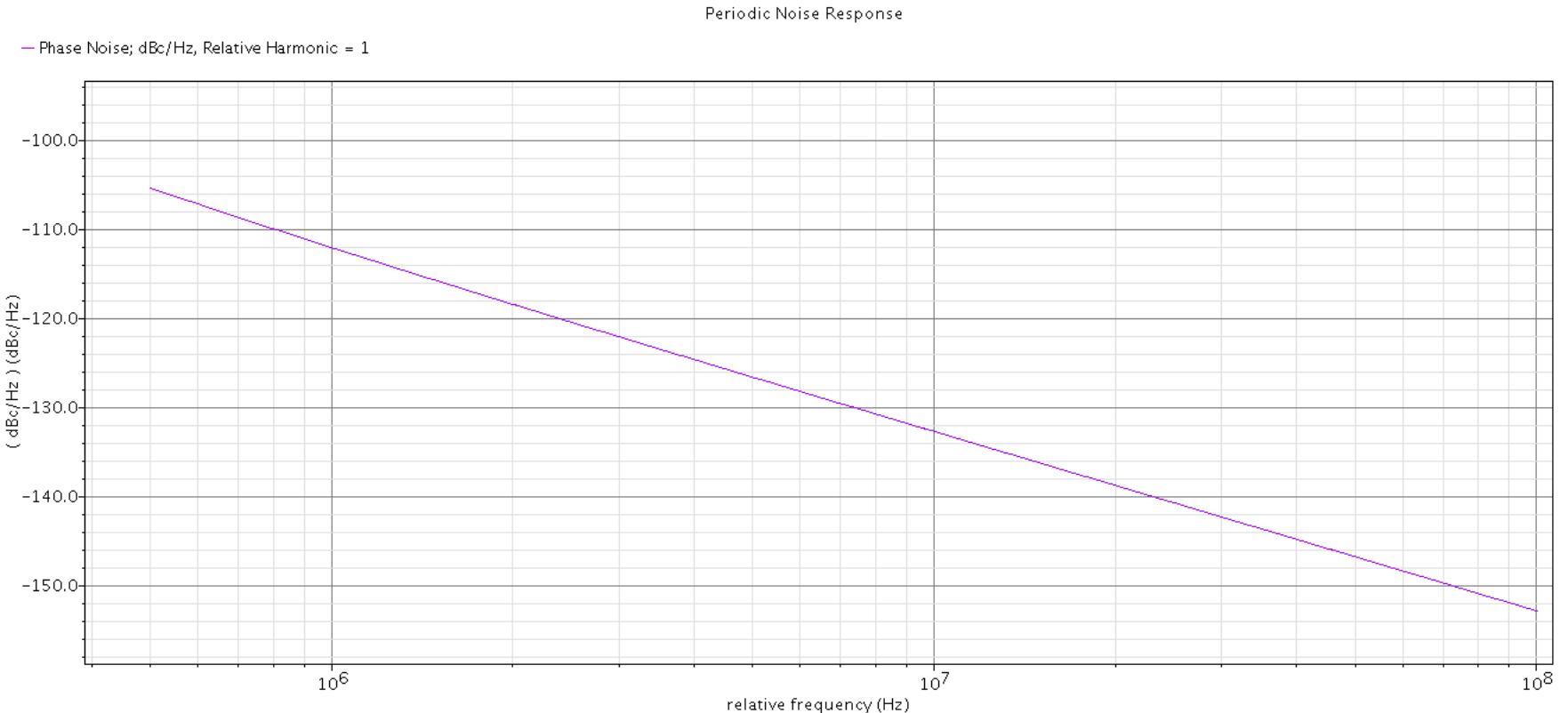
Performance with current source



Without current source



Without current source



Comparison

	Without Current tail	With Current tail
Power consumption	3.7mW	3.09mW
Kvco	800MHz/V	550MHz/V
Phase noise at 1MHz	-112dBc/Hz	-105.2dBc/Hz
Figure Of Merit	186.3dBc/Hz	180.3dBc/Hz

$$\text{Figure Of Merit} = 10 \log \left\{ \left(f_0 / \Delta f \right)^2 / L \{ \Delta f \} \cdot P \right\}$$

Corners Results

- Across different corners, phase noise has not exceeded -110dBc/Hz
- Locking frequency is within the range of 0.25-0.85V

Area and power

NMOS	105µm / 360nm				
PMOS	105µm/300nm				
Capacitance range	1.23pF – 1.5pF				
Inductance	Width = 9µm	R = 40µm	Turn s = 1	L = 186. 5pH	Q Fact or = 20.6
	Area width = 153µm		Area length = 147.5µm		



Questions ?

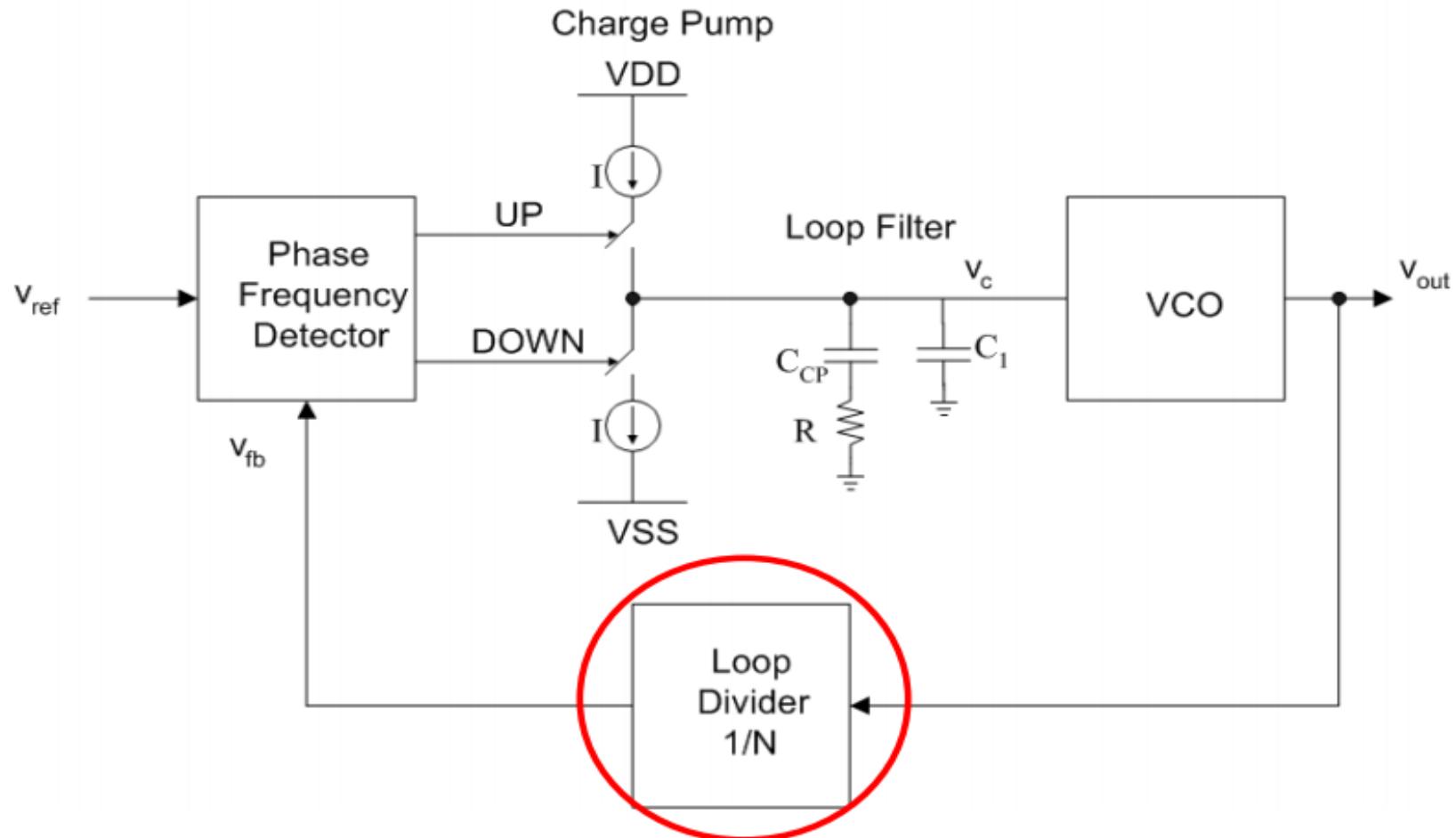


Divider

Overview

- Introduction
- Proposed Divider
 - Divide by 2
 - Divide by 3
 - Divide by 11
- Simulations and Results

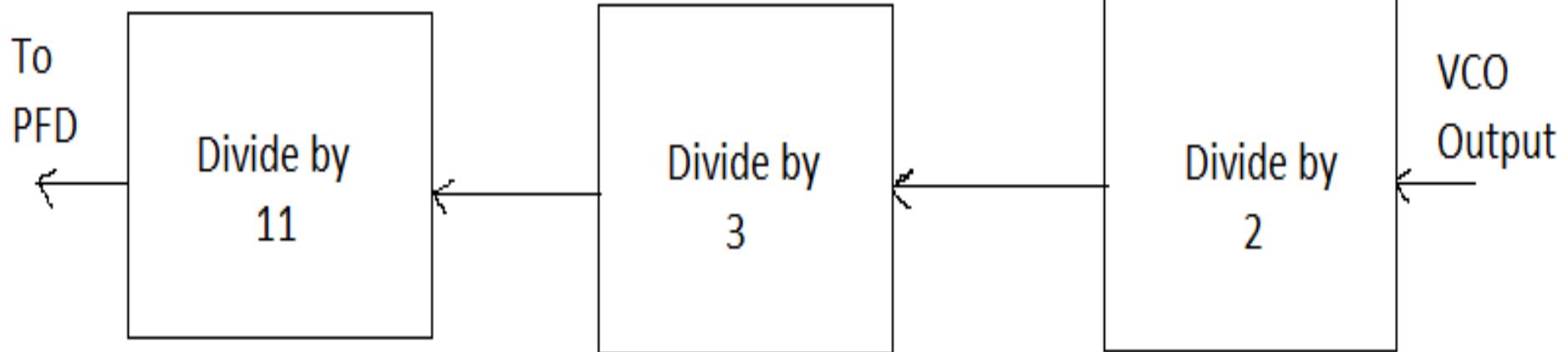
Introduction



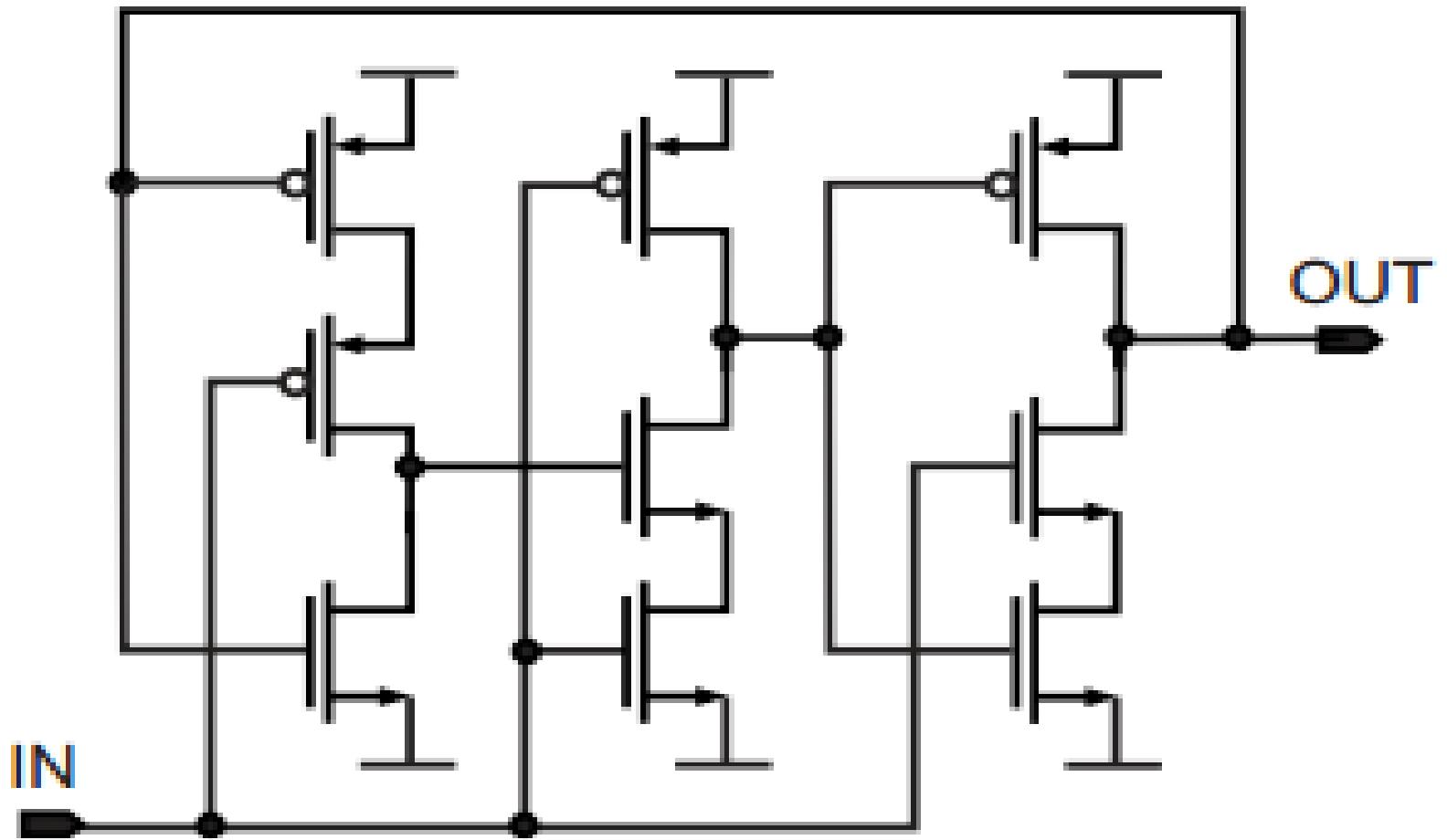
Proposed System

- Output of the VCO is 10.3125 GHz
- Output of the divider 156.25 MHz
- The division ratio is 66

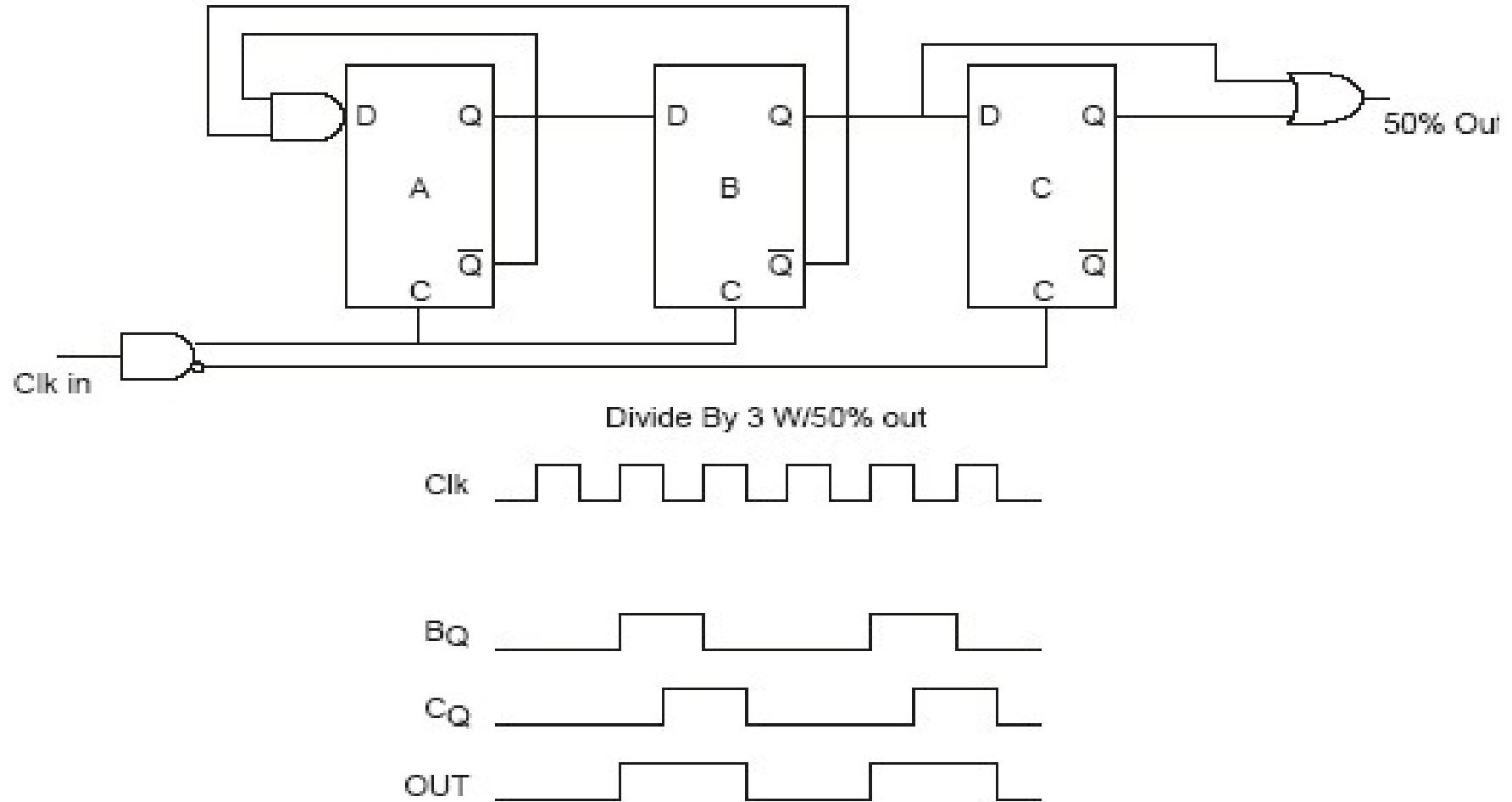
Cont'd Proposed Divider



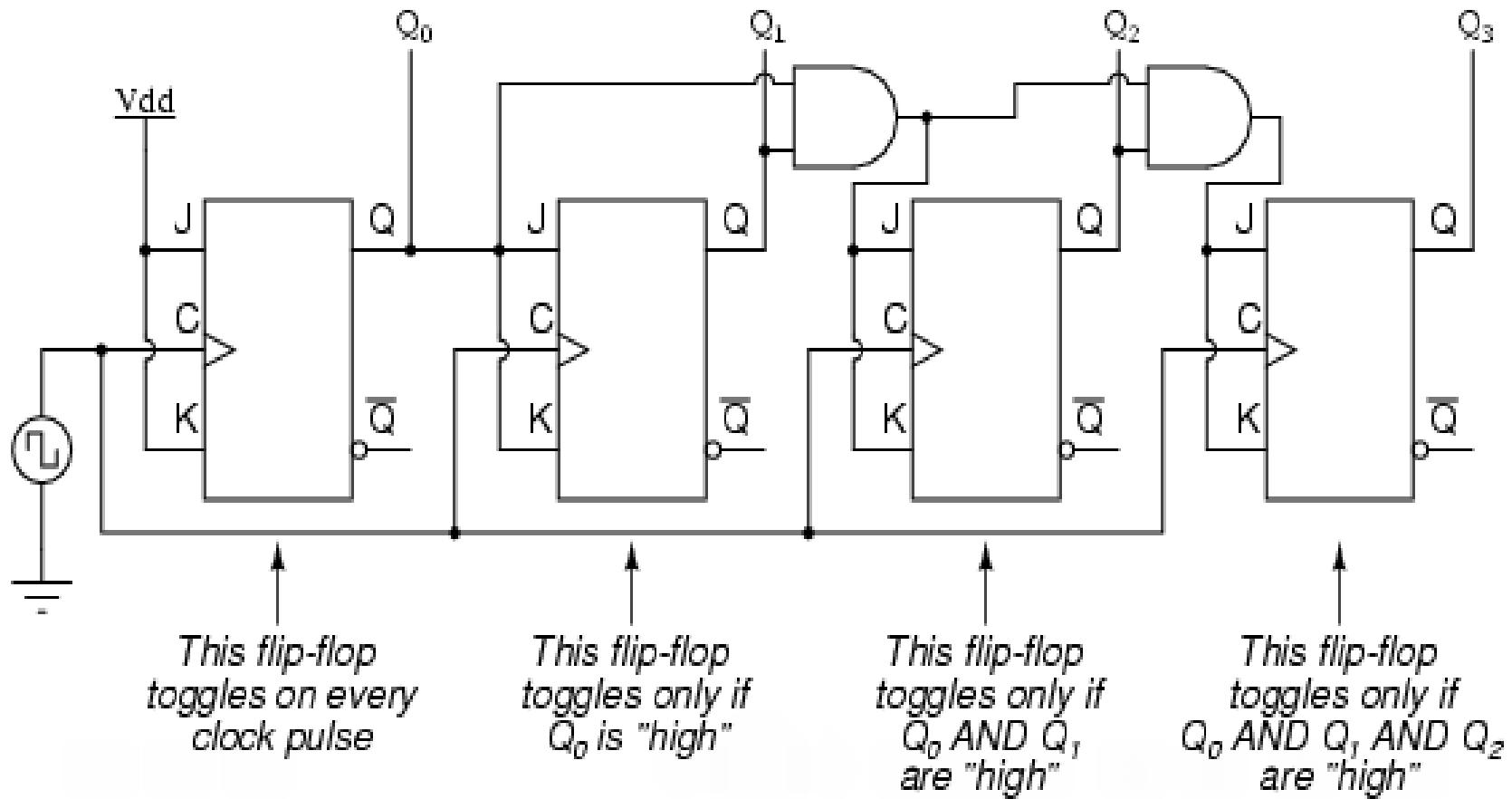
Divide by 2



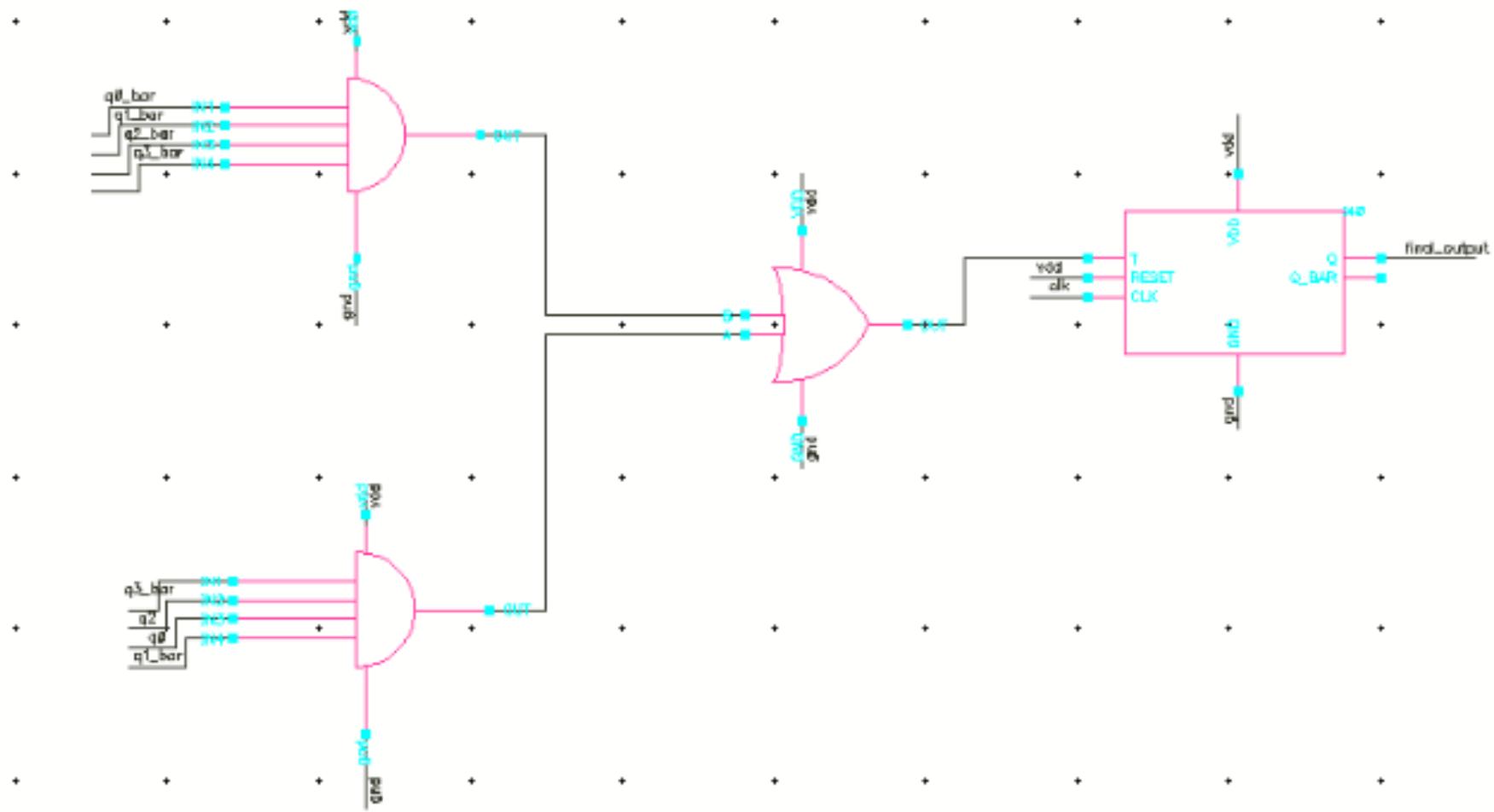
Divide by 3



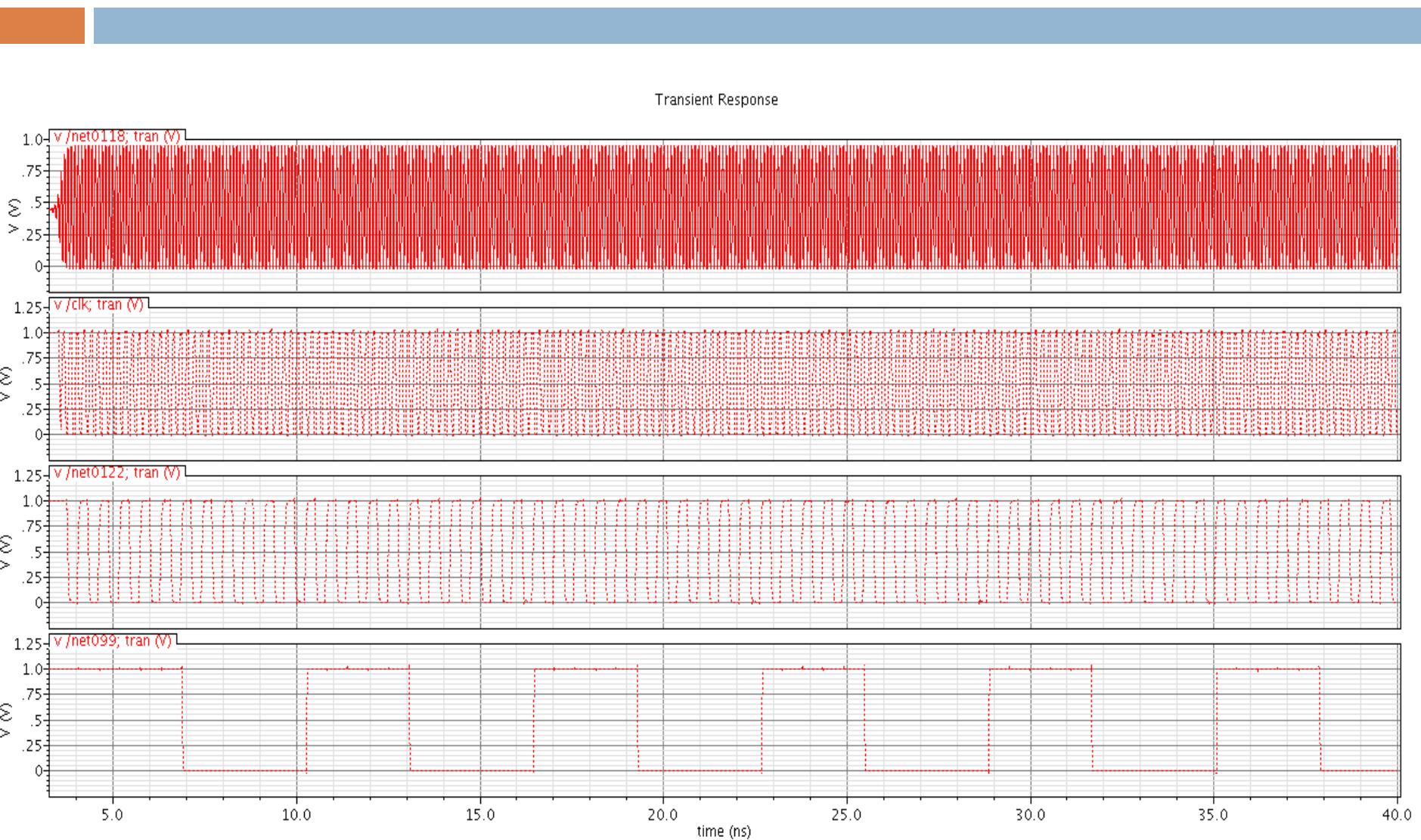
Divide by 11



Divide by 11

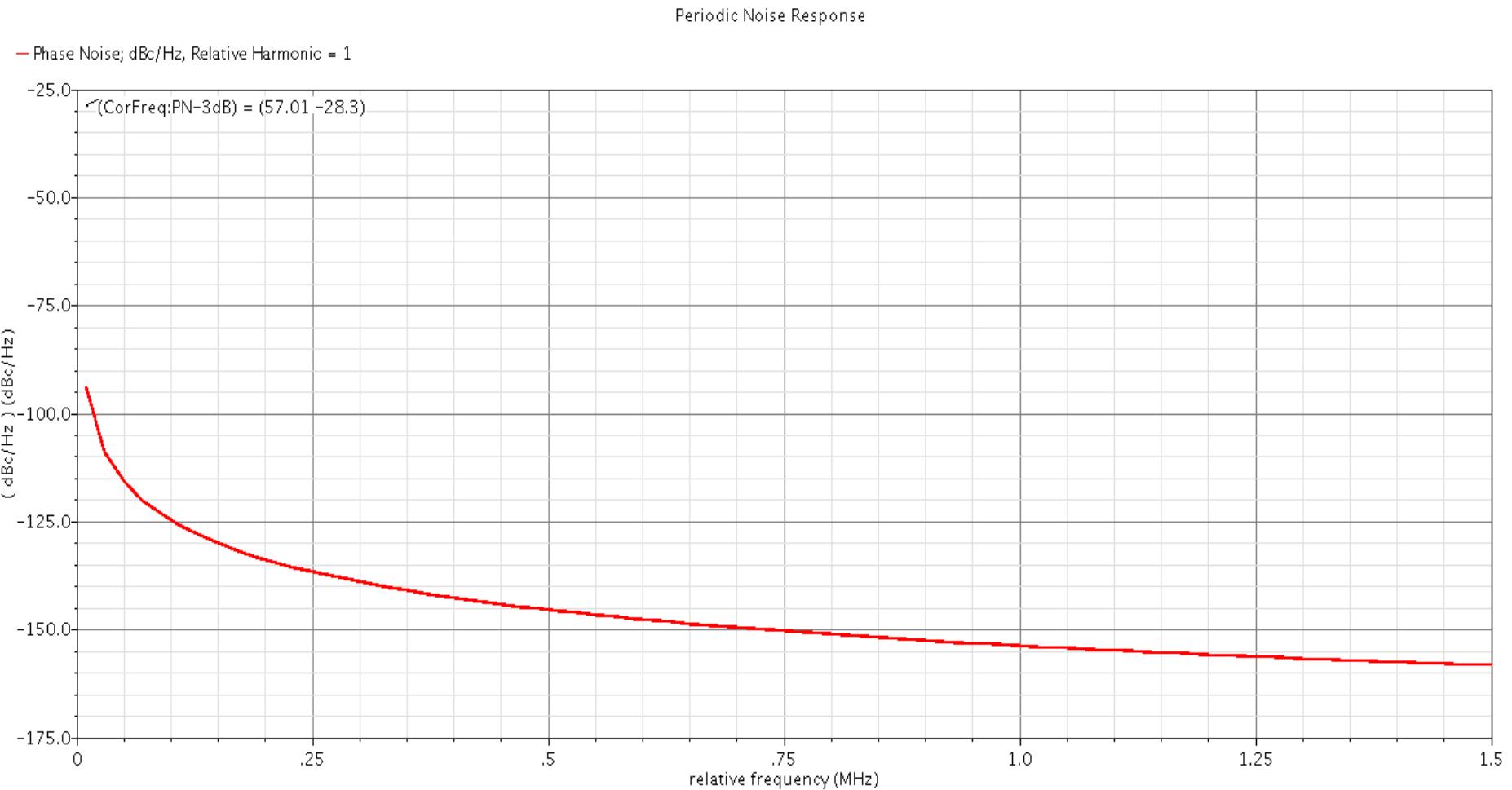


Simulations and Results



Cont'd Simulations and Results

Phase noise Simulation



Cont'd Simulations and Results

□ Power consumption

	Power consumption
Divide by 2	1.38 mw
Divide by 6	3.32 mw
The whole divider	5.7 mw



Questions ?



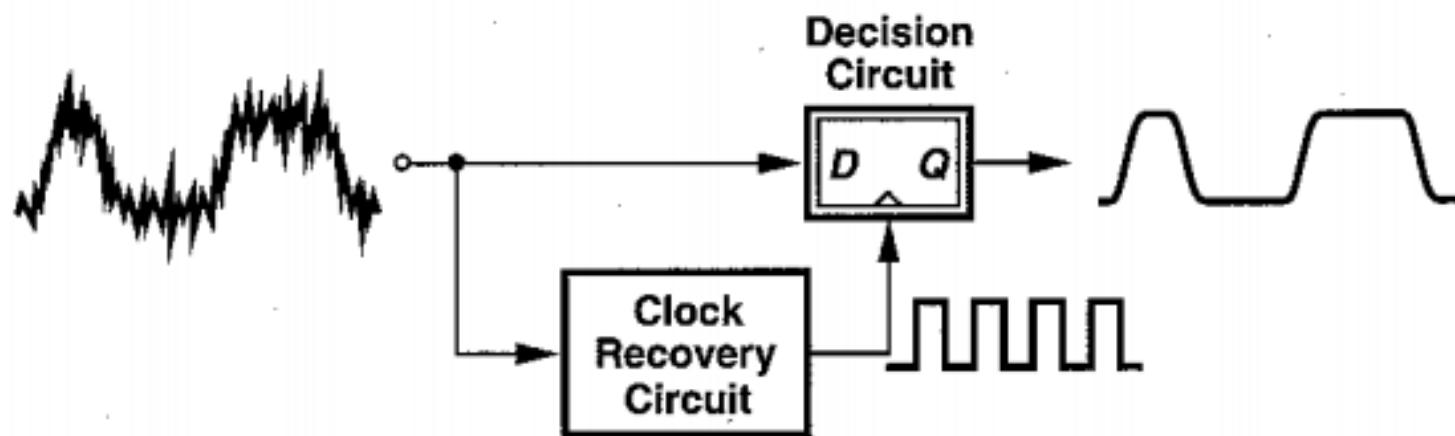
Clock and data recovery (CDR)

Overview

- Basic CDR
- CDR architectures:
 - Single loop
 - Dual loop
 - PI based CDR
- Proposed system:
 - Advantages
 - Challenges

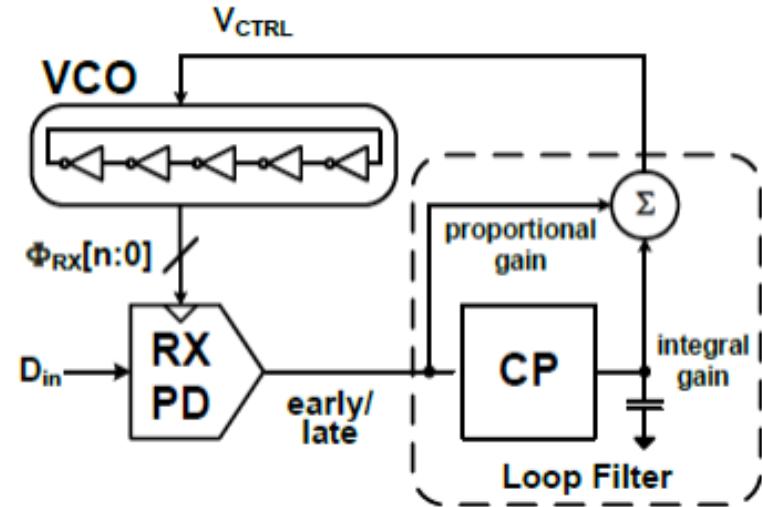
Basic CDR

- Clock recovery
- Data retiming



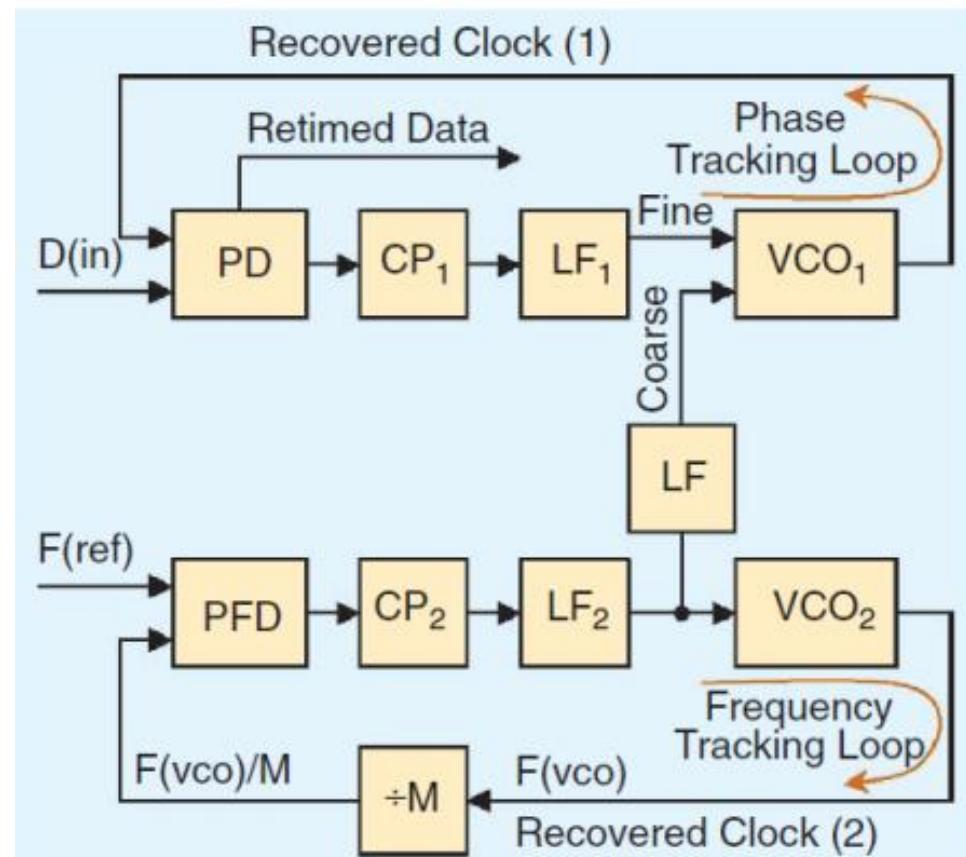
CDR Architectures

- Single loop:
- Disadvantages:
 - Noisy VCO requires large BW.
 - Large BW results in passing input jitter to output.
 - Harmonics
 - Large lock times

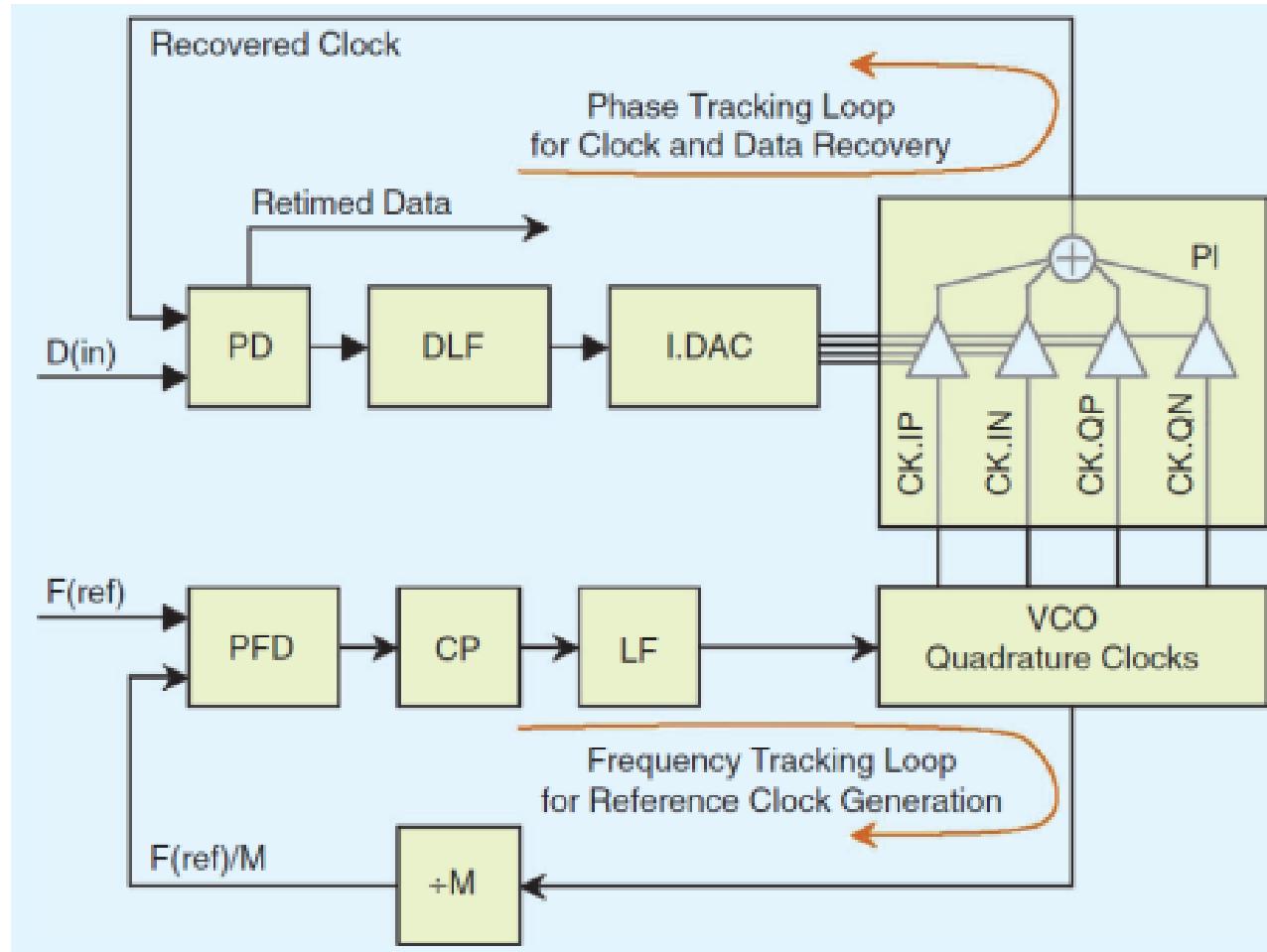


Dual loop

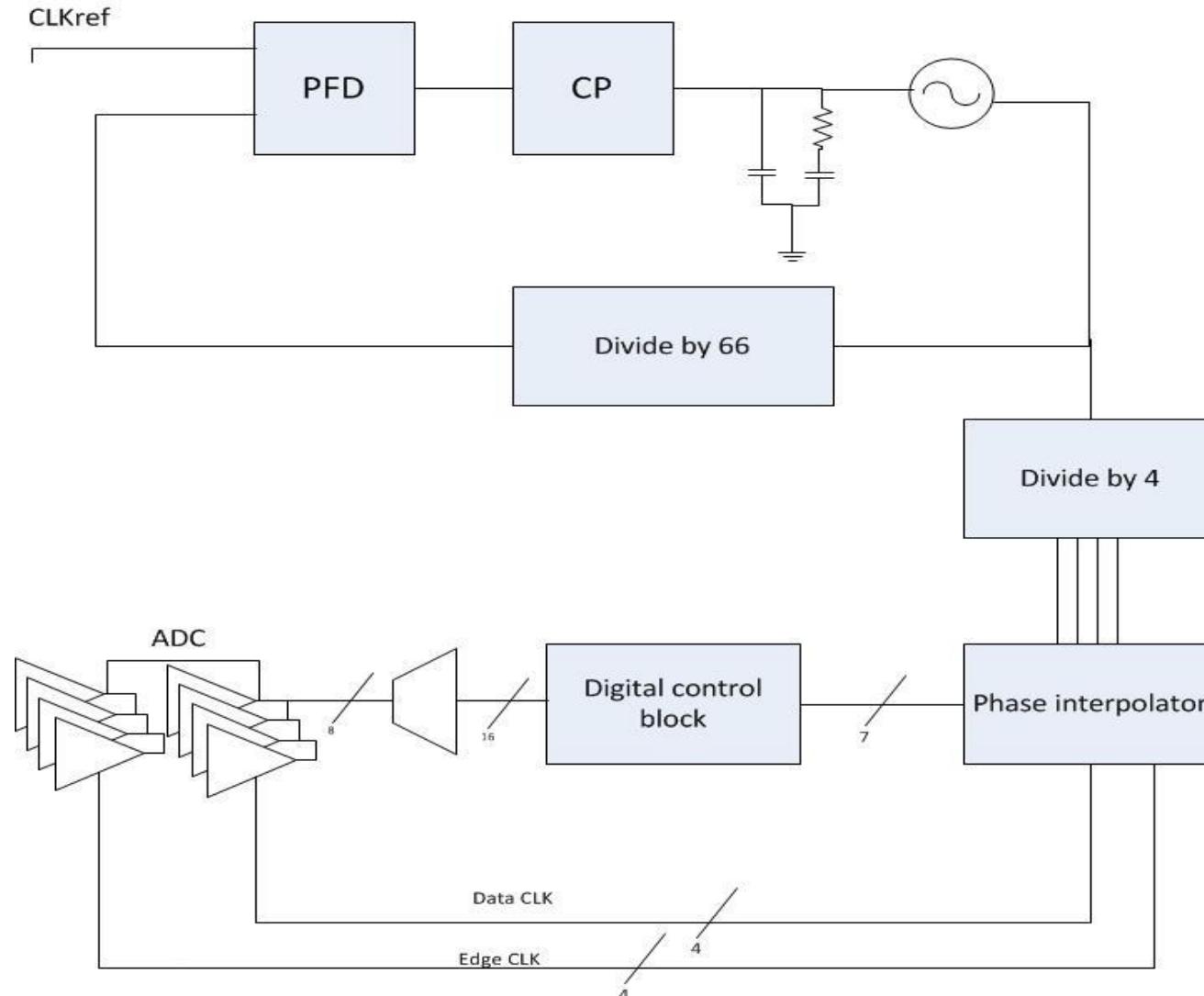
- One loop generates the required freq.
- The other tracks the phase.
- Advantage: BW of the two loops are independent.
- Disadvantages:
 - Frequency offset and VCO matching



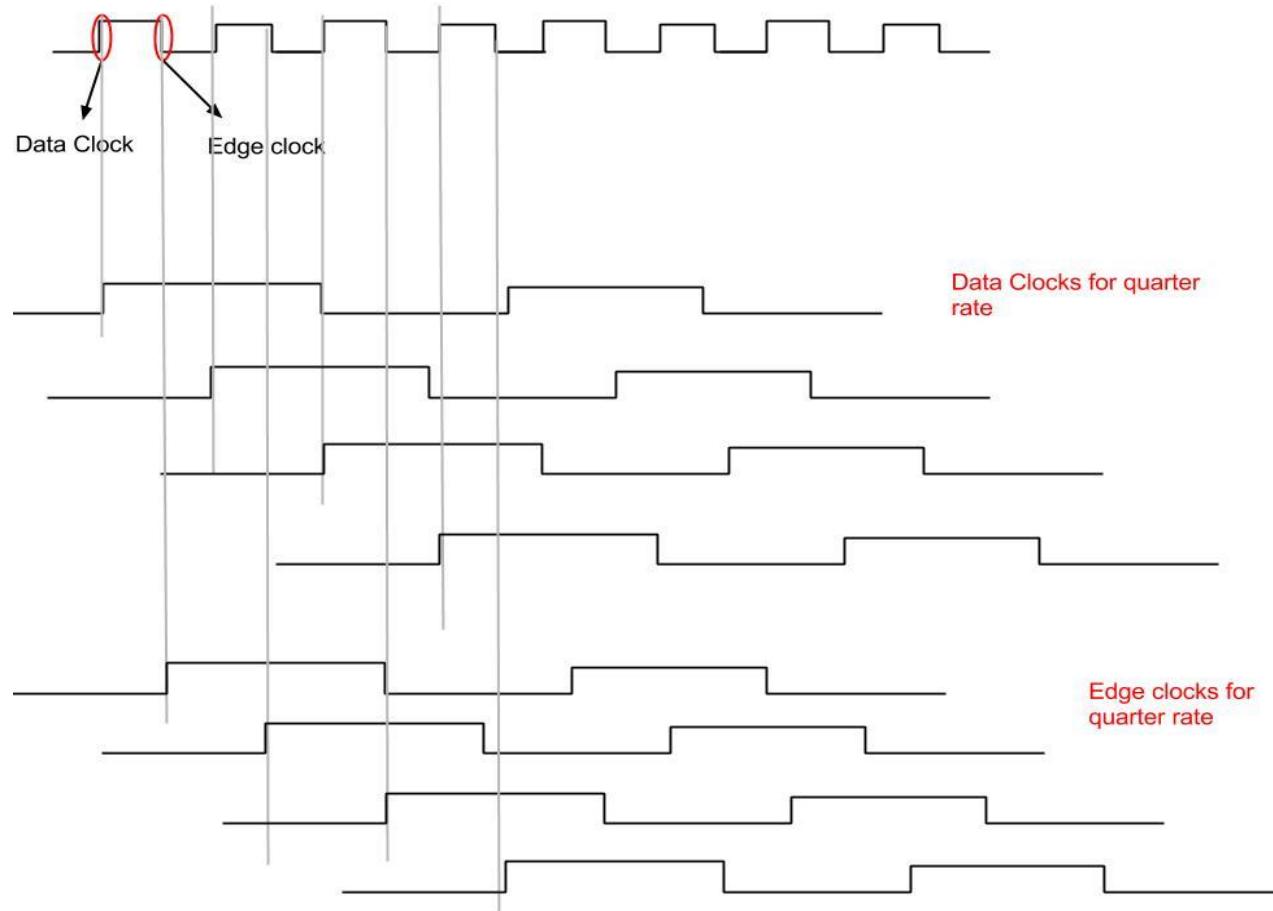
PI based CDR



Proposed system



Clocking schemes

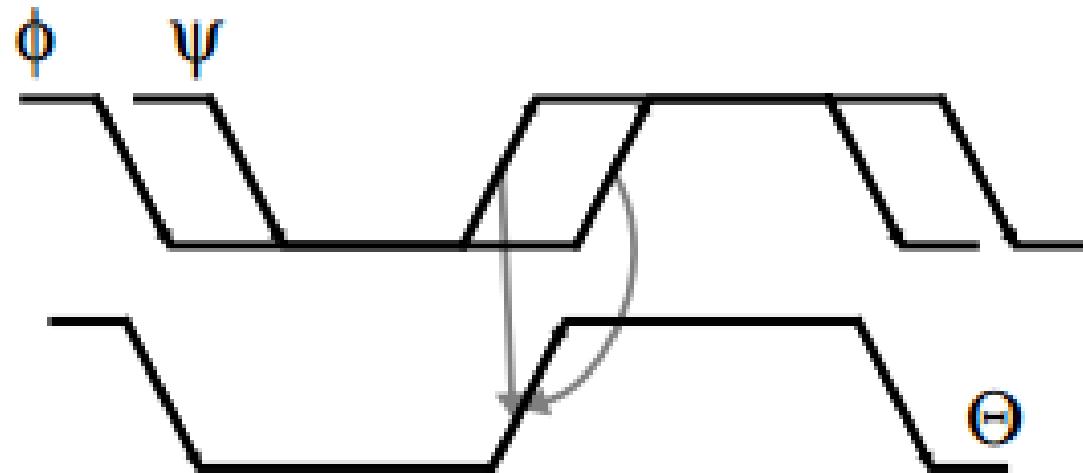




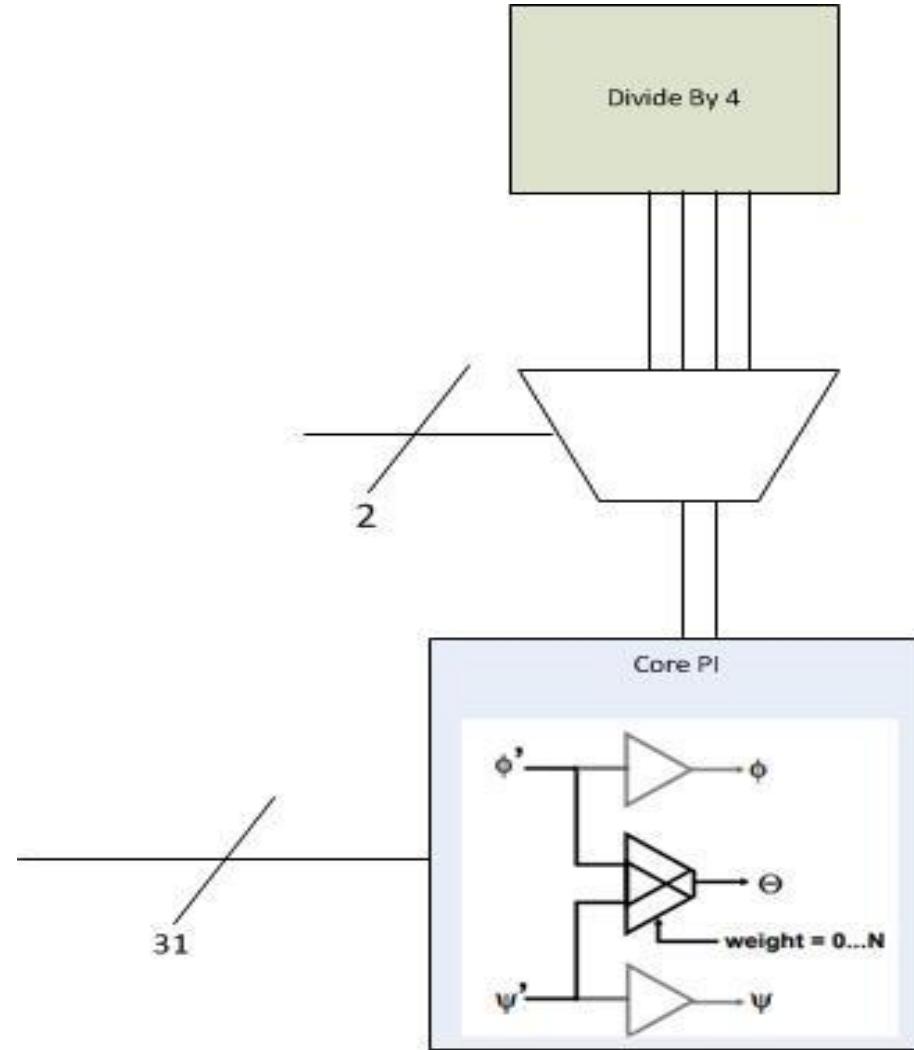
Questions ?

Phase interpolator

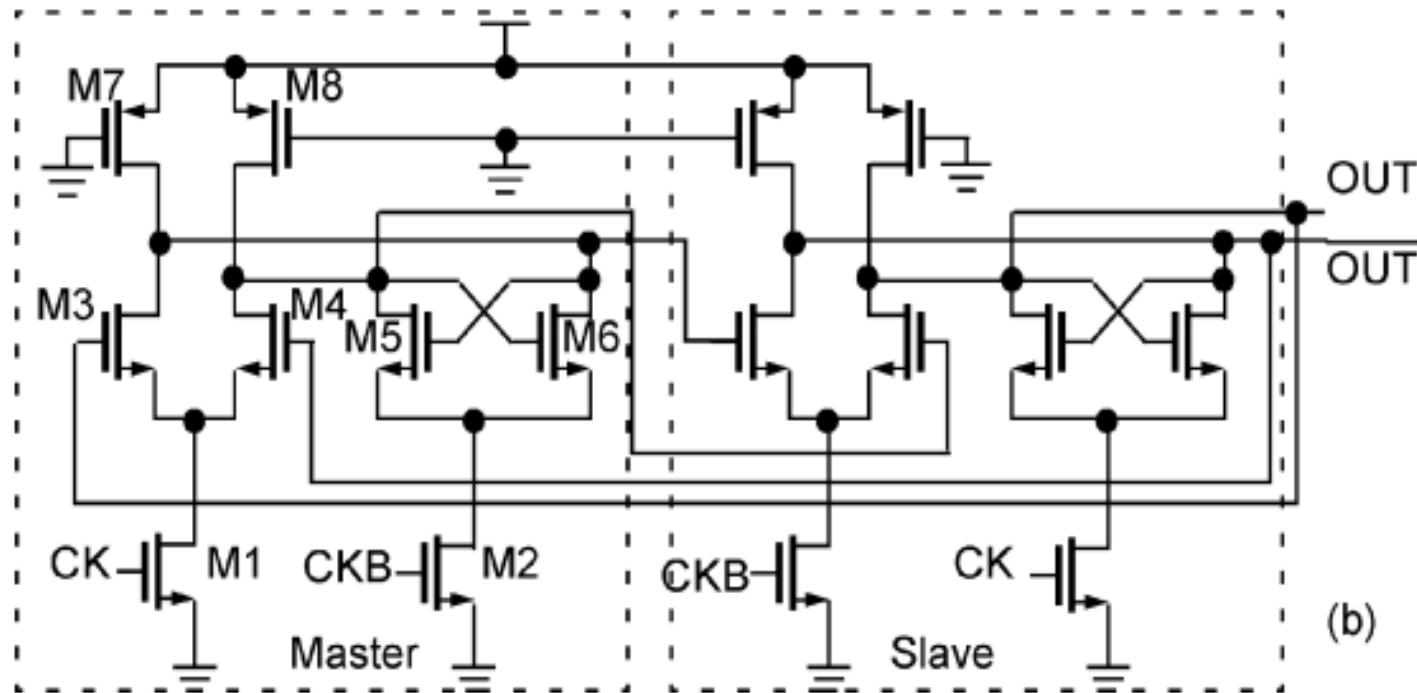
Phase interpolator



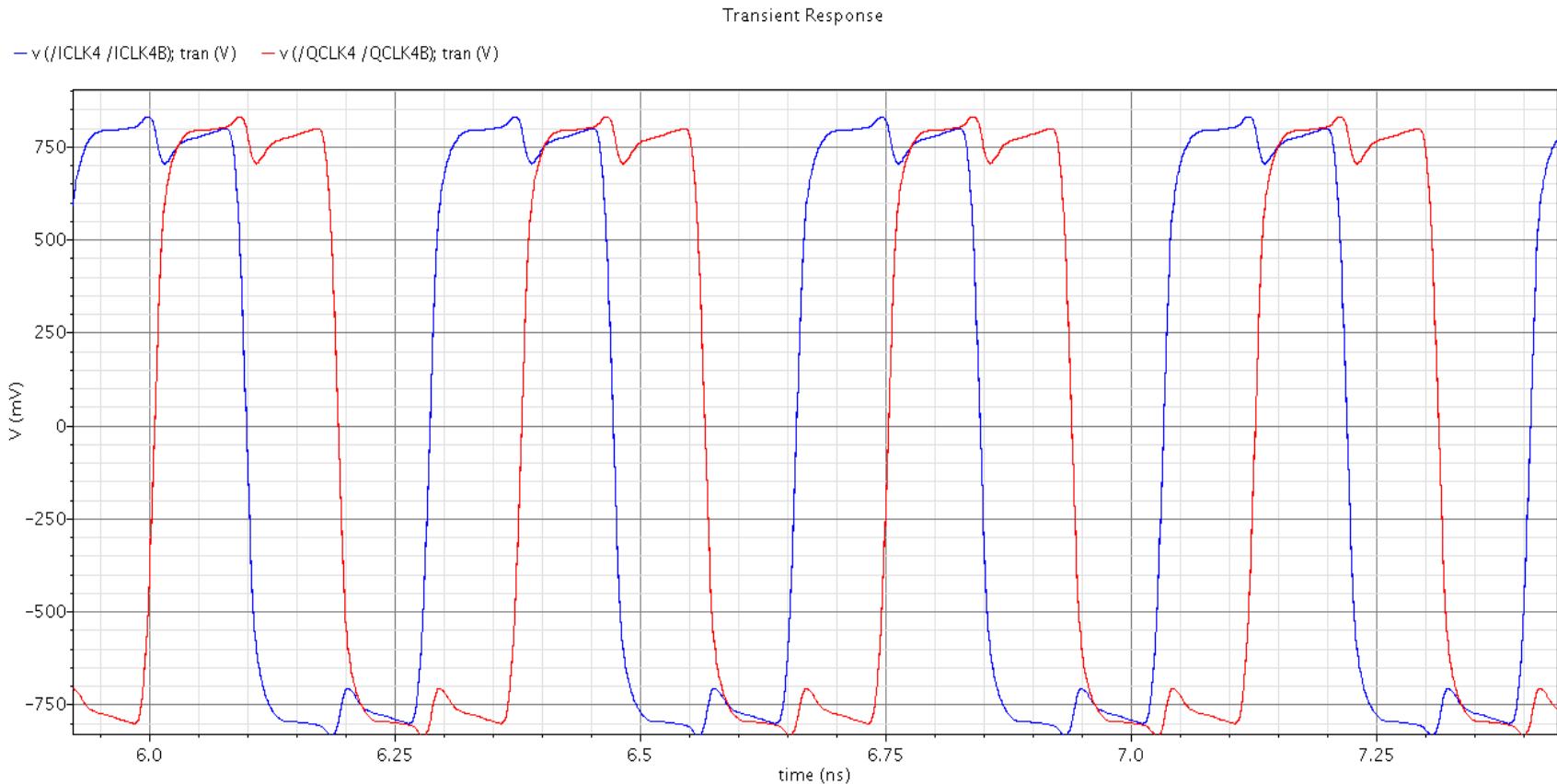
Block Diagram



Divider



Divider

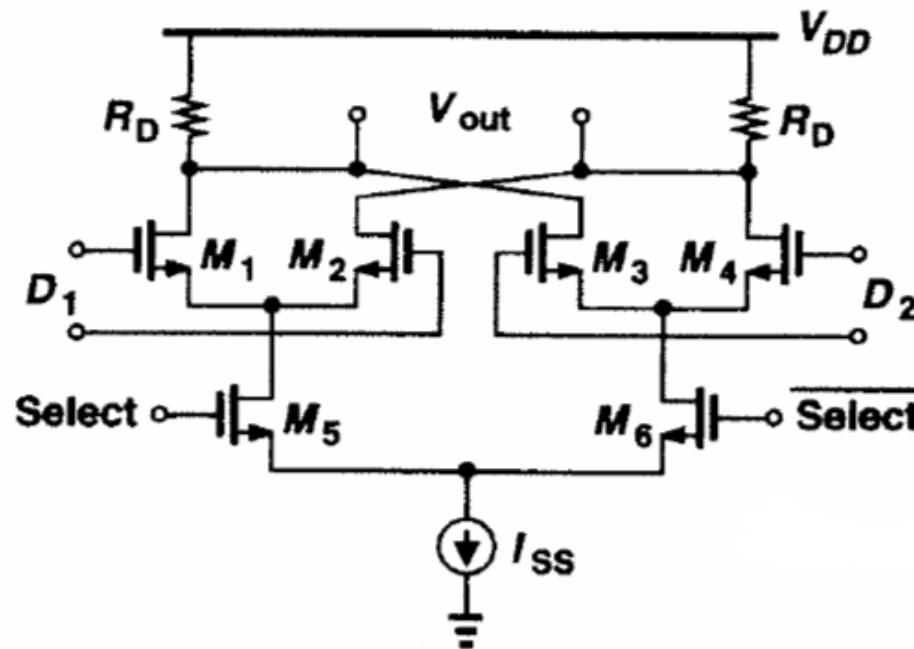


Divider

- The divider has two advantages for the next stages:
 - It automatically produces in-phase and quadrature-phase.
 - It produces differential clock, so I practically have 4 phases I, Ibar, Q and Qbar.

Multiplexers

- Two 2-1 multiplexers, one for I-phase and one for Q-phase.
- CML multiplexers are used.

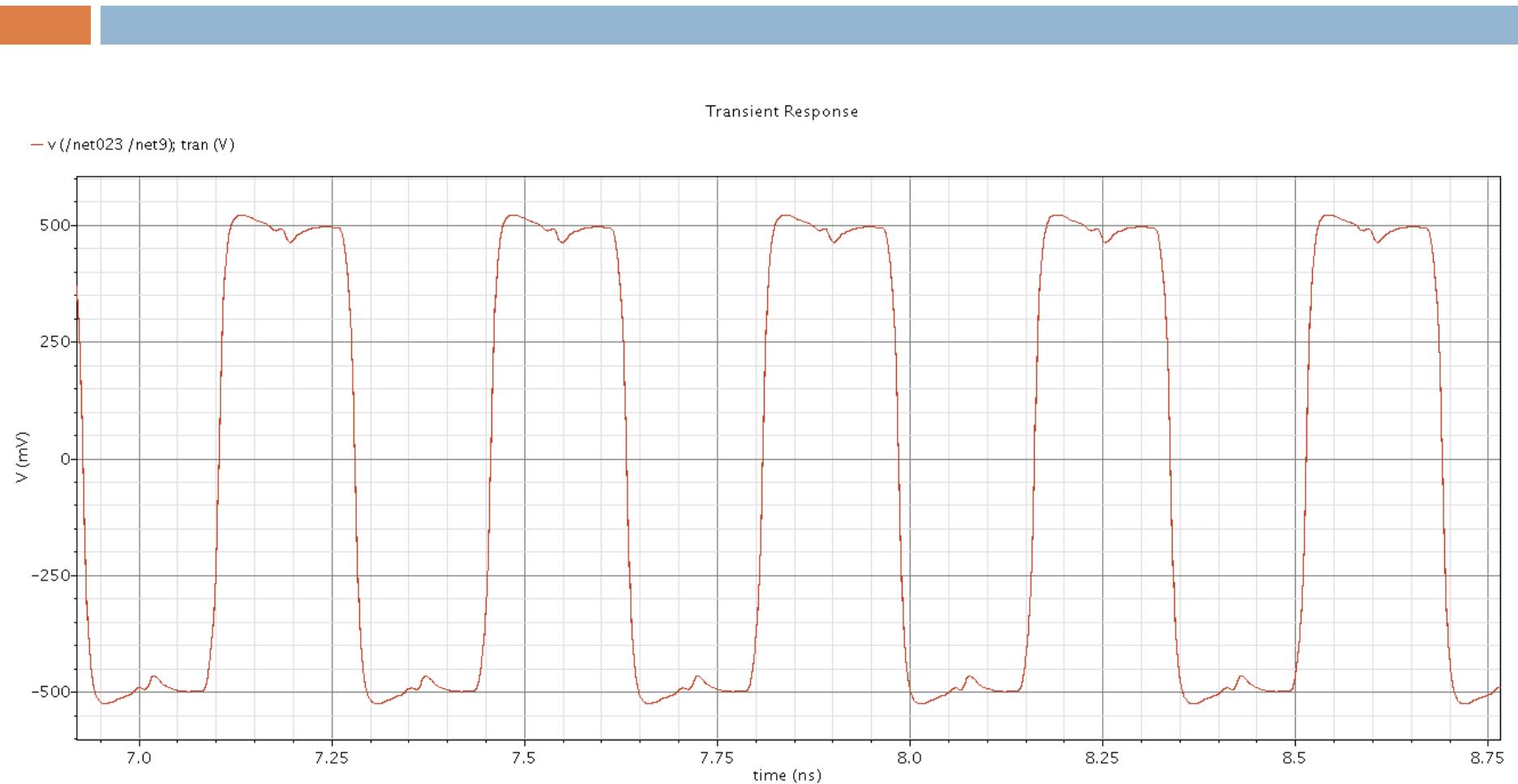


Selecting the quadrant

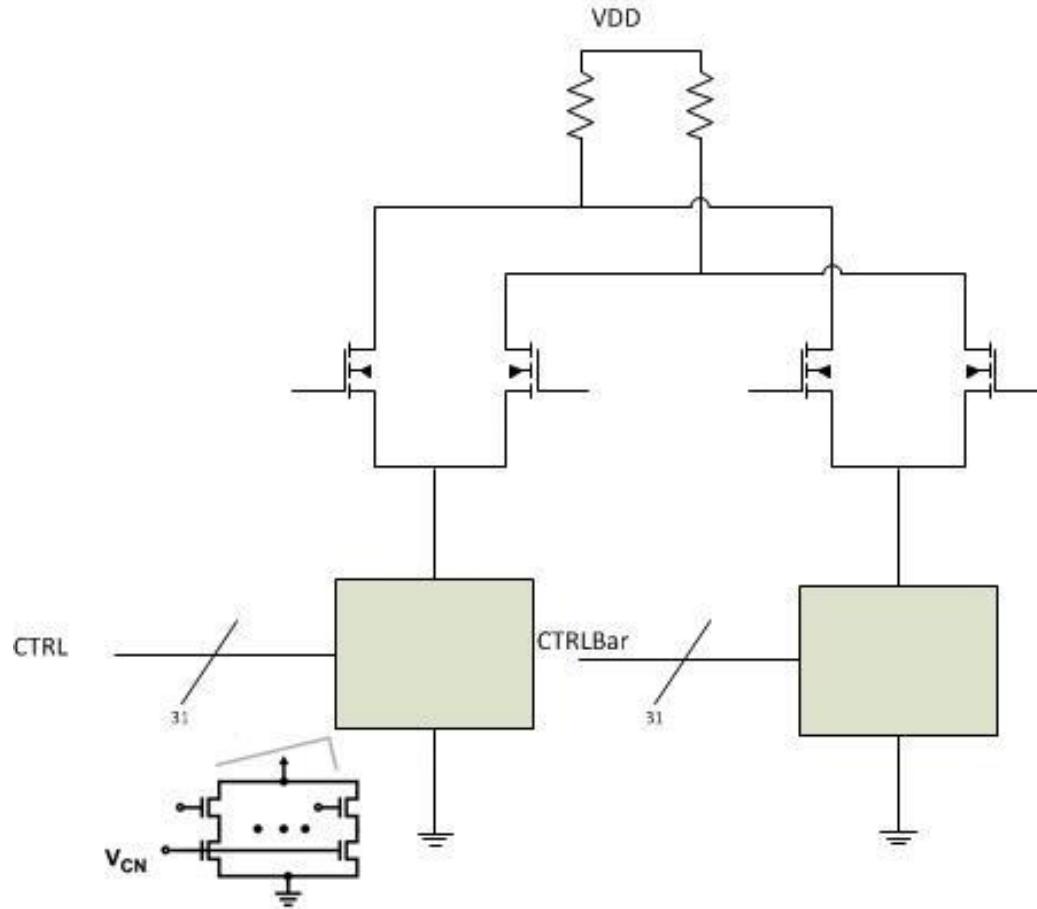
- Gray coded selecors.

Quadrant	S1 S0
1 st	00
2 nd	01
3 rd	11
4 th	10

Output waveform



Core phase Interpolator

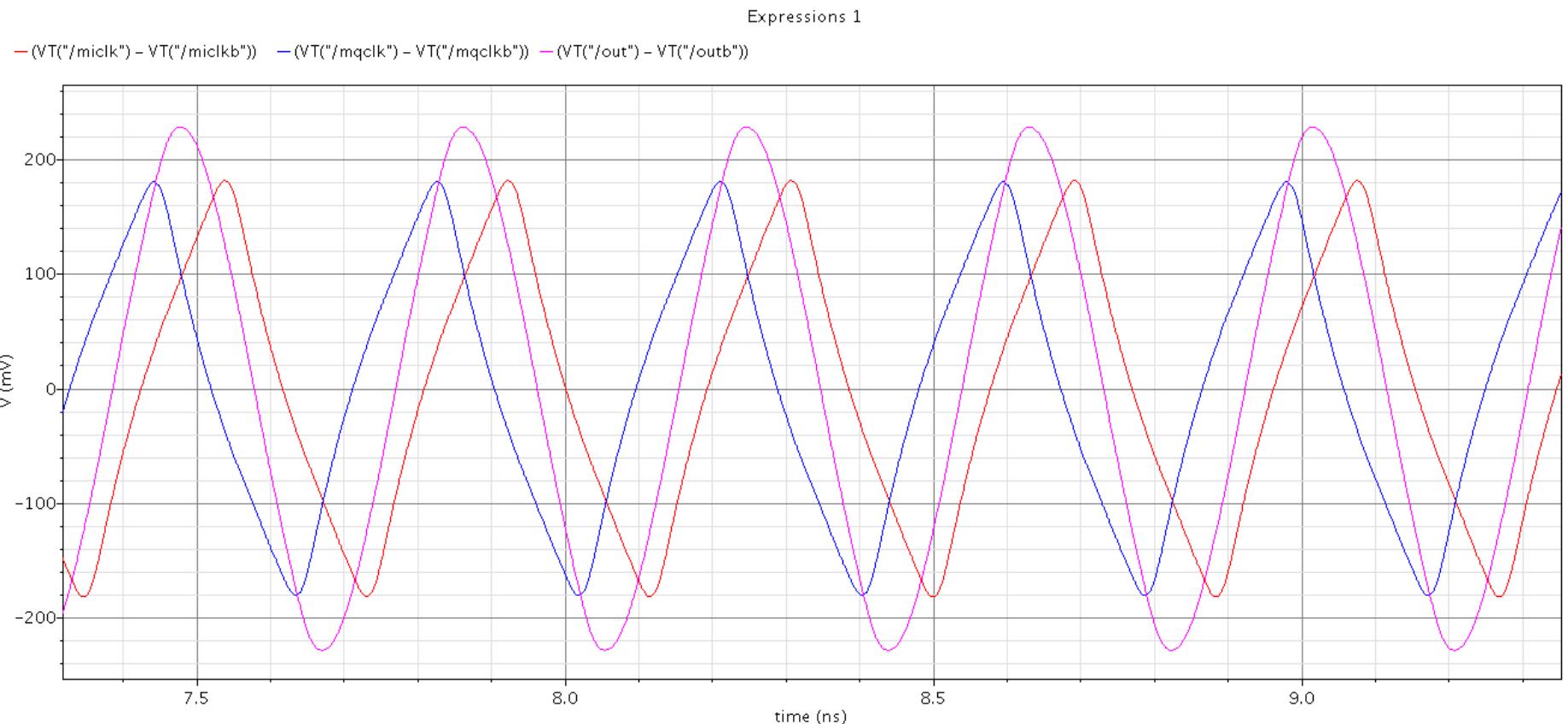


Degeneration capacitance

- Degeneration capacitance at the input.

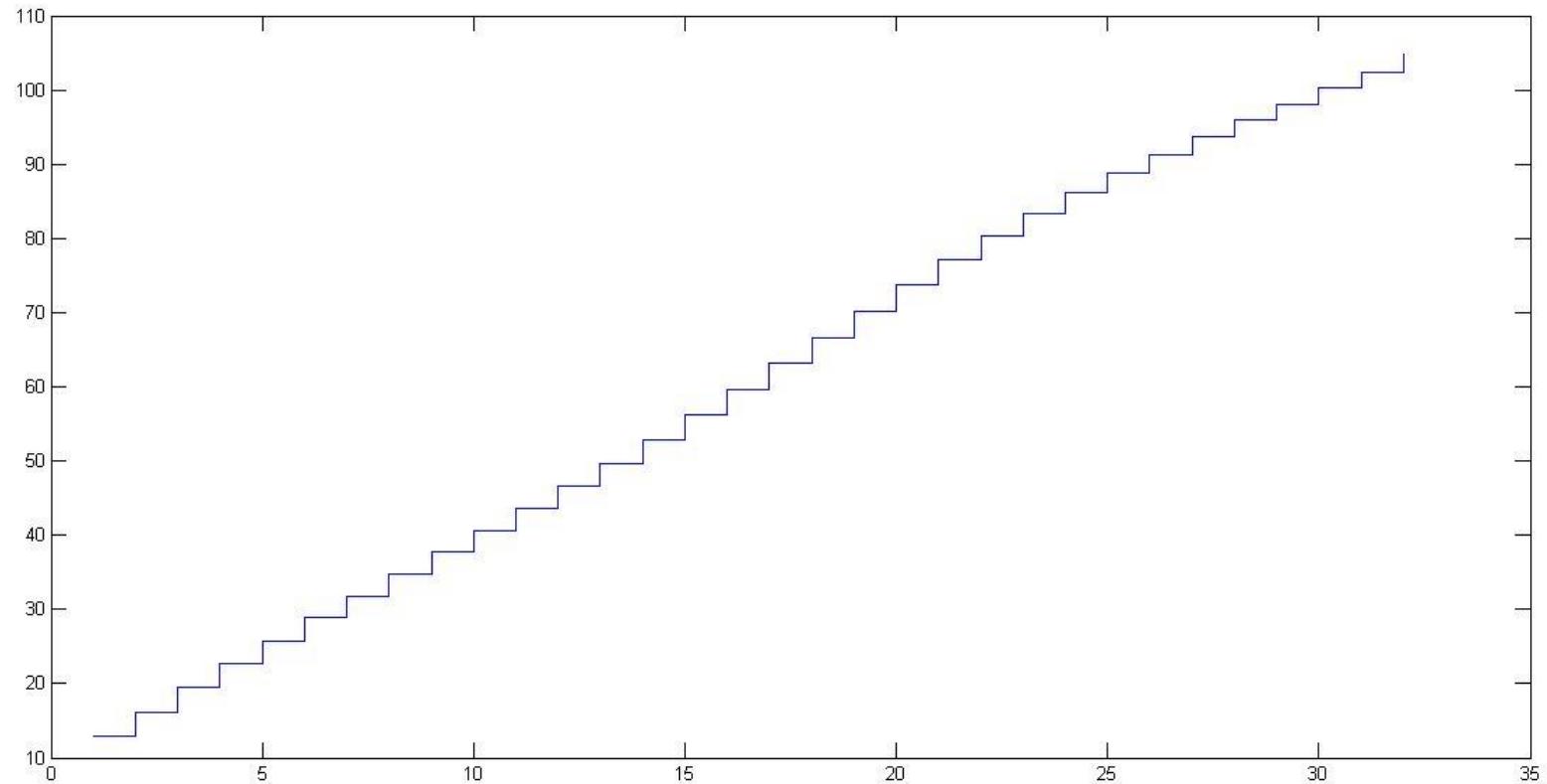
- Advantages:
 - Eliminate the sharp edges to allow proper interpolation.
 - Decrease the swing to drive the interpolator to a linear region.

Interpolation waveform



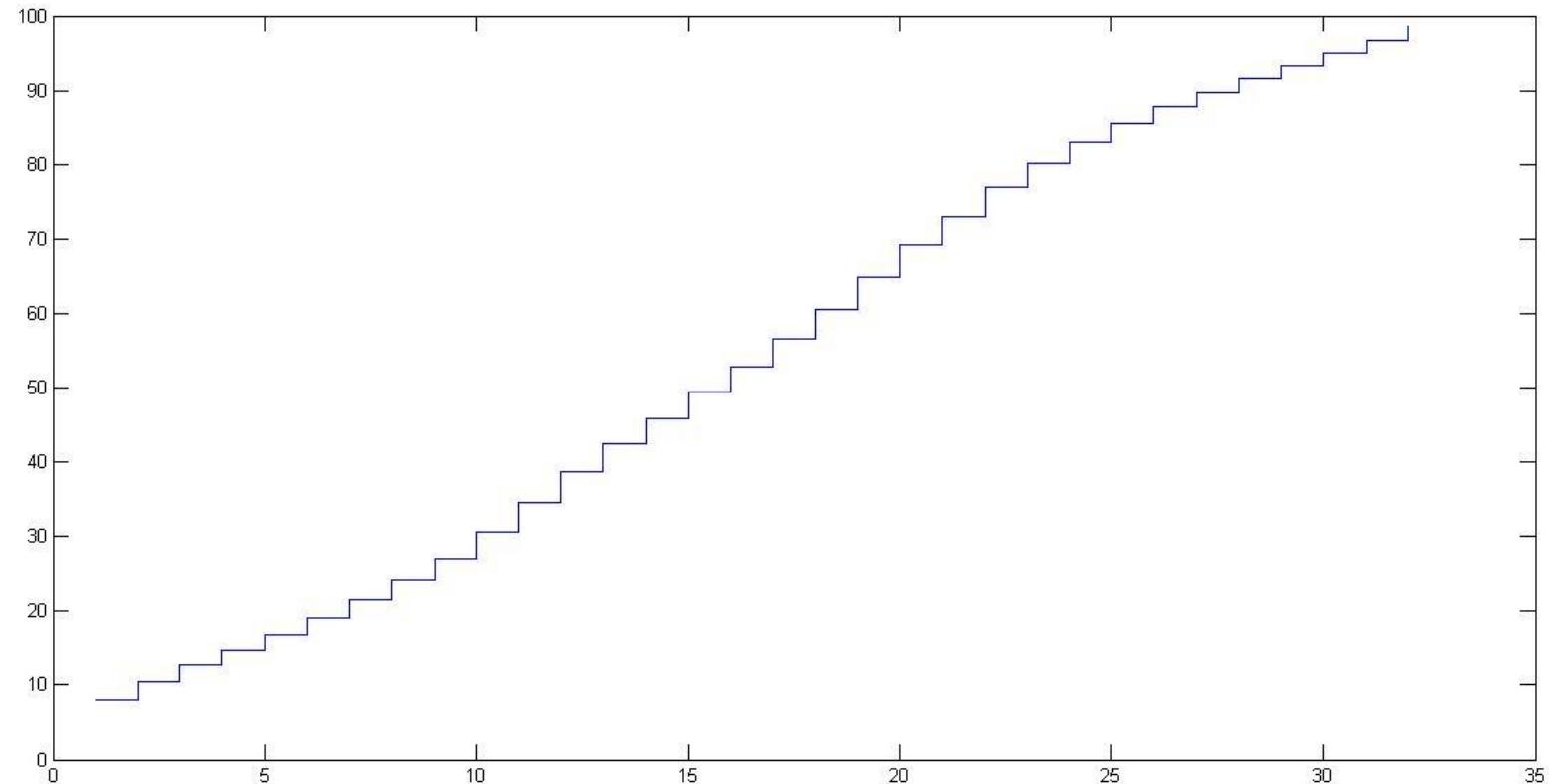
Simulation and results

□ Typical corner



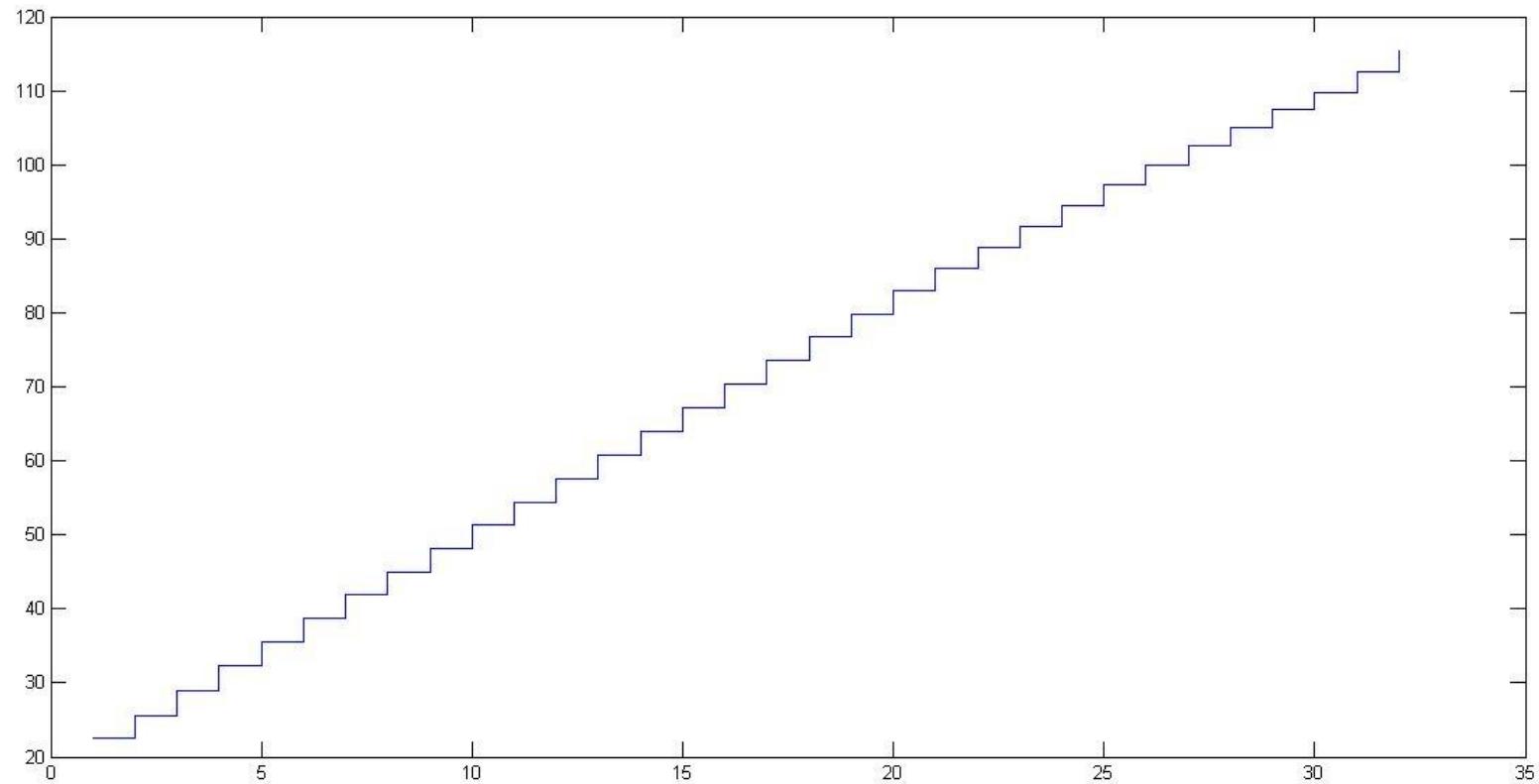
Simulation and results

□ Ff-0deg-1.1V

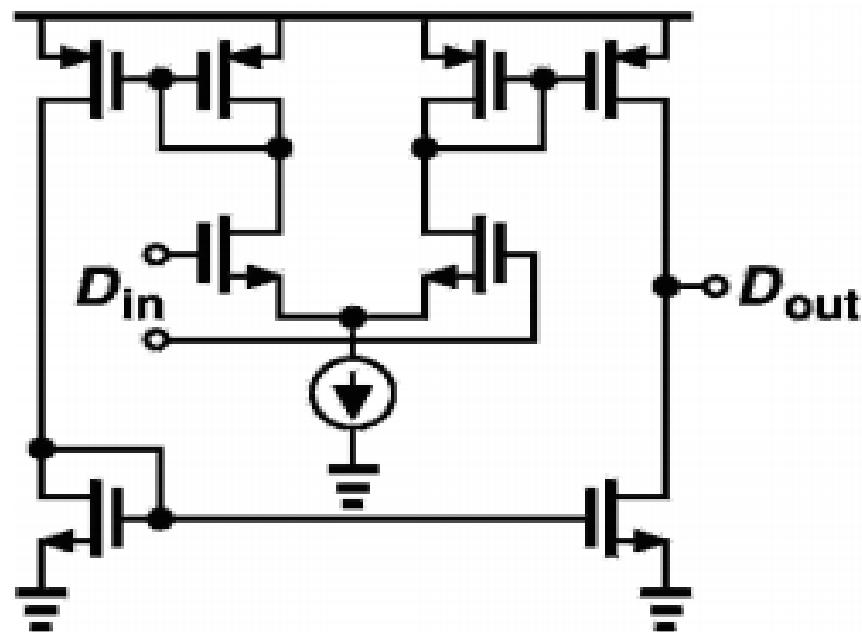


Simulation and results

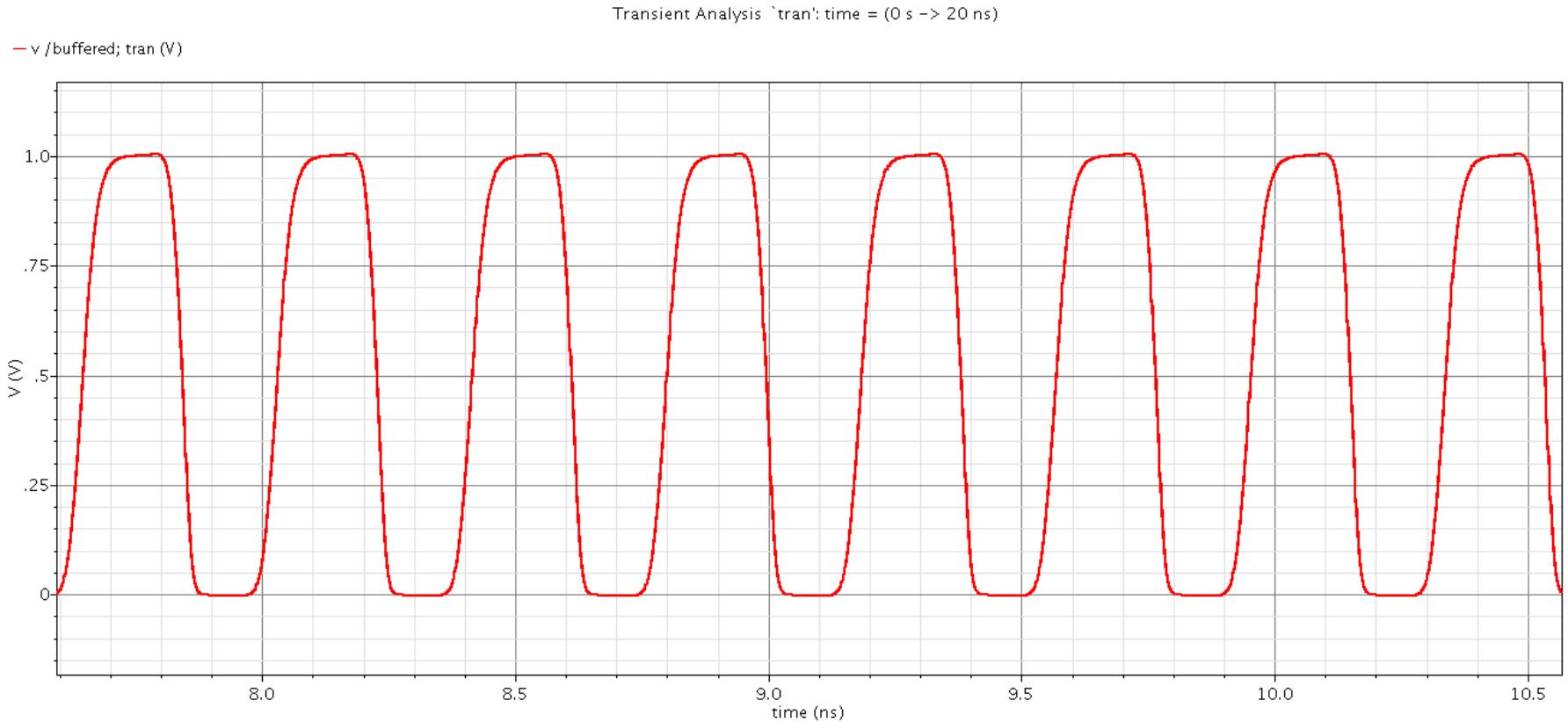
□ Ss-125deg-0.9V



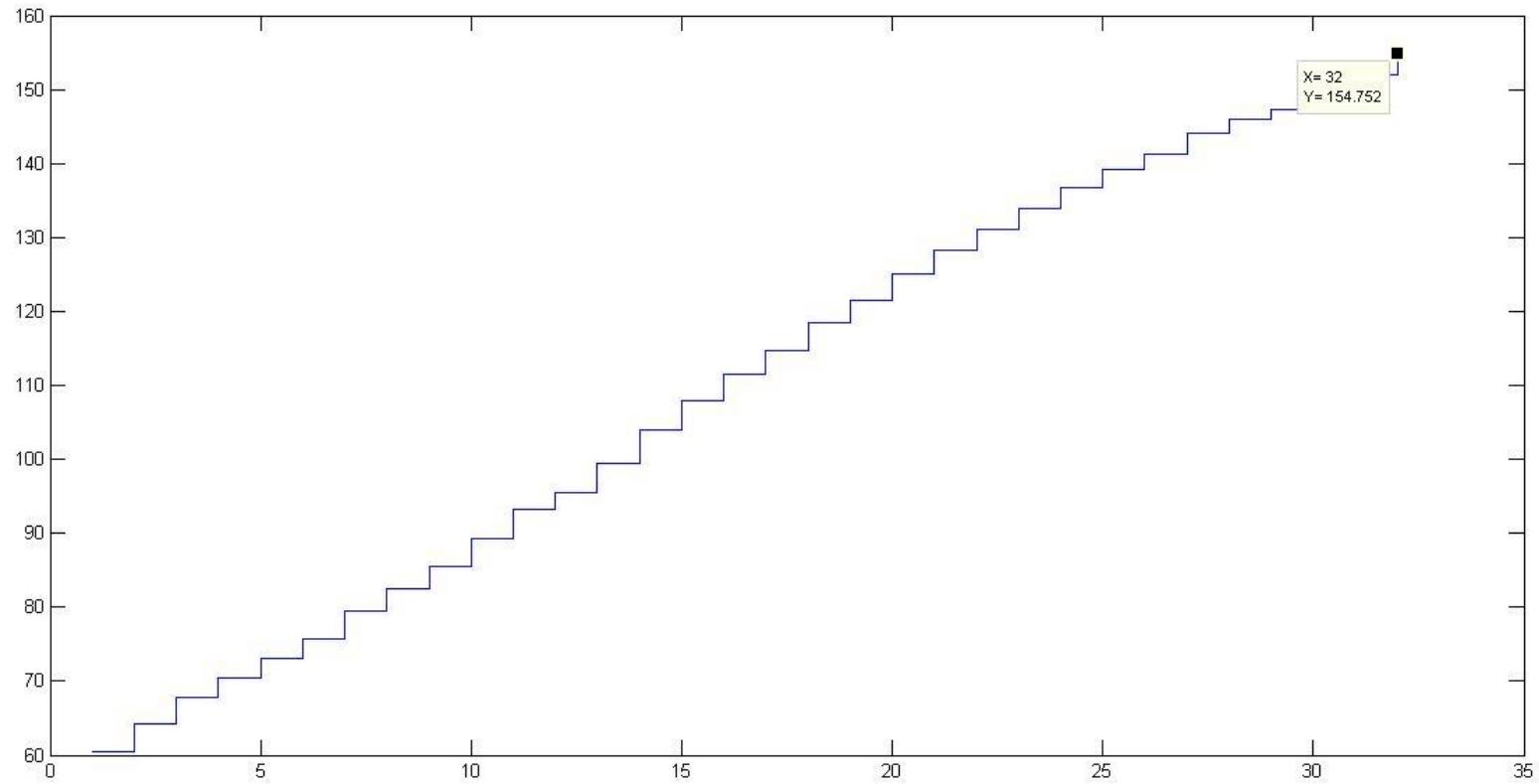
CML to CMOS



CML to CMOS



CML to CMOS



Power Consumption

Stage	Power consumption
Divider	0.93mW
Mux	0.75mW
Core PI	0.18mW
CML to CMOS	1.60mW
Total	3.46mW



Questions ?

Thank you !!!



WOOHOO!!!

Backup slides



Area and power (MUX)

Device/Property	Value
Diff pair	$2.4\mu\text{m}/60\text{nm}$
Select switches	$1.2\mu\text{m}/60\text{nm}$
Current mirror	$29\mu\text{m}/240\text{nm}$
Resistance	$1.25\text{k}\Omega$
Power consumption	0.75mW

Power and area (DIVIDER)

Device/Property	Value
M1 – M2	800n/60n
M3 – M4	1u/60n
M5 – M6	1u/60n
M7 – M8	600n/60n
Power consumption	0.93mW

Power (Core PI)

Device/property	Value
Diff pair	7μm/60nm
Switch transistors	200nm/60nm
Current sources	8 μm/360nm
Power consumption	0.179mW



Questions ?