Low Power High Speed 1-bit Full Adder Circuit design at 45nm CMOS Technology

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Abstract*—One bit full adder cell is one of the most frequently used digital circuit component in arithmetic logic unit (ALU) and it is the essential functional unit of all computational circuit. Till now lots of improvement has been done in this area to refine the architecture and performance of full adder circuit design. In this paper two designs of novel 1-bit full adder cell at 45nm CMOS technology is implemented by using ten transistors (10-T) along with the three existing 1-bit full adder cell. Later the complete comparison and verification is performed with the different existing and proposed adder cells on different supply voltages at 100MHz operating frequency. From the simulation results by performing the comparison among proposed adder cells and existing adder cells it is found that the proposed adder cells are better than the existing adder cells in terms of power consumption, delay and power delay product (PDP). From the simulation result it is observed that the first proposed adder circuit using XOR module has achieved maximum saving of power 91.65%, saving of delay 59.37% and saving of overall PDP of 91.64% when compared to existing Static Energy Recovery Full (SERF) full adder and Gate Diffusion Input (GDI) full adder circuit respectively. When second proposed adder circuit using XOR module is compared with existing SERF and GDI adder circuit maximum saving of power 93.04%, saving of delay 76.76% and saving of overall PDP of 96.01% is achieved. All above statistical analysis is given by performing the comparison between existing and proposed adder circuits which have same number of transistors count (10-T) in designing at supply voltage 1 volt.

Keywords— Conventional Adder, CMOS Adder, Full Adder, GDI, SERF,

I. INTRODUCTION

Demand for usage of battery based portable electronic system is increasing day by day,as the devices are portable they need battery for driving them. So power consumption and speed becomes the main concern in designing of devices such as laptops, tablets, mobile phones, notebooks, and many other personal communication devices.The power consumption plays vital role in VLSI technology. More power consumption leads to more heating which results in decreasing battery life and also needs cooling fan to cool the circuitry. Therefore power consumption affects the battery life and the cost of the whole system.Mostly all digital communication devices and the devices about which we have discussed above are used in the applications like digital signal processing, image and video processing, microcontrollers and these applications uses various arithmetic and logic operations to perform addition, subtraction, multiplication etc. All these operations like addition subtraction and multiplication could be performed internally with the help of adder cells only. Since one bit adder circuit (cell) plays most important role in designing these digital communication devices. Frequently all digital communication devices have multiple numbers of 1-bit full adder cells integrated within it to perform one or many bits addition operation, this is the reason adder cell plays an important role in determining the performance of the whole system.

To reduce the area of chip, the complexity in the circuits has increased significantly, because of that the power dissipation and performance of the adder circuit are being affected. So there is concern towards circuits design in low power VLSI design to reduce the chip size and power dissipation. There are two types of power dissipations in MOSFET technology i.e. static power dissipation and dynamic power dissipation. In Static power dissipation there are few parameters which effect operation of device like sub threshold leakage, reverse-biased junction leakage, gate direct tunneling leakage and gate induced drain leakage shows the major effect in various scaling parameters. In Dynamic power dissipation mainly switching and short circuit power is considered. The static and dynamic power dissipations are calculated theoretically from the equations shown in (1) and (2) respectively.

$$P_S = I_C * Vdd (1)$$

$$P_D = \frac{1}{2} C_L (\Delta V_o)^2 f \ (2)$$

Where I_C = Leakage current, Vdd = Supply voltage, C_L= Load capacitance, ΔV_o= Logic voltage swing,f = Operating frequency.

Power delay product (PDP) is a parameter which is used in this paper for comparison between various adder circuits to estimate the optimized results either at a single operating frequency or at different operating frequency regions [1,2].

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Theoretically power delay product can be calculated from the equation (3) shown below.

$$PDP=P_{AVG}*T_D \quad (3)$$

Where P_{AVG}= Average power dissipation, T_D= Delay of the circuit.

The rest of paper is organized as- In section 1 we have discussed about introductory part of 1-bit full adder, various type of existing adder is discussed in section 2, proposed work is discussed in section 3, later simulation and results are discussed in section 4 and conclusion is discussed in section 5.

II. LITRATURE SURVEY

Till now in digital world different types of full adder cells are designed with different logic styles. Some of them are good for low power application, some of them for high speed, few of them full fill minimum area requirement but all these design has its own merits and demerits. According to requirement of applications these adders are used. Few full adder cells which are already implemented are conventional (28T) full adder cell [3-6], Static Energy Recovery Full adder cell (SERF) [7-10], Gate Diffusion Input (GDI) full adder Cell [11, 12] etc.

Most of the complex computational circuit requires full adder circuitry hence the whole power consumption and speed of computational circuit can be managed by the implementing the low power and high speed adder cell, so overall performance of computational circuits are totally depends on the adder cell. A full adder cell consists of three inputs named A, B and Carry in (Cin) with two outputs named Sum and Carry out (Cout) as shown in Fig.1.

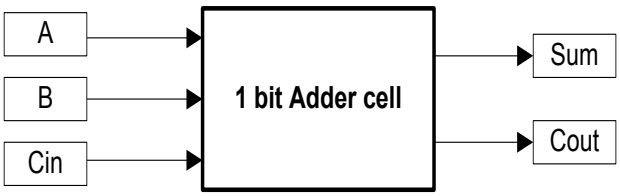

Fig.1. Basic building block of 1 bit full Adder cell.

TABLEI.Truth table of 1 bit full adder cell.

Inputs			Outputs	
A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Expression for sum and carry out

Sum = A'.b'.Cin +A'.B.Cin'+ A.B'.Cin'+ A.B.Cin (4)

$$= (A \oplus B) \oplus Cin(5)$$

Carry out (Cout) = A'.b.Cin +A.B'.Cin+ A.B.Cin' +A.B.Cin(6)

$$= A.B + B.Cin + Cin.A(7)$$

$$= (A \oplus B)\, Cin + (A \oplus B)'\, B \quad (8)$$

The output expression for Sum and Carry out (Cout) of one bit full adder cell is theoretically derived from Table 1 and shown above by equation (5) and (8) respectively.

First of all the analysis of existing design i.e. one bit full adder cell is carried out at the operating frequency of 100 MHz along with their advantages and disadvantages.

A. C-CMOS Full Adder Cell

The conventional C-CMOS 1-bit adder cell using 28 transistors is based on standard CMOS topology as shown in Fig.2. Due to large number of transistors used in designing it's power consumption is high and the critical path with the input of the circuit consist of 5 transistors in its forward path so propagation delay is more [1-4, 6, 13]. This design does not uses compliment of input signals and therefore the short circuit current is reduced and the most important advantage of this circuit is it produces full output voltage swing, thus this circuit has high noise margin that is why it is reliable to operate at the low voltages.

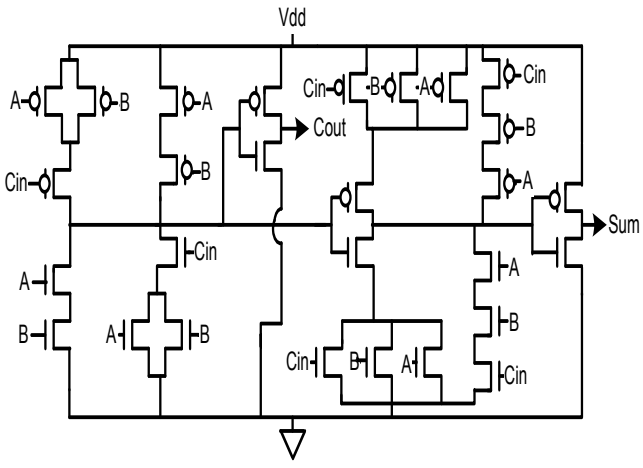

Fig.2. C-CMOS Full Adder Cell (Conventional full adder cell)

B. Static Energy Recovery Full Adder Cell

StaticEnergy Recovery Full (SERF) adder requires ten transistors (10-T) to implement it [7-10,13]. It can be implemented by using XOR or XNOR gates, Fig. 3 shows

implementation of SERF with the help of XOR gates. To produce sum output it uses two cascaded XOR gates. Here is threshold loss problem in SERF circuit and the result of these output signals (Sum, Cout) will not provide full swing of voltages means degradation of output signal take place which is not at all desirable condition for cascaded structure. Main disadvantage of SERF along with output logic swing is that both the power dissipation and delay are more. The advantage of SERF is that it uses the least number of transistors in designing so the chip area is reduced and also it should be noted that the SERF adder cell has no direct path with the ground. Because of nonexistence of ground path it reduces power consumption.

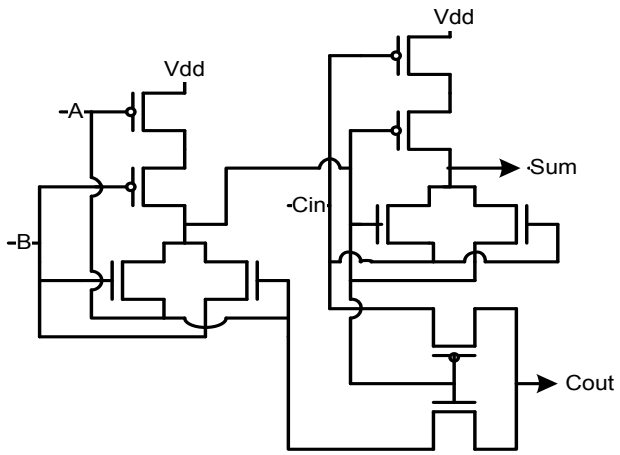

Fig.3. SERF Adder Cell (10T)

C. Gate Diffusion Input Full Adder Cell

The design of Gate Diffusion Input(GDI) full adder cell consists of two XOR/XNOR gates, GDI circuitimplemented in this paper consist of two XOR gates which are designed by using four transistors each as shown in Fig.4 [11, 12]. The GDI full adder cell requires ten transistors, which is very less in number as compared to conventional CMOS design and the speed is also more as compared conventional CMOS design. But in other hand GDI technique suffers from voltage swing degradation due to voltage loss problem and also the major problem of a GDI full adder cell is that it requires twin-well CMOS or Silicon On Insulator (SOI) process to construct it, so it will be more expensive to implement a GDI chip. If GDI uses only standard p-well CMOS process to implement it, the new problem arises that is decrease in driving capability which makes this process more expensive and also not easy to realize.

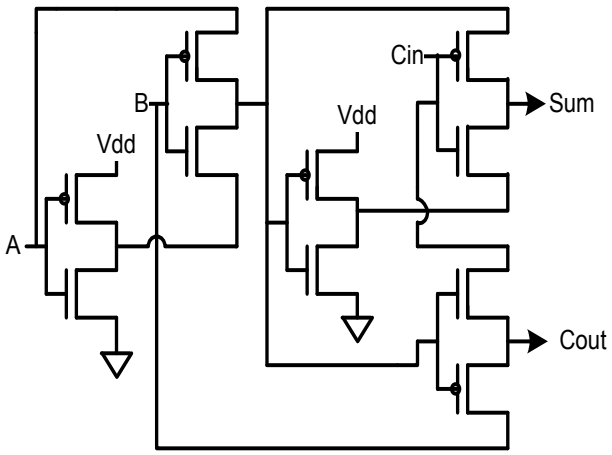

Fig.4. GDI full Adder Cell (10T)

III. PROPOSED WORK

After doing analysis of all existing full adder cells two new designs have been proposed, which is implemented with the help of ten transistors. The first proposed circuit is implemented by using XOR module shown in Fig.5, it uses two XOR module section and one inverter section. Each XOR module is made by using 4 CMOS transistor (2 NMOS & 2 PMOS).The only difference between first and second proposed adder cell is that the second adder cell is made with the help of two XNOR modules instead of using two XOR modules as shown in Fig 6. These two proposed circuits are giving better power and delay as compared with the existing 10T structure i.e. SERF and GDI. The problem with SERF and GDI one bit full adder is output voltage swing which is also present in proposed 1-bit adder cell but it has better performance (less delay), lesser power consumption and efficiently less power delay product.

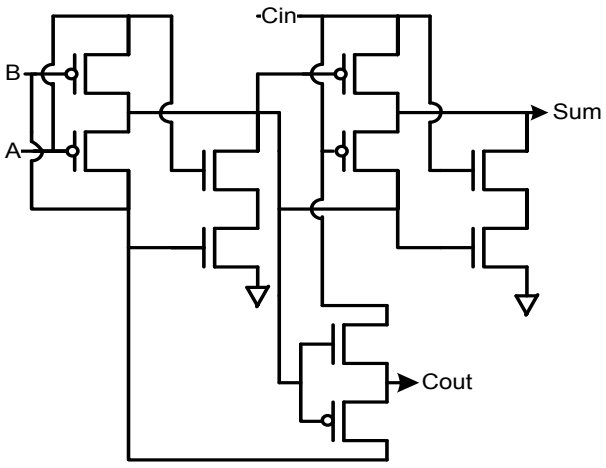

Fig.5. Proposed full adder cell using XOR module

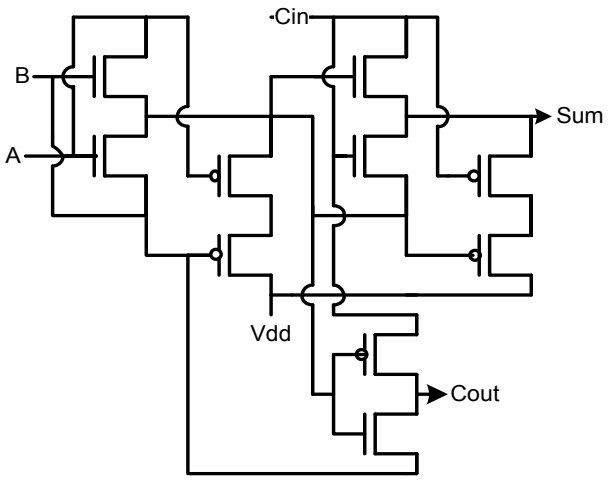

Fig.6. Proposed full adder cell using XNOR module

IV. RESULT AND SIMULATION

The simulation part which is performed of existing and proposed adder circuit at the same design parameters as shown in Table 2, it shows the calculation of average powerof the proposed adder along with the existing adders at room temperature (25°c) at different supply voltages on 100MHz frequency. These results are calculated by using Synopsys H-SPICE tool at 45nm MOSFET technology and it is clearly seen that the power consumption of the both proposed circuit is better than the existing SERF and GDI at the same numbers of transistors count i.e. 10-T.

Table II. Average power at different Vdd.

Parameter	Avg. Power (E-9W) at respective Vdd				
	1V	1.1V	1.2V	1.3V	1.4V
Conventional (28T)	10.63	13.52	17.10	27.27	112.2
SERF (10T)	11.81	14.92	19.51	42.52	311.5
GDI (10T)	59.73	278.3	778.6	1768	3771
Proposed1 (10T)	4.989	5.412	5.194	5.174	5.163
Proposed2 (10T)	4.157	5.152	6.518	23.46	274.8

Table 3 shows the variation in delay of proposed and existing adders at room temperature at different Vdd. It is found from table 3 the delays are more in GDI and SERF adderas compared to proposed adder circuits.

Table III. Average delay at different Vdd.

Parameter	Delay (E-11S) at respective Vdd				
	1V	1.1V	1.2V	1.3V	1.4V
Conventional (28T)	7.978	6.459	5.515	4.863	4.389
SERF (10T)	1.835	1.442	1.169	0.966	0.795
GDI (10T)	5.698	4.635	4.778	4.353	3.642
Proposed1 (10T)	2.315	2.459	2.459	2.740	2.949
Proposed2 (10T)	1.324	1.045	0.850	0.706	0.587

The proposed circuits have very less power delay product (PDP)as compared to existing SERF and GDI adder circuits, which is shown in Table 4.

Table IV.Power delay product at different Vdd.

Parameter	PDP(E-20J) at respective Vdd				
	1V	1.1V	1.2V	1.3V	1.4V
Conventional (28T)	84.84	87.34	94.33	132.6	492.8
SERF (10T)	21.67	21.52	22.83	41.09	247.8
GDI (10T)	138.3	1290	3720	7697	1373
Proposed1 (10T)	11.55	13.31	12.77	14.18	15.23
Proposed2 (10T)	5.506	5.384	5.543	16.57	161.3

At 1V operating voltage (Vdd) Conventional adder cell gives proper output voltage swing i.e. 1v at the both output (Sum, Cout) terminals of the adder cell that means in conventional adder cell no degradation of output voltage take place. But at Vdd 1v in SERF adder cell 0.635v output voltage swing take place and for GDI adder cell 0.66v output voltage swing take place, this output voltage degradation problem occur in both SERF and GDI adder cell which is not a desirable condition to operate these adder cell at low input voltage. In proposed adder cell by using XOR module at 1v Vdd 0.62v output voltage swing take place for the carry output (Cout), and in second proposed adder cell i.e. in XNOR module output voltage swing is 0.64v arise for carry output. The problem of degraded output voltage is also remain in the proposed adder cells which is clearly seen in transient analysis of proposed adder cell as shown in Fig.8 and Fig.9.

Fig.8 & Fig.9 shows the transient response of proposed full adder cell using XOR and XNOR modules simultaneously at 45nm CMOS technology.

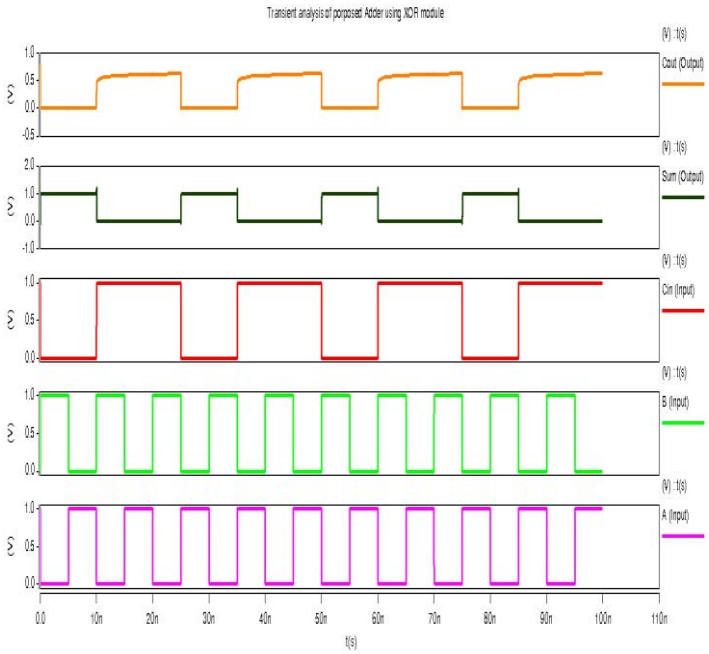

Fig. 8. Transient analysis of proposed one bit full adder cell using XOR module.

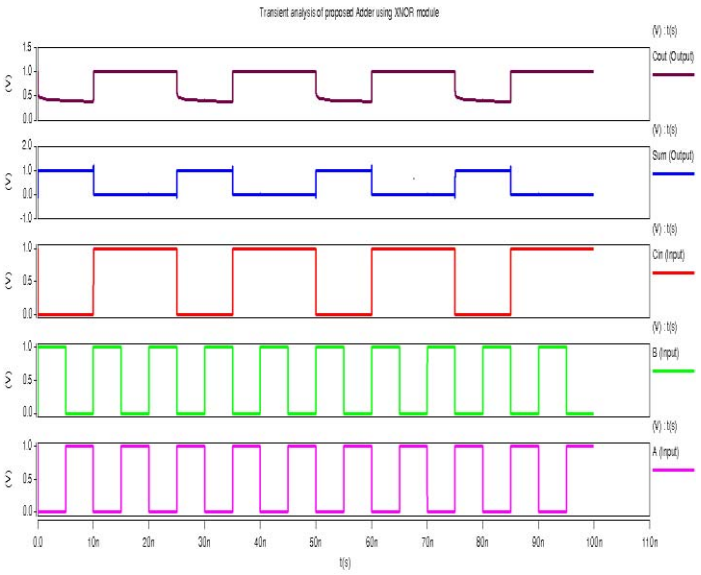

Fig. 9. Transient analysis of proposed one bit full adder cell using XNOR module.

V. CONCLUSION

In this paper, two new full adder circuits have been proposed and corresponding simulation results have been generated and then compared with existing adder circuits at 45nm CMOS technology using HSPICE tool. According to the simulationresults it is observed that the proposed designs have achieved maximum saving of power 91.65% and 93.04%, maximum reduction in delay 59.37% and 76.76% and maximum saving of PDP 91.64% and 96.01% when compared to the existing SERF and GDI adder respectively. The proposed circuits are also giving better performance at different supply voltage compare to existing adder circuits.

References

[1] M. Aguirre-Hernandez and M. Linares-Aranda, "CMOS full-adders for energy-efficient arithmetic applications," IEEE Transaction Very Large ScaleIntegration (VLSI) Syst., vol. 19, no. 4, pp. 718–721, Apr. 2011.

[2] M. Alioto, G. Di Cataldo, G. Palumbo, "Mixed full adder topologies for high-performance low-power arithmetic circuits," Microelectronics Journal, vol. 38, no. 1, pp. 130–139, Jan. 2007.

[3] R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic," IEEE Journal of Solid-State Circuits, vol. 32, no. 7, pp. 1079–1090, Jul. 1997.

[4] Hung Tien Bui, Yuke Wang, and Yingtao Jiang, "Design and Analysis of Low-Power 10-Transistor Full Adders Using Novel XOR–XNOR Gates," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol. 49, no 1, Jan. 2002.

[5] N. Zhuan, H. Wu, "A new design of the CMOS full adder," IEEE Journal Solid-State Circuits, vol. 27, no. 5, pp. 840–844, May 1992.

[6] C.-K. Tung, Y.-C. Hung, S.-H. Shieh, and G.-S. Huang," A low-power high-speed hybrid CMOS full adder for embedded system," IEEE Conference Design and Diagnostics of Electronic Circuits and Systems., vol. 13. pp. 1-4, Apr. 2007.

[7] Anandi, R. Rangarajan, M. Ramesh, "Power Efficient adder Cell For Low Power Bio Medical Devices," IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Vol. 4, Issue 2, Ver. III, pp 39-45 Mar-Apr. 2014.

[8] Mohanraj S, Maheswari M, "Power SERF and Modified SERF Adders for Ultra Low PowerDesign Techniques," International Conference on Communication Technology and System Design,2011.

[9] Deepa, Sampath Kumar V, "Analysis of Low Power 1-bit Adder Cells usingdifferent XOR-XNOR gates," IEEE International Conference on Computational Intelligence & Communication Technology, 2015.

[10] Jin-Fa Lin, Yin-Tsung Hwang, Ming-Hwa Sheu, "A Novel High-Speed and Energy Efficient10-Transistor Full Adder Design," IEEE Transactions on Circuits and Systems-I: Regular Papers, vol. 54, no. 5, May 2007.

[11] [11] Sujatha,Hiremath and Deepali Koppad, "Low Power Full Adder Circuit Using Gate Diffusion Input (GDI) MUX," Communication and Computing (ARTCom2012), Fourth International Conference on Advances in Recent Technologies, 19-20 Oct. 2012.

[12] Soolmaz Abbasalizadeh, Behjat Forouzandeh, "Full Adder Design with GDI Cell and IndependentDouble Gate Transistor," 20th Iranian Conference on Electrical Engineering, (ICEE2012), Tehran, Iran, May 15-17, 2012.

[13] Yingtao Jiang, Abdulkarim Al-Sheraidah, Yuke Wang, Edwin Sha, and Jin-Gyun Chung, "A Novel Multiplexer-Based Low-Power Full Adder," IEEE Transactions on Circuits and Systems-II: Express BRIEFS, vol. 51, no. 7, July 2004.

[14] I. S. Abu-Khater, A. Bellaouar, M. I. Elmasry, “Circuit techniques for CMOS low-power high-performance multipliers,” IEEEJournal Solid-State Circuits, vol. 31, no. 10, pp. 1535–1546, Oct. 1996.

[15] Arvind Nigam, Raghvendra Singh, “Comparative Analysis of 28T Full adder with 14T Full adder using 180nm,” International Journal of Engineering Science Advance Research;2(1), pp.27-32, March 2016.

[16] Anuj Kumar Shrivastava, Shyam Akashe,” Design High performance and Low Power 10T Full Adder Cell Using Double Gate MOSFET at 45nm Technology,” International Conference on Control, Computing, Communication and Materials (ICCCCM), 2013

[17] Sneh Lata Murotiya, Anu Gupta, “Design of high speed ternary full adder and three input XOR circuits using CNTFETs,” 28th International Conference on VLSI Design and 14th International Conference on Embedded Systems, 2015

[18] Partha Bhattacharyya, Bijoy Kundu, Sovan Ghosh, Vinay Kumar,” Performance Analysis of a Low-Power High-Speed Hybrid 1-bit Full Adder Circuit,” IEEE Transactions on Very Large scale Integration (VLSI) Systems, vol. 24, no. 11, Non. 2015.

[19] Yavar Safaei Mehrabani, Mohammad Eshghi, ”Noise and Process Variation Tolerant, Low-Power, High-Speed, and Low-Energy Full Adders in CNFET Technology”, IEEE Transactions on Very Large scale Integration (VLSI) Systems, vol. 24, no. 11, Nov. 2016.

[20] I. Hassoune, D. Flandre, I. O’Connor, and J. Legat, “ULPFA: A new efficient design of a power-aware full adder,” IEEE Transaction Circuits SystemI, Reg. Papers, vol. 57, no. 8, pp. 2066–2074, Aug. 2010.

[21] Ashok Kumar, Magdy A,” Design of Robust, Energy-Efficient Full Adders for Deep-Sub micrometer Design Using Hybrid-CMOS Logic Style,” IEEE Transactions on Very Large scale Integration (VLSI) Systems, vol.14, no.12, December2006.