Technical Reference Manual for the Pixel Array Control Monitor and Network (PACMAN) Card

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1 Introduction

The Pixel Array Control Monitor and Network (PACMAN) card is the warm electronics (located outside of the cryostat) for the pixellated liquid argon (LAr) time projection chamber (TPC) based on the LArPix ASIC. The PACMAN card provides power and digital I/O to arrays of LArPix ASICs hosted on pixel tile cards located within the cryostat. In the production system, each PACMAN card handles up to ten pixel tile cards. The PACMAN card provides analog test and monitor signals as well as digital control signals for clock, exernal trigger, and reset, and sync. The PACMAN card serves as a timing system end point, hosts a linux CPU, and is connected to the data acquisition system via ethernet.

The PACMAN card plays a supporting role in the LArPix system. It does not face technical challenges as severe as the cold electronics of the LArPix system and therefore a basic design constraint is that it in no way limits the performance of the supported system.

2 Prototype Results

Many of the specifications for the PACMAN are driven by measurements, using prototype devices, as described in this section.

The Intrinsic RMS noise on the LArPix ASIC was benchtested[1] at ~ 3 mV.

The PACMAN card provides digital (VDDD) and analog (VDDA) power for the LArPix ASICs. The ASIC power draw during power up was measured[2] as follows:

Table 1: ASIC Current Draw at Power-up

	Voltage (V)	Current (mA)	Power (mW)	Power (μW/chan)
VDDA	1.8	1.4	2.5	39
VDDD	1.8	6.92	12.5	195

[1] Reported 6 Mar 2020, Brooke

[2] Reported 13 Feb 2020, Brooke

The 10x10 pixel-tile power draw was measured [3] as follows:

Table 2: 10x10 Power Draw

	Voltage (V)	Current (mA)	Power (W)
VDDA	1.8	166	0.3
VDDD	1.8	611	1.1

3 Specifications for the PACMAN Card

3.1 Overview

Each PACMAN card provides power, digital I/O, and analog test and monitoring signals to up to ten pixel tile cards. Each pixel tile card will consist of 160 ASICs.

3.2 Power

The PACMAN card provides digital and analog power to up to ten pixel tile cards. The digital voltage level (VDDD) and analog voltage level (VDDA) are digitally controlled independently for each pixel tile card, within the limits and at the stability specified below.

The power requirements of the PACMAN are based on scaling the measured power consumption of the 100 ASIC pixel tile cards to 160 ASIC pixel tile cards of the production system, a scale factor of 1.6. An additional (minimum) safety factor of 10% is added to these extrapolated power requirements to derive the following specifications:

Table 3: Digital and Analog Power Requirements (per tile card)

	Stability	Min (V)	Max (V)	Max Current (A)	Max Power (W)
VDDA	1%	0	1.8	0.3	0.7
VDDD	1%	0	1.8	1.1	2.2

Reaching a 1% stability on VDDA and VDDD requires linear regulation and so the power requirements at the input of the PACMAN are derived from a higher voltage level of 3 V. This implies that the initial switching voltage requirement must provide at least 42 W at 3 V.

The PACMAN power is provided by a single nominal 48 V 2 A DC input. The power connection is the four position terminal connector (Phenoix Contact P/N 5444660). The inner two pins provide power and the outer two are for sense:

Table 4: Input Power Connections

pin	function
1	V+ sense
2	V+
3	V-
4	V- sense

The connector is rated for 8 A and 300 V. The PACMAN is fused at 2.5 A and has over voltage protection at 60 V. The sense pins are fused at 0.5 A.

[3] Reported 14 Jan 2021, Brooke

3.3 Digital Signals

The LArPix-v2 ASIC uses a bit-serial protocol to transmit and receive data. The PACMAN is the primary and the LARPix ASIC the secondary, so that the PACMAN transmits POSI and receives PISO signals.

The PACMAN shall provide the following digital IO signals to each pixel tile card:

Table 5: Digital Signals (per pixel tile card)

Signal	Quantity	Description
POSI	4	Bit serial transmission to pixel tile
PISO	4	Bit serial reception from pixel tile
CLK	1	Clock
TRIG	1	Trigger
SYNC	1	Multiplexed Synchronization and Reset

Each POSI signal is received by a single ASIC, but the clock, trigger, and sync signals are fanned out to every ASIC on the tile card. The PACMAN must be capable of driving the resulting capacitive load.

The nominal clock rate is 10 MHz with a maximum of 40 MHz. The LArPix ASIC uses an LVDS signal with custom voltage level which the PACMAN is capable of transmitting and receiving.

3.4 Noise

The noise injected into the pixel tile from the controller is less than 1 mV.

3.5 Pixel Tile Interface

A single PACMAN card drive up to ten pixel tile cards through a single flange card. The interface to the eight-tile flange card is through a 6 row by 50 pin high-desnity SAMTEC connector `SEAF-50-01-L-06-1-RA-K-TR` on the PACMAN card.

The PACMAN card shall provide a footprint for an optional 2x17 connector to drive a pixel card directly without the use of flange card.

3.6 Front Panel Interface

The PACMAN card implements the front-panel interfaces listed below in the specified quantity with specified routing. When routing to programmable logic (PL) is specified, the specified purpose is nominal and can be repurposed through firmware changes.

Table 6: Required Front Panel Interface

Interface	Quantity	Routing
SMA Jack	1	Multiplexed to eight tile analog monitor
SMA Jack	1	Multiplexed to eight tile adc test
Lemo Jack	2	PL: Trigger and Sync
Push Button	1	Reset
LED	4	PL: General Purpose

3.7 Timing System Endpoint

The PACMAN card implement a ProtoDUNE-SP timing system endpoint[4] of a single fiber-optic link.

3.8 Embedded Linux

The PACMAN is an embedded Linux system and supports several standard embedded Linux interfaces:

Interface	P/N	Notes
Ethernet		Gigabit
SD Card		Bootable from SD card
JTAG		SoC Configuration
UART		Linux Terminal

The JTAG and UART interface are multiplexed to provide a linux terminal and firmware configuration over a single USB port.

[4]DUNE-doc-1651-v3

A PACMAN Evolution

Table 7: PACMAN Evolution

Card	Designer	Date	Notes
PACMAN v1r1	Hillbrand	Feb 2020	Initial Prototype
PACMAN v1r2	Karcher	July 2020	Single-tile capable
PACMAN v1r3	Berns/Karcher	Jan 2021	Eight-tile capable - Module 0
PACMAN v2	Berns/Karcher	Feb 2022	LArPix-v2b, Power, TX
PACMAN v3	Berns/Karcher	TBD	Ten-tile capable