Technical Reference Manual for the Pixel Array Control Monitor and Network (Pac-Man) Card

May 20, 2021

1 Requirements for Demonstrator PACMAN

This section describes the requirements of the PACMAN card intended to drive the demonstrator systems through the ArgonCube 2x2 demonstrator.

1.1 Pixel Tile Interface

A single PACMAN card shall drive up to eight pixel tile cards through a single flange card. The interface to the eight-tile flange card used in demonstrator systems and subsequent pixel tile cards is through a single 6 row by 50 pin high-desnity SAMTEC connector `SEAF-50-01-L-06-1-RA-K-TR` on the PACMAN card.

The PACMAN card shall provide a footprint for an optional 2x17 connector to drive a pixel card directly without the use of flange card.

1.2 Front Panel Interface

The PACMAN card shall implement the following front panel interfaces in specified quantity with specified routing. When routing to programmable logic (PL) is specified, the specified purpose is nominal and can be repurposed through firmware changes.

Table 1: Required Front Panel Interface

Interface	Quantity	Routing
SMA Jack	1	Multiplexed to eight tile analog monitor
SMA Jack	1	Multiplexed to eight tile adc test
Lemo Jack	2	PL: Trigger and Sync
Push Button	1	Reset
LED	4	PL: General Purpose

1.3 Timing System Endpoint

The PACMAN card shall implement a ProtoDUNE-SP timing system endpoint[1] of a single fiber-optic link. The simplest hardware implementation of such an endpoint includes a PIN diode (photodetector), transimpedance amplifier, and a clock and data recovery IC such as ADN2814.

[1] DUNE-doc-1651-v3

1.4 Linux System and Peripherals

The PACMAN card shall provide a linux host with system peripherals:

Table 2: Required Peripherals

	Notes
SD Card	Firmware, linux images, linux root filesytem
Ethernet	Gigabit
JTAG	Configure FPGA
UART	Linux terminal

1.5 Power Requirements

The PACMAN card shall provide digital and analog power to each pixel tile card. The digital voltage level (VDDD) and analog voltage level (VDDA) are digitally controlled independently for each pixel tile, within the limits and at the stability specified below.

Table 3: Digital and Analog Power Requirements

	Stability	Min (V)	Max (V)	Max Current (A)	Max Power (W)
VDDA	1%	0	1.8	0.5	0.9
VDDD	1%	0	1.8	1	1.8 W

1.6 Digital Signals

The LArPix-v2 ASIC uses a bit-serial protocol to transmit and receive data. The PACMAN is the primary and the LARPix ASIC the secondary, so that the PACMAN transmits POSI and receives PISO signals.

The PACMAN shall provide the following digital IO signals to each pixel tile card:

Table 4: Digital and Analog Power Requirements

Signal	Quantity	Description
POSI	4	Bit serial transmission to pixel tile
PISO	4	Bit serial reception from pixel tile
CLK	1	Clock
TRIG	1	Trigger
SYNC	1	Multiplexed Synchronization and Reset

Each POSI signal is received by a single ASIC, but the clock, trigger, and sync signals are fanned out to every ASIC on the tile card. The PACMAN must be capable of driving the resulting capacitive load (XXX pF) with XXX.

The nominal clock rate is 10 MHz with a maximum 40 MHz.

The LArPix-v2 ASIC uses an LVDS-like pseudo-differential CMOS signal which the PACMAN shall be capable of transmitting and receiving.

1.7 Noise

The noise injected into the pixel tile from the controller shall be less than 1 mV.

1.8 Monitoring

2 Test-Bench Results

2.1 Power

Benchtests[2] of ASIC power drawer during power up.

Table 5: ASIC Current Draw at Power-up

	Voltage (V)	Current (mA)	Power (mW)	Power (μW/chan)
VDDA	1.8	1.4	2.5	39
VDDD	1.8	6.92	12.5	195

Benchtests[3] of 10x10 pixel-tile power draw:

Table 6: 10x10 Power Draw

	Voltage (V)	Current (mA)	Power (W)
VDDA	1.8	166	0.3
VDDD	1.8	611	1.1

When driving the 10x10 tile, the PACMAN v1r3 drew 611 mA through the LT3045 with nominal limit of 500 mA. When driving eight tiles the XXXX was overpowered. To drive eight pixel tiles with PACMAN v1r3, VDDD was reduced to 1.6 V on v1r3, and one 2 A regulator was bypassed. In this configuration, PACMAN draws 1.4 A from the supplies.

2.2 Low-Noise Requirements

Intrinsic RMS noise on ASIC was benchtested[4] at ~ 3 mV.

[2]Reported 13 Feb 2020, Brooke
[3]Reported 14 Jan 2021, Brooke
[4]Reported 6 Mar 2020, Brooke

A PACMAN Evolution

Table 7: PACMAN Evolution

Card	Designer	Data	Notes
PACMAN v1r1	Hillbrand	Feb 2020	Initial Prototype
PACMAN v1r2	Karcher	July 2020	Single-tile capable
PACMAN v1r3	Berns/Karcher	Jan 2021	Eight-tile capable - Module 0
PACMAN v2	Berns/Karcher	July 2021 (Est)	LArPix-v2b, Power, TX
PACMAN v3	Berns/Karcher	Feb 2022 (Est)	Ten-tile capable

B Trenz Connector Pinout

Logical	Trenz	Pin	Note
TILE6_POSI_0	B33_L7_P	JB2-12	EVAL
TILE6_POSI_1	B33_L7_N	JB2-14	EVAL
TILE6_POSI_2	B33_L8_P	JB2-16	EVAL
TILE6_POSI_3	B33_L8_N	JB2-18	EVAL
TILE6_PISO_0	B33_L11_P	JB2-22	EVAL
TILE6_PISO_1	B33_L11_N	JB2-24	EVAL
TILE6_PISO_2	B33_L12_P	JB2-26	EVAL
TILE6_PISO_3	B33_L12_N	JB2-28	EVAL
TILE7_POSI_0	B33_L17_P	JB2-32	
TILE7_POSI_1	B33_L17_N	JB2-34	
TILE7_POSI_2	B33_L18_P	JB2-36	
TILE7_POSI_3	B33_L18_N	JB2-38	
TILE7_PISO_0	B13_L7_P	JB2-42	
TILE7_PISO_1	B13_L7_N	JB2-44	
TILE7_PISO_2	B13_L8_P	JB2-46	
TILE7_PISO_3	B13_L8_N	JB2-48	
TILE4_POSI_0	B13_L11_P	JB2-52	
TILE4_POSI_1	B13_L11_N	JB2-54	
TILE4_POSI_2	B13_L9_P	JB2-56	
TILE4_POSI_3	B13_L9_N	JB2-58	
TILE4_PISO_0	B13_L20_P	JB2-62	
TILE4_PISO_1	B13_L20_N	JB2-64	
TILE4_PISO_2	B13_L17_P	JB2-66	
TILE4_PISO_3	B13_L17_N	JB2-68	
TILE1_POSI_0	B13_L16_P	JB2-72	
TILE1_POSI_1	B13_L16_N	JB2-74	
TILE1_POSI_2	B13_L18_P	JB2-76	
TILE1_POSI_3	B13_L18_N	JB2-78	
TILE1_PISO_0	B13_L15_P	JB2-82	
TILE1_PISO_1	B13_L15_N	JB2-84	
TILE1_PISO_2	B13_L21_P	JB2-86	
TILE1_PISO_3	B13_L21_N	JB2-88	

Logical	Trenz	Pin	Note
TILE3_POSI_3	B33_L13_P	JB2-21	
TILE3_POSI_2	B33_L13_N	JB2-23	
TILE3_POSI_1	B33_L14_P	JB2-25	
TILE3_POSI_0	B33_L14_N	JB2-27	
TILE3_PISO_3	B13_L5_P	JB2-31	
TILE3_PISO_2	B13_L5_N	JB2-33	
TILE3_PISO_1	B13_L6_P	JB2-35	
TILE3_PISO_0	B13_L6_N	JB2-37	
TILE2_POSI_3	B13_L1_P	JB2-41	
TILE2_POSI_2	B13_L1_N	JB2-43	
TILE2_POSI_1	B13_L12_P	JB2-45	
TILE2_POSI_0	B13_L12_N	JB2-47	
TILE2_PISO_3	B13_L14_P	JB2-51	
TILE2_PISO_2	B13_L14_N	JB2-53	
TILE2_PISO_1	B13_L13_P	JB2-55	
TILE2_PISO_0	B13_L13_N	JB2-57	
TILE5_POSI_3	B13_L4_P	JB2-61	
TILE5_POSI_2	B13_L4_N	JB2-63	
TILE5_POSI_1	B13_L3_P	JB2-65	
TILE5_POSI_0	B13_L3_N	JB2-67	
TILE5_PISO_3	B13_L10_P	JB2-71	
TILE5_PISO_2	B13_L10_N	JB2-73	
TILE5_PISO_1	B13_L2_P	JB2-75	
TILE5_PISO_0	B13_L2_N	JB2-77	
TILE8_POSI_3	B13_L23_P	JB2-81	
TILE8_POSI_2	B13_L23_N	JB2-83	
TILE8_POSI_1	B13_L24_P	JB2-85	
TILE8_POSI_0	B13_L24_N	JB2-87	
TILE8_PISO_3	B13_L19_P	JB2-91	
TILE8_PISO_2	B13_L19_N	JB2-93	
TILE8_PISO_1	B13_L22_P	JB2-95	
TILE8_PISO_0	B13_L22_N	JB2-97	

Logical	Trenz	Pin	Note
TILE6_SYNC_DN	B35_L16_N	JB1-32	EVAL
TILE6_SYNC_DP	B35_L16_P	JB1-34	EVAL
TILE6_TRIG_DN	B35_L24_N	JB1-36	EVAL
TILE6_TRIG_DP	B35_L24_P	JB1-38	EVAL
TILE6_CLK_DN	B35_L18_N	JB1-42	EVAL
TILE6_CLK_DP	B35_L18_P	JB1-44	EVAL
TILE7_SYNC_DN	B35_L15_N	JB1-46	
TILE7_SYNC_DP	B35_L15_P	JB1-48	
TILE7_TRIG_DN	B35_L22_N	JB1-50	
TILE7_TRIG_DP	B35_L22_P	JB1-52	
TILE7_CLK_DN	B35_L17_N	JB1-56	
TILE7_CLK_DP	B35_L17_P	JB1-58	
TILE4_SYNC_DN	B35_L13_N	JB1-60	
TILE4_SYNC_DP	B35_L13_P	JB1-62	
TILE4_TRIG_DN	B35_L14_N	JB1-66	
TILE4_TRIG_DP	B35_L14_P	JB1-68	
TILE4_CLK_DN	B35_L4_N	JB1-70	
TILE4_CLK_DP	B35_L4_P	JB1-72	
TILE1_SYNC_DN	B35_L12_N	JB1-76	
TILE1_SYNC_DP	B35_L12_P	JB1-78	
TILE1_TRIG_DN	B35_L20_N	JB1-82	
TILE1_TRIG_DP	B35_L20_P	JB1-84	
TILE1_CLK_DN	B35_L19_N	JB1-97	non-contiguous
TILE1_CLK_DP	B35_L19_P	JB1-99	non-contiguous
TILE3_CLK_DN	B35_L10_N	JB1-35	
TILE3_CLK_DP	B35_L10_P	JB1-37	
TILE3_TRIG_DN	B35_L9_N	JB1-39	
TILE3_TRIG_DP	B35_L9_P	JB1-41	
TILE3_SYNC_DN	B35_L7_N	JB1-45	
TILE3_SYNC_DP	B35_L7_P	JB1-47	
TILE2_CLK_DN	B35_L2_N	JB1-49	
TILE2_CLK_DP	B35_L2_P	JB1-51	
TILE2_TRIG_DN	B35_L8_N	JB1-55	
TILE2_TRIG_DP	B35_L8_P	JB1-57	
TILE2_SYNC_DN	B35_L21_N	JB1-59	
TILE2_SYNC_DP	B35_L21_P	JB1-61	
TILE5_CLK_DN	B35_L11_N	JB1-65	
TILE5_CLK_DP	B35_L11_P	JB1-67	
TILE5_TRIG_DN	B35_L23_N	JB1-69	
TILE5_TRIG_DP	B35_L23_P	JB1-71	
TILE5_SYNC_DN	B35_L5_N	JB1-75	
TILE5_SYNC_DP	B35_L5_P	JB1-77	
TILE8_CLK_DN	B35_L3_N	JB1-79	
TILE8_CLK_DP	B35_L3_P	JB1-81	
TILE8_TRIG_DN	B35_L6_N	JB1-85	
TILE8_TRIG_DP	B35_L6_P	JB1-87	
TILE8_SYNC_DN	B35_L1_N	JB1-93	
TILE8_SYNC_DP	B35_L1_P	JB1-95	

Logical	Trenz	Pin	Note
TILE1_EN	B34_L1_P	JB3-7	
TILE4_EN	B34_L1_N	JB3-9	
TILE7_EN	B34_L18_P	JB3-13	
TILE6_EN	B34_L18_N	JB3-15	
TILE3_EN	B34_L20_P	JB3-19	
TILE2_EN	B34_L20_N	JB3-21	
TILE5_EN	B34_L10_P	JB3-25	
TILE8_EN	B34_L10_N	JB3-27	

Logical	Trenz	Package Pin
SCL-1	MIO10	
SDA-1	MIO11	
SCL-LOOPBACK	B34_L8_P	
SDA-LOOPBACK	B34_L8_N	
SCL-2	B34_L9_P	
SDA-2	B34_L9_N	
LED	MIO12	
LED	MIO13	
LED	B34_L22_P	
LED	B34_L22_N	
ANALOG_PWR_EN	B34_L2_P	JB3-14
TRIG_ISO	B34_L7_P	JB3-8
SYNC_ISO	B34_L7_N	JB3-10
CLK	TBD	
TRIG	TBD	
SYNC	TBD	