

ATLAS MUCTPI  
Serial Link Test Report  
January 25, 2018

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# **Chapter 1**

## **6.4 Gbps**

## 1.1 MSP\_A TX1 MSP\_C RX16 Minipod Loopback

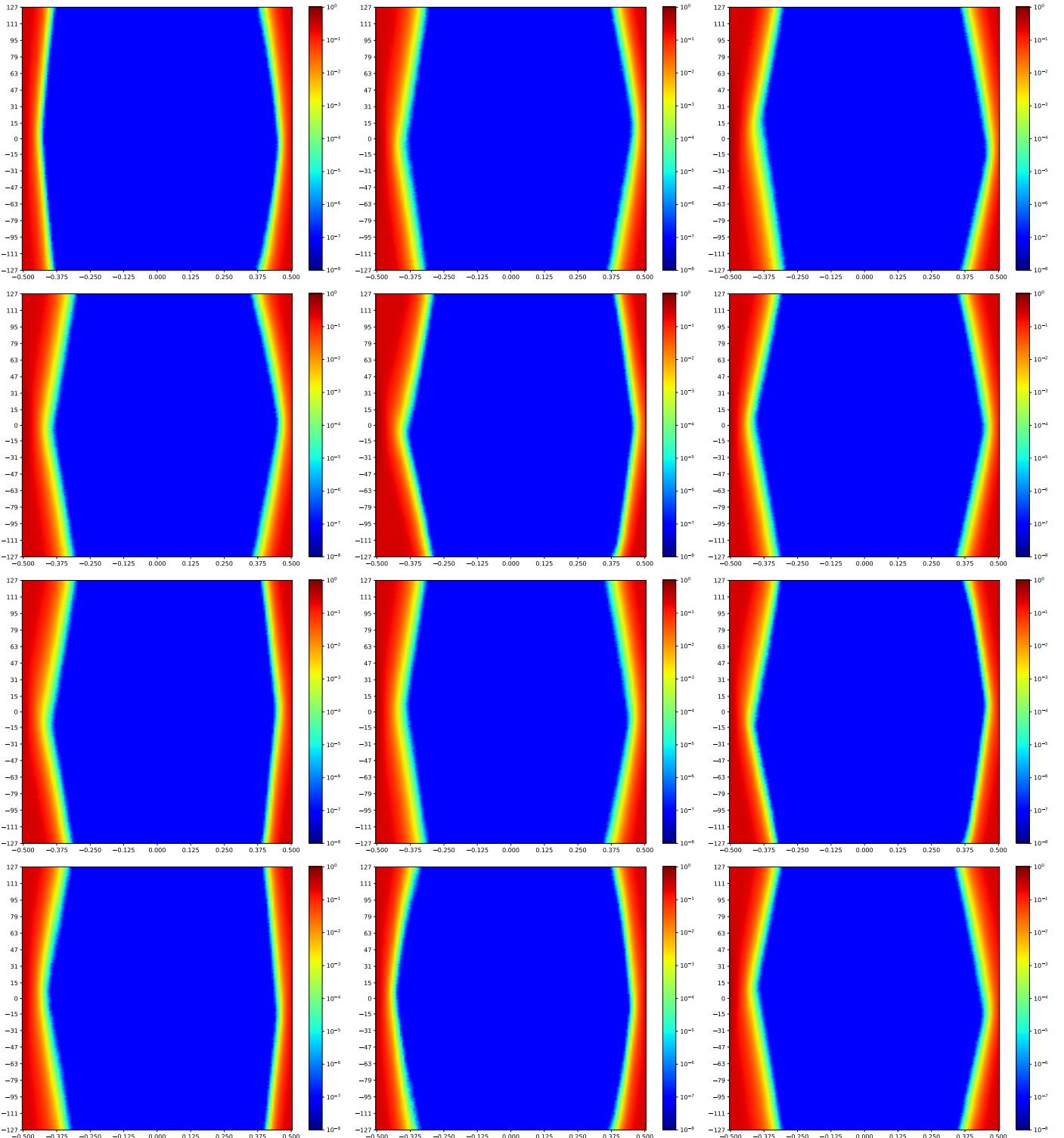


Figure 1.1: MSP\_A TX1 MSP\_C RX16 Minipod Loopback

A cross-reference to Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.14.

### 1.1.1 MSP\_A\_FPGA-TX1-00-RX16-00-MSP\_C\_FPGA

Table 1.1: MSP\_A\_FPGA-TX1-00-RX16-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:01:44		2018-Jan-24 03:02:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26480	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

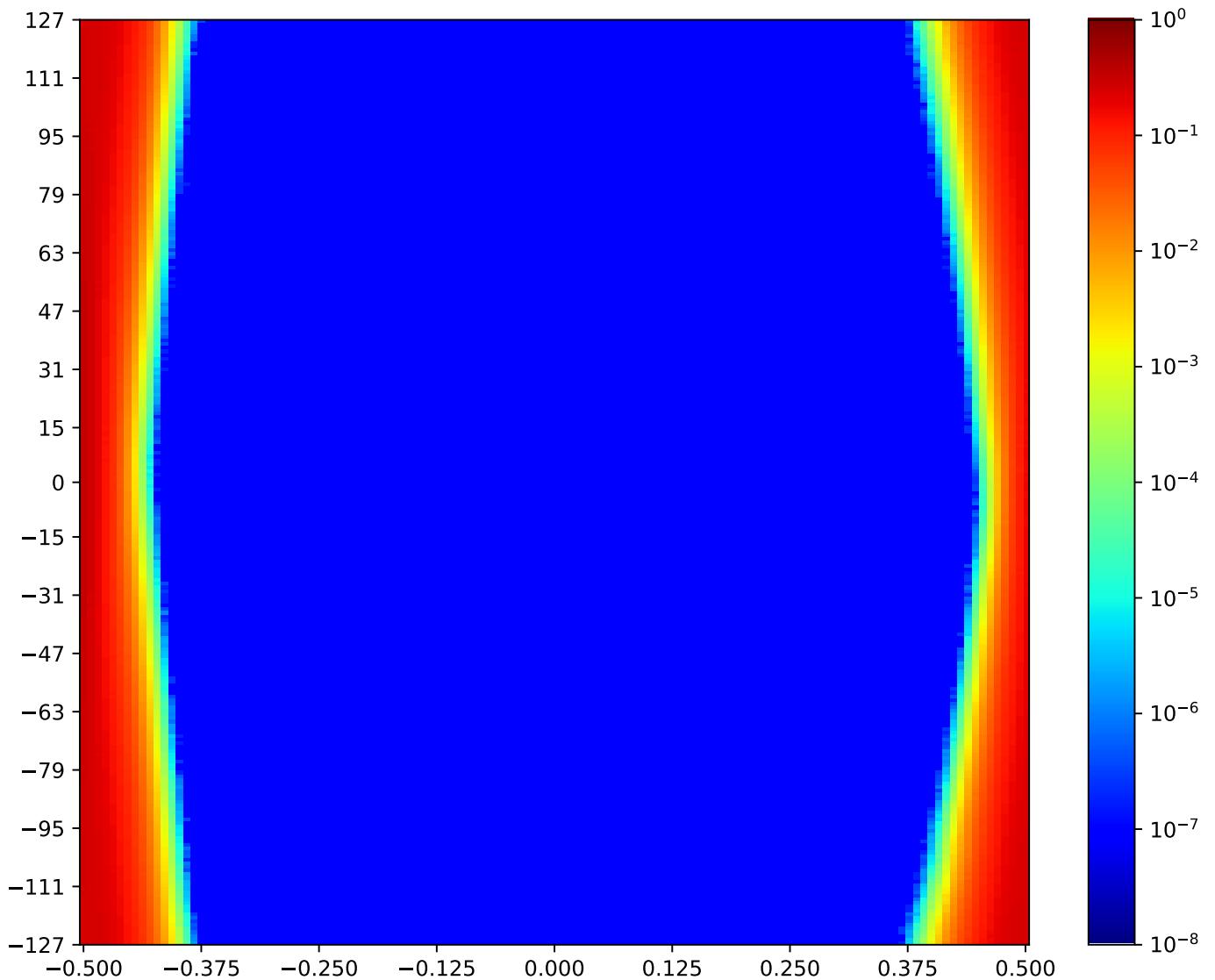


Figure 1.2: MSP\_A\_FPGA-TX1-00-RX16-00-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.2 MSP\_A\_FPGA-TX1-01-RX16-01-MSP\_C\_FPGA

Table 1.2: MSP\_A\_FPGA-TX1-01-RX16-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:04:07		2018-Jan-24 03:05:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24136	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

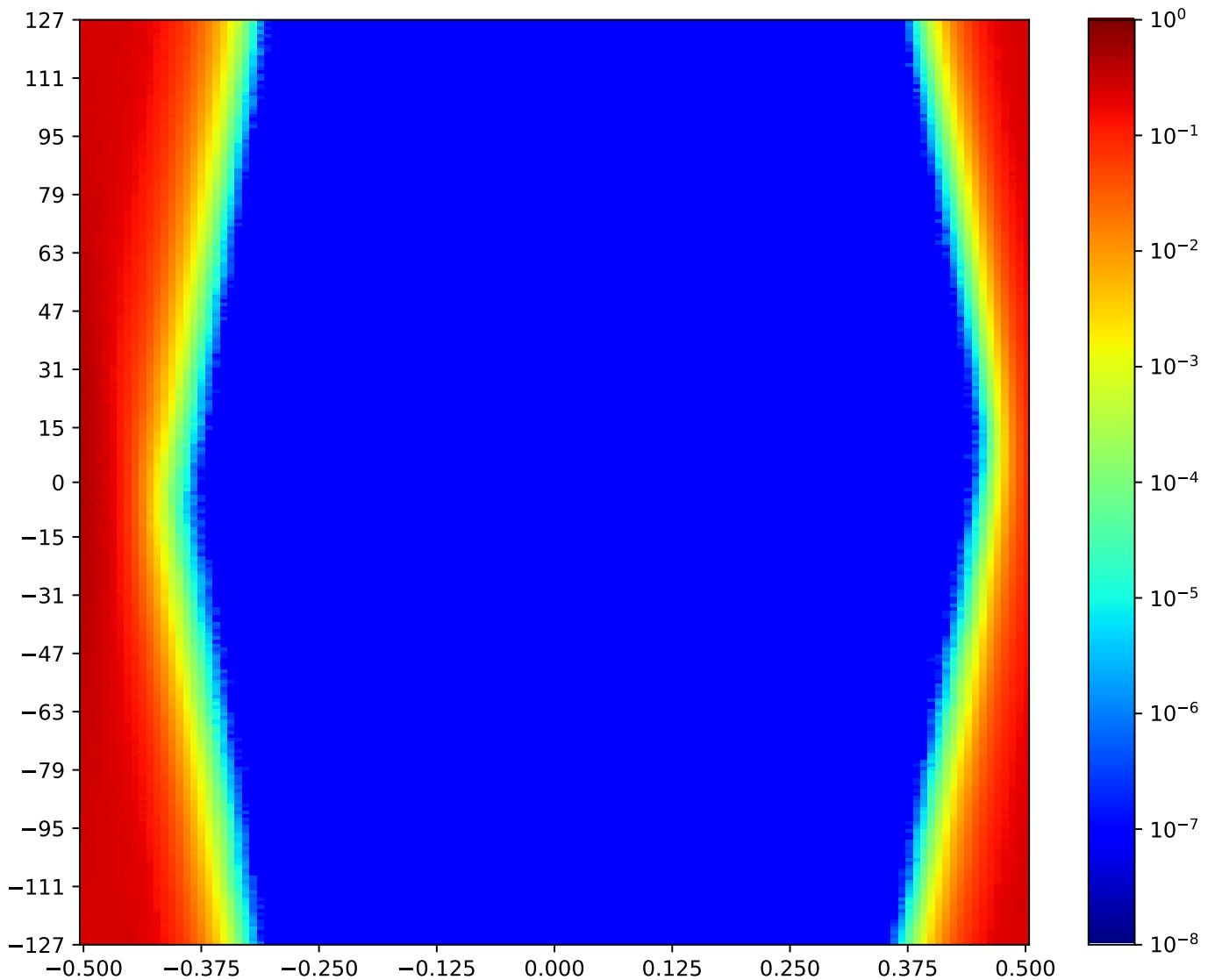


Figure 1.3: MSP\_A\_FPGA-TX1-01-RX16-01-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.3 MSP\_A\_FPGA-TX1-02-RX16-02-MSP\_C\_FPGA

Table 1.3: MSP\_A\_FPGA-TX1-02-RX16-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:05:16		2018-Jan-24 03:06:25	
Reset RX	OA	HO		HO (%)	
true	23799	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

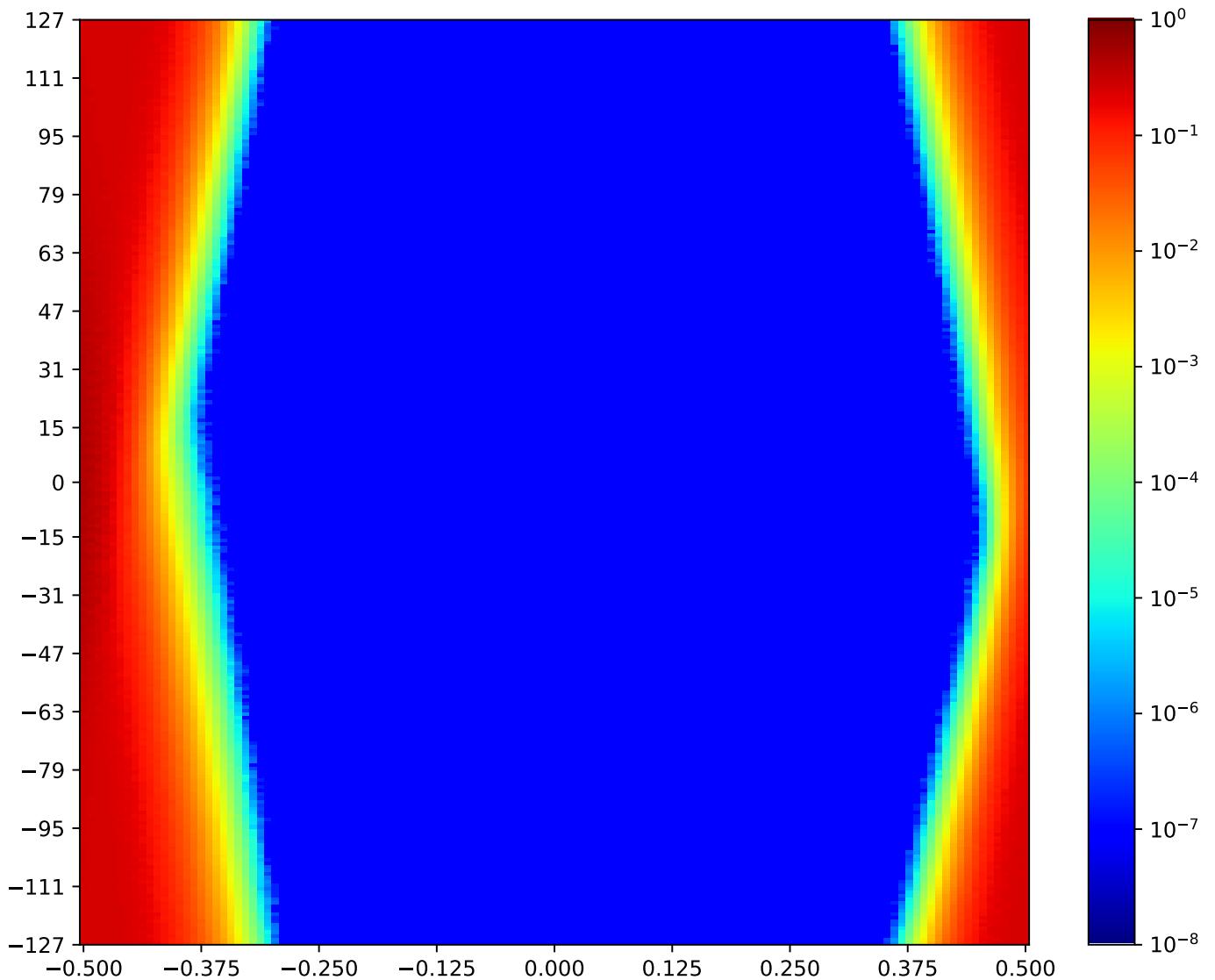


Figure 1.4: MSP\_A\_FPGA-TX1-02-RX16-02-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.1.4 MSP\_A\_FPGA-TX1-03-RX16-03-MSP\_C\_FPGA

Table 1.4: MSP\_A\_FPGA-TX1-03-RX16-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 02:59:26		2018-Jan-24 03:00:35	
Reset RX	OA	HO		HO (%)	
true	23900	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

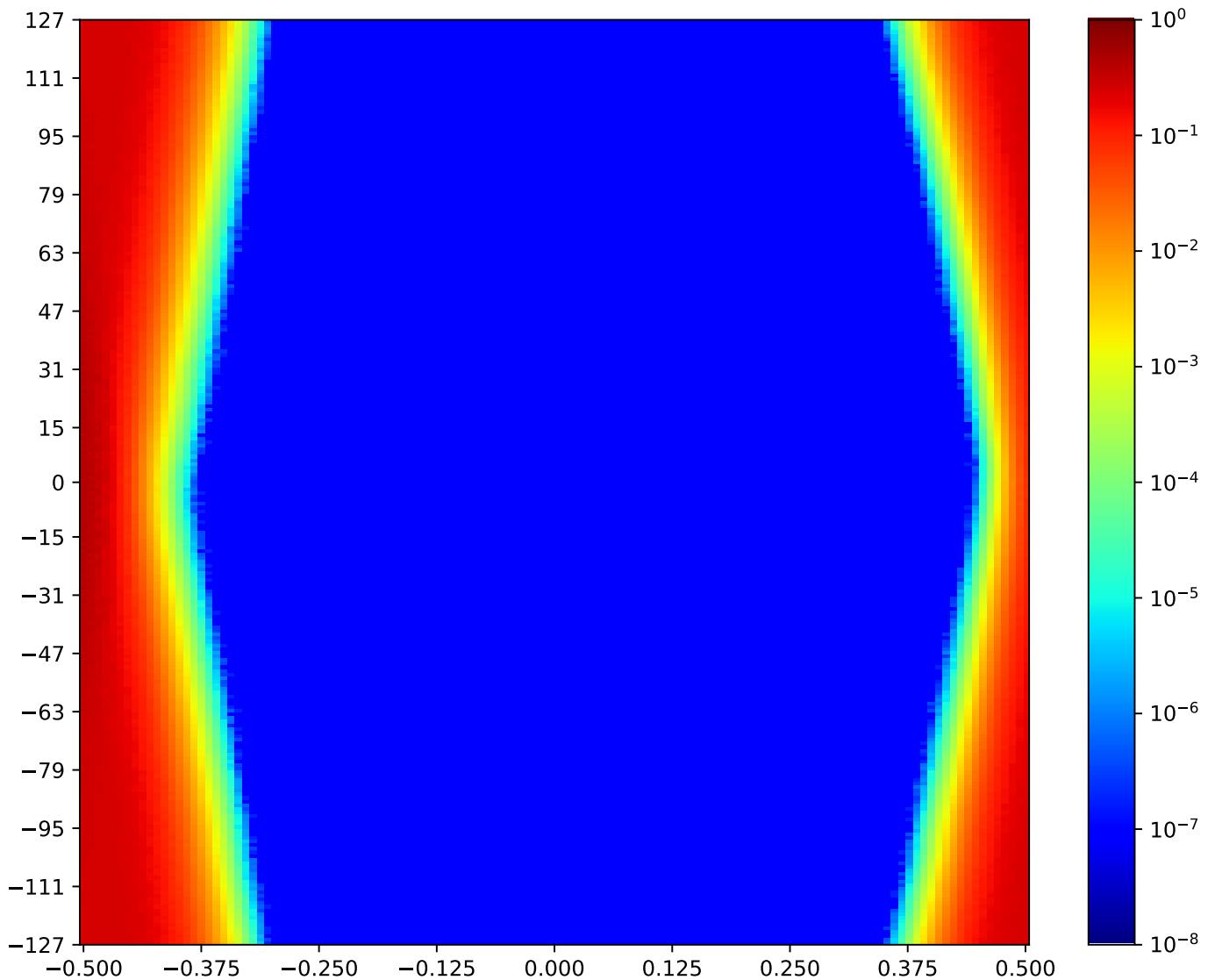


Figure 1.5: MSP\_A\_FPGA-TX1-03-RX16-03-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.5 MSP\_A\_FPGA-TX1-04-RX16-04-MSP\_C\_FPGA

Table 1.5: MSP\_A\_FPGA-TX1-04-RX16-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:08:45		2018-Jan-24 03:09:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24095	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

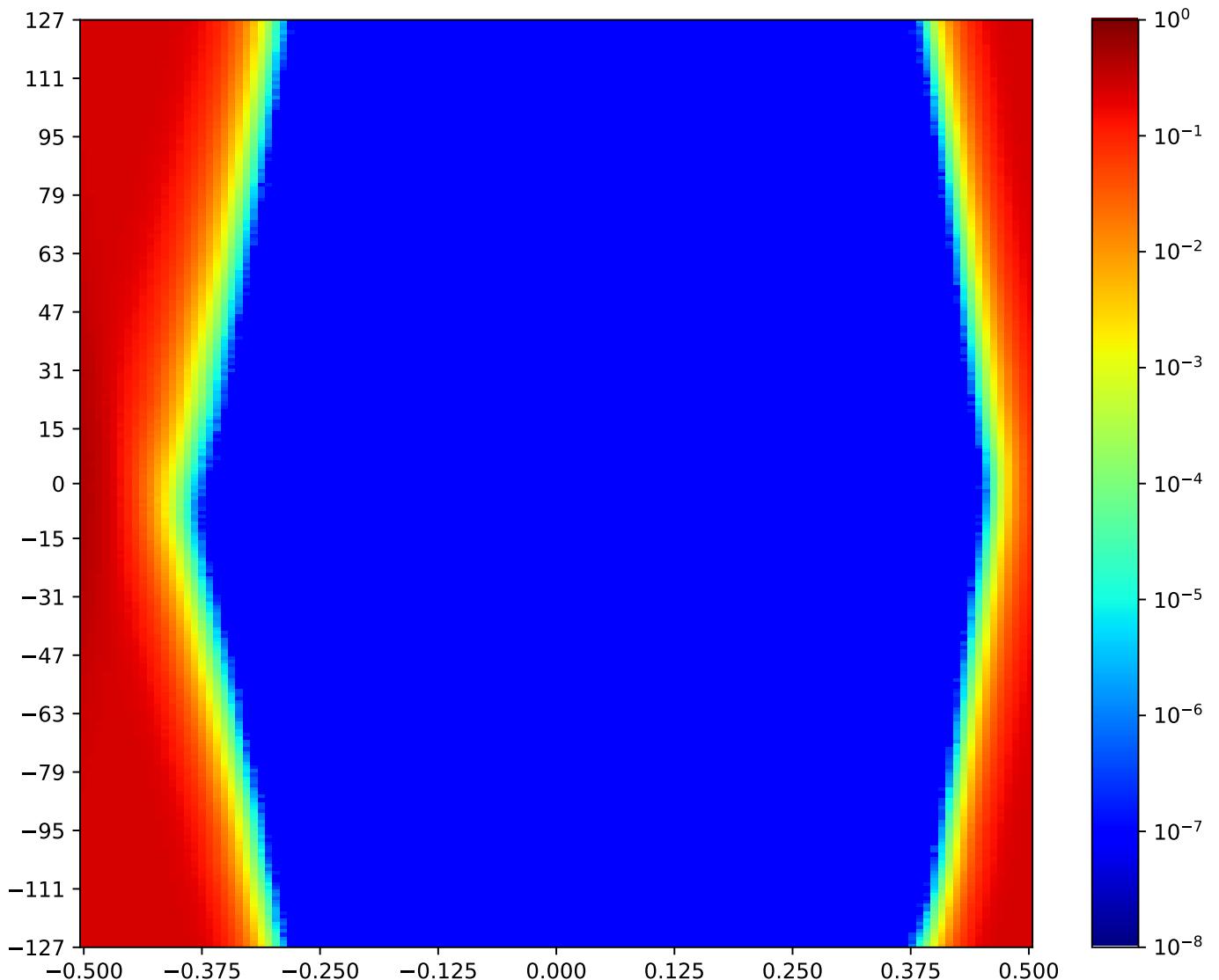


Figure 1.6: MSP\_A\_FPGA-TX1-04-RX16-04-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.6 MSP\_A\_FPGA-TX1-05-RX16-05-MSP\_C\_FPGA

Table 1.6: MSP\_A\_FPGA-TX1-05-RX16-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 02:58:17		2018-Jan-24 02:59:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24014	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

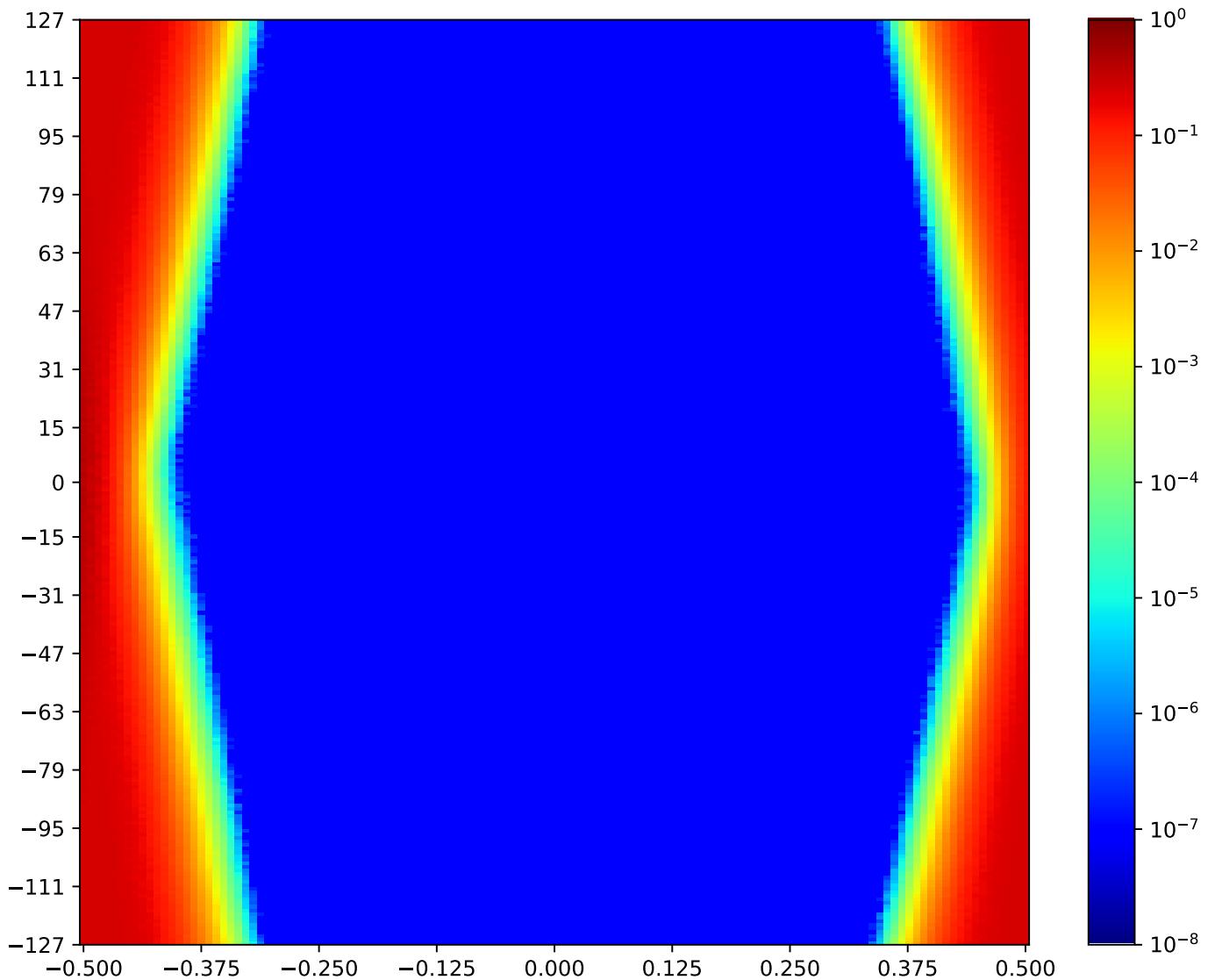


Figure 1.7: MSP\_A\_FPGA-TX1-05-RX16-05-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.7 MSP\_A\_FPGA-TX1-06-RX16-06-MSP\_C\_FPGA

Table 1.7: MSP\_A\_FPGA-TX1-06-RX16-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:11:04		2018-Jan-24 03:12:14	
Reset RX	OA	HO		HO (%)	
true	24471	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

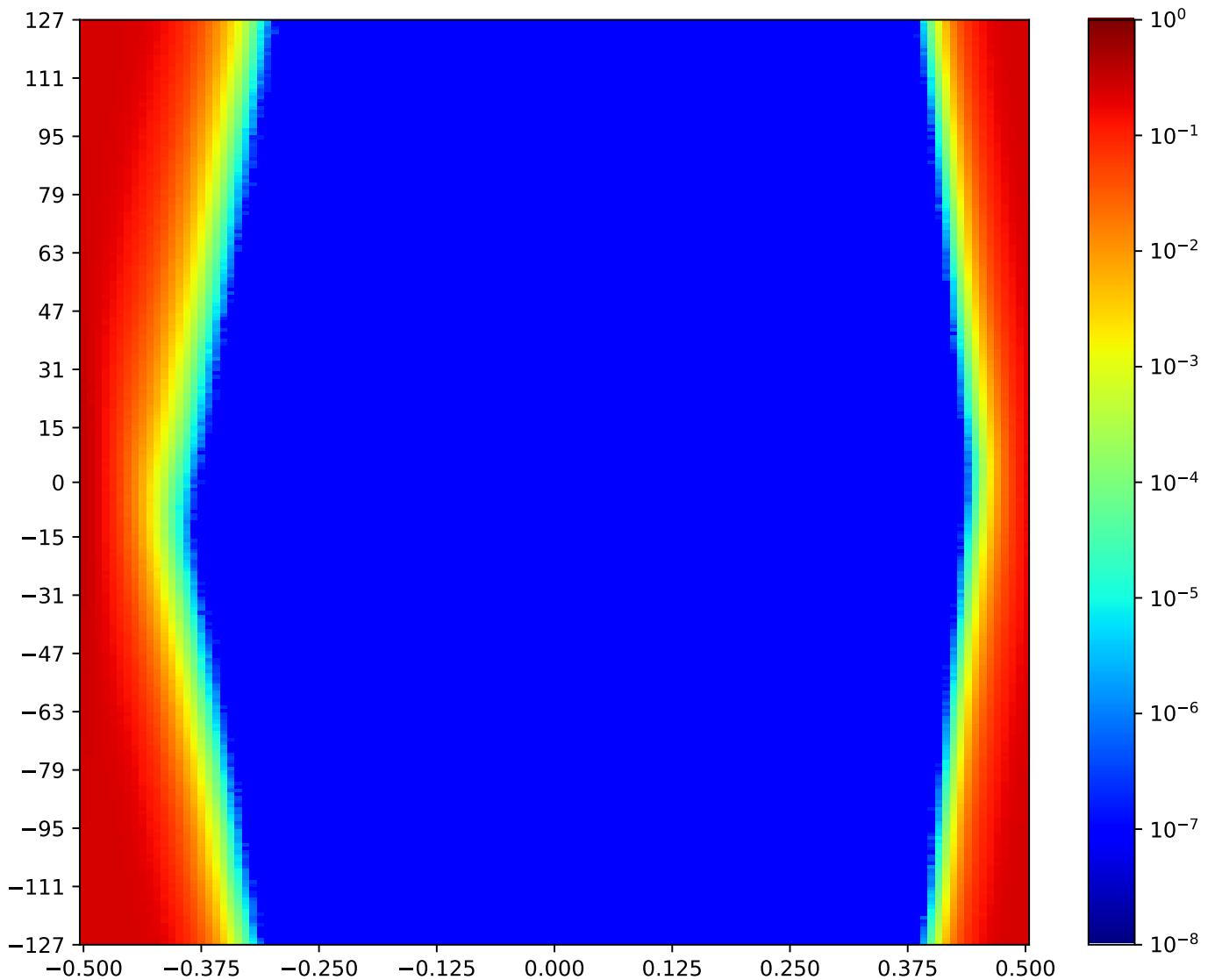


Figure 1.8: MSP\_A\_FPGA-TX1-06-RX16-06-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.8 MSP\_A\_FPGA-TX1-07-RX16-07-MSP\_C\_FPGA

Table 1.8: MSP\_A\_FPGA-TX1-07-RX16-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:00:35		2018-Jan-24 03:01:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23737	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

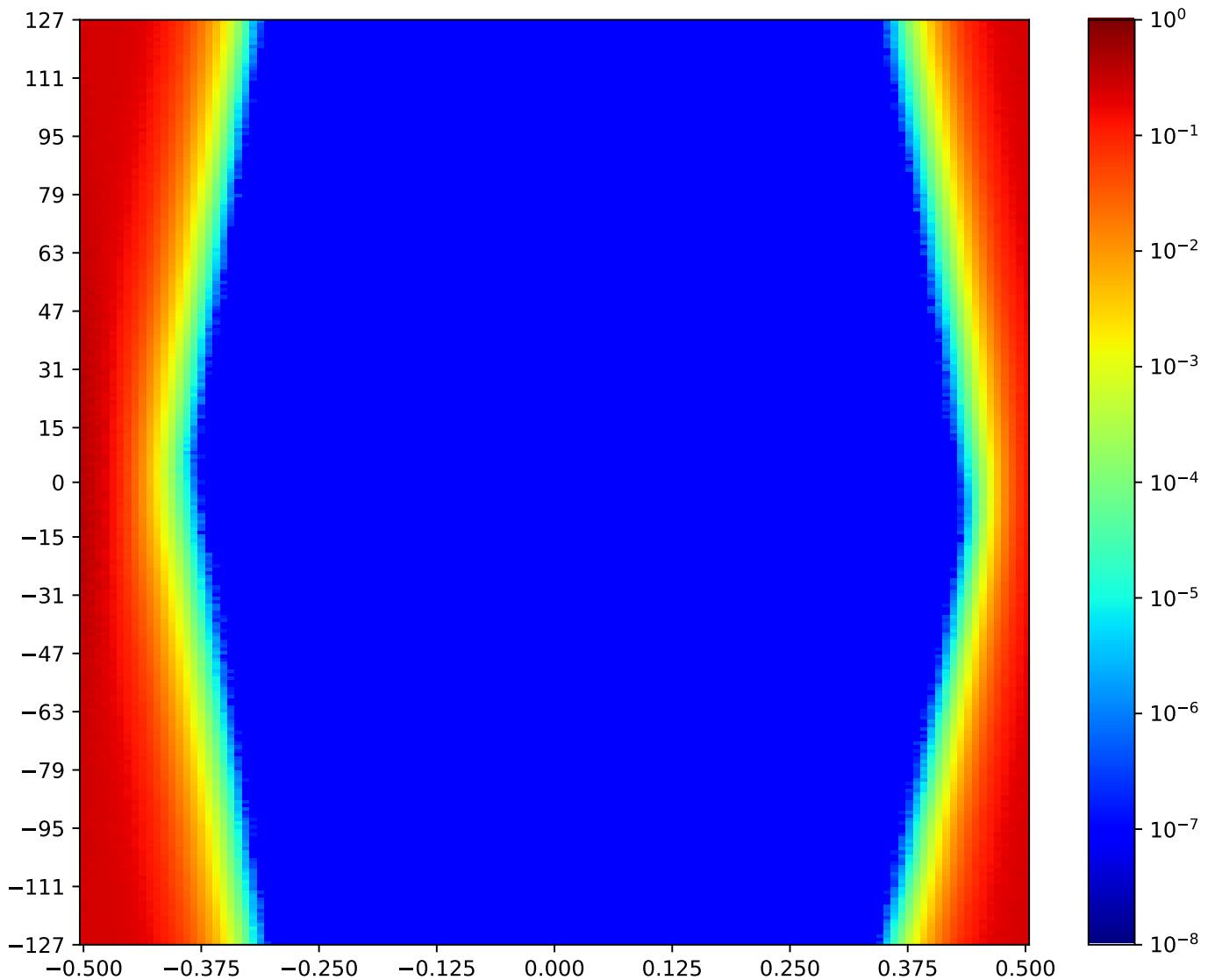


Figure 1.9: MSP\_A\_FPGA-TX1-07-RX16-07-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.9 MSP\_A\_FPGA-TX1-08-RX16-08-MSP\_C\_FPGA

Table 1.9: MSP\_A\_FPGA-TX1-08-RX16-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:09:54		2018-Jan-24 03:11:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24784	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

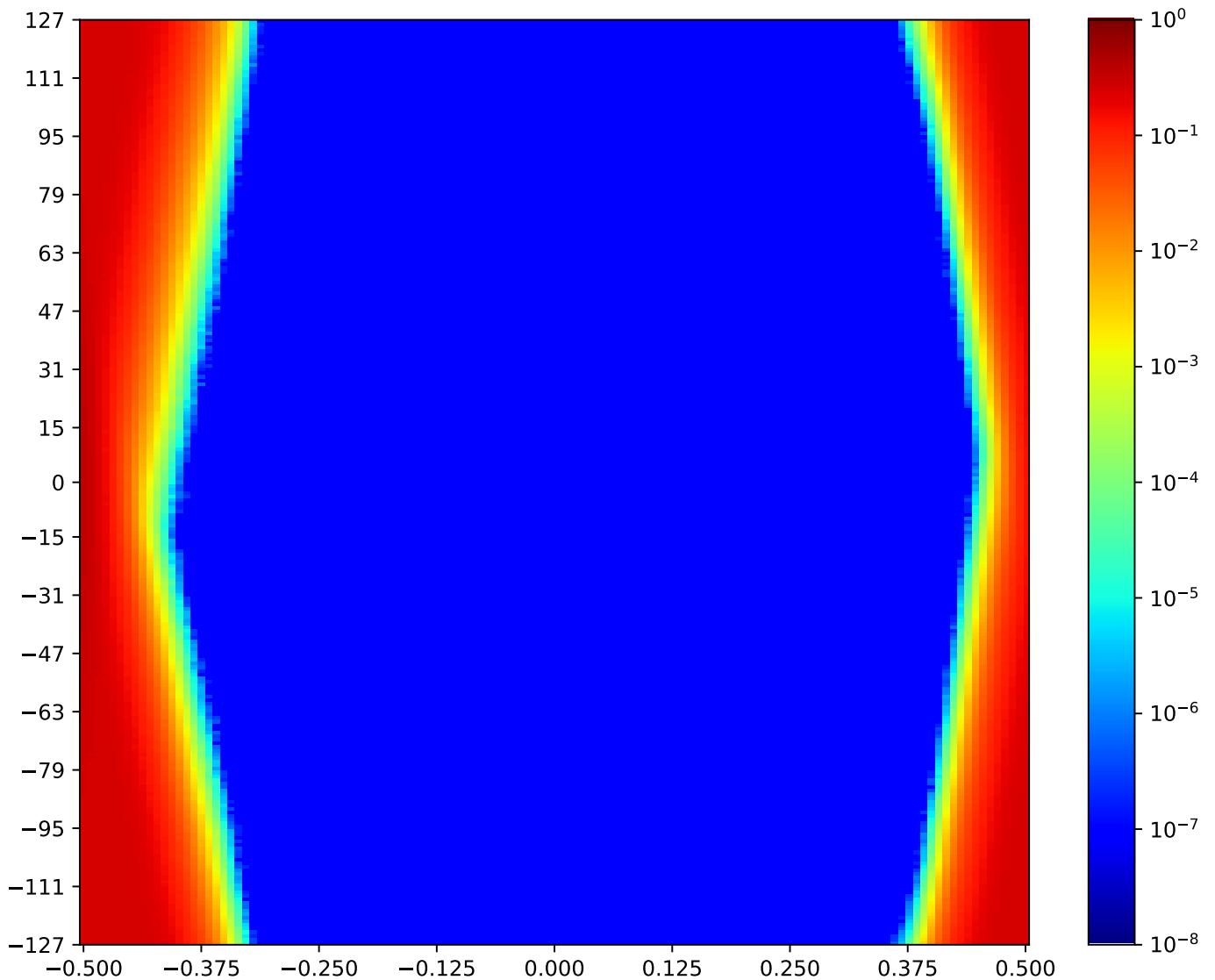


Figure 1.10: MSP\_A\_FPGA-TX1-08-RX16-08-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.10 MSP\_A\_FPGA-TX1-09-RX16-09-MSP\_C\_FPGA

Table 1.10: MSP\_A\_FPGA-TX1-09-RX16-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:02:56		2018-Jan-24 03:04:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25174	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

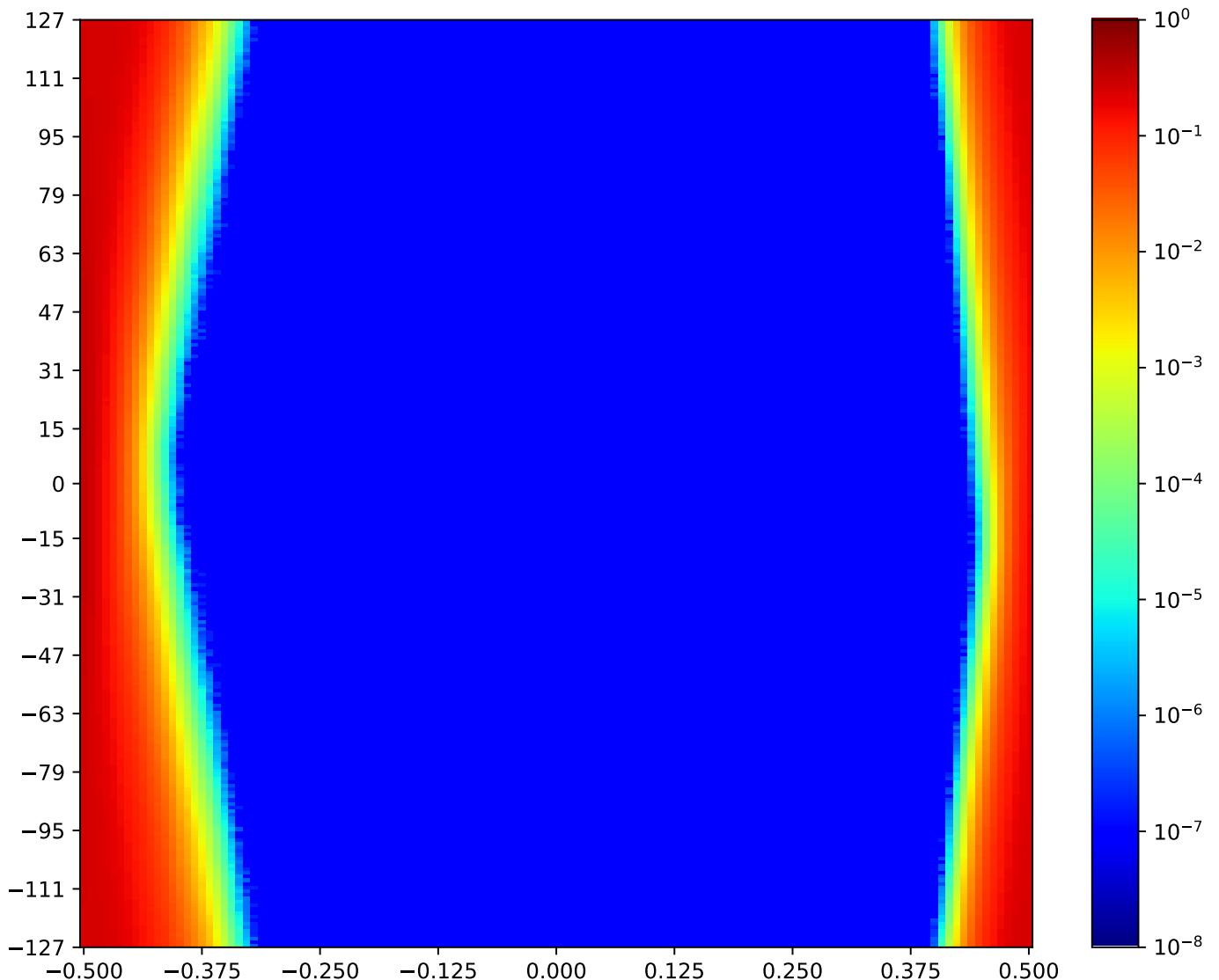


Figure 1.11: MSP\_A\_FPGA-TX1-09-RX16-09-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.11 MSP\_A\_FPGA-TX1-10-RX16-10-MSP\_C\_FPGA

Table 1.11: MSP\_A\_FPGA-TX1-10-RX16-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:07:34		2018-Jan-24 03:08:45	
Reset RX	OA	HO		HO (%)	
true	25665	110		84.50%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

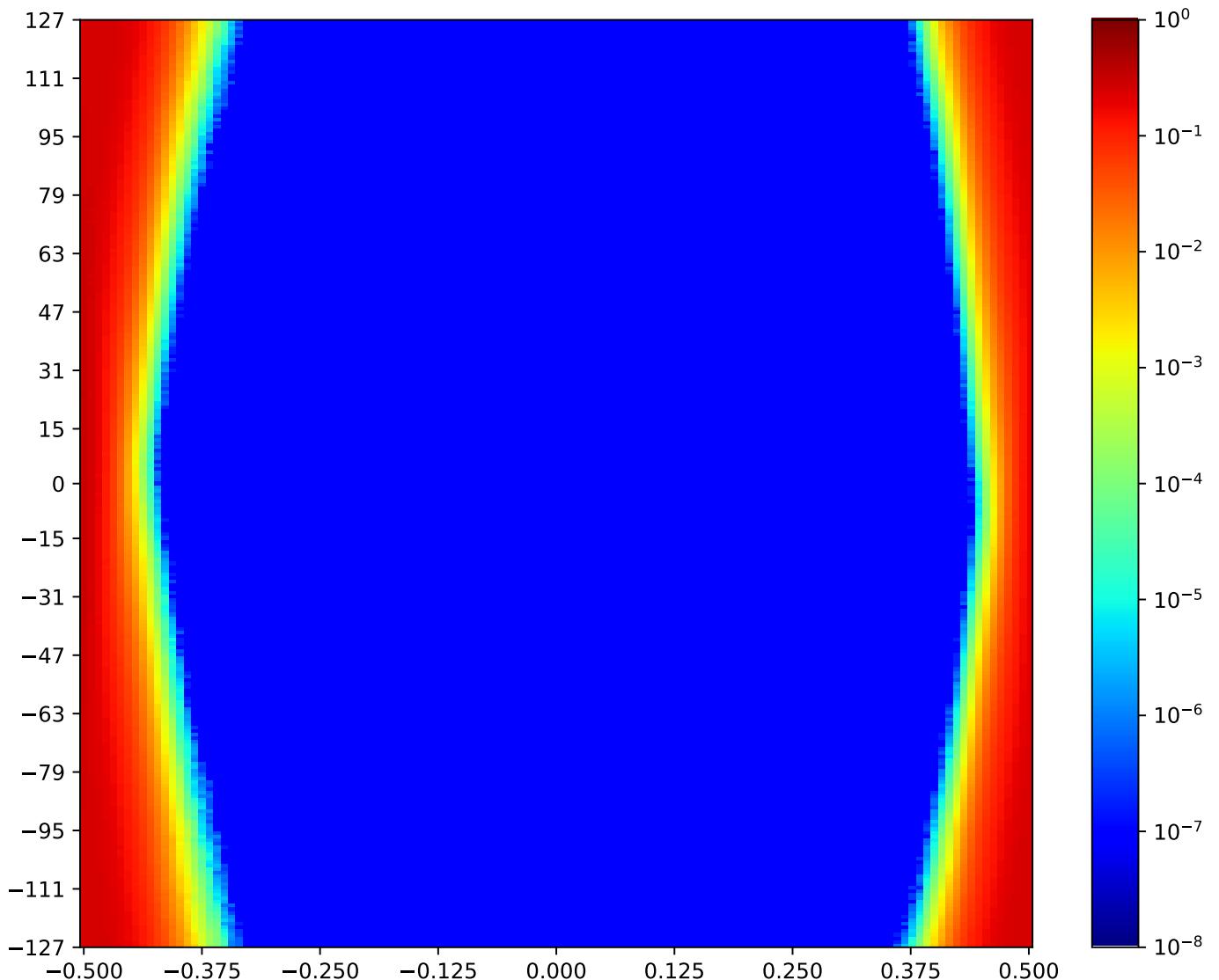


Figure 1.12: MSP\_A\_FPGA-TX1-10-RX16-10-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.1.12 MSP\_A\_FPGA-TX1-11-RX16-11-MSP\_C\_FPGA

Table 1.12: MSP\_A\_FPGA-TX1-11-RX16-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:06:25		2018-Jan-24 03:07:34	
Reset RX	OA	HO		HO (%)	
true	23816	103		79.84%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

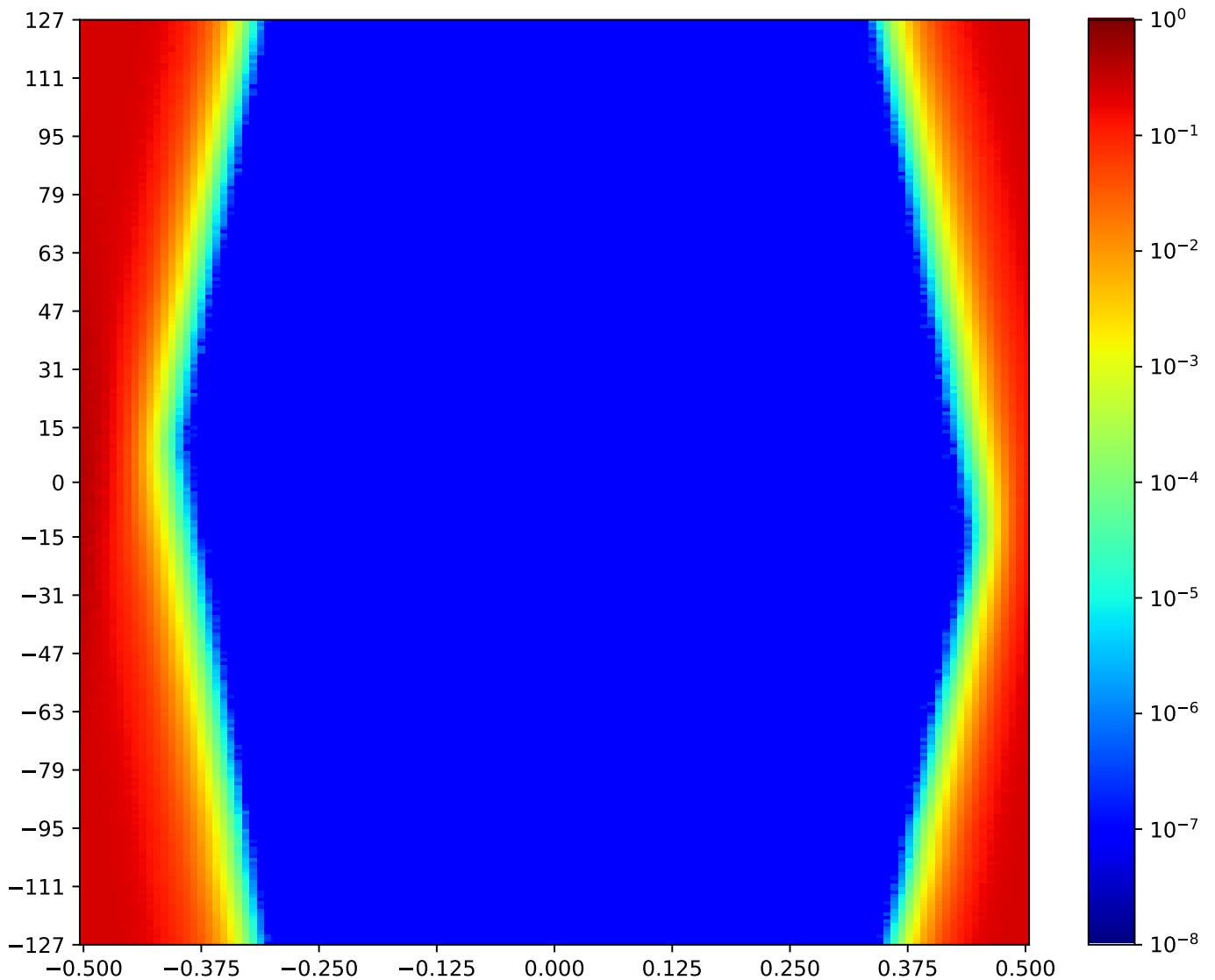


Figure 1.13: MSP\_A\_FPGA-TX1-11-RX16-11-MSP\_C\_FPGA

Call back to summary Figure 1.1. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.2 MSP\_A TX2 MSP\_C RX15 Minipod Loopback

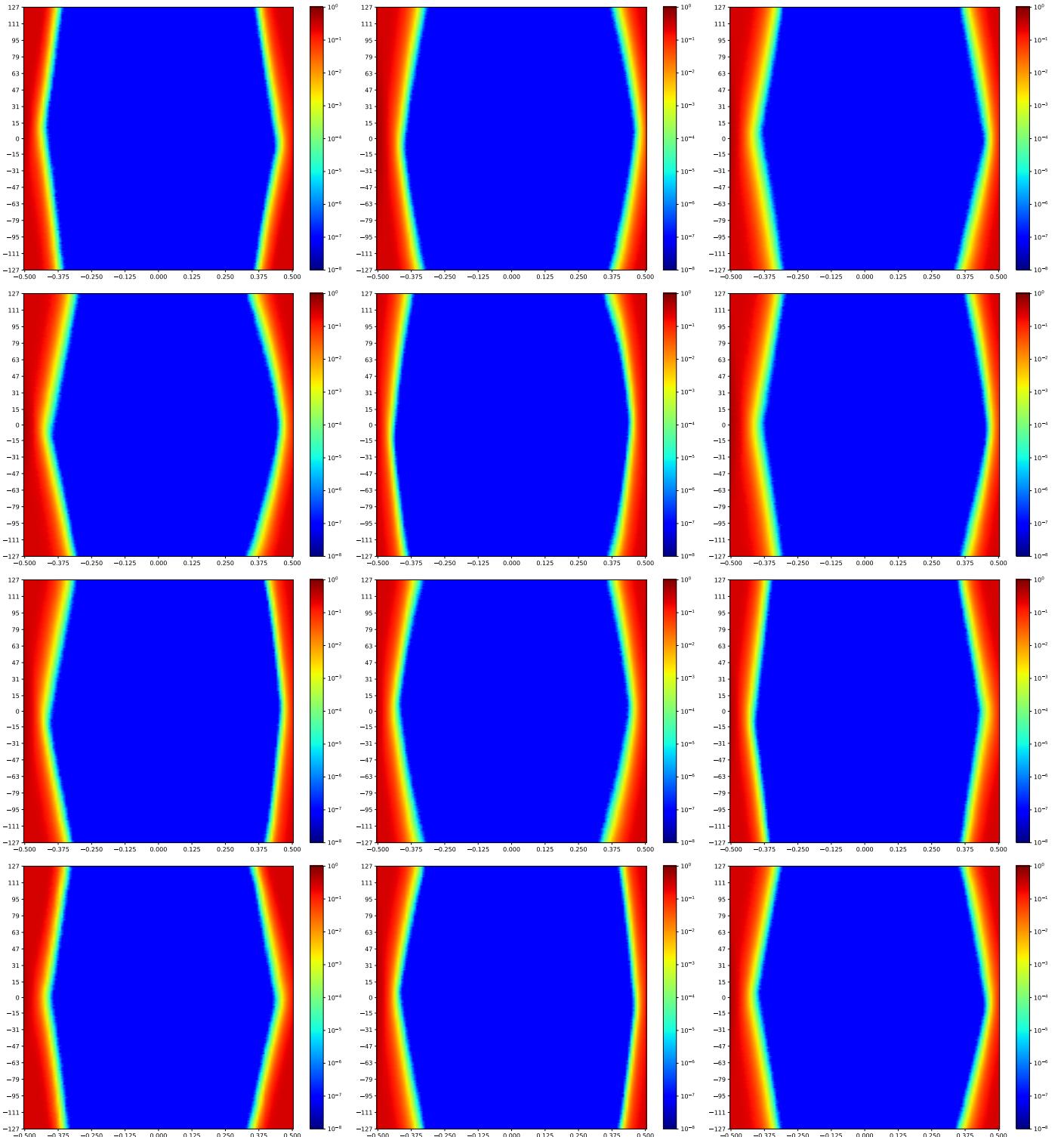


Figure 1.14: MSP\_A TX2 MSP\_C RX15 Minipod Loopback

A cross-reference to Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.27.

### 1.2.1 MSP\_A\_FPGA-TX2-00-RX15-00-MSP\_C\_FPGA

Table 1.13: MSP\_A\_FPGA-TX2-00-RX15-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:15:44		2018-Jan-24 03:16:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25122	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

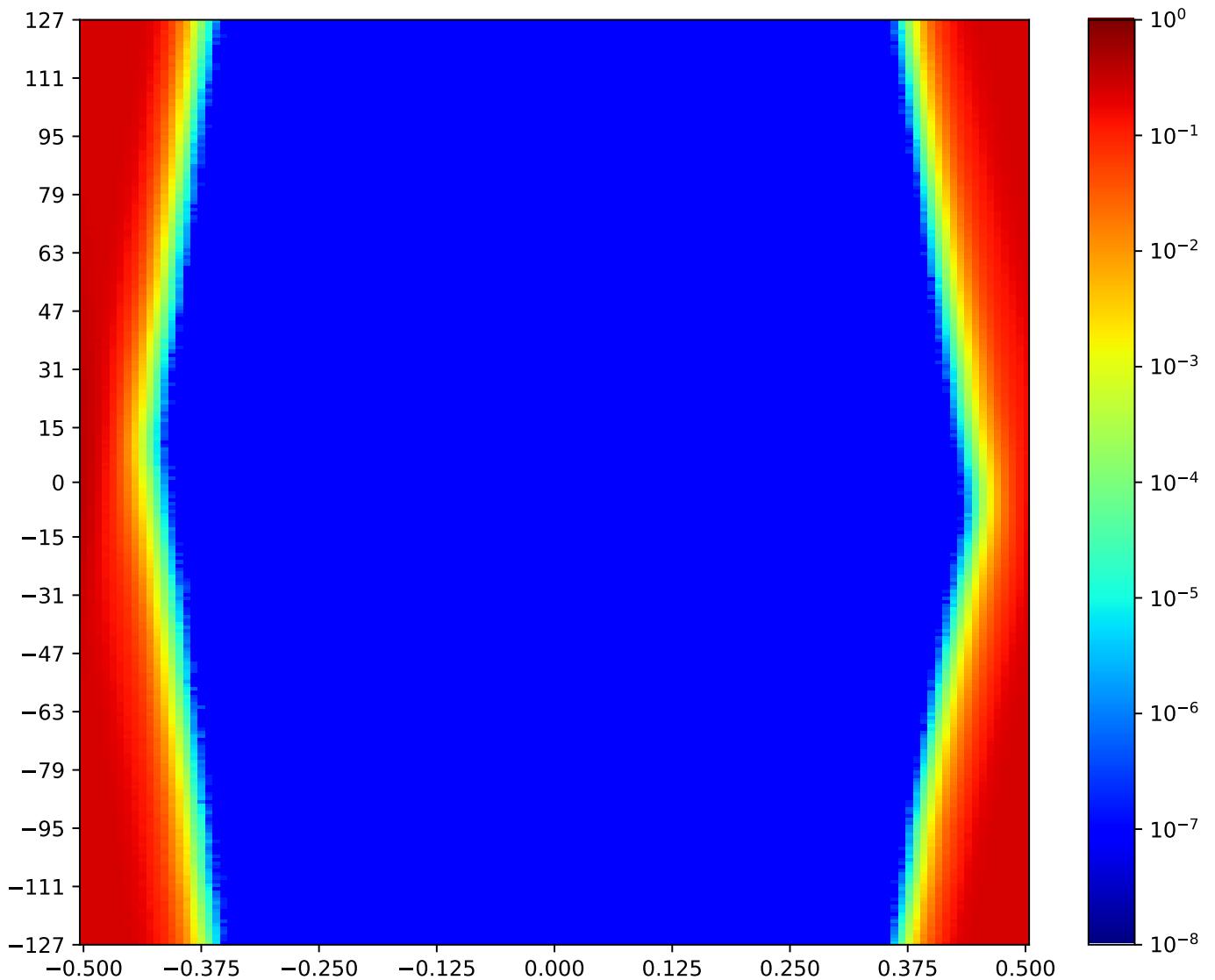


Figure 1.15: MSP\_A\_FPGA-TX2-00-RX15-00-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.2.2 MSP\_A\_FPGA-TX2-01-RX15-01-MSP\_C\_FPGA

Table 1.14: MSP\_A\_FPGA-TX2-01-RX15-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:13:24		2018-Jan-24 03:14:34	
Reset RX	OA	HO		HO (%)	
true	24923	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

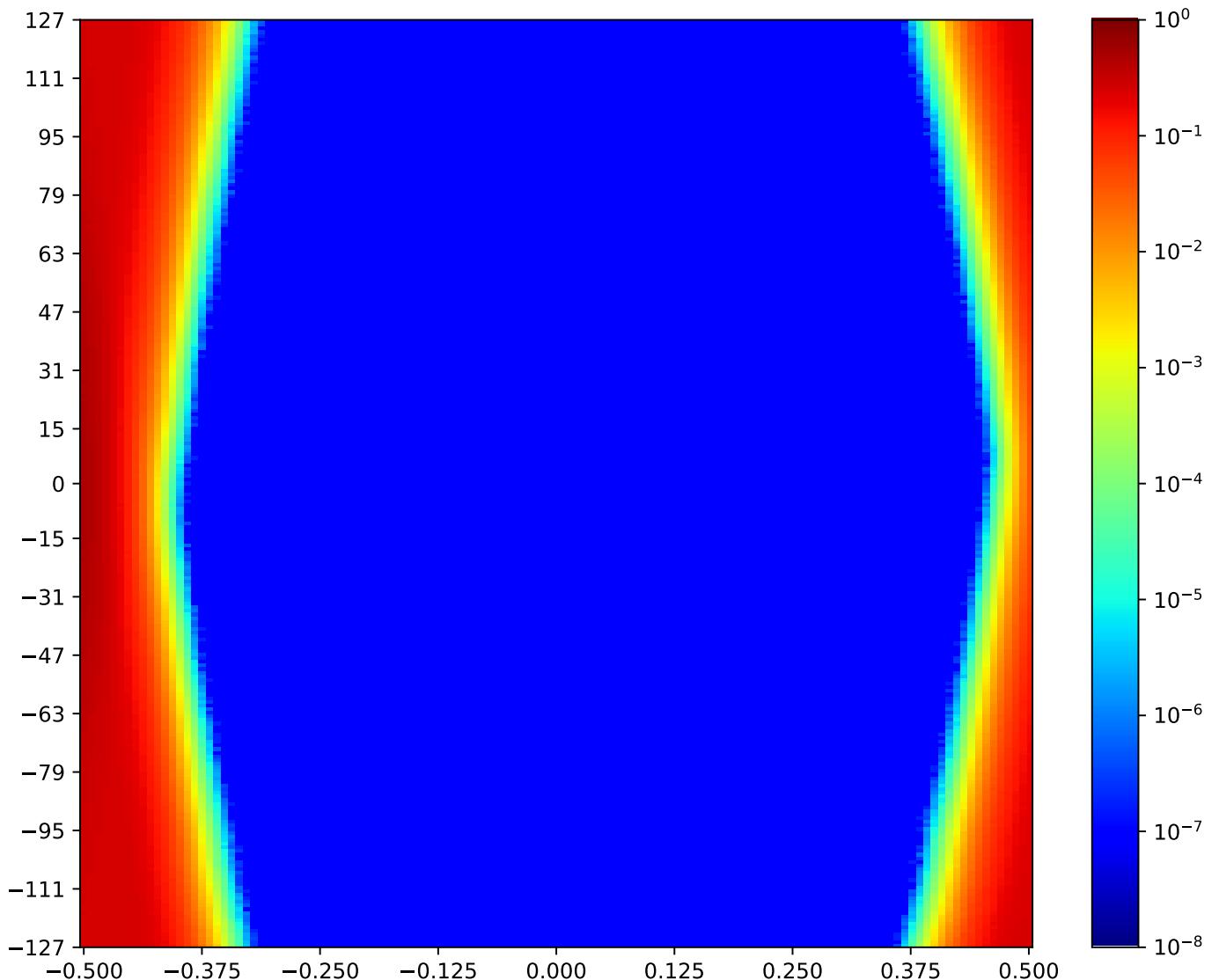


Figure 1.16: MSP\_A\_FPGA-TX2-01-RX15-01-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.2.3 MSP\_A\_FPGA-TX2-02-RX15-02-MSP\_C\_FPGA

Table 1.15: MSP\_A\_FPGA-TX2-02-RX15-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:19:16		2018-Jan-24 03:20:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23533	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

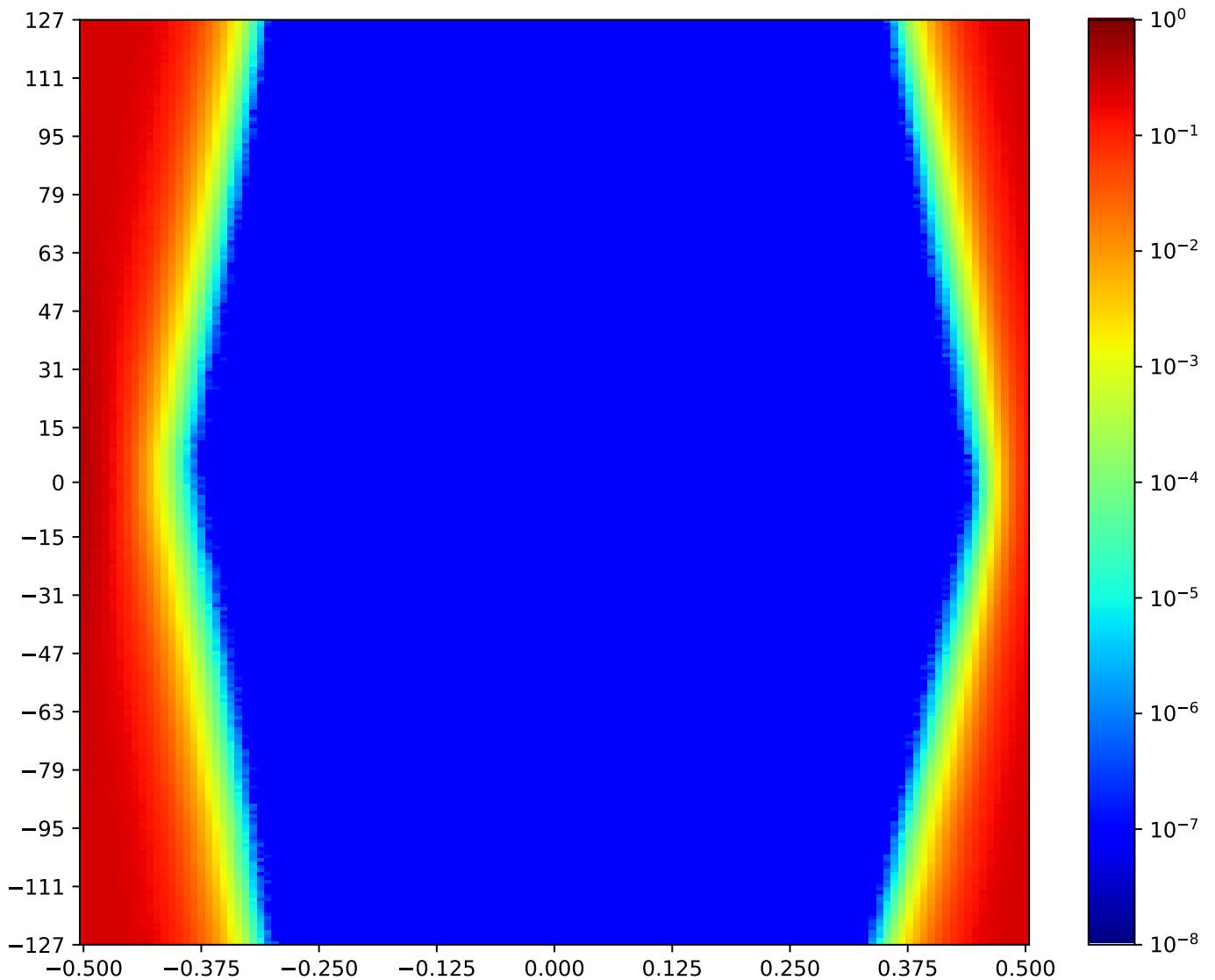


Figure 1.17: MSP\_A\_FPGA-TX2-02-RX15-02-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.2.4 MSP\_A\_FPGA-TX2-03-RX15-03-MSP\_C\_FPGA

Table 1.16: MSP\_A\_FPGA-TX2-03-RX15-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:12:14		2018-Jan-24 03:13:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23818	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

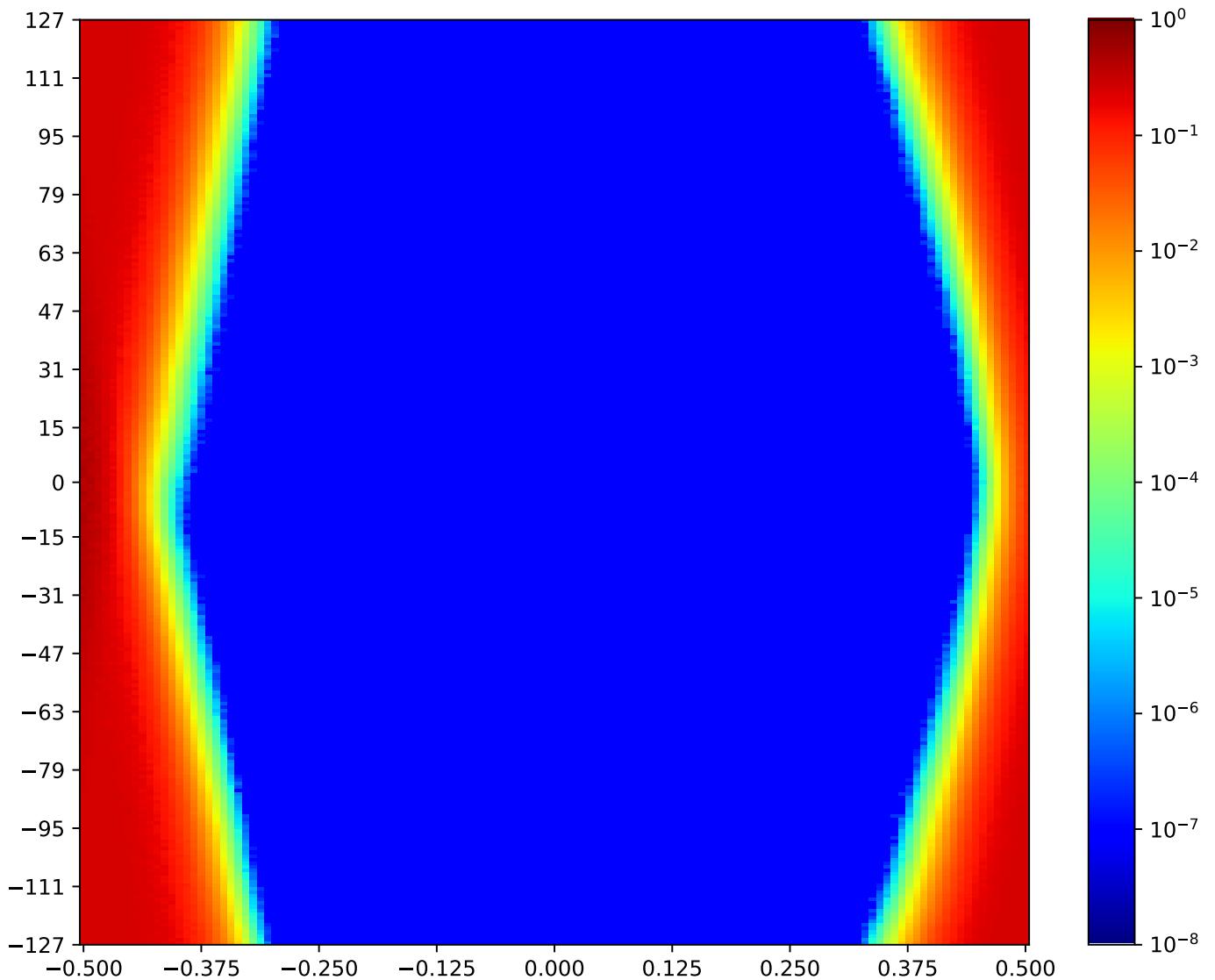


Figure 1.18: MSP\_A\_FPGA-TX2-03-RX15-03-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.2.5 MSP\_A\_FPGA-TX2-04-RX15-04-MSP\_C\_FPGA

Table 1.17: MSP\_A\_FPGA-TX2-04-RX15-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:22:48		2018-Jan-24 03:24:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26054	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

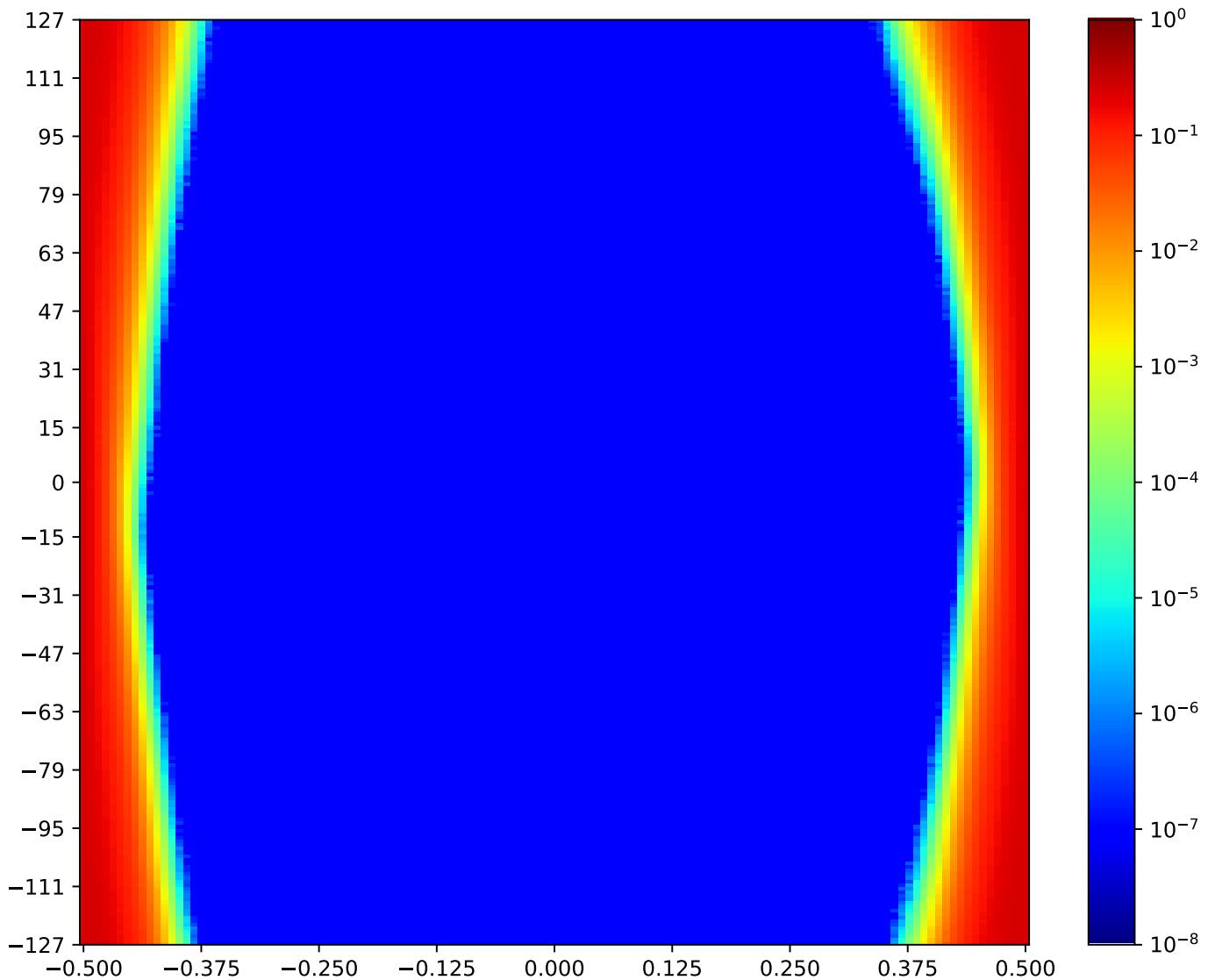


Figure 1.19: MSP\_A\_FPGA-TX2-04-RX15-04-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.2.6 MSP\_A\_FPGA-TX2-05-RX15-05-MSP\_C\_FPGA

Table 1.18: MSP\_A\_FPGA-TX2-05-RX15-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:14:34		2018-Jan-24 03:15:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24033	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

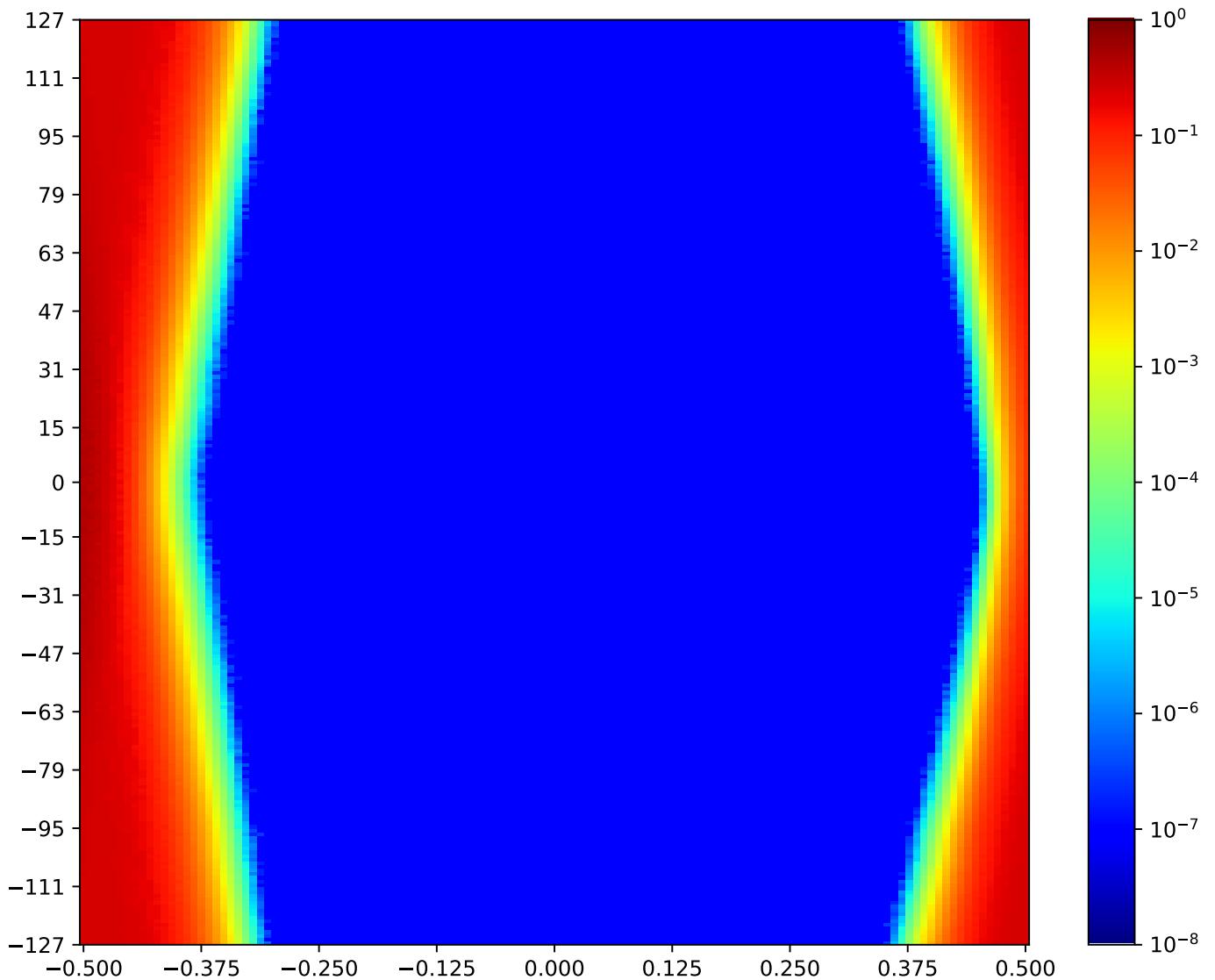


Figure 1.20: MSP\_A\_FPGA-TX2-05-RX15-05-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.2.7 MSP\_A\_FPGA-TX2-06-RX15-06-MSP\_C\_FPGA

Table 1.19: MSP\_A\_FPGA-TX2-06-RX15-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:25:11		2018-Jan-24 03:26:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25298	107	82.95%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

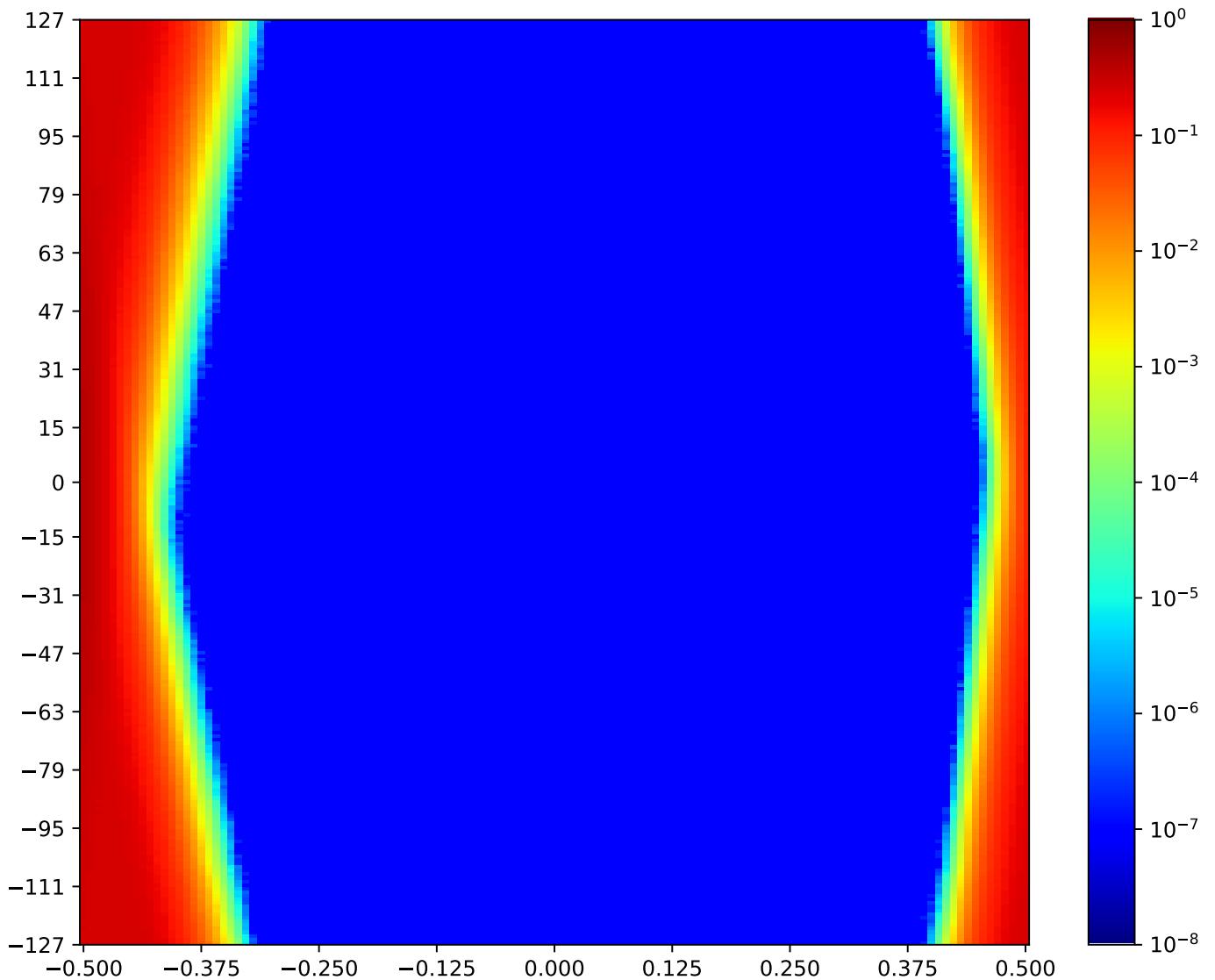


Figure 1.21: MSP\_A\_FPGA-TX2-06-RX15-06-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.2.8 MSP\_A\_FPGA-TX2-07-RX15-07-MSP\_C\_FPGA

Table 1.20: MSP\_A\_FPGA-TX2-07-RX15-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:16:54		2018-Jan-24 03:18:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24574	107	82.95%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

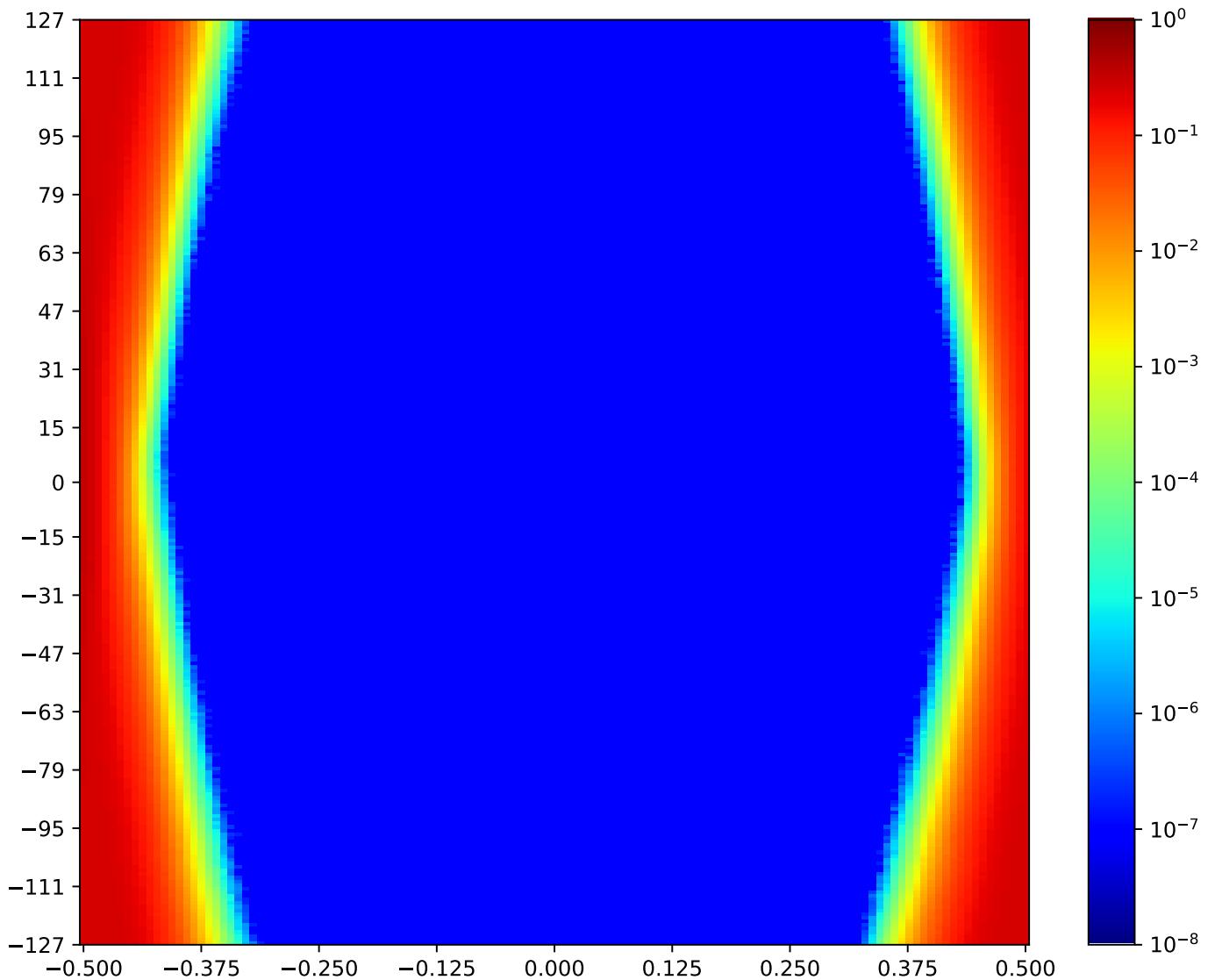


Figure 1.22: MSP\_A\_FPGA-TX2-07-RX15-07-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.2.9 MSP\_A\_FPGA-TX2-08-RX15-08-MSP\_C\_FPGA

Table 1.21: MSP\_A\_FPGA-TX2-08-RX15-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:24:00		2018-Jan-24 03:25:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24627	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

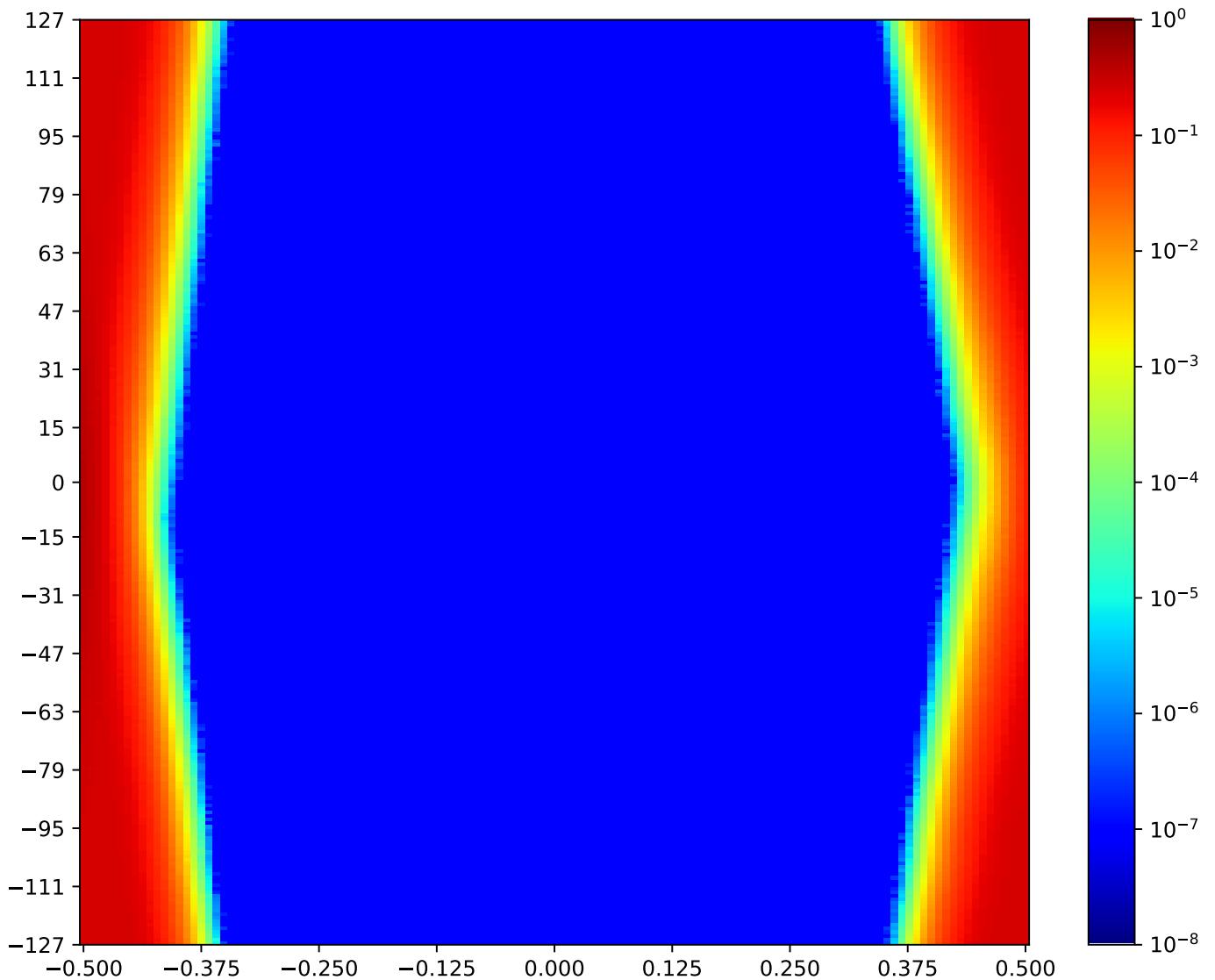


Figure 1.23: MSP\_A\_FPGA-TX2-08-RX15-08-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.2.10 MSP\_A\_FPGA-TX2-09-RX15-09-MSP\_C\_FPGA

Table 1.22: MSP\_A\_FPGA-TX2-09-RX15-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:18:06		2018-Jan-24 03:19:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23995	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

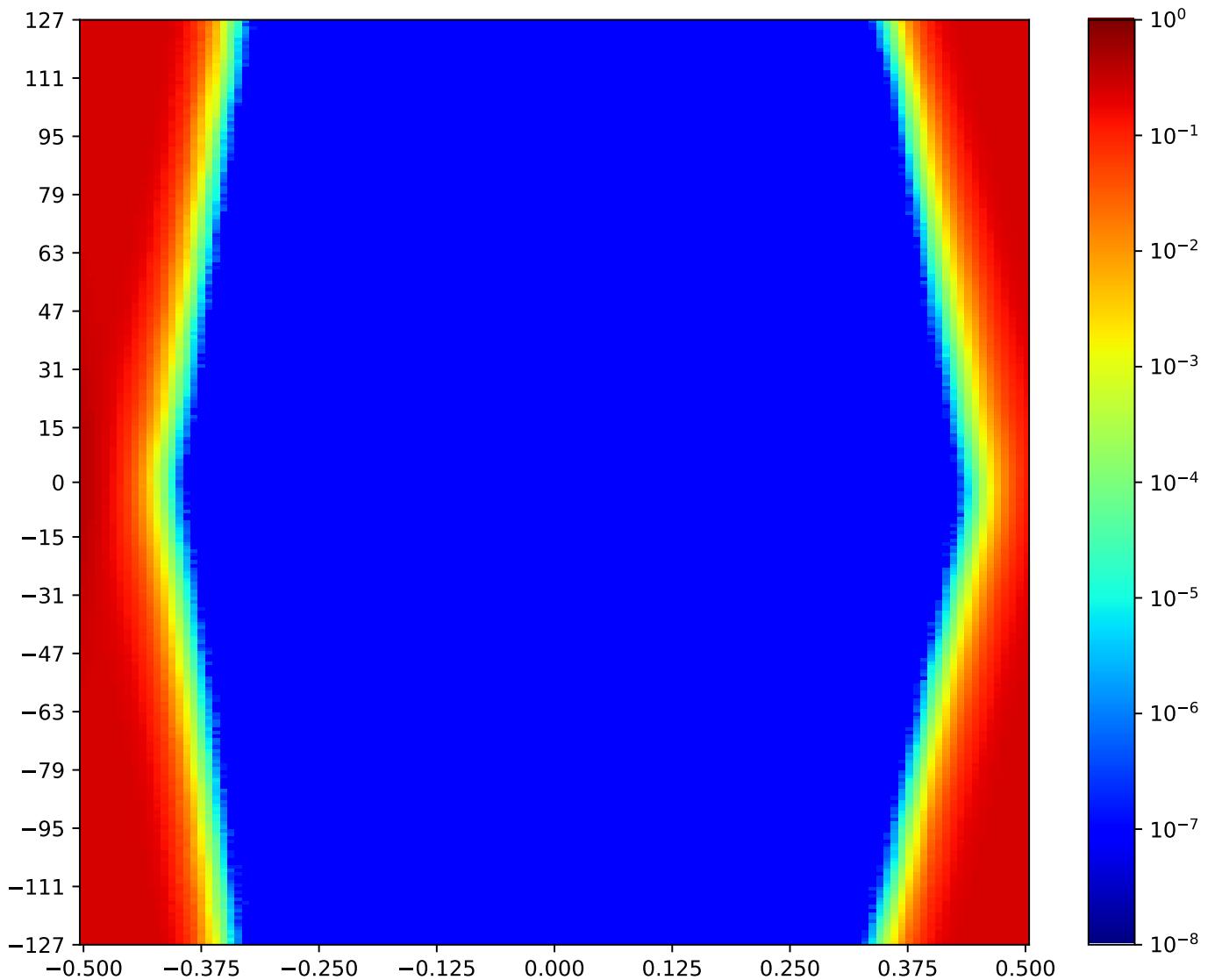


Figure 1.24: MSP\_A\_FPGA-TX2-09-RX15-09-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.2.11 MSP\_A\_FPGA-TX2-10-RX15-10-MSP\_C\_FPGA

Table 1.23: MSP\_A\_FPGA-TX2-10-RX15-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:21:36		2018-Jan-24 03:22:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25713	108	83.72%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

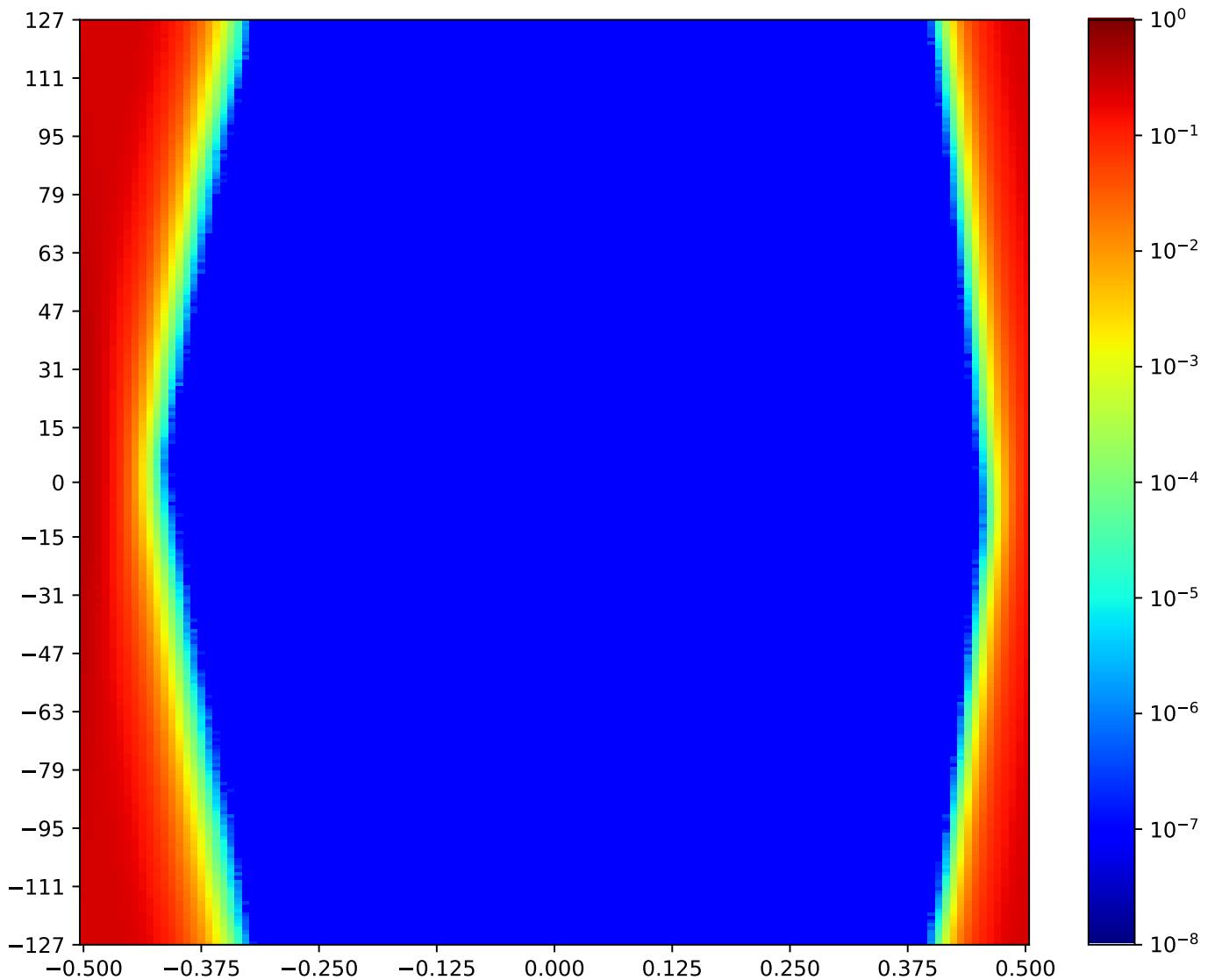


Figure 1.25: MSP\_A\_FPGA-TX2-10-RX15-10-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.2.12 MSP\_A\_FPGA-TX2-11-RX15-11-MSP\_C\_FPGA

Table 1.24: MSP\_A\_FPGA-TX2-11-RX15-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:20:26		2018-Jan-24 03:21:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24162	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

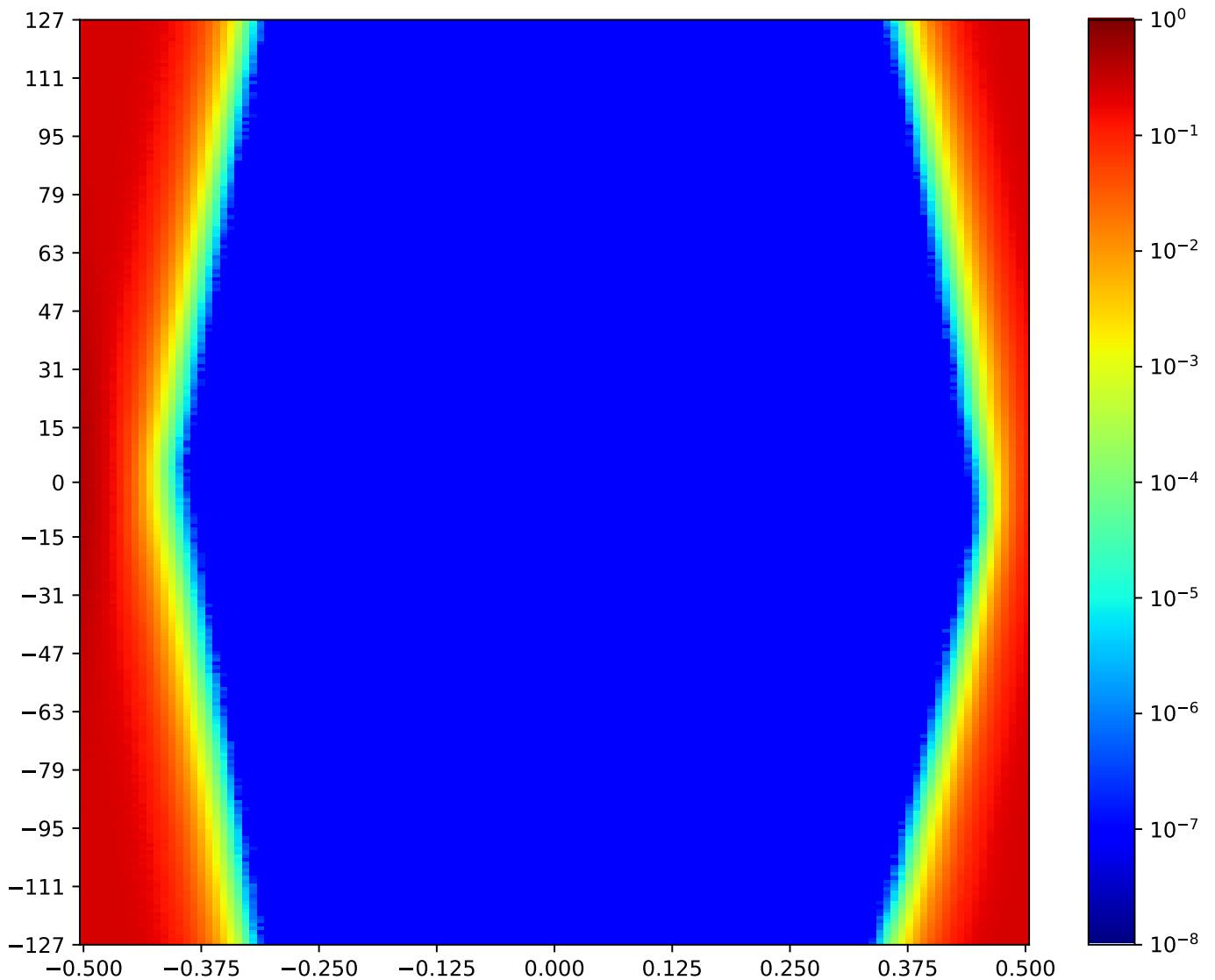


Figure 1.26: MSP\_A\_FPGA-TX2-11-RX15-11-MSP\_C\_FPGA

Call back to summary Figure 1.14. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3 MSP\_C TX3 MSP\_A RX7 Minipod Loopback

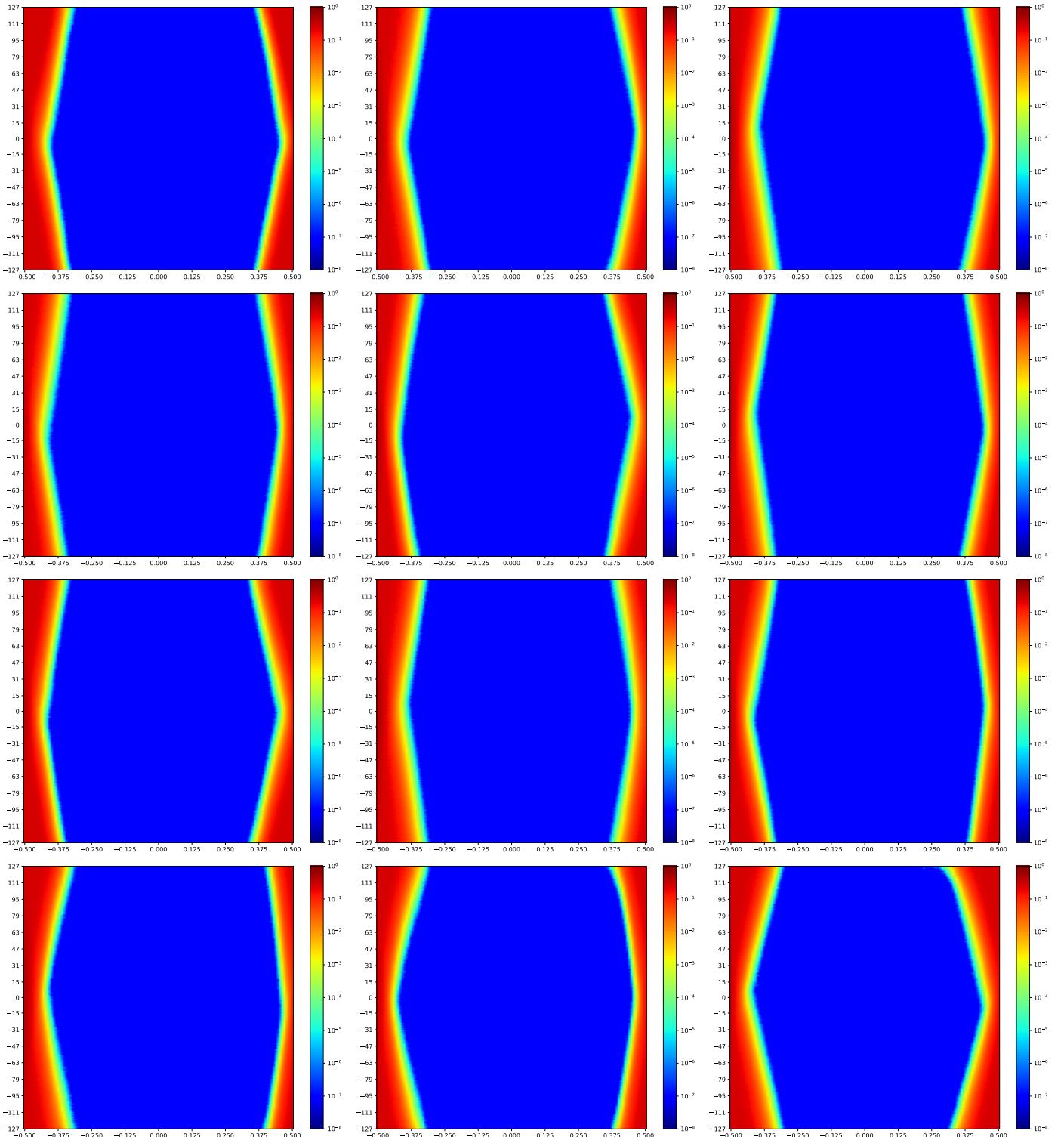


Figure 1.27: MSP\_C TX3 MSP\_A RX7 Minipod Loopback

A cross-reference to Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.40.

### 1.3.1 MSP\_C\_FPGA-TX3-00-RX7-00-MSP\_A\_FPGA

Table 1.25: MSP\_C\_FPGA-TX3-00-RX7-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:29:54		2018-Jan-24 03:31:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24473	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

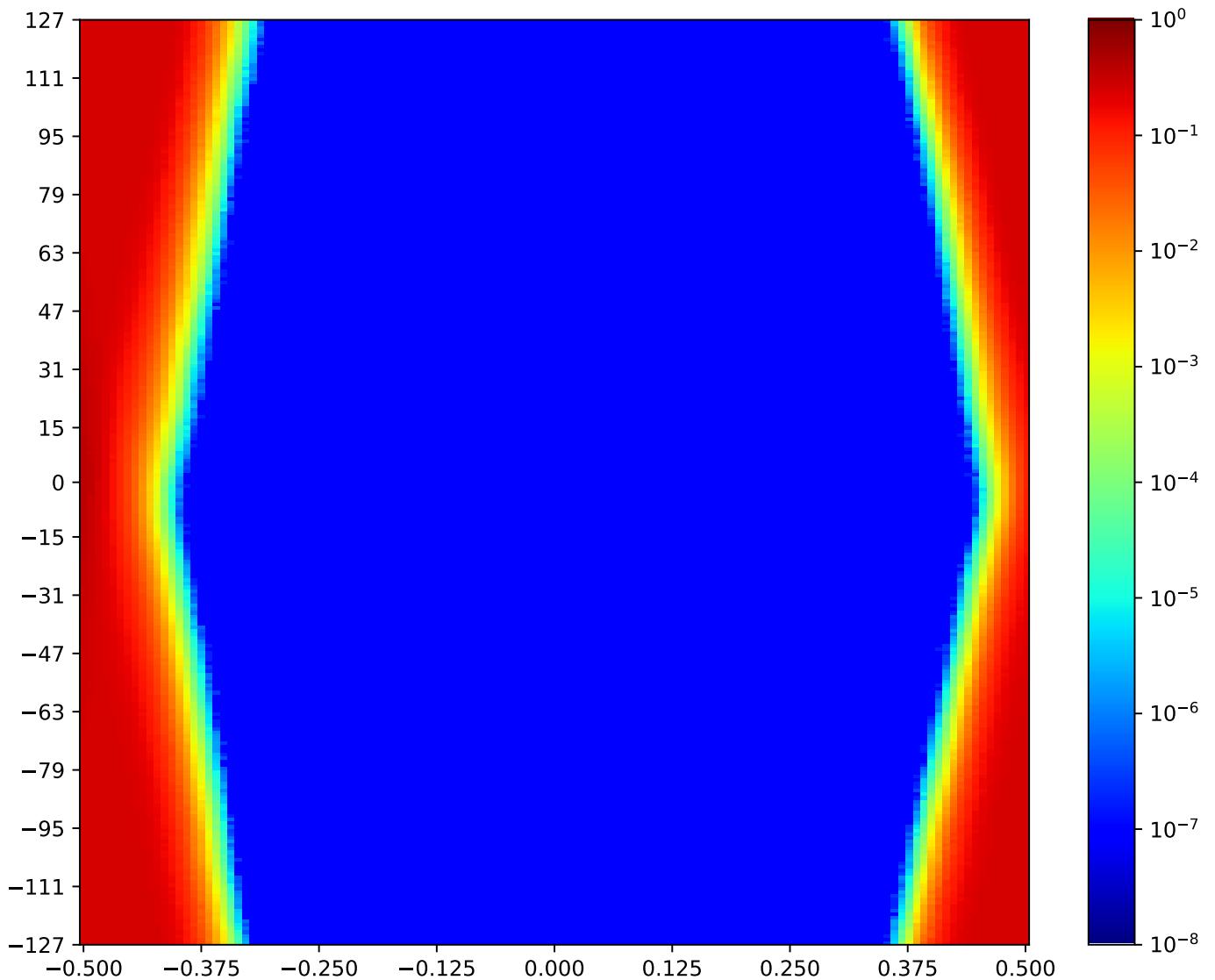


Figure 1.28: MSP\_C\_FPGA-TX3-00-RX7-00-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.2 MSP\_C\_FPGA-TX3-01-RX7-01-MSP\_A\_FPGA

Table 1.26: MSP\_C\_FPGA-TX3-01-RX7-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:32:15		2018-Jan-24 03:33:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24117	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

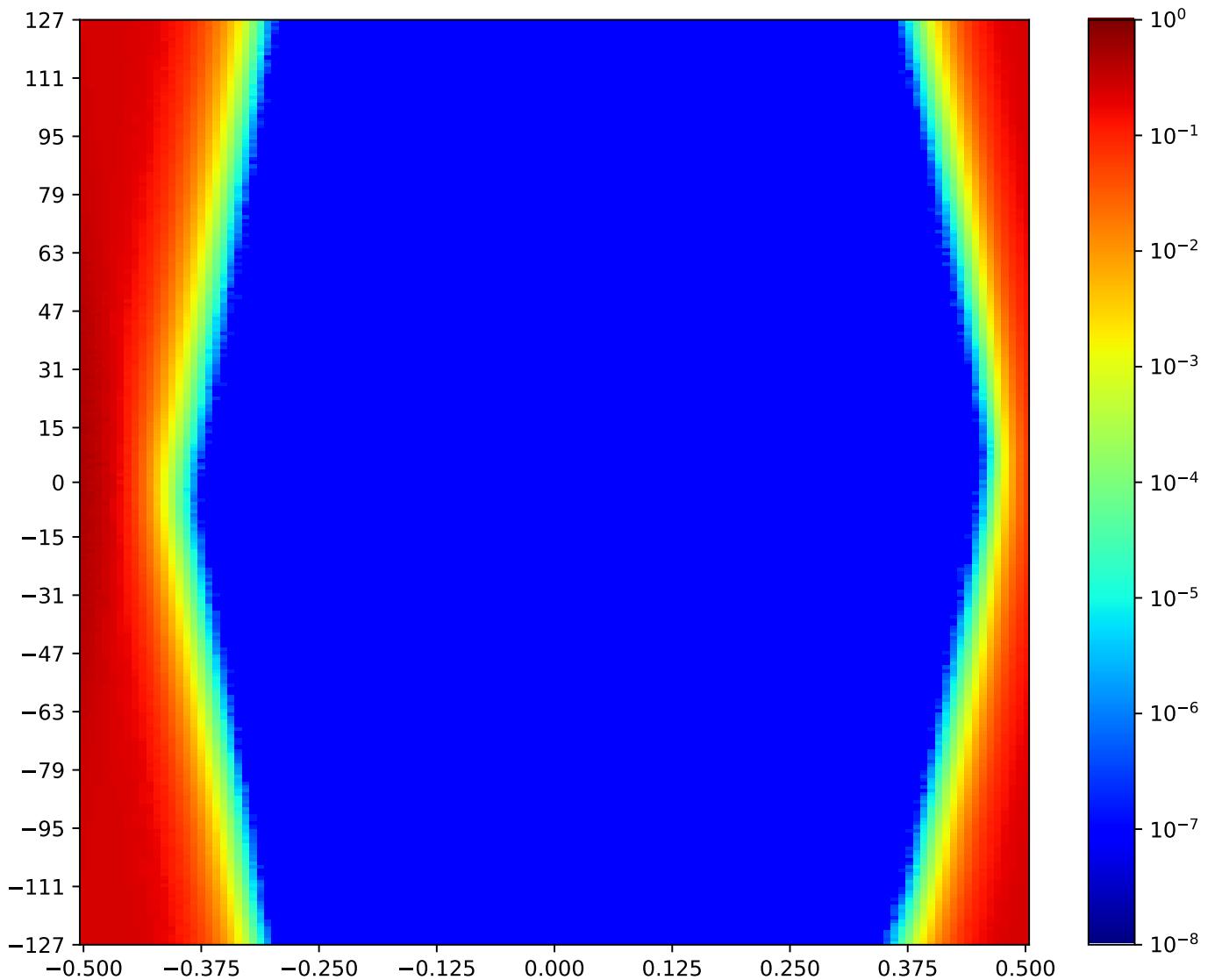


Figure 1.29: MSP\_C\_FPGA-TX3-01-RX7-01-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.3 MSP\_C\_FPGA-TX3-02-RX7-02-MSP\_A\_FPGA

Table 1.27: MSP\_C\_FPGA-TX3-02-RX7-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:33:25		2018-Jan-24 03:34:35	
Reset RX	OA	HO		HO (%)	
true	24045	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

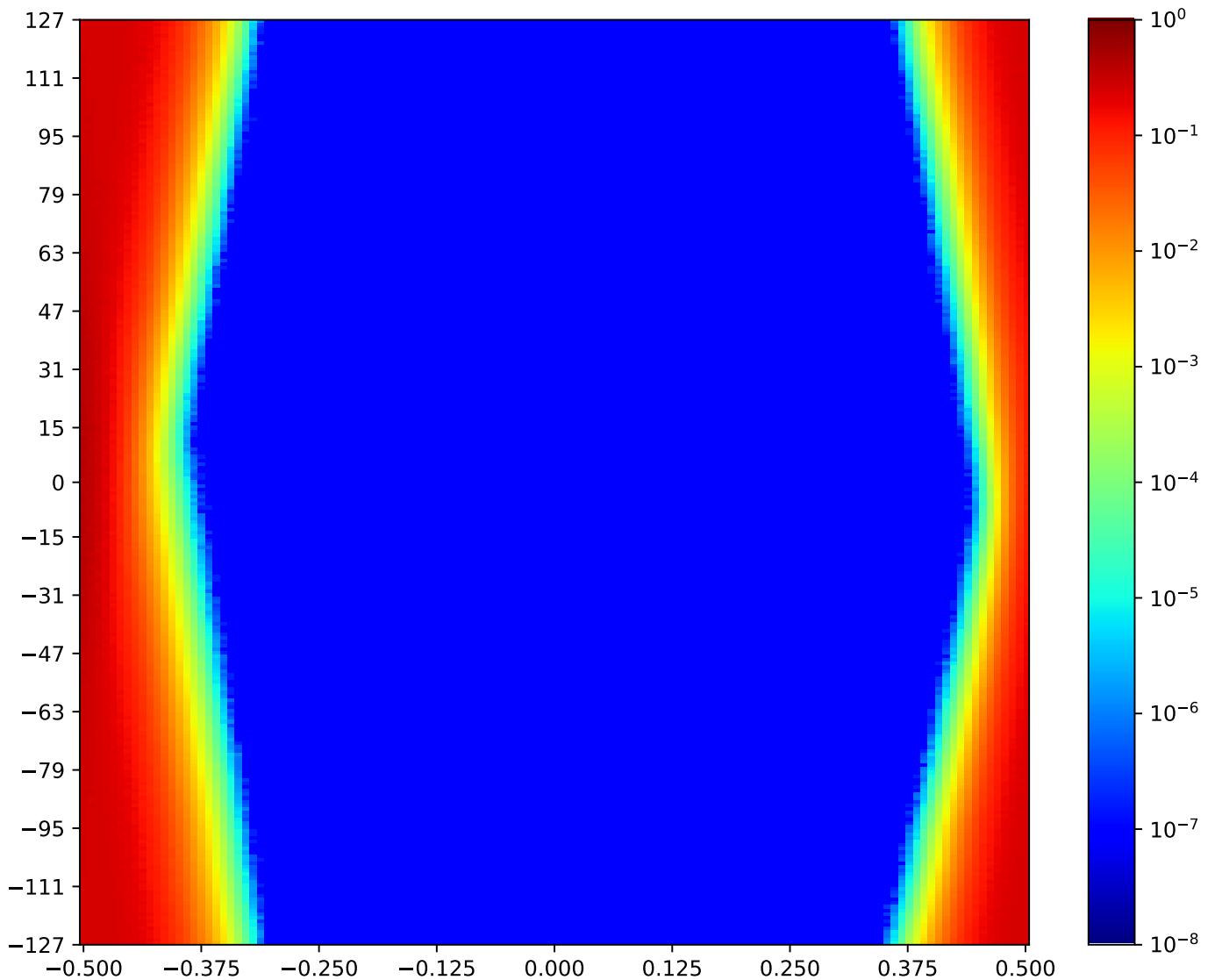


Figure 1.30: MSP\_C\_FPGA-TX3-02-RX7-02-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.4 MSP\_C\_FPGA-TX3-03-RX7-03-MSP\_A\_FPGA

Table 1.28: MSP\_C\_FPGA-TX3-03-RX7-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:27:34		2018-Jan-24 03:28:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24759	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

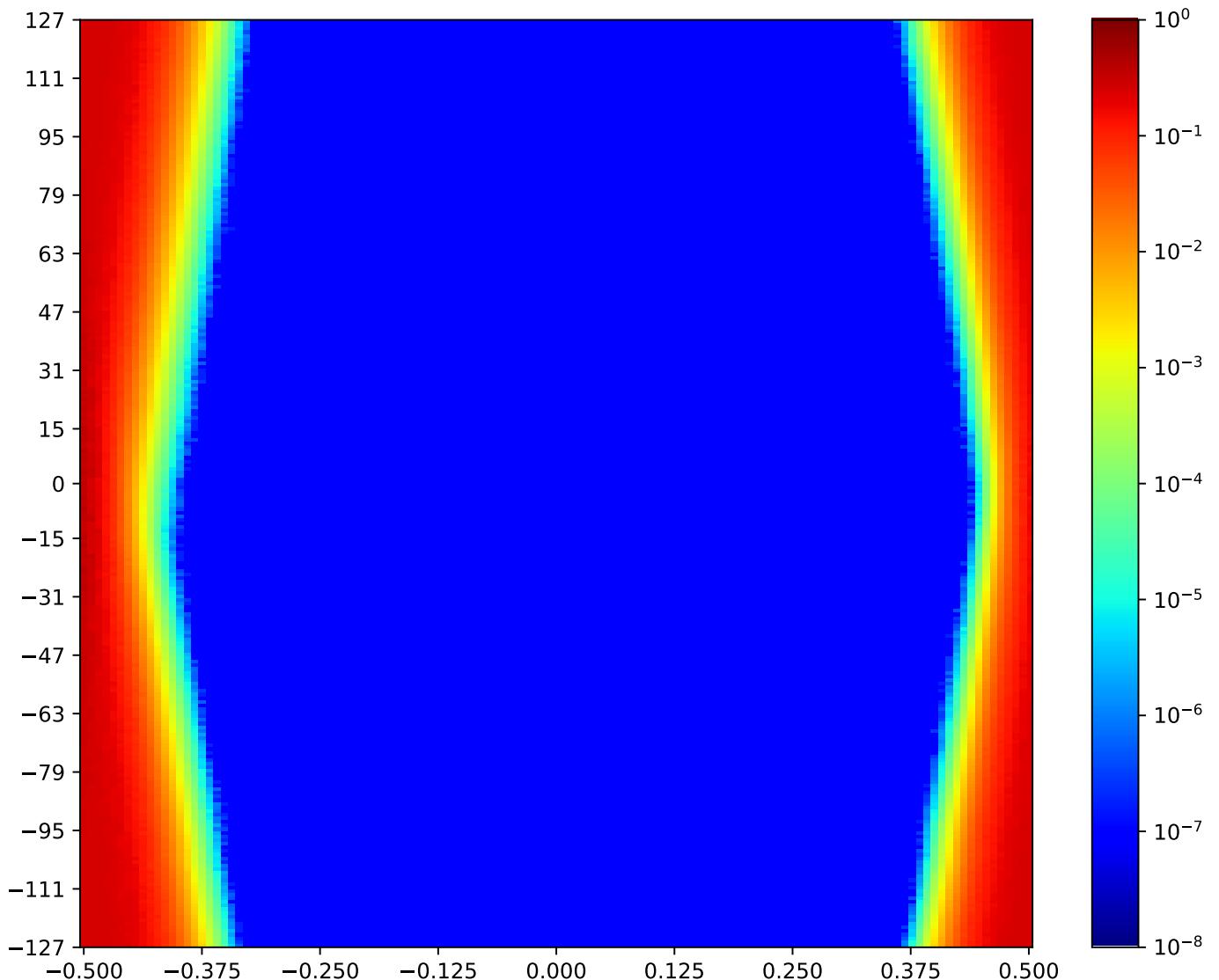


Figure 1.31: MSP\_C\_FPGA-TX3-03-RX7-03-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.5 MSP\_C\_FPGA-TX3-04-RX7-04-MSP\_A\_FPGA

Table 1.29: MSP\_C\_FPGA-TX3-04-RX7-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:36:56		2018-Jan-24 03:38:07	
Reset RX	OA	HO		VO   VO (%)	
true	24517	105		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

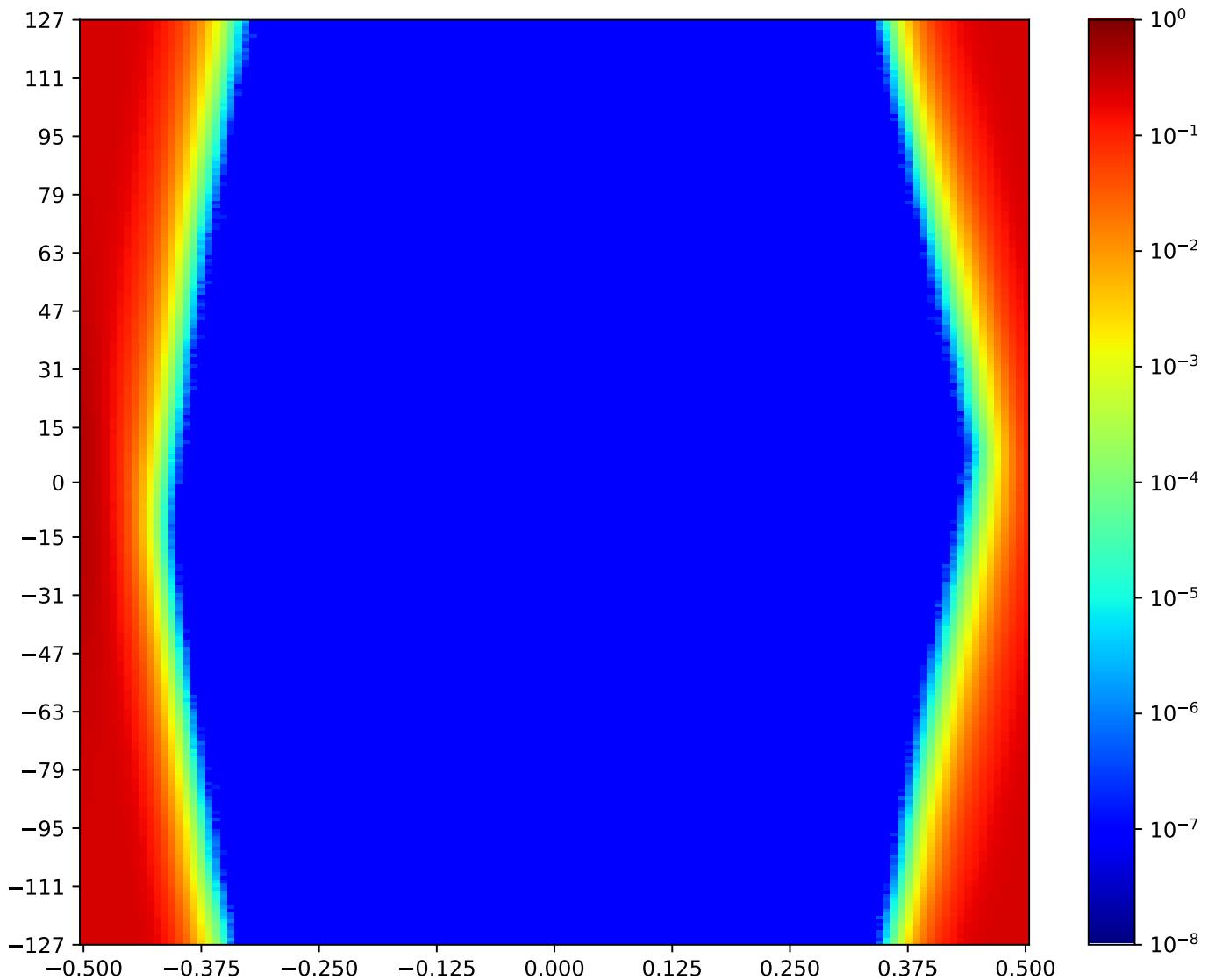


Figure 1.32: MSP\_C\_FPGA-TX3-04-RX7-04-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.6 MSP\_C\_FPGA-TX3-05-RX7-05-MSP\_A\_FPGA

Table 1.30: MSP\_C\_FPGA-TX3-05-RX7-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:26:23		2018-Jan-24 03:27:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24534	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

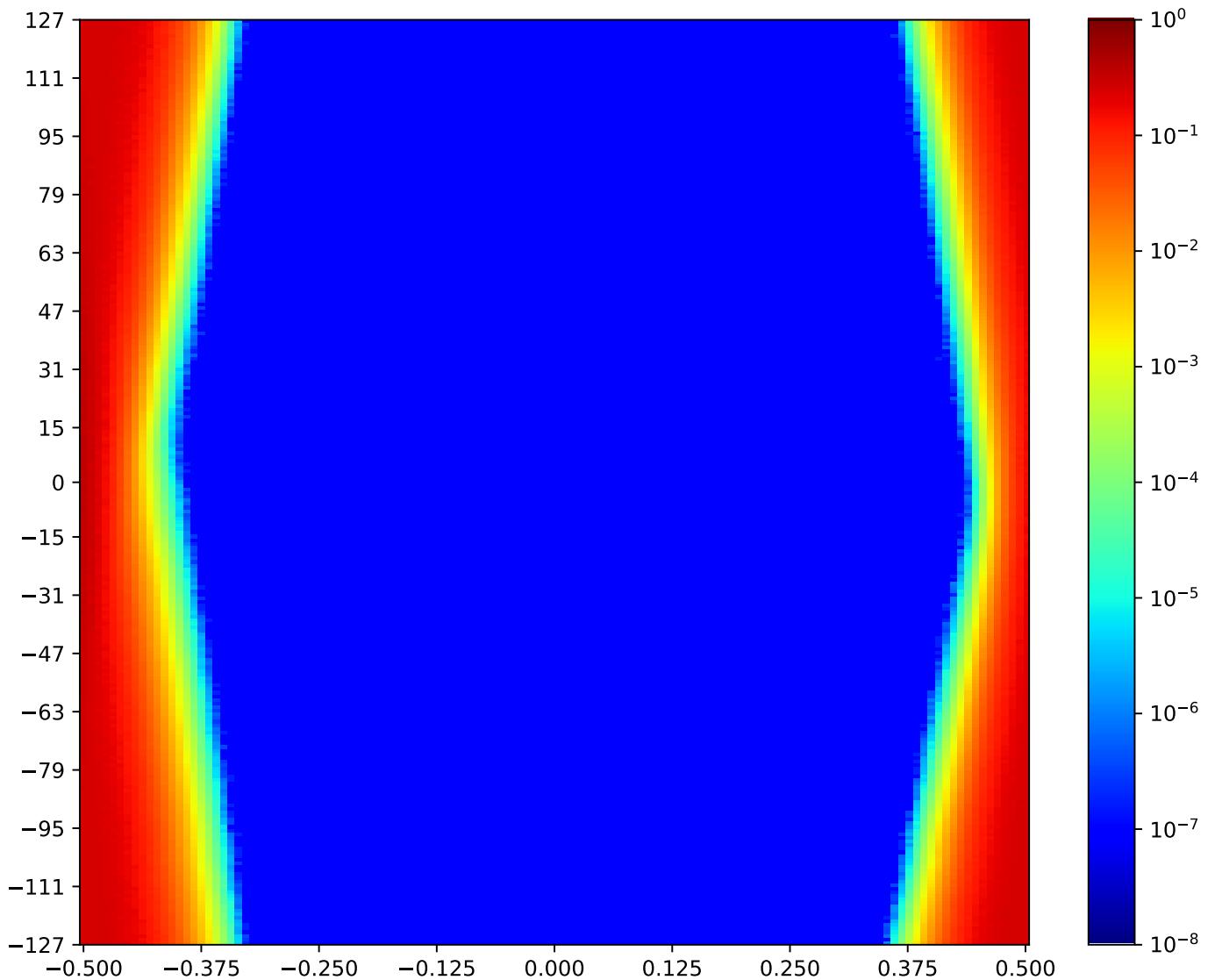


Figure 1.33: MSP\_C\_FPGA-TX3-05-RX7-05-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.7 MSP\_C\_FPGA-TX3-06-RX7-06-MSP\_A\_FPGA

Table 1.31: MSP\_C\_FPGA-TX3-06-RX7-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:39:19		2018-Jan-24 03:40:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24508	107	82.95%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

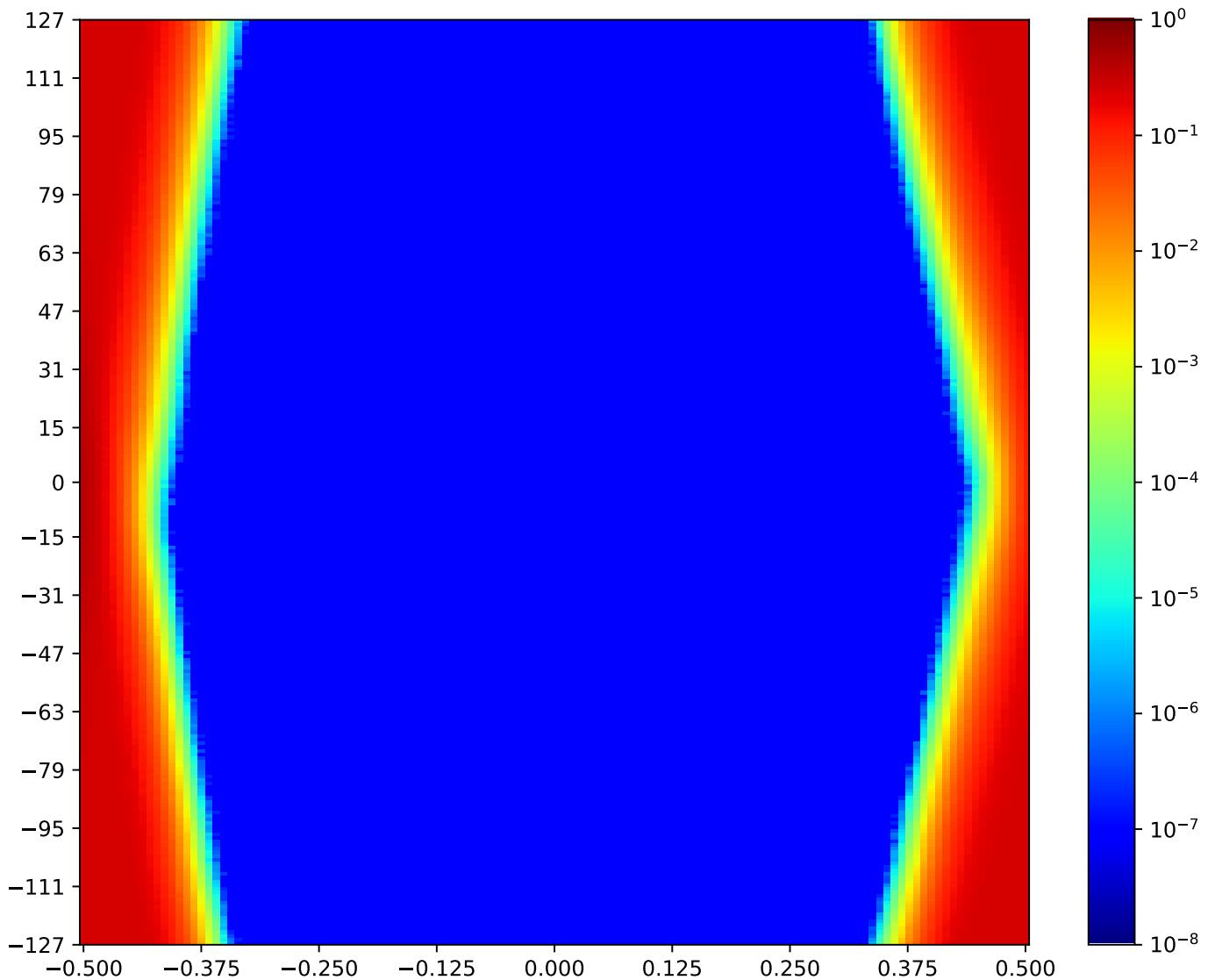


Figure 1.34: MSP\_C\_FPGA-TX3-06-RX7-06-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.8 MSP\_C\_FPGA-TX3-07-RX7-07-MSP\_A\_FPGA

Table 1.32: MSP\_C\_FPGA-TX3-07-RX7-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:28:45		2018-Jan-24 03:29:54	
Reset RX	OA	HO		HO (%)	
true	24044	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

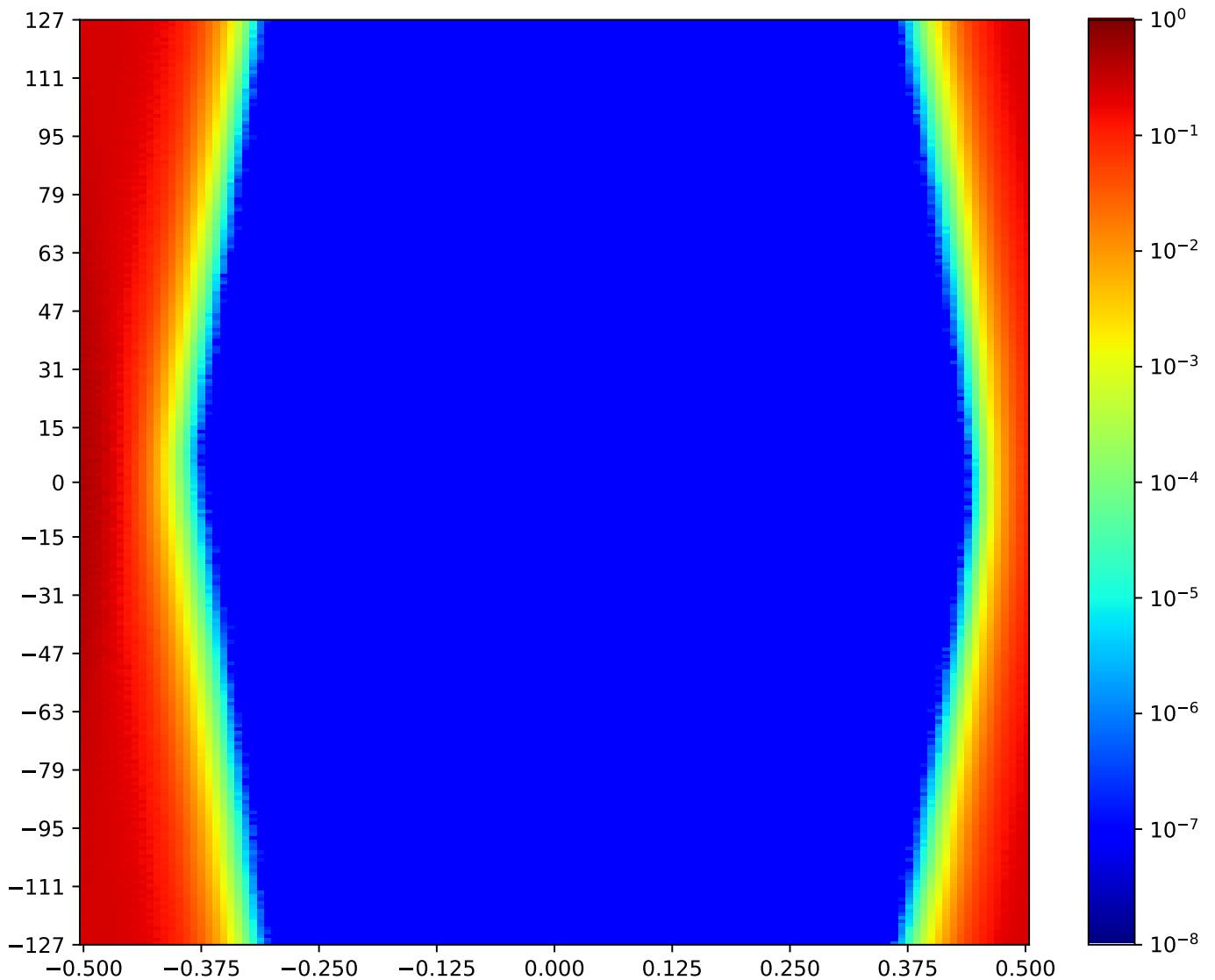


Figure 1.35: MSP\_C\_FPGA-TX3-07-RX7-07-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.9 MSP\_C\_FPGA-TX3-08-RX7-08-MSP\_A\_FPGA

Table 1.33: MSP\_C\_FPGA-TX3-08-RX7-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:38:07		2018-Jan-24 03:39:19	
Reset RX	OA	HO		HO (%)	
true	24952	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

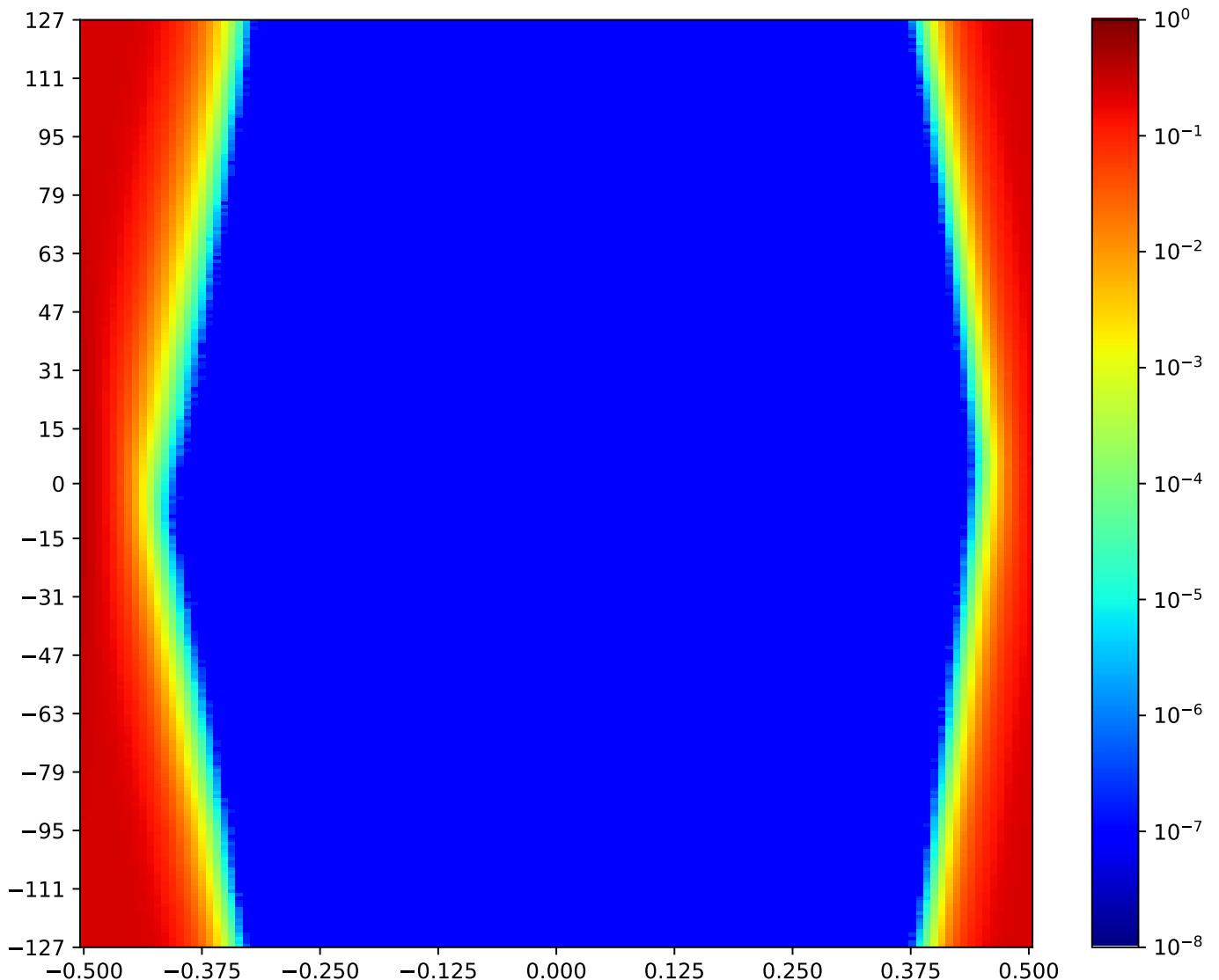


Figure 1.36: MSP\_C\_FPGA-TX3-08-RX7-08-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.10 MSP\_C\_FPGA-TX3-09-RX7-09-MSP\_A\_FPGA

Table 1.34: MSP\_C\_FPGA-TX3-09-RX7-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:31:04		2018-Jan-24 03:32:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25299	108	83.72%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

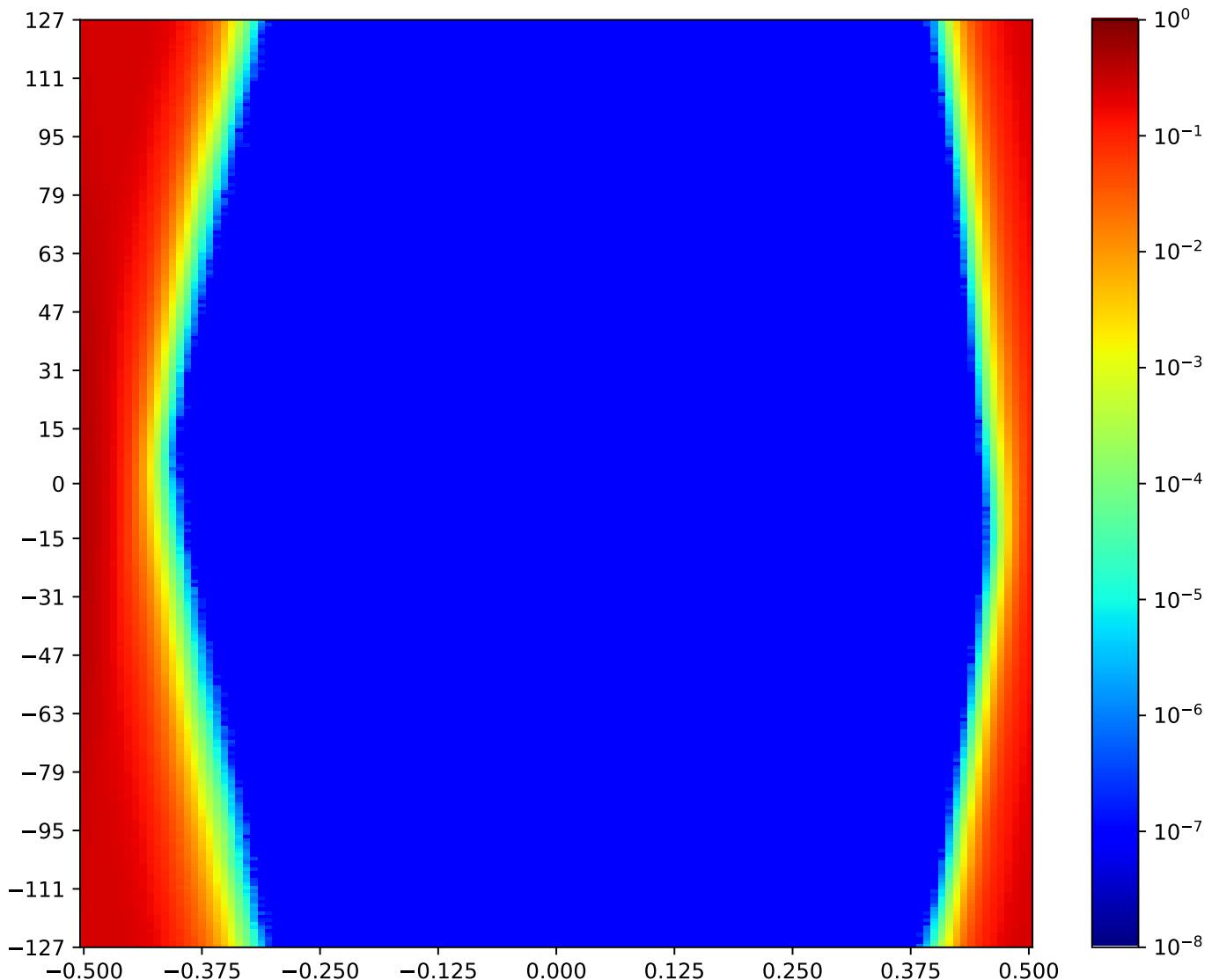


Figure 1.37: MSP\_C\_FPGA-TX3-09-RX7-09-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.11 MSP\_C\_FPGA-TX3-10-RX7-10-MSP\_A\_FPGA

Table 1.35: MSP\_C\_FPGA-TX3-10-RX7-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:35:45		2018-Jan-24 03:36:56	
Reset RX	OA	HO		HO (%)	
true	25247	110		85.27%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

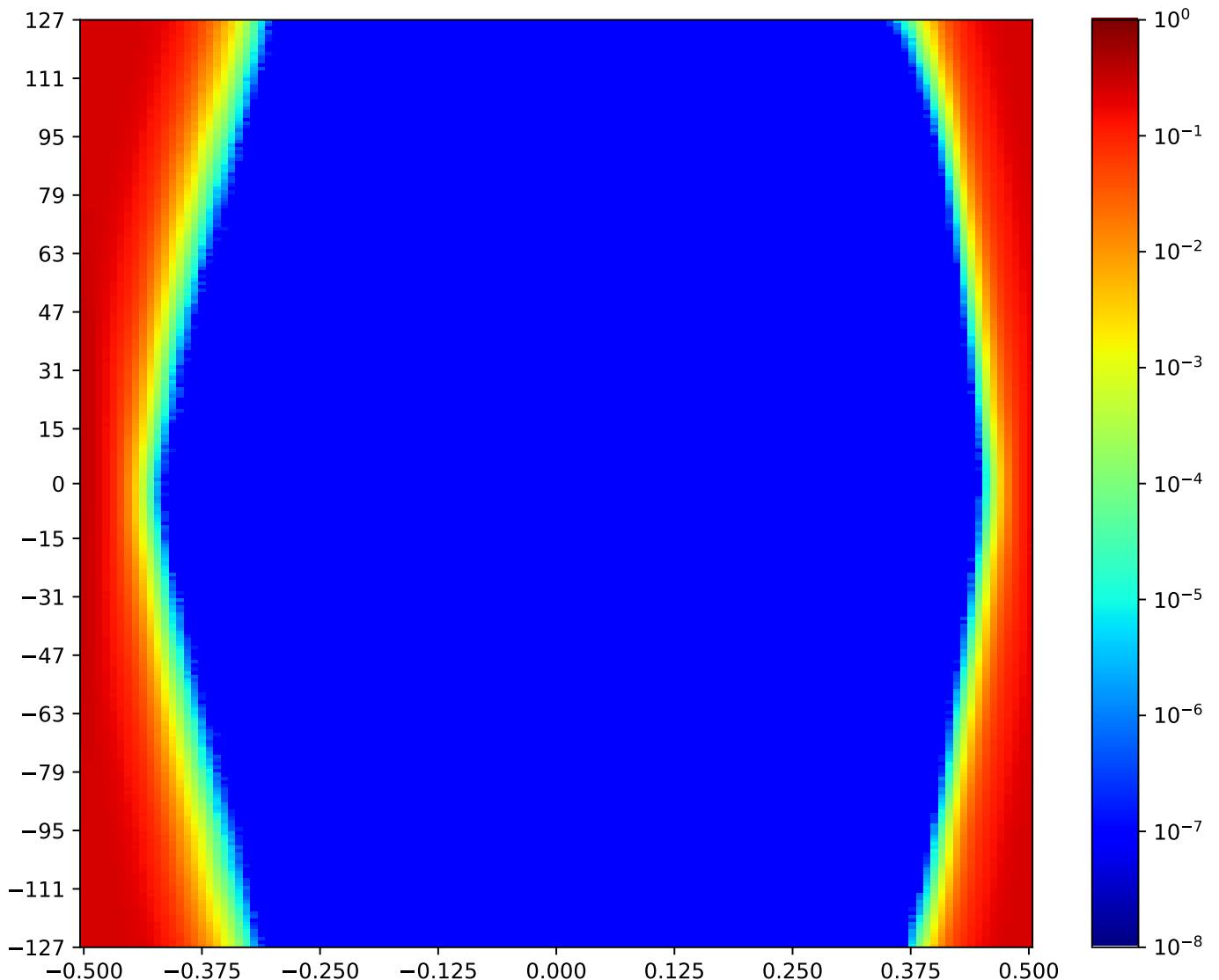


Figure 1.38: MSP\_C\_FPGA-TX3-10-RX7-10-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.3.12 MSP\_C\_FPGA-TX3-11-RX7-11-MSP\_A\_FPGA

Table 1.36: MSP\_C\_FPGA-TX3-11-RX7-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:34:35		2018-Jan-24 03:35:45	
Reset RX	OA	HO		HO (%)	
true	23369	105		81.40%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

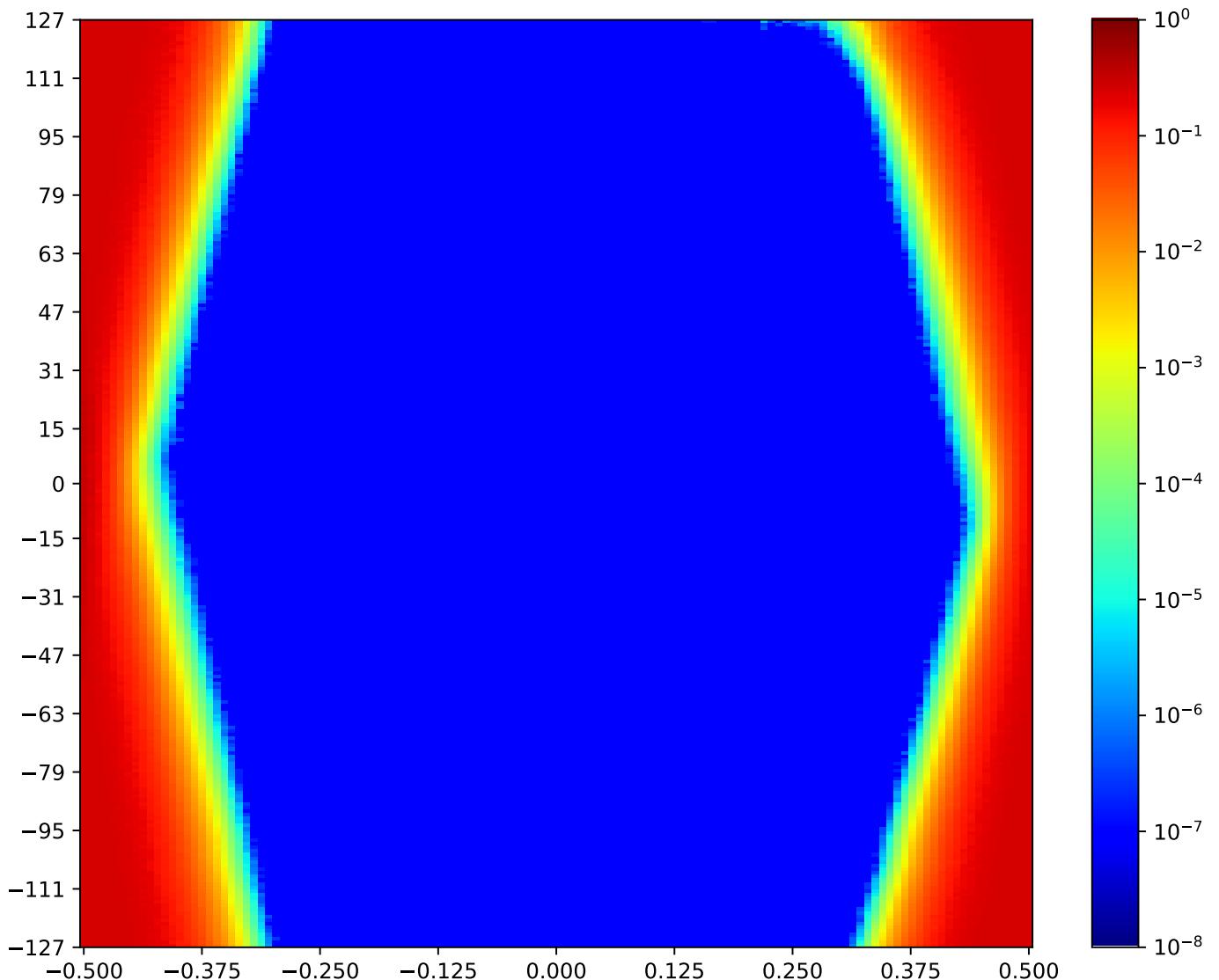


Figure 1.39: MSP\_C\_FPGA-TX3-11-RX7-11-MSP\_A\_FPGA

Call back to summary Figure 1.27. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.4 MSP\_C TX4 MSP\_A RX6 Minipod Loopback

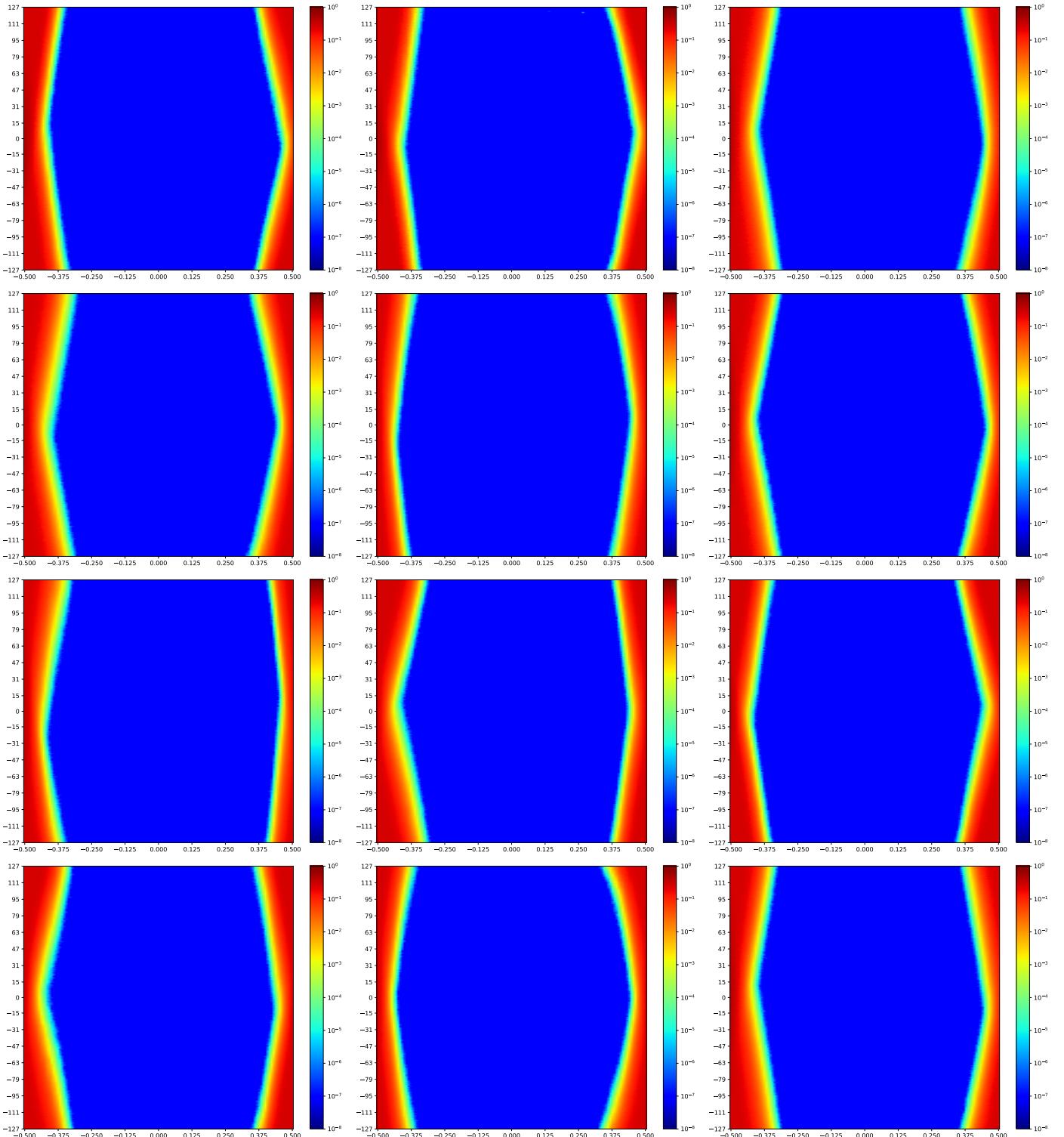


Figure 1.40: MSP\_C TX4 MSP\_A RX6 Minipod Loopback

A cross-reference to Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.53.

#### 1.4.1 MSP\_C\_FPGA-TX4-00-RX6-00-MSP\_A\_FPGA

Table 1.37: MSP\_C\_FPGA-TX4-00-RX6-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:44:00		2018-Jan-24 03:45:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24953	107	82.95%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

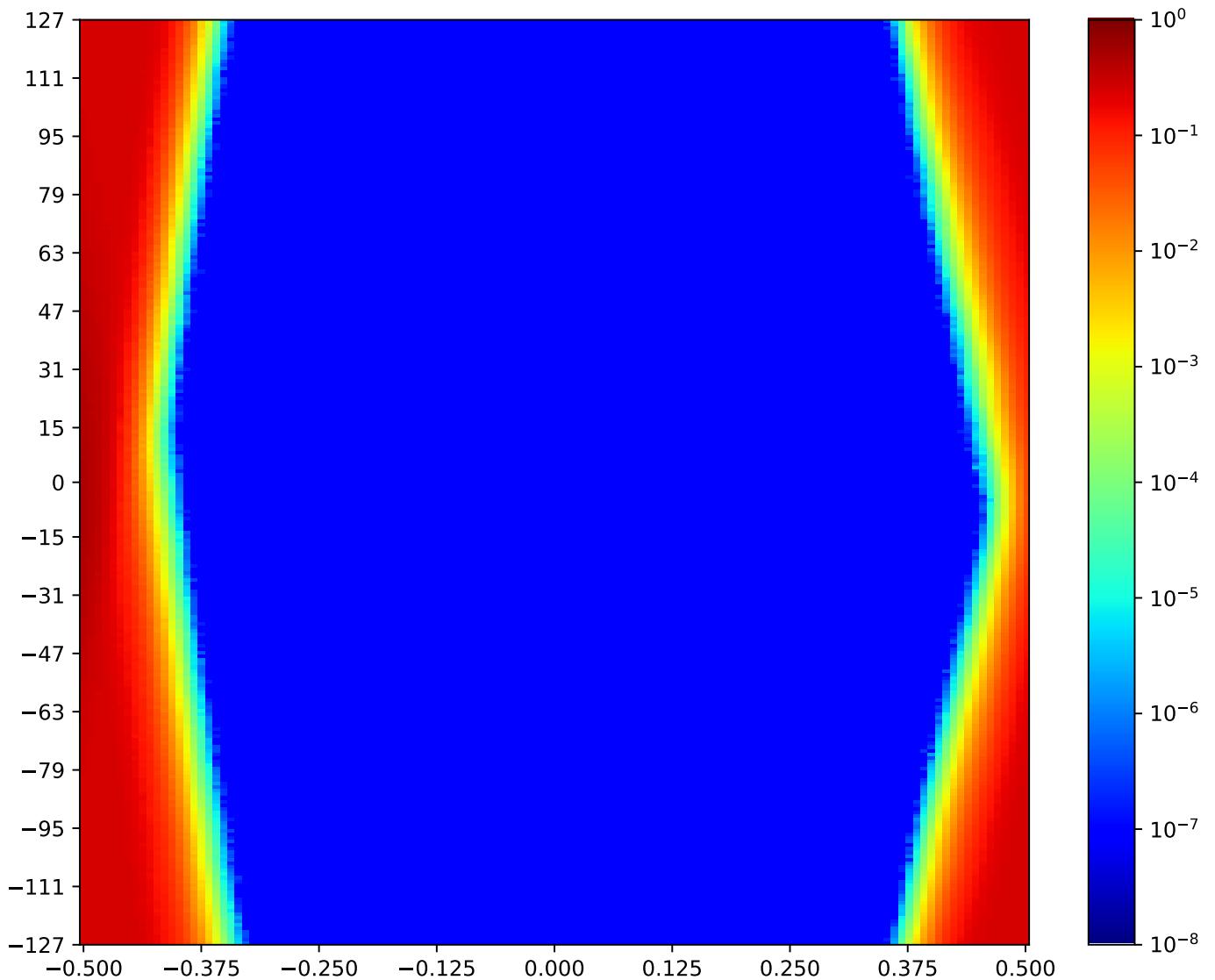


Figure 1.41: MSP\_C\_FPGA-TX4-00-RX6-00-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.2 MSP\_C\_FPGA-TX4-01-RX6-01-MSP\_A\_FPGA

Table 1.38: MSP\_C\_FPGA-TX4-01-RX6-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:41:39		2018-Jan-24 03:42:49	
Reset RX	OA	HO		HO (%)	
true	24589	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

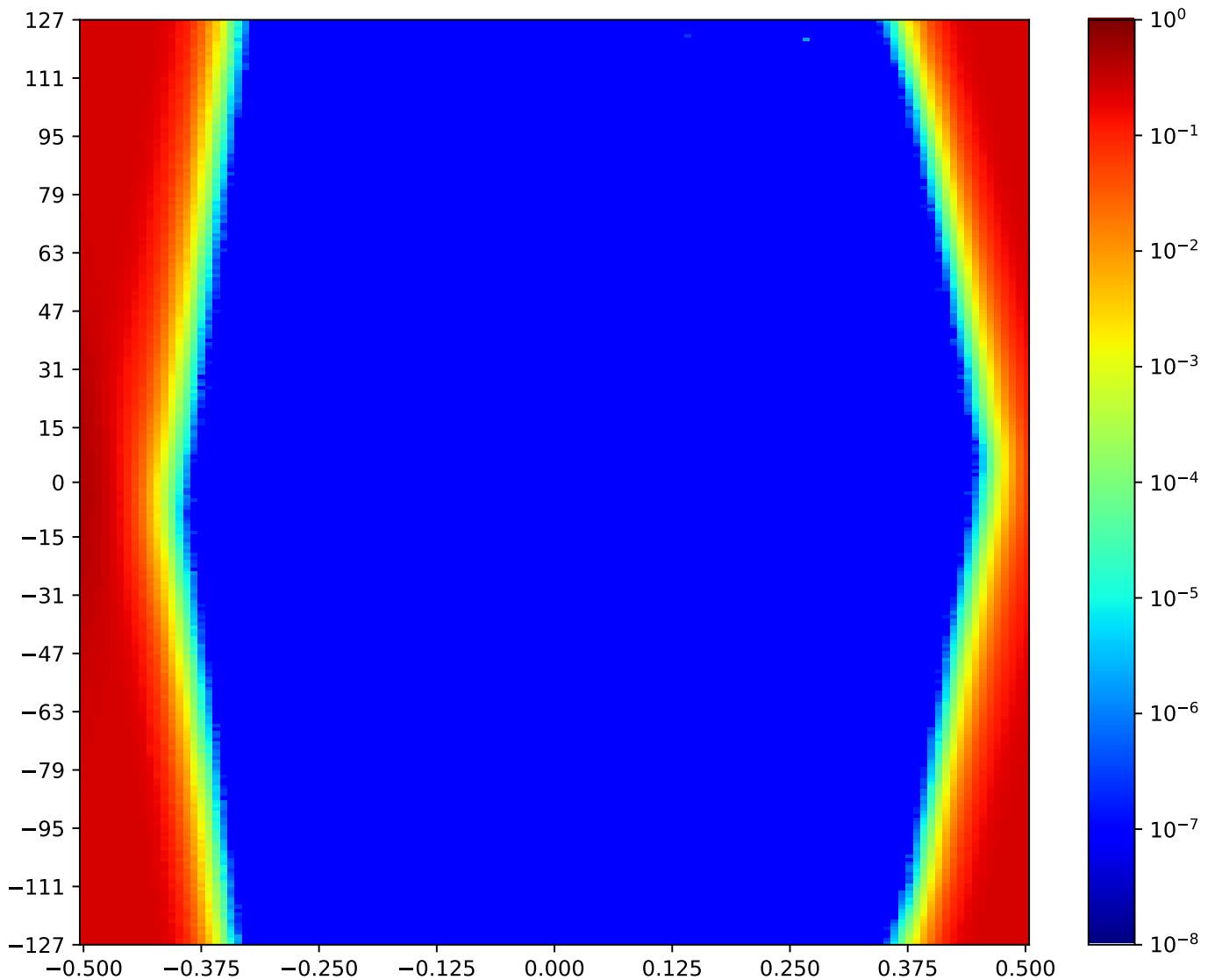


Figure 1.42: MSP\_C\_FPGA-TX4-01-RX6-01-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.4.3 MSP\_C\_FPGA-TX4-02-RX6-02-MSP\_A\_FPGA

Table 1.39: MSP\_C\_FPGA-TX4-02-RX6-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:47:33		2018-Jan-24 03:48:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23831	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

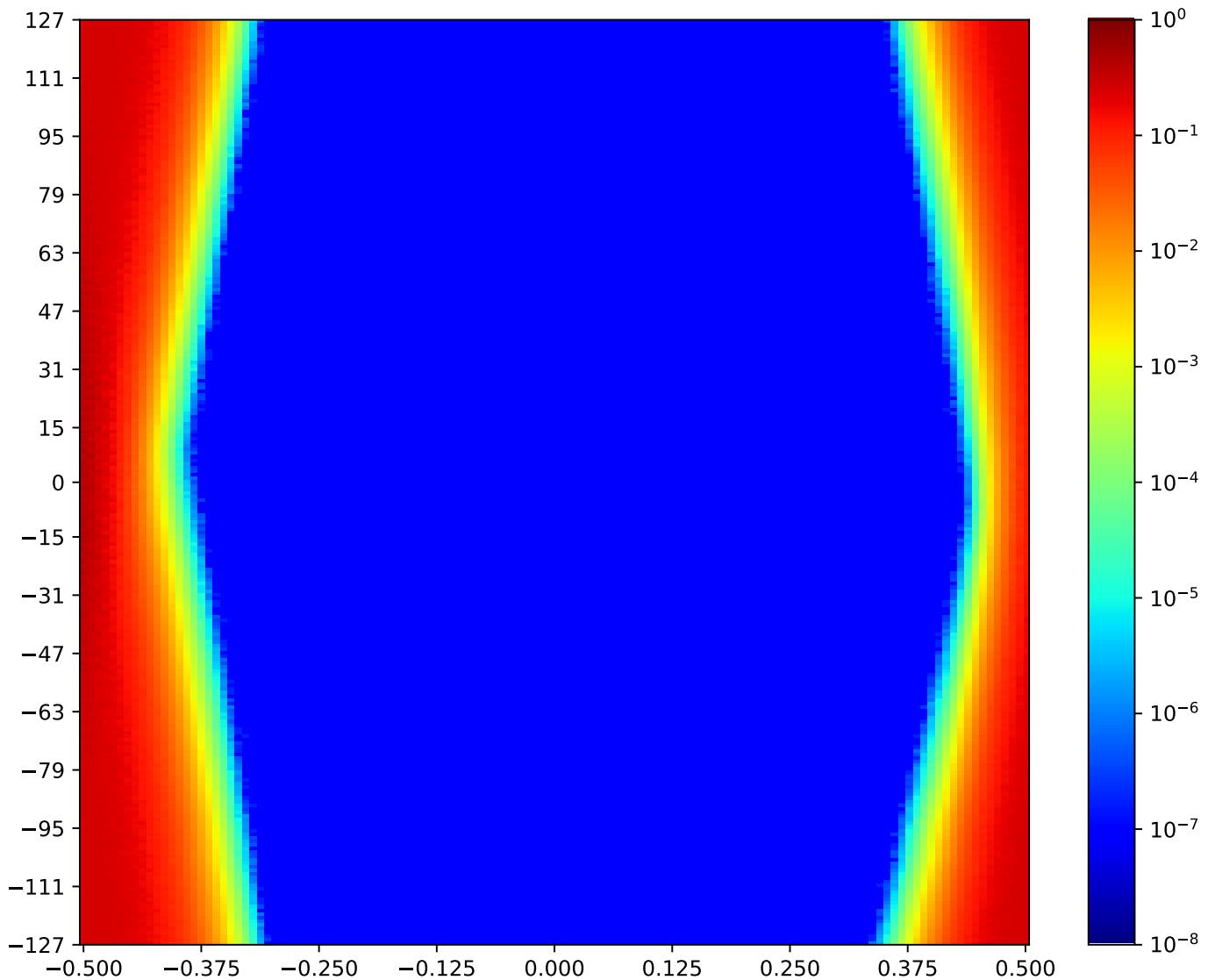


Figure 1.43: MSP\_C\_FPGA-TX4-02-RX6-02-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.4 MSP\_C\_FPGA-TX4-03-RX6-03-MSP\_A\_FPGA

Table 1.40: MSP\_C\_FPGA-TX4-03-RX6-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:40:29		2018-Jan-24 03:41:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23501	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

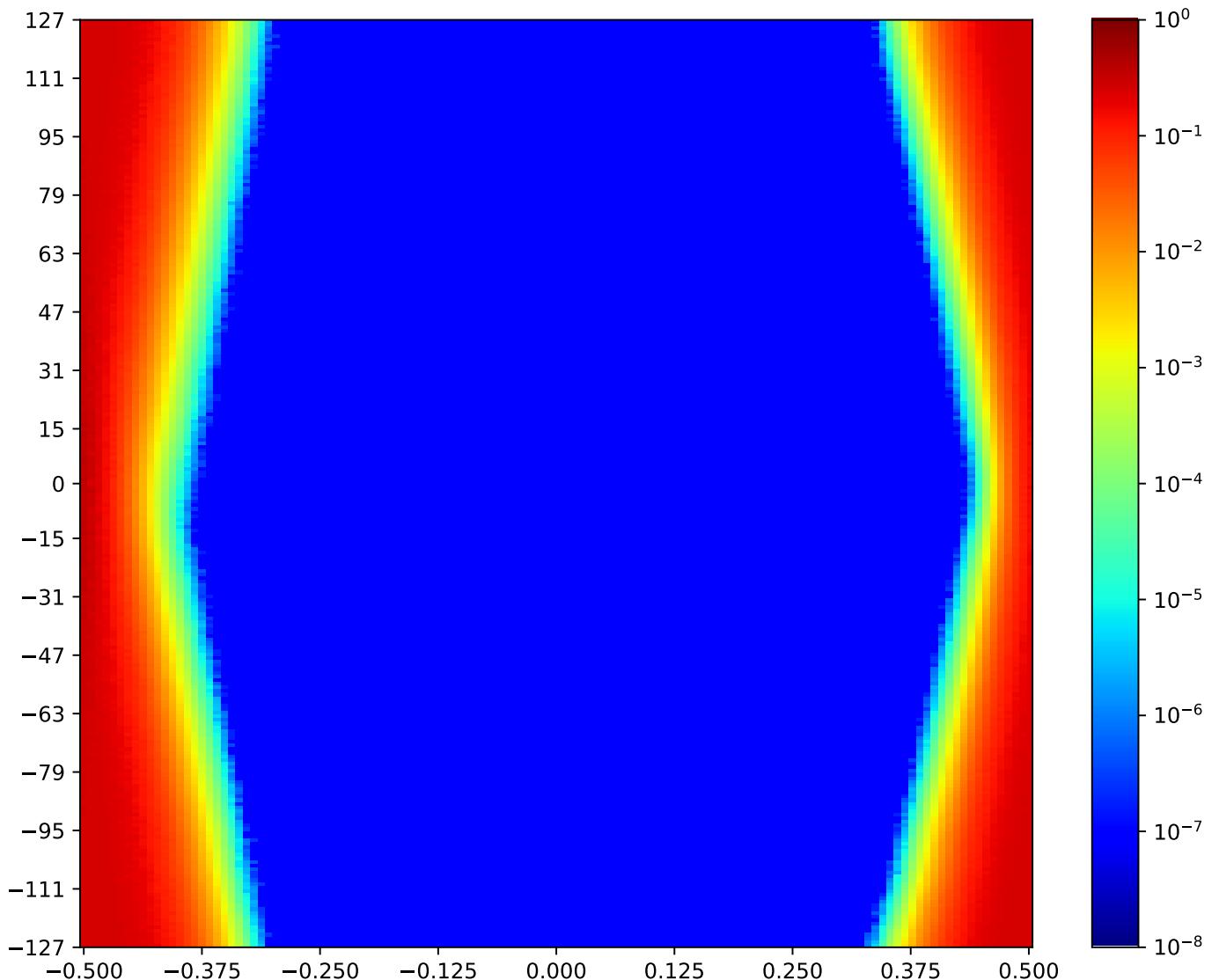


Figure 1.44: MSP\_C\_FPGA-TX4-03-RX6-03-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.5 MSP\_C\_FPGA-TX4-04-RX6-04-MSP\_A\_FPGA

Table 1.41: MSP\_C\_FPGA-TX4-04-RX6-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:51:04		2018-Jan-24 03:52:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25545	107	82.95%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

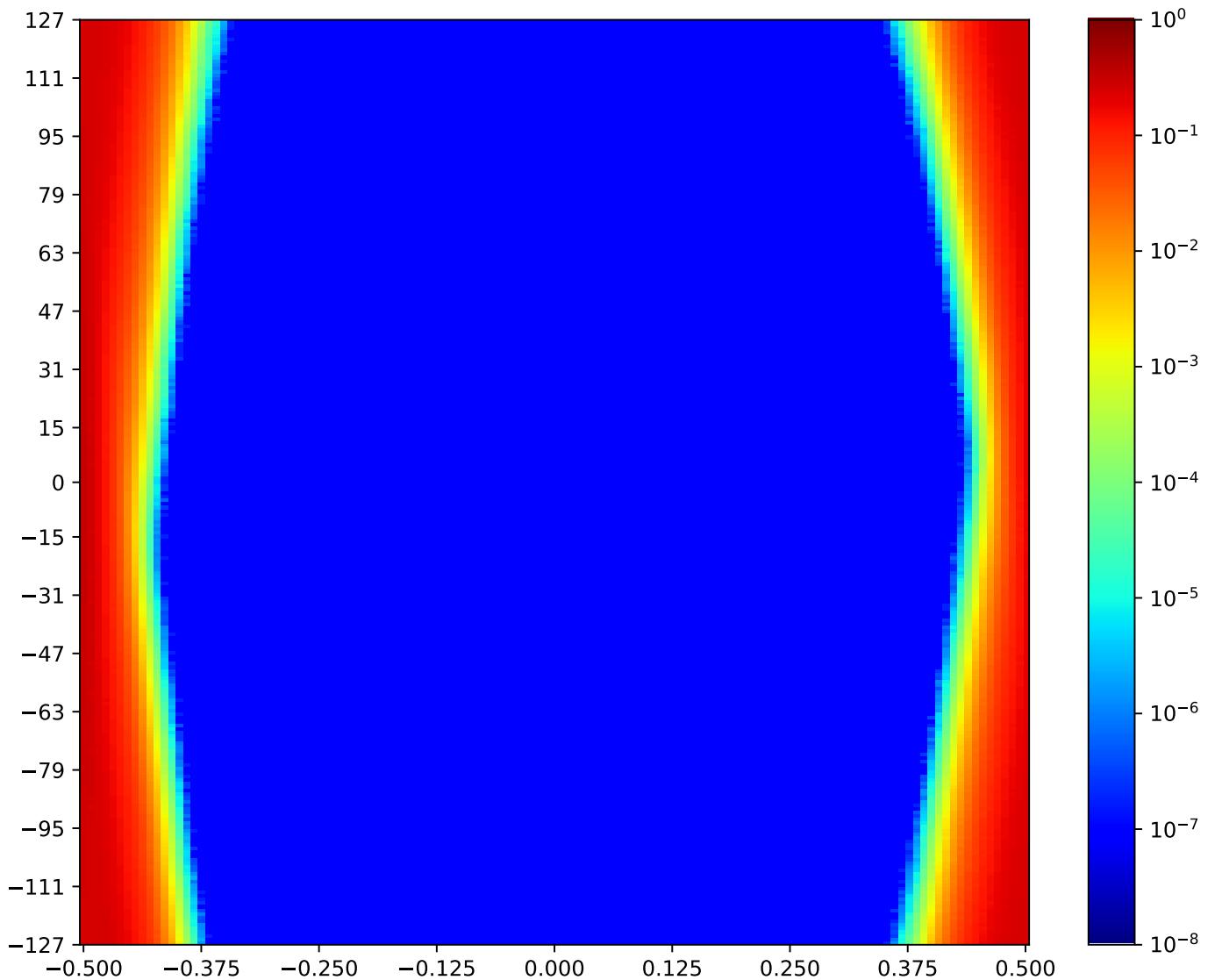


Figure 1.45: MSP\_C\_FPGA-TX4-04-RX6-04-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.6 MSP\_C\_FPGA-TX4-05-RX6-05-MSP\_A\_FPGA

Table 1.42: MSP\_C\_FPGA-TX4-05-RX6-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:42:49		2018-Jan-24 03:44:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24175	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

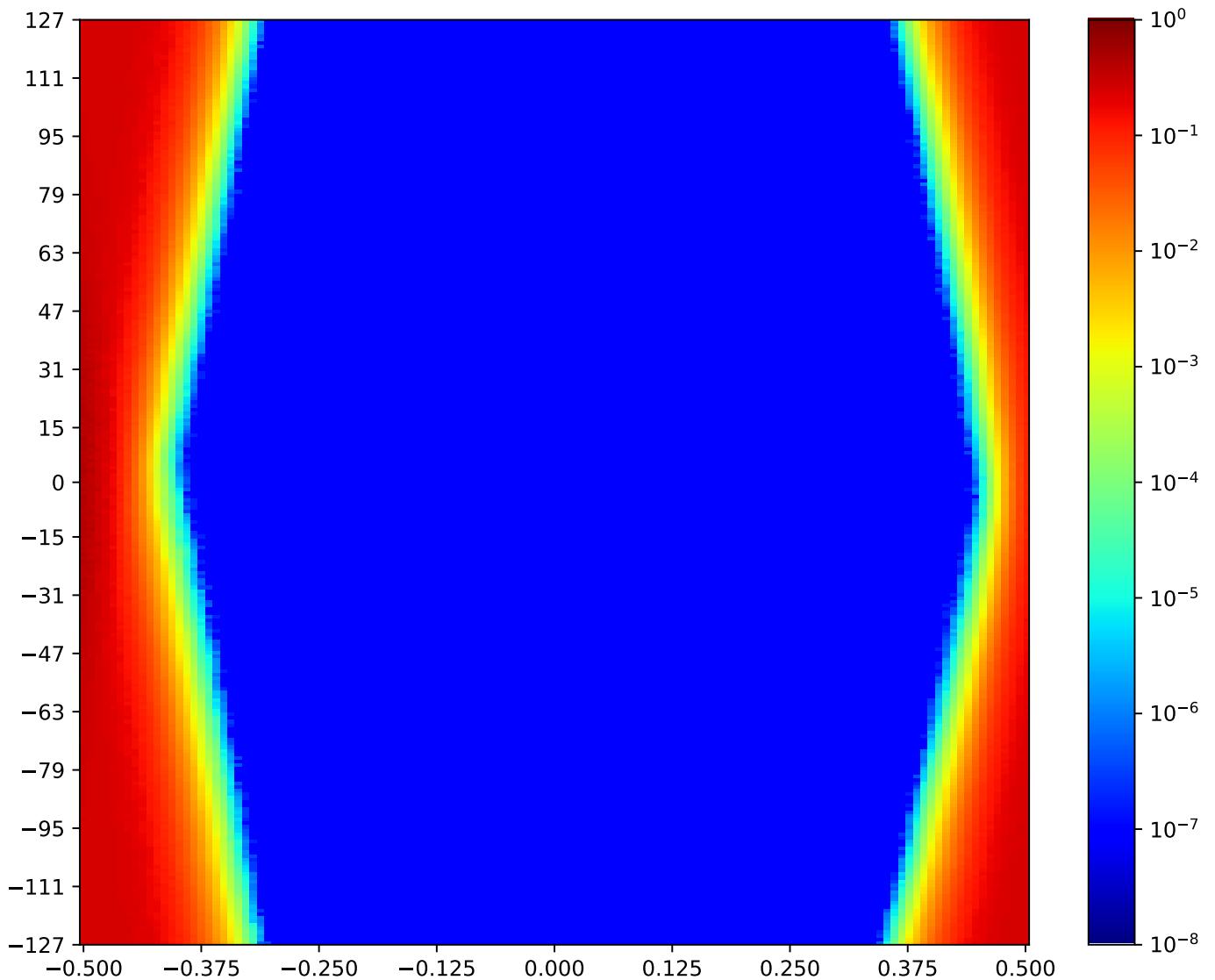


Figure 1.46: MSP\_C\_FPGA-TX4-05-RX6-05-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.7 MSP\_C\_FPGA-TX4-06-RX6-06-MSP\_A\_FPGA

Table 1.43: MSP\_C\_FPGA-TX4-06-RX6-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:53:26		2018-Jan-24 03:54:38	
Reset RX	OA	HO		HO (%)	
true	25715	107		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

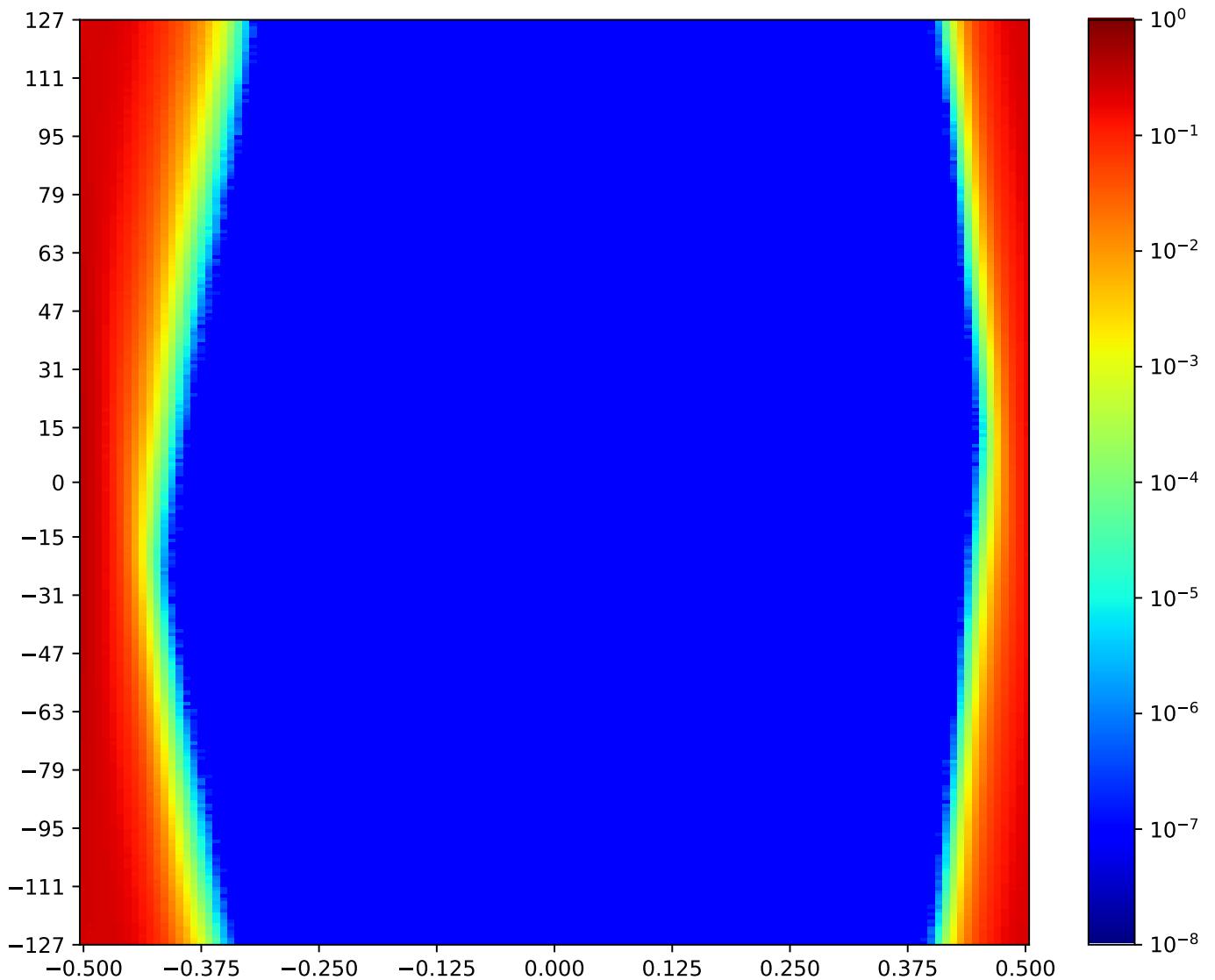


Figure 1.47: MSP\_C\_FPGA-TX4-06-RX6-06-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.8 MSP\_C\_FPGA-TX4-07-RX6-07-MSP\_A\_FPGA

Table 1.44: MSP\_C\_FPGA-TX4-07-RX6-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:45:11		2018-Jan-24 03:46:22	
Reset RX	OA	HO		HO (%)	
true	24237	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

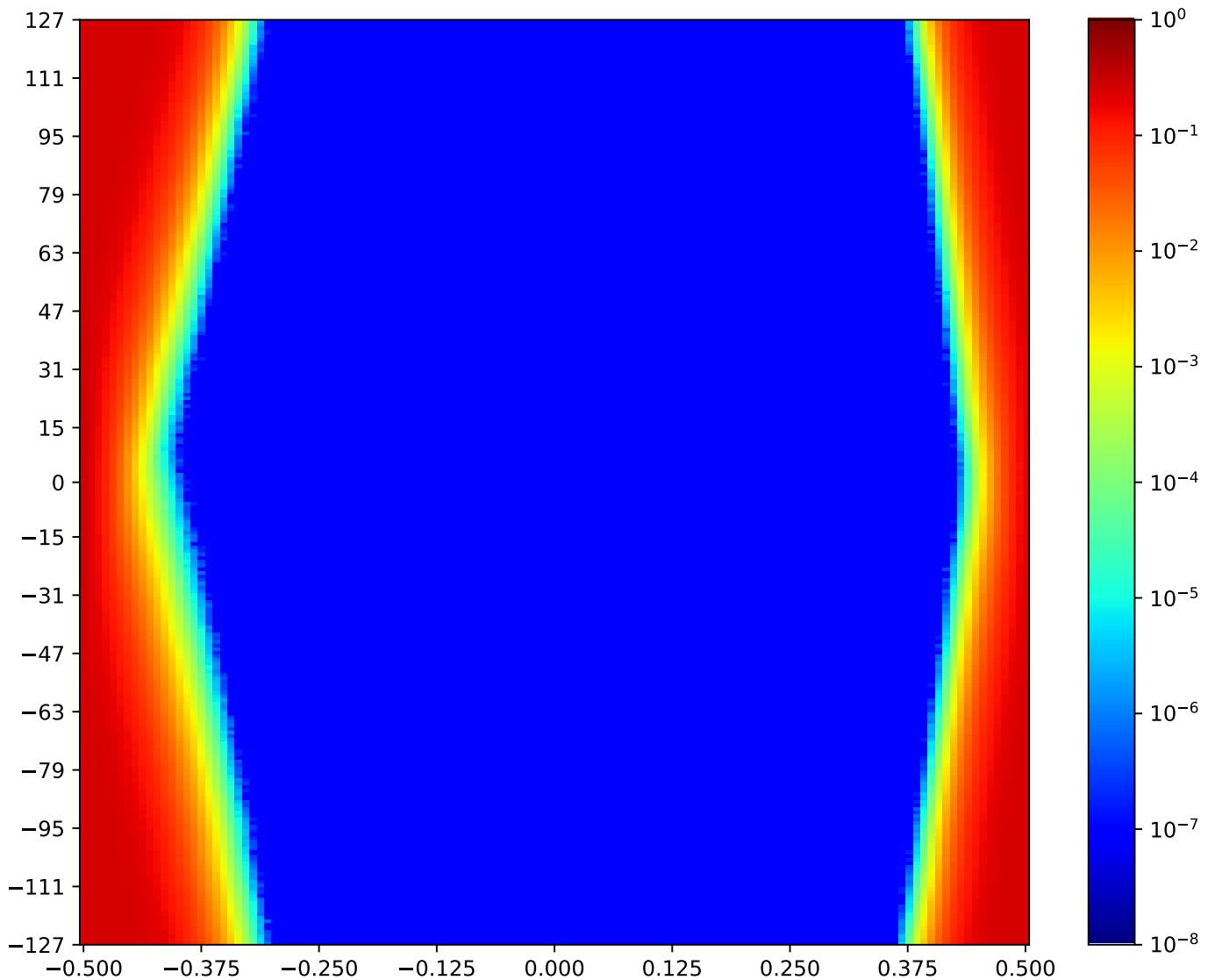


Figure 1.48: MSP\_C\_FPGA-TX4-07-RX6-07-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.9 MSP\_C\_FPGA-TX4-08-RX6-08-MSP\_A\_FPGA

Table 1.45: MSP\_C\_FPGA-TX4-08-RX6-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:52:15		2018-Jan-24 03:53:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24361	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

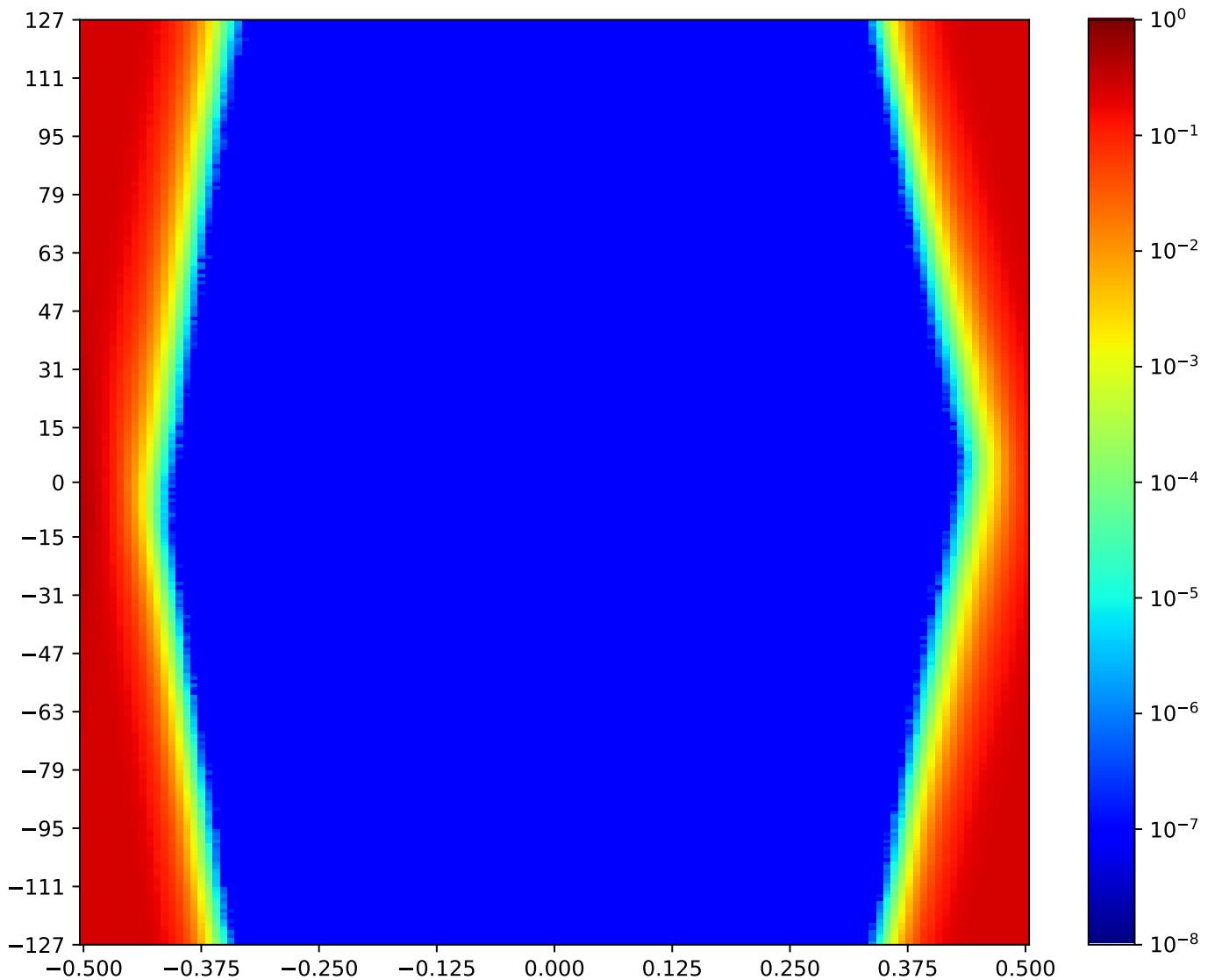


Figure 1.49: MSP\_C\_FPGA-TX4-08-RX6-08-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.10 MSP\_C\_FPGA-TX4-09-RX6-09-MSP\_A\_FPGA

Table 1.46: MSP\_C\_FPGA-TX4-09-RX6-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:46:22		2018-Jan-24 03:47:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24115	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

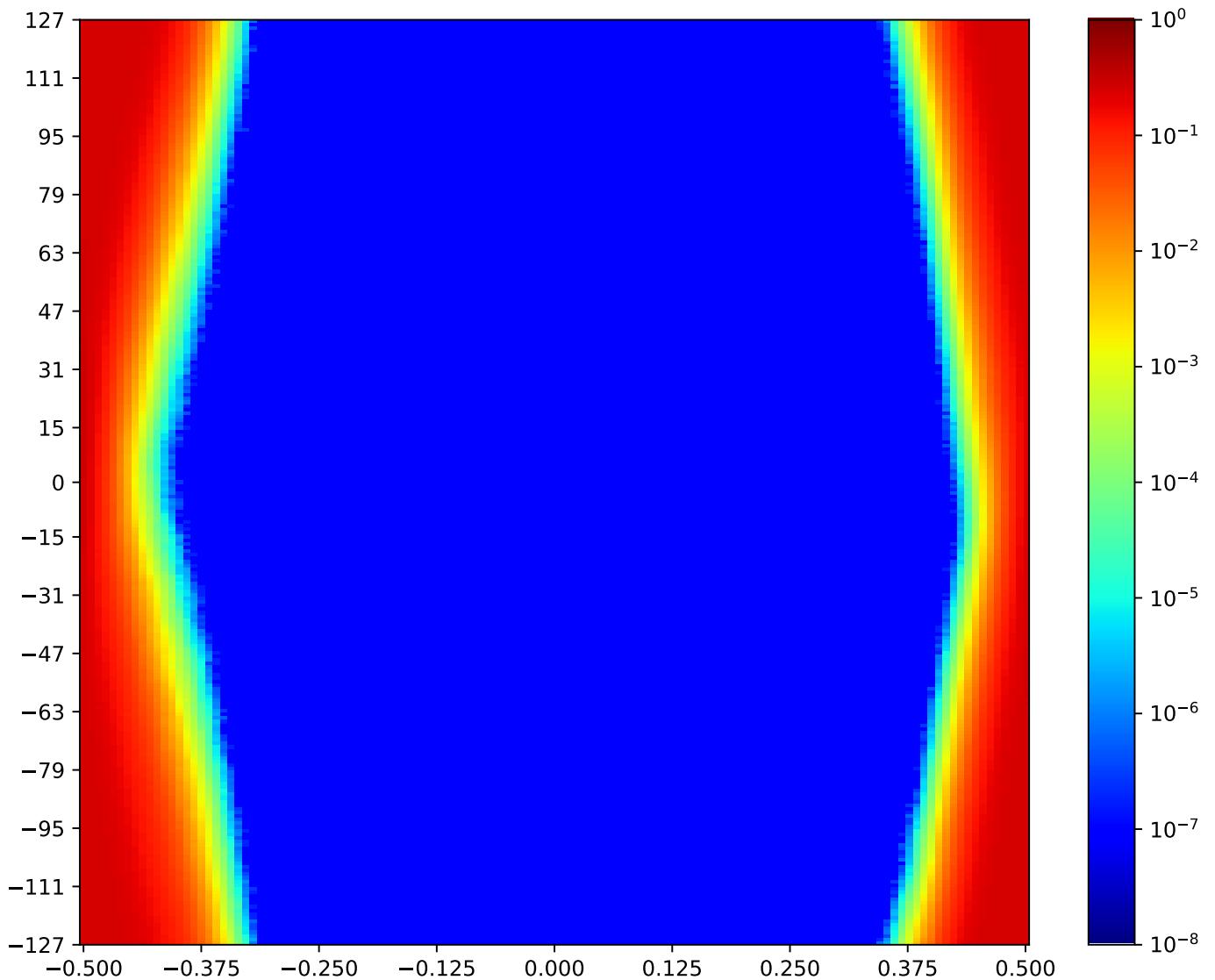


Figure 1.50: MSP\_C\_FPGA-TX4-09-RX6-09-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.11 MSP\_C\_FPGA-TX4-10-RX6-10-MSP\_A\_FPGA

Table 1.47: MSP\_C\_FPGA-TX4-10-RX6-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:49:53		2018-Jan-24 03:51:04	
Reset RX	OA	HO		VO   VO (%)	
true	25295	110		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

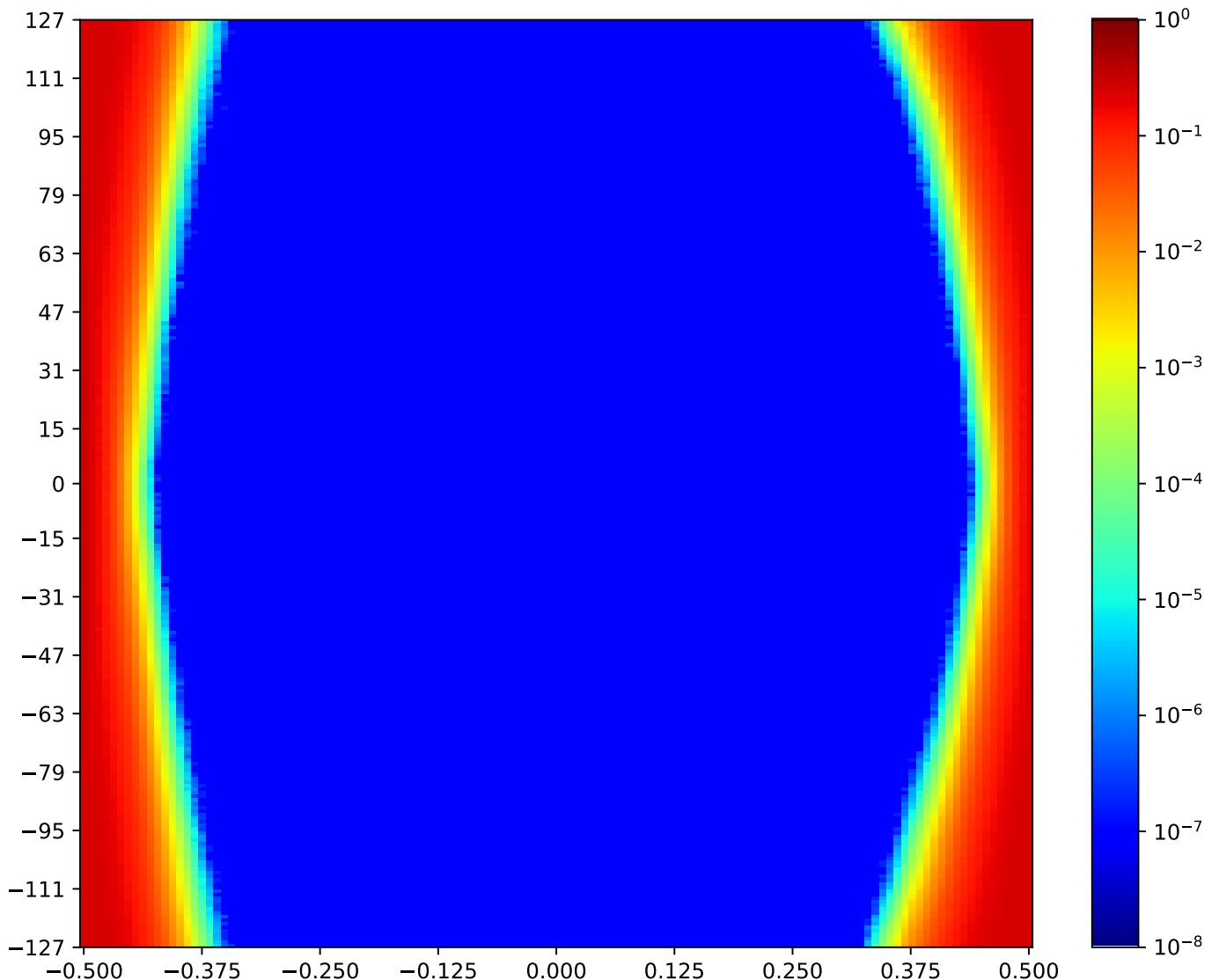


Figure 1.51: MSP\_C\_FPGA-TX4-10-RX6-10-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.4.12 MSP\_C\_FPGA-TX4-11-RX6-11-MSP\_A\_FPGA

Table 1.48: MSP\_C\_FPGA-TX4-11-RX6-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:48:43		2018-Jan-24 03:49:52	
Reset RX	OA	HO		HO (%)	
true	24154	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

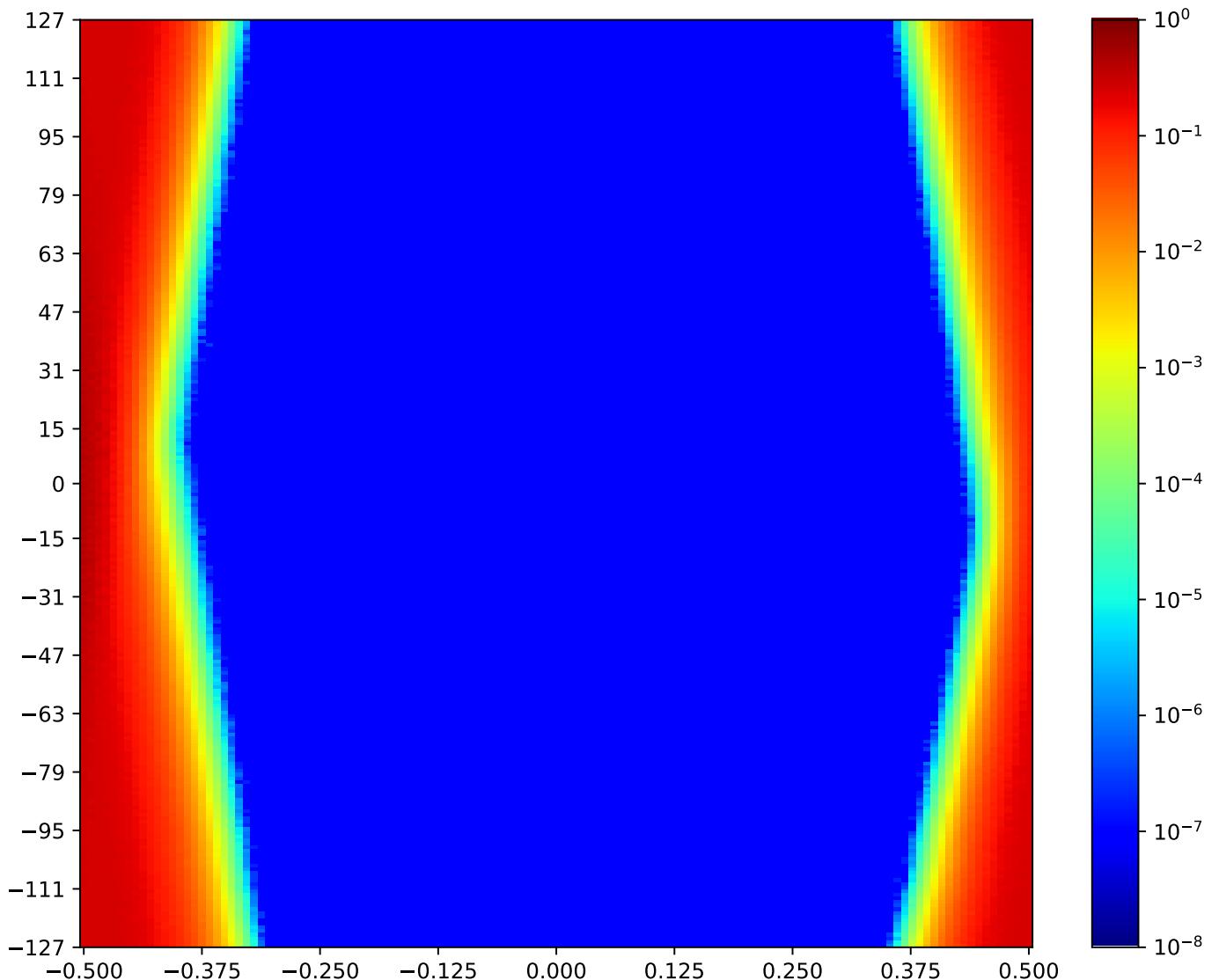


Figure 1.52: MSP\_C\_FPGA-TX4-11-RX6-11-MSP\_A\_FPGA

Call back to summary Figure 1.40. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.5 Partial TRP TX5 MSP\_A RX5 Minipod Loopback

A cross-reference to Figure 1.53. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

Next summary Figure 1.62.

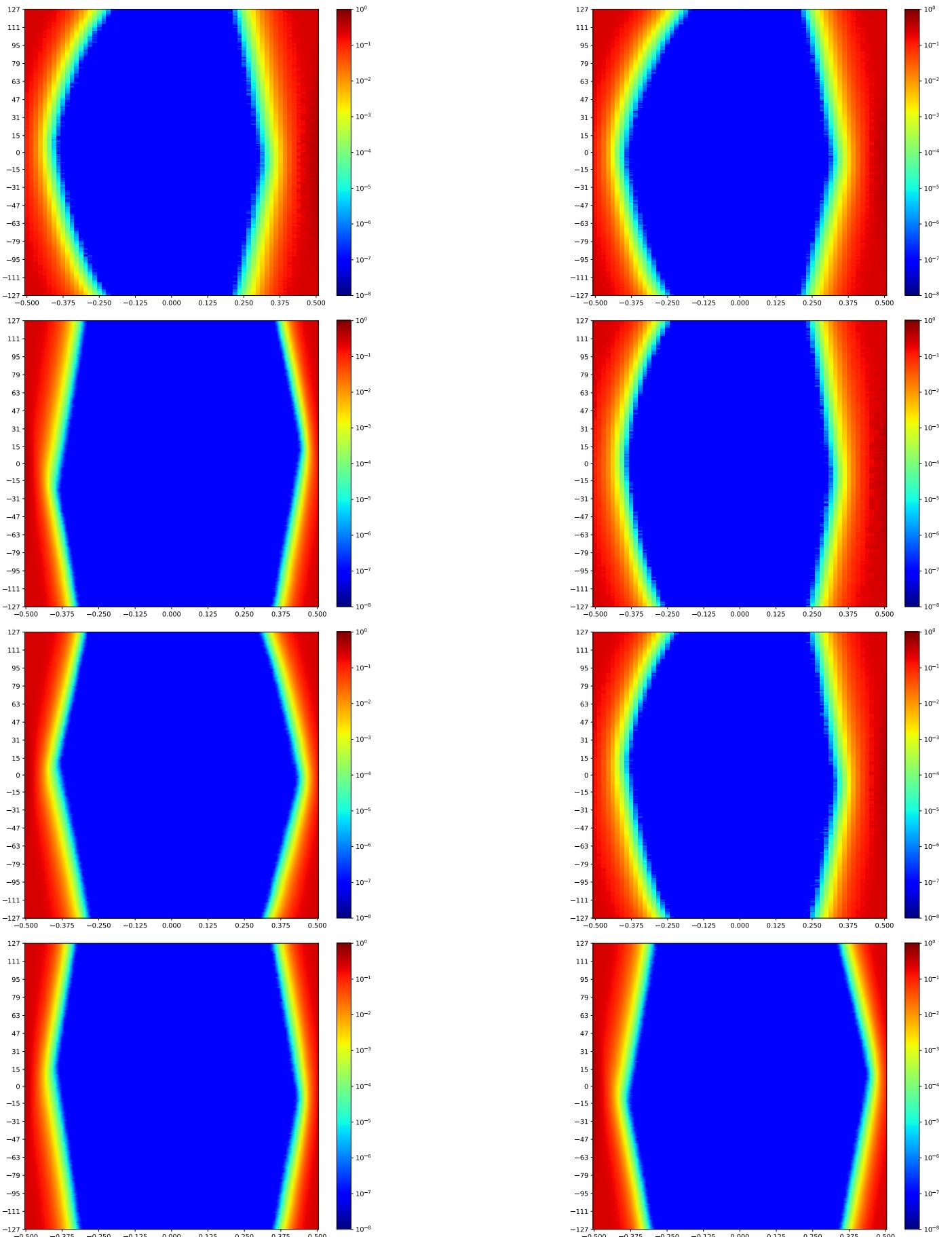


Figure 1.53: Partial TRP TX5 MSP\_A RX5 Minipod Loopback

### 1.5.1 TRP\_FPGA-TX5-00-RX5-00-MSP\_A\_FPGA

Table 1.49: TRP\_FPGA-TX5-00-RX5-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 03:56:27		2018-Jan-24 03:57:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9300	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

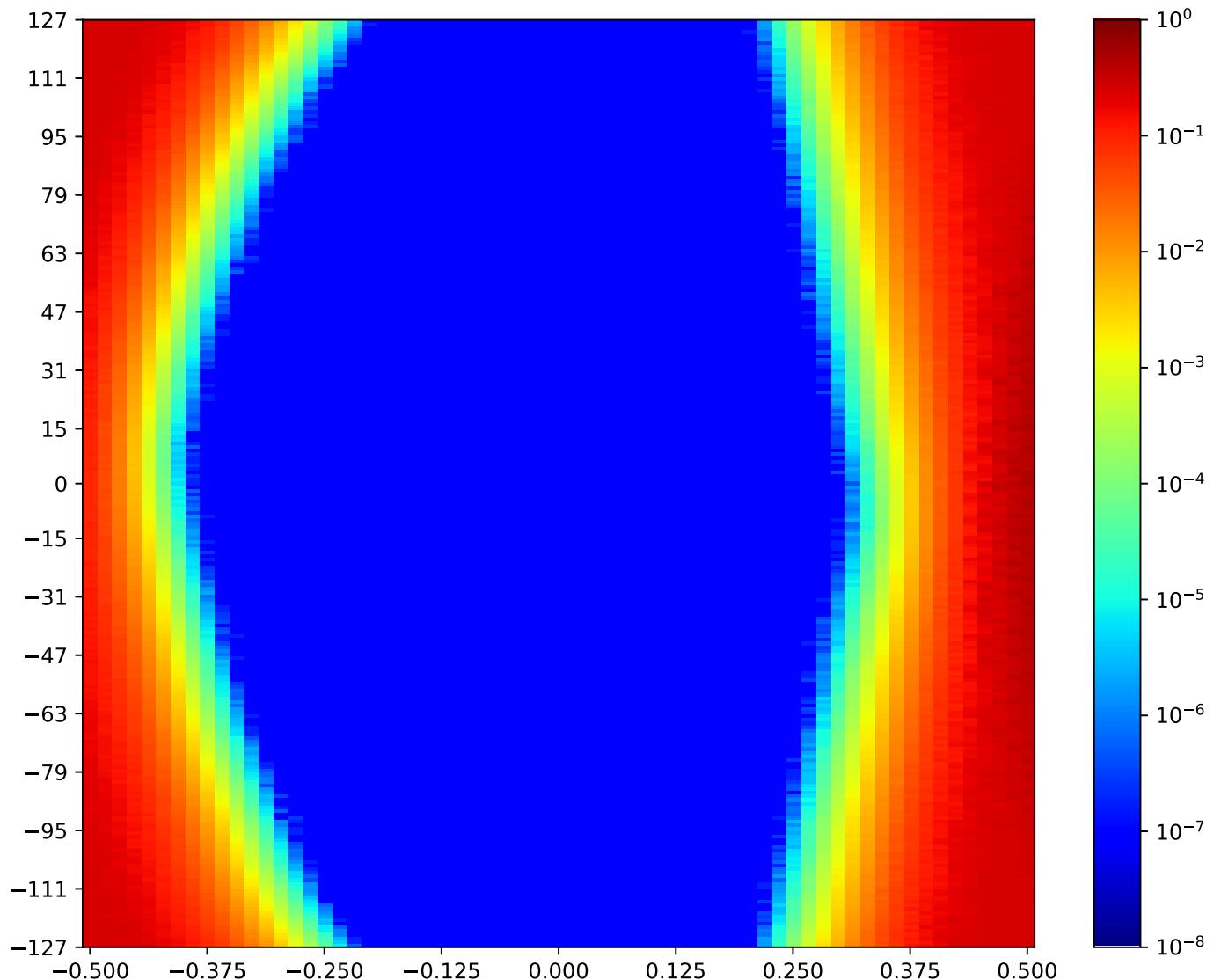


Figure 1.54: TRP\_FPGA-TX5-00-RX5-00-MSP\_A\_FPGA

Call back to summary Figure 1.53. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.5.2 TRP\_FPGA-TX5-01-RX5-01-MSP\_A\_FPGA

Table 1.50: TRP\_FPGA-TX5-01-RX5-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 03:55:14		2018-Jan-24 03:55:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9161	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

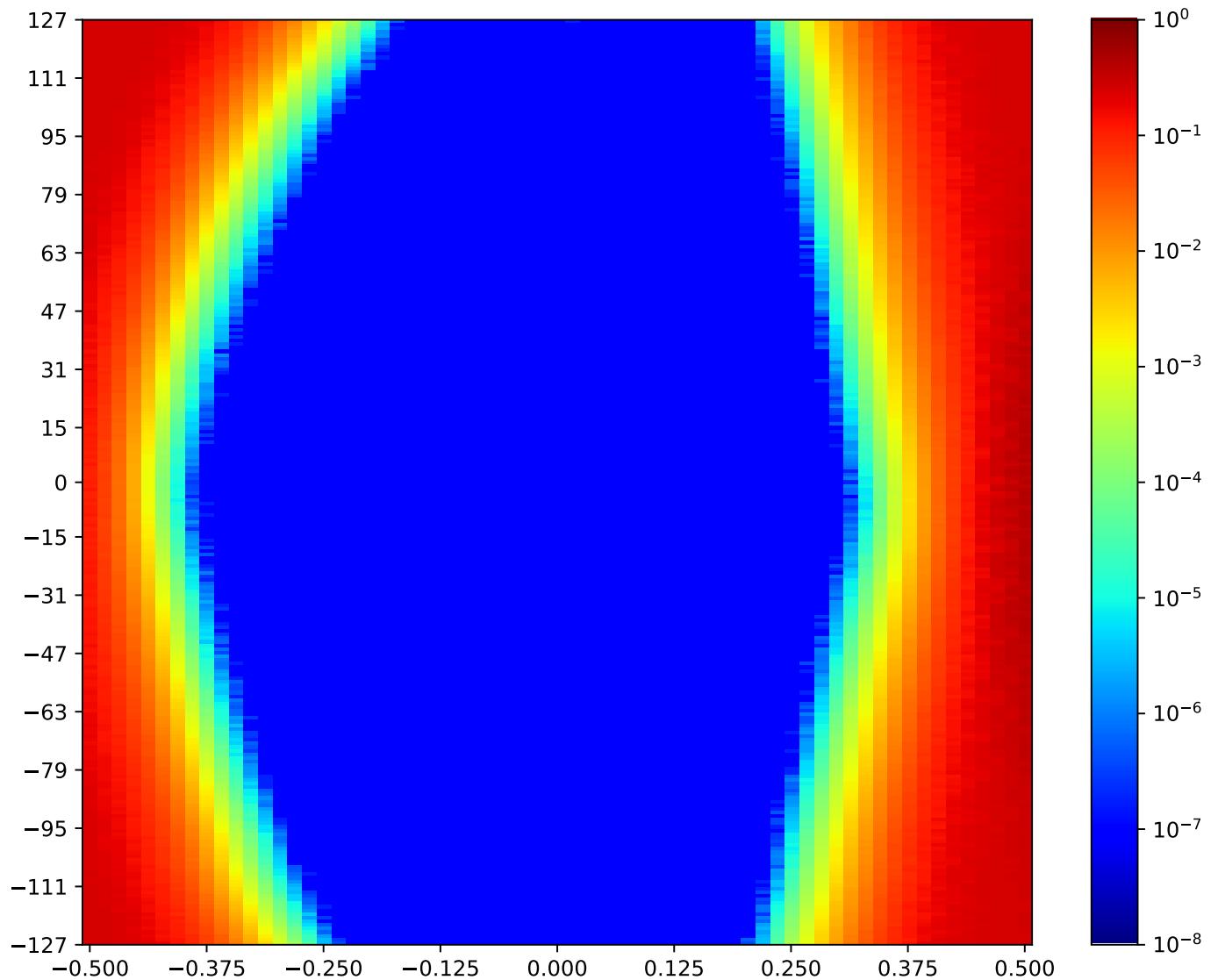


Figure 1.55: TRP\_FPGA-TX5-01-RX5-01-MSP\_A\_FPGA

Call back to summary Figure 1.53. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.5.3 TRP\_FPGA-TX5-02-RX5-02-MSP\_A\_FPGA

Table 1.51: TRP\_FPGA-TX5-02-RX5-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:58:15		2018-Jan-24 03:59:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23781	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

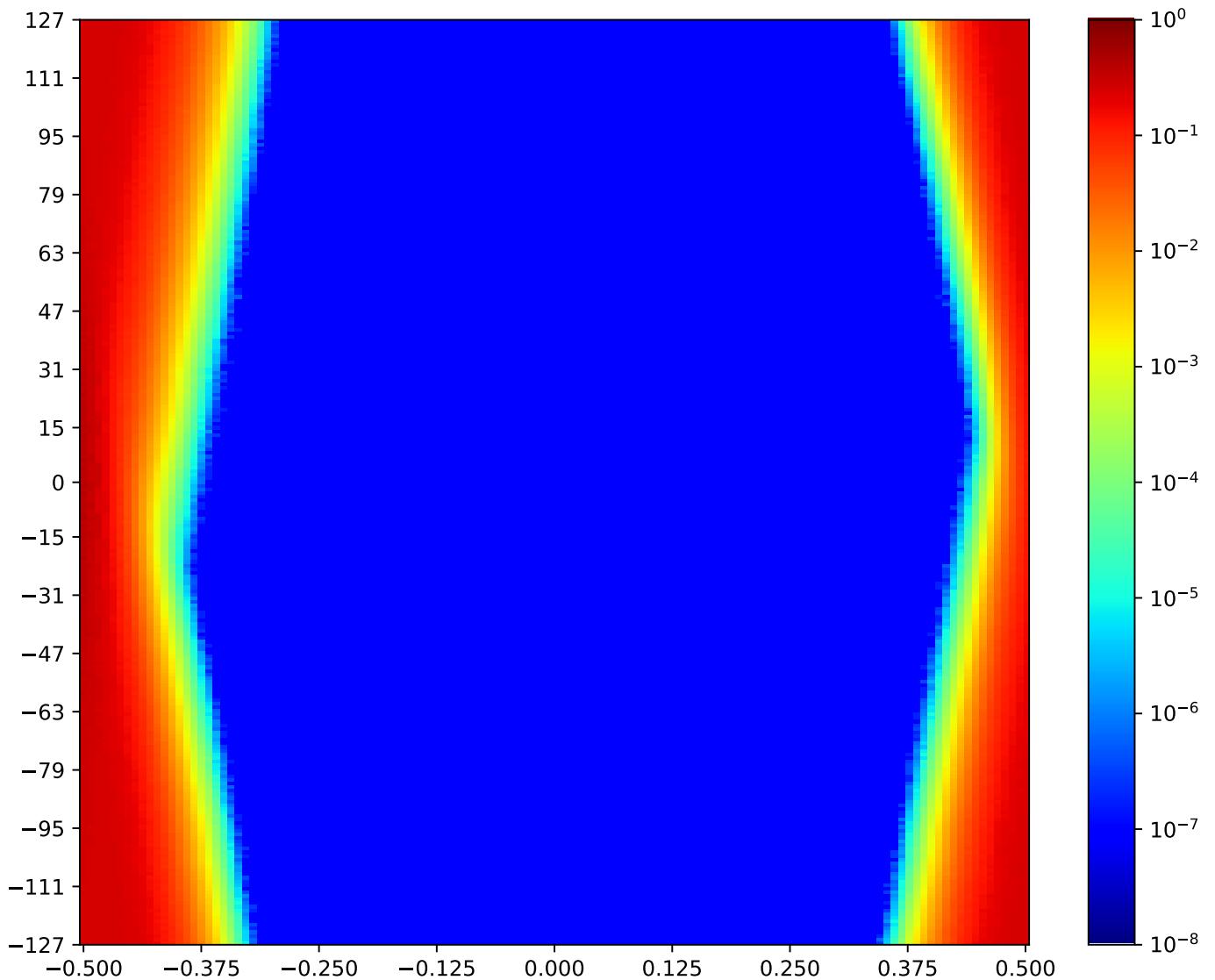


Figure 1.56: TRP\_FPGA-TX5-02-RX5-02-MSP\_A\_FPGA

Call back to summary Figure 1.53. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.5.4 TRP\_FPGA-TX5-03-RX5-03-MSP\_A\_FPGA

Table 1.52: TRP\_FPGA-TX5-03-RX5-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 03:55:50		2018-Jan-24 03:56:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9700	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

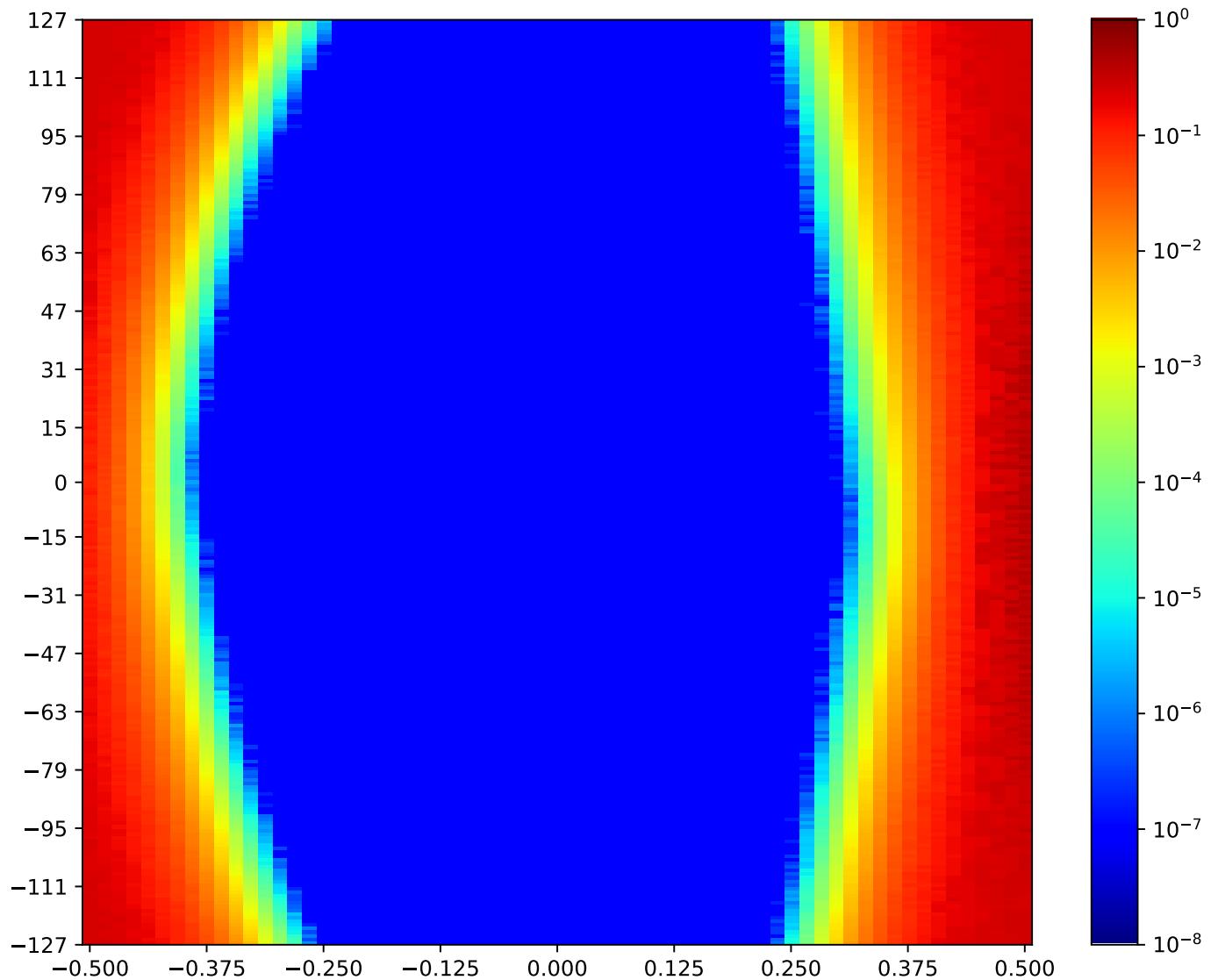


Figure 1.57: TRP\_FPGA-TX5-03-RX5-03-MSP\_A\_FPGA

Call back to summary Figure 1.53. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.5.5 TRP\_FPGA-TX5-04-RX5-04-MSP\_A\_FPGA

Table 1.53: TRP\_FPGA-TX5-04-RX5-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:00:34		2018-Jan-24 04:01:43	
Reset RX	OA	HO		HO (%)	
true	22608	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

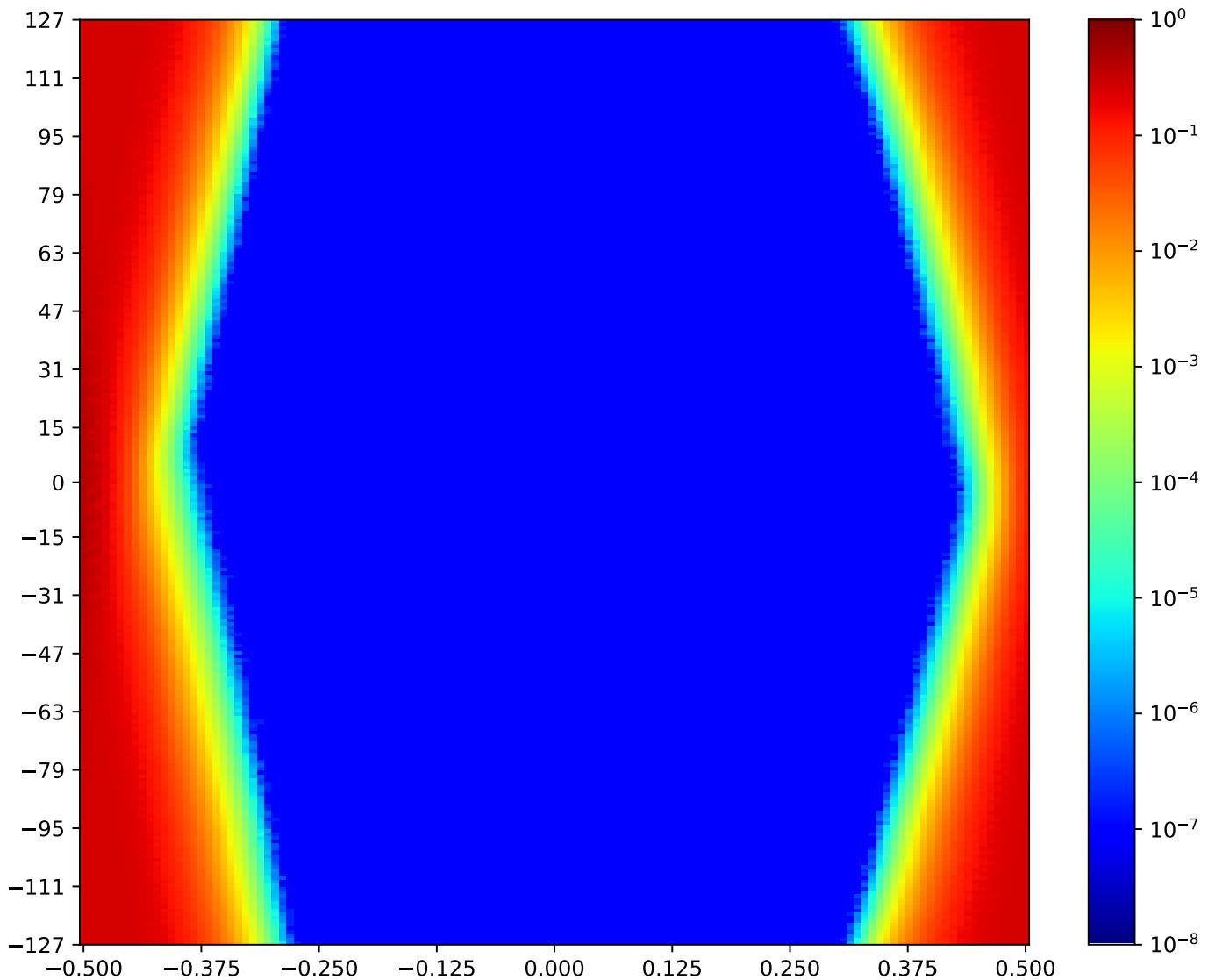


Figure 1.58: TRP\_FPGA-TX5-04-RX5-04-MSP\_A\_FPGA

Call back to summary Figure 1.53. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.5.6 TRP\_FPGA-TX5-05-RX5-05-MSP\_A\_FPGA

Table 1.54: TRP\_FPGA-TX5-05-RX5-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 03:54:38		2018-Jan-24 03:55:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9645	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

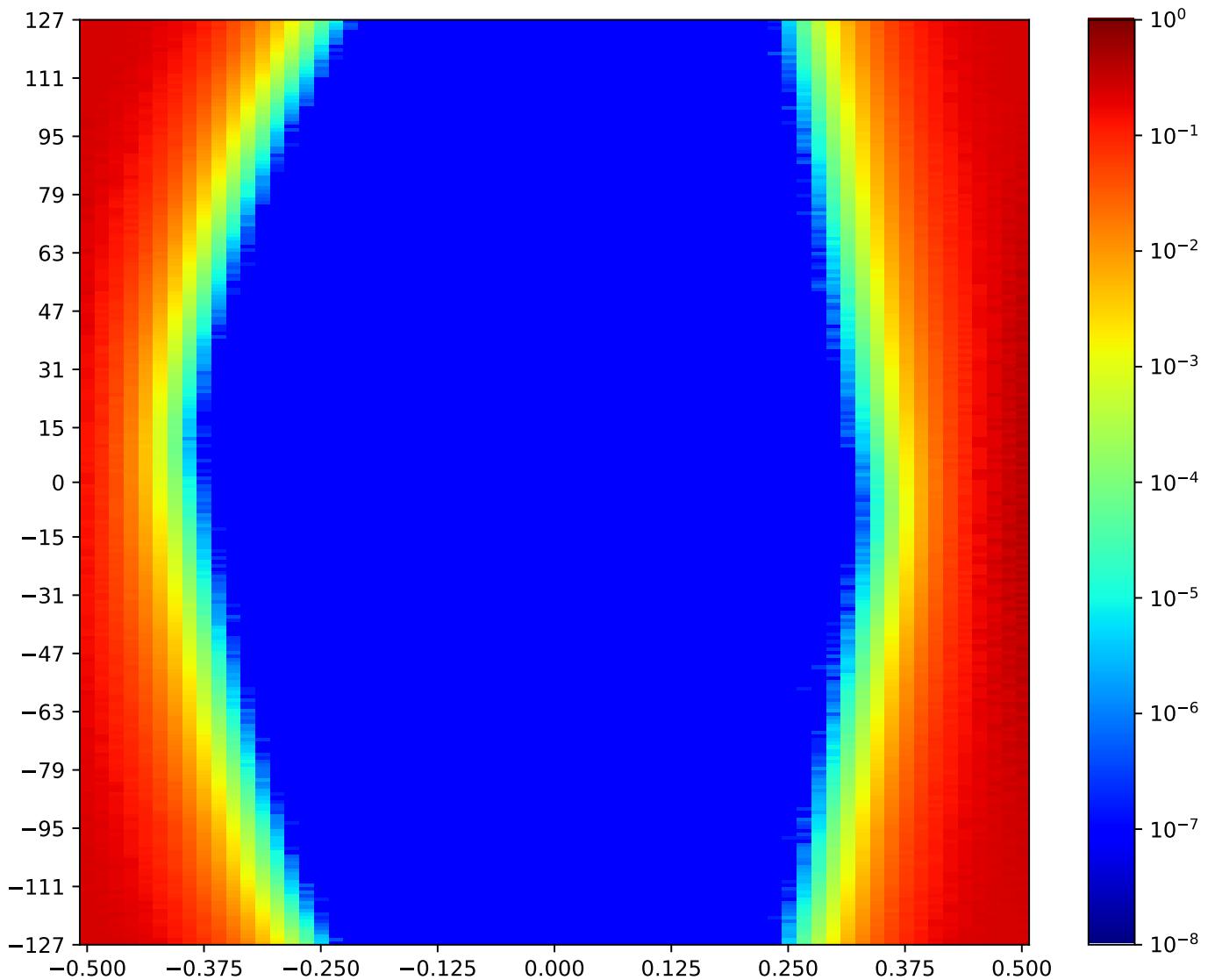


Figure 1.59: TRP\_FPGA-TX5-05-RX5-05-MSP\_A\_FPGA

Call back to summary Figure 1.53. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.5.7 TRP\_FPGA-TX5-06-RX5-06-MSP\_A\_FPGA

Table 1.55: TRP\_FPGA-TX5-06-RX5-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:57:04		2018-Jan-24 03:58:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23835	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

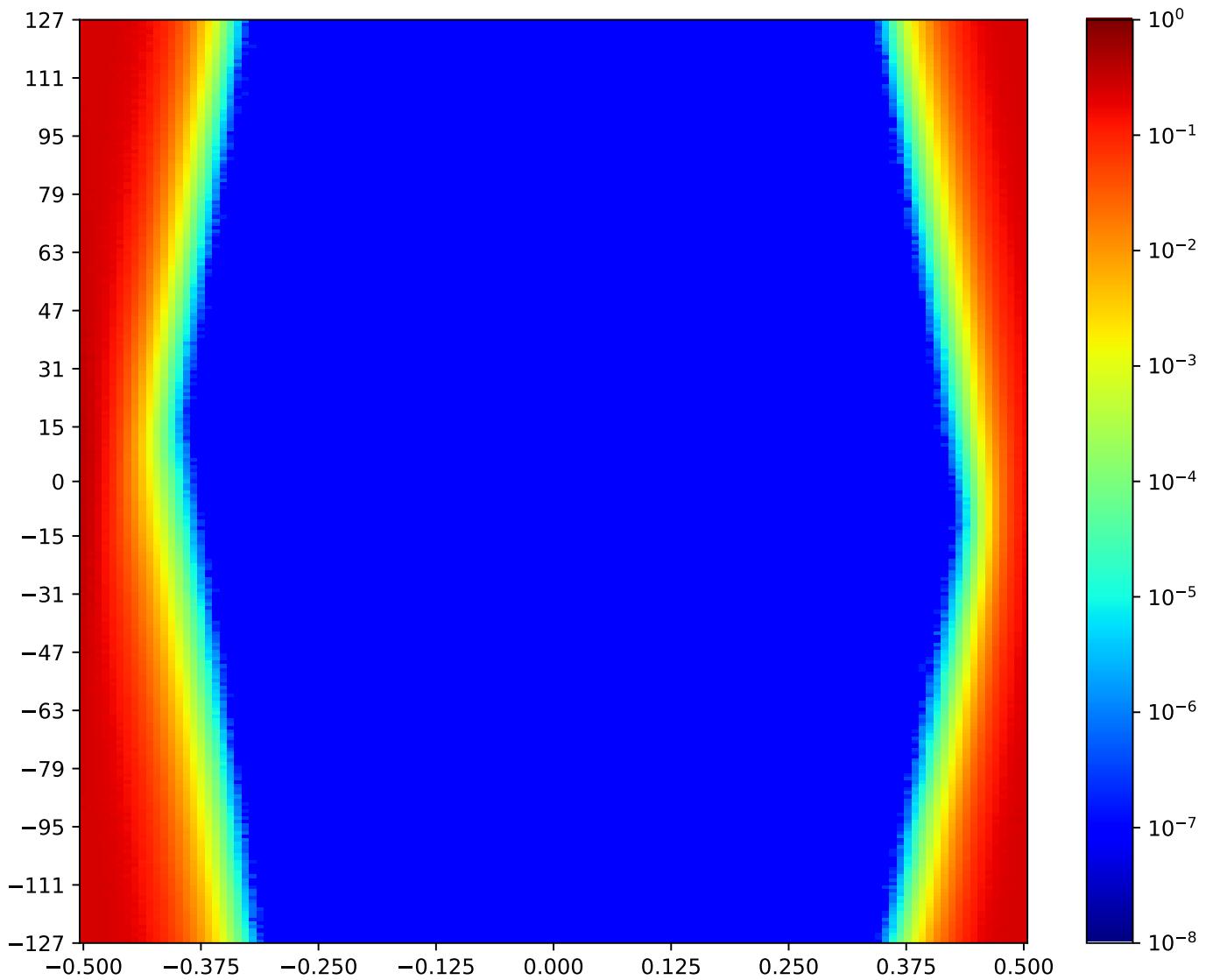


Figure 1.60: TRP\_FPGA-TX5-06-RX5-06-MSP\_A\_FPGA

Call back to summary Figure 1.53. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.5.8 TRP\_FPGA-TX5-07-RX5-07-MSP\_A\_FPGA

Table 1.56: TRP\_FPGA-TX5-07-RX5-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:59:25		2018-Jan-24 04:00:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23218	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

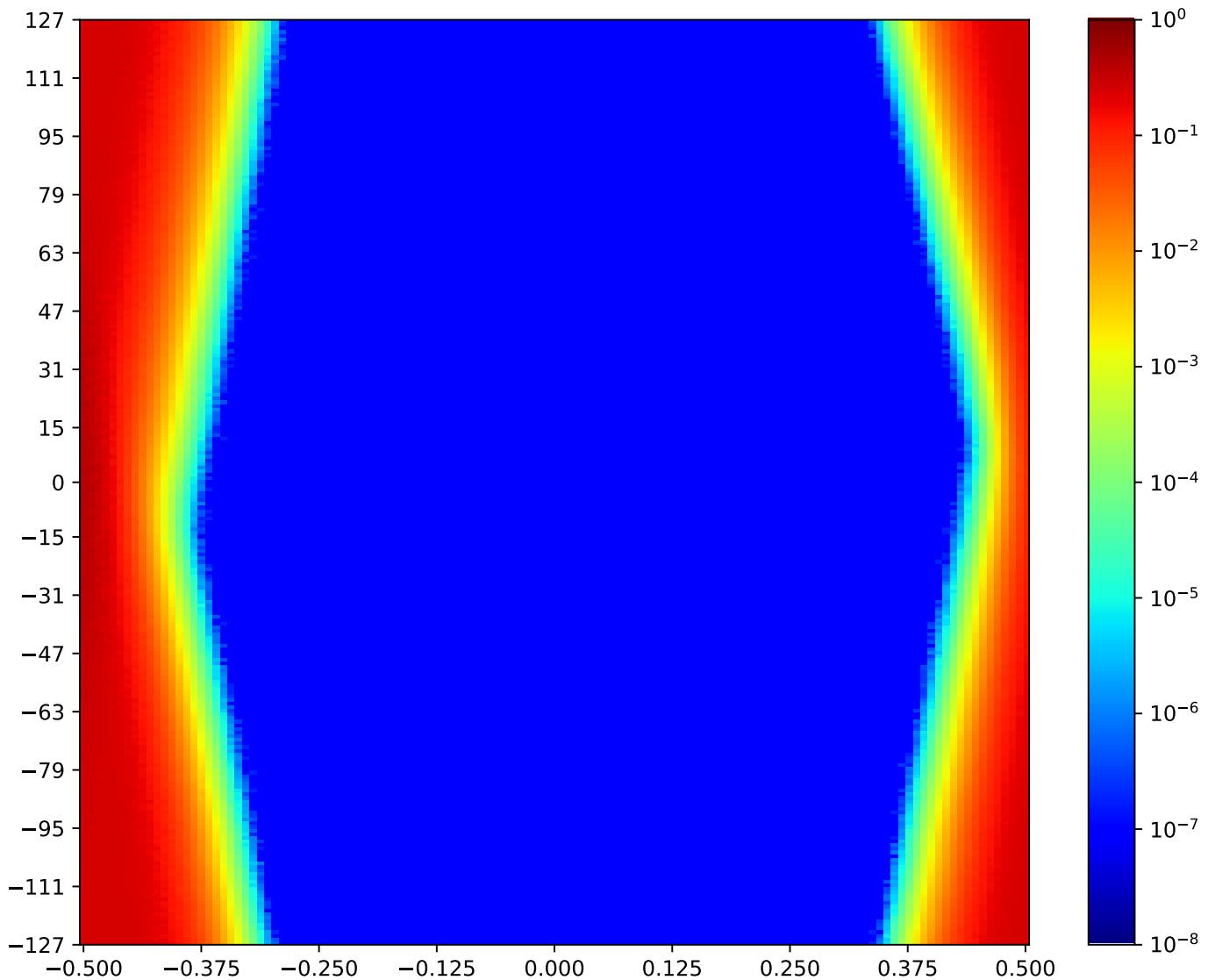


Figure 1.61: TRP\_FPGA-TX5-07-RX5-07-MSP\_A\_FPGA

Call back to summary Figure 1.53. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.6 TRP J1 QSFP Loopback

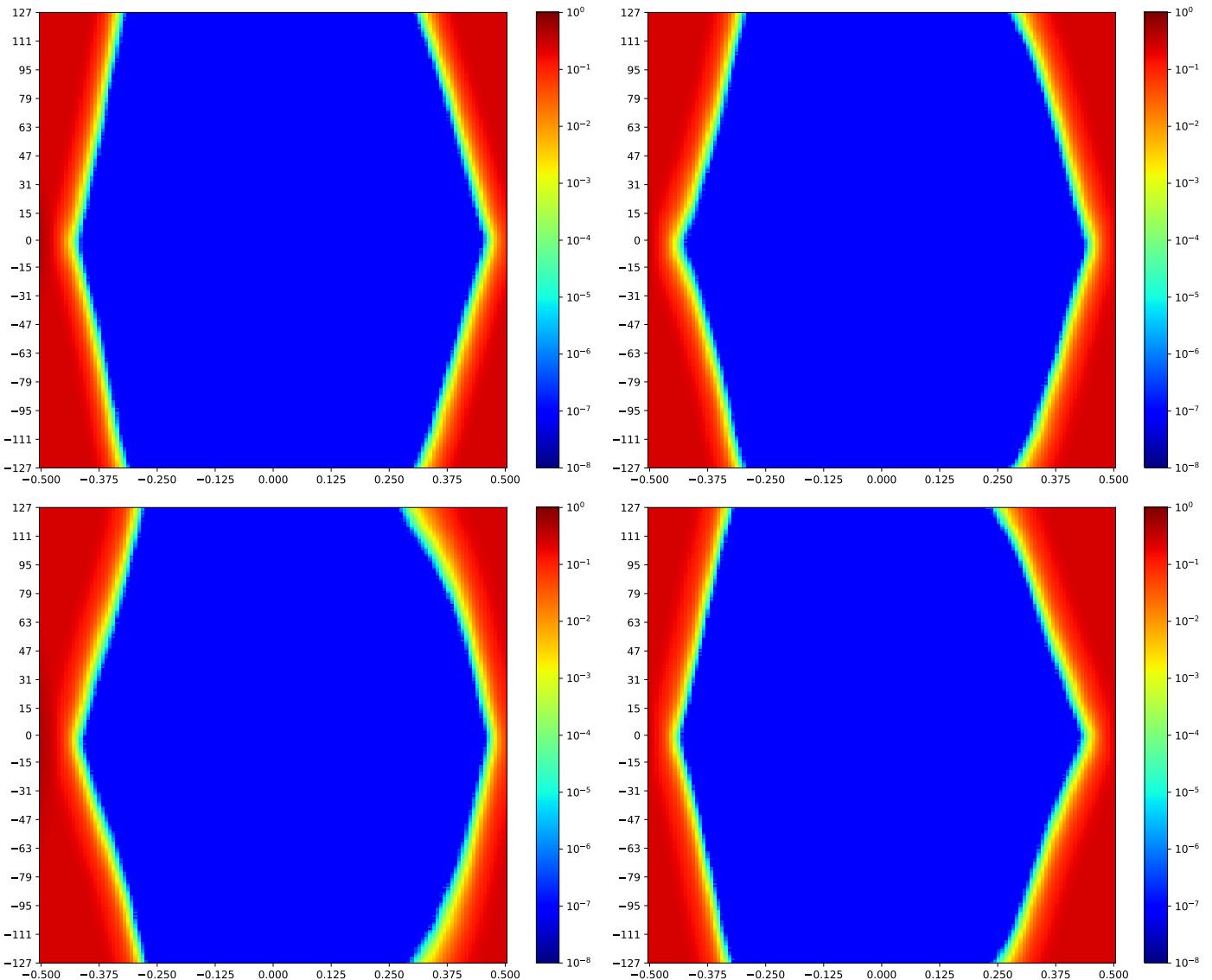


Figure 1.62: TRP J1 QSFP Loopback

A cross-reference to Figure 1.62. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.67.

### 1.6.1 TRP\_FPGA-J1-00–J1-00-TRP\_FPGA

Table 1.57: TRP\_FPGA-J1-00–J1-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:01:43		2018-Jan-24 04:02:52	
Reset RX	OA	HO		VO   VO (%)	
true	24091	109		84.50%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

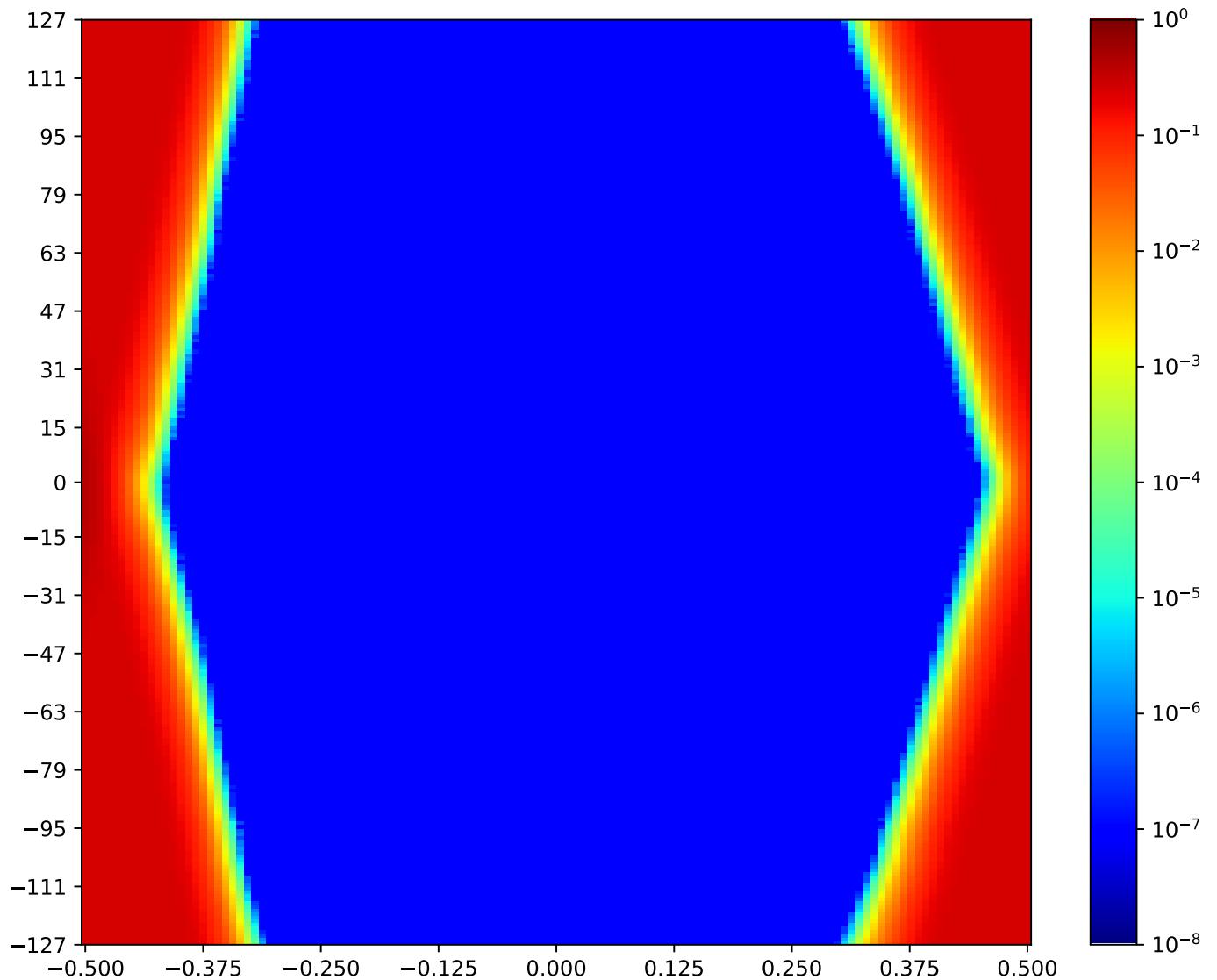


Figure 1.63: TRP\_FPGA-J1-00–J1-00-TRP\_FPGA

Call back to summary Figure 1.62. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.6.2 TRP\_FPGA-J1-01–J1-01-TRP\_FPGA

Table 1.58: TRP\_FPGA-J1-01–J1-01-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:02:52		2018-Jan-24 04:04:00	
Reset RX	OA	HO		HO (%)	
true	23169	108		83.72%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

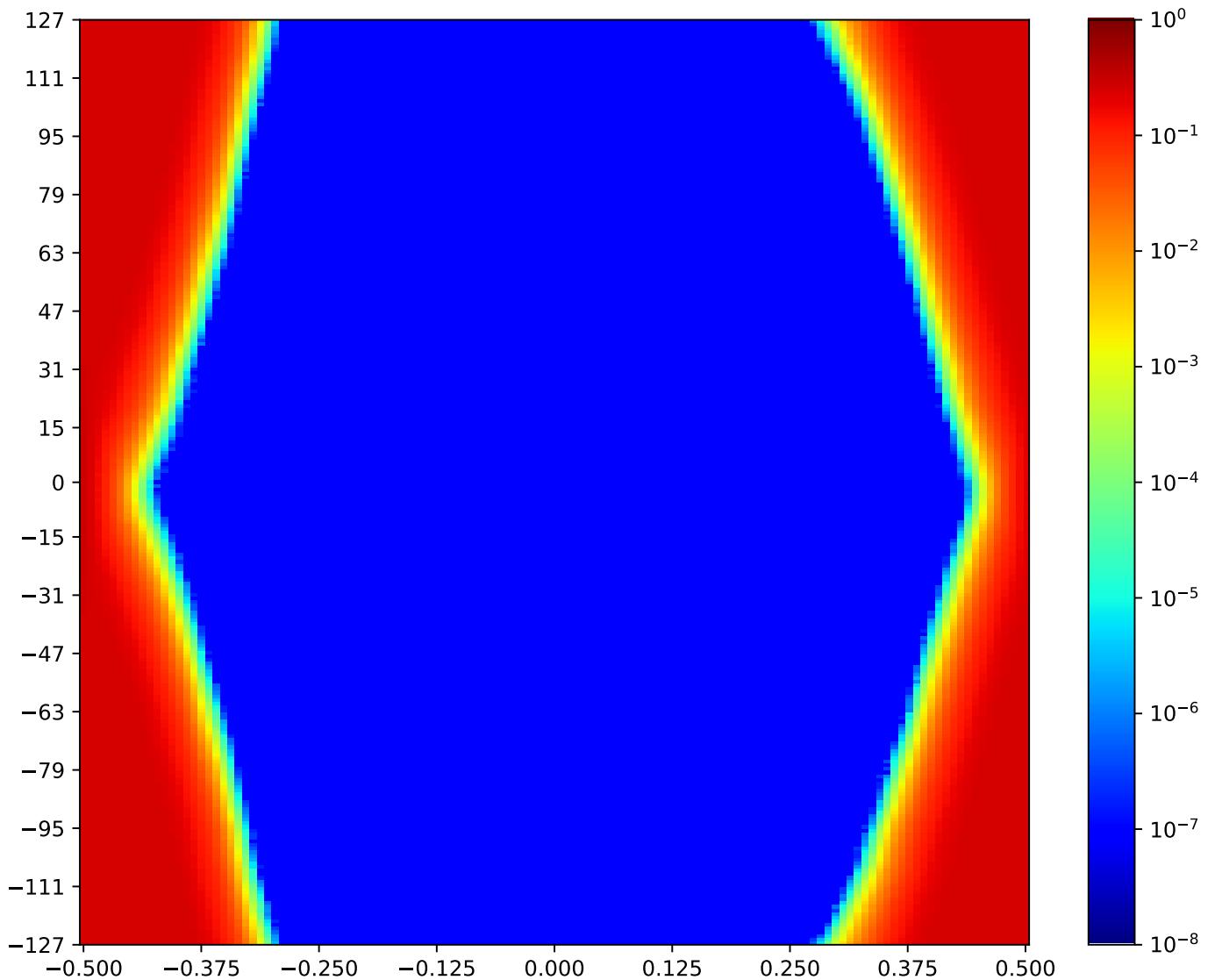


Figure 1.64: TRP\_FPGA-J1-01–J1-01-TRP\_FPGA

Call back to summary Figure 1.62. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.6.3 TRP\_FPGA-J1-02–J1-02-TRP\_FPGA

Table 1.59: TRP\_FPGA-J1-02–J1-02-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:04:00		2018-Jan-24 04:05:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23460	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

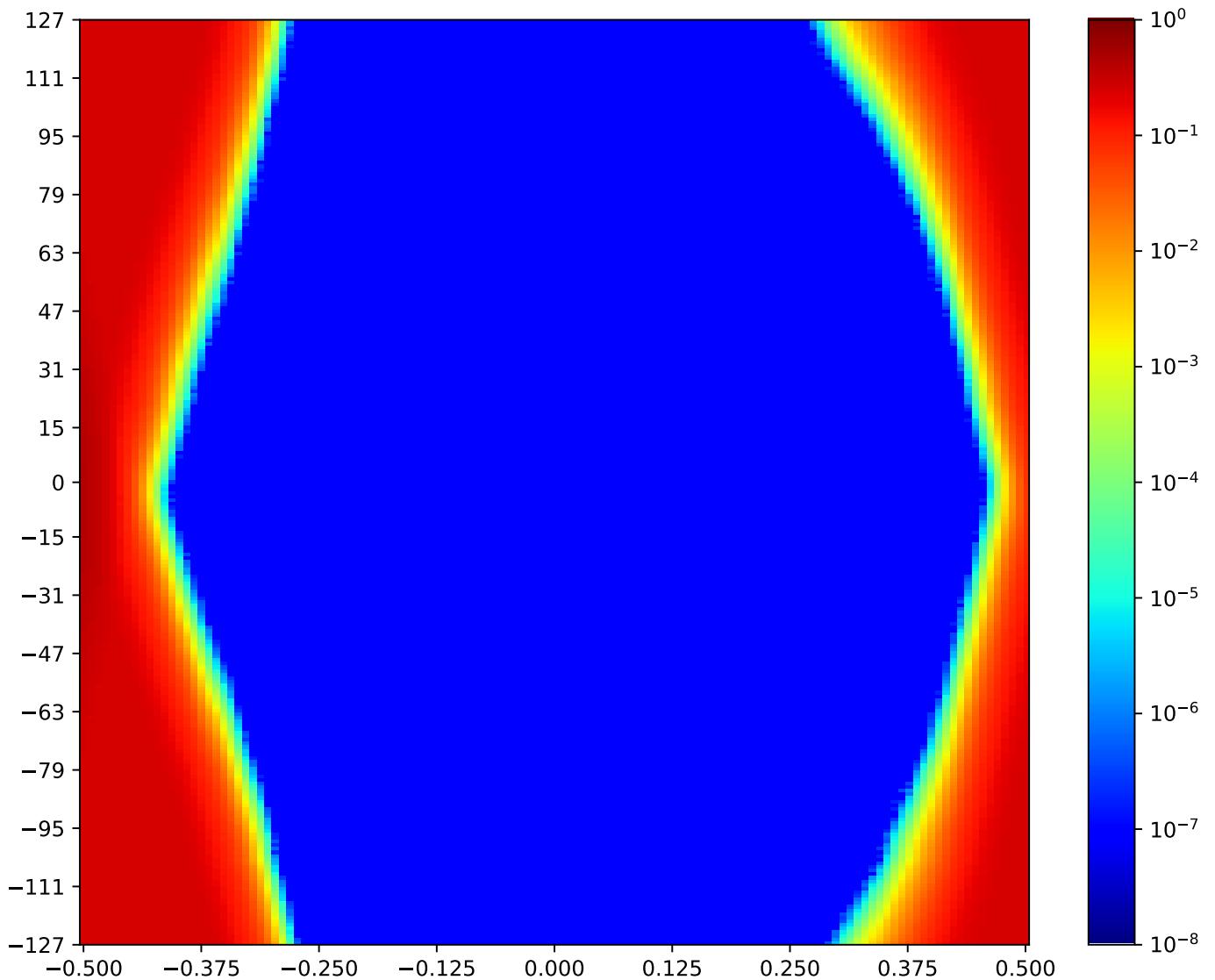


Figure 1.65: TRP\_FPGA-J1-02–J1-02-TRP\_FPGA

Call back to summary Figure 1.62. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.6.4 TRP\_FPGA-J1-03–J1-03-TRP\_FPGA

Table 1.60: TRP\_FPGA-J1-03–J1-03-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:05:09		2018-Jan-24 04:06:18	
Reset RX	OA	HO		VO   VO (%)	
true	23051	108		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

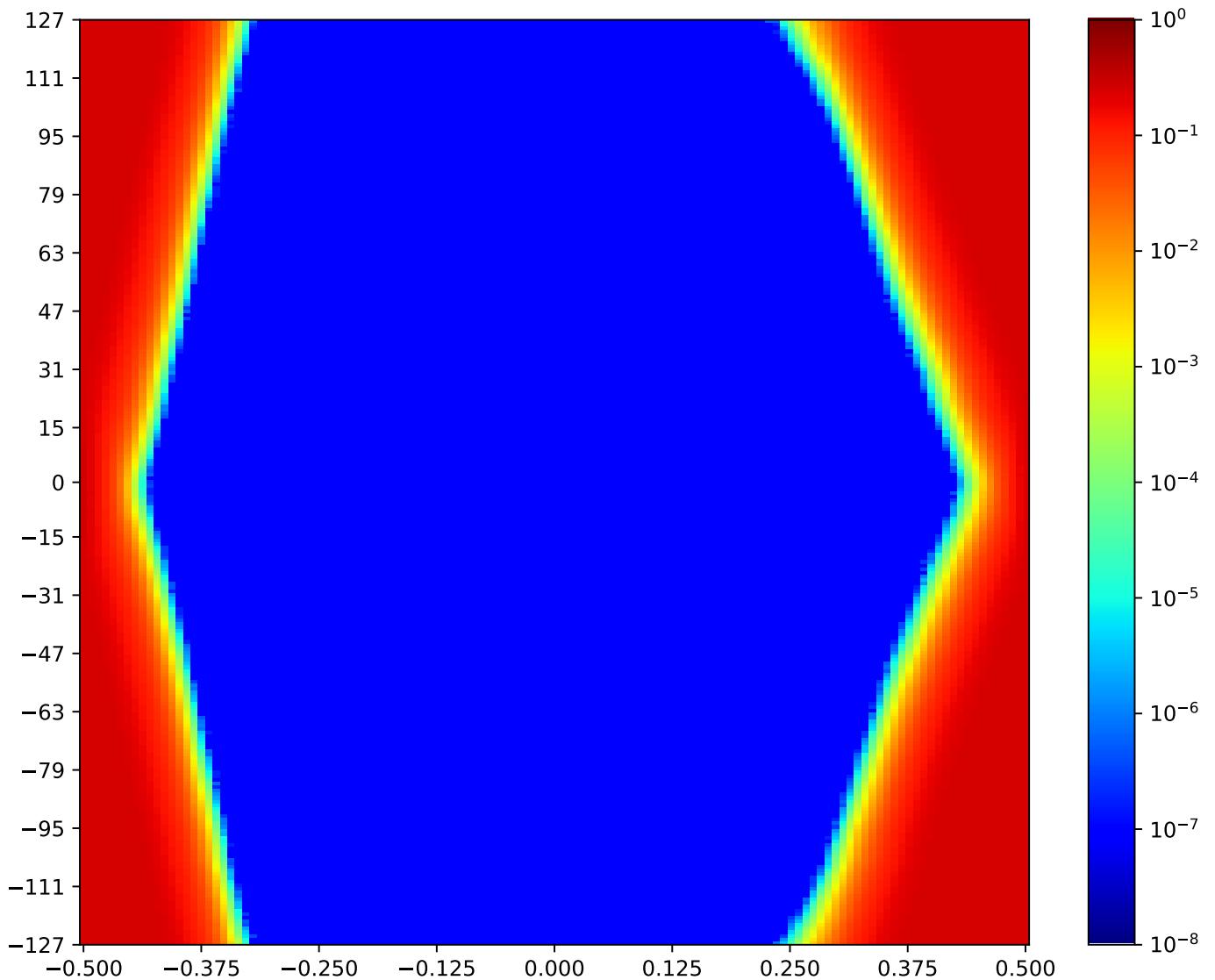


Figure 1.66: TRP\_FPGA-J1-03–J1-03-TRP\_FPGA

Call back to summary Figure 1.62. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.7 TRP J3 SFP Loopback

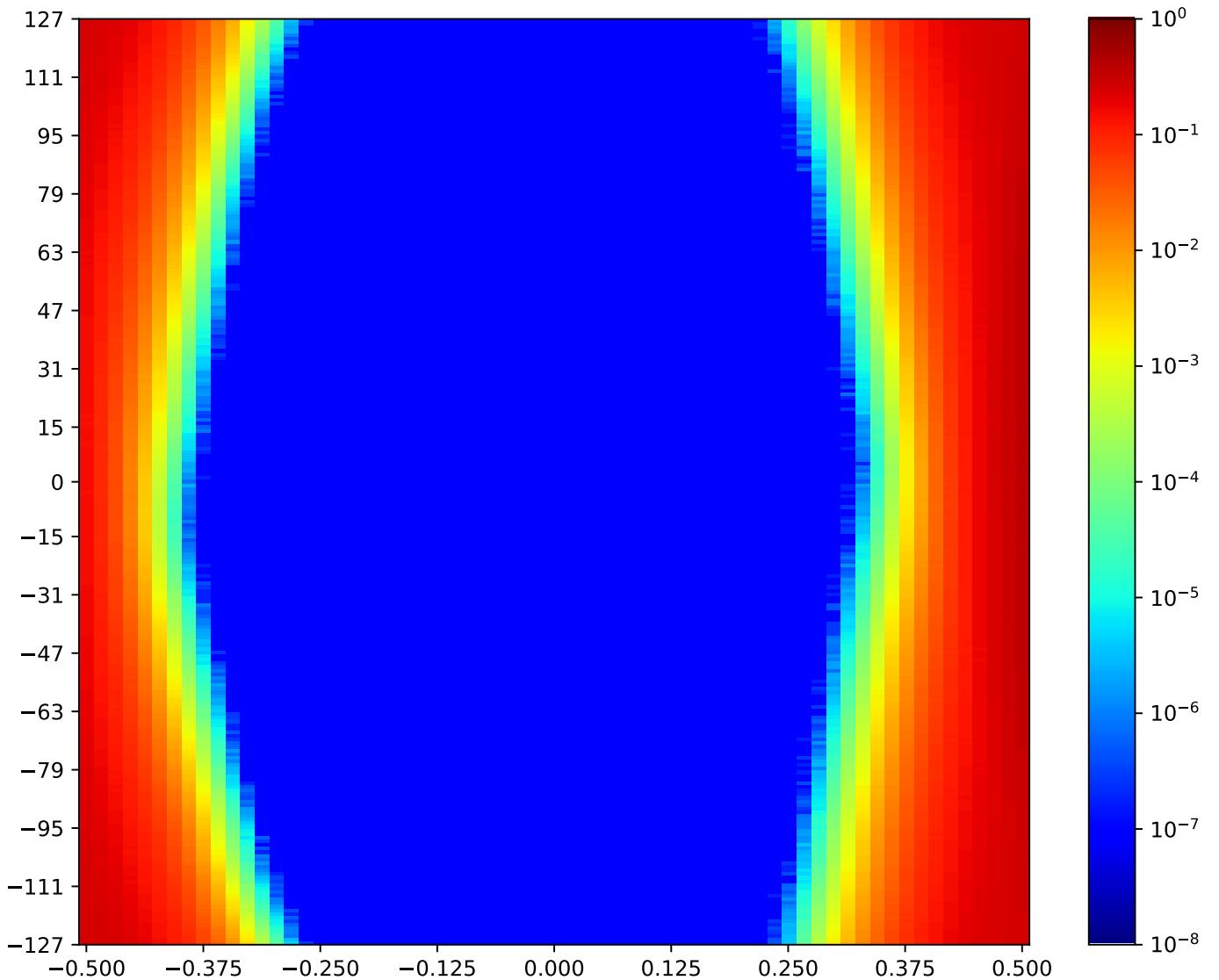


Figure 1.67: TRP J3 SFP Loopback

A cross-reference to Figure 1.67. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.69.

### 1.7.1 TRP\_FPGA-J3-00–J3-00-TRP\_FPGA

Table 1.61: TRP\_FPGA-J3-00–J3-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:06:19		2018-Jan-24 04:06:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9895	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

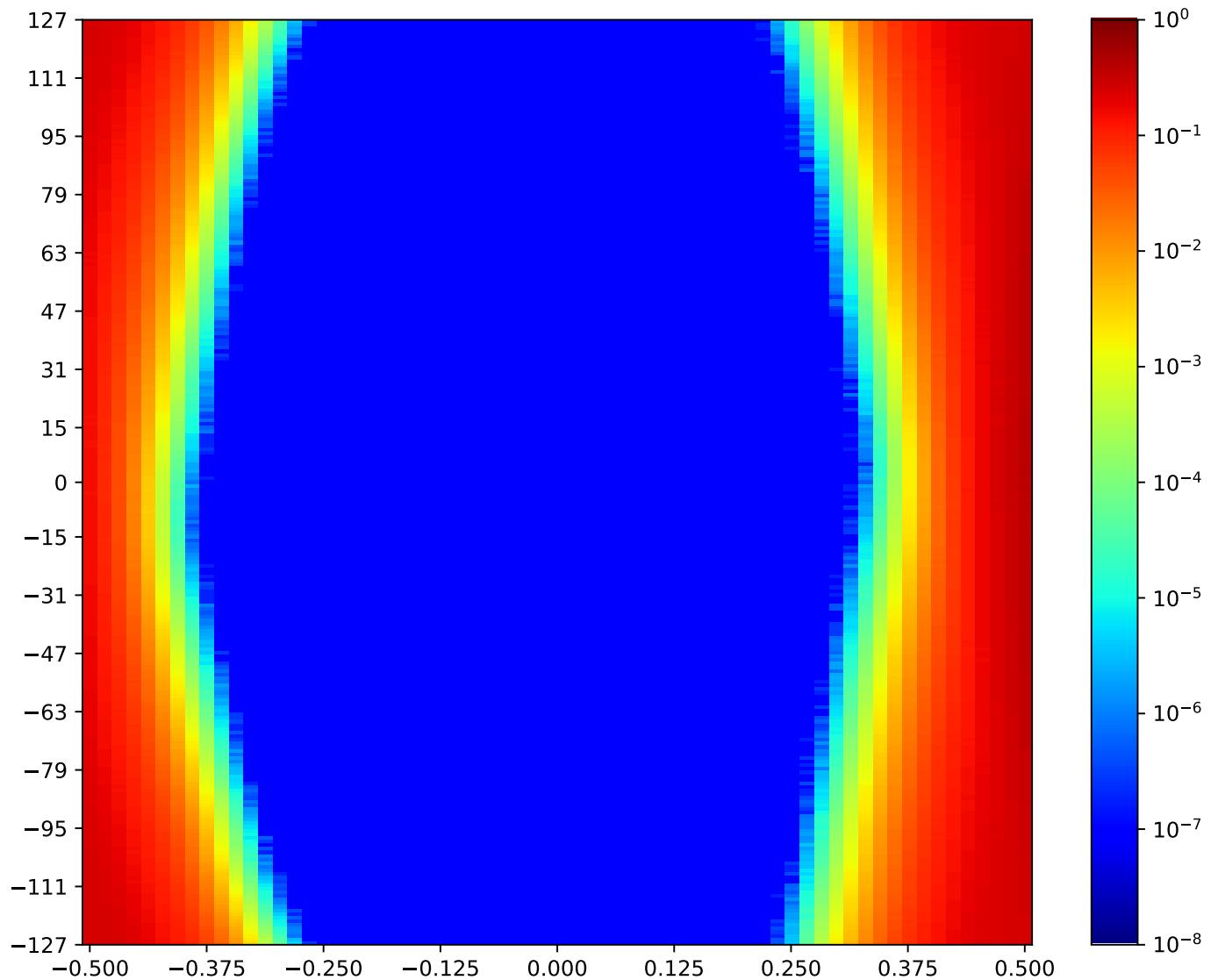


Figure 1.68: TRP\_FPGA-J3-00–J3-00-TRP\_FPGA

Call back to summary Figure 1.67. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.8 MSP\_A TRP On board links

A cross-reference to Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.98.

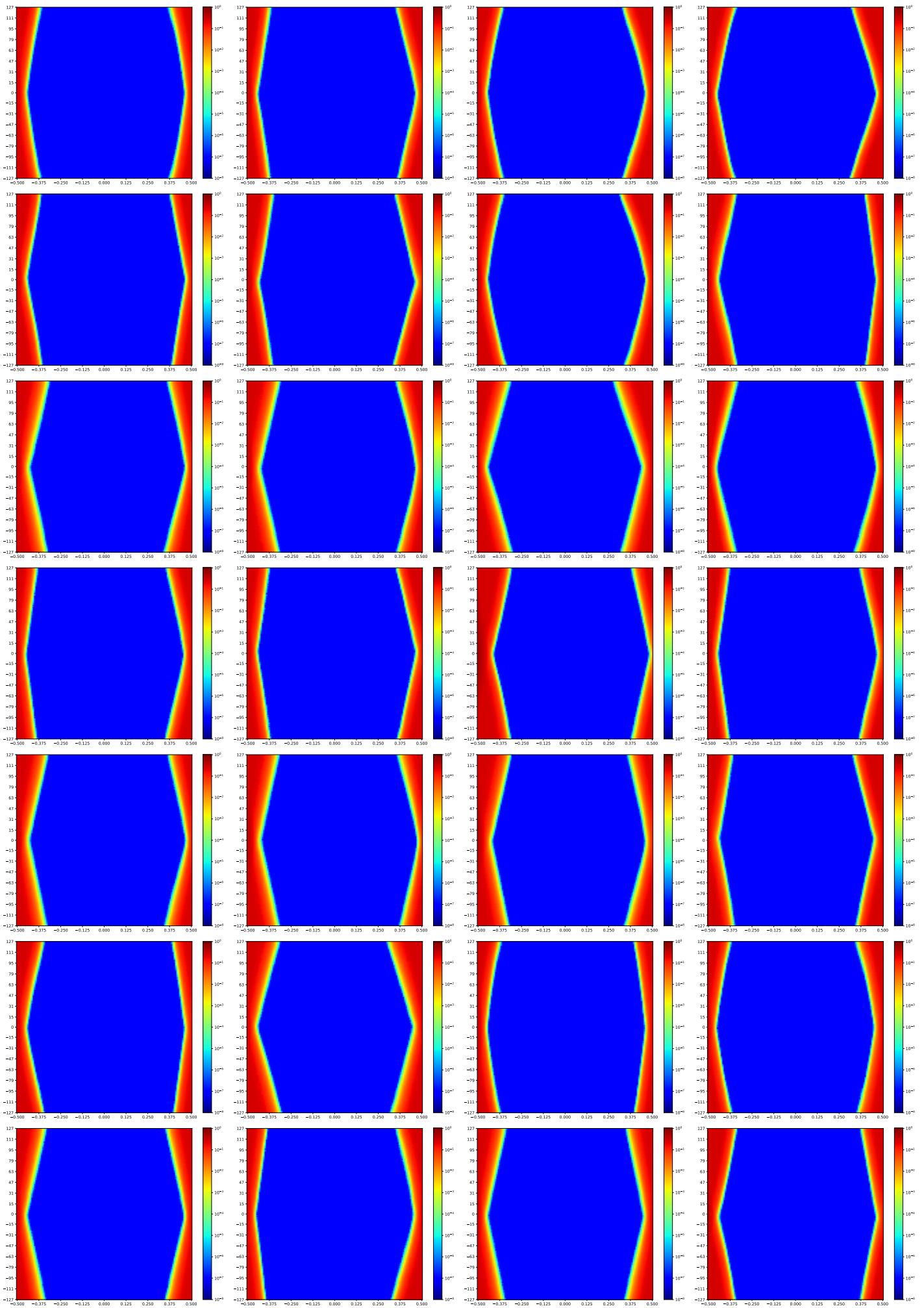


Figure 1.69: MSP\_A TRP On board links

### 1.8.1 MSP\_A\_FPGA-IC39-00-IC4-00-TRP\_FPGA

Table 1.62: MSP\_A\_FPGA-IC39-00-IC4-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:06:55		2018-Jan-24 04:08:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26390	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

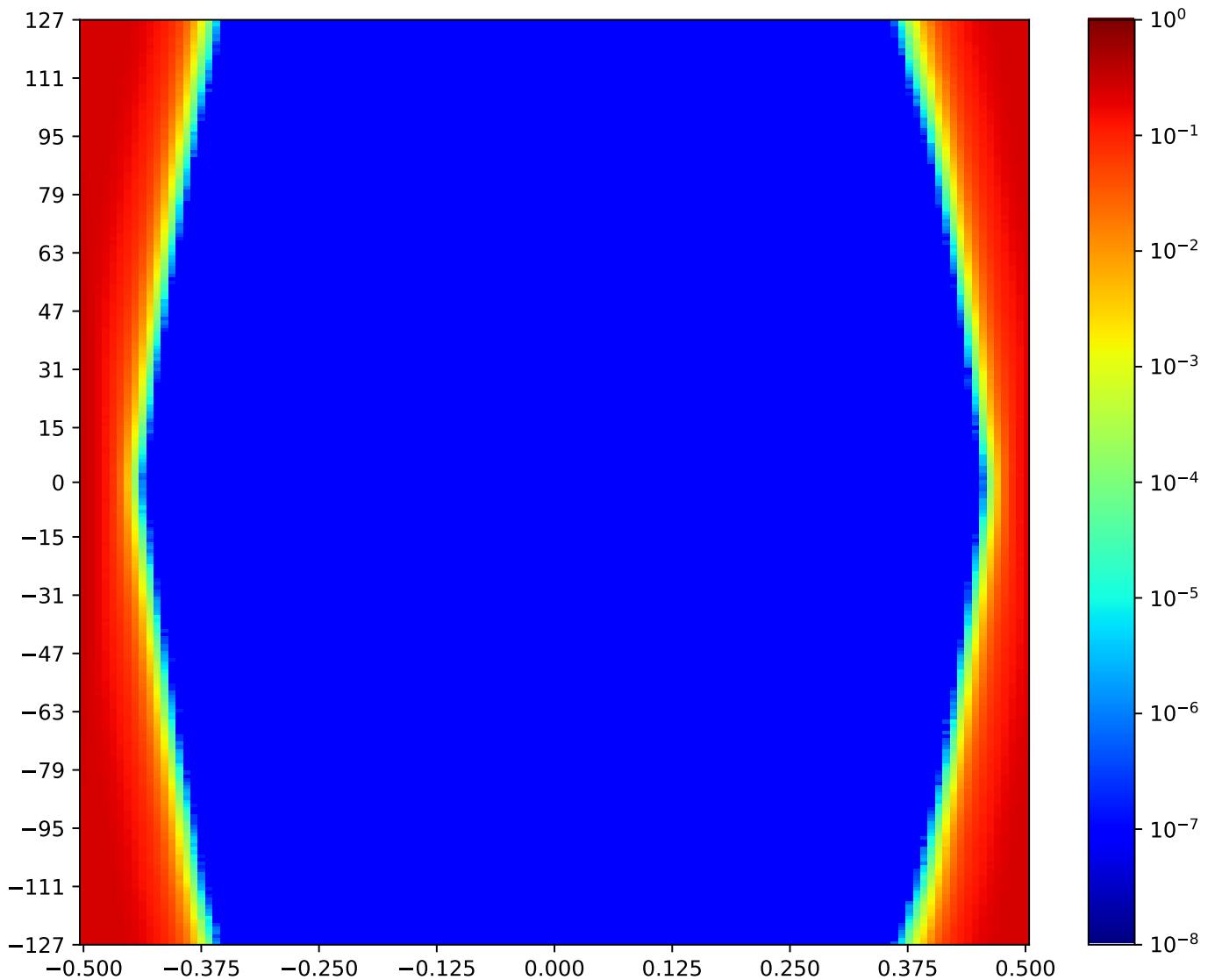


Figure 1.70: MSP\_A\_FPGA-IC39-00-IC4-00-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.2 MSP\_A\_FPGA-IC39-01-IC4-01-TRP\_FPGA

Table 1.63: MSP\_A\_FPGA-IC39-01-IC4-01-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:08:07		2018-Jan-24 04:09:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25962	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

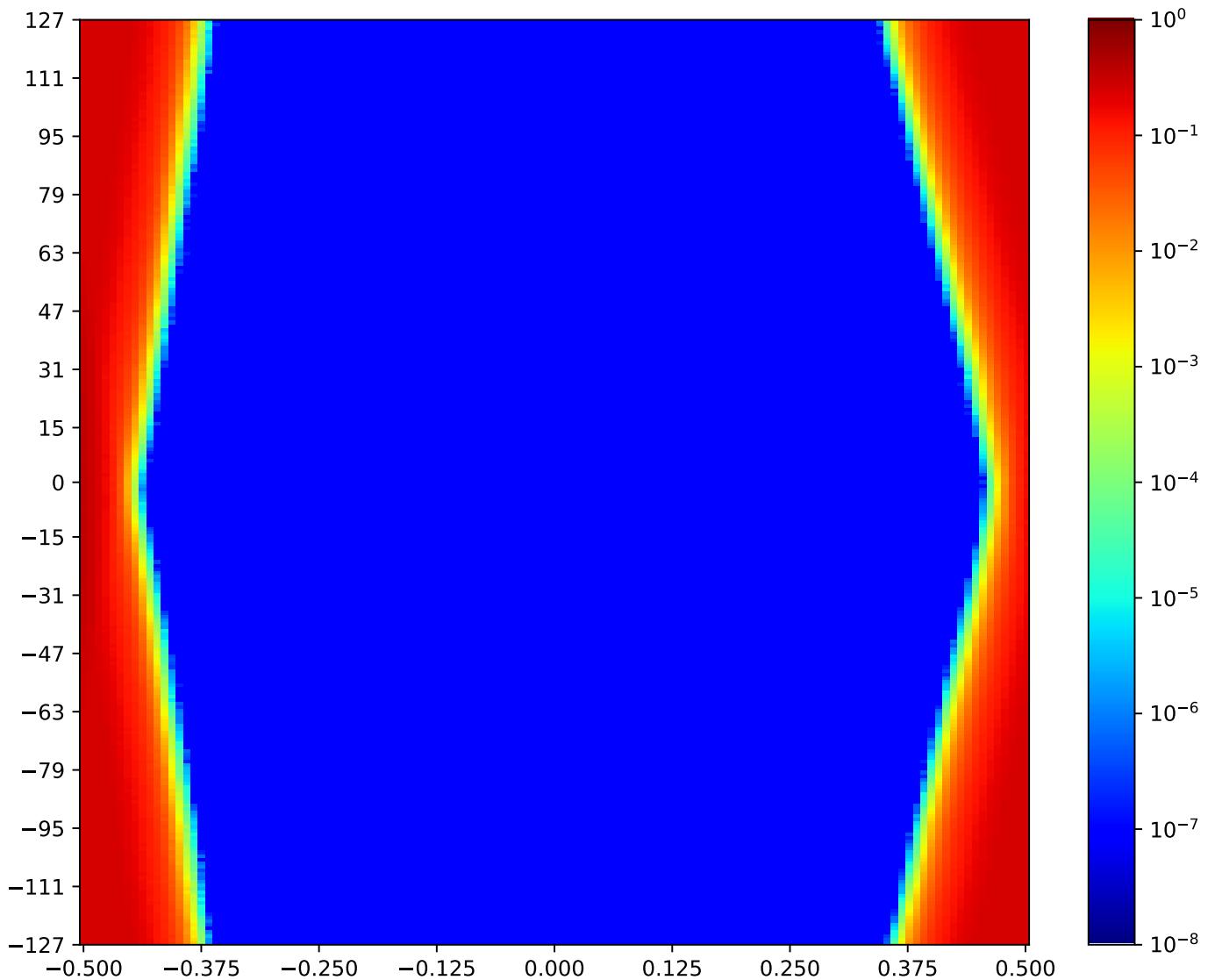


Figure 1.71: MSP\_A\_FPGA-IC39-01-IC4-01-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.3 MSP\_A\_FPGA-IC39-02-IC4-02-TRP\_FPGA

Table 1.64: MSP\_A\_FPGA-IC39-02-IC4-02-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:09:17		2018-Jan-24 04:10:28	
Reset RX	OA	HO		VO   VO (%)	
true	25694	113		87.60%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

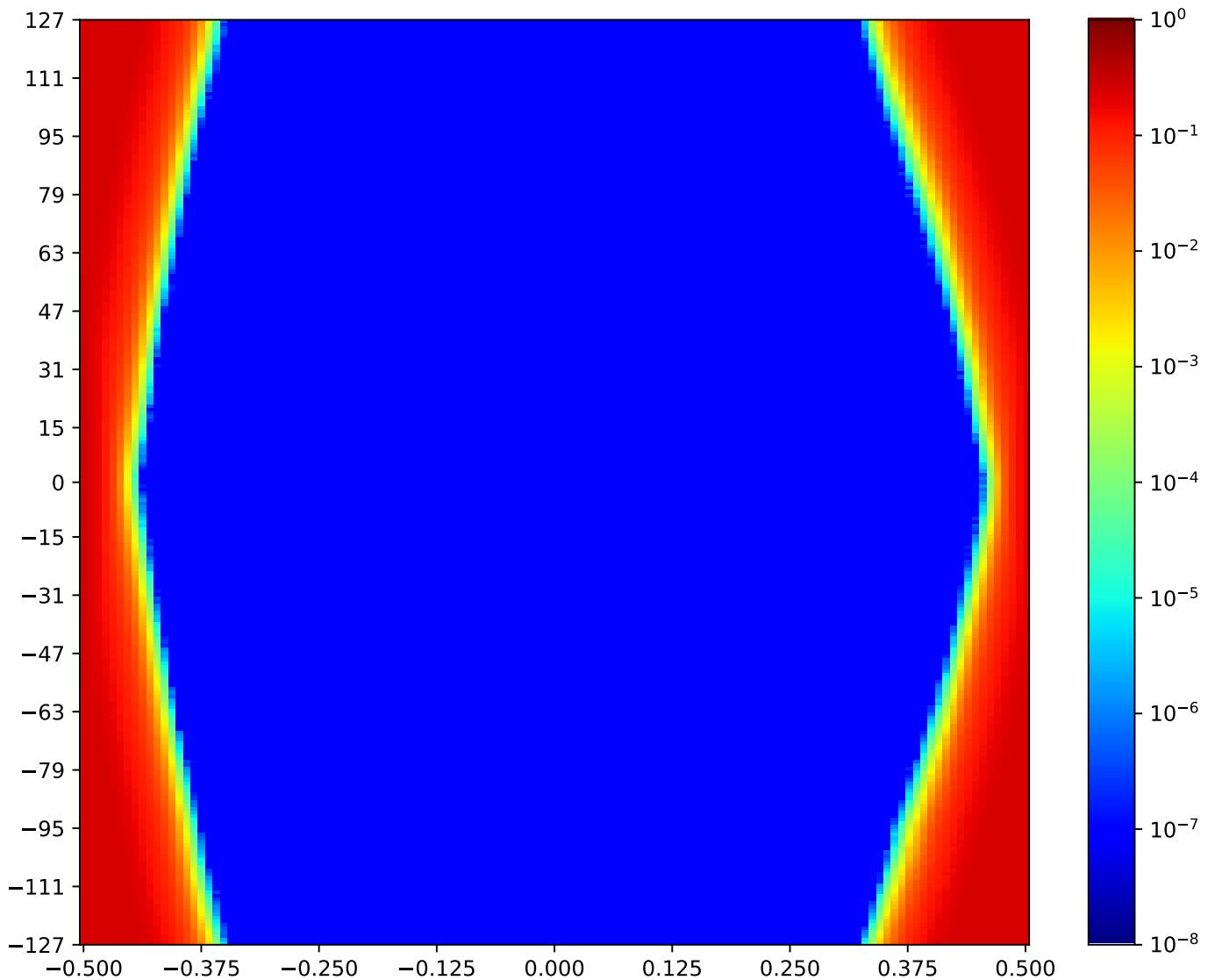


Figure 1.72: MSP\_A\_FPGA-IC39-02-IC4-02-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.8.4 MSP\_A\_FPGA-IC39-03-IC4-03-TRP\_FPGA

Table 1.65: MSP\_A\_FPGA-IC39-03-IC4-03-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:10:28		2018-Jan-24 04:11:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25246	115	89.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

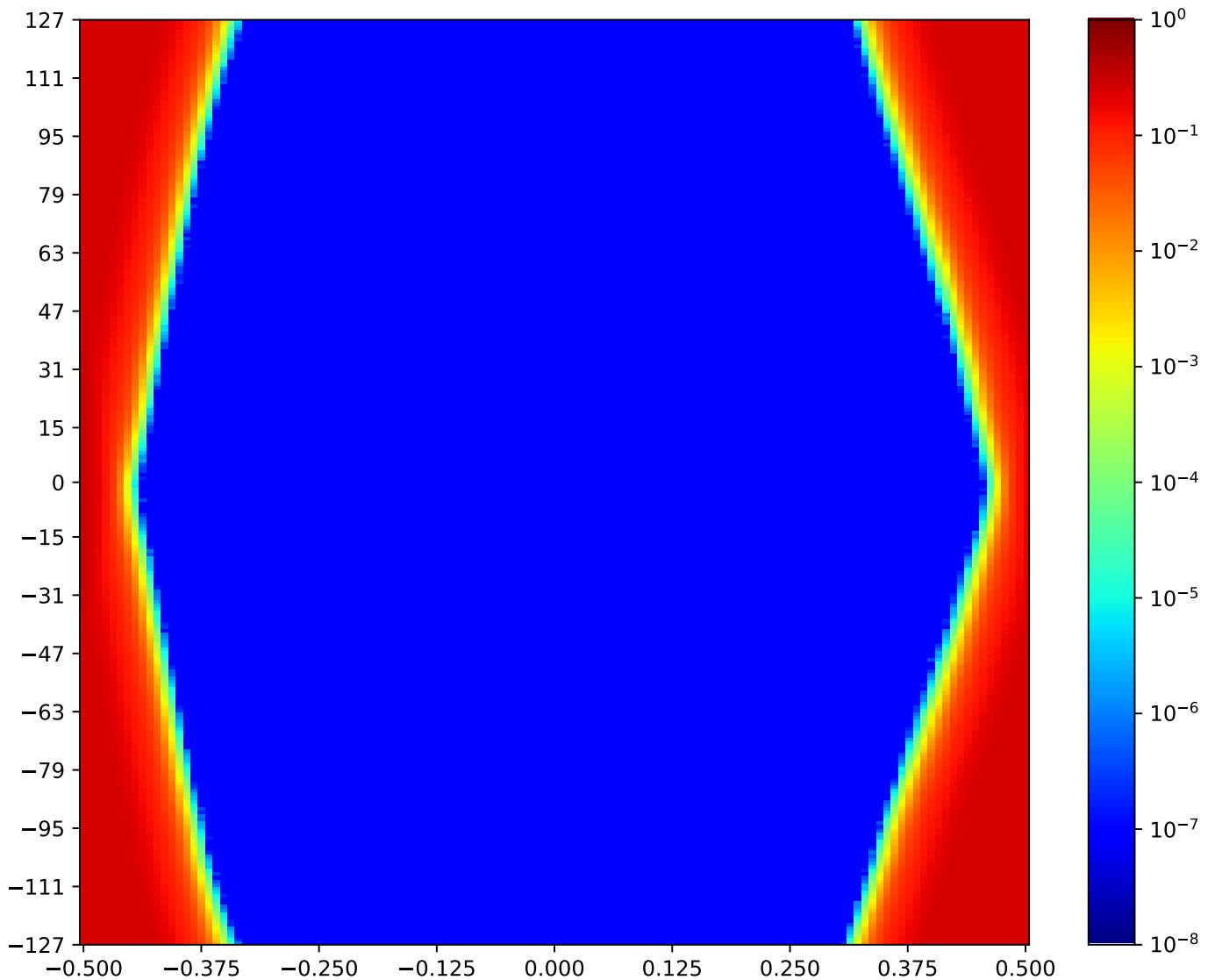


Figure 1.73: MSP\_A\_FPGA-IC39-03-IC4-03-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.5 MSP\_A\_FPGA-IC39-04-IC4-04-TRP\_FPGA

Table 1.66: MSP\_A\_FPGA-IC39-04-IC4-04-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:11:39		2018-Jan-24 04:12:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26162	114	88.37%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

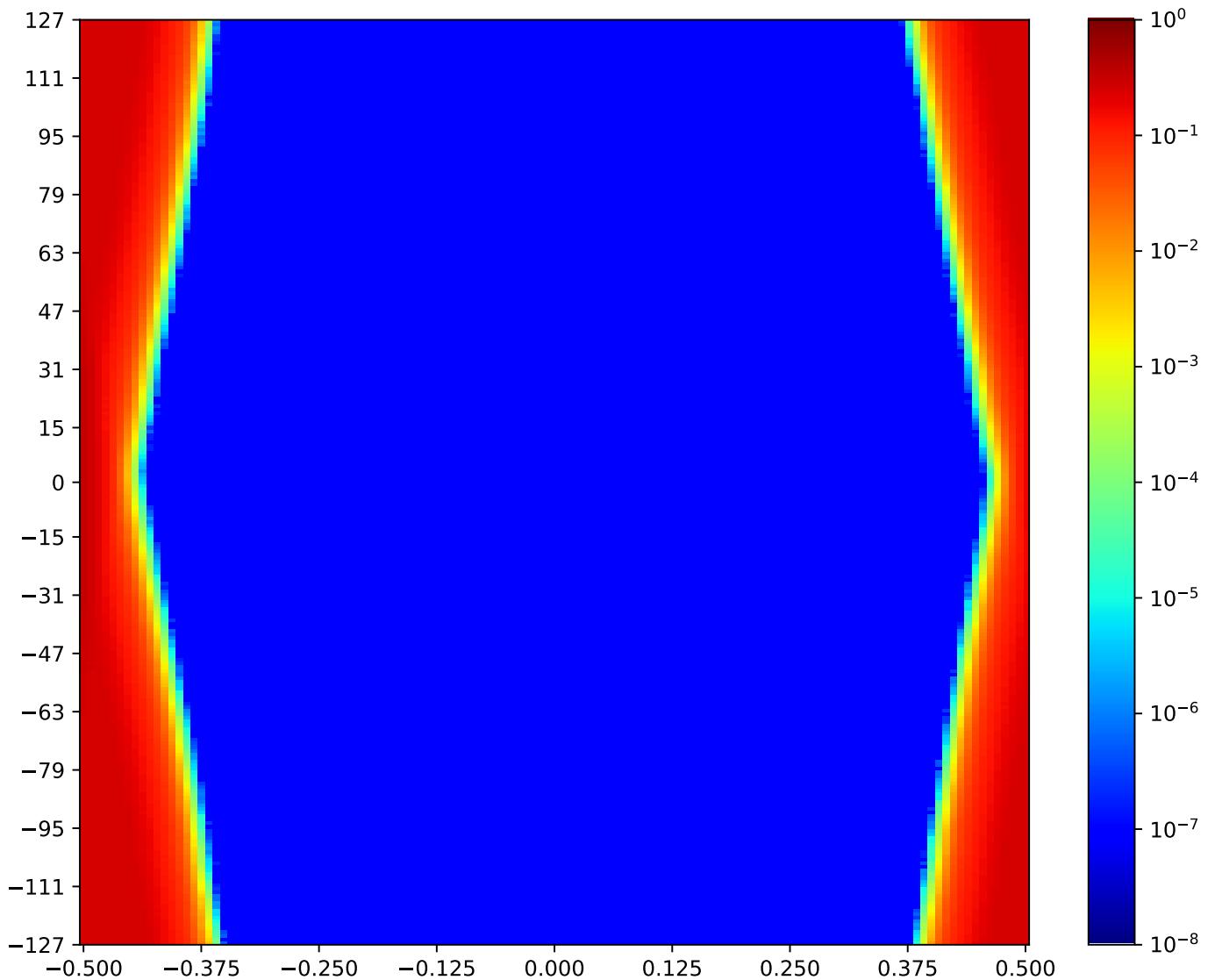


Figure 1.74: MSP\_A\_FPGA-IC39-04-IC4-04-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.6 MSP\_A\_FPGA-IC39-05-IC4-05-TRP\_FPGA

Table 1.67: MSP\_A\_FPGA-IC39-05-IC4-05-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:12:50		2018-Jan-24 04:14:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25140	111	86.05%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

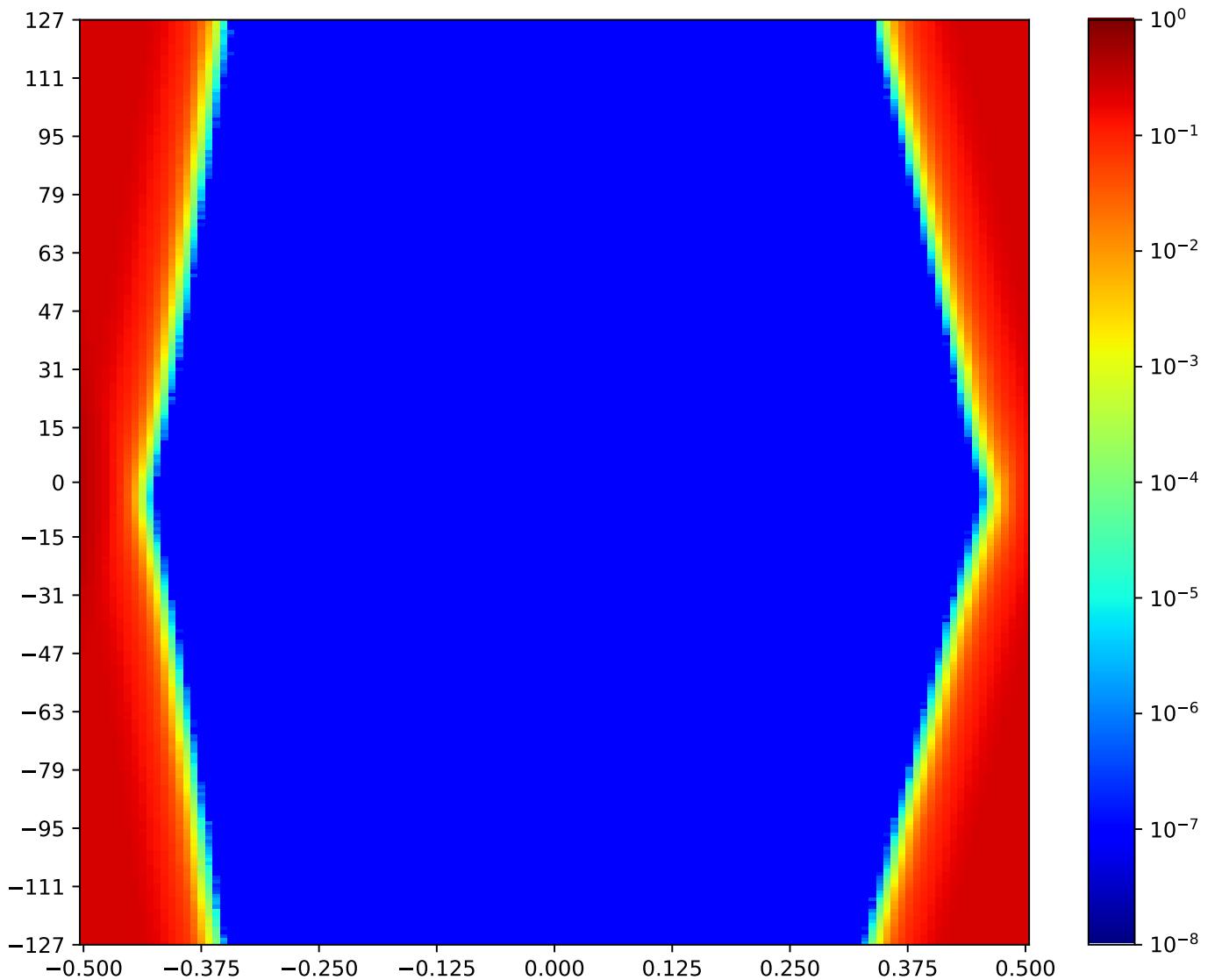


Figure 1.75: MSP\_A\_FPGA-IC39-05-IC4-05-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.7 MSP\_A\_FPGA-IC39-06-IC4-06-TRP\_FPGA

Table 1.68: MSP\_A\_FPGA-IC39-06-IC4-06-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:14:00		2018-Jan-24 04:15:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25577	114	88.37%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

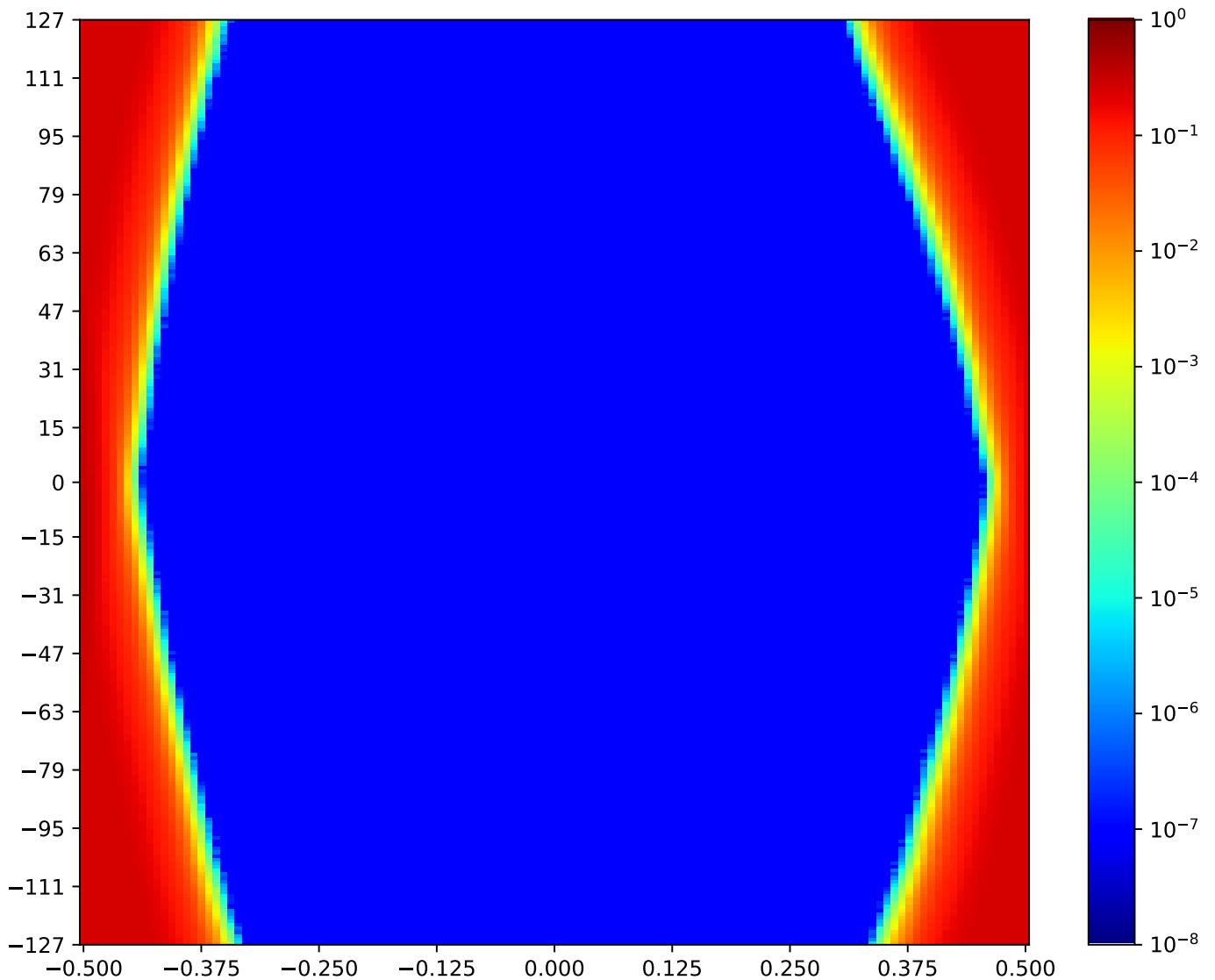


Figure 1.76: MSP\_A\_FPGA-IC39-06-IC4-06-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.8 MSP\_A\_FPGA-IC39-07-IC4-07-TRP\_FPGA

Table 1.69: MSP\_A\_FPGA-IC39-07-IC4-07-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:15:11		2018-Jan-24 04:16:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26077	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

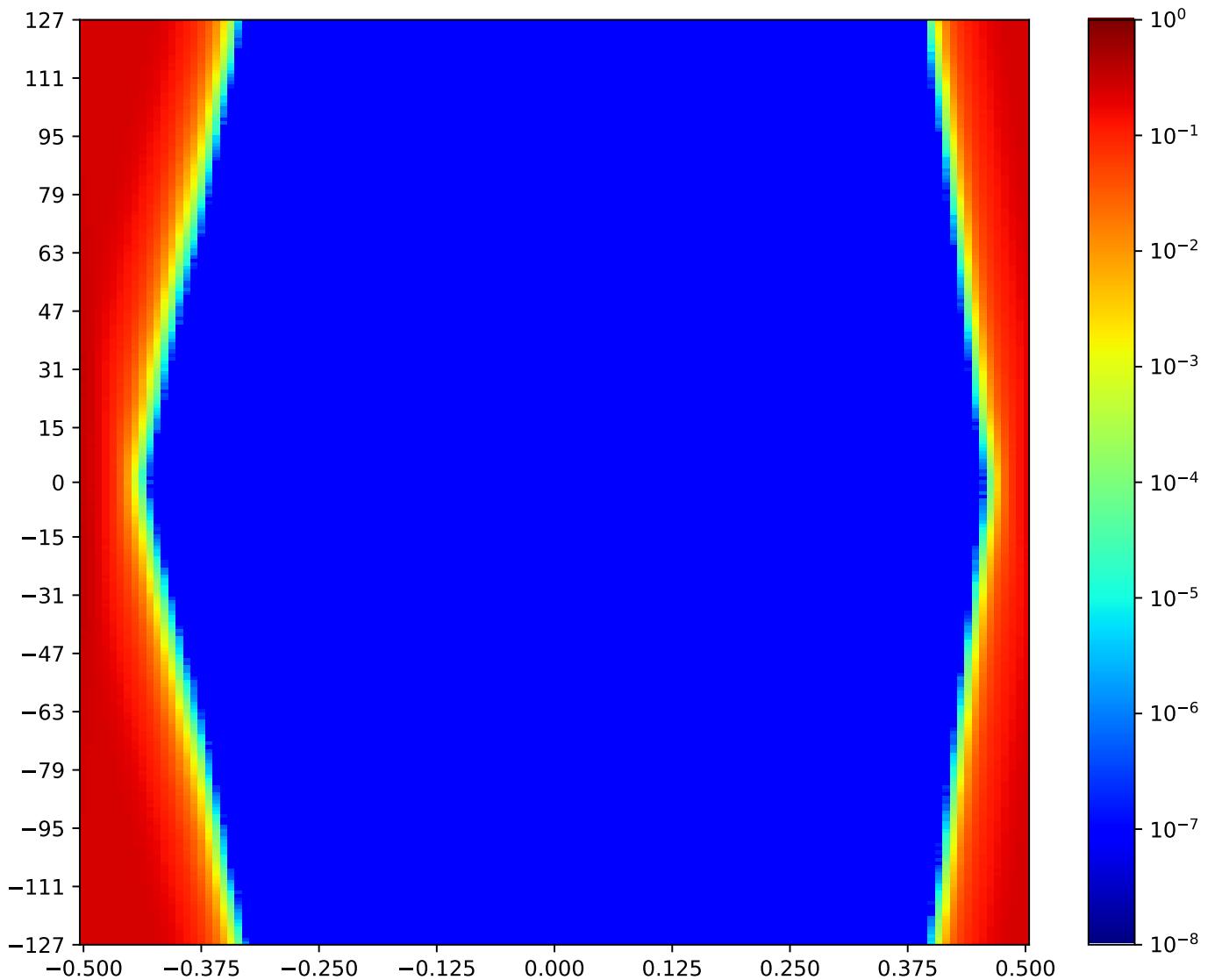


Figure 1.77: MSP\_A\_FPGA-IC39-07-IC4-07-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.9 MSP\_A\_FPGA-IC39-08-IC4-08-TRP\_FPGA

Table 1.70: MSP\_A\_FPGA-IC39-08-IC4-08-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:16:23		2018-Jan-24 04:17:33	
Reset RX	OA	HO		VO   VO (%)	
true	24814	111		86.05%   255   100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

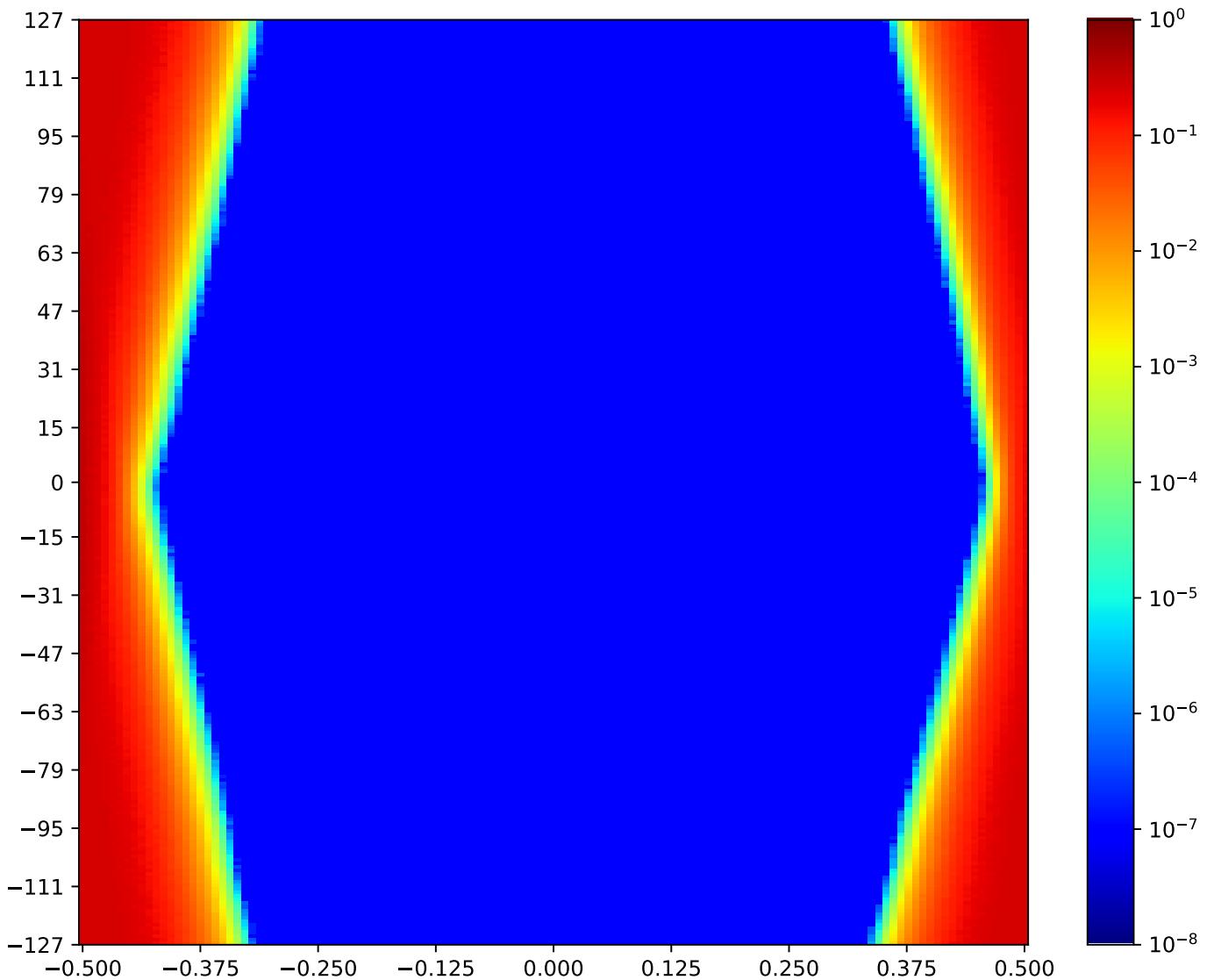


Figure 1.78: MSP\_A\_FPGA-IC39-08-IC4-08-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.10 MSP\_A\_FPGA-IC39-09-IC4-09-TRP\_FPGA

Table 1.71: MSP\_A\_FPGA-IC39-09-IC4-09-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:17:33		2018-Jan-24 04:18:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24850	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

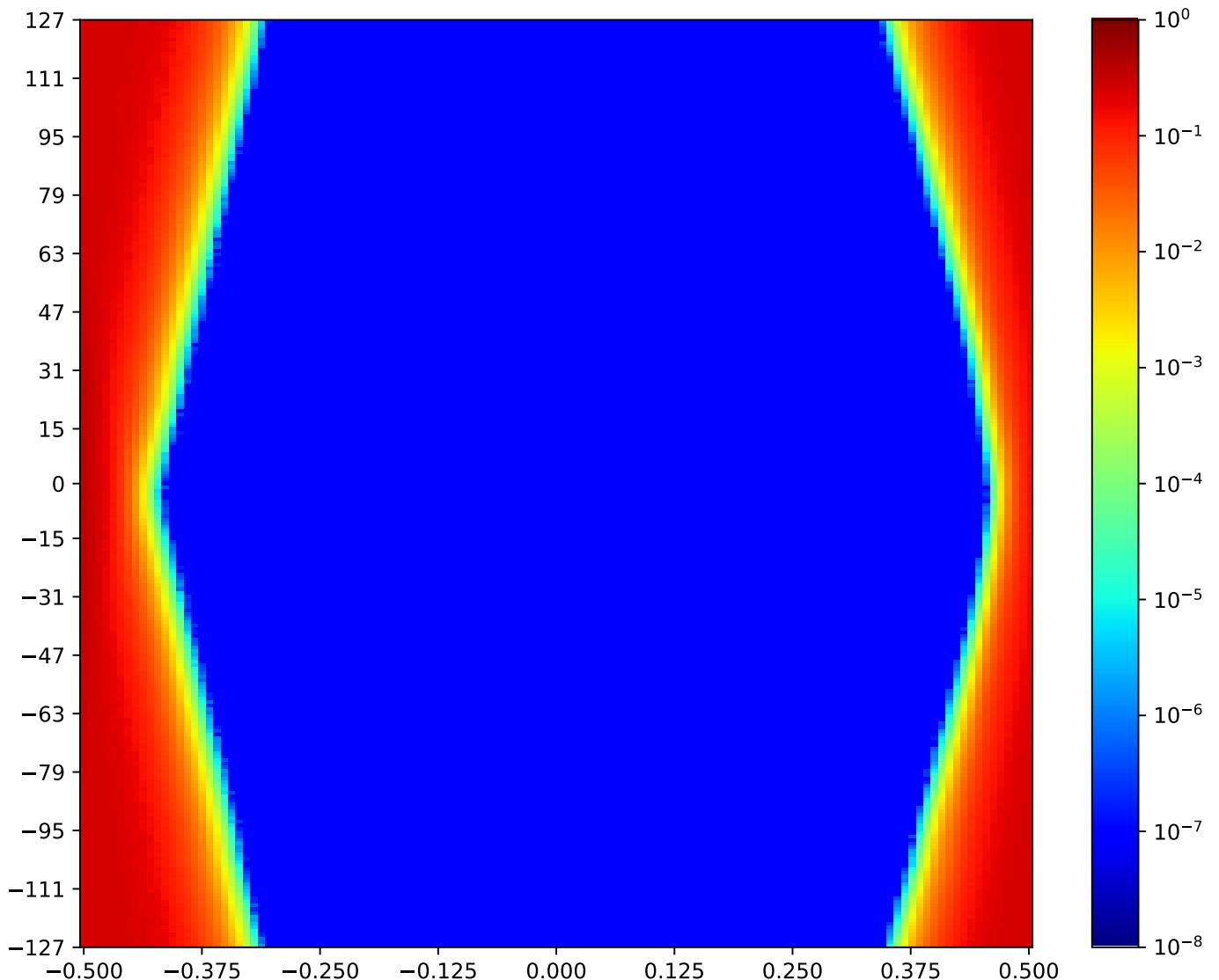


Figure 1.79: MSP\_A\_FPGA-IC39-09-IC4-09-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.11 MSP\_A\_FPGA-IC39-10-IC4-10-TRP\_FPGA

Table 1.72: MSP\_A\_FPGA-IC39-10-IC4-10-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:18:43		2018-Jan-24 04:19:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23569	111	86.05%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

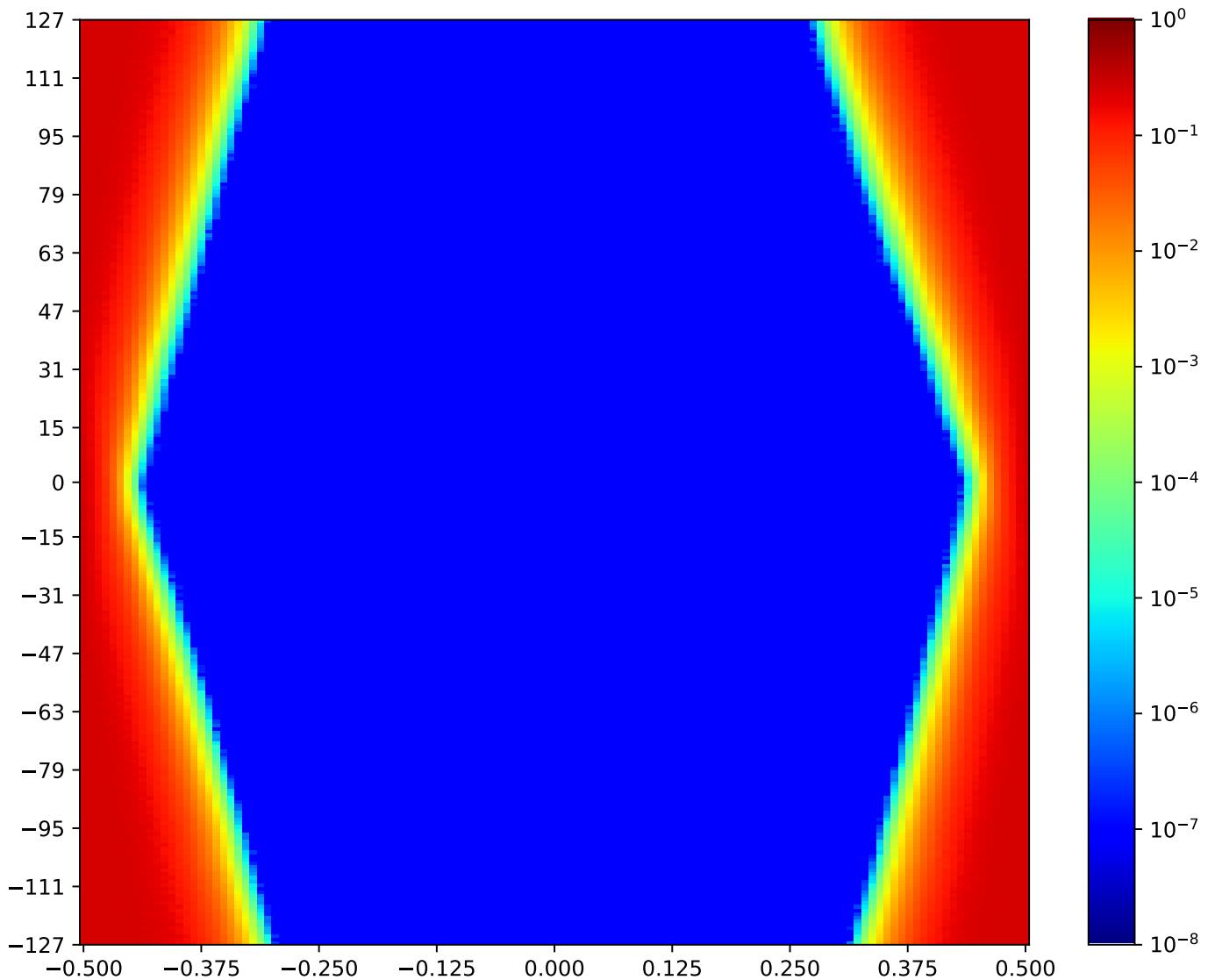


Figure 1.80: MSP\_A\_FPGA-IC39-10-IC4-10-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.12 MSP\_A\_FPGA-IC39-11-IC4-11-TRP\_FPGA

Table 1.73: MSP\_A\_FPGA-IC39-11-IC4-11-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:19:52		2018-Jan-24 04:21:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25462	114	88.37%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

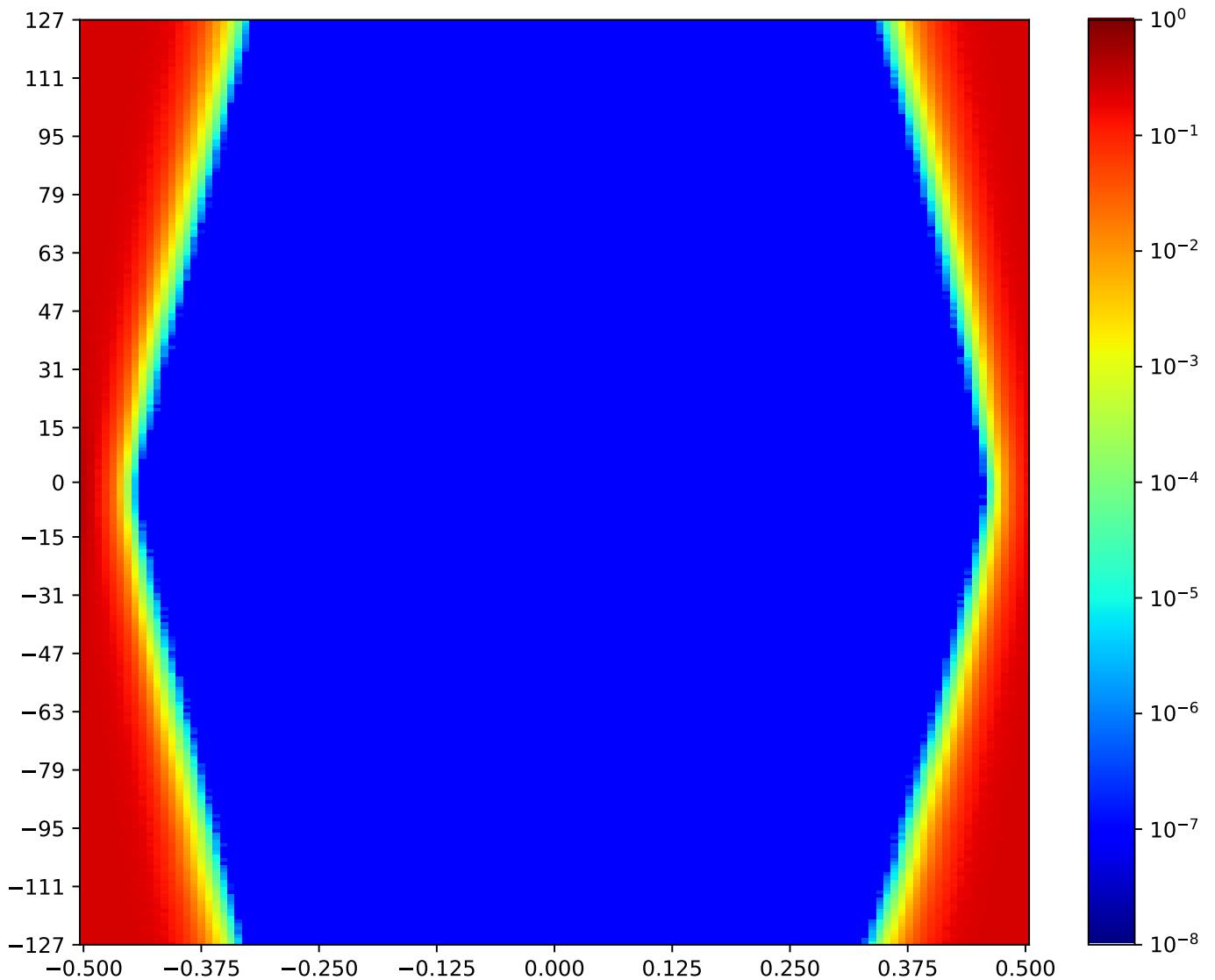


Figure 1.81: MSP\_A\_FPGA-IC39-11-IC4-11-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.13 MSP\_A\_FPGA-IC39-12-IC4-12-TRP\_FPGA

Table 1.74: MSP\_A\_FPGA-IC39-12-IC4-12-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:21:03		2018-Jan-24 04:22:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26216	114	88.37%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

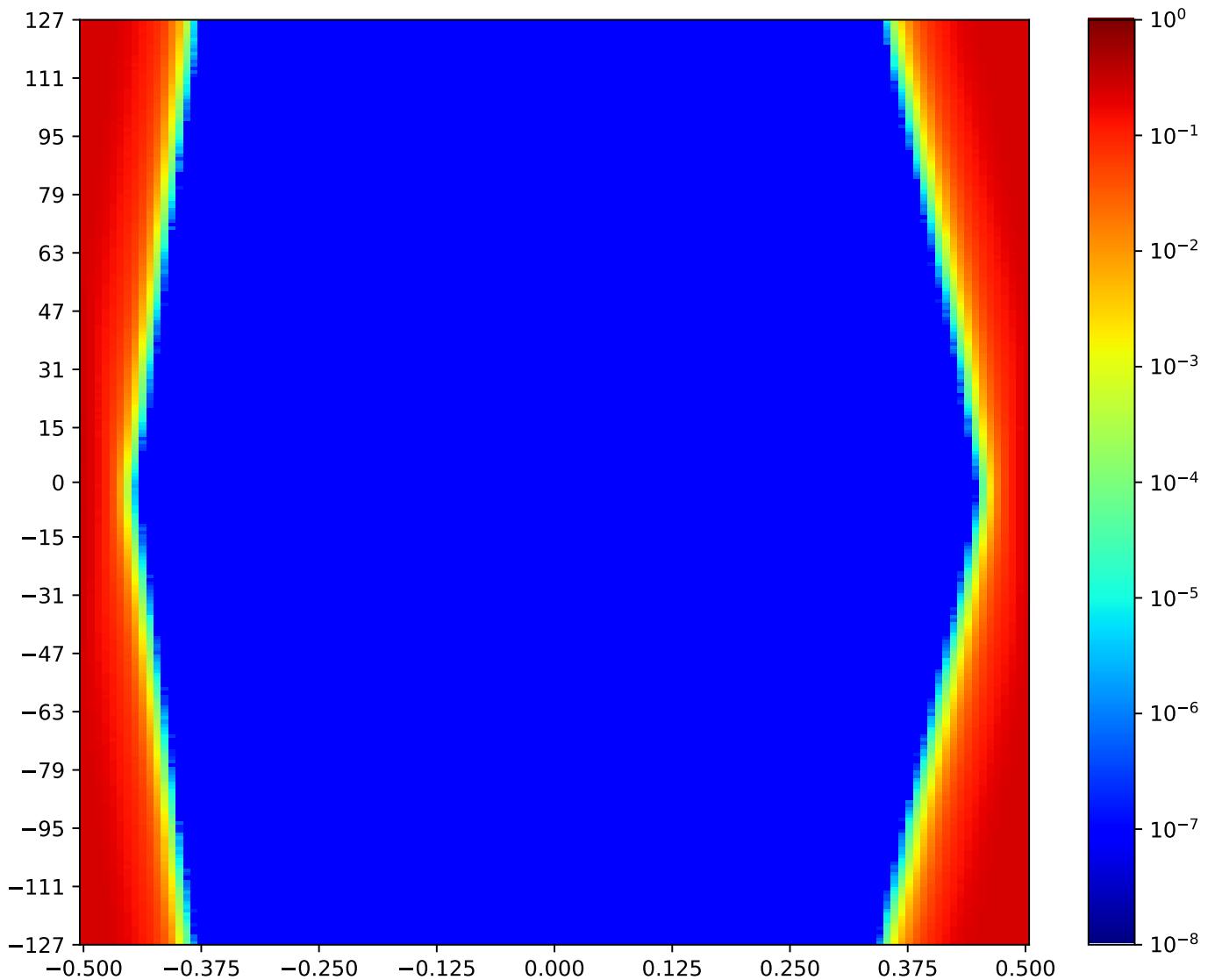


Figure 1.82: MSP\_A\_FPGA-IC39-12-IC4-12-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.14 MSP\_A\_FPGA-IC39-13-IC4-13-TRP\_FPGA

Table 1.75: MSP\_A\_FPGA-IC39-13-IC4-13-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:22:14		2018-Jan-24 04:23:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26043	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

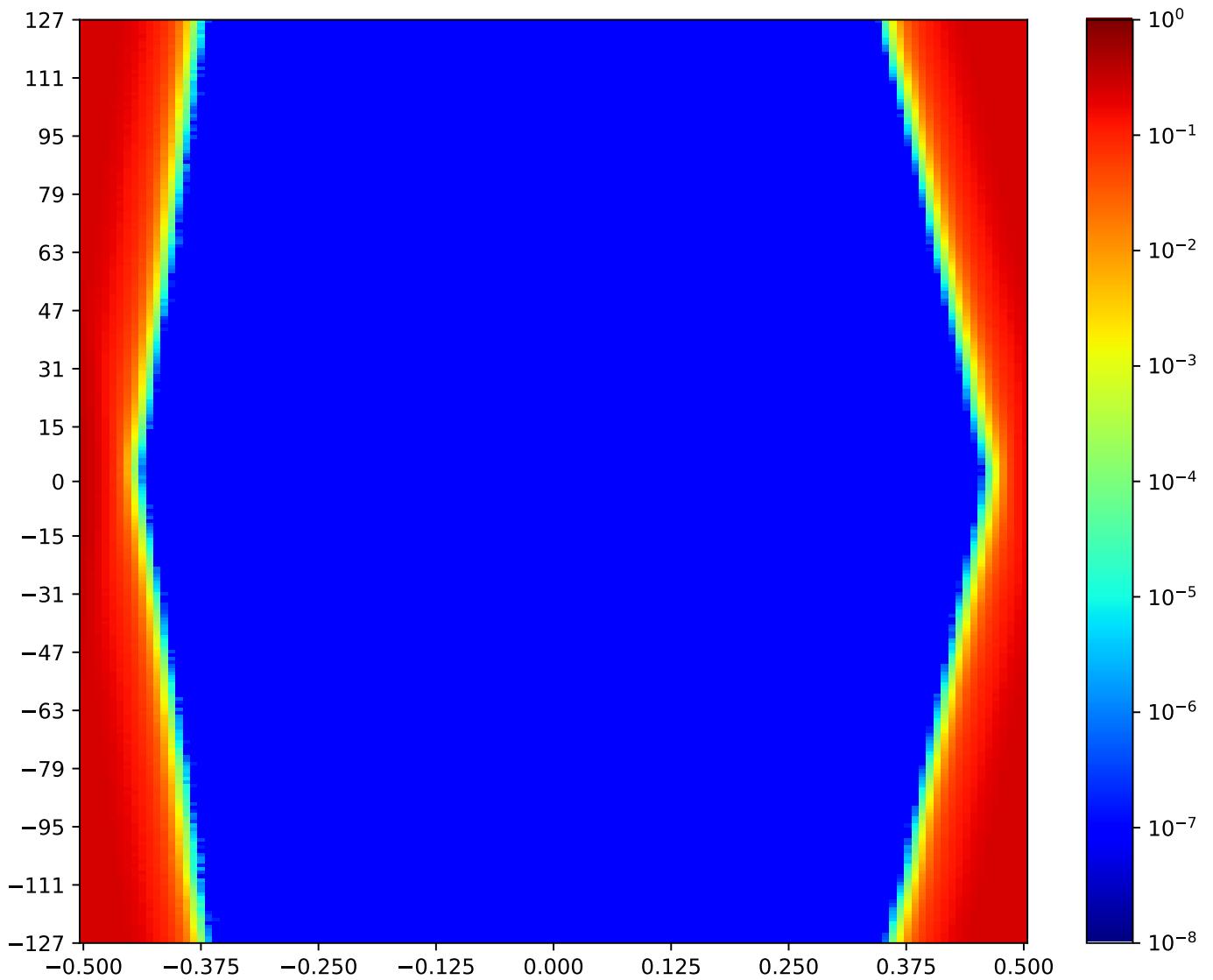


Figure 1.83: MSP\_A\_FPGA-IC39-13-IC4-13-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.15 MSP\_A\_FPGA-IC39-14-IC4-14-TRP\_FPGA

Table 1.76: MSP\_A\_FPGA-IC39-14-IC4-14-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:23:25		2018-Jan-24 04:24:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25265	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

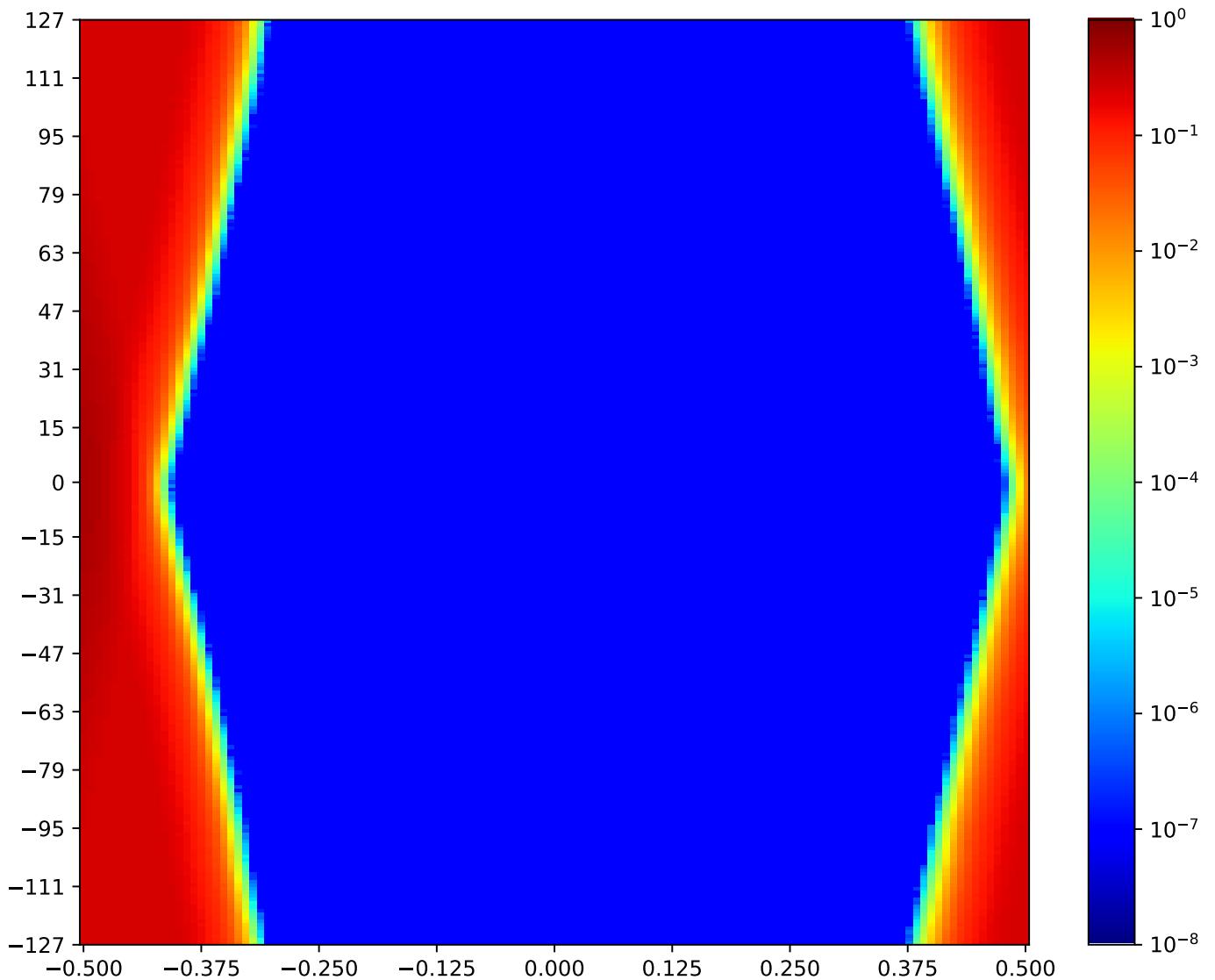


Figure 1.84: MSP\_A\_FPGA-IC39-14-IC4-14-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.16 MSP\_A\_FPGA-IC39-15-IC4-15-TRP\_FPGA

Table 1.77: MSP\_A\_FPGA-IC39-15-IC4-15-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:24:35		2018-Jan-24 04:25:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26431	114	88.37%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

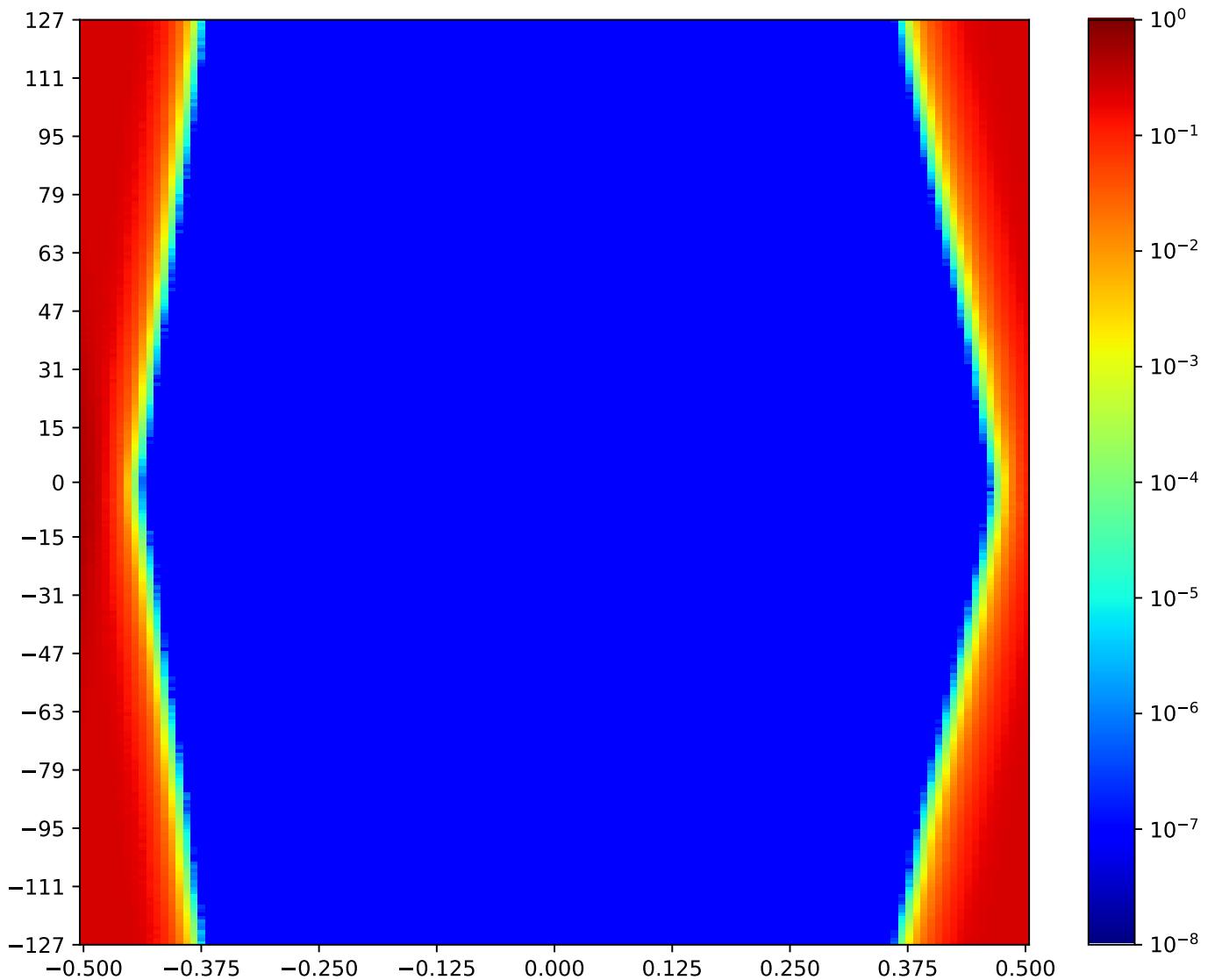


Figure 1.85: MSP\_A\_FPGA-IC39-15-IC4-15-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.17 MSP\_A\_FPGA-IC39-16-IC4-16-TRP\_FPGA

Table 1.78: MSP\_A\_FPGA-IC39-16-IC4-16-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:25:46		2018-Jan-24 04:26:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25058	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

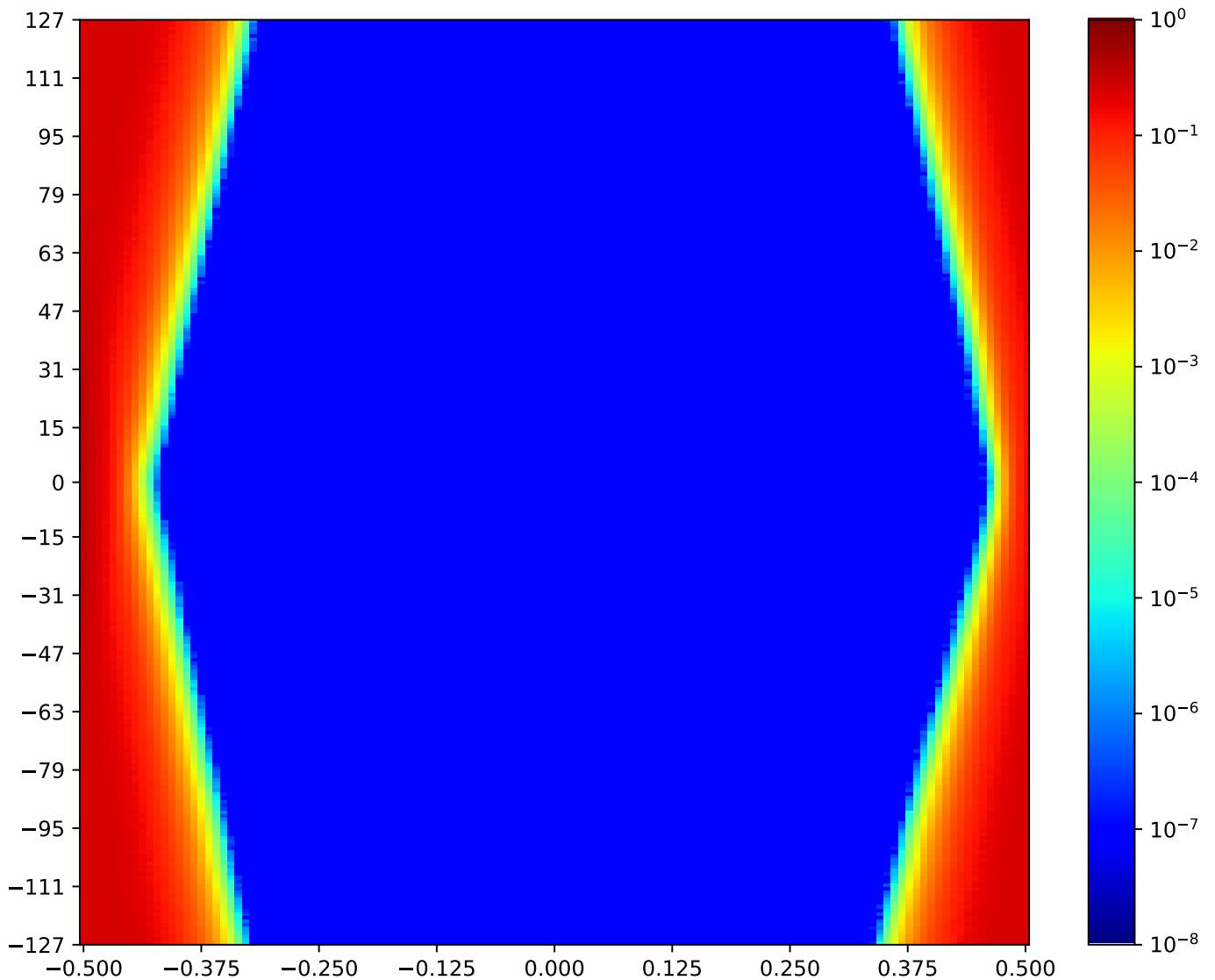


Figure 1.86: MSP\_A\_FPGA-IC39-16-IC4-16-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.18 MSP\_A\_FPGA-IC39-17-IC4-17-TRP\_FPGA

Table 1.79: MSP\_A\_FPGA-IC39-17-IC4-17-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:26:57		2018-Jan-24 04:28:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25220	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

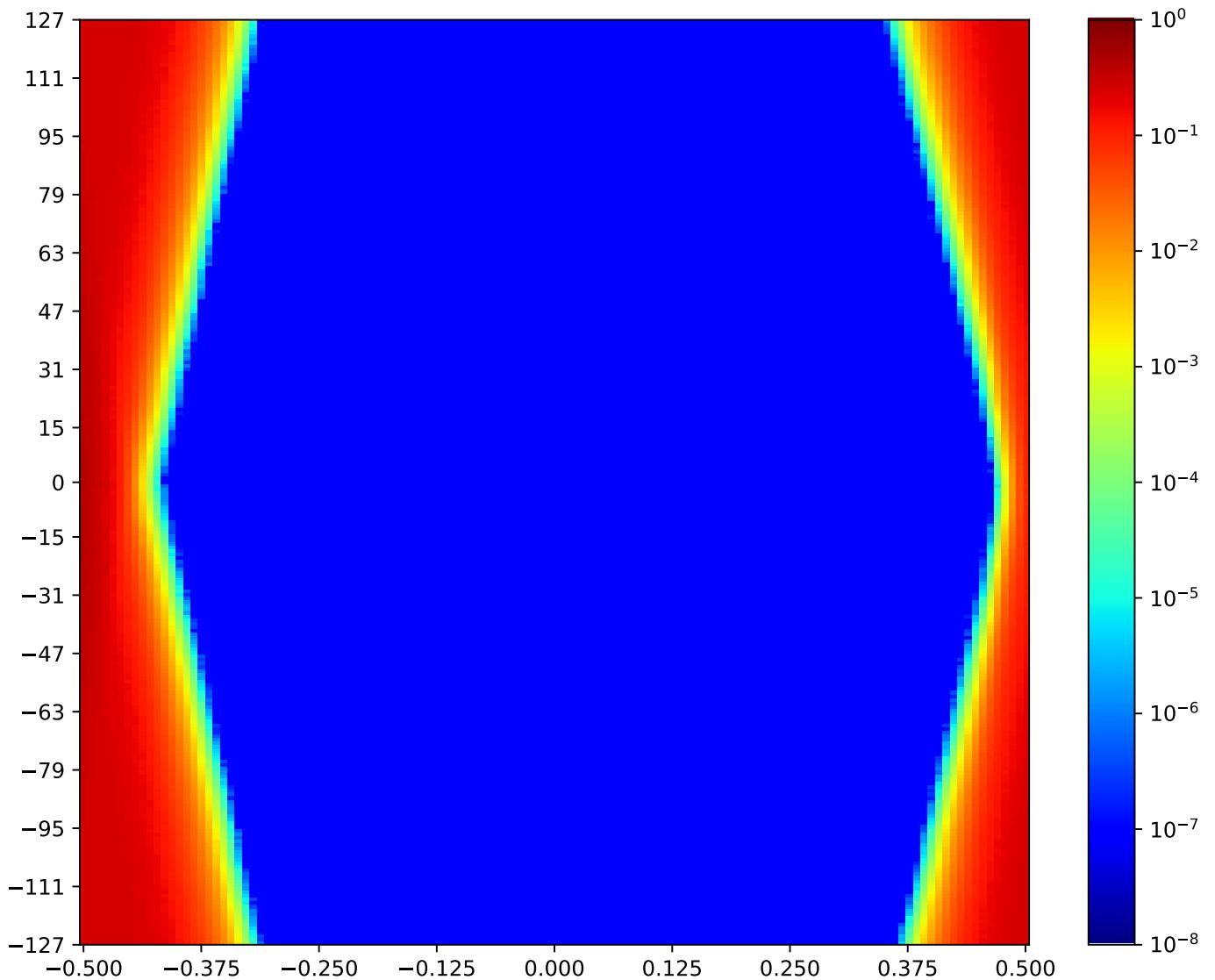


Figure 1.87: MSP\_A\_FPGA-IC39-17-IC4-17-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.19 MSP\_A\_FPGA-IC39-18-IC4-18-TRP\_FPGA

Table 1.80: MSP\_A\_FPGA-IC39-18-IC4-18-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:28:09		2018-Jan-24 04:29:18	
Reset RX	OA	HO		VO   VO (%)	
true	24698	110		85.27%   255   100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

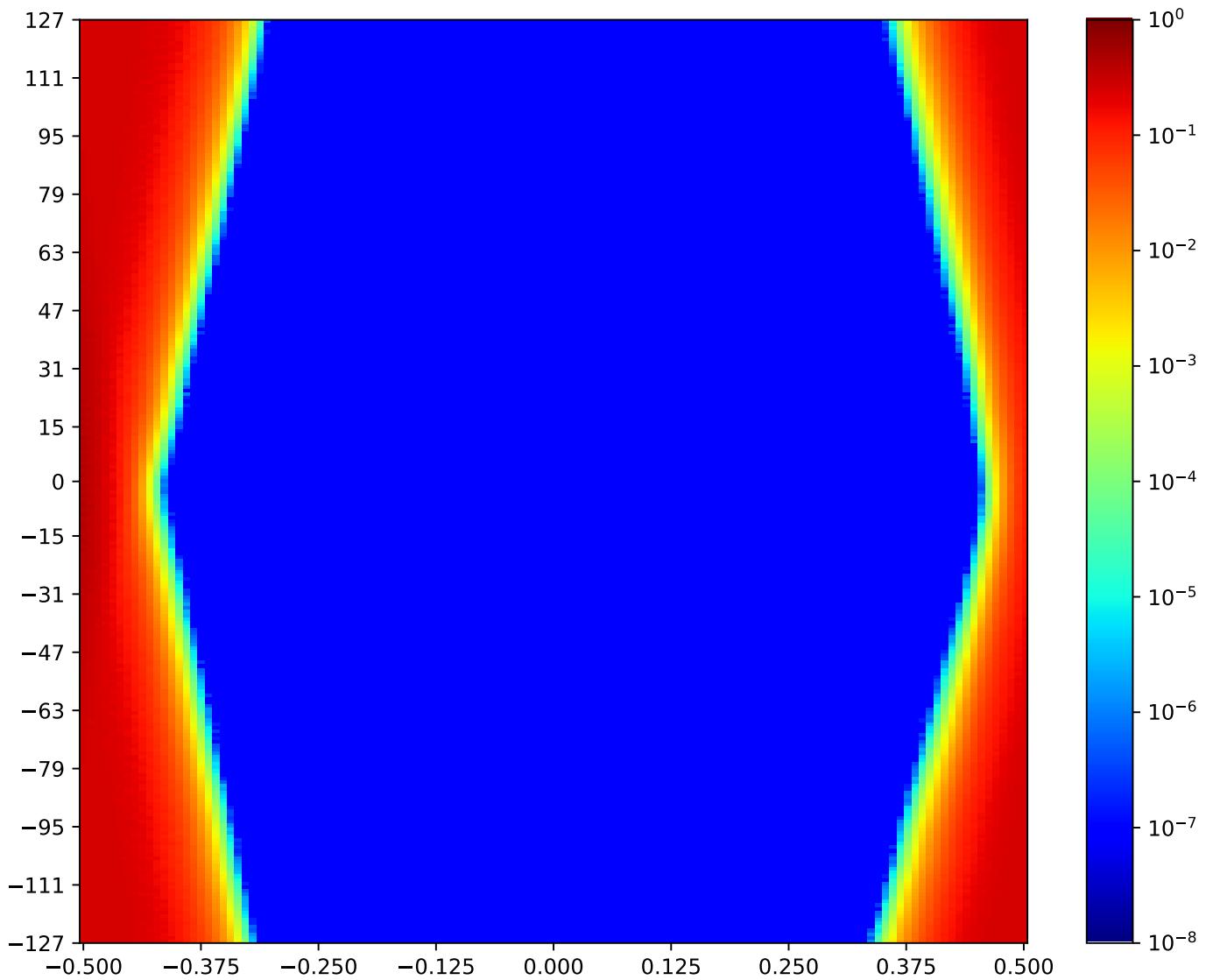


Figure 1.88: MSP\_A\_FPGA-IC39-18-IC4-18-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.20 MSP\_A\_FPGA-IC39-19-IC4-19-TRP\_FPGA

Table 1.81: MSP\_A\_FPGA-IC39-19-IC4-19-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:29:18		2018-Jan-24 04:30:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24985	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

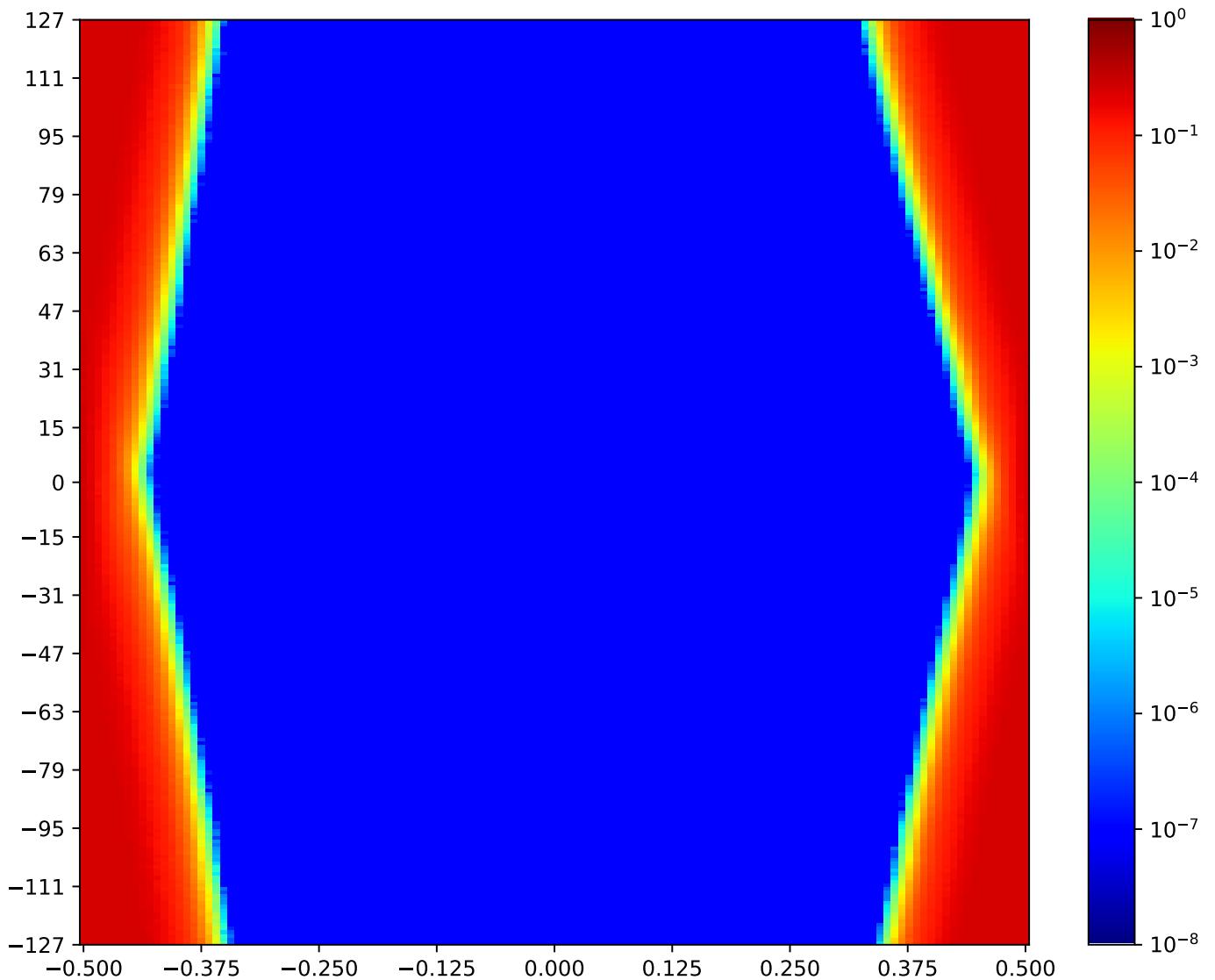


Figure 1.89: MSP\_A\_FPGA-IC39-19-IC4-19-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.21 MSP\_A\_FPGA-IC39-20-IC4-20-TRP\_FPGA

Table 1.82: MSP\_A\_FPGA-IC39-20-IC4-20-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:30:28		2018-Jan-24 04:31:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26272	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

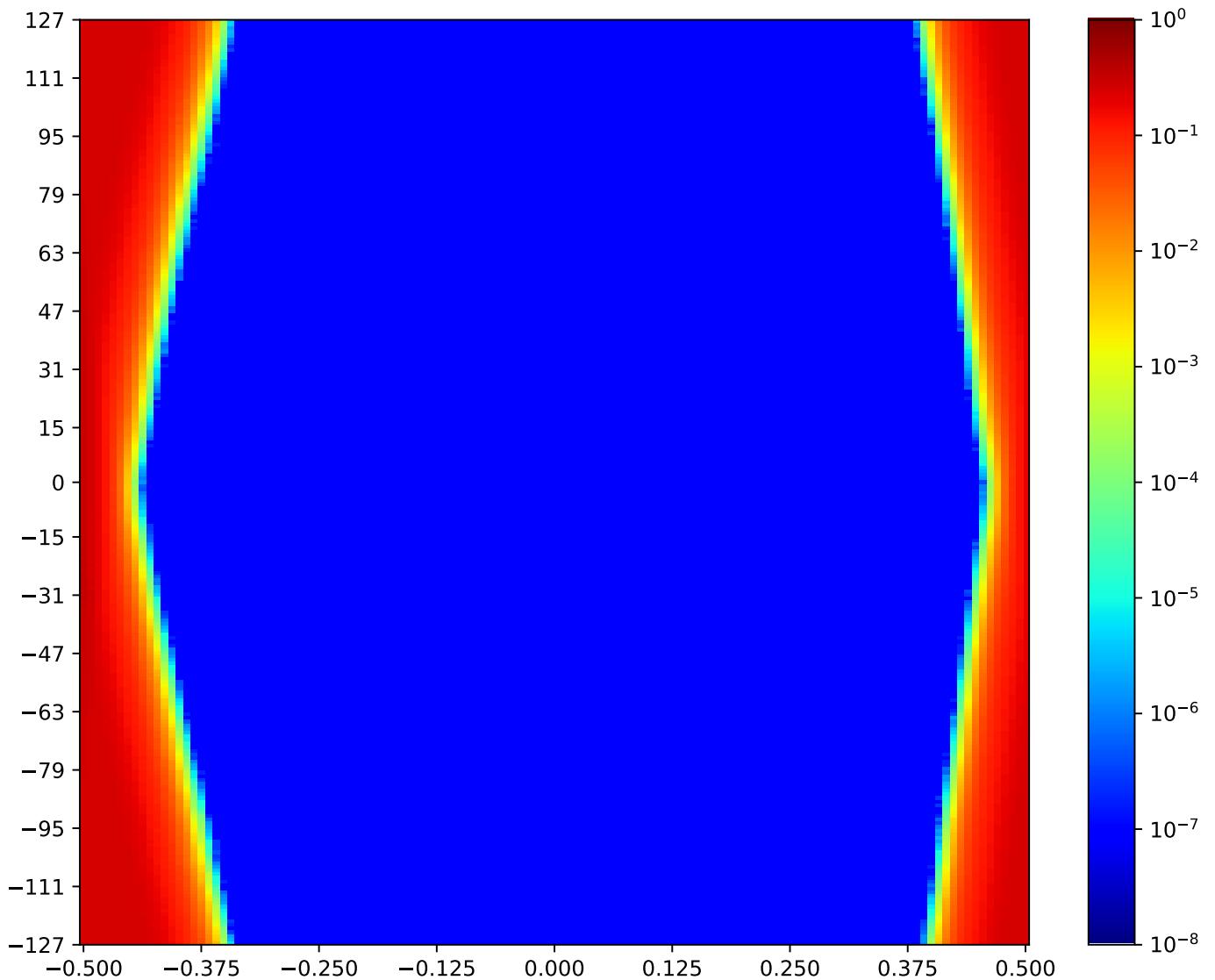


Figure 1.90: MSP\_A\_FPGA-IC39-20-IC4-20-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.22 MSP\_A\_FPGA-IC39-21-IC4-21-TRP\_FPGA

Table 1.83: MSP\_A\_FPGA-IC39-21-IC4-21-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:31:39		2018-Jan-24 04:32:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24021	111	86.05%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

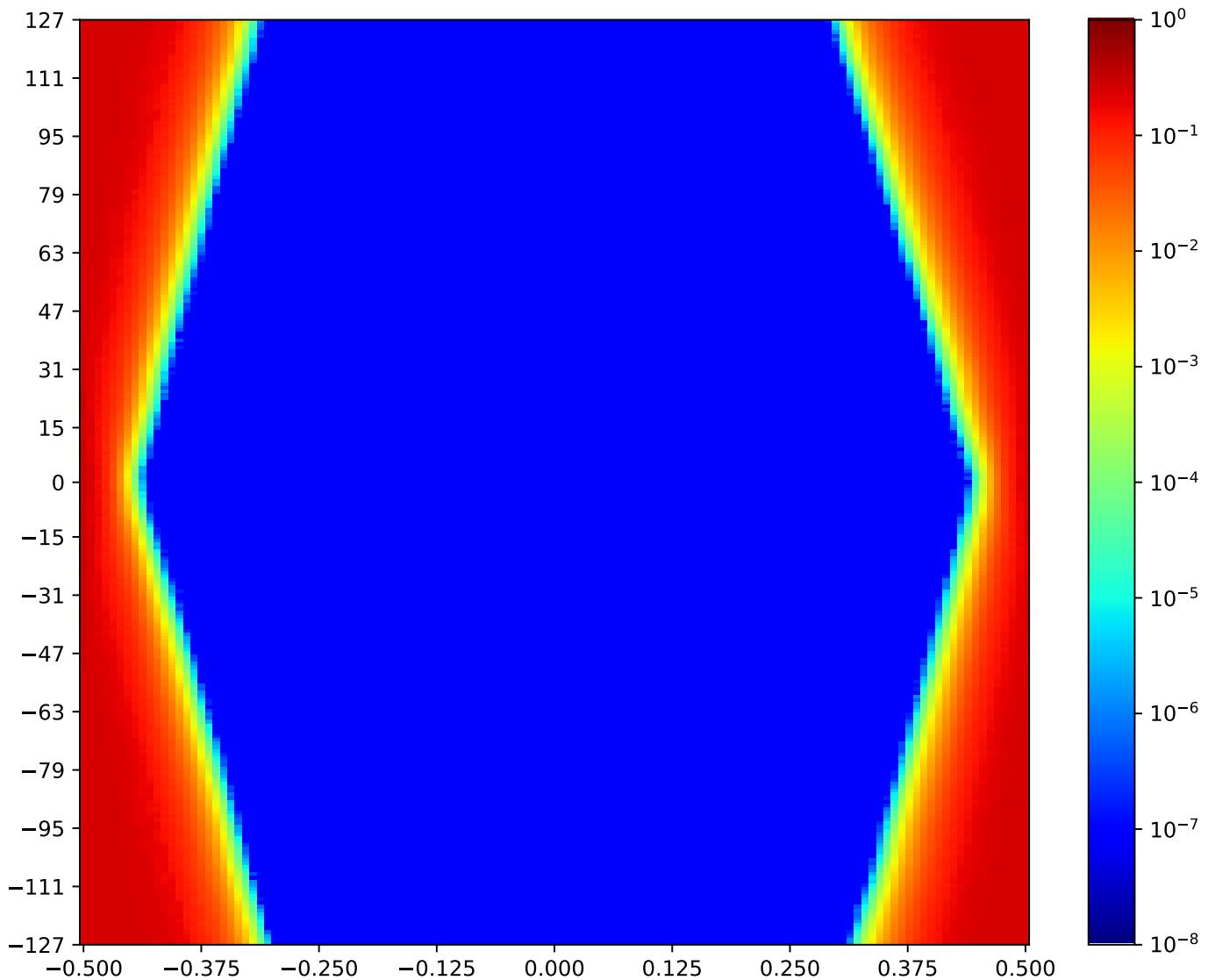


Figure 1.91: MSP\_A\_FPGA-IC39-21-IC4-21-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.23 MSP\_A\_FPGA-IC39-22-IC4-22-TRP\_FPGA

Table 1.84: MSP\_A\_FPGA-IC39-22-IC4-22-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:32:50		2018-Jan-24 04:34:02	
Reset RX	OA	HO		VO   VO (%)	
true	27017	114		88.37%   255   100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

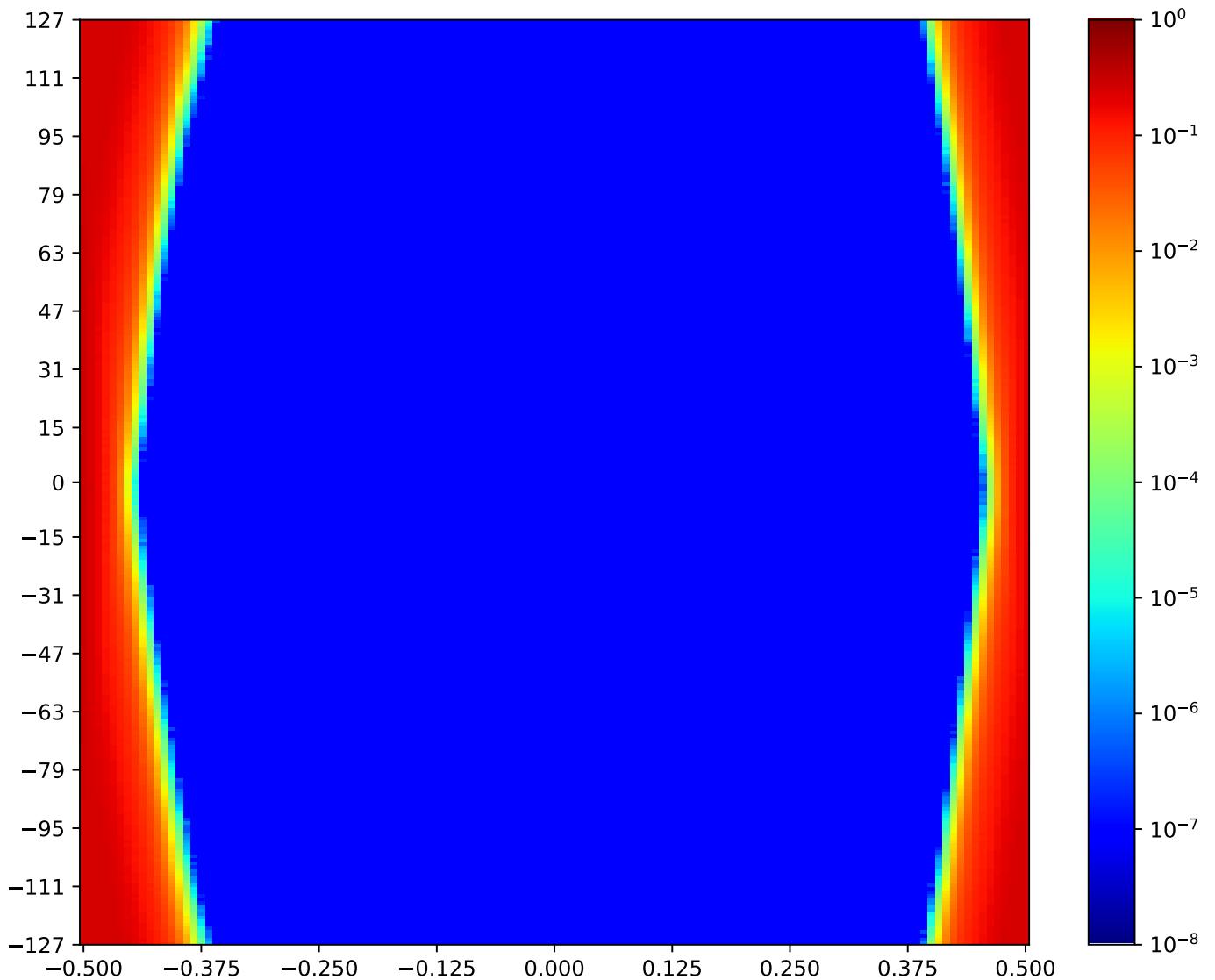


Figure 1.92: MSP\_A\_FPGA-IC39-22-IC4-22-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.24 MSP\_A\_FPGA-IC39-23-IC4-23-TRP\_FPGA

Table 1.85: MSP\_A\_FPGA-IC39-23-IC4-23-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:34:02		2018-Jan-24 04:35:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26158	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

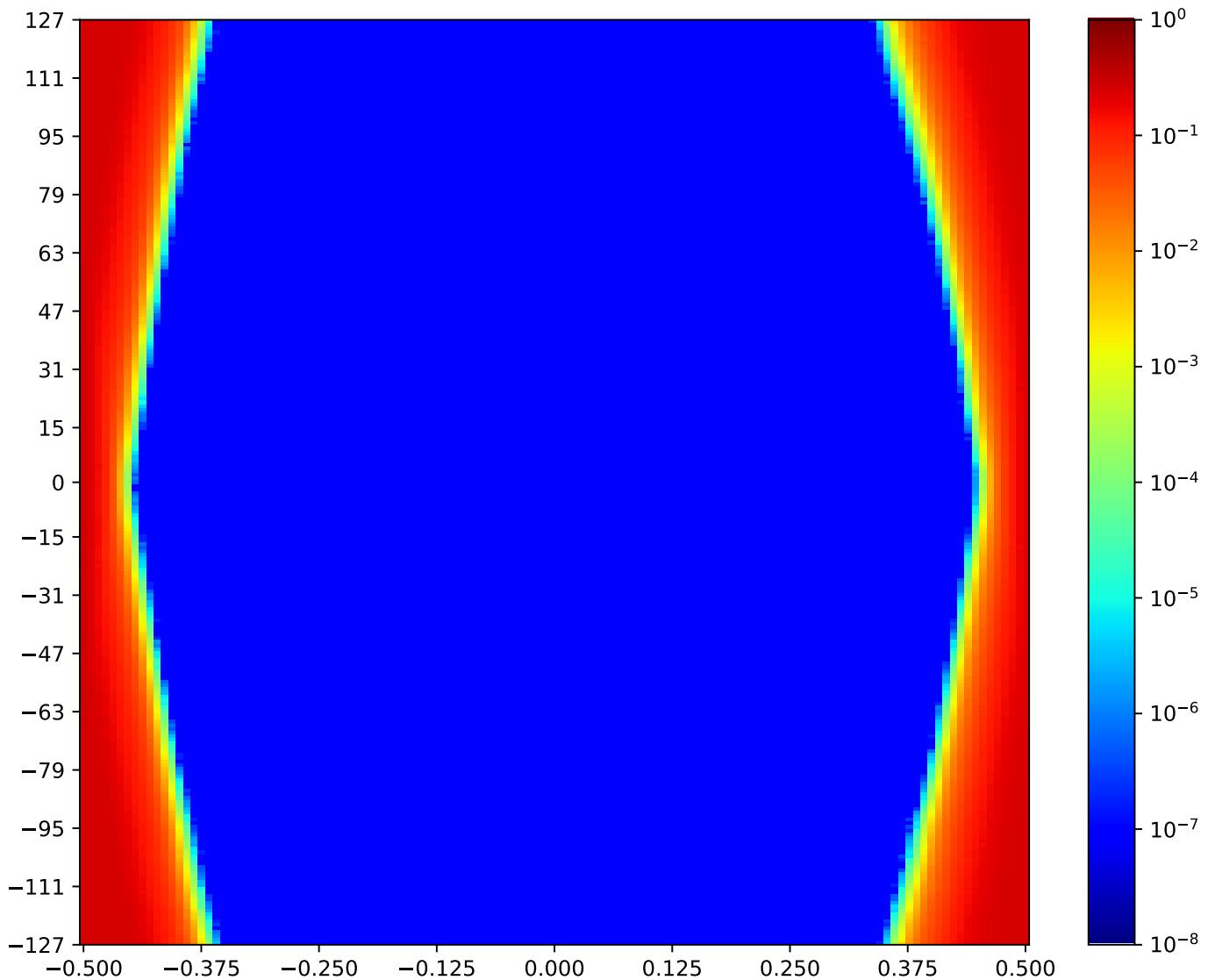


Figure 1.93: MSP\_A\_FPGA-IC39-23-IC4-23-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.25 MSP\_A\_FPGA-IC39-24-IC4-24-TRP\_FPGA

Table 1.86: MSP\_A\_FPGA-IC39-24-IC4-24-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:35:14		2018-Jan-24 04:36:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25233	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

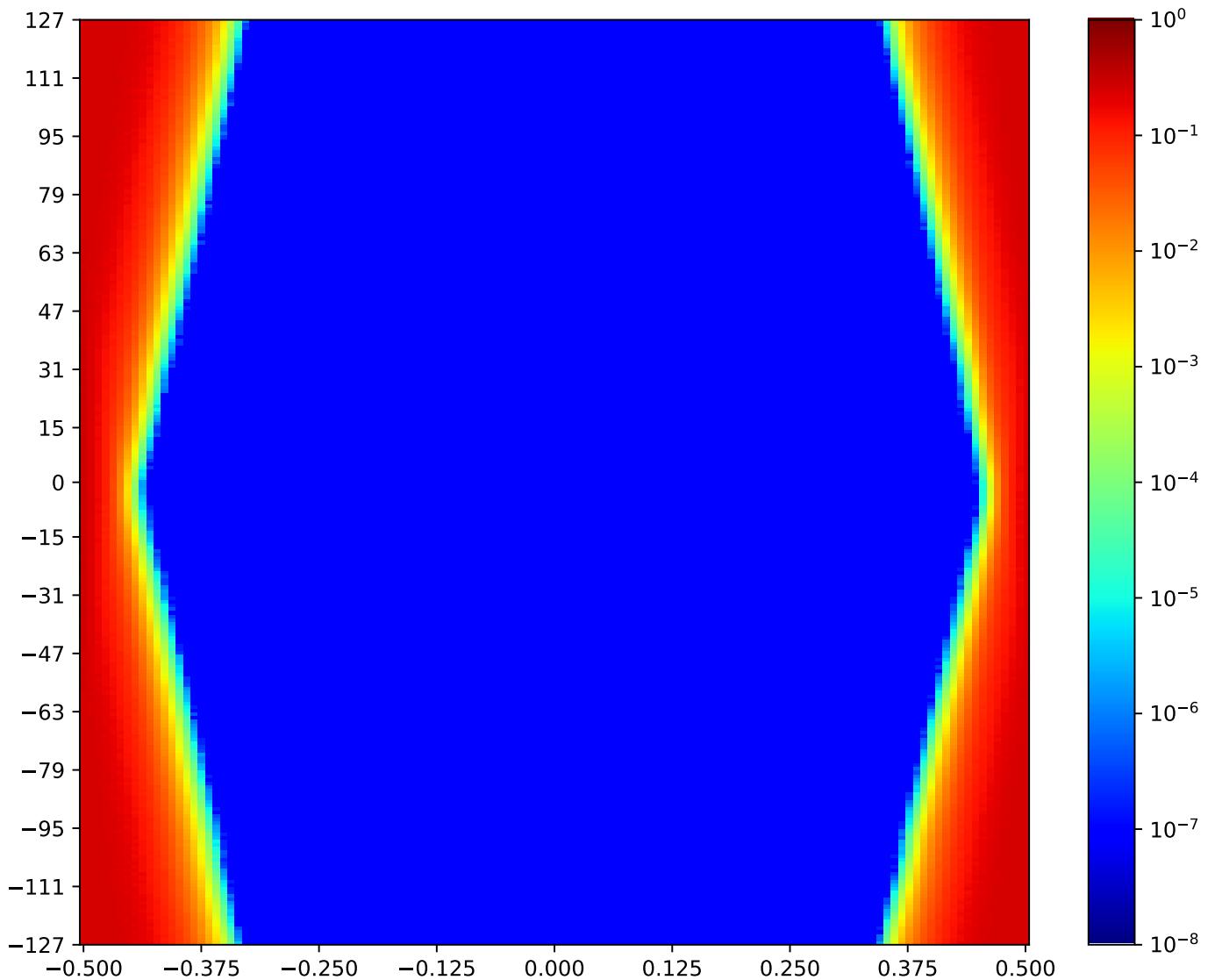


Figure 1.94: MSP\_A\_FPGA-IC39-24-IC4-24-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.26 MSP\_A\_FPGA-IC39-25-IC4-25-TRP\_FPGA

Table 1.87: MSP\_A\_FPGA-IC39-25-IC4-25-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:36:24		2018-Jan-24 04:37:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26102	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

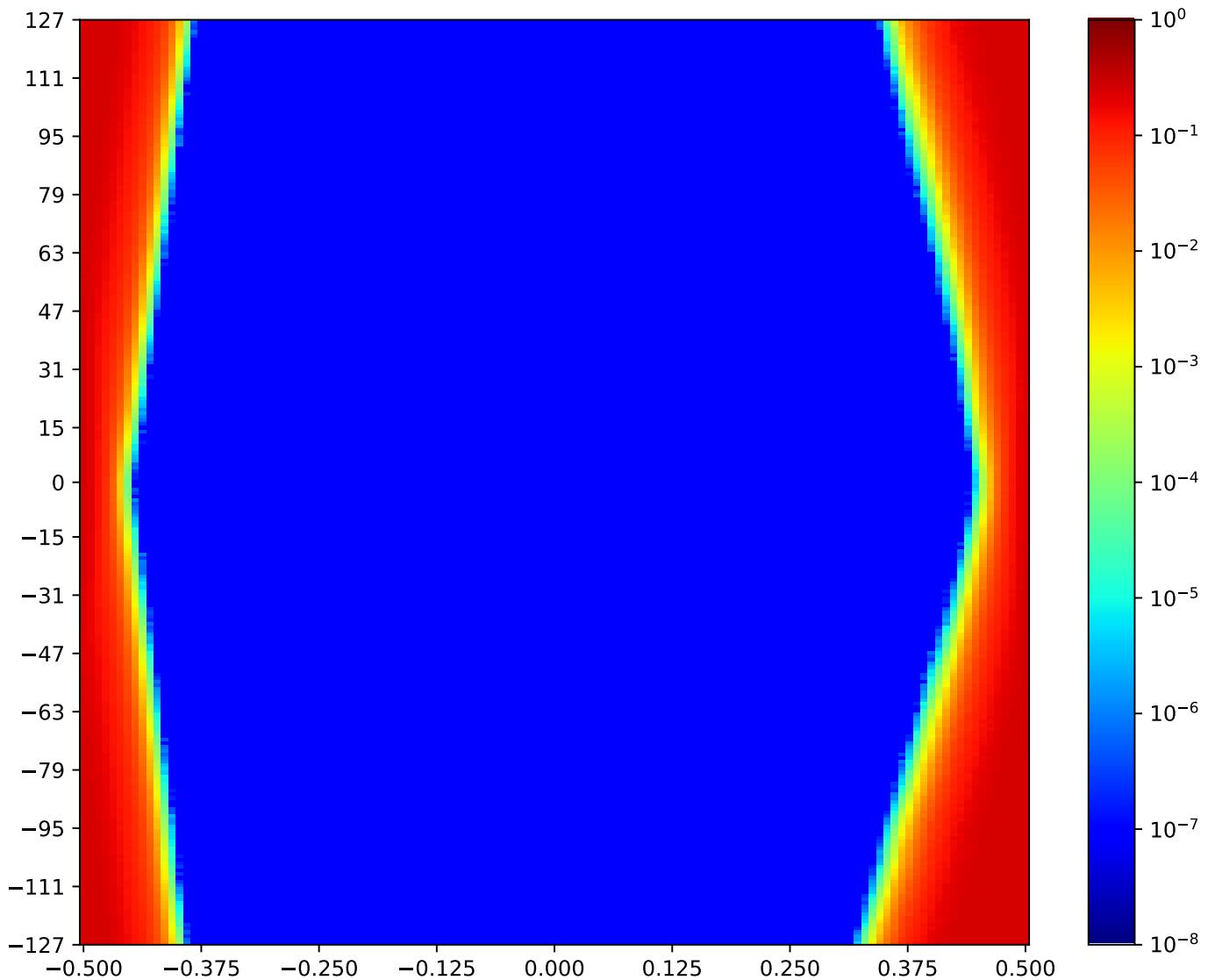


Figure 1.95: MSP\_A\_FPGA-IC39-25-IC4-25-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.27 MSP\_A\_FPGA-IC39-26-IC4-26-TRP\_FPGA

Table 1.88: MSP\_A\_FPGA-IC39-26-IC4-26-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:37:36		2018-Jan-24 04:38:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25203	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

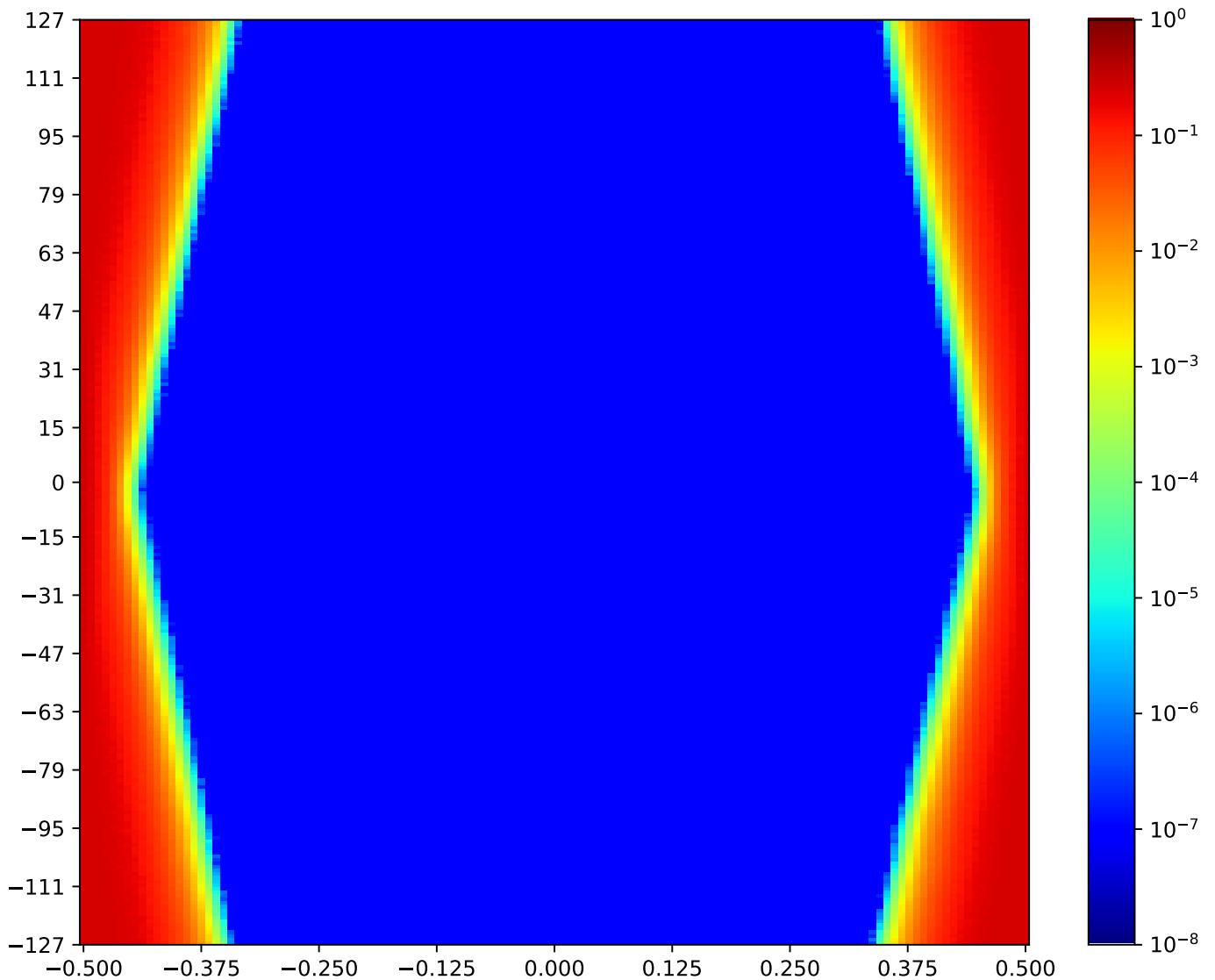


Figure 1.96: MSP\_A\_FPGA-IC39-26-IC4-26-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.8.28 MSP\_A\_FPGA-IC39-27-IC4-27-TRP\_FPGA

Table 1.89: MSP\_A\_FPGA-IC39-27-IC4-27-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:38:47		2018-Jan-24 04:39:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25578	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

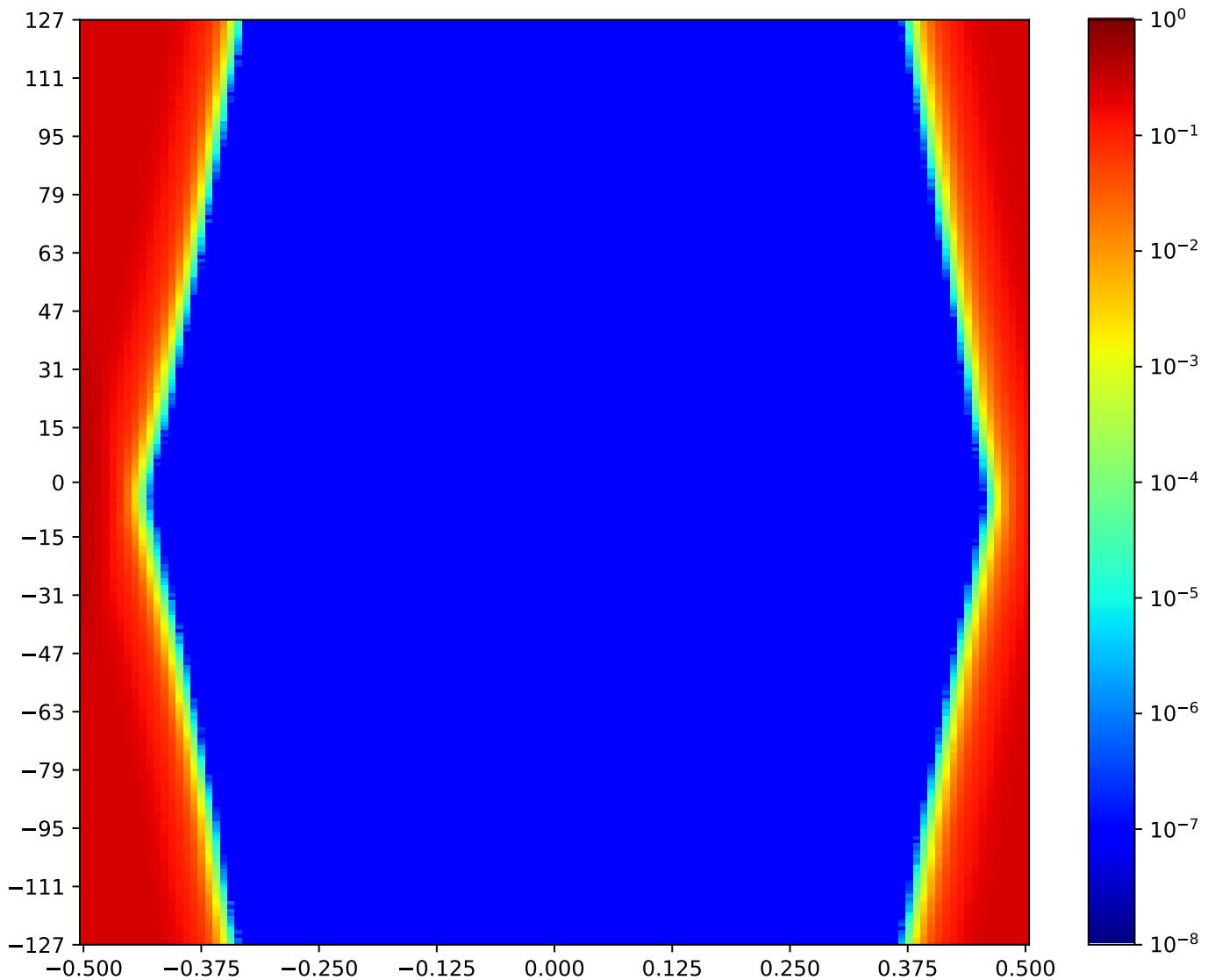


Figure 1.97: MSP\_A\_FPGA-IC39-27-IC4-27-TRP\_FPGA

Call back to summary Figure 1.69. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.9 MSP\_C TRP On board links

A cross-reference to Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.127.

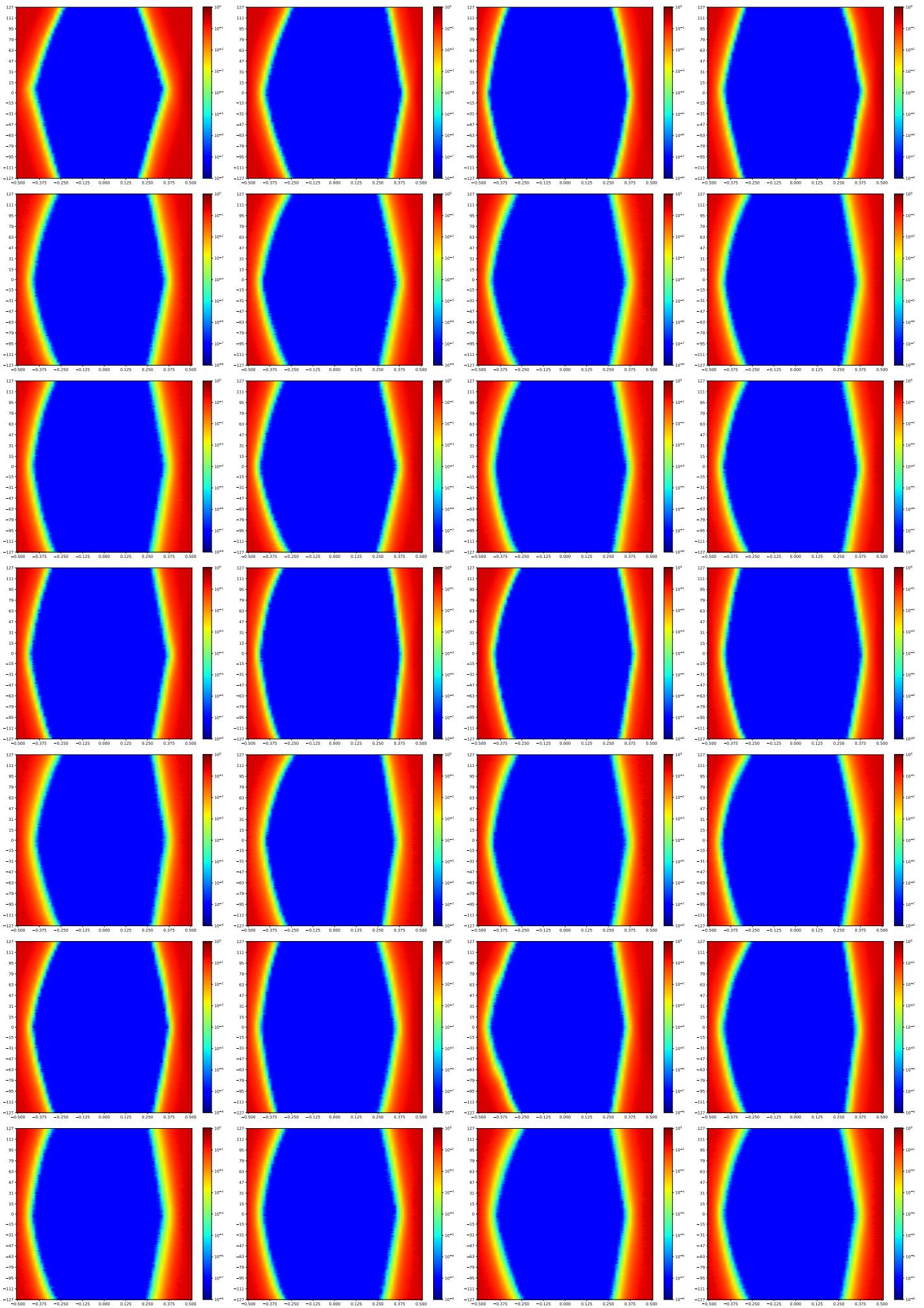


Figure 1.98: MSP\_C TRP On board links

### 1.9.1 MSP\_C\_FPGA-IC39-00-IC15-00-TRP\_FPGA

Table 1.90: MSP\_C\_FPGA-IC39-00-IC15-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:39:58		2018-Jan-24 04:40:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9329	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

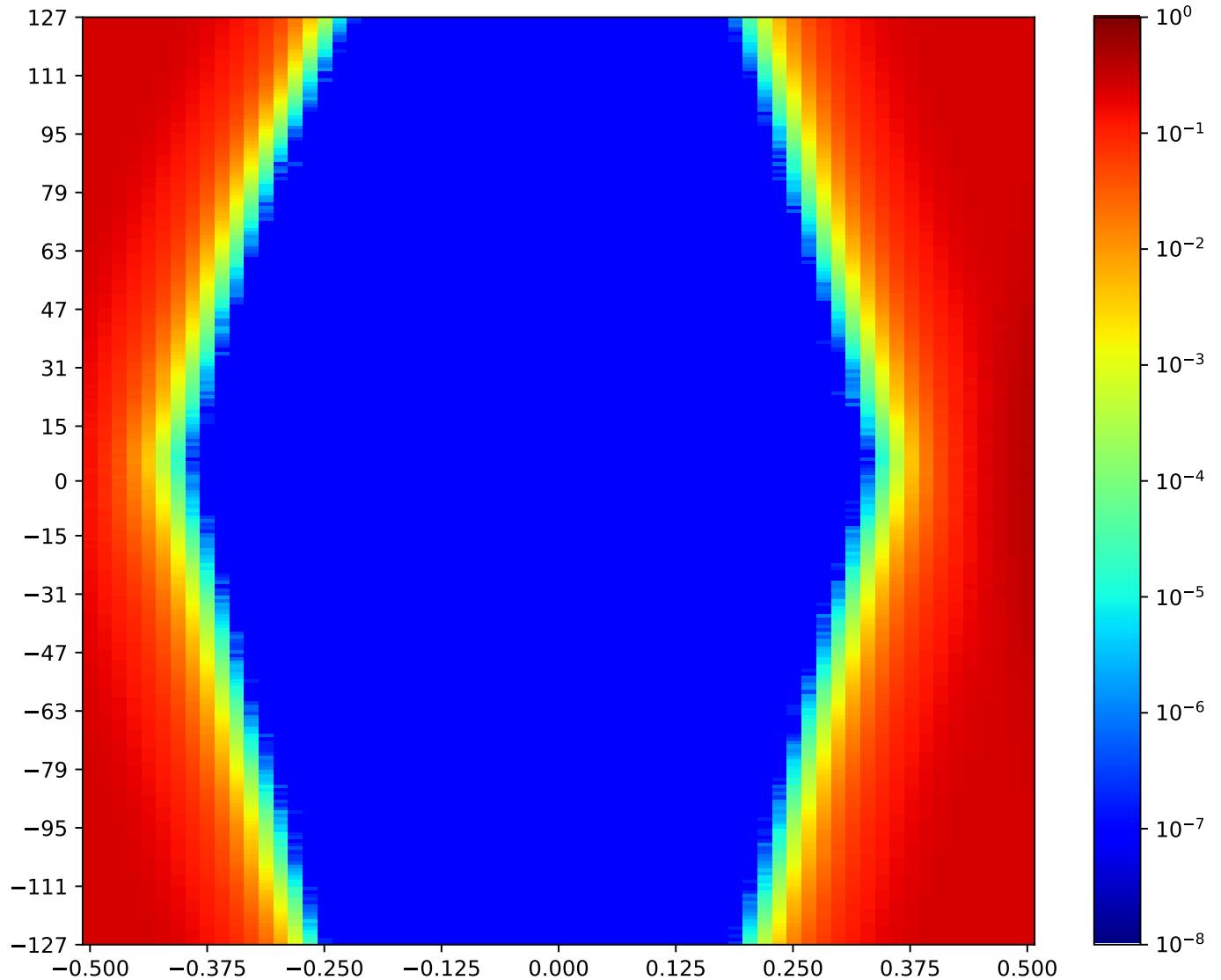


Figure 1.99: MSP\_C\_FPGA-IC39-00-IC15-00-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.2 MSP\_C\_FPGA-IC39-01-IC15-01-TRP\_FPGA

Table 1.91: MSP\_C\_FPGA-IC39-01-IC15-01-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:40:32		2018-Jan-24 04:41:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10647	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

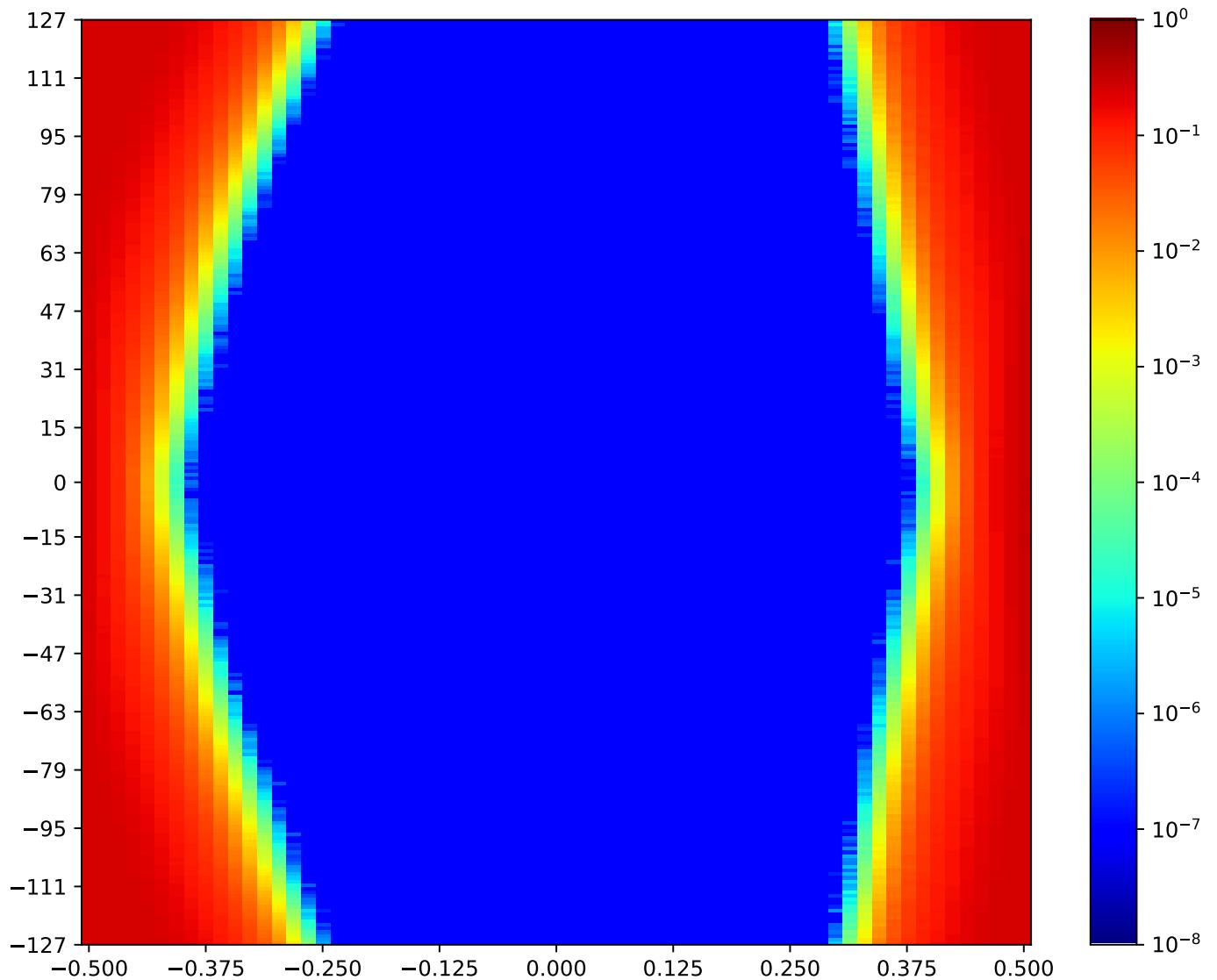


Figure 1.100: MSP\_C\_FPGA-IC39-01-IC15-01-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.3 MSP\_C\_FPGA-IC39-02-IC15-02-TRP\_FPGA

Table 1.92: MSP\_C\_FPGA-IC39-02-IC15-02-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:41:09		2018-Jan-24 04:41:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11284	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

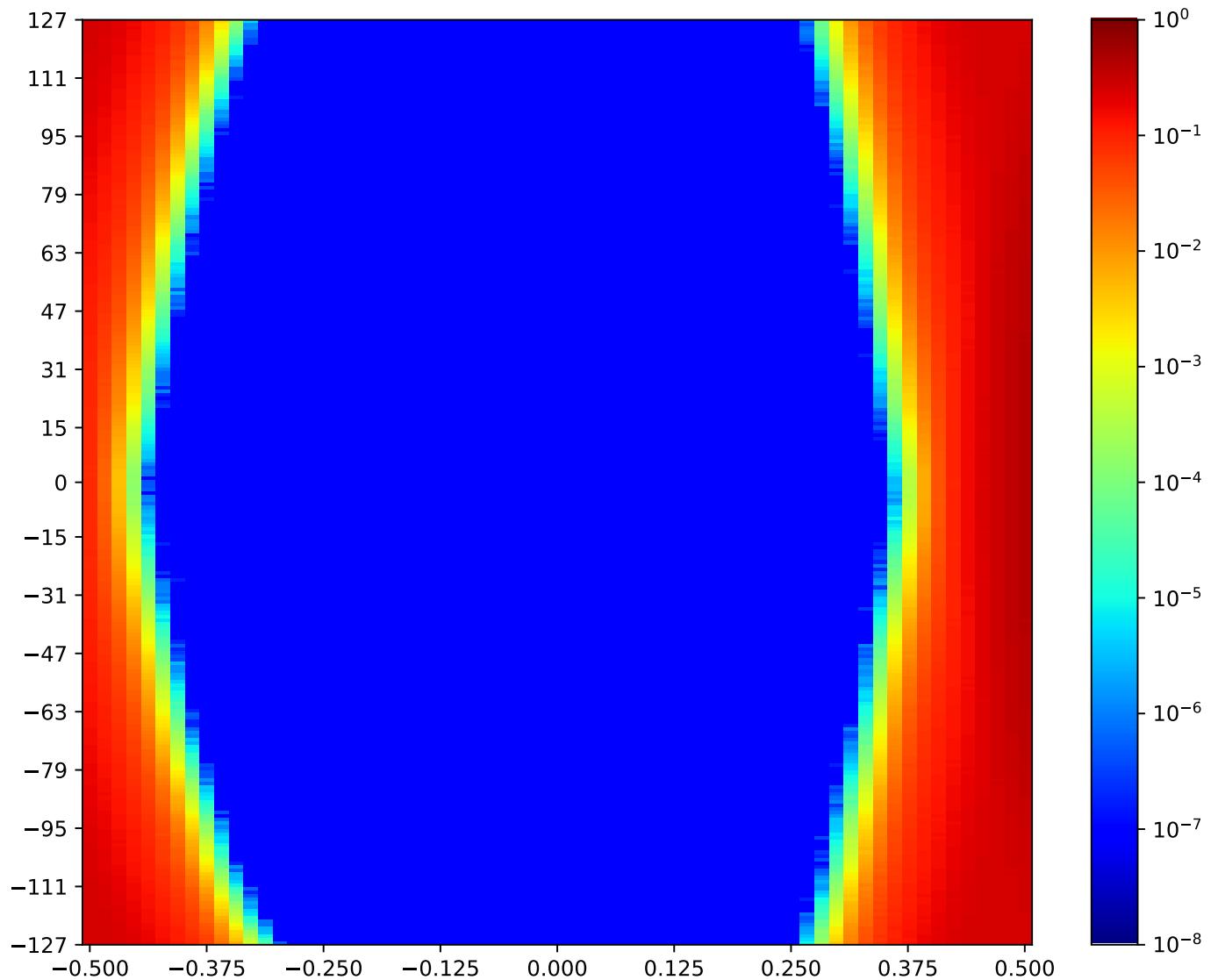


Figure 1.101: MSP\_C\_FPGA-IC39-02-IC15-02-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.9.4 MSP\_C\_FPGA-IC39-03-IC15-03-TRP\_FPGA

Table 1.93: MSP\_C\_FPGA-IC39-03-IC15-03-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:41:45		2018-Jan-24 04:42:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10814	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

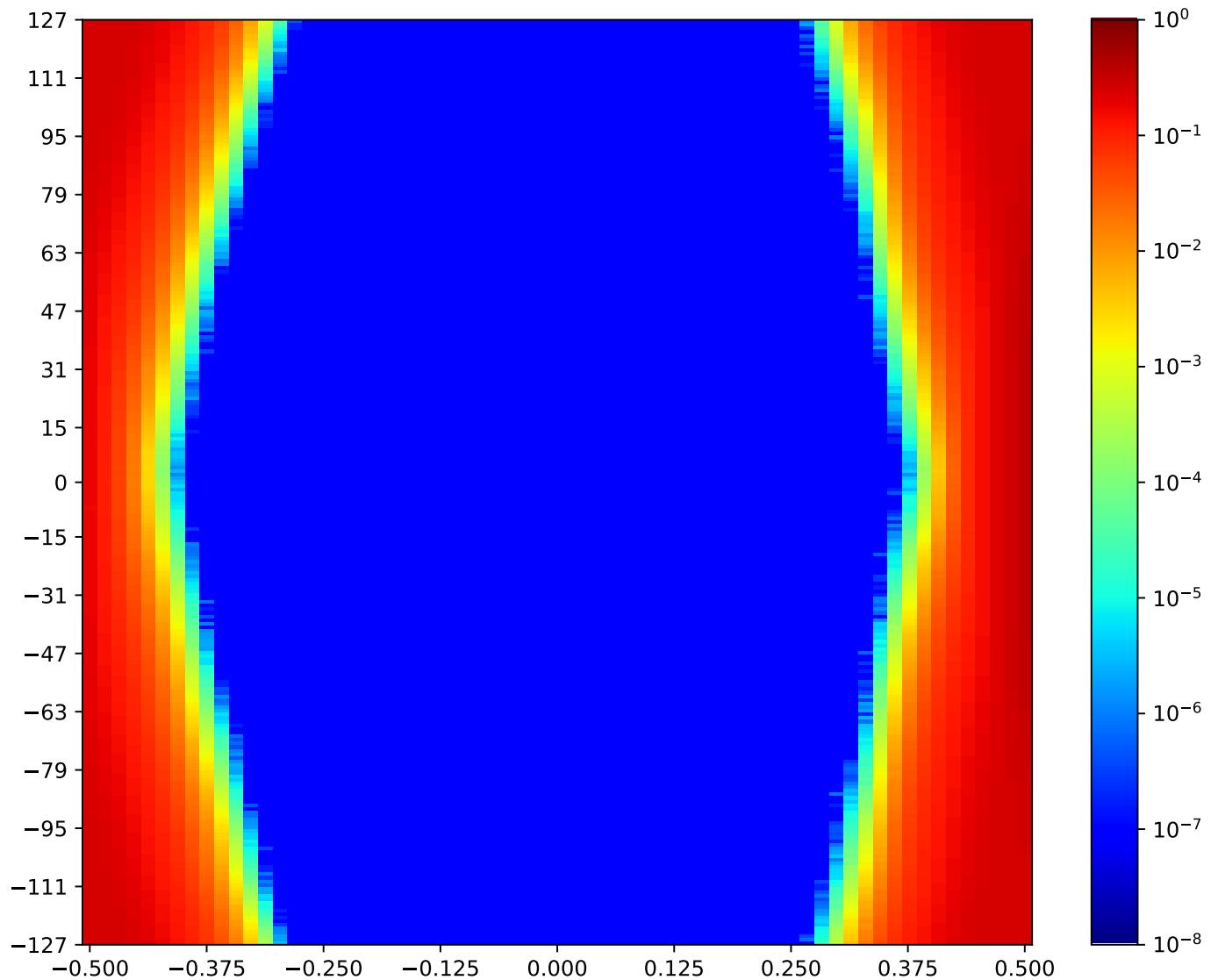


Figure 1.102: MSP\_C\_FPGA-IC39-03-IC15-03-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.5 MSP\_C\_FPGA-IC39-04-IC15-04-TRP\_FPGA

Table 1.94: MSP\_C\_FPGA-IC39-04-IC15-04-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:42:22		2018-Jan-24 04:42:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10218	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

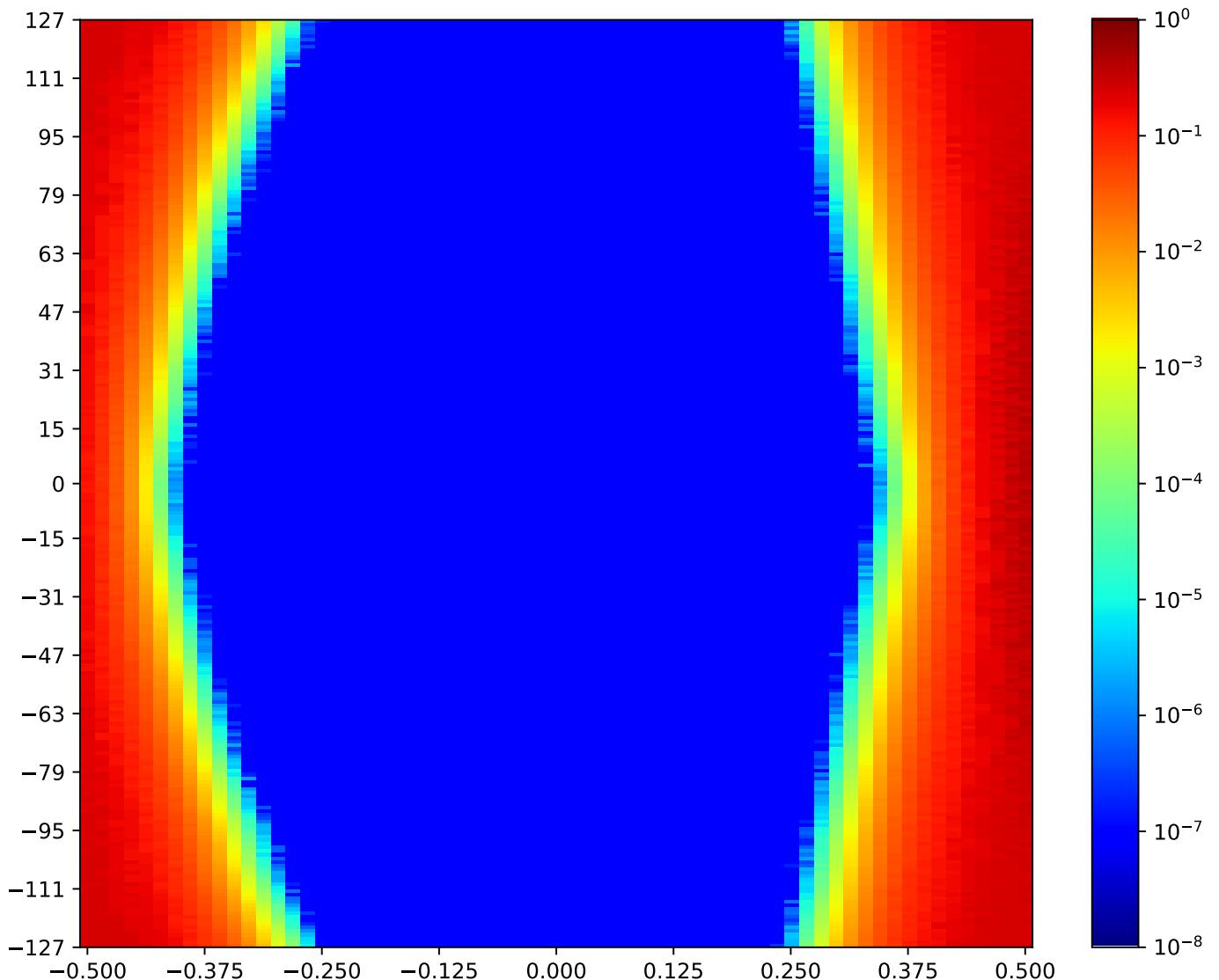


Figure 1.103: MSP\_C\_FPGA-IC39-04-IC15-04-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.6 MSP\_C\_FPGA-IC39-05-IC15-05-TRP\_FPGA

Table 1.95: MSP\_C\_FPGA-IC39-05-IC15-05-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:42:59		2018-Jan-24 04:43:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10324	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

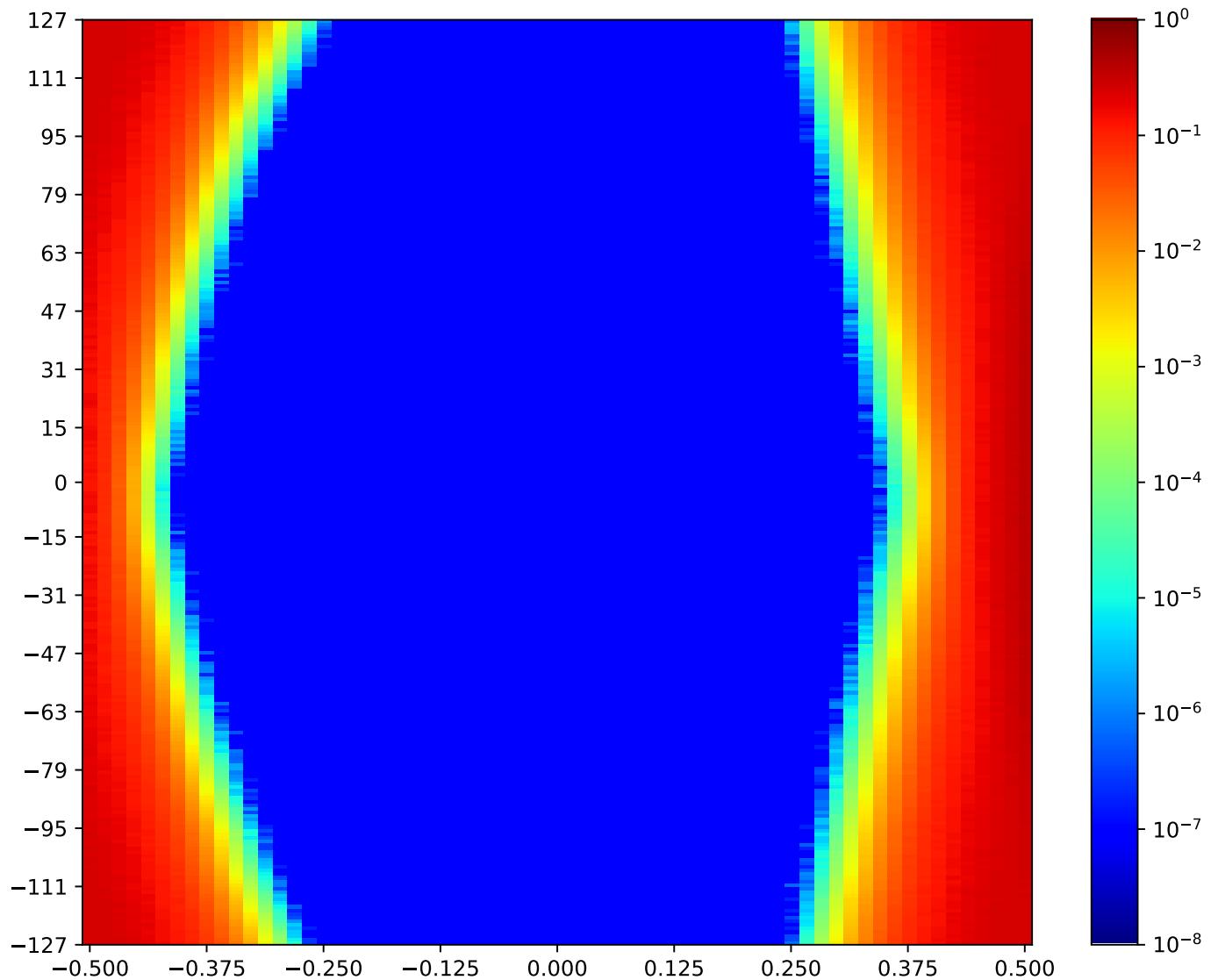


Figure 1.104: MSP\_C\_FPGA-IC39-05-IC15-05-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.7 MSP\_C\_FPGA-IC39-06-IC15-06-TRP\_FPGA

Table 1.96: MSP\_C\_FPGA-IC39-06-IC15-06-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:43:35		2018-Jan-24 04:44:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10407	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

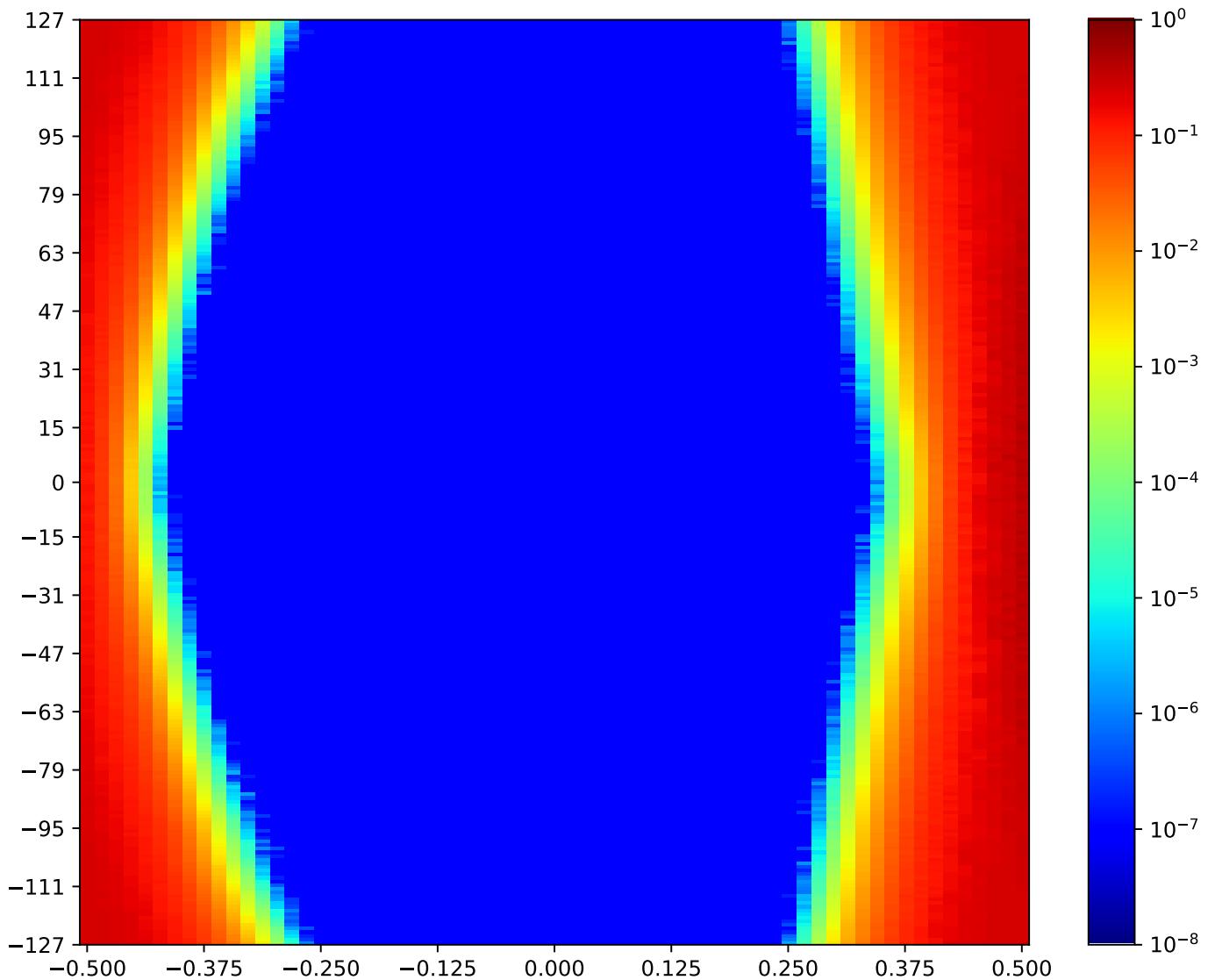


Figure 1.105: MSP\_C\_FPGA-IC39-06-IC15-06-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.8 MSP\_C\_FPGA-IC39-07-IC15-07-TRP\_FPGA

Table 1.97: MSP\_C\_FPGA-IC39-07-IC15-07-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:44:12		2018-Jan-24 04:44:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10368	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

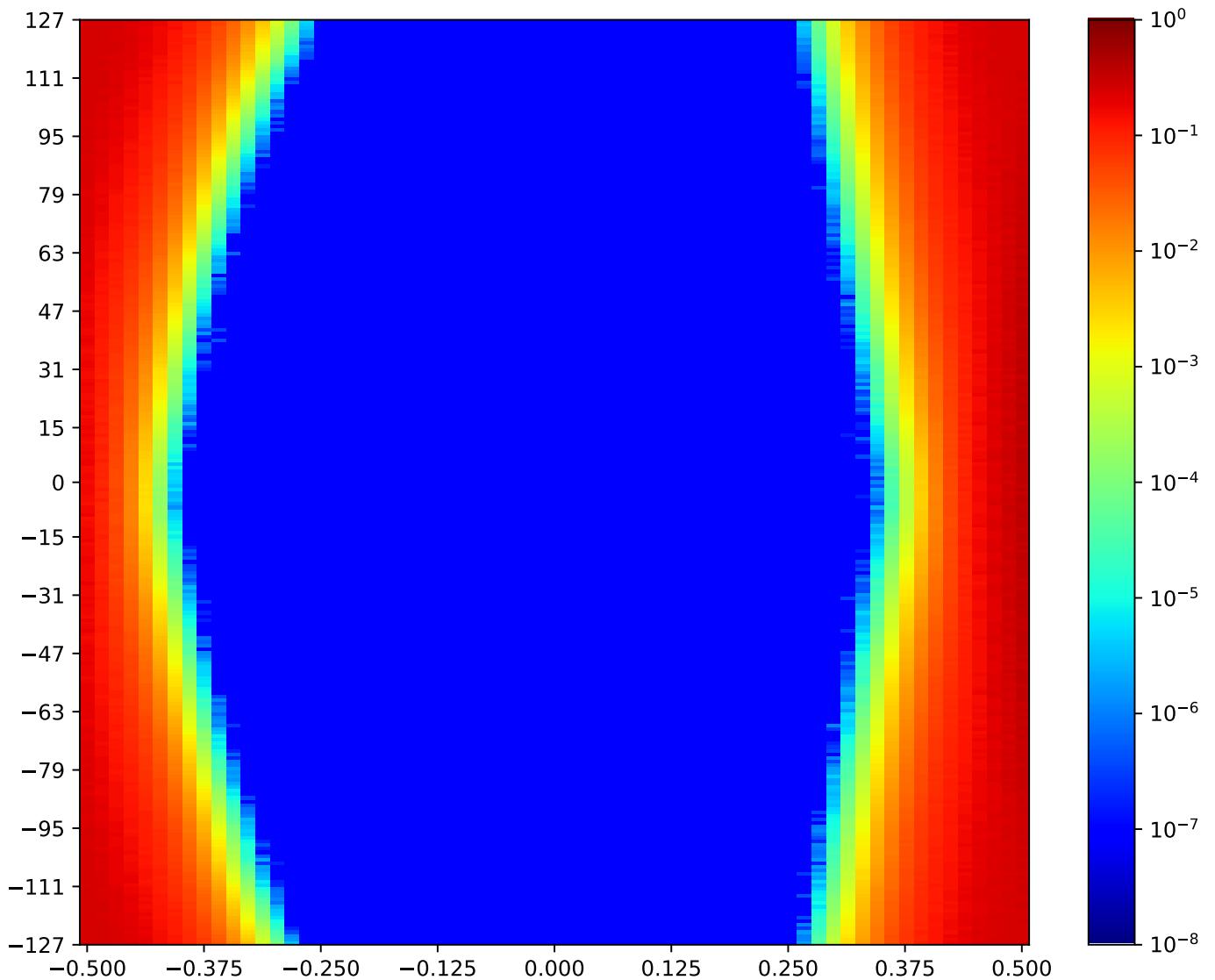


Figure 1.106: MSP\_C\_FPGA-IC39-07-IC15-07-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.9 MSP\_C\_FPGA-IC39-08-IC15-08-TRP\_FPGA

Table 1.98: MSP\_C\_FPGA-IC39-08-IC15-08-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:44:49		2018-Jan-24 04:45:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10358	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

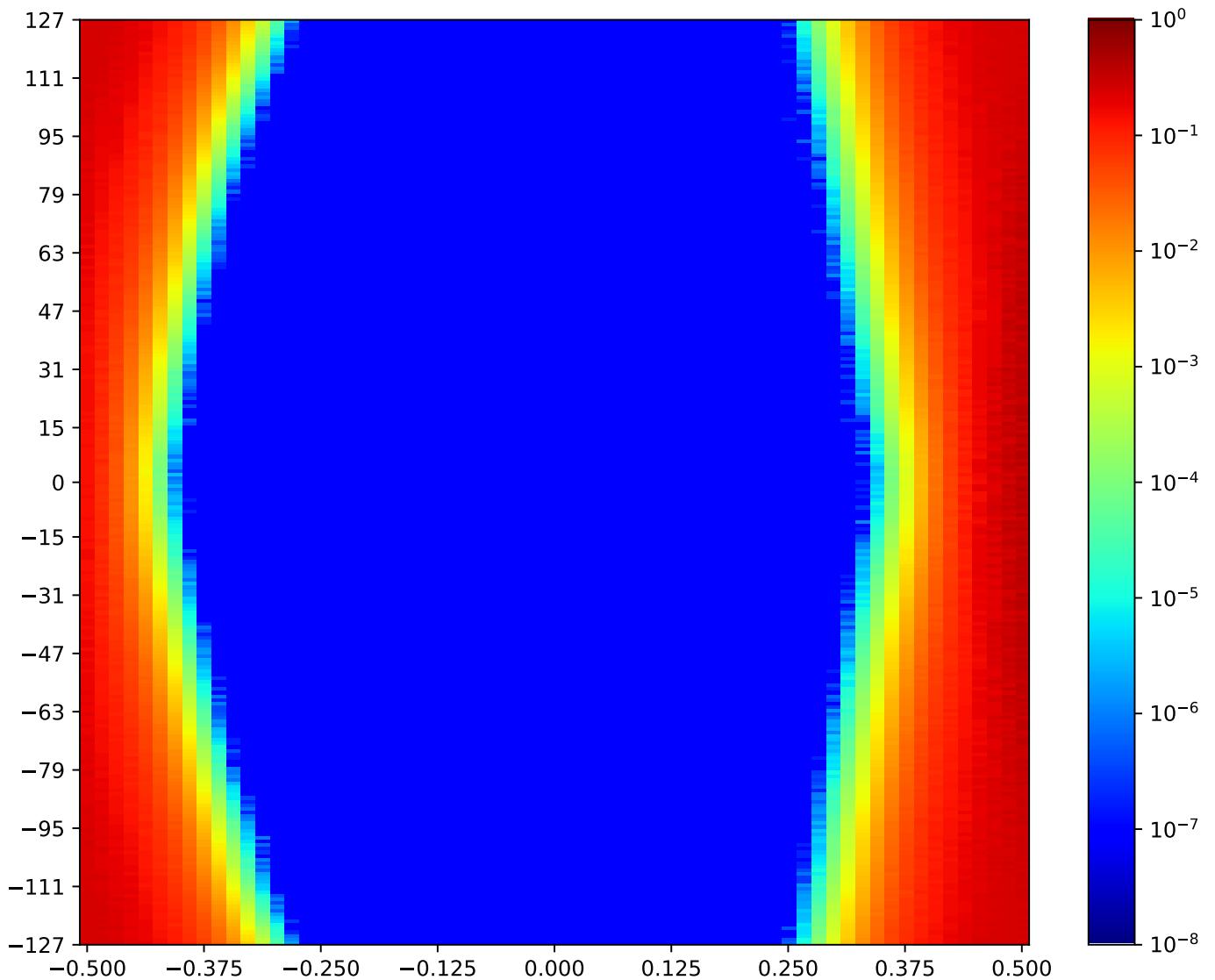


Figure 1.107: MSP\_C\_FPGA-IC39-08-IC15-08-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.10 MSP\_C\_FPGA-IC39-09-IC15-09-TRP\_FPGA

Table 1.99: MSP\_C\_FPGA-IC39-09-IC15-09-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:45:26		2018-Jan-24 04:46:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10570	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

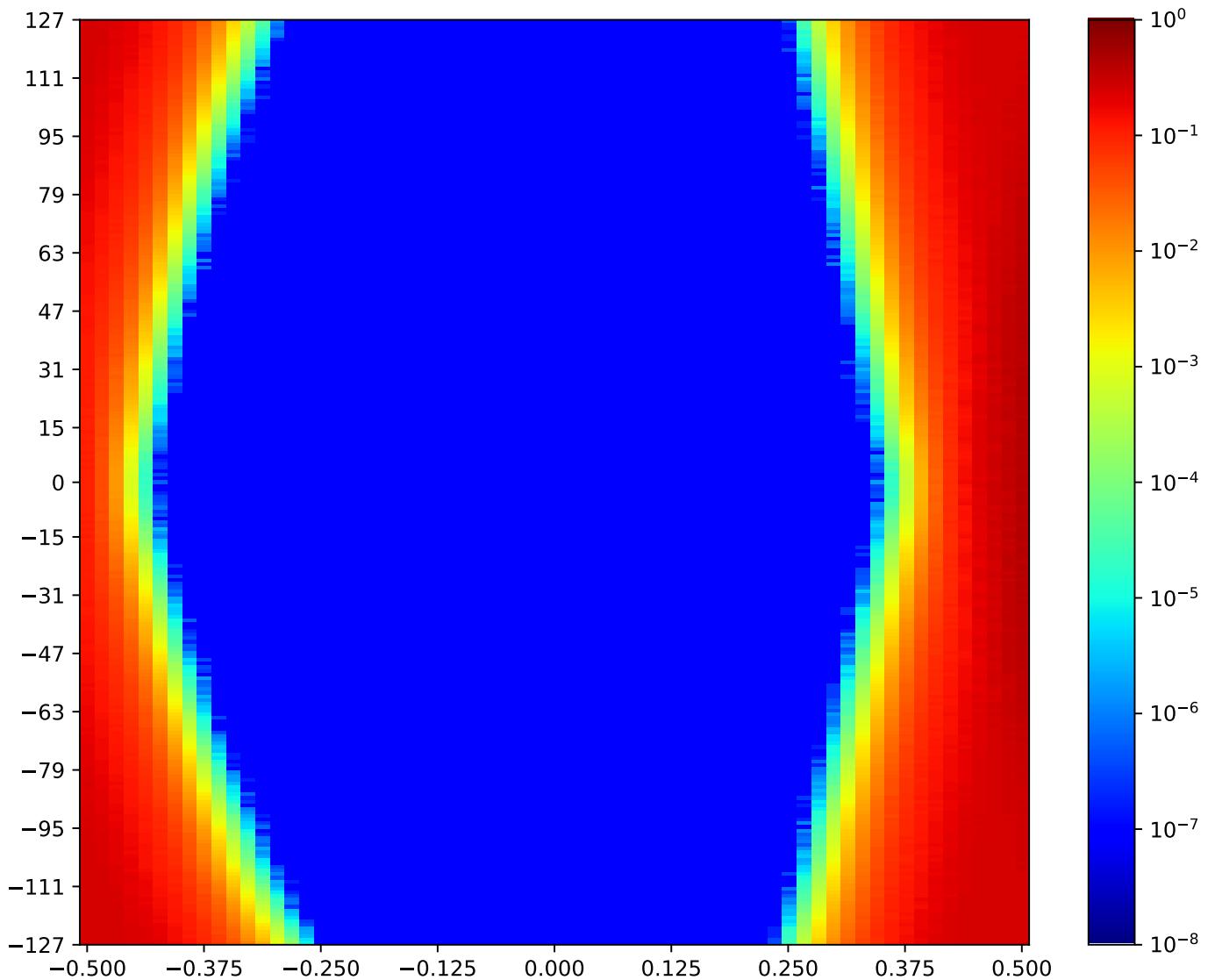


Figure 1.108: MSP\_C\_FPGA-IC39-09-IC15-09-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.11 MSP\_C\_FPGA-IC39-10-IC15-10-TRP\_FPGA

Table 1.100: MSP\_C\_FPGA-IC39-10-IC15-10-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:46:02		2018-Jan-24 04:46:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10483	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

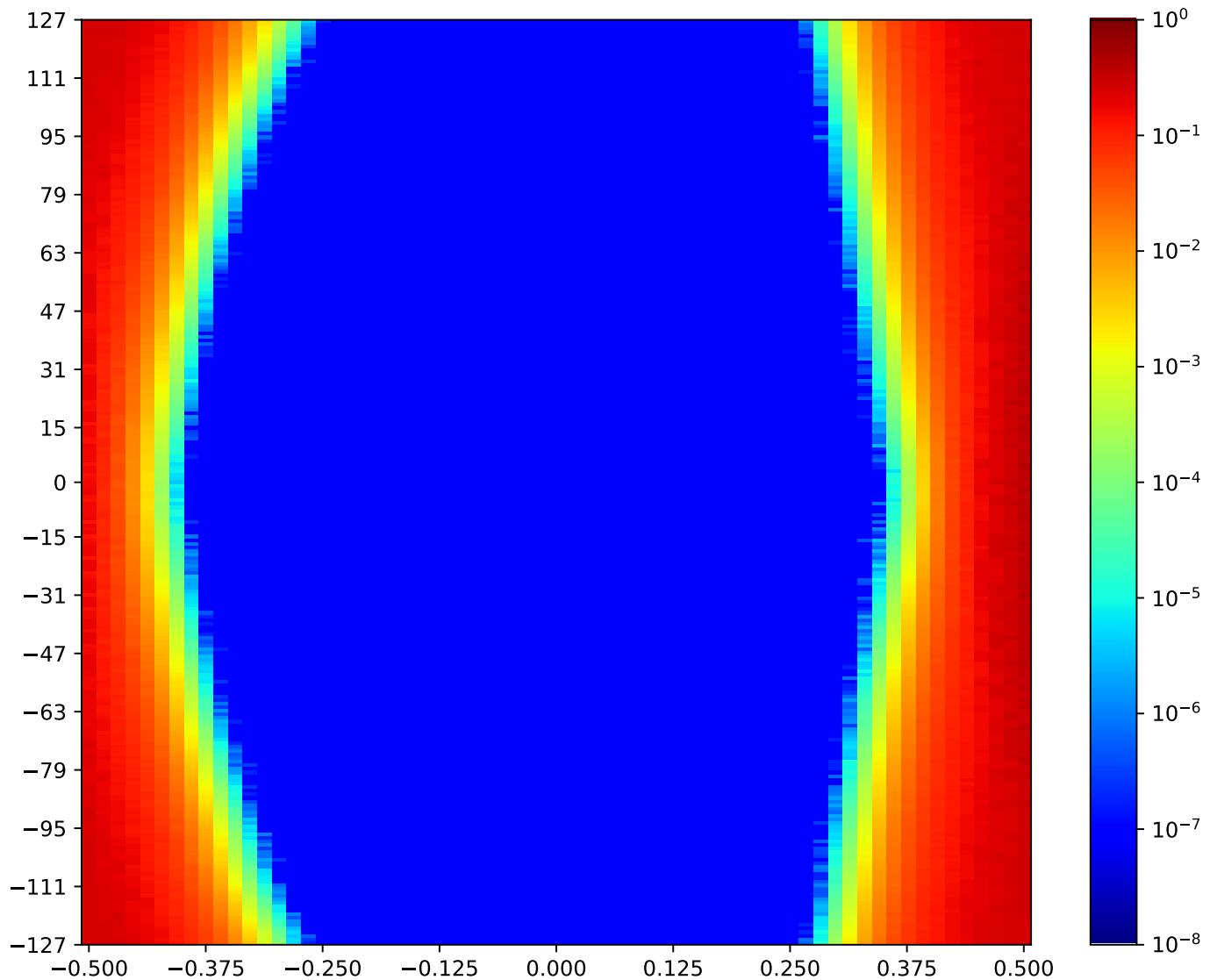


Figure 1.109: MSP\_C\_FPGA-IC39-10-IC15-10-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.12 MSP\_C\_FPGA-IC39-11-IC15-11-TRP\_FPGA

Table 1.101: MSP\_C\_FPGA-IC39-11-IC15-11-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:46:39		2018-Jan-24 04:47:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10606	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

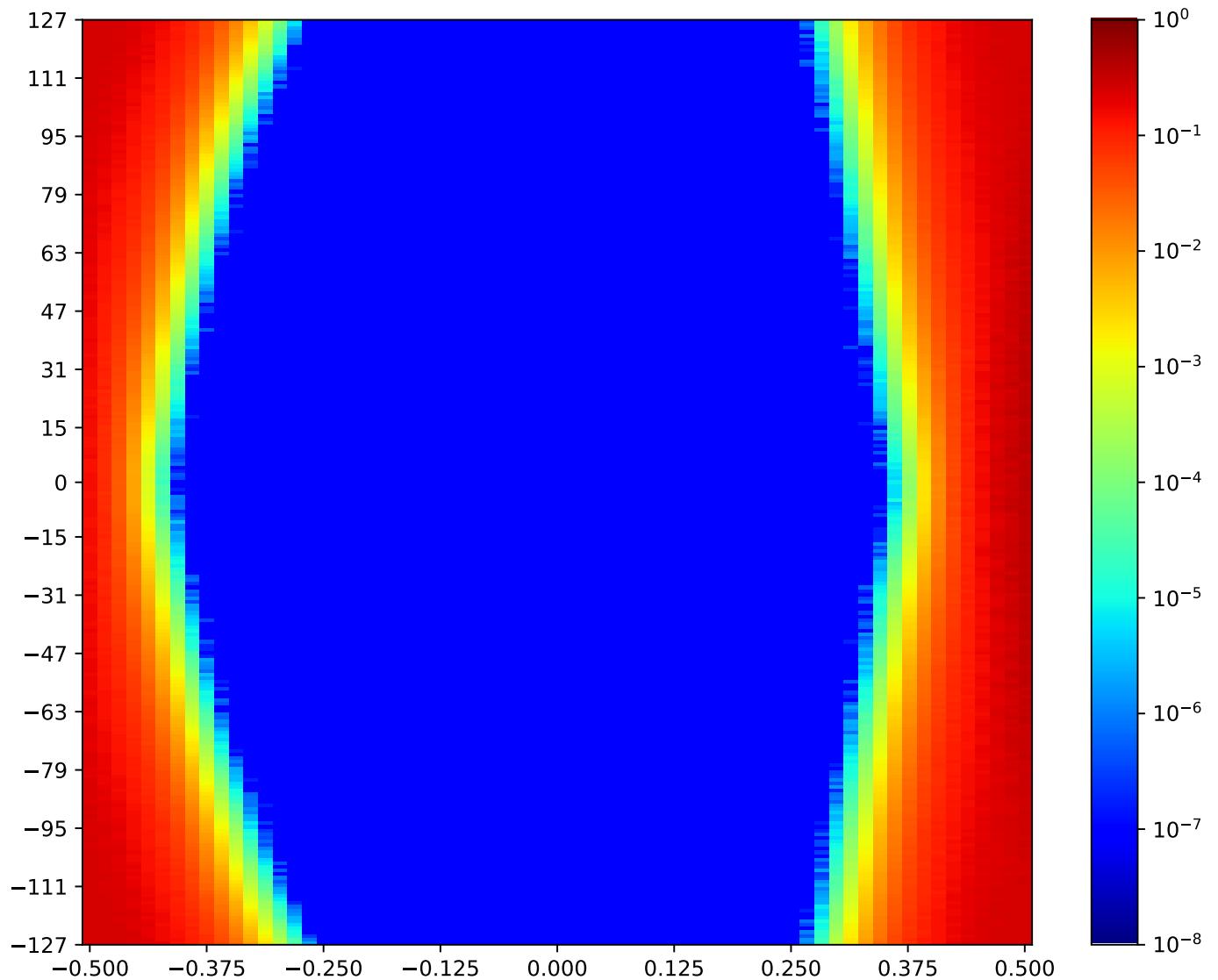


Figure 1.110: MSP\_C\_FPGA-IC39-11-IC15-11-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.13 MSP\_C\_FPGA-IC39-12-IC15-12-TRP\_FPGA

Table 1.102: MSP\_C\_FPGA-IC39-12-IC15-12-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:47:15		2018-Jan-24 04:47:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10889	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

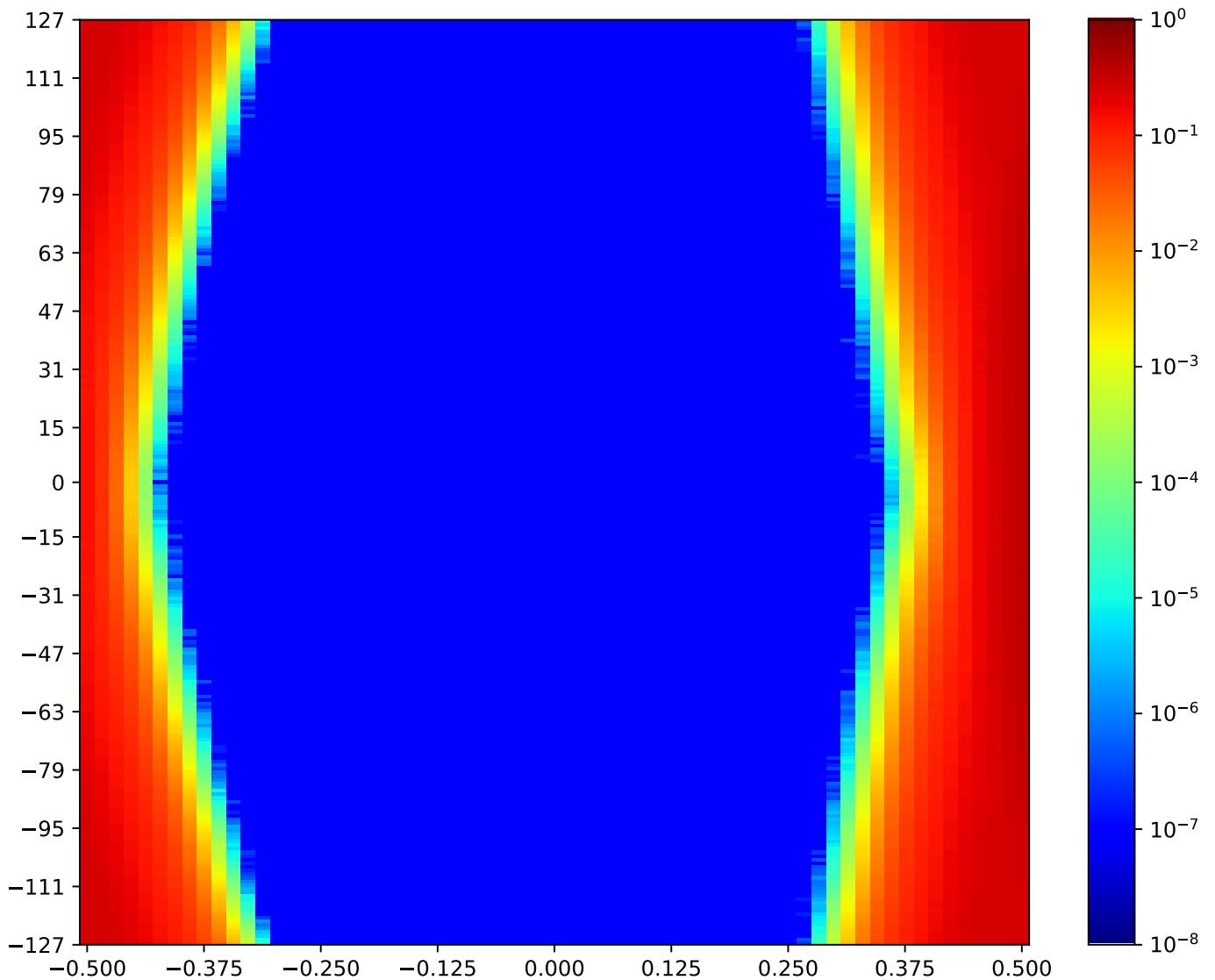


Figure 1.111: MSP\_C\_FPGA-IC39-12-IC15-12-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.14 MSP\_C\_FPGA-IC39-13-IC15-13-TRP\_FPGA

Table 1.103: MSP\_C\_FPGA-IC39-13-IC15-13-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:47:52		2018-Jan-24 04:48:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11580	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

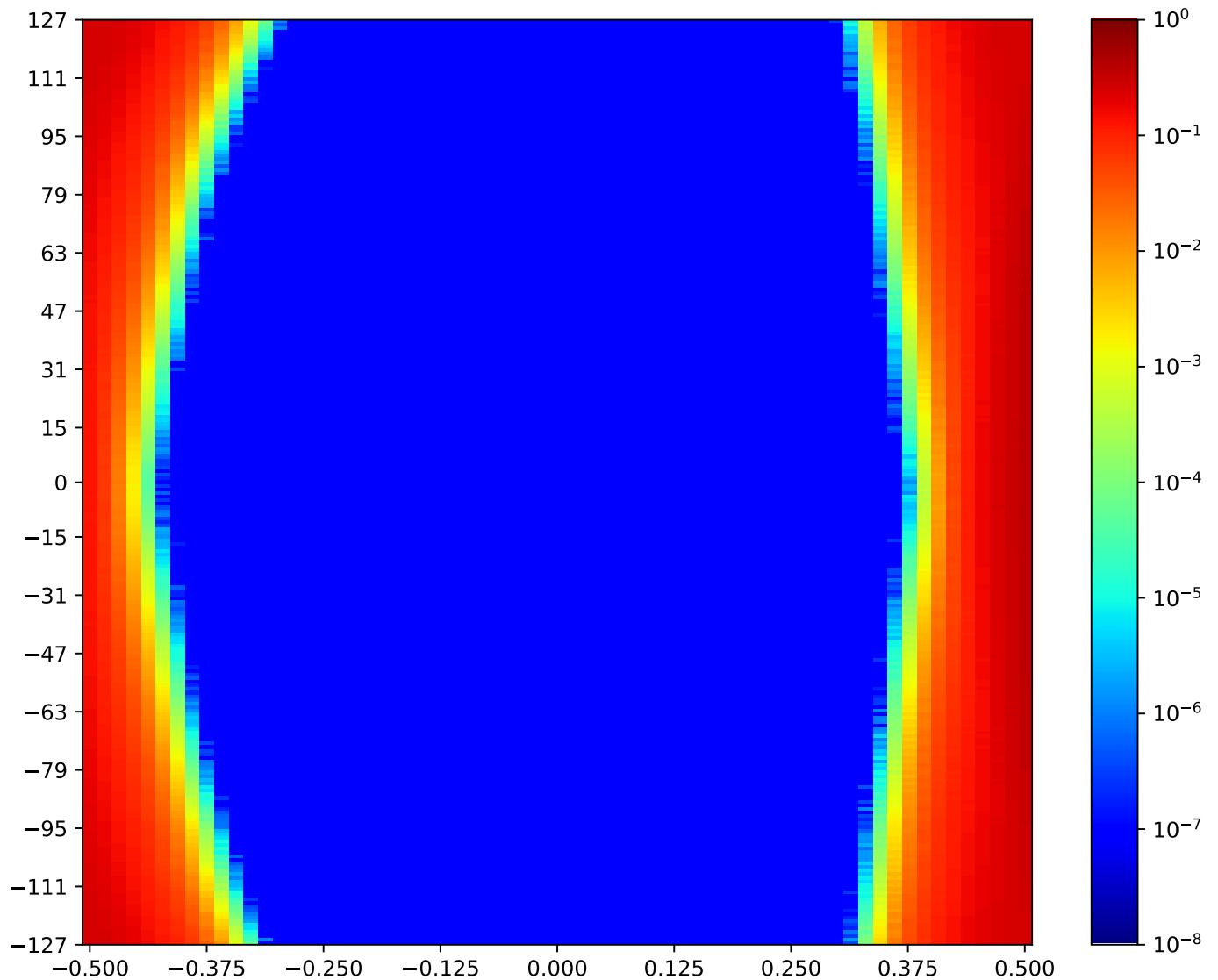


Figure 1.112: MSP\_C\_FPGA-IC39-13-IC15-13-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.15 MSP\_C\_FPGA-IC39-14-IC15-14-TRP\_FPGA

Table 1.104: MSP\_C\_FPGA-IC39-14-IC15-14-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:48:28		2018-Jan-24 04:49:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11183	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

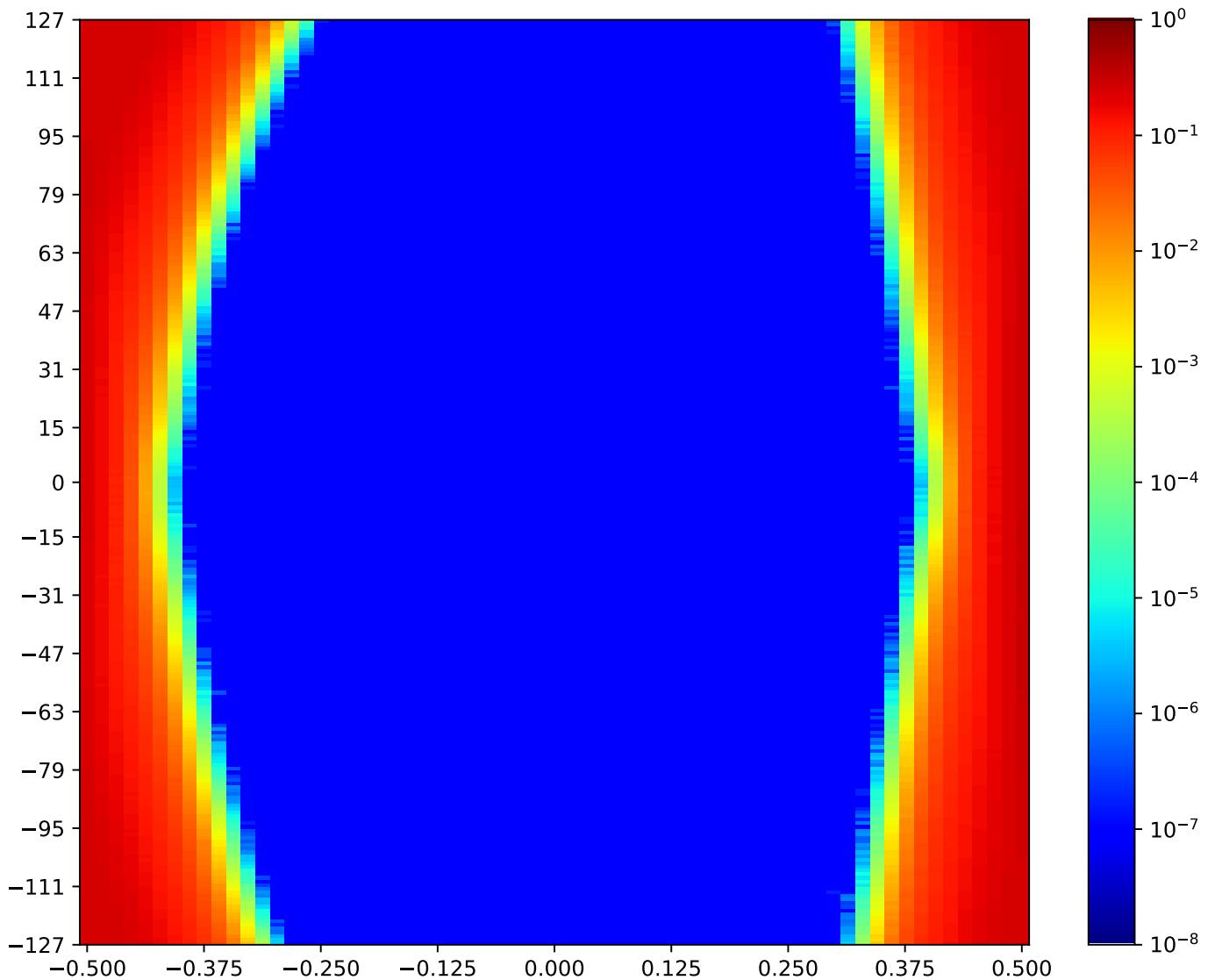


Figure 1.113: MSP\_C\_FPGA-IC39-14-IC15-14-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.16 MSP\_C\_FPGA-IC39-15-IC15-15-TRP\_FPGA

Table 1.105: MSP\_C\_FPGA-IC39-15-IC15-15-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:49:04		2018-Jan-24 04:49:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11184	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

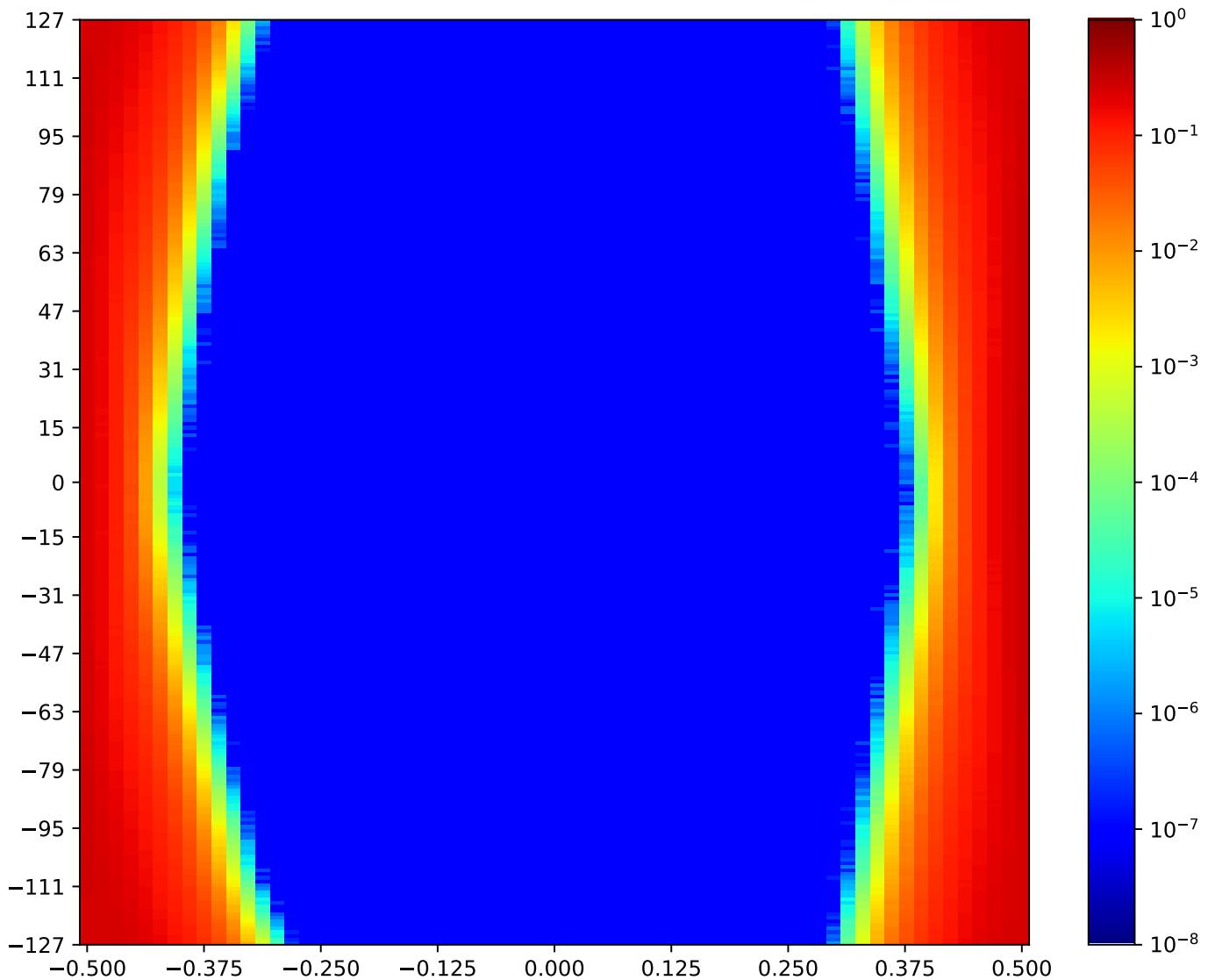


Figure 1.114: MSP\_C\_FPGA-IC39-15-IC15-15-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.17 MSP\_C\_FPGA-IC39-16-IC15-16-TRP\_FPGA

Table 1.106: MSP\_C\_FPGA-IC39-16-IC15-16-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:49:41		2018-Jan-24 04:50:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10134	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

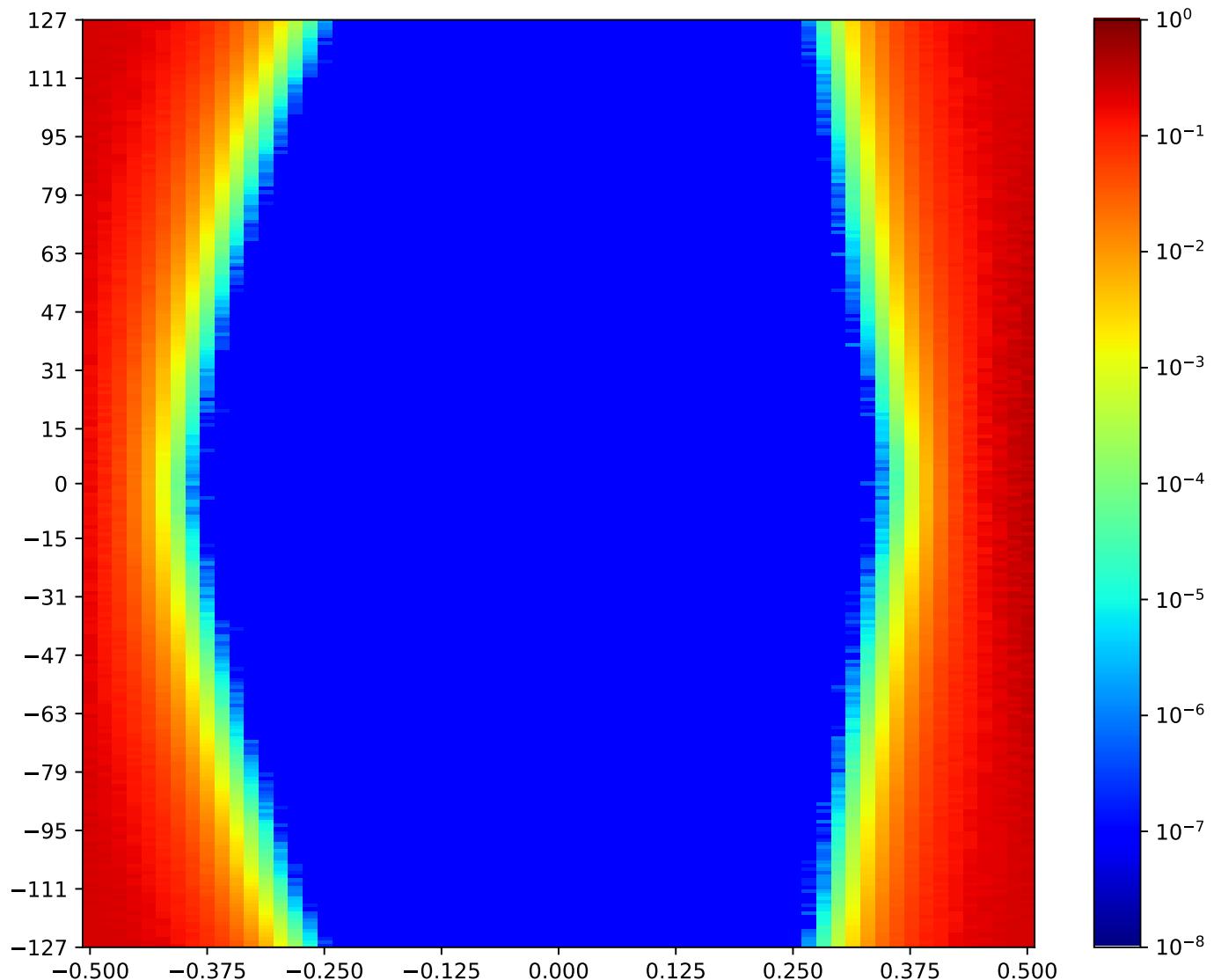


Figure 1.115: MSP\_C\_FPGA-IC39-16-IC15-16-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.18 MSP\_C\_FPGA-IC39-17-IC15-17-TRP\_FPGA

Table 1.107: MSP\_C\_FPGA-IC39-17-IC15-17-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:50:17		2018-Jan-24 04:50:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10236	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

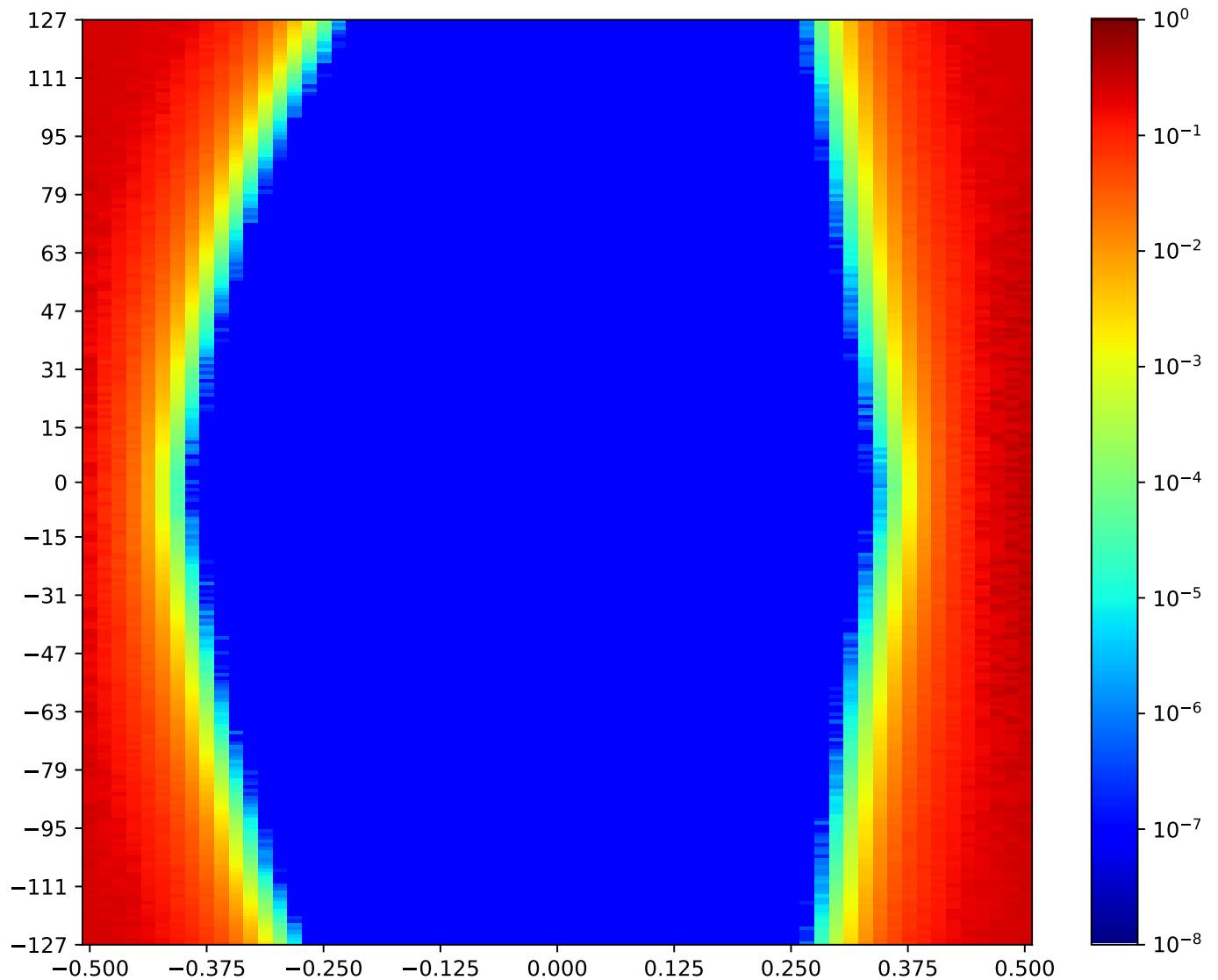


Figure 1.116: MSP\_C\_FPGA-IC39-17-IC15-17-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.19 MSP\_C\_FPGA-IC39-18-IC15-18-TRP\_FPGA

Table 1.108: MSP\_C\_FPGA-IC39-18-IC15-18-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:50:53		2018-Jan-24 04:51:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10543	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

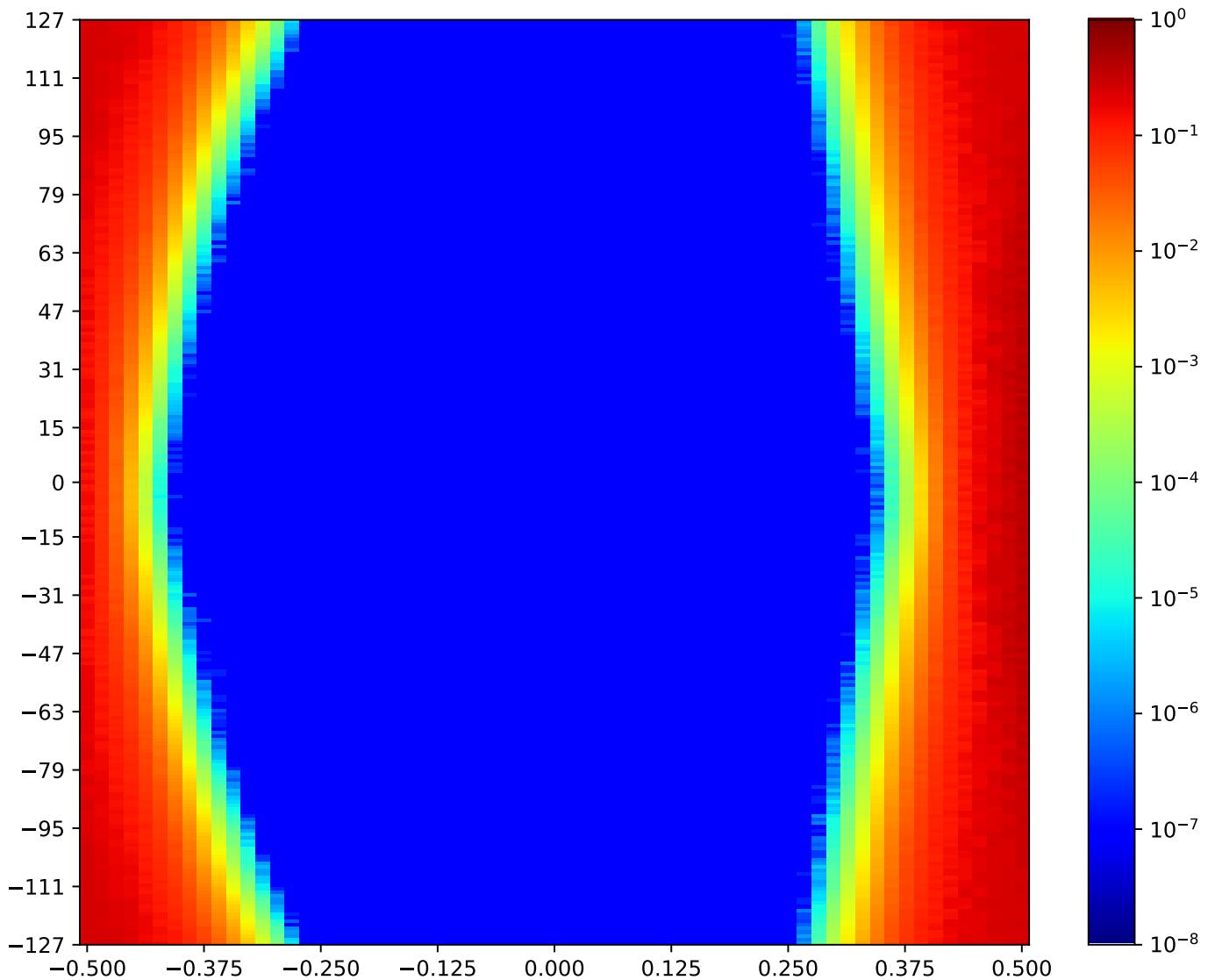


Figure 1.117: MSP\_C\_FPGA-IC39-18-IC15-18-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.20 MSP\_C\_FPGA-IC39-19-IC15-19-TRP\_FPGA

Table 1.109: MSP\_C\_FPGA-IC39-19-IC15-19-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:51:29		2018-Jan-24 04:52:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10508	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

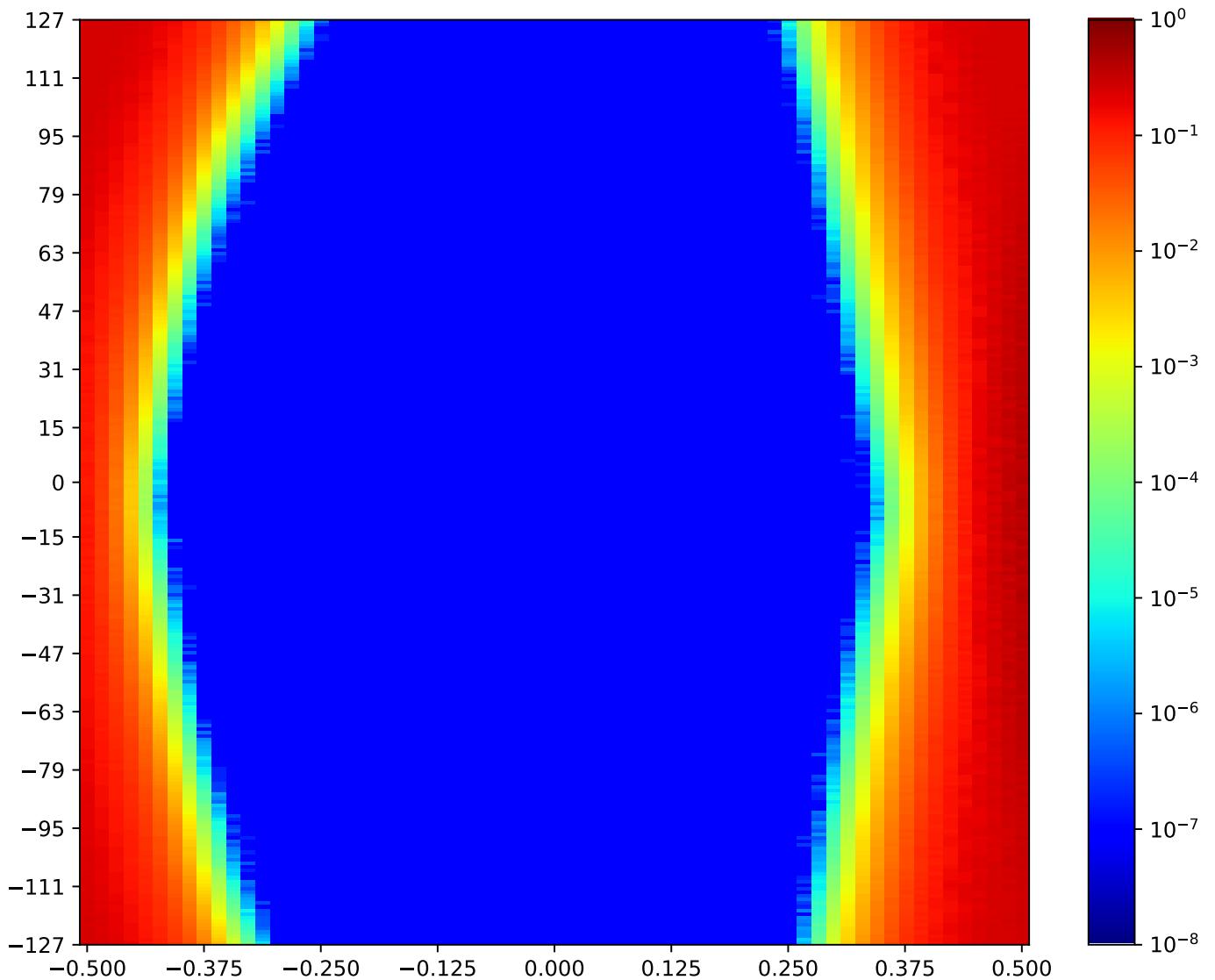


Figure 1.118: MSP\_C\_FPGA-IC39-19-IC15-19-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.21 MSP\_C\_FPGA-IC39-20-IC15-20-TRP\_FPGA

Table 1.110: MSP\_C\_FPGA-IC39-20-IC15-20-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:52:06		2018-Jan-24 04:52:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10753	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

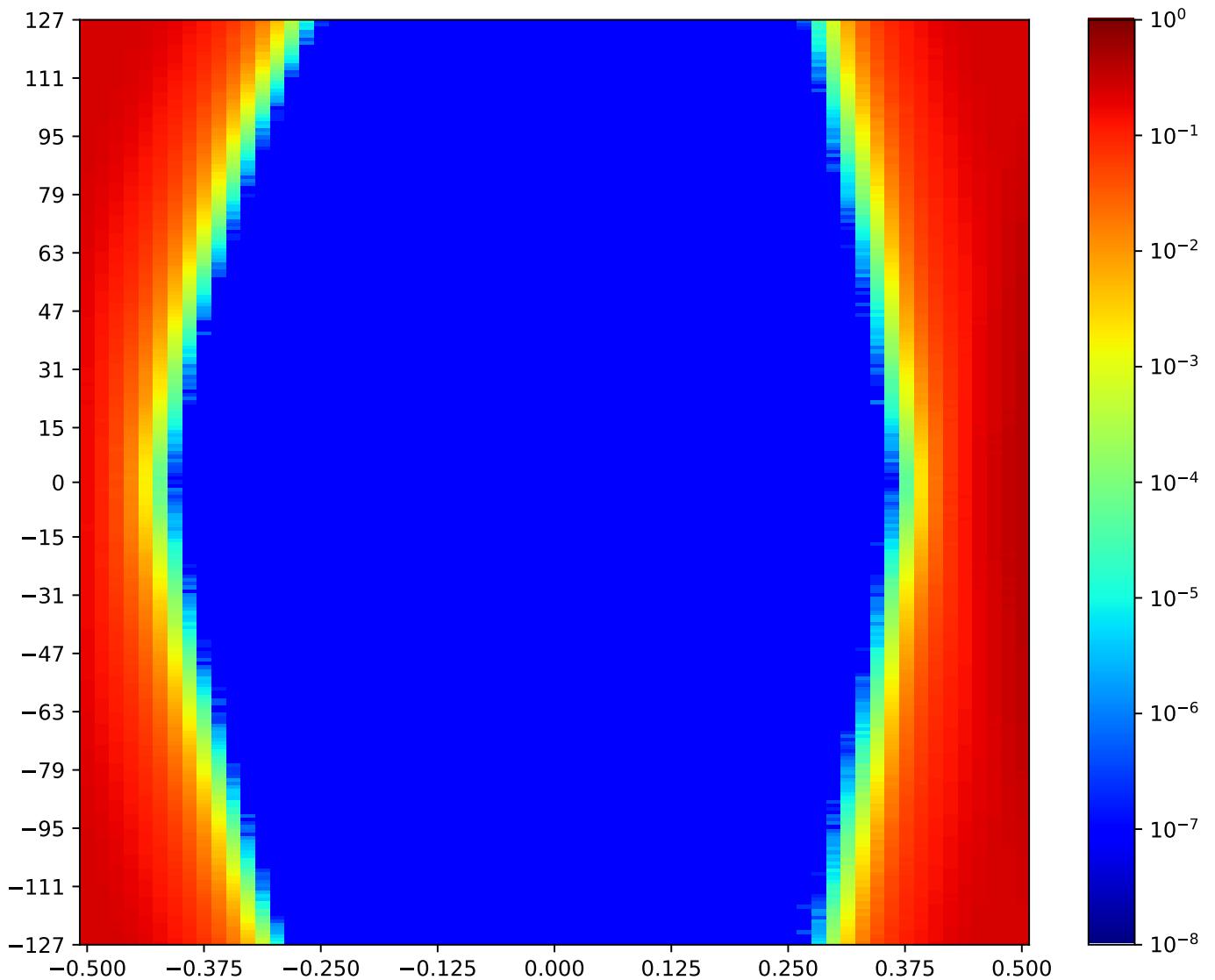


Figure 1.119: MSP\_C\_FPGA-IC39-20-IC15-20-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.22 MSP\_C\_FPGA-IC39-21-IC15-21-TRP\_FPGA

Table 1.111: MSP\_C\_FPGA-IC39-21-IC15-21-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:52:42		2018-Jan-24 04:53:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10797	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

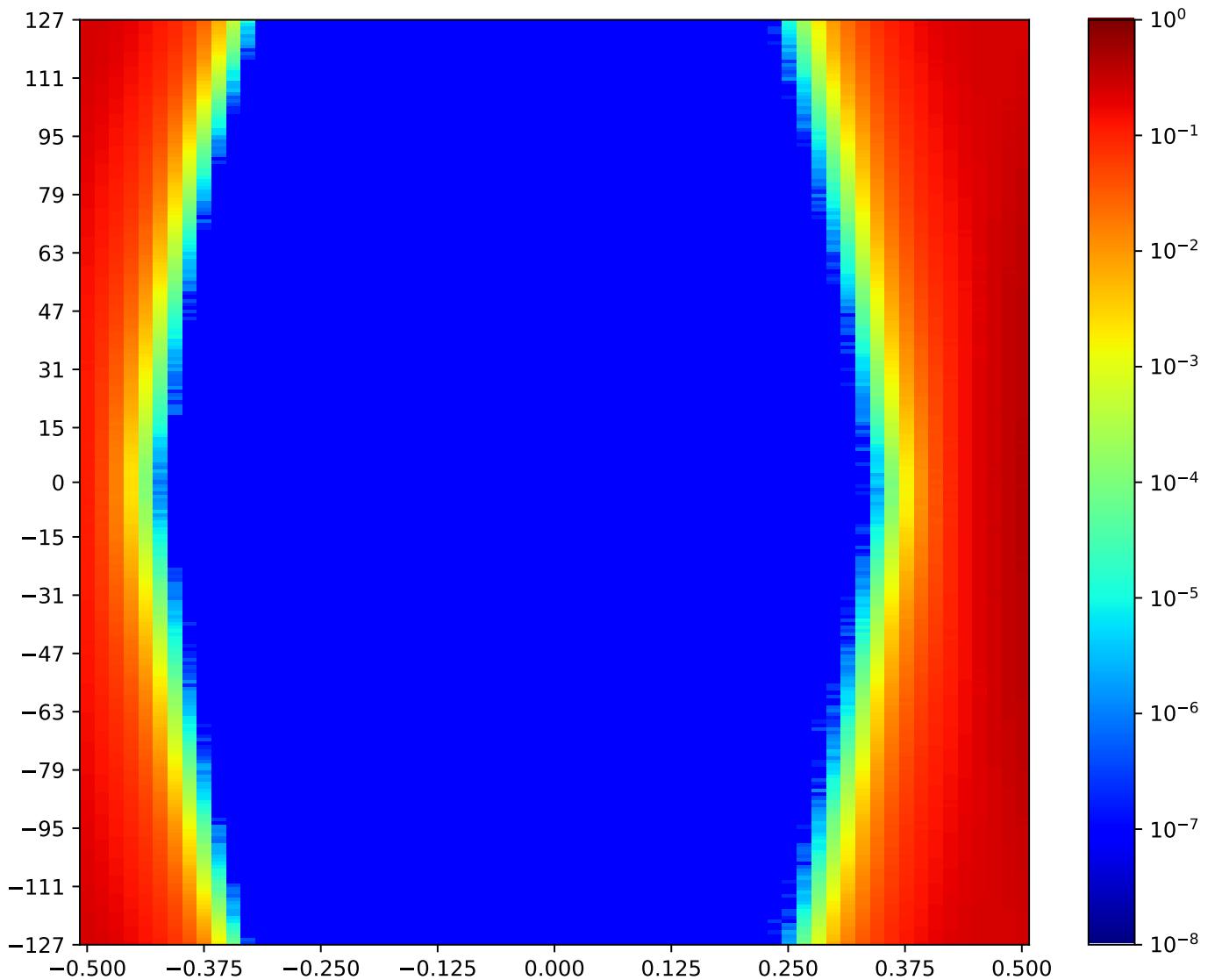


Figure 1.120: MSP\_C\_FPGA-IC39-21-IC15-21-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.23 MSP\_C\_FPGA-IC39-22-IC15-22-TRP\_FPGA

Table 1.112: MSP\_C\_FPGA-IC39-22-IC15-22-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:53:19		2018-Jan-24 04:53:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10526	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

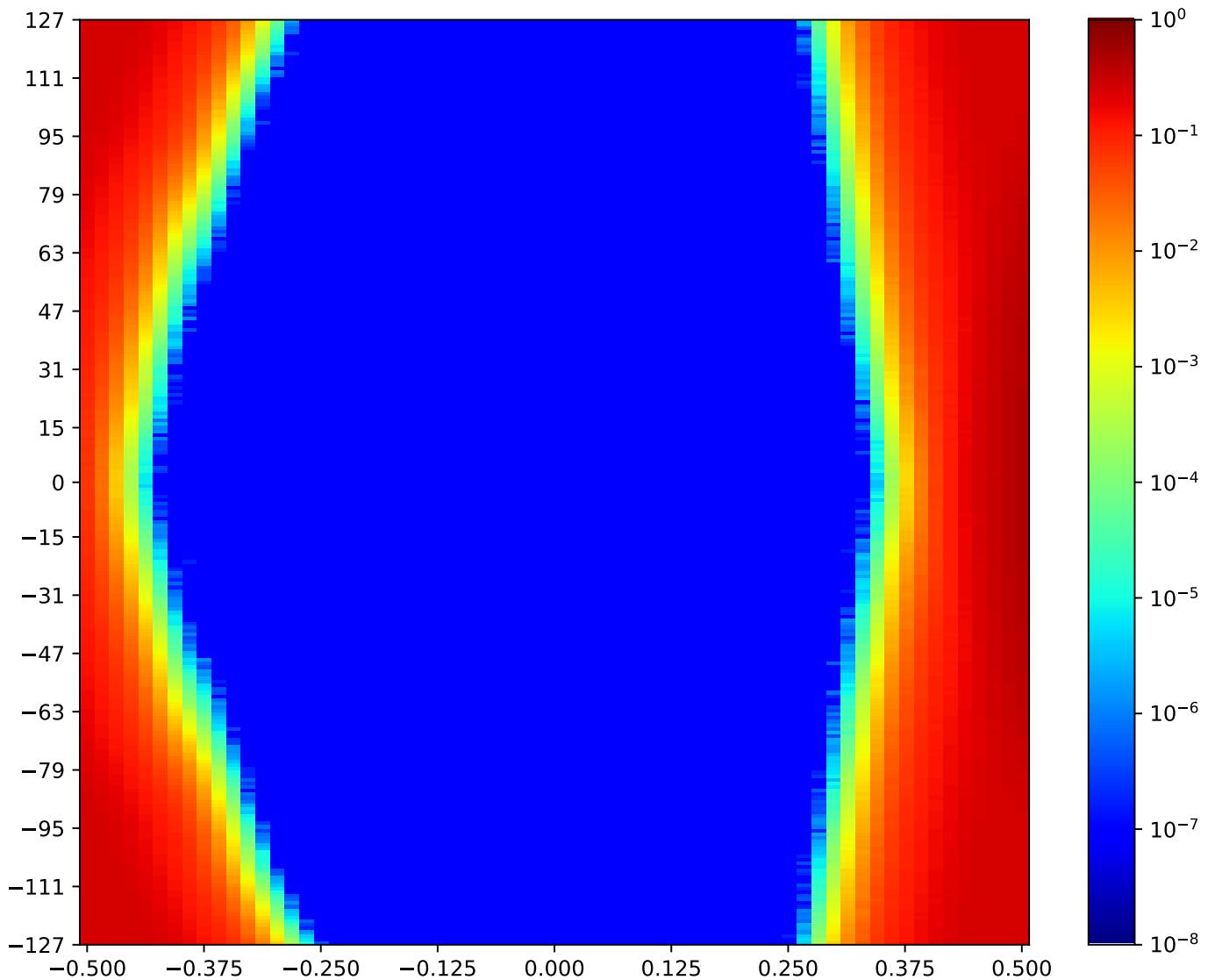


Figure 1.121: MSP\_C\_FPGA-IC39-22-IC15-22-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.24 MSP\_C\_FPGA-IC39-23-IC15-23-TRP\_FPGA

Table 1.113: MSP\_C\_FPGA-IC39-23-IC15-23-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:53:54		2018-Jan-24 04:54:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10510	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

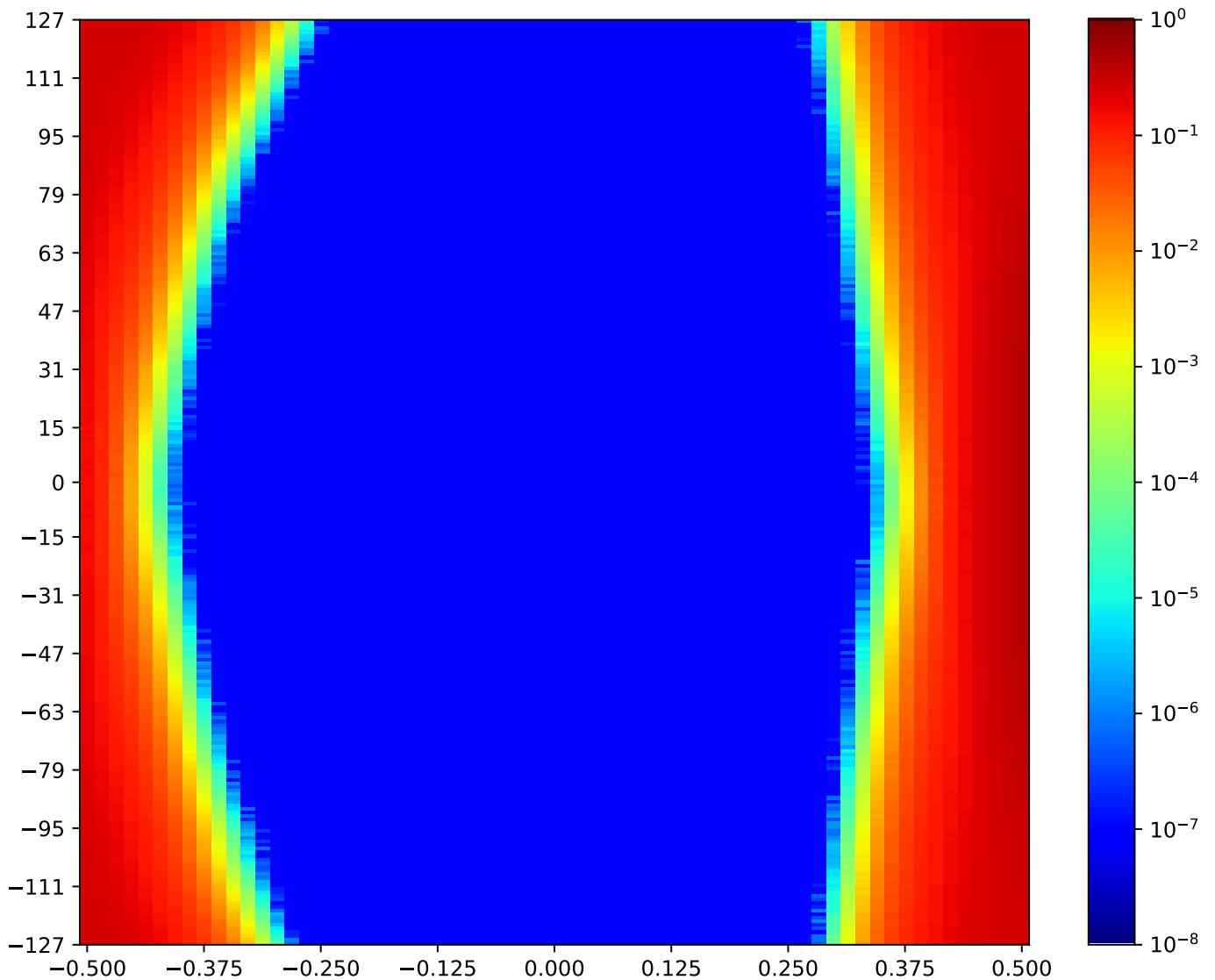


Figure 1.122: MSP\_C\_FPGA-IC39-23-IC15-23-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.25 MSP\_C\_FPGA-IC39-24-IC15-24-TRP\_FPGA

Table 1.114: MSP\_C\_FPGA-IC39-24-IC15-24-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:54:30		2018-Jan-24 04:55:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10410	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

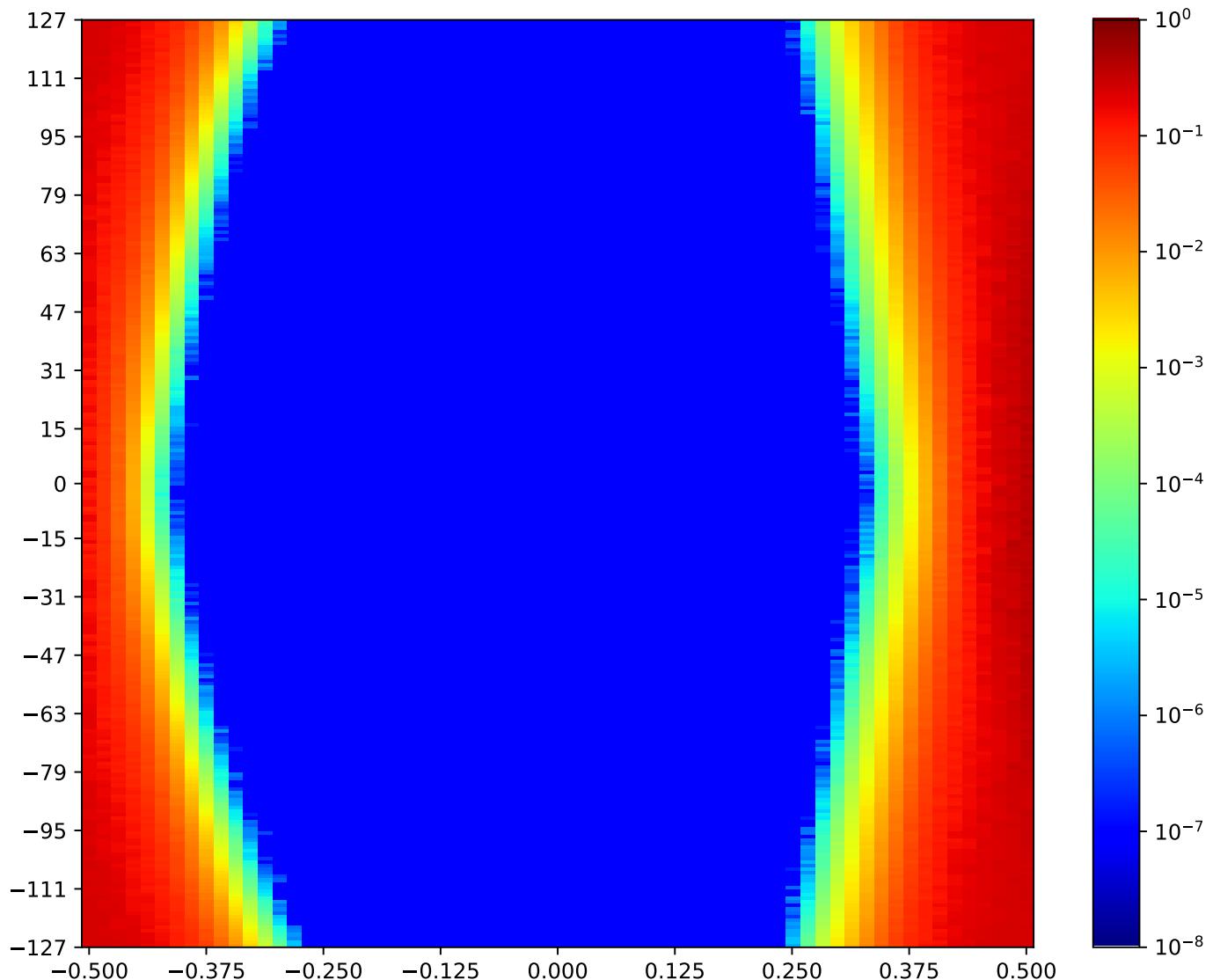


Figure 1.123: MSP\_C\_FPGA-IC39-24-IC15-24-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.26 MSP\_C\_FPGA-IC39-25-IC15-25-TRP\_FPGA

Table 1.115: MSP\_C\_FPGA-IC39-25-IC15-25-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:55:07		2018-Jan-24 04:55:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10608	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

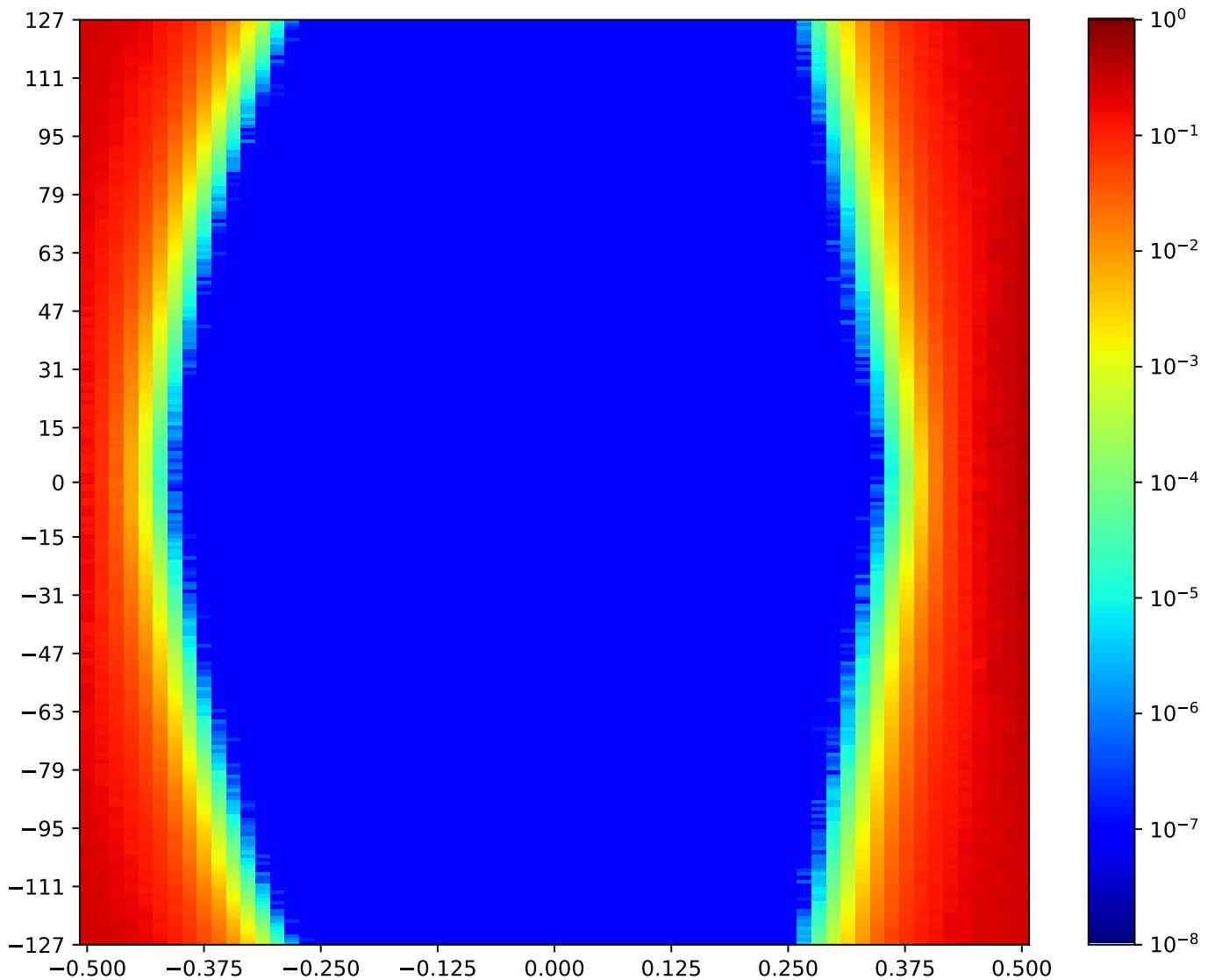


Figure 1.124: MSP\_C\_FPGA-IC39-25-IC15-25-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.27 MSP\_C\_FPGA-IC39-26-IC15-26-TRP\_FPGA

Table 1.116: MSP\_C\_FPGA-IC39-26-IC15-26-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:55:44		2018-Jan-24 04:56:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10023	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

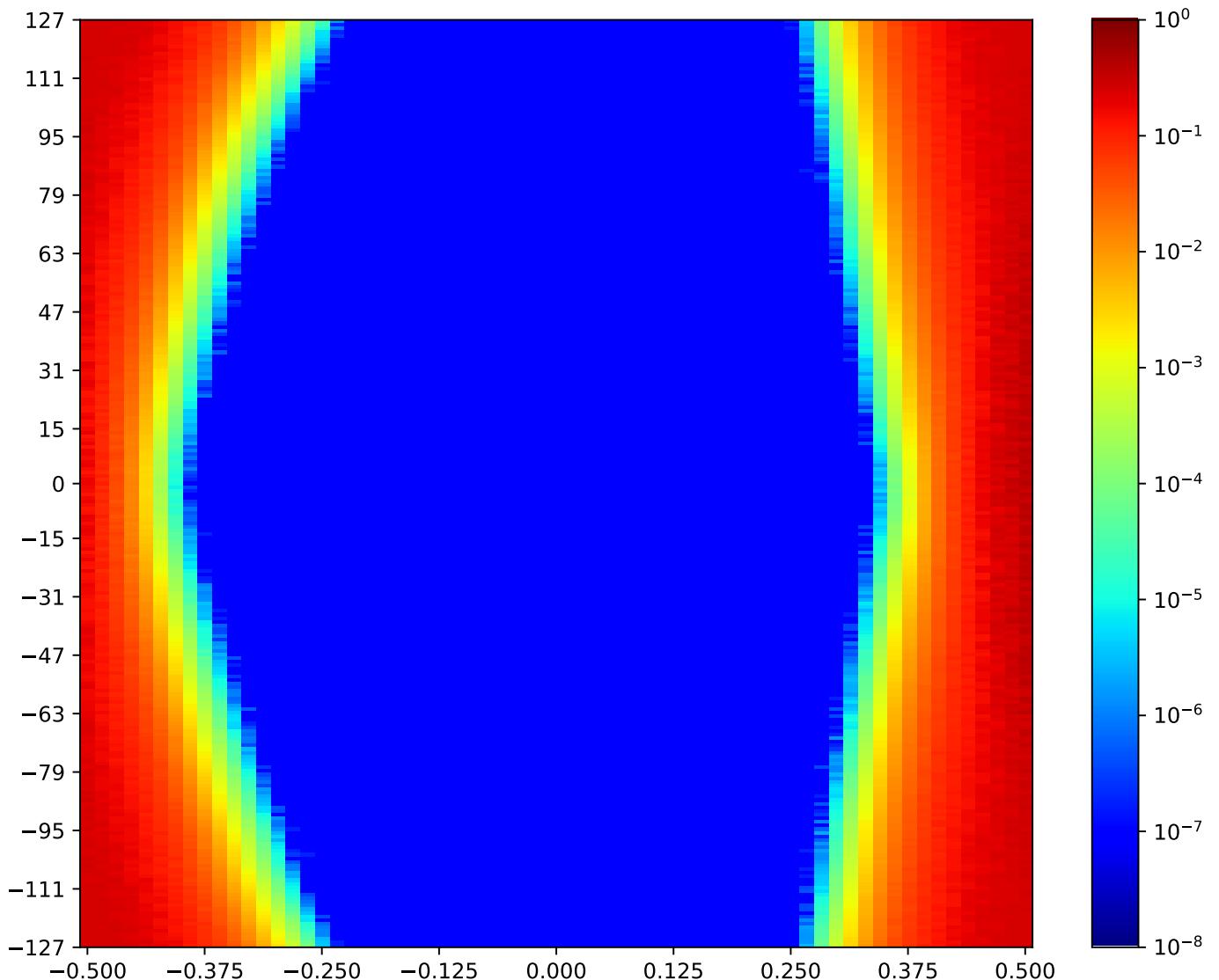


Figure 1.125: MSP\_C\_FPGA-IC39-26-IC15-26-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.9.28 MSP\_C\_FPGA-IC39-27-IC15-27-TRP\_FPGA

Table 1.117: MSP\_C\_FPGA-IC39-27-IC15-27-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:56:20		2018-Jan-24 04:56:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10306	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

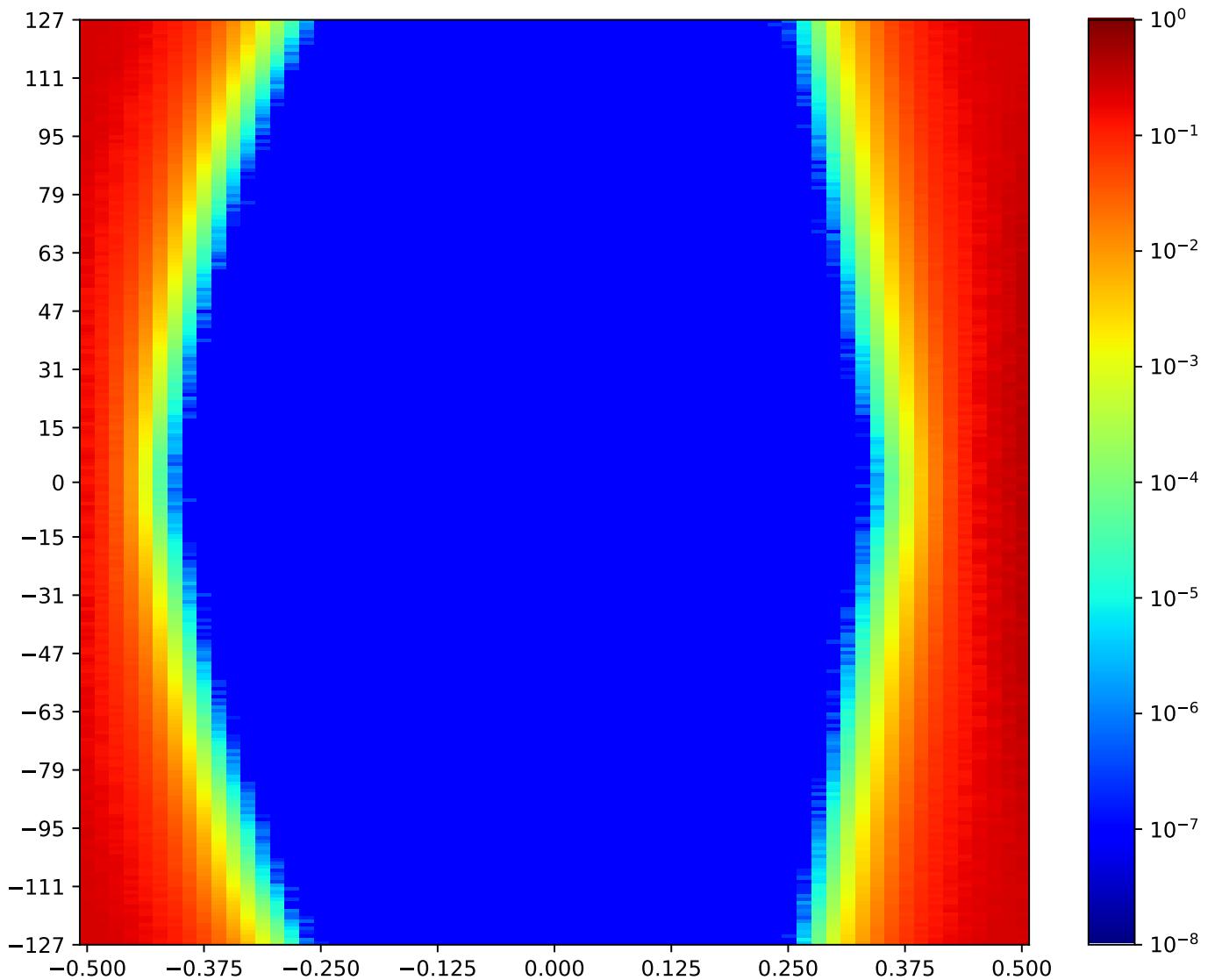


Figure 1.126: MSP\_C\_FPGA-IC39-27-IC15-27-TRP\_FPGA

Call back to summary Figure 1.98. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.10 MSP\_A TX1 MSP\_C RX18 Minipod Loopback

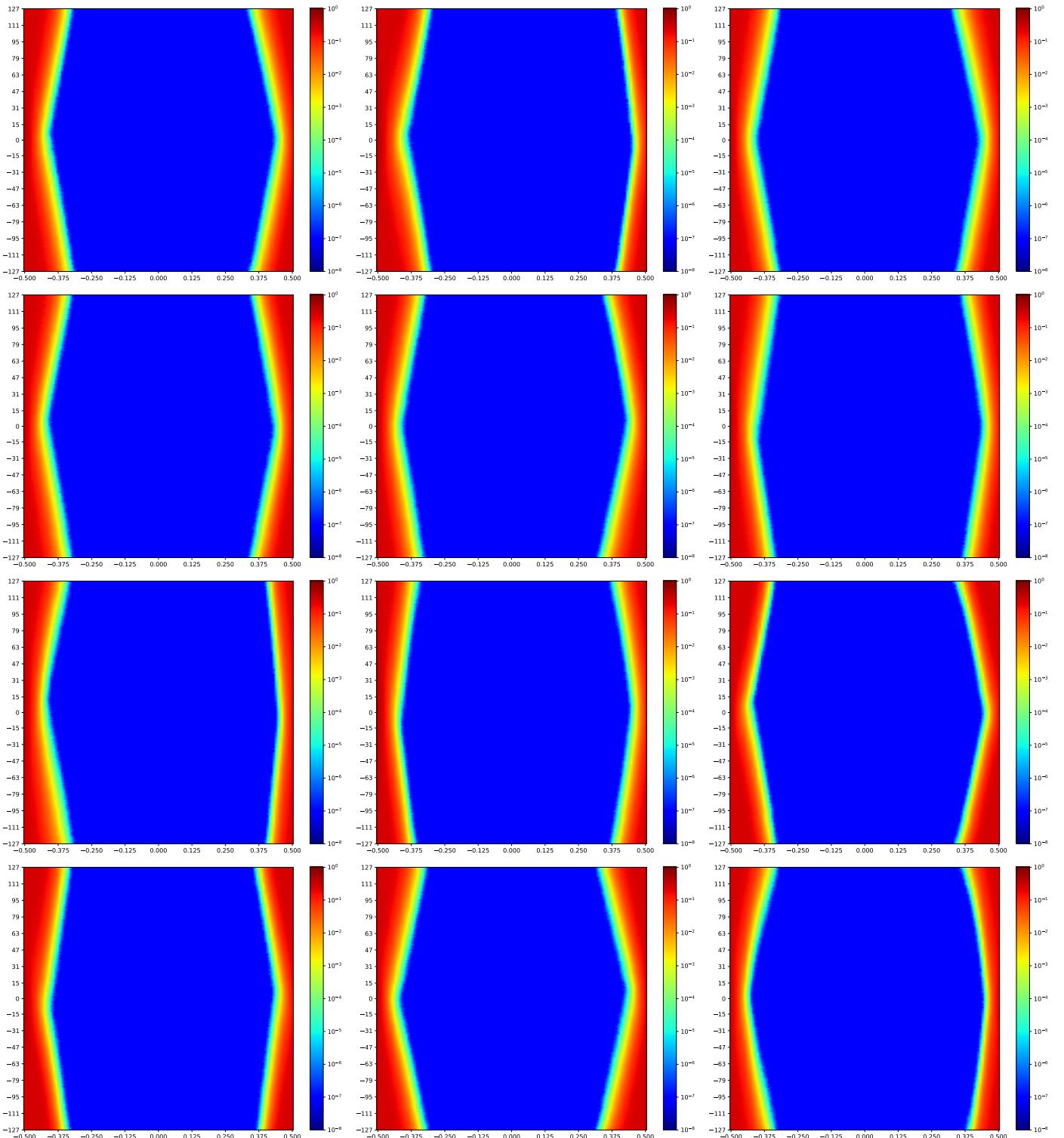


Figure 1.127: MSP\_A TX1 MSP\_C RX18 Minipod Loopback

A cross-reference to Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.140.

### 1.10.1 MSP\_A\_FPGA-TX1-00-RX18-00-MSP\_C\_FPGA

Table 1.118: MSP\_A\_FPGA-TX1-00-RX18-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:31:48		2018-Jan-24 15:32:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23780	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

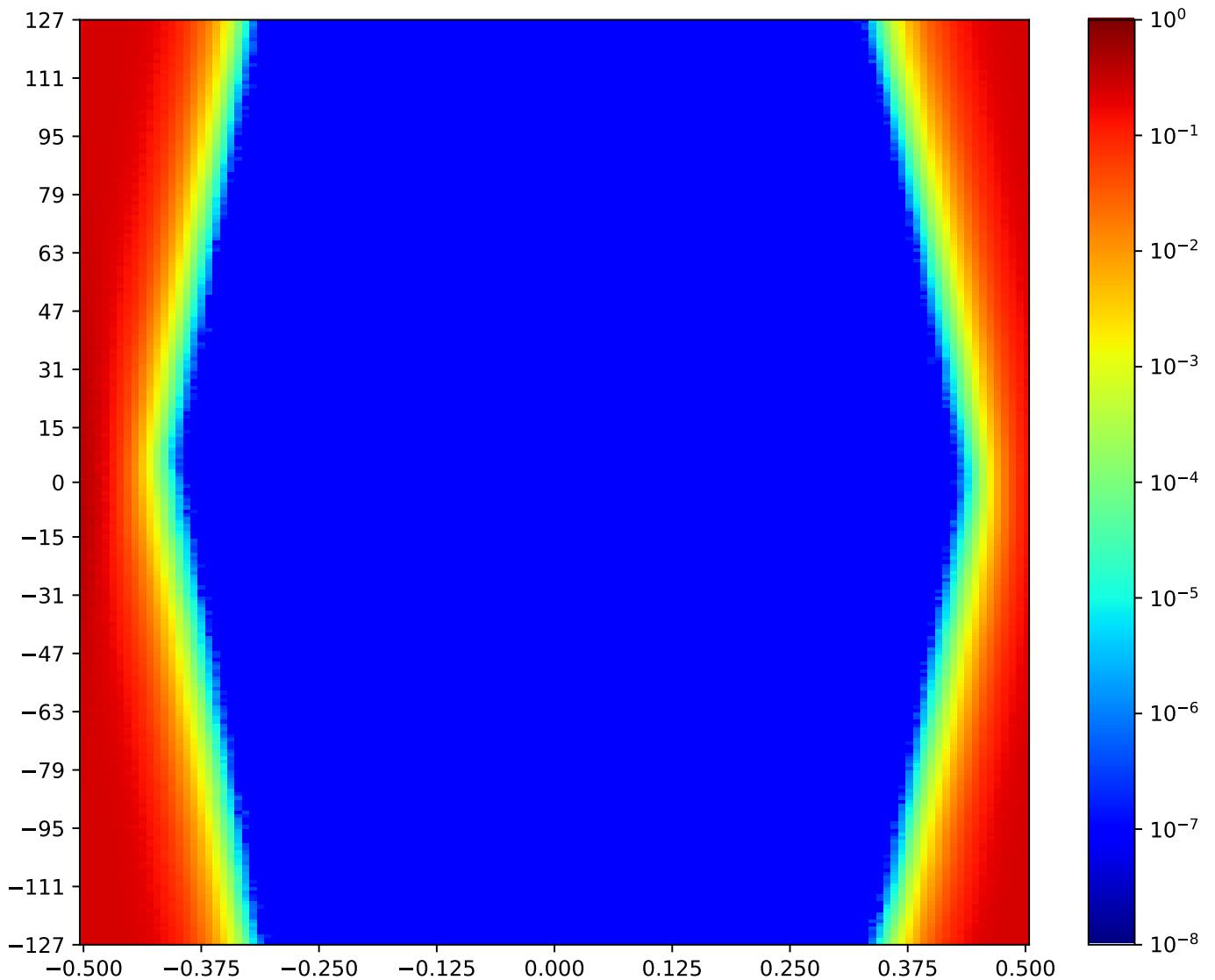


Figure 1.128: MSP\_A\_FPGA-TX1-00-RX18-00-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.2 MSP\_A\_FPGA-TX1-01-RX18-01-MSP\_C\_FPGA

Table 1.119: MSP\_A\_FPGA-TX1-01-RX18-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:34:06		2018-Jan-24 15:35:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24279	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

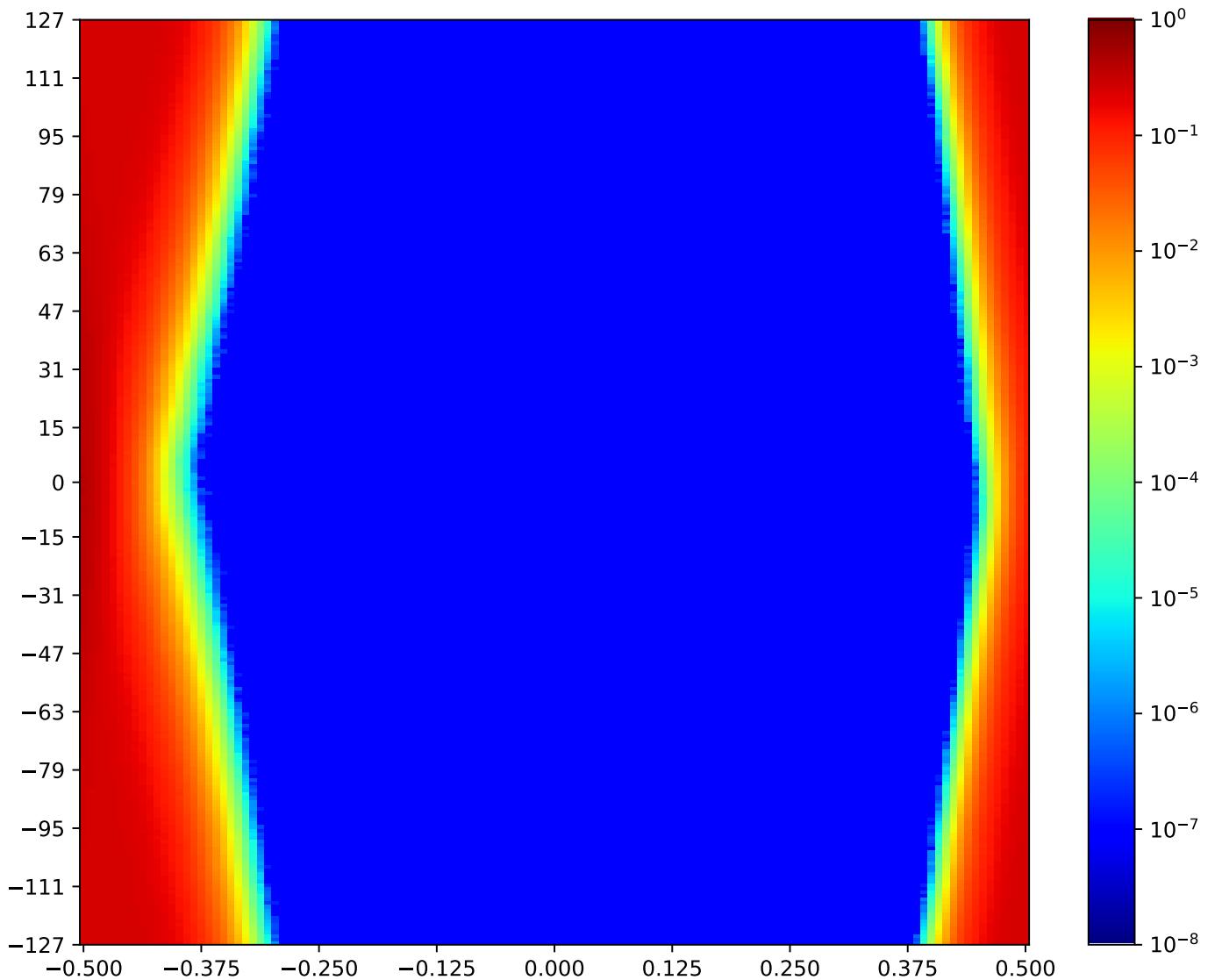


Figure 1.129: MSP\_A\_FPGA-TX1-01-RX18-01-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.3 MSP\_A\_FPGA-TX1-02-RX18-02-MSP\_C\_FPGA

Table 1.120: MSP\_A\_FPGA-TX1-02-RX18-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:35:16		2018-Jan-24 15:36:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23426	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

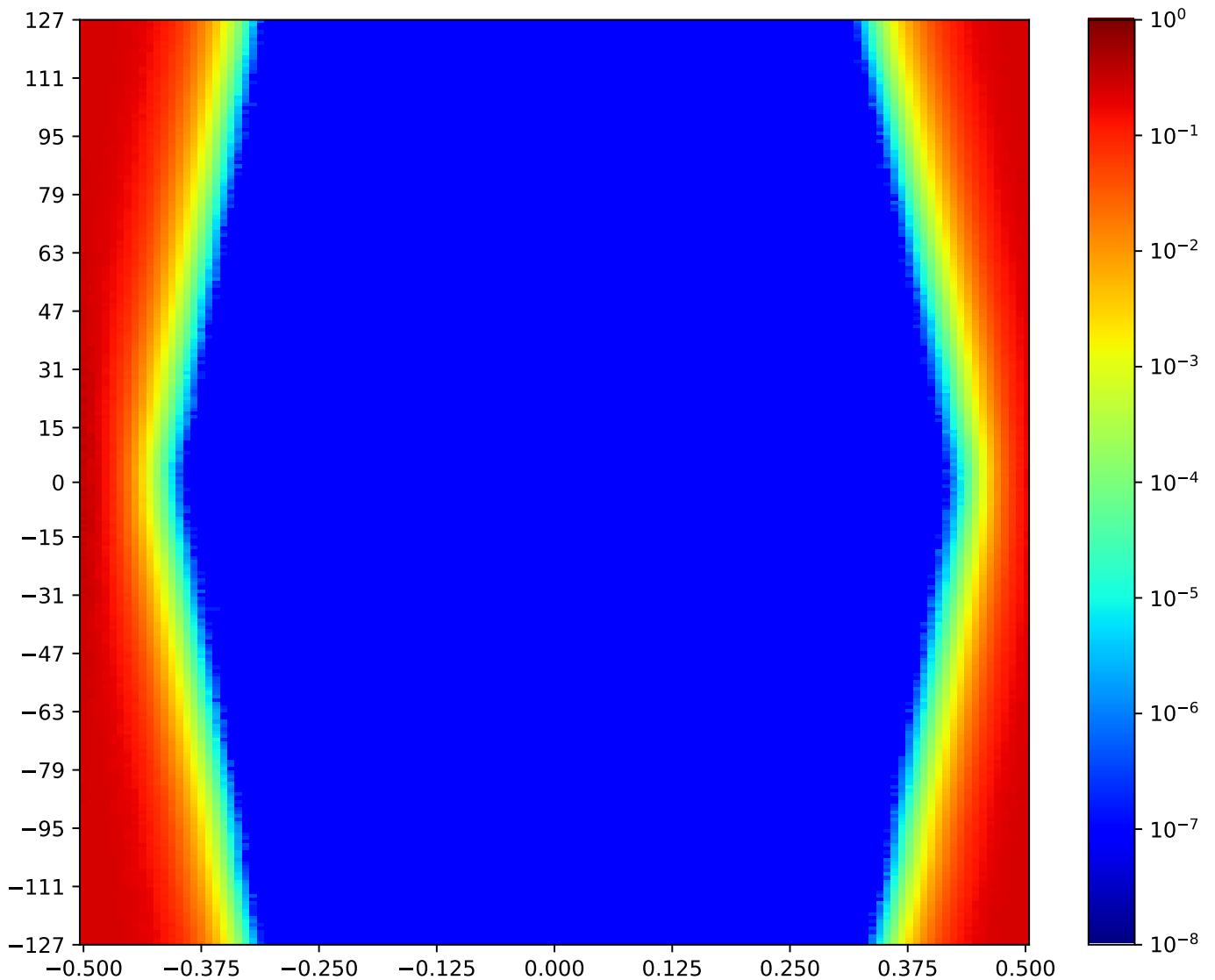


Figure 1.130: MSP\_A\_FPGA-TX1-02-RX18-02-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.10.4 MSP\_A\_FPGA-TX1-03-RX18-03-MSP\_C\_FPGA

Table 1.121: MSP\_A\_FPGA-TX1-03-RX18-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:29:30		2018-Jan-24 15:30:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23913	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

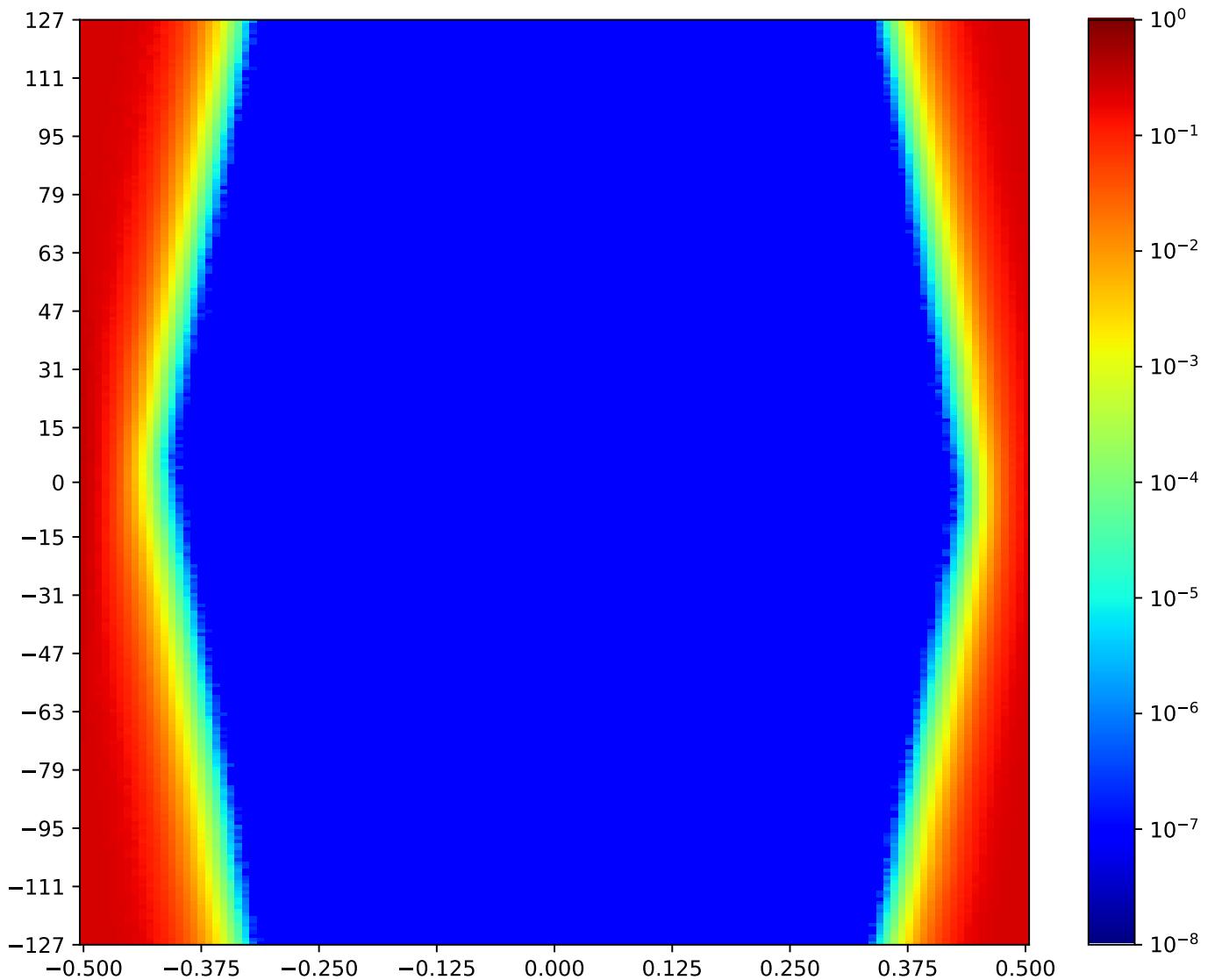


Figure 1.131: MSP\_A\_FPGA-TX1-03-RX18-03-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.5 MSP\_A\_FPGA-TX1-04-RX18-04-MSP\_C\_FPGA

Table 1.122: MSP\_A\_FPGA-TX1-04-RX18-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:38:45		2018-Jan-24 15:39:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23720	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

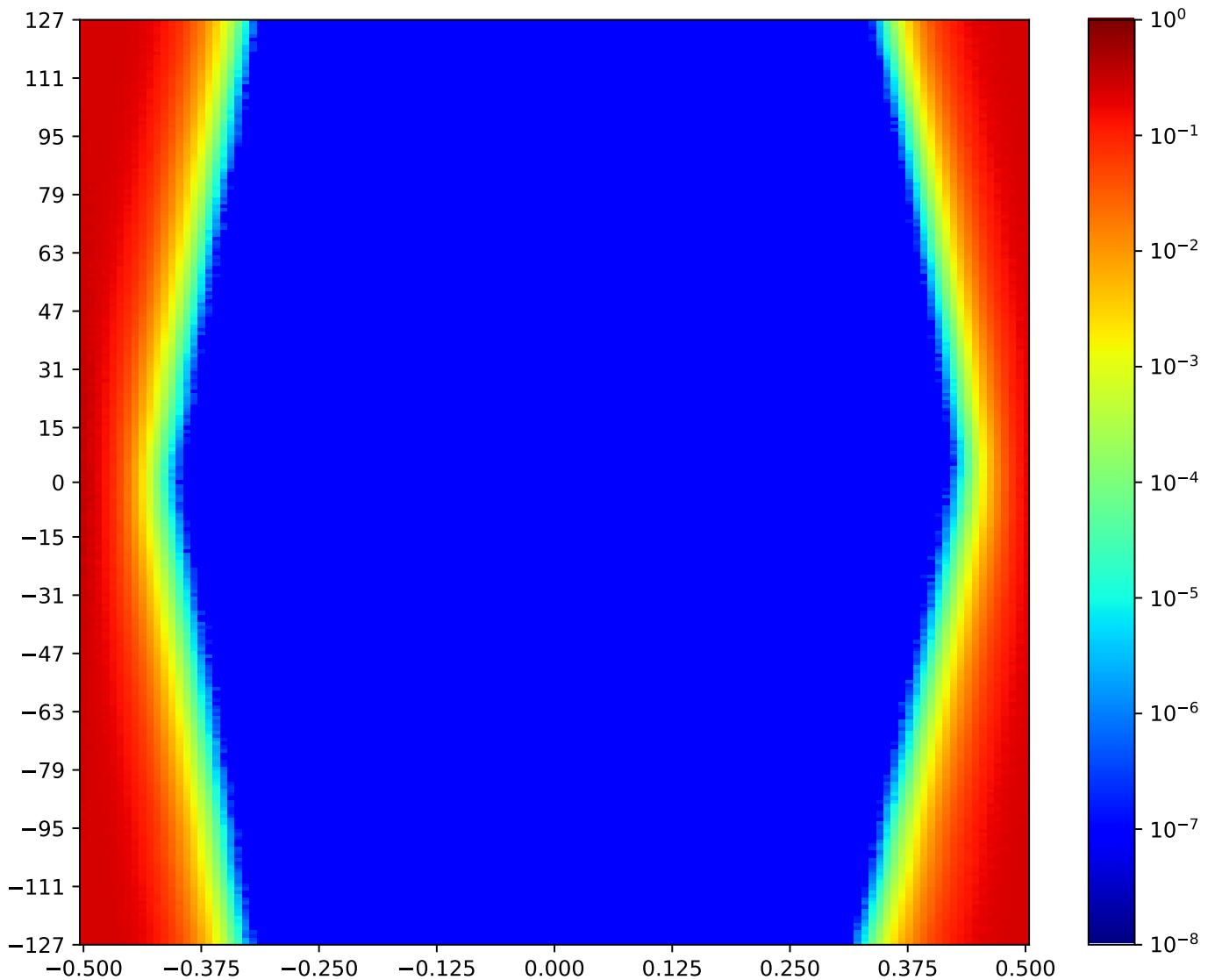


Figure 1.132: MSP\_A\_FPGA-TX1-04-RX18-04-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.6 MSP\_A\_FPGA-TX1-05-RX18-05-MSP\_C\_FPGA

Table 1.123: MSP\_A\_FPGA-TX1-05-RX18-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:28:21		2018-Jan-24 15:29:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24172	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

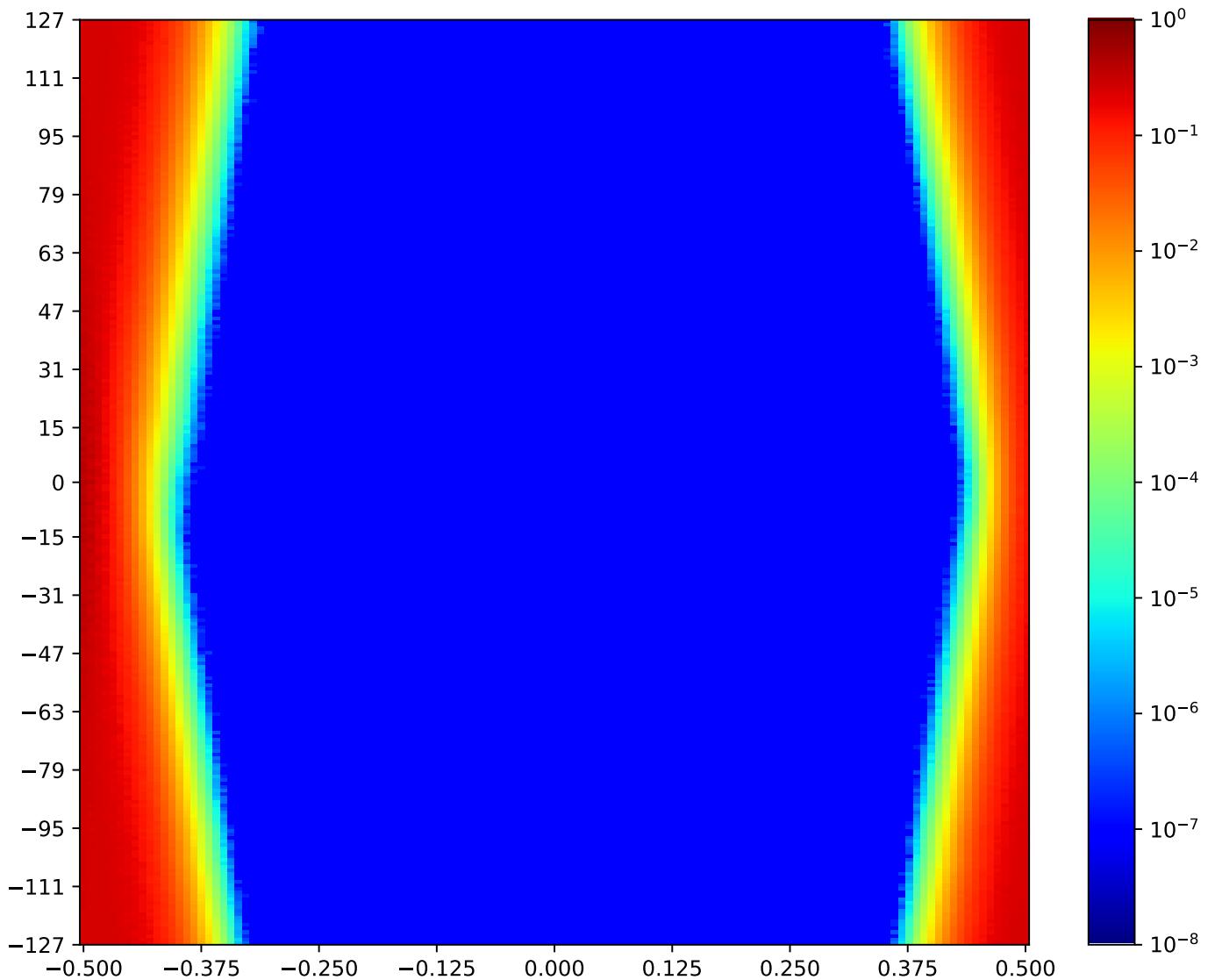


Figure 1.133: MSP\_A\_FPGA-TX1-05-RX18-05-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.7 MSP\_A\_FPGA-TX1-06-RX18-06-MSP\_C\_FPGA

Table 1.124: MSP\_A\_FPGA-TX1-06-RX18-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:41:05		2018-Jan-24 15:42:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25351	107	82.95%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

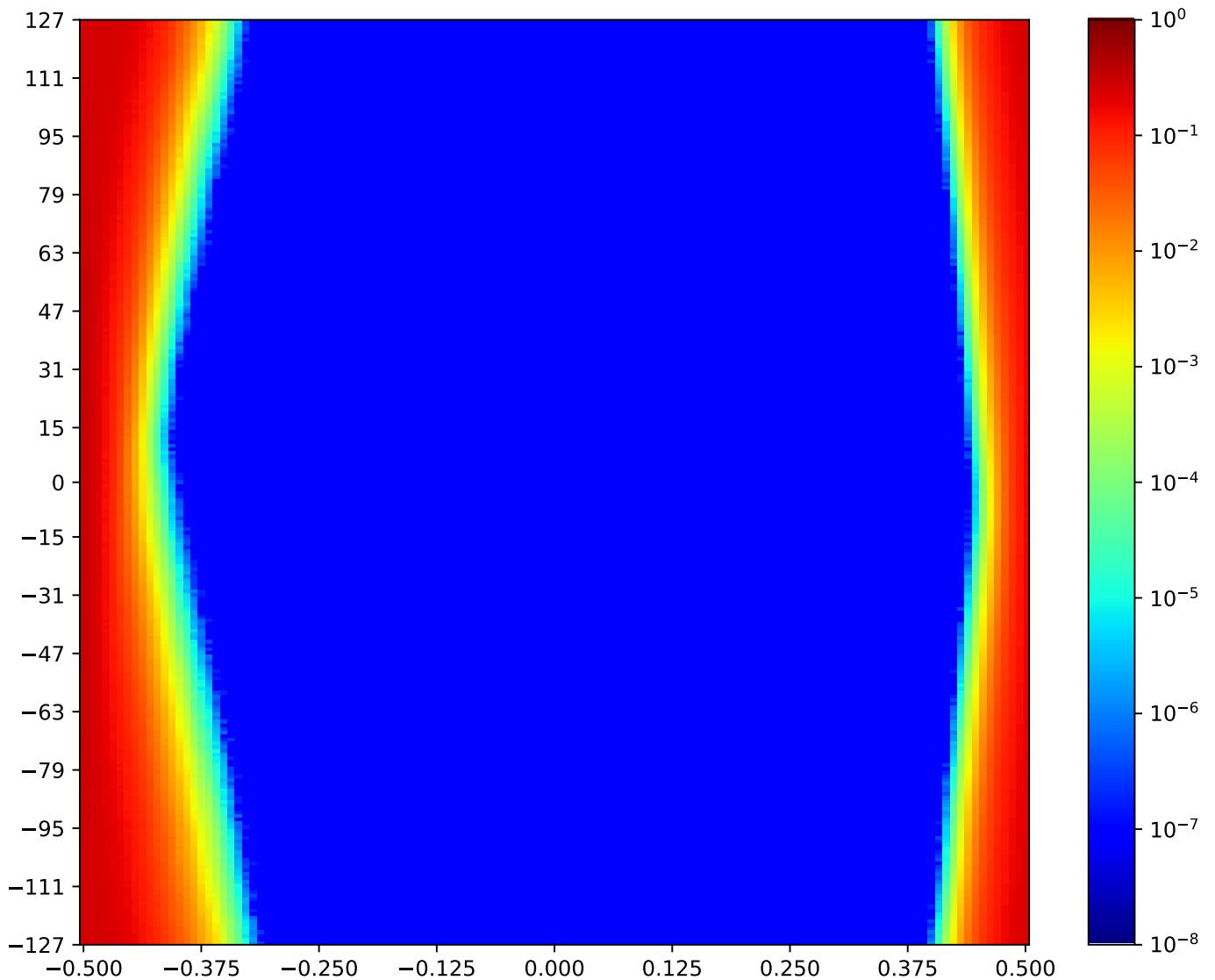


Figure 1.134: MSP\_A\_FPGA-TX1-06-RX18-06-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.8 MSP\_A\_FPGA-TX1-07-RX18-07-MSP\_C\_FPGA

Table 1.125: MSP\_A\_FPGA-TX1-07-RX18-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:30:39		2018-Jan-24 15:31:48	
Reset RX	OA	HO		HO (%)	
true	25212	107		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

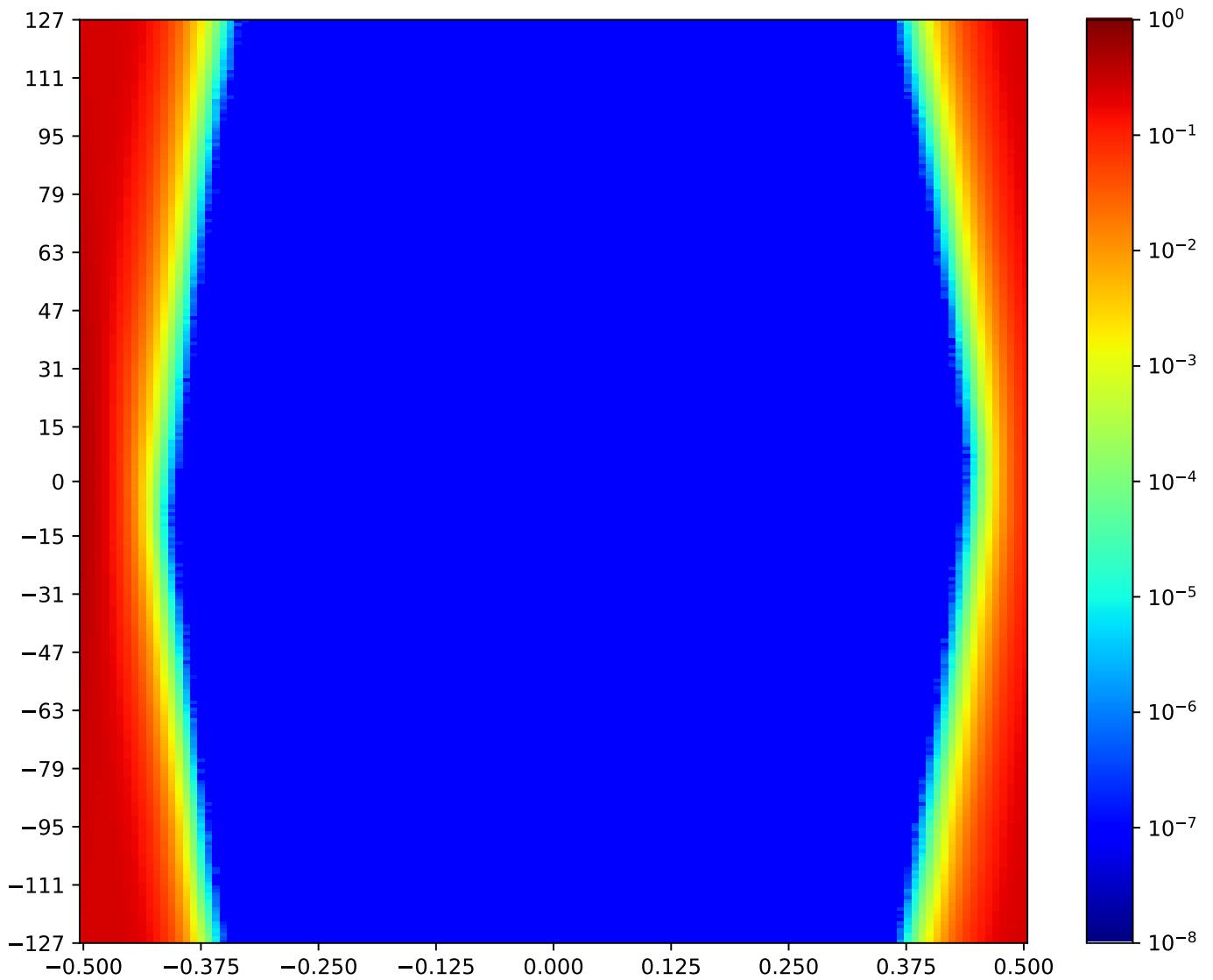


Figure 1.135: MSP\_A\_FPGA-TX1-07-RX18-07-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.9 MSP\_A\_FPGA-TX1-08-RX18-08-MSP\_C\_FPGA

Table 1.126: MSP\_A\_FPGA-TX1-08-RX18-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:39:55		2018-Jan-24 15:41:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24400	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

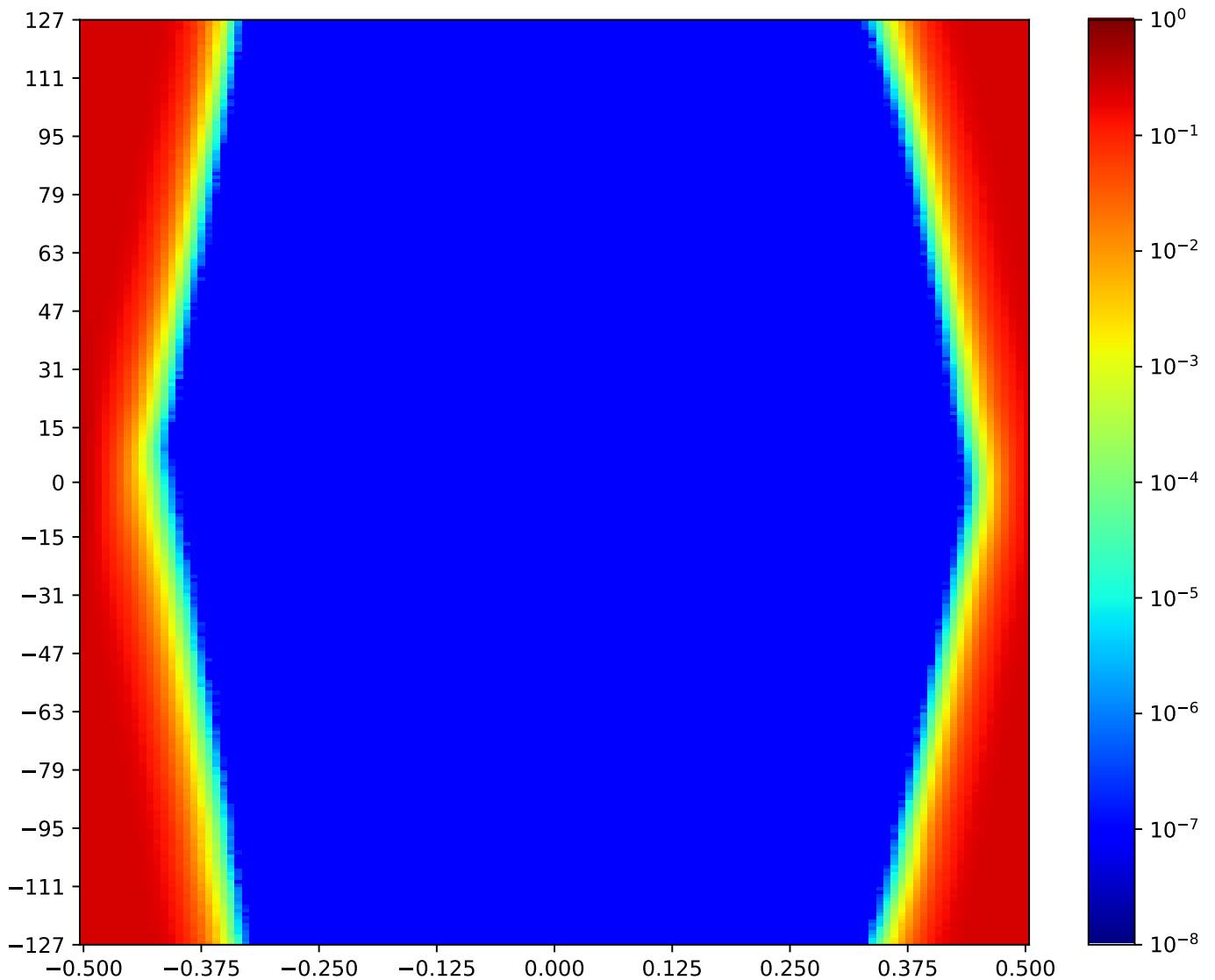


Figure 1.136: MSP\_A\_FPGA-TX1-08-RX18-08-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.10 MSP\_A\_FPGA-TX1-09-RX18-09-MSP\_C\_FPGA

Table 1.127: MSP\_A\_FPGA-TX1-09-RX18-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:32:58		2018-Jan-24 15:34:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24246	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

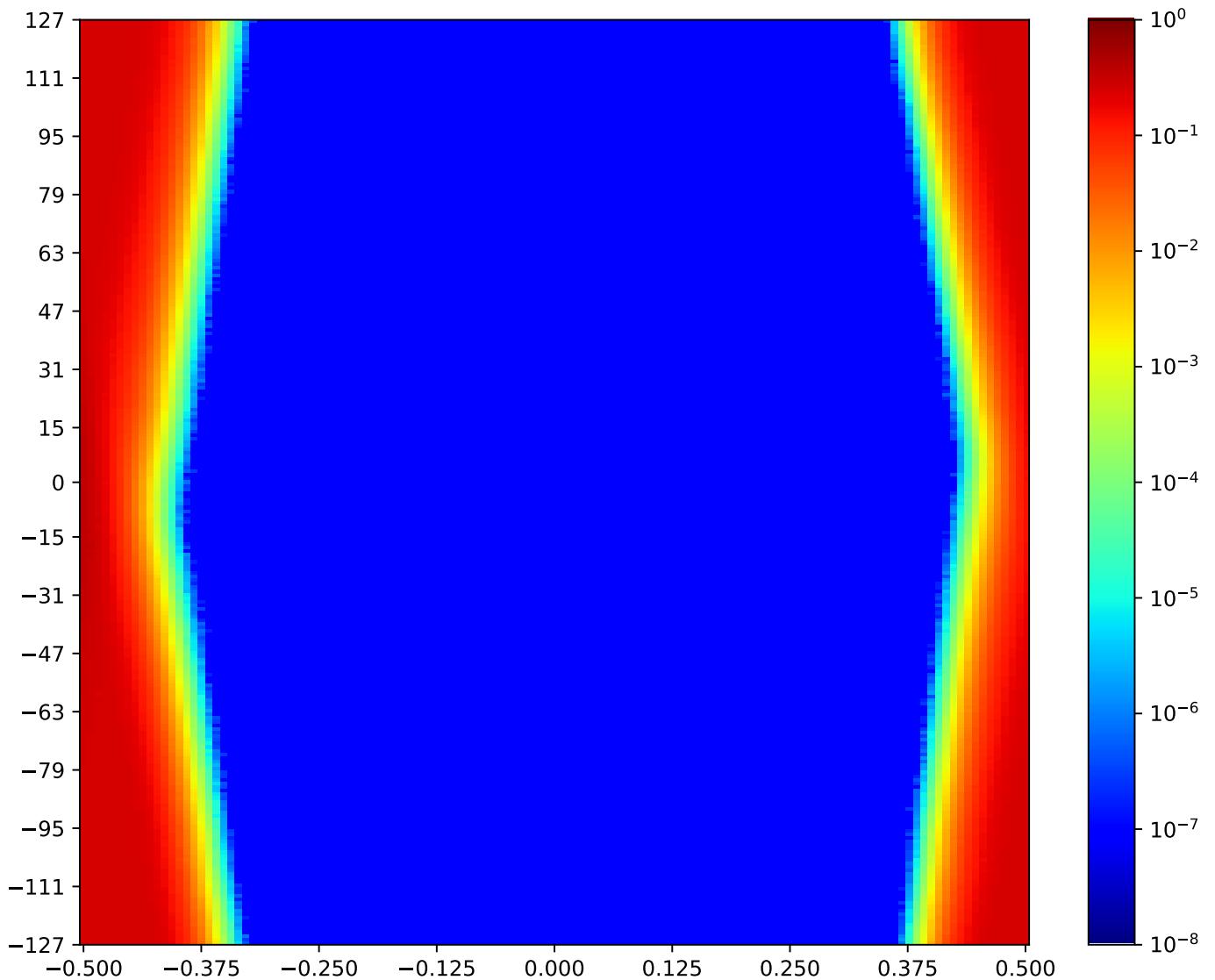


Figure 1.137: MSP\_A\_FPGA-TX1-09-RX18-09-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.11 MSP\_A\_FPGA-TX1-10-RX18-10-MSP\_C\_FPGA

Table 1.128: MSP\_A\_FPGA-TX1-10-RX18-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:37:36		2018-Jan-24 15:38:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23357	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

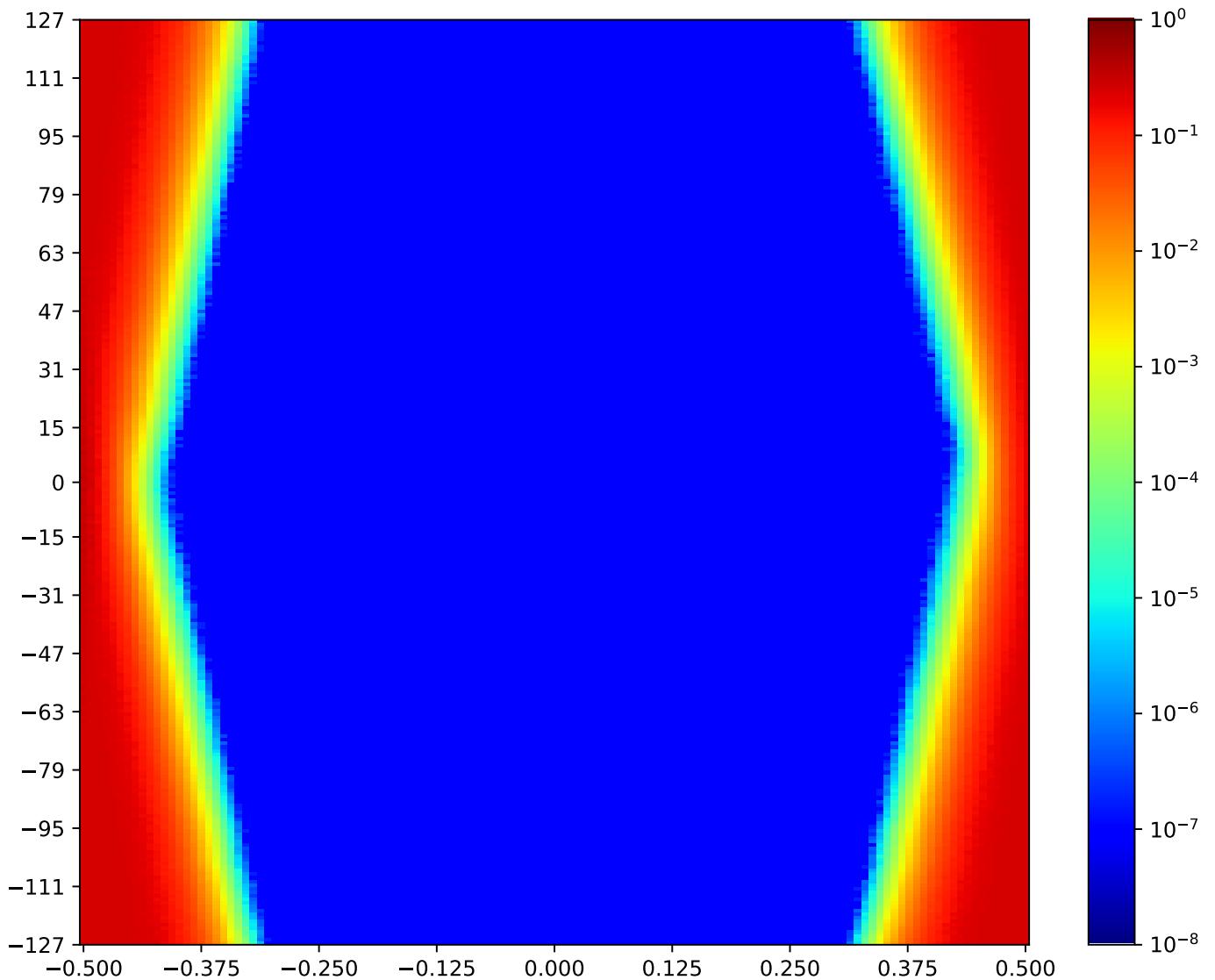


Figure 1.138: MSP\_A\_FPGA-TX1-10-RX18-10-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.10.12 MSP\_A\_FPGA-TX1-11-RX18-11-MSP\_C\_FPGA

Table 1.129: MSP\_A\_FPGA-TX1-11-RX18-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:36:25		2018-Jan-24 15:37:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25337	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

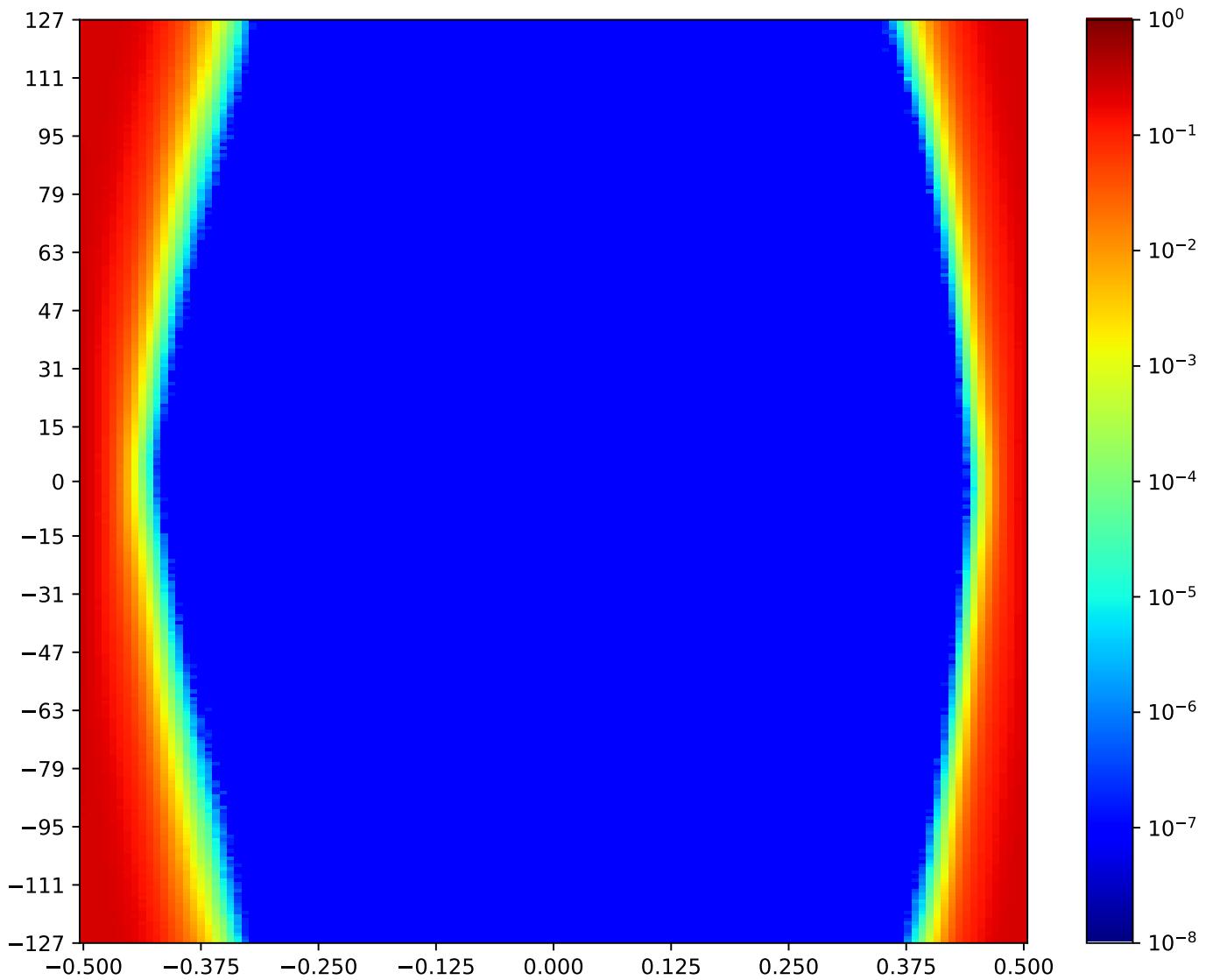


Figure 1.139: MSP\_A\_FPGA-TX1-11-RX18-11-MSP\_C\_FPGA

Call back to summary Figure 1.127. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.11 MSP\_A TX2 MSP\_C RX17 Minipod Loopback

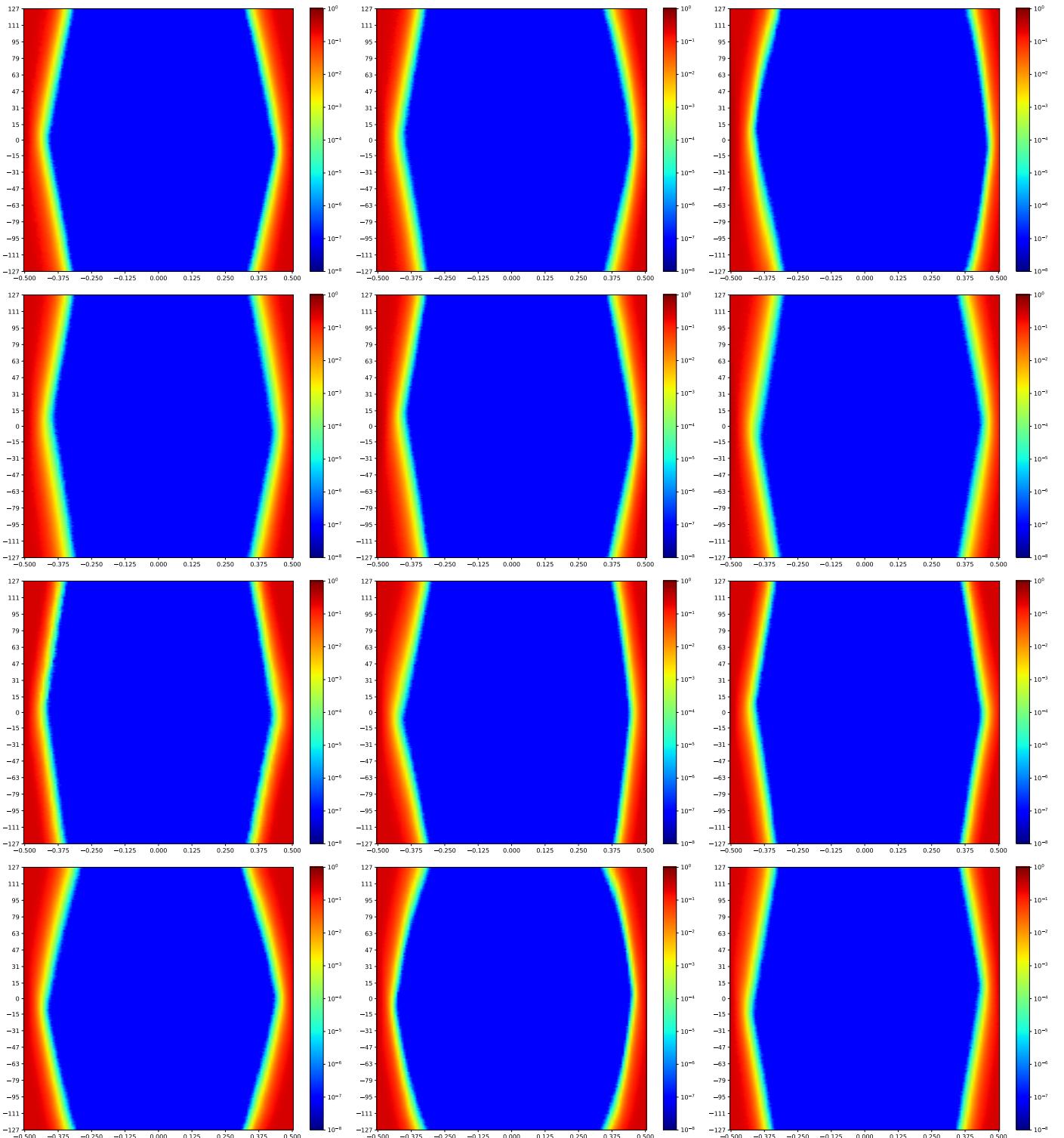


Figure 1.140: MSP\_A TX2 MSP\_C RX17 Minipod Loopback

A cross-reference to Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.153.

### 1.11.1 MSP\_A\_FPGA-TX2-00-RX17-00-MSP\_C\_FPGA

Table 1.130: MSP\_A\_FPGA-TX2-00-RX17-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:45:47		2018-Jan-24 15:46:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23920	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

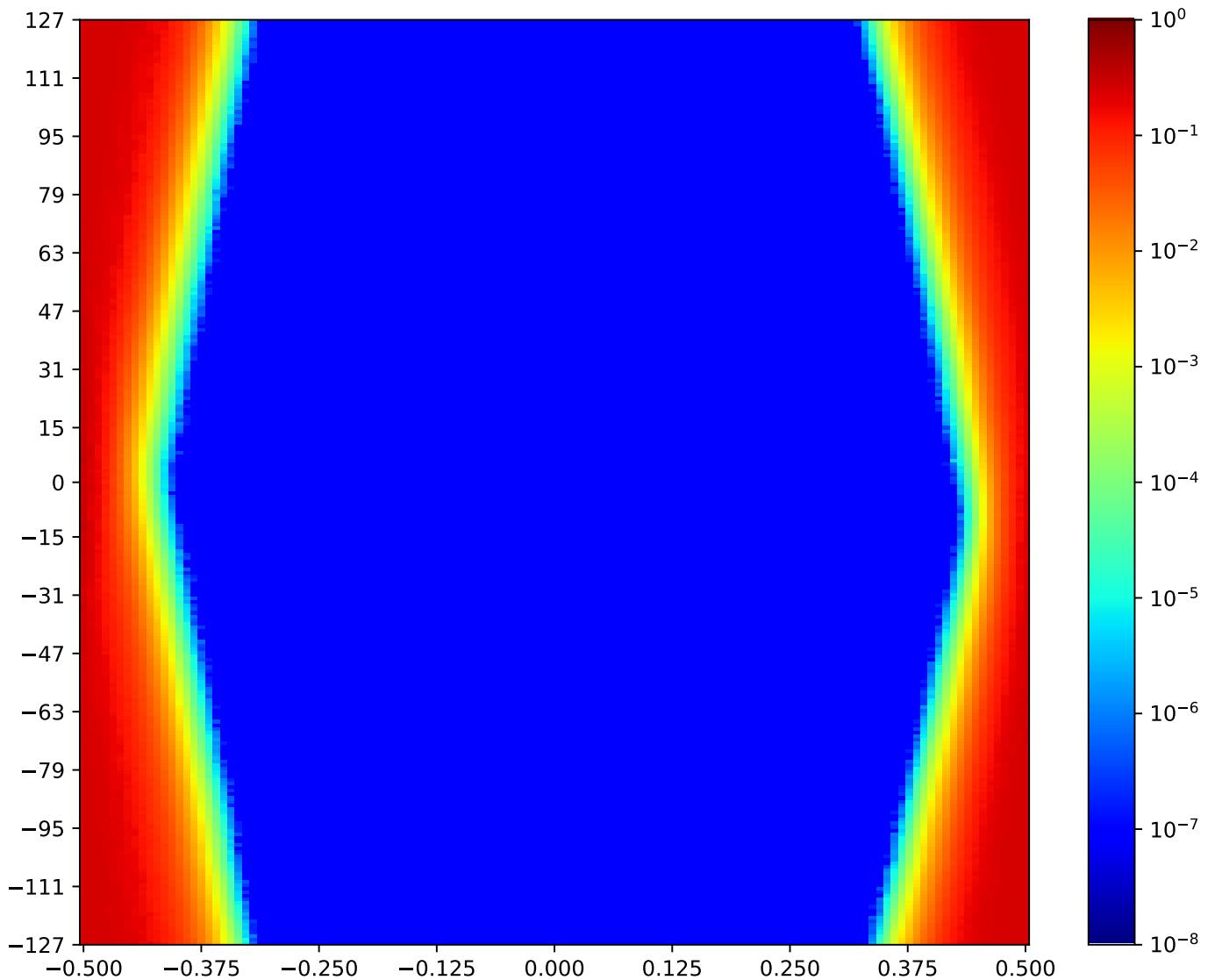


Figure 1.141: MSP\_A\_FPGA-TX2-00-RX17-00-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.2 MSP\_A\_FPGA-TX2-01-RX17-01-MSP\_C\_FPGA

Table 1.131: MSP\_A\_FPGA-TX2-01-RX17-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:43:26		2018-Jan-24 15:44:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24122	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

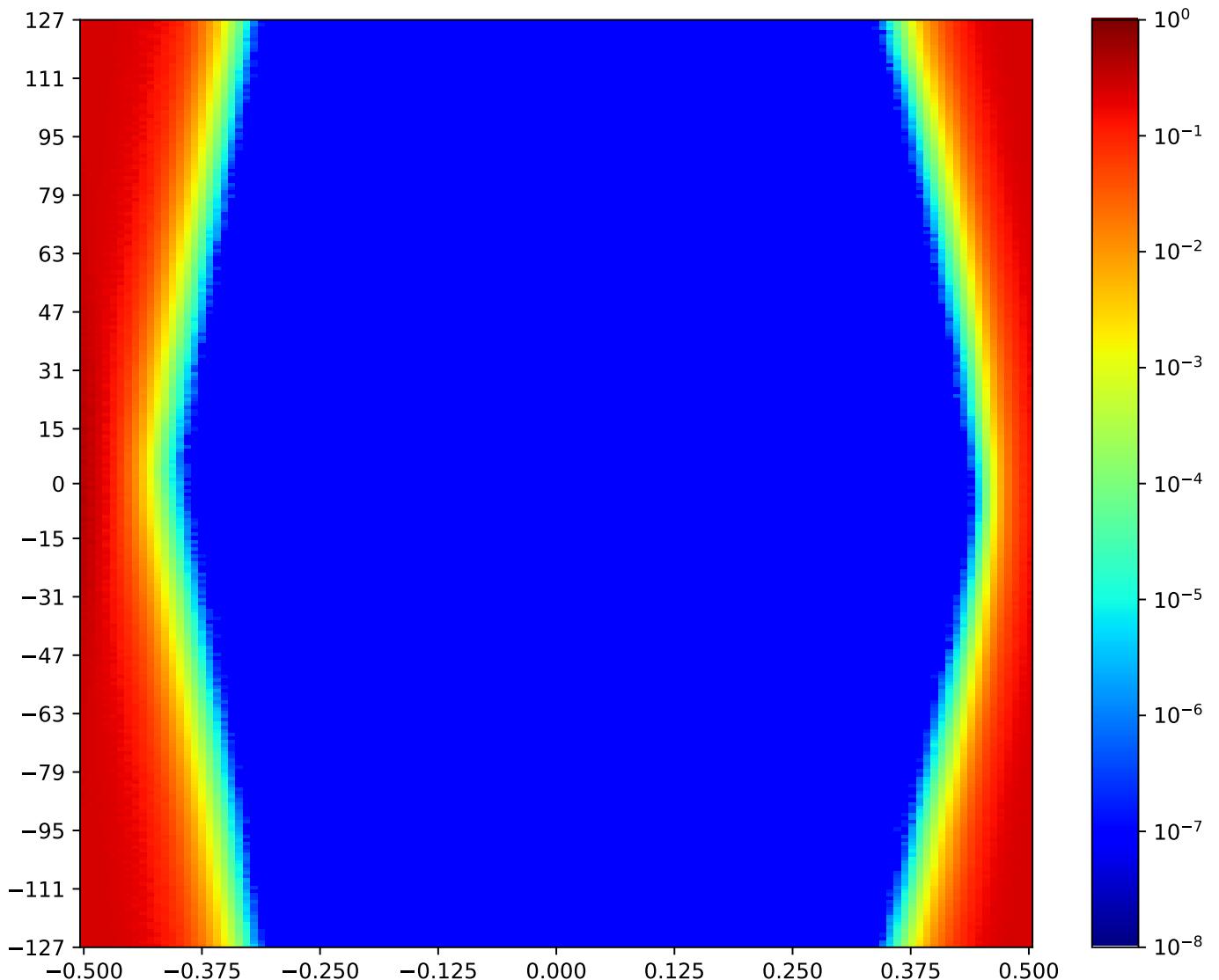


Figure 1.142: MSP\_A\_FPGA-TX2-01-RX17-01-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.3 MSP\_A\_FPGA-TX2-02-RX17-02-MSP\_C\_FPGA

Table 1.132: MSP\_A\_FPGA-TX2-02-RX17-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:49:16		2018-Jan-24 15:50:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24995	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

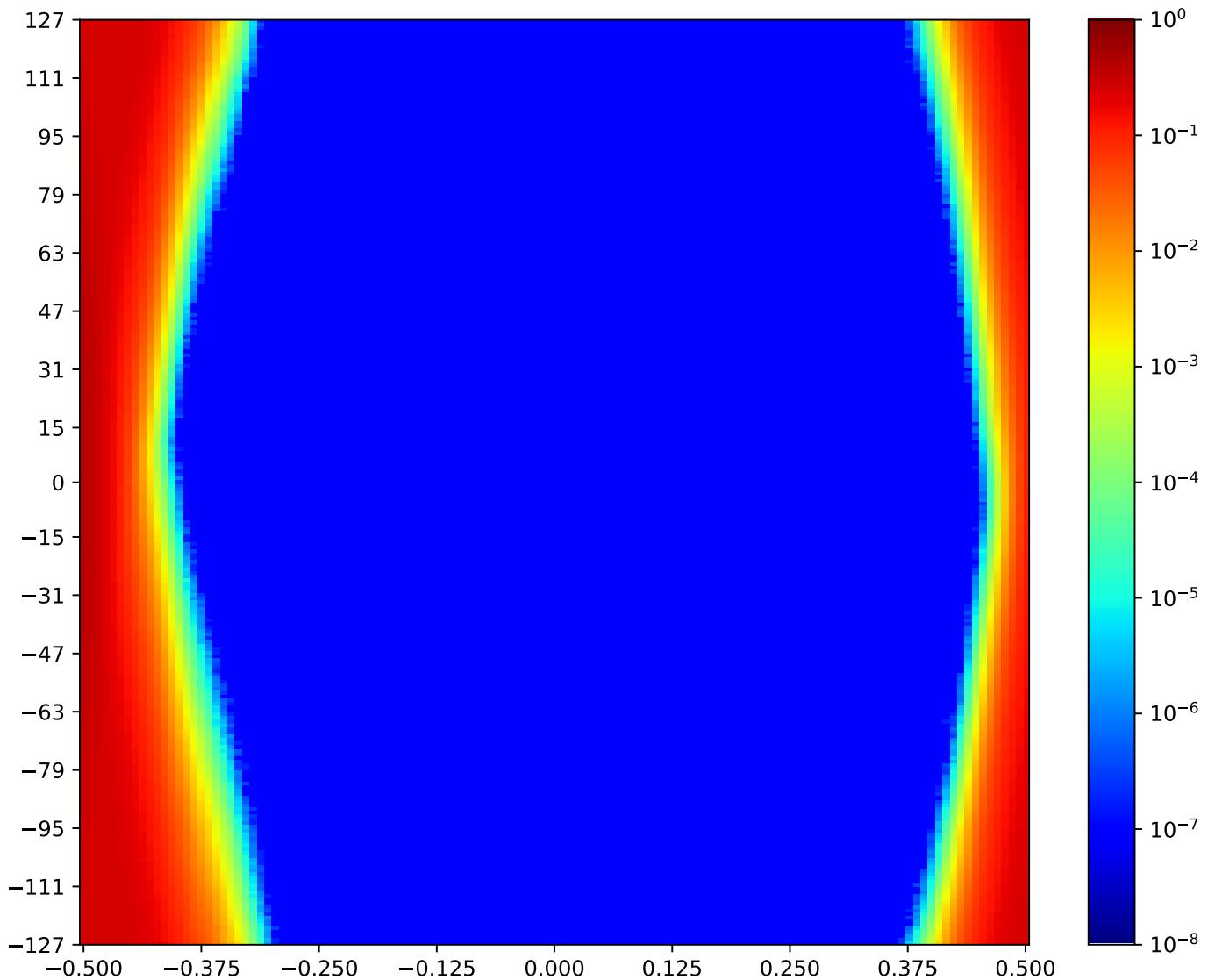


Figure 1.143: MSP\_A\_FPGA-TX2-02-RX17-02-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.11.4 MSP\_A\_FPGA-TX2-03-RX17-03-MSP\_C\_FPGA

Table 1.133: MSP\_A\_FPGA-TX2-03-RX17-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:42:15		2018-Jan-24 15:43:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23435	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

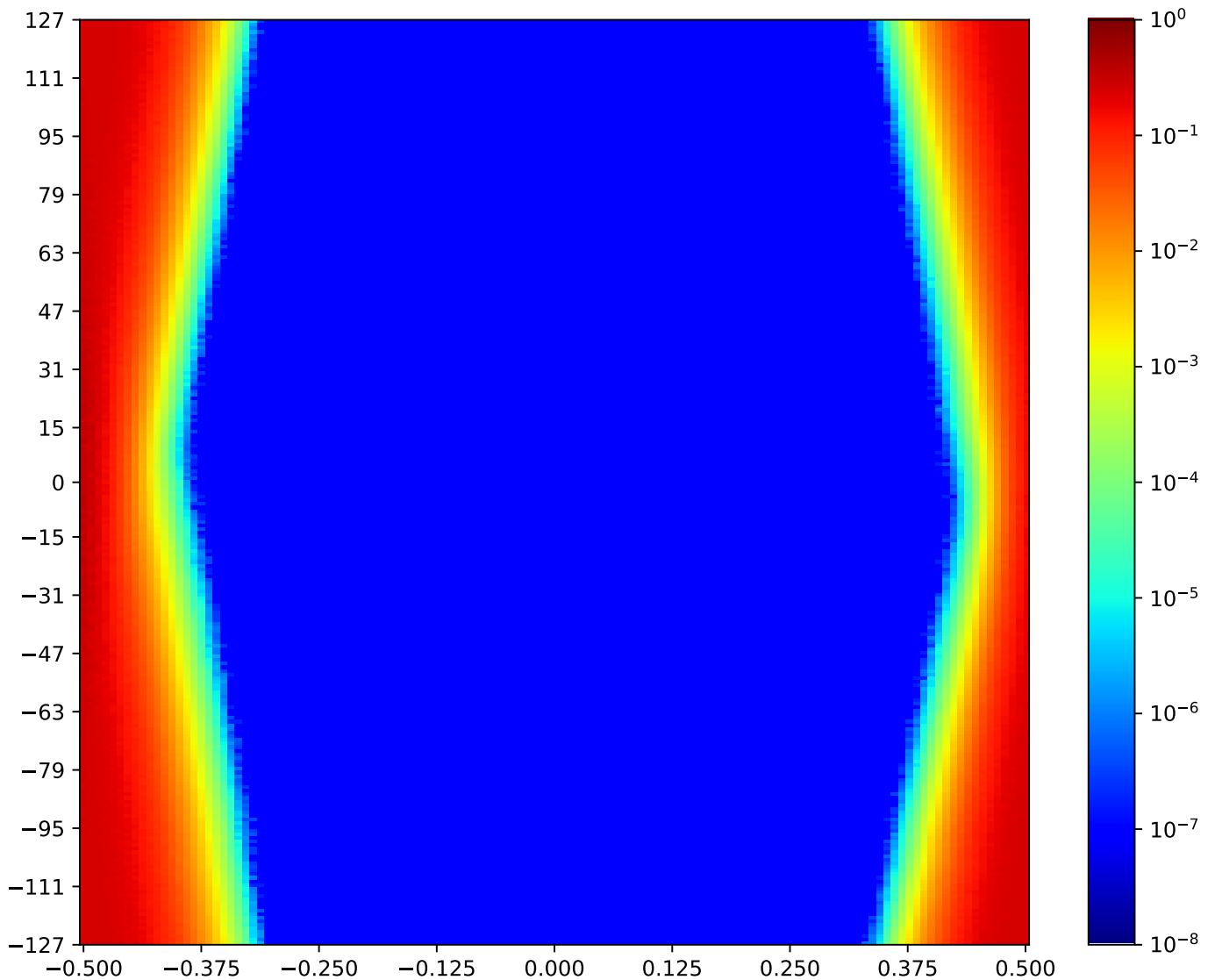


Figure 1.144: MSP\_A\_FPGA-TX2-03-RX17-03-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.5 MSP\_A\_FPGA-TX2-04-RX17-04-MSP\_C\_FPGA

Table 1.134: MSP\_A\_FPGA-TX2-04-RX17-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:52:51		2018-Jan-24 15:54:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24225	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

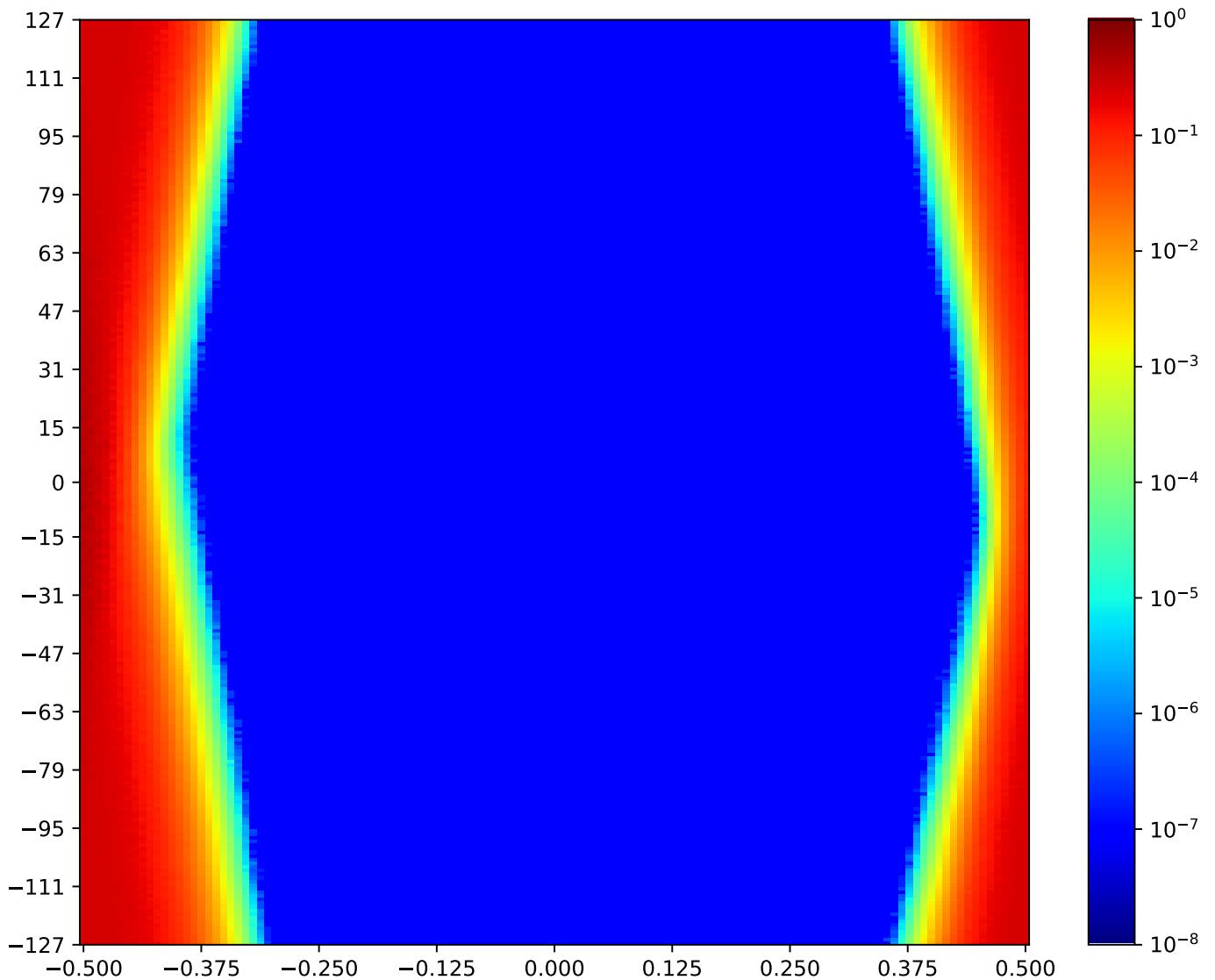


Figure 1.145: MSP\_A\_FPGA-TX2-04-RX17-04-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.6 MSP\_A\_FPGA-TX2-05-RX17-05-MSP\_C\_FPGA

Table 1.135: MSP\_A\_FPGA-TX2-05-RX17-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:44:36		2018-Jan-24 15:45:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23474	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

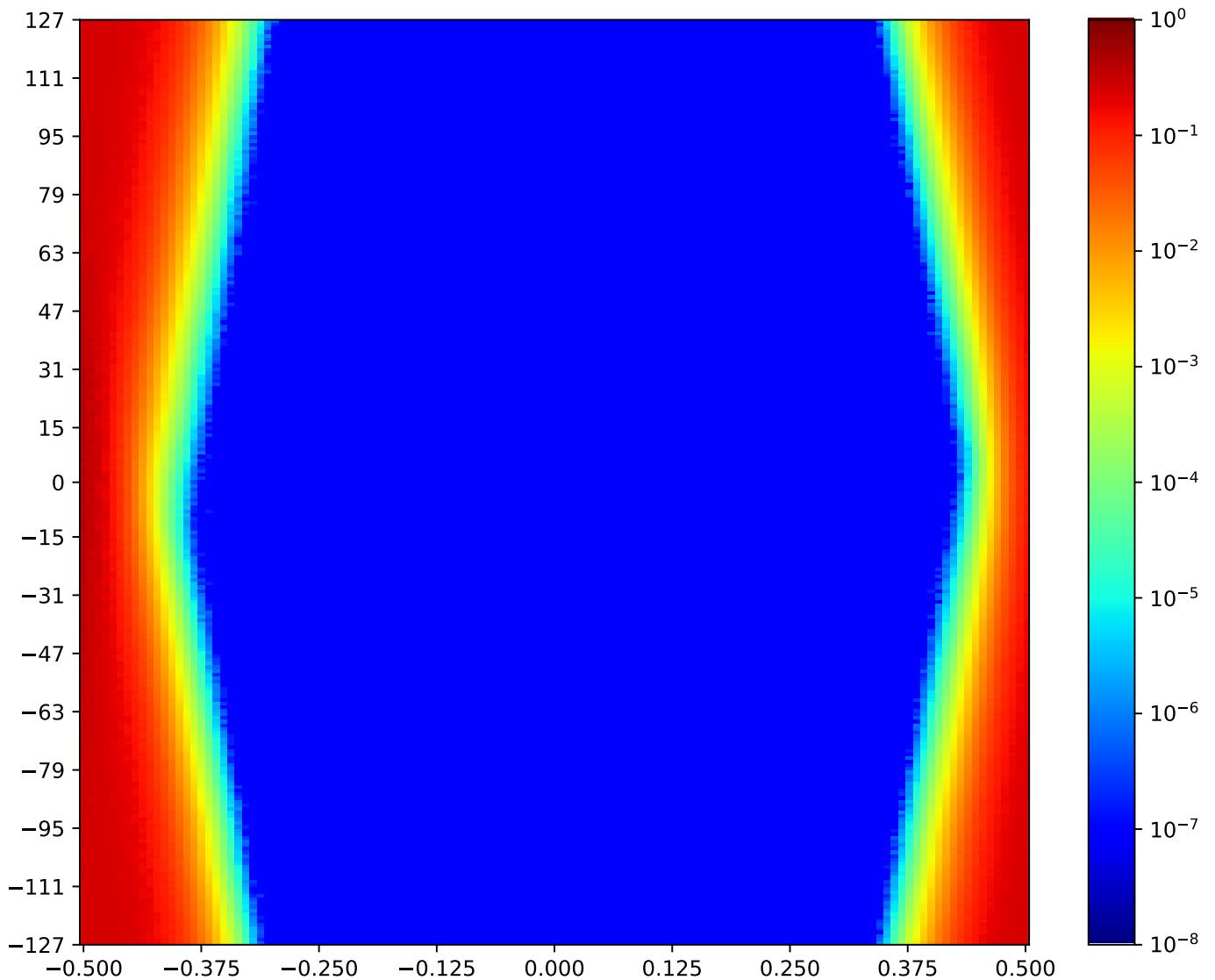


Figure 1.146: MSP\_A\_FPGA-TX2-05-RX17-05-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.7 MSP\_A\_FPGA-TX2-06-RX17-06-MSP\_C\_FPGA

Table 1.136: MSP\_A\_FPGA-TX2-06-RX17-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:55:11		2018-Jan-24 15:56:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24264	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

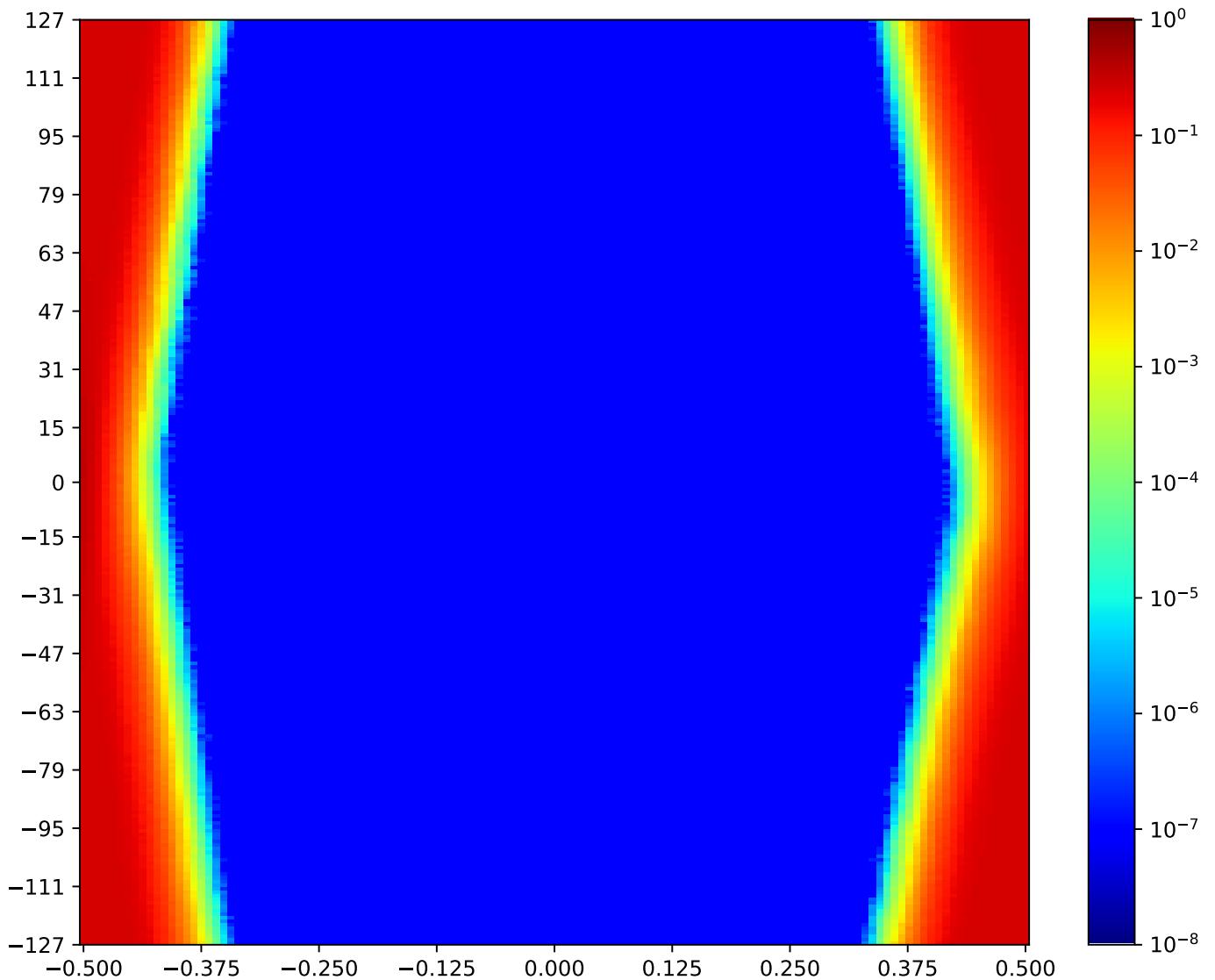


Figure 1.147: MSP\_A\_FPGA-TX2-06-RX17-06-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.8 MSP\_A\_FPGA-TX2-07-RX17-07-MSP\_C\_FPGA

Table 1.137: MSP\_A\_FPGA-TX2-07-RX17-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:46:57		2018-Jan-24 15:48:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24407	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

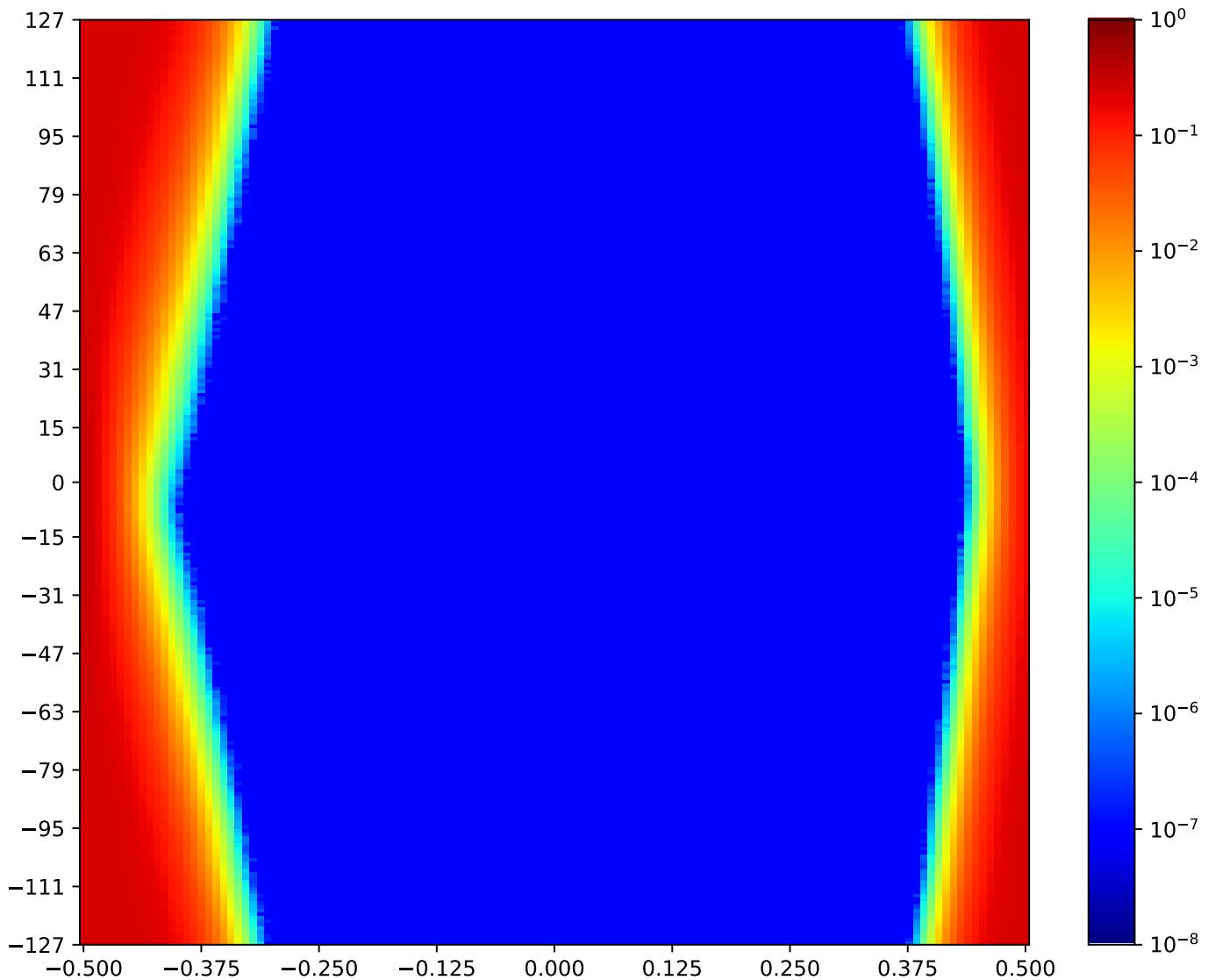


Figure 1.148: MSP\_A\_FPGA-TX2-07-RX17-07-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.9 MSP\_A\_FPGA-TX2-08-RX17-08-MSP\_C\_FPGA

Table 1.138: MSP\_A\_FPGA-TX2-08-RX17-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:54:01		2018-Jan-24 15:55:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24308	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

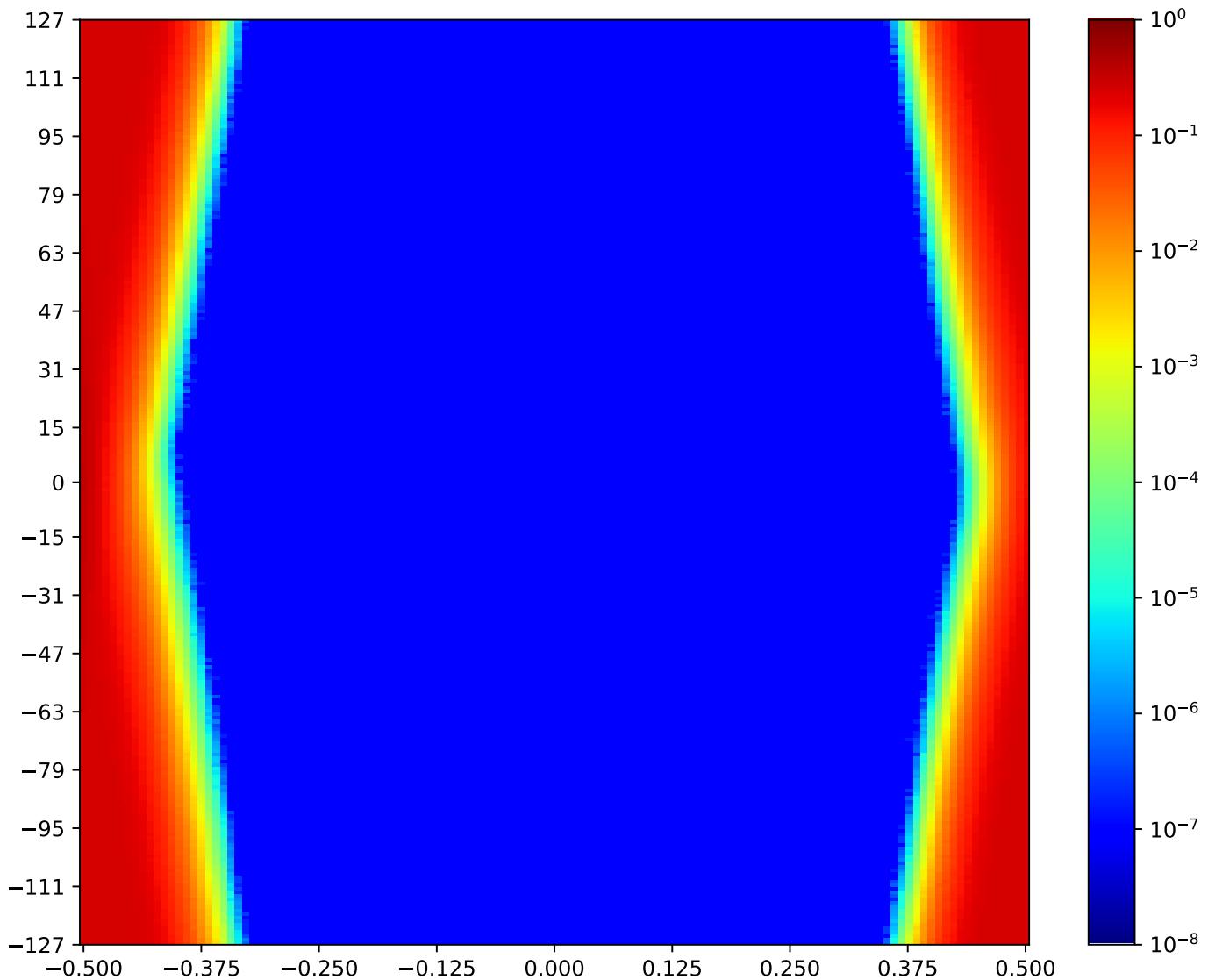


Figure 1.149: MSP\_A\_FPGA-TX2-08-RX17-08-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.10 MSP\_A\_FPGA-TX2-09-RX17-09-MSP\_C\_FPGA

Table 1.139: MSP\_A\_FPGA-TX2-09-RX17-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:48:07		2018-Jan-24 15:49:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23551	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

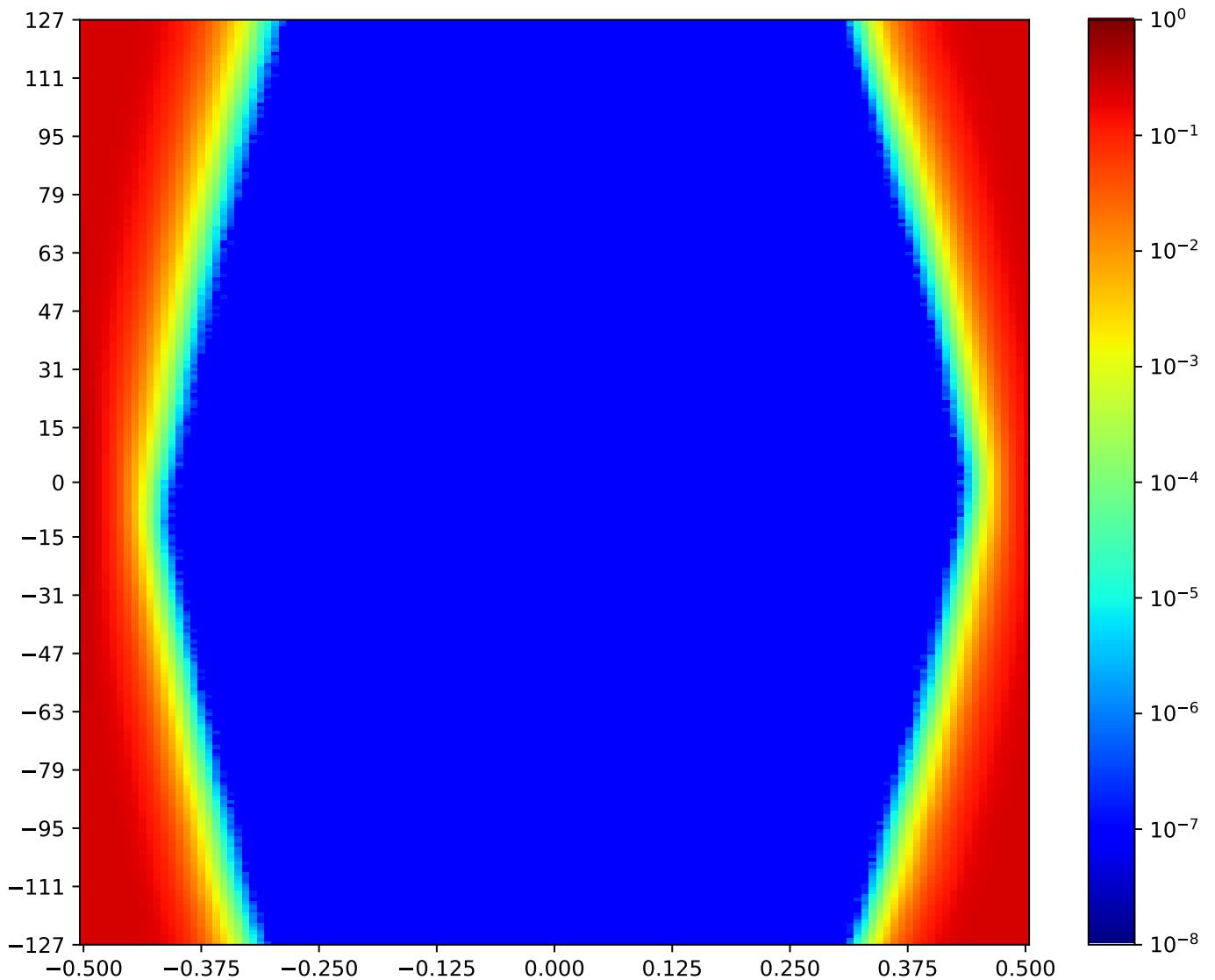


Figure 1.150: MSP\_A\_FPGA-TX2-09-RX17-09-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.11 MSP\_A\_FPGA-TX2-10-RX17-10-MSP\_C\_FPGA

Table 1.140: MSP\_A\_FPGA-TX2-10-RX17-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:51:38		2018-Jan-24 15:52:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25126	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

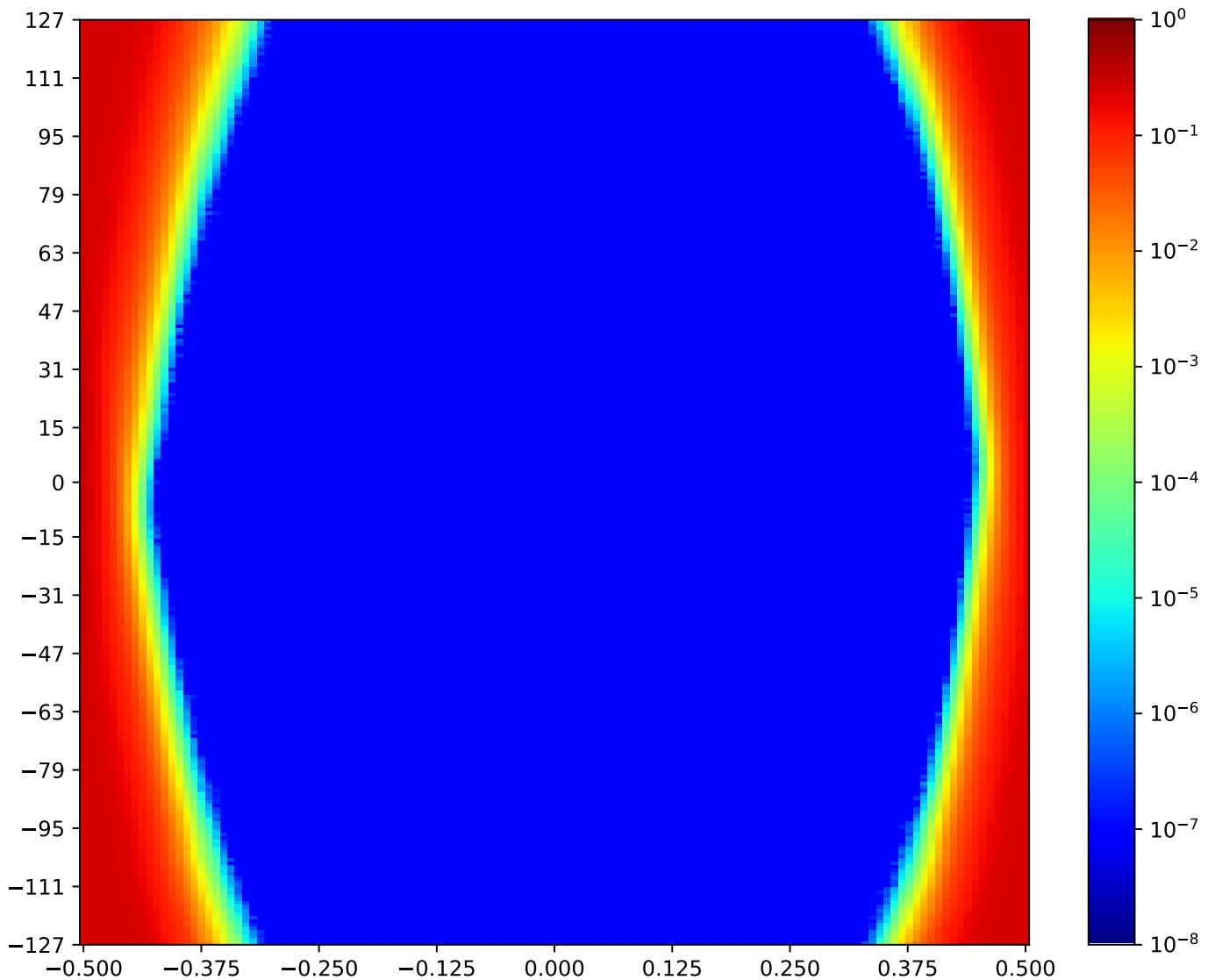


Figure 1.151: MSP\_A\_FPGA-TX2-10-RX17-10-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.11.12 MSP\_A\_FPGA-TX2-11-RX17-11-MSP\_C\_FPGA

Table 1.141: MSP\_A\_FPGA-TX2-11-RX17-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:50:27		2018-Jan-24 15:51:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24326	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

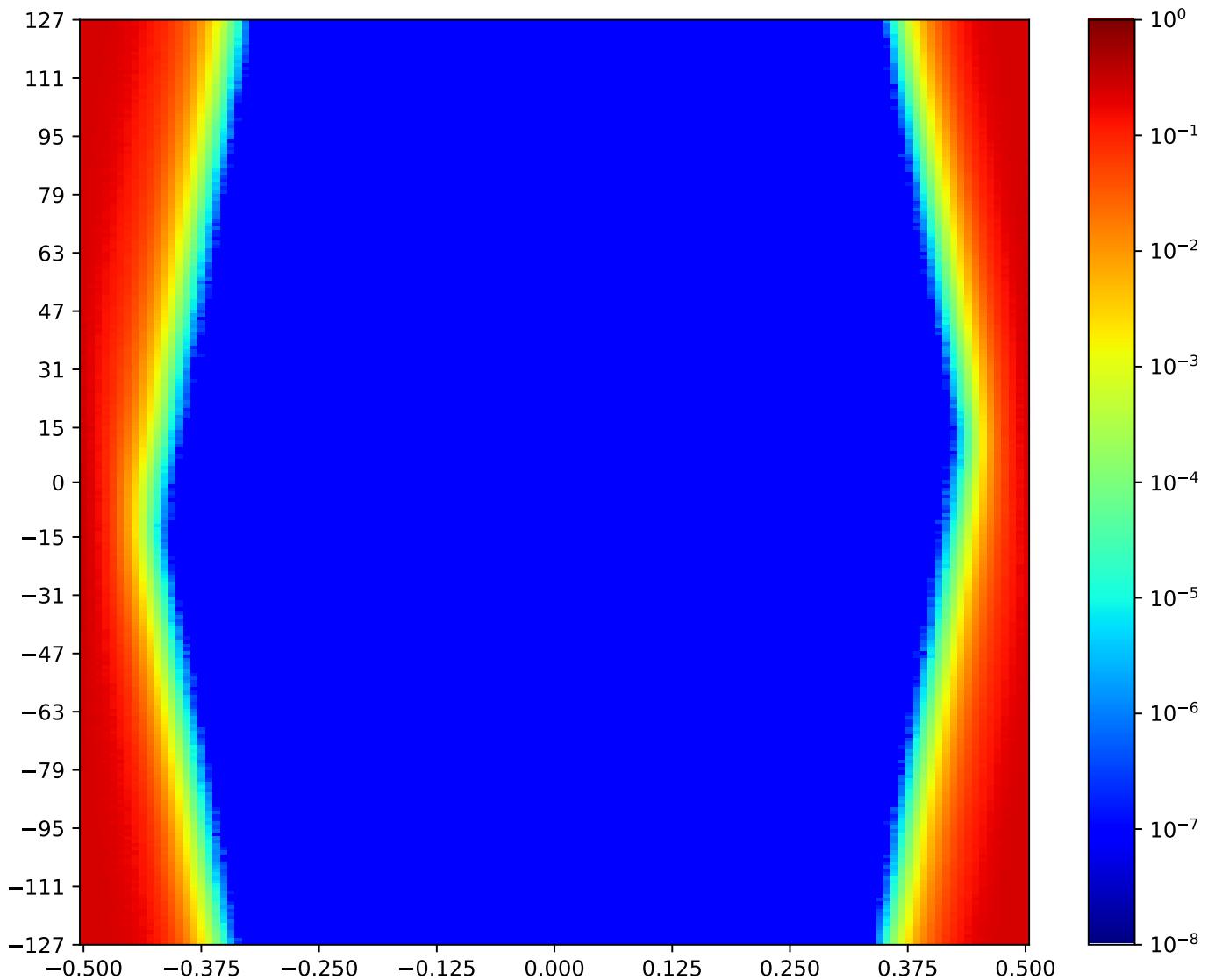


Figure 1.152: MSP\_A\_FPGA-TX2-11-RX17-11-MSP\_C\_FPGA

Call back to summary Figure 1.140. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.12 MSP\_C TX3 MSP\_A RX9 Minipod Loopback

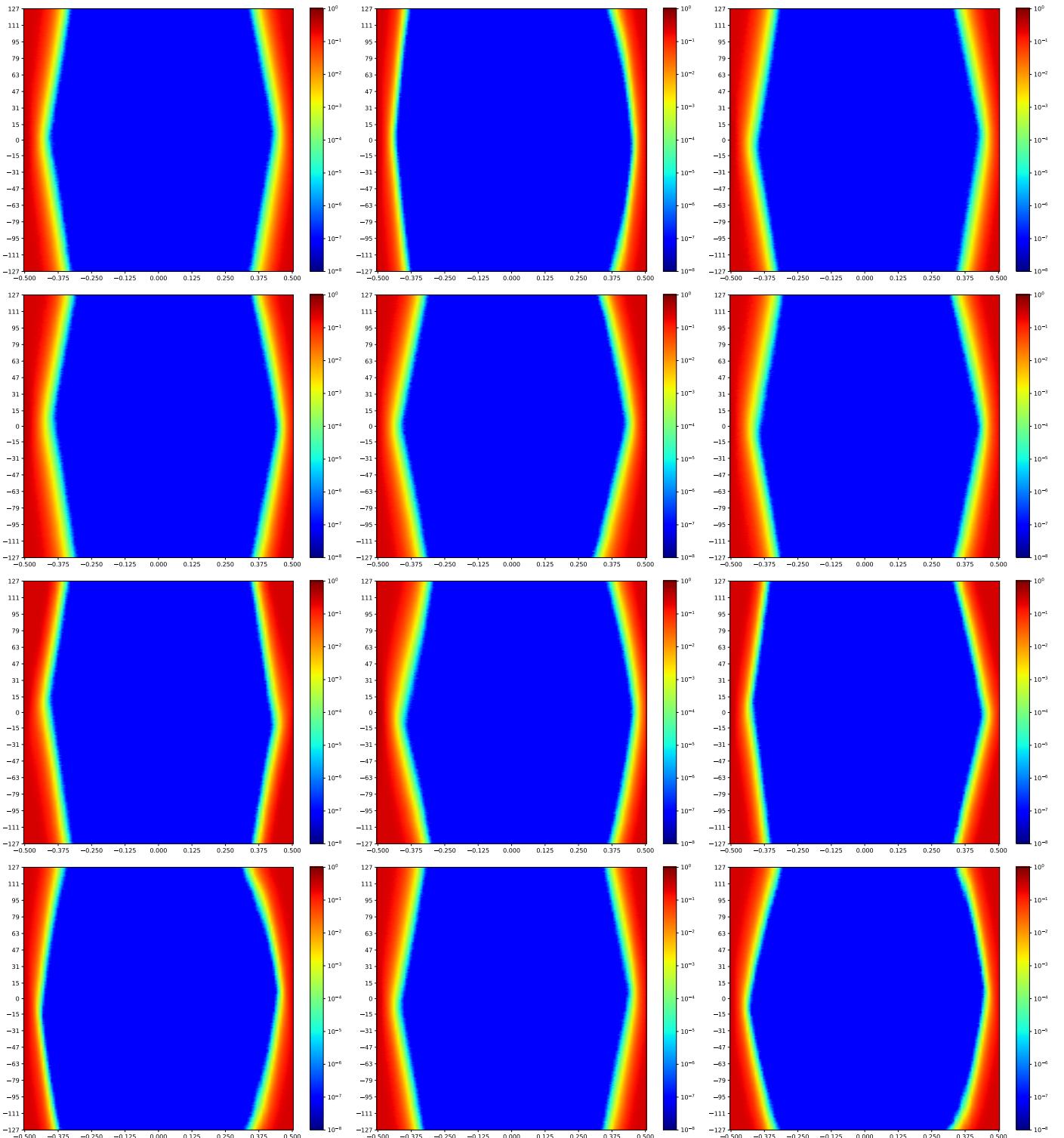


Figure 1.153: MSP\_C TX3 MSP\_A RX9 Minipod Loopback

A cross-reference to Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.166.

### 1.12.1 MSP\_C\_FPGA-TX3-00-RX9-00-MSP\_A\_FPGA

Table 1.142: MSP\_C\_FPGA-TX3-00-RX9-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:59:53		2018-Jan-24 16:01:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23958	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

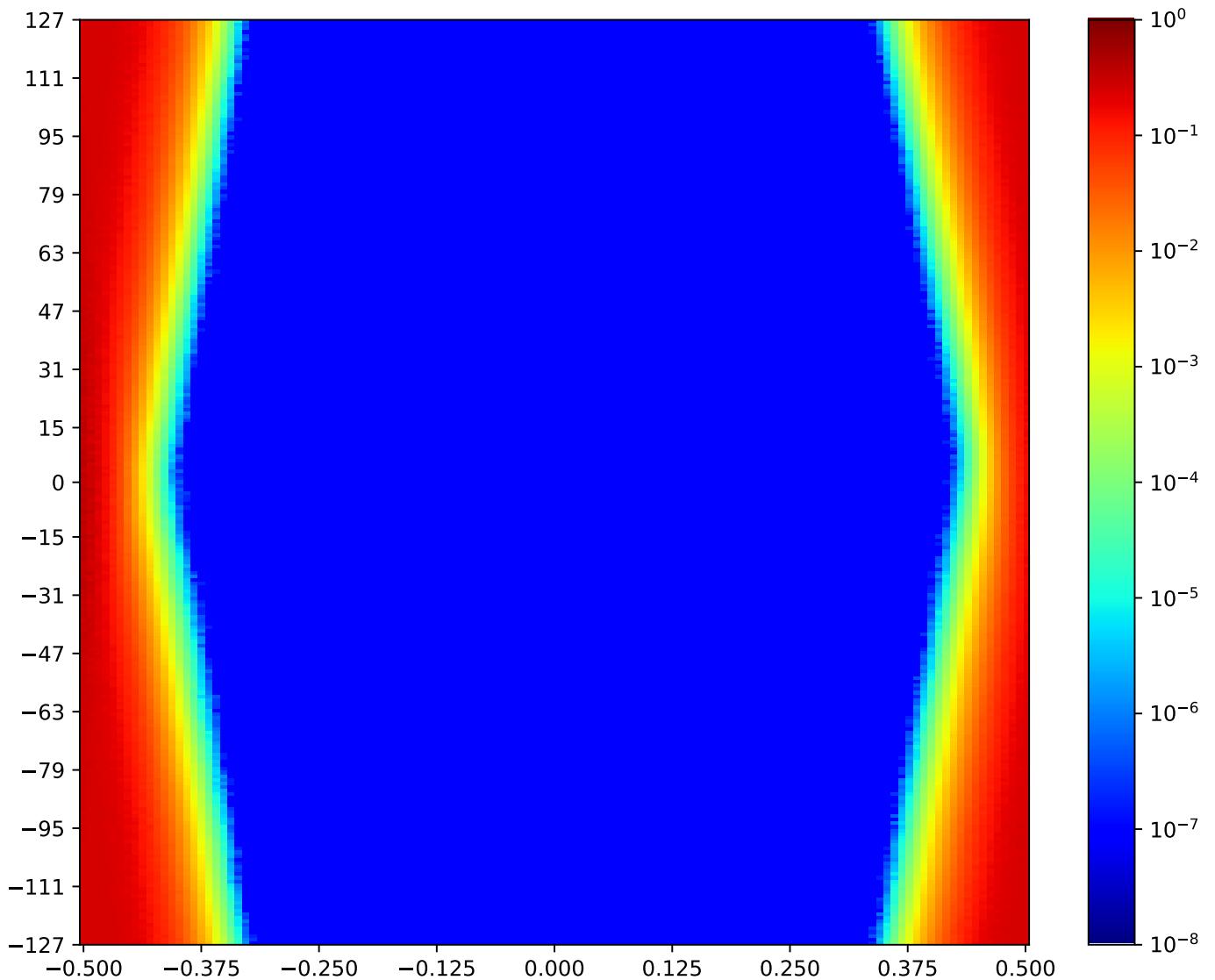


Figure 1.154: MSP\_C\_FPGA-TX3-00-RX9-00-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.2 MSP\_C\_FPGA-TX3-01-RX9-01-MSP\_A\_FPGA

Table 1.143: MSP\_C\_FPGA-TX3-01-RX9-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:02:15		2018-Jan-24 16:03:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26307	111	86.05%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

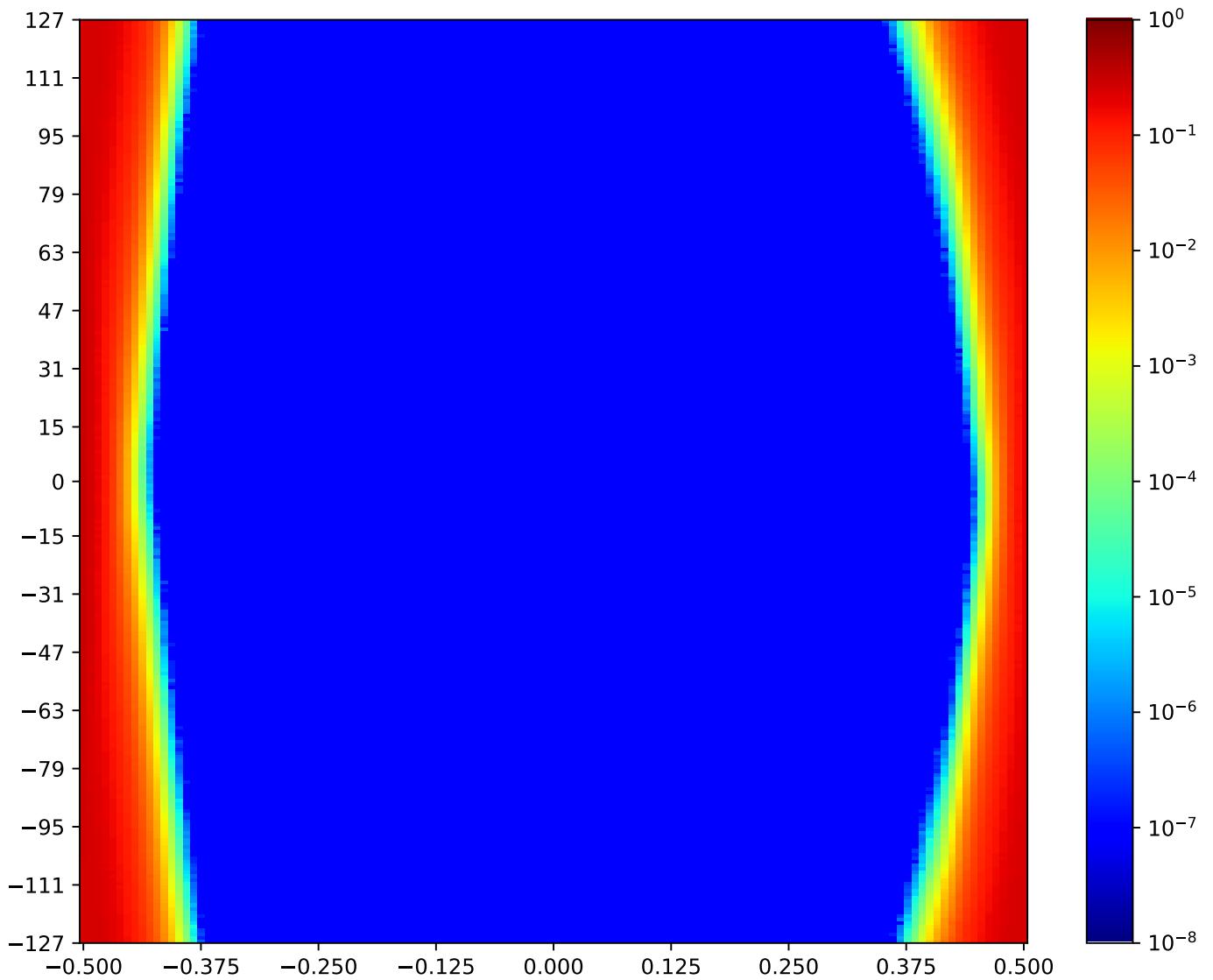


Figure 1.155: MSP\_C\_FPGA-TX3-01-RX9-01-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.3 MSP\_C\_FPGA-TX3-02-RX9-02-MSP\_A\_FPGA

Table 1.144: MSP\_C\_FPGA-TX3-02-RX9-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:03:27		2018-Jan-24 16:04:36	
Reset RX	OA	HO		HO (%)	
true	23633	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

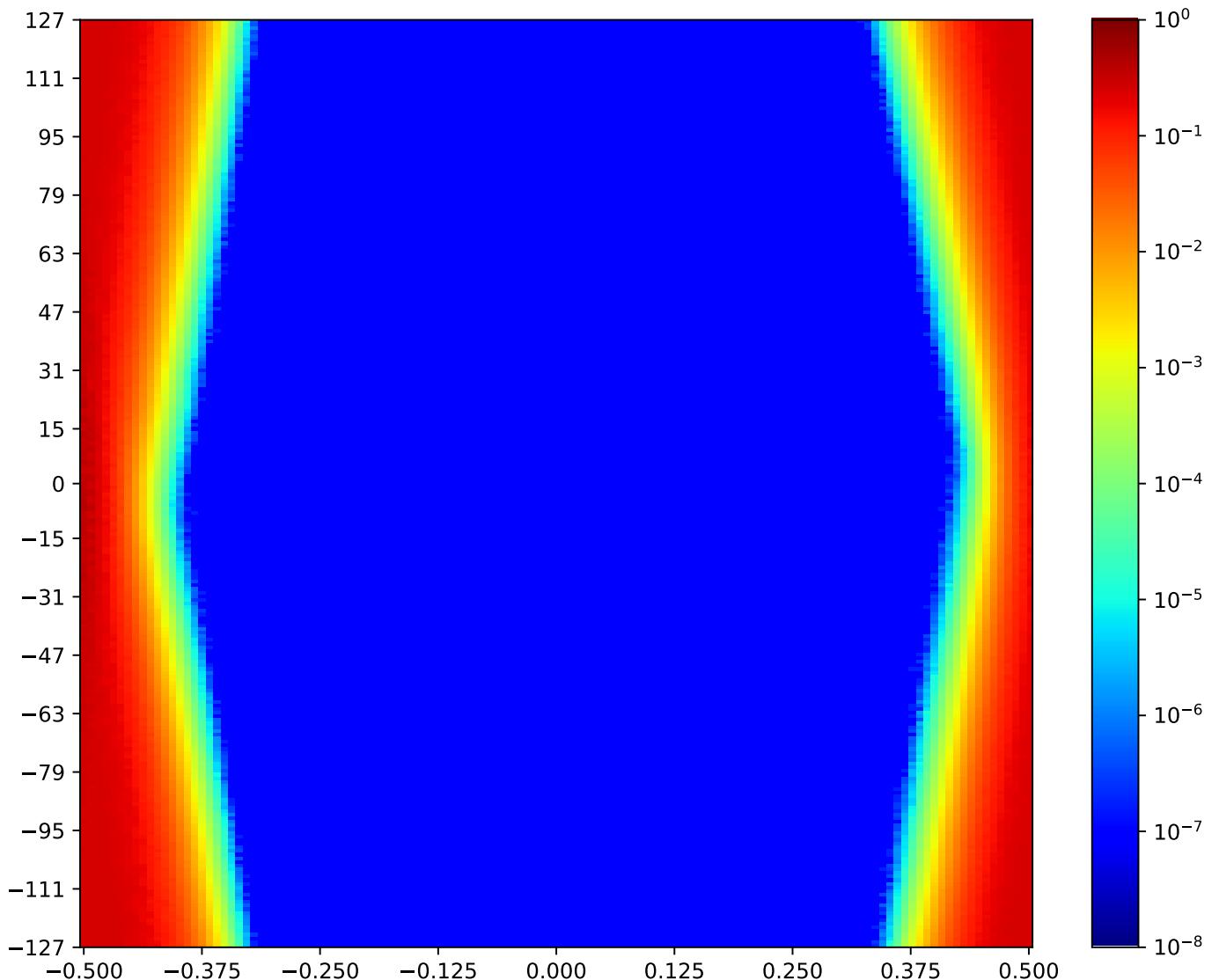


Figure 1.156: MSP\_C\_FPGA-TX3-02-RX9-02-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.12.4 MSP\_C\_FPGA-TX3-03-RX9-03-MSP\_A\_FPGA

Table 1.145: MSP\_C\_FPGA-TX3-03-RX9-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:57:33		2018-Jan-24 15:58:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23780	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

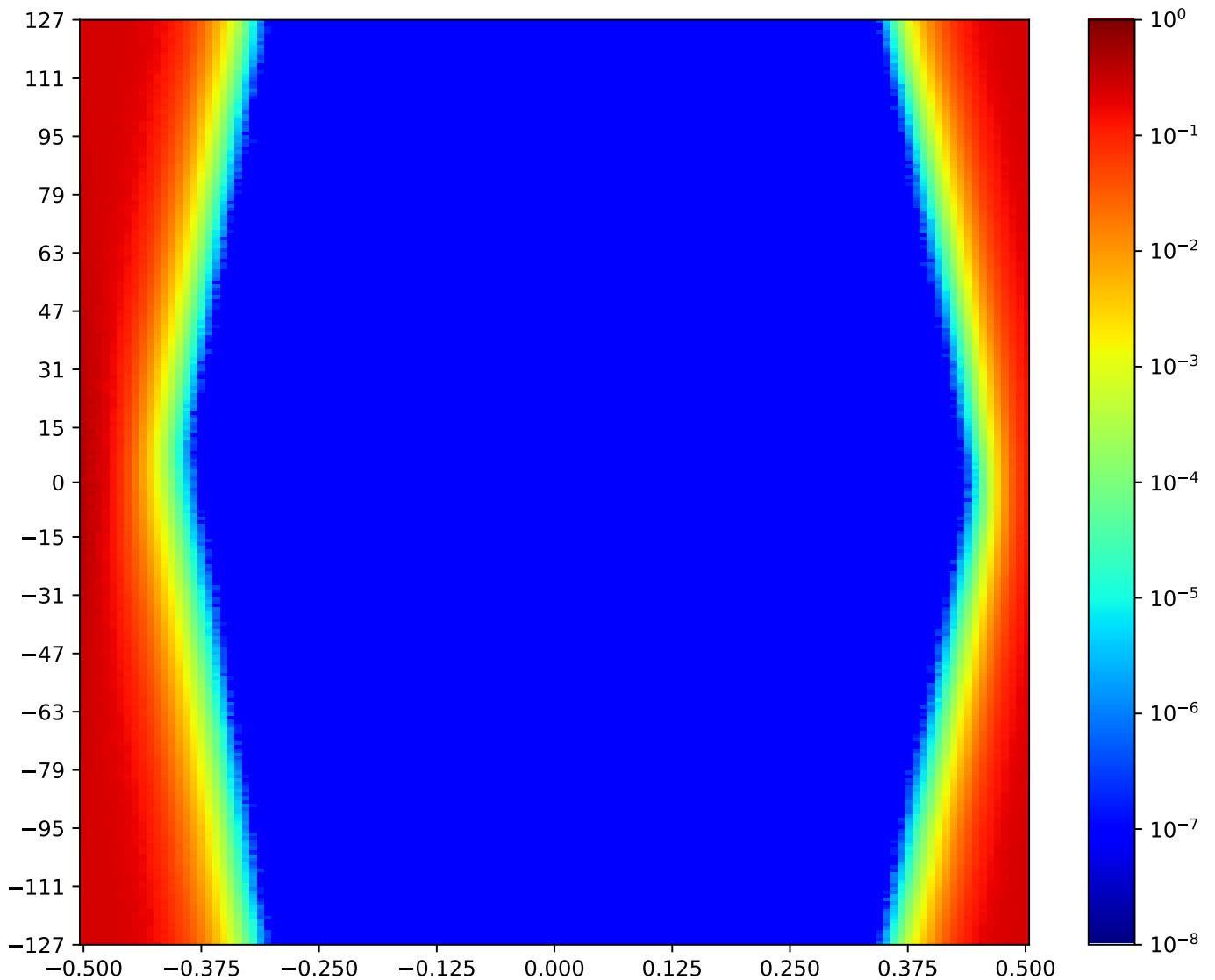


Figure 1.157: MSP\_C\_FPGA-TX3-03-RX9-03-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.5 MSP\_C\_FPGA-TX3-04-RX9-04-MSP\_A\_FPGA

Table 1.146: MSP\_C\_FPGA-TX3-04-RX9-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:06:57		2018-Jan-24 16:08:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23296	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

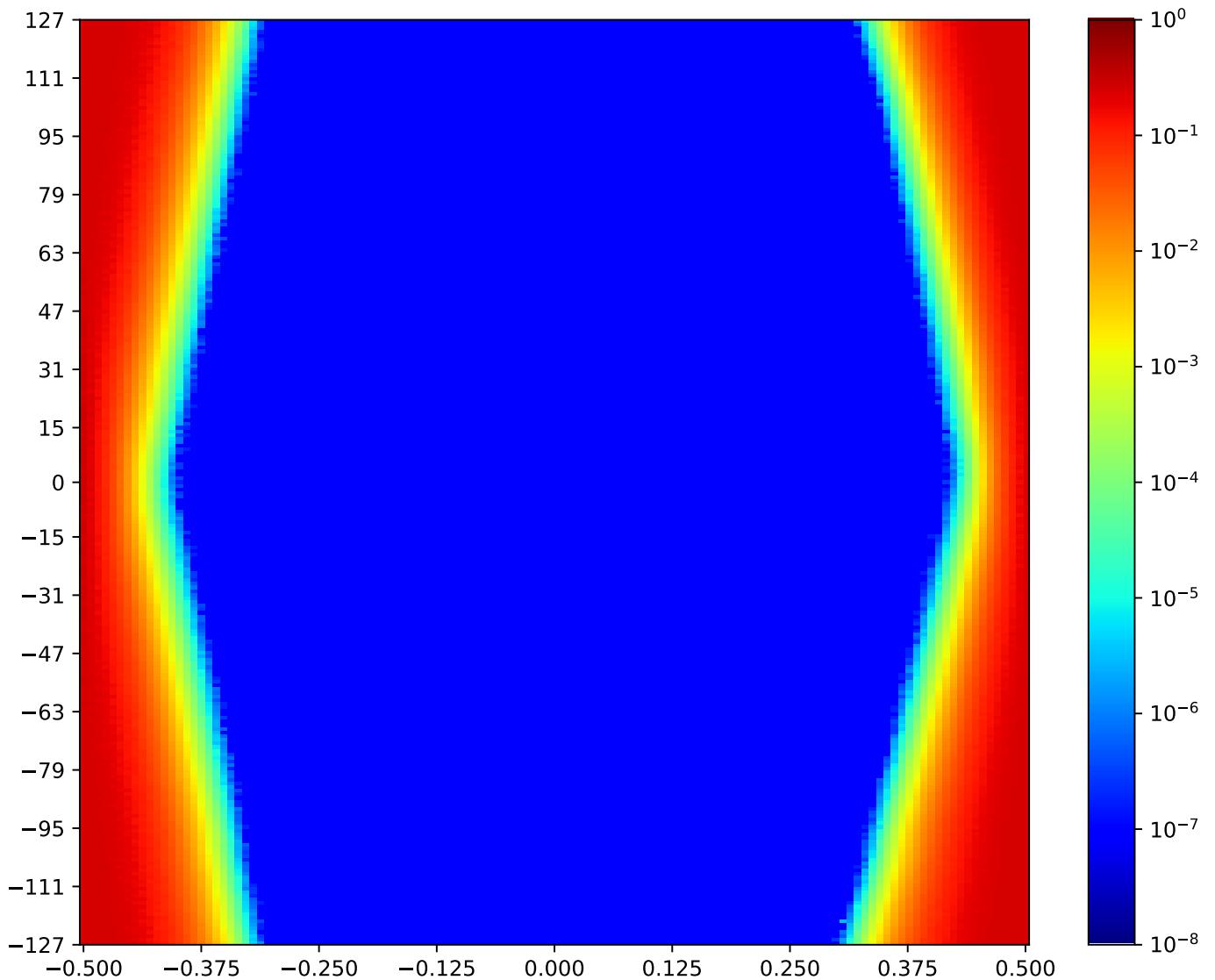


Figure 1.158: MSP\_C\_FPGA-TX3-04-RX9-04-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.6 MSP\_C\_FPGA-TX3-05-RX9-05-MSP\_A\_FPGA

Table 1.147: MSP\_C\_FPGA-TX3-05-RX9-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:56:23		2018-Jan-24 15:57:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23205	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

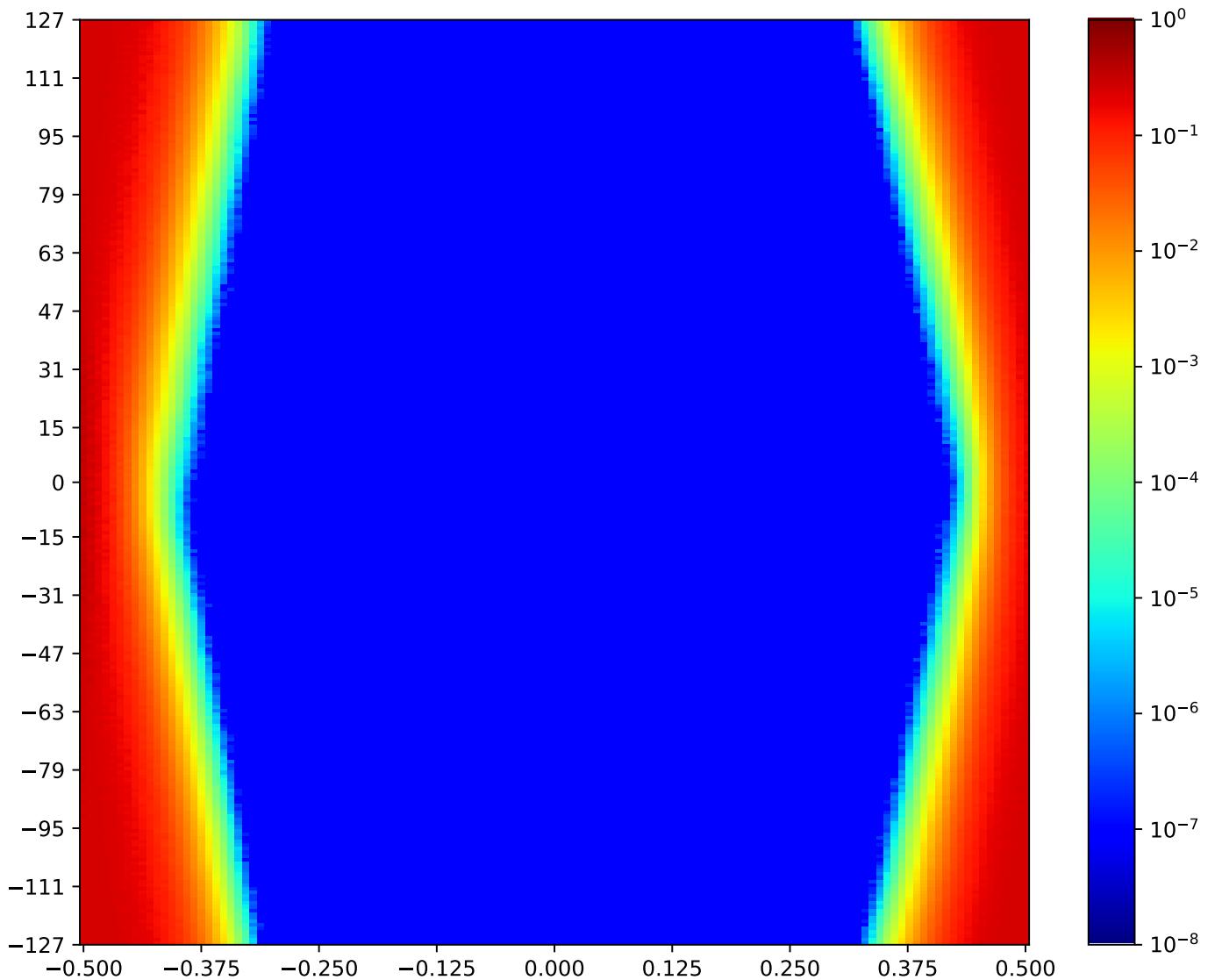


Figure 1.159: MSP\_C\_FPGA-TX3-05-RX9-05-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.7 MSP\_C\_FPGA-TX3-06-RX9-06-MSP\_A\_FPGA

Table 1.148: MSP\_C\_FPGA-TX3-06-RX9-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:09:17		2018-Jan-24 16:10:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24025	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

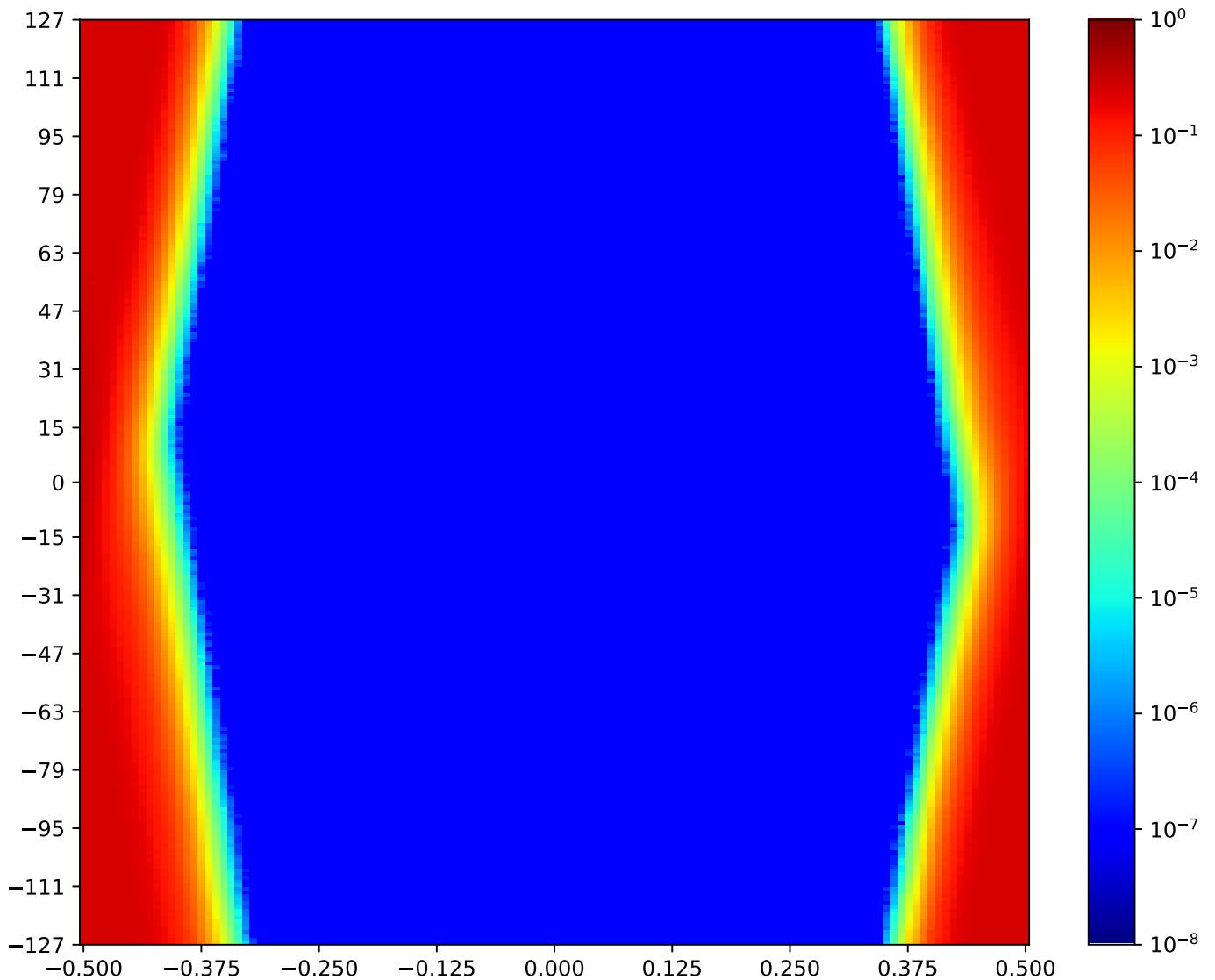


Figure 1.160: MSP\_C\_FPGA-TX3-06-RX9-06-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.8 MSP\_C\_FPGA-TX3-07-RX9-07-MSP\_A\_FPGA

Table 1.149: MSP\_C\_FPGA-TX3-07-RX9-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:58:43		2018-Jan-24 15:59:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24012	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

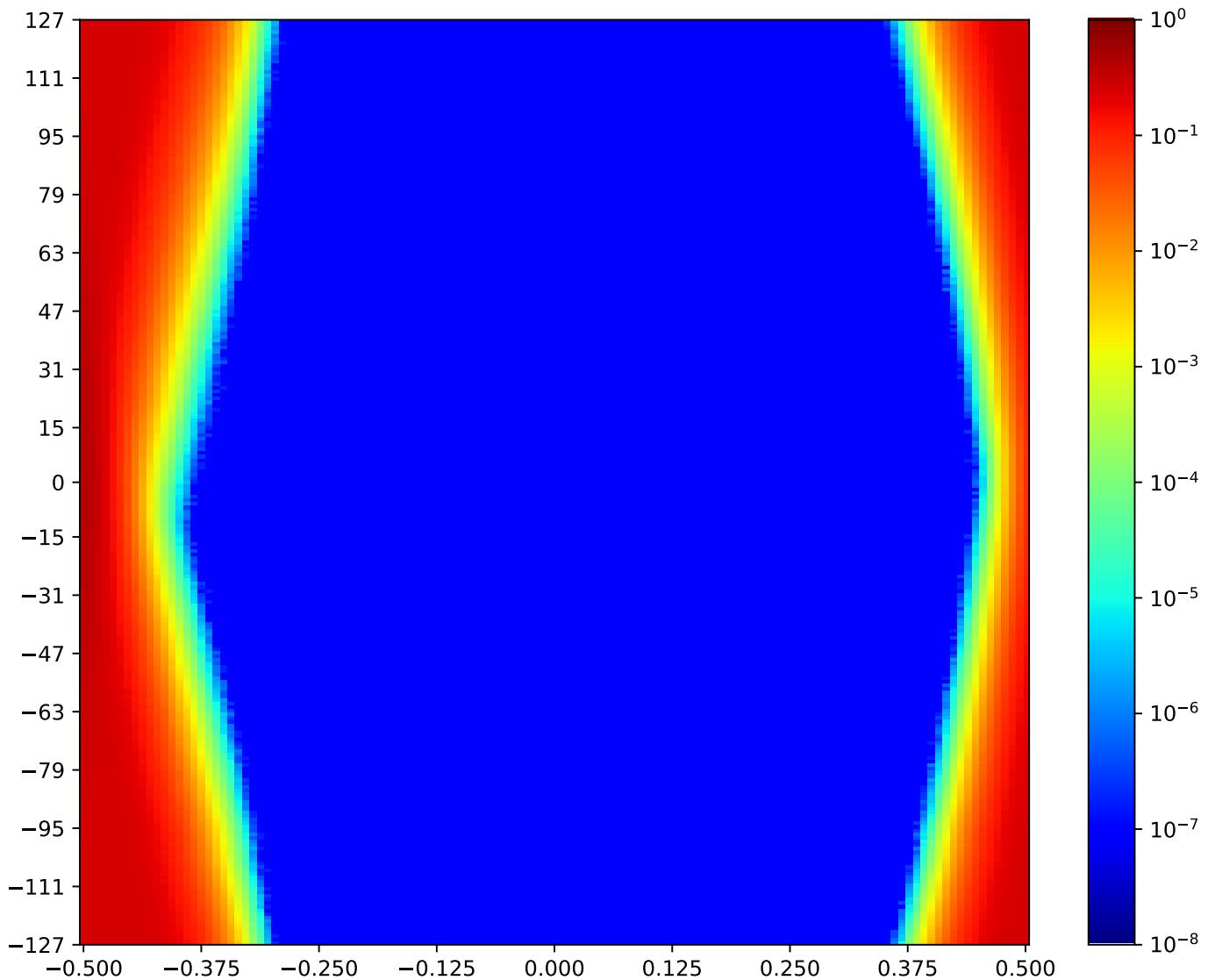


Figure 1.161: MSP\_C\_FPGA-TX3-07-RX9-07-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.9 MSP\_C\_FPGA-TX3-08-RX9-08-MSP\_A\_FPGA

Table 1.150: MSP\_C\_FPGA-TX3-08-RX9-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:08:08		2018-Jan-24 16:09:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24620	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

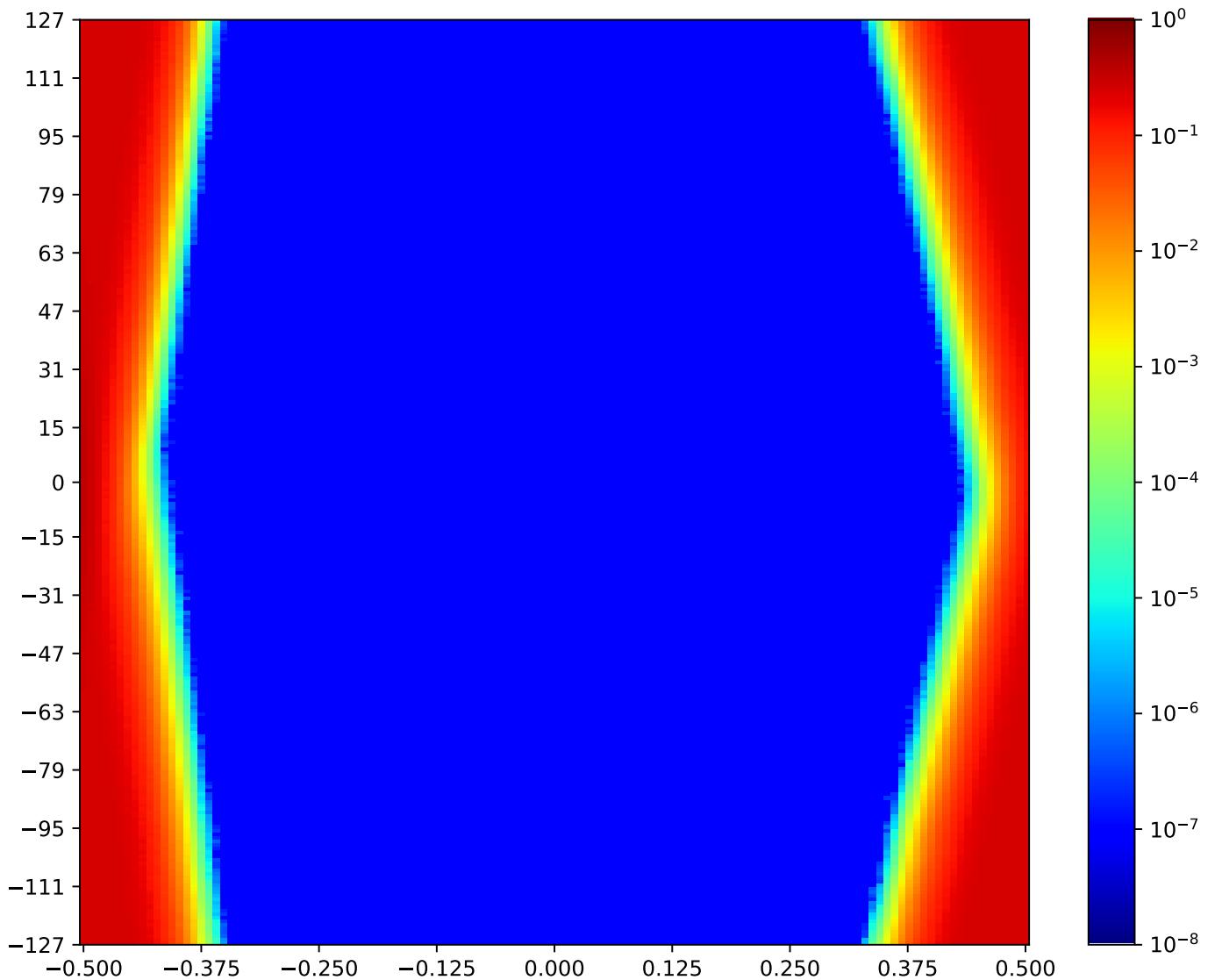


Figure 1.162: MSP\_C\_FPGA-TX3-08-RX9-08-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.10 MSP\_C\_FPGA-TX3-09-RX9-09-MSP\_A\_FPGA

Table 1.151: MSP\_C\_FPGA-TX3-09-RX9-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:01:04		2018-Jan-24 16:02:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25363	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

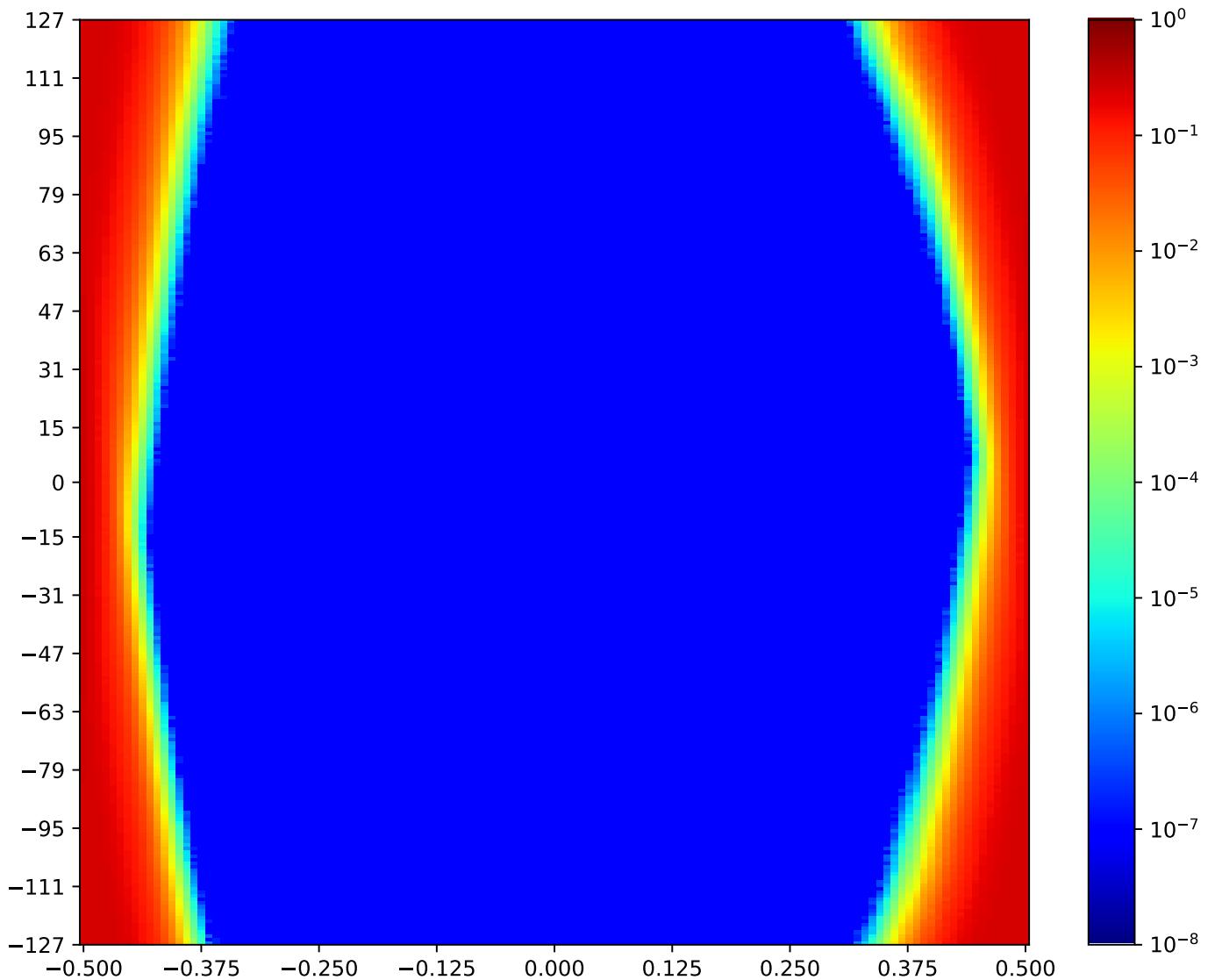


Figure 1.163: MSP\_C\_FPGA-TX3-09-RX9-09-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.11 MSP\_C\_FPGA-TX3-10-RX9-10-MSP\_A\_FPGA

Table 1.152: MSP\_C\_FPGA-TX3-10-RX9-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:05:47		2018-Jan-24 16:06:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24122	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

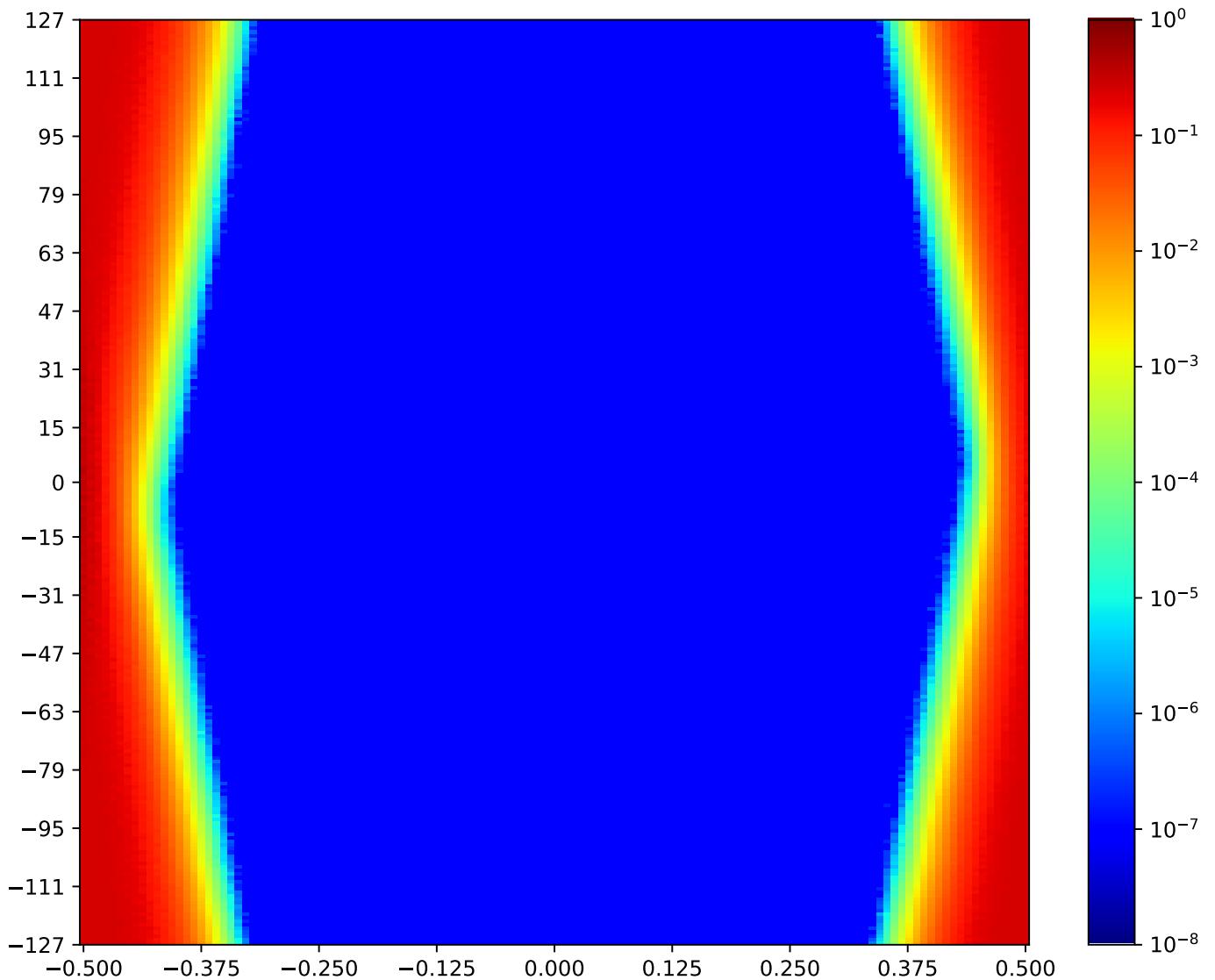


Figure 1.164: MSP\_C\_FPGA-TX3-10-RX9-10-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.12.12 MSP\_C\_FPGA-TX3-11-RX9-11-MSP\_A\_FPGA

Table 1.153: MSP\_C\_FPGA-TX3-11-RX9-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:04:36		2018-Jan-24 16:05:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24800	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

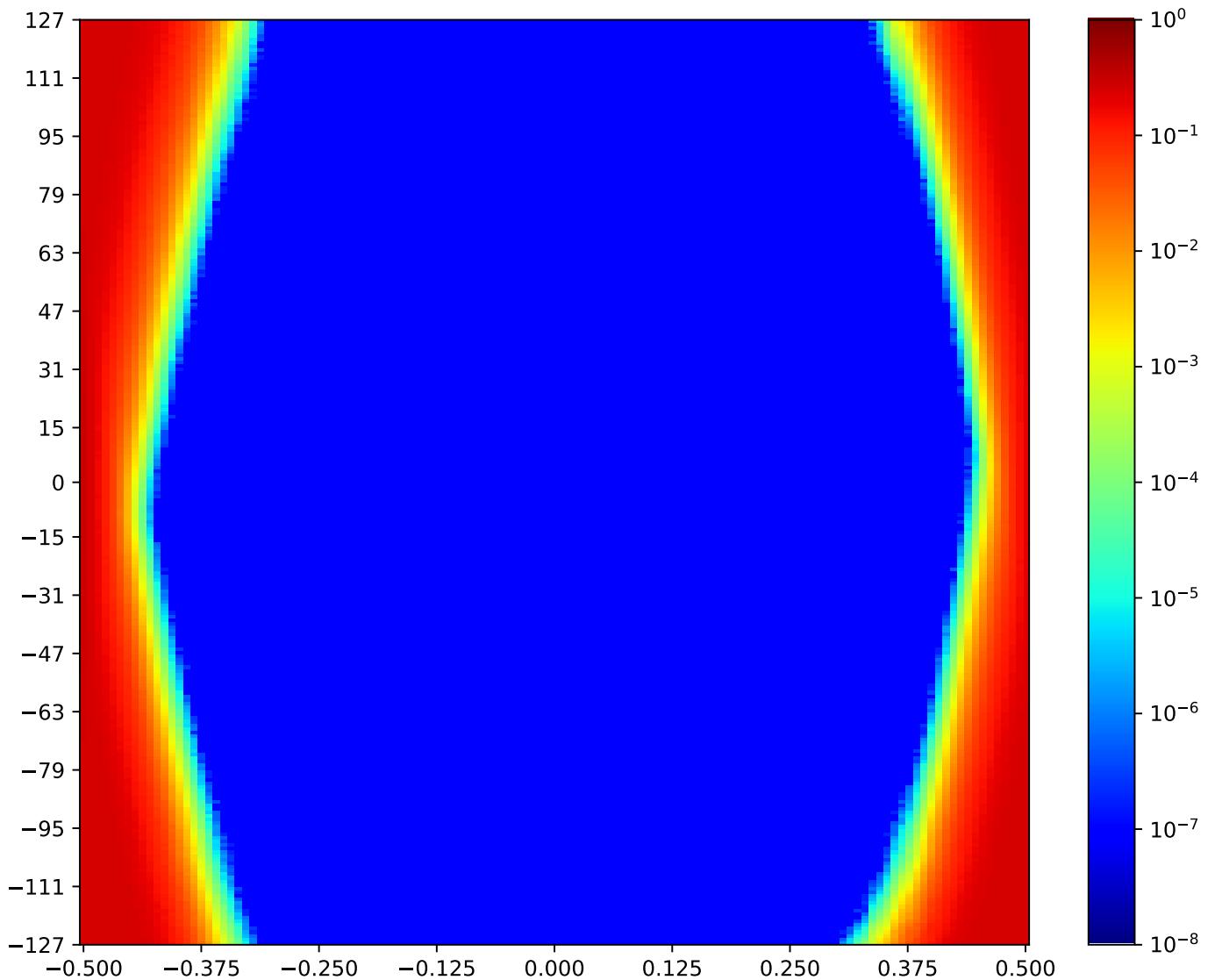


Figure 1.165: MSP\_C\_FPGA-TX3-11-RX9-11-MSP\_A\_FPGA

Call back to summary Figure 1.153. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.13 MSP\_C TX4 MSP\_A RX8 Minipod Loopback

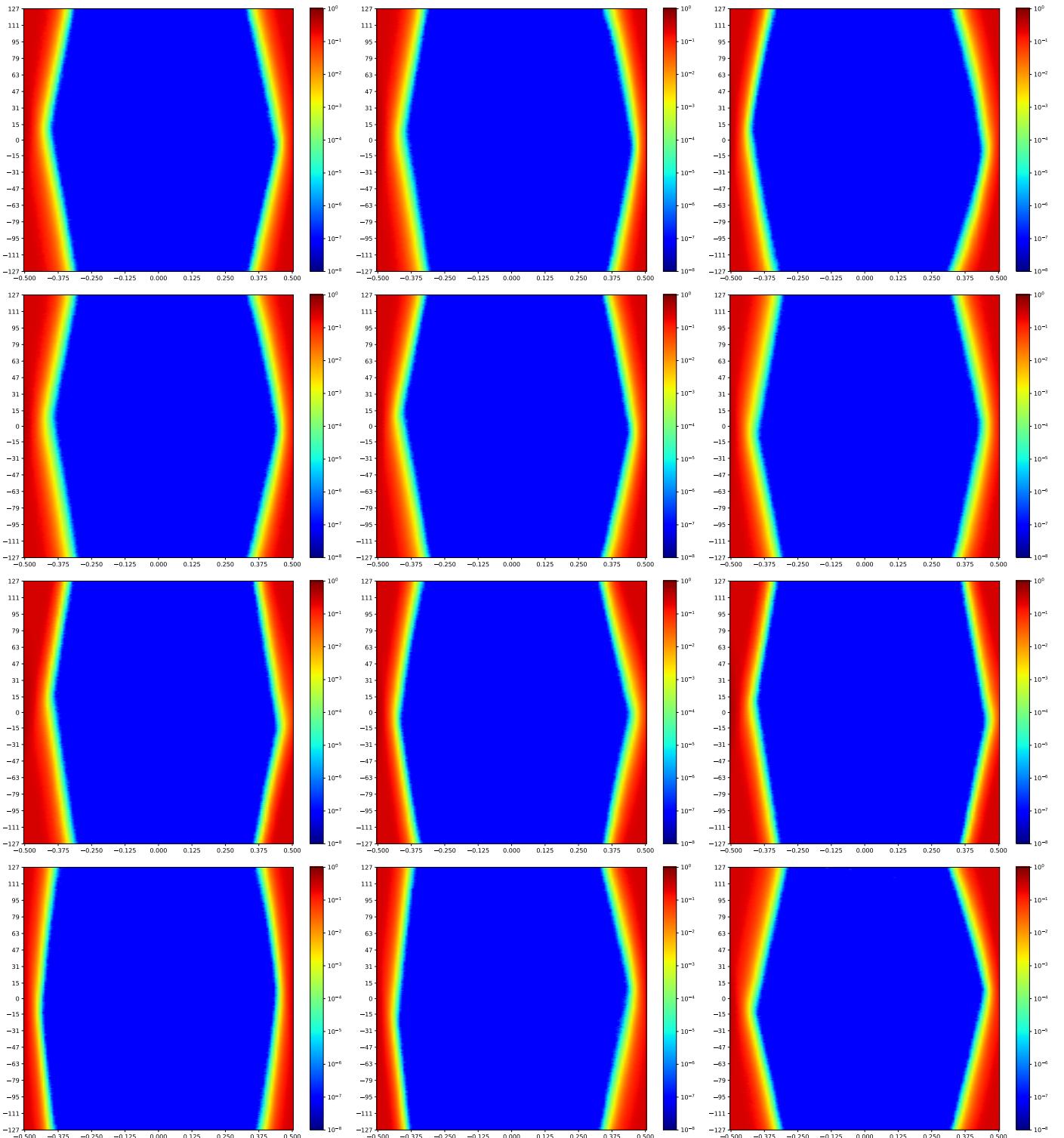


Figure 1.166: MSP\_C TX4 MSP\_A RX8 Minipod Loopback

A cross-reference to Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.179.

### 1.13.1 MSP\_C\_FPGA-TX4-00-RX8-00-MSP\_A\_FPGA

Table 1.154: MSP\_C\_FPGA-TX4-00-RX8-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:13:55		2018-Jan-24 16:15:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23614	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

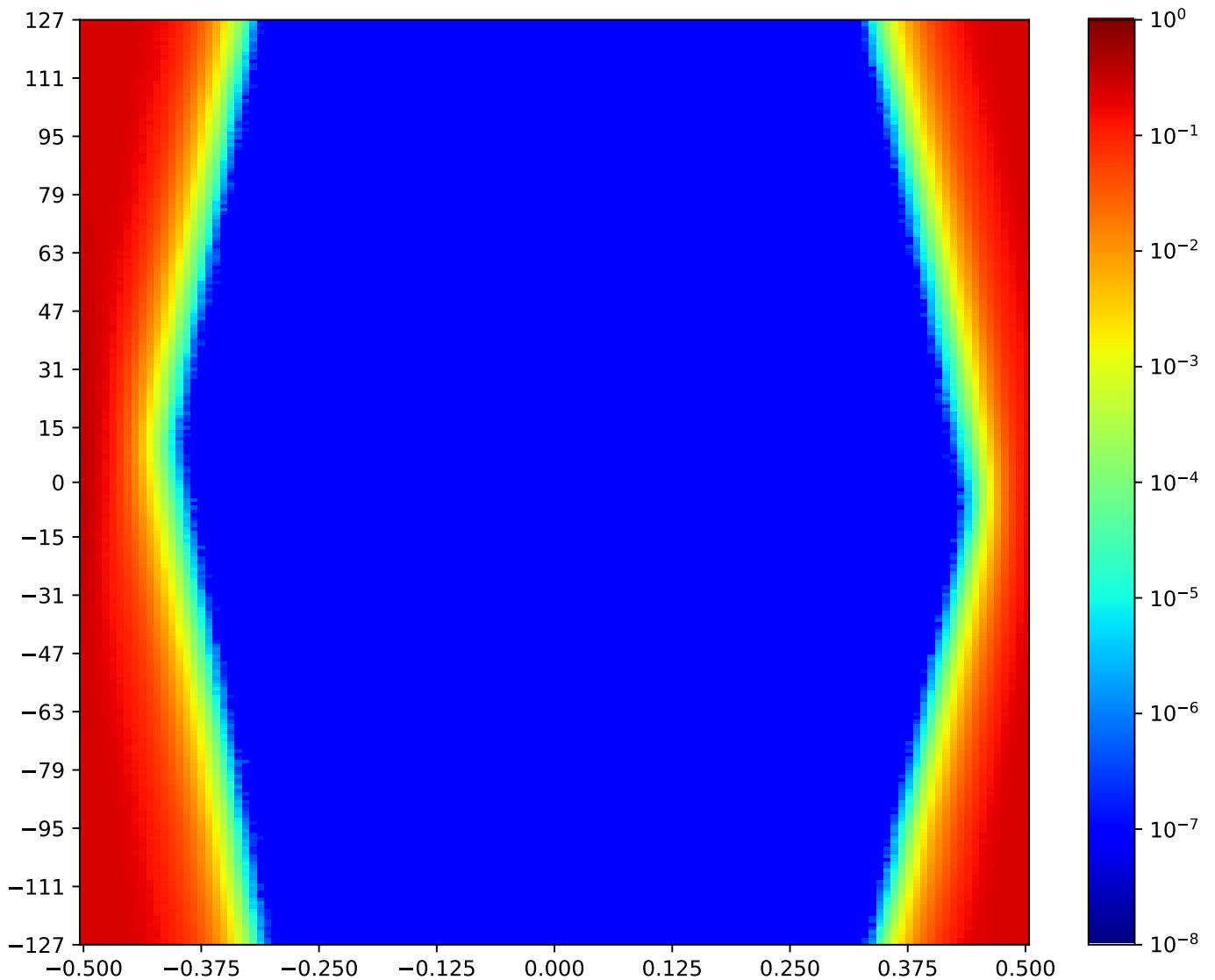


Figure 1.167: MSP\_C\_FPGA-TX4-00-RX8-00-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.2 MSP\_C\_FPGA-TX4-01-RX8-01-MSP\_A\_FPGA

Table 1.155: MSP\_C\_FPGA-TX4-01-RX8-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:11:36		2018-Jan-24 16:12:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23971	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

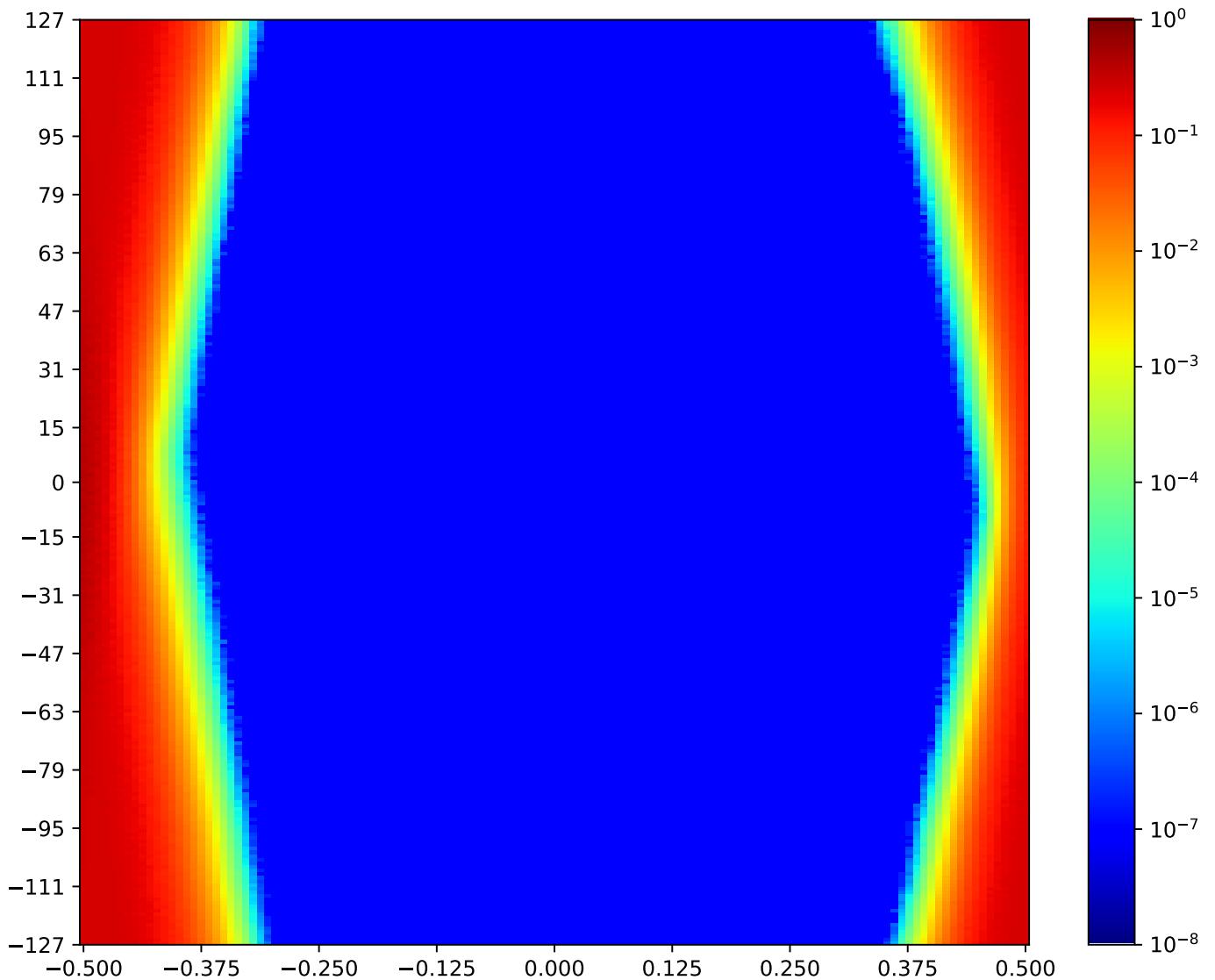


Figure 1.168: MSP\_C\_FPGA-TX4-01-RX8-01-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.3 MSP\_C\_FPGA-TX4-02-RX8-02-MSP\_A\_FPGA

Table 1.156: MSP\_C\_FPGA-TX4-02-RX8-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:17:28		2018-Jan-24 16:18:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24149	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

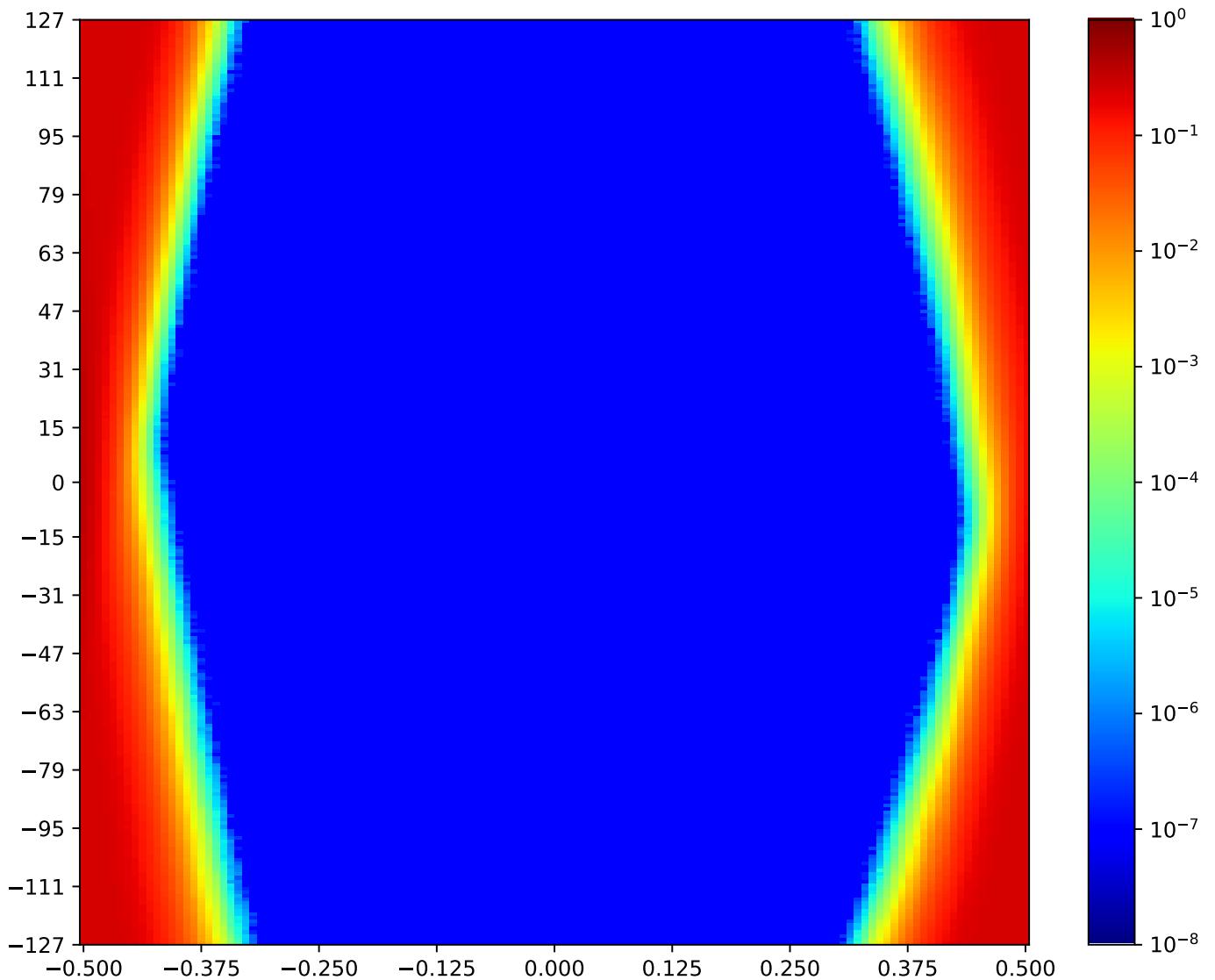


Figure 1.169: MSP\_C\_FPGA-TX4-02-RX8-02-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.13.4 MSP\_C\_FPGA-TX4-03-RX8-03-MSP\_A\_FPGA

Table 1.157: MSP\_C\_FPGA-TX4-03-RX8-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:10:27		2018-Jan-24 16:11:36	
Reset RX	OA	HO		HO (%)	
true	23407	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

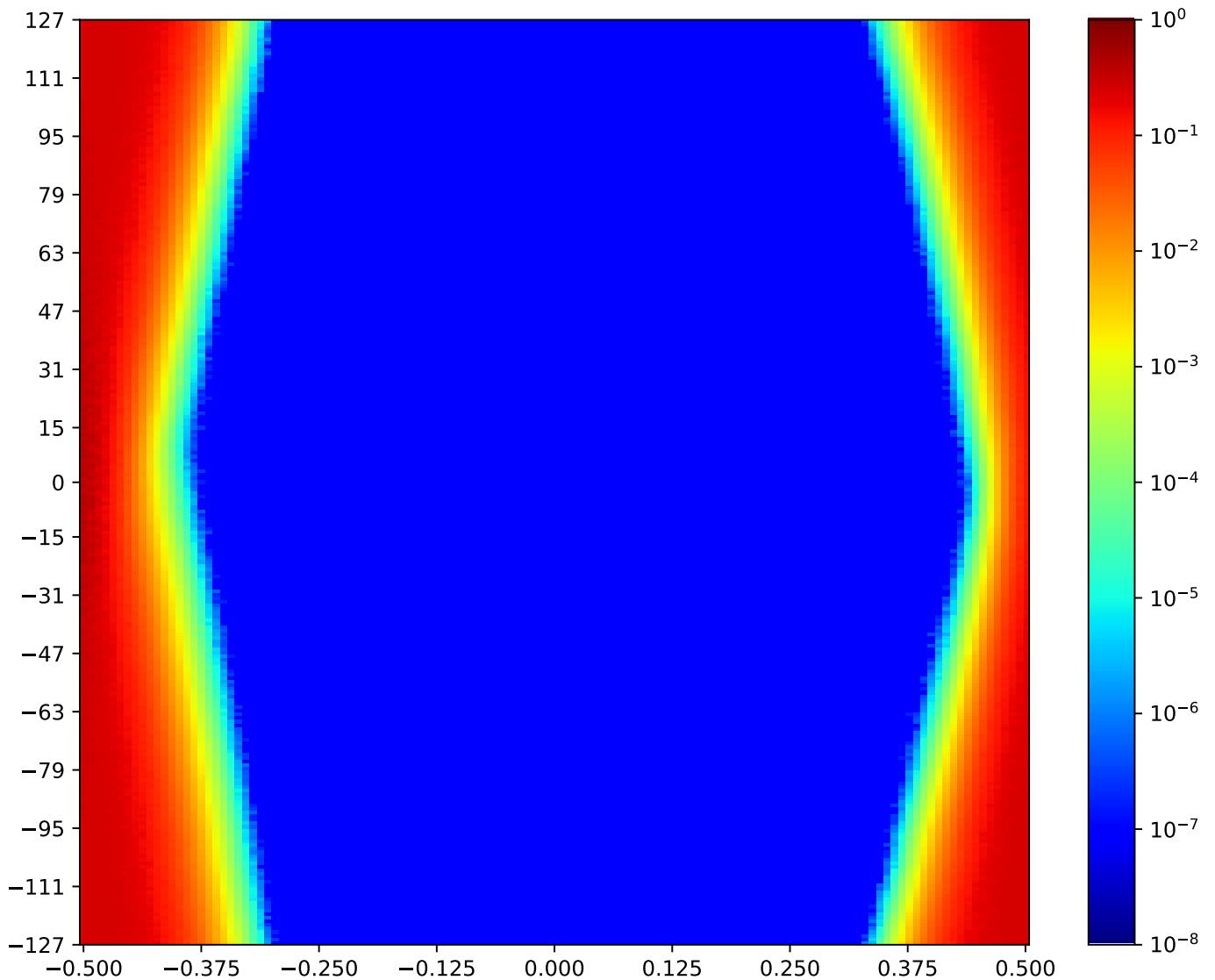


Figure 1.170: MSP\_C\_FPGA-TX4-03-RX8-03-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.5 MSP\_C\_FPGA-TX4-04-RX8-04-MSP\_A\_FPGA

Table 1.158: MSP\_C\_FPGA-TX4-04-RX8-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:20:59		2018-Jan-24 16:22:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23756	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

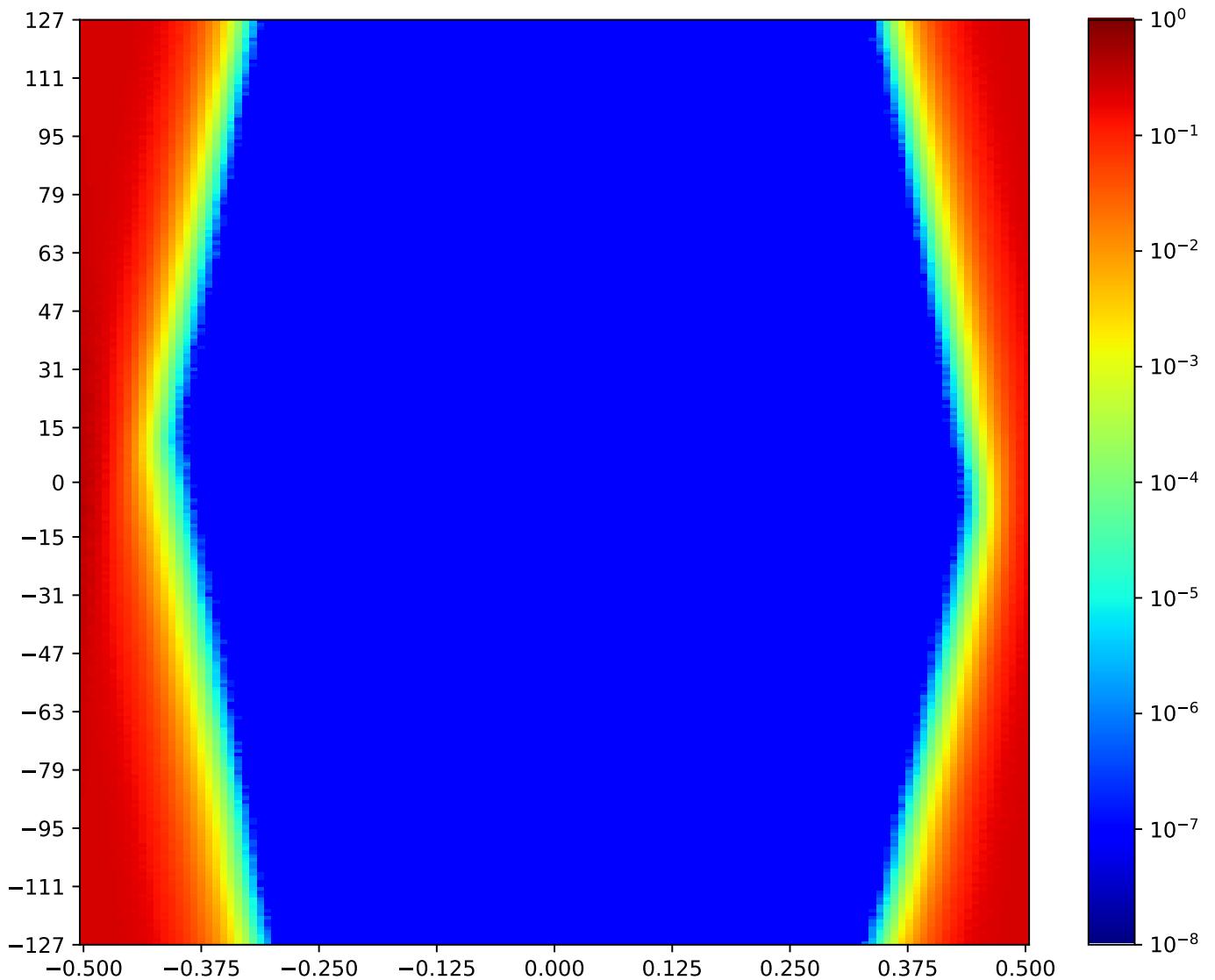


Figure 1.171: MSP\_C\_FPGA-TX4-04-RX8-04-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.6 MSP\_C\_FPGA-TX4-05-RX8-05-MSP\_A\_FPGA

Table 1.159: MSP\_C\_FPGA-TX4-05-RX8-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:12:46		2018-Jan-24 16:13:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23153	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

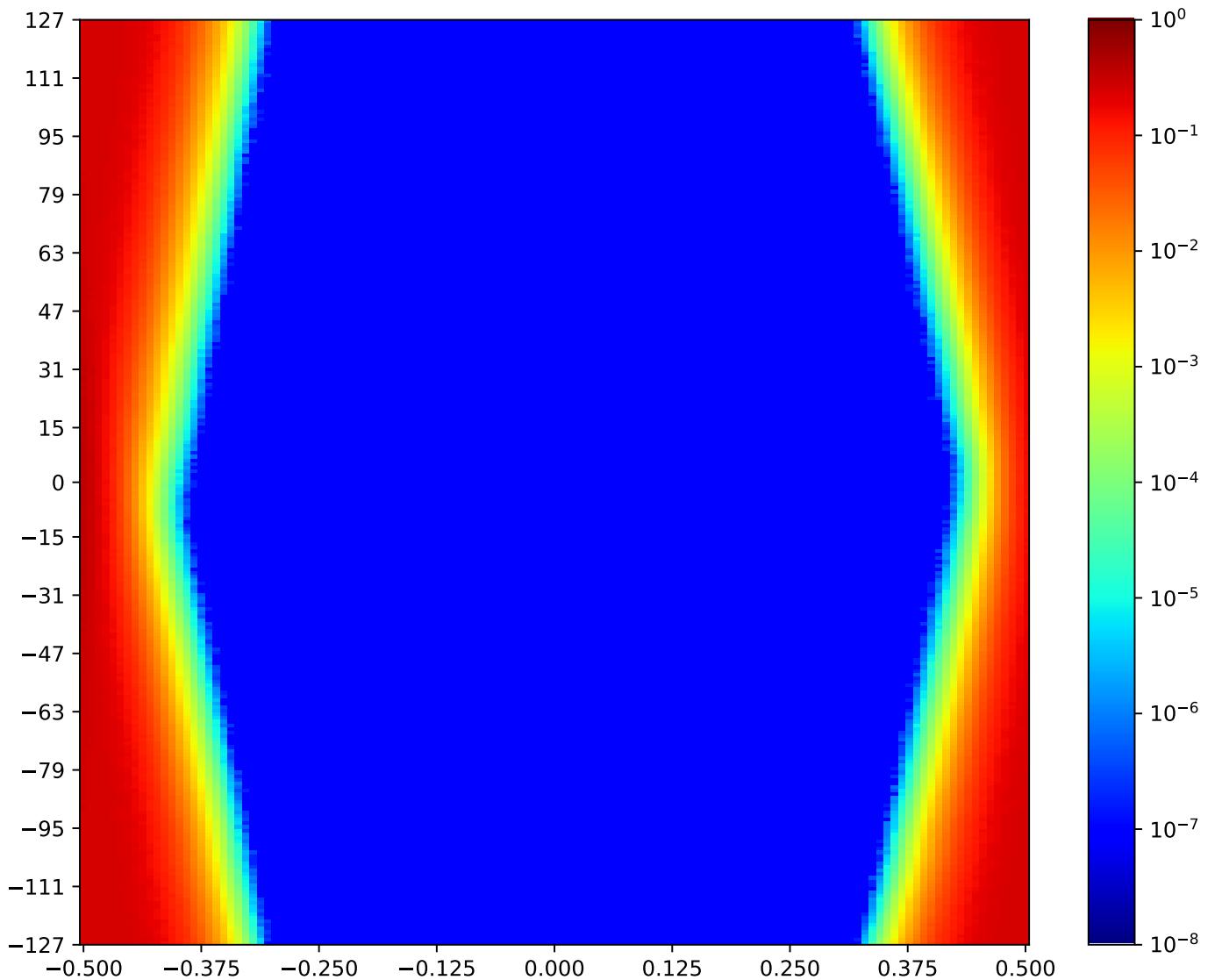


Figure 1.172: MSP\_C\_FPGA-TX4-05-RX8-05-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.7 MSP\_C\_FPGA-TX4-06-RX8-06-MSP\_A\_FPGA

Table 1.160: MSP\_C\_FPGA-TX4-06-RX8-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:23:20		2018-Jan-24 16:24:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23919	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

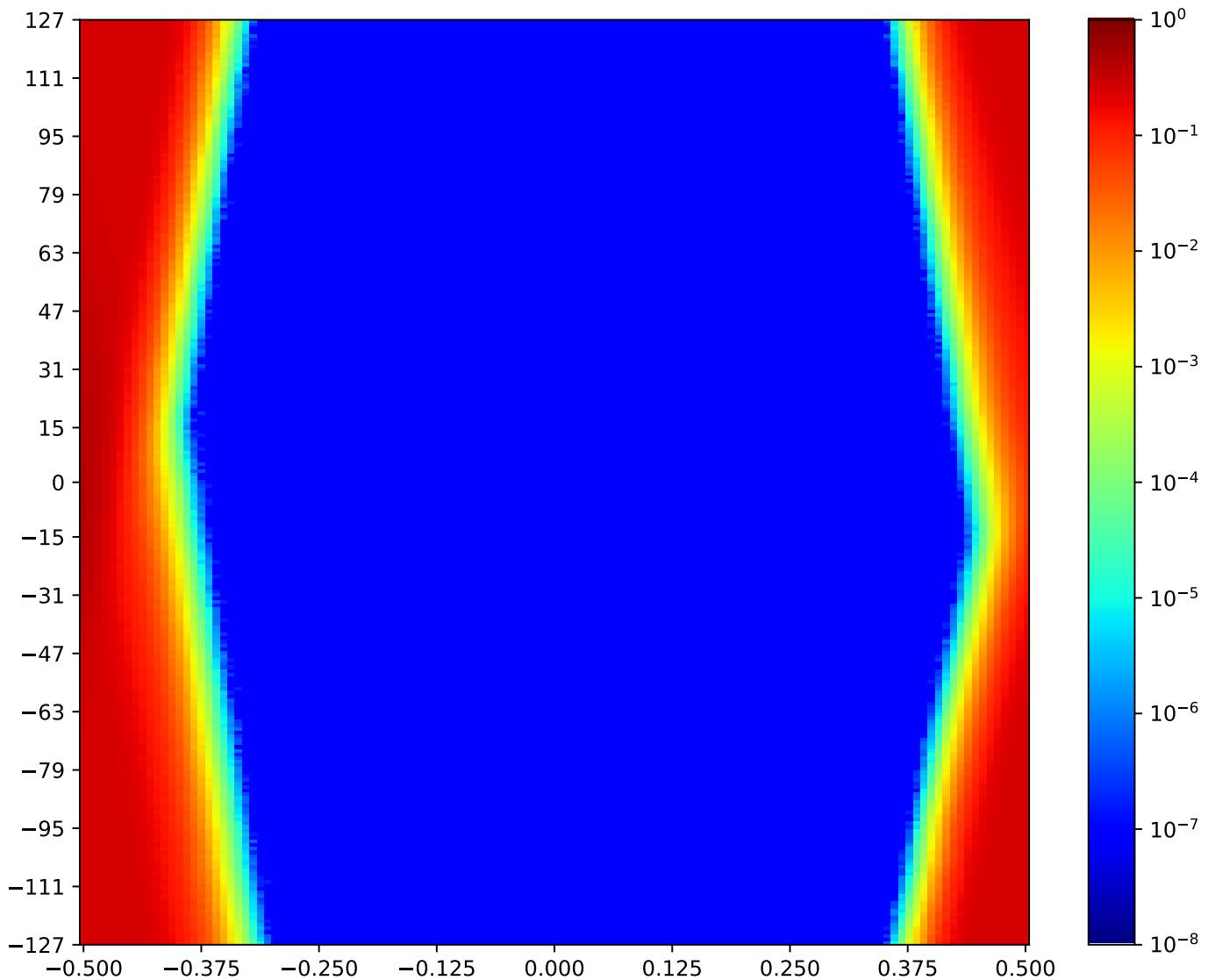


Figure 1.173: MSP\_C\_FPGA-TX4-06-RX8-06-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.8 MSP\_C\_FPGA-TX4-07-RX8-07-MSP\_A\_FPGA

Table 1.161: MSP\_C\_FPGA-TX4-07-RX8-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:15:05		2018-Jan-24 16:16:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24251	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

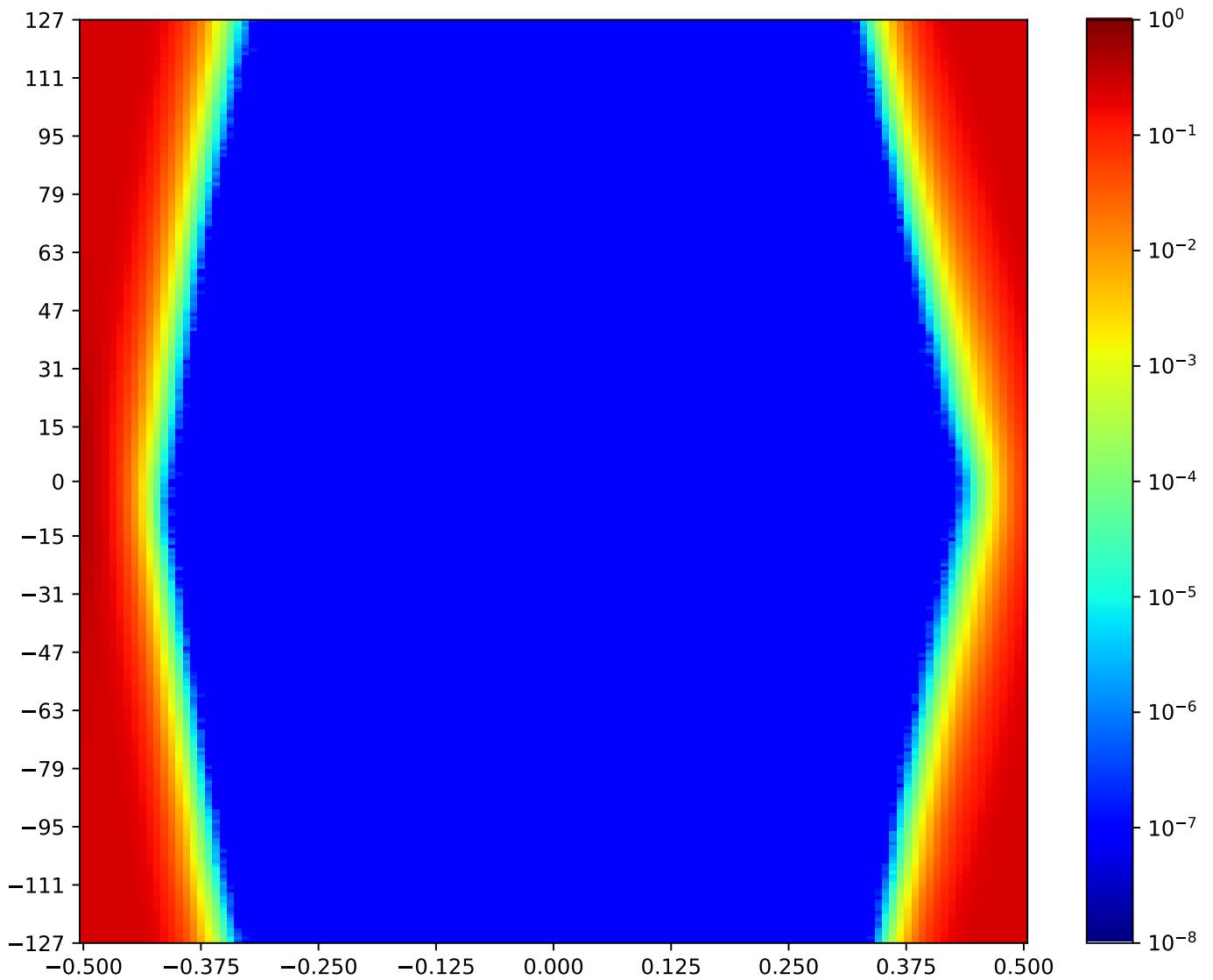


Figure 1.174: MSP\_C\_FPGA-TX4-07-RX8-07-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.9 MSP\_C\_FPGA-TX4-08-RX8-08-MSP\_A\_FPGA

Table 1.162: MSP\_C\_FPGA-TX4-08-RX8-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:22:10		2018-Jan-24 16:23:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24374	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

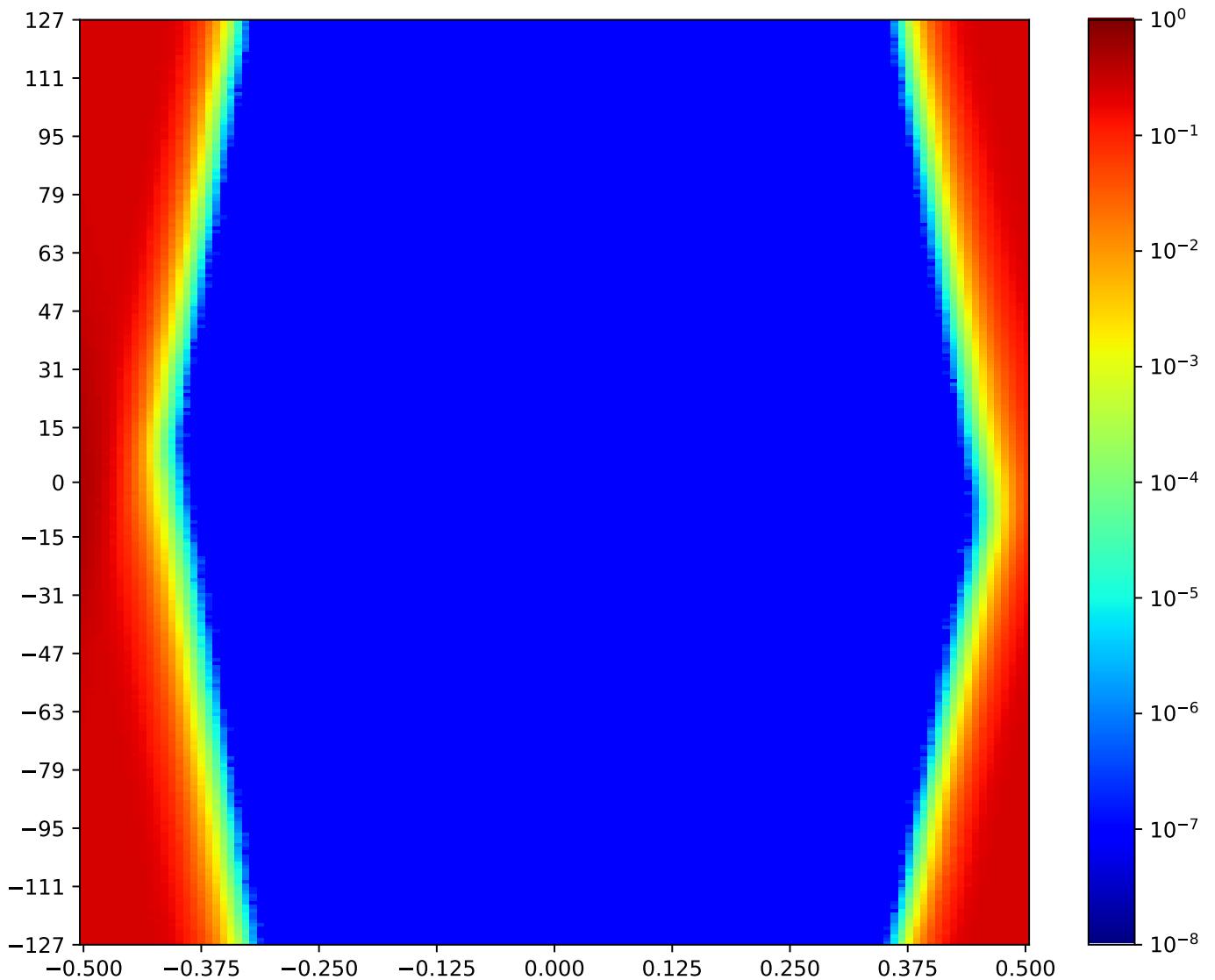


Figure 1.175: MSP\_C\_FPGA-TX4-08-RX8-08-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.10 MSP\_C\_FPGA-TX4-09-RX8-09-MSP\_A\_FPGA

Table 1.163: MSP\_C\_FPGA-TX4-09-RX8-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:16:15		2018-Jan-24 16:17:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26067	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

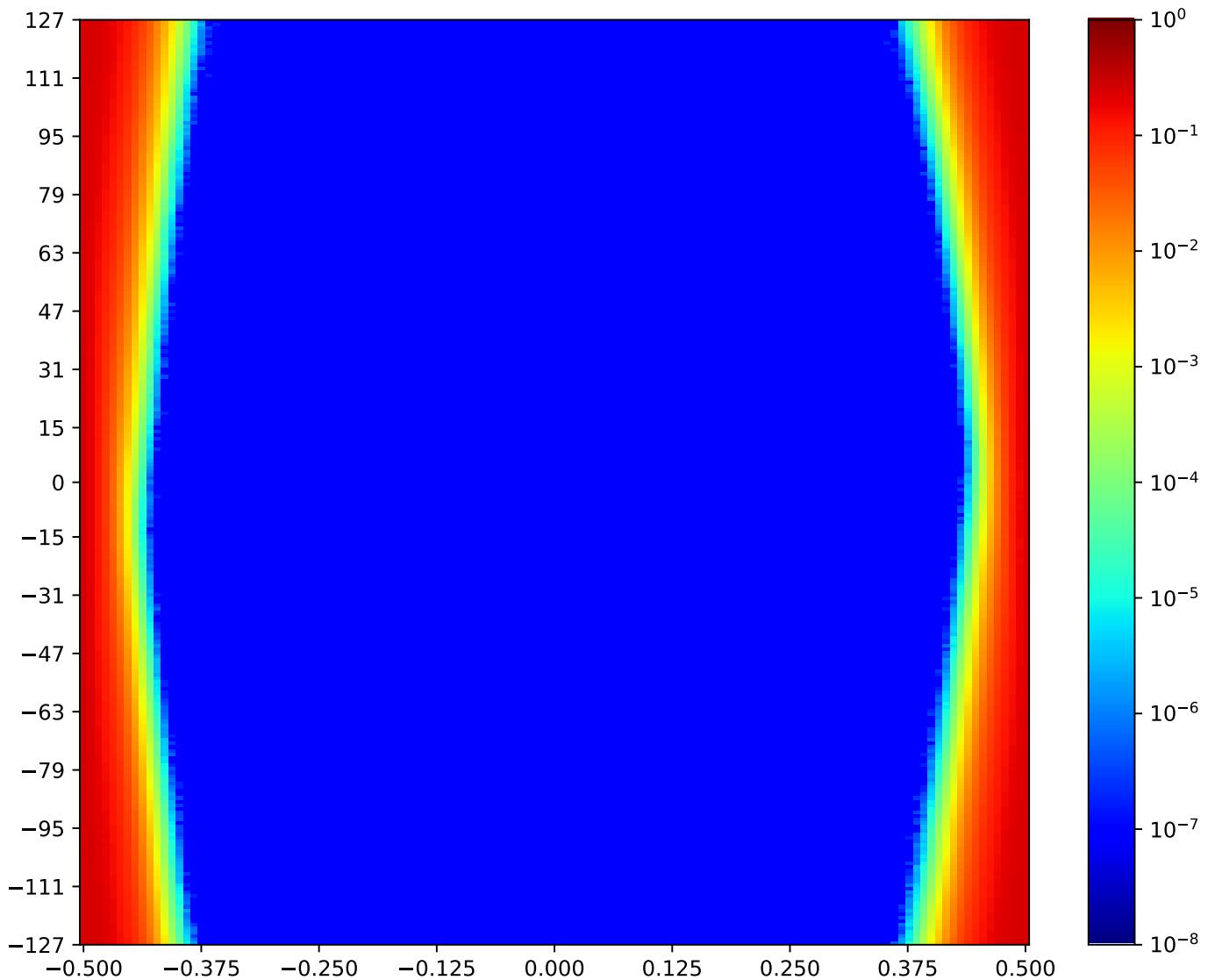


Figure 1.176: MSP\_C\_FPGA-TX4-09-RX8-09-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.11 MSP\_C\_FPGA-TX4-10-RX8-10-MSP\_A\_FPGA

Table 1.164: MSP\_C\_FPGA-TX4-10-RX8-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:19:47		2018-Jan-24 16:20:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24853	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

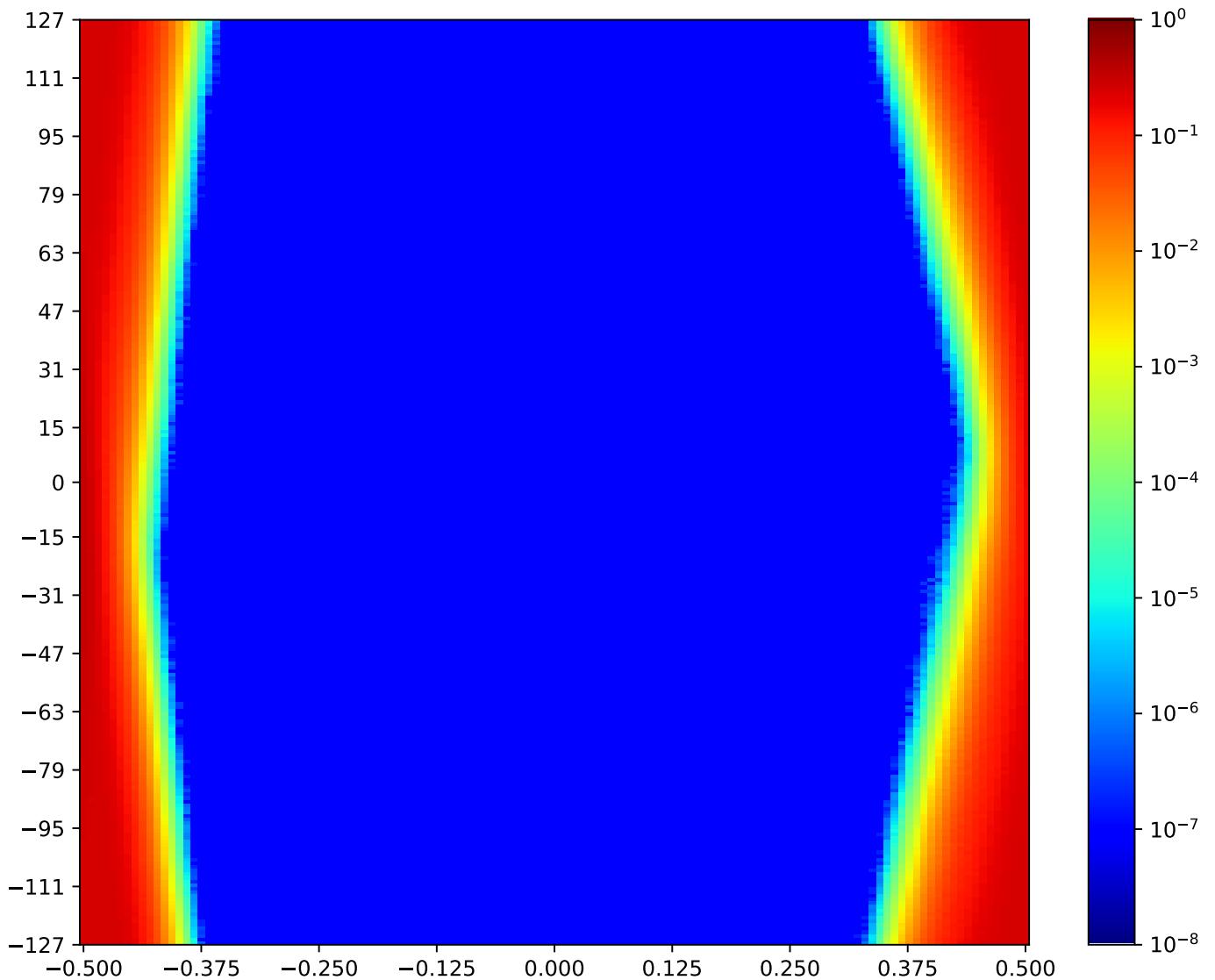


Figure 1.177: MSP\_C\_FPGA-TX4-10-RX8-10-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.13.12 MSP\_C\_FPGA-TX4-11-RX8-11-MSP\_A\_FPGA

Table 1.165: MSP\_C\_FPGA-TX4-11-RX8-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:18:39		2018-Jan-24 16:19:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23351	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

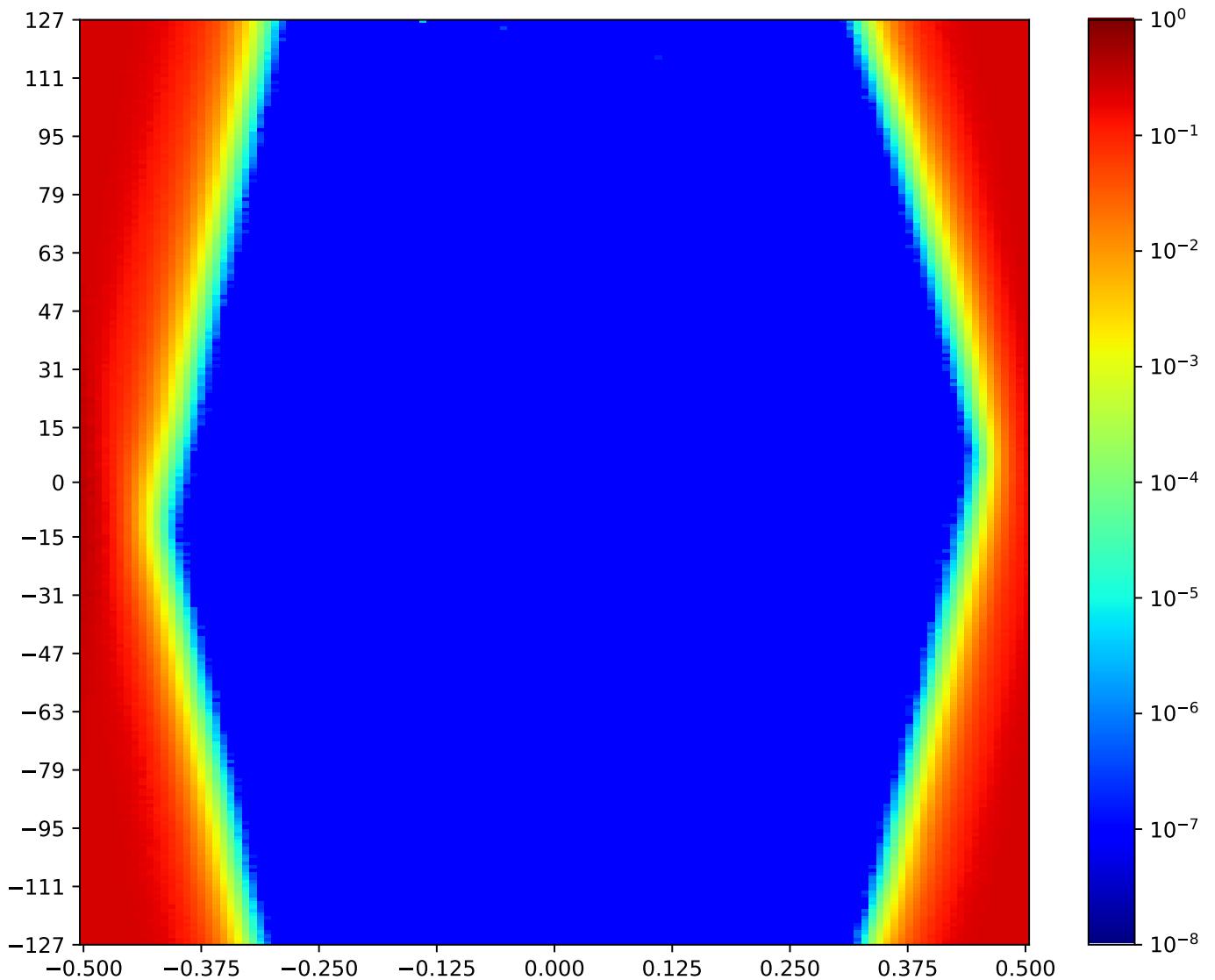


Figure 1.178: MSP\_C\_FPGA-TX4-11-RX8-11-MSP\_A\_FPGA

Call back to summary Figure 1.166. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## **1.14 Partial TRP TX5 MSP\_C RX14 Minipod Loopback**

A cross-reference to Figure 1.179. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.188.

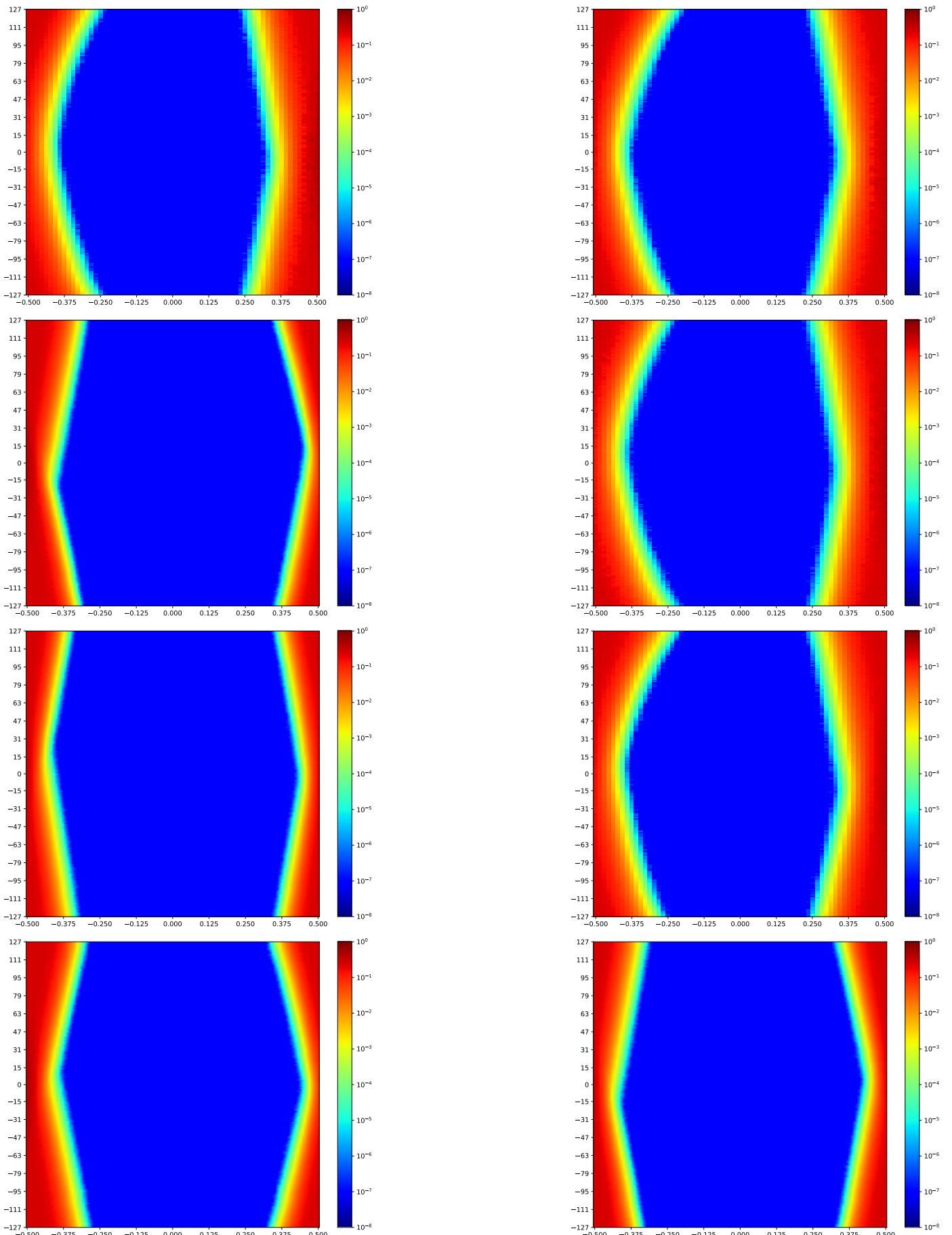


Figure 1.179: Partial TRP TX5 MSP\_C RX14 Minipod Loopback

### 1.14.1 TRP\_FPGA-TX5-00-RX14-00-MSP\_C\_FPGA

Table 1.166: TRP\_FPGA-TX5-00-RX14-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:26:20		2018-Jan-24 16:26:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9606	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

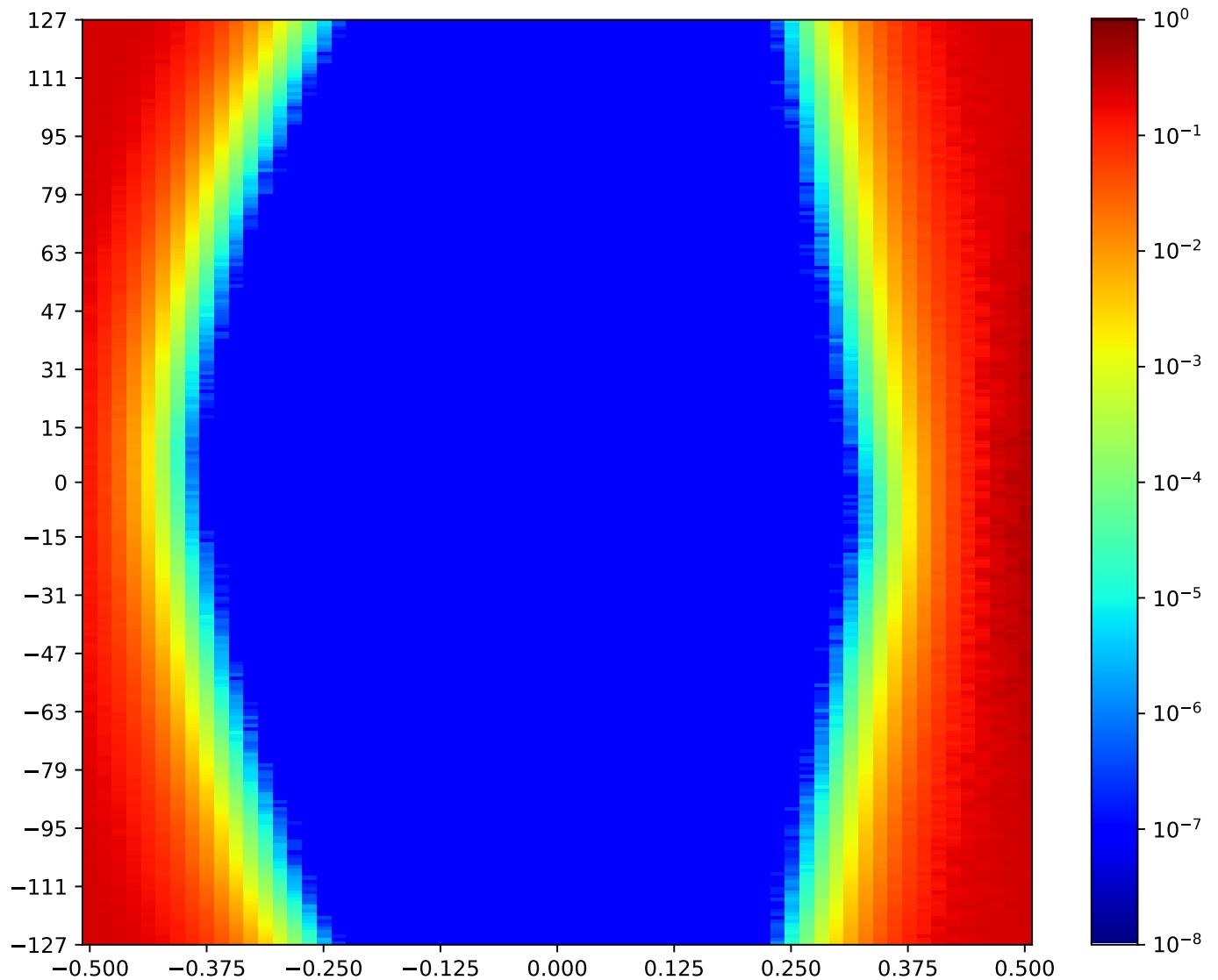


Figure 1.180: TRP\_FPGA-TX5-00-RX14-00-MSP\_C\_FPGA

Call back to summary Figure 1.179. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.14.2 TRP\_FPGA-TX5-01-RX14-01-MSP\_C\_FPGA

Table 1.167: TRP\_FPGA-TX5-01-RX14-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:25:06		2018-Jan-24 16:25:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9161	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

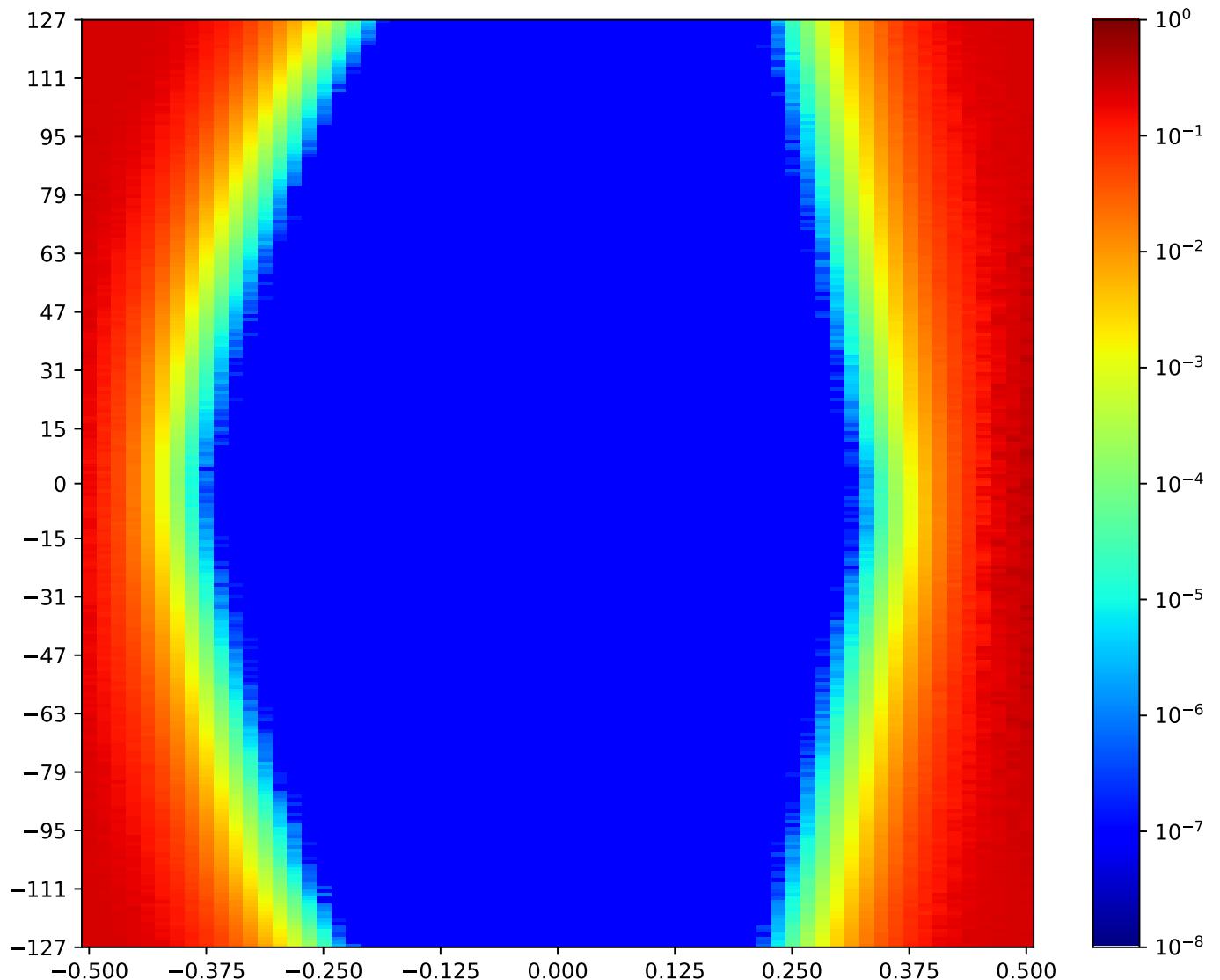


Figure 1.181: TRP\_FPGA-TX5-01-RX14-01-MSP\_C\_FPGA

Call back to summary Figure 1.179. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.14.3 TRP\_FPGA-TX5-02-RX14-02-MSP\_C\_FPGA

Table 1.168: TRP\_FPGA-TX5-02-RX14-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:28:05		2018-Jan-24 16:29:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23674	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

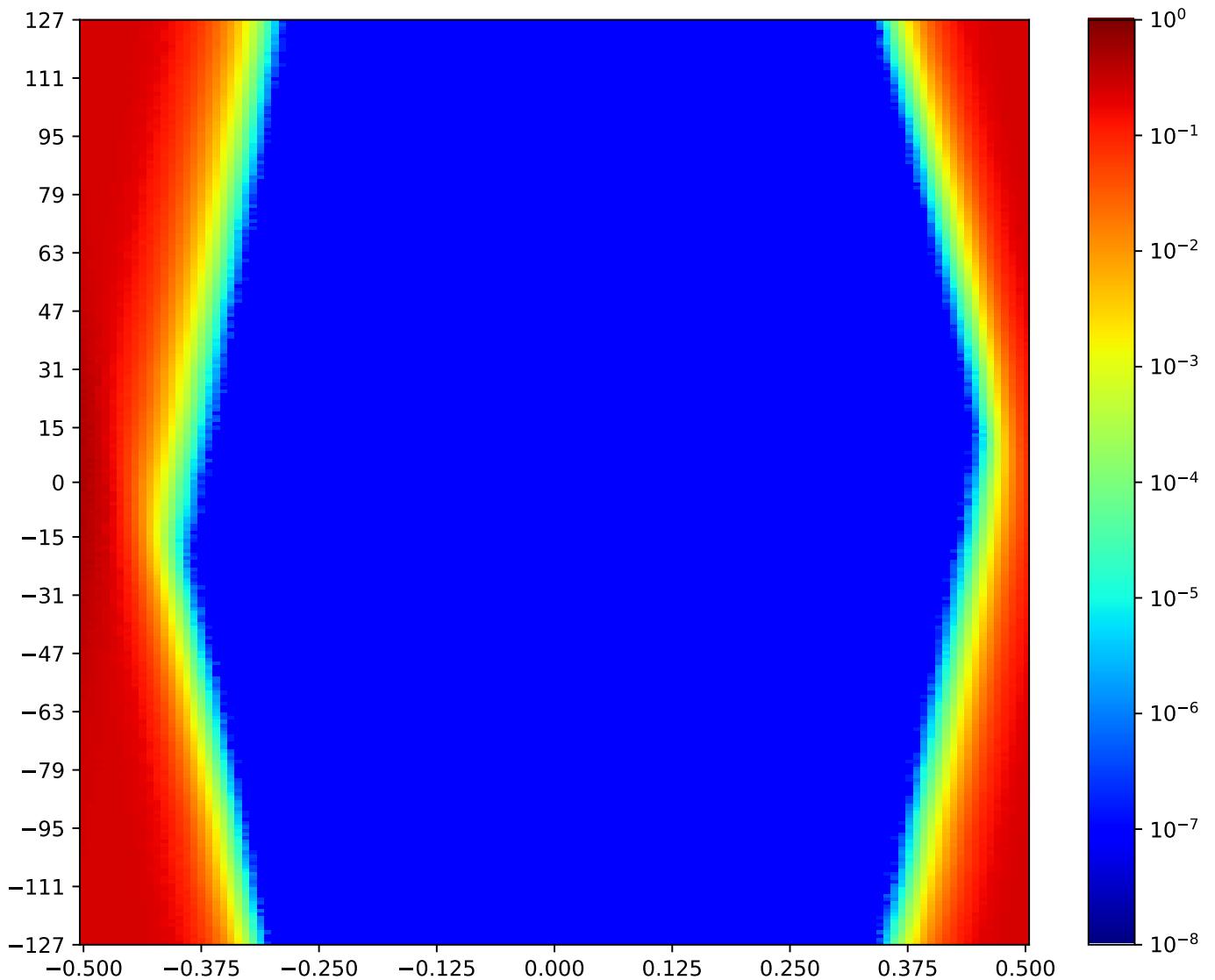


Figure 1.182: TRP\_FPGA-TX5-02-RX14-02-MSP\_C\_FPGA

Call back to summary Figure 1.179. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.14.4 TRP\_FPGA-TX5-03-RX14-03-MSP\_C\_FPGA

Table 1.169: TRP\_FPGA-TX5-03-RX14-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:25:43		2018-Jan-24 16:26:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9248	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

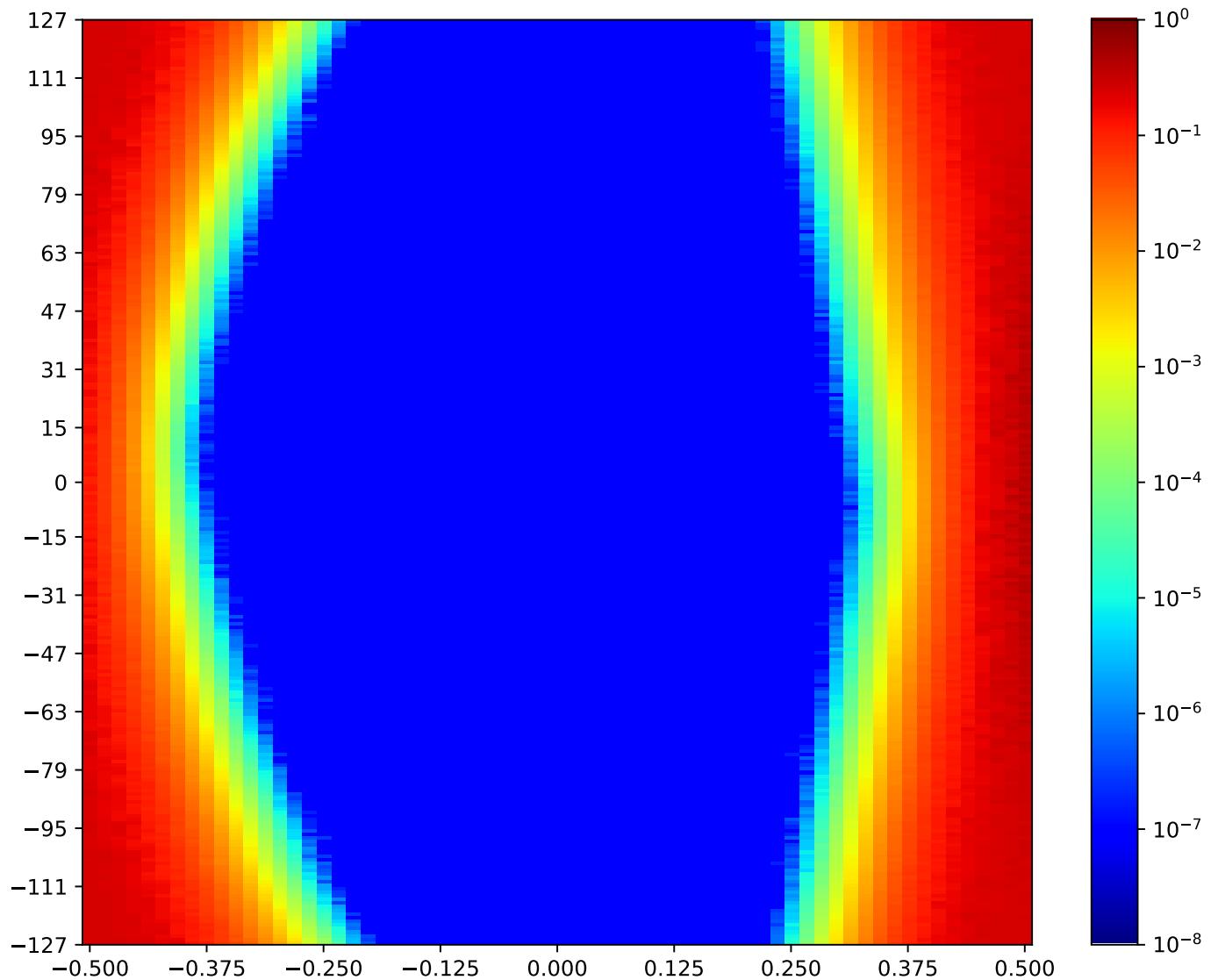


Figure 1.183: TRP\_FPGA-TX5-03-RX14-03-MSP\_C\_FPGA

Call back to summary Figure 1.179. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.14.5 TRP\_FPGA-TX5-04-RX14-04-MSP\_C\_FPGA

Table 1.170: TRP\_FPGA-TX5-04-RX14-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:30:24		2018-Jan-24 16:31:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24092	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

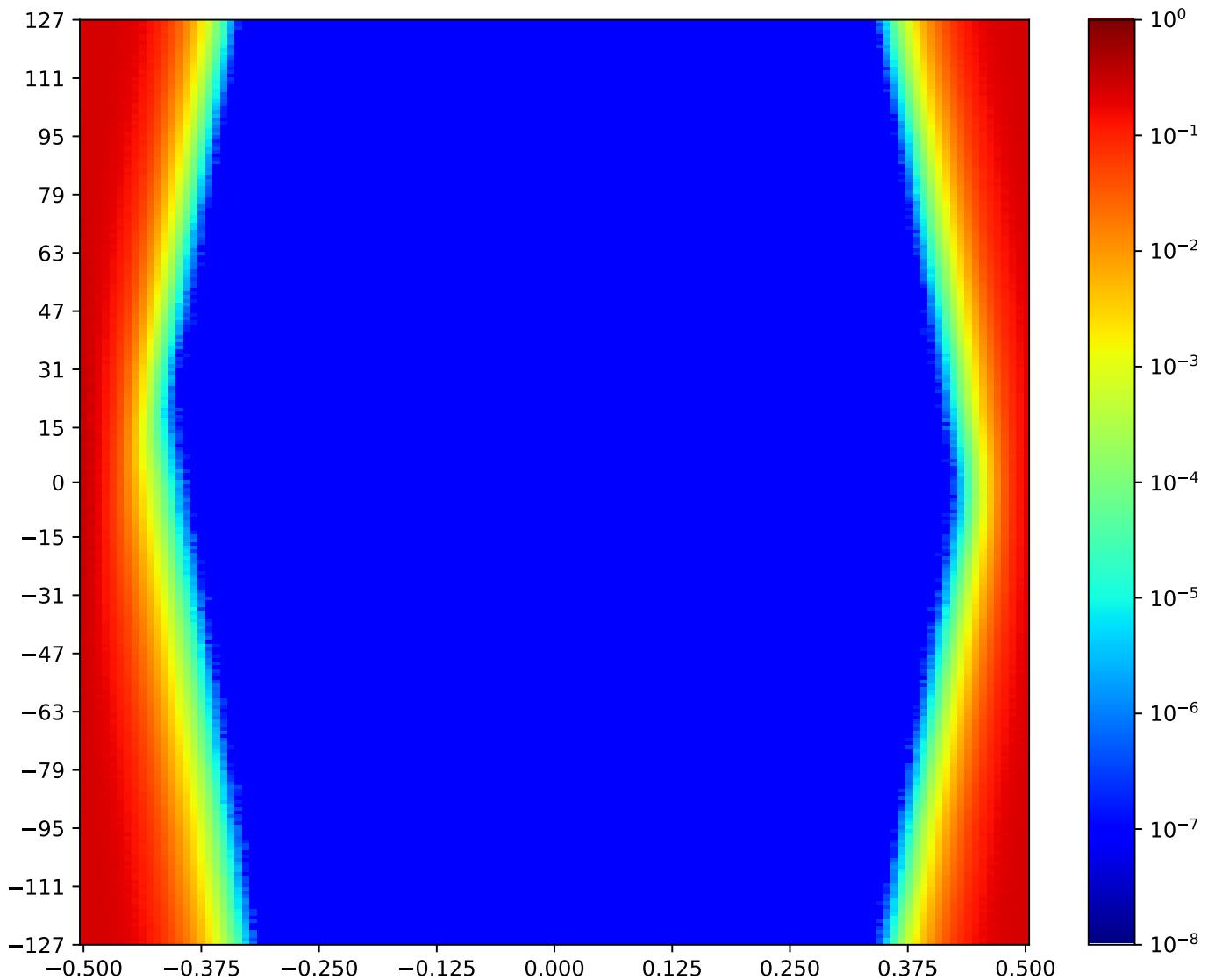


Figure 1.184: TRP\_FPGA-TX5-04-RX14-04-MSP\_C\_FPGA

Call back to summary Figure 1.179. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.14.6 TRP\_FPGA-TX5-05-RX14-05-MSP\_C\_FPGA

Table 1.171: TRP\_FPGA-TX5-05-RX14-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:24:30		2018-Jan-24 16:25:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9530	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

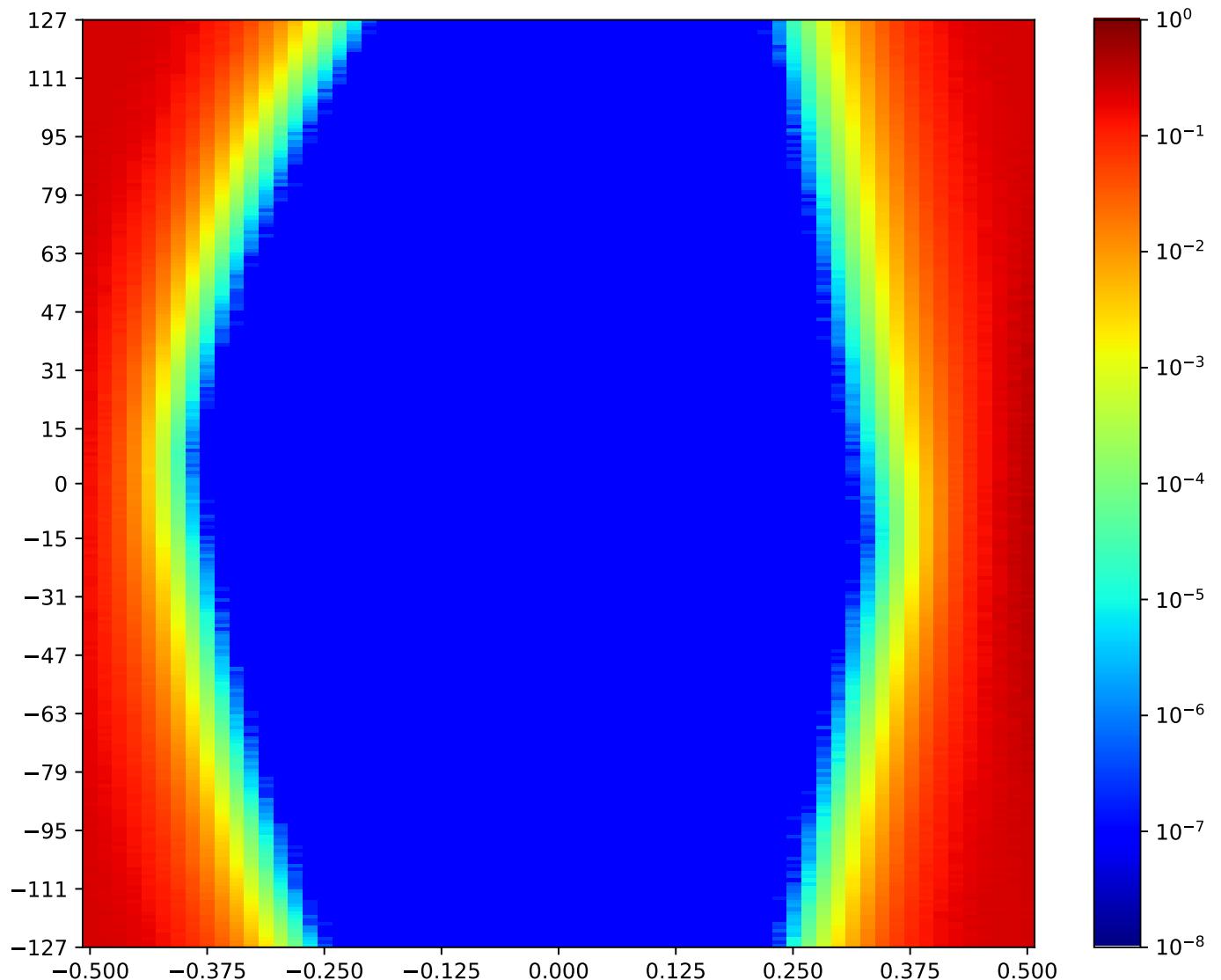


Figure 1.185: TRP\_FPGA-TX5-05-RX14-05-MSP\_C\_FPGA

Call back to summary Figure 1.179. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.14.7 TRP\_FPGA-TX5-06-RX14-06-MSP\_C\_FPGA

Table 1.172: TRP\_FPGA-TX5-06-RX14-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:26:57		2018-Jan-24 16:28:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	22893	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

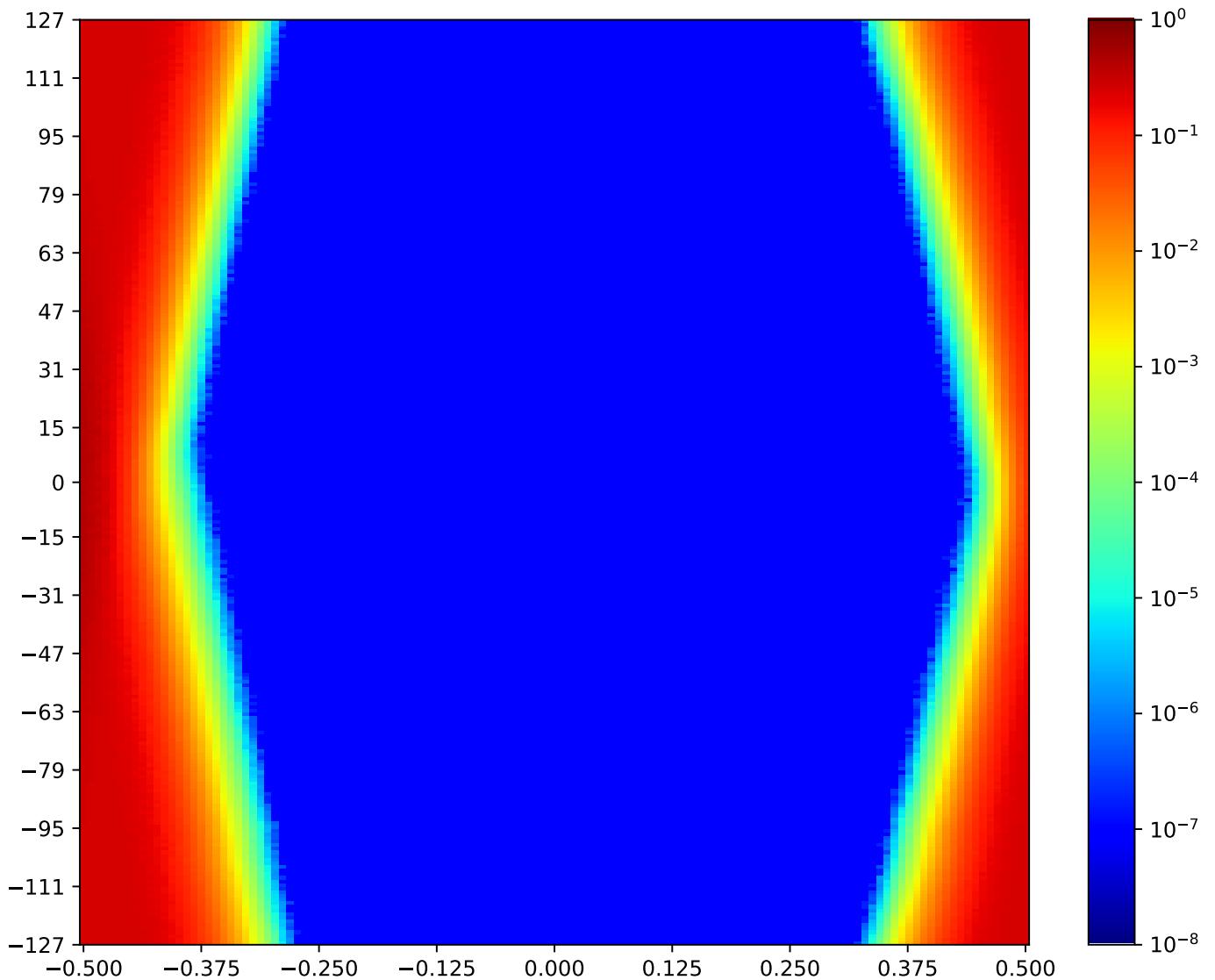


Figure 1.186: TRP\_FPGA-TX5-06-RX14-06-MSP\_C\_FPGA

Call back to summary Figure 1.179. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.14.8 TRP\_FPGA-TX5-07-RX14-07-MSP\_C\_FPGA

Table 1.173: TRP\_FPGA-TX5-07-RX14-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:29:14		2018-Jan-24 16:30:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23417	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

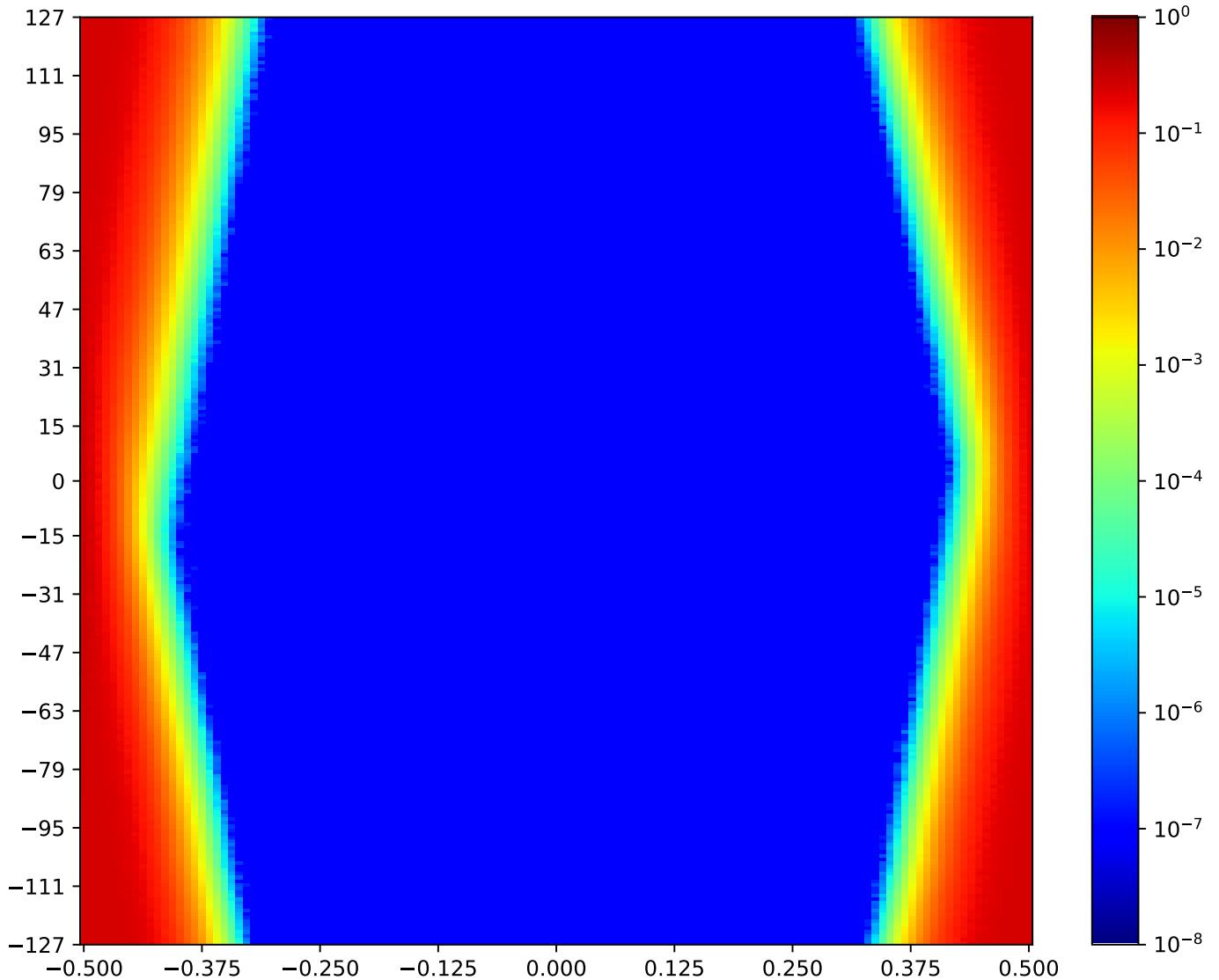


Figure 1.187: TRP\_FPGA-TX5-07-RX14-07-MSP\_C\_FPGA

Call back to summary Figure 1.179. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.15 MSP\_A TX1 MSP\_C RX11 Minipod Loopback

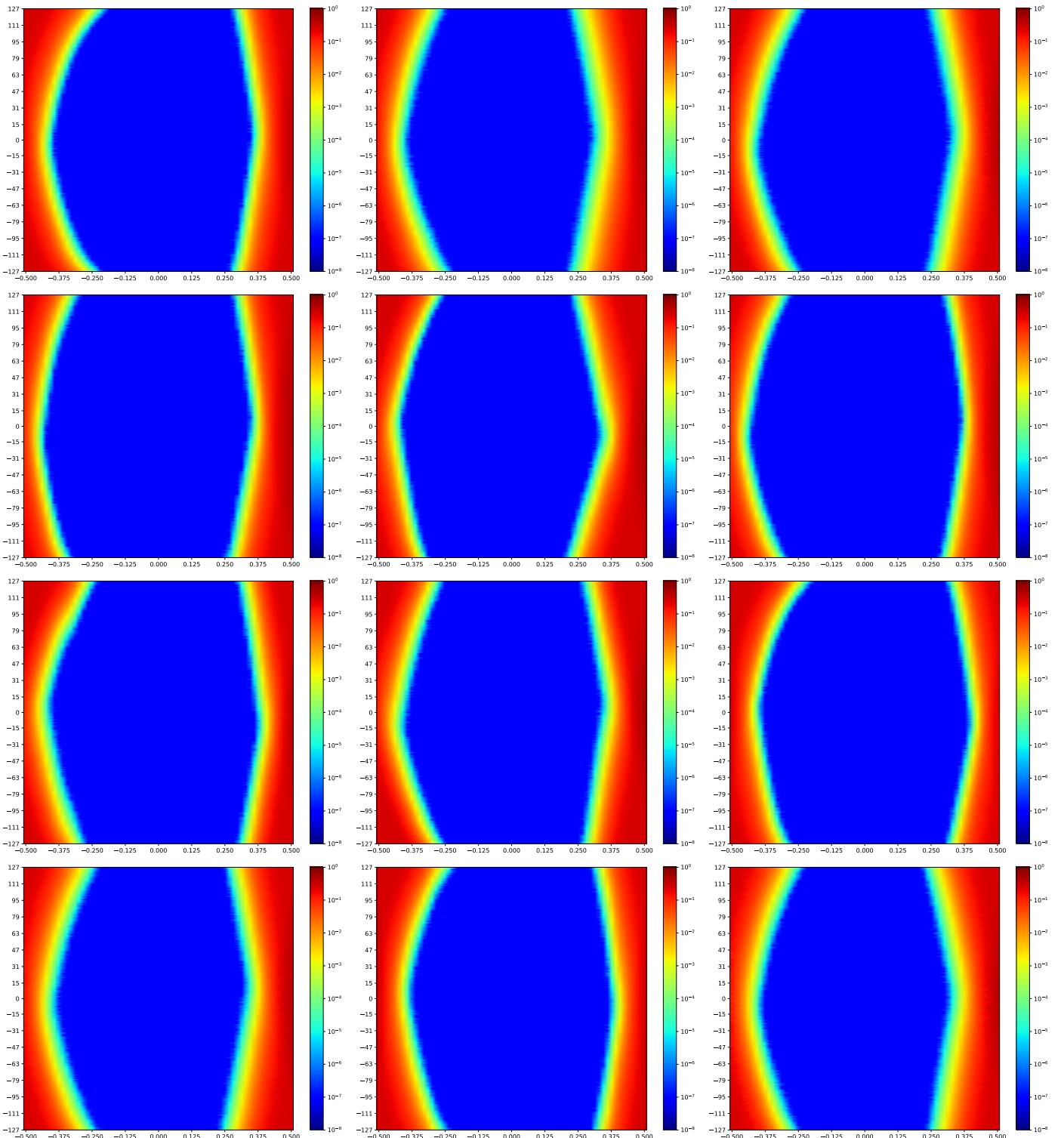


Figure 1.188: MSP\_A TX1 MSP\_C RX11 Minipod Loopback

A cross-reference to Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.201.

### 1.15.1 MSP\_A\_FPGA-TX1-00-RX11-00-MSP\_C\_FPGA

Table 1.174: MSP\_A\_FPGA-TX1-00-RX11-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:50:09		2018-Jan-24 16:50:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10284	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

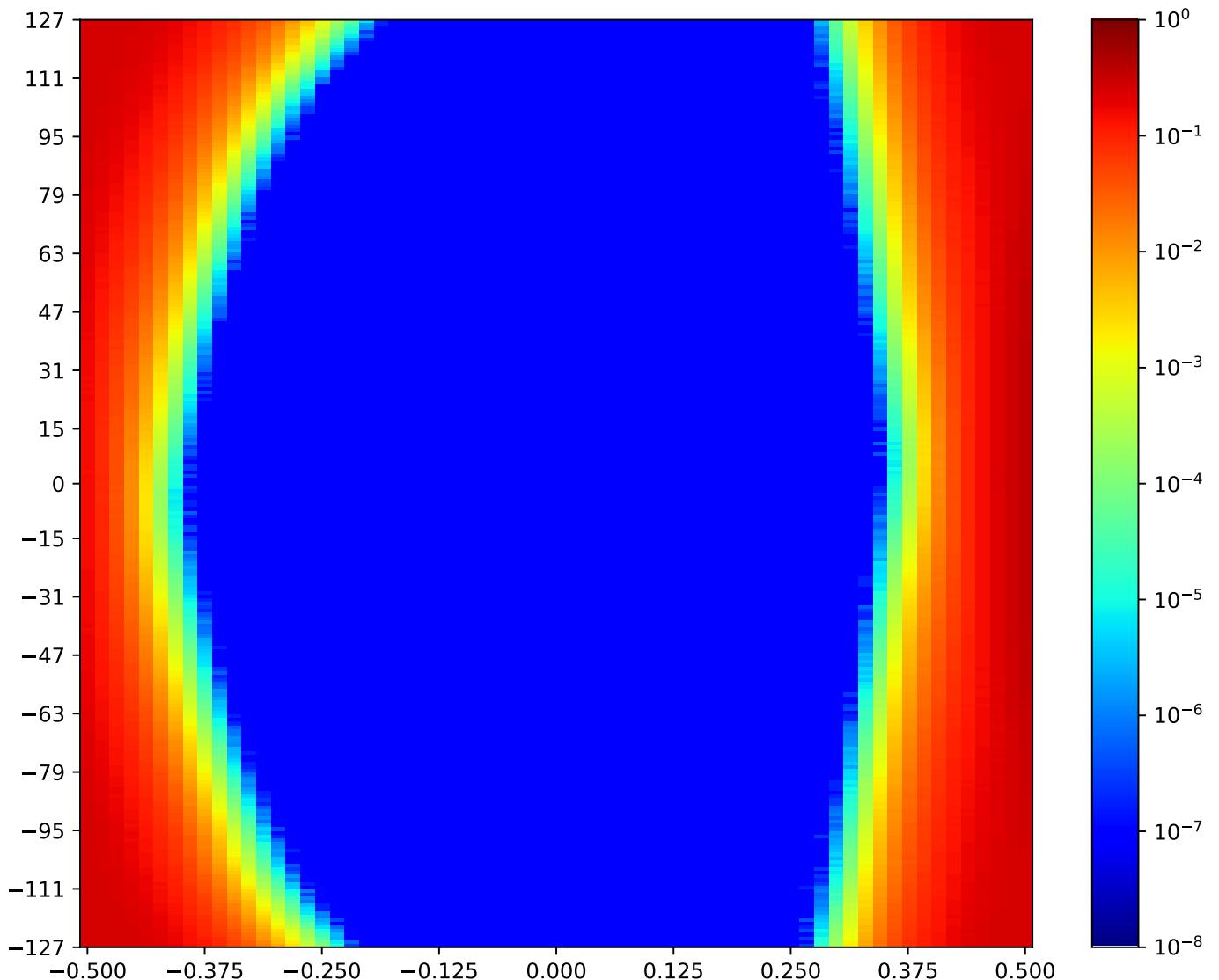


Figure 1.189: MSP\_A\_FPGA-TX1-00-RX11-00-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.2 MSP\_A\_FPGA-TX1-01-RX11-01-MSP\_C\_FPGA

Table 1.175: MSP\_A\_FPGA-TX1-01-RX11-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:51:17		2018-Jan-24 16:51:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9215	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

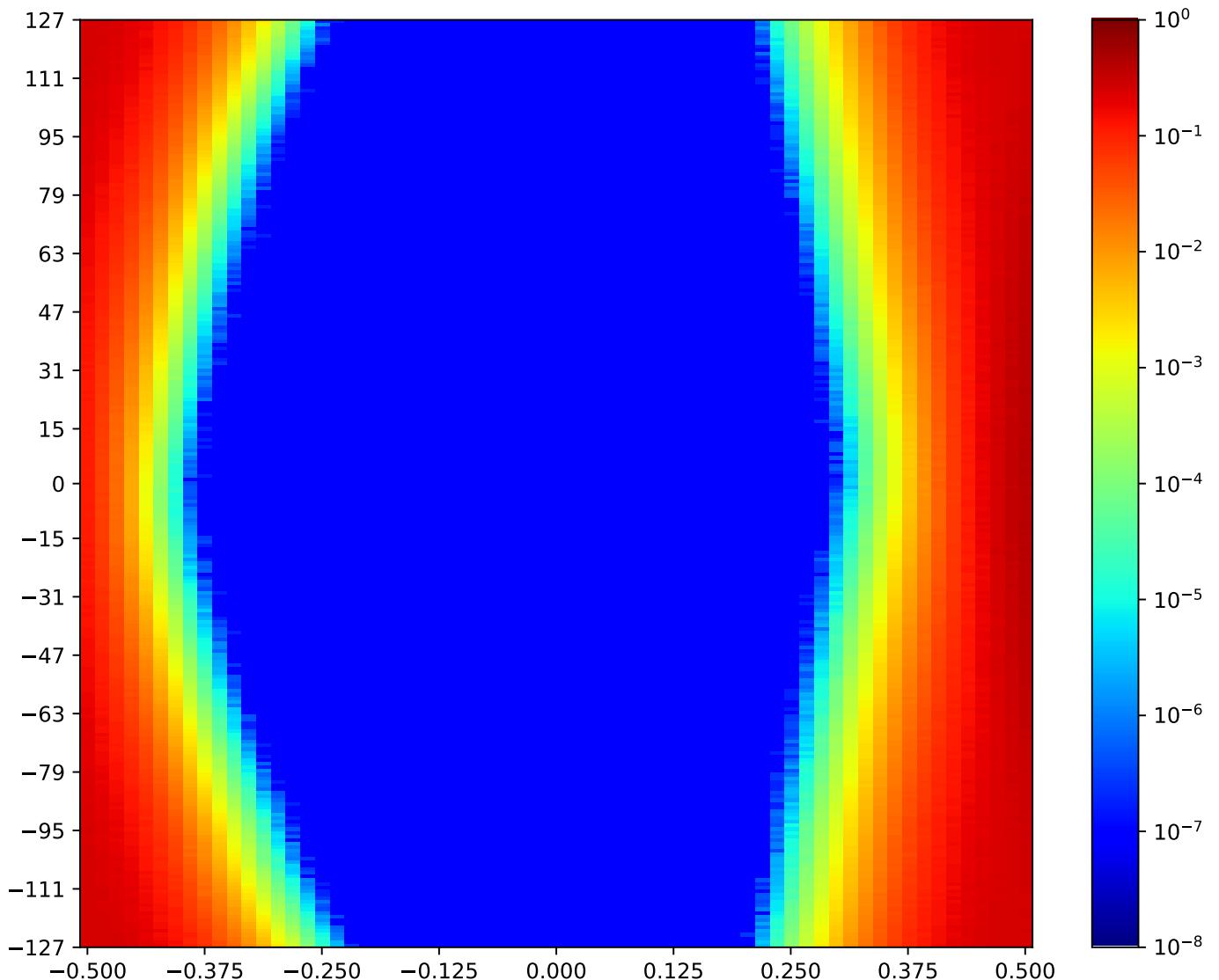


Figure 1.190: MSP\_A\_FPGA-TX1-01-RX11-01-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.3 MSP\_A\_FPGA-TX1-02-RX11-02-MSP\_C\_FPGA

Table 1.176: MSP\_A\_FPGA-TX1-02-RX11-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:51:51		2018-Jan-24 16:52:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9521	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

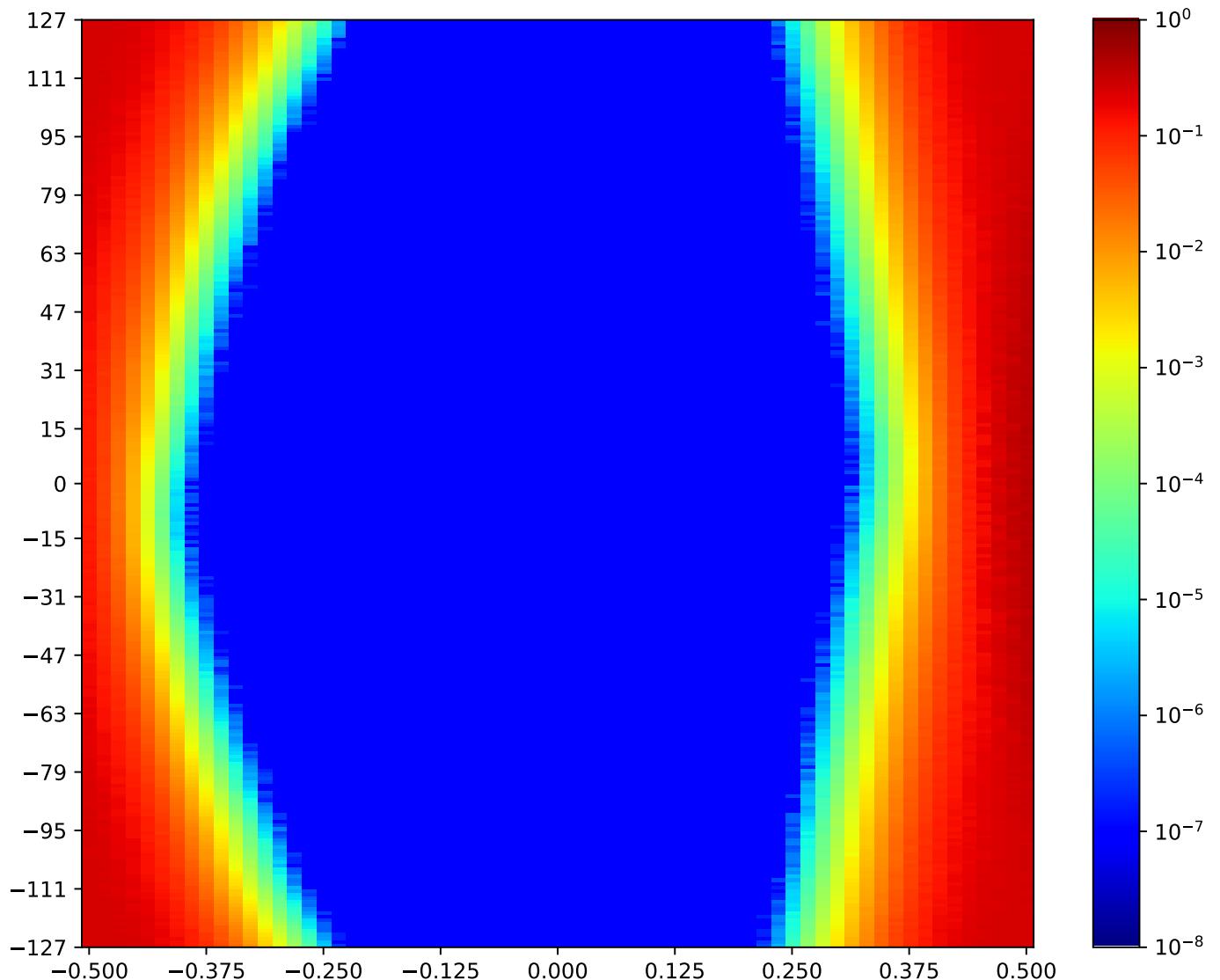


Figure 1.191: MSP\_A\_FPGA-TX1-02-RX11-02-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.15.4 MSP\_A\_FPGA-TX1-03-RX11-03-MSP\_C\_FPGA

Table 1.177: MSP\_A\_FPGA-TX1-03-RX11-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:48:59		2018-Jan-24 16:49:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11027	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

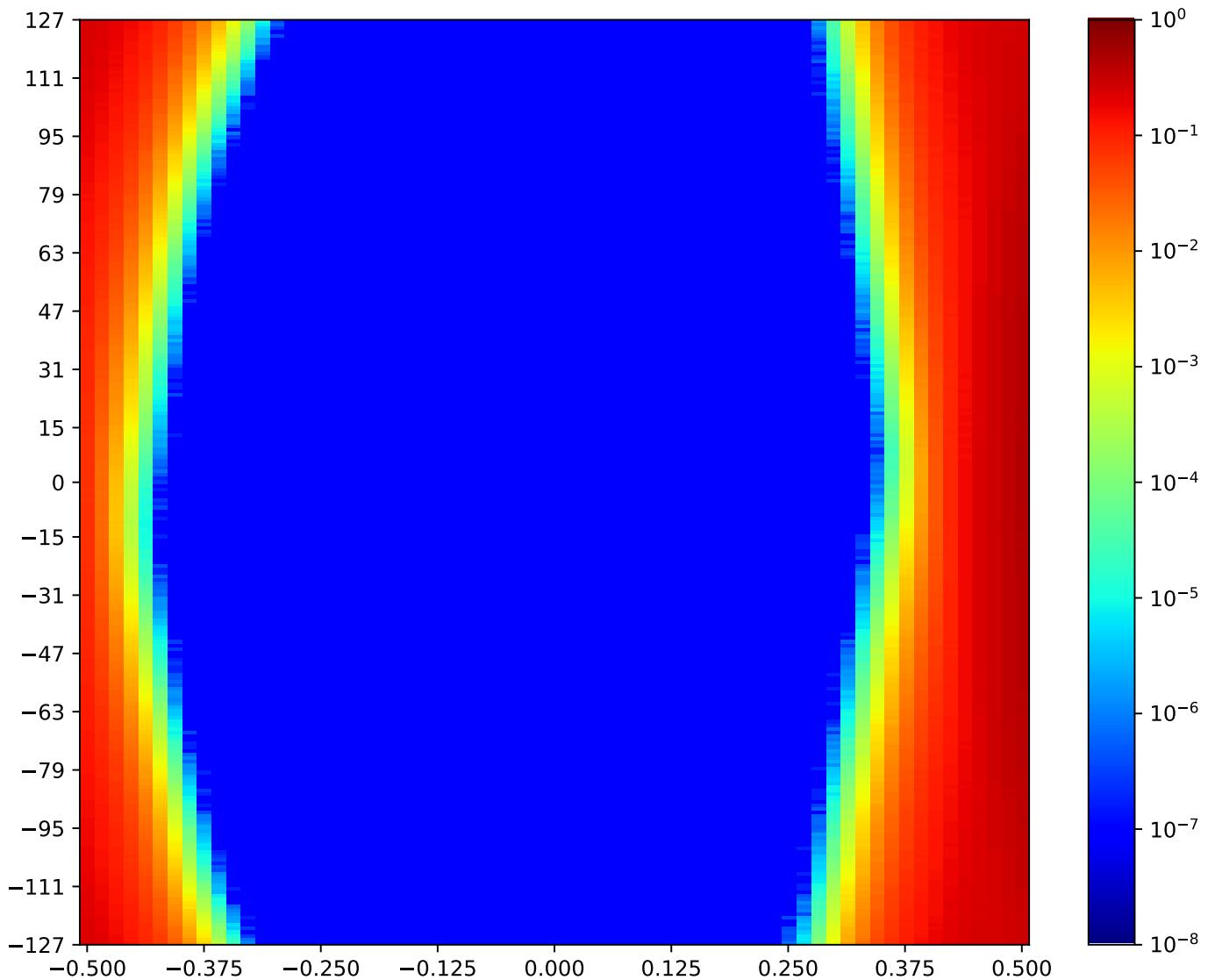


Figure 1.192: MSP\_A\_FPGA-TX1-03-RX11-03-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.5 MSP\_A\_FPGA-TX1-04-RX11-04-MSP\_C\_FPGA

Table 1.178: MSP\_A\_FPGA-TX1-04-RX11-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:53:38		2018-Jan-24 16:54:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10031	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

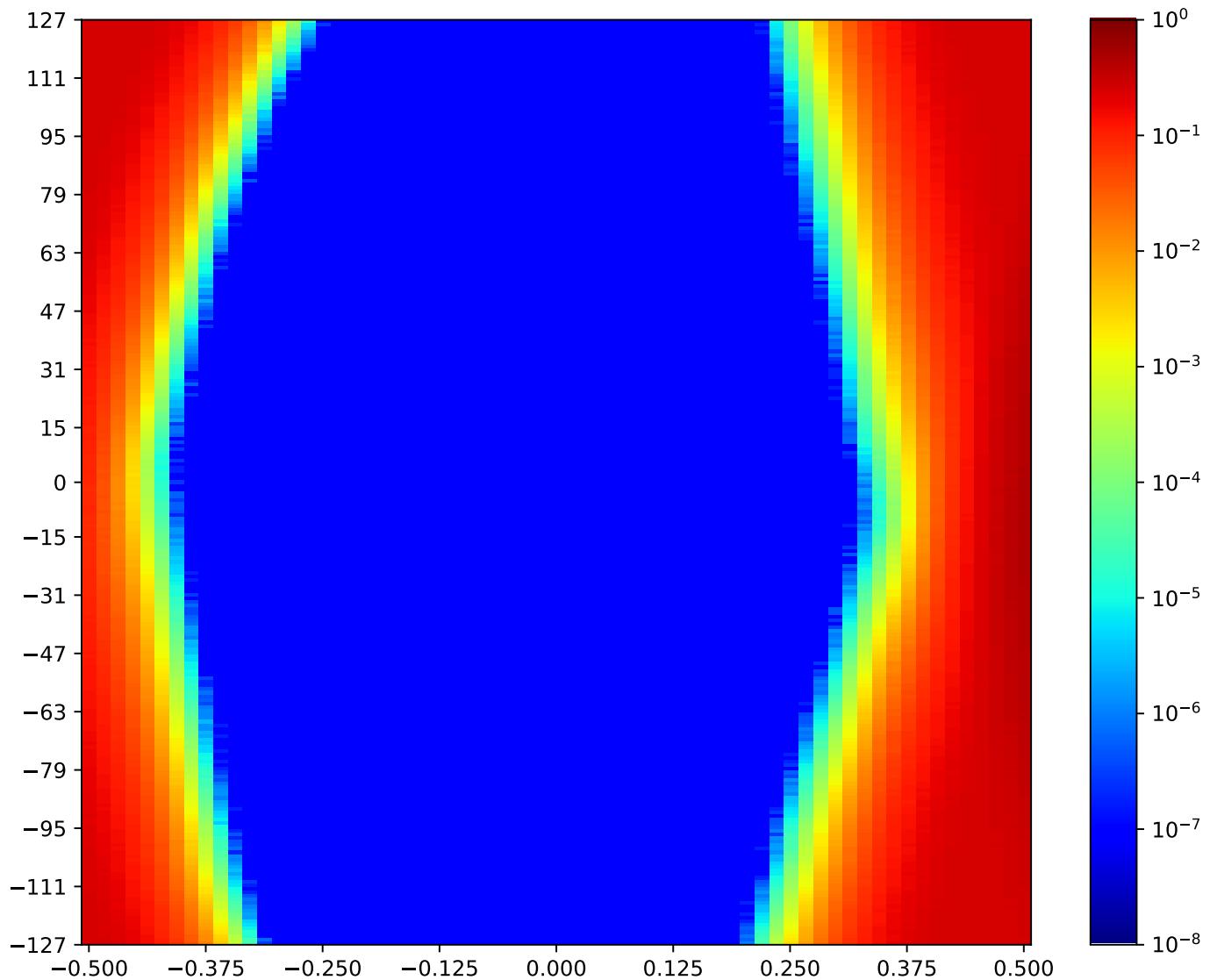


Figure 1.193: MSP\_A\_FPGA-TX1-04-RX11-04-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.6 MSP\_A\_FPGA-TX1-05-RX11-05-MSP\_C\_FPGA

Table 1.179: MSP\_A\_FPGA-TX1-05-RX11-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:48:24		2018-Jan-24 16:48:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11151	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

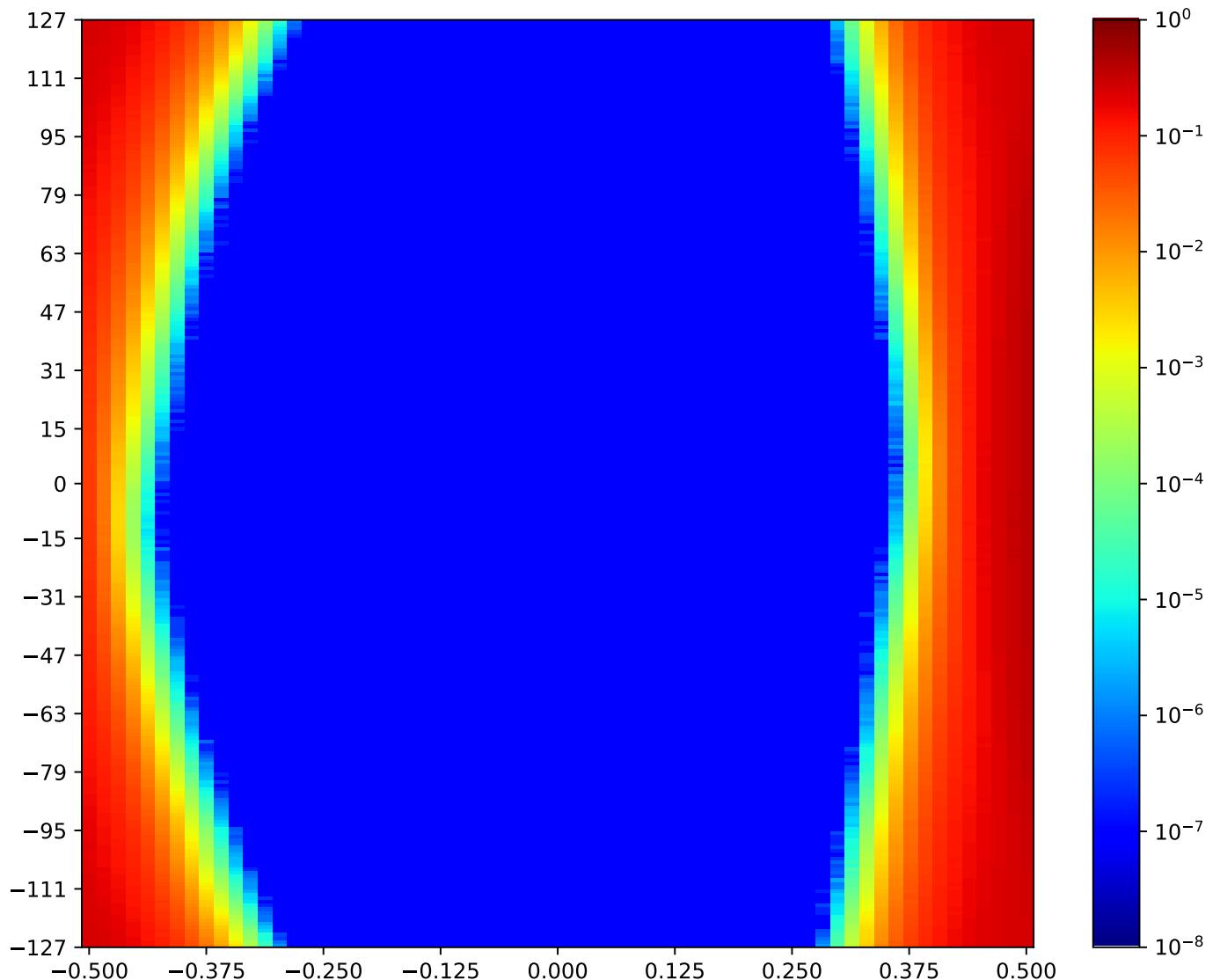


Figure 1.194: MSP\_A\_FPGA-TX1-05-RX11-05-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.7 MSP\_A\_FPGA-TX1-06-RX11-06-MSP\_C\_FPGA

Table 1.180: MSP\_A\_FPGA-TX1-06-RX11-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:54:48		2018-Jan-24 16:55:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10738	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

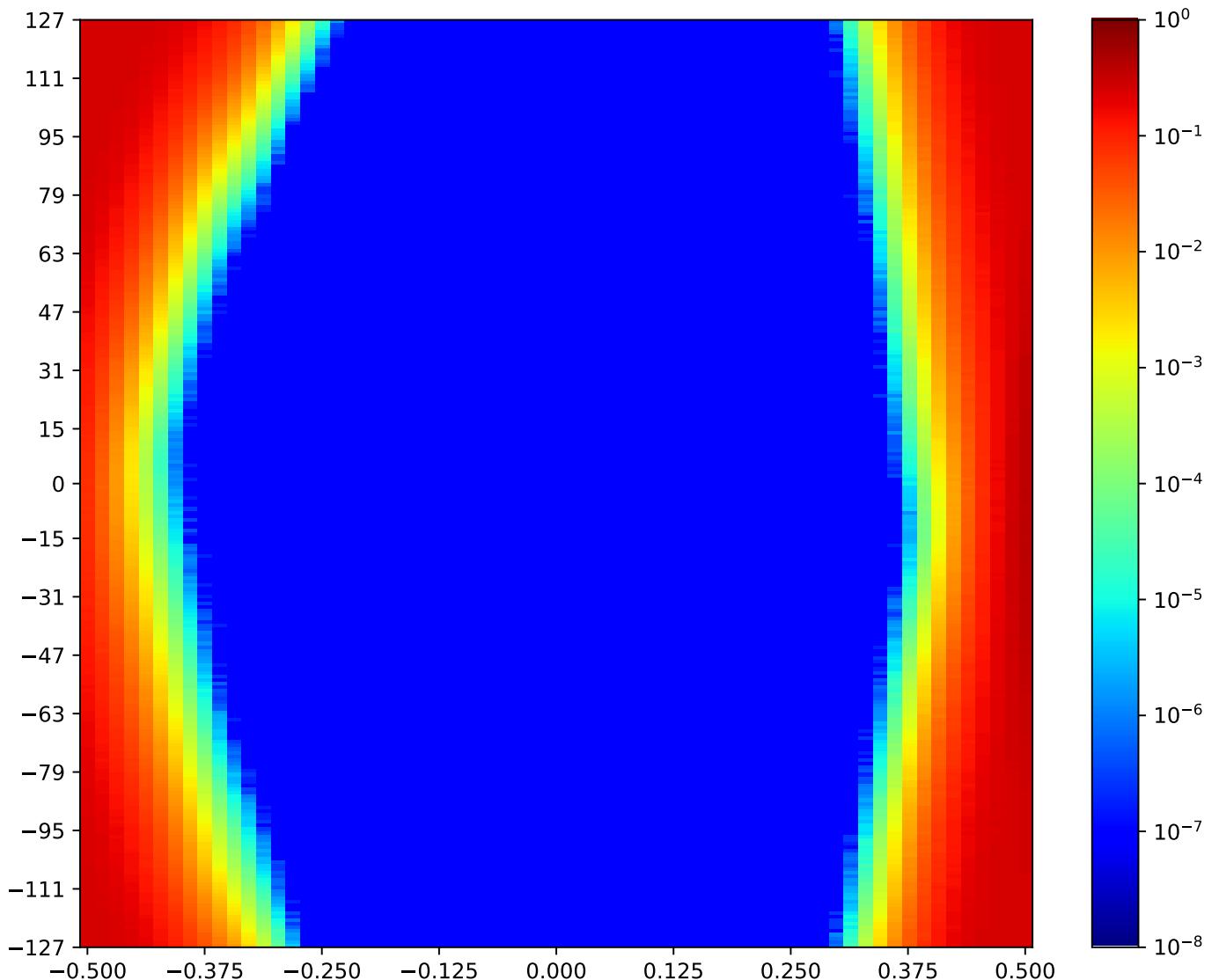


Figure 1.195: MSP\_A\_FPGA-TX1-06-RX11-06-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.8 MSP\_A\_FPGA-TX1-07-RX11-07-MSP\_C\_FPGA

Table 1.181: MSP\_A\_FPGA-TX1-07-RX11-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:49:34		2018-Jan-24 16:50:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10090	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

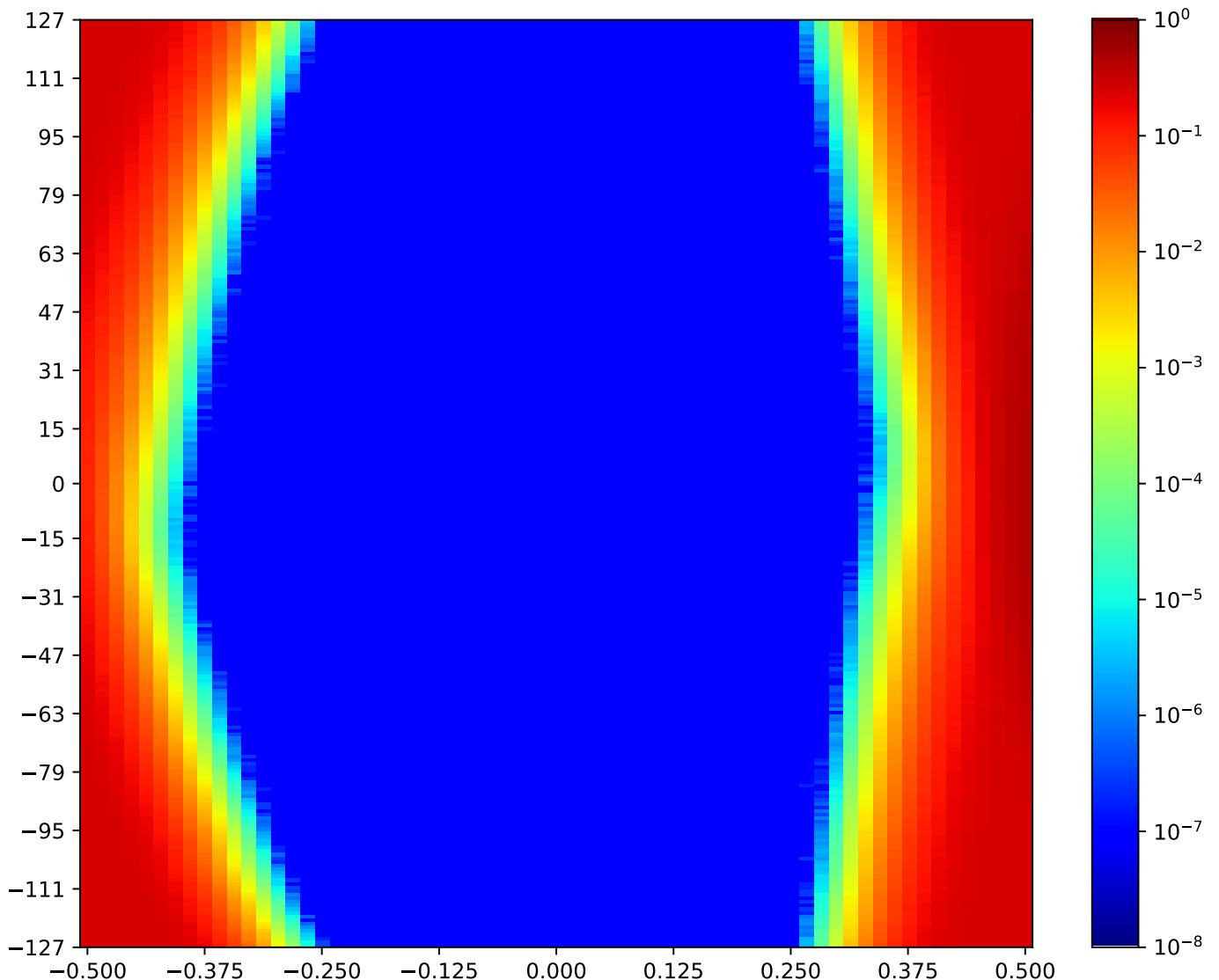


Figure 1.196: MSP\_A\_FPGA-TX1-07-RX11-07-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.9 MSP\_A\_FPGA-TX1-08-RX11-08-MSP\_C\_FPGA

Table 1.182: MSP\_A\_FPGA-TX1-08-RX11-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:54:13		2018-Jan-24 16:54:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10946	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

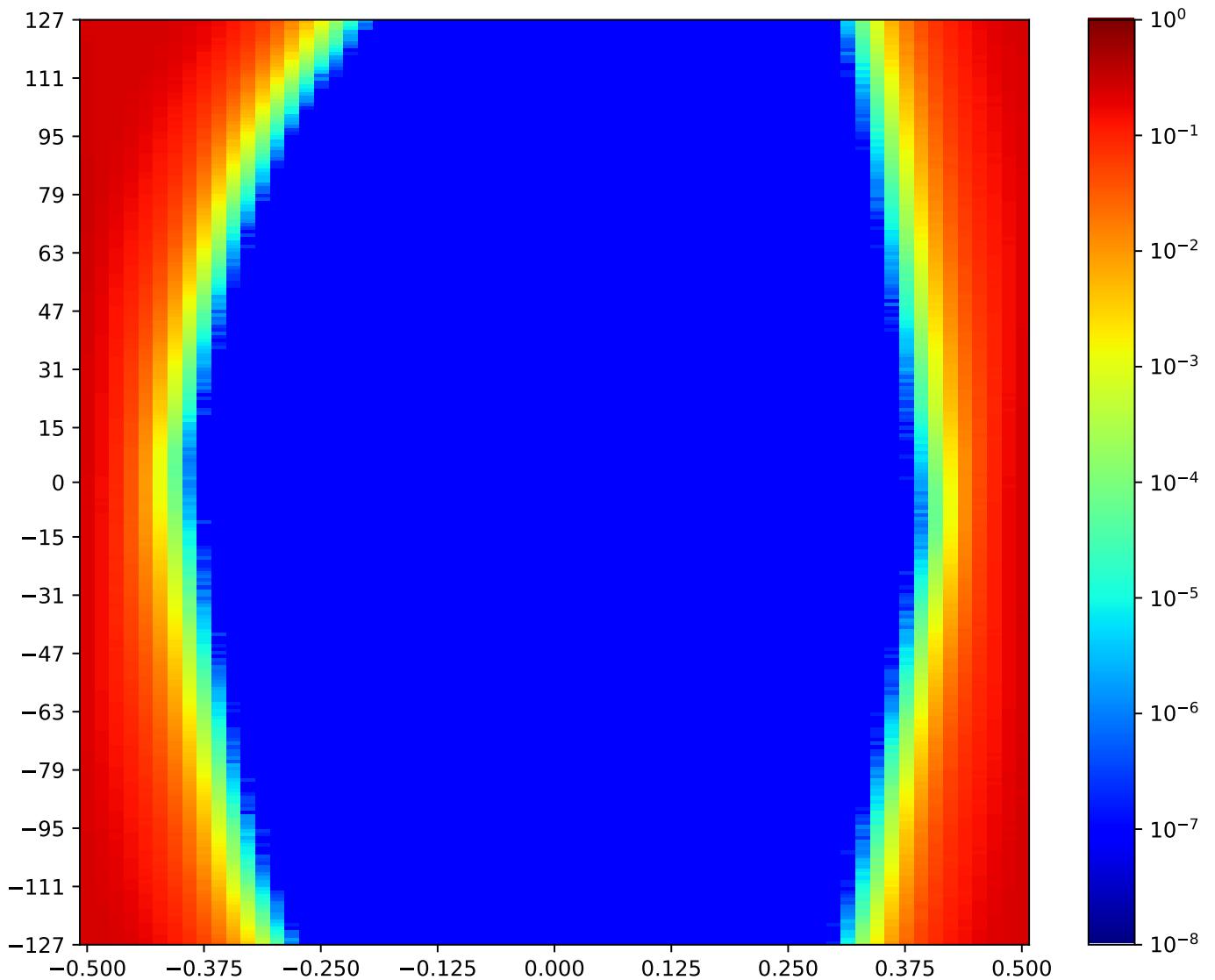


Figure 1.197: MSP\_A\_FPGA-TX1-08-RX11-08-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.10 MSP\_A\_FPGA-TX1-09-RX11-09-MSP\_C\_FPGA

Table 1.183: MSP\_A\_FPGA-TX1-09-RX11-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:50:42		2018-Jan-24 16:51:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9517	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

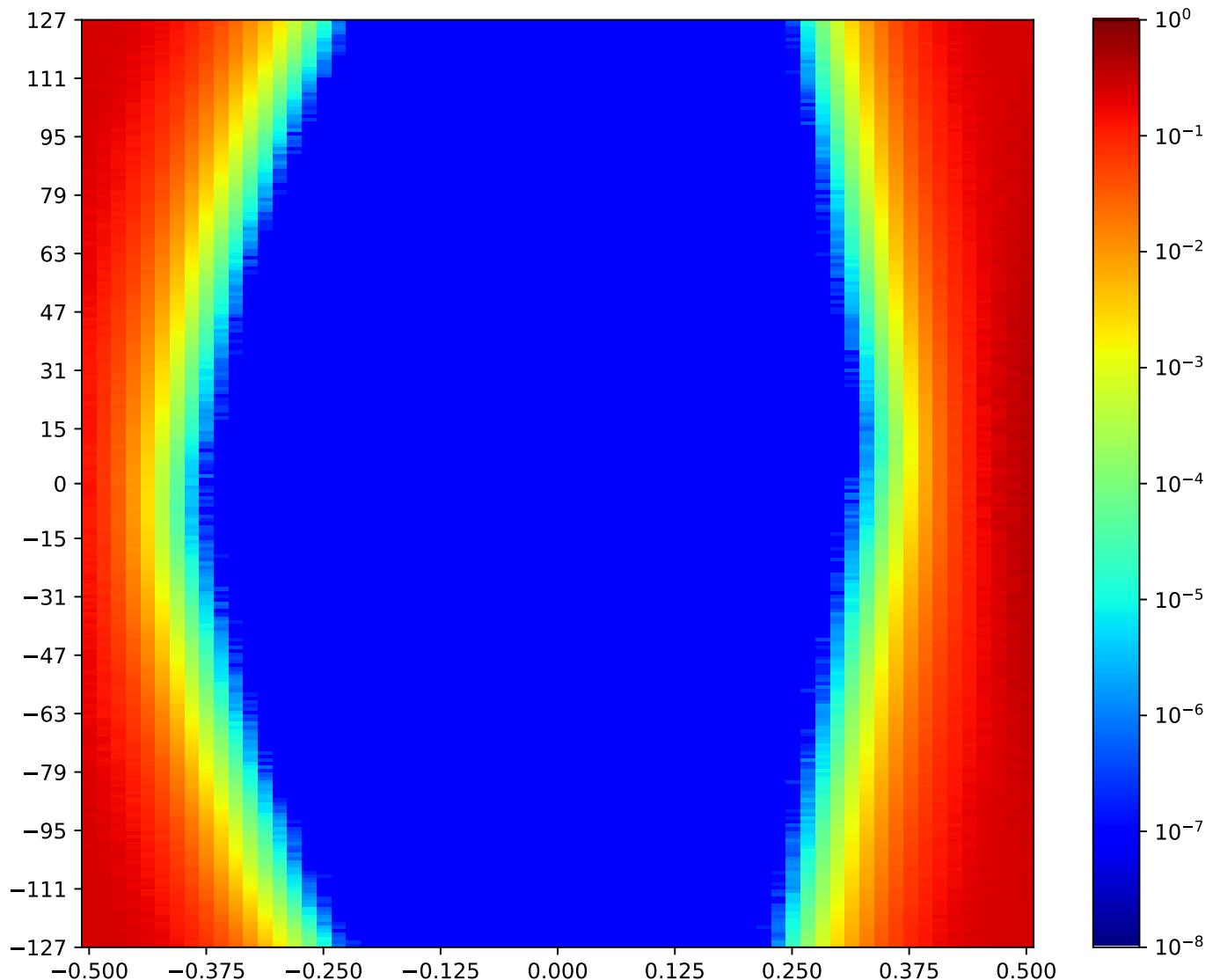


Figure 1.198: MSP\_A\_FPGA-TX1-09-RX11-09-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.11 MSP\_A\_FPGA-TX1-10-RX11-10-MSP\_C\_FPGA

Table 1.184: MSP\_A\_FPGA-TX1-10-RX11-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:53:02		2018-Jan-24 16:53:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10481	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

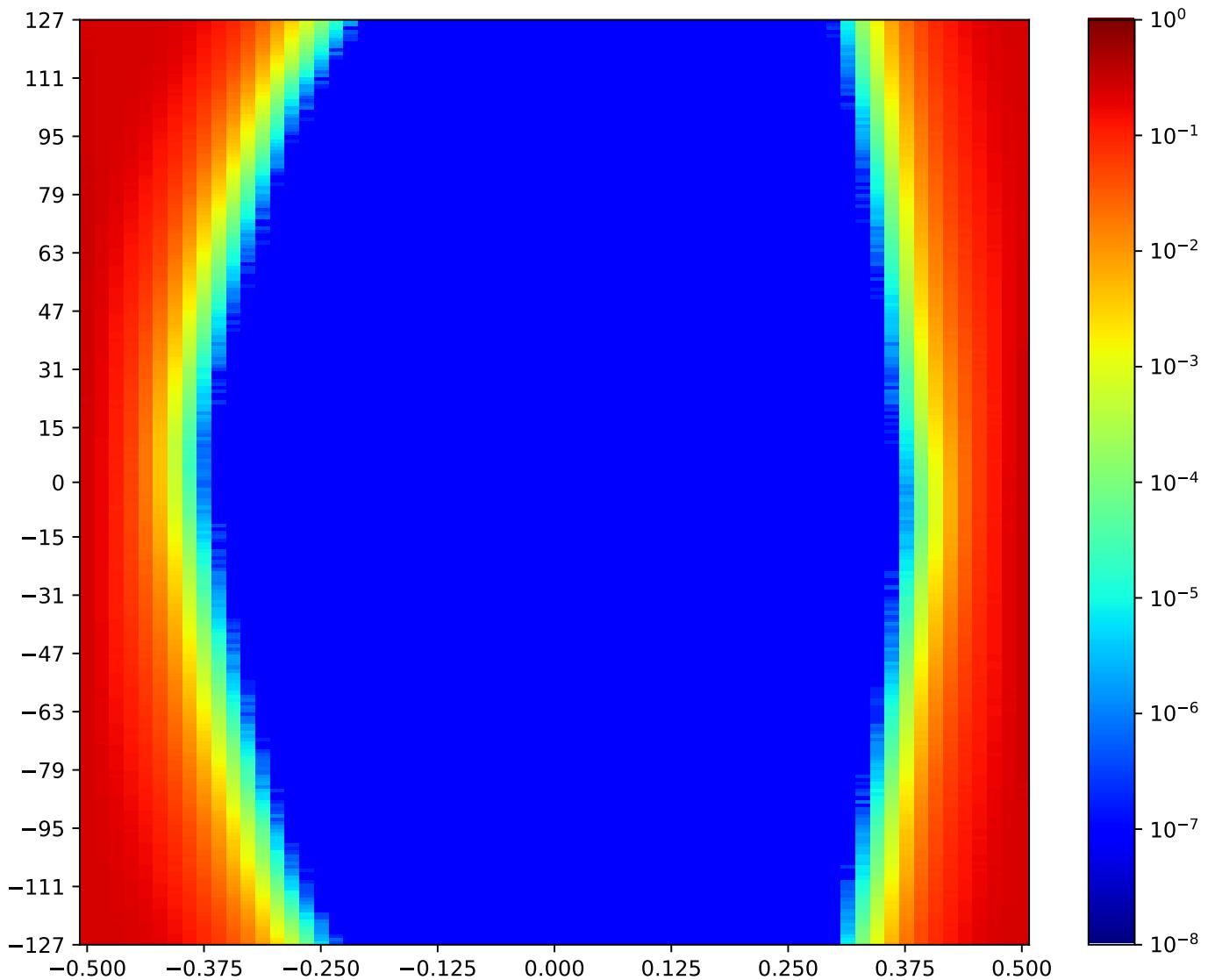


Figure 1.199: MSP\_A\_FPGA-TX1-10-RX11-10-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.15.12 MSP\_A\_FPGA-TX1-11-RX11-11-MSP\_C\_FPGA

Table 1.185: MSP\_A\_FPGA-TX1-11-RX11-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:52:27		2018-Jan-24 16:53:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9481	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

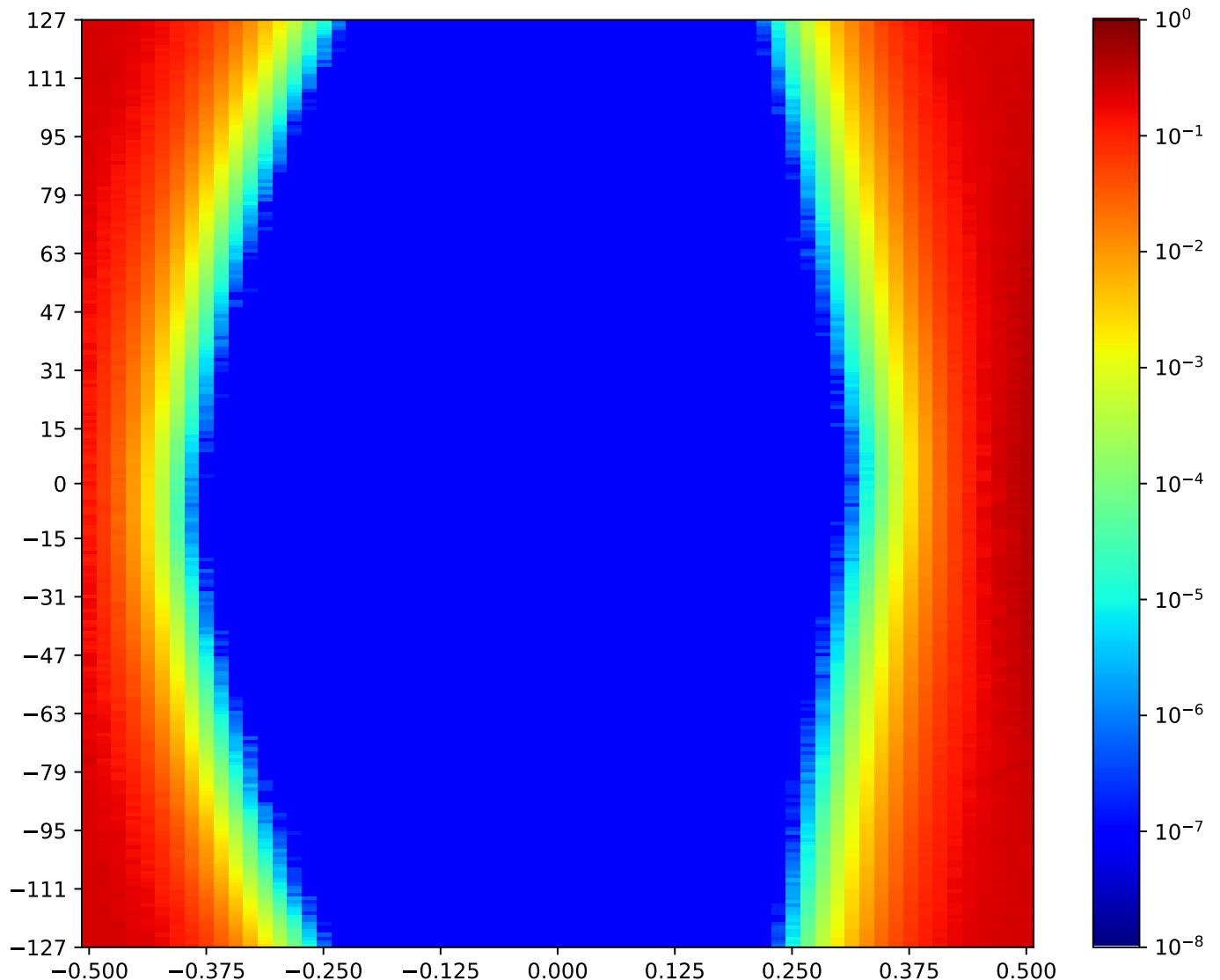


Figure 1.200: MSP\_A\_FPGA-TX1-11-RX11-11-MSP\_C\_FPGA

Call back to summary Figure 1.188. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.16 MSP\_A TX2 MSP\_C RX10 Minipod Loopback

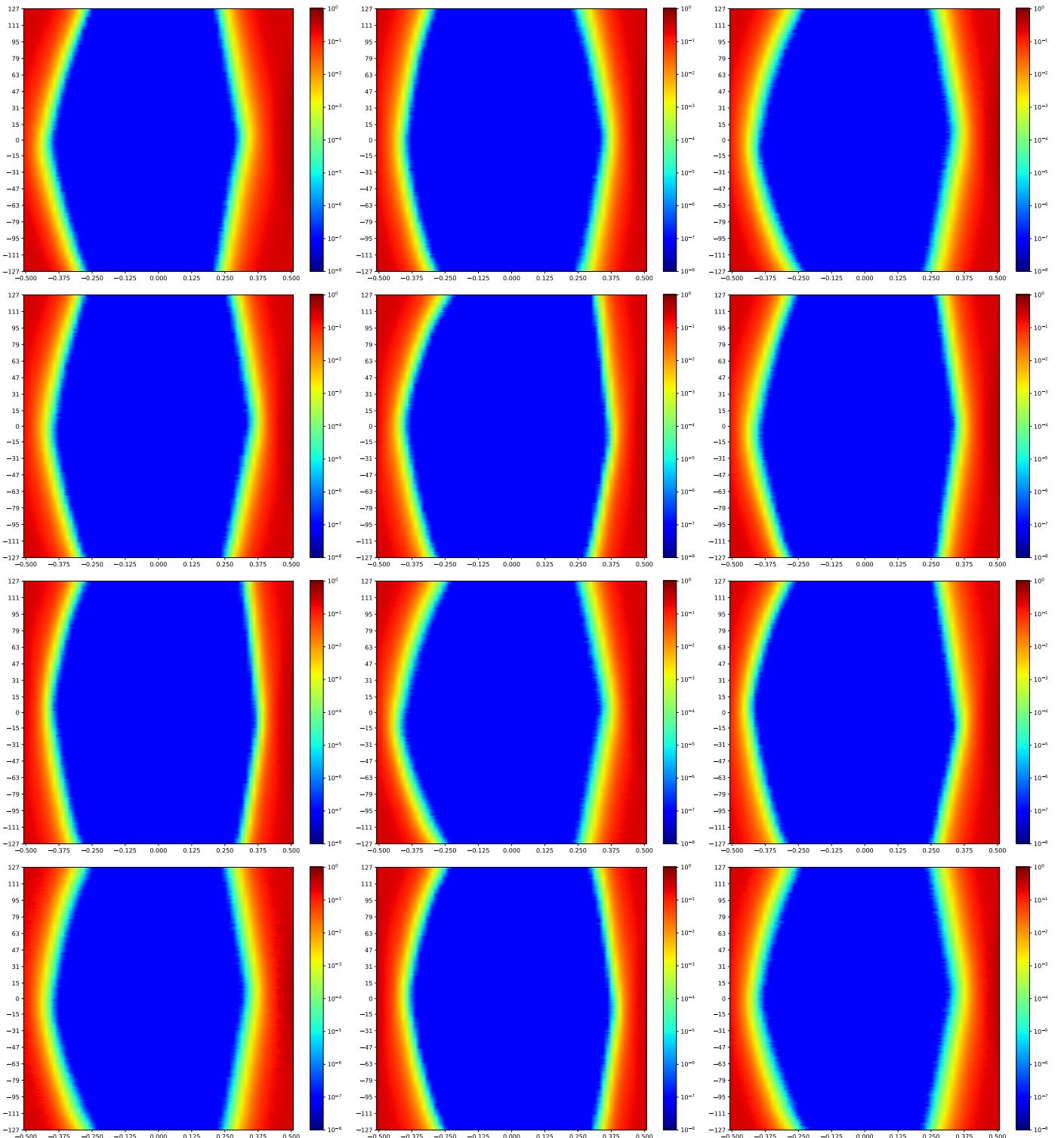


Figure 1.201: MSP\_A TX2 MSP\_C RX10 Minipod Loopback

A cross-reference to Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.214.

### 1.16.1 MSP\_A\_FPGA-TX2-00-RX10-00-MSP\_C\_FPGA

Table 1.186: MSP\_A\_FPGA-TX2-00-RX10-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:57:12		2018-Jan-24 16:57:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9347	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

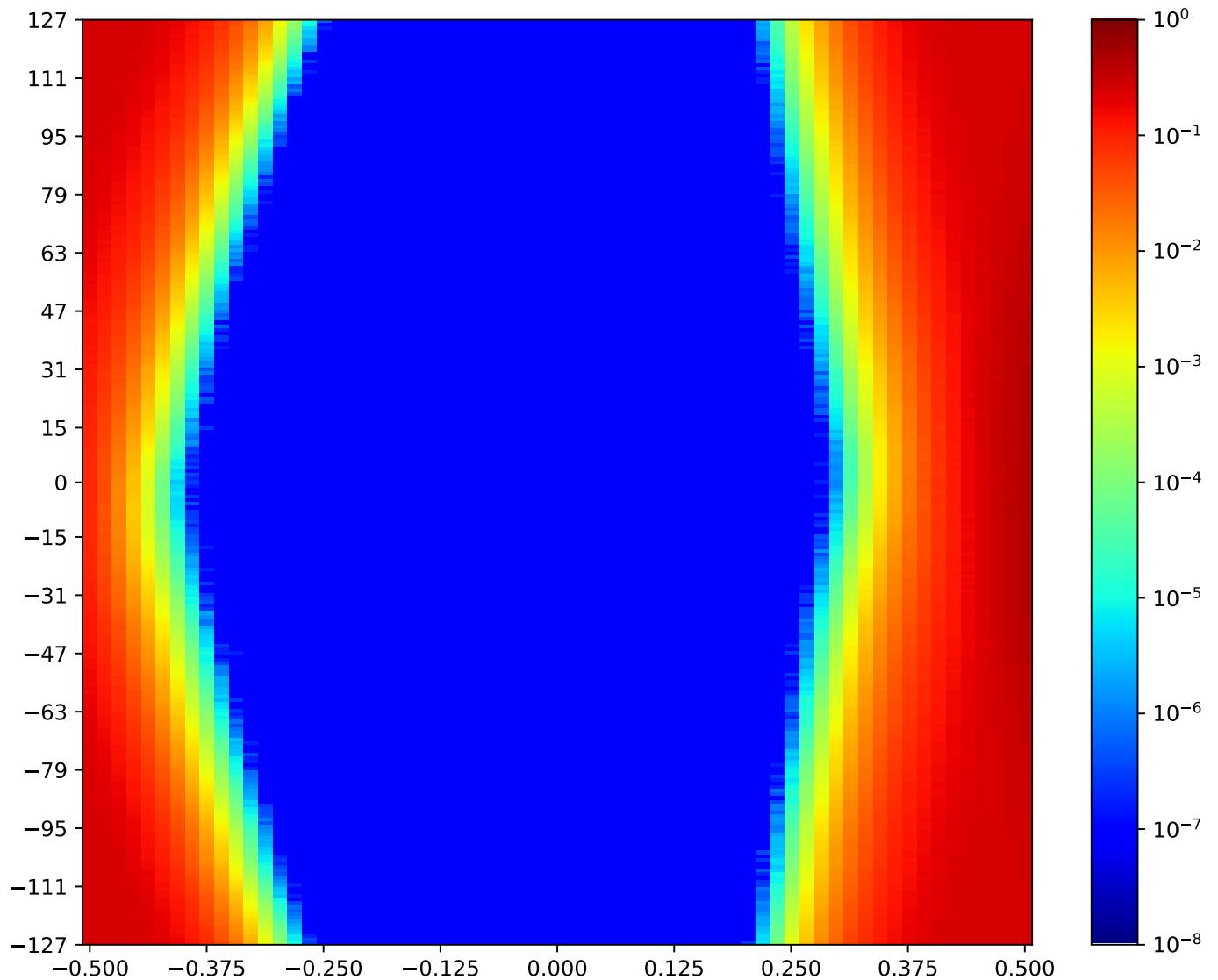


Figure 1.202: MSP\_A\_FPGA-TX2-00-RX10-00-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.16.2 MSP\_A\_FPGA-TX2-01-RX10-01-MSP\_C\_FPGA

Table 1.187: MSP\_A\_FPGA-TX2-01-RX10-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:56:01		2018-Jan-24 16:56:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10109	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

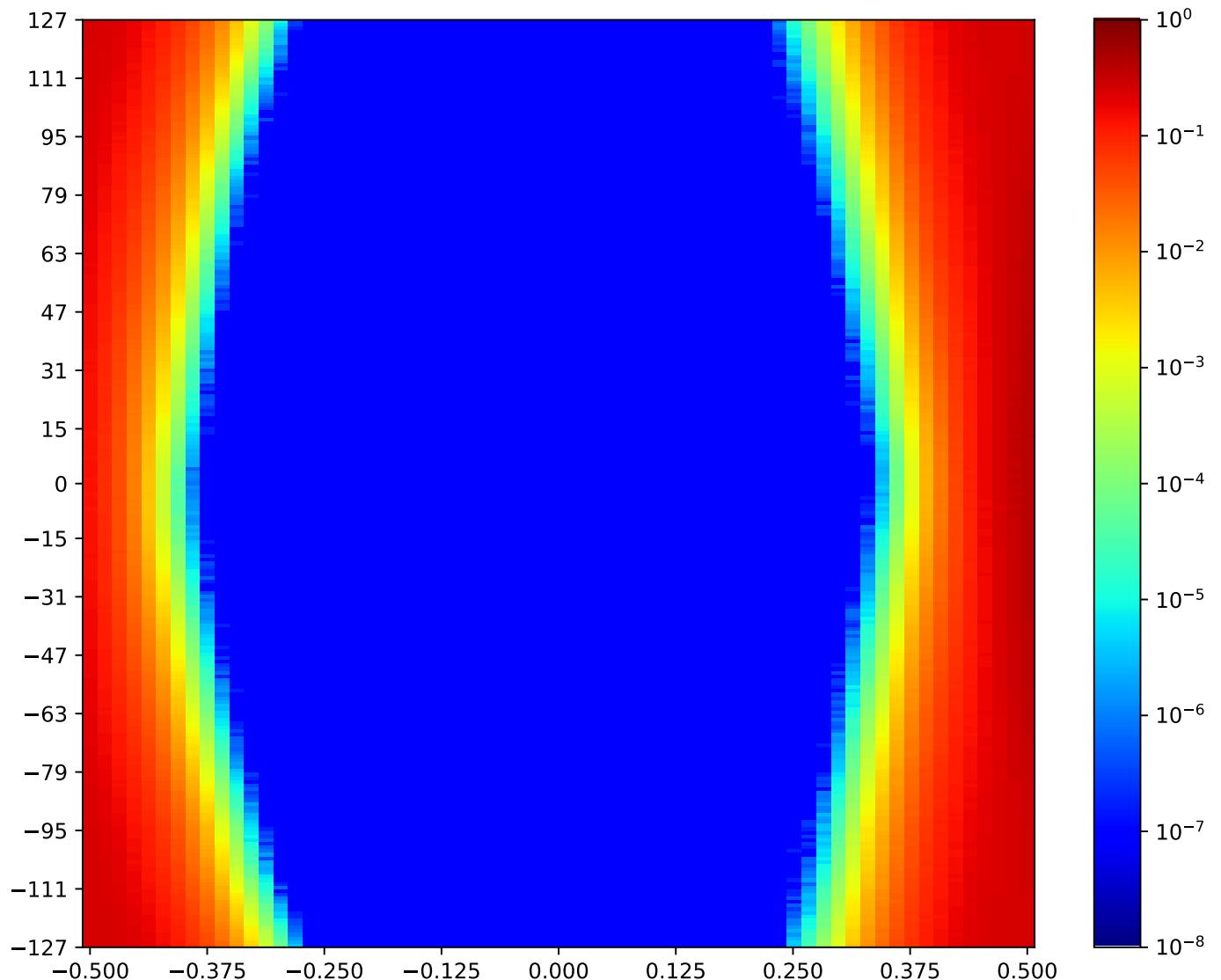


Figure 1.203: MSP\_A\_FPGA-TX2-01-RX10-01-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.16.3 MSP\_A\_FPGA-TX2-02-RX10-02-MSP\_C\_FPGA

Table 1.188: MSP\_A\_FPGA-TX2-02-RX10-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:59:00		2018-Jan-24 16:59:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9467	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

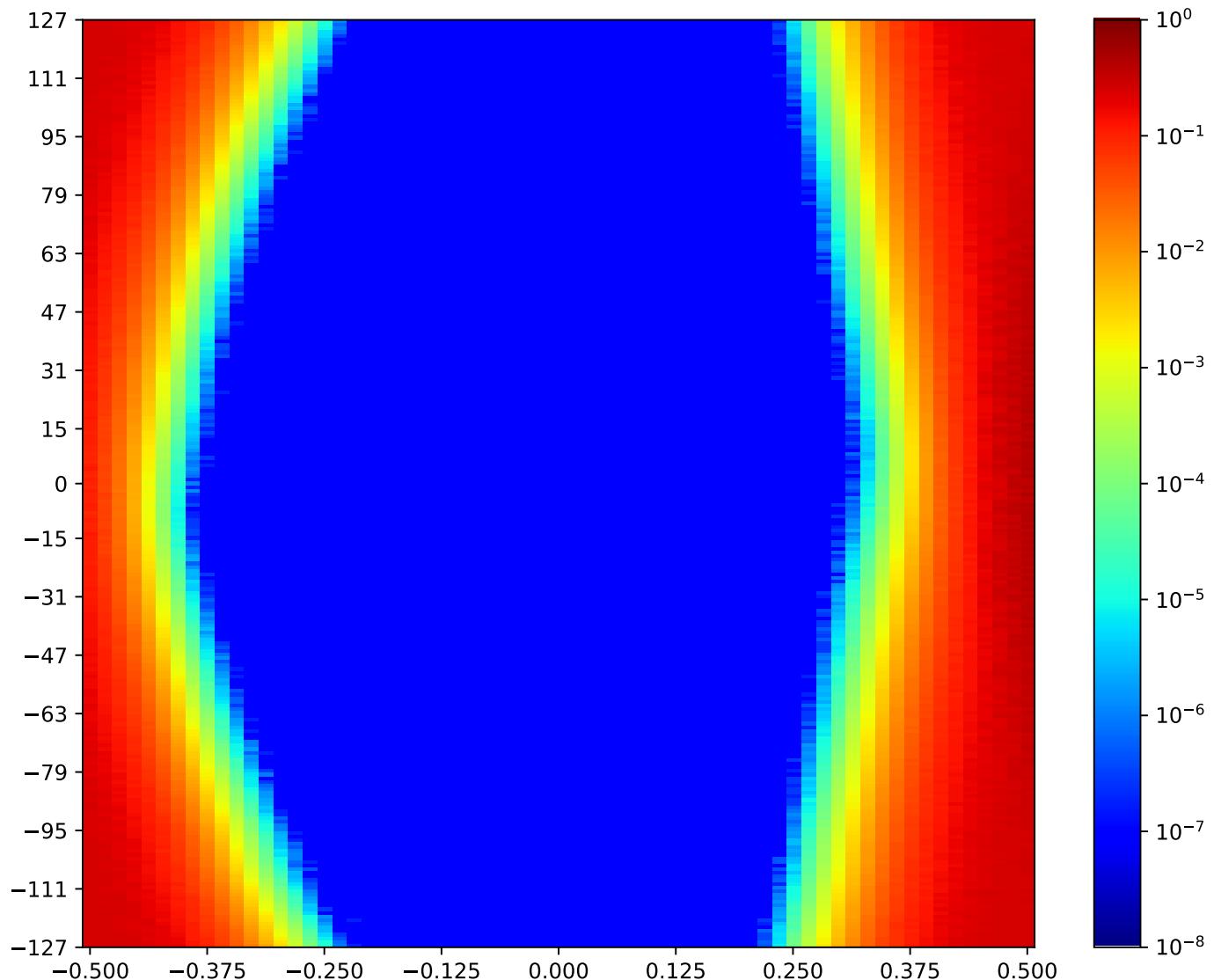


Figure 1.204: MSP\_A\_FPGA-TX2-02-RX10-02-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.16.4 MSP\_A\_FPGA-TX2-03-RX10-03-MSP\_C\_FPGA

Table 1.189: MSP\_A\_FPGA-TX2-03-RX10-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:55:25		2018-Jan-24 16:56:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10061	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

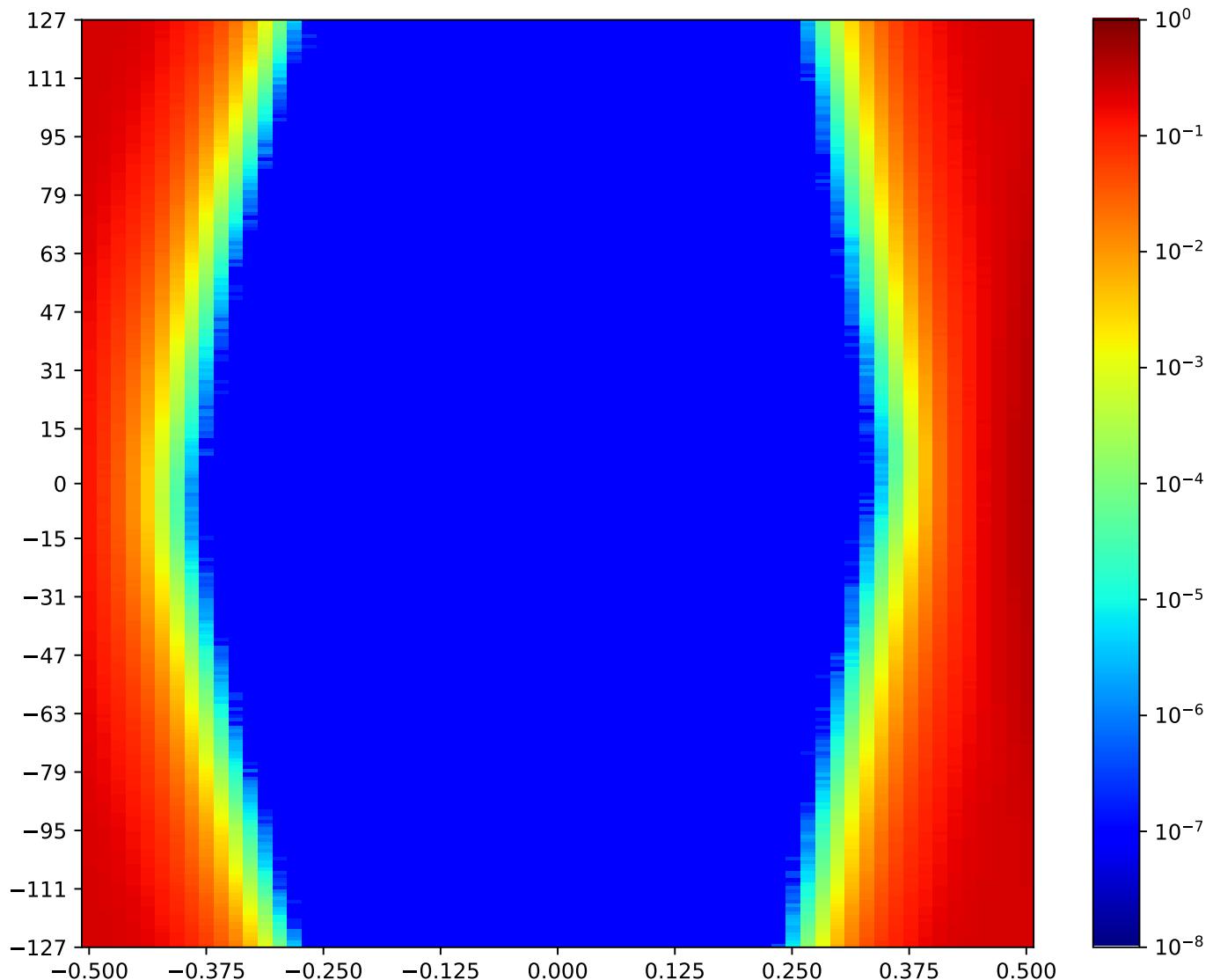


Figure 1.205: MSP\_A\_FPGA-TX2-03-RX10-03-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.16.5 MSP\_A\_FPGA-TX2-04-RX10-04-MSP\_C\_FPGA

Table 1.190: MSP\_A\_FPGA-TX2-04-RX10-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:00:49		2018-Jan-24 17:01:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10520	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

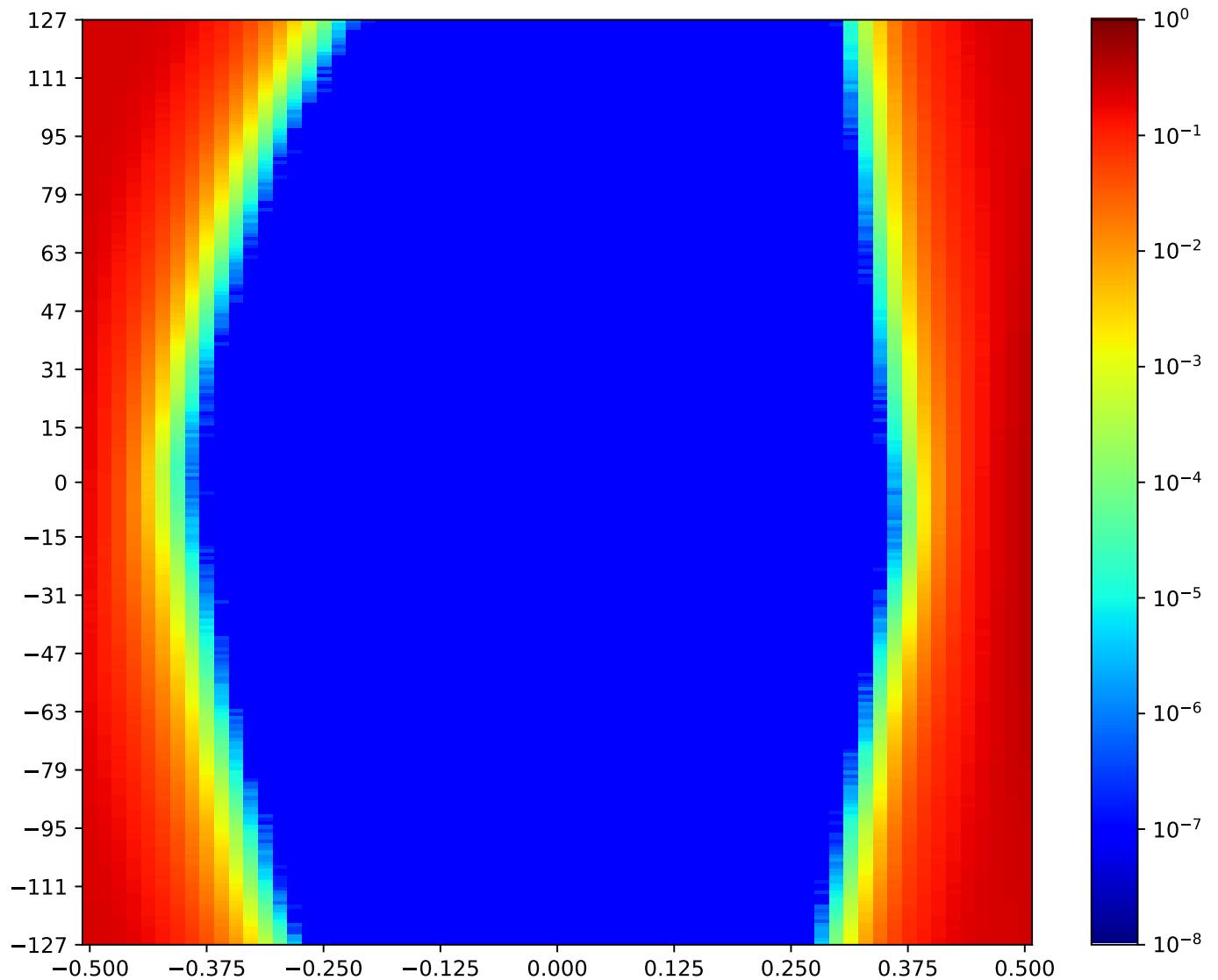


Figure 1.206: MSP\_A\_FPGA-TX2-04-RX10-04-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.16.6 MSP\_A\_FPGA-TX2-05-RX10-05-MSP\_C\_FPGA

Table 1.191: MSP\_A\_FPGA-TX2-05-RX10-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:56:37		2018-Jan-24 16:57:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10066	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

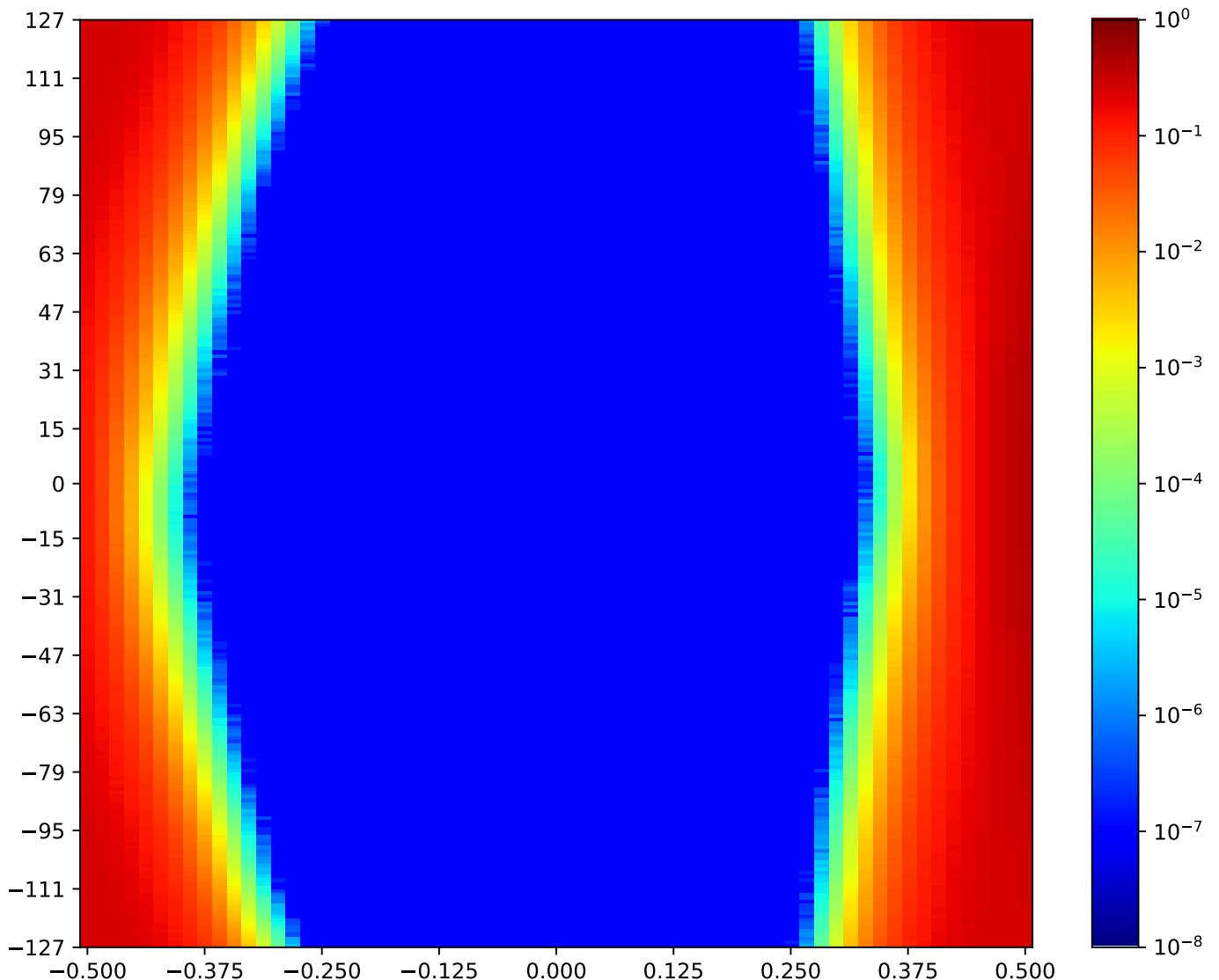


Figure 1.207: MSP\_A\_FPGA-TX2-05-RX10-05-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.16.7 MSP\_A\_FPGA-TX2-06-RX10-06-MSP\_C\_FPGA

Table 1.192: MSP\_A\_FPGA-TX2-06-RX10-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:02:03		2018-Jan-24 17:02:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10811	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

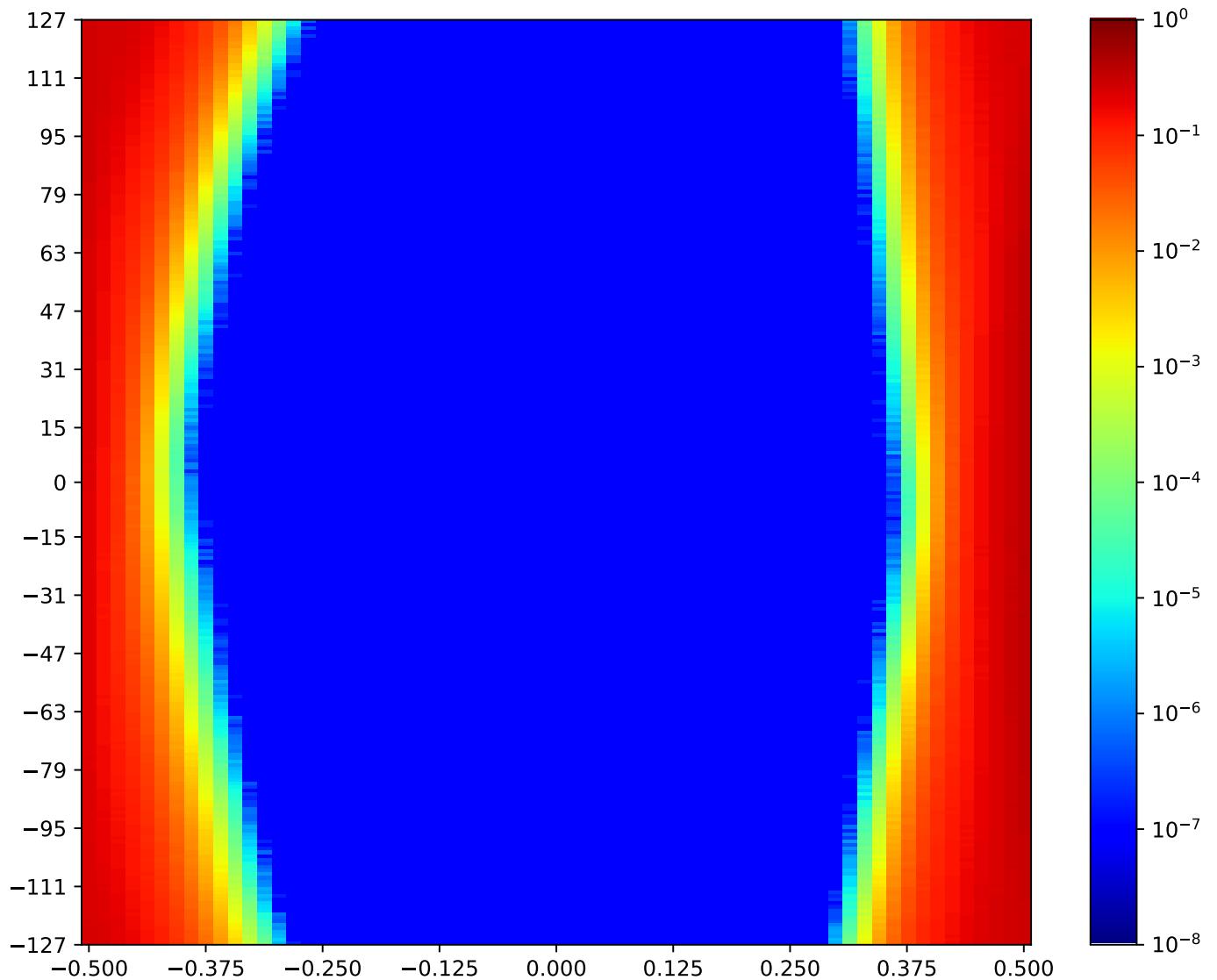


Figure 1.208: MSP\_A\_FPGA-TX2-06-RX10-06-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.16.8 MSP\_A\_FPGA-TX2-07-RX10-07-MSP\_C\_FPGA

Table 1.193: MSP\_A\_FPGA-TX2-07-RX10-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:57:47		2018-Jan-24 16:58:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9804	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

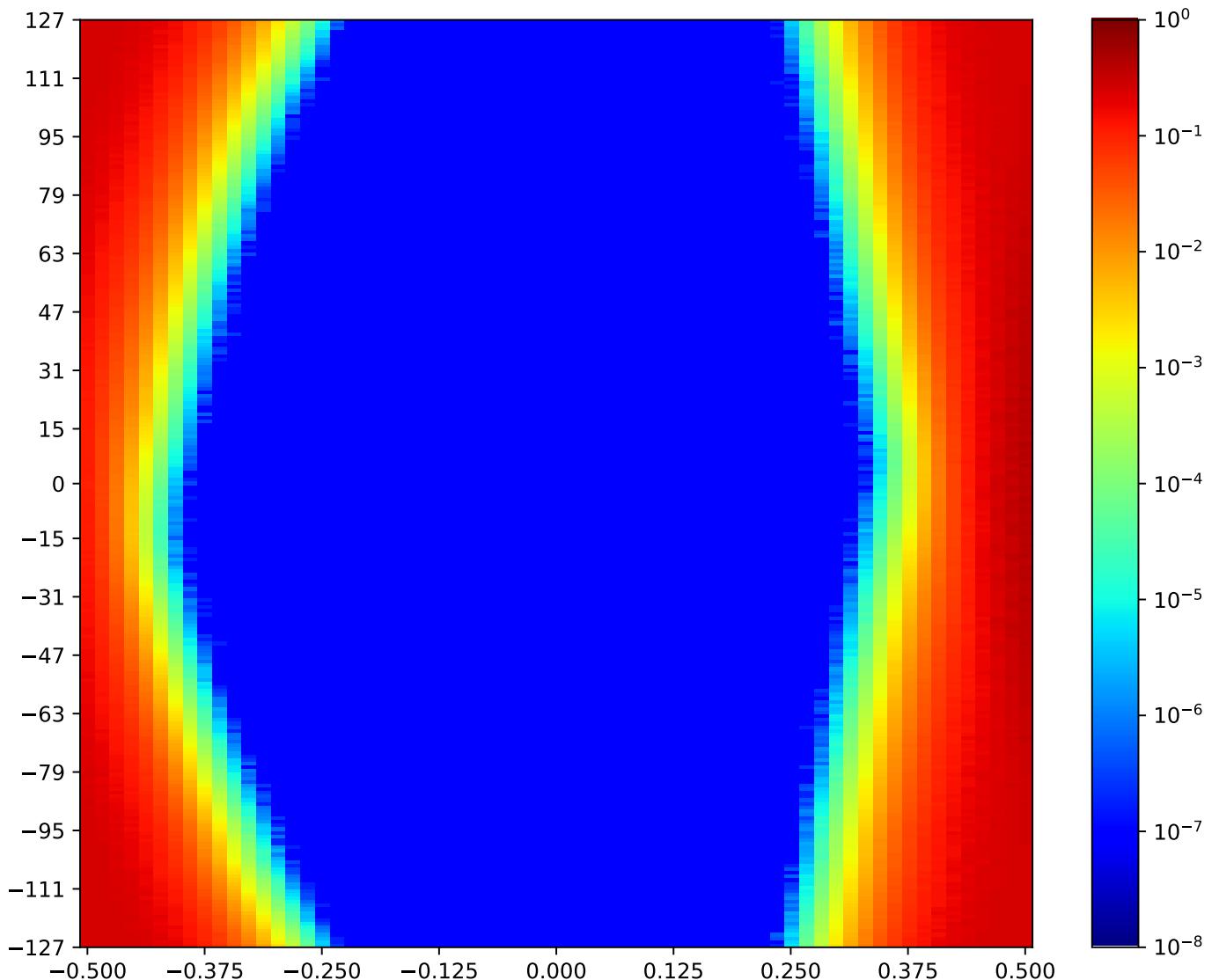


Figure 1.209: MSP\_A\_FPGA-TX2-07-RX10-07-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.16.9 MSP\_A\_FPGA-TX2-08-RX10-08-MSP\_C\_FPGA

Table 1.194: MSP\_A\_FPGA-TX2-08-RX10-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:01:26		2018-Jan-24 17:02:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10399	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

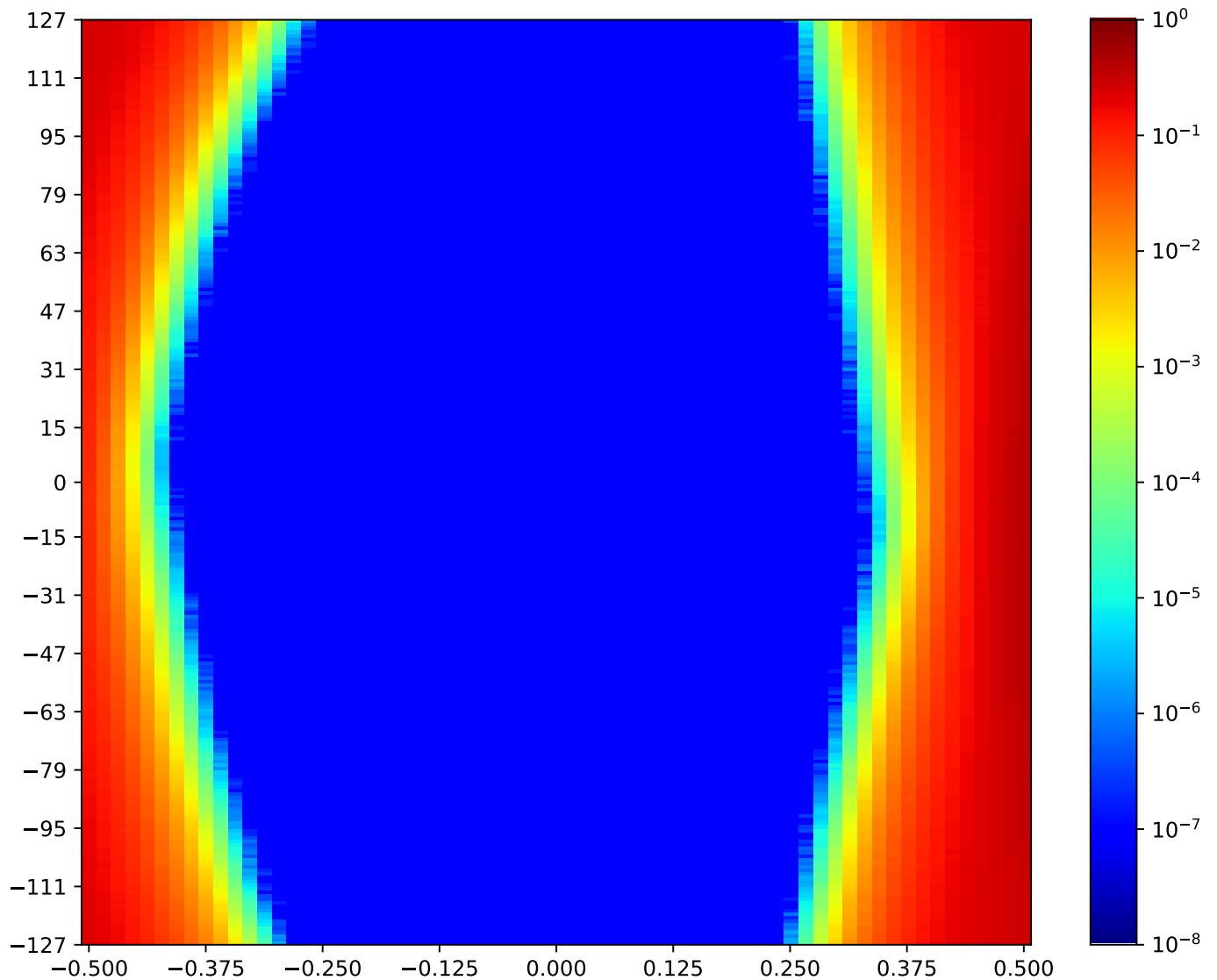


Figure 1.210: MSP\_A\_FPGA-TX2-08-RX10-08-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.16.10 MSP\_A\_FPGA-TX2-09-RX10-09-MSP\_C\_FPGA

Table 1.195: MSP\_A\_FPGA-TX2-09-RX10-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:58:23		2018-Jan-24 16:59:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9677	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

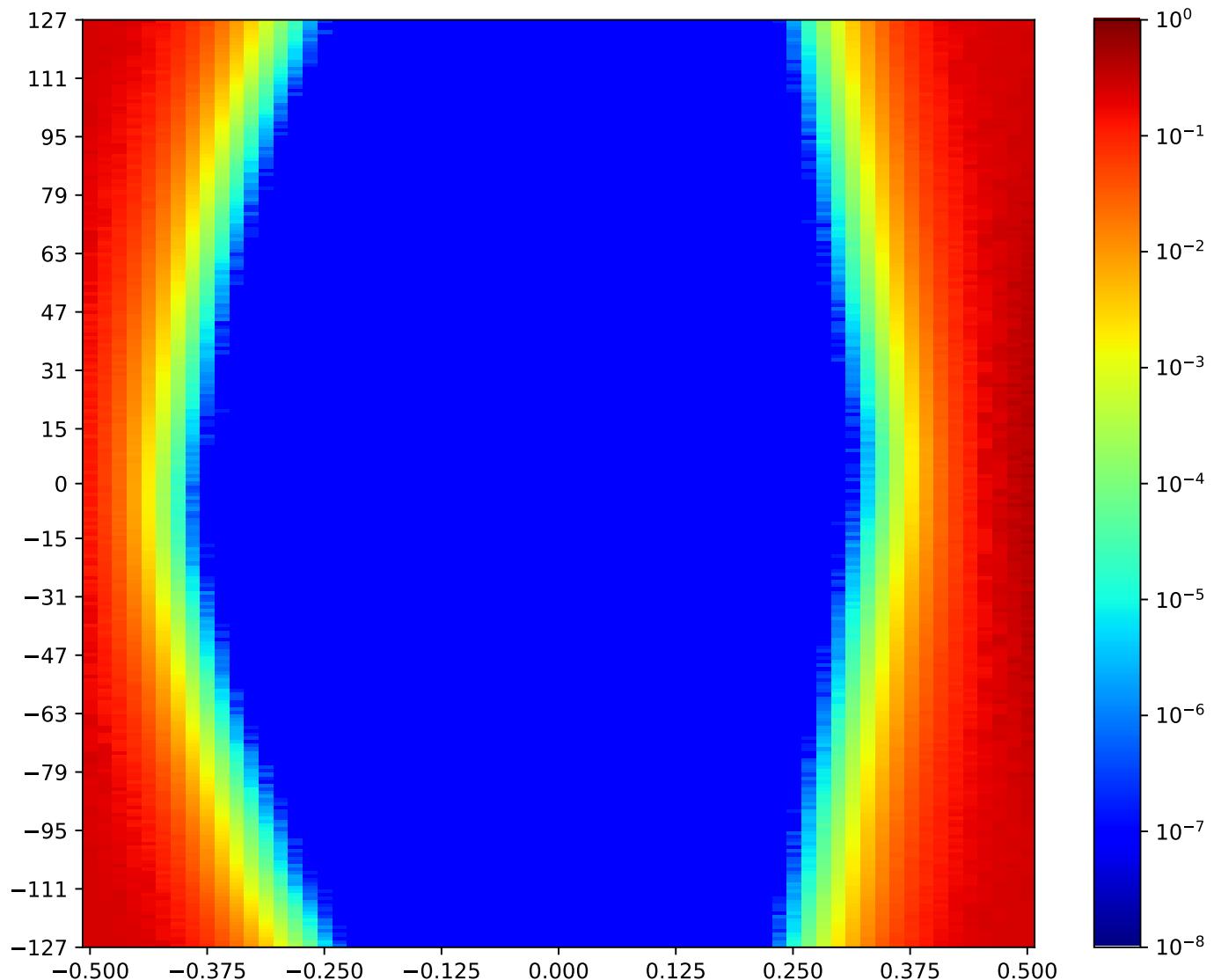


Figure 1.211: MSP\_A\_FPGA-TX2-09-RX10-09-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.16.11 MSP\_A\_FPGA-TX2-10-RX10-10-MSP\_C\_FPGA

Table 1.196: MSP\_A\_FPGA-TX2-10-RX10-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:00:13		2018-Jan-24 17:00:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10521	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

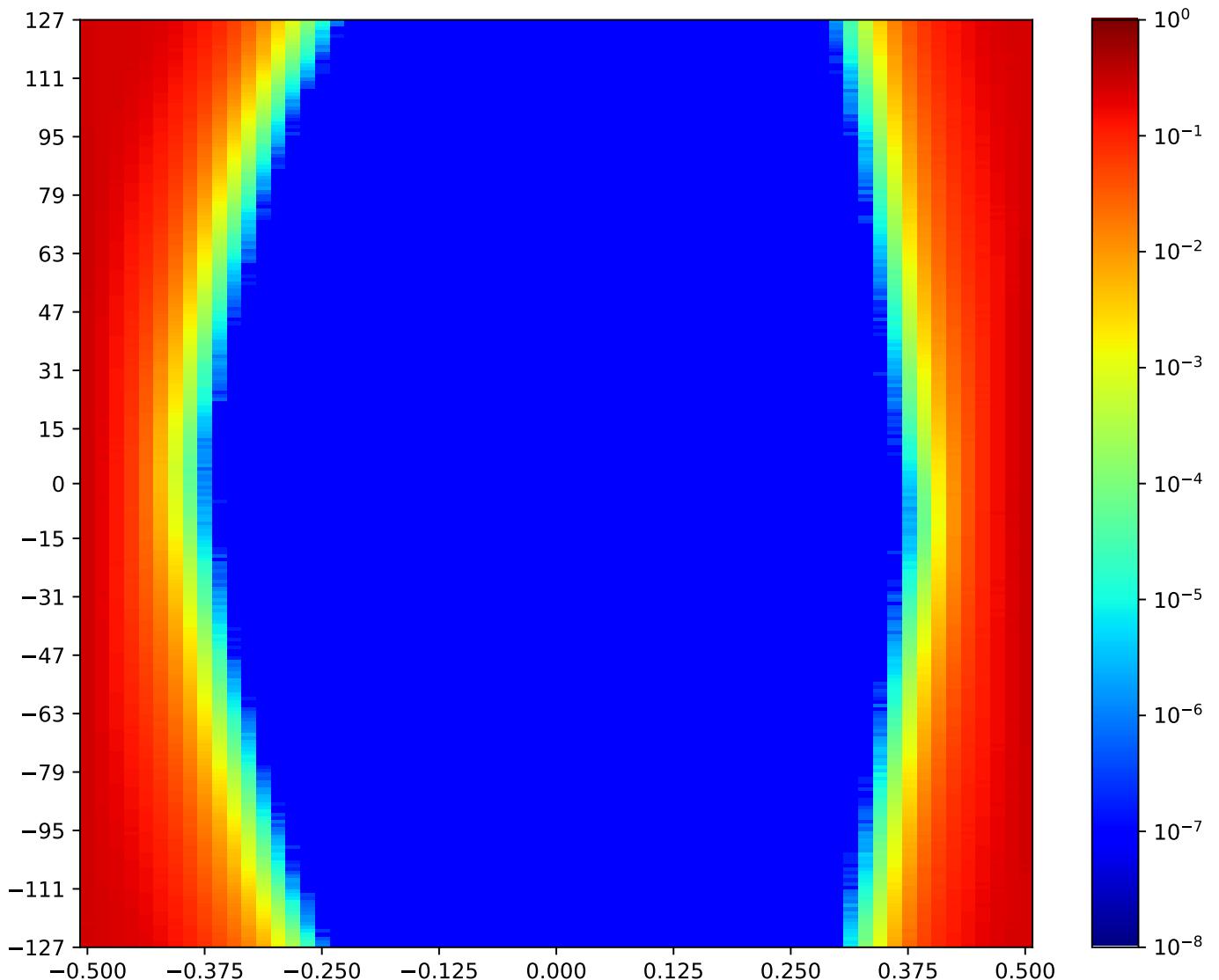


Figure 1.212: MSP\_A\_FPGA-TX2-10-RX10-10-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.16.12 MSP\_A\_FPGA-TX2-11-RX10-11-MSP\_C\_FPGA

Table 1.197: MSP\_A\_FPGA-TX2-11-RX10-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:59:36		2018-Jan-24 17:00:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9373	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

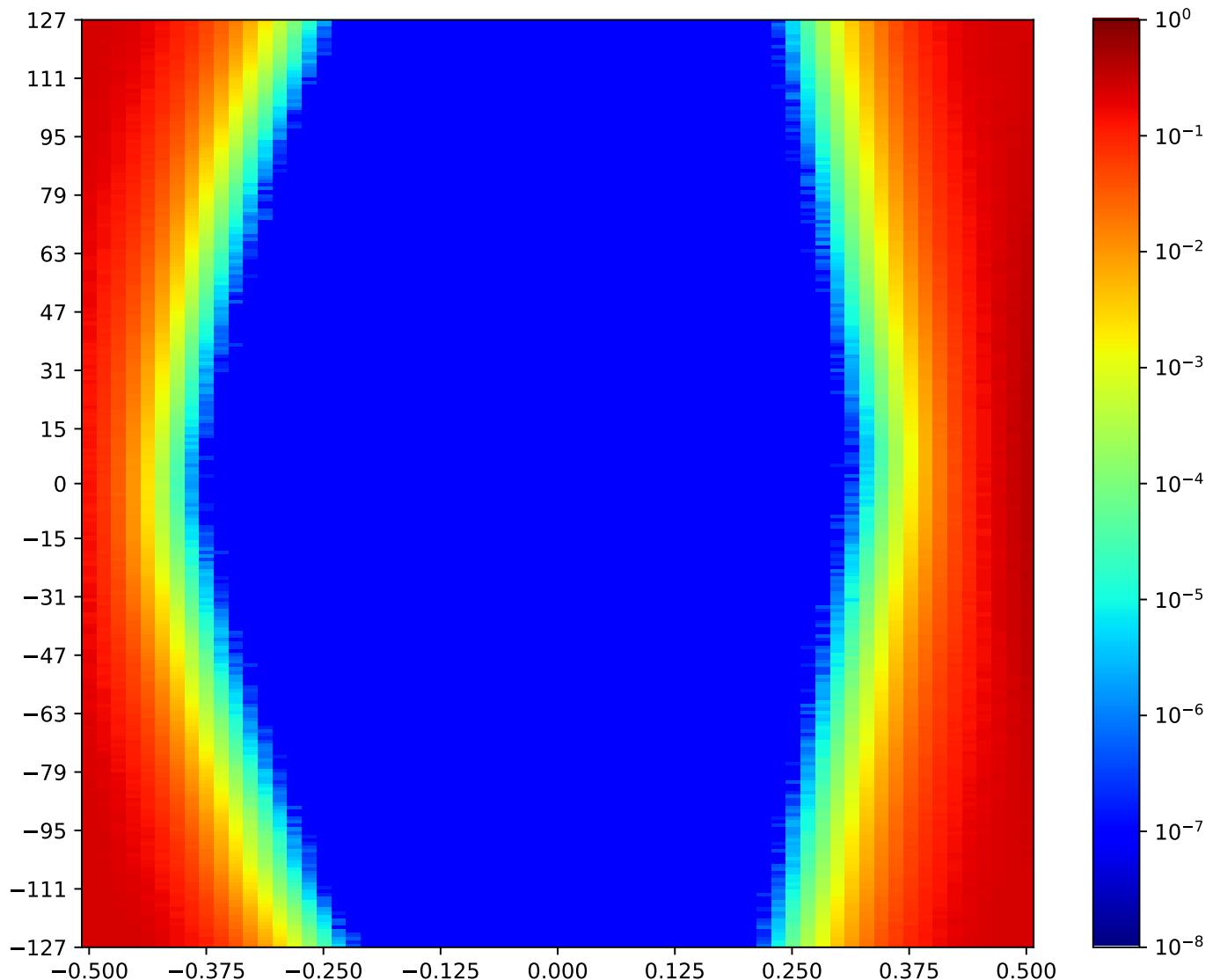


Figure 1.213: MSP\_A\_FPGA-TX2-11-RX10-11-MSP\_C\_FPGA

Call back to summary Figure 1.201. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.17 MSP\_C TX3 MSP\_A RX2 Minipod Loopback

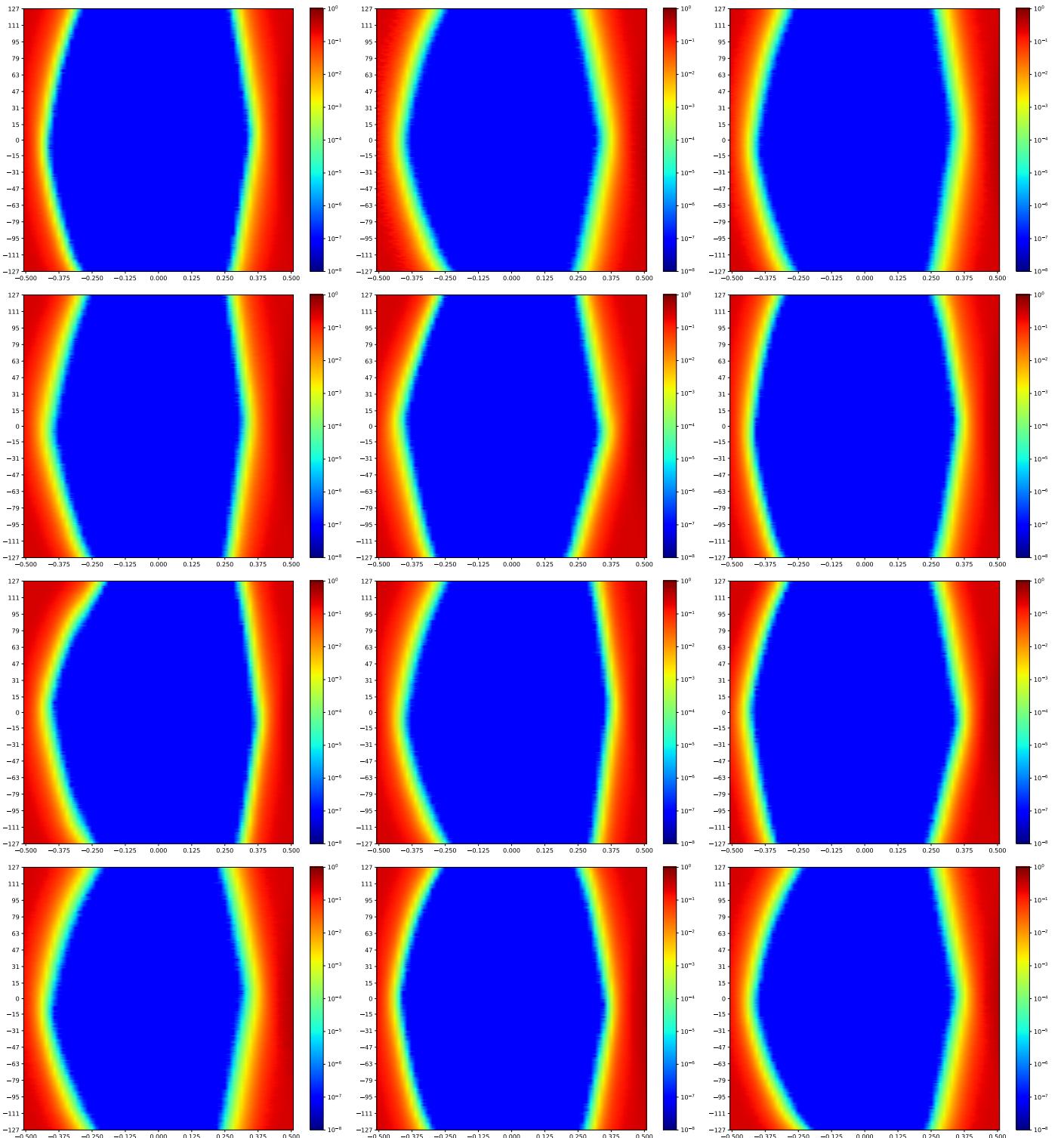


Figure 1.214: MSP\_C TX3 MSP\_A RX2 Minipod Loopback

A cross-reference to Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.227.

### 1.17.1 MSP\_C\_FPGA-TX3-00-RX2-00-MSP\_A\_FPGA

Table 1.198: MSP\_C\_FPGA-TX3-00-RX2-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:04:29		2018-Jan-24 17:05:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10572	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

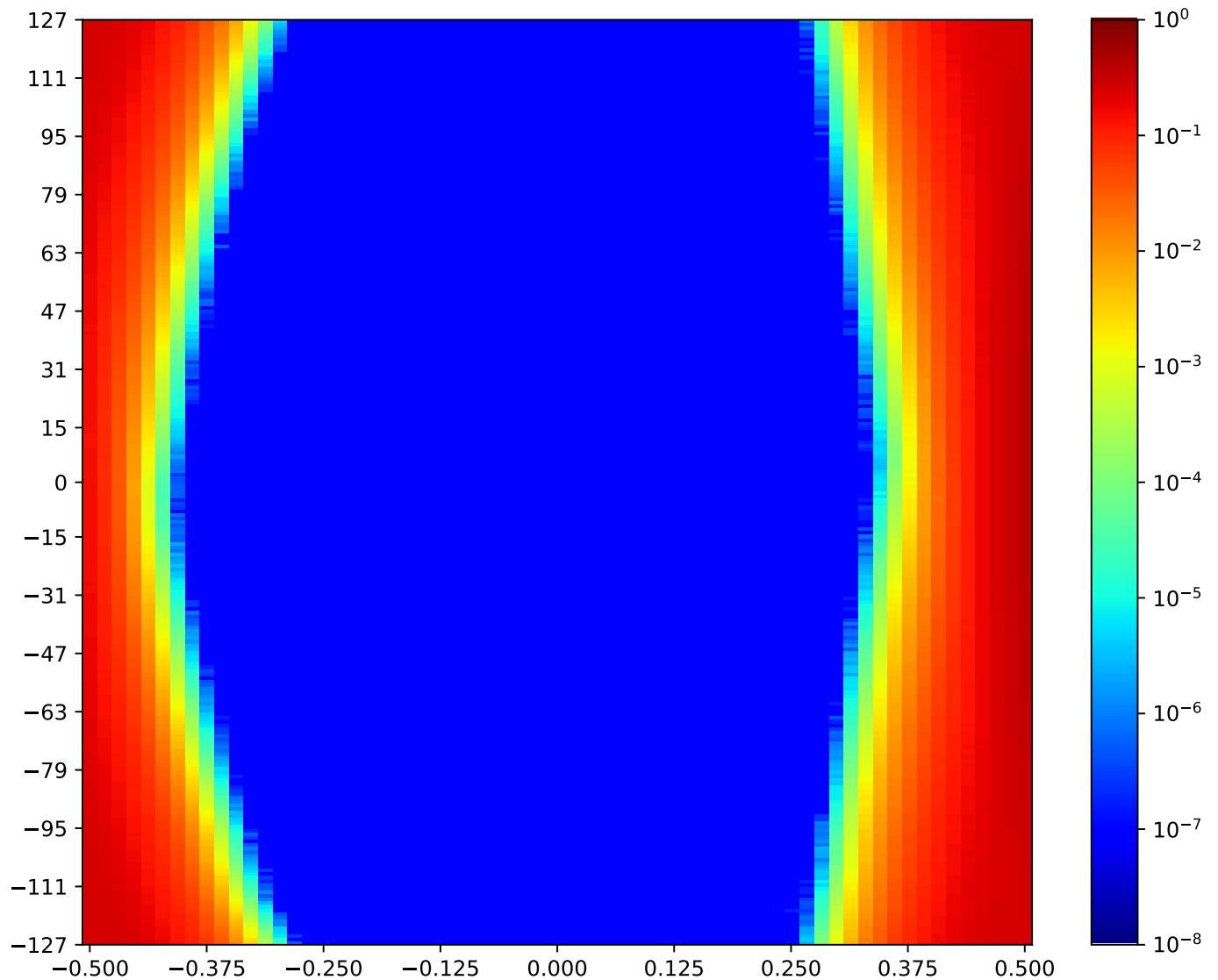


Figure 1.215: MSP\_C\_FPGA-TX3-00-RX2-00-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.2 MSP\_C\_FPGA-TX3-01-RX2-01-MSP\_A\_FPGA

Table 1.199: MSP\_C\_FPGA-TX3-01-RX2-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:05:42		2018-Jan-24 17:06:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9499	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

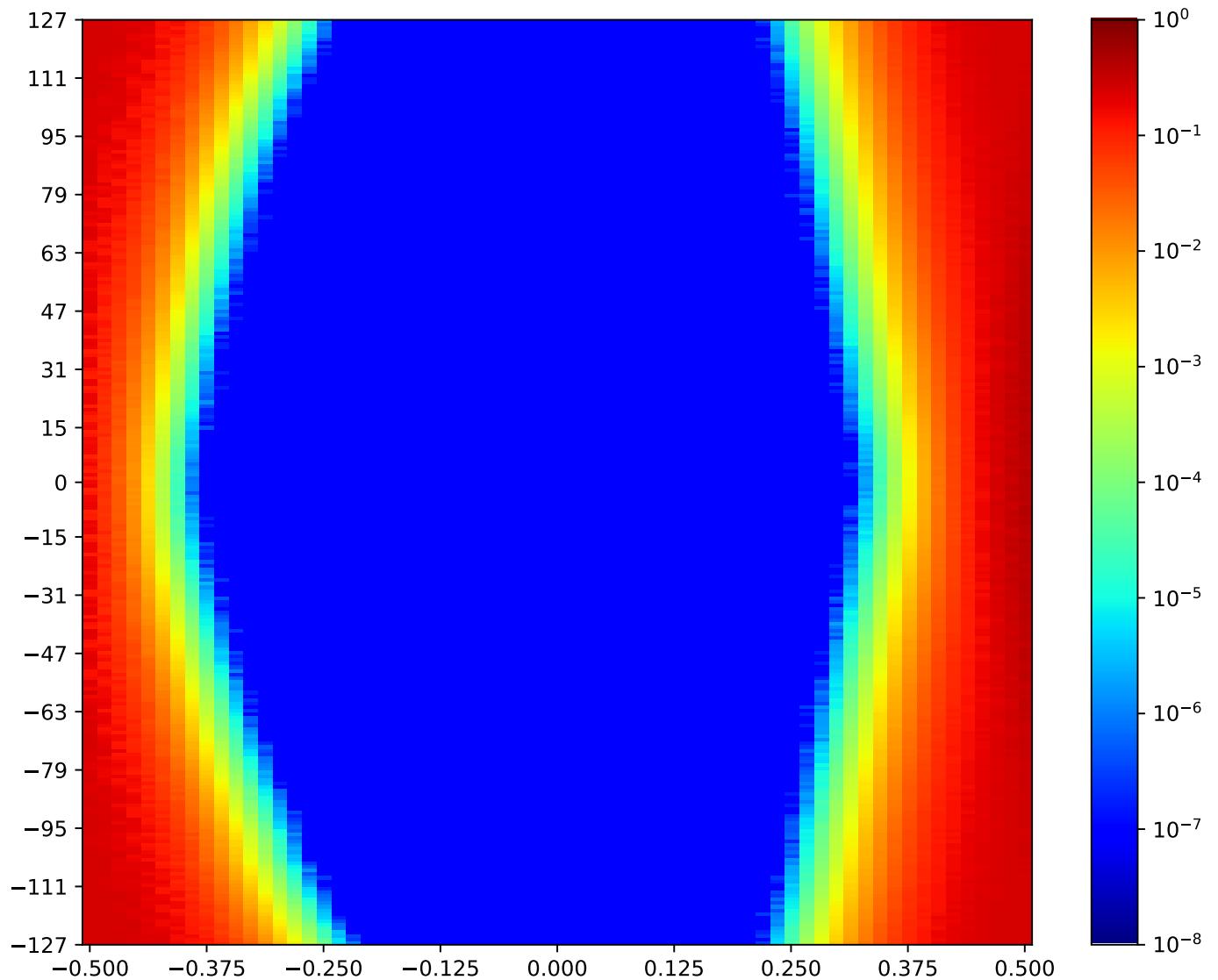


Figure 1.216: MSP\_C\_FPGA-TX3-01-RX2-01-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.3 MSP\_C\_FPGA-TX3-02-RX2-02-MSP\_A\_FPGA

Table 1.200: MSP\_C\_FPGA-TX3-02-RX2-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:06:20		2018-Jan-24 17:06:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9884	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

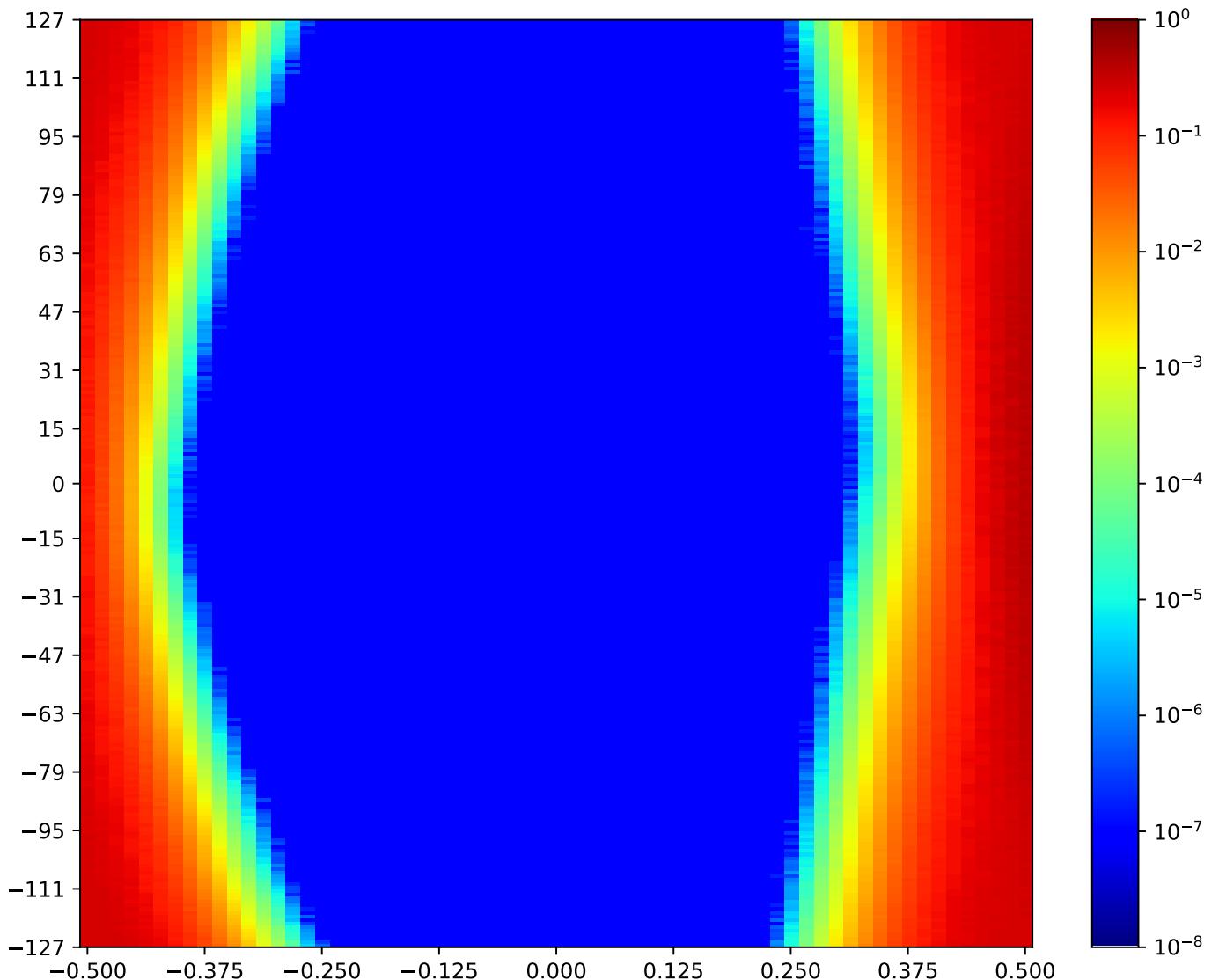


Figure 1.217: MSP\_C\_FPGA-TX3-02-RX2-02-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.17.4 MSP\_C\_FPGA-TX3-03-RX2-03-MSP\_A\_FPGA

Table 1.201: MSP\_C\_FPGA-TX3-03-RX2-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:03:16		2018-Jan-24 17:03:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9661	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

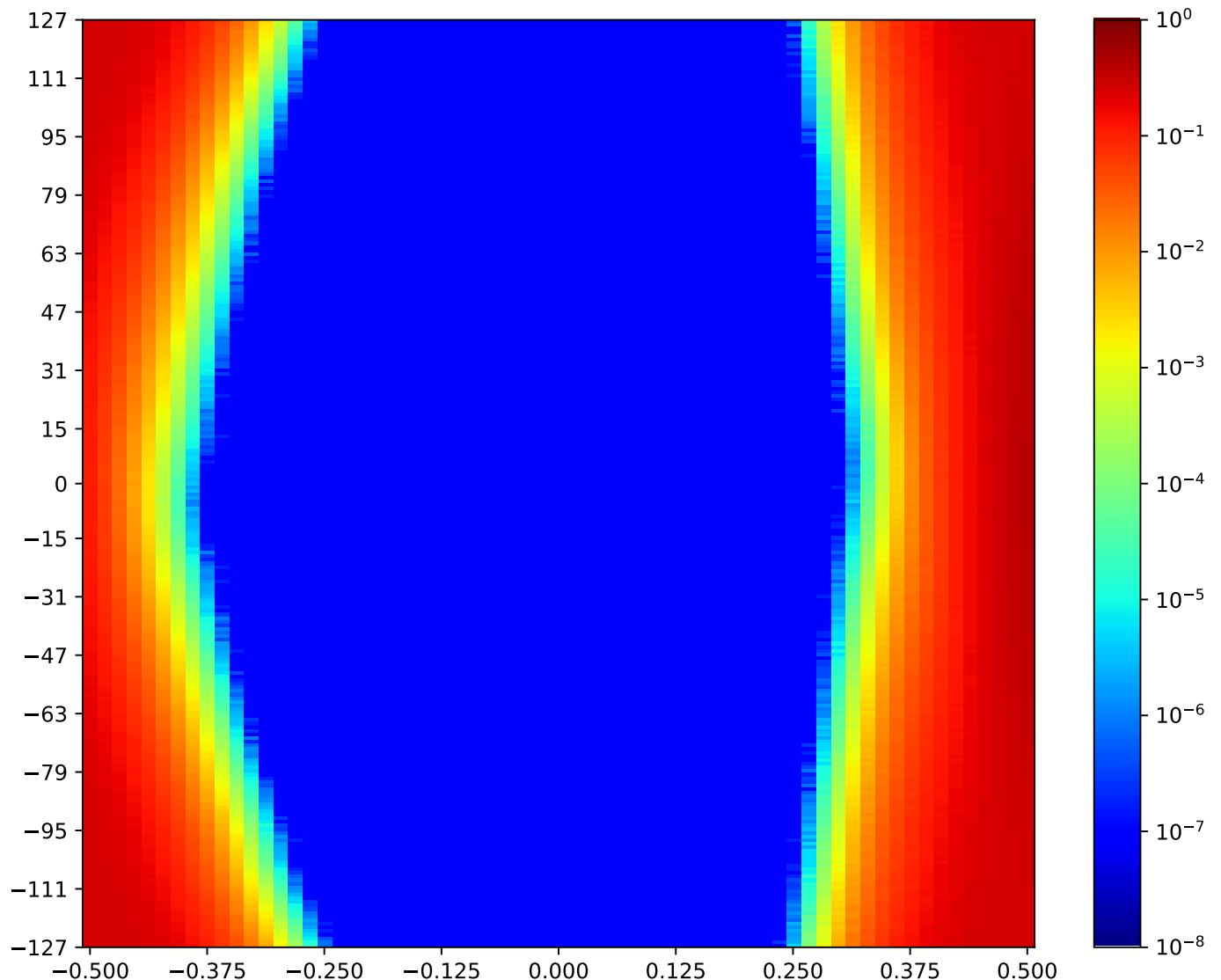


Figure 1.218: MSP\_C\_FPGA-TX3-03-RX2-03-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.5 MSP\_C\_FPGA-TX3-04-RX2-04-MSP\_A\_FPGA

Table 1.202: MSP\_C\_FPGA-TX3-04-RX2-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:08:11		2018-Jan-24 17:08:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9647	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

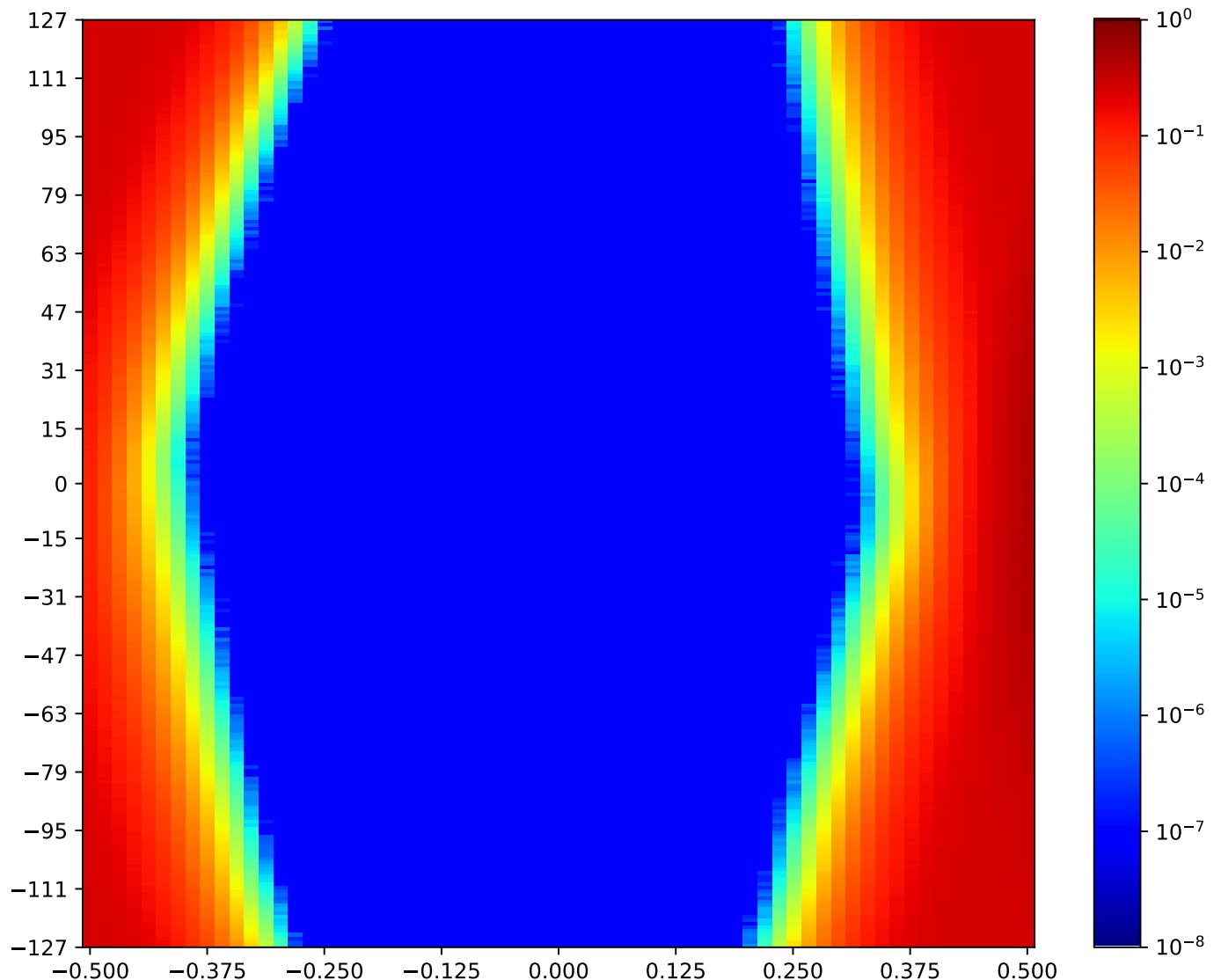


Figure 1.219: MSP\_C\_FPGA-TX3-04-RX2-04-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.6 MSP\_C\_FPGA-TX3-05-RX2-05-MSP\_A\_FPGA

Table 1.203: MSP\_C\_FPGA-TX3-05-RX2-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:02:40		2018-Jan-24 17:03:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10571	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

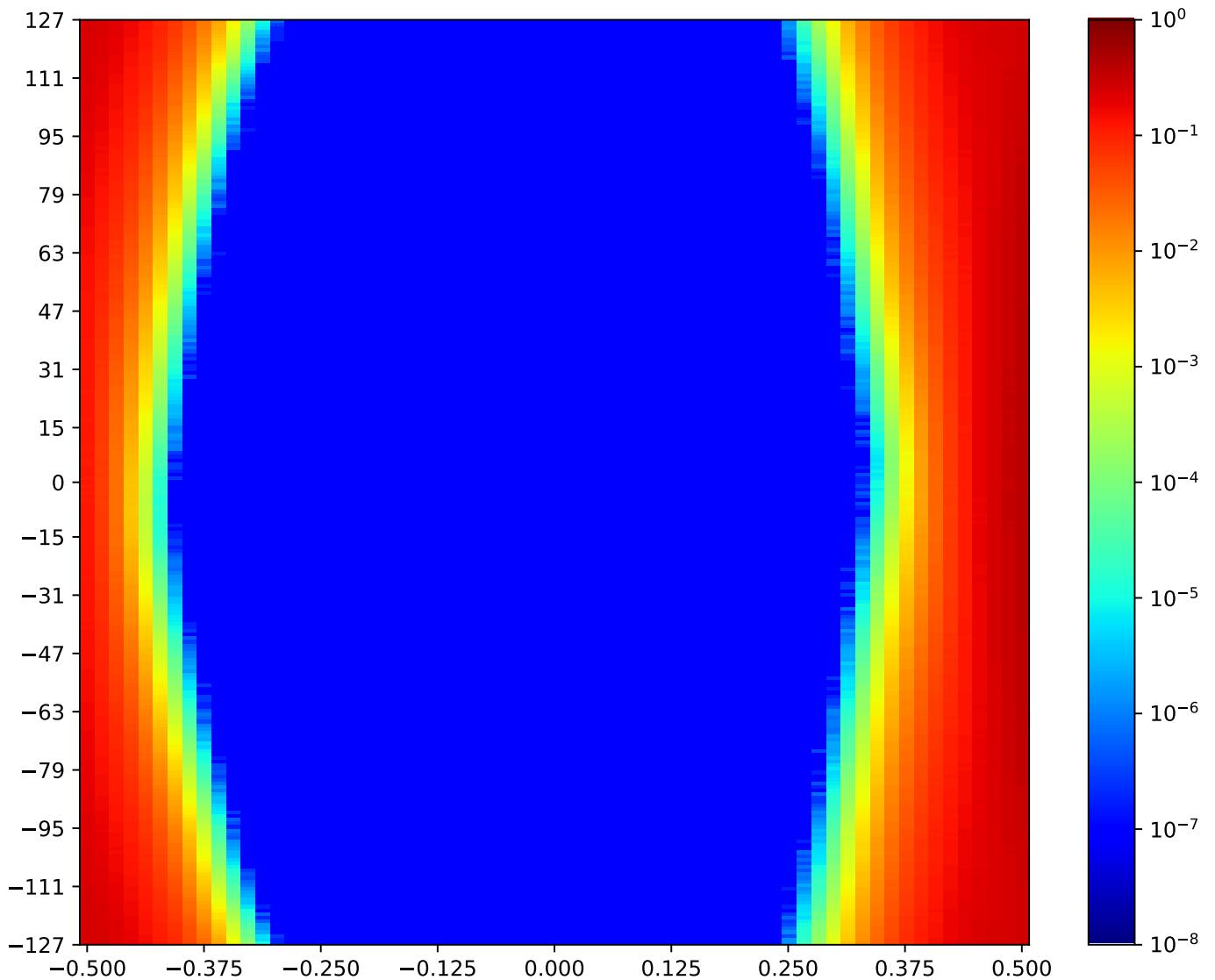


Figure 1.220: MSP\_C\_FPGA-TX3-05-RX2-05-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.7 MSP\_C\_FPGA-TX3-06-RX2-06-MSP\_A\_FPGA

Table 1.204: MSP\_C\_FPGA-TX3-06-RX2-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:09:24		2018-Jan-24 17:10:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10302	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

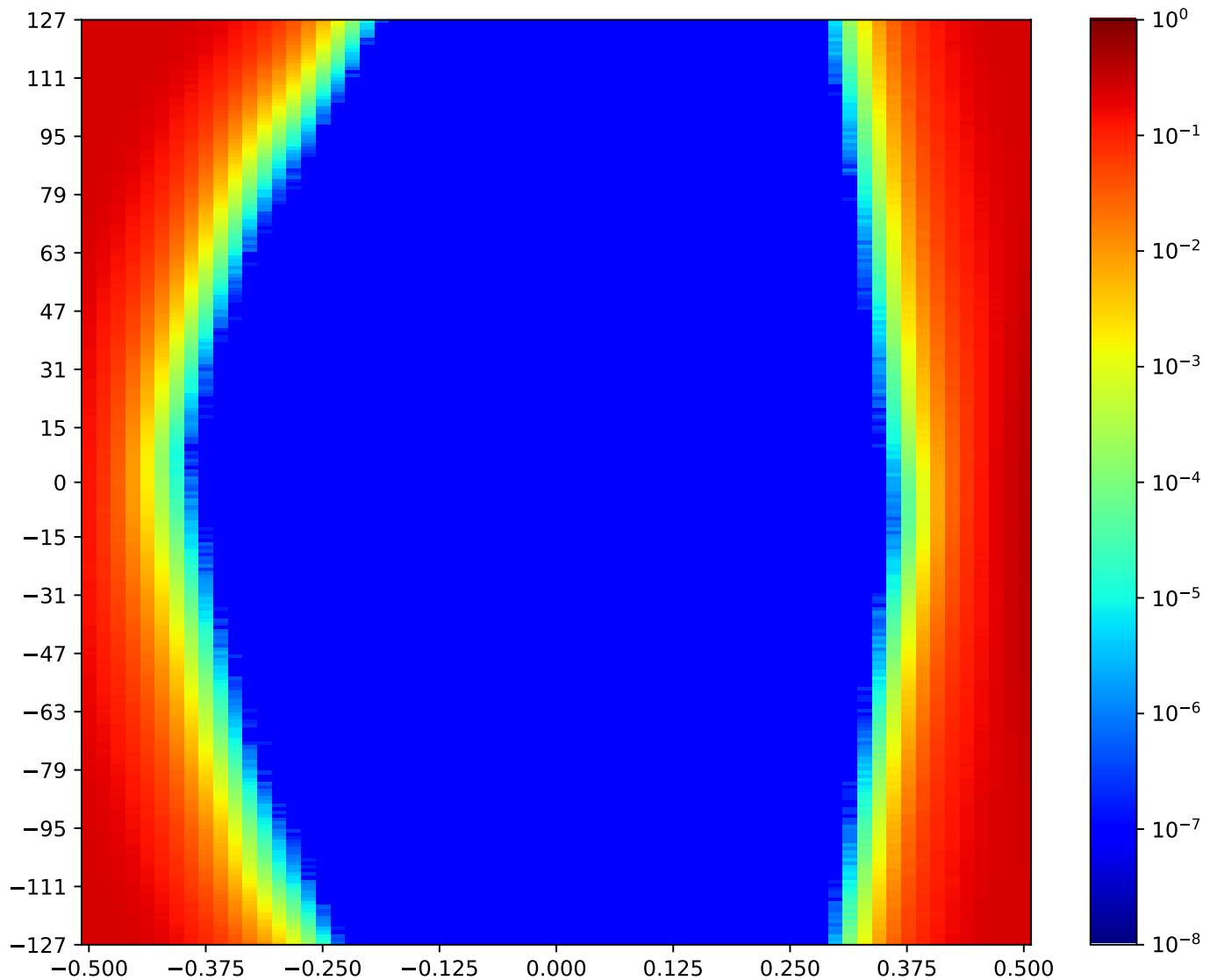


Figure 1.221: MSP\_C\_FPGA-TX3-06-RX2-06-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.8 MSP\_C\_FPGA-TX3-07-RX2-07-MSP\_A\_FPGA

Table 1.205: MSP\_C\_FPGA-TX3-07-RX2-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:03:51		2018-Jan-24 17:04:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10336	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

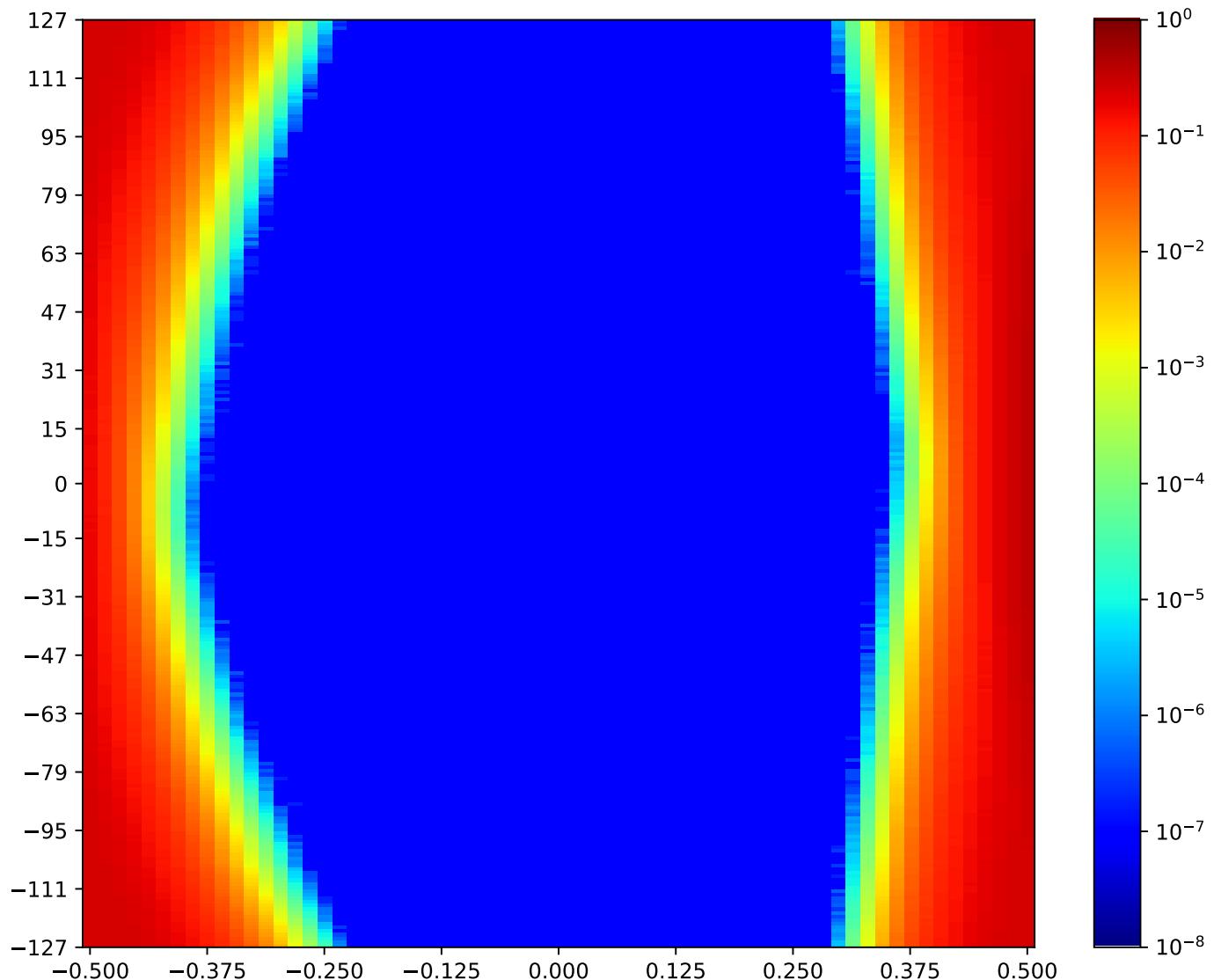


Figure 1.222: MSP\_C\_FPGA-TX3-07-RX2-07-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.9 MSP\_C\_FPGA-TX3-08-RX2-08-MSP\_A\_FPGA

Table 1.206: MSP\_C\_FPGA-TX3-08-RX2-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:08:47		2018-Jan-24 17:09:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10515	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

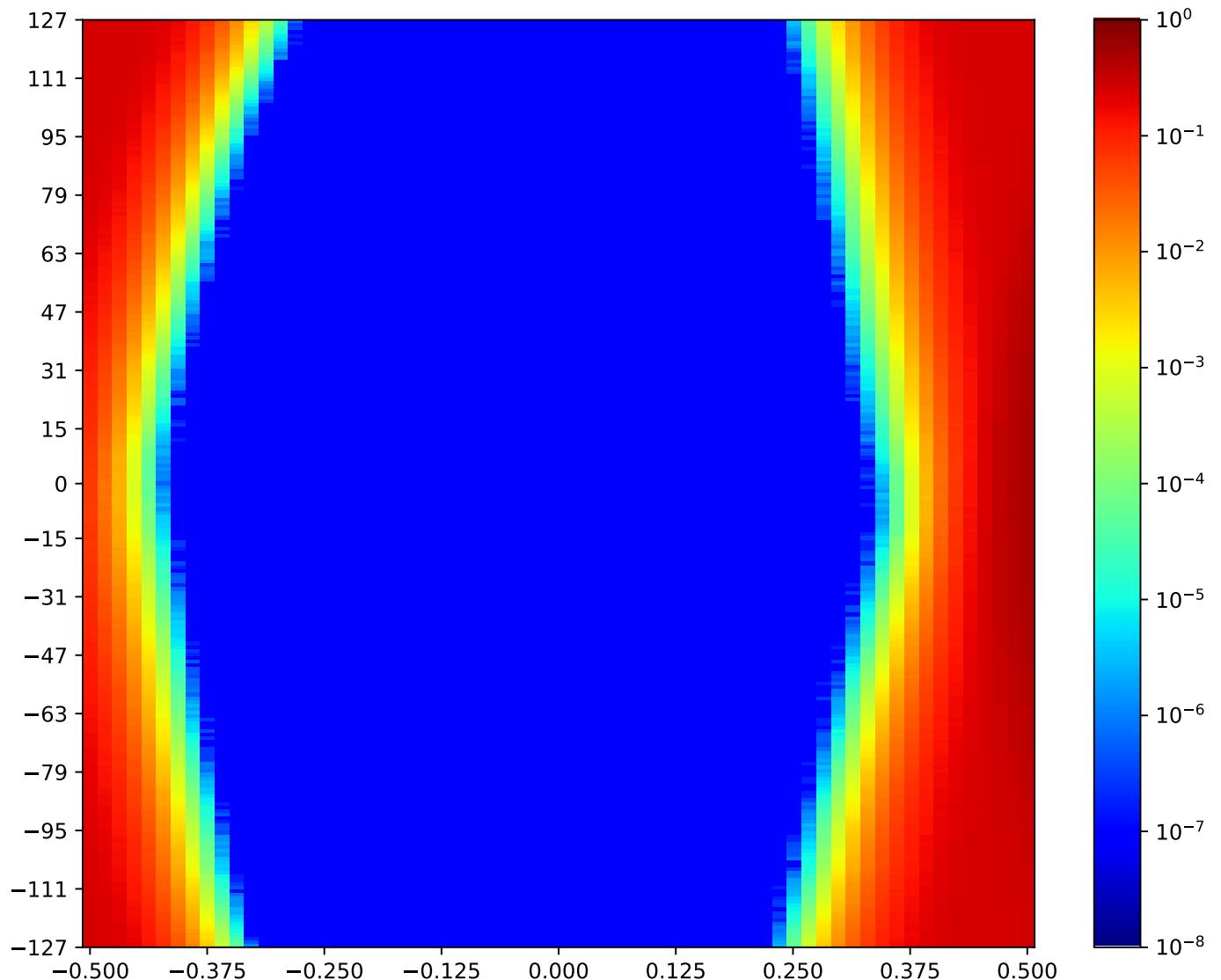


Figure 1.223: MSP\_C\_FPGA-TX3-08-RX2-08-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.10 MSP\_C\_FPGA-TX3-09-RX2-09-MSP\_A\_FPGA

Table 1.207: MSP\_C\_FPGA-TX3-09-RX2-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:05:06		2018-Jan-24 17:05:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9389	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

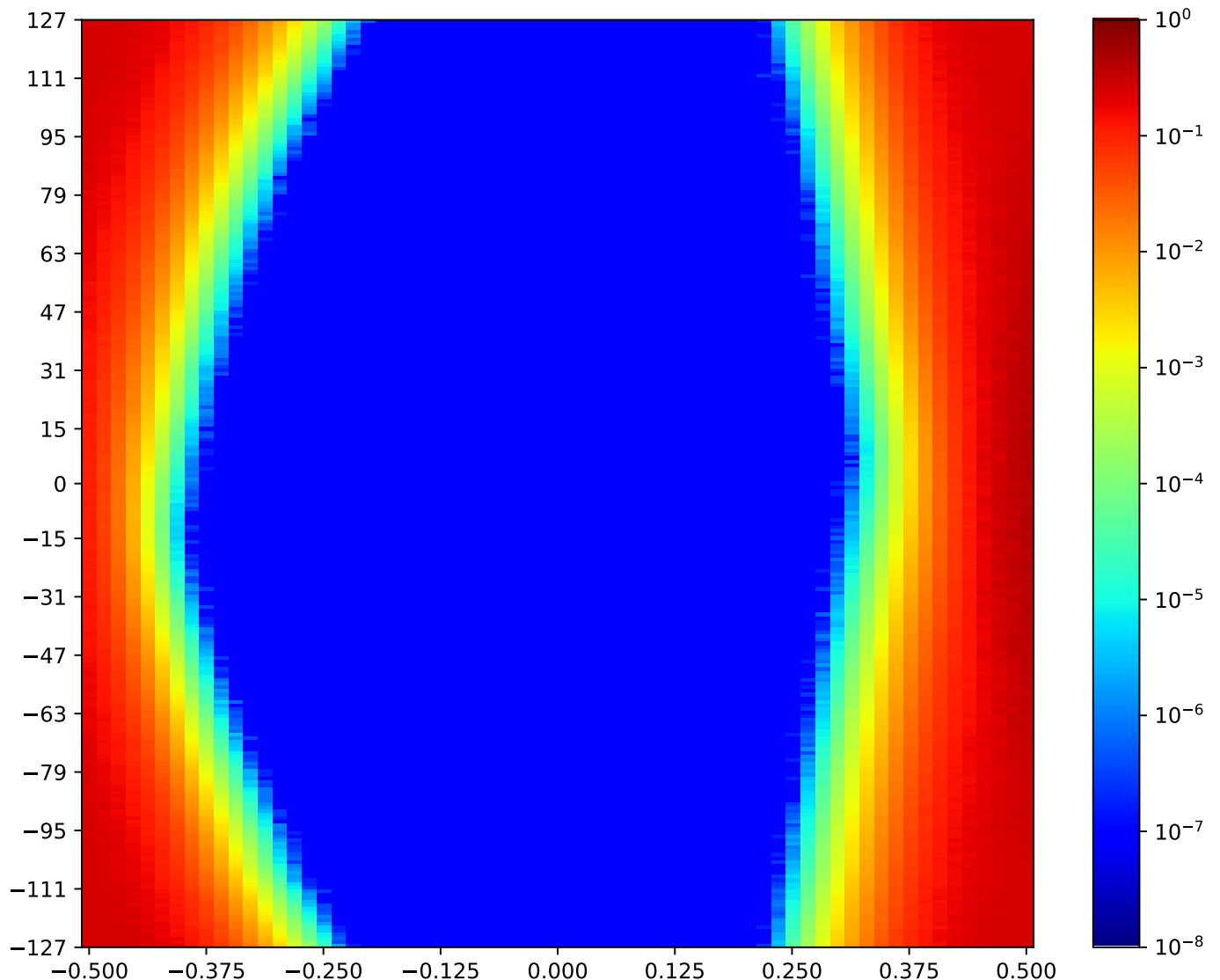


Figure 1.224: MSP\_C\_FPGA-TX3-09-RX2-09-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.11 MSP\_C\_FPGA-TX3-10-RX2-10-MSP\_A\_FPGA

Table 1.208: MSP\_C\_FPGA-TX3-10-RX2-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:07:34		2018-Jan-24 17:08:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10517	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

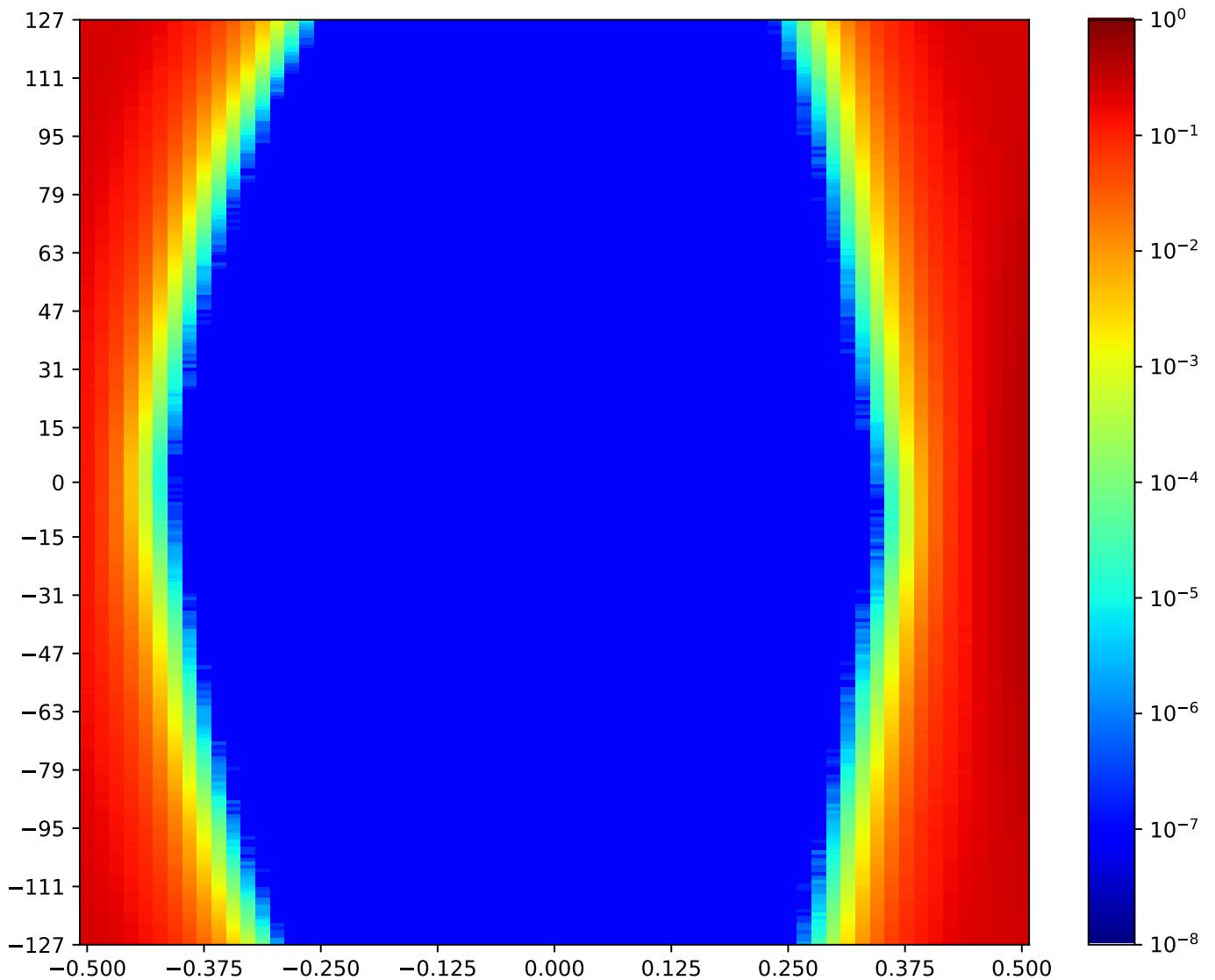


Figure 1.225: MSP\_C\_FPGA-TX3-10-RX2-10-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.17.12 MSP\_C\_FPGA-TX3-11-RX2-11-MSP\_A\_FPGA

Table 1.209: MSP\_C\_FPGA-TX3-11-RX2-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:06:57		2018-Jan-24 17:07:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9717	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

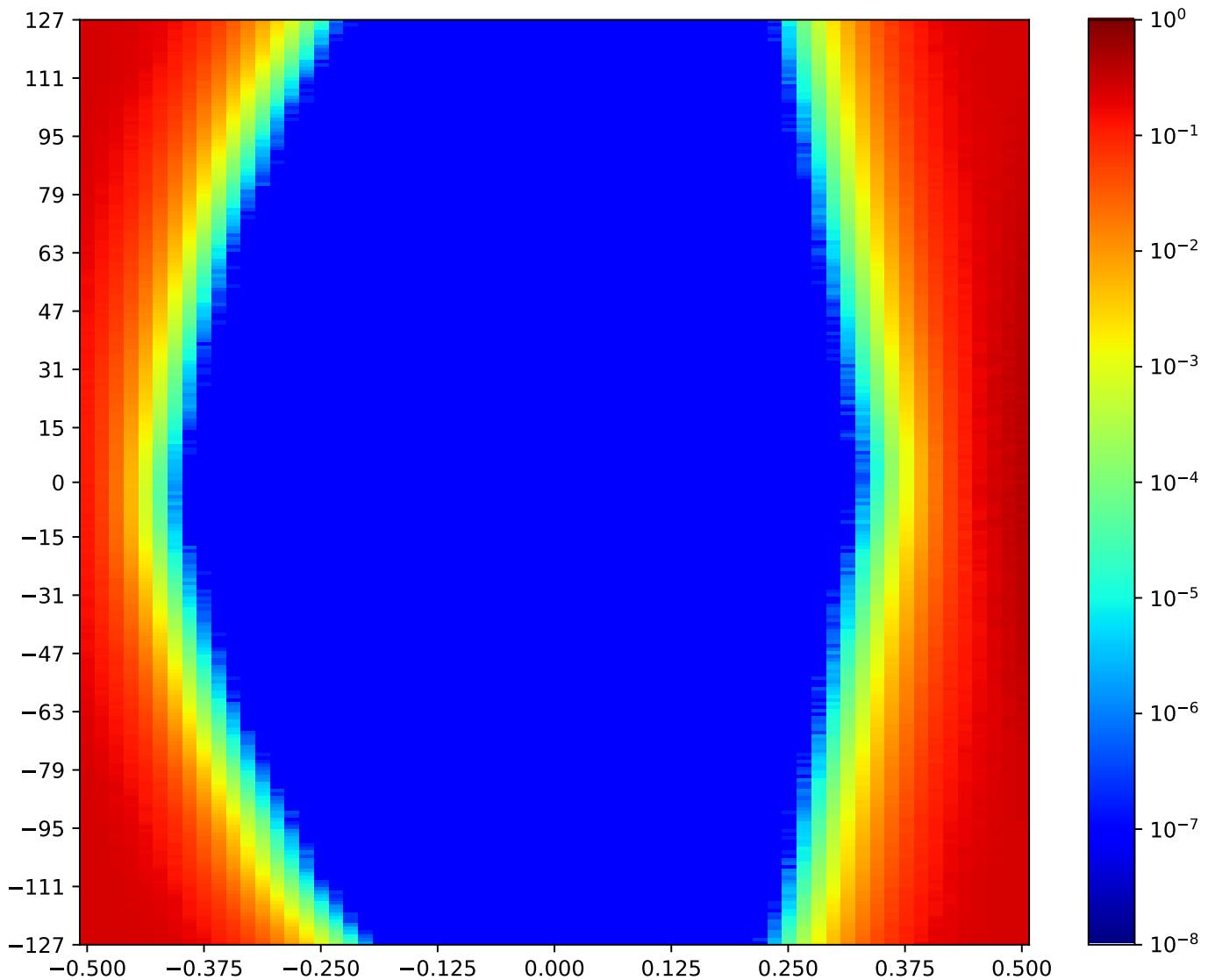


Figure 1.226: MSP\_C\_FPGA-TX3-11-RX2-11-MSP\_A\_FPGA

Call back to summary Figure 1.214. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.18 MSP\_C TX4 MSP\_A RX1 Minipod Loopback

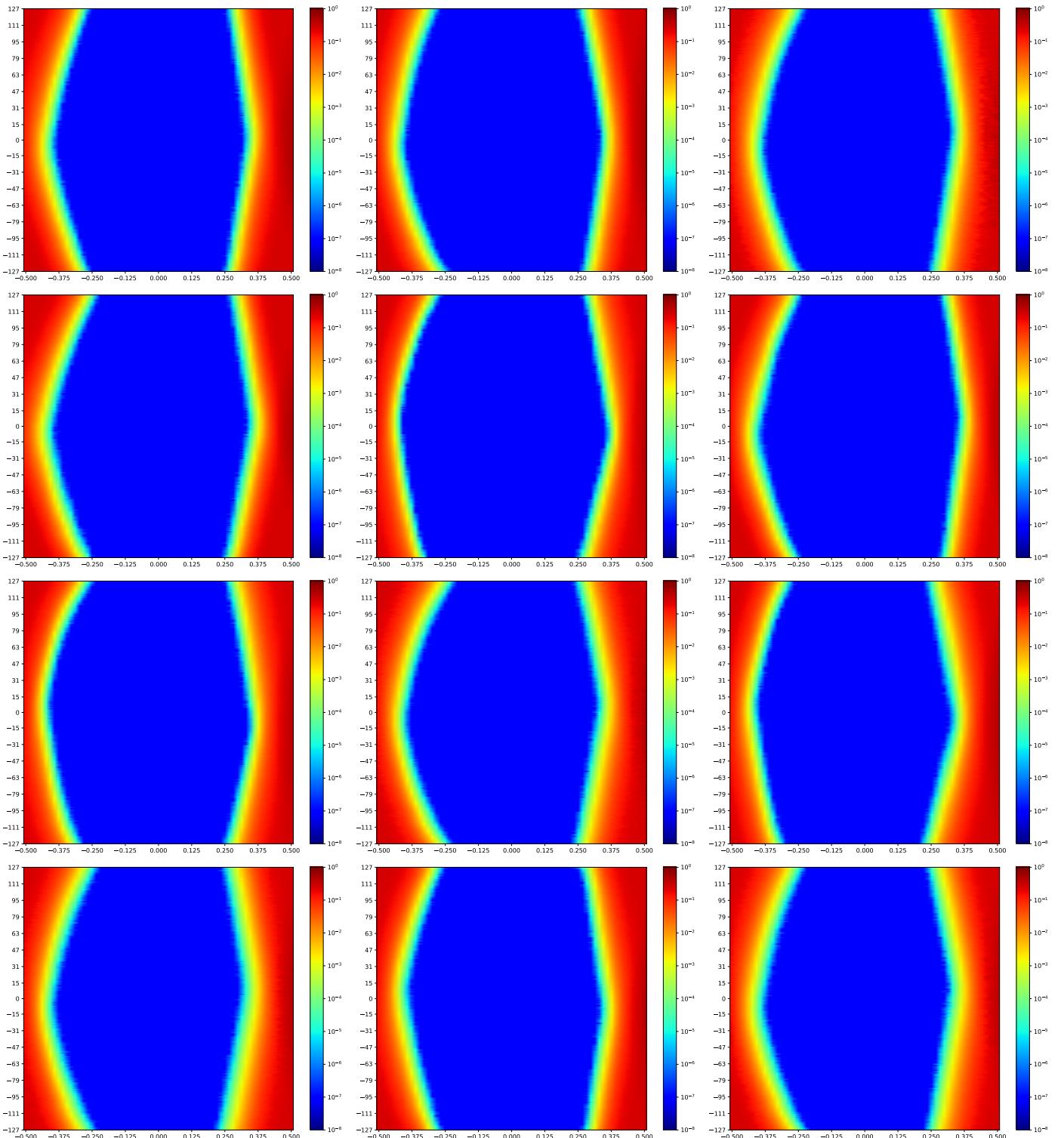


Figure 1.227: MSP\_C TX4 MSP\_A RX1 Minipod Loopback

A cross-reference to Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.240.

### 1.18.1 MSP\_C\_FPGA-TX4-00-RX1-00-MSP\_A\_FPGA

Table 1.210: MSP\_C\_FPGA-TX4-00-RX1-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:11:51		2018-Jan-24 17:12:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9864	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

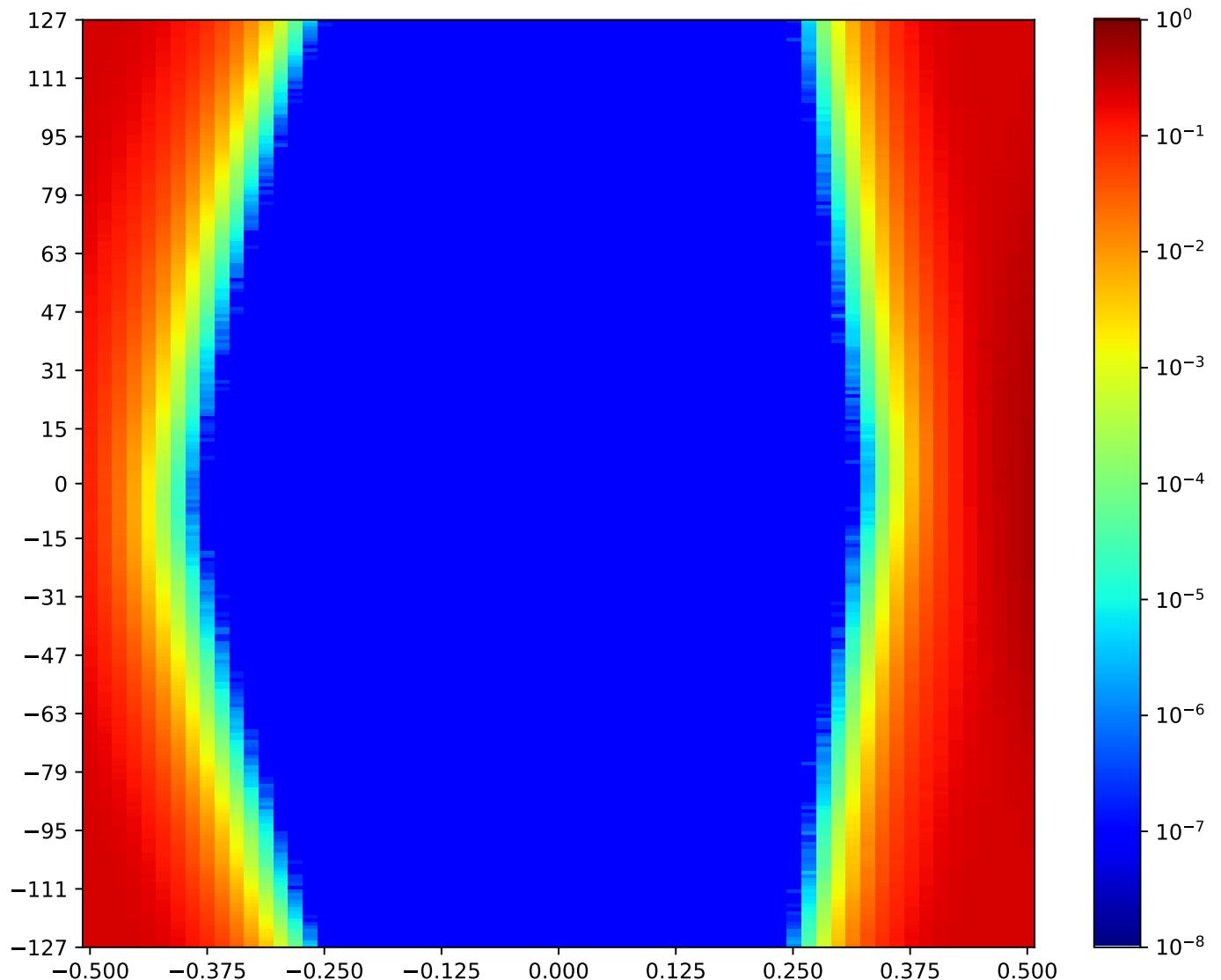


Figure 1.228: MSP\_C\_FPGA-TX4-00-RX1-00-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.2 MSP\_C\_FPGA-TX4-01-RX1-01-MSP\_A\_FPGA

Table 1.211: MSP\_C\_FPGA-TX4-01-RX1-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:10:38		2018-Jan-24 17:11:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10164	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

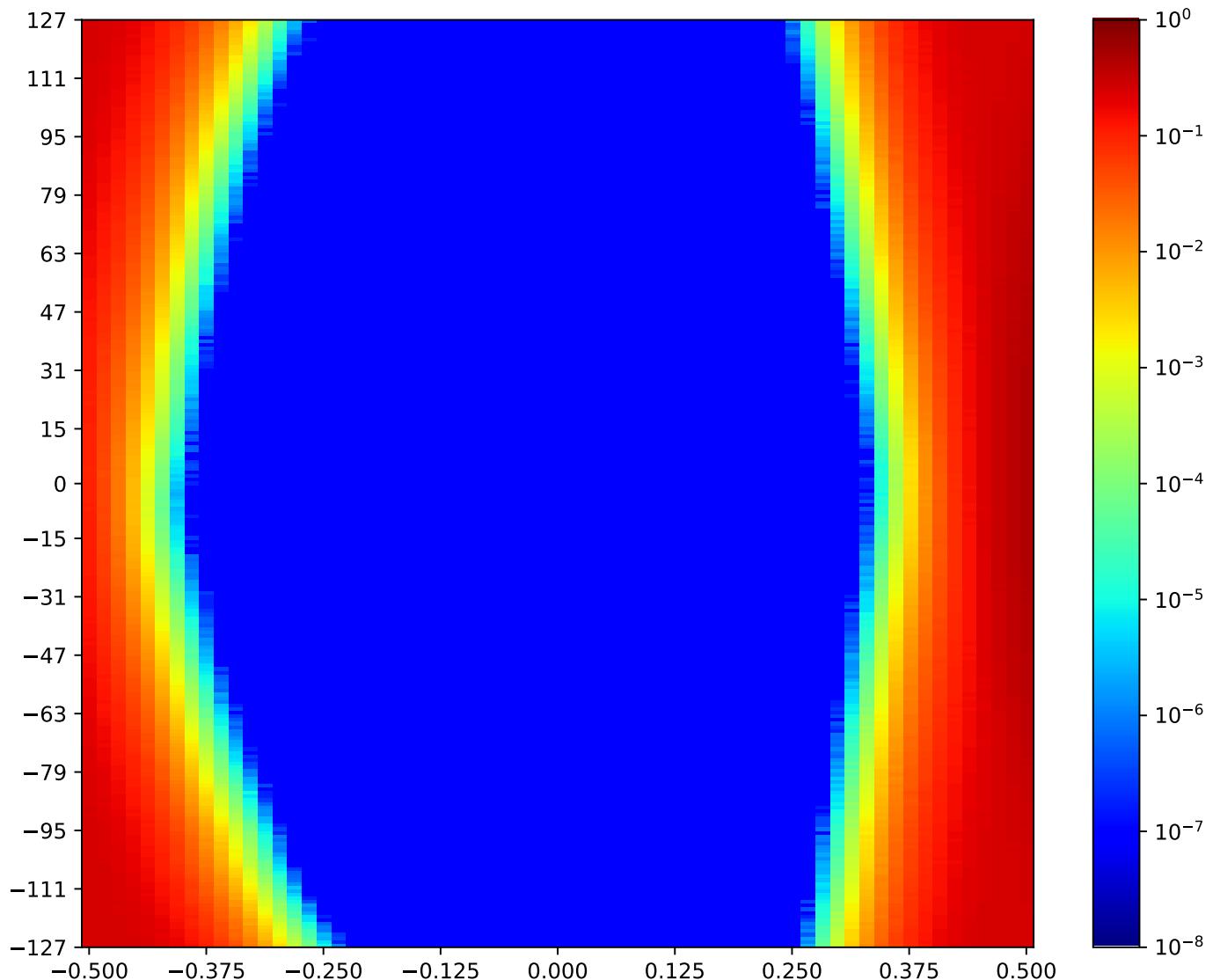


Figure 1.229: MSP\_C\_FPGA-TX4-01-RX1-01-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.3 MSP\_C\_FPGA-TX4-02-RX1-02-MSP\_A\_FPGA

Table 1.212: MSP\_C\_FPGA-TX4-02-RX1-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:13:40		2018-Jan-24 17:14:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9515	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

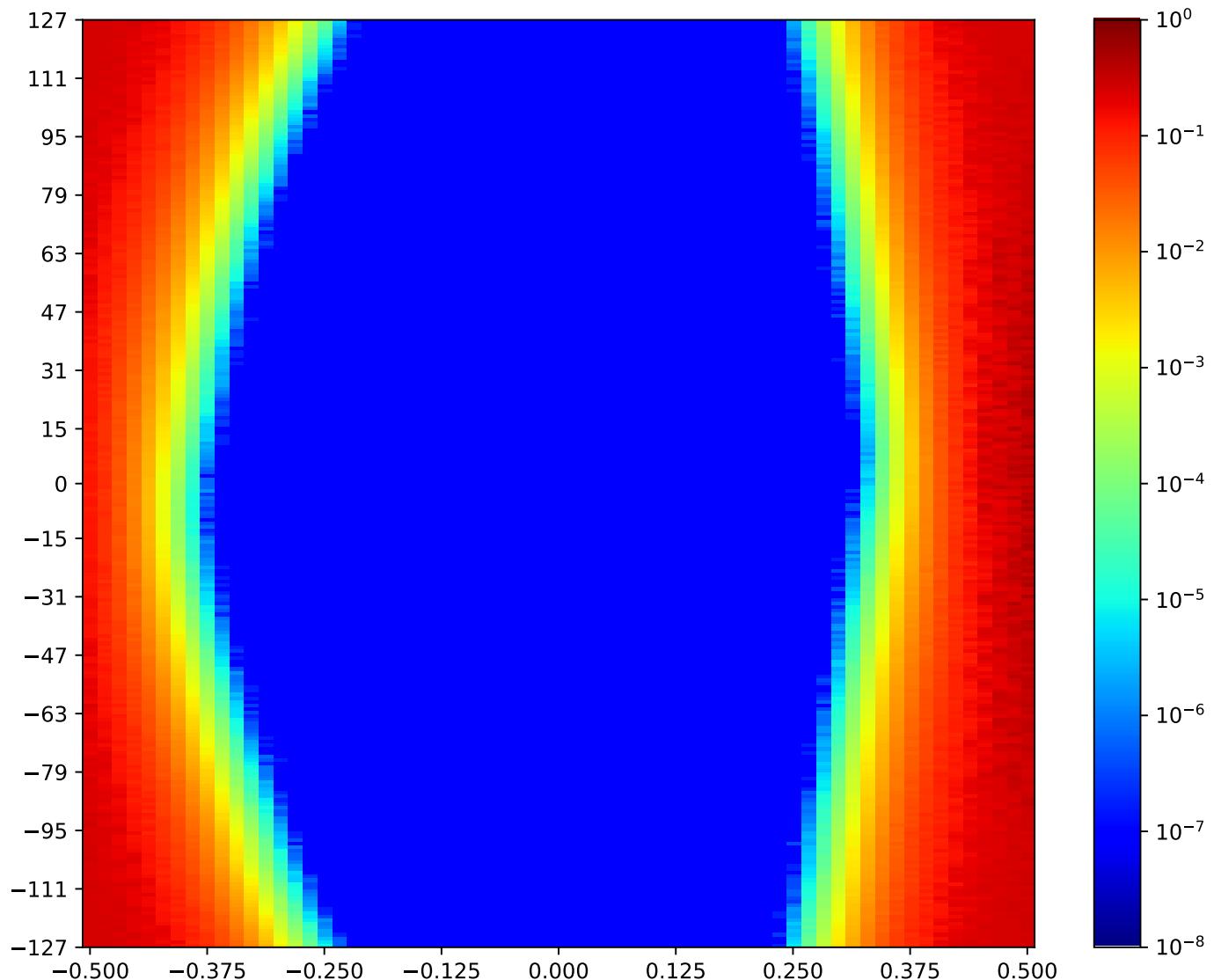


Figure 1.230: MSP\_C\_FPGA-TX4-02-RX1-02-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.18.4 MSP\_C\_FPGA-TX4-03-RX1-03-MSP\_A\_FPGA

Table 1.213: MSP\_C\_FPGA-TX4-03-RX1-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:10:01		2018-Jan-24 17:10:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9848	45	69.23%	255	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

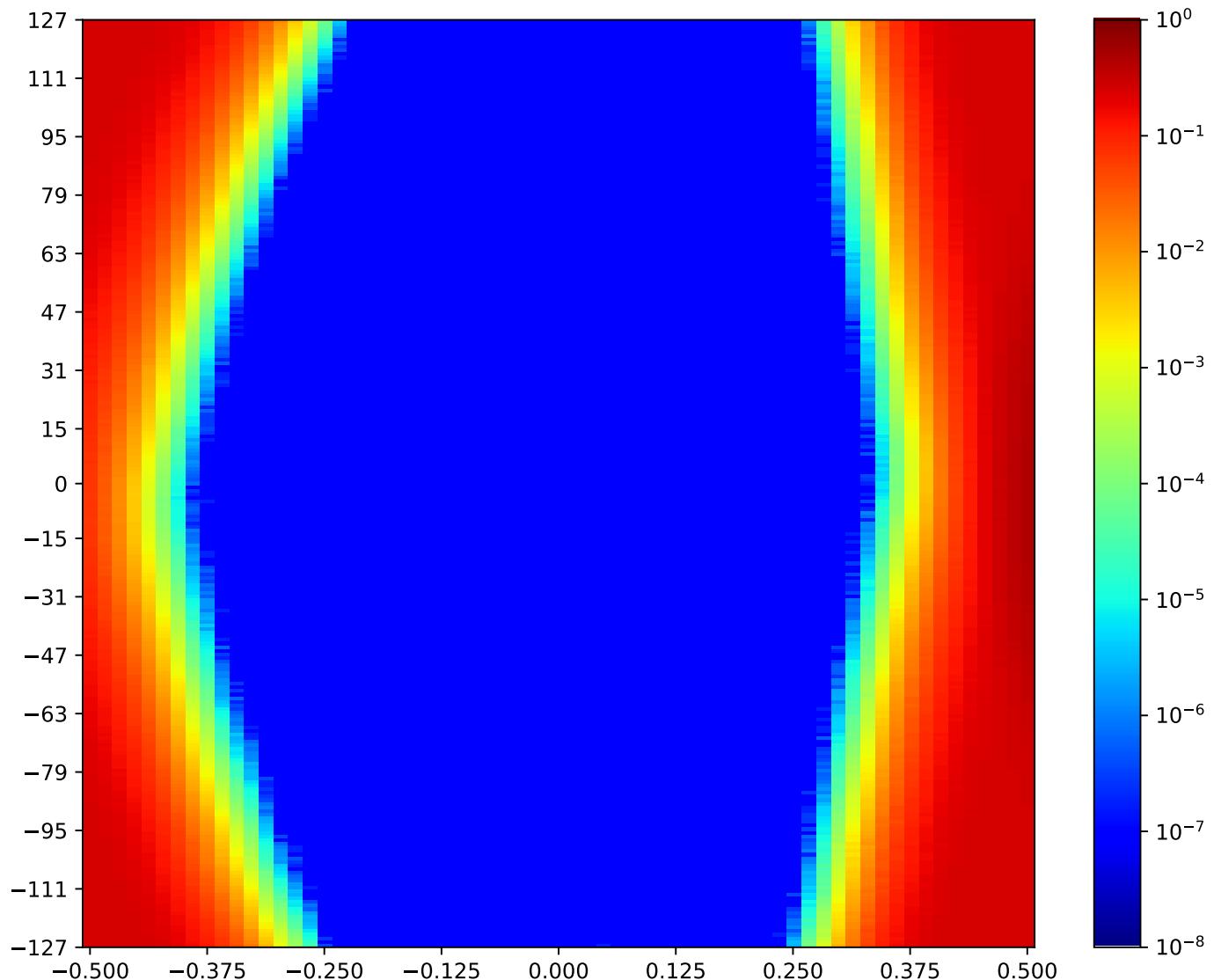


Figure 1.231: MSP\_C\_FPGA-TX4-03-RX1-03-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.5 MSP\_C\_FPGA-TX4-04-RX1-04-MSP\_A\_FPGA

Table 1.214: MSP\_C\_FPGA-TX4-04-RX1-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:15:29		2018-Jan-24 17:16:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10751	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

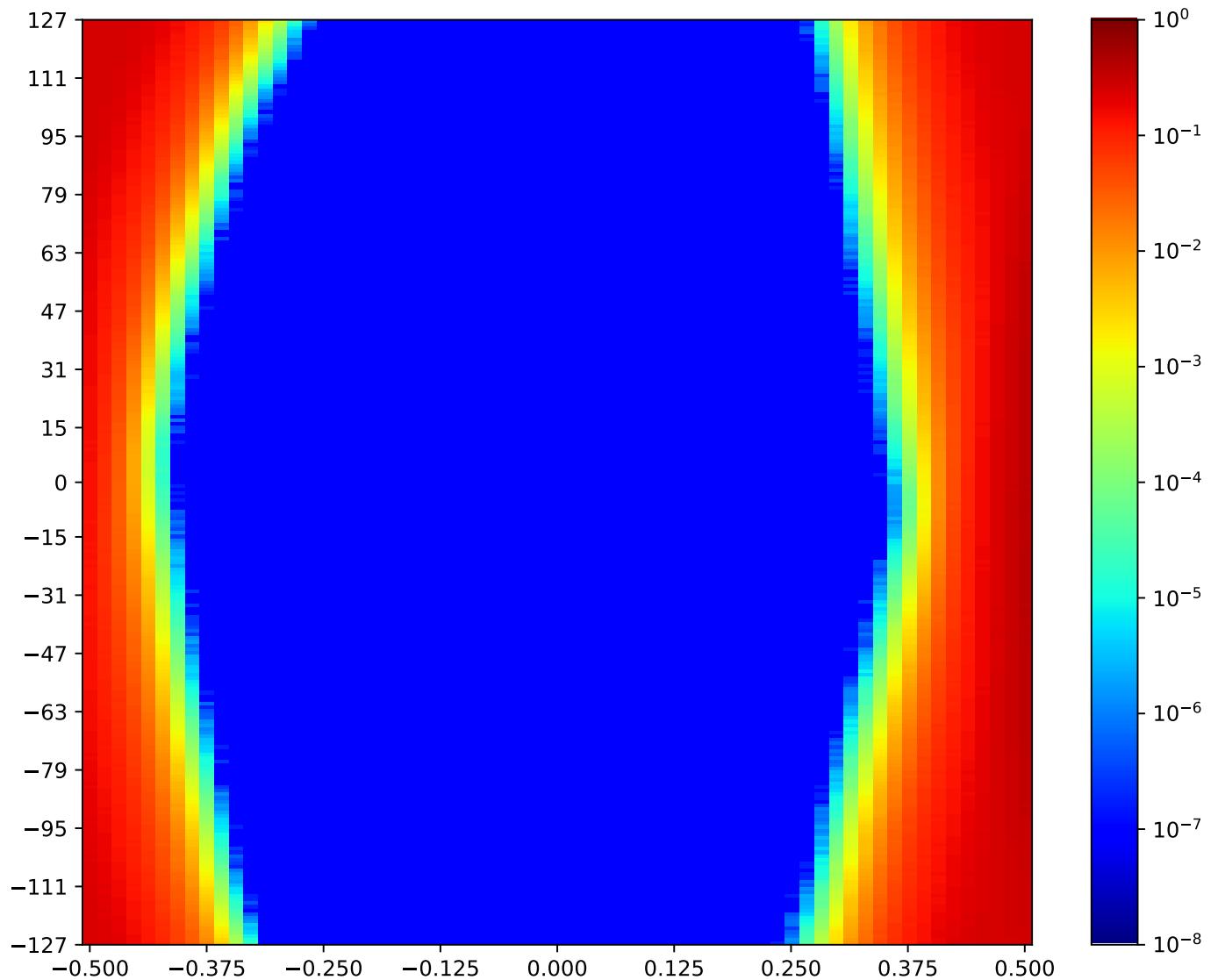


Figure 1.232: MSP\_C\_FPGA-TX4-04-RX1-04-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.6 MSP\_C\_FPGA-TX4-05-RX1-05-MSP\_A\_FPGA

Table 1.215: MSP\_C\_FPGA-TX4-05-RX1-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:11:15		2018-Jan-24 17:11:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10213	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

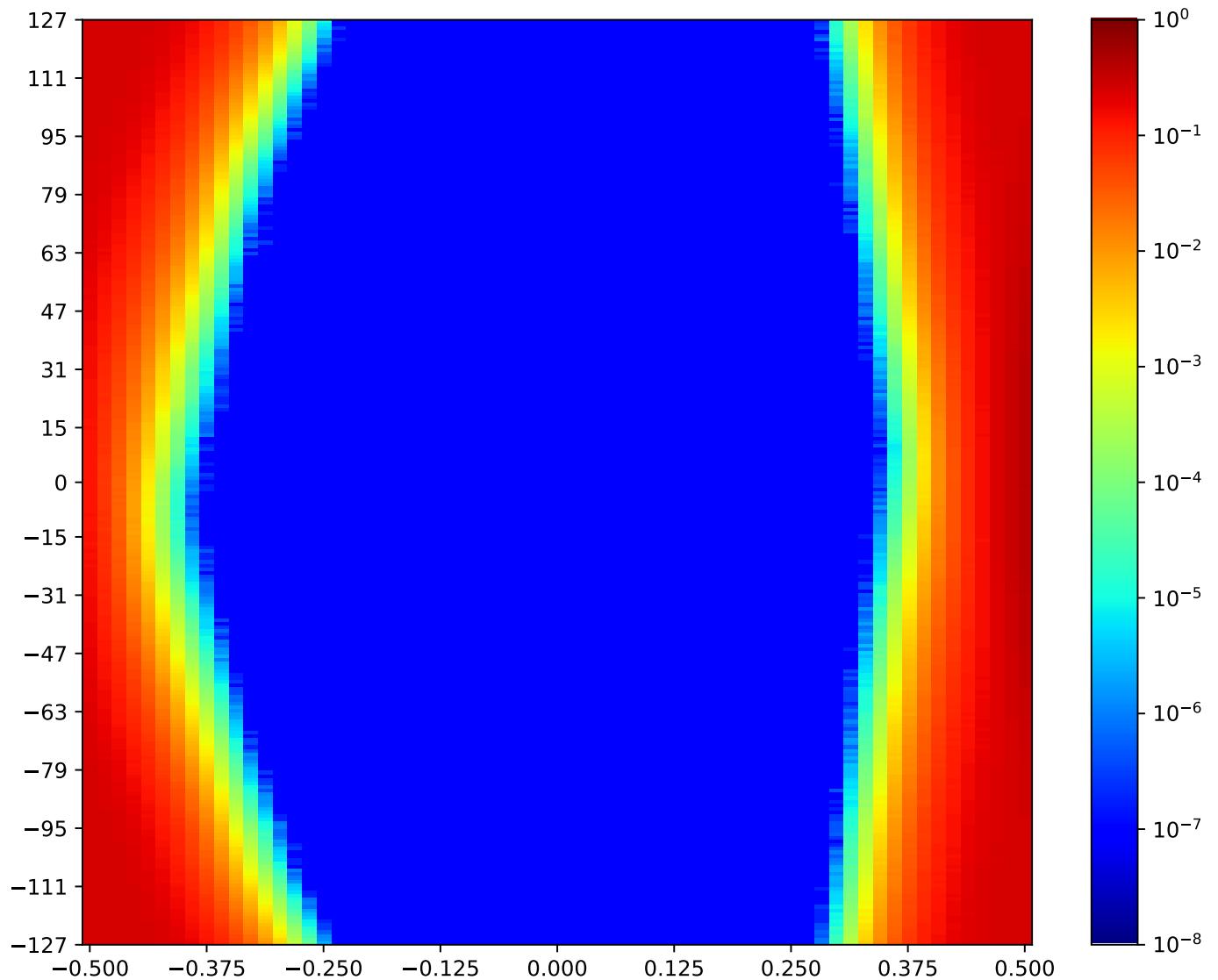


Figure 1.233: MSP\_C\_FPGA-TX4-05-RX1-05-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.7 MSP\_C\_FPGA-TX4-06-RX1-06-MSP\_A\_FPGA

Table 1.216: MSP\_C\_FPGA-TX4-06-RX1-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:16:43		2018-Jan-24 17:17:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10381	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

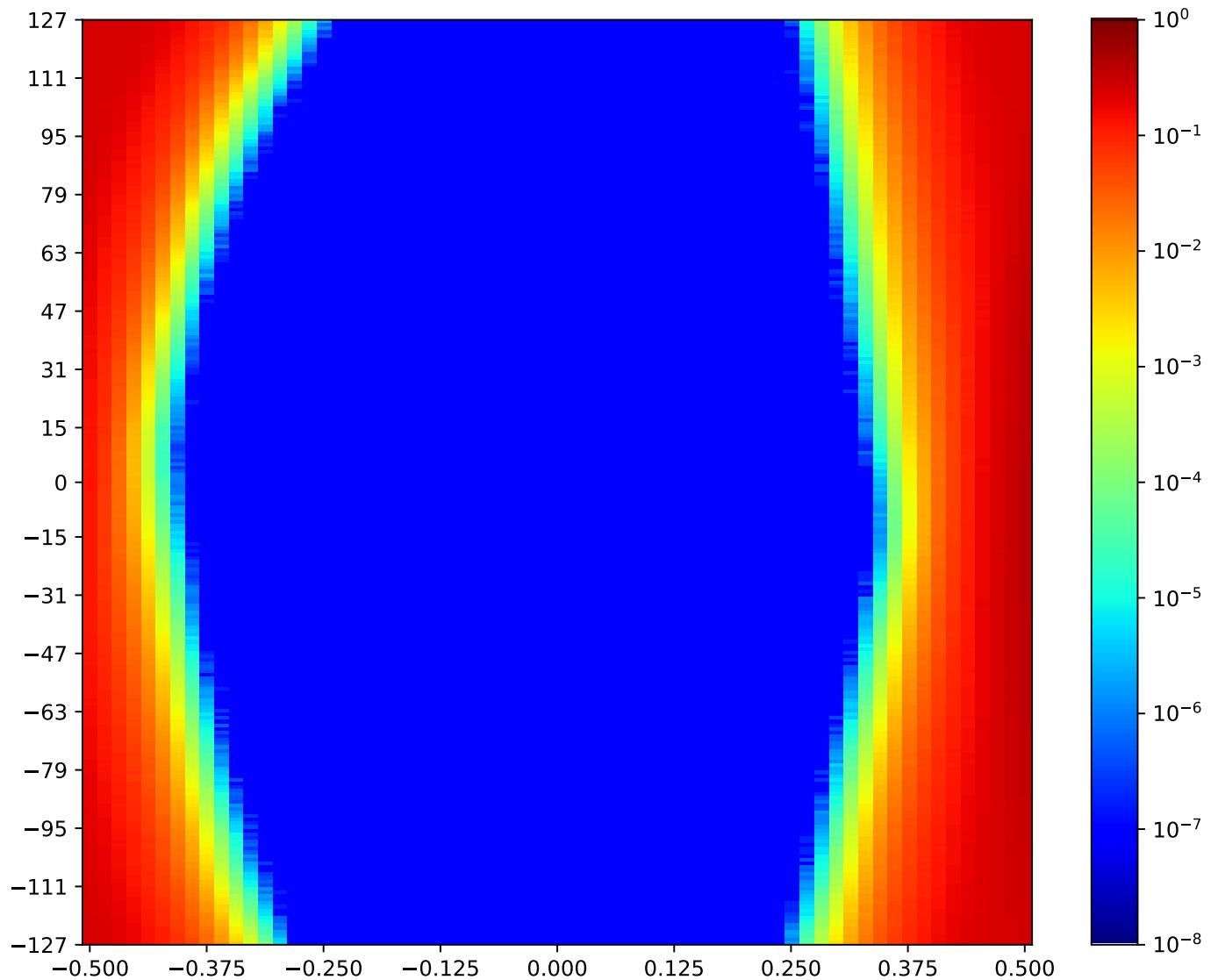


Figure 1.234: MSP\_C\_FPGA-TX4-06-RX1-06-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.8 MSP\_C\_FPGA-TX4-07-RX1-07-MSP\_A\_FPGA

Table 1.217: MSP\_C\_FPGA-TX4-07-RX1-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:12:27		2018-Jan-24 17:13:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9532	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

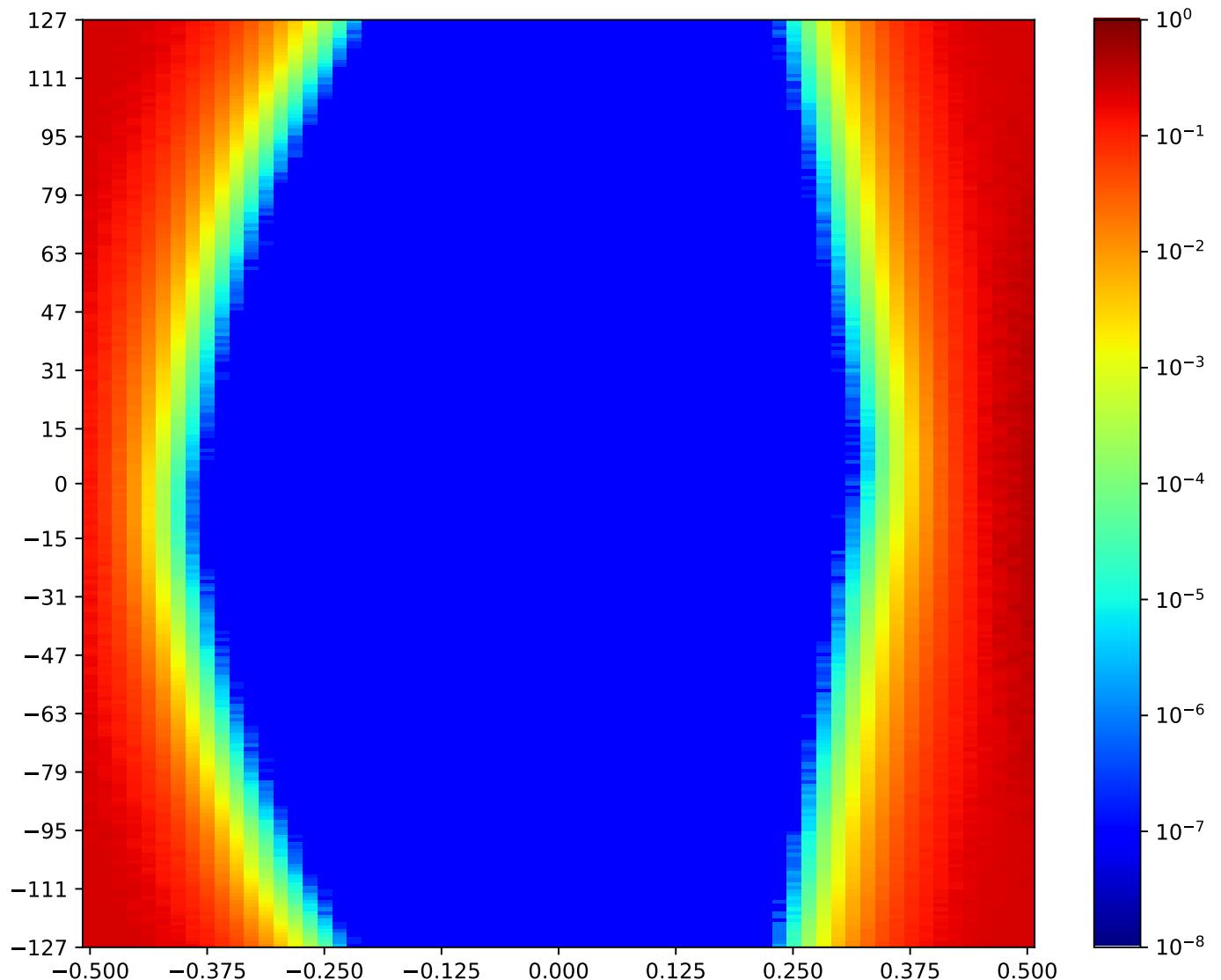


Figure 1.235: MSP\_C\_FPGA-TX4-07-RX1-07-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.9 MSP\_C\_FPGA-TX4-08-RX1-08-MSP\_A\_FPGA

Table 1.218: MSP\_C\_FPGA-TX4-08-RX1-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:16:06		2018-Jan-24 17:16:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9922	46	70.77%	255	100.00%
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BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

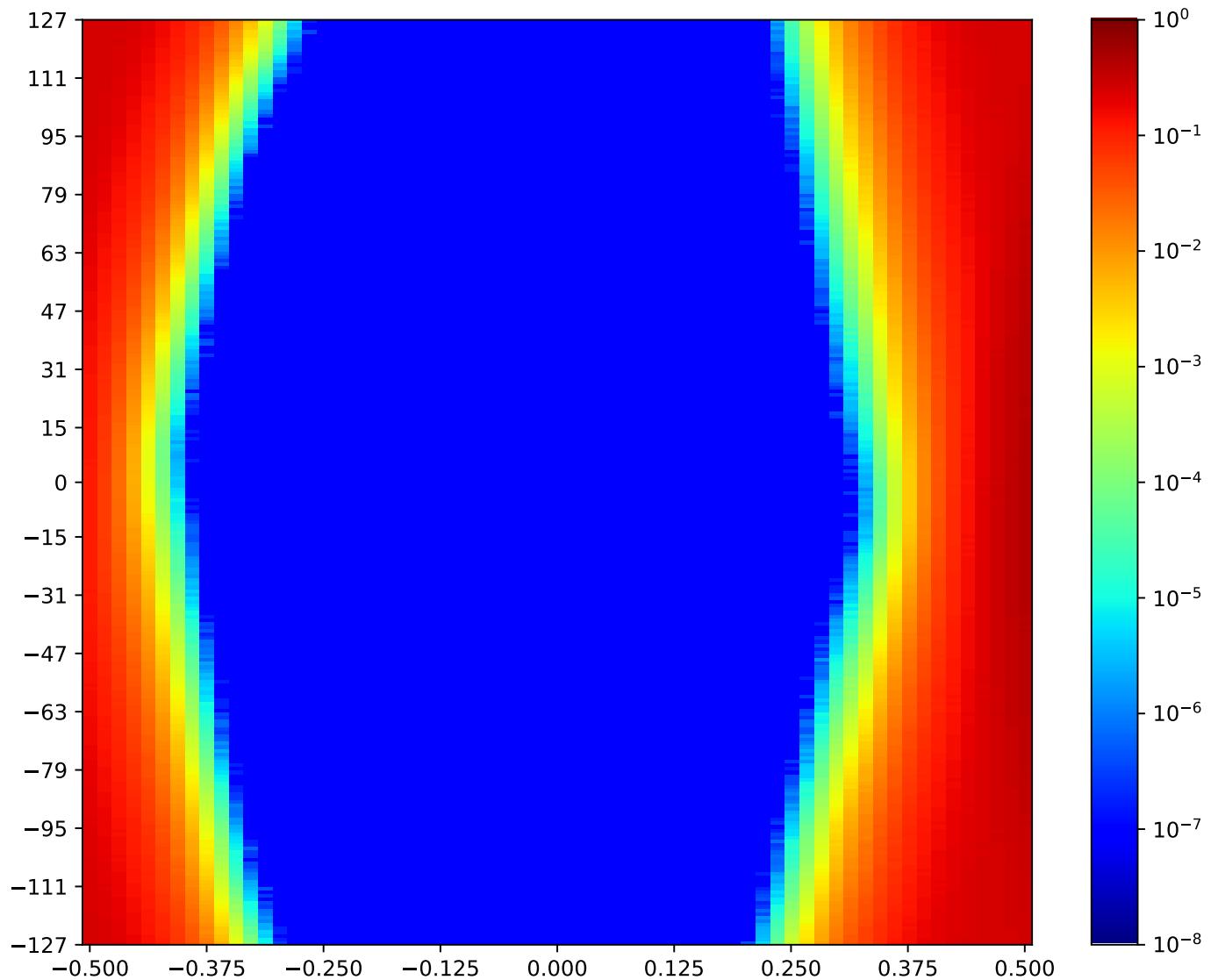


Figure 1.236: MSP\_C\_FPGA-TX4-08-RX1-08-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.10 MSP\_C\_FPGA-TX4-09-RX1-09-MSP\_A\_FPGA

Table 1.219: MSP\_C\_FPGA-TX4-09-RX1-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:13:03		2018-Jan-24 17:13:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9374	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

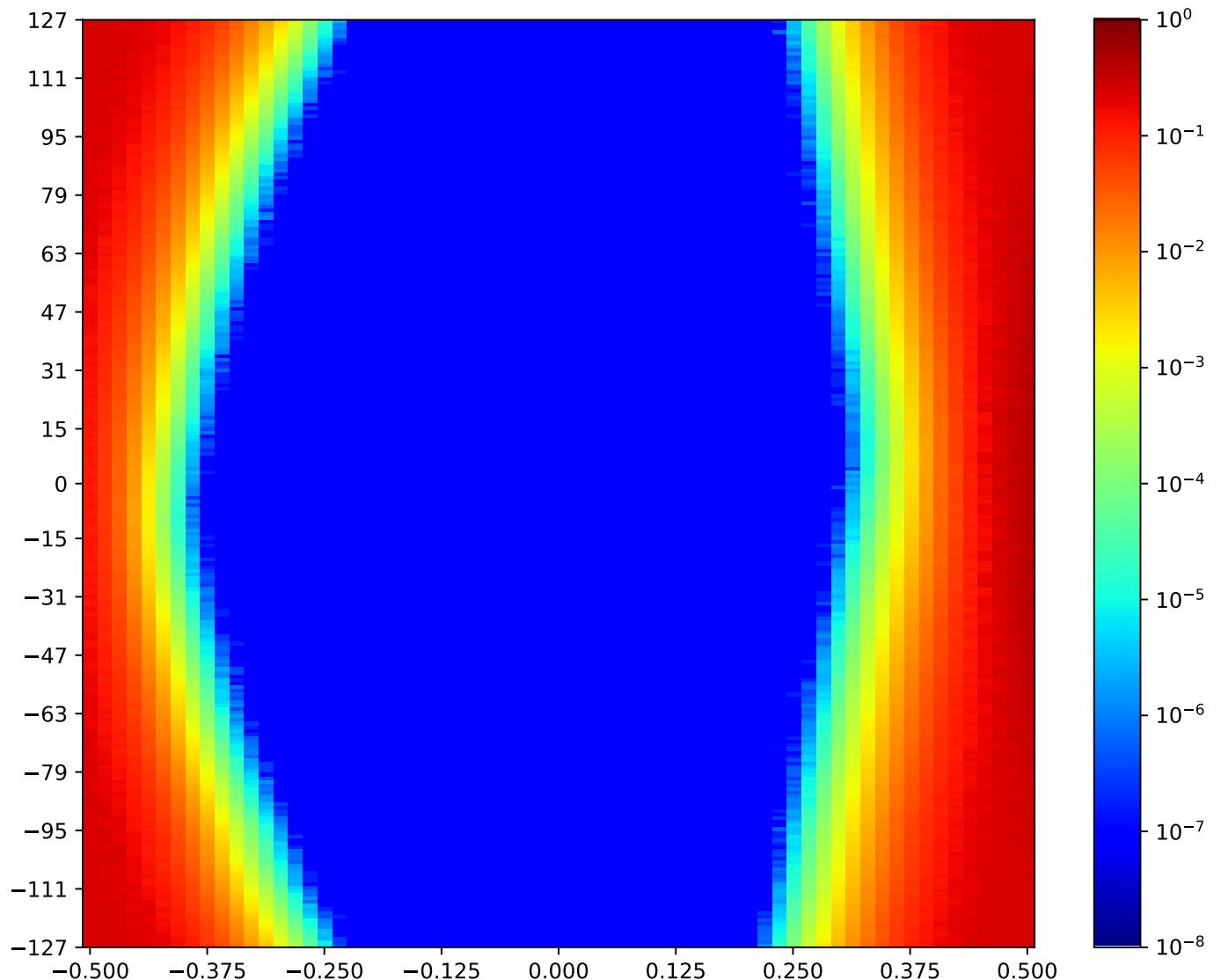


Figure 1.237: MSP\_C\_FPGA-TX4-09-RX1-09-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.11 MSP\_C\_FPGA-TX4-10-RX1-10-MSP\_A\_FPGA

Table 1.220: MSP\_C\_FPGA-TX4-10-RX1-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:14:53		2018-Jan-24 17:15:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9938	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
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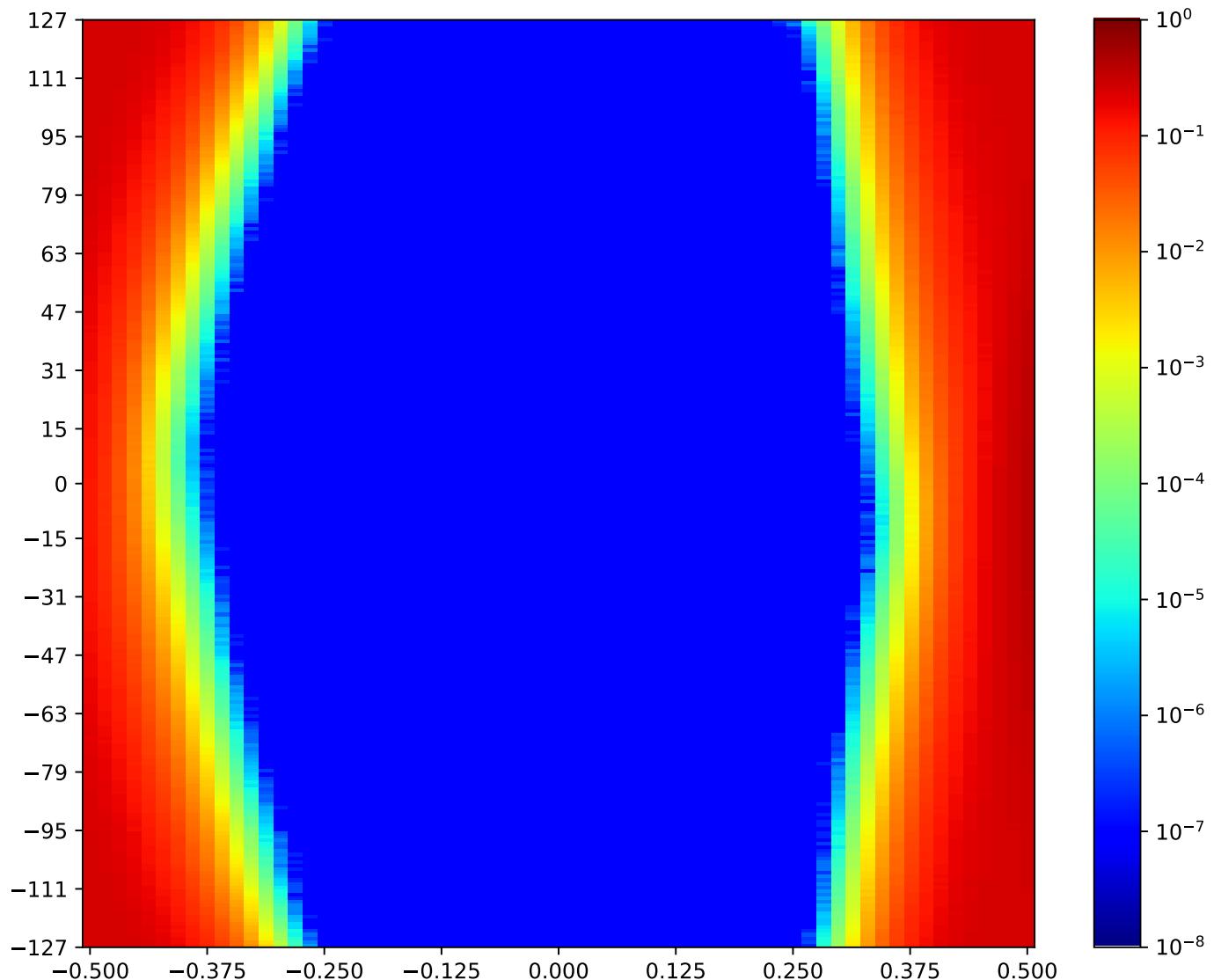


Figure 1.238: MSP\_C\_FPGA-TX4-10-RX1-10-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.18.12 MSP\_C\_FPGA-TX4-11-RX1-11-MSP\_A\_FPGA

Table 1.221: MSP\_C\_FPGA-TX4-11-RX1-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:14:16		2018-Jan-24 17:14:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9223	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
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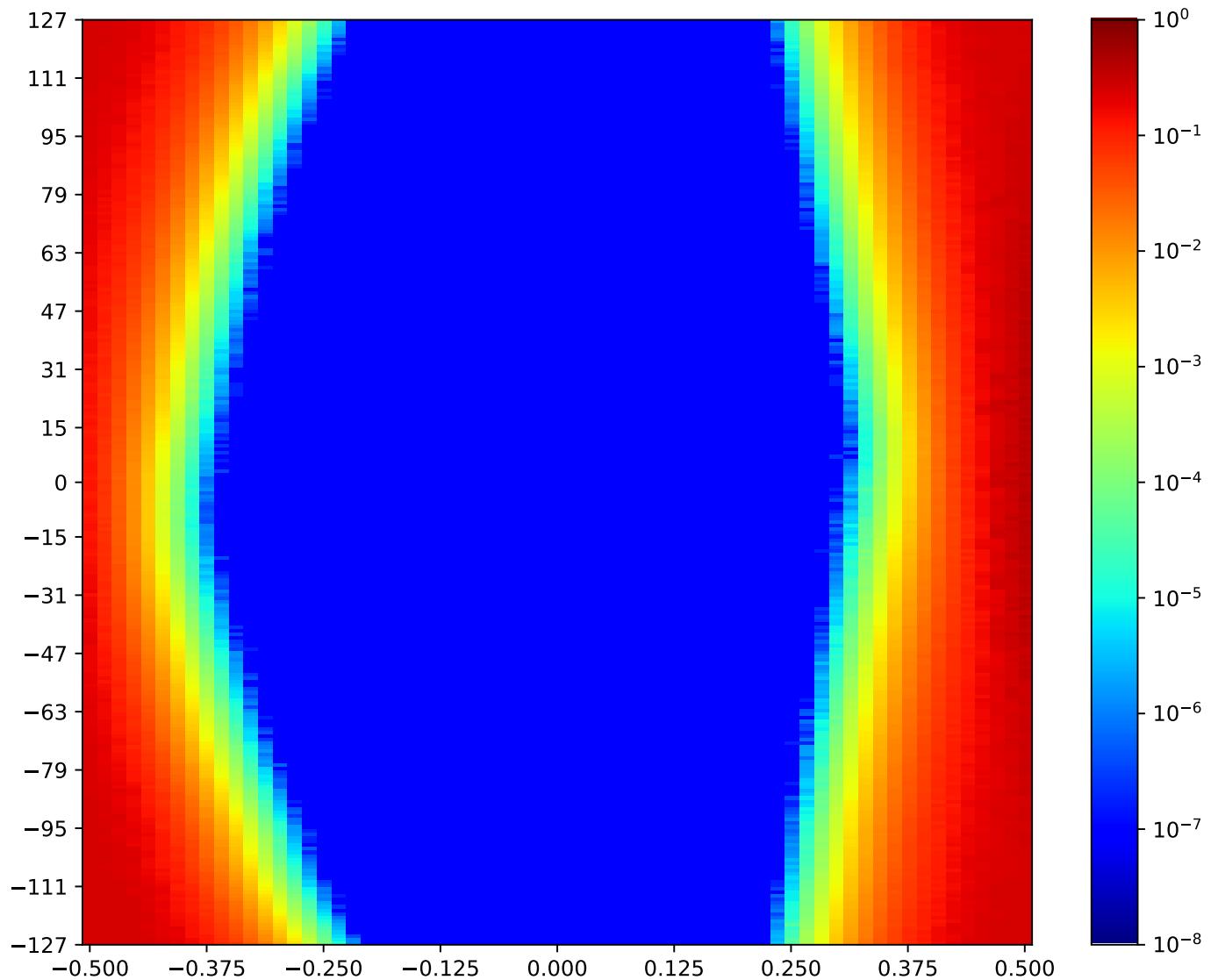


Figure 1.239: MSP\_C\_FPGA-TX4-11-RX1-11-MSP\_A\_FPGA

Call back to summary Figure 1.227. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.19 MSP\_A TX1 MSP\_C RX13 Minipod Loopback

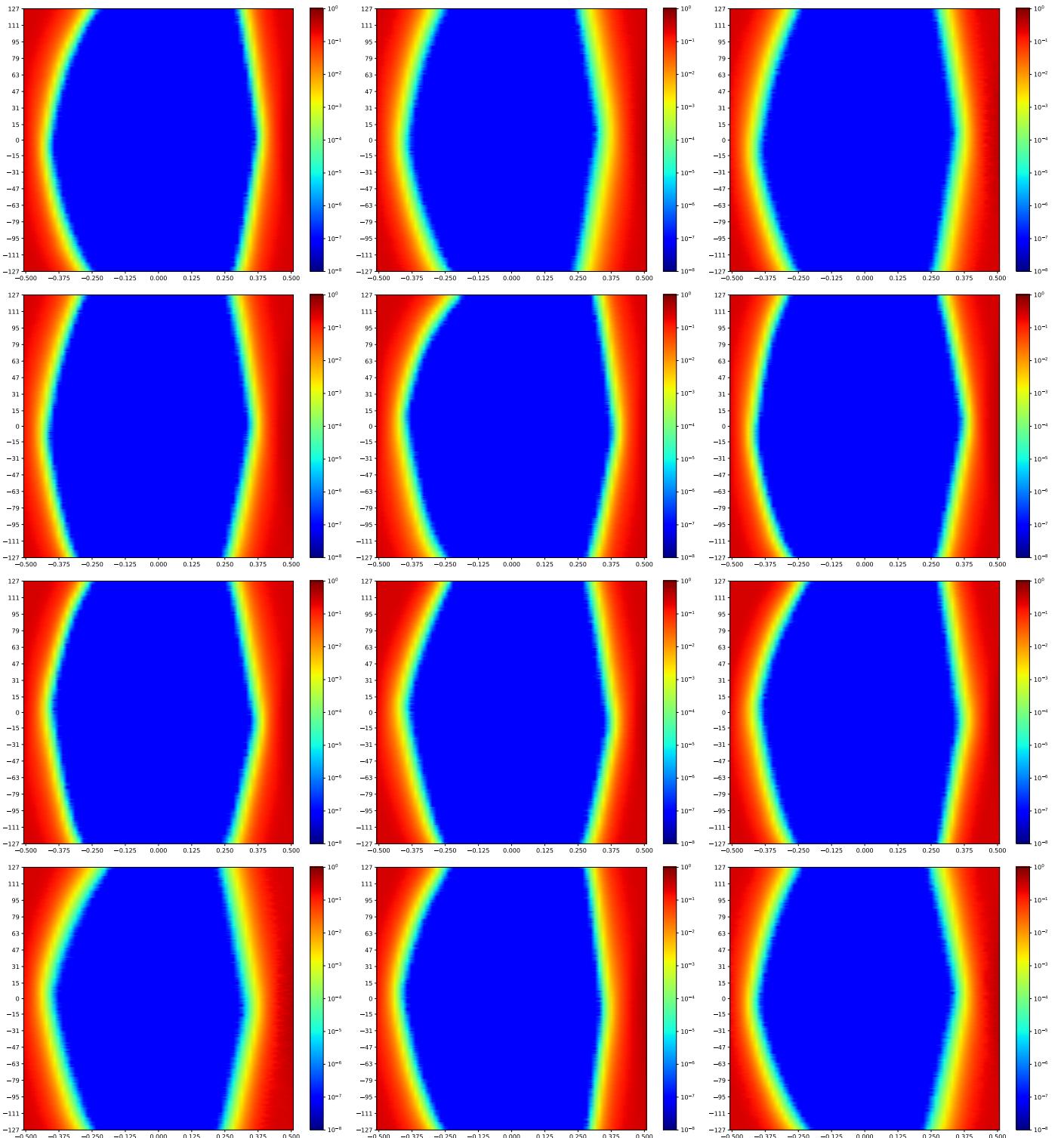


Figure 1.240: MSP\_A TX1 MSP\_C RX13 Minipod Loopback

A cross-reference to Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.253.

### 1.19.1 MSP\_A\_FPGA-TX1-00-RX13-00-MSP\_C\_FPGA

Table 1.222: MSP\_A\_FPGA-TX1-00-RX13-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:33:20		2018-Jan-24 17:33:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10586	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

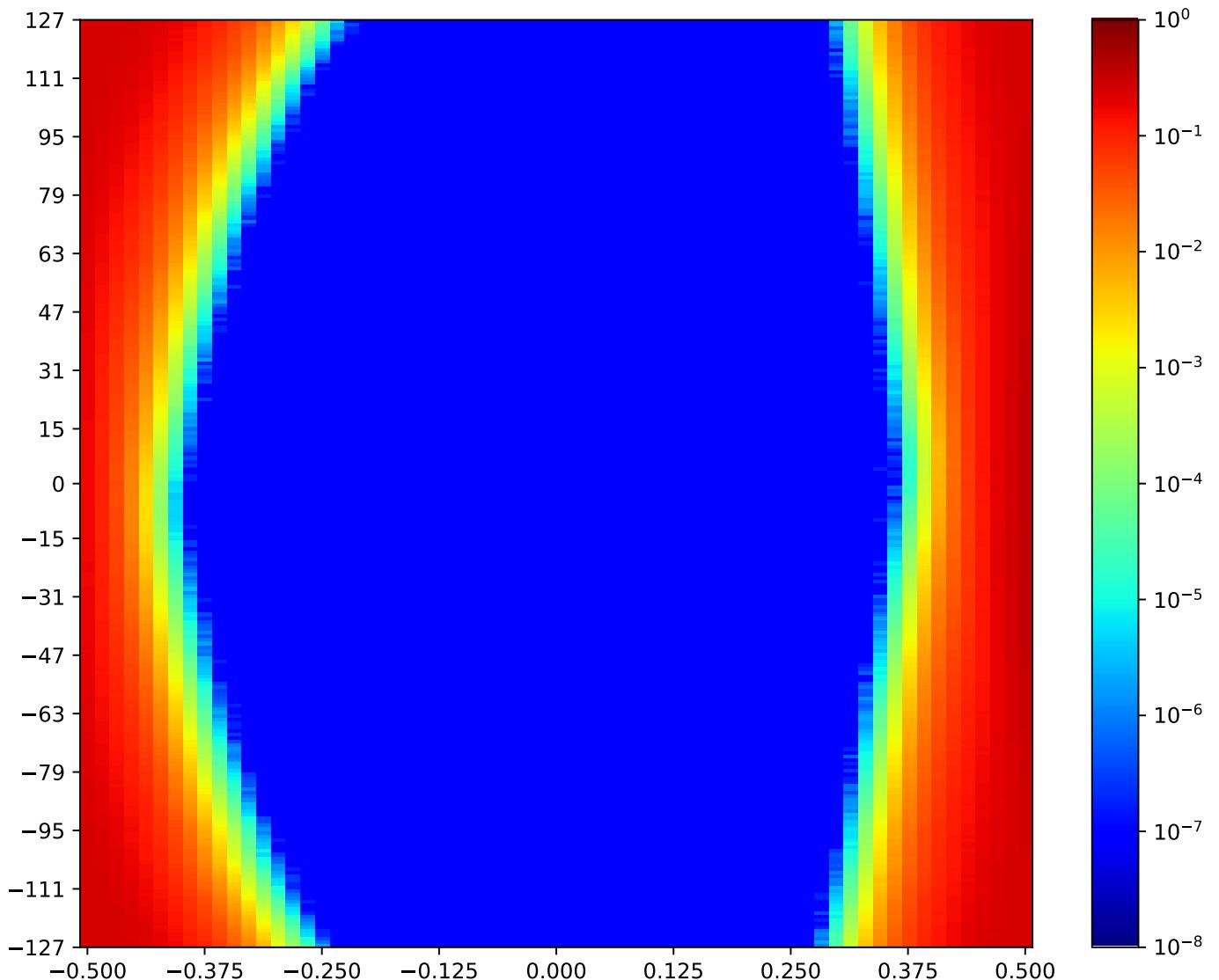


Figure 1.241: MSP\_A\_FPGA-TX1-00-RX13-00-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.2 MSP\_A\_FPGA-TX1-01-RX13-01-MSP\_C\_FPGA

Table 1.223: MSP\_A\_FPGA-TX1-01-RX13-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:34:31		2018-Jan-24 17:35:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9453	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

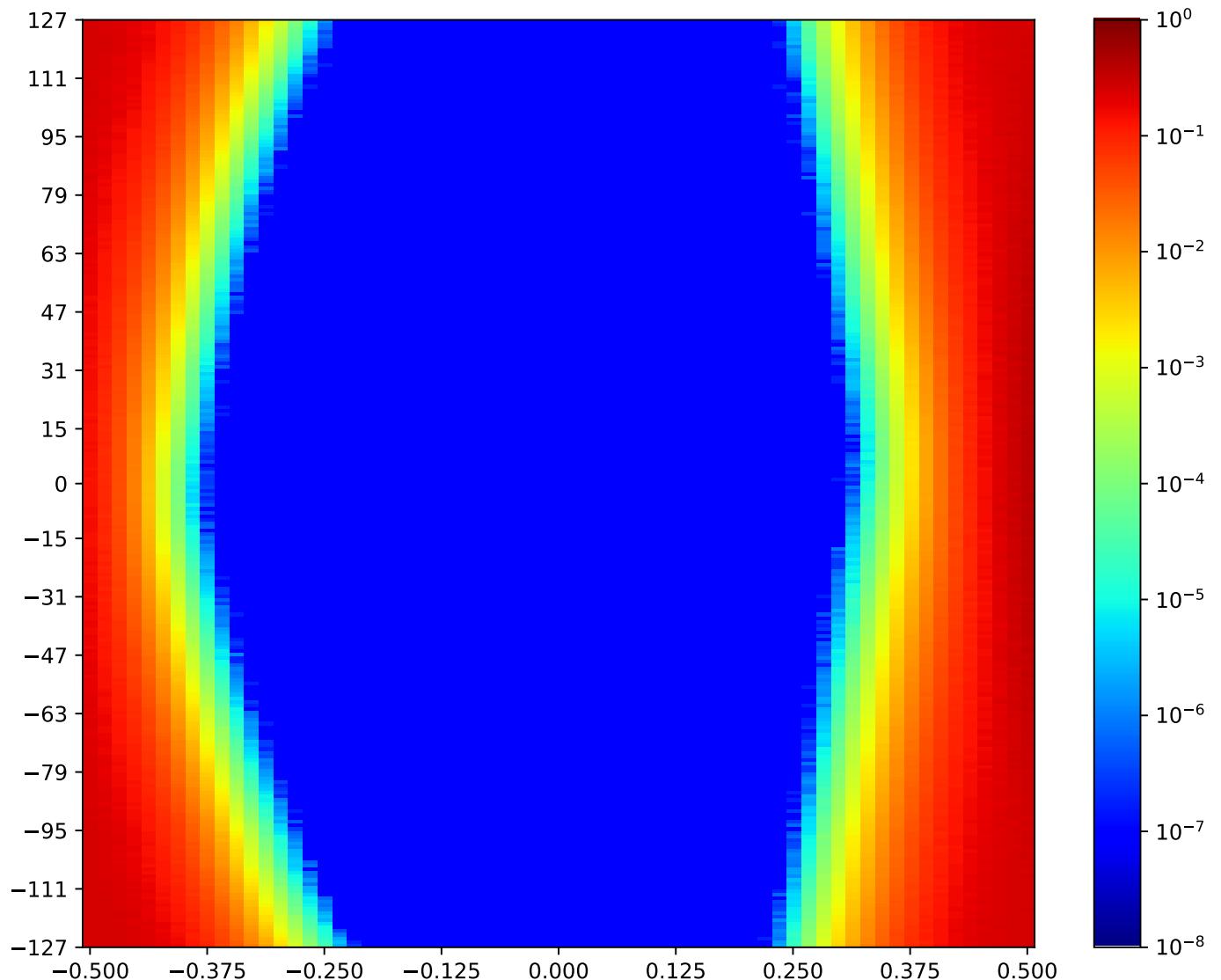


Figure 1.242: MSP\_A\_FPGA-TX1-01-RX13-01-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.3 MSP\_A\_FPGA-TX1-02-RX13-02-MSP\_C\_FPGA

Table 1.224: MSP\_A\_FPGA-TX1-02-RX13-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:35:06		2018-Jan-24 17:35:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9799	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

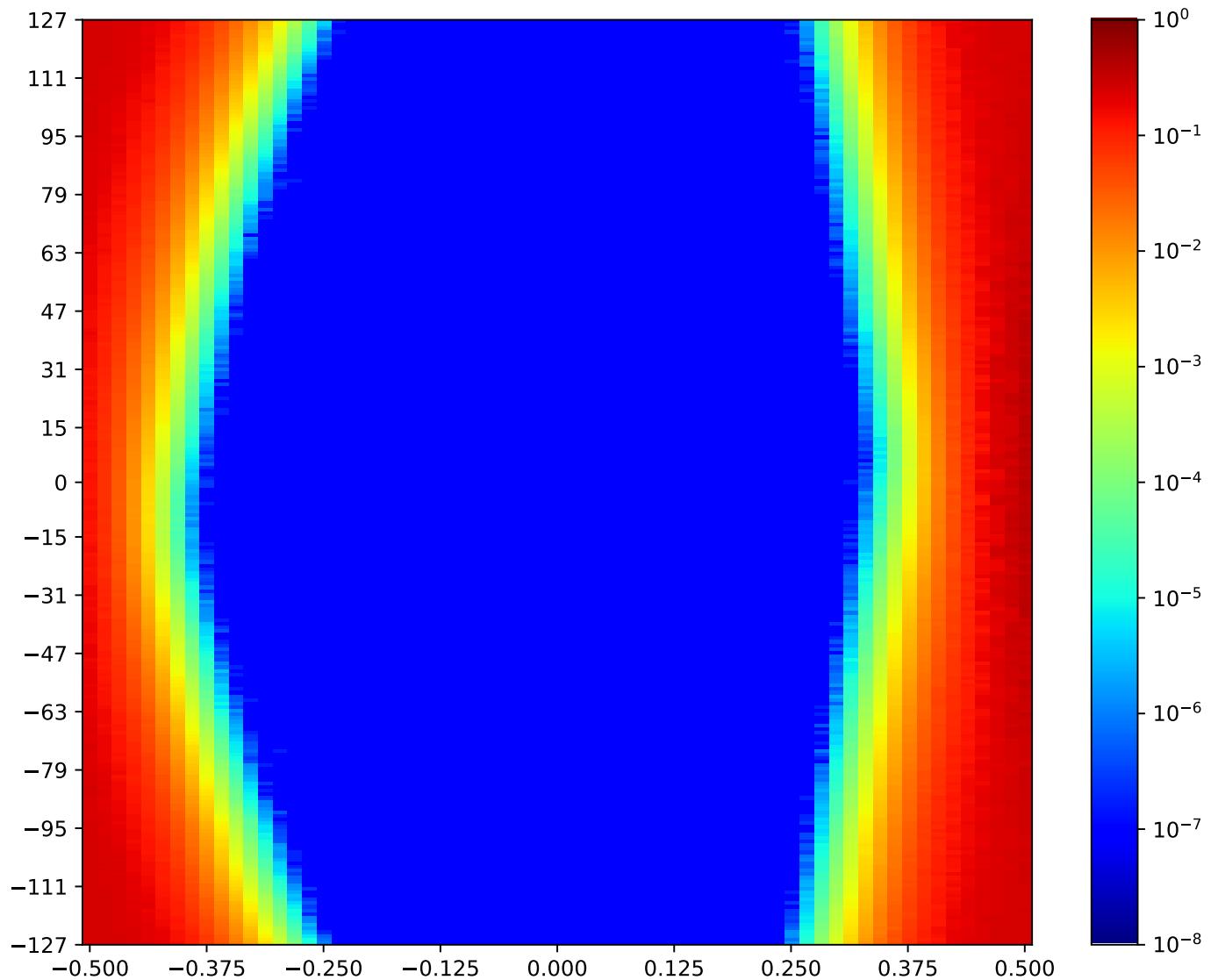


Figure 1.243: MSP\_A\_FPGA-TX1-02-RX13-02-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.19.4 MSP\_A\_FPGA-TX1-03-RX13-03-MSP\_C\_FPGA

Table 1.225: MSP\_A\_FPGA-TX1-03-RX13-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:32:10		2018-Jan-24 17:32:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10448	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

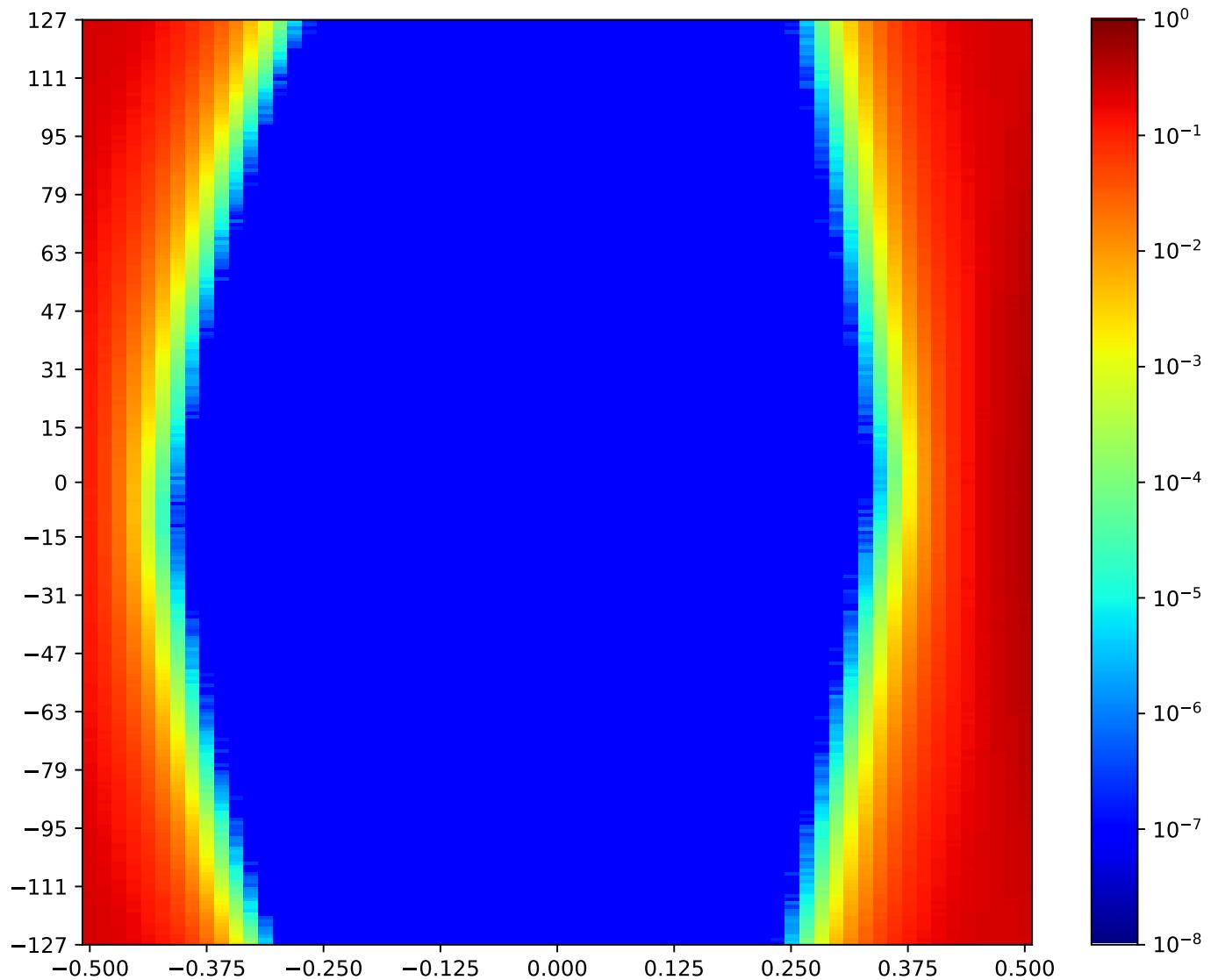


Figure 1.244: MSP\_A\_FPGA-TX1-03-RX13-03-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.5 MSP\_A\_FPGA-TX1-04-RX13-04-MSP\_C\_FPGA

Table 1.226: MSP\_A\_FPGA-TX1-04-RX13-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:36:51		2018-Jan-24 17:37:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10450	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

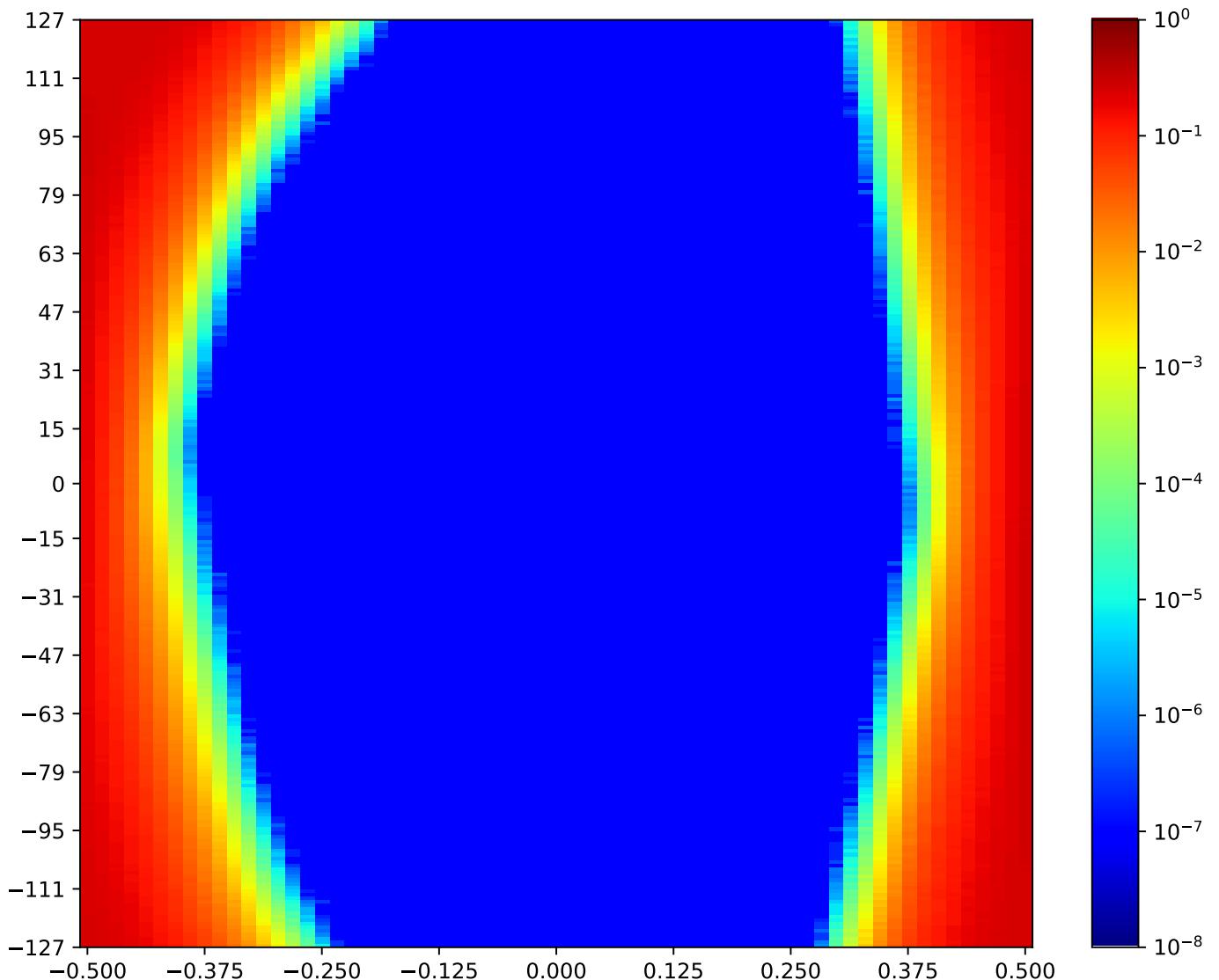


Figure 1.245: MSP\_A\_FPGA-TX1-04-RX13-04-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.6 MSP\_A\_FPGA-TX1-05-RX13-05-MSP\_C\_FPGA

Table 1.227: MSP\_A\_FPGA-TX1-05-RX13-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:31:34		2018-Jan-24 17:32:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10642	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

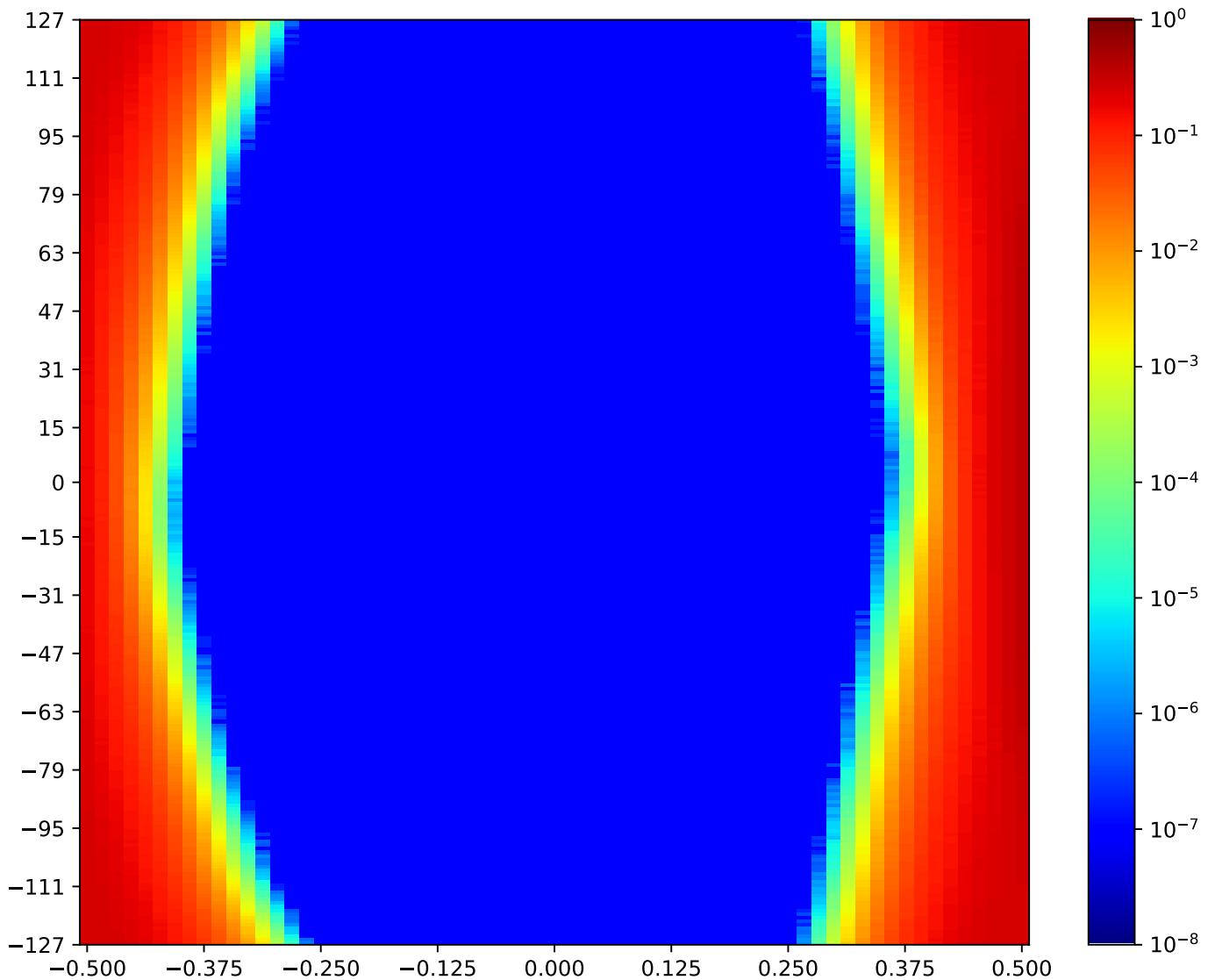


Figure 1.246: MSP\_A\_FPGA-TX1-05-RX13-05-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.7 MSP\_A\_FPGA-TX1-06-RX13-06-MSP\_C\_FPGA

Table 1.228: MSP\_A\_FPGA-TX1-06-RX13-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:38:02		2018-Jan-24 17:38:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10339	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

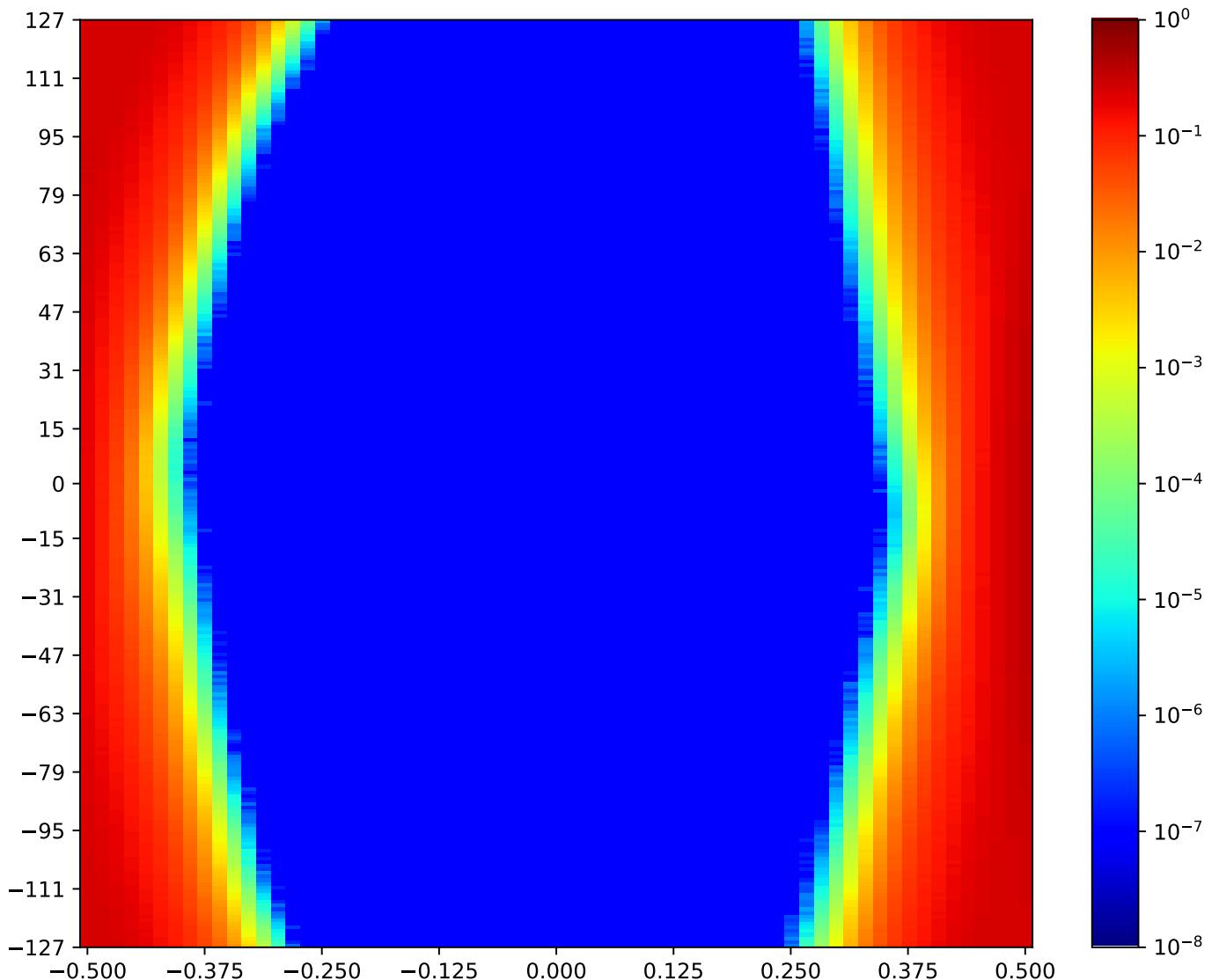


Figure 1.247: MSP\_A\_FPGA-TX1-06-RX13-06-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.8 MSP\_A\_FPGA-TX1-07-RX13-07-MSP\_C\_FPGA

Table 1.229: MSP\_A\_FPGA-TX1-07-RX13-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:32:45		2018-Jan-24 17:33:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10064	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

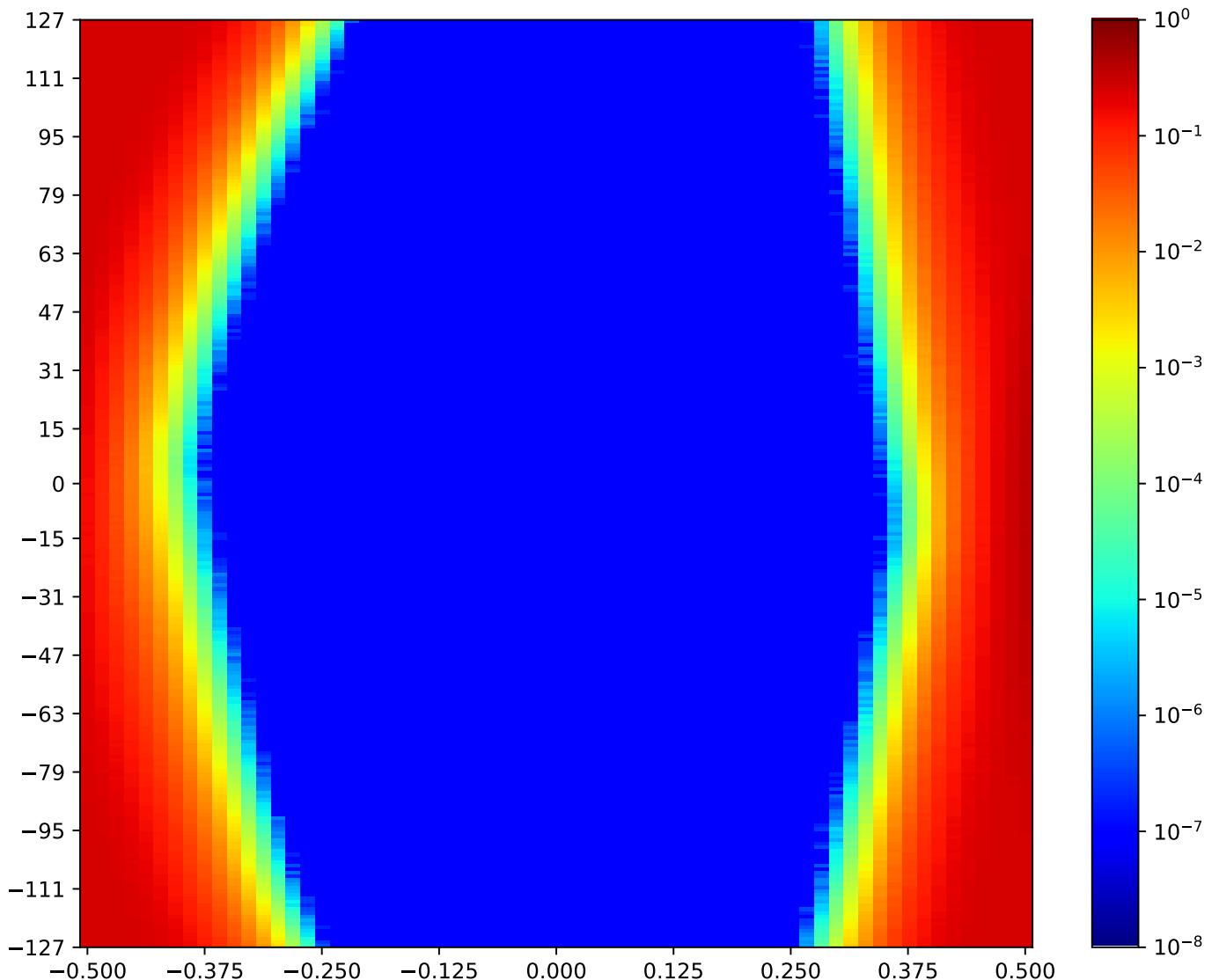


Figure 1.248: MSP\_A\_FPGA-TX1-07-RX13-07-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.9 MSP\_A\_FPGA-TX1-08-RX13-08-MSP\_C\_FPGA

Table 1.230: MSP\_A\_FPGA-TX1-08-RX13-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:37:27		2018-Jan-24 17:38:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10003	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

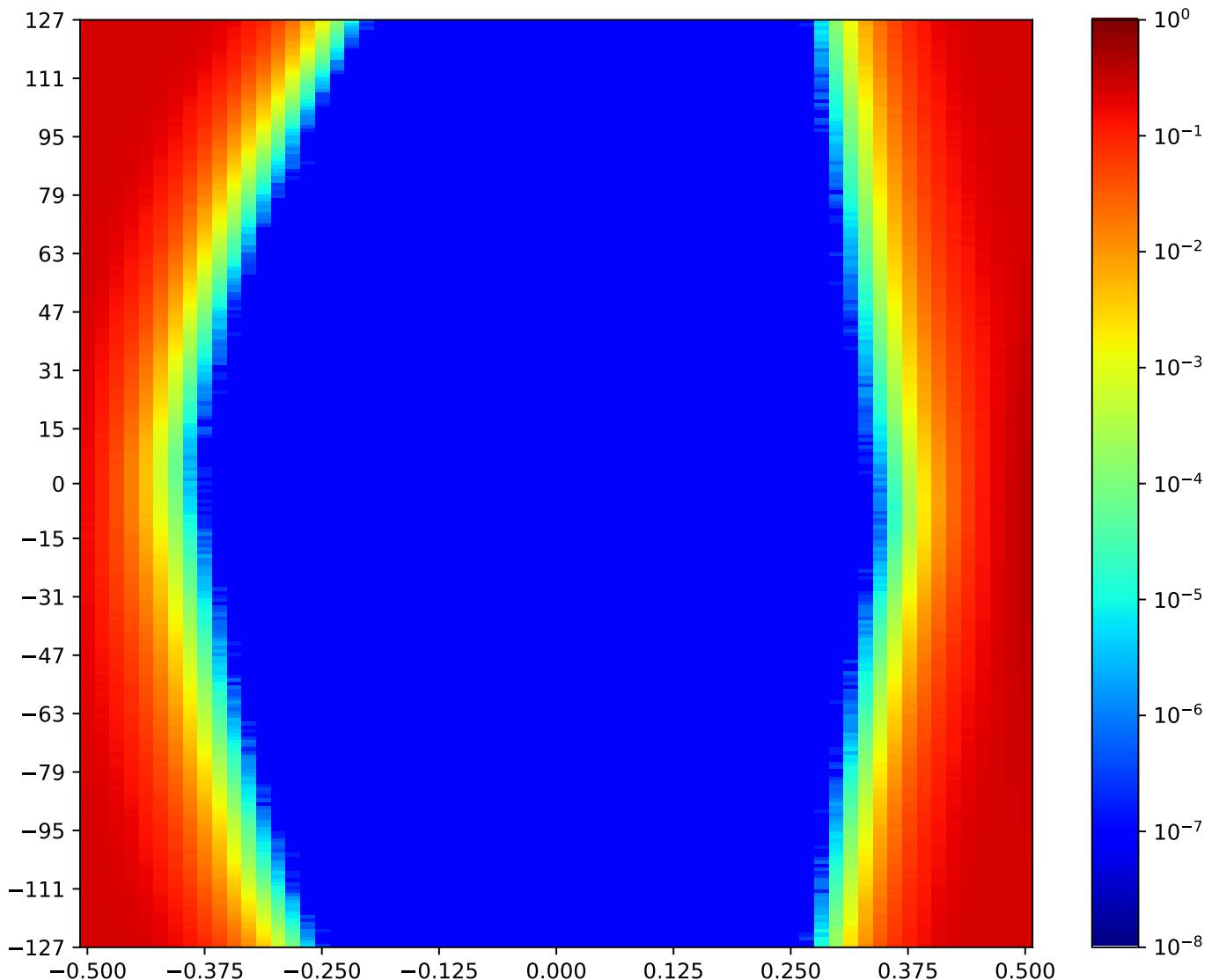


Figure 1.249: MSP\_A\_FPGA-TX1-08-RX13-08-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.10 MSP\_A\_FPGA-TX1-09-RX13-09-MSP\_C\_FPGA

Table 1.231: MSP\_A\_FPGA-TX1-09-RX13-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:33:57		2018-Jan-24 17:34:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9246	44	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

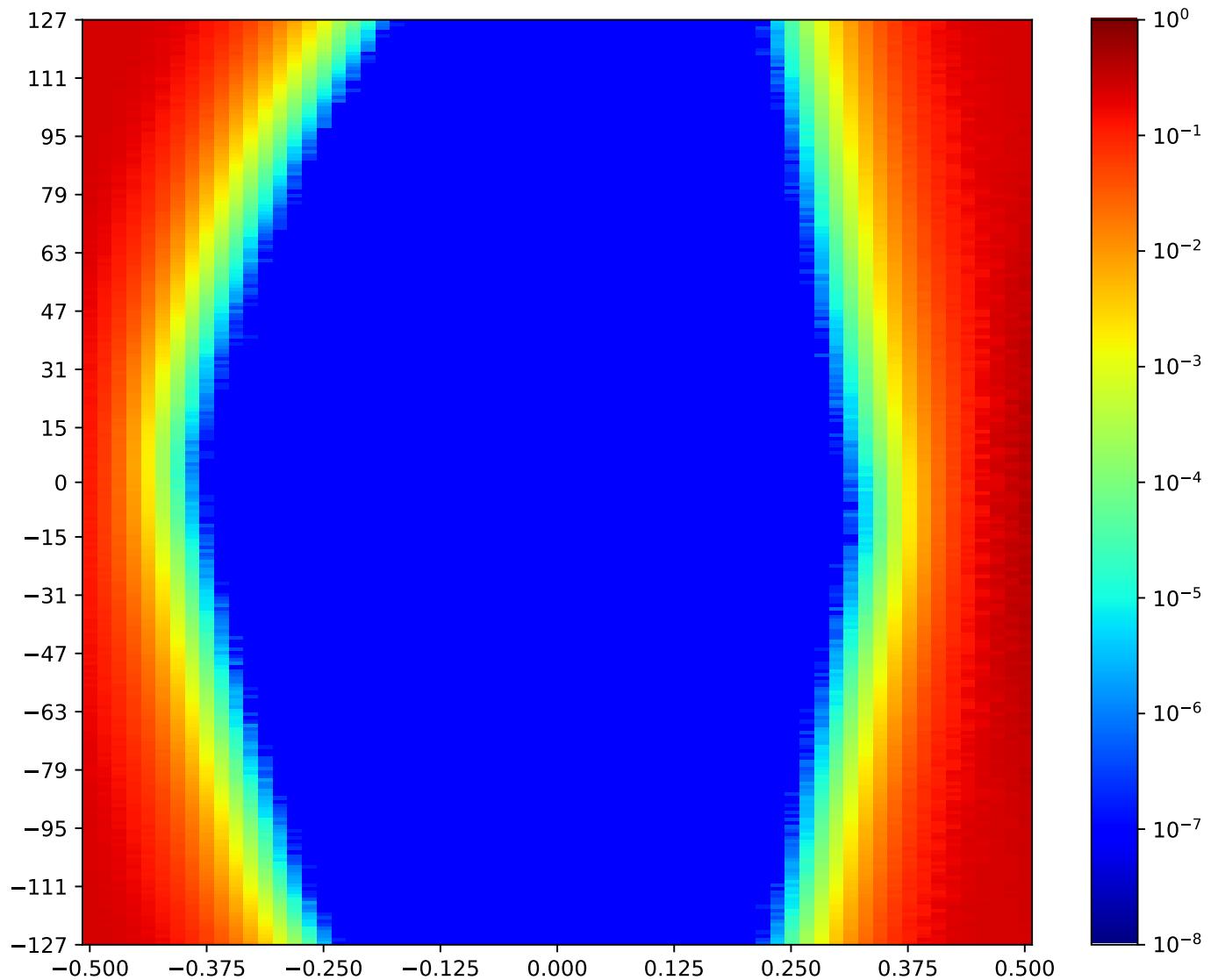


Figure 1.250: MSP\_A\_FPGA-TX1-09-RX13-09-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.11 MSP\_A\_FPGA-TX1-10-RX13-10-MSP\_C\_FPGA

Table 1.232: MSP\_A\_FPGA-TX1-10-RX13-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:36:16		2018-Jan-24 17:36:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10194	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

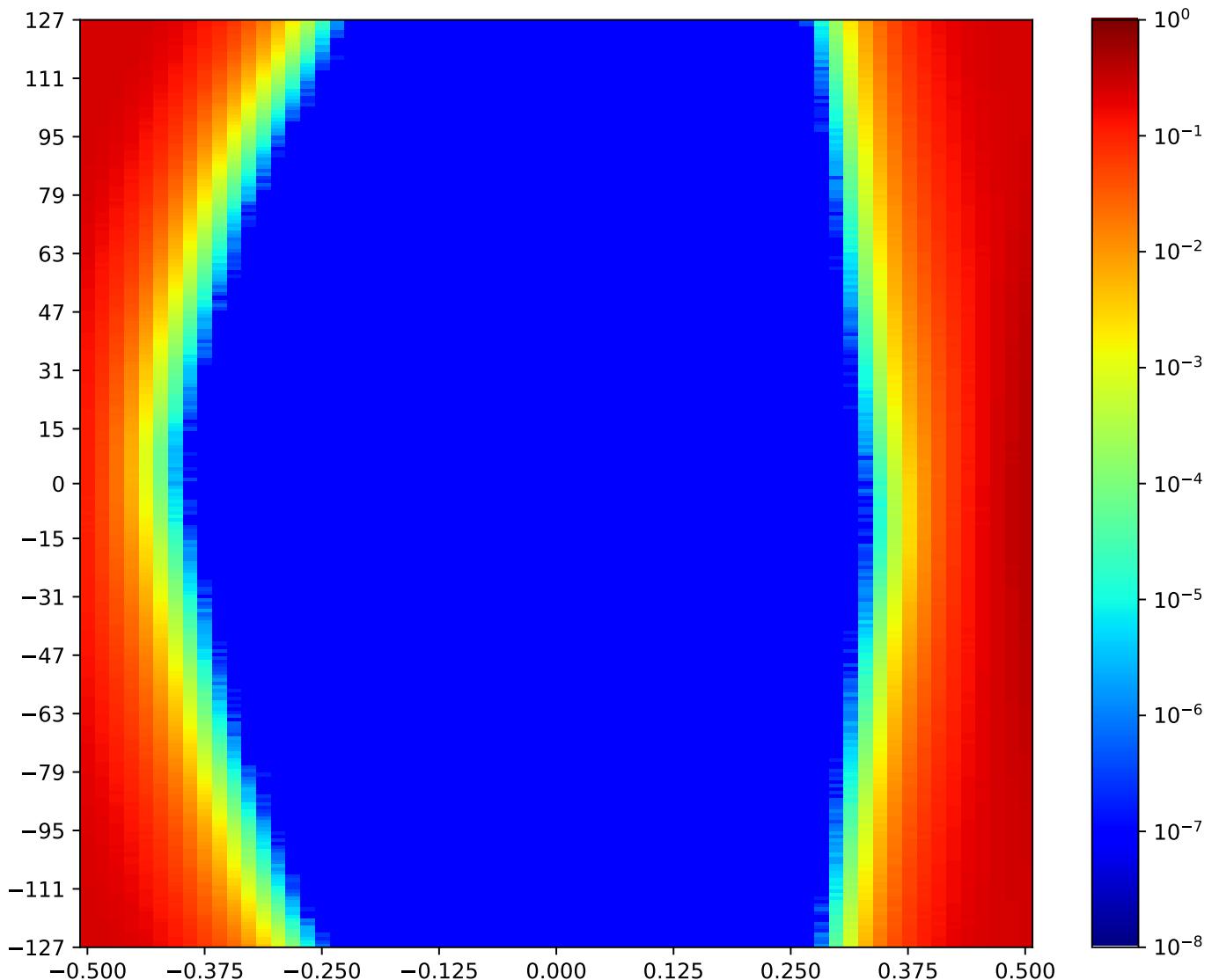


Figure 1.251: MSP\_A\_FPGA-TX1-10-RX13-10-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.19.12 MSP\_A\_FPGA-TX1-11-RX13-11-MSP\_C\_FPGA

Table 1.233: MSP\_A\_FPGA-TX1-11-RX13-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:35:41		2018-Jan-24 17:36:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9570	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

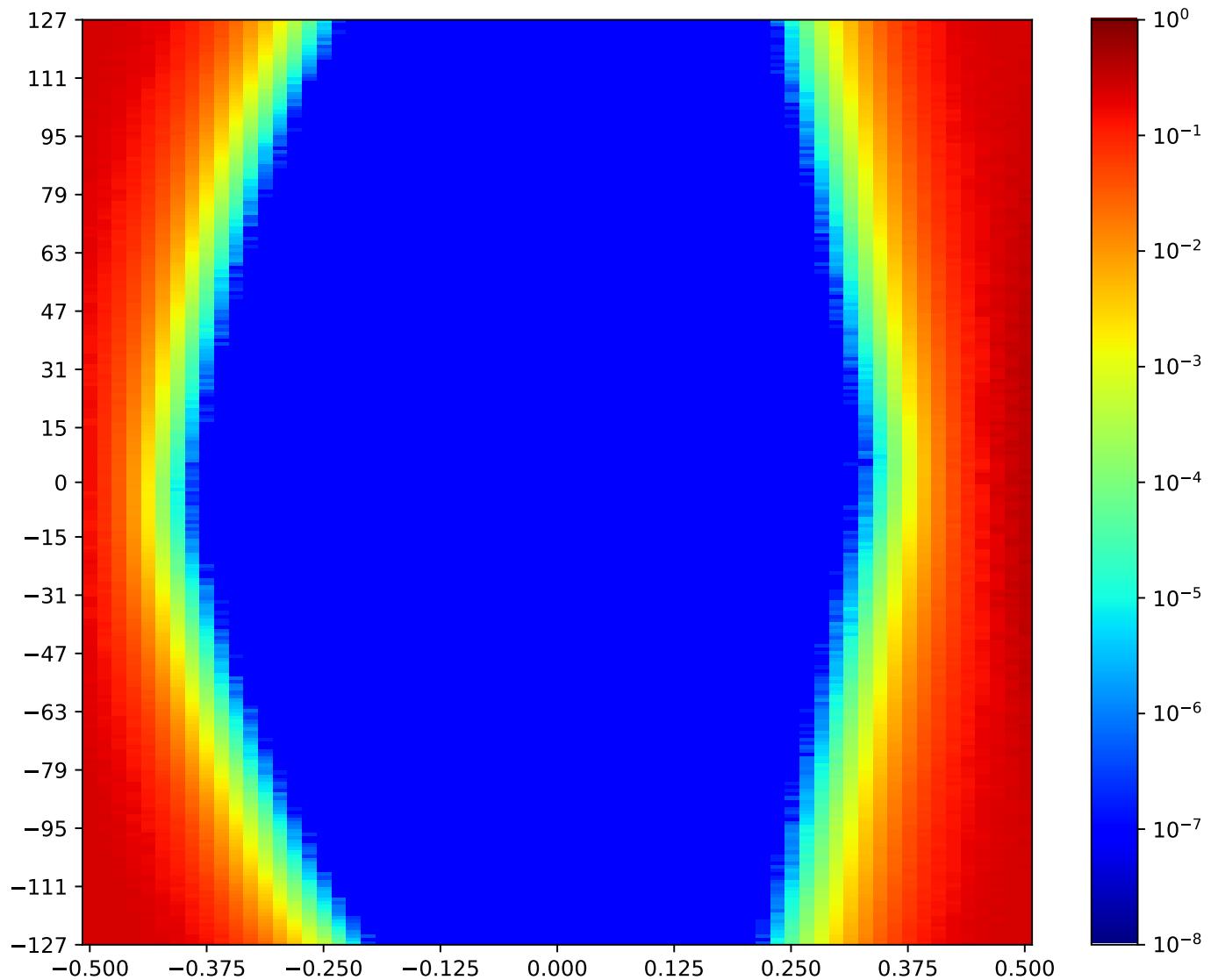


Figure 1.252: MSP\_A\_FPGA-TX1-11-RX13-11-MSP\_C\_FPGA

Call back to summary Figure 1.240. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.20 MSP\_A TX2 MSP\_C RX12 Minipod Loopback

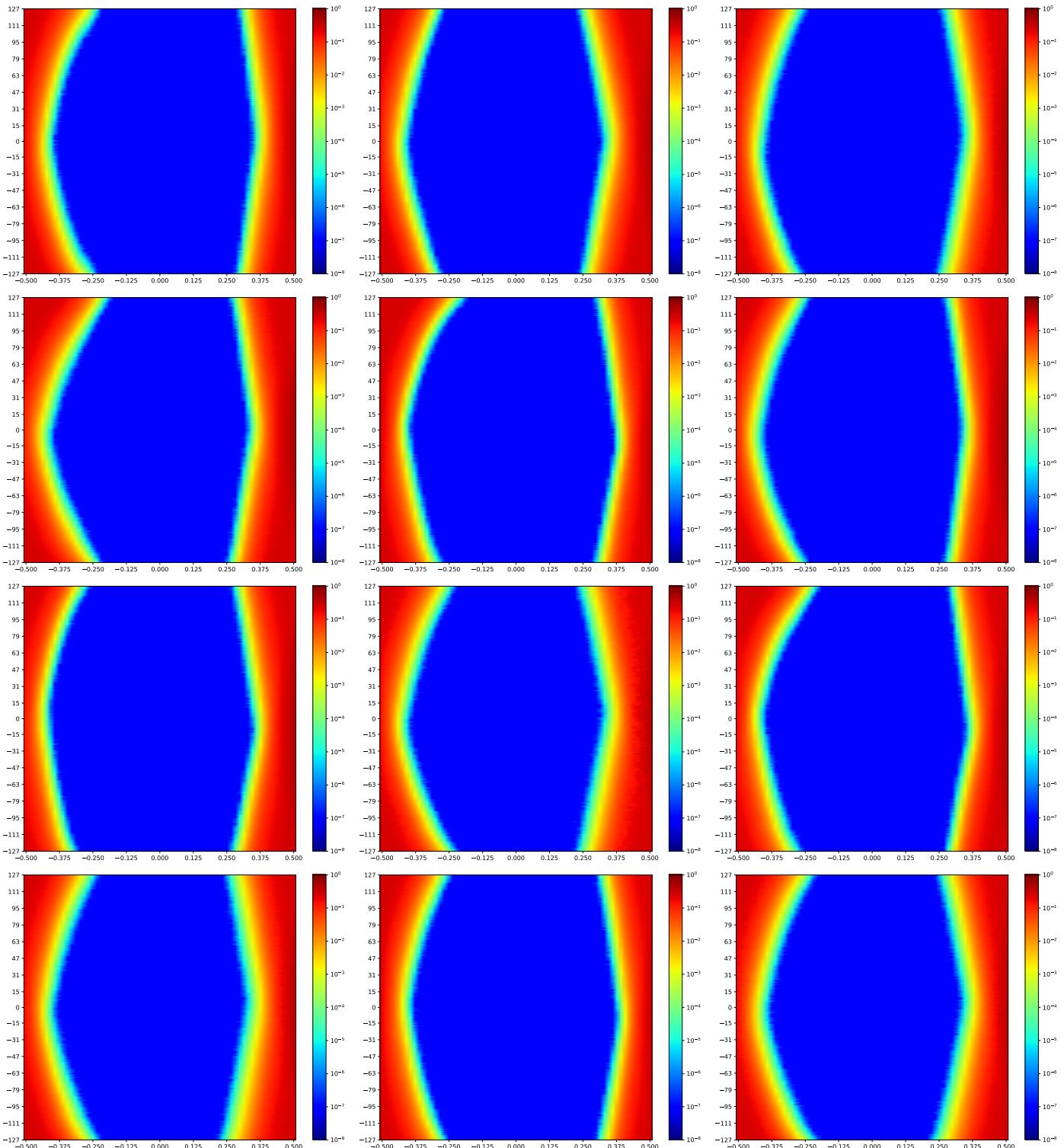


Figure 1.253: MSP\_A TX2 MSP\_C RX12 Minipod Loopback

A cross-reference to Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.266.

### 1.20.1 MSP\_A\_FPGA-TX2-00-RX12-00-MSP\_C\_FPGA

Table 1.234: MSP\_A\_FPGA-TX2-00-RX12-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:40:25		2018-Jan-24 17:41:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10309	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

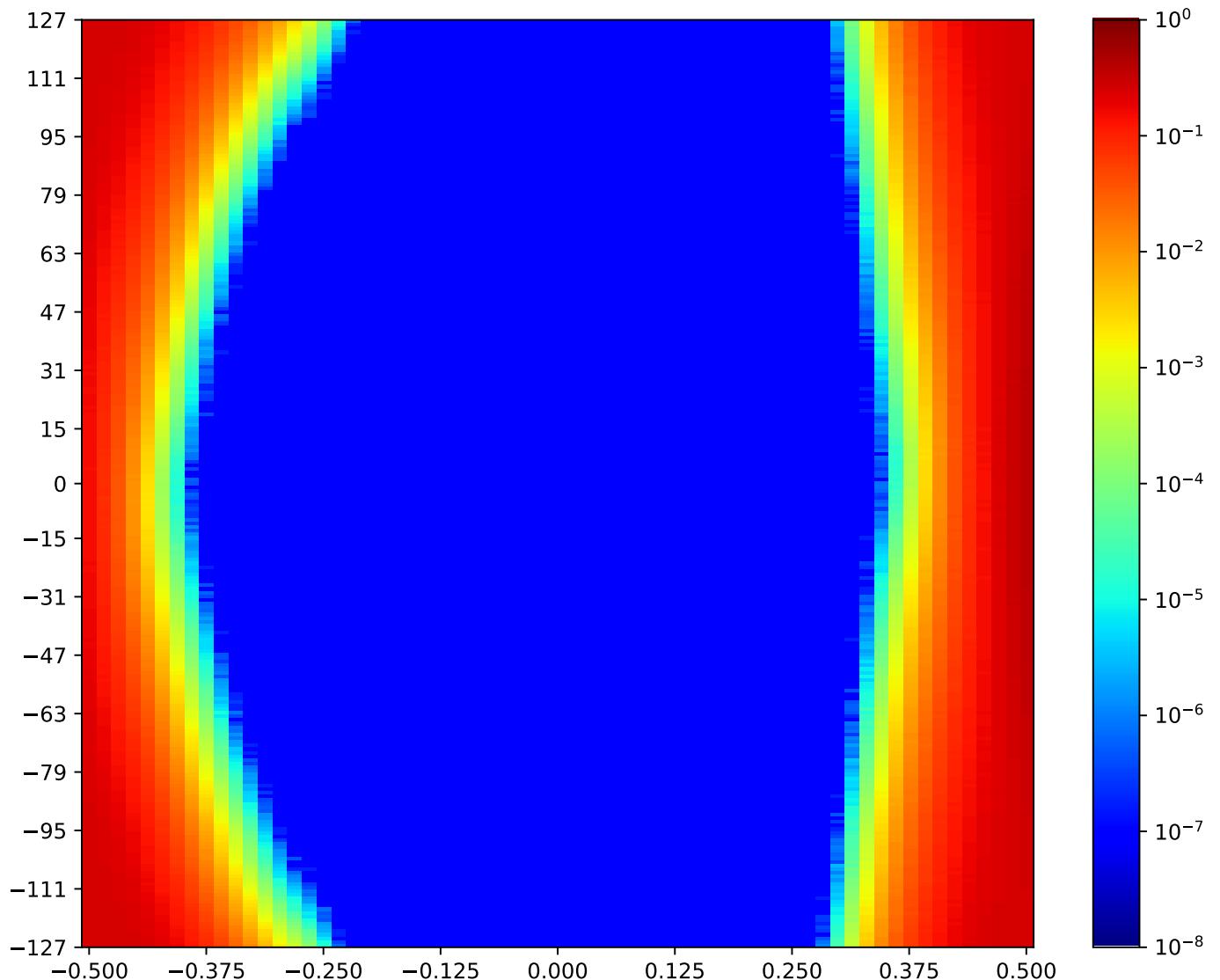


Figure 1.254: MSP\_A\_FPGA-TX2-00-RX12-00-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.20.2 MSP\_A\_FPGA-TX2-01-RX12-01-MSP\_C\_FPGA

Table 1.235: MSP\_A\_FPGA-TX2-01-RX12-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:39:14		2018-Jan-24 17:39:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9844	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

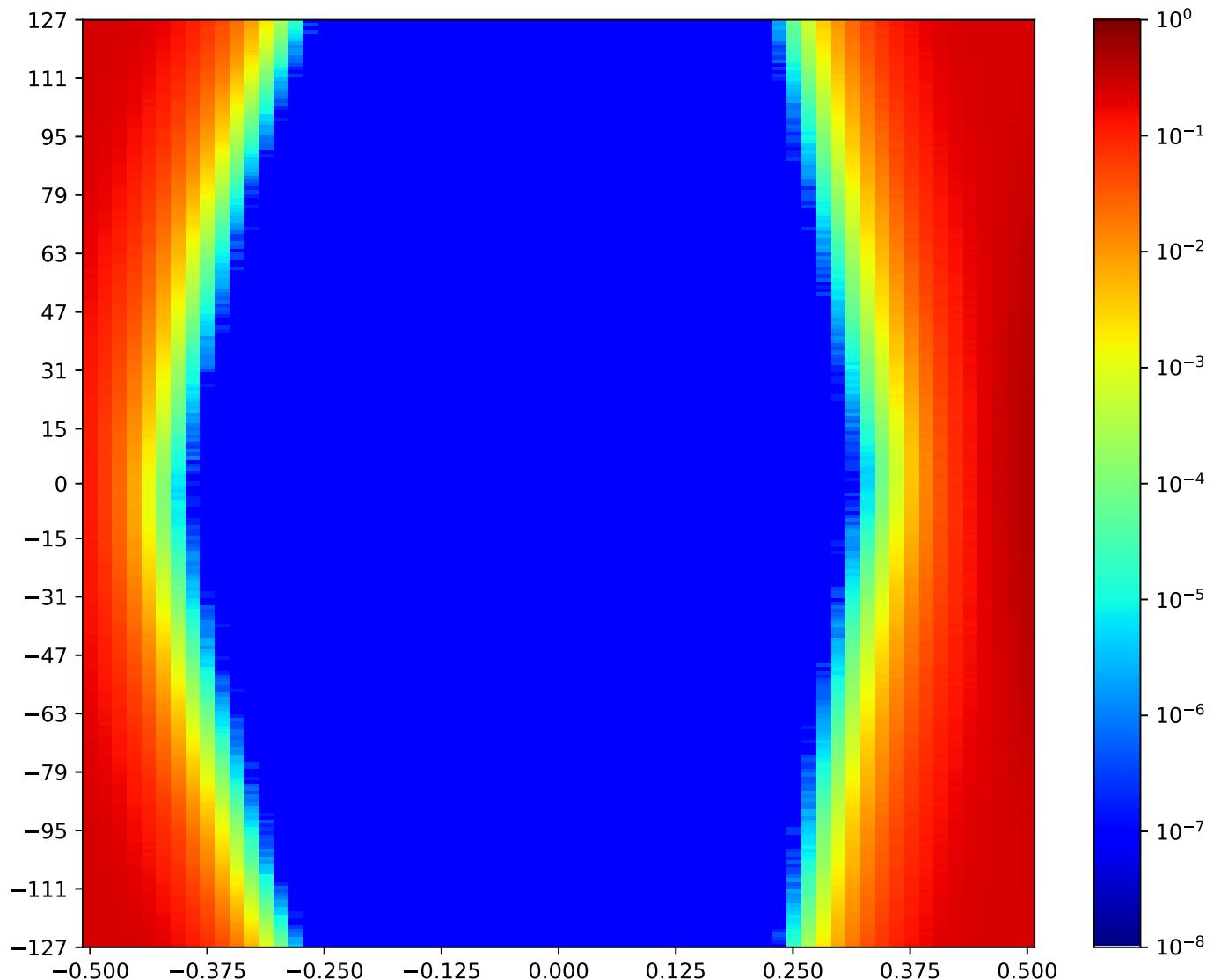


Figure 1.255: MSP\_A\_FPGA-TX2-01-RX12-01-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.20.3 MSP\_A\_FPGA-TX2-02-RX12-02-MSP\_C\_FPGA

Table 1.236: MSP\_A\_FPGA-TX2-02-RX12-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:42:12		2018-Jan-24 17:42:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9925	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

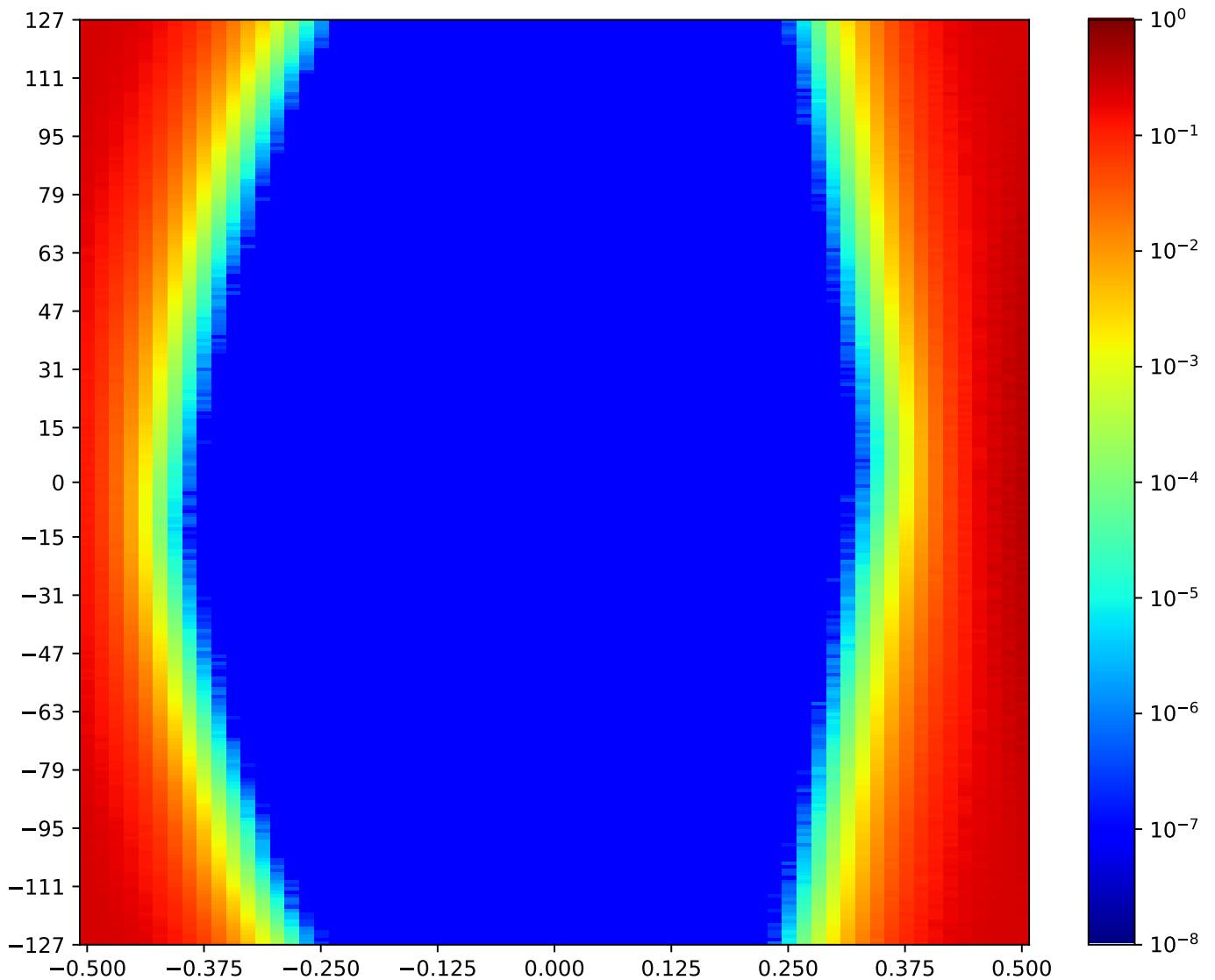


Figure 1.256: MSP\_A\_FPGA-TX2-02-RX12-02-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.20.4 MSP\_A\_FPGA-TX2-03-RX12-03-MSP\_C\_FPGA

Table 1.237: MSP\_A\_FPGA-TX2-03-RX12-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:38:39		2018-Jan-24 17:39:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9632	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

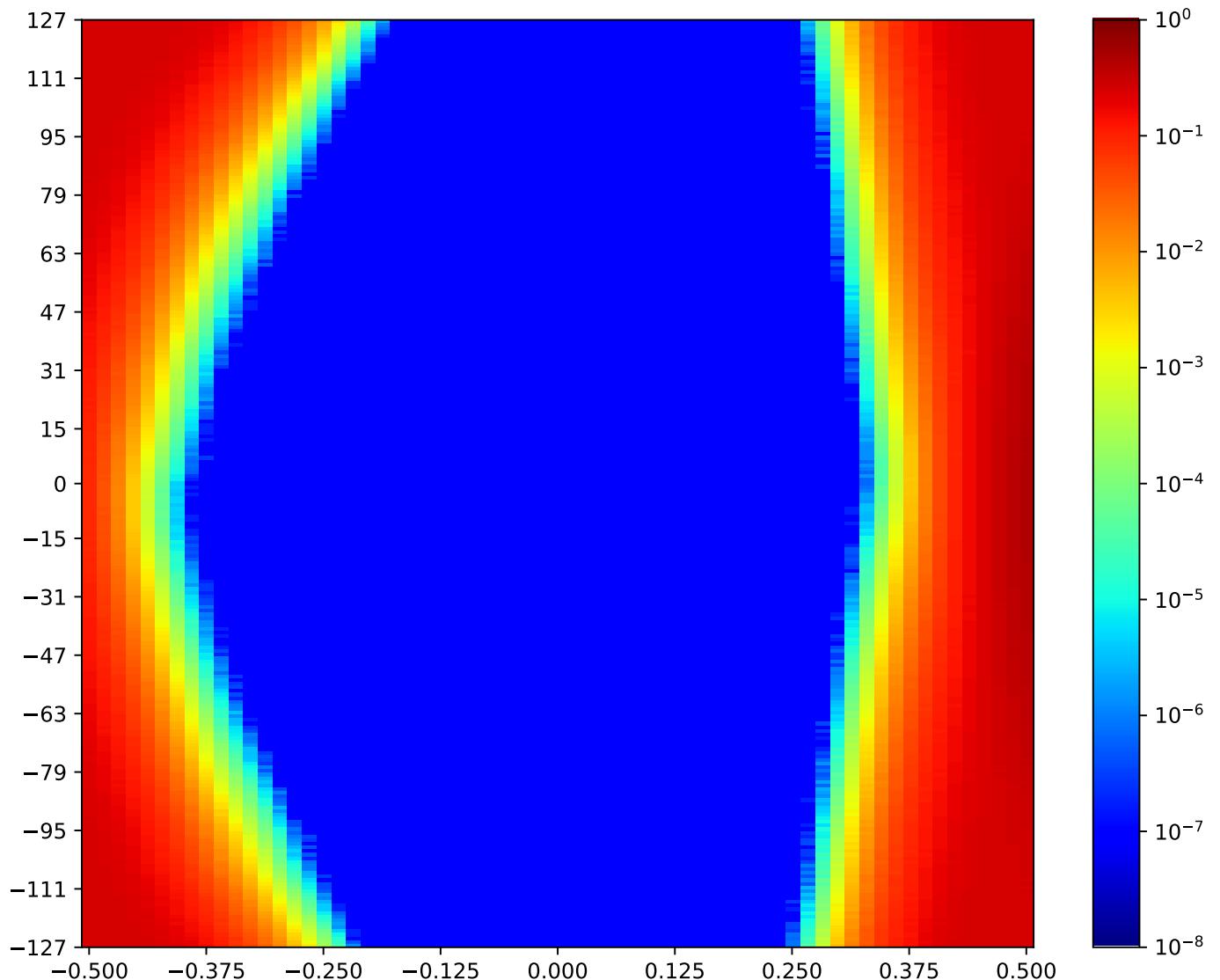


Figure 1.257: MSP\_A\_FPGA-TX2-03-RX12-03-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.20.5 MSP\_A\_FPGA-TX2-04-RX12-04-MSP\_C\_FPGA

Table 1.238: MSP\_A\_FPGA-TX2-04-RX12-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:44:01		2018-Jan-24 17:44:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10527	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

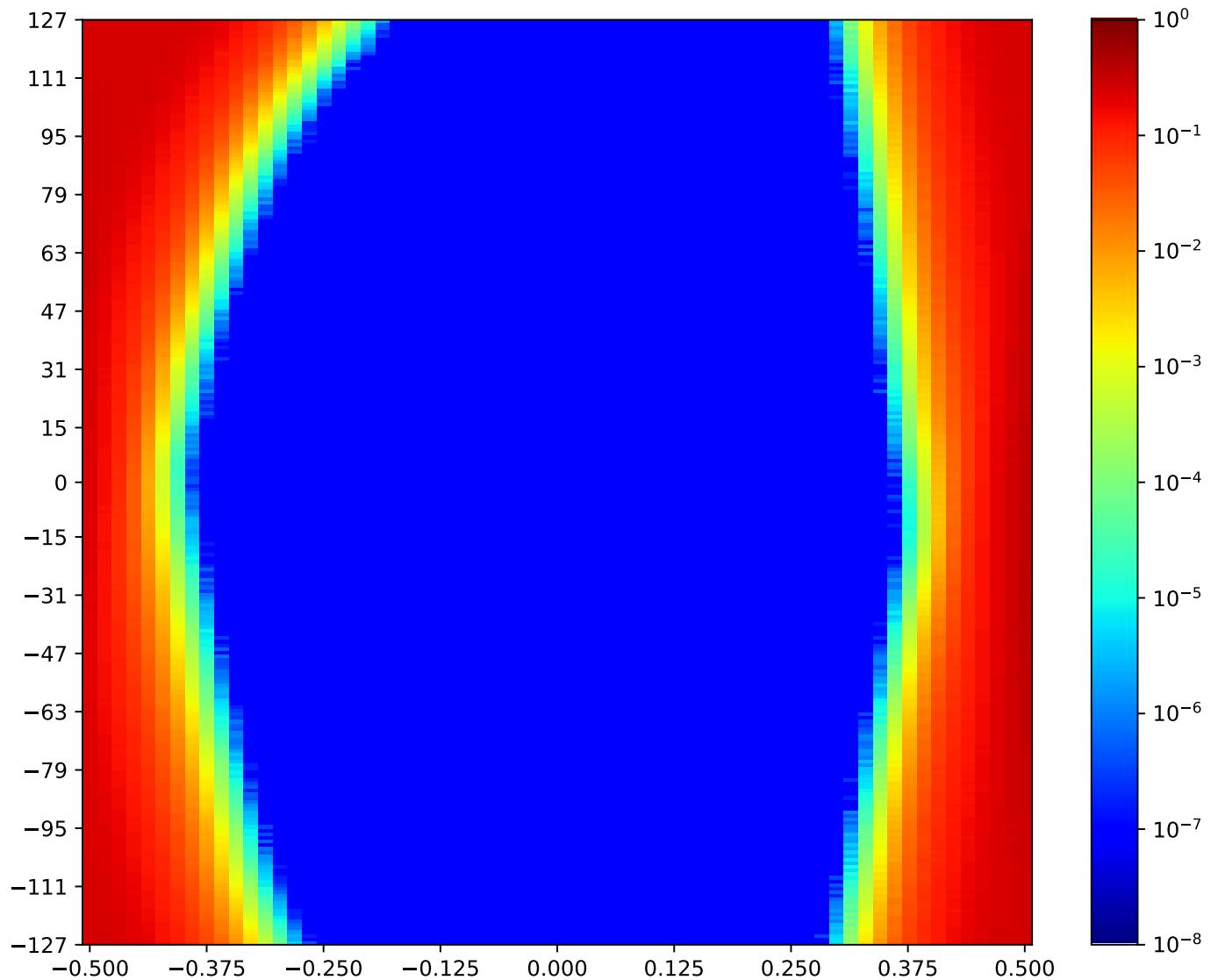


Figure 1.258: MSP\_A\_FPGA-TX2-04-RX12-04-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.20.6 MSP\_A\_FPGA-TX2-05-RX12-05-MSP\_C\_FPGA

Table 1.239: MSP\_A\_FPGA-TX2-05-RX12-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:39:49		2018-Jan-24 17:40:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10060	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

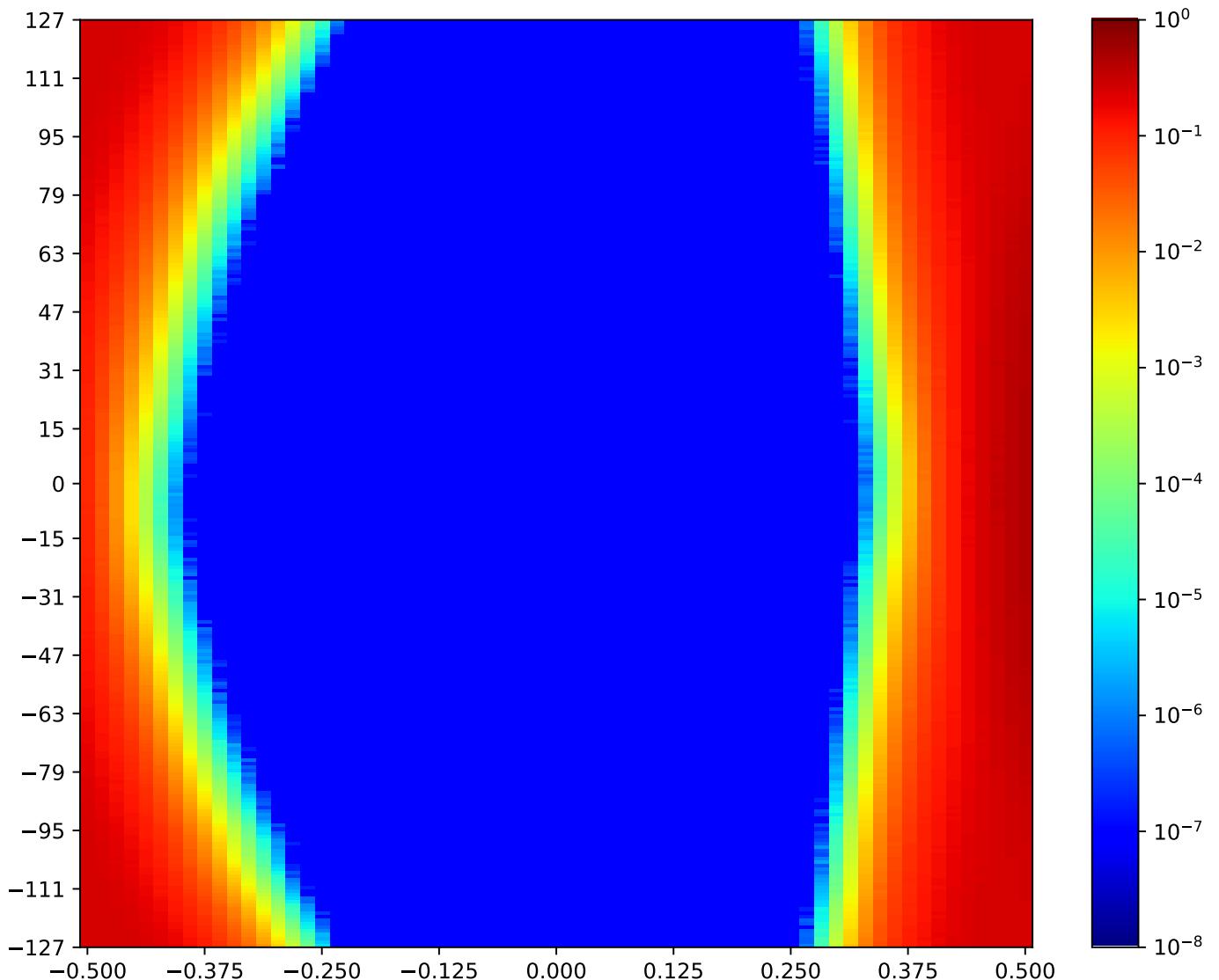


Figure 1.259: MSP\_A\_FPGA-TX2-05-RX12-05-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.20.7 MSP\_A\_FPGA-TX2-06-RX12-06-MSP\_C\_FPGA

Table 1.240: MSP\_A\_FPGA-TX2-06-RX12-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:45:14		2018-Jan-24 17:45:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10641	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

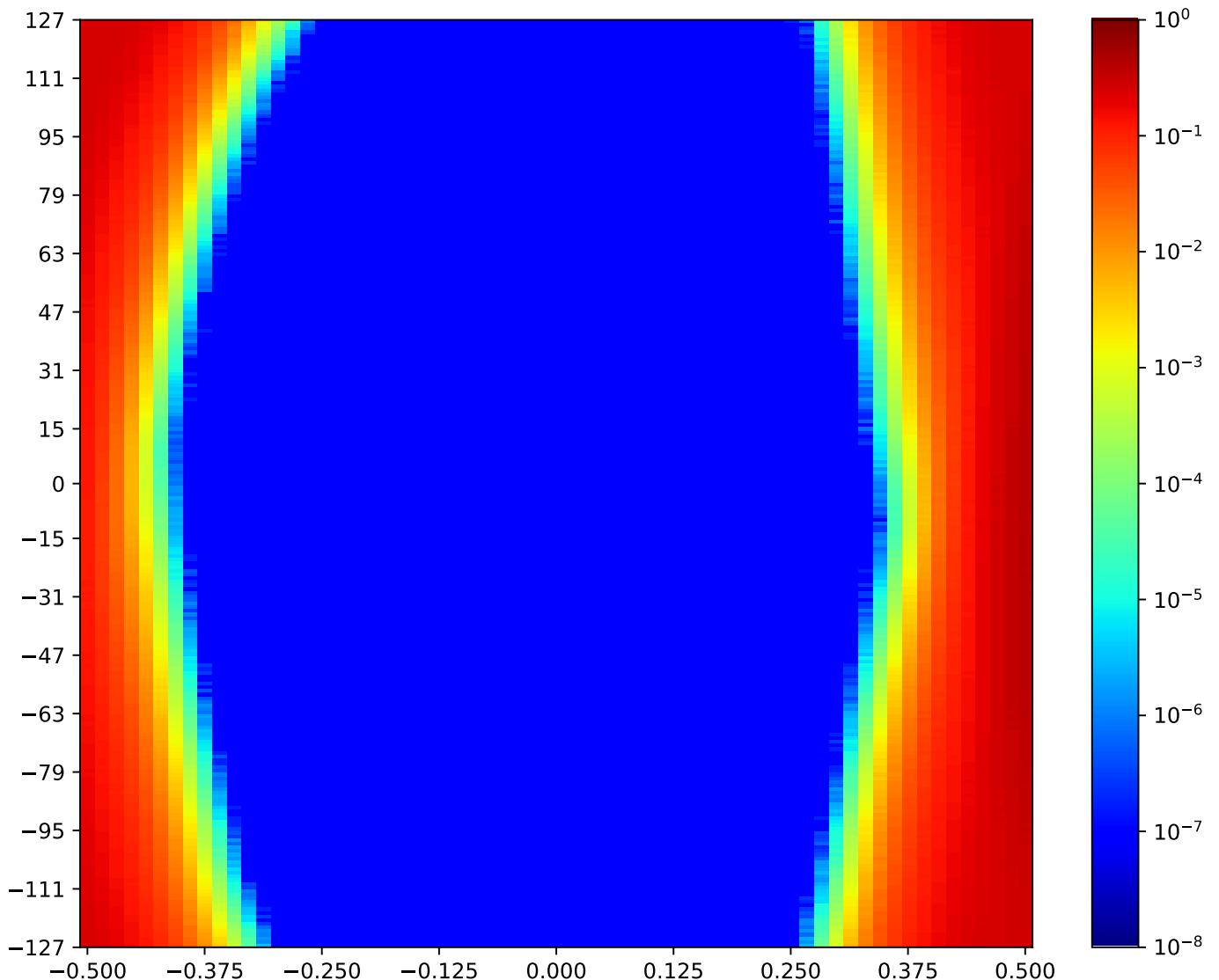


Figure 1.260: MSP\_A\_FPGA-TX2-06-RX12-06-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.20.8 MSP\_A\_FPGA-TX2-07-RX12-07-MSP\_C\_FPGA

Table 1.241: MSP\_A\_FPGA-TX2-07-RX12-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:41:01		2018-Jan-24 17:41:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9436	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

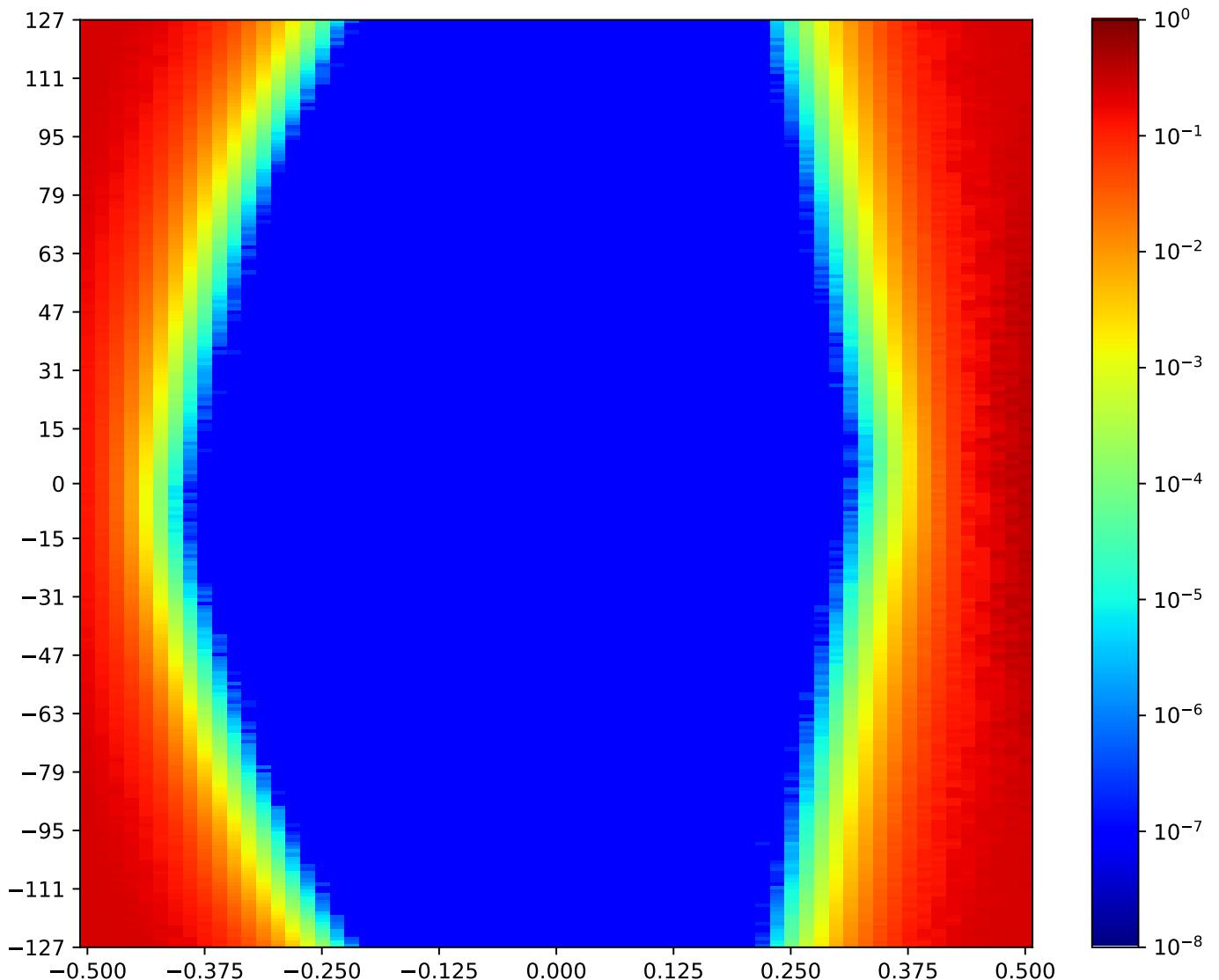


Figure 1.261: MSP\_A\_FPGA-TX2-07-RX12-07-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.20.9 MSP\_A\_FPGA-TX2-08-RX12-08-MSP\_C\_FPGA

Table 1.242: MSP\_A\_FPGA-TX2-08-RX12-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:44:37		2018-Jan-24 17:45:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10209	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

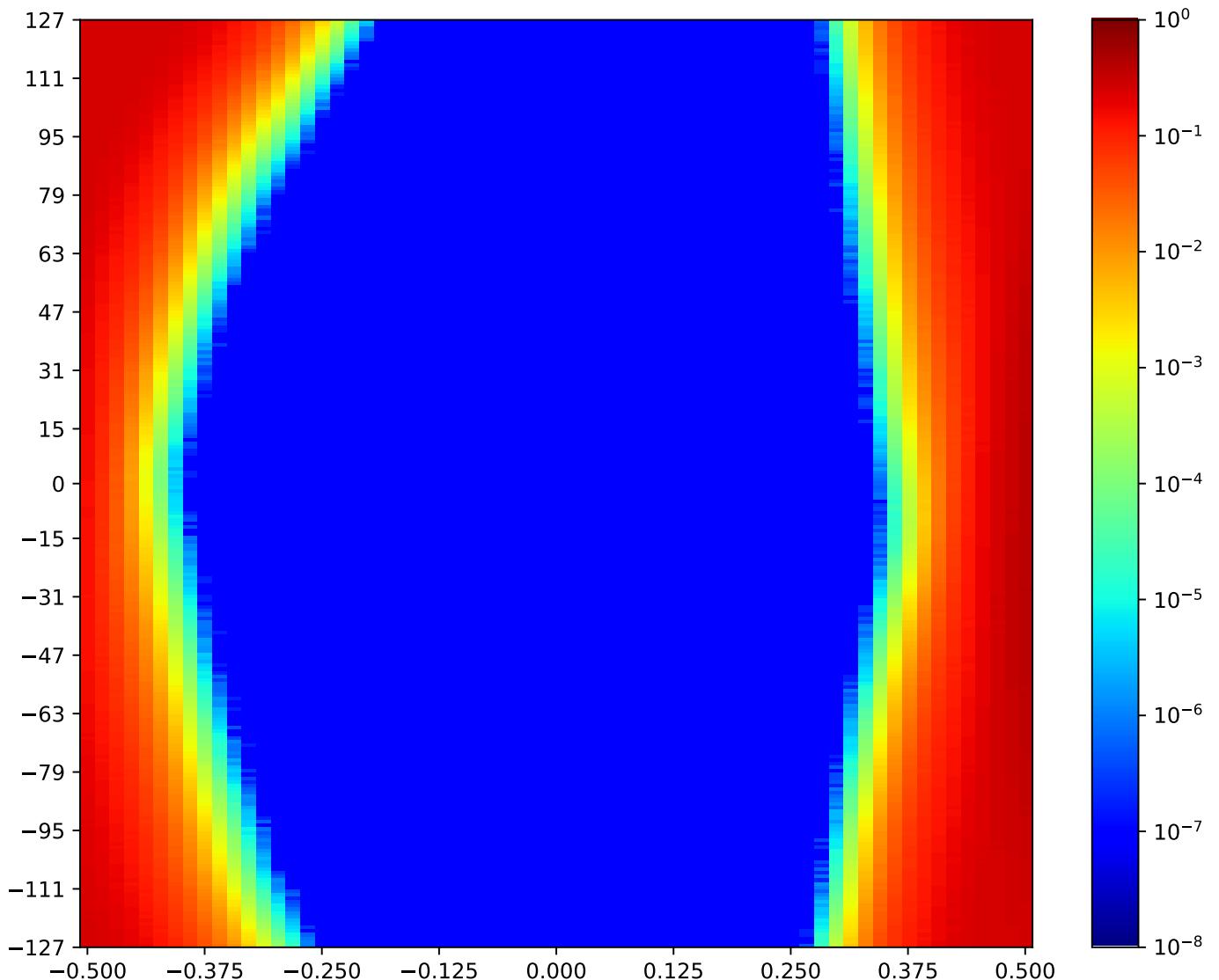


Figure 1.262: MSP\_A\_FPGA-TX2-08-RX12-08-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.20.10 MSP\_A\_FPGA-TX2-09-RX12-09-MSP\_C\_FPGA

Table 1.243: MSP\_A\_FPGA-TX2-09-RX12-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:41:37		2018-Jan-24 17:42:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9434	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

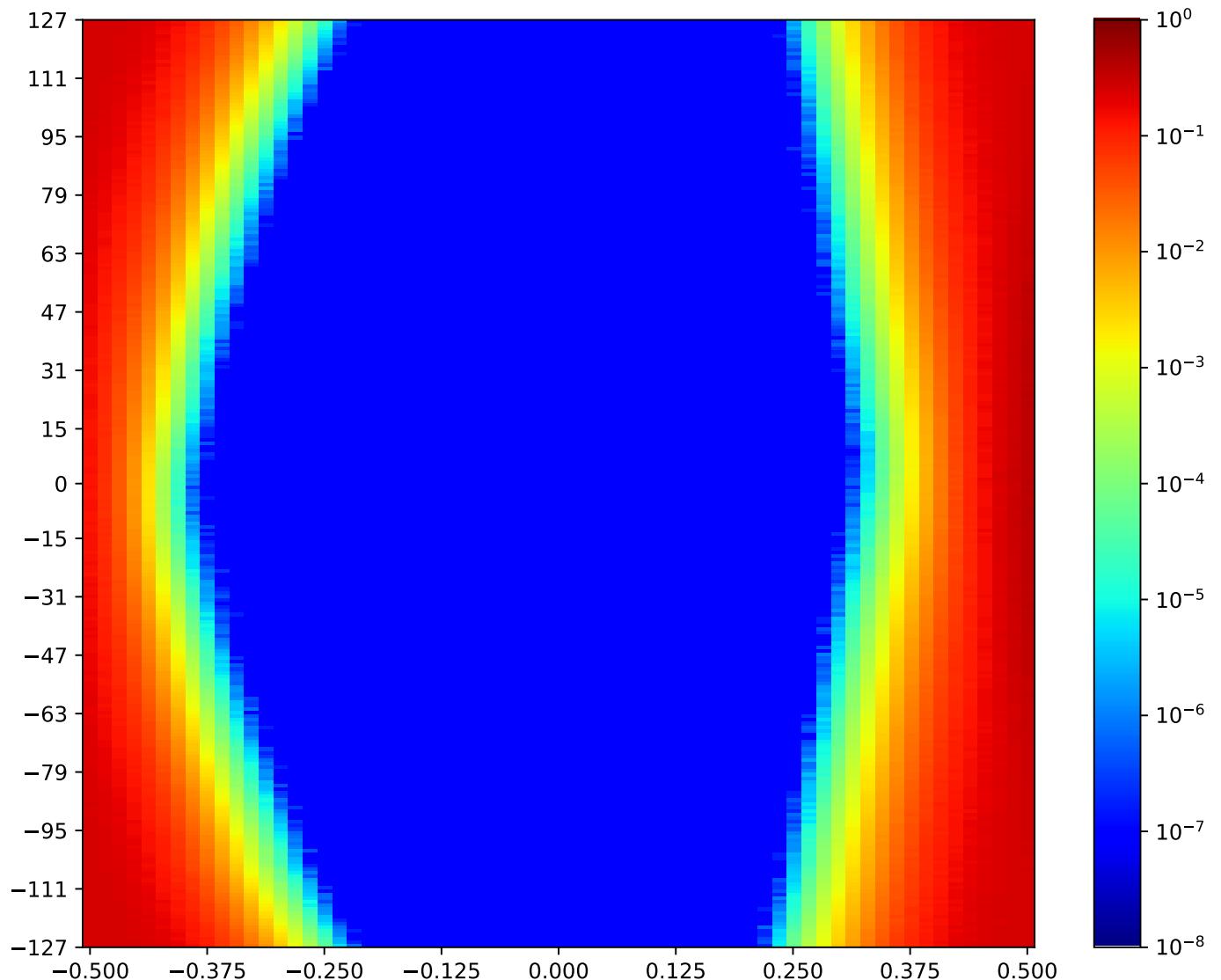


Figure 1.263: MSP\_A\_FPGA-TX2-09-RX12-09-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.20.11 MSP\_A\_FPGA-TX2-10-RX12-10-MSP\_C\_FPGA

Table 1.244: MSP\_A\_FPGA-TX2-10-RX12-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:43:24		2018-Jan-24 17:44:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10612	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

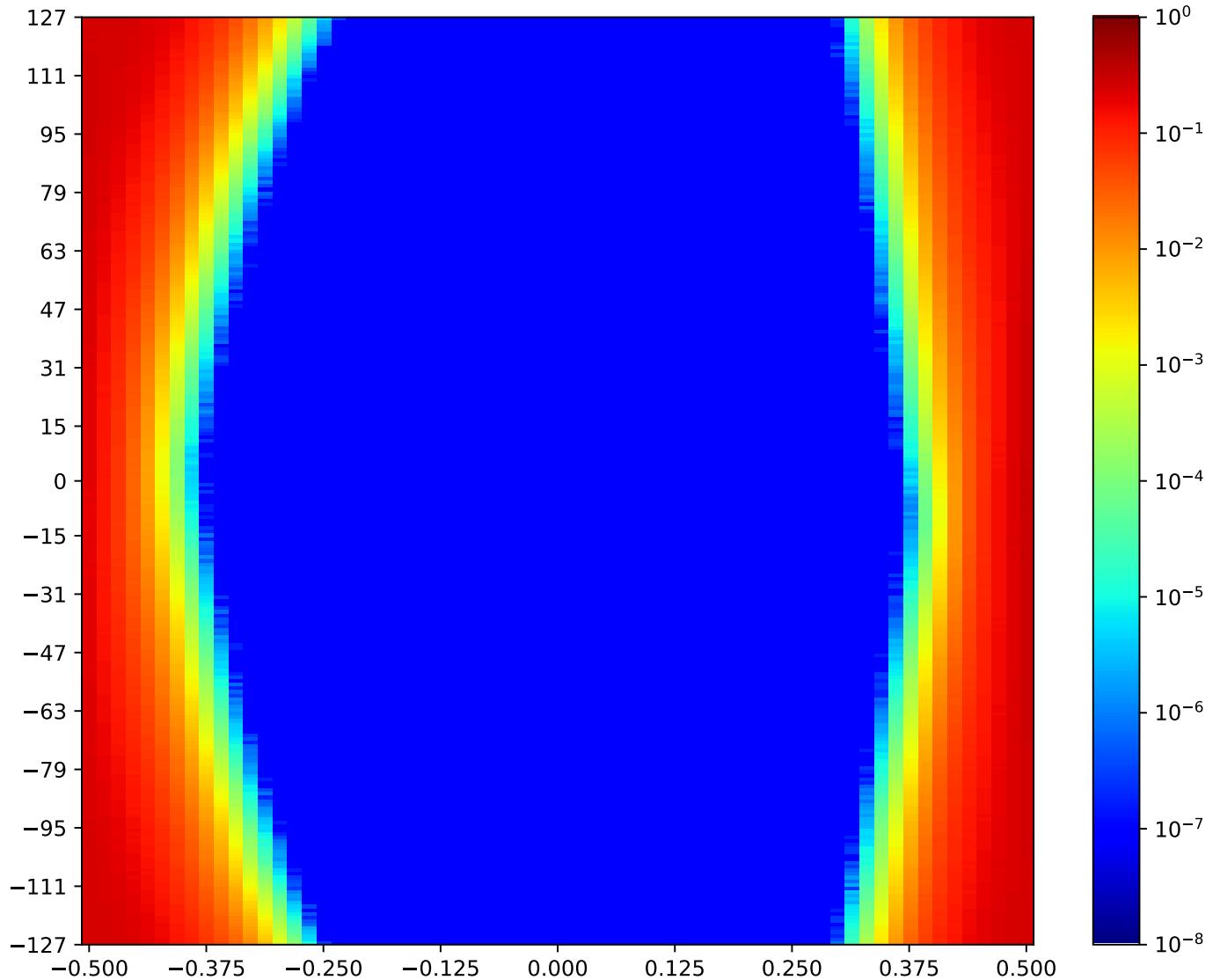


Figure 1.264: MSP\_A\_FPGA-TX2-10-RX12-10-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.20.12 MSP\_A\_FPGA-TX2-11-RX12-11-MSP\_C\_FPGA

Table 1.245: MSP\_A\_FPGA-TX2-11-RX12-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:42:48		2018-Jan-24 17:43:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9389	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

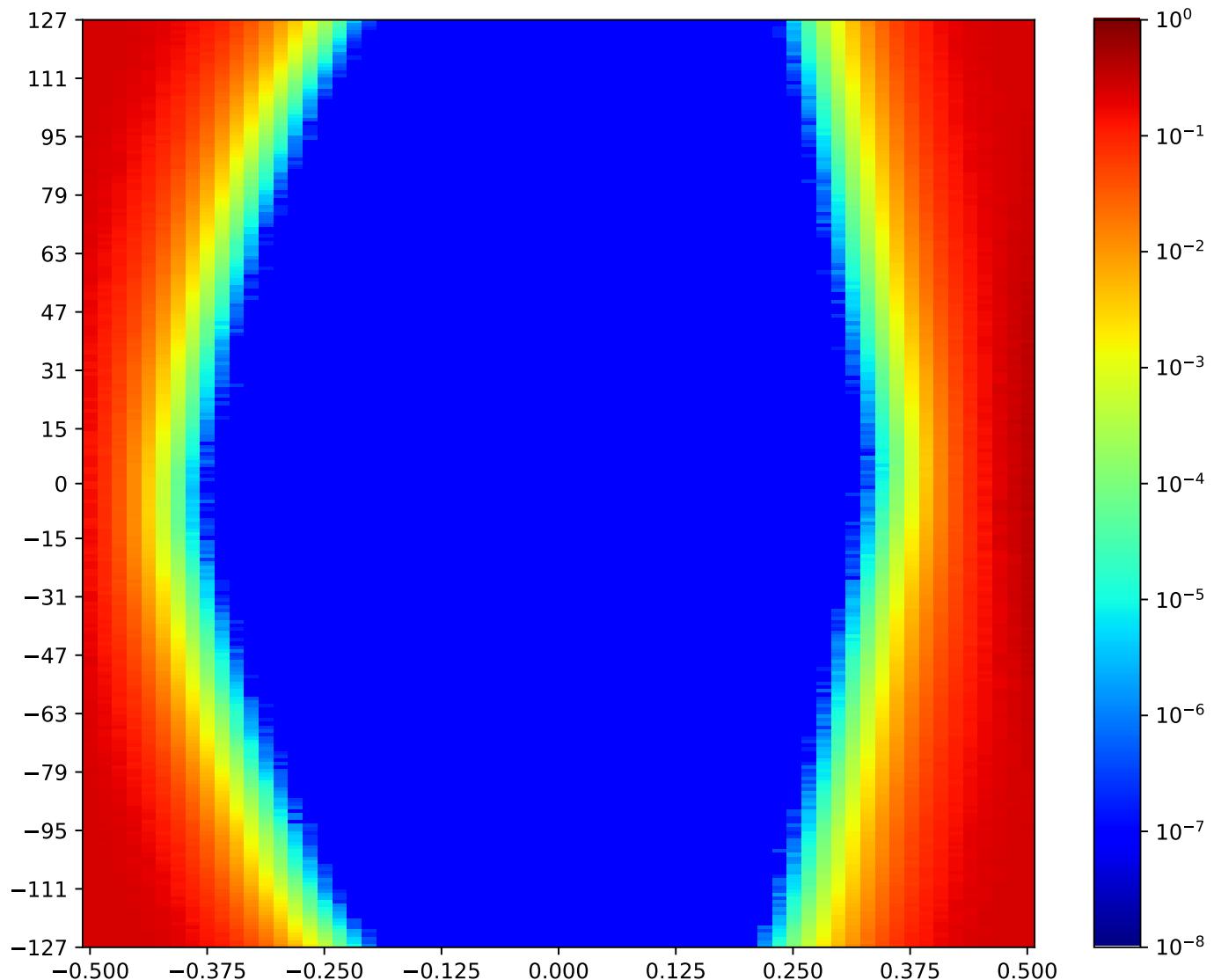


Figure 1.265: MSP\_A\_FPGA-TX2-11-RX12-11-MSP\_C\_FPGA

Call back to summary Figure 1.253. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.21 MSP\_C TX3 MSP\_A RX4 Minipod Loopback

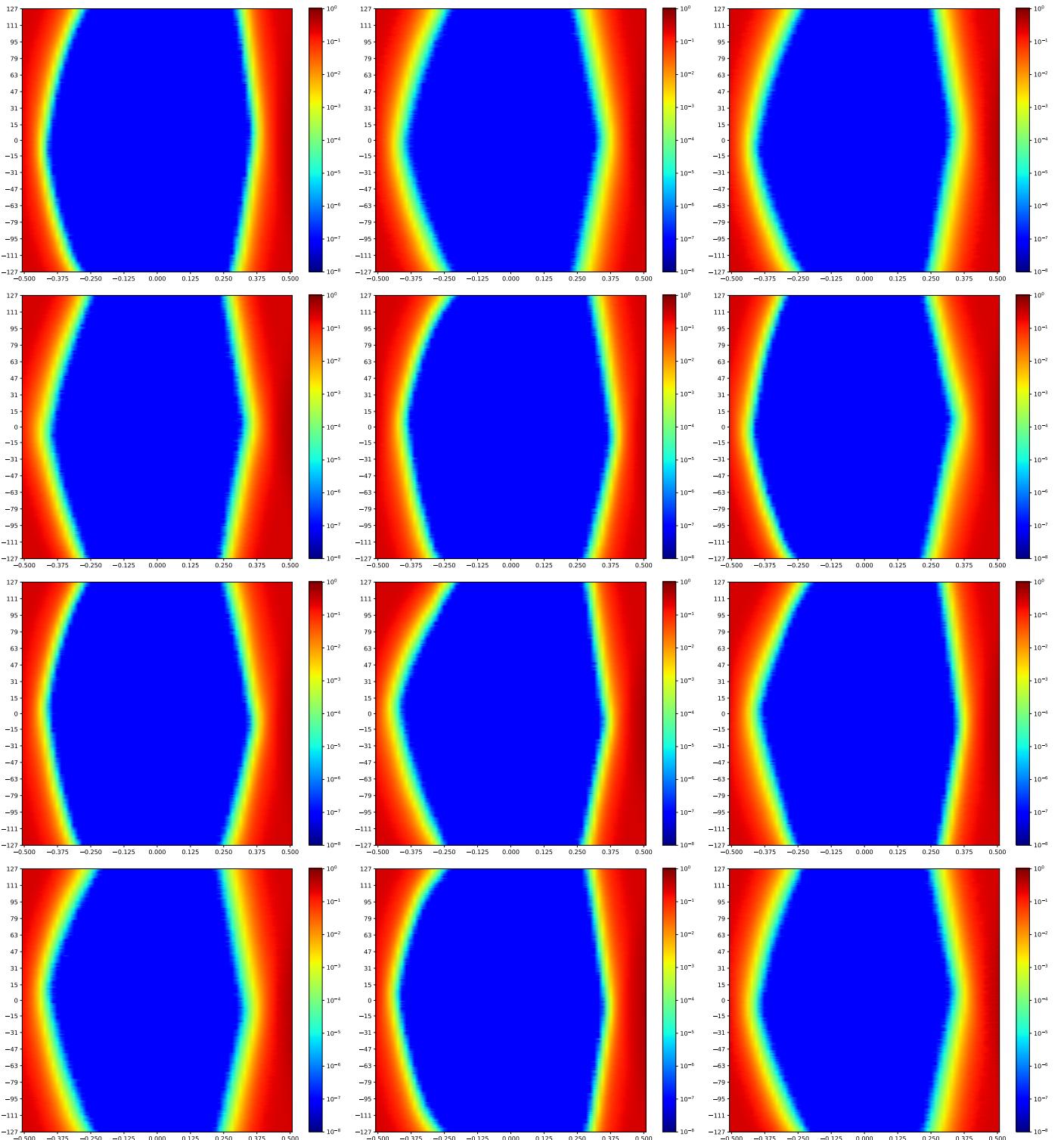


Figure 1.266: MSP\_C TX3 MSP\_A RX4 Minipod Loopback

A cross-reference to Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 1.279.

### 1.21.1 MSP\_C\_FPGA-TX3-00-RX4-00-MSP\_A\_FPGA

Table 1.246: MSP\_C\_FPGA-TX3-00-RX4-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:47:37		2018-Jan-24 17:48:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10745	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

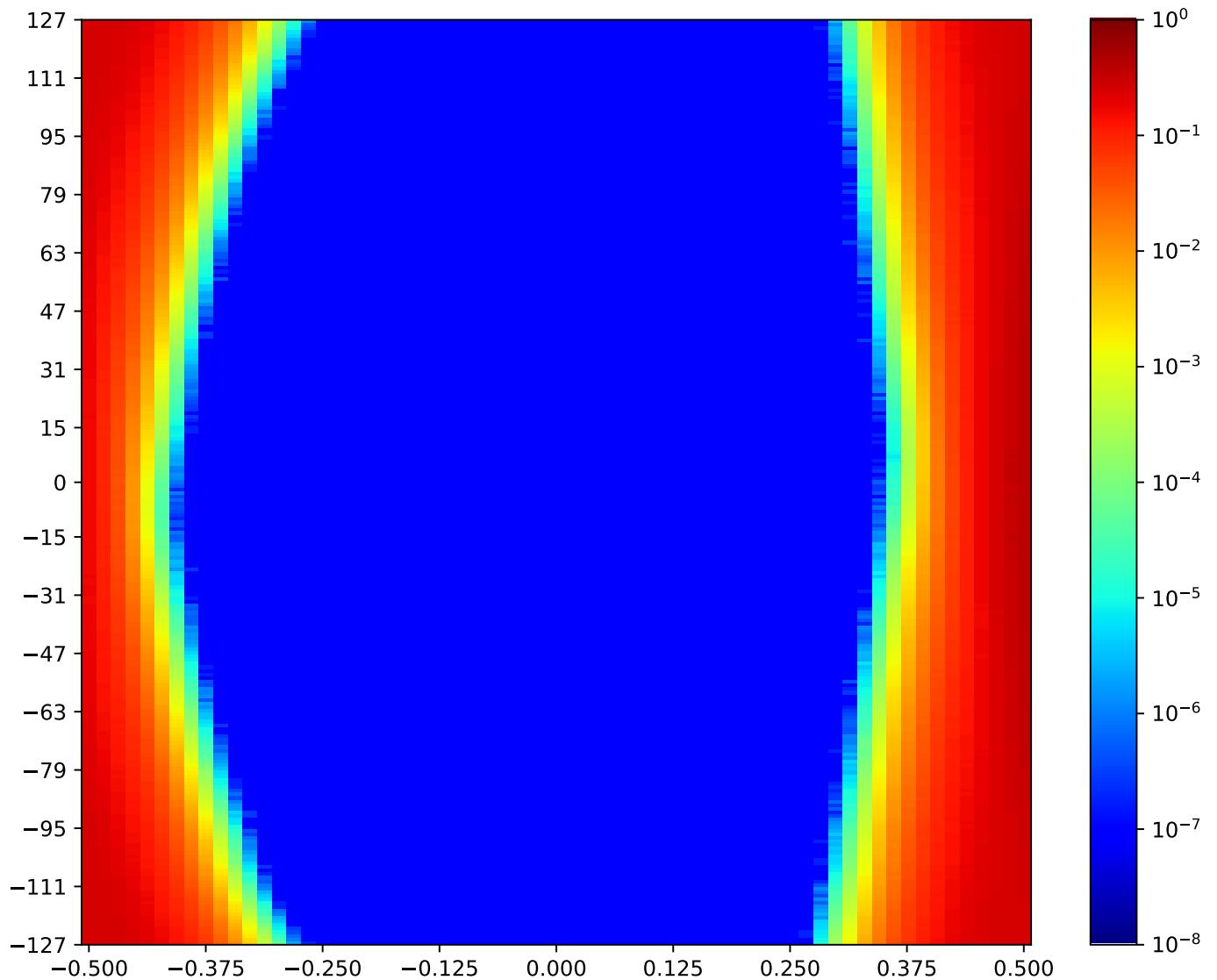


Figure 1.267: MSP\_C\_FPGA-TX3-00-RX4-00-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.2 MSP\_C\_FPGA-TX3-01-RX4-01-MSP\_A\_FPGA

Table 1.247: MSP\_C\_FPGA-TX3-01-RX4-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:48:49		2018-Jan-24 17:49:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9327	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

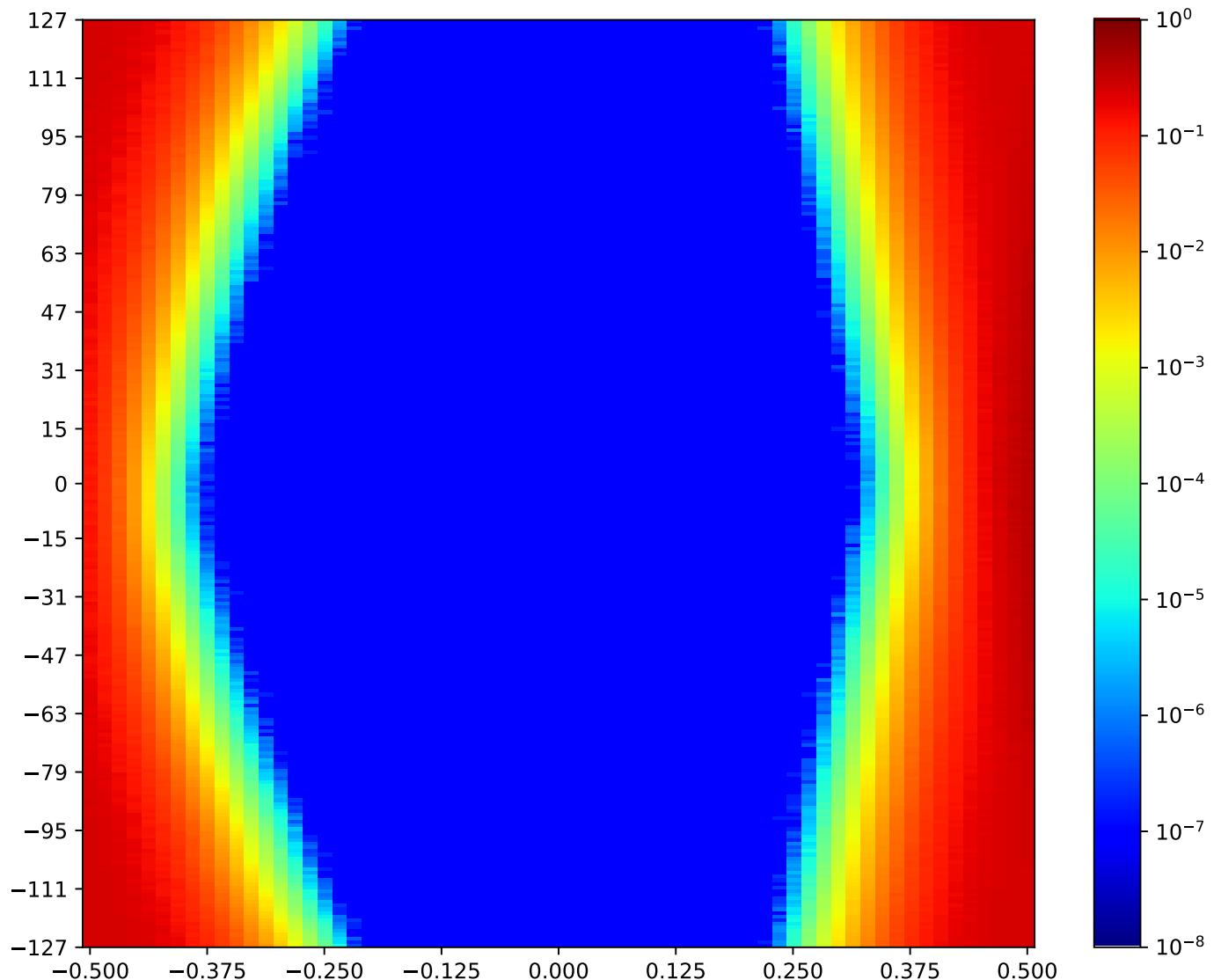


Figure 1.268: MSP\_C\_FPGA-TX3-01-RX4-01-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.3 MSP\_C\_FPGA-TX3-02-RX4-02-MSP\_A\_FPGA

Table 1.248: MSP\_C\_FPGA-TX3-02-RX4-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:49:25		2018-Jan-24 17:50:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9474	44	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

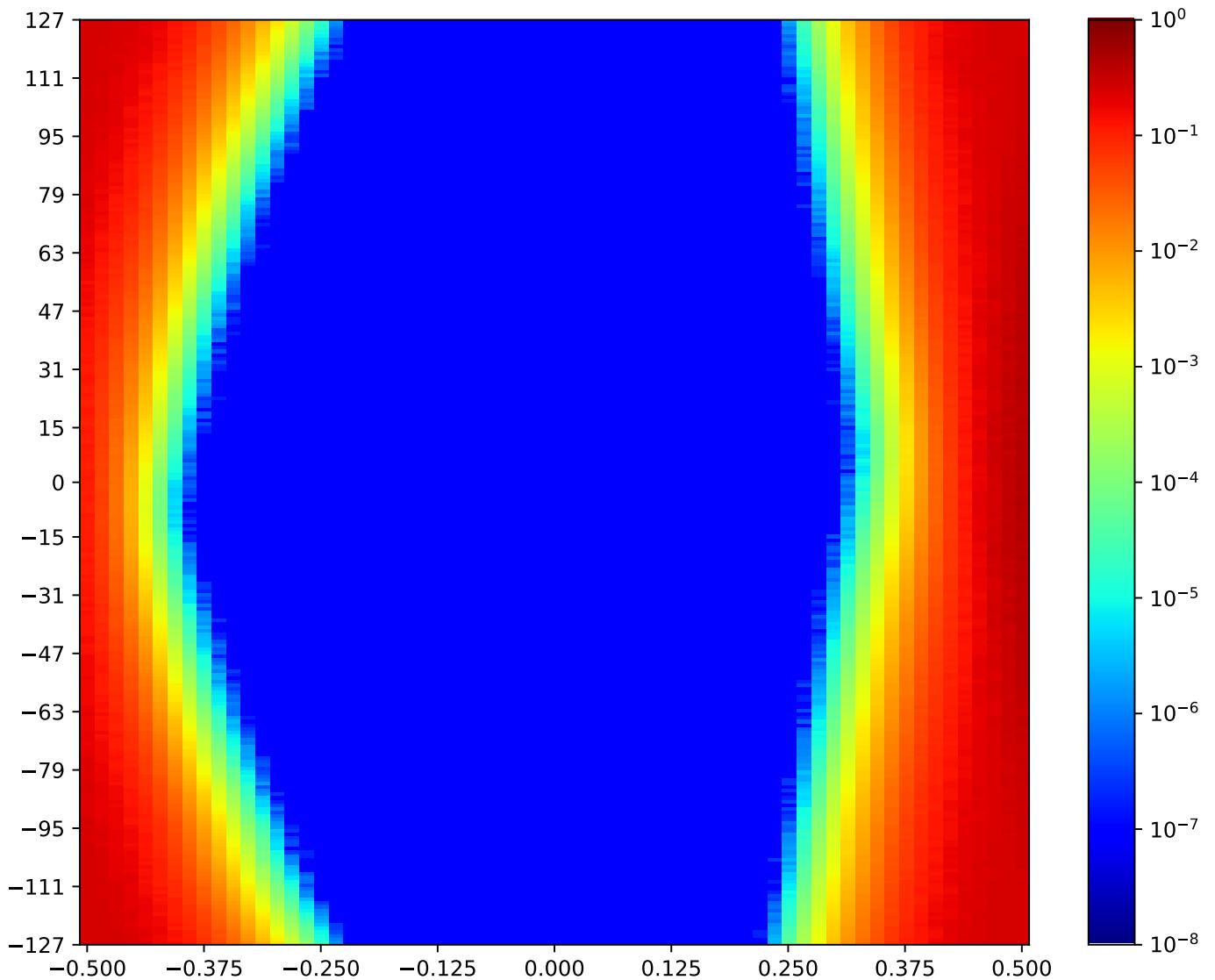


Figure 1.269: MSP\_C\_FPGA-TX3-02-RX4-02-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.21.4 MSP\_C\_FPGA-TX3-03-RX4-03-MSP\_A\_FPGA

Table 1.249: MSP\_C\_FPGA-TX3-03-RX4-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:46:26		2018-Jan-24 17:47:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9584	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

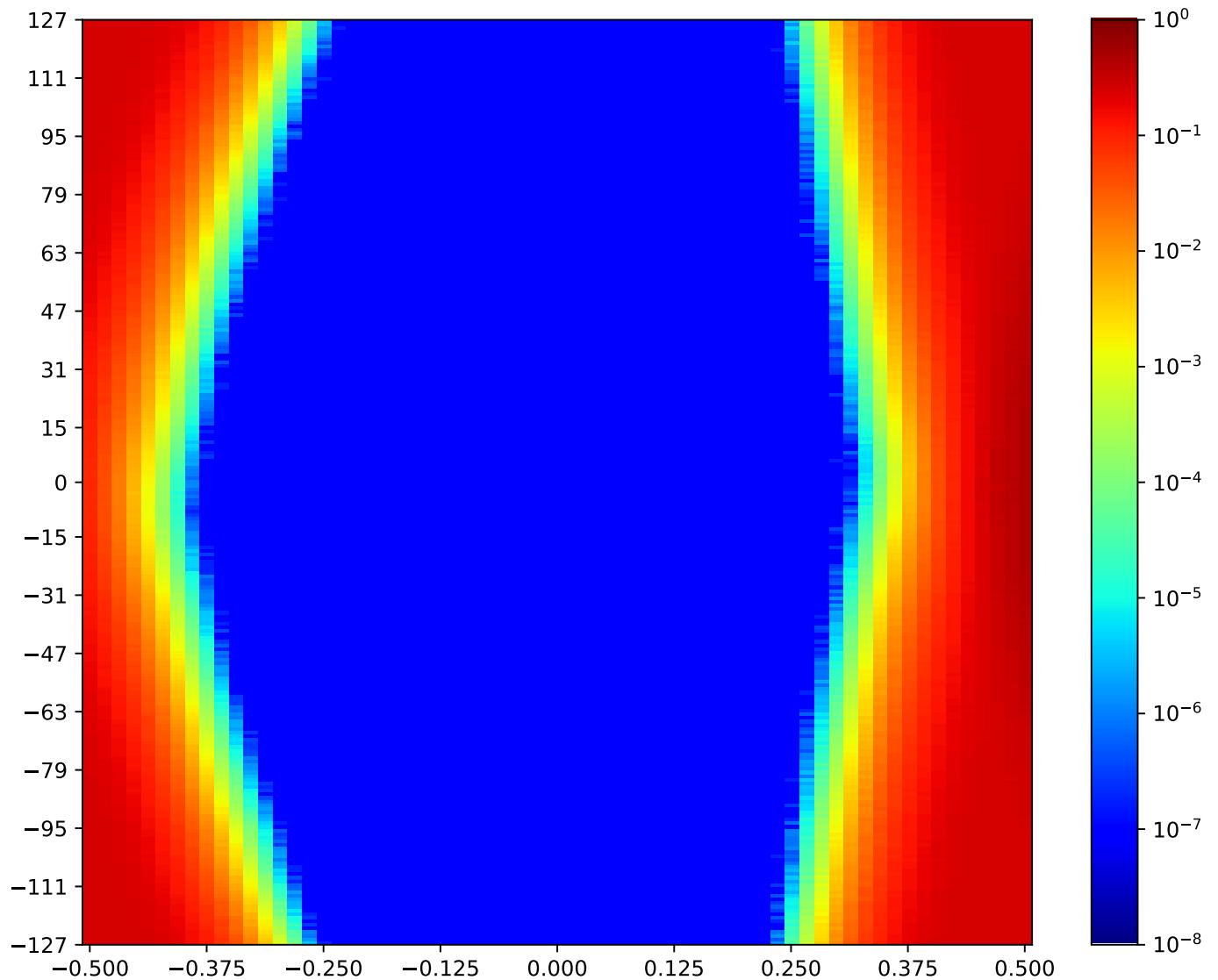


Figure 1.270: MSP\_C\_FPGA-TX3-03-RX4-03-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.5 MSP\_C\_FPGA-TX3-04-RX4-04-MSP\_A\_FPGA

Table 1.250: MSP\_C\_FPGA-TX3-04-RX4-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:51:13		2018-Jan-24 17:51:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10410	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

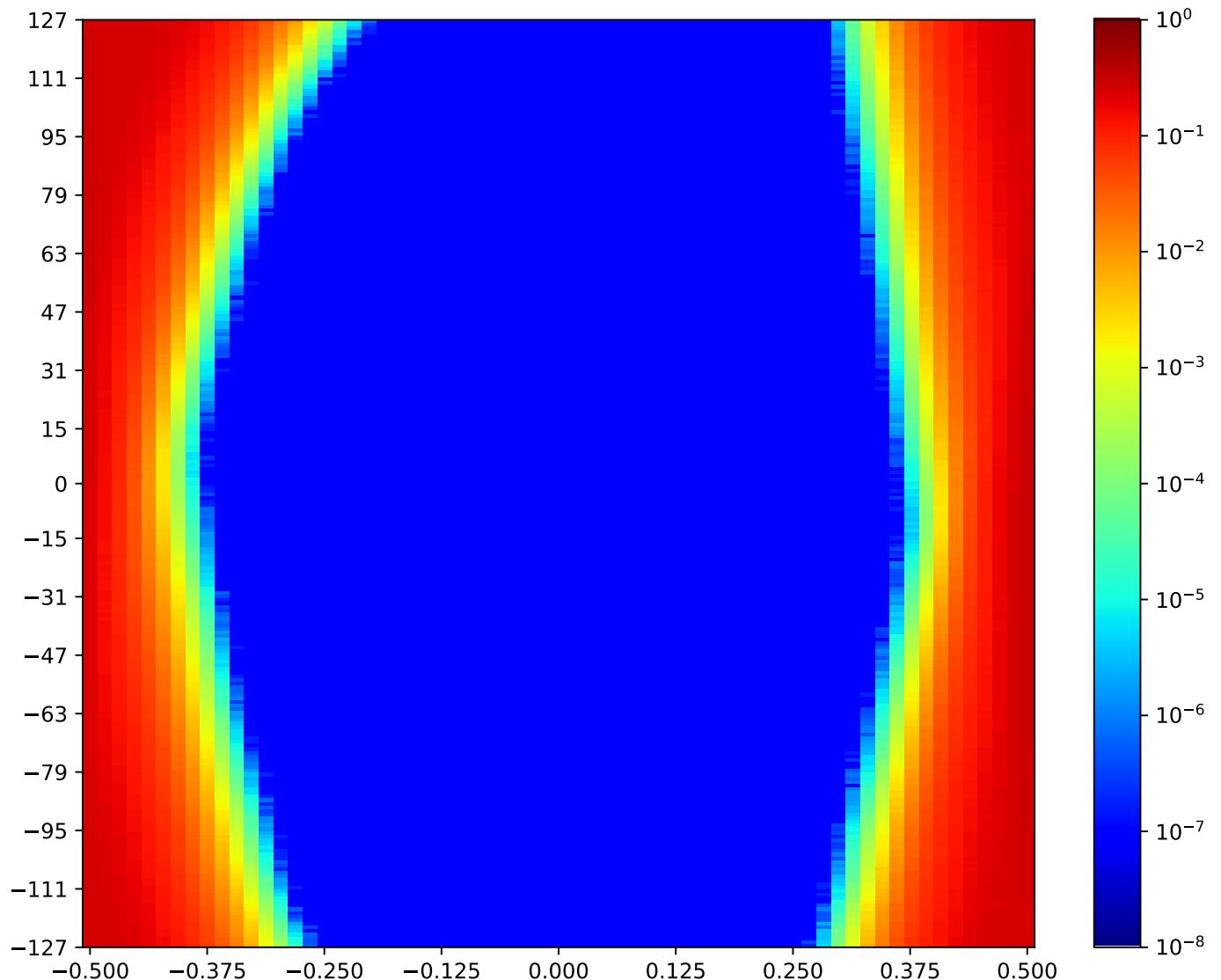


Figure 1.271: MSP\_C\_FPGA-TX3-04-RX4-04-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.6 MSP\_C\_FPGA-TX3-05-RX4-05-MSP\_A\_FPGA

Table 1.251: MSP\_C\_FPGA-TX3-05-RX4-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:45:50		2018-Jan-24 17:46:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9895	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

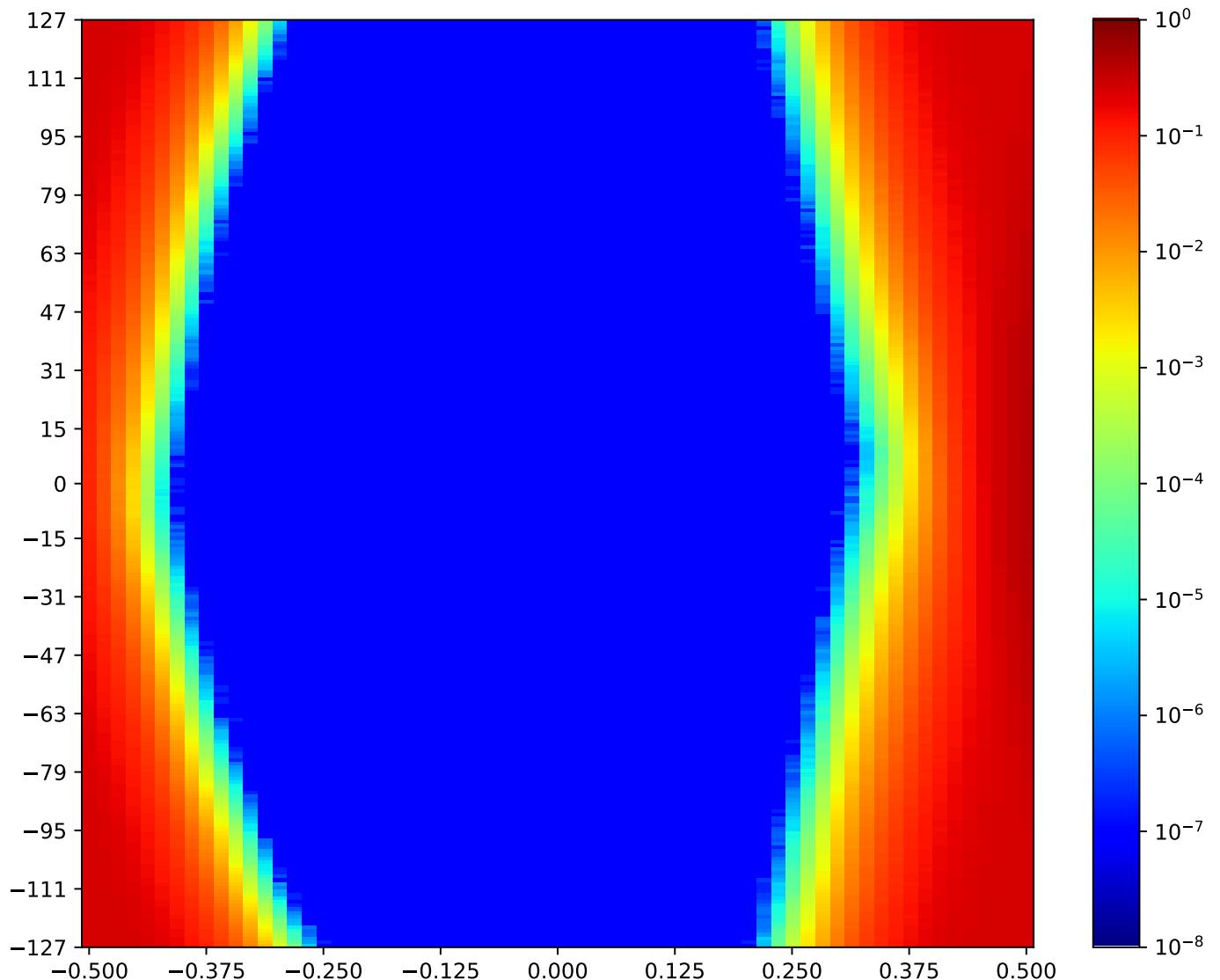


Figure 1.272: MSP\_C\_FPGA-TX3-05-RX4-05-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.7 MSP\_C\_FPGA-TX3-06-RX4-06-MSP\_A\_FPGA

Table 1.252: MSP\_C\_FPGA-TX3-06-RX4-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:52:24		2018-Jan-24 17:53:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10308	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

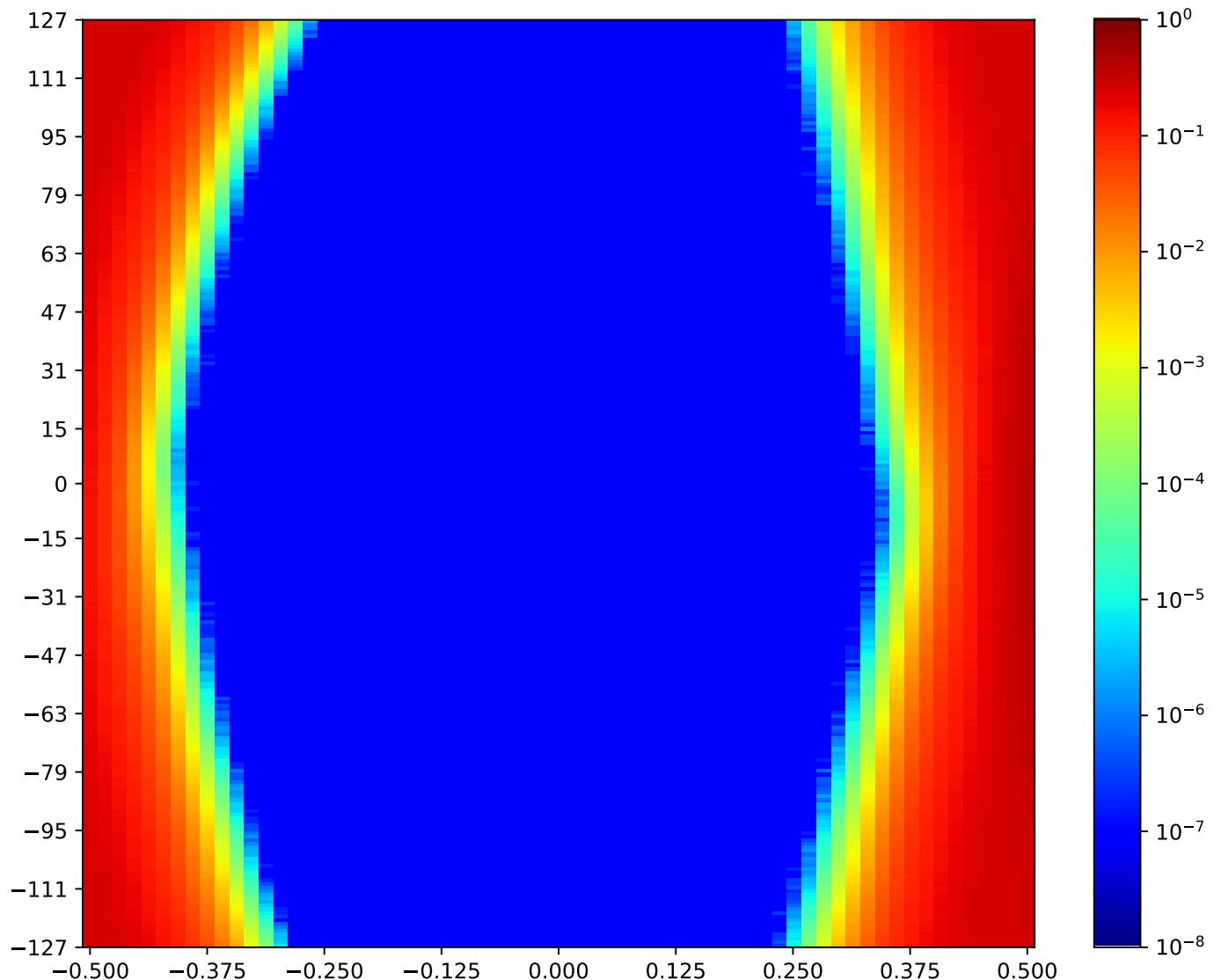


Figure 1.273: MSP\_C\_FPGA-TX3-06-RX4-06-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.8 MSP\_C\_FPGA-TX3-07-RX4-07-MSP\_A\_FPGA

Table 1.253: MSP\_C\_FPGA-TX3-07-RX4-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:47:02		2018-Jan-24 17:47:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10057	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

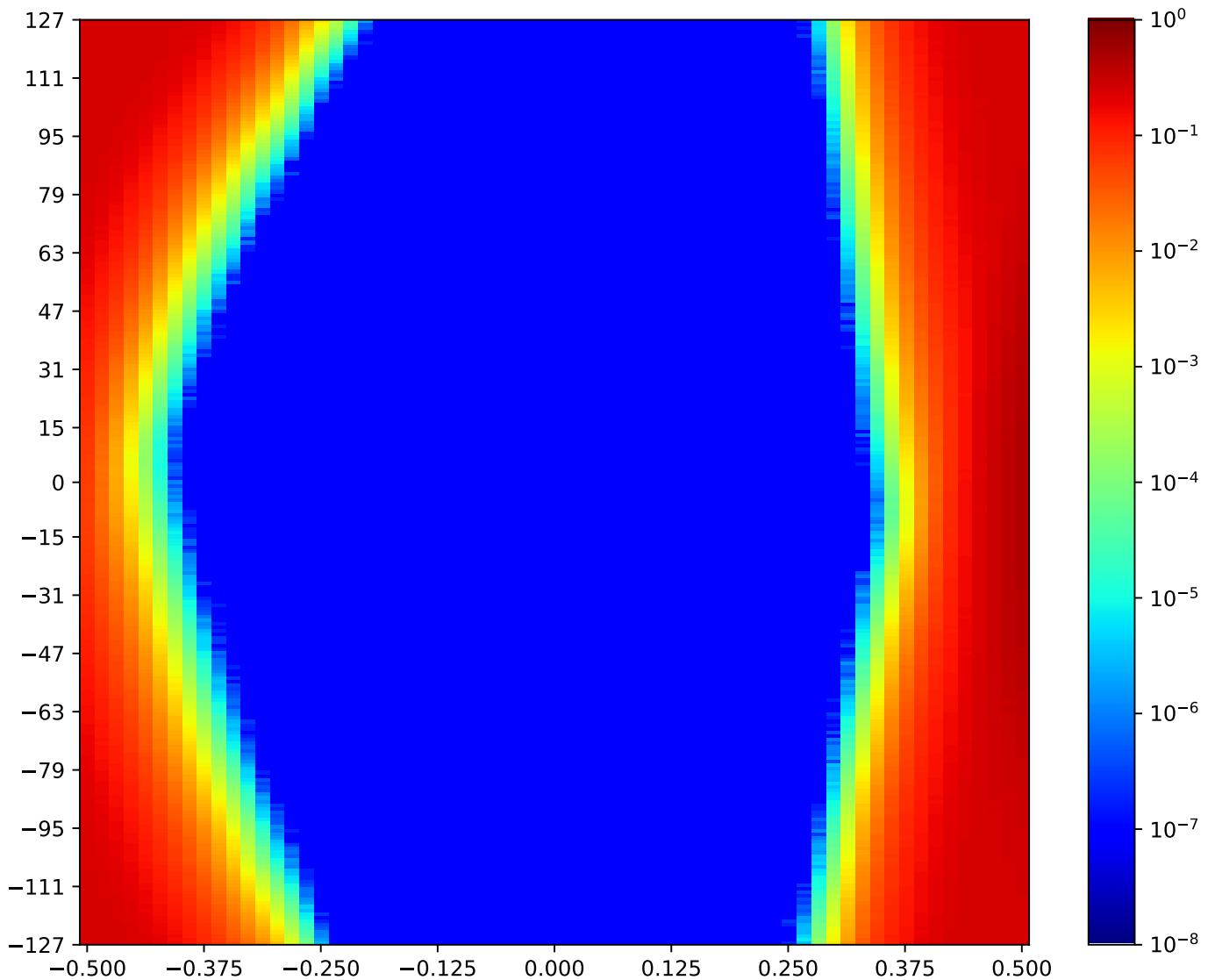


Figure 1.274: MSP\_C\_FPGA-TX3-07-RX4-07-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.9 MSP\_C\_FPGA-TX3-08-RX4-08-MSP\_A\_FPGA

Table 1.254: MSP\_C\_FPGA-TX3-08-RX4-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:51:49		2018-Jan-24 17:52:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9879	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

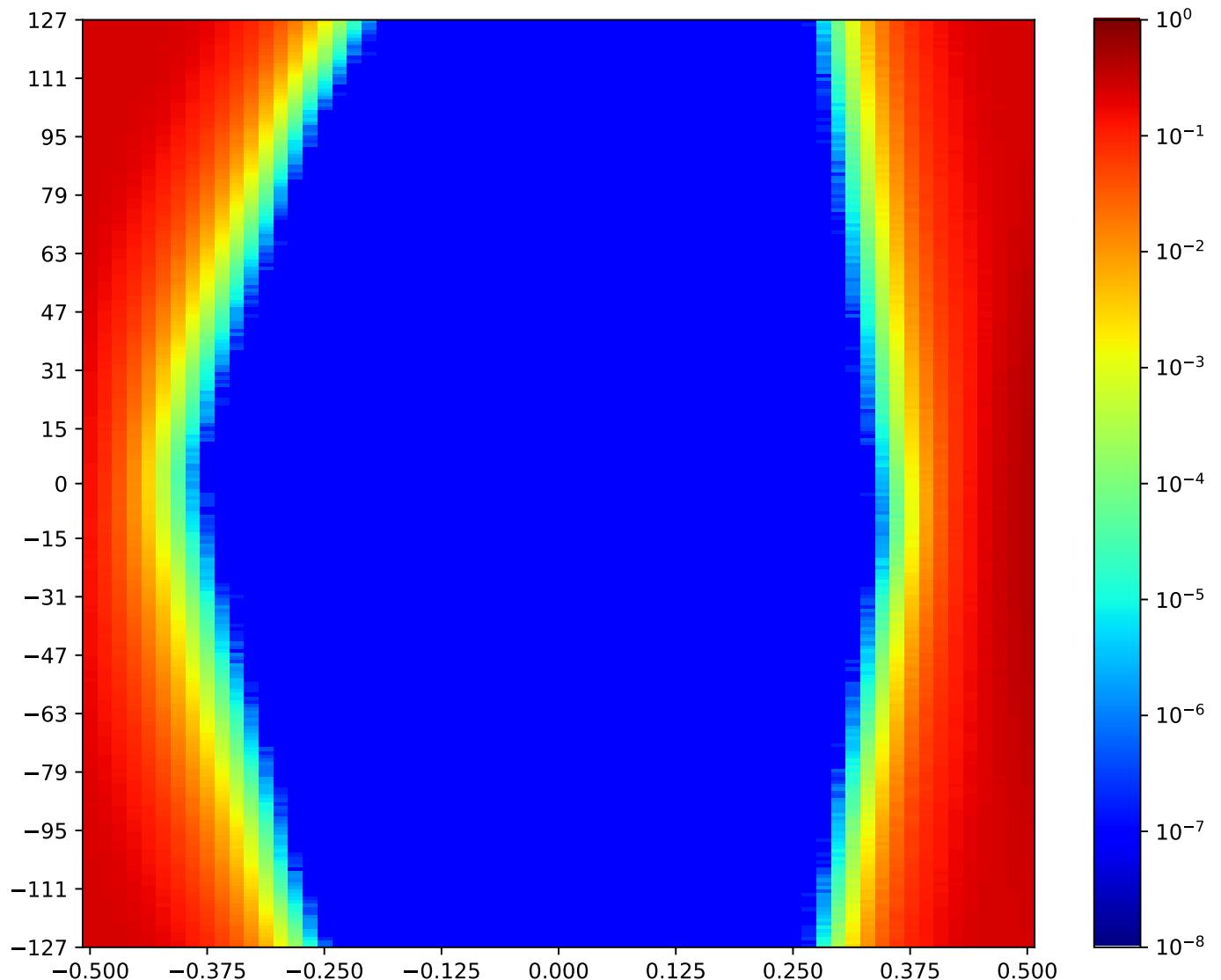


Figure 1.275: MSP\_C\_FPGA-TX3-08-RX4-08-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.10 MSP\_C\_FPGA-TX3-09-RX4-09-MSP\_A\_FPGA

Table 1.255: MSP\_C\_FPGA-TX3-09-RX4-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:48:13		2018-Jan-24 17:48:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9384	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

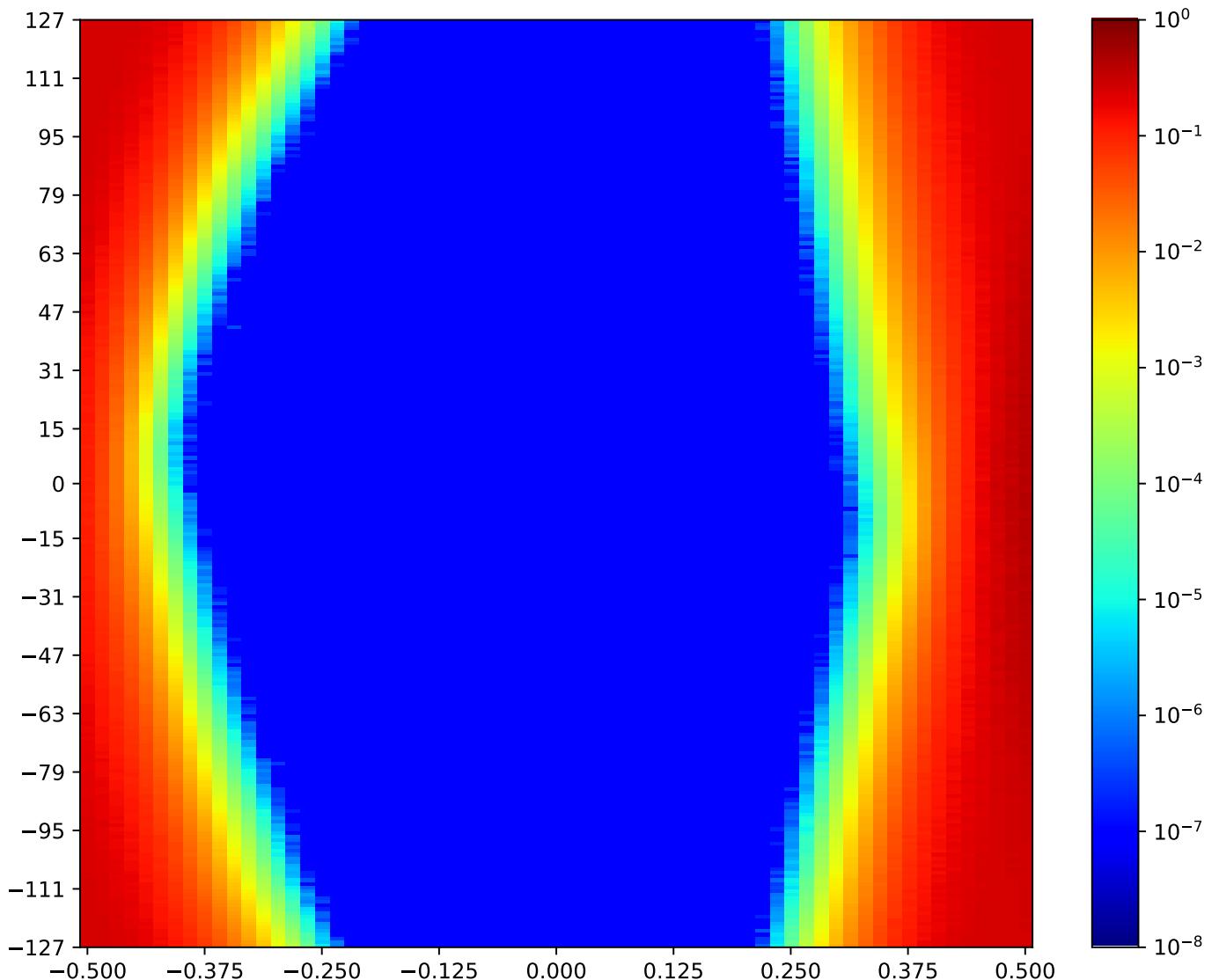


Figure 1.276: MSP\_C\_FPGA-TX3-09-RX4-09-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.11 MSP\_C\_FPGA-TX3-10-RX4-10-MSP\_A\_FPGA

Table 1.256: MSP\_C\_FPGA-TX3-10-RX4-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:50:37		2018-Jan-24 17:51:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10617	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

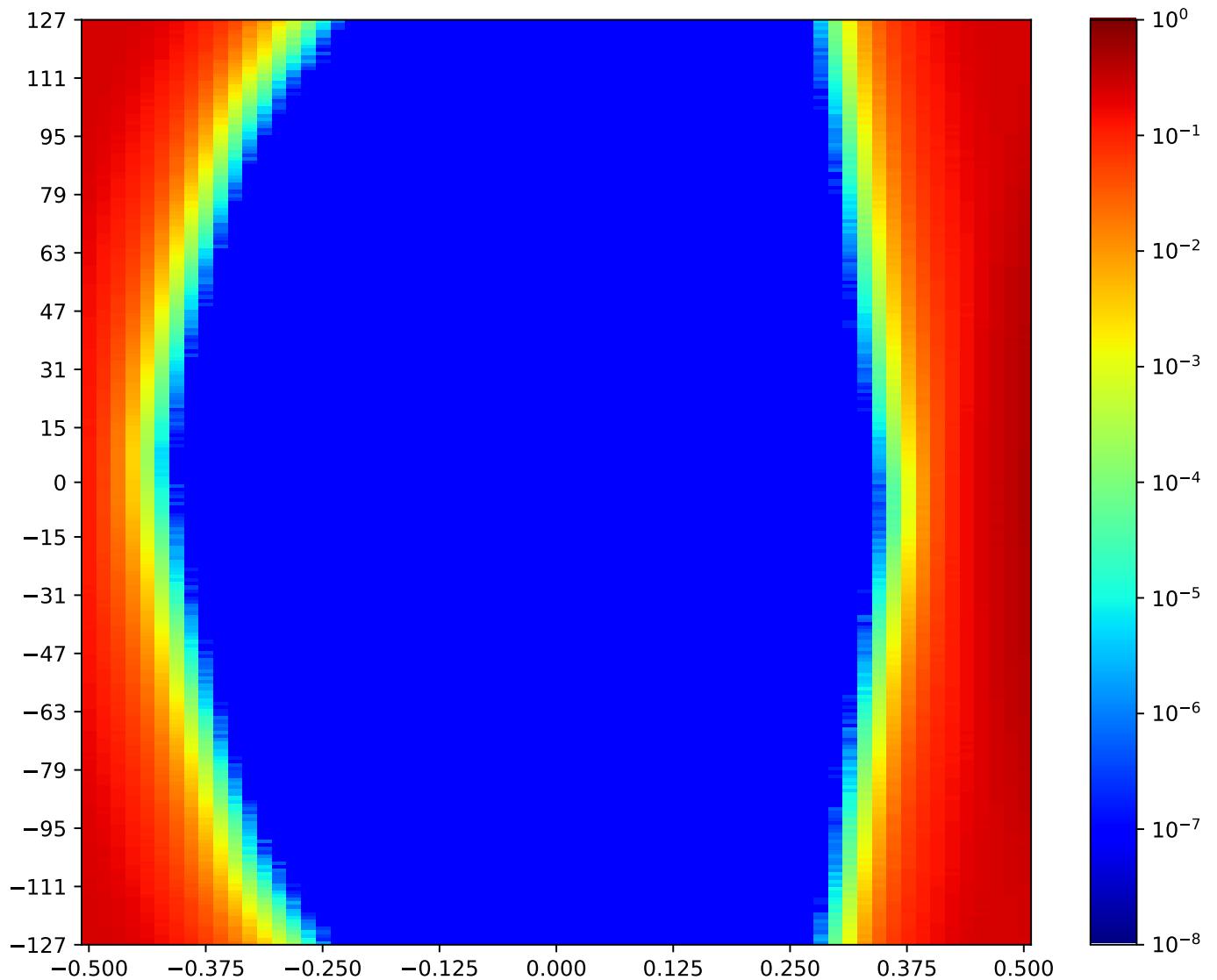


Figure 1.277: MSP\_C\_FPGA-TX3-10-RX4-10-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.21.12 MSP\_C\_FPGA-TX3-11-RX4-11-MSP\_A\_FPGA

Table 1.257: MSP\_C\_FPGA-TX3-11-RX4-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:50:01		2018-Jan-24 17:50:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9338	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

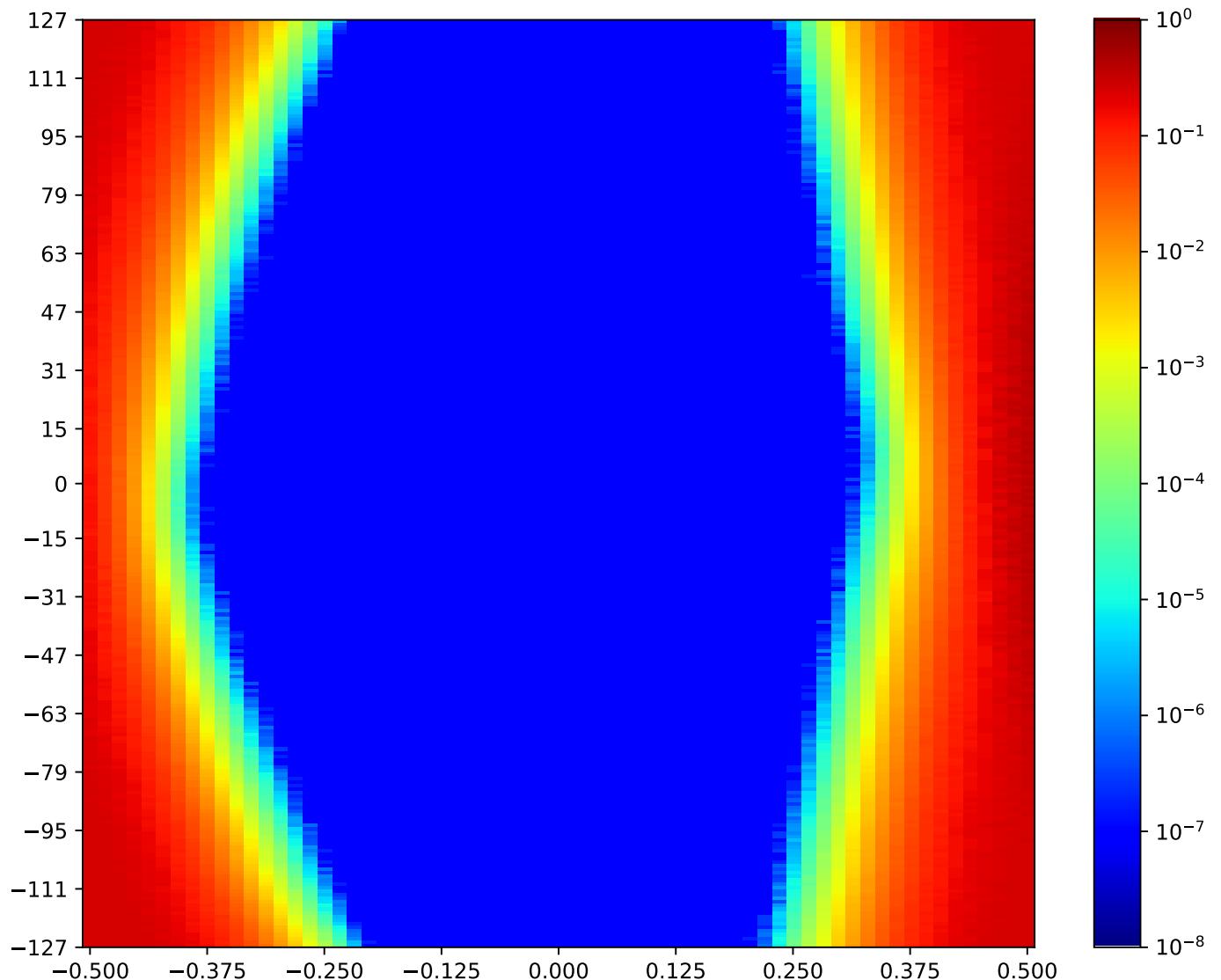


Figure 1.278: MSP\_C\_FPGA-TX3-11-RX4-11-MSP\_A\_FPGA

Call back to summary Figure 1.266. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.22 MSP\_C TX4 MSP\_A RX3 Minipod Loopback

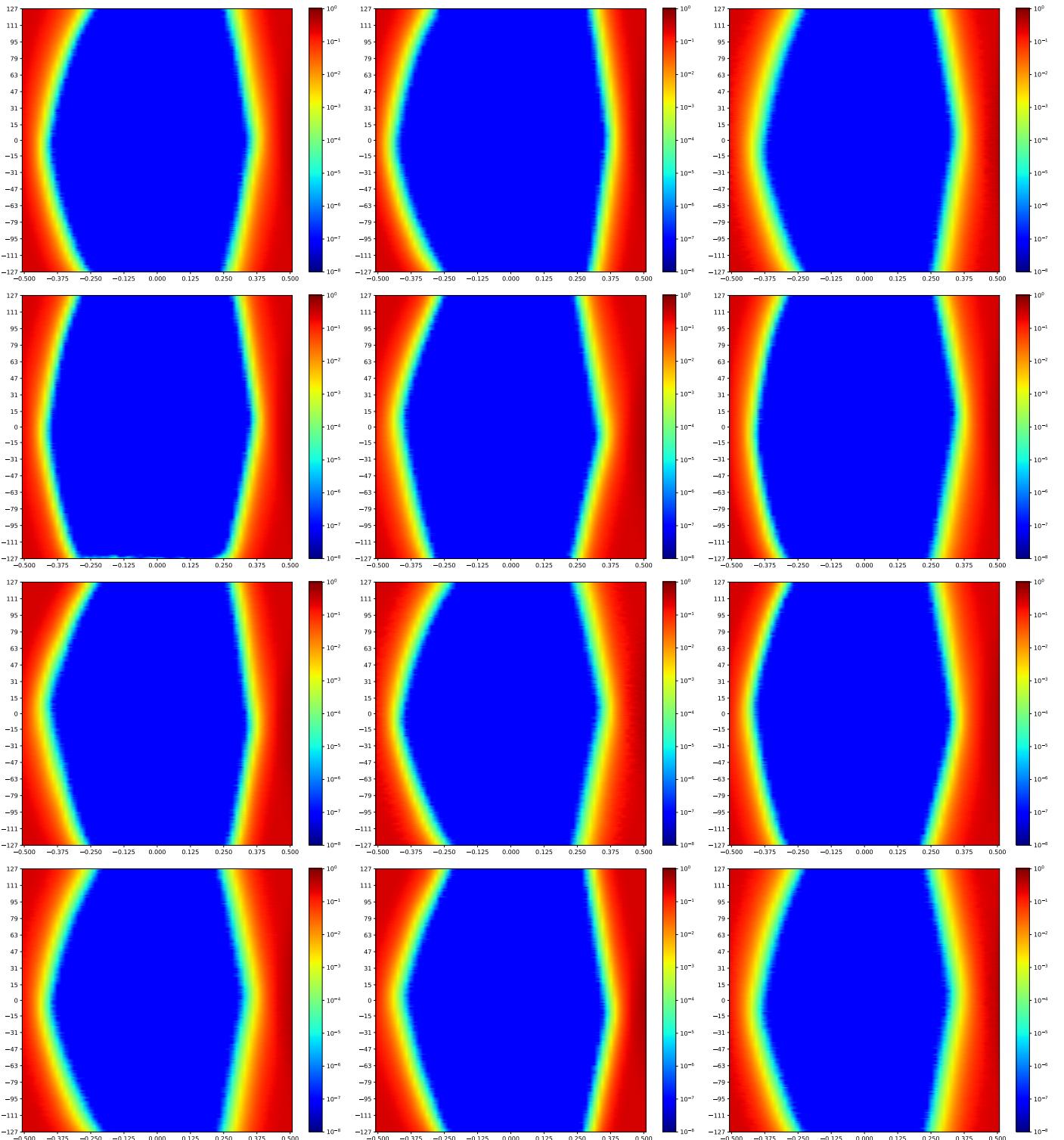


Figure 1.279: MSP\_C TX4 MSP\_A RX3 Minipod Loopback

A cross-reference to Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.  
Next summary Figure 2.1.

### 1.22.1 MSP\_C\_FPGA-TX4-00-RX3-00-MSP\_A\_FPGA

Table 1.258: MSP\_C\_FPGA-TX4-00-RX3-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:54:49		2018-Jan-24 17:55:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10077	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

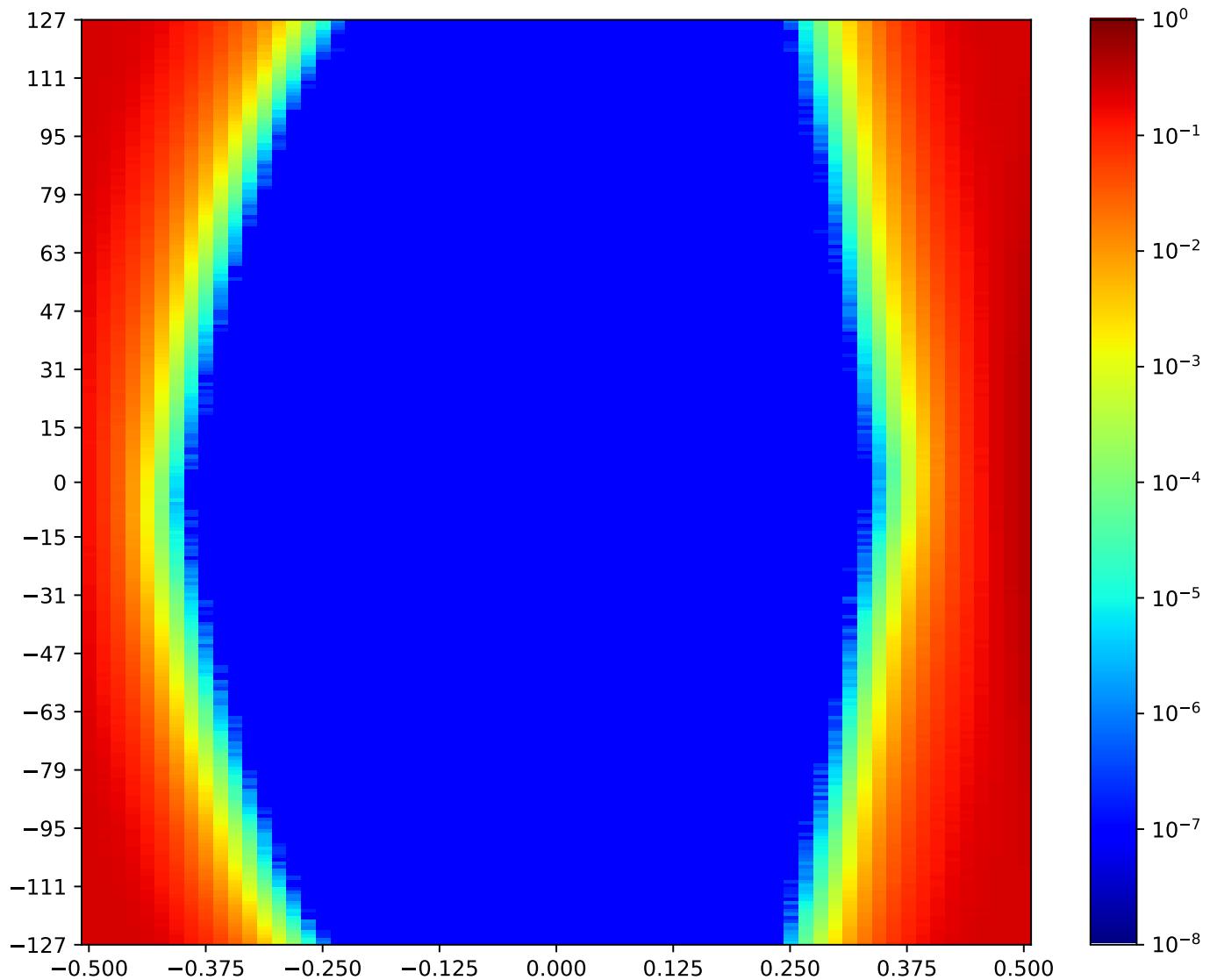


Figure 1.280: MSP\_C\_FPGA-TX4-00-RX3-00-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.22.2 MSP\_C\_FPGA-TX4-01-RX3-01-MSP\_A\_FPGA

Table 1.259: MSP\_C\_FPGA-TX4-01-RX3-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:53:37		2018-Jan-24 17:54:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10755	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

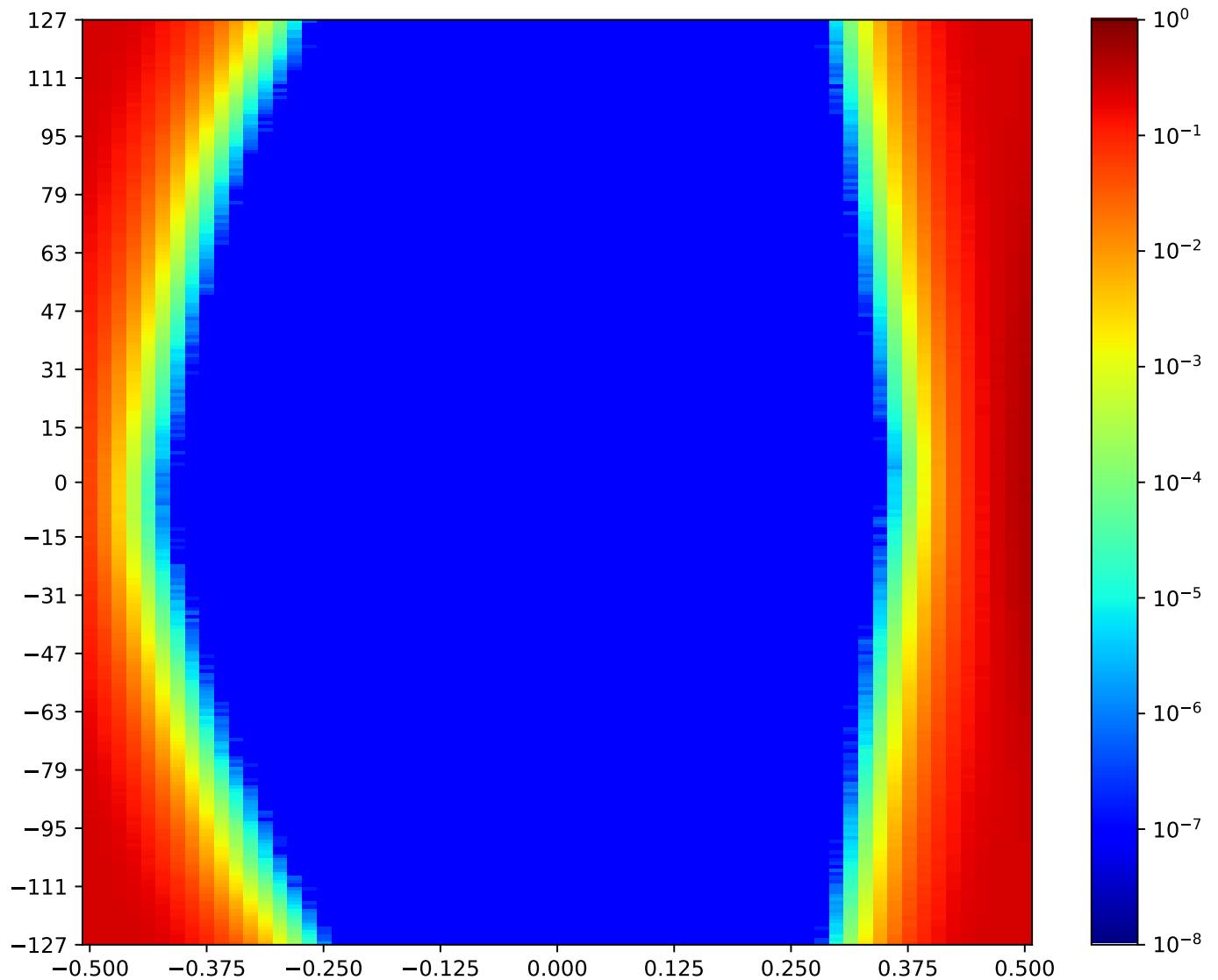


Figure 1.281: MSP\_C\_FPGA-TX4-01-RX3-01-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.22.3 MSP\_C\_FPGA-TX4-02-RX3-02-MSP\_A\_FPGA

Table 1.260: MSP\_C\_FPGA-TX4-02-RX3-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:56:39		2018-Jan-24 17:57:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9436	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

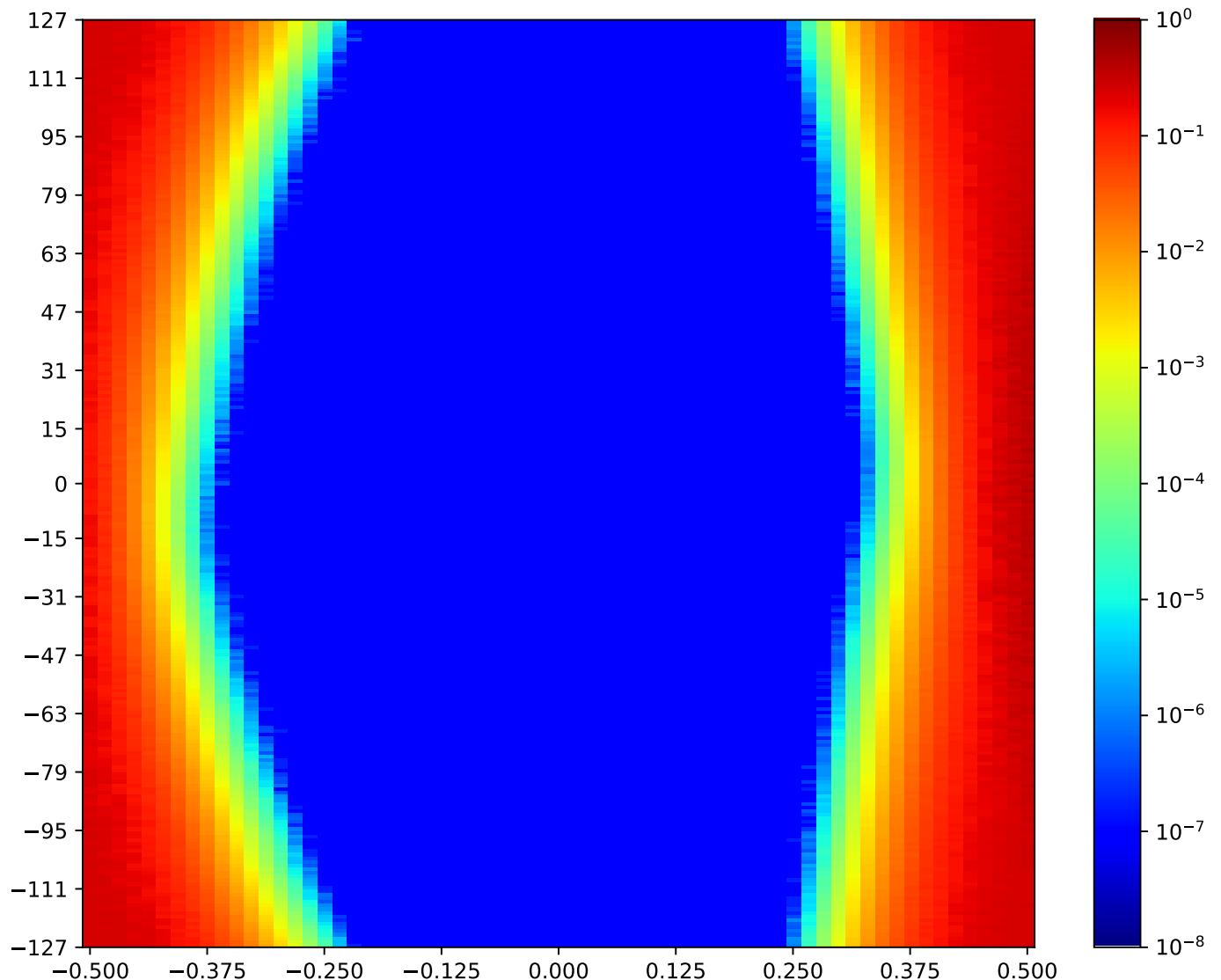


Figure 1.282: MSP\_C\_FPGA-TX4-02-RX3-02-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

#### 1.22.4 MSP\_C\_FPGA-TX4-03-RX3-03-MSP\_A\_FPGA

Table 1.261: MSP\_C\_FPGA-TX4-03-RX3-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:53:00		2018-Jan-24 17:53:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10510	47	72.31%	253	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

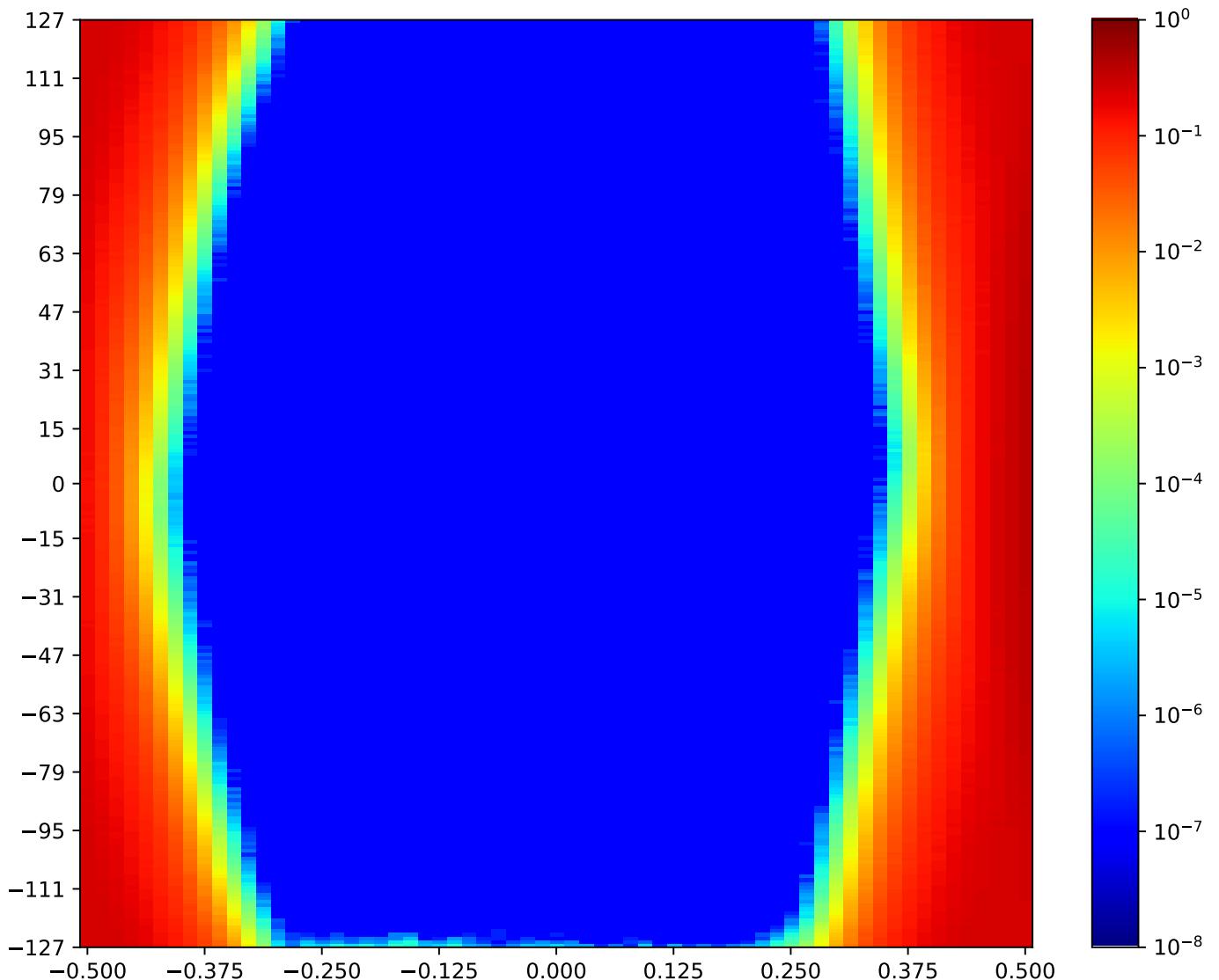


Figure 1.283: MSP\_C\_FPGA-TX4-03-RX3-03-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.22.5 MSP\_C\_FPGA-TX4-04-RX3-04-MSP\_A\_FPGA

Table 1.262: MSP\_C\_FPGA-TX4-04-RX3-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:58:28		2018-Jan-24 17:59:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9723	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

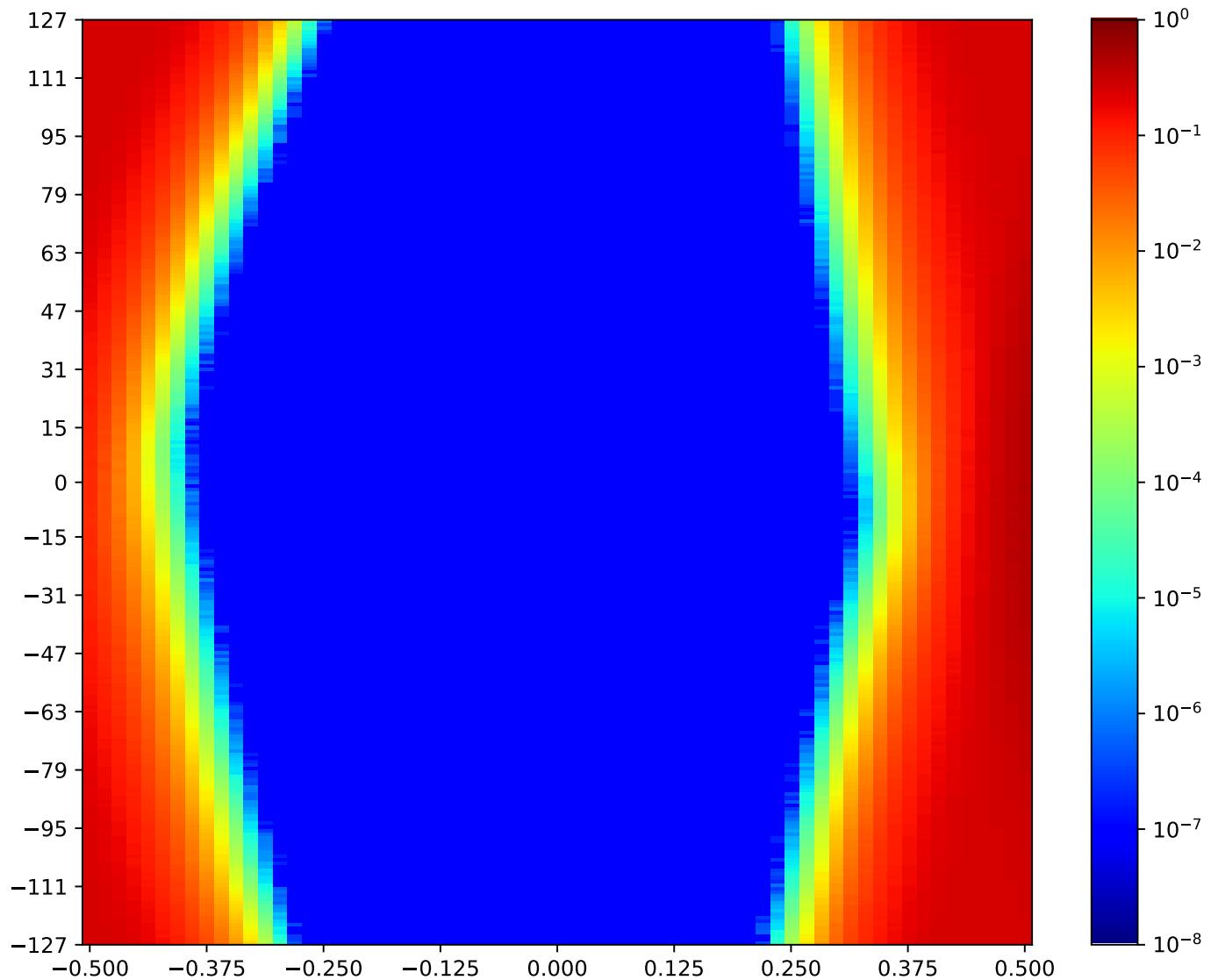


Figure 1.284: MSP\_C\_FPGA-TX4-04-RX3-04-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.22.6 MSP\_C\_FPGA-TX4-05-RX3-05-MSP\_A\_FPGA

Table 1.263: MSP\_C\_FPGA-TX4-05-RX3-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:54:13		2018-Jan-24 17:54:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10308	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

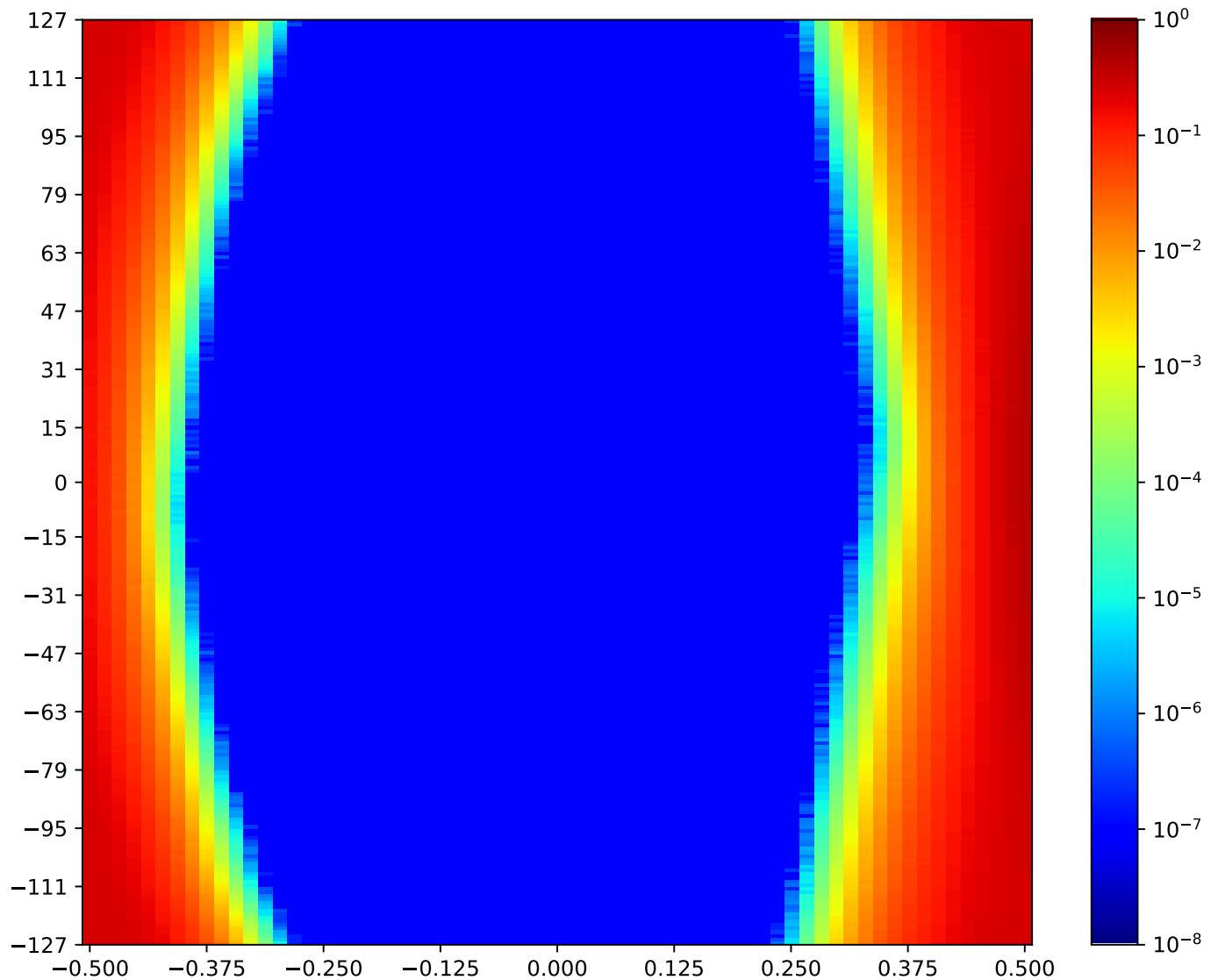


Figure 1.285: MSP\_C\_FPGA-TX4-05-RX3-05-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.22.7 MSP\_C\_FPGA-TX4-06-RX3-06-MSP\_A\_FPGA

Table 1.264: MSP\_C\_FPGA-TX4-06-RX3-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:59:37		2018-Jan-24 18:00:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9958	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

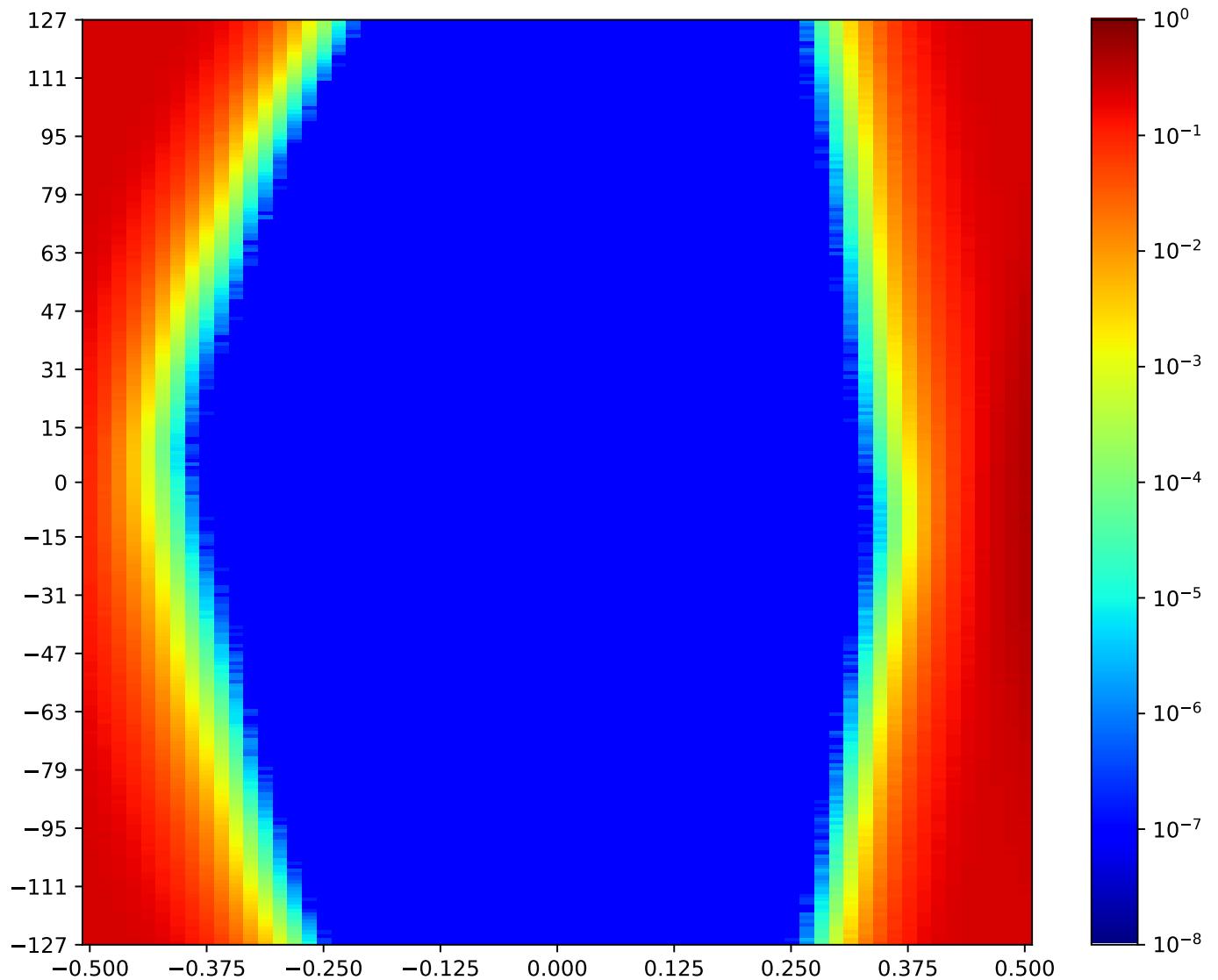


Figure 1.286: MSP\_C\_FPGA-TX4-06-RX3-06-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## 1.22.8 MSP\_C\_FPGA-TX4-07-RX3-07-MSP\_A\_FPGA

Table 1.265: MSP\_C\_FPGA-TX4-07-RX3-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:55:26		2018-Jan-24 17:56:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9504	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

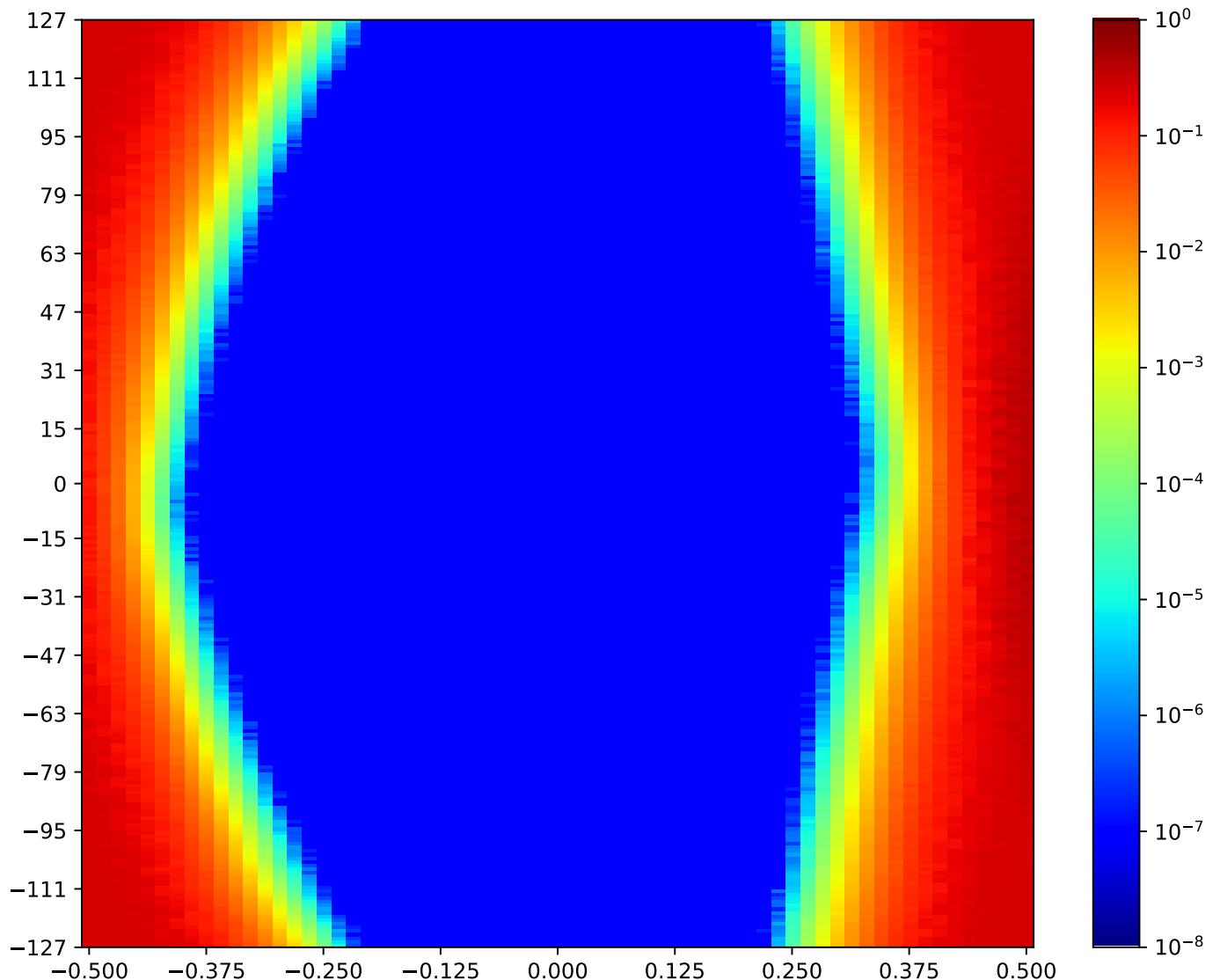


Figure 1.287: MSP\_C\_FPGA-TX4-07-RX3-07-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.22.9 MSP\_C\_FPGA-TX4-08-RX3-08-MSP\_A\_FPGA

Table 1.266: MSP\_C\_FPGA-TX4-08-RX3-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:59:02		2018-Jan-24 17:59:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9976	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

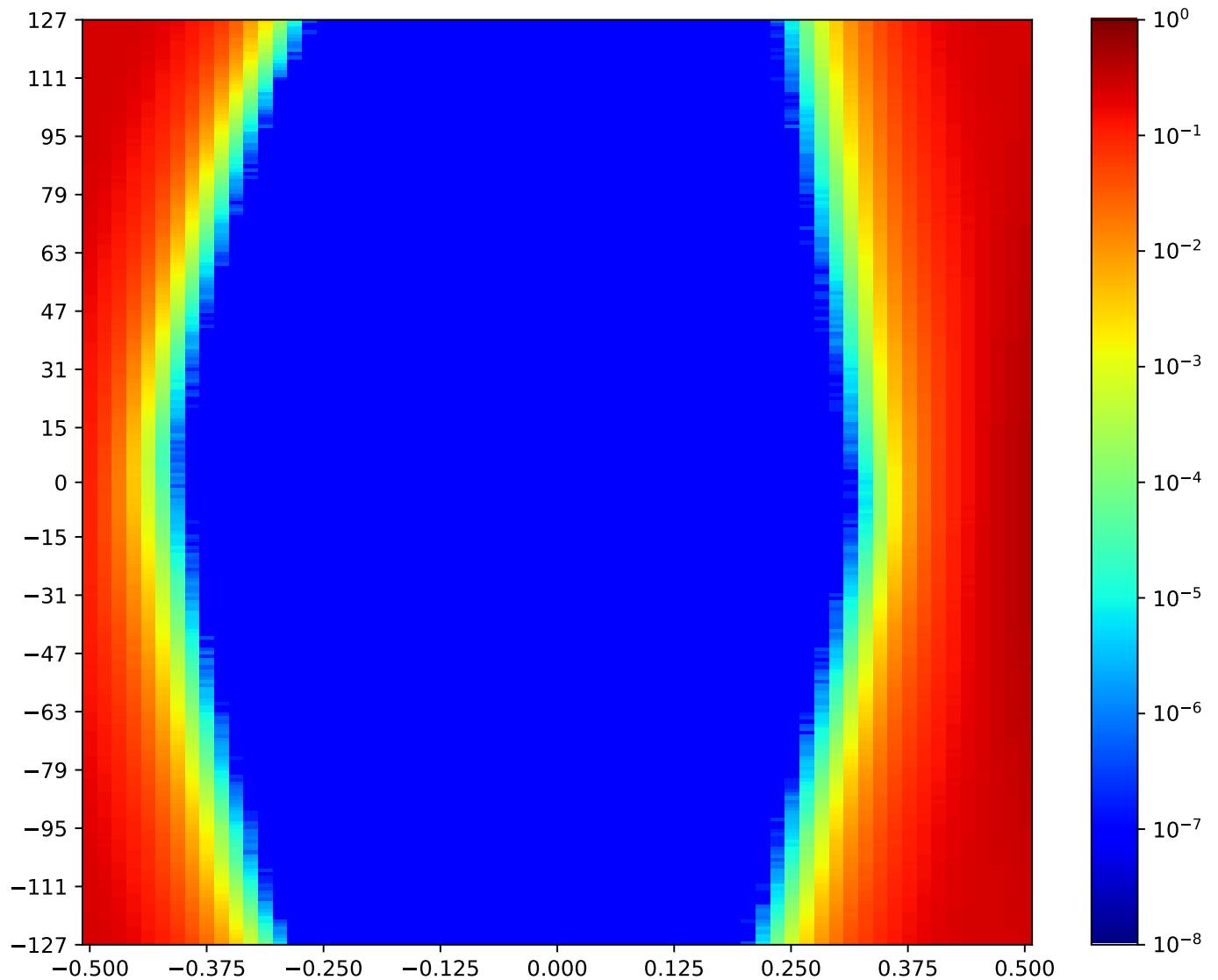


Figure 1.288: MSP\_C\_FPGA-TX4-08-RX3-08-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.22.10 MSP\_C\_FPGA-TX4-09-RX3-09-MSP\_A\_FPGA

Table 1.267: MSP\_C\_FPGA-TX4-09-RX3-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:56:03		2018-Jan-24 17:56:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9280	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

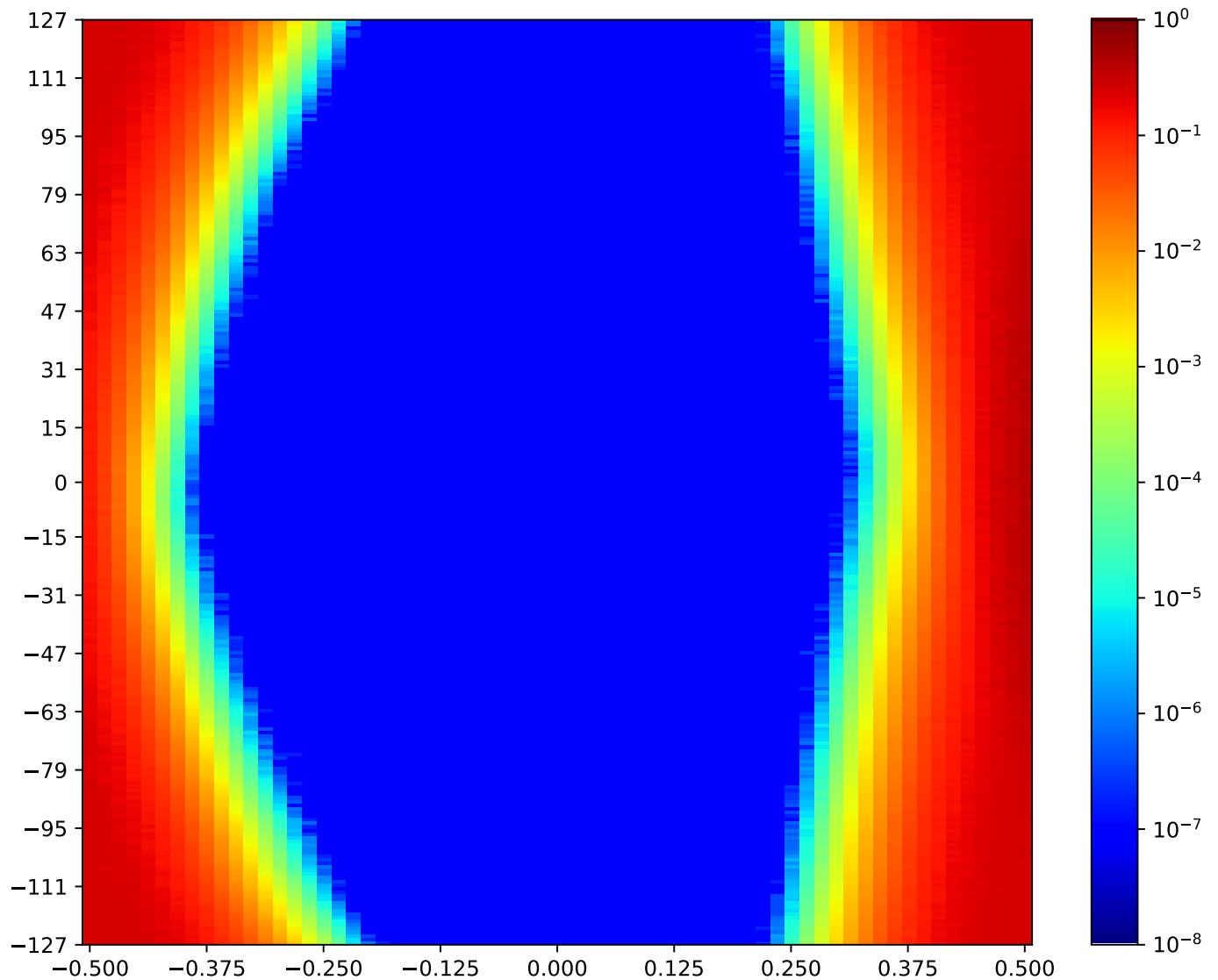


Figure 1.289: MSP\_C\_FPGA-TX4-09-RX3-09-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.22.11 MSP\_C\_FPGA-TX4-10-RX3-10-MSP\_A\_FPGA

Table 1.268: MSP\_C\_FPGA-TX4-10-RX3-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:57:51		2018-Jan-24 17:58:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9915	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

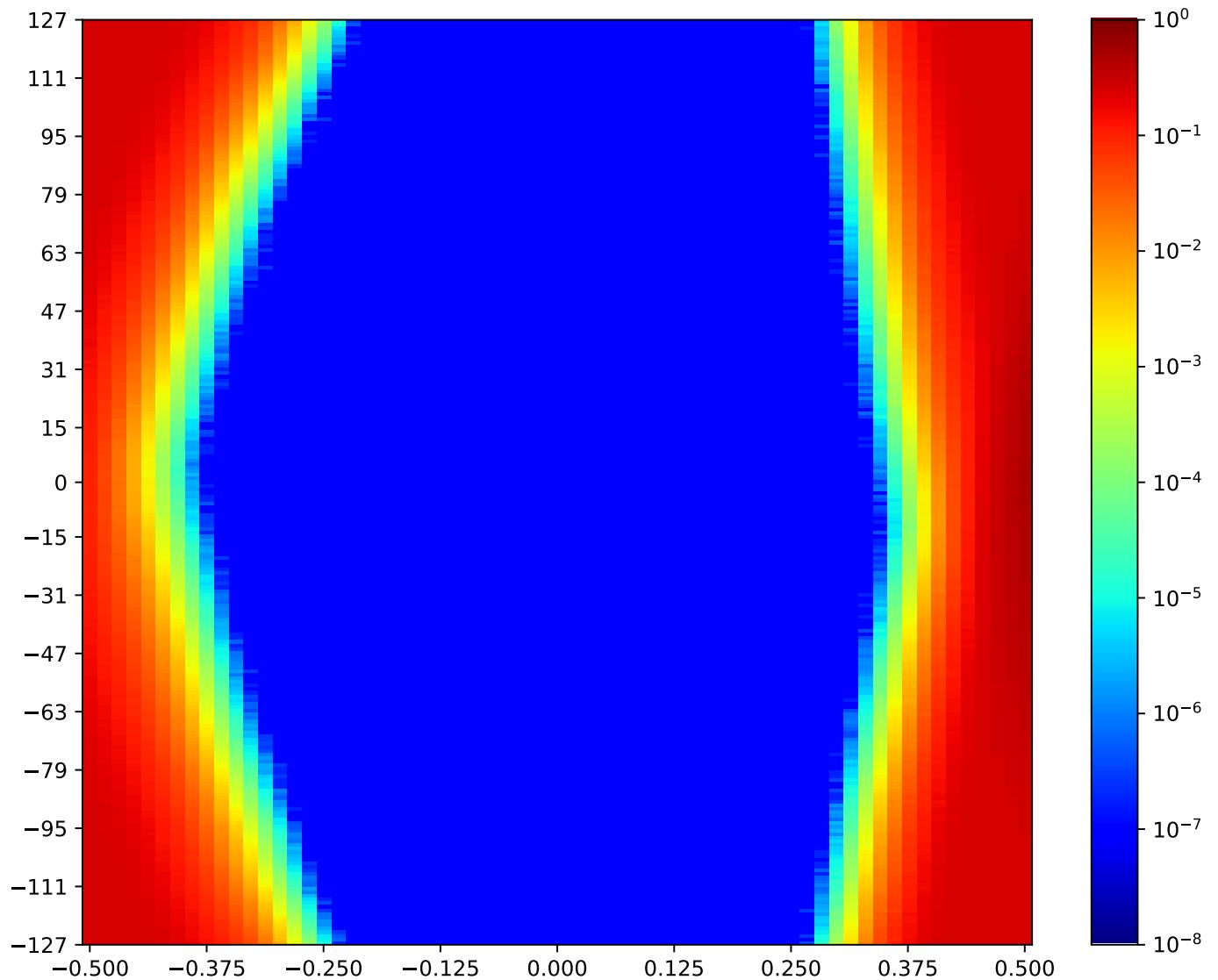


Figure 1.290: MSP\_C\_FPGA-TX4-10-RX3-10-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

### 1.22.12 MSP\_C\_FPGA-TX4-11-RX3-11-MSP\_A\_FPGA

Table 1.269: MSP\_C\_FPGA-TX4-11-RX3-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:57:15		2018-Jan-24 17:57:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9166	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

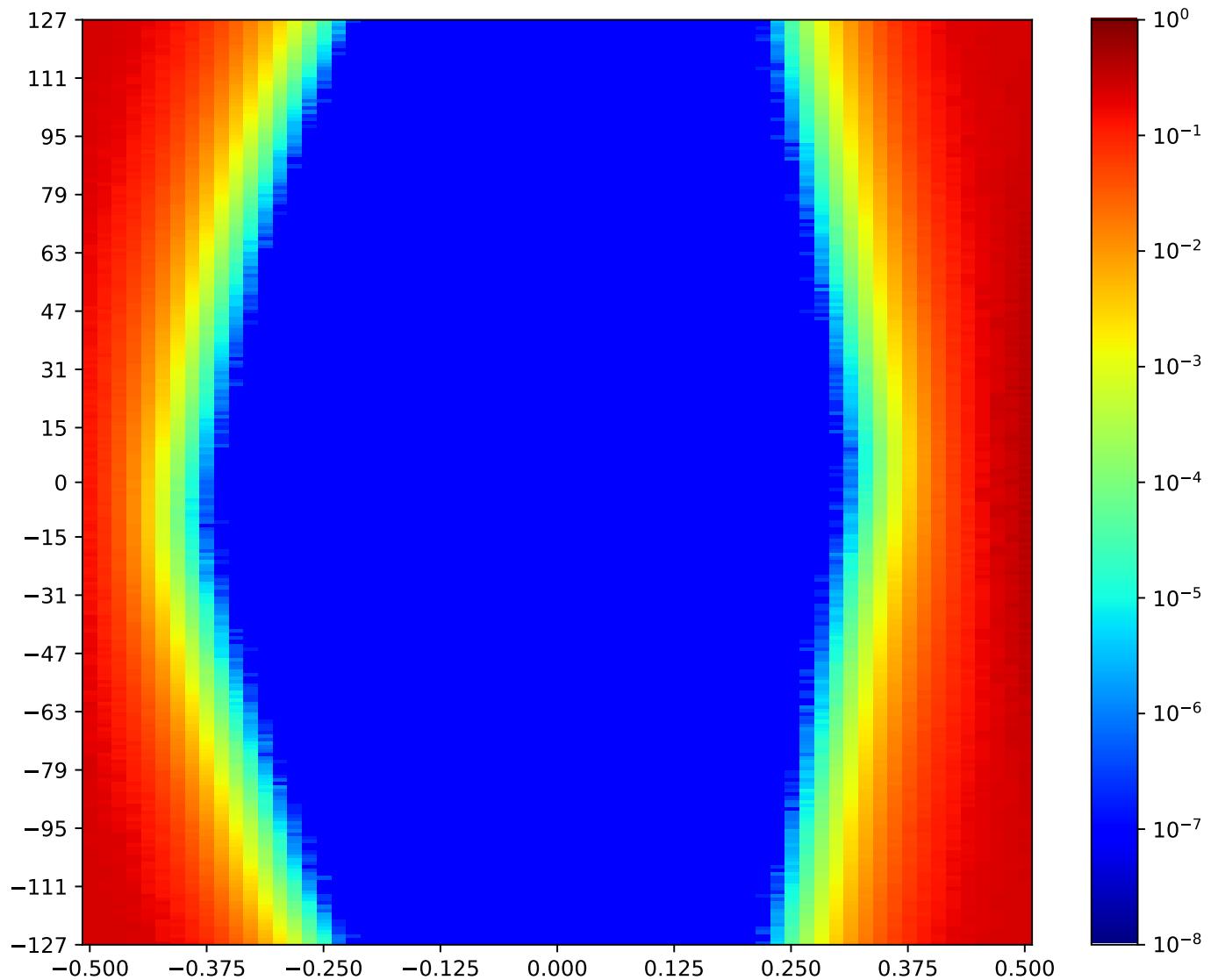


Figure 1.291: MSP\_C\_FPGA-TX4-11-RX3-11-MSP\_A\_FPGA

Call back to summary Figure 1.279. Sibling eye diagrams: 9.6-optimized, 12.8-optimized.

## **Chapter 2**

### **9.6 Gbps**

## 2.1 MSP\_A TX1 MSP\_C RX16 Minipod Loopback

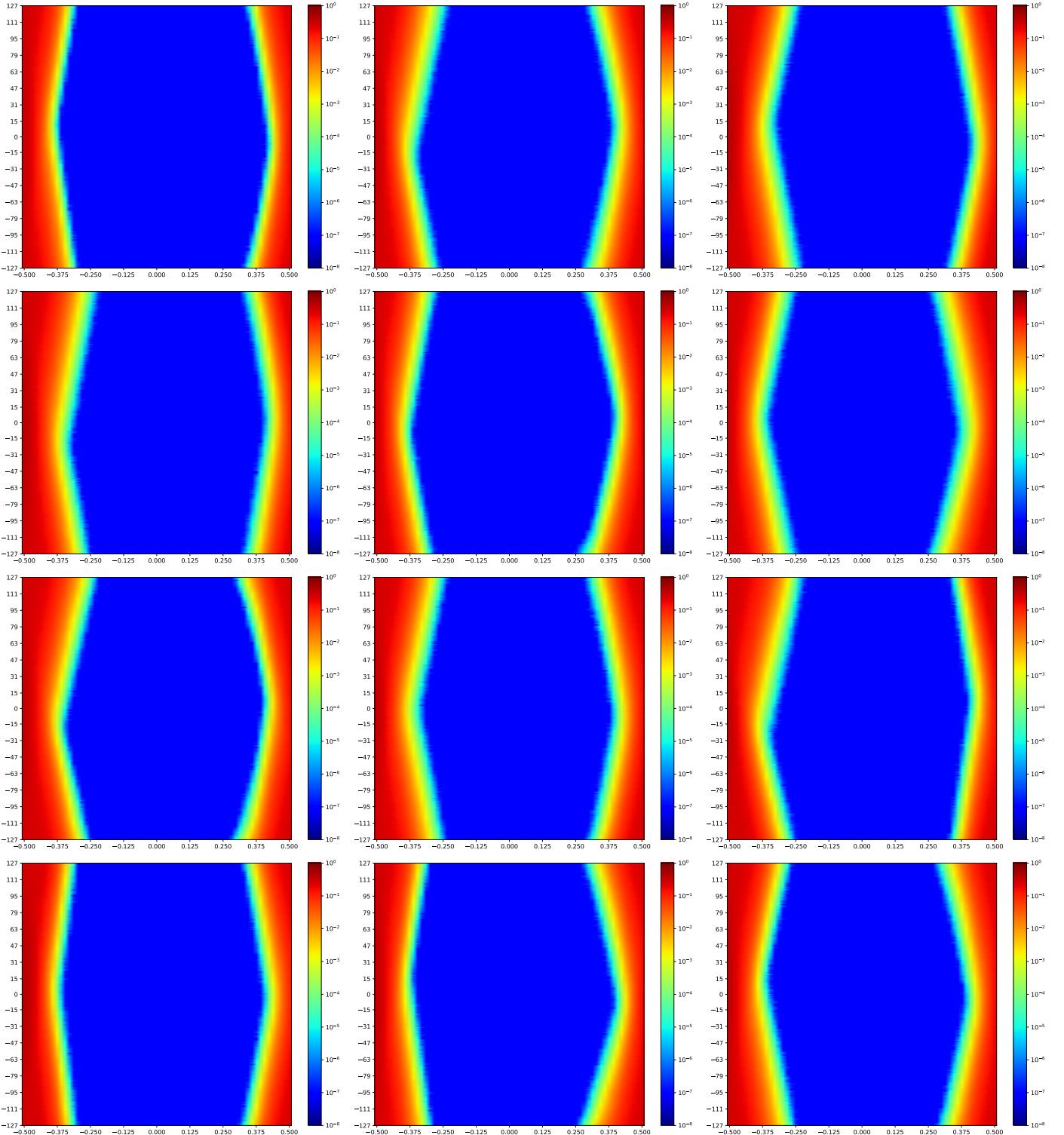


Figure 2.1: MSP\_A TX1 MSP\_C RX16 Minipod Loopback

A cross-reference to Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.14.

### 2.1.1 MSP\_A\_FPGA-TX1-00-RX16-00-MSP\_C\_FPGA

Table 2.1: MSP\_A\_FPGA-TX1-00-RX16-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:11:32		2018-Jan-24 19:12:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11440	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

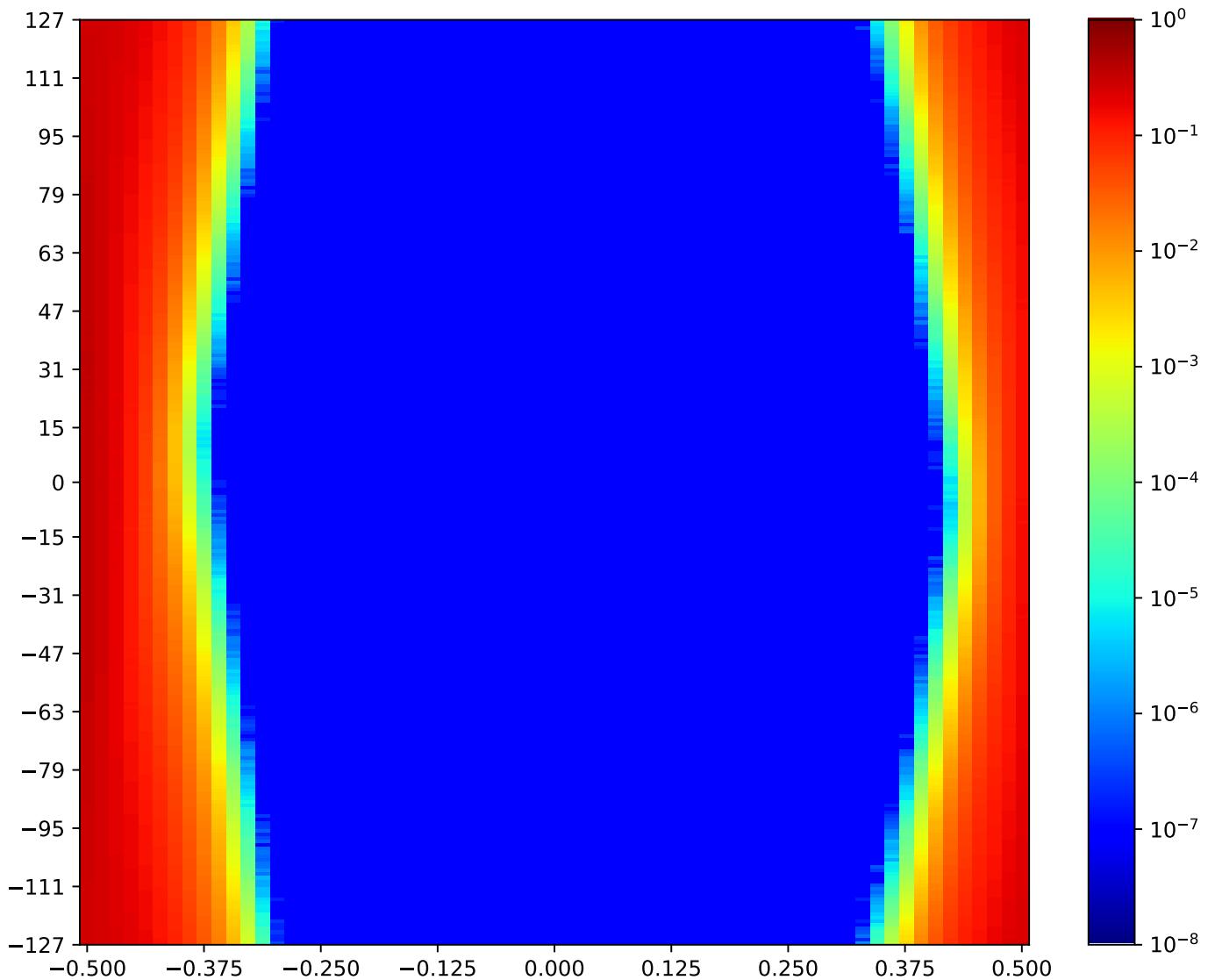


Figure 2.2: MSP\_A\_FPGA-TX1-00-RX16-00-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.1.2 MSP\_A\_FPGA-TX1-01-RX16-01-MSP\_C\_FPGA

Table 2.2: MSP\_A\_FPGA-TX1-01-RX16-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:12:37		2018-Jan-24 19:13:08	
Reset RX	OA	HO		HO (%)	
true	9948	44		67.69%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

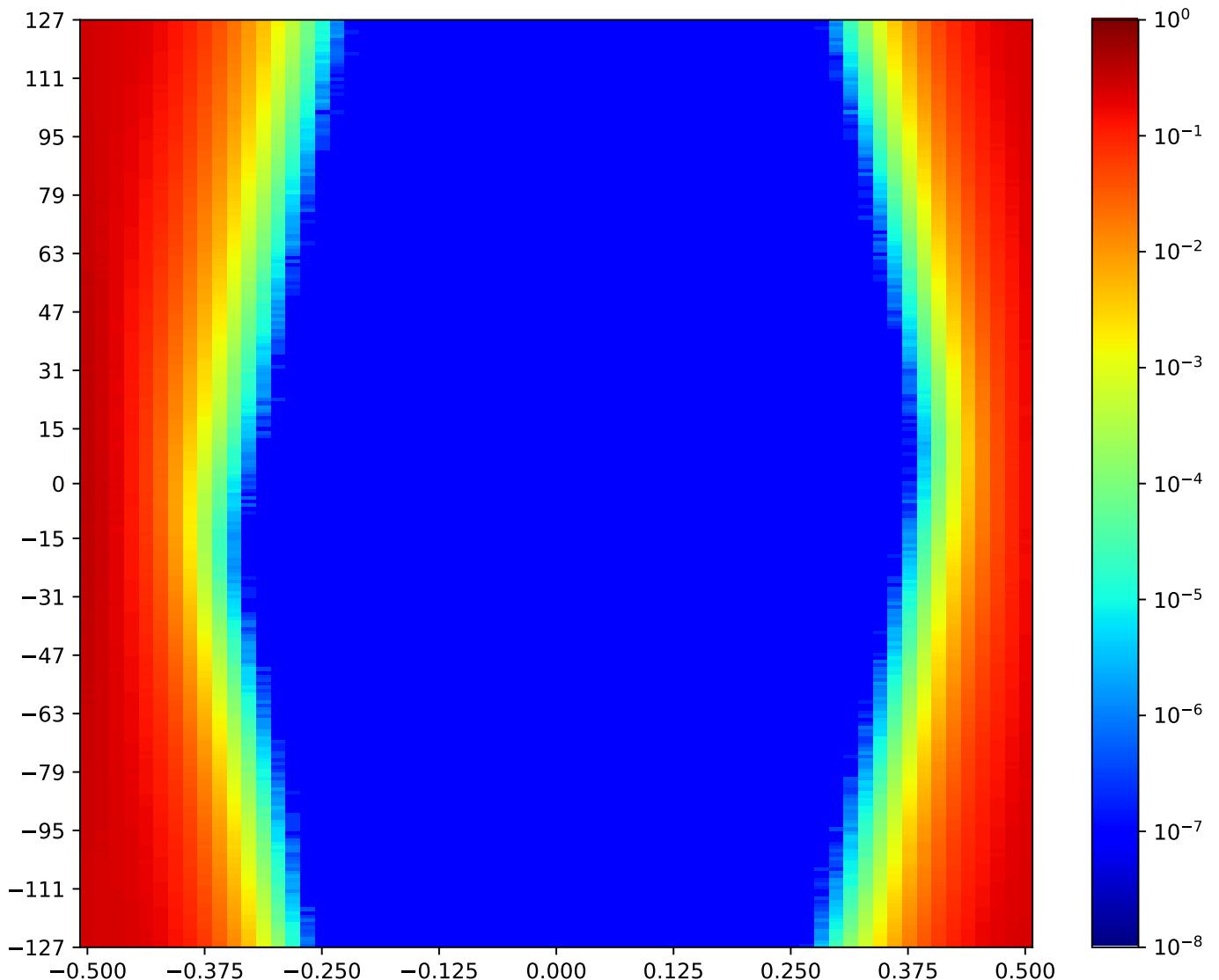


Figure 2.3: MSP\_A\_FPGA-TX1-01-RX16-01-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.1.3 MSP\_A\_FPGA-TX1-02-RX16-02-MSP\_C\_FPGA

Table 2.3: MSP\_A\_FPGA-TX1-02-RX16-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:13:08		2018-Jan-24 19:13:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10076	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

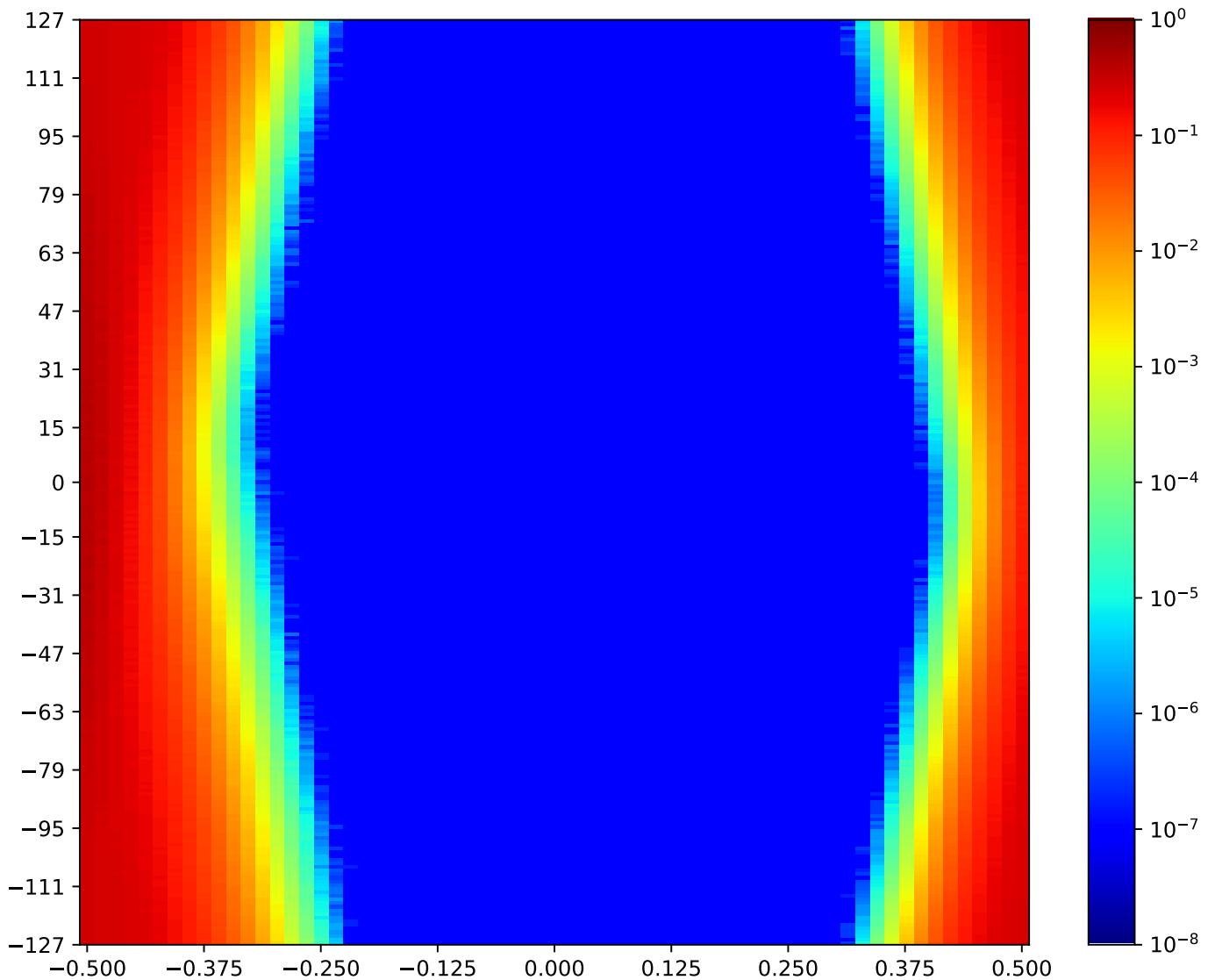


Figure 2.4: MSP\_A\_FPGA-TX1-02-RX16-02-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.1.4 MSP\_A\_FPGA-TX1-03-RX16-03-MSP\_C\_FPGA

Table 2.4: MSP\_A\_FPGA-TX1-03-RX16-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:10:29		2018-Jan-24 19:11:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10196	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

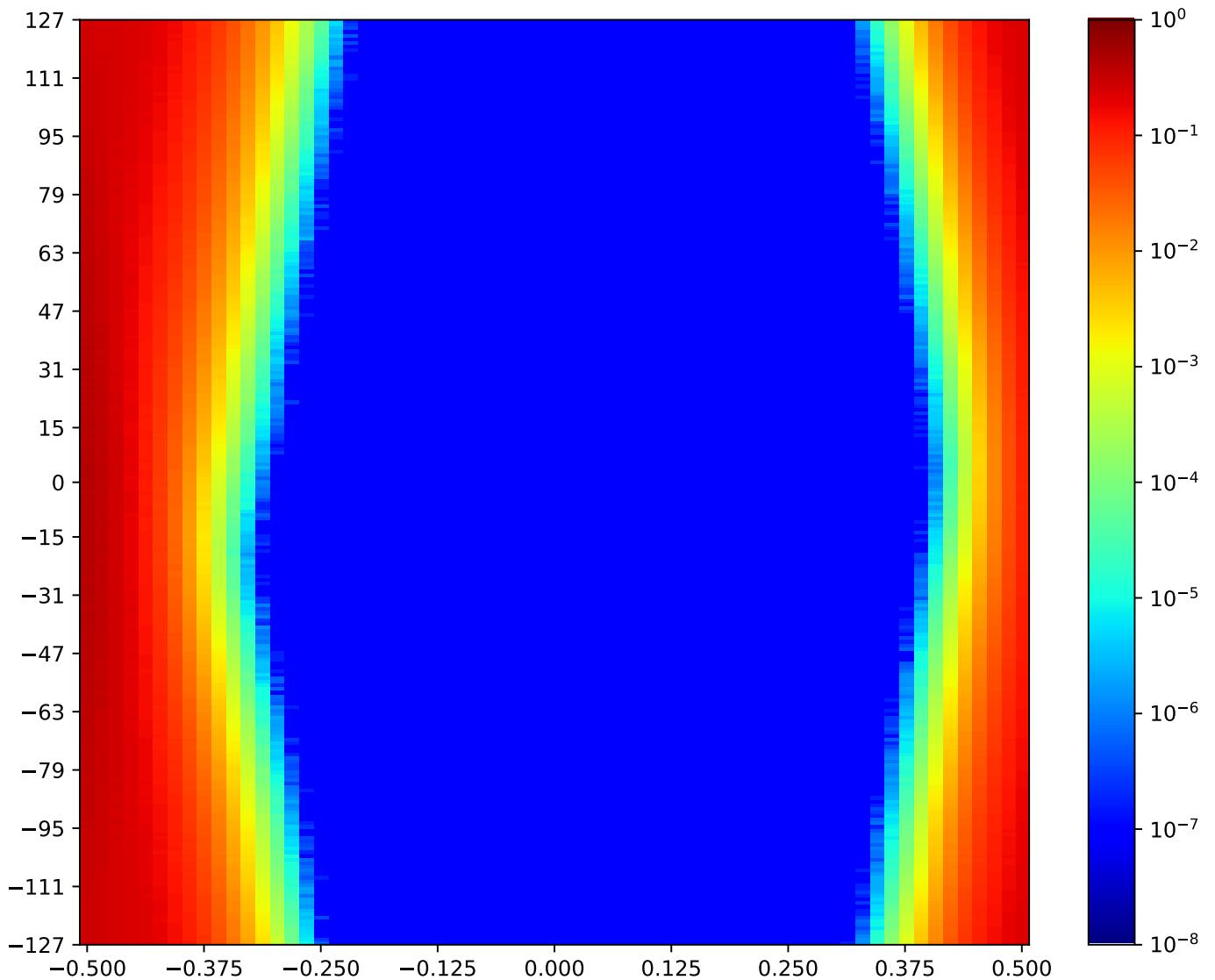


Figure 2.5: MSP\_A\_FPGA-TX1-03-RX16-03-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.1.5 MSP\_A\_FPGA-TX1-04-RX16-04-MSP\_C\_FPGA

Table 2.5: MSP\_A\_FPGA-TX1-04-RX16-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:14:43		2018-Jan-24 19:15:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10484	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

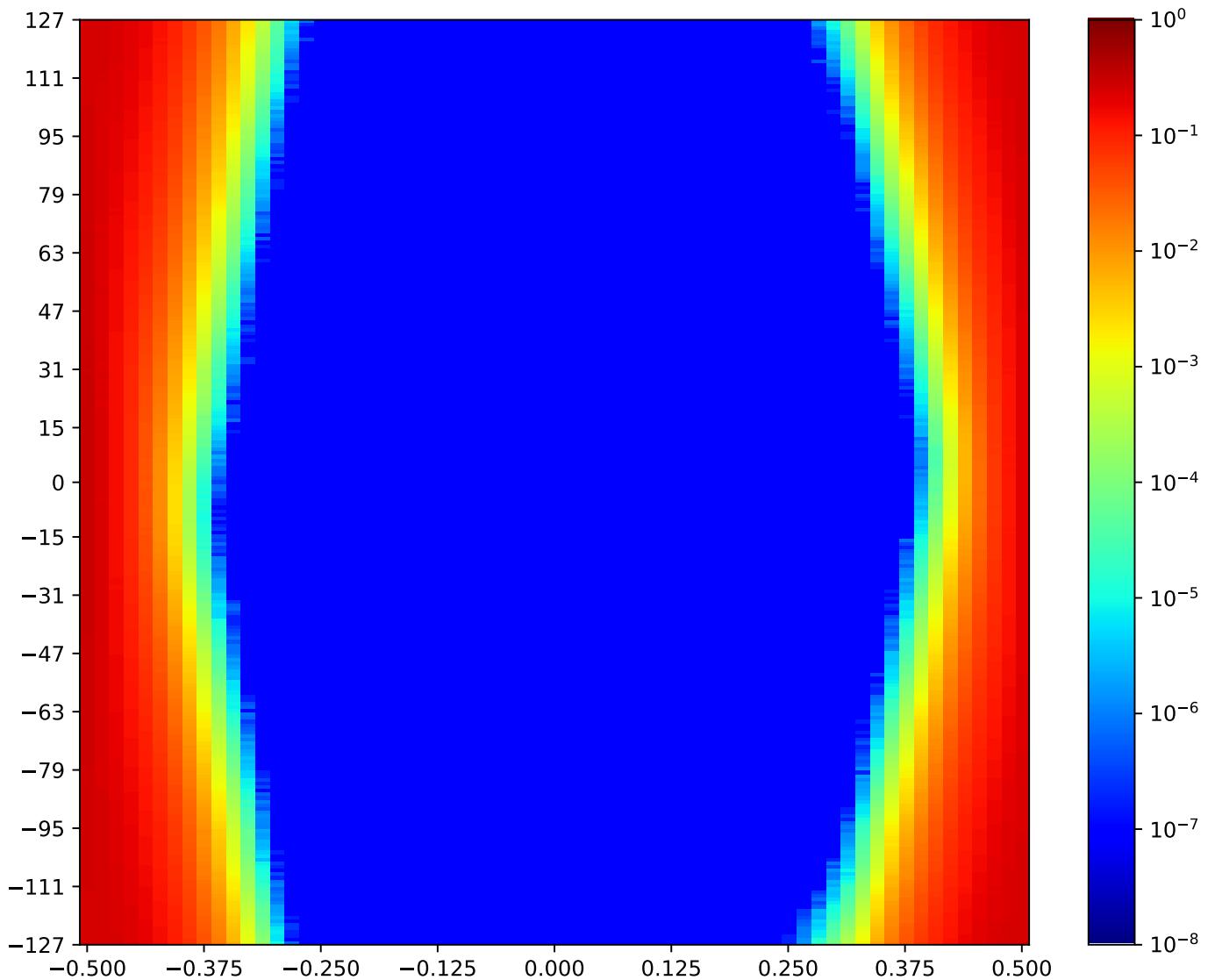


Figure 2.6: MSP\_A\_FPGA-TX1-04-RX16-04-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.1.6 MSP\_A\_FPGA-TX1-05-RX16-05-MSP\_C\_FPGA

Table 2.6: MSP\_A\_FPGA-TX1-05-RX16-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:09:58		2018-Jan-24 19:10:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9514	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

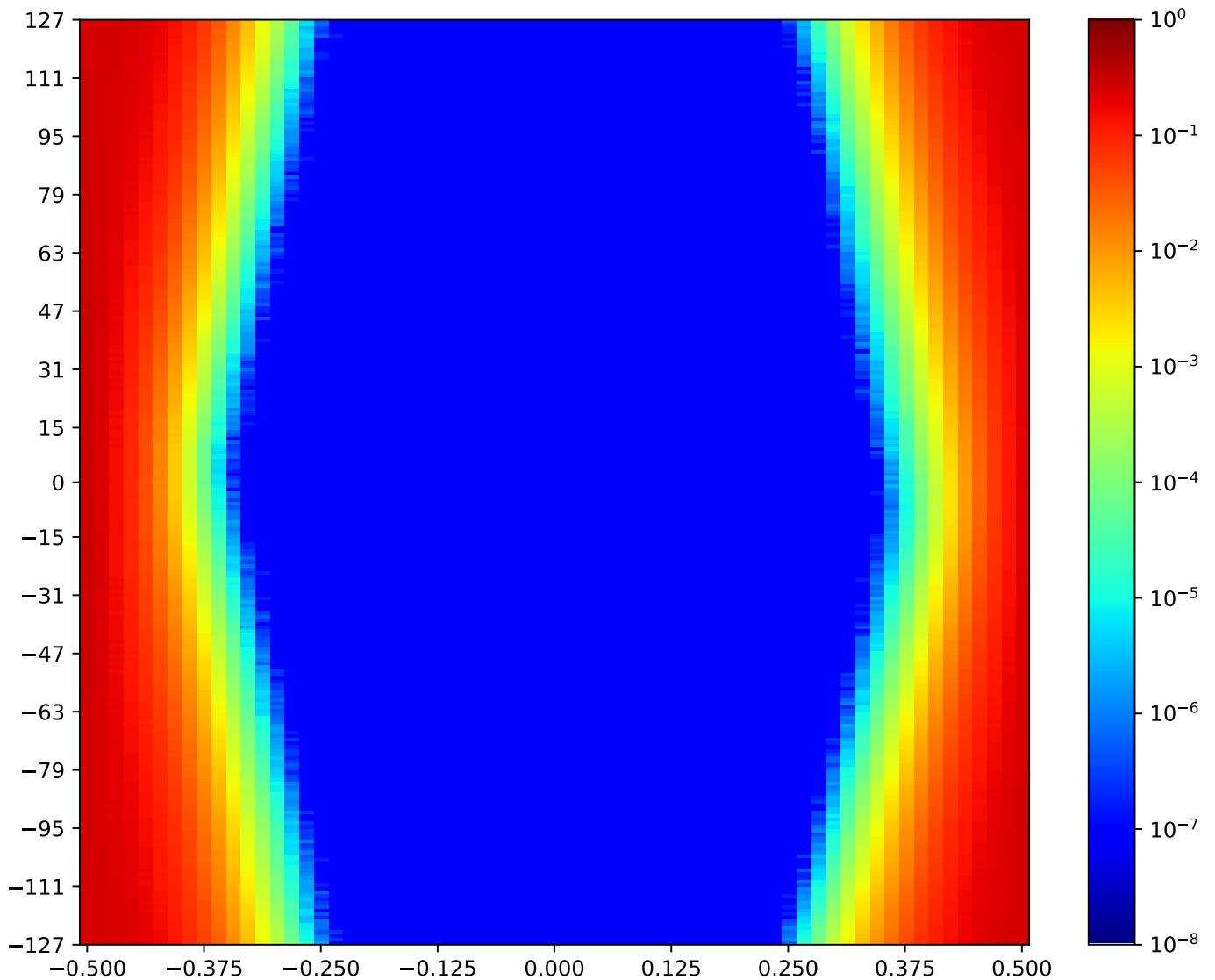


Figure 2.7: MSP\_A\_FPGA-TX1-05-RX16-05-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.1.7 MSP\_A\_FPGA-TX1-06-RX16-06-MSP\_C\_FPGA

Table 2.7: MSP\_A\_FPGA-TX1-06-RX16-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:15:43		2018-Jan-24 19:16:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10241	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

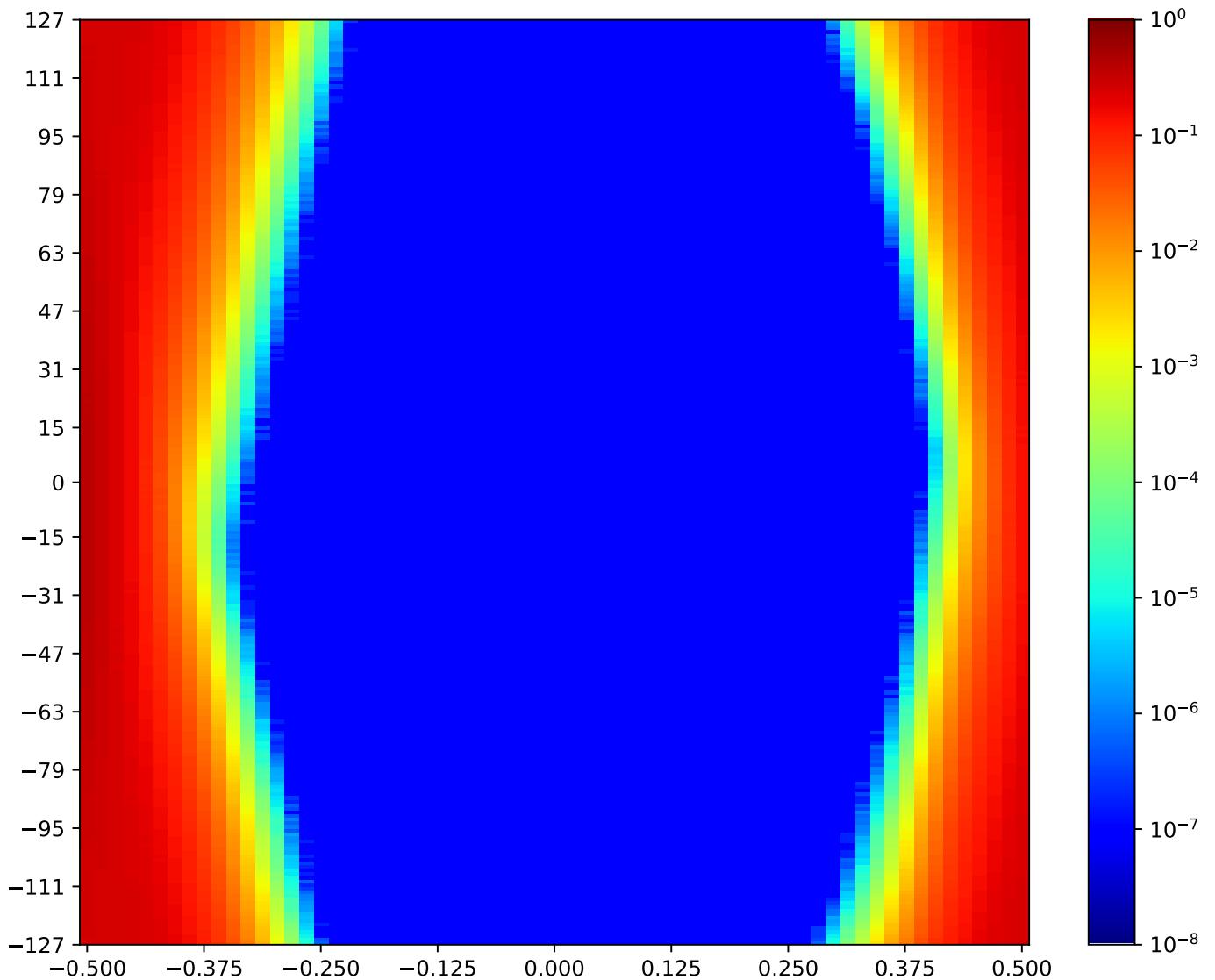


Figure 2.8: MSP\_A\_FPGA-TX1-06-RX16-06-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.1.8 MSP\_A\_FPGA-TX1-07-RX16-07-MSP\_C\_FPGA

Table 2.8: MSP\_A\_FPGA-TX1-07-RX16-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:11:01		2018-Jan-24 19:11:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9854	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

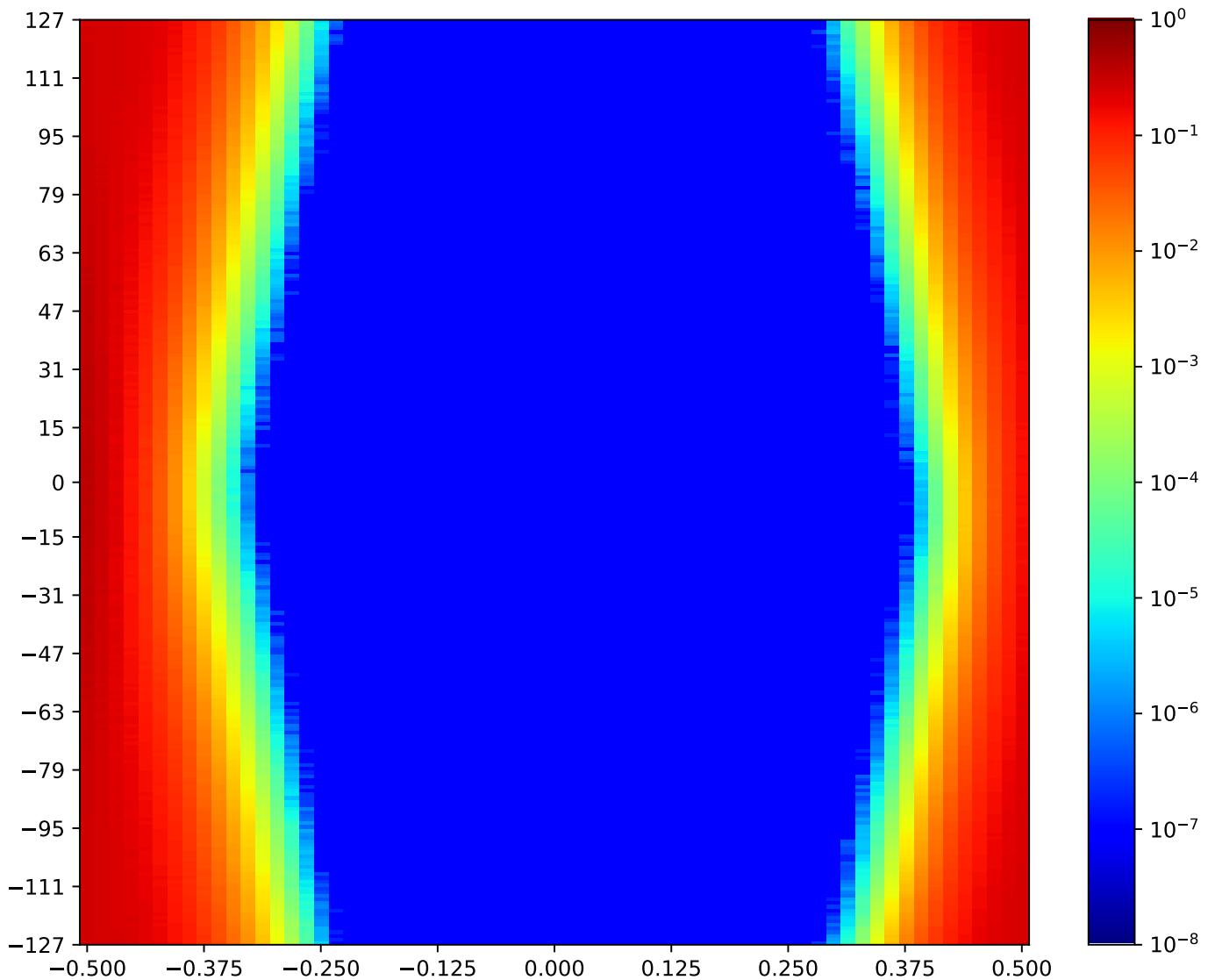


Figure 2.9: MSP\_A\_FPGA-TX1-07-RX16-07-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.1.9 MSP\_A\_FPGA-TX1-08-RX16-08-MSP\_C\_FPGA

Table 2.9: MSP\_A\_FPGA-TX1-08-RX16-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:15:14		2018-Jan-24 19:15:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10254	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

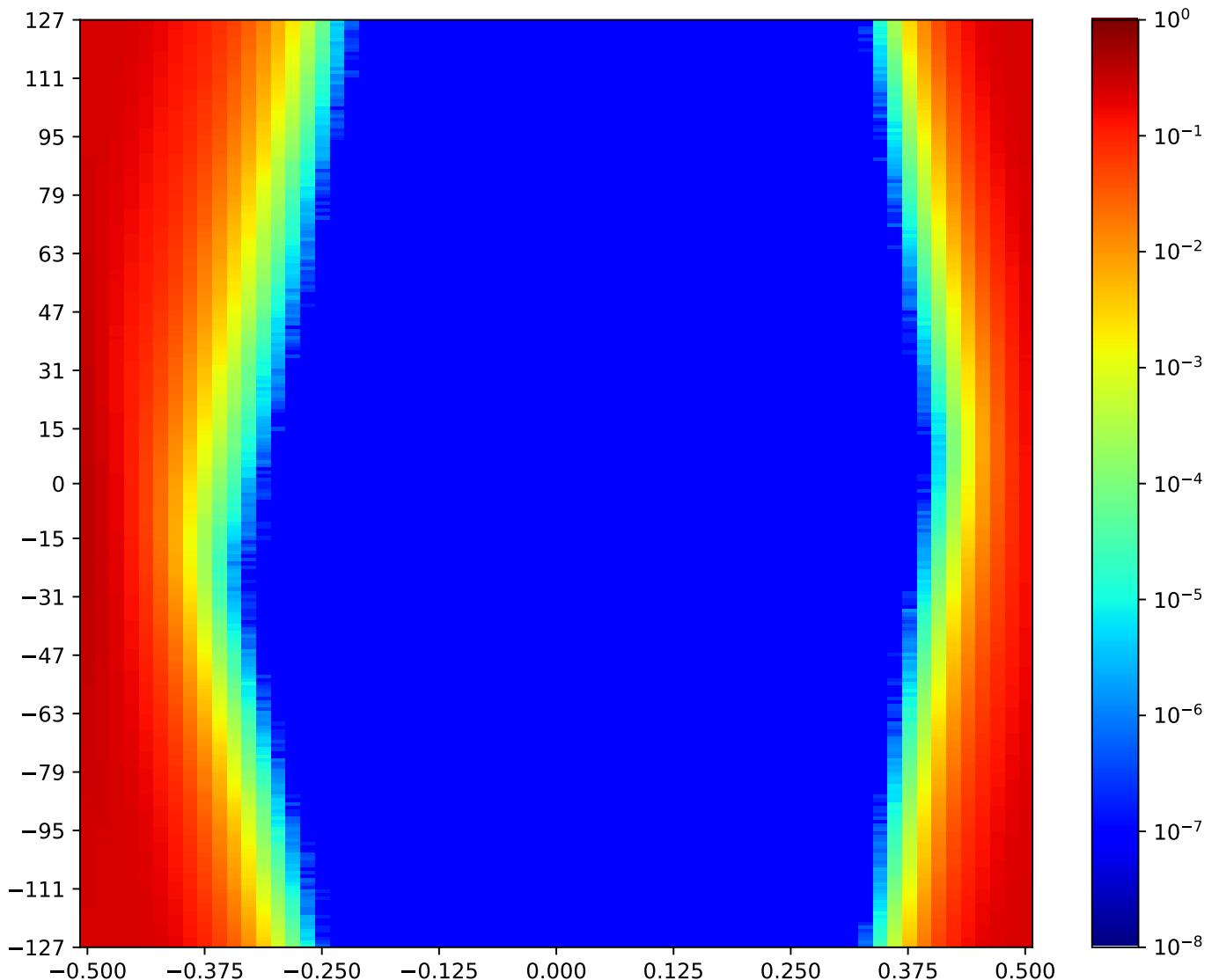


Figure 2.10: MSP\_A\_FPGA-TX1-08-RX16-08-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.1.10 MSP\_A\_FPGA-TX1-09-RX16-09-MSP\_C\_FPGA

Table 2.10: MSP\_A\_FPGA-TX1-09-RX16-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:12:05		2018-Jan-24 19:12:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11001	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

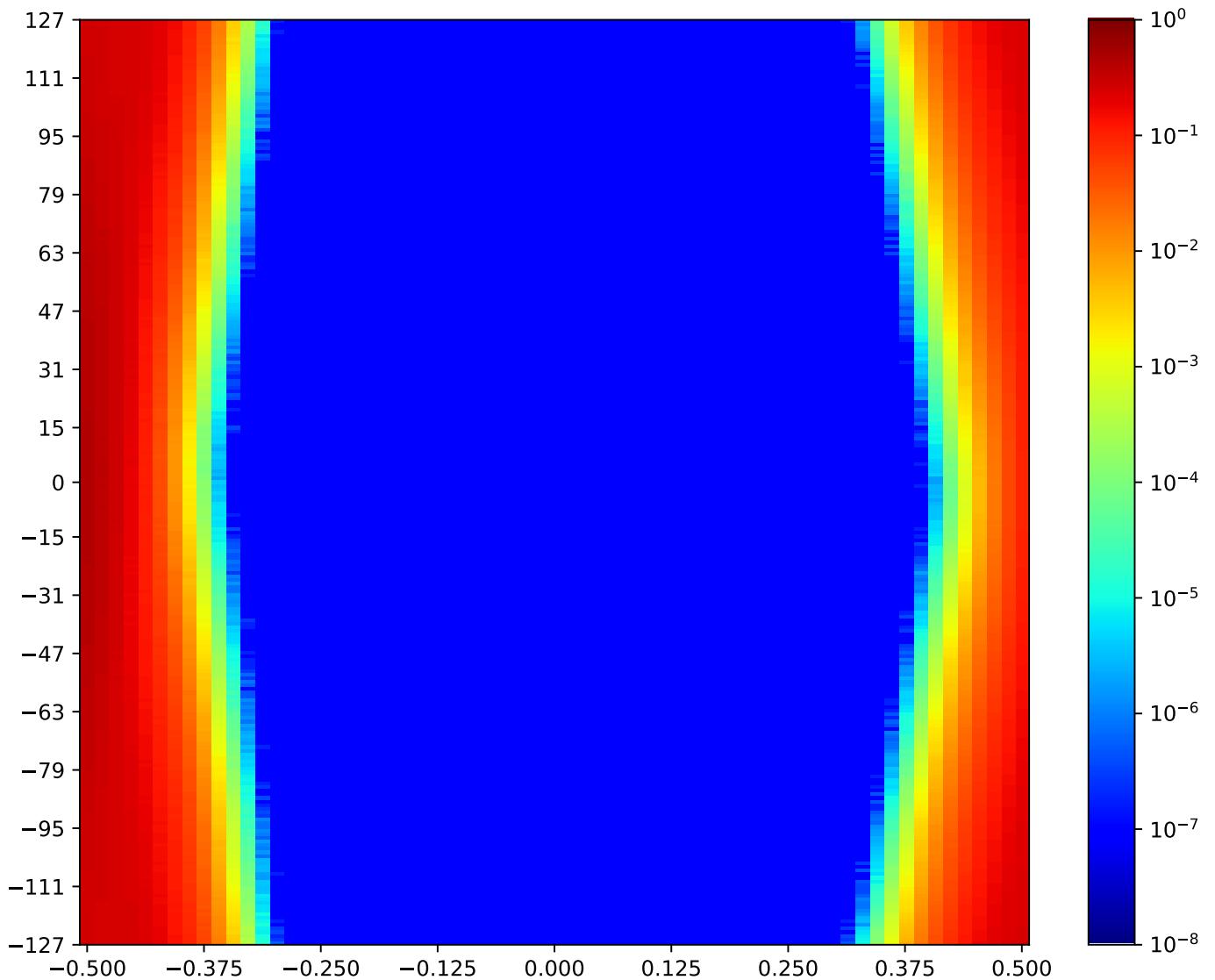


Figure 2.11: MSP\_A\_FPGA-TX1-09-RX16-09-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.1.11 MSP\_A\_FPGA-TX1-10-RX16-10-MSP\_C\_FPGA

Table 2.11: MSP\_A\_FPGA-TX1-10-RX16-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:14:11		2018-Jan-24 19:14:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10546	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

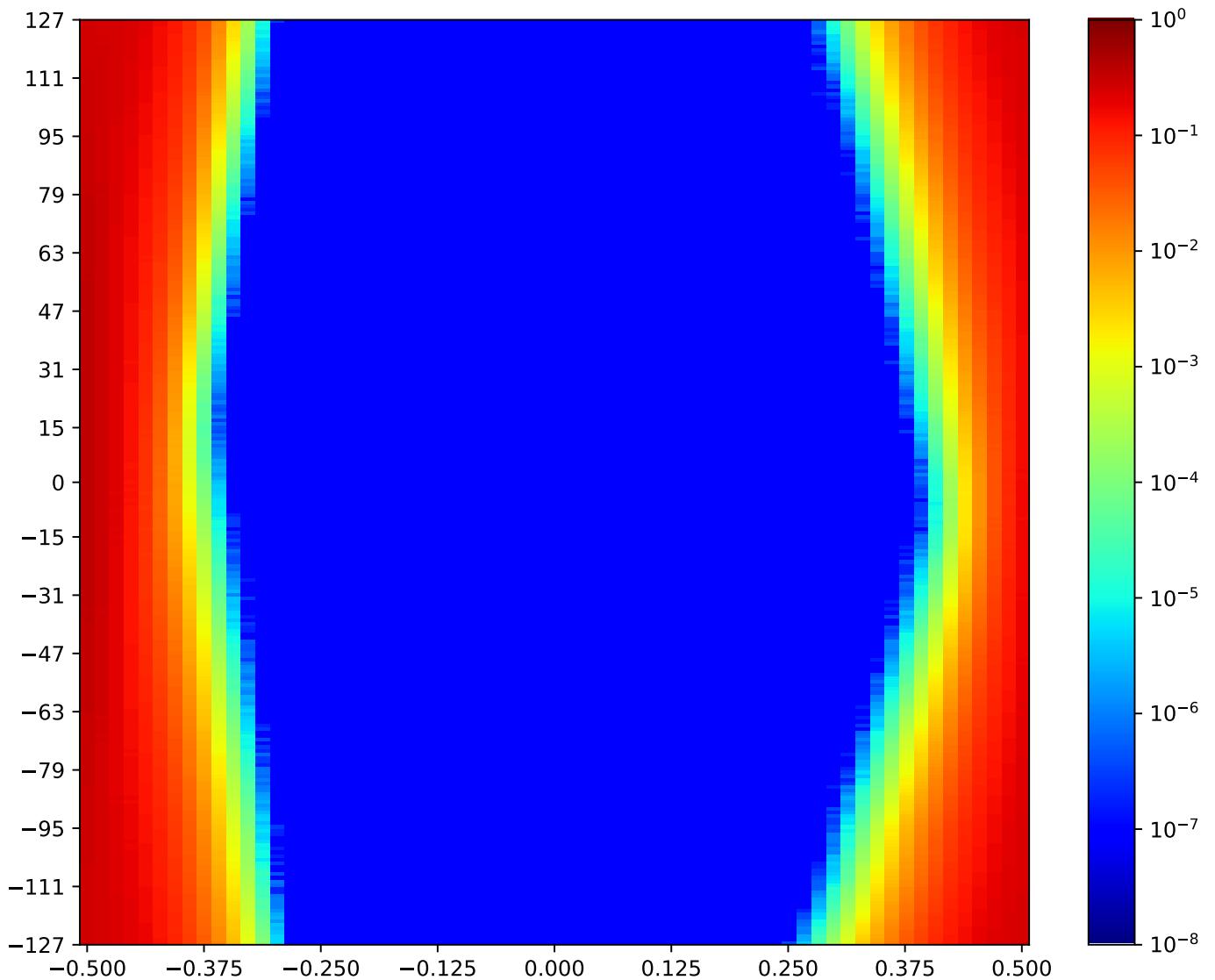


Figure 2.12: MSP\_A\_FPGA-TX1-10-RX16-10-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.1.12 MSP\_A\_FPGA-TX1-11-RX16-11-MSP\_C\_FPGA

Table 2.12: MSP\_A\_FPGA-TX1-11-RX16-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:13:40		2018-Jan-24 19:14:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10150	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

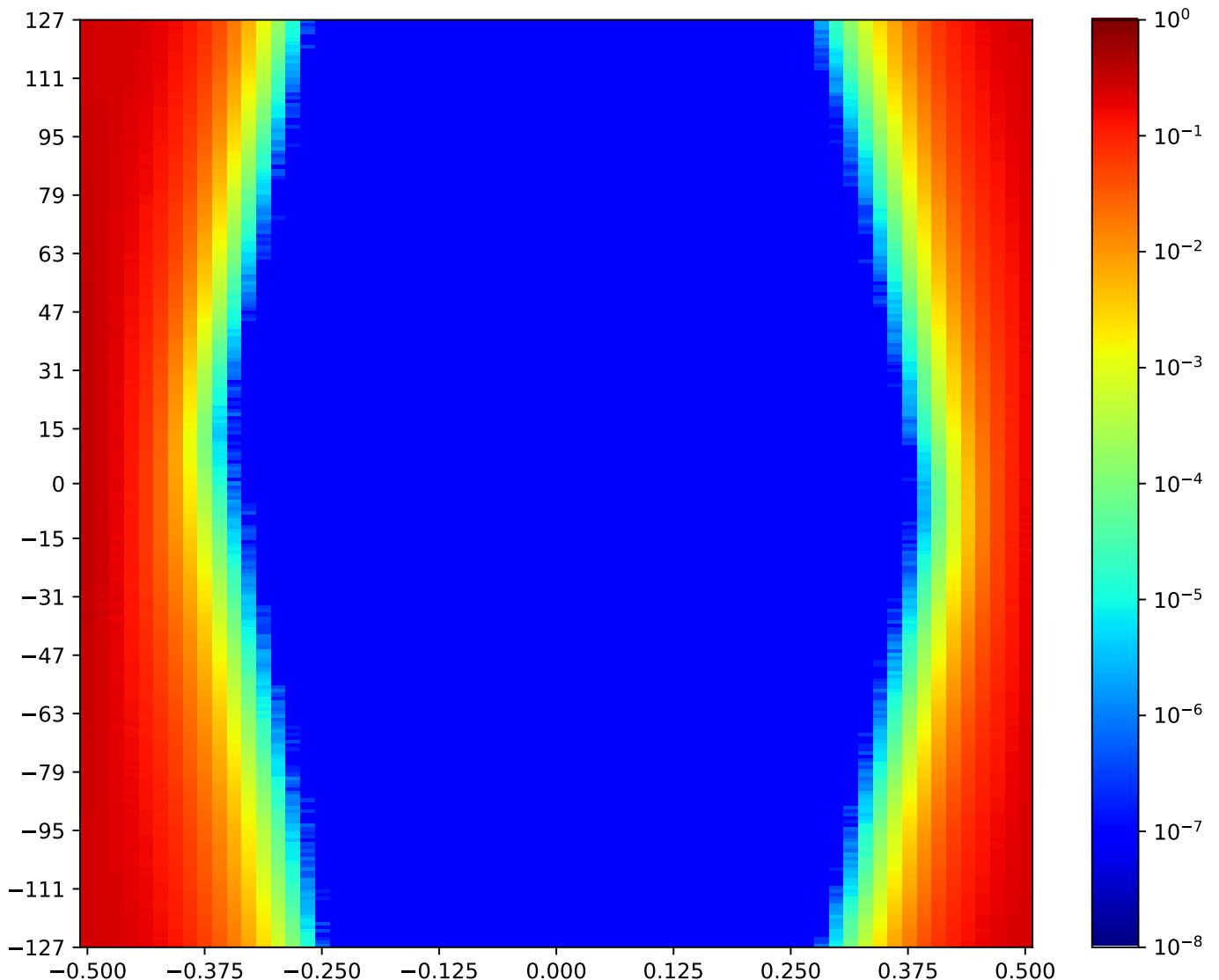


Figure 2.13: MSP\_A\_FPGA-TX1-11-RX16-11-MSP\_C\_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.2 MSP\_A TX2 MSP\_C RX15 Minipod Loopback

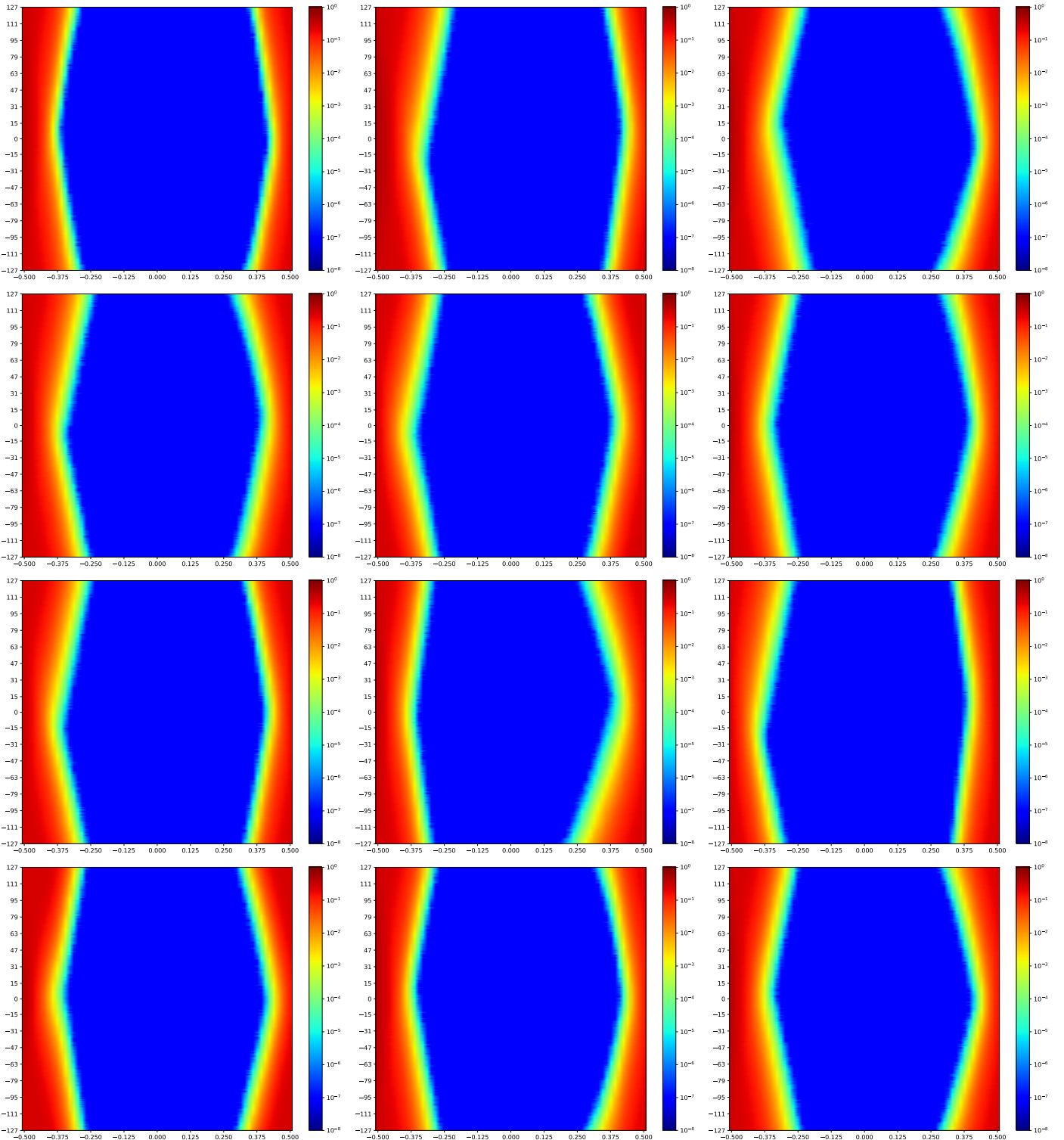


Figure 2.14: MSP\_A TX2 MSP\_C RX15 Minipod Loopback

A cross-reference to Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.27.

### 2.2.1 MSP\_A\_FPGA-TX2-00-RX15-00-MSP\_C\_FPGA

Table 2.13: MSP\_A\_FPGA-TX2-00-RX15-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:17:47		2018-Jan-24 19:18:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11237	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

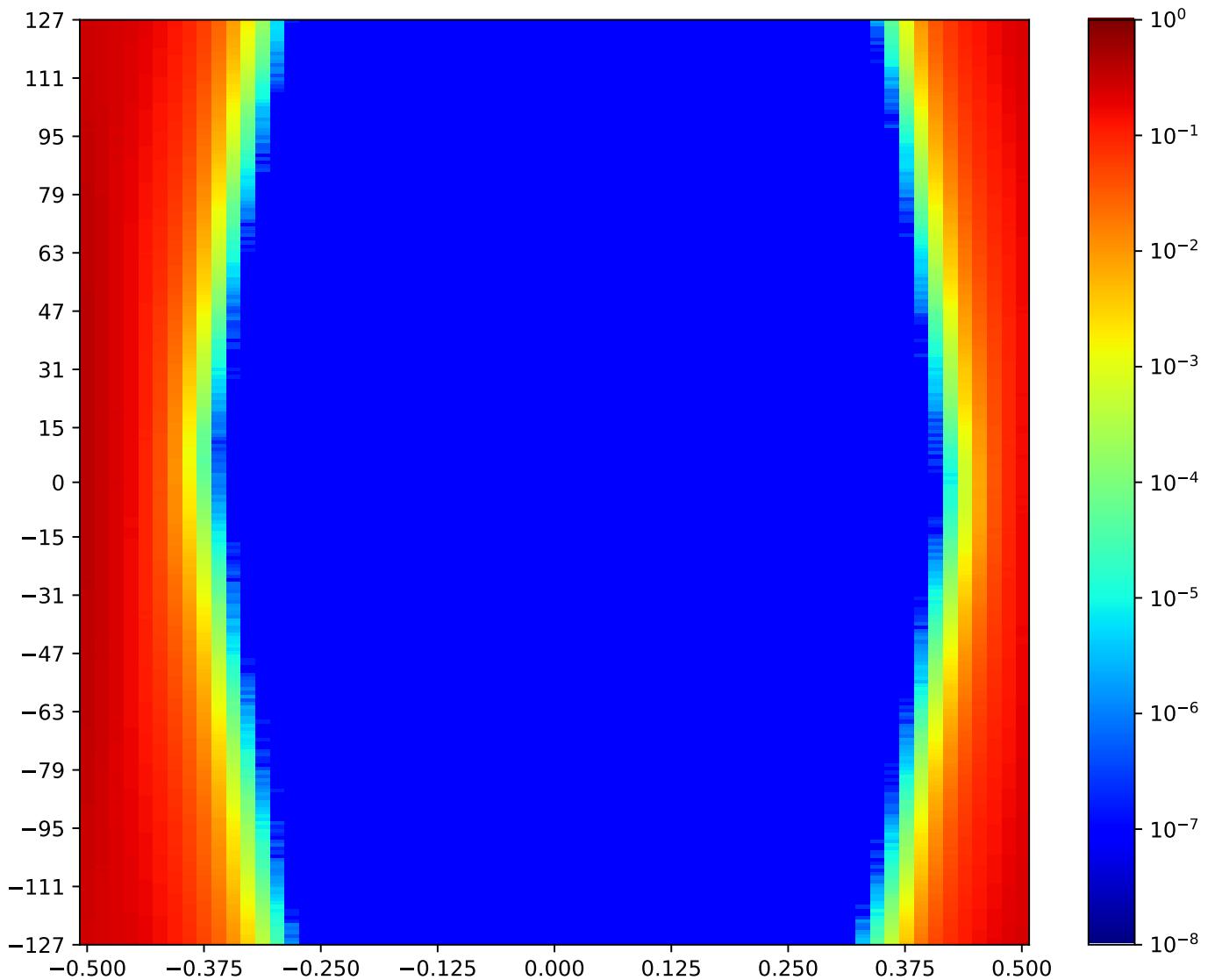


Figure 2.15: MSP\_A\_FPGA-TX2-00-RX15-00-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.2.2 MSP\_A\_FPGA-TX2-01-RX15-01-MSP\_C\_FPGA

Table 2.14: MSP\_A\_FPGA-TX2-01-RX15-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:16:45		2018-Jan-24 19:17:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10221	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

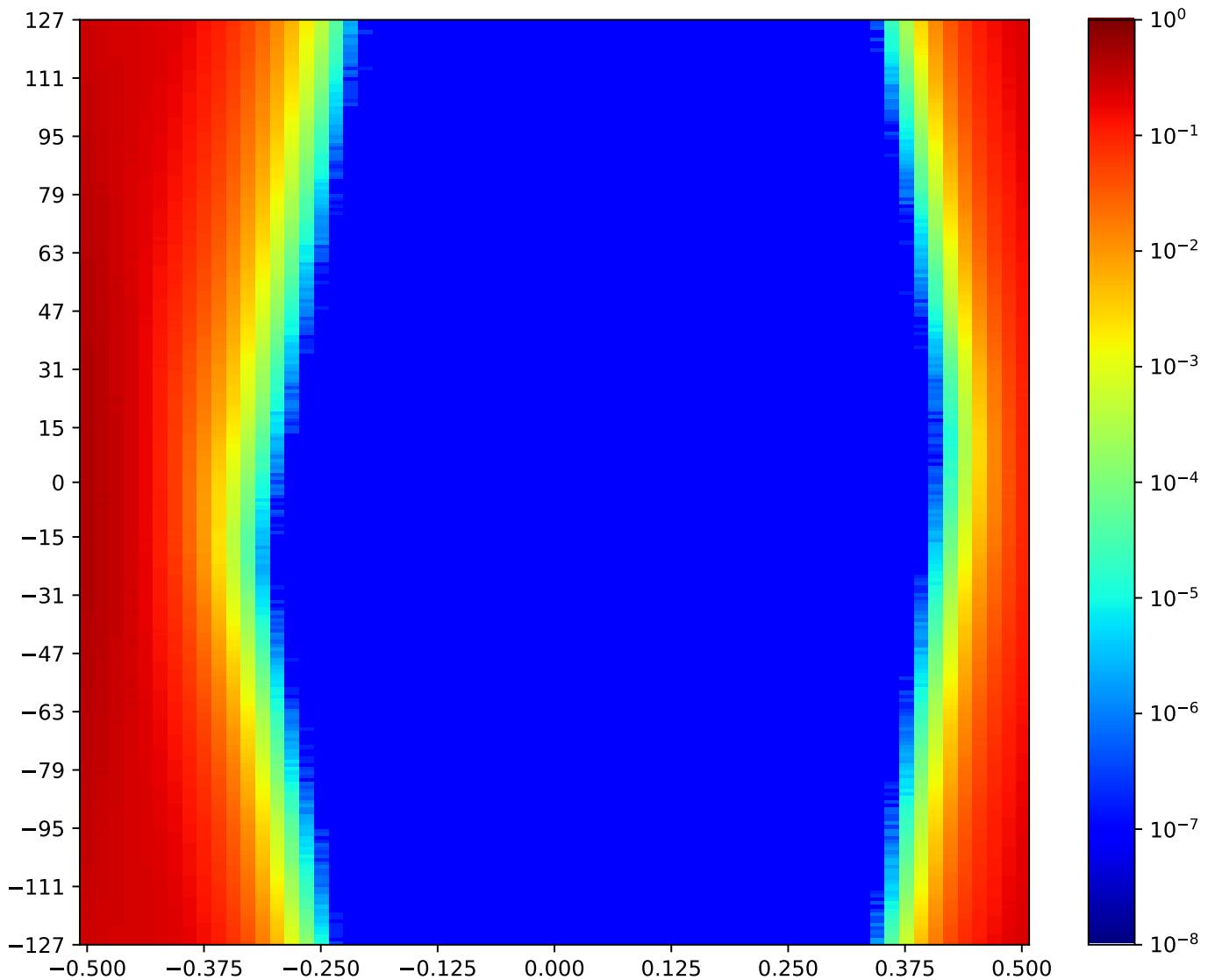


Figure 2.16: MSP\_A\_FPGA-TX2-01-RX15-01-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.2.3 MSP\_A\_FPGA-TX2-02-RX15-02-MSP\_C\_FPGA

Table 2.15: MSP\_A\_FPGA-TX2-02-RX15-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:19:17		2018-Jan-24 19:19:46	
Reset RX	OA	HO		HO (%)	
true	9425	42		64.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

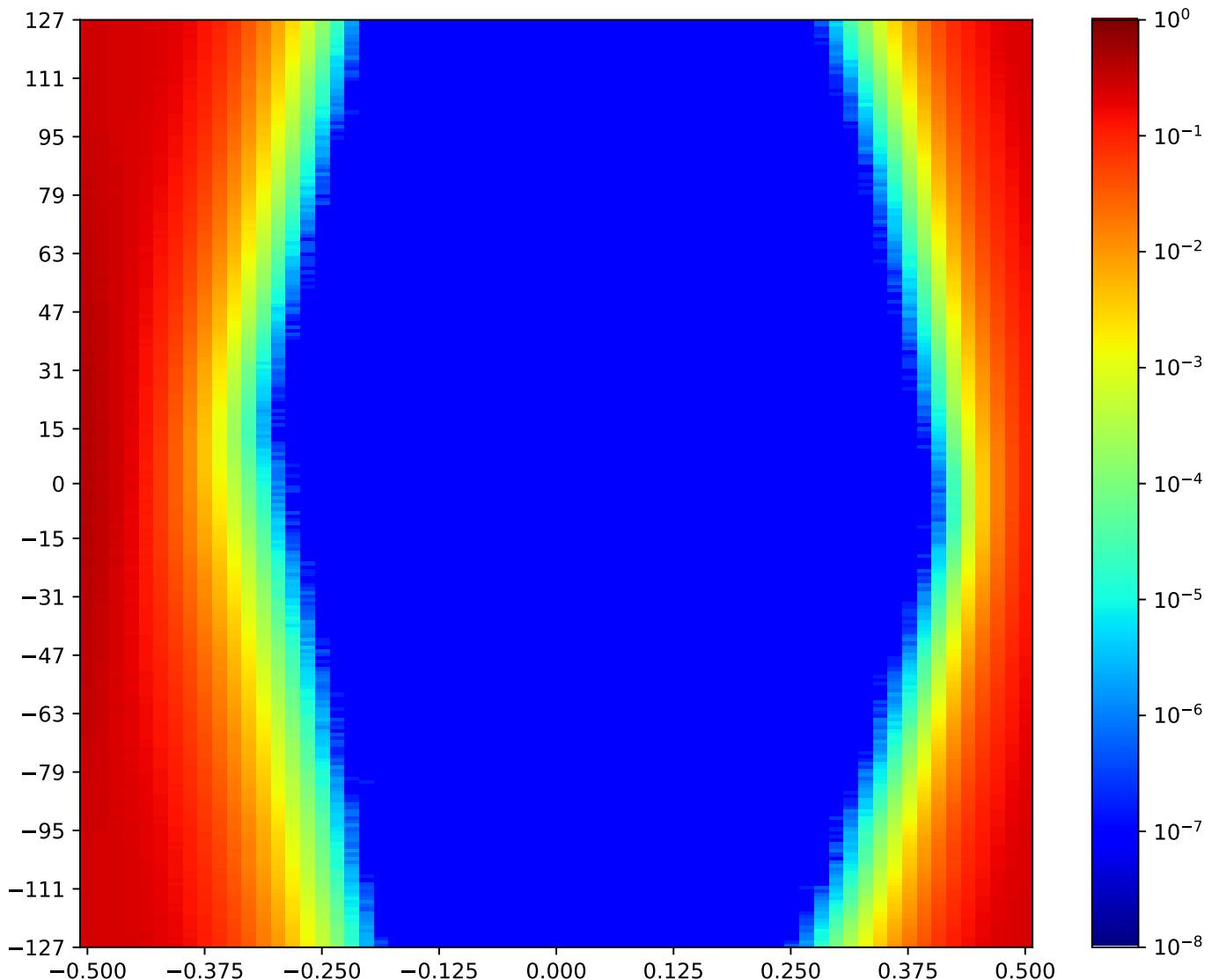


Figure 2.17: MSP\_A\_FPGA-TX2-02-RX15-02-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.2.4 MSP\_A\_FPGA-TX2-03-RX15-03-MSP\_C\_FPGA

Table 2.16: MSP\_A\_FPGA-TX2-03-RX15-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:16:12		2018-Jan-24 19:16:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9859	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

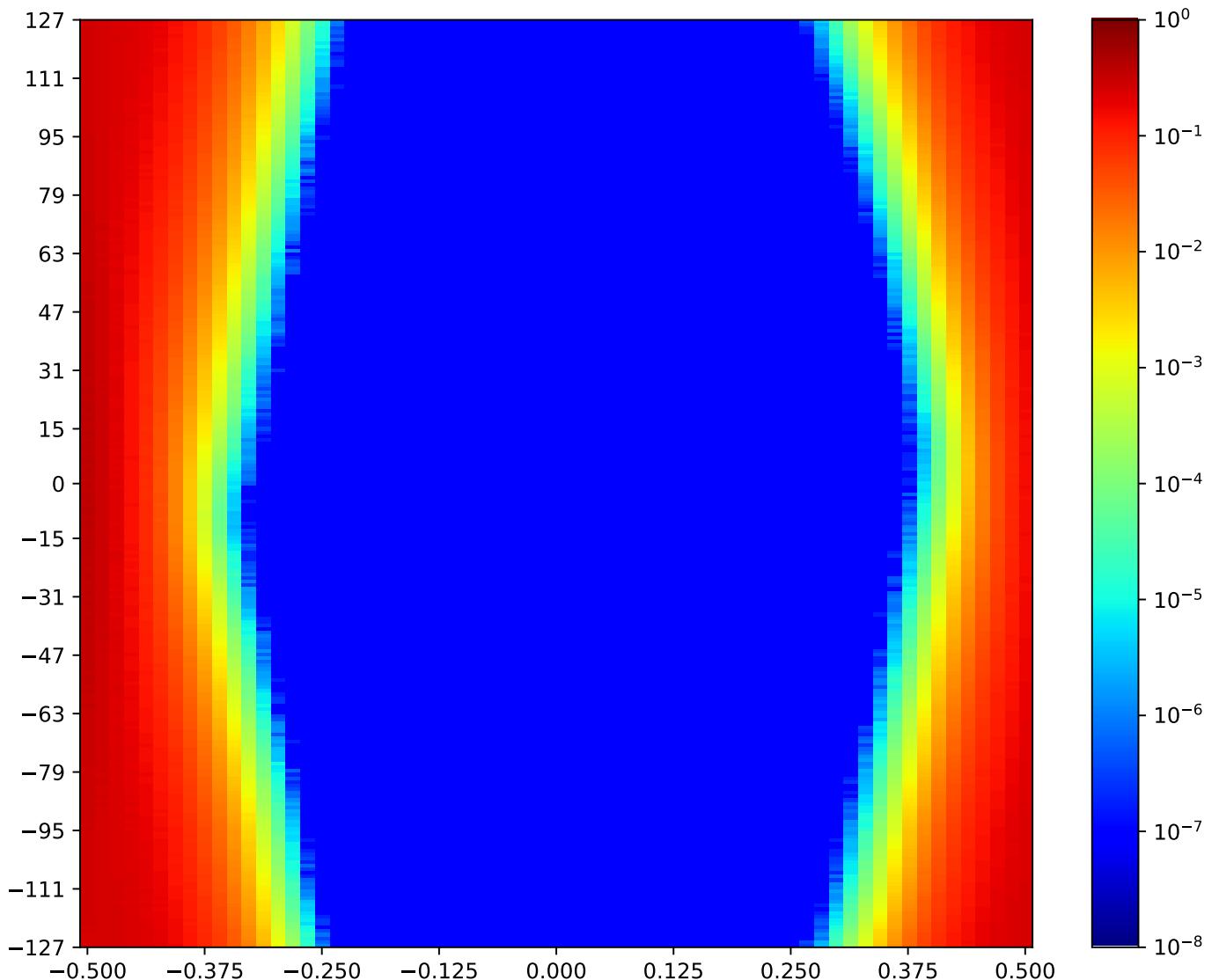


Figure 2.18: MSP\_A\_FPGA-TX2-03-RX15-03-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.2.5 MSP\_A\_FPGA-TX2-04-RX15-04-MSP\_C\_FPGA

Table 2.17: MSP\_A\_FPGA-TX2-04-RX15-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:20:48		2018-Jan-24 19:21:17	
Reset RX	OA	HO		HO (%)	
true	9961	44		67.69%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

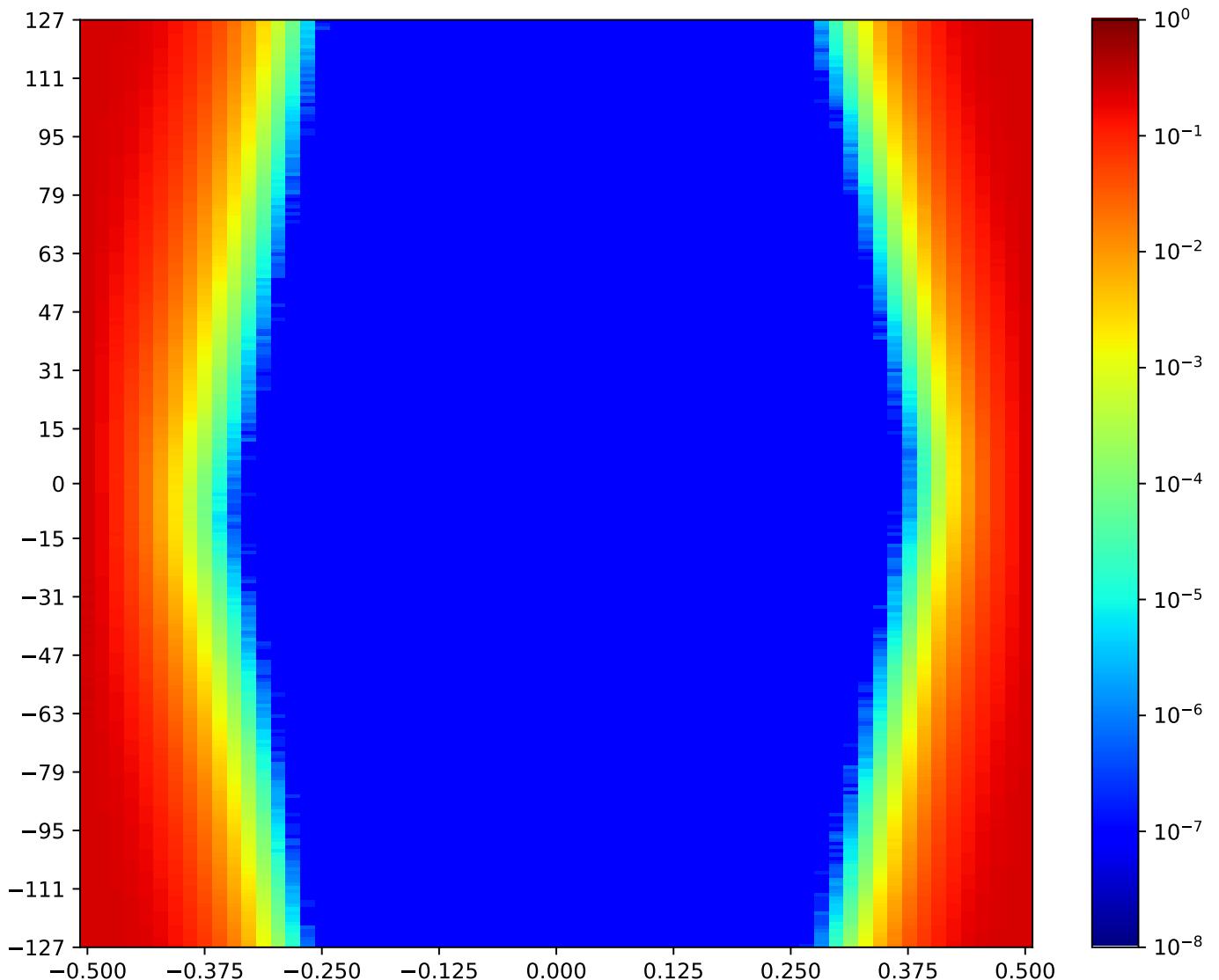


Figure 2.19: MSP\_A\_FPGA-TX2-04-RX15-04-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.2.6 MSP\_A\_FPGA-TX2-05-RX15-05-MSP\_C\_FPGA

Table 2.18: MSP\_A\_FPGA-TX2-05-RX15-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:17:17		2018-Jan-24 19:17:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9746	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

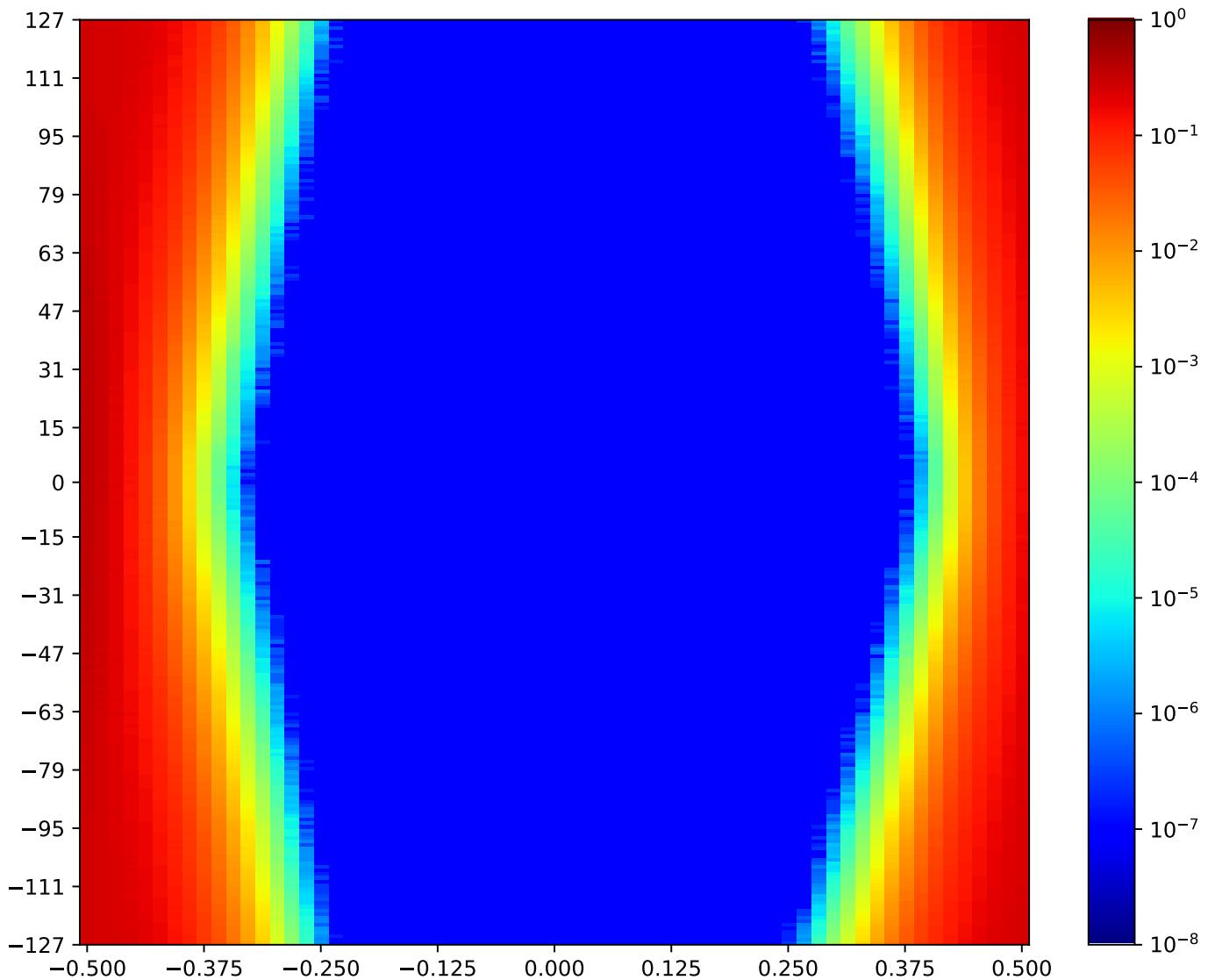


Figure 2.20: MSP\_A\_FPGA-TX2-05-RX15-05-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.2.7 MSP\_A\_FPGA-TX2-06-RX15-06-MSP\_C\_FPGA

Table 2.19: MSP\_A\_FPGA-TX2-06-RX15-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:21:47		2018-Jan-24 19:22:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10495	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

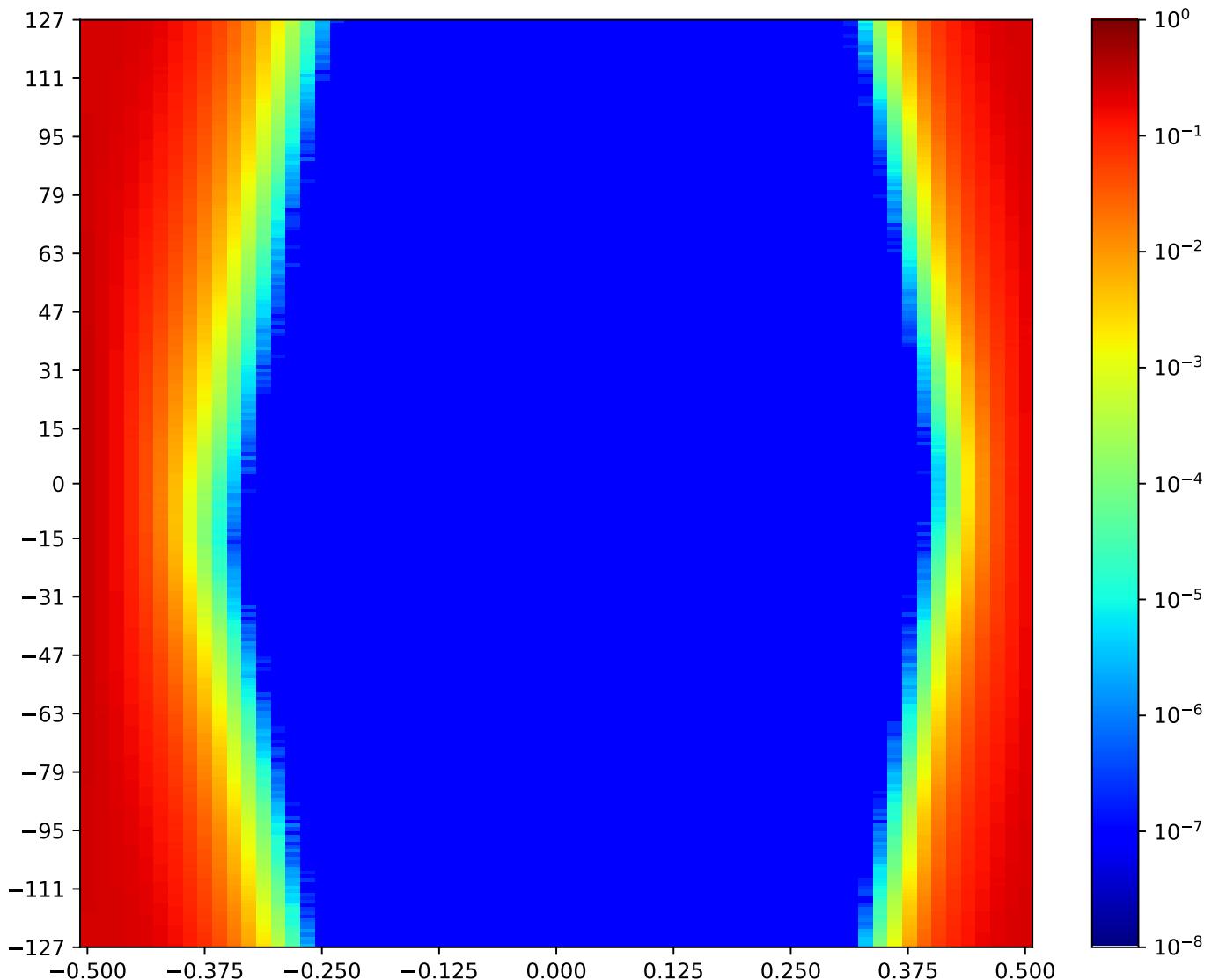


Figure 2.21: MSP\_A\_FPGA-TX2-06-RX15-06-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.2.8 MSP\_A\_FPGA-TX2-07-RX15-07-MSP\_C\_FPGA

Table 2.20: MSP\_A\_FPGA-TX2-07-RX15-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:18:19		2018-Jan-24 19:18:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9839	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

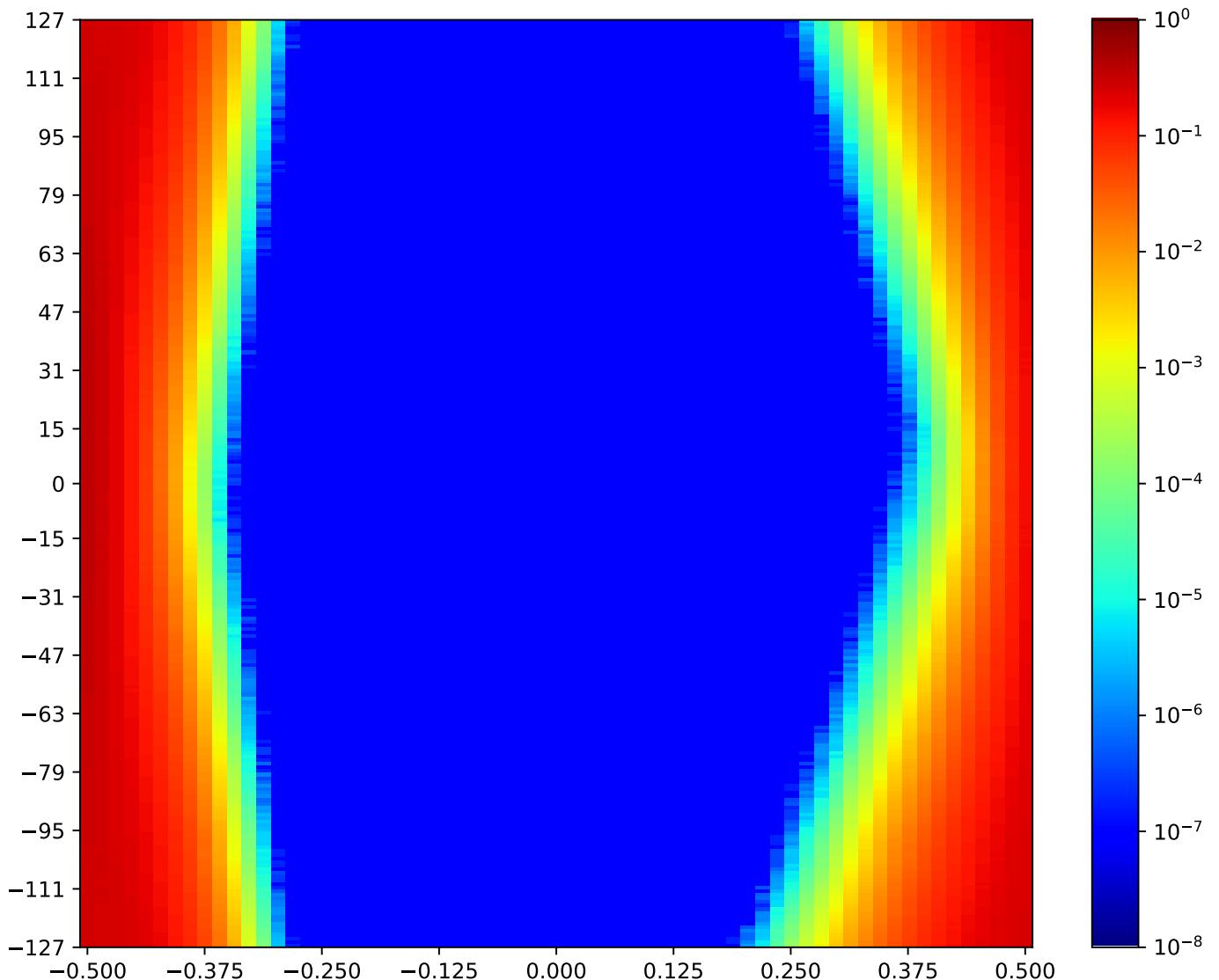


Figure 2.22: MSP\_A\_FPGA-TX2-07-RX15-07-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.2.9 MSP\_A\_FPGA-TX2-08-RX15-08-MSP\_C\_FPGA

Table 2.21: MSP\_A\_FPGA-TX2-08-RX15-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:21:17		2018-Jan-24 19:21:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10636	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

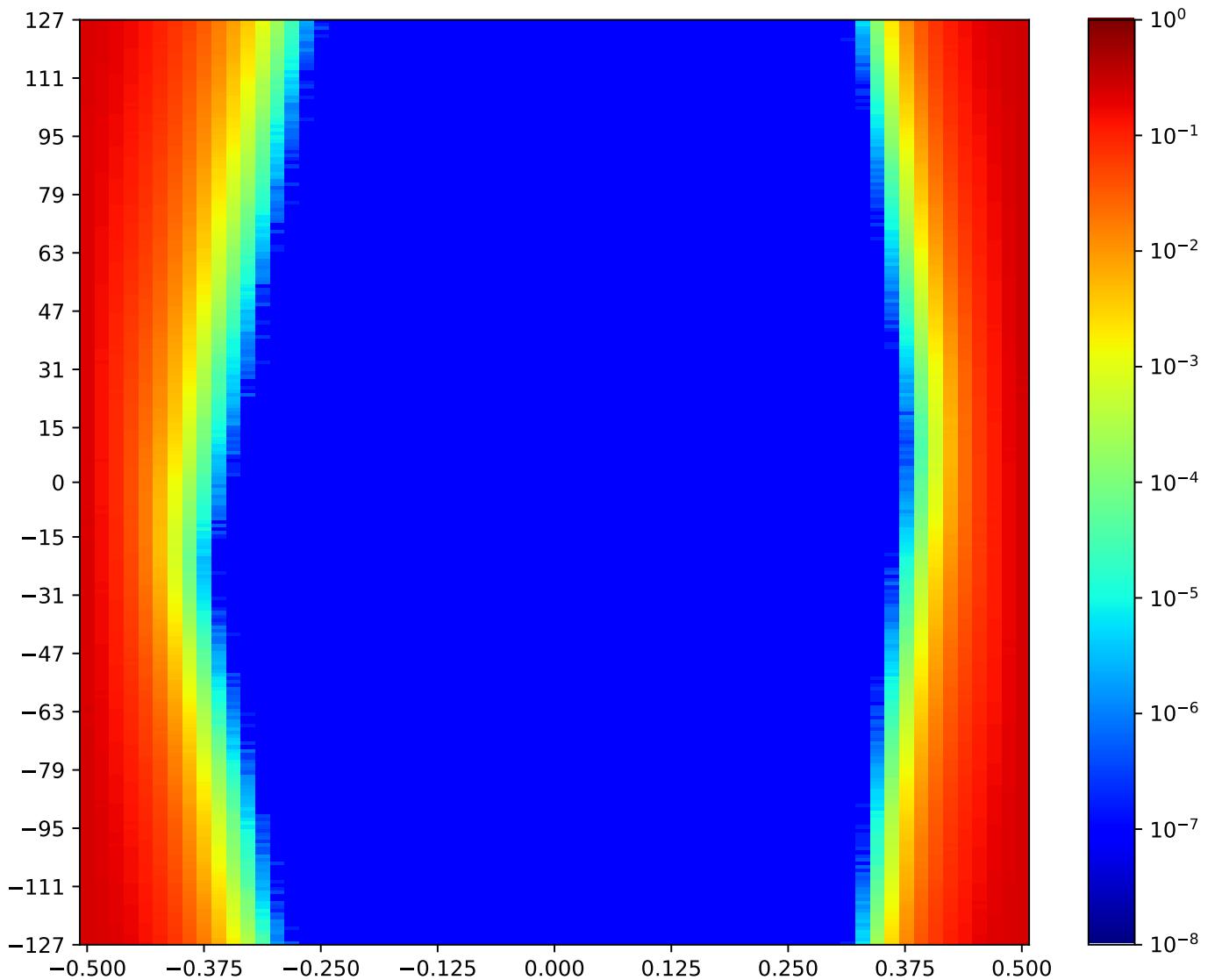


Figure 2.23: MSP\_A\_FPGA-TX2-08-RX15-08-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.2.10 MSP\_A\_FPGA-TX2-09-RX15-09-MSP\_C\_FPGA

Table 2.22: MSP\_A\_FPGA-TX2-09-RX15-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:18:48		2018-Jan-24 19:19:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10431	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

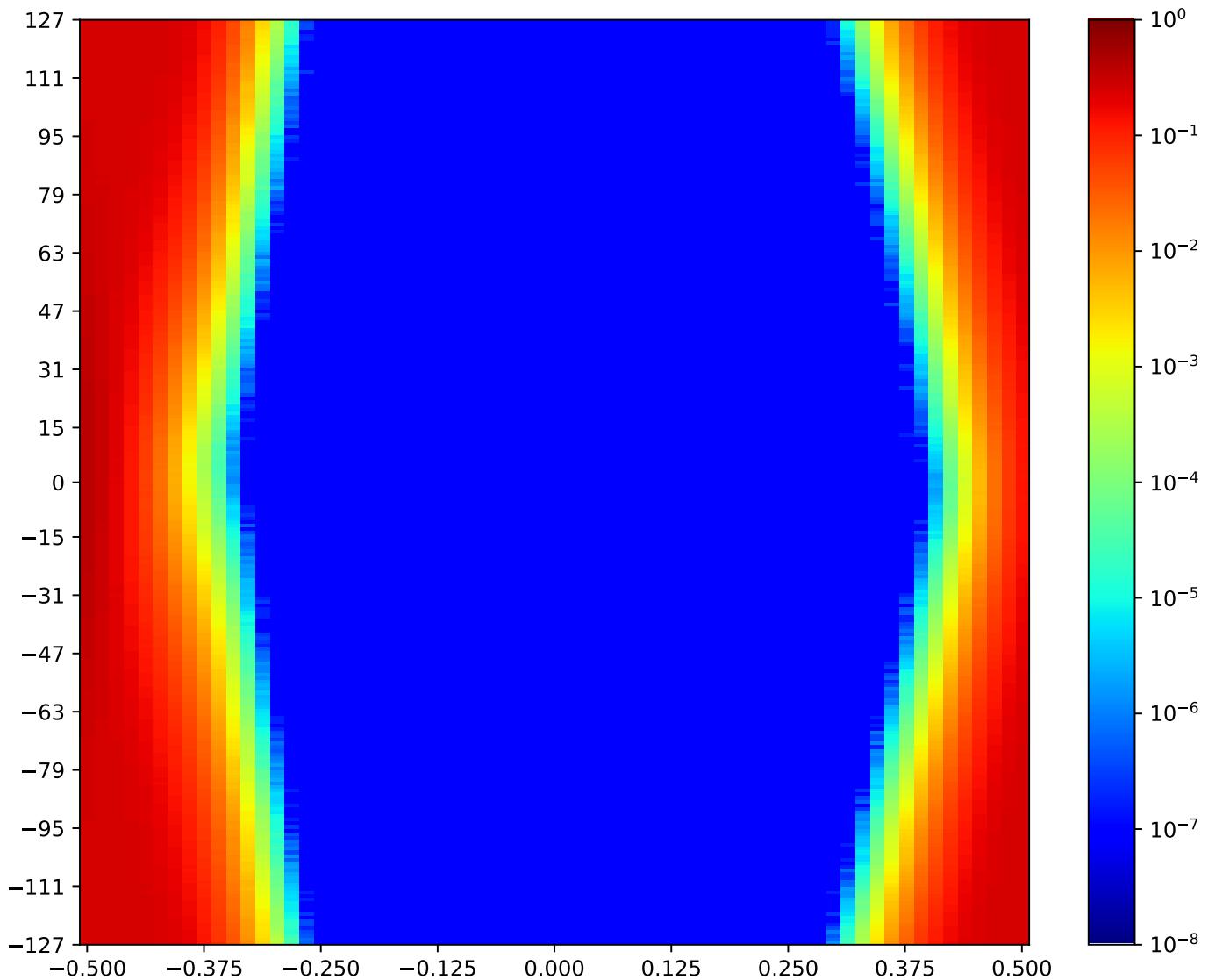


Figure 2.24: MSP\_A\_FPGA-TX2-09-RX15-09-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.2.11 MSP\_A\_FPGA-TX2-10-RX15-10-MSP\_C\_FPGA

Table 2.23: MSP\_A\_FPGA-TX2-10-RX15-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:20:17		2018-Jan-24 19:20:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10706	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

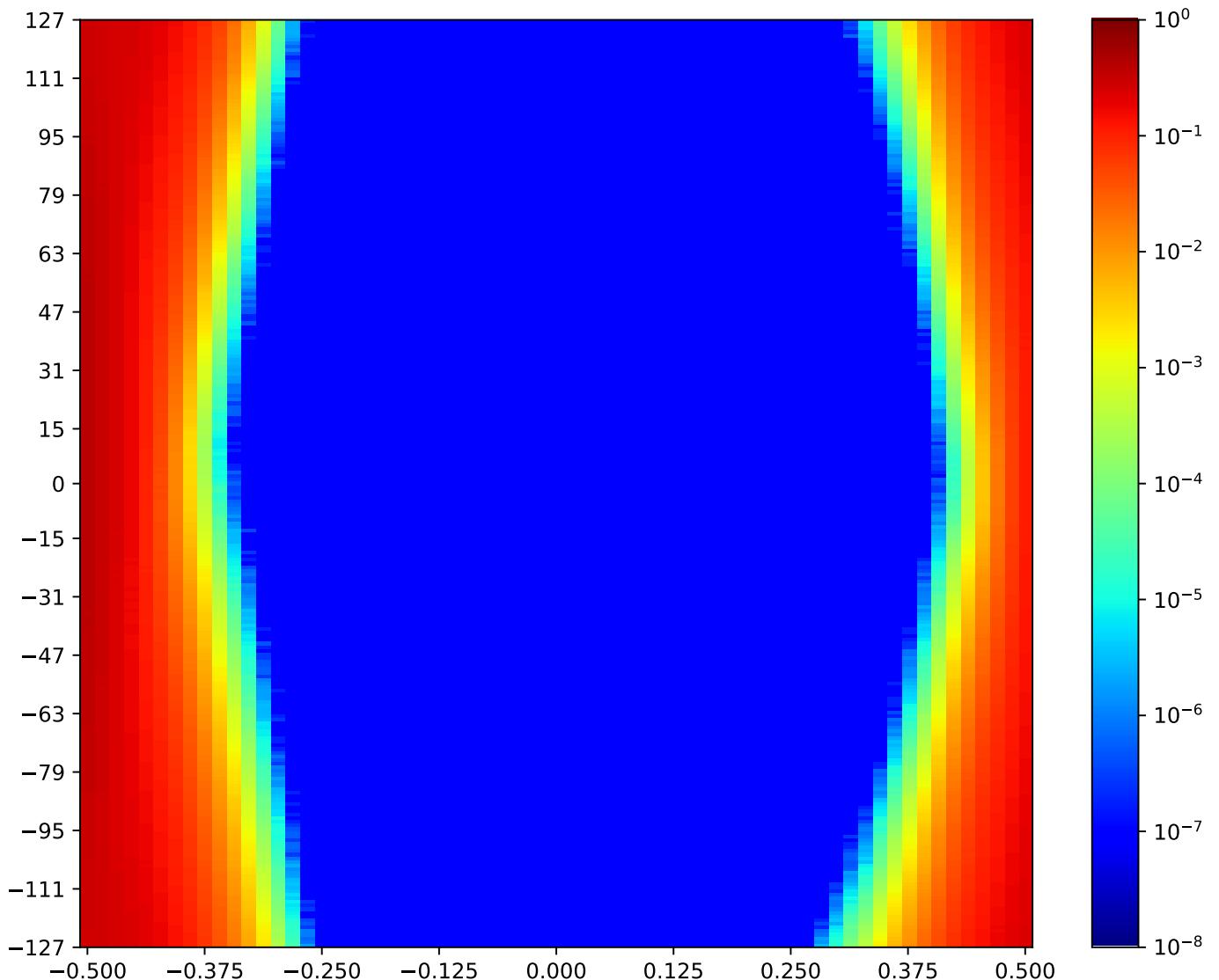


Figure 2.25: MSP\_A\_FPGA-TX2-10-RX15-10-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.2.12 MSP\_A\_FPGA-TX2-11-RX15-11-MSP\_C\_FPGA

Table 2.24: MSP\_A\_FPGA-TX2-11-RX15-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:19:46		2018-Jan-24 19:20:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10012	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

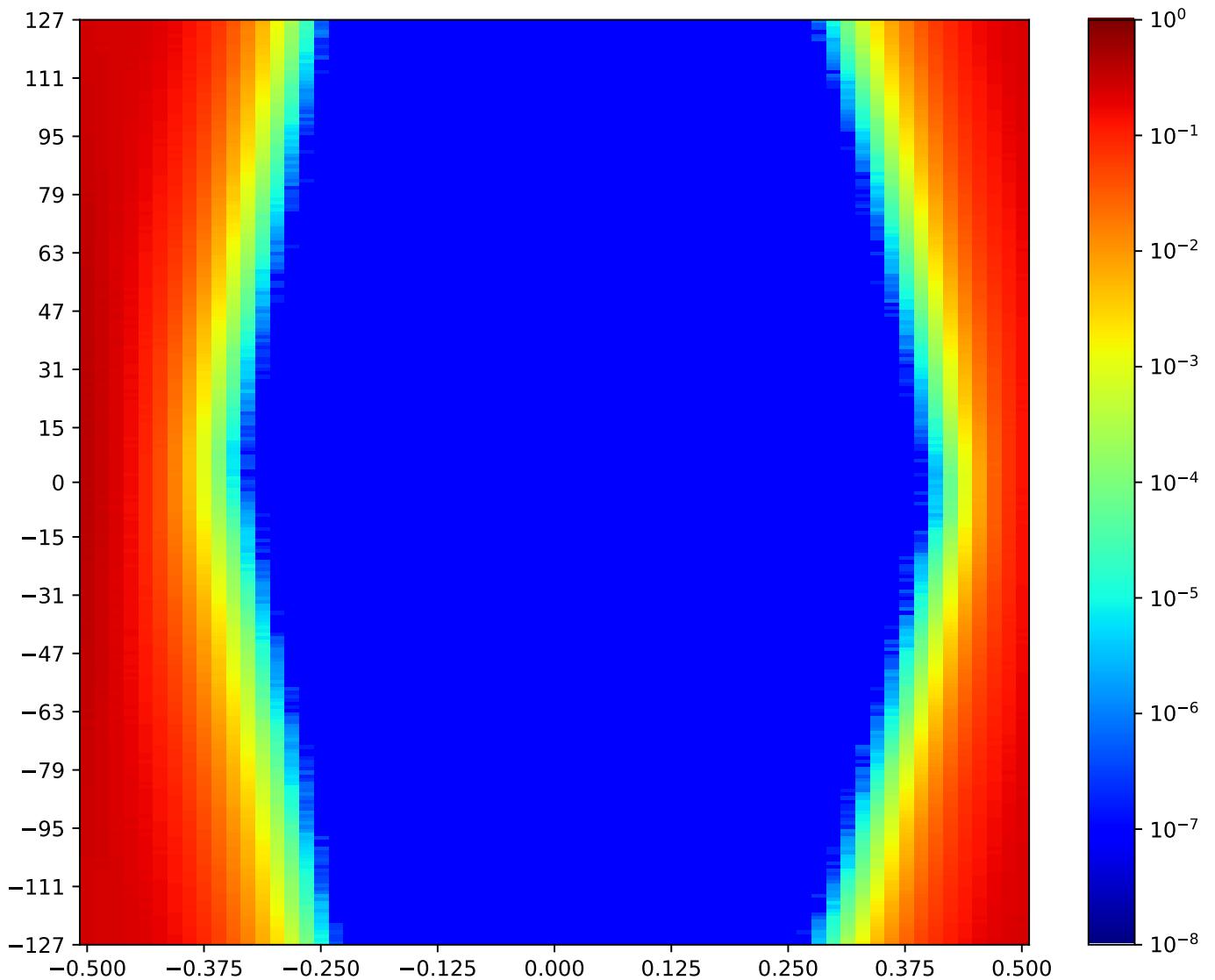


Figure 2.26: MSP\_A\_FPGA-TX2-11-RX15-11-MSP\_C\_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.3 MSP\_C TX3 MSP\_A RX7 Minipod Loopback

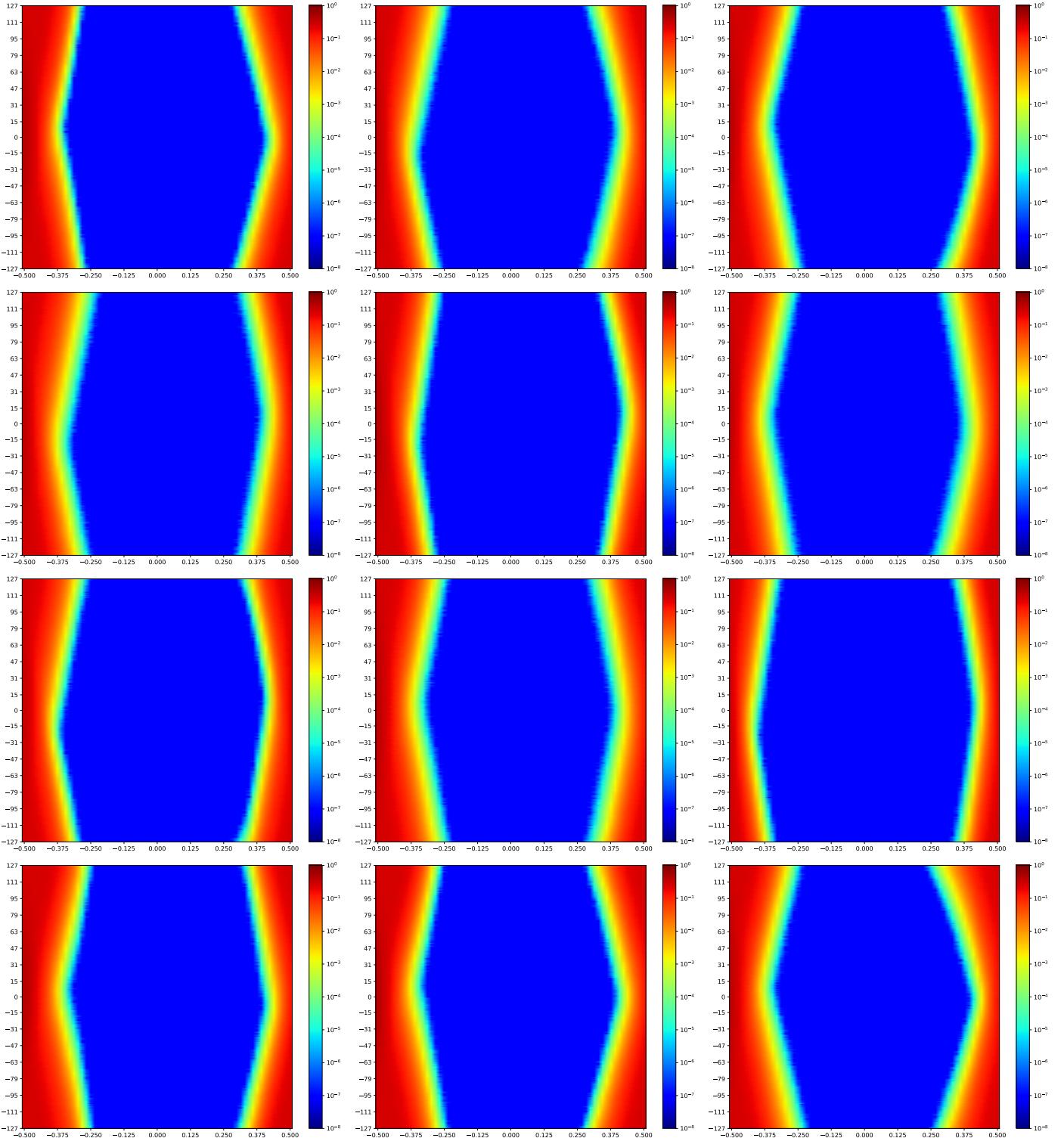


Figure 2.27: MSP\_C TX3 MSP\_A RX7 Minipod Loopback

A cross-reference to Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.40.

### 2.3.1 MSP\_C\_FPGA-TX3-00-RX7-00-MSP\_A\_FPGA

Table 2.25: MSP\_C\_FPGA-TX3-00-RX7-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:23:47		2018-Jan-24 19:24:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10383	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

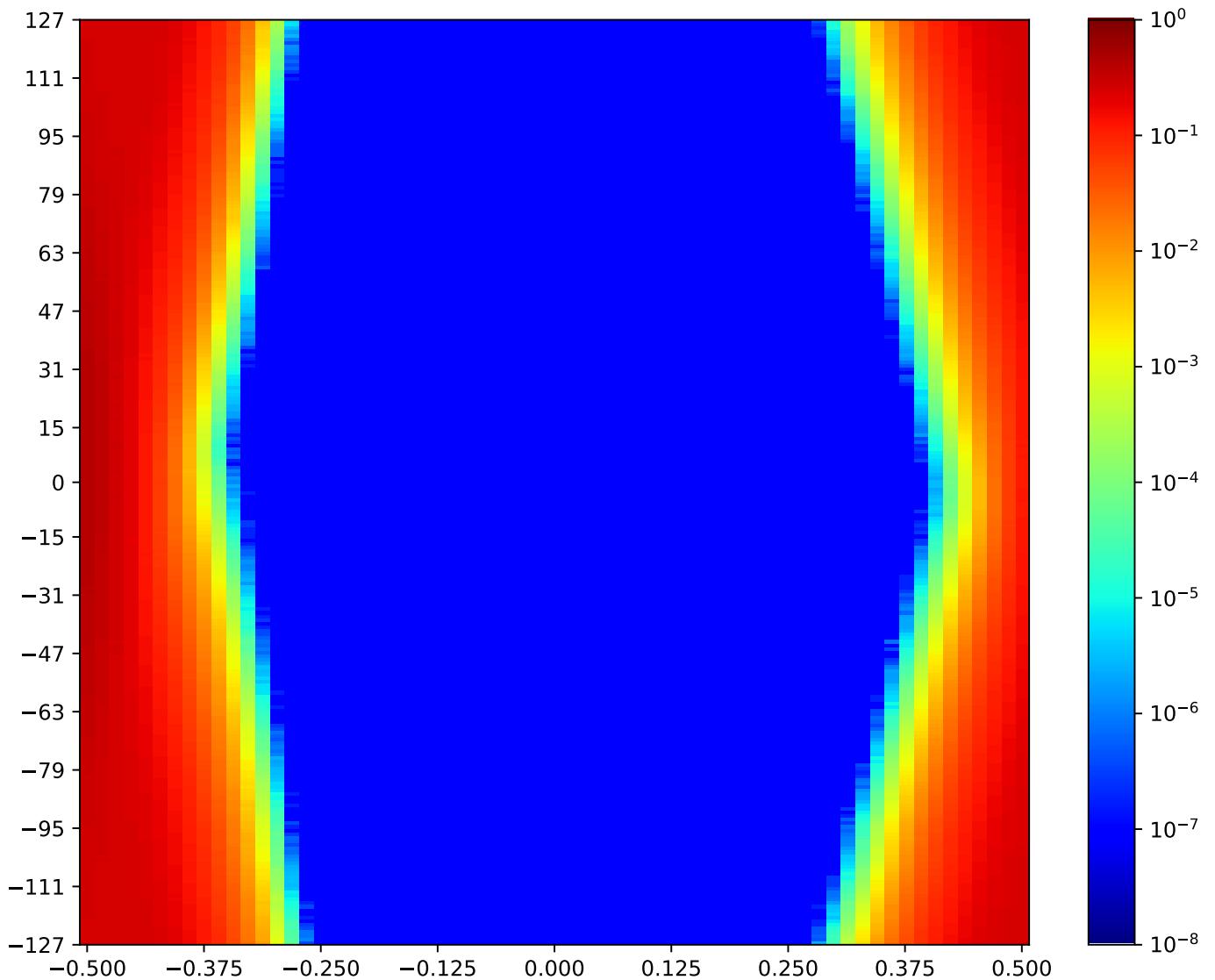


Figure 2.28: MSP\_C\_FPGA-TX3-00-RX7-00-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.2 MSP\_C\_FPGA-TX3-01-RX7-01-MSP\_A\_FPGA

Table 2.26: MSP\_C\_FPGA-TX3-01-RX7-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:24:48		2018-Jan-24 19:25:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9789	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

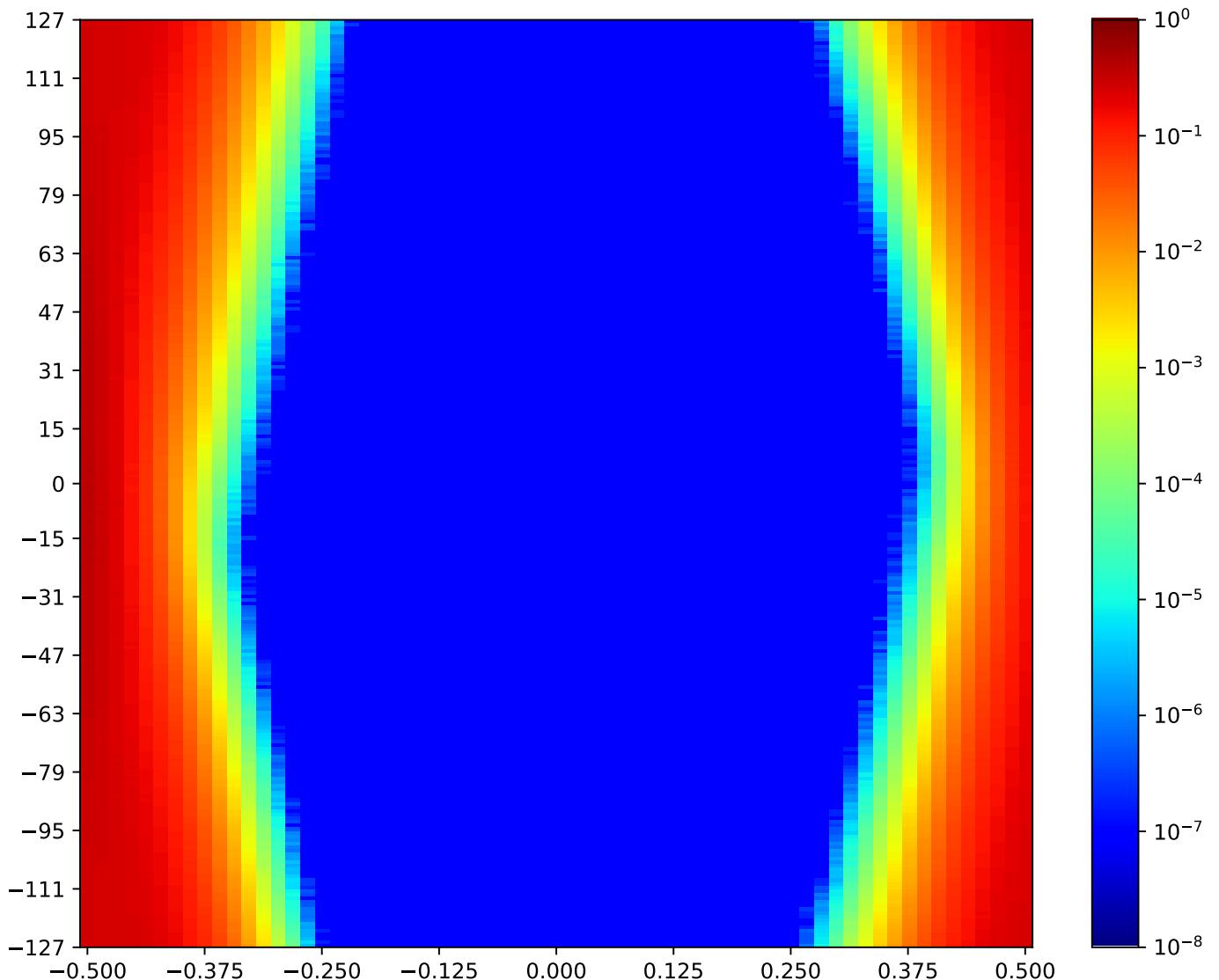


Figure 2.29: MSP\_C\_FPGA-TX3-01-RX7-01-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.3 MSP\_C\_FPGA-TX3-02-RX7-02-MSP\_A\_FPGA

Table 2.27: MSP\_C\_FPGA-TX3-02-RX7-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:25:18		2018-Jan-24 19:25:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9906	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

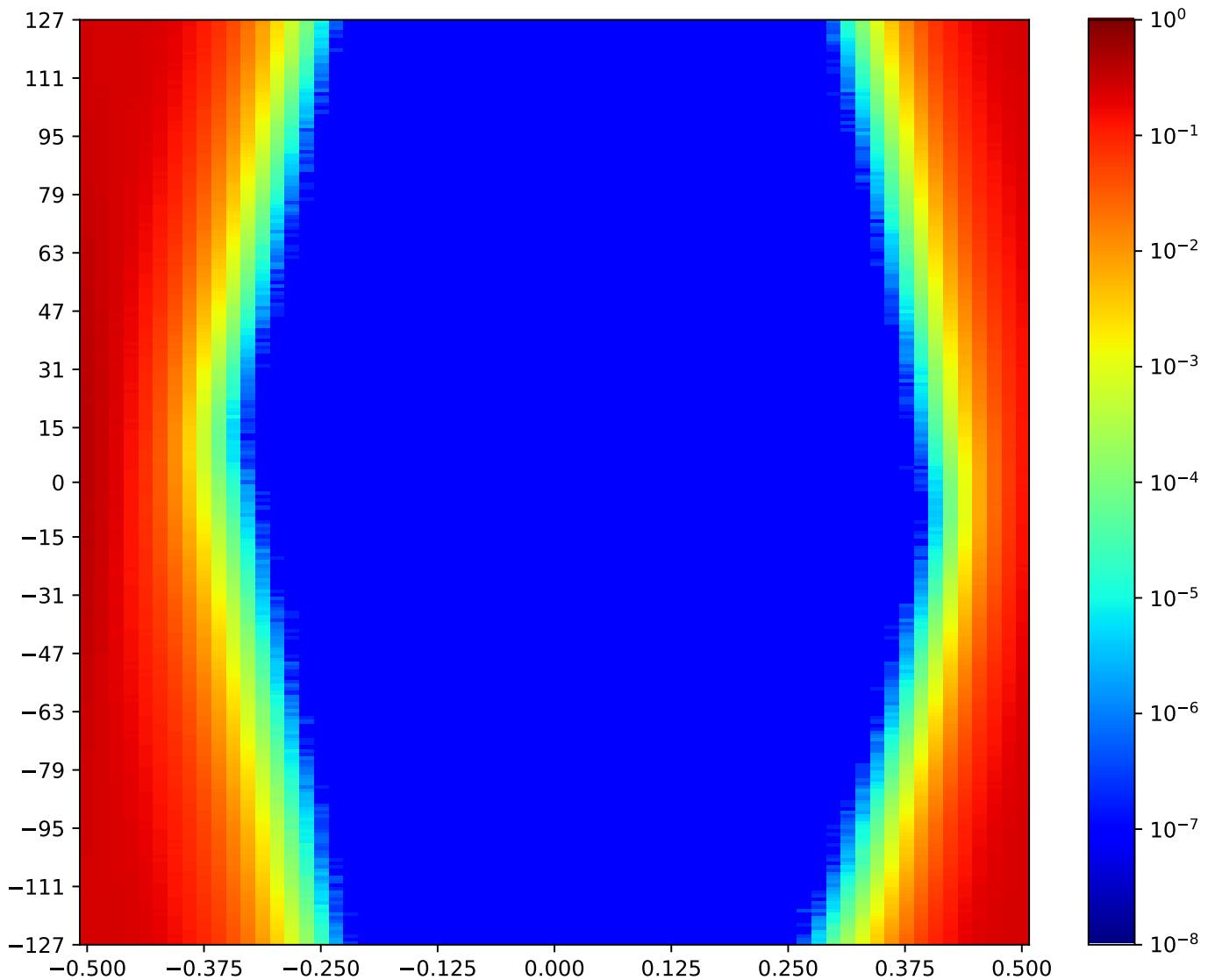


Figure 2.30: MSP\_C\_FPGA-TX3-02-RX7-02-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.4 MSP\_C\_FPGA-TX3-03-RX7-03-MSP\_A\_FPGA

Table 2.28: MSP\_C\_FPGA-TX3-03-RX7-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:22:48		2018-Jan-24 19:23:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9775	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

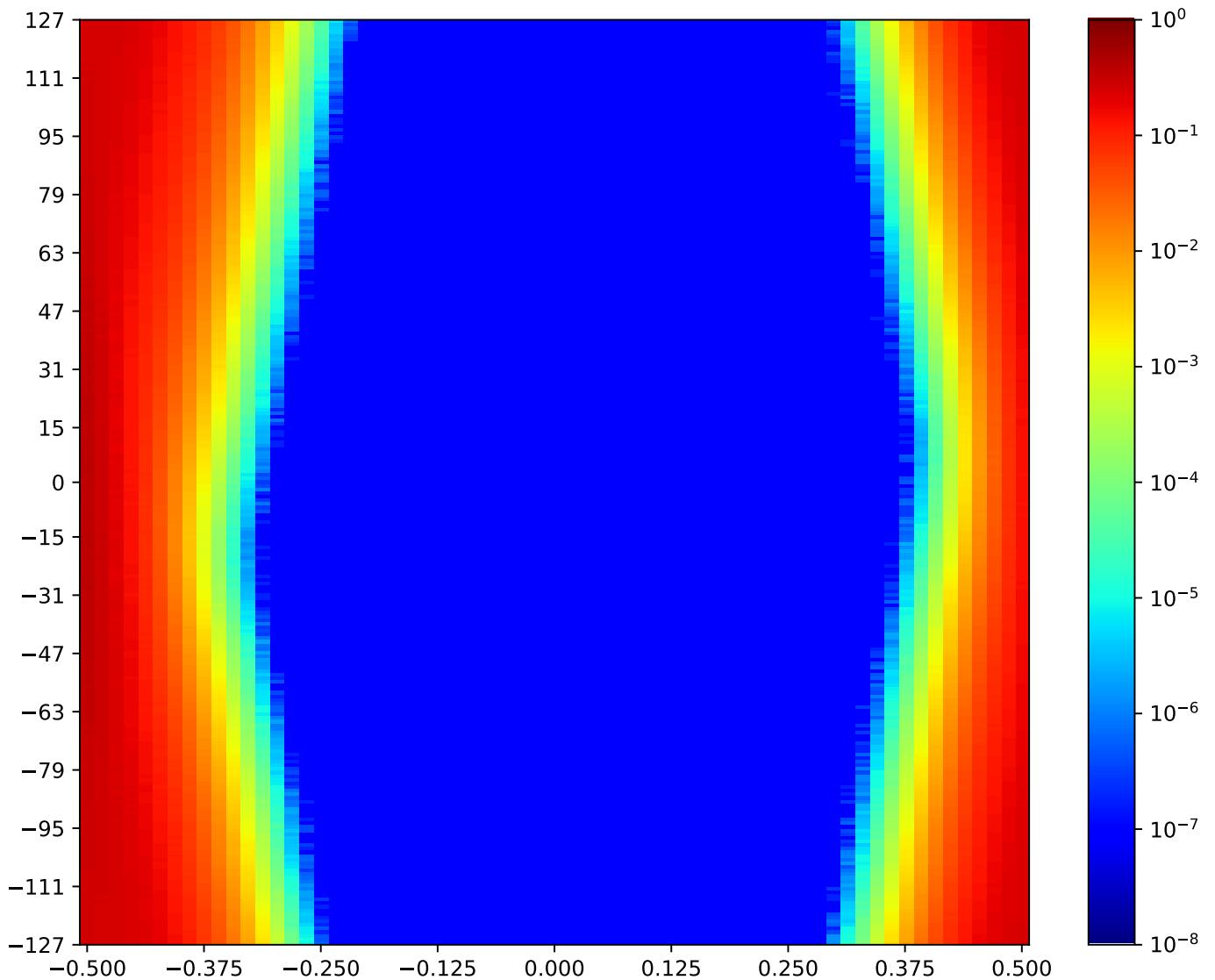


Figure 2.31: MSP\_C\_FPGA-TX3-03-RX7-03-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.5 MSP\_C\_FPGA-TX3-04-RX7-04-MSP\_A\_FPGA

Table 2.29: MSP\_C\_FPGA-TX3-04-RX7-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:26:47		2018-Jan-24 19:27:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10595	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

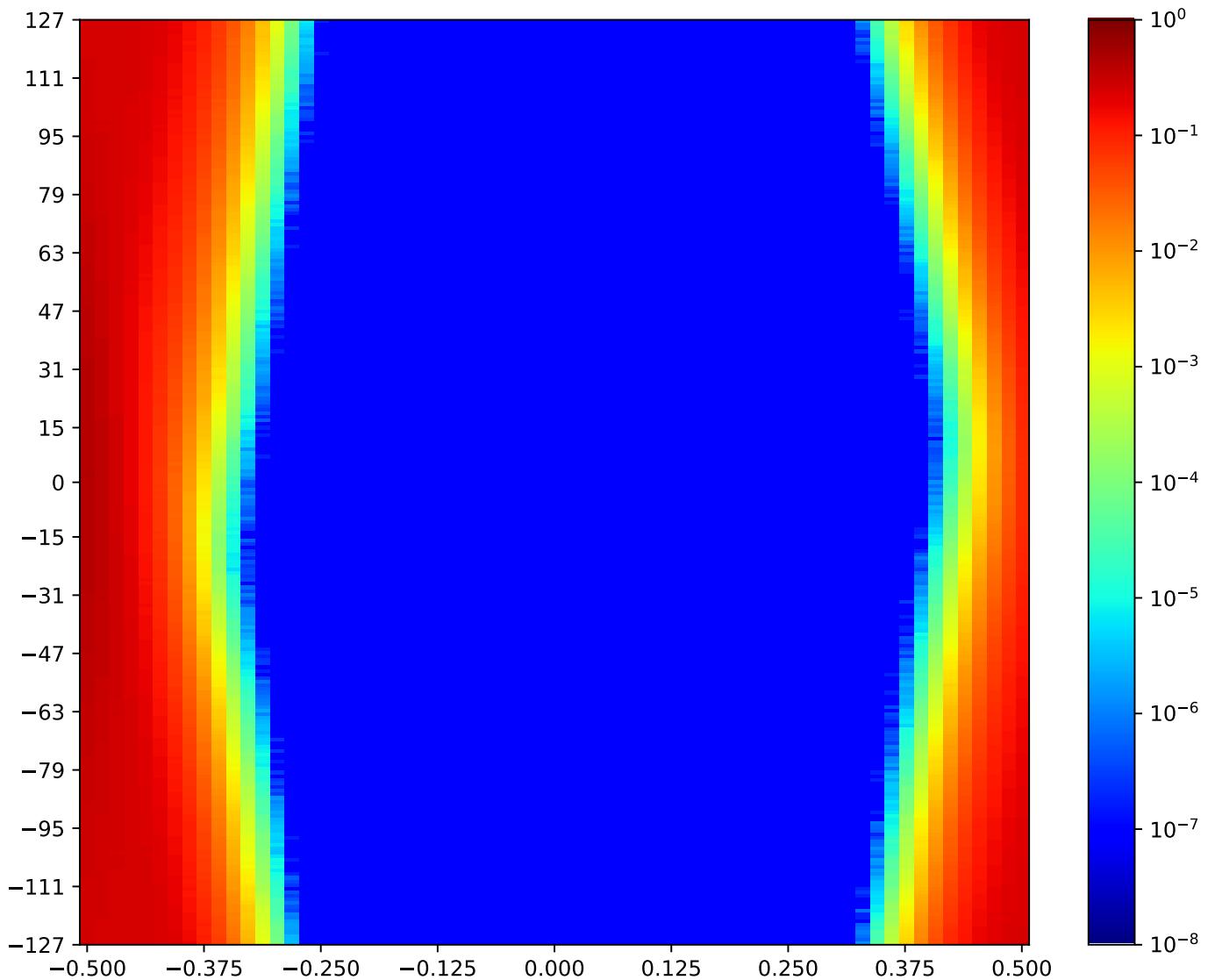


Figure 2.32: MSP\_C\_FPGA-TX3-04-RX7-04-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.6 MSP\_C\_FPGA-TX3-05-RX7-05-MSP\_A\_FPGA

Table 2.30: MSP\_C\_FPGA-TX3-05-RX7-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:22:16		2018-Jan-24 19:22:48	
Reset RX	OA	HO		HO (%)	
true	9424	42		64.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

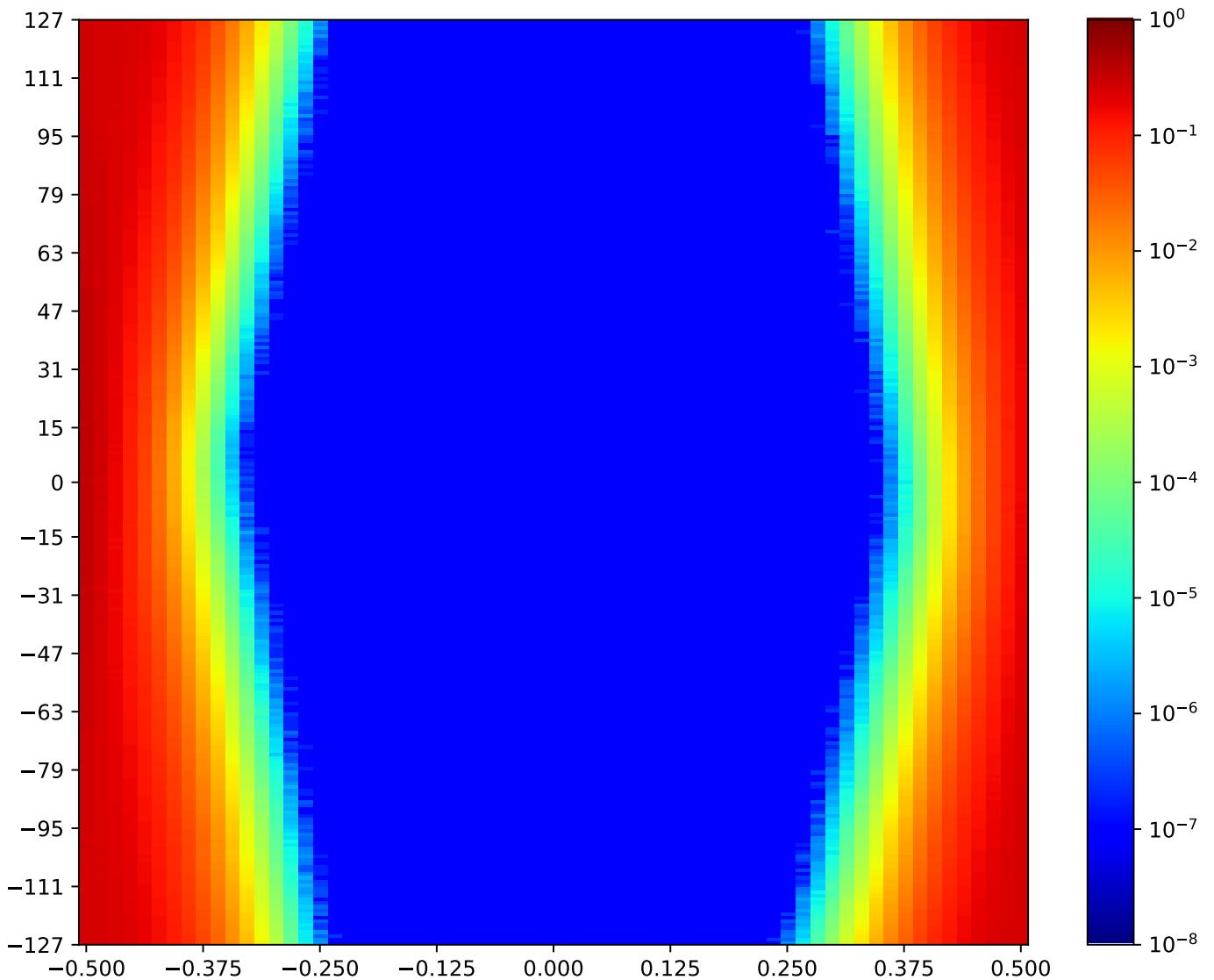


Figure 2.33: MSP\_C\_FPGA-TX3-05-RX7-05-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.7 MSP\_C\_FPGA-TX3-06-RX7-06-MSP\_A\_FPGA

Table 2.31: MSP\_C\_FPGA-TX3-06-RX7-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:27:49		2018-Jan-24 19:28:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10726	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

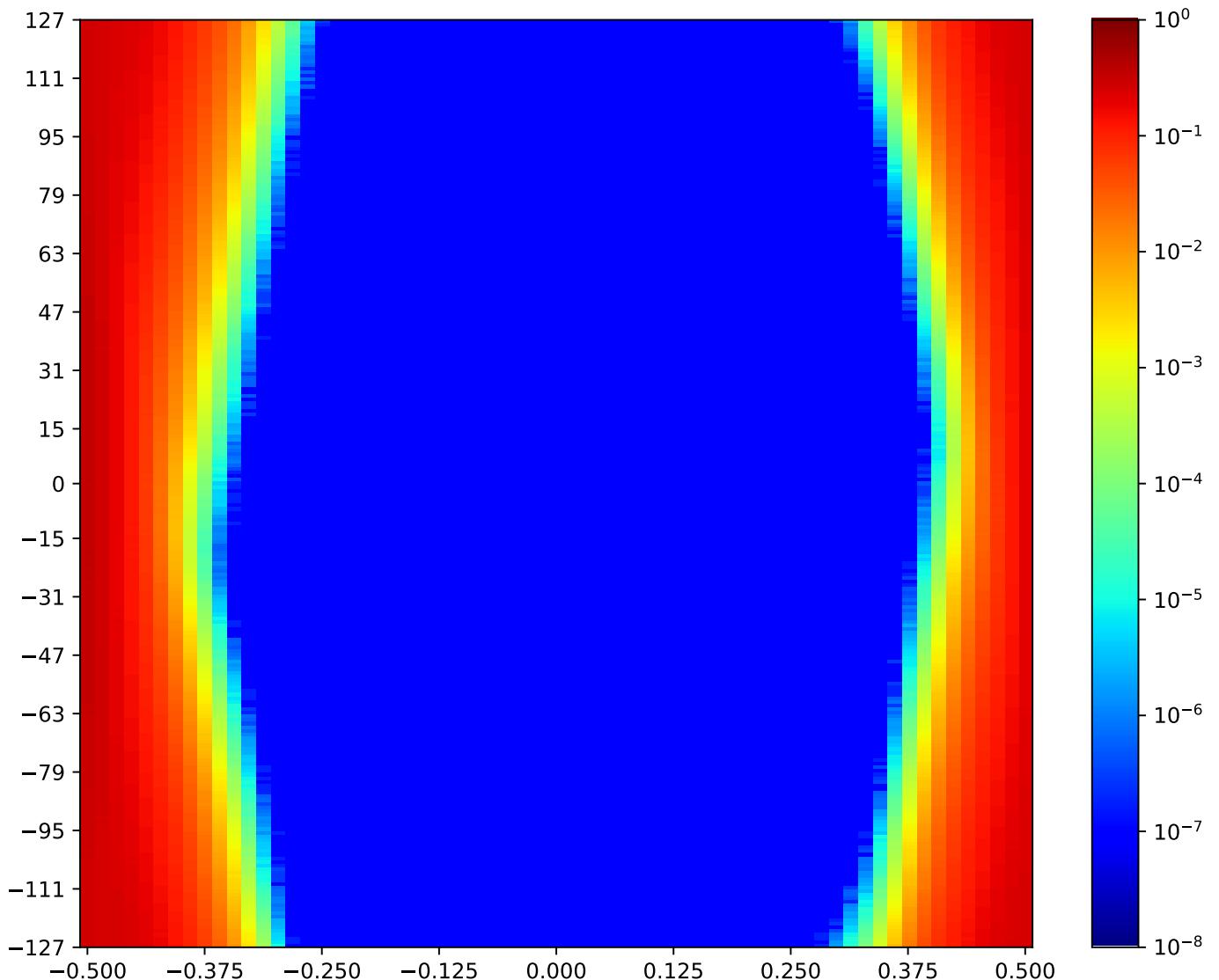


Figure 2.34: MSP\_C\_FPGA-TX3-06-RX7-06-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.8 MSP\_C\_FPGA-TX3-07-RX7-07-MSP\_A\_FPGA

Table 2.32: MSP\_C\_FPGA-TX3-07-RX7-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:23:18		2018-Jan-24 19:23:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9478	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

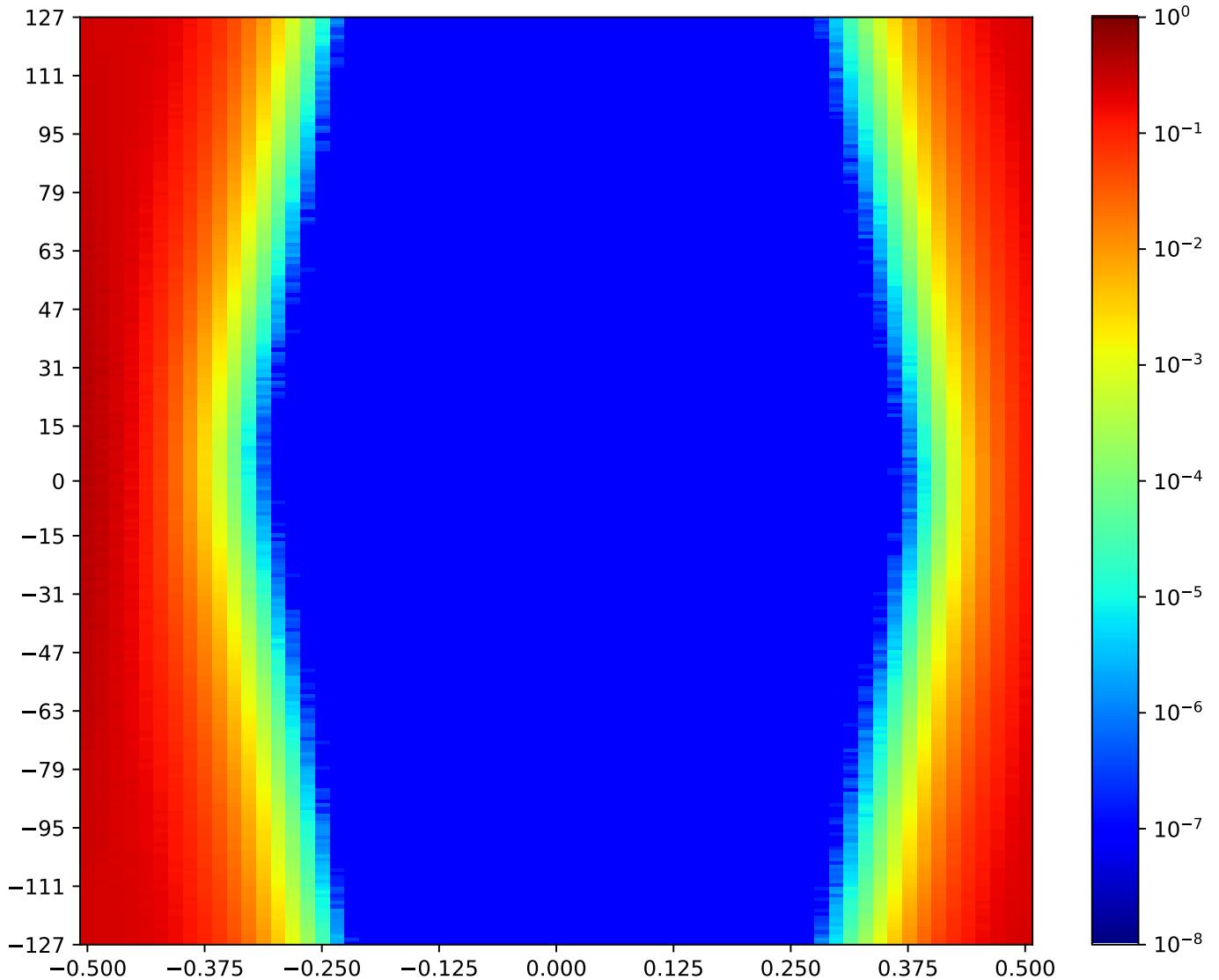


Figure 2.35: MSP\_C\_FPGA-TX3-07-RX7-07-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.9 MSP\_C\_FPGA-TX3-08-RX7-08-MSP\_A\_FPGA

Table 2.33: MSP\_C\_FPGA-TX3-08-RX7-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:27:18		2018-Jan-24 19:27:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11540	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

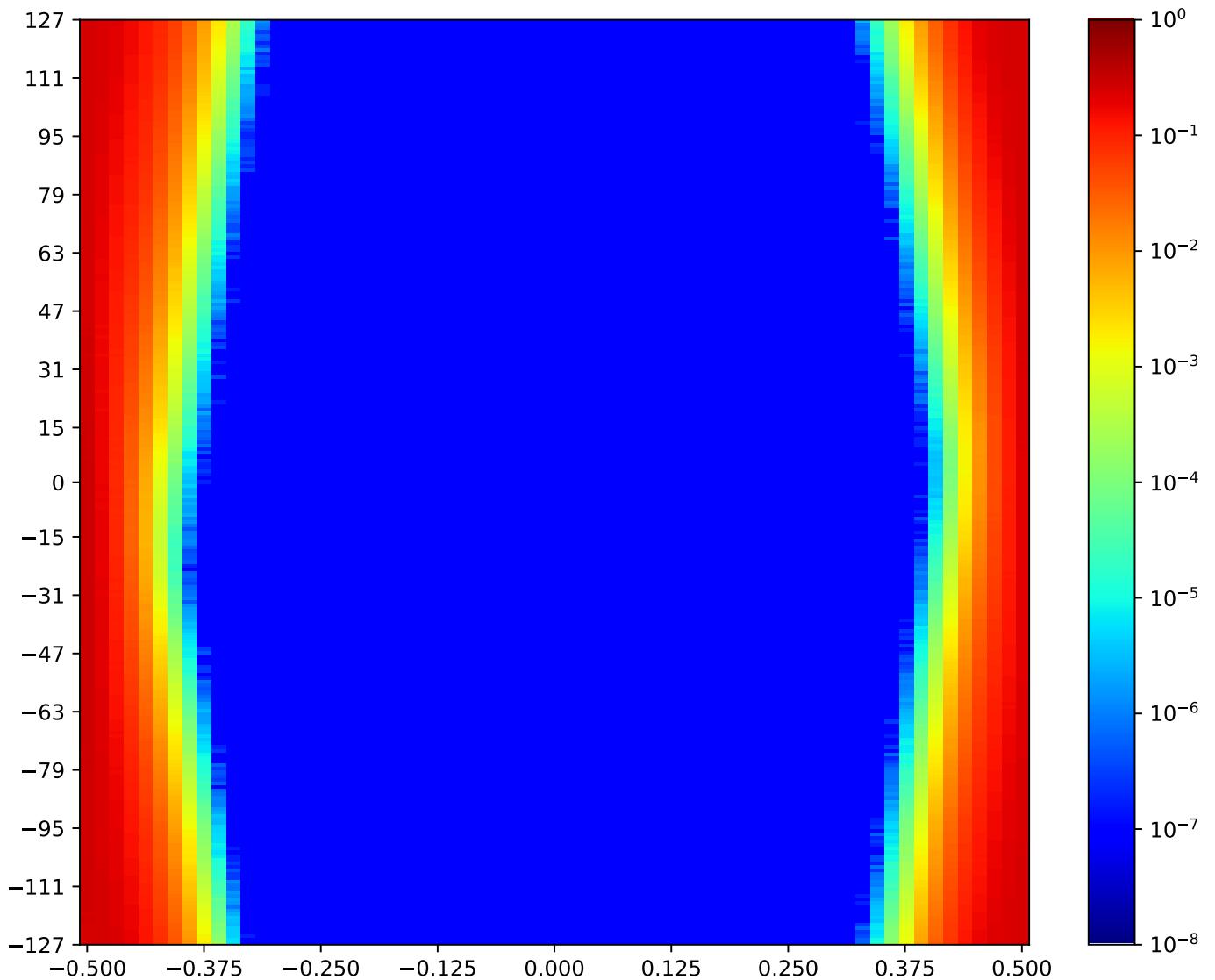


Figure 2.36: MSP\_C\_FPGA-TX3-08-RX7-08-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.10 MSP\_C\_FPGA-TX3-09-RX7-09-MSP\_A\_FPGA

Table 2.34: MSP\_C\_FPGA-TX3-09-RX7-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:24:19		2018-Jan-24 19:24:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10061	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

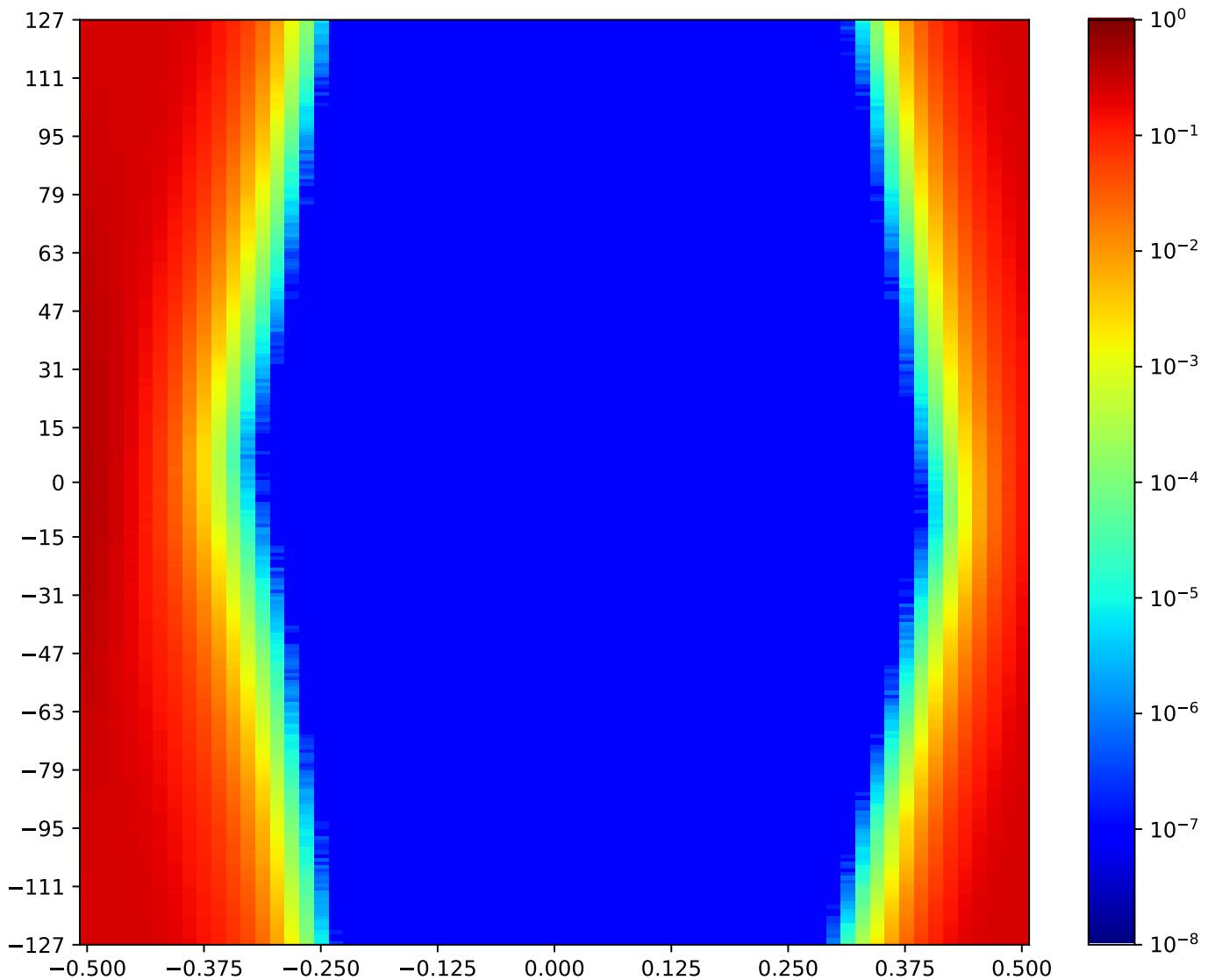


Figure 2.37: MSP\_C\_FPGA-TX3-09-RX7-09-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.11 MSP\_C\_FPGA-TX3-10-RX7-10-MSP\_A\_FPGA

Table 2.35: MSP\_C\_FPGA-TX3-10-RX7-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:26:18		2018-Jan-24 19:26:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9818	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

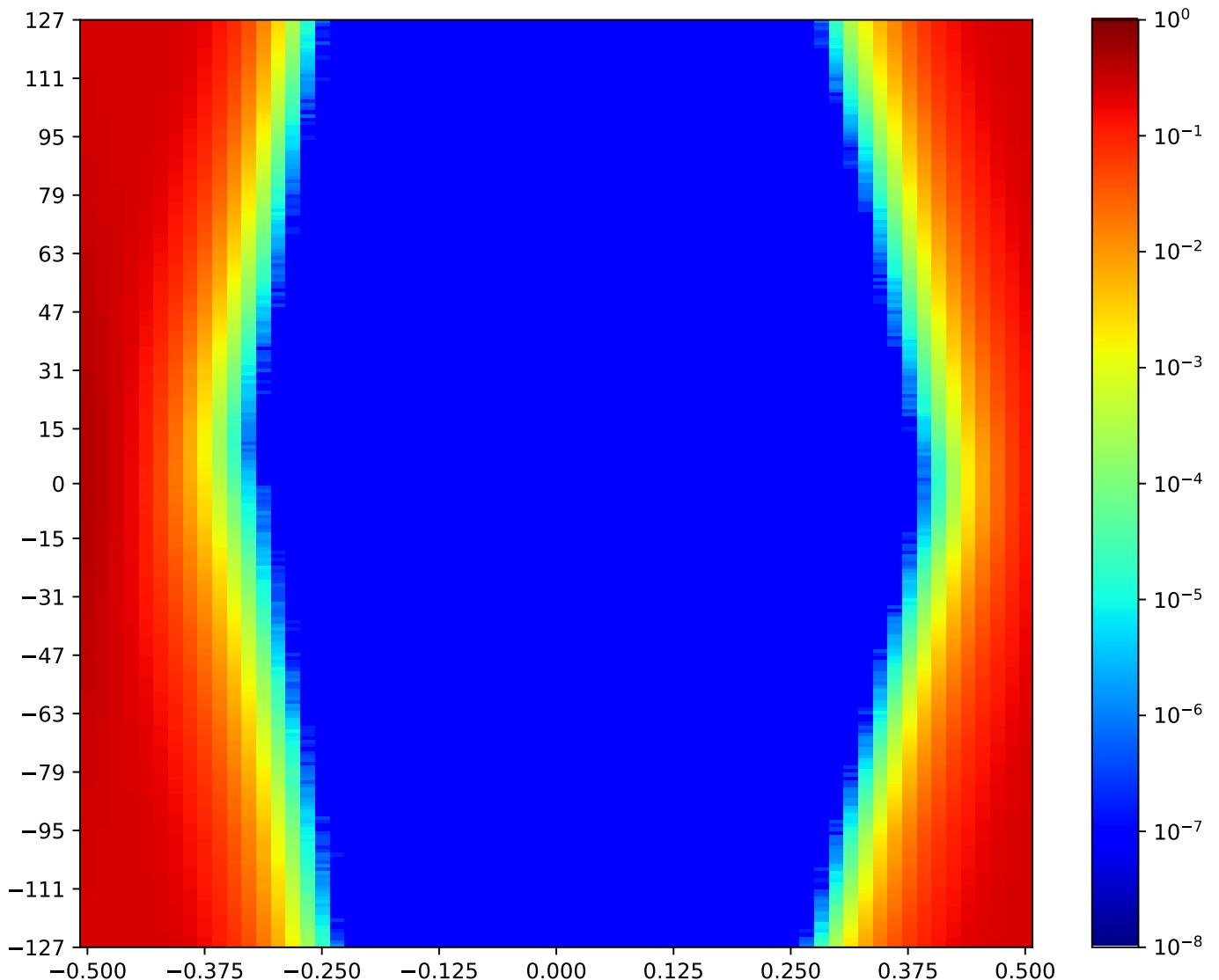


Figure 2.38: MSP\_C\_FPGA-TX3-10-RX7-10-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.3.12 MSP\_C\_FPGA-TX3-11-RX7-11-MSP\_A\_FPGA

Table 2.36: MSP\_C\_FPGA-TX3-11-RX7-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:25:48		2018-Jan-24 19:26:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9567	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

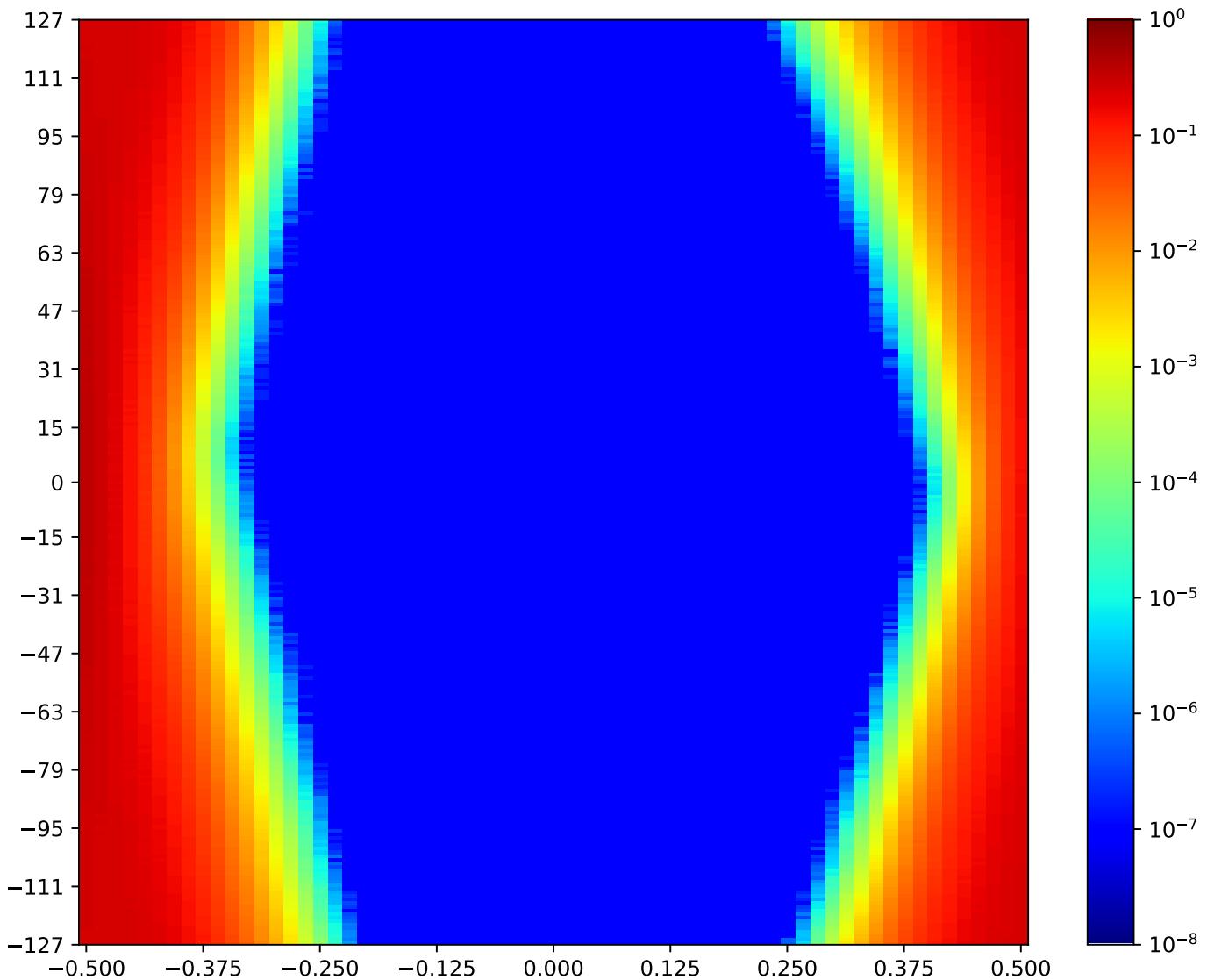


Figure 2.39: MSP\_C\_FPGA-TX3-11-RX7-11-MSP\_A\_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.4 MSP\_C TX4 MSP\_A RX6 Minipod Loopback

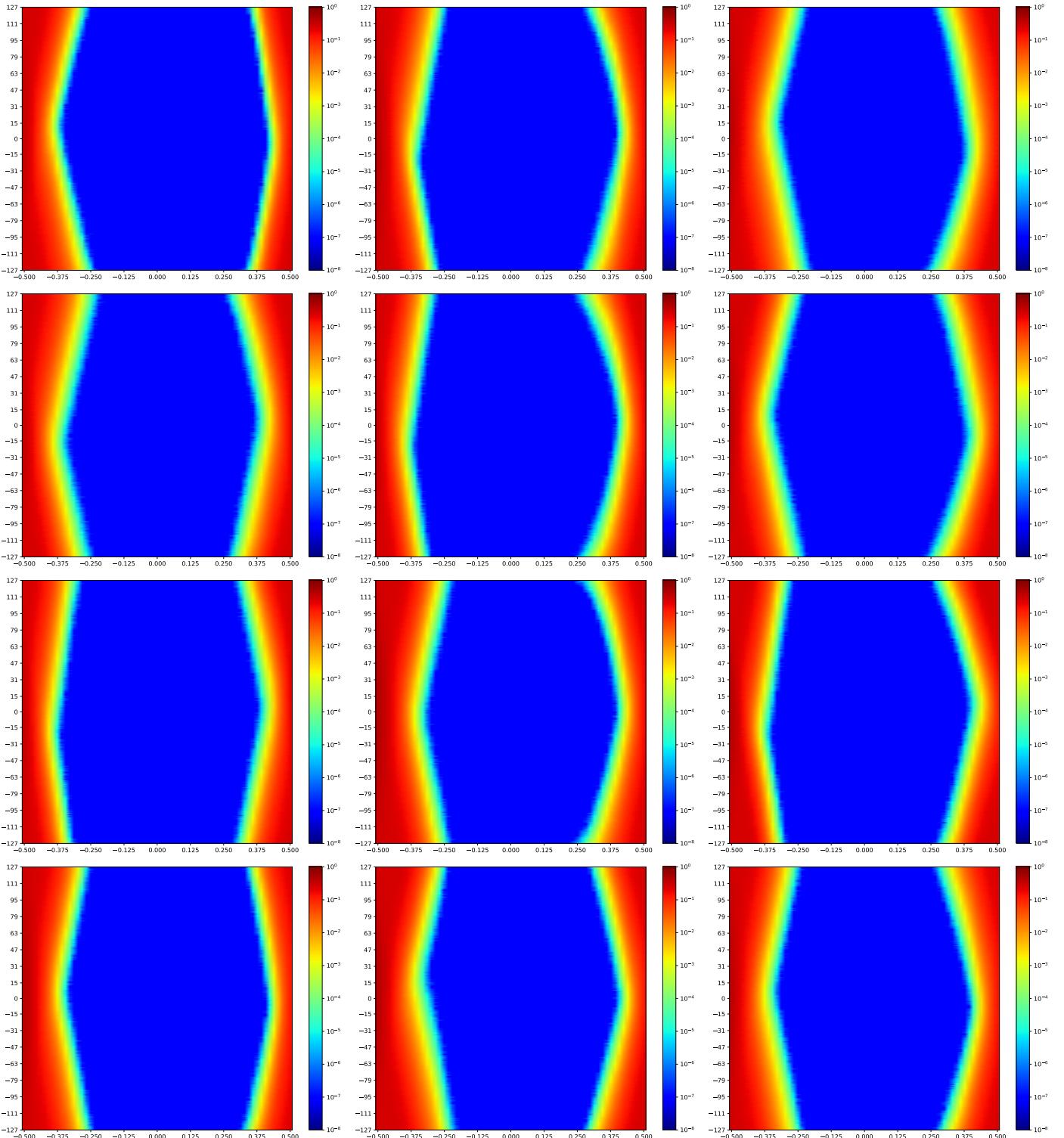


Figure 2.40: MSP\_C TX4 MSP\_A RX6 Minipod Loopback

A cross-reference to Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.53.

### 2.4.1 MSP\_C\_FPGA-TX4-00-RX6-00-MSP\_A\_FPGA

Table 2.37: MSP\_C\_FPGA-TX4-00-RX6-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:29:49		2018-Jan-24 19:30:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10923	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

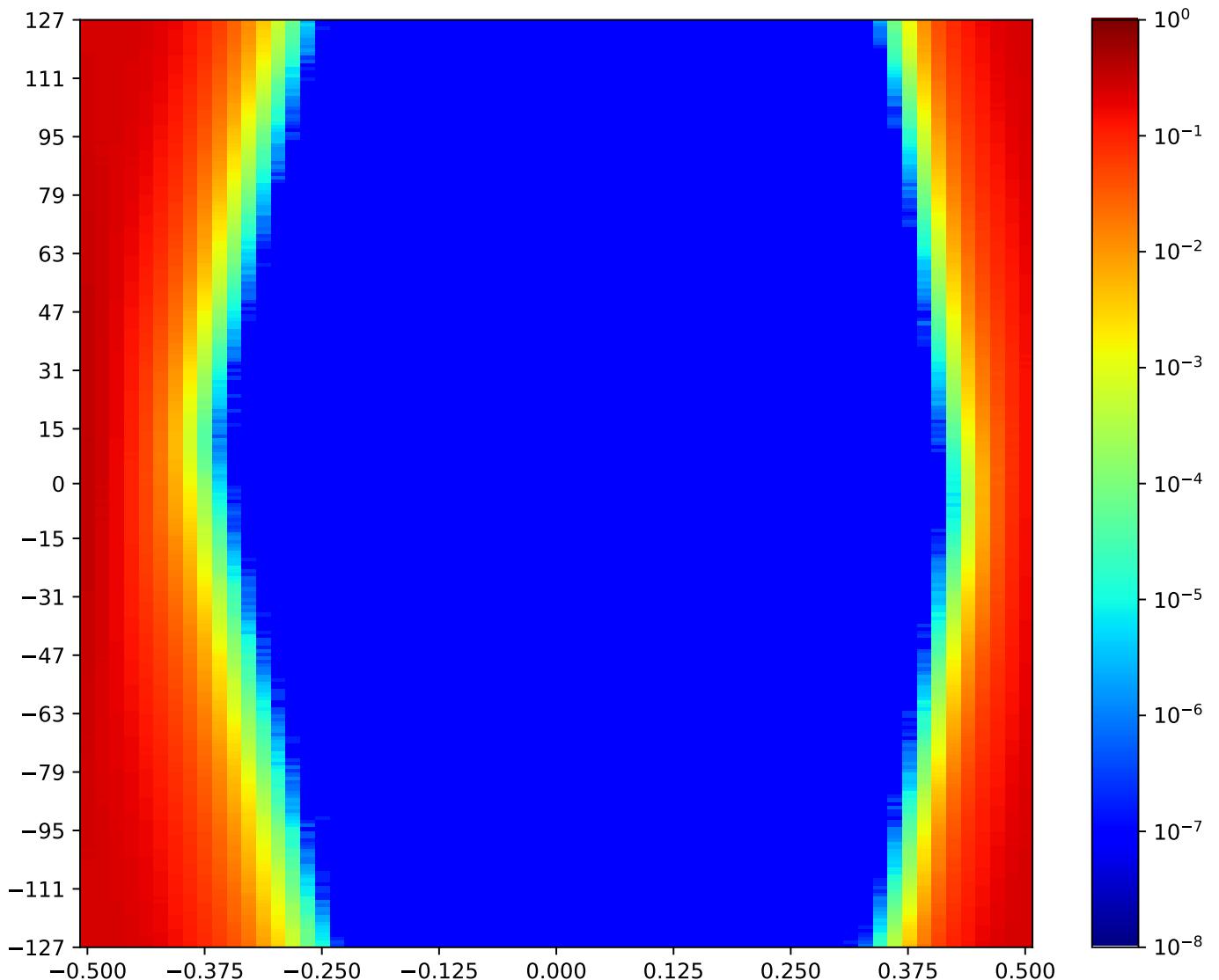


Figure 2.41: MSP\_C\_FPGA-TX4-00-RX6-00-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.4.2 MSP\_C\_FPGA-TX4-01-RX6-01-MSP\_A\_FPGA

Table 2.38: MSP\_C\_FPGA-TX4-01-RX6-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:28:49		2018-Jan-24 19:29:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10103	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

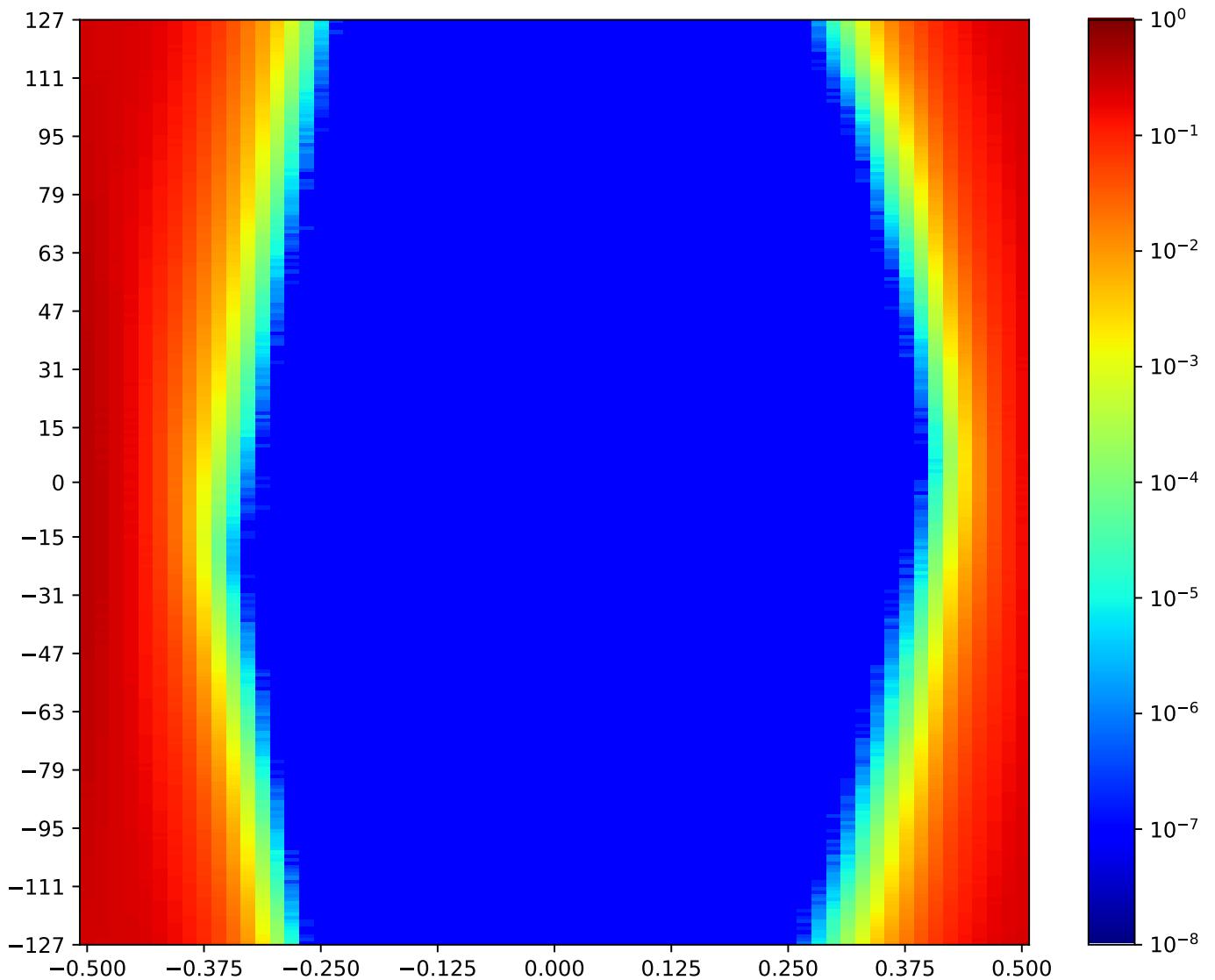


Figure 2.42: MSP\_C\_FPGA-TX4-01-RX6-01-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.4.3 MSP\_C\_FPGA-TX4-02-RX6-02-MSP\_A\_FPGA

Table 2.39: MSP\_C\_FPGA-TX4-02-RX6-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:31:20		2018-Jan-24 19:31:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9058	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

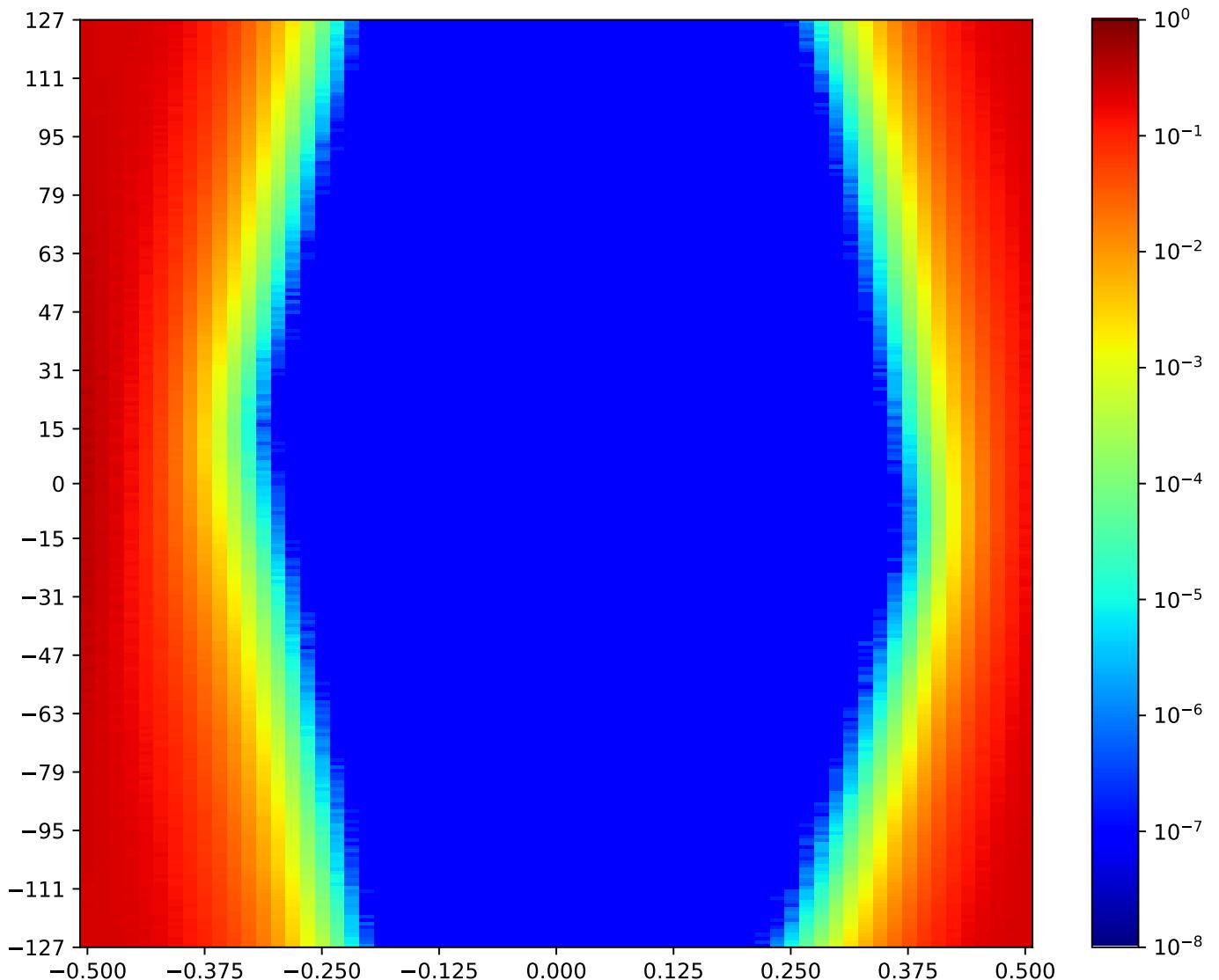


Figure 2.43: MSP\_C\_FPGA-TX4-02-RX6-02-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

#### 2.4.4 MSP\_C\_FPGA-TX4-03-RX6-03-MSP\_A\_FPGA

Table 2.40: MSP\_C\_FPGA-TX4-03-RX6-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:28:19		2018-Jan-24 19:28:49	
Reset RX	OA	HO		HO (%)	
true	9501	43		66.15%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

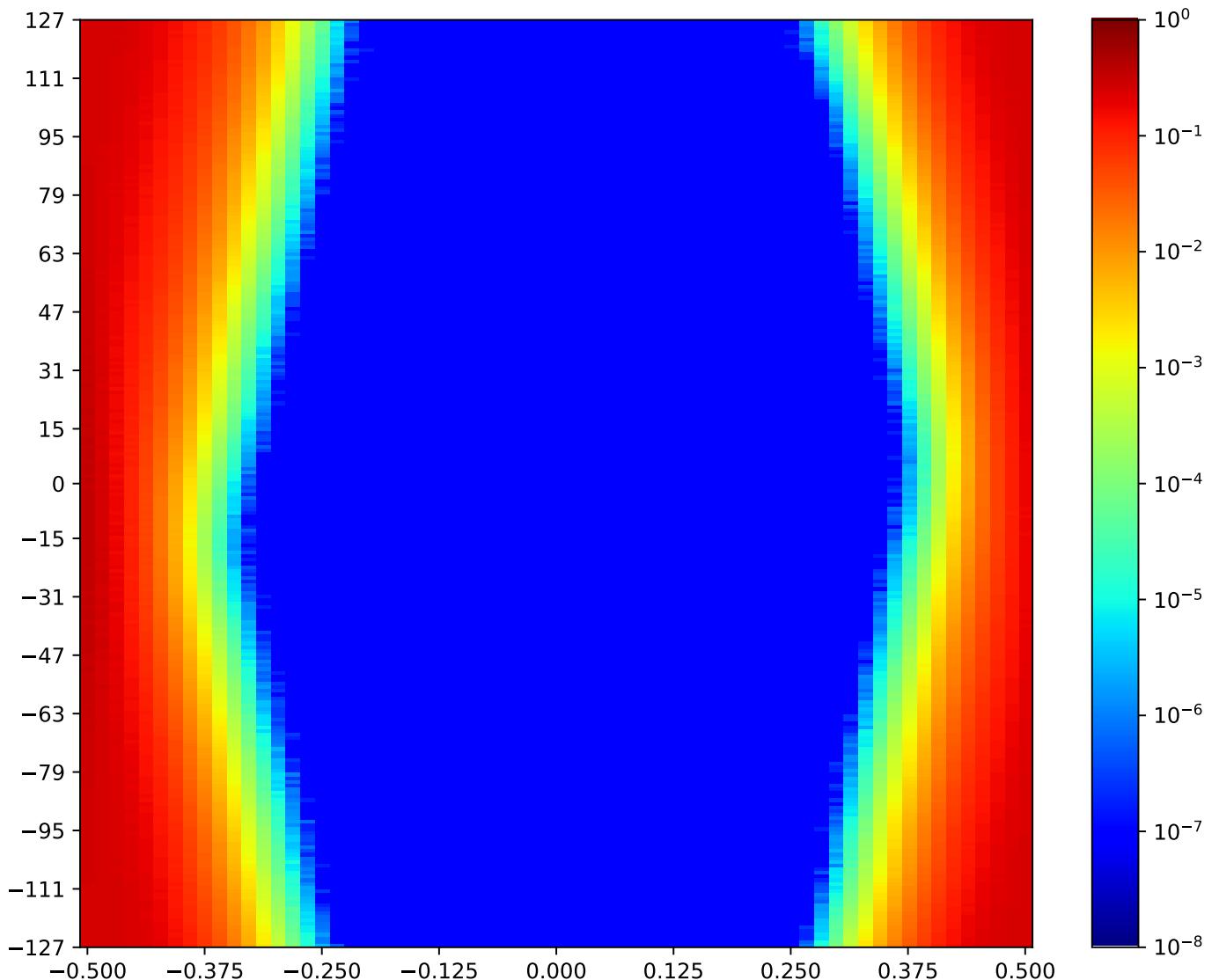


Figure 2.44: MSP\_C\_FPGA-TX4-03-RX6-03-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.4.5 MSP\_C\_FPGA-TX4-04-RX6-04-MSP\_A\_FPGA

Table 2.41: MSP\_C\_FPGA-TX4-04-RX6-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:32:49		2018-Jan-24 19:33:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10478	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

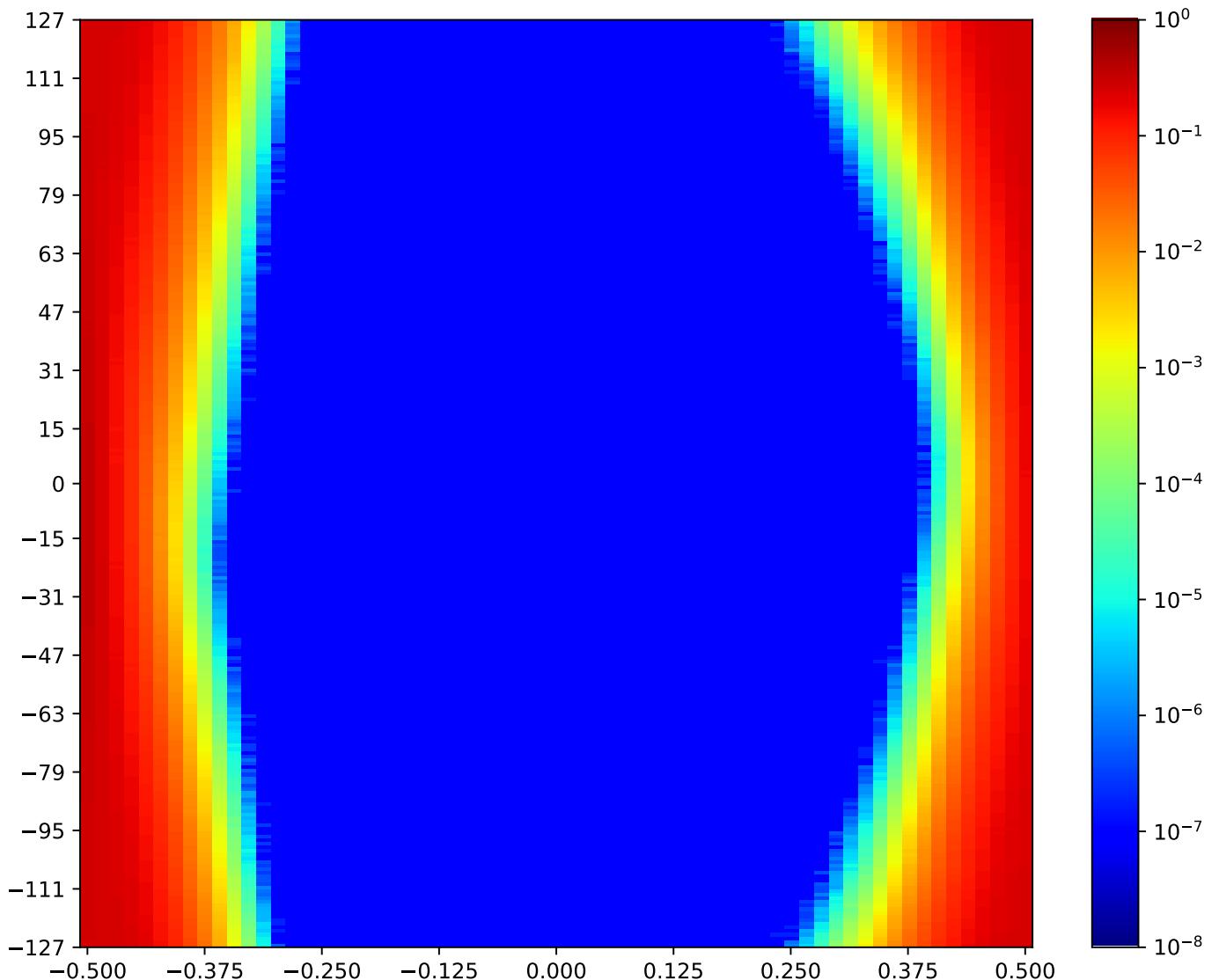


Figure 2.45: MSP\_C\_FPGA-TX4-04-RX6-04-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.4.6 MSP\_C\_FPGA-TX4-05-RX6-05-MSP\_A\_FPGA

Table 2.42: MSP\_C\_FPGA-TX4-05-RX6-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:29:20		2018-Jan-24 19:29:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9425	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

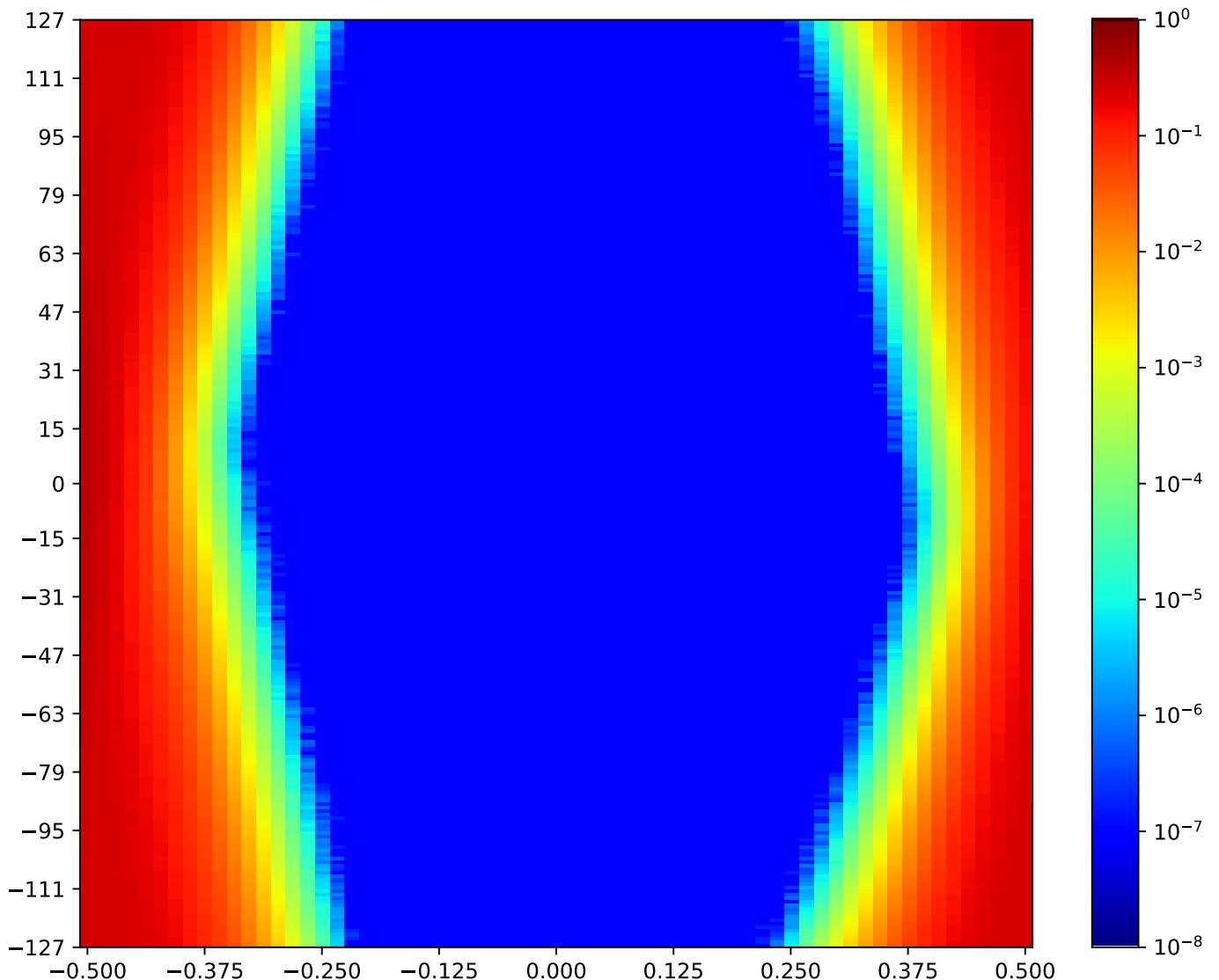


Figure 2.46: MSP\_C\_FPGA-TX4-05-RX6-05-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

#### 2.4.7 MSP\_C\_FPGA-TX4-06-RX6-06-MSP\_A\_FPGA

Table 2.43: MSP\_C\_FPGA-TX4-06-RX6-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:33:49		2018-Jan-24 19:34:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10695	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

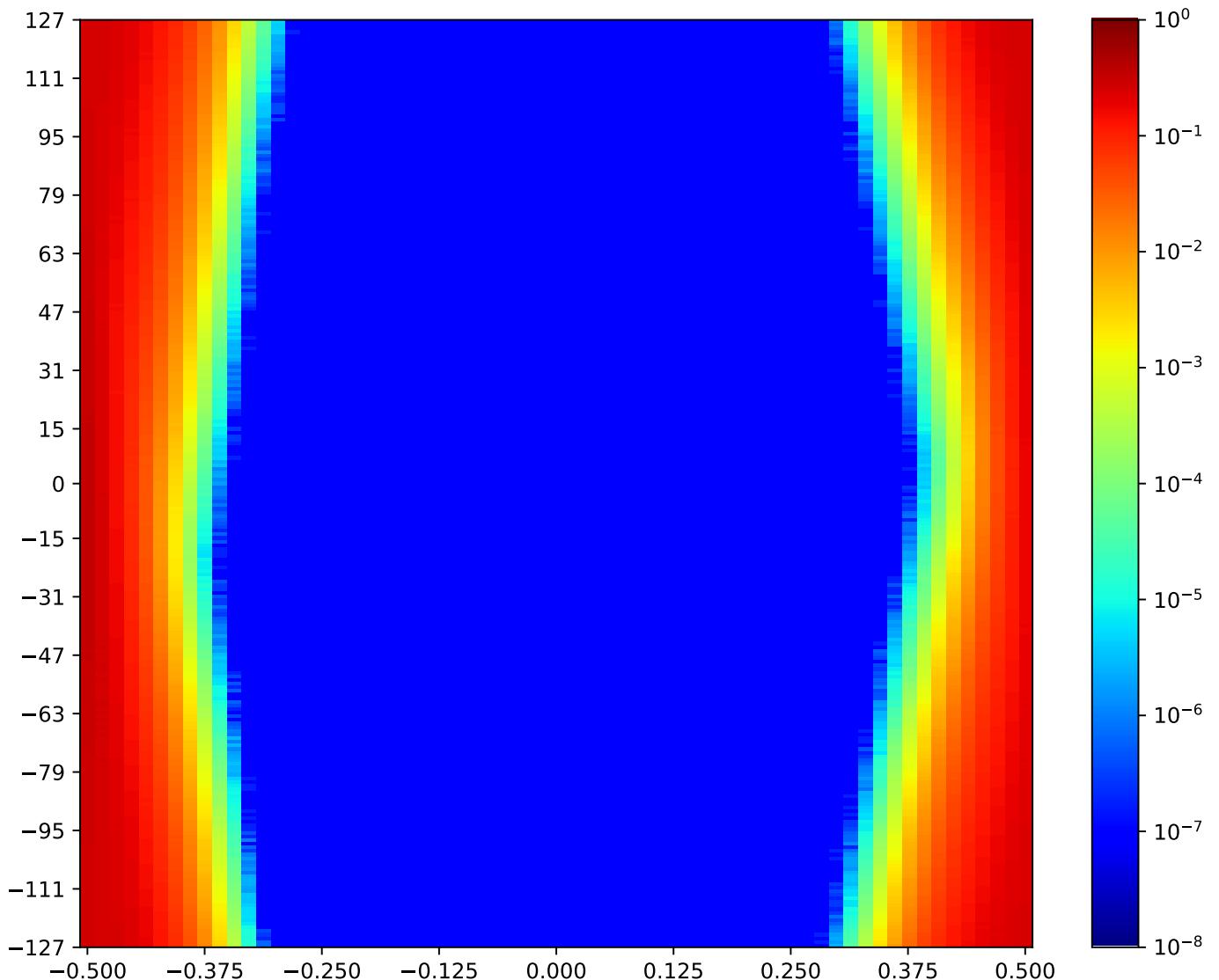


Figure 2.47: MSP\_C\_FPGA-TX4-06-RX6-06-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.4.8 MSP\_C\_FPGA-TX4-07-RX6-07-MSP\_A\_FPGA

Table 2.44: MSP\_C\_FPGA-TX4-07-RX6-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:30:20		2018-Jan-24 19:30:50	
Reset RX	OA	HO		HO (%)	
true	9602	43		66.15%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

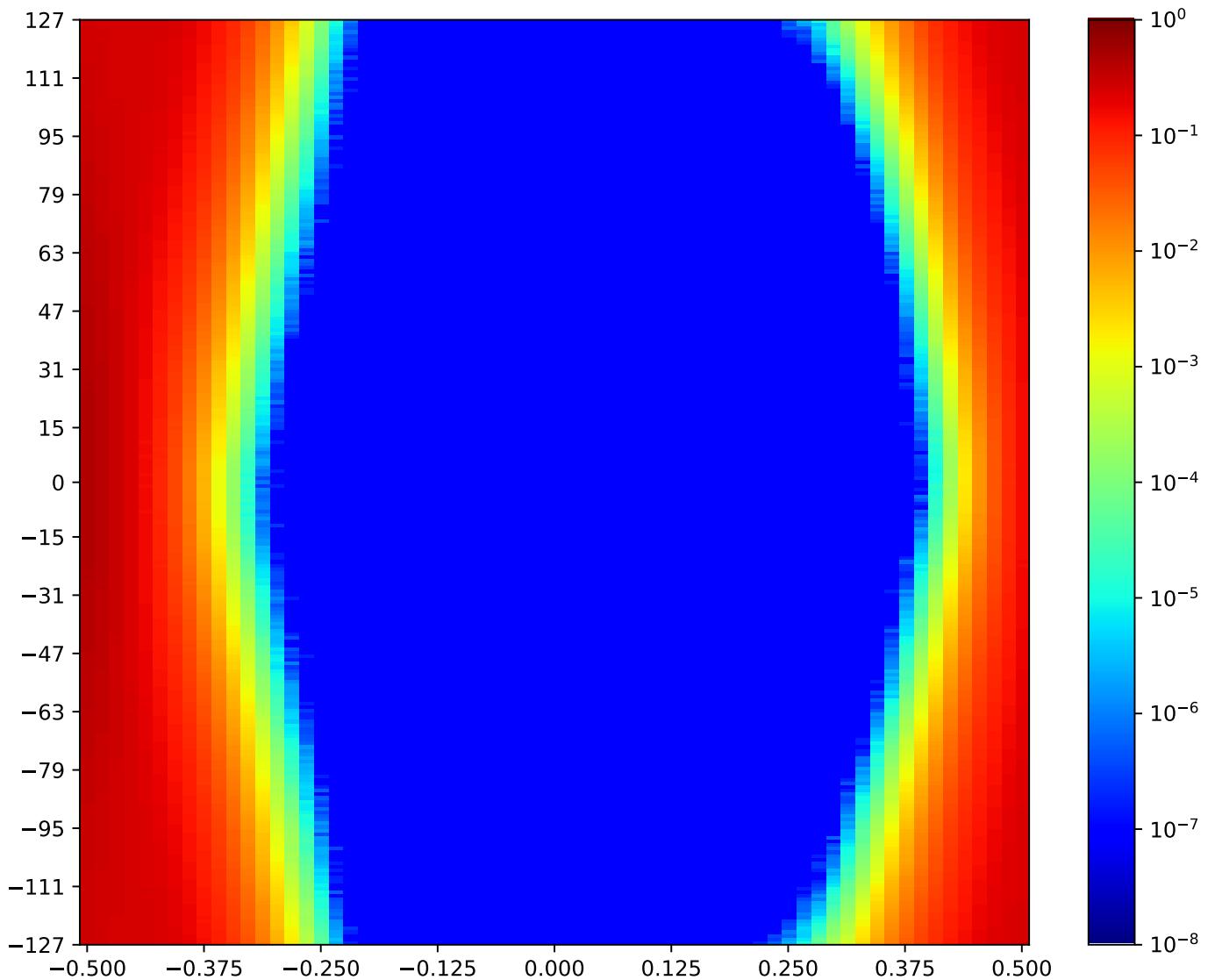


Figure 2.48: MSP\_C\_FPGA-TX4-07-RX6-07-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.4.9 MSP\_C\_FPGA-TX4-08-RX6-08-MSP\_A\_FPGA

Table 2.45: MSP\_C\_FPGA-TX4-08-RX6-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:33:19		2018-Jan-24 19:33:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10311	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

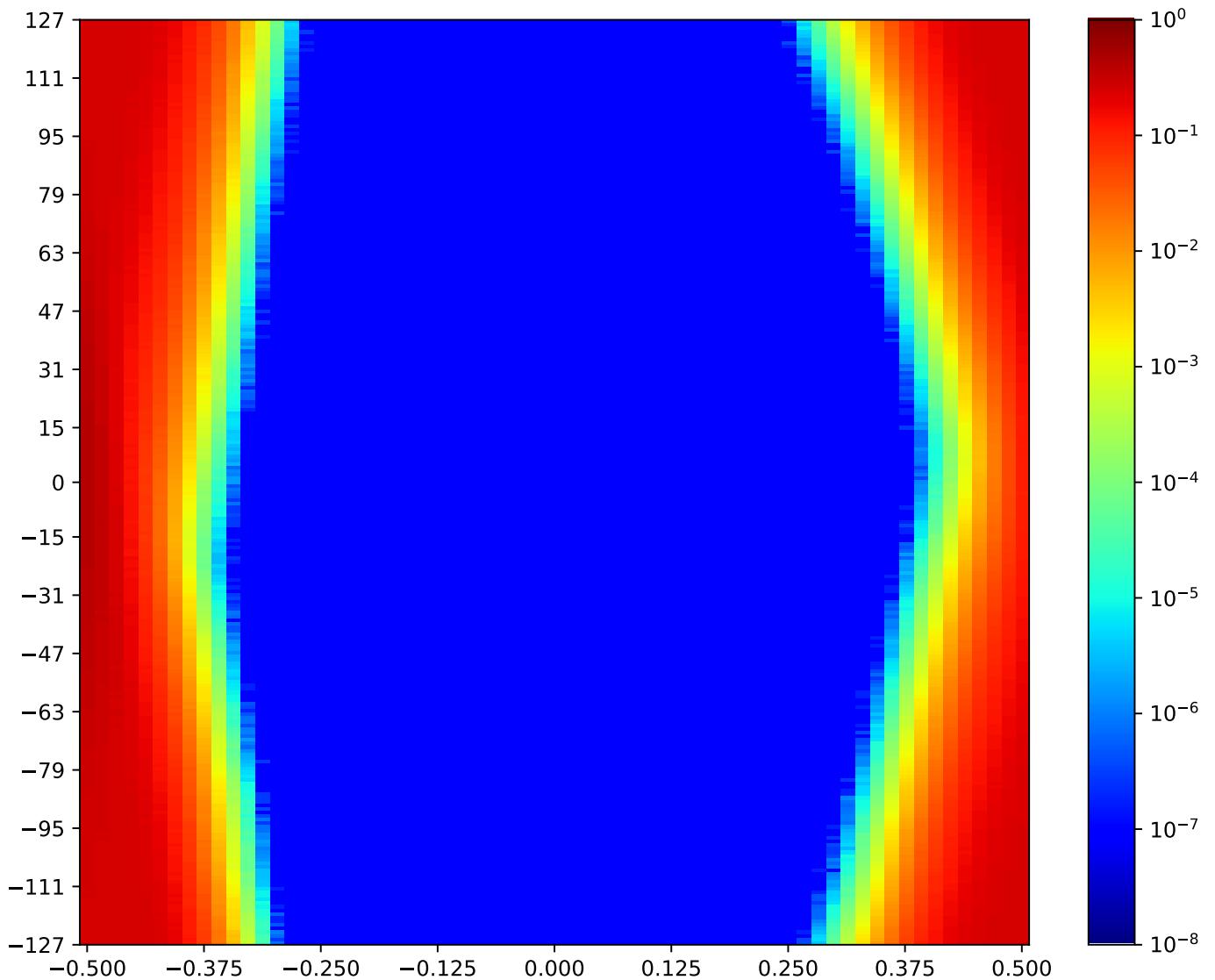


Figure 2.49: MSP\_C\_FPGA-TX4-08-RX6-08-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

#### 2.4.10 MSP\_C\_FPGA-TX4-09-RX6-09-MSP\_A\_FPGA

Table 2.46: MSP\_C\_FPGA-TX4-09-RX6-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:30:50		2018-Jan-24 19:31:20	
Reset RX	OA	HO		HO (%)	
true	10578	46		70.77%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

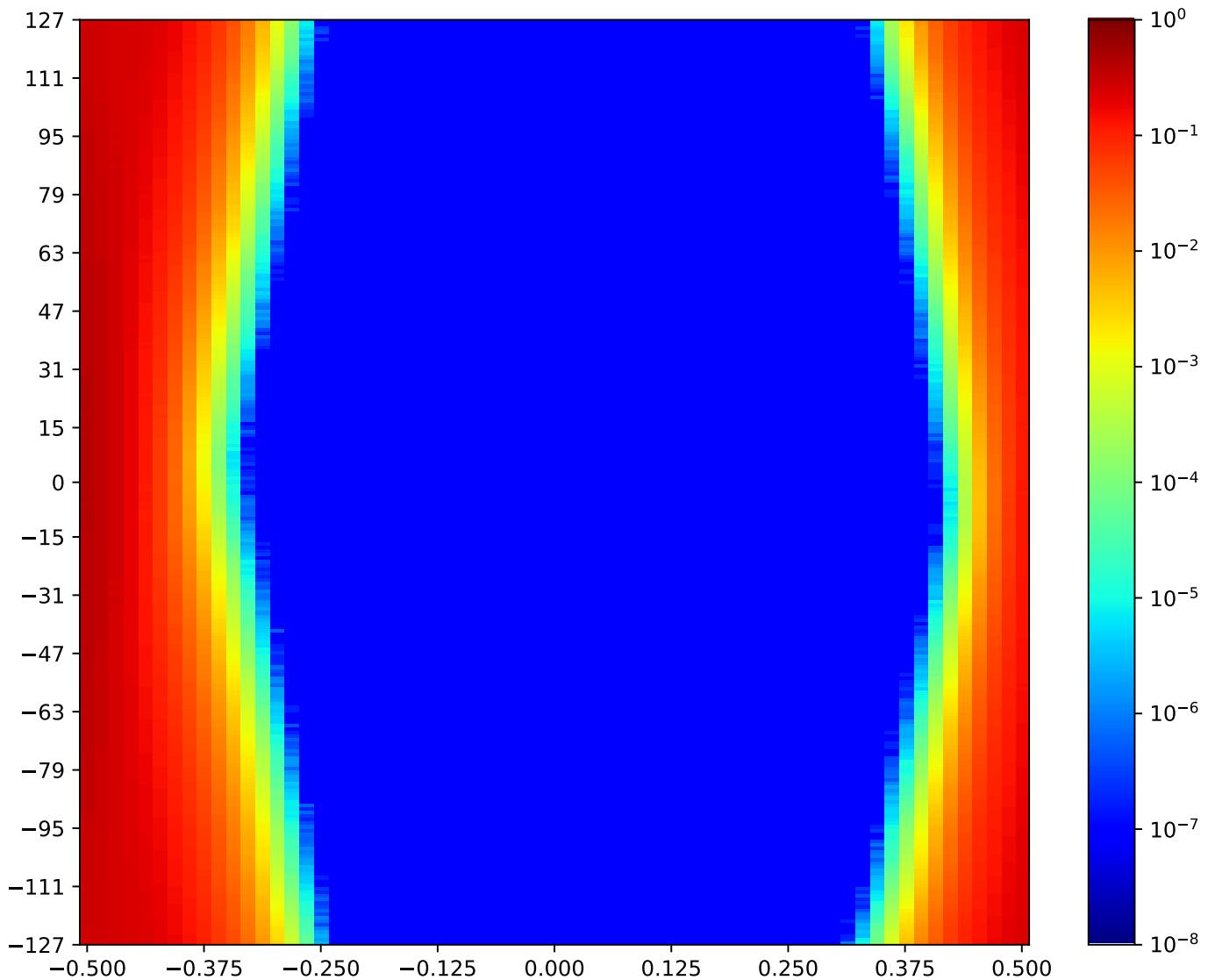


Figure 2.50: MSP\_C\_FPGA-TX4-09-RX6-09-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.4.11 MSP\_C\_FPGA-TX4-10-RX6-10-MSP\_A\_FPGA

Table 2.47: MSP\_C\_FPGA-TX4-10-RX6-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:32:19		2018-Jan-24 19:32:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9612	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

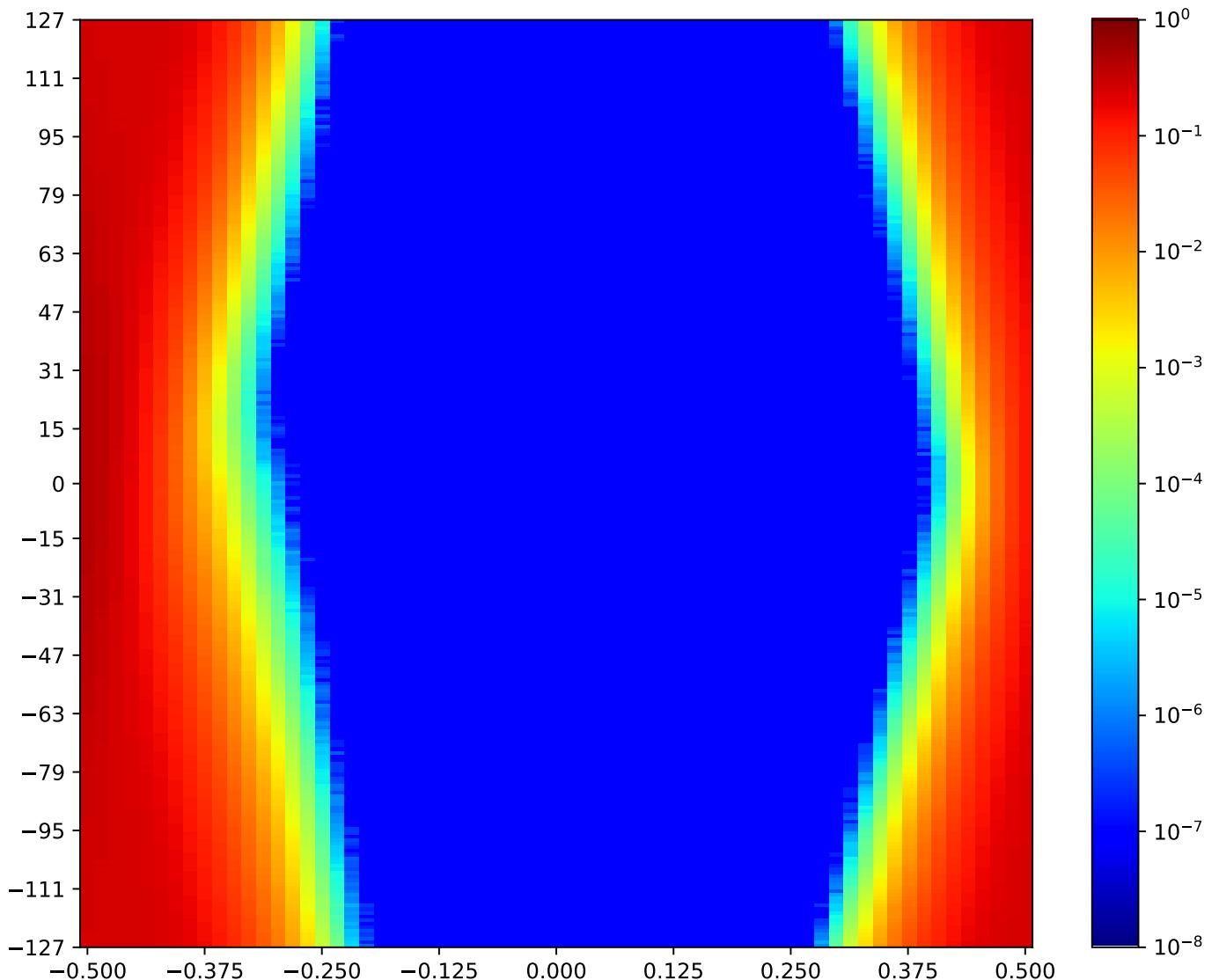


Figure 2.51: MSP\_C\_FPGA-TX4-10-RX6-10-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

#### 2.4.12 MSP\_C\_FPGA-TX4-11-RX6-11-MSP\_A\_FPGA

Table 2.48: MSP\_C\_FPGA-TX4-11-RX6-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:31:50		2018-Jan-24 19:32:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9797	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

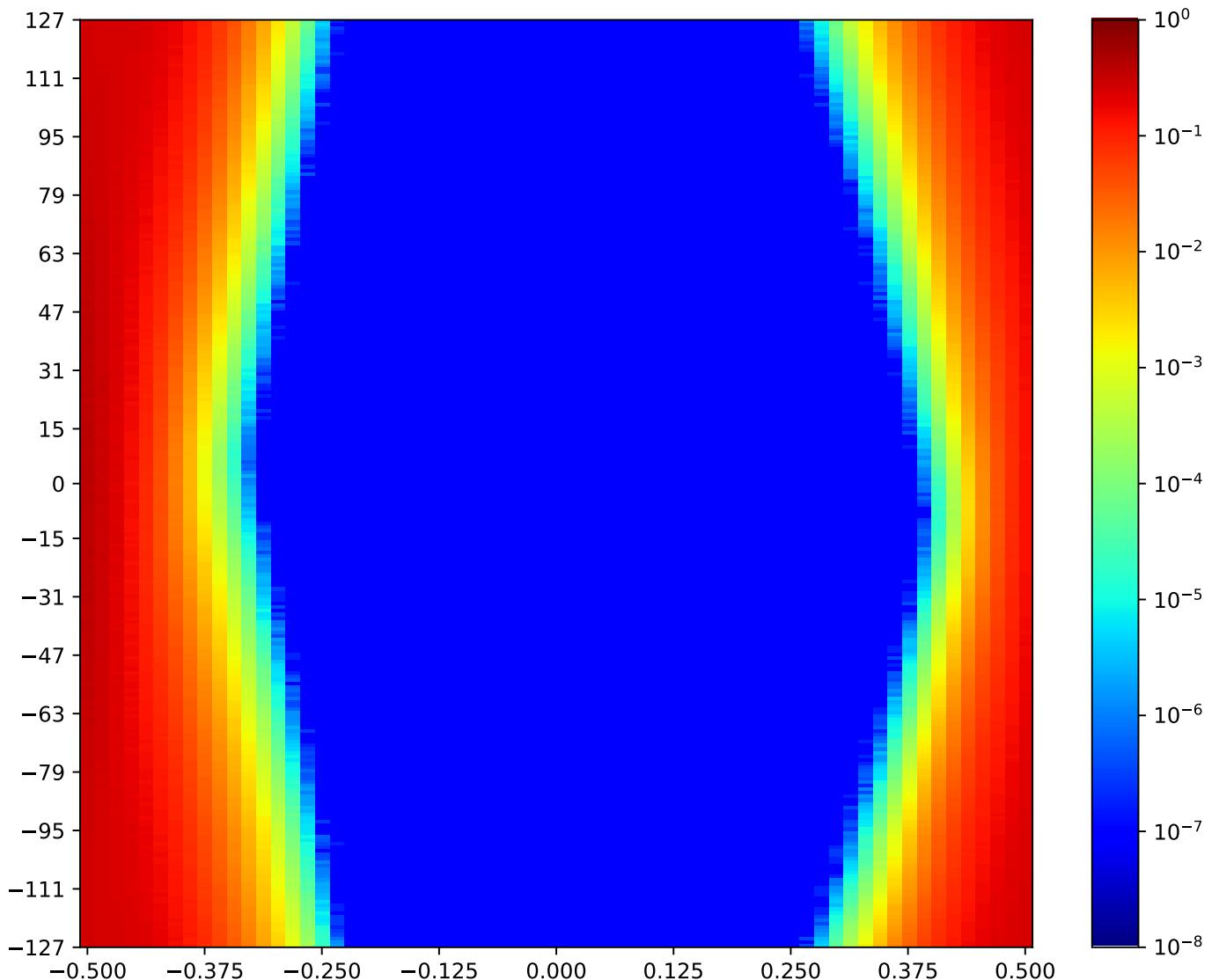


Figure 2.52: MSP\_C\_FPGA-TX4-11-RX6-11-MSP\_A\_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.5 Partial TRP TX5 MSP\_A RX5 Minipod Loopback

A cross-reference to Figure 2.53. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

Next summary Figure 2.62.

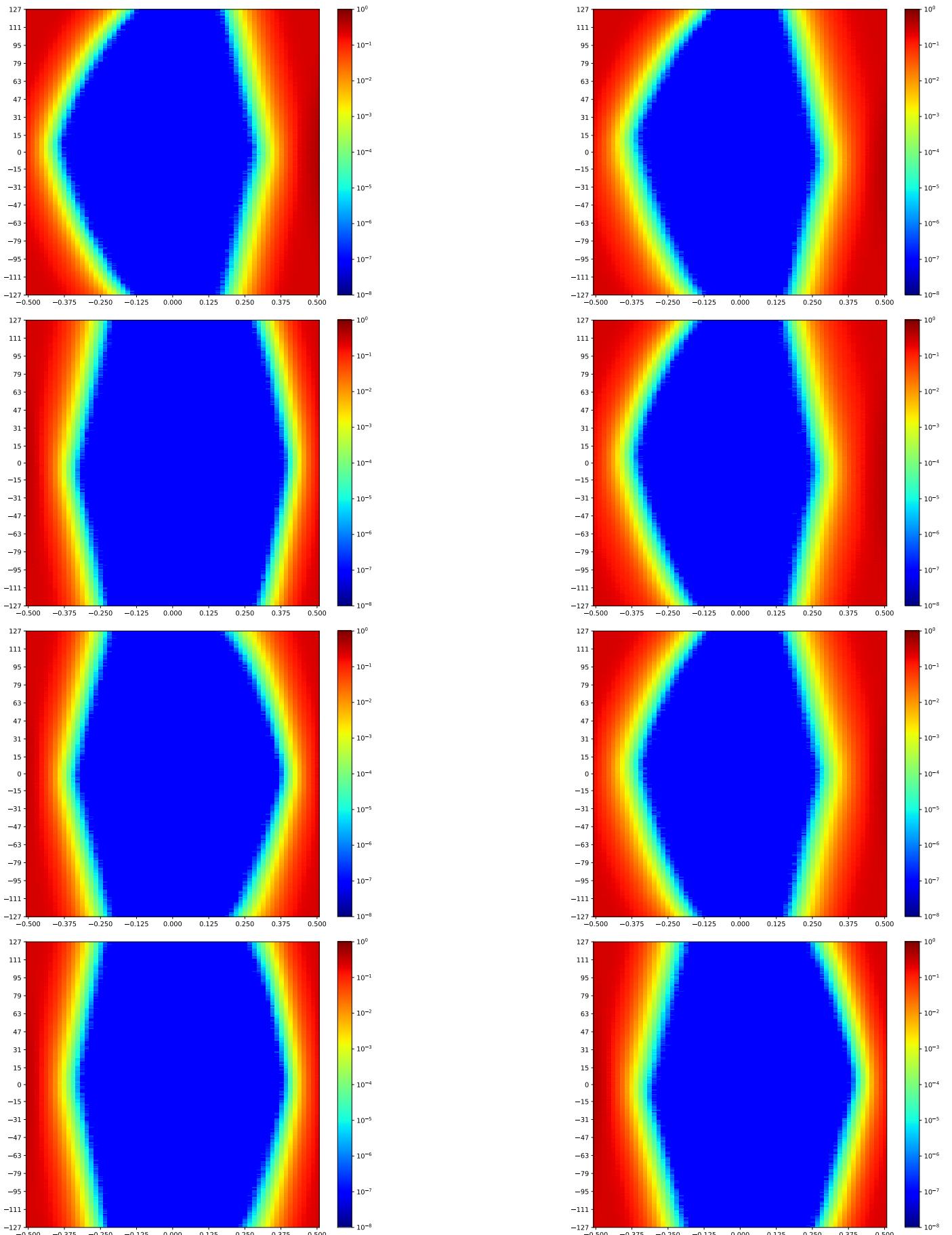


Figure 2.53: Partial TRP TX5 MSP\_A RX5 Minipod Loopback

### 2.5.1 TRP\_FPGA-TX5-00-RX5-00-MSP\_A\_FPGA

Table 2.49: TRP\_FPGA-TX5-00-RX5-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:35:48		2018-Jan-24 19:36:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7803	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

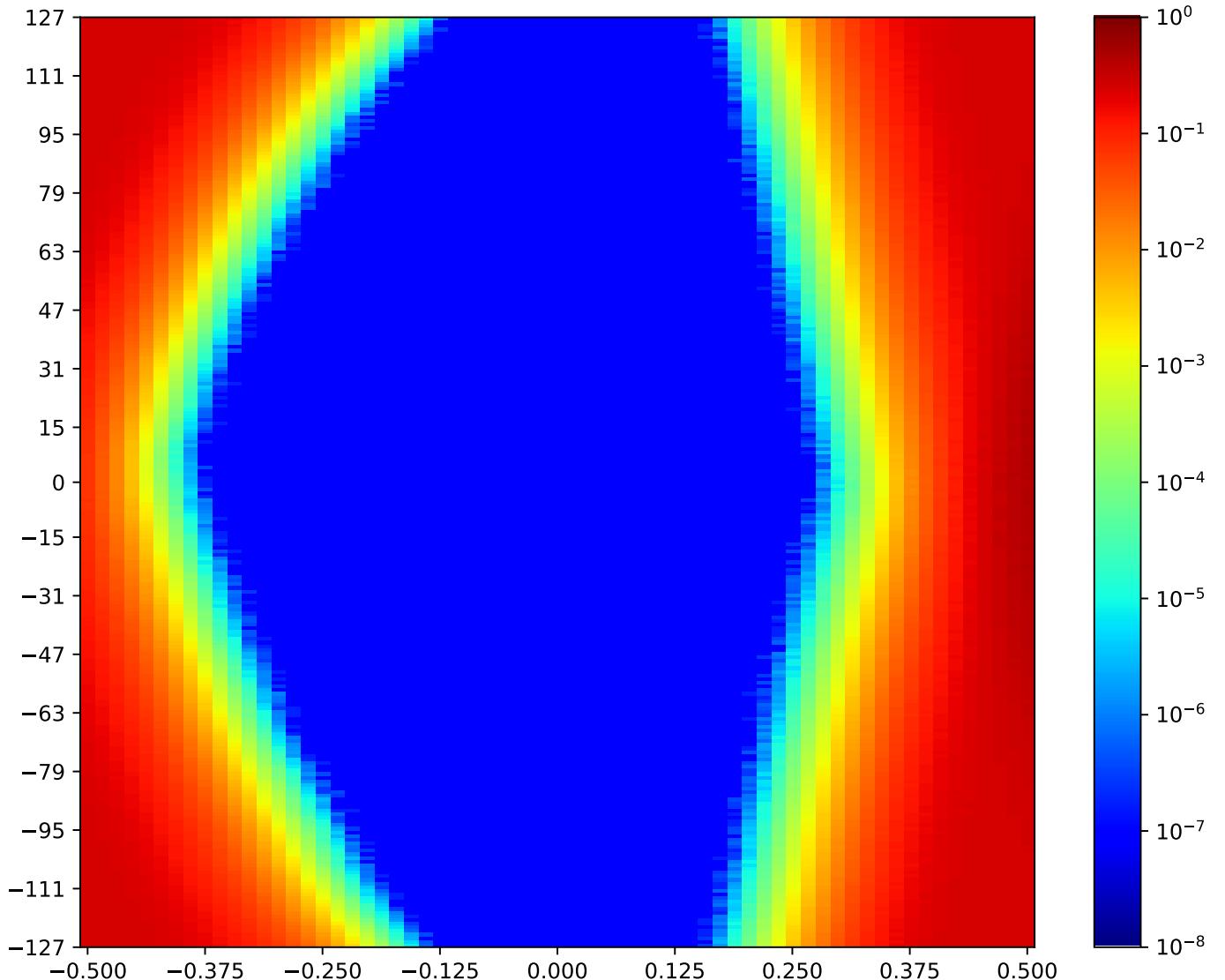


Figure 2.54: TRP\_FPGA-TX5-00-RX5-00-MSP\_A\_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.5.2 TRP\_FPGA-TX5-01-RX5-01-MSP\_A\_FPGA

Table 2.50: TRP\_FPGA-TX5-01-RX5-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:34:50		2018-Jan-24 19:35:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6996	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

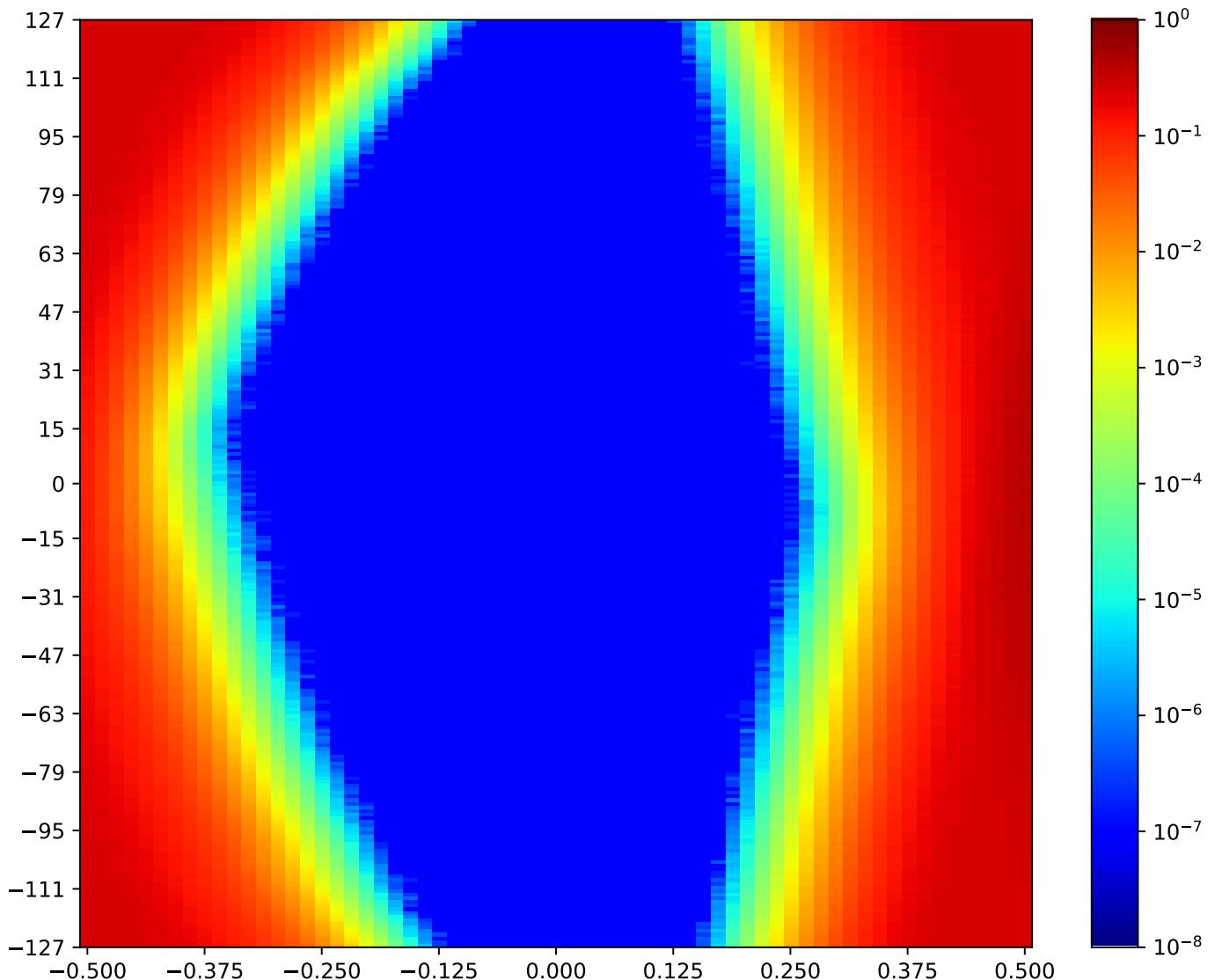


Figure 2.55: TRP\_FPGA-TX5-01-RX5-01-MSP\_A\_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.5.3 TRP\_FPGA-TX5-02-RX5-02-MSP\_A\_FPGA

Table 2.51: TRP\_FPGA-TX5-02-RX5-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:36:47		2018-Jan-24 19:37:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9629	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

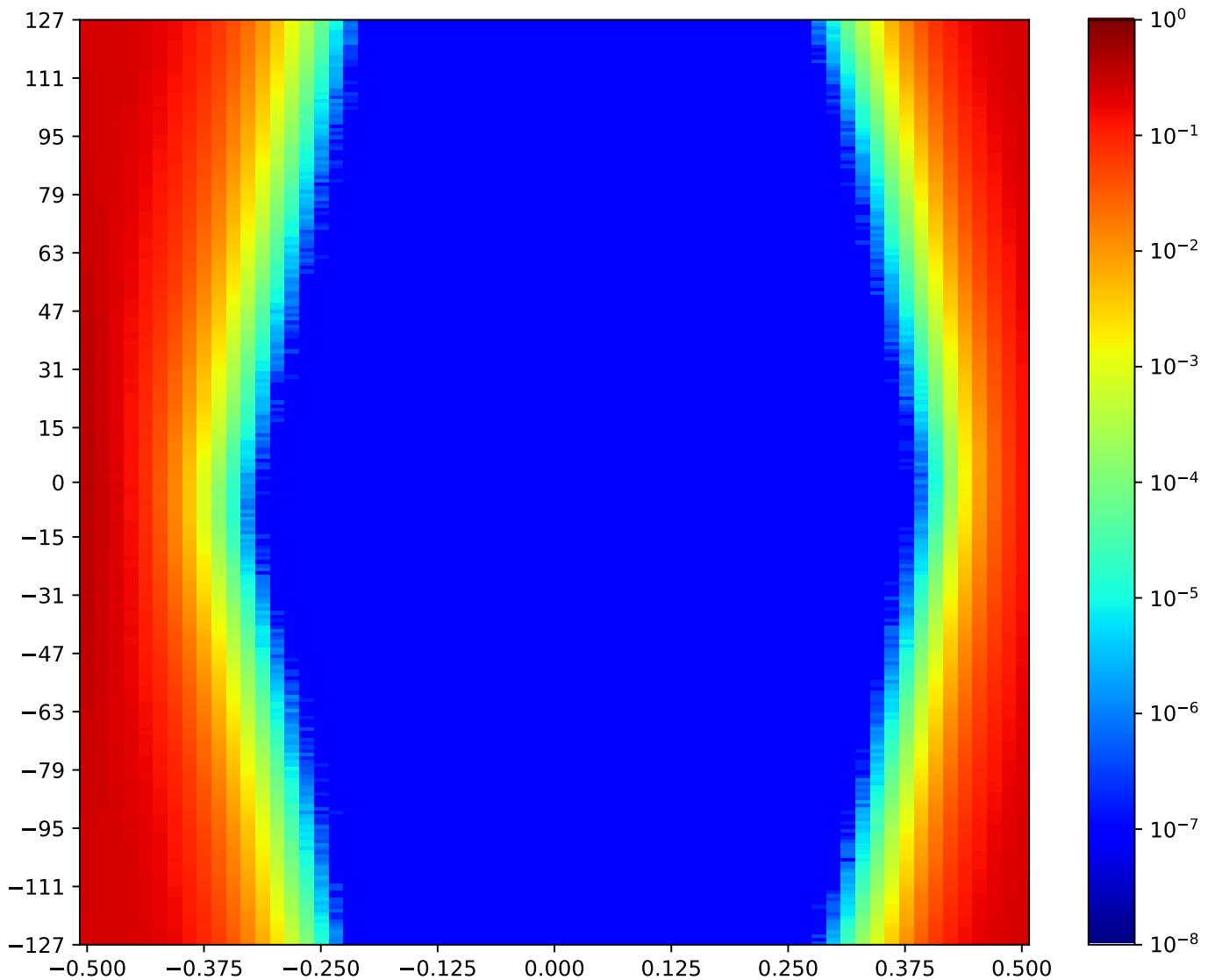


Figure 2.56: TRP\_FPGA-TX5-02-RX5-02-MSP\_A\_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.5.4 TRP\_FPGA-TX5-03-RX5-03-MSP\_A\_FPGA

Table 2.52: TRP\_FPGA-TX5-03-RX5-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:35:19		2018-Jan-24 19:35:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7247	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

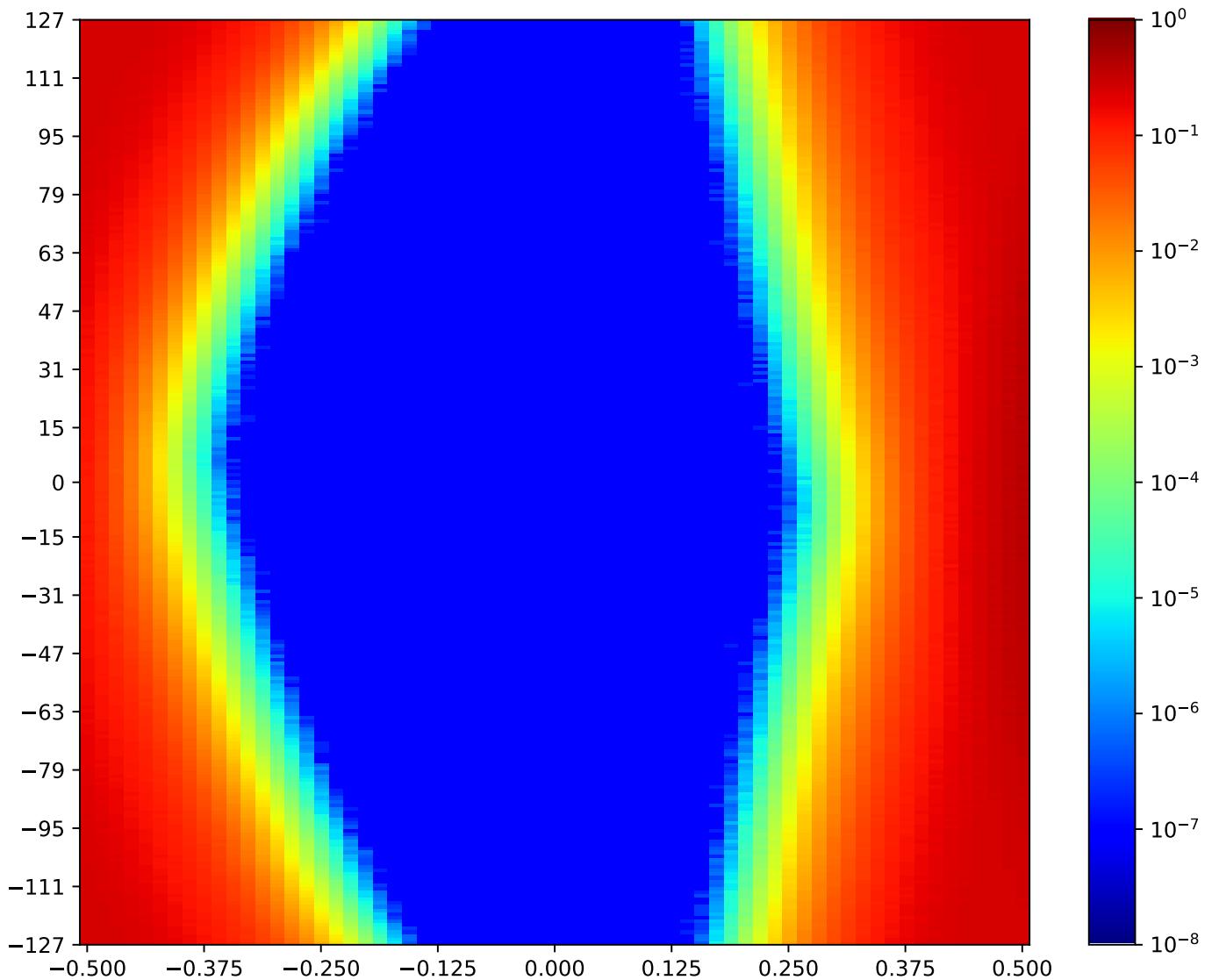


Figure 2.57: TRP\_FPGA-TX5-03-RX5-03-MSP\_A\_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.5.5 TRP\_FPGA-TX5-04-RX5-04-MSP\_A\_FPGA

Table 2.53: TRP\_FPGA-TX5-04-RX5-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:37:46		2018-Jan-24 19:38:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8886	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

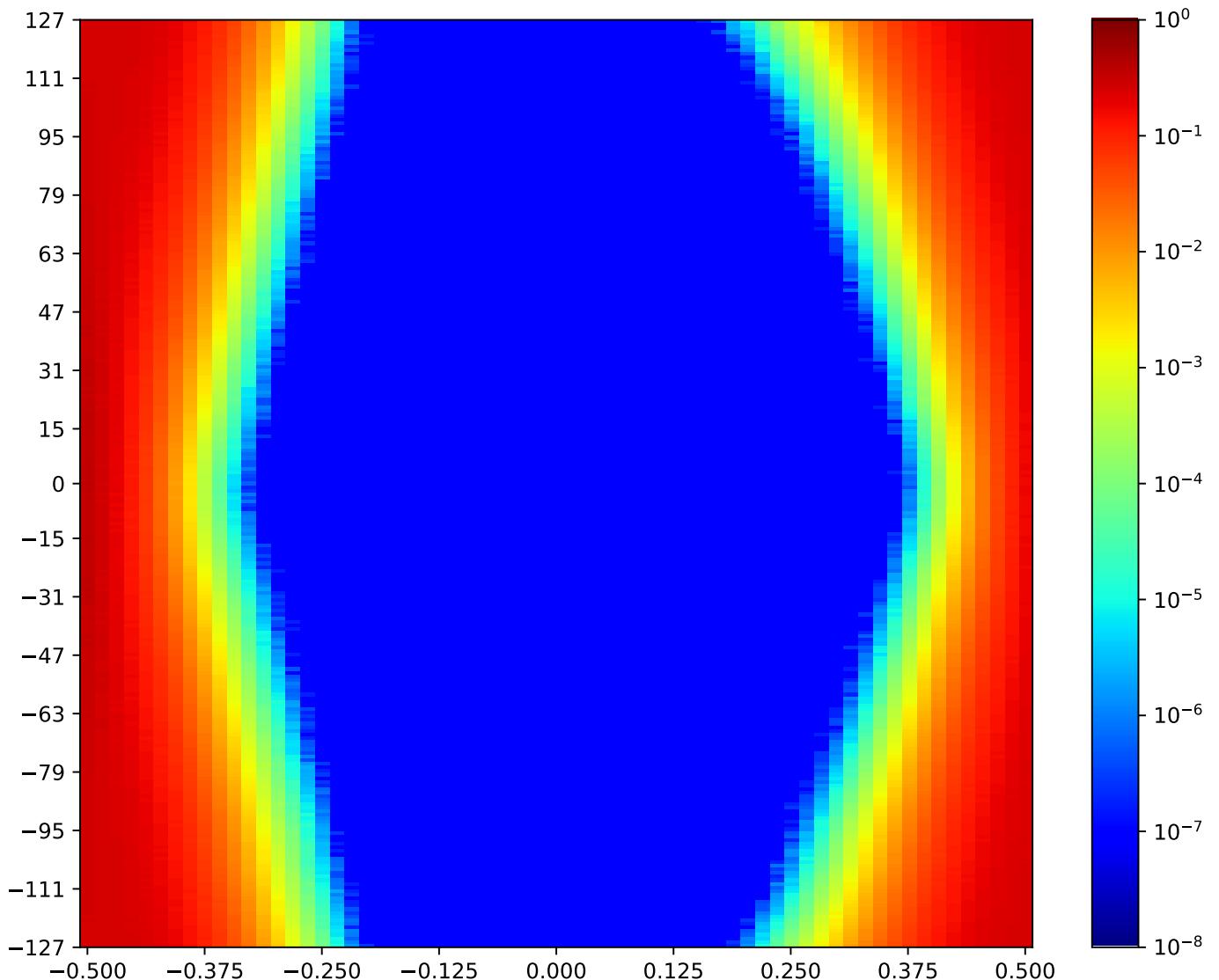


Figure 2.58: TRP\_FPGA-TX5-04-RX5-04-MSP\_A\_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.5.6 TRP\_FPGA-TX5-05-RX5-05-MSP\_A\_FPGA

Table 2.54: TRP\_FPGA-TX5-05-RX5-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:34:20		2018-Jan-24 19:34:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7050	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

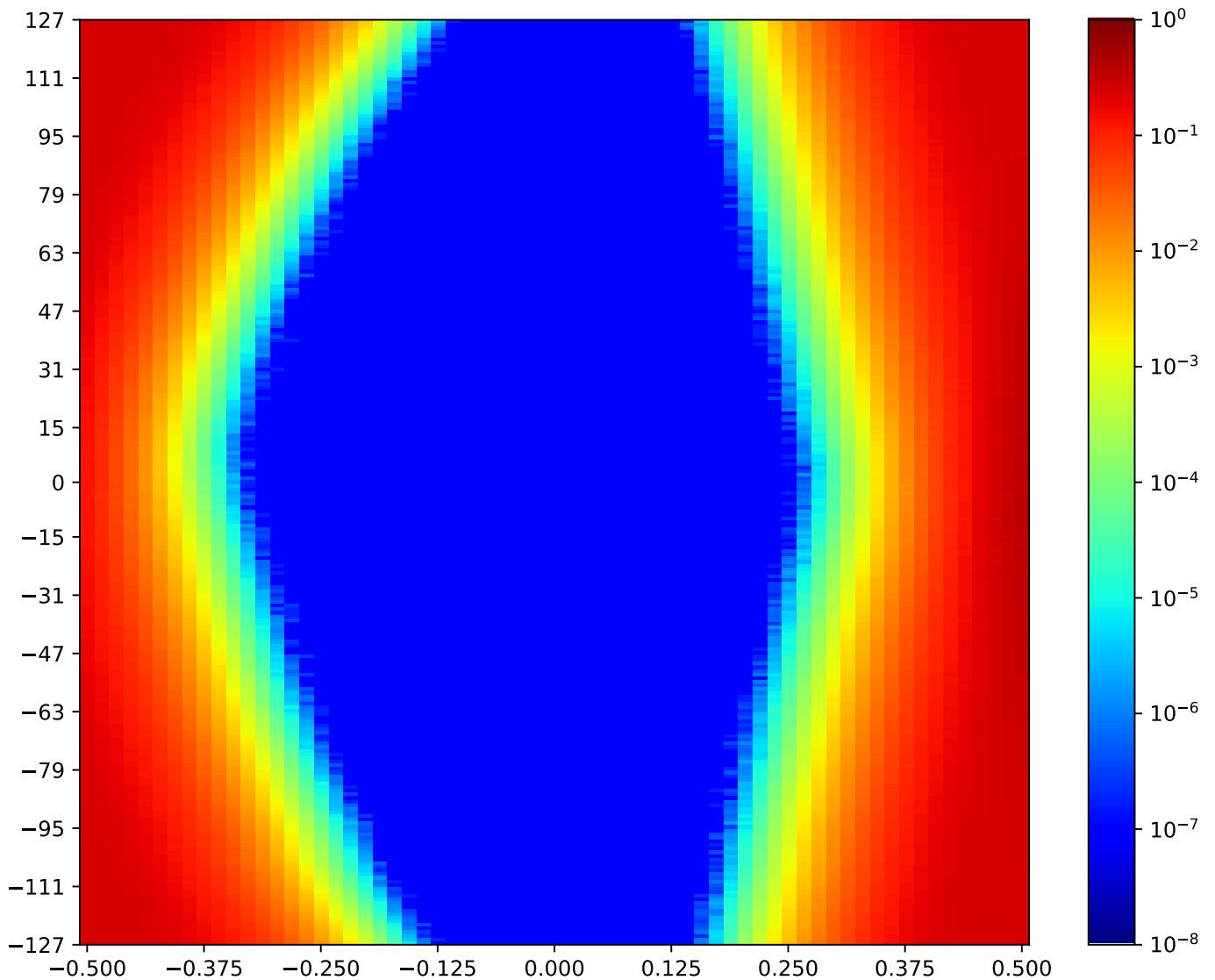


Figure 2.59: TRP\_FPGA-TX5-05-RX5-05-MSP\_A\_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.5.7 TRP\_FPGA-TX5-06-RX5-06-MSP\_A\_FPGA

Table 2.55: TRP\_FPGA-TX5-06-RX5-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:36:17		2018-Jan-24 19:36:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9514	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

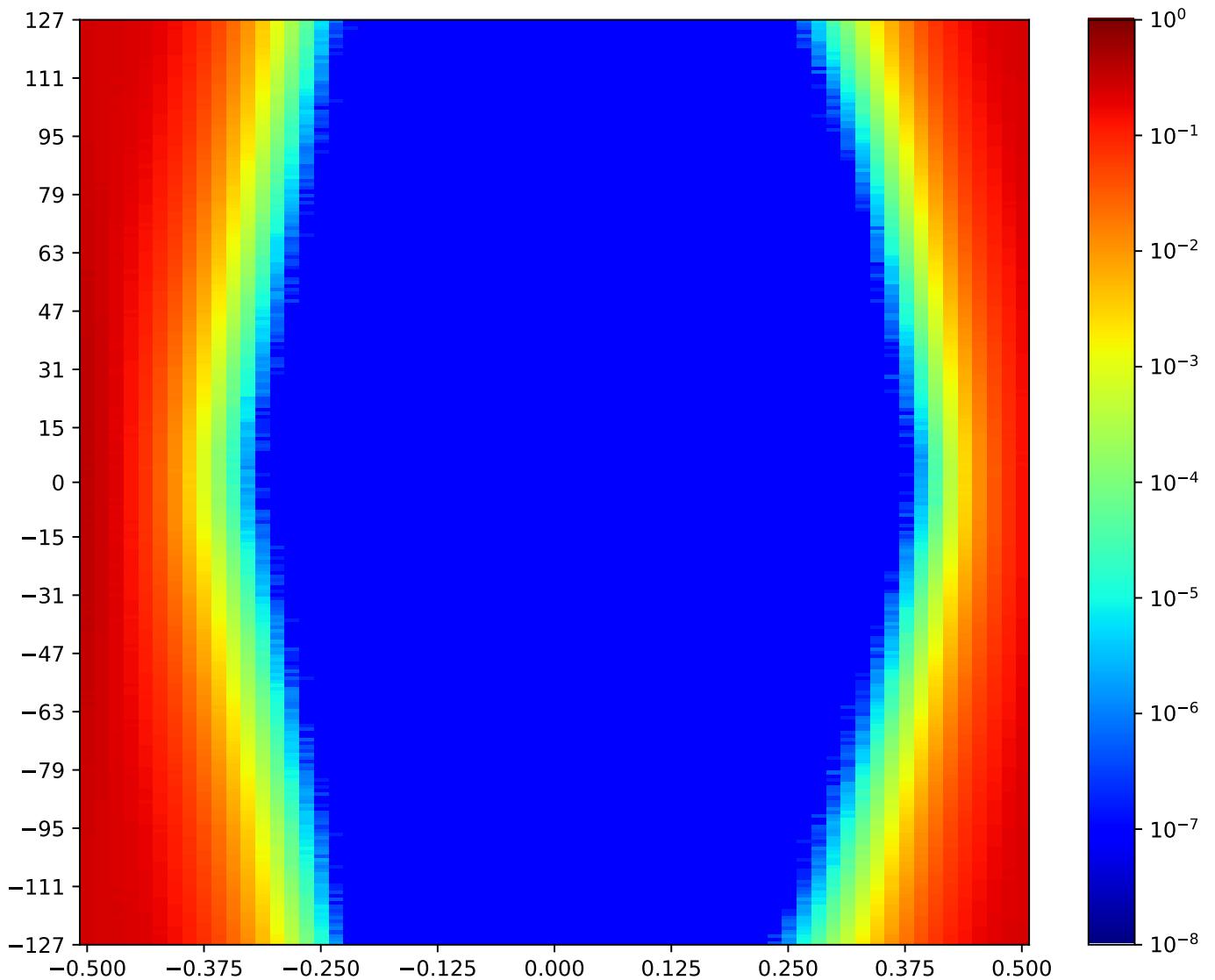


Figure 2.60: TRP\_FPGA-TX5-06-RX5-06-MSP\_A\_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.5.8 TRP\_FPGA-TX5-07-RX5-07-MSP\_A\_FPGA

Table 2.56: TRP\_FPGA-TX5-07-RX5-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:37:16		2018-Jan-24 19:37:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8915	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

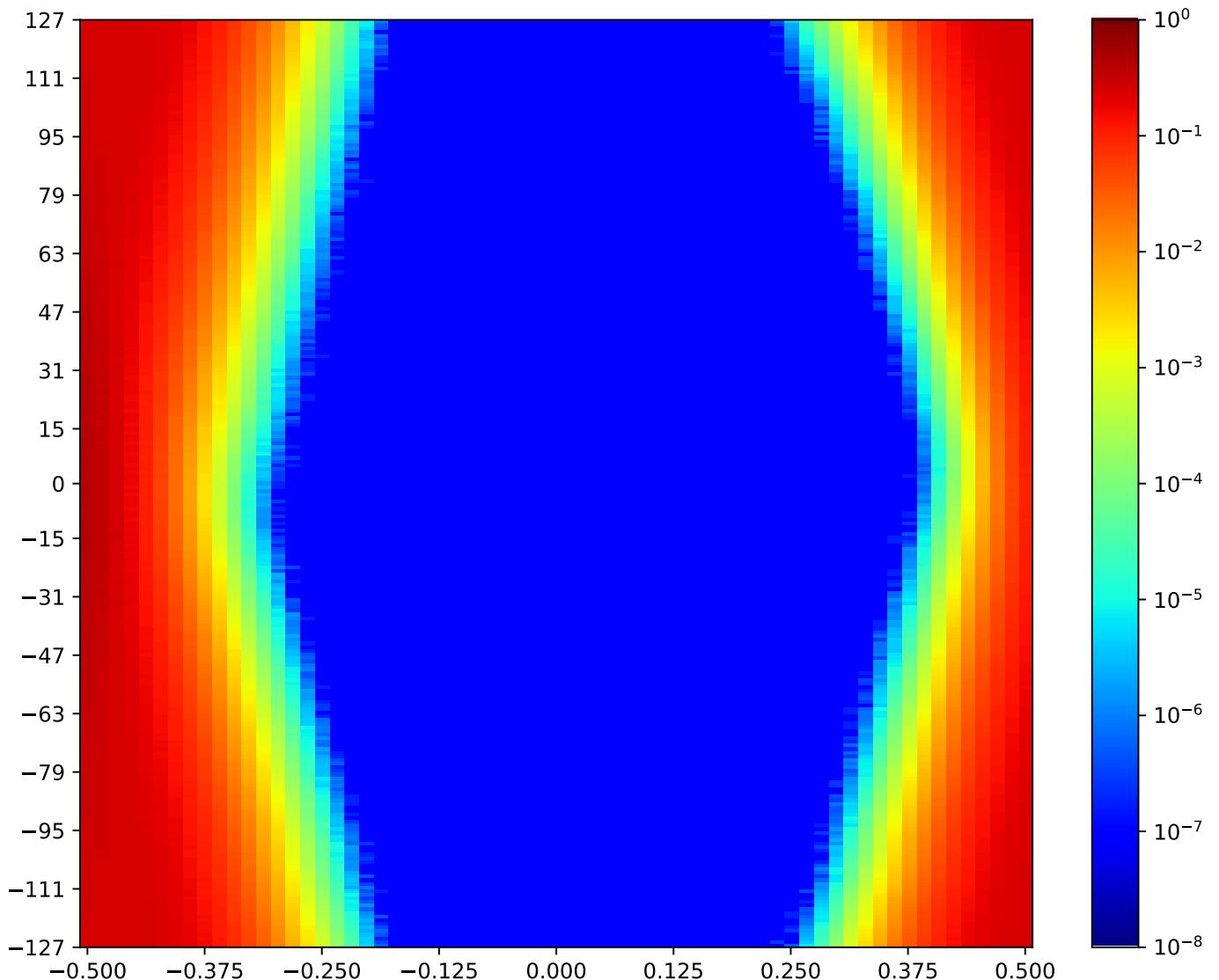


Figure 2.61: TRP\_FPGA-TX5-07-RX5-07-MSP\_A\_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.6 TRP J1 QSFP Loopback

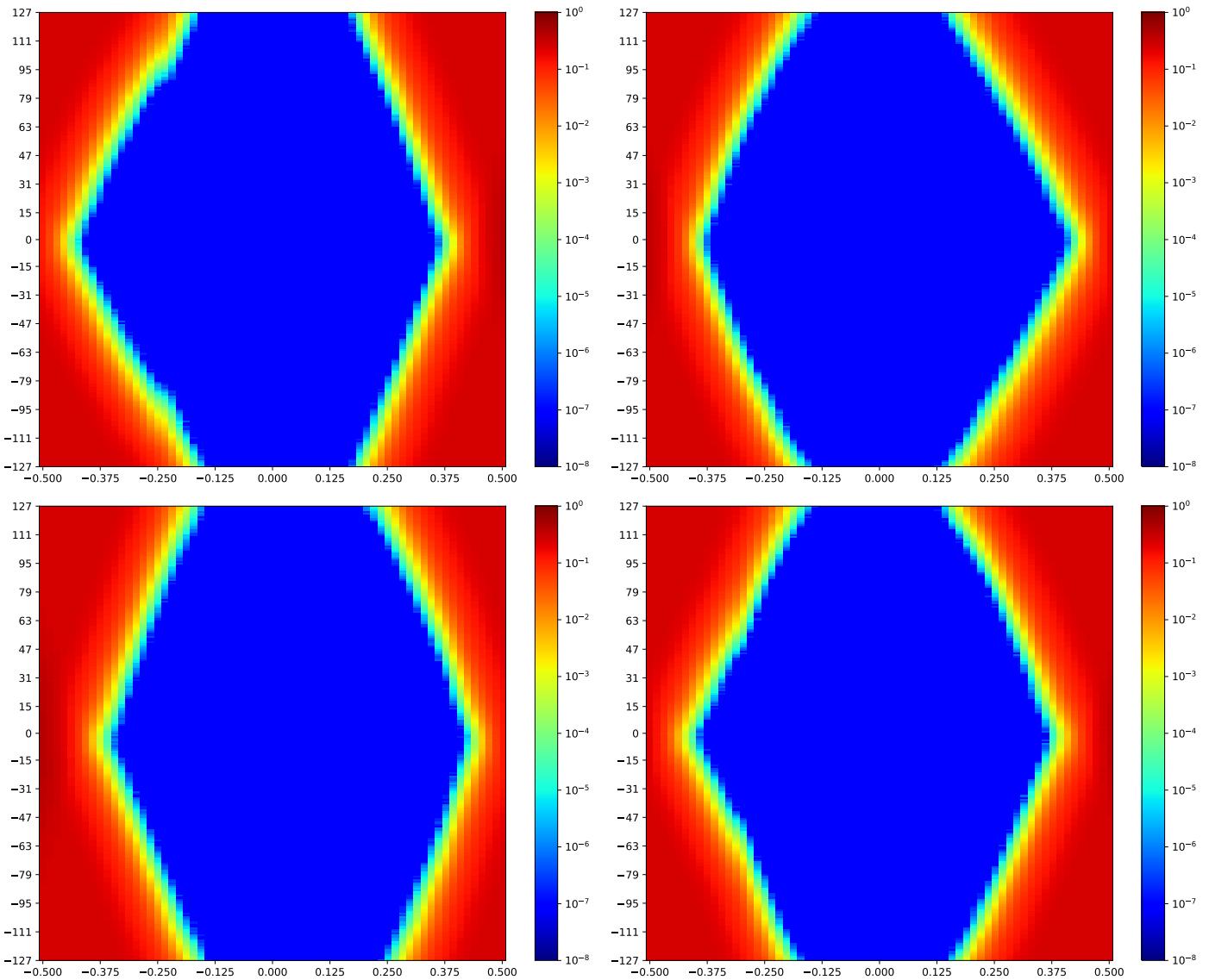


Figure 2.62: TRP J1 QSFP Loopback

A cross-reference to Figure 2.62. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.67.

### 2.6.1 TRP\_FPGA-J1-00–J1-00-TRP\_FPGA

Table 2.57: TRP\_FPGA-J1-00–J1-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:38:15		2018-Jan-24 19:38:42	
Reset RX	OA	HO		HO (%)	
true	8833	49		75.38%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

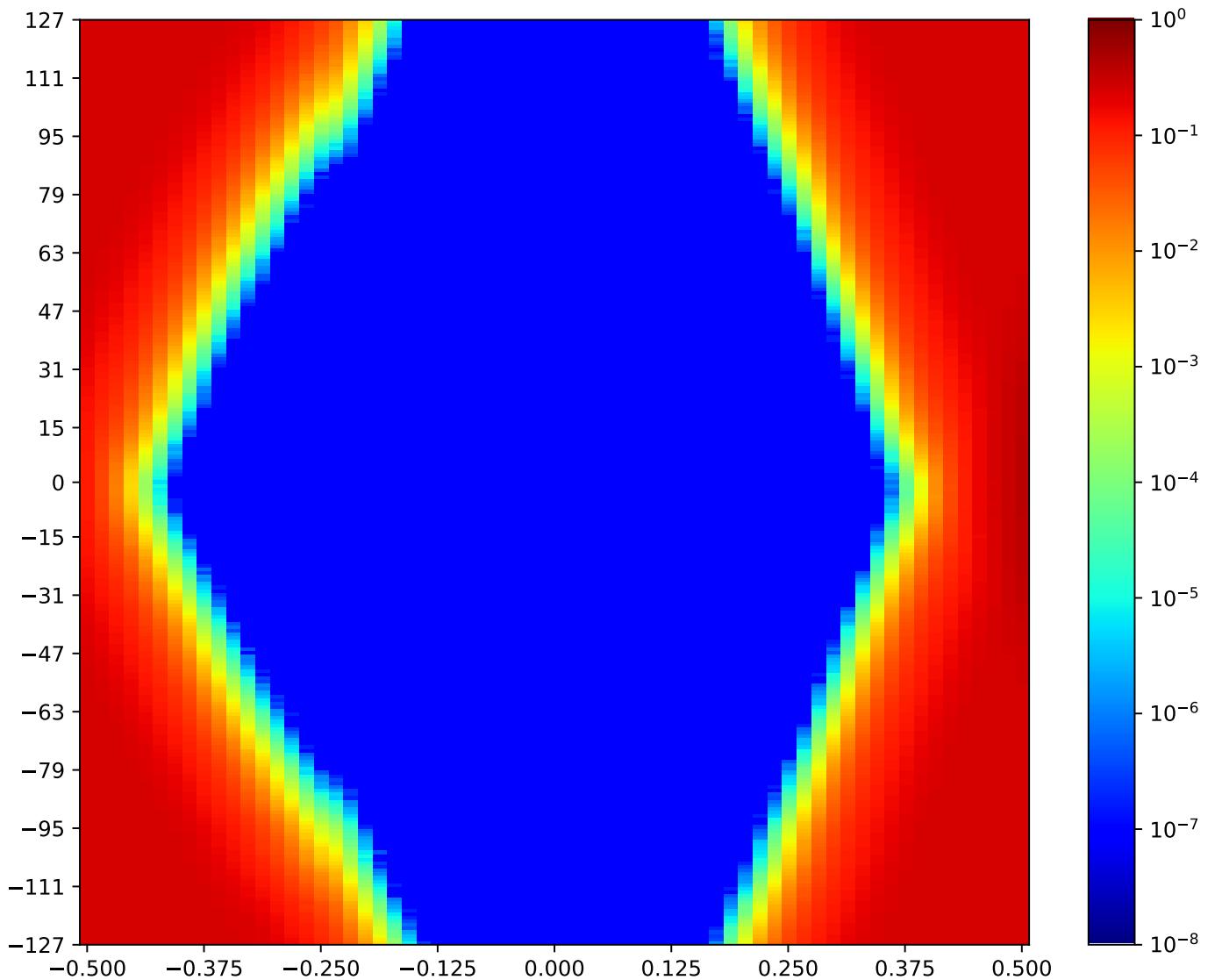


Figure 2.63: TRP\_FPGA-J1-00–J1-00-TRP\_FPGA

Call back to summary Figure 2.62. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.6.2 TRP\_FPGA-J1-01–J1-01-TRP\_FPGA

Table 2.58: TRP\_FPGA-J1-01–J1-01-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:38:43		2018-Jan-24 19:39:10	
Reset RX	OA	HO		HO (%)	
true	8780	49		75.38%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

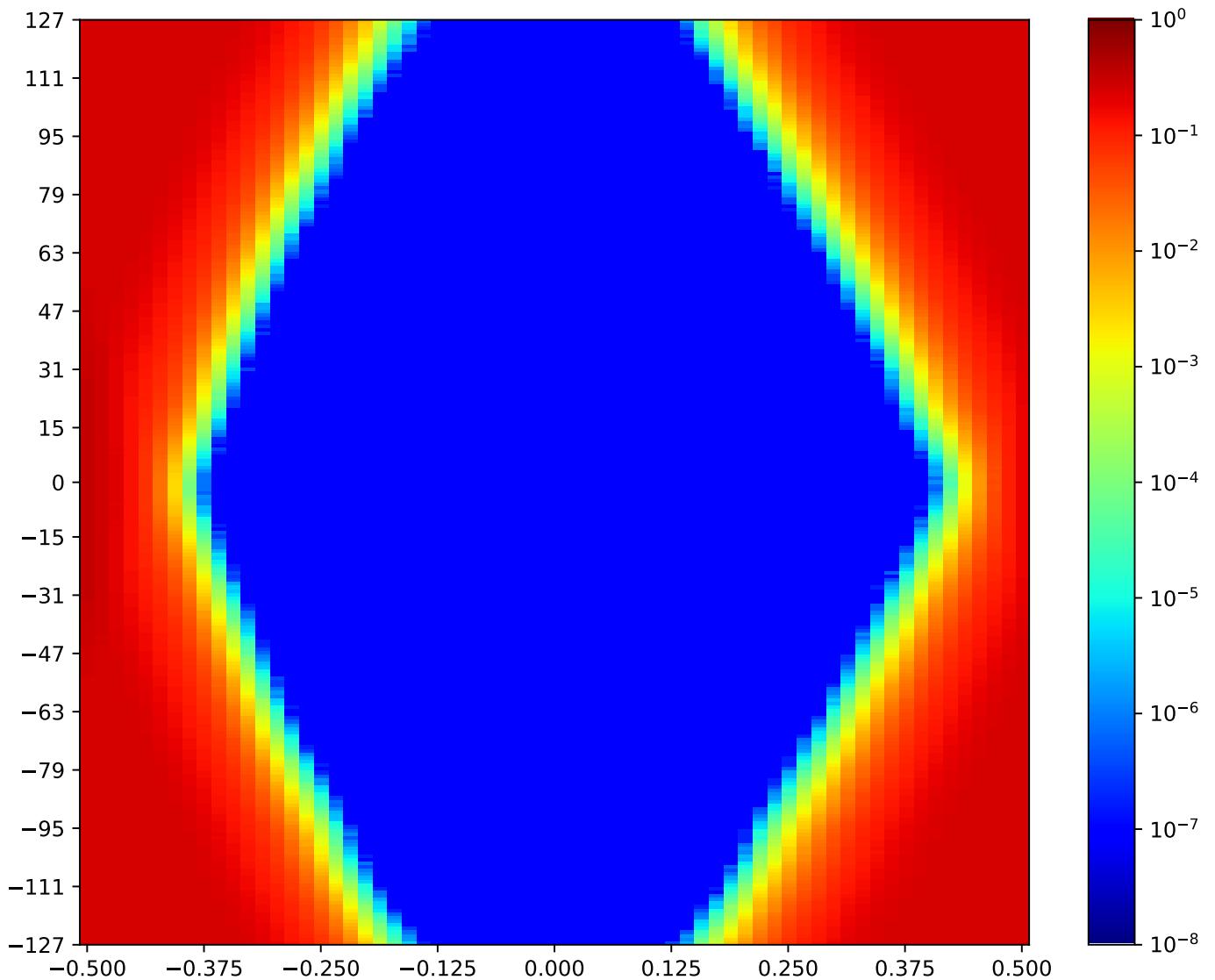


Figure 2.64: TRP\_FPGA-J1-01–J1-01-TRP\_FPGA

Call back to summary Figure 2.62. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.6.3 TRP\_FPGA-J1-02–J1-02-TRP\_FPGA

Table 2.59: TRP\_FPGA-J1-02–J1-02-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:39:11		2018-Jan-24 19:39:39	
Reset RX	OA	HO		HO (%)	
true	9207	47		72.31%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

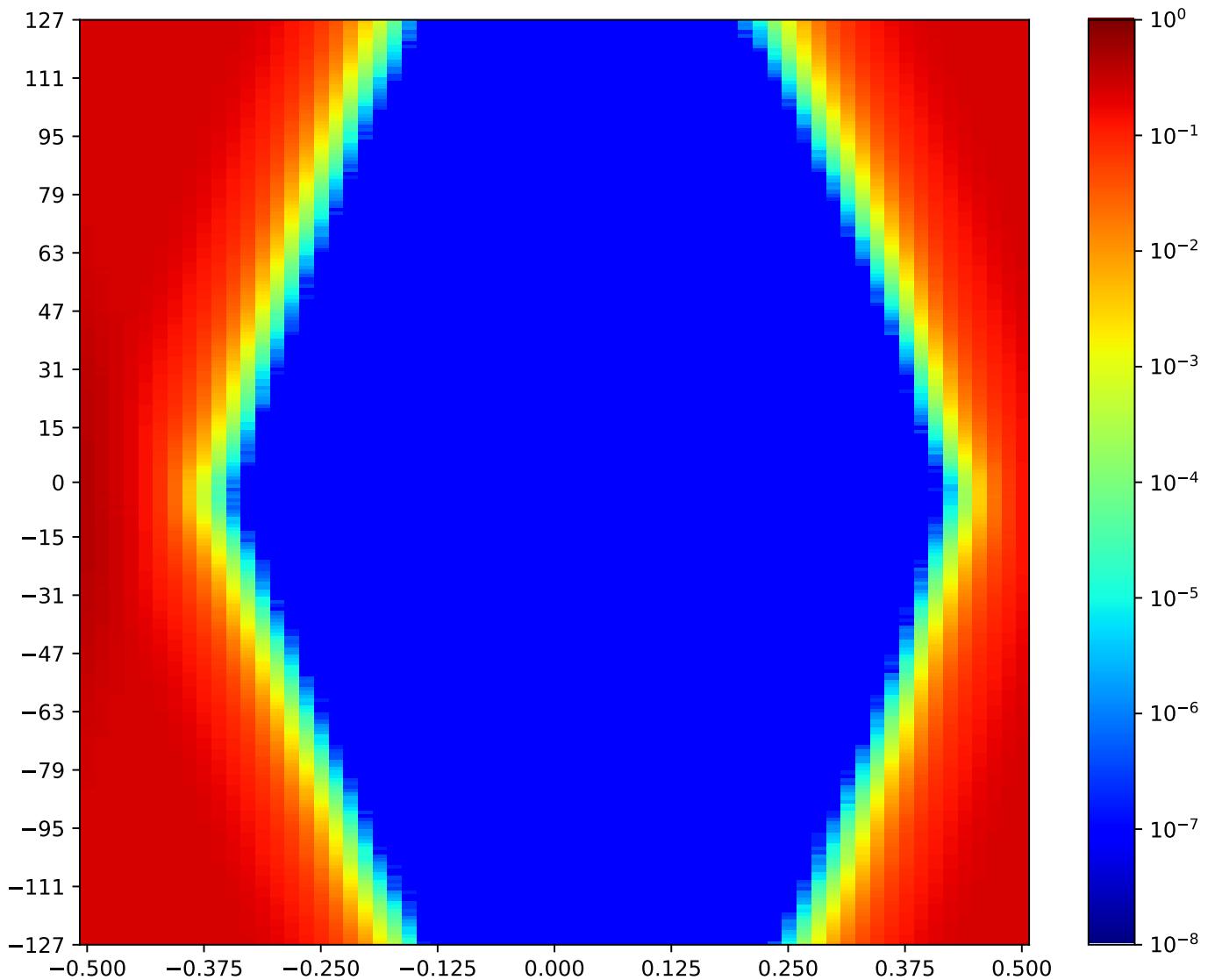


Figure 2.65: TRP\_FPGA-J1-02–J1-02-TRP\_FPGA

Call back to summary Figure 2.62. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.6.4 TRP\_FPGA-J1-03–J1-03-TRP\_FPGA

Table 2.60: TRP\_FPGA-J1-03–J1-03-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:39:39		2018-Jan-24 19:40:06	
Reset RX	OA	HO		HO (%)	
true	8577	47		72.31%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

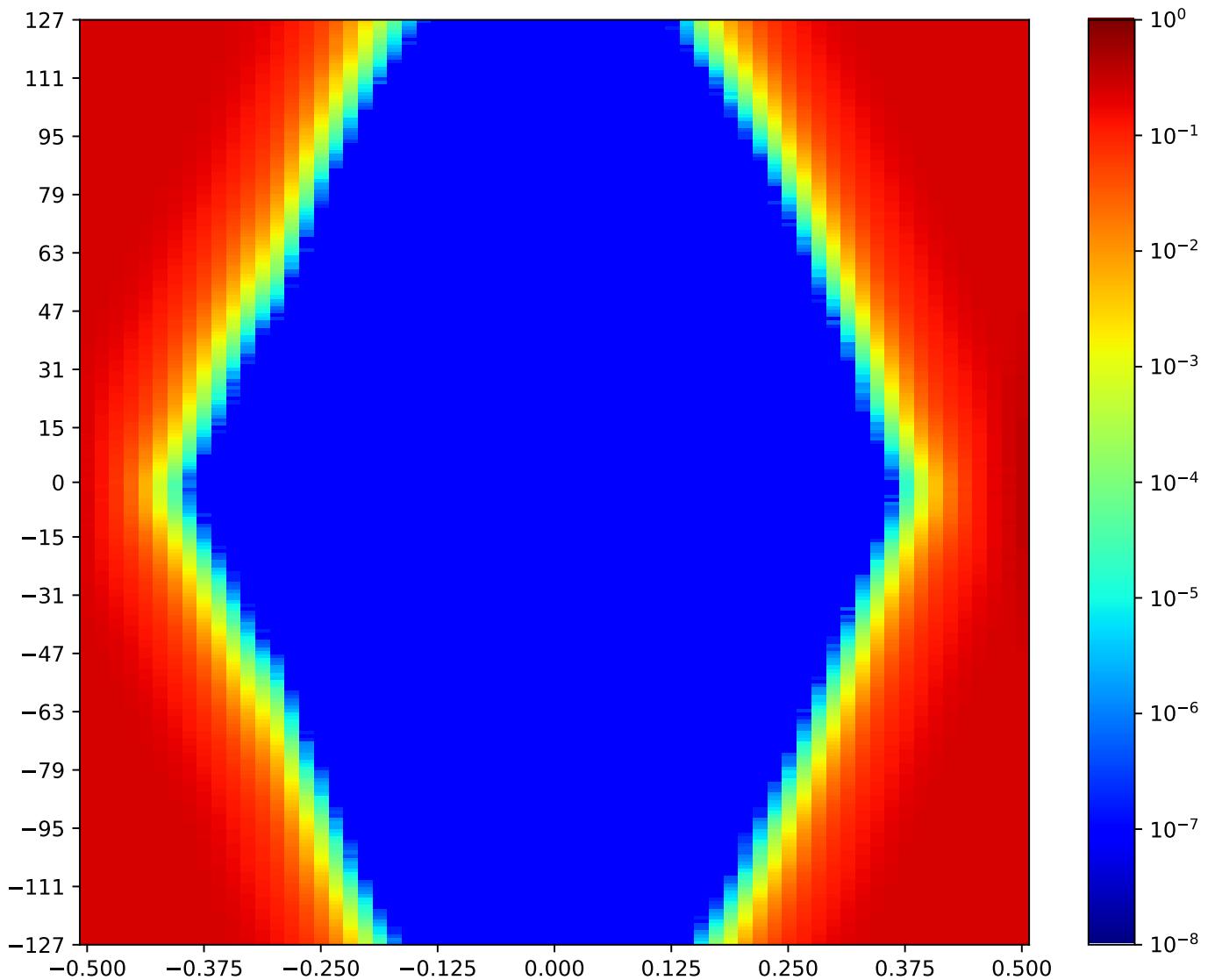


Figure 2.66: TRP\_FPGA-J1-03–J1-03-TRP\_FPGA

Call back to summary Figure 2.62. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.7 TRP J3 SFP Loopback

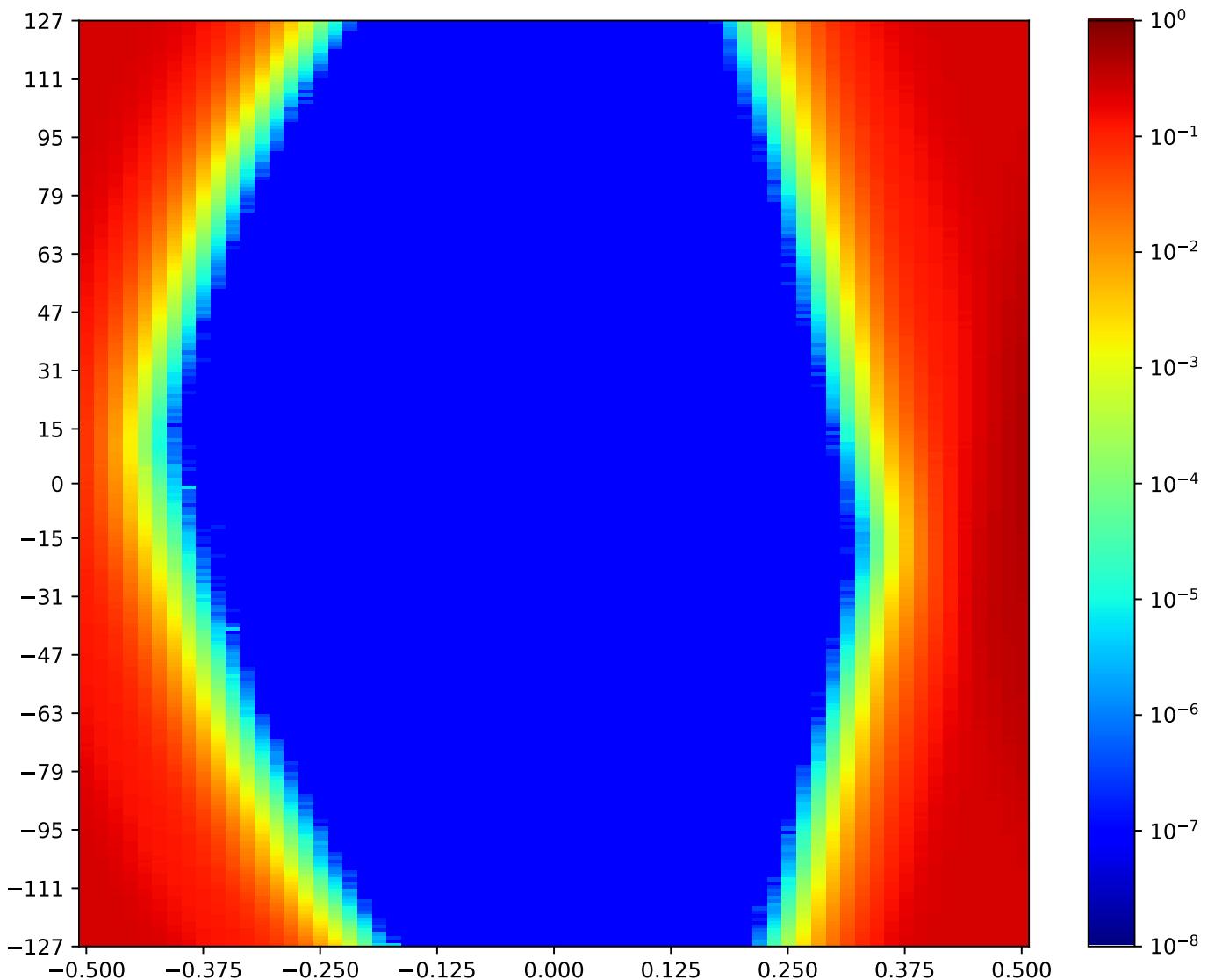


Figure 2.67: TRP J3 SFP Loopback

A cross-reference to Figure 2.67. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.69.

### 2.7.1 TRP\_FPGA-J3-00–J3-00-TRP\_FPGA

Table 2.61: TRP\_FPGA-J3-00–J3-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:40:06		2018-Jan-24 19:40:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9224	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

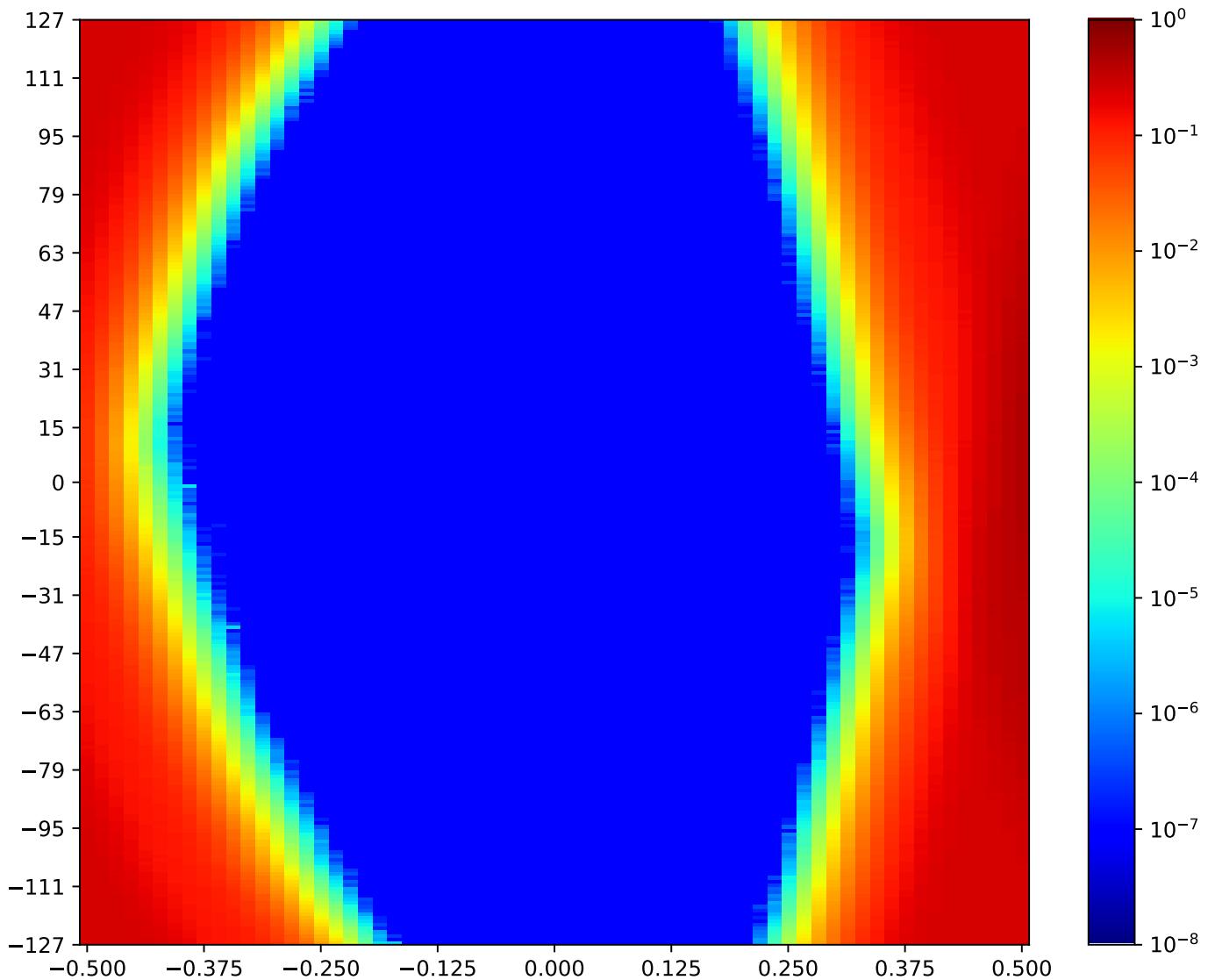


Figure 2.68: TRP\_FPGA-J3-00–J3-00-TRP\_FPGA

Call back to summary Figure 2.67. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8 MSP\_A TRP On board links

A cross-reference to Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.98.

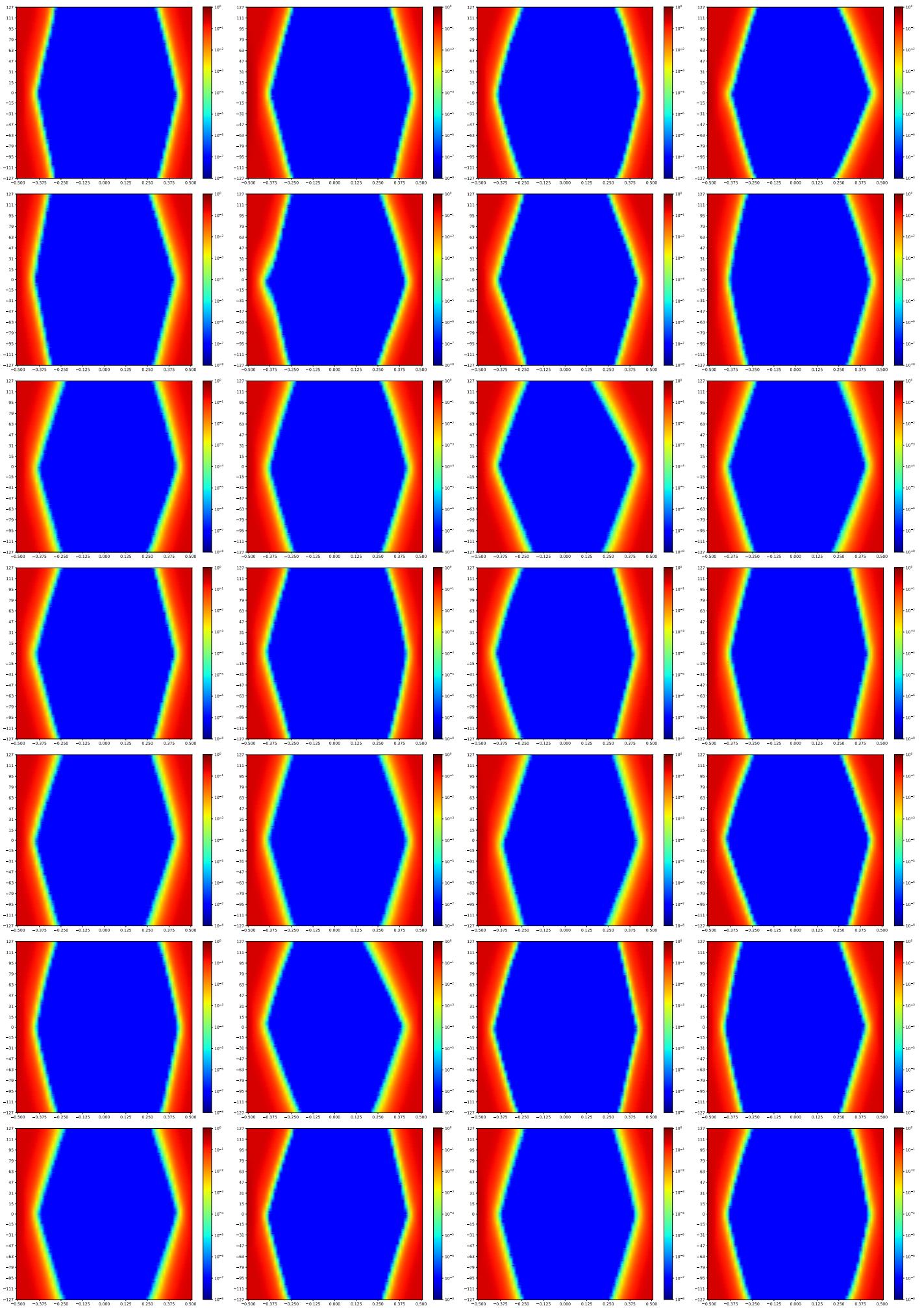


Figure 2.69: MSP\_A TRP On board links

### 2.8.1 MSP\_A\_FPGA-IC39-00-IC4-00-TRP\_FPGA

Table 2.62: MSP\_A\_FPGA-IC39-00-IC4-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:40:36		2018-Jan-24 19:41:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11037	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

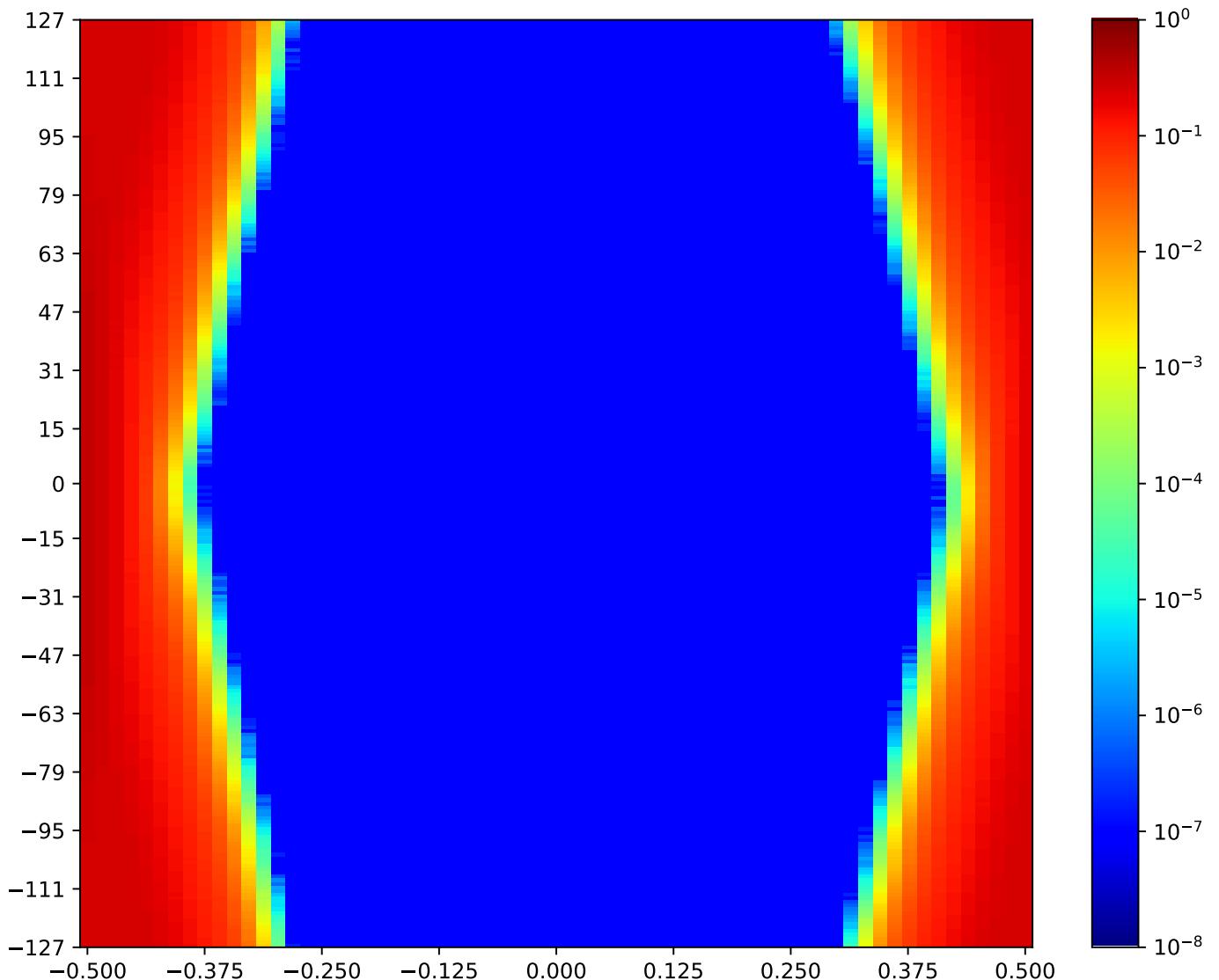


Figure 2.70: MSP\_A\_FPGA-IC39-00-IC4-00-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.2 MSP\_A\_FPGA-IC39-01-IC4-01-TRP\_FPGA

Table 2.63: MSP\_A\_FPGA-IC39-01-IC4-01-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:41:06		2018-Jan-24 19:41:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10888	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

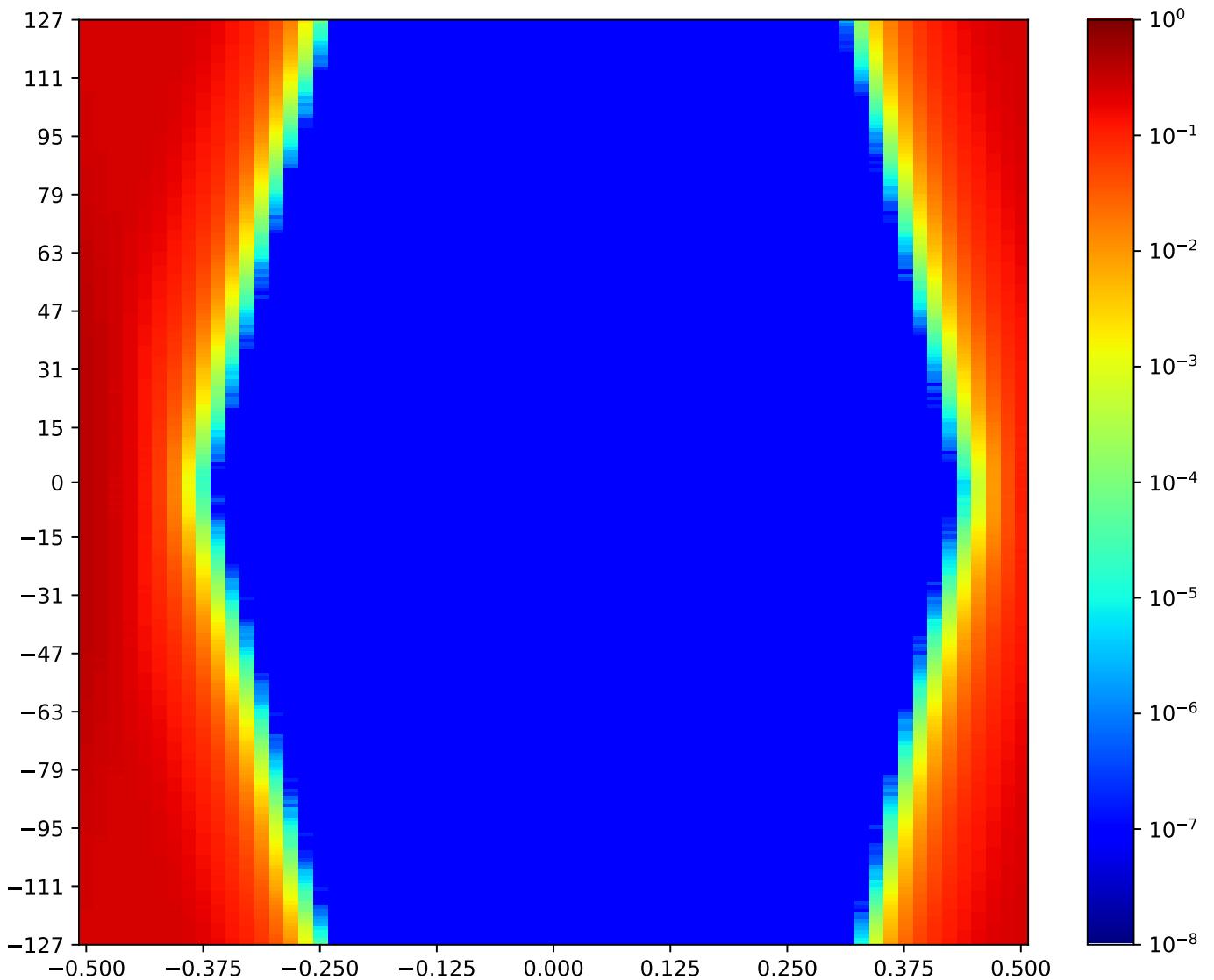


Figure 2.71: MSP\_A\_FPGA-IC39-01-IC4-01-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.3 MSP\_A\_FPGA-IC39-02-IC4-02-TRP\_FPGA

Table 2.64: MSP\_A\_FPGA-IC39-02-IC4-02-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:41:36		2018-Jan-24 19:42:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11017	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

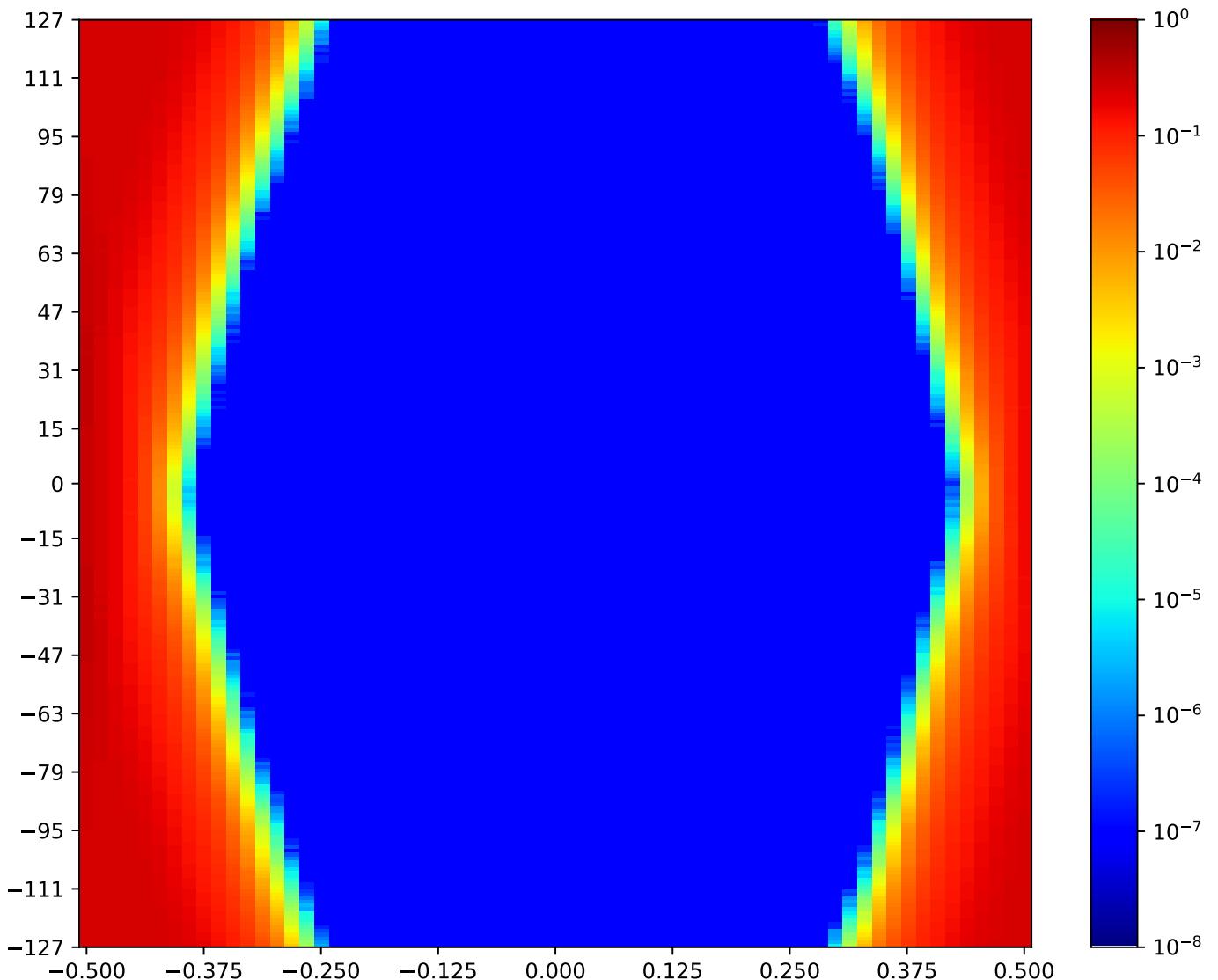


Figure 2.72: MSP\_A\_FPGA-IC39-02-IC4-02-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.4 MSP\_A\_FPGA-IC39-03-IC4-03-TRP\_FPGA

Table 2.65: MSP\_A\_FPGA-IC39-03-IC4-03-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:42:05		2018-Jan-24 19:42:34	
Reset RX	OA	HO		HO (%)	
true	10063	49		75.38%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

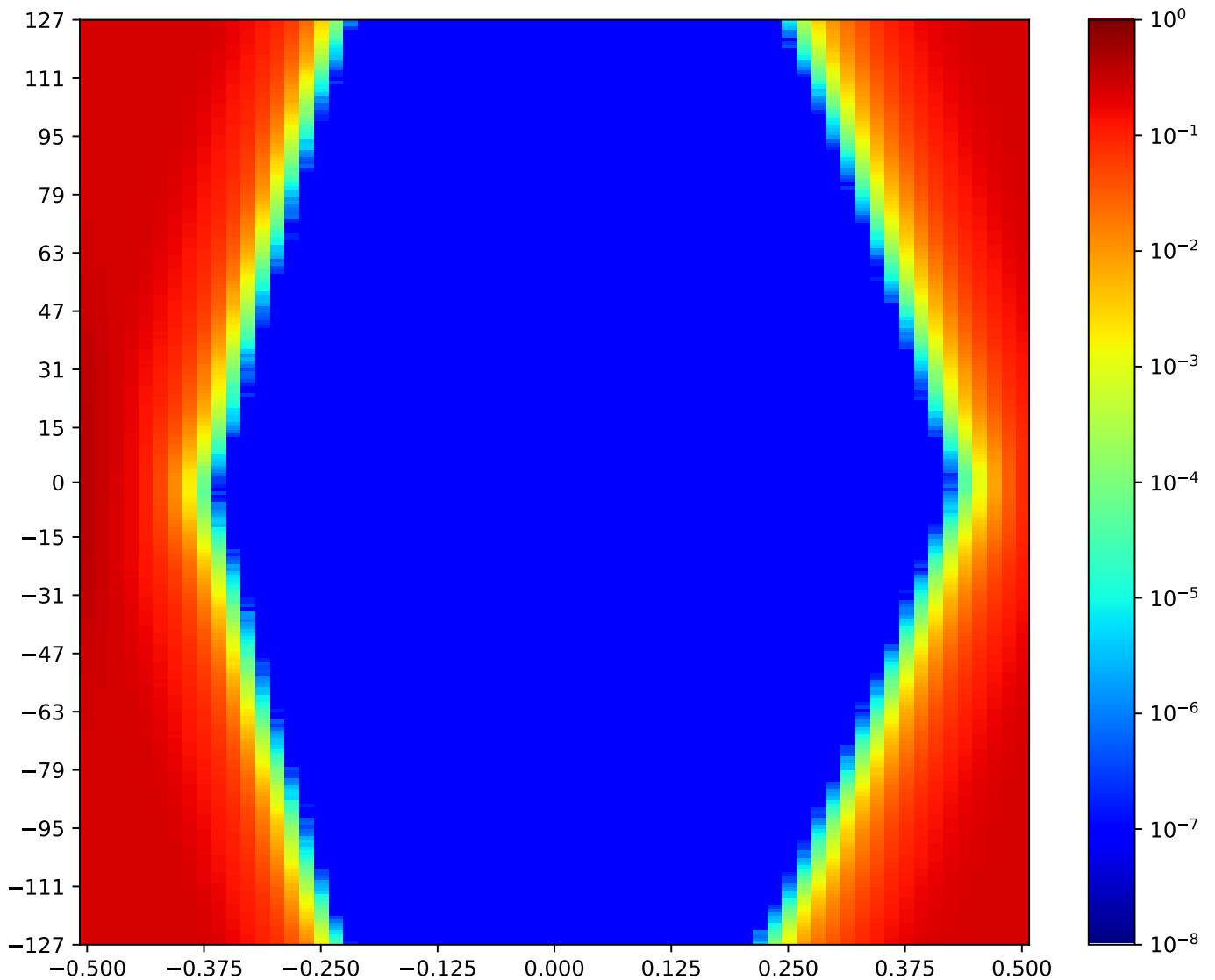


Figure 2.73: MSP\_A\_FPGA-IC39-03-IC4-03-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.5 MSP\_A\_FPGA-IC39-04-IC4-04-TRP\_FPGA

Table 2.66: MSP\_A\_FPGA-IC39-04-IC4-04-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:42:34		2018-Jan-24 19:43:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10948	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

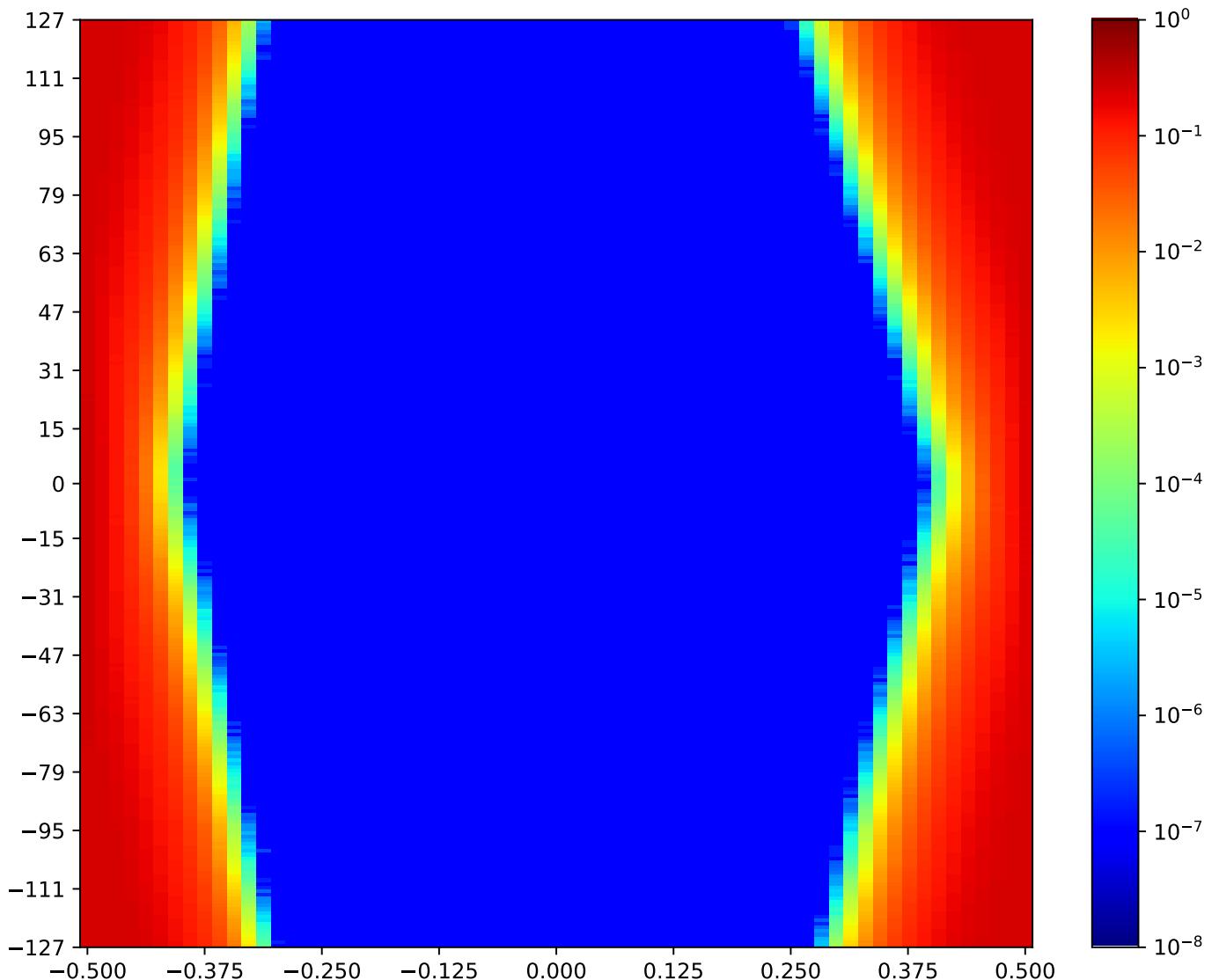


Figure 2.74: MSP\_A\_FPGA-IC39-04-IC4-04-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.6 MSP\_A\_FPGA-IC39-05-IC4-05-TRP\_FPGA

Table 2.67: MSP\_A\_FPGA-IC39-05-IC4-05-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:43:04		2018-Jan-24 19:43:33	
Reset RX	OA	HO		HO (%)	
true	10249	49		75.38%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

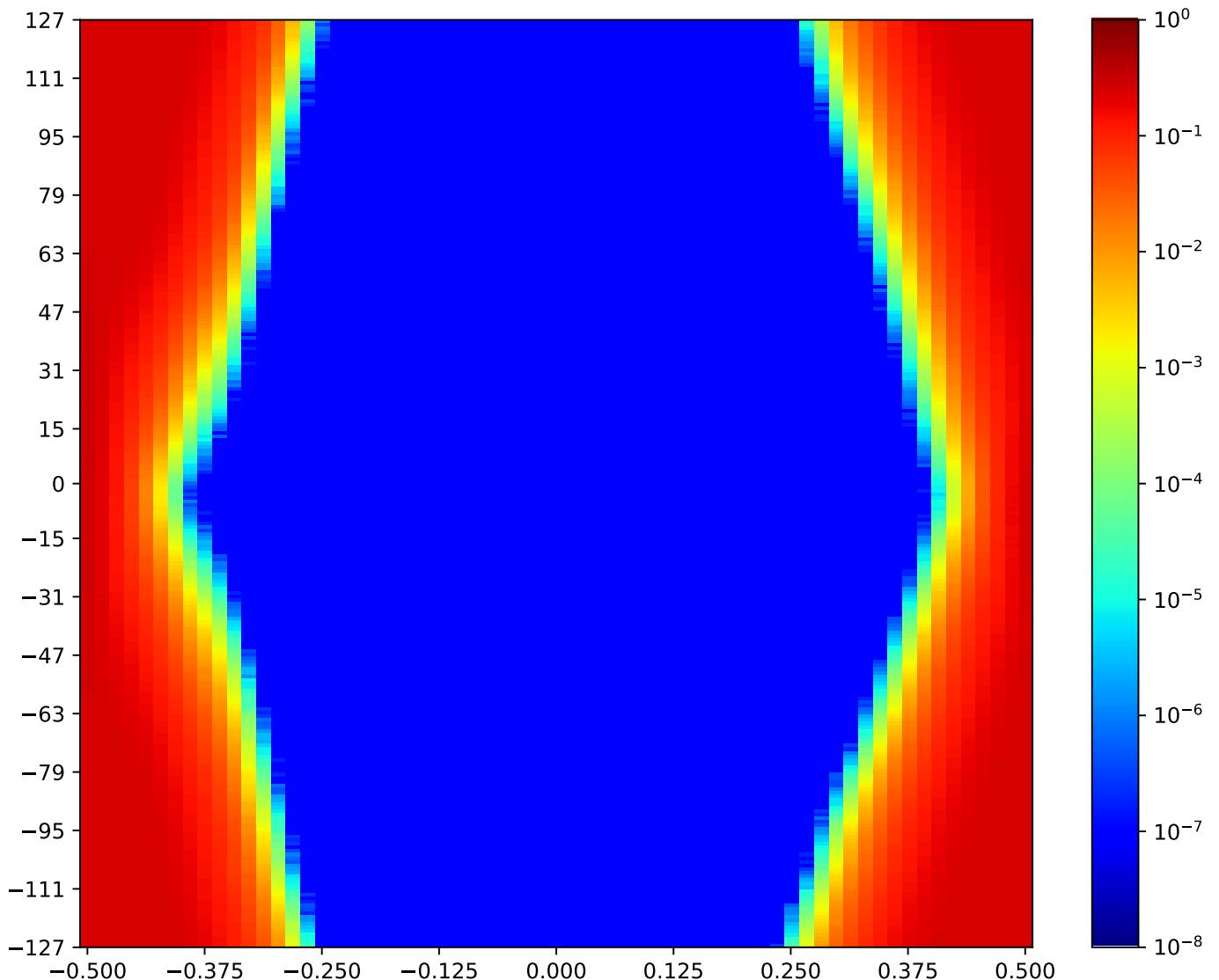


Figure 2.75: MSP\_A\_FPGA-IC39-05-IC4-05-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.7 MSP\_A\_FPGA-IC39-06-IC4-06-TRP\_FPGA

Table 2.68: MSP\_A\_FPGA-IC39-06-IC4-06-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:43:34		2018-Jan-24 19:44:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10270	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

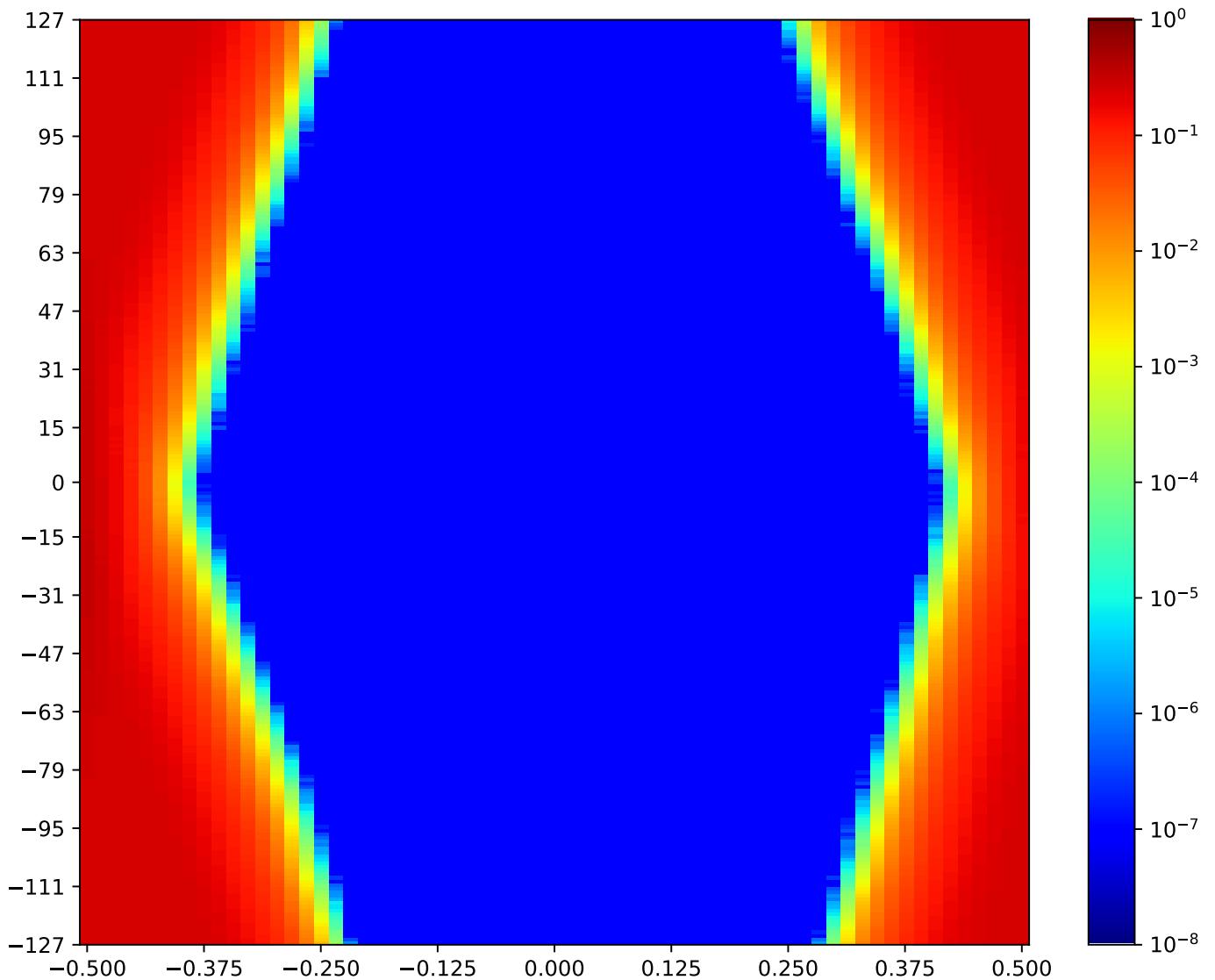


Figure 2.76: MSP\_A\_FPGA-IC39-06-IC4-06-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.8 MSP\_A\_FPGA-IC39-07-IC4-07-TRP\_FPGA

Table 2.69: MSP\_A\_FPGA-IC39-07-IC4-07-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:44:03		2018-Jan-24 19:44:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10992	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

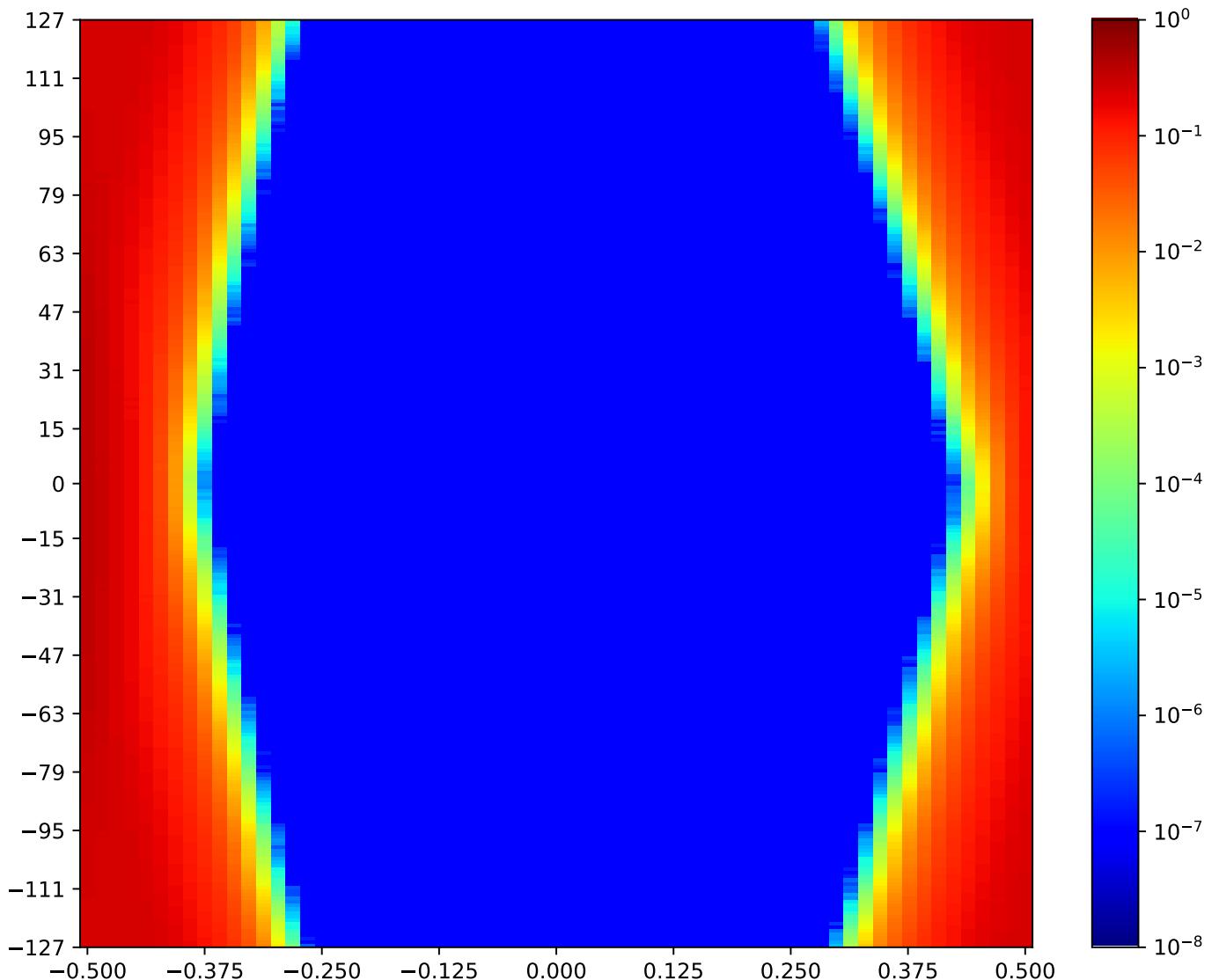


Figure 2.77: MSP\_A\_FPGA-IC39-07-IC4-07-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.9 MSP\_A\_FPGA-IC39-08-IC4-08-TRP\_FPGA

Table 2.70: MSP\_A\_FPGA-IC39-08-IC4-08-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:44:32		2018-Jan-24 19:45:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10227	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

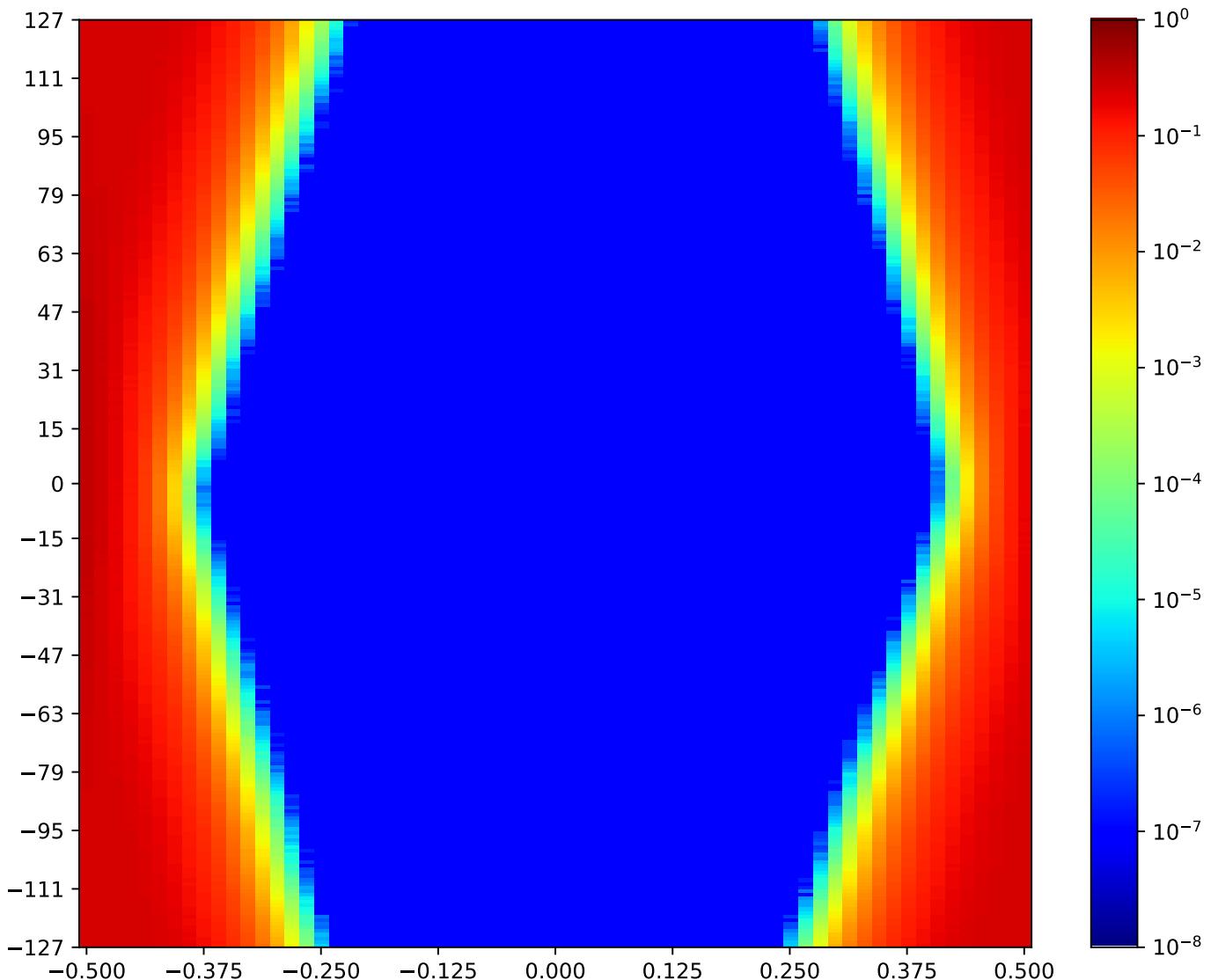


Figure 2.78: MSP\_A\_FPGA-IC39-08-IC4-08-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.10 MSP\_A\_FPGA-IC39-09-IC4-09-TRP\_FPGA

Table 2.71: MSP\_A\_FPGA-IC39-09-IC4-09-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:45:02		2018-Jan-24 19:45:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10269	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

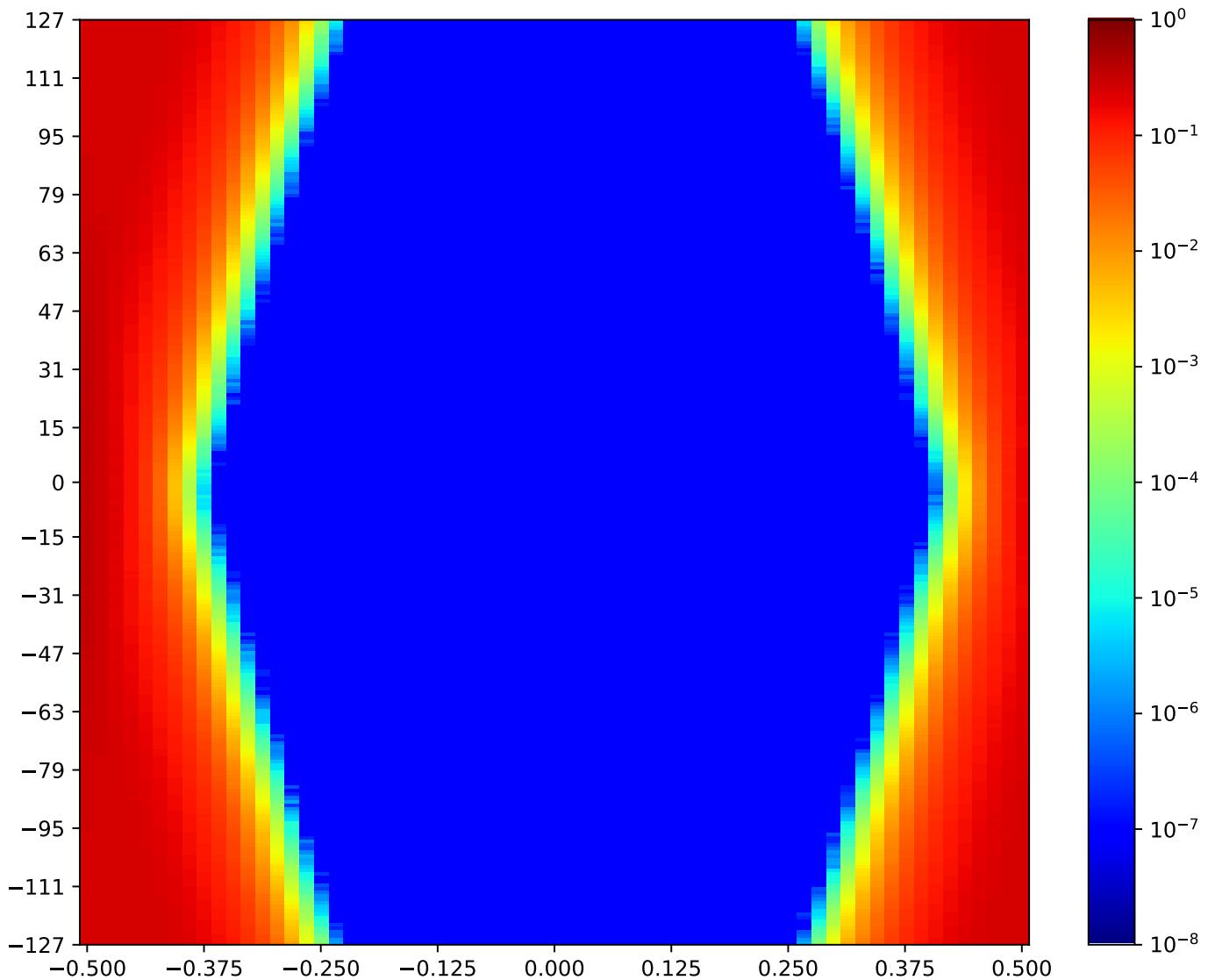


Figure 2.79: MSP\_A\_FPGA-IC39-09-IC4-09-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.11 MSP\_A\_FPGA-IC39-10-IC4-10-TRP\_FPGA

Table 2.72: MSP\_A\_FPGA-IC39-10-IC4-10-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:45:31		2018-Jan-24 19:45:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9250	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

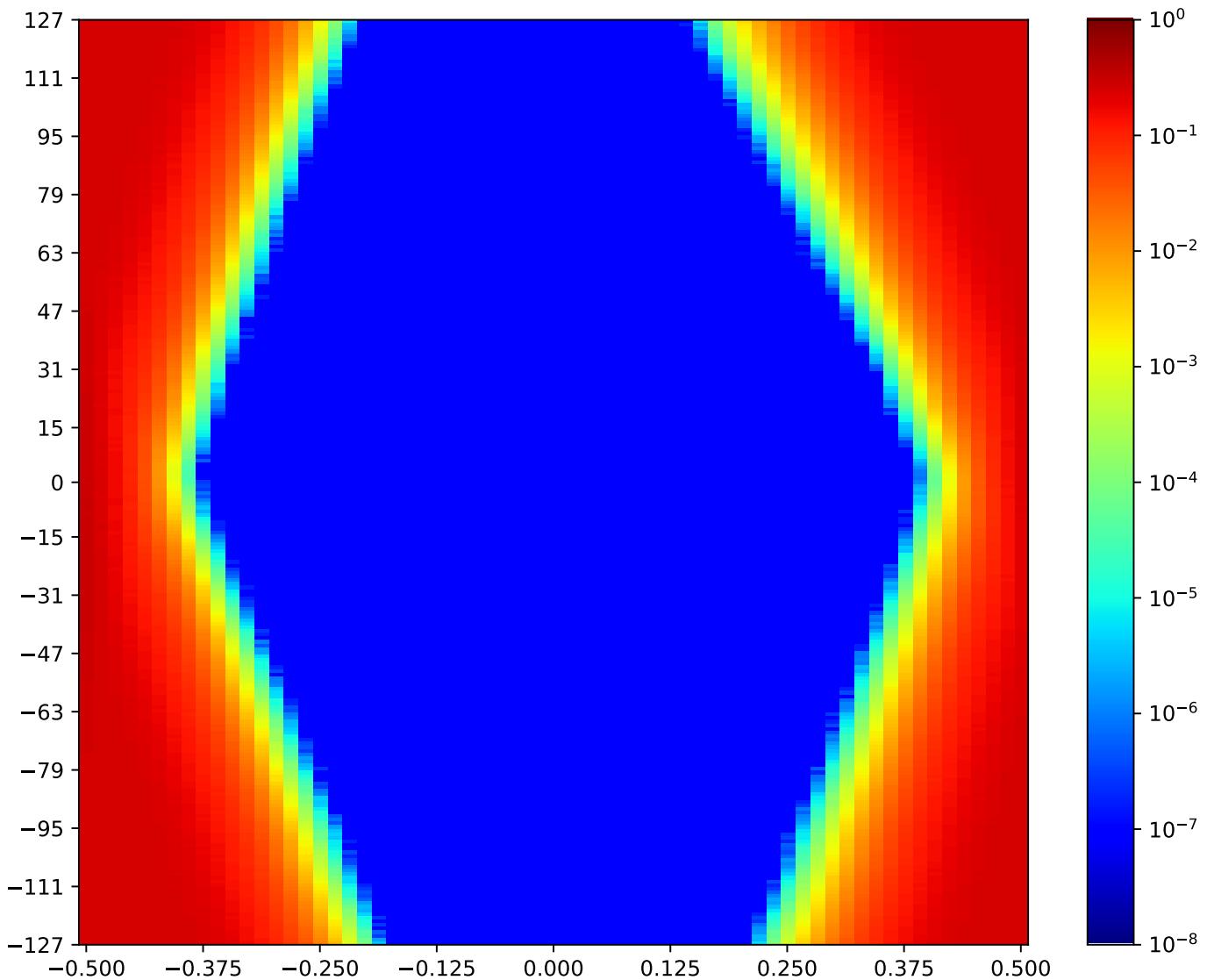


Figure 2.80: MSP\_A\_FPGA-IC39-10-IC4-10-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.12 MSP\_A\_FPGA-IC39-11-IC4-11-TRP\_FPGA

Table 2.73: MSP\_A\_FPGA-IC39-11-IC4-11-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:46:00		2018-Jan-24 19:46:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9889	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

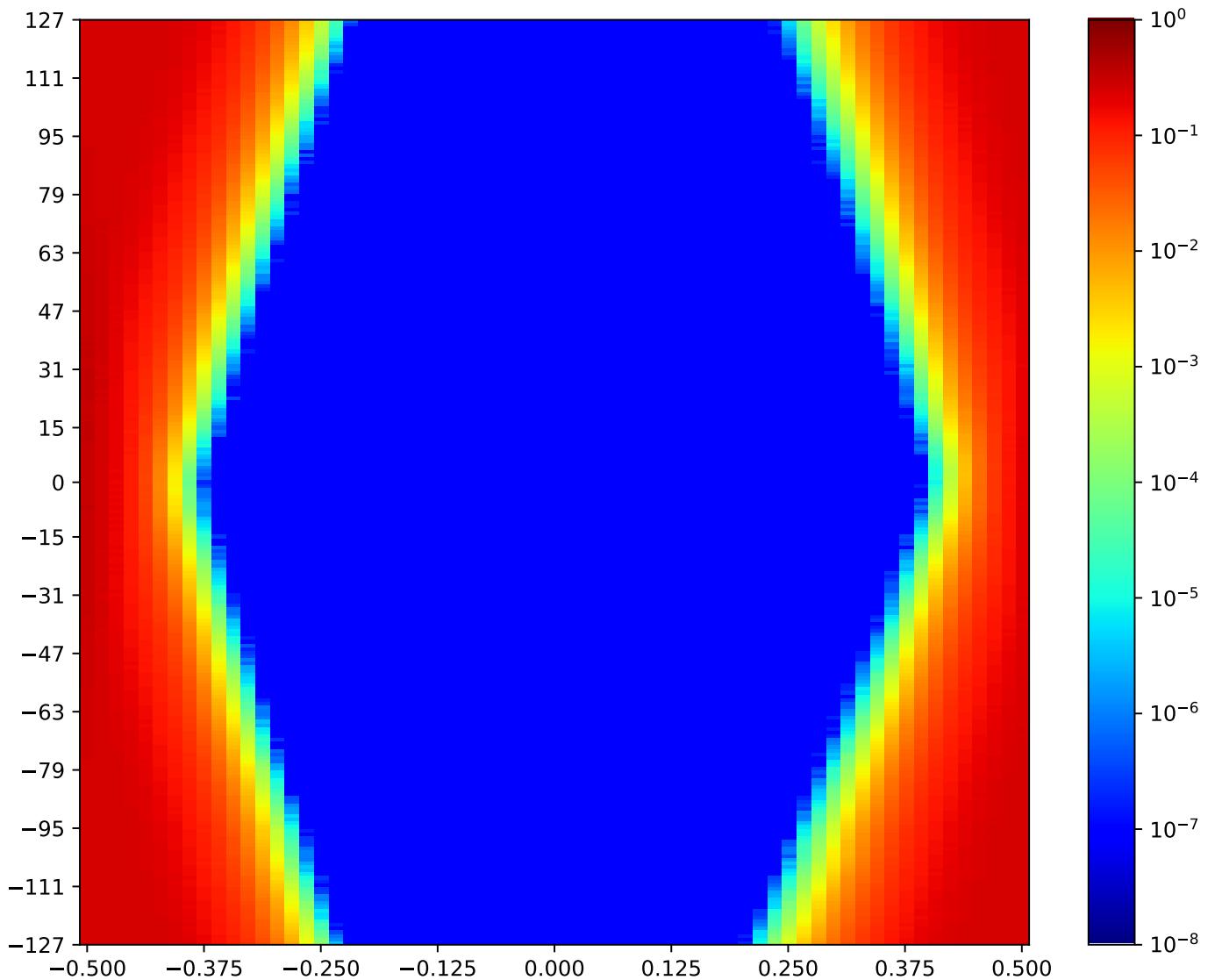


Figure 2.81: MSP\_A\_FPGA-IC39-11-IC4-11-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.13 MSP\_A\_FPGA-IC39-12-IC4-12-TRP\_FPGA

Table 2.74: MSP\_A\_FPGA-IC39-12-IC4-12-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:46:28		2018-Jan-24 19:46:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10600	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

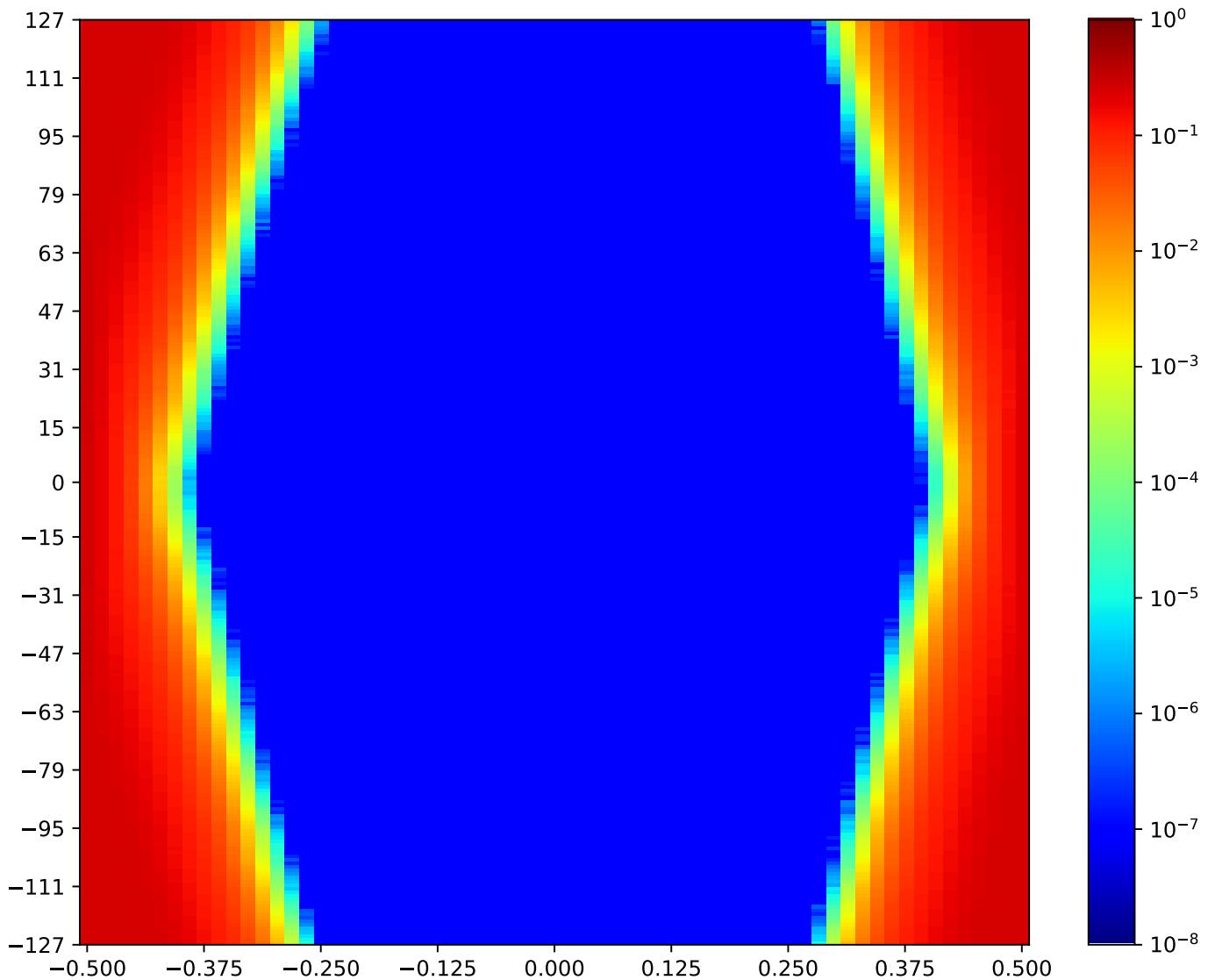


Figure 2.82: MSP\_A\_FPGA-IC39-12-IC4-12-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.14 MSP\_A\_FPGA-IC39-13-IC4-13-TRP\_FPGA

Table 2.75: MSP\_A\_FPGA-IC39-13-IC4-13-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:46:58		2018-Jan-24 19:47:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10907	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

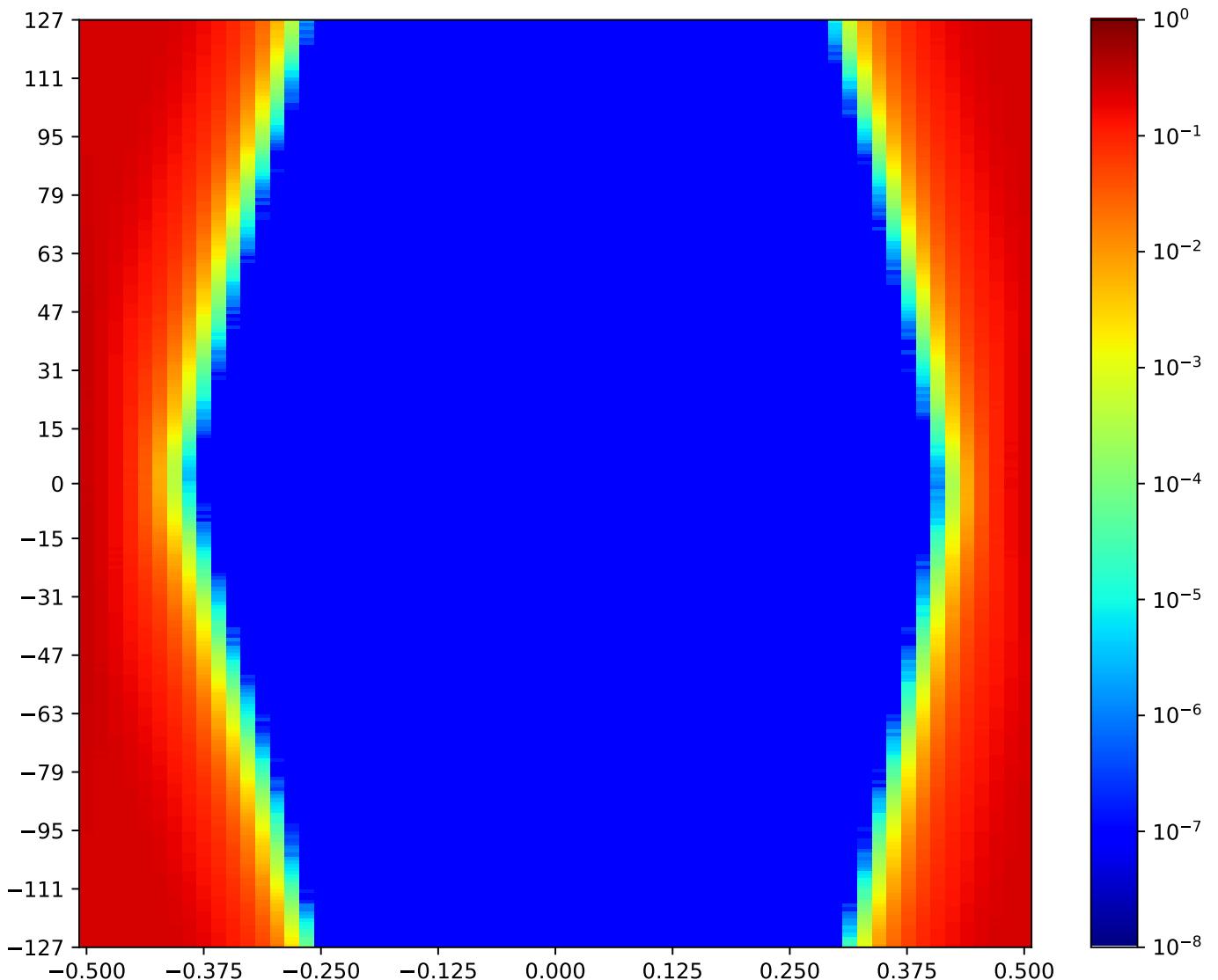


Figure 2.83: MSP\_A\_FPGA-IC39-13-IC4-13-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.15 MSP\_A\_FPGA-IC39-14-IC4-14-TRP\_FPGA

Table 2.76: MSP\_A\_FPGA-IC39-14-IC4-14-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:47:27		2018-Jan-24 19:47:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10560	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

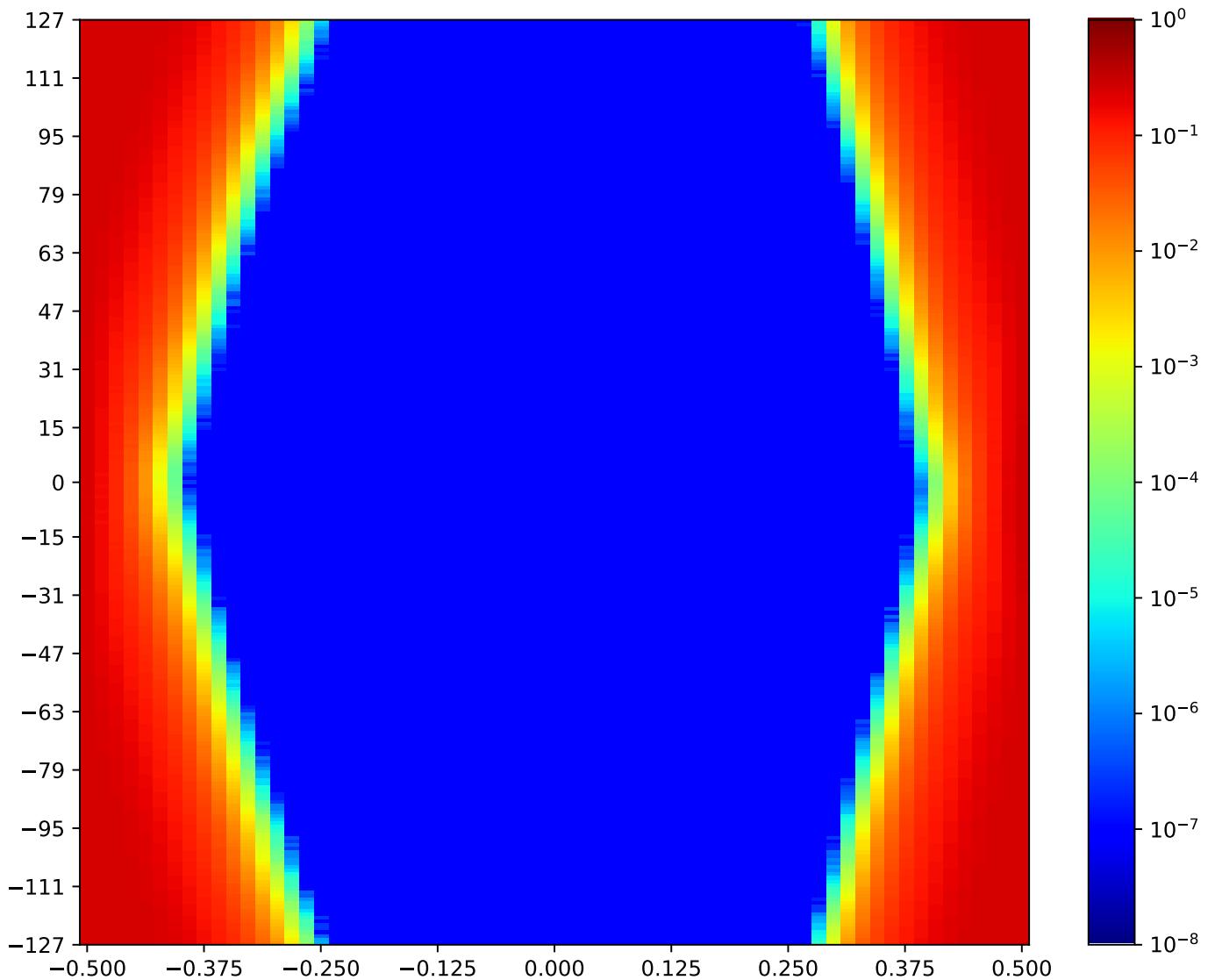


Figure 2.84: MSP\_A\_FPGA-IC39-14-IC4-14-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.16 MSP\_A\_FPGA-IC39-15-IC4-15-TRP\_FPGA

Table 2.77: MSP\_A\_FPGA-IC39-15-IC4-15-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:47:57		2018-Jan-24 19:48:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10773	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

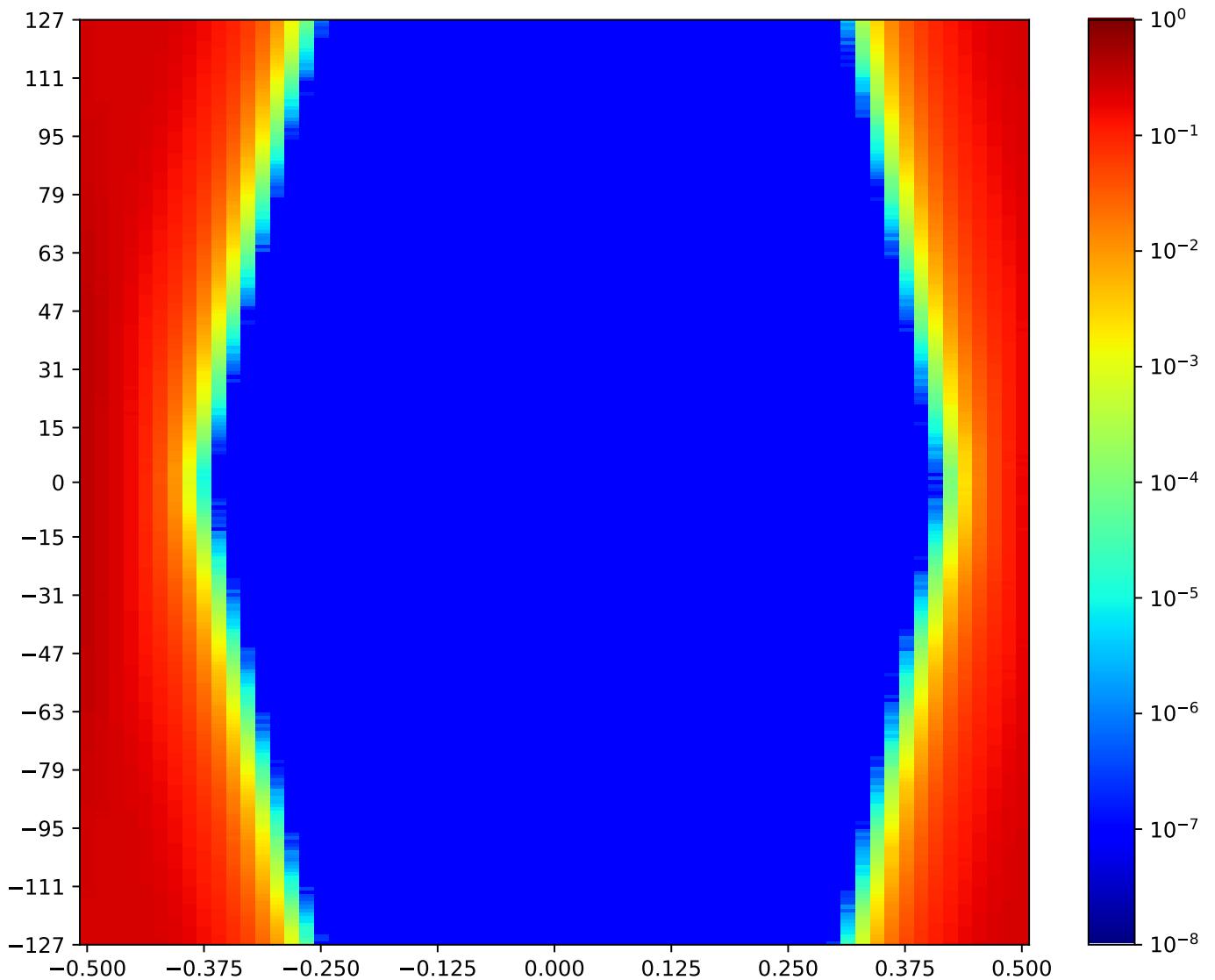


Figure 2.85: MSP\_A\_FPGA-IC39-15-IC4-15-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.17 MSP\_A\_FPGA-IC39-16-IC4-16-TRP\_FPGA

Table 2.78: MSP\_A\_FPGA-IC39-16-IC4-16-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:48:26		2018-Jan-24 19:48:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10354	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

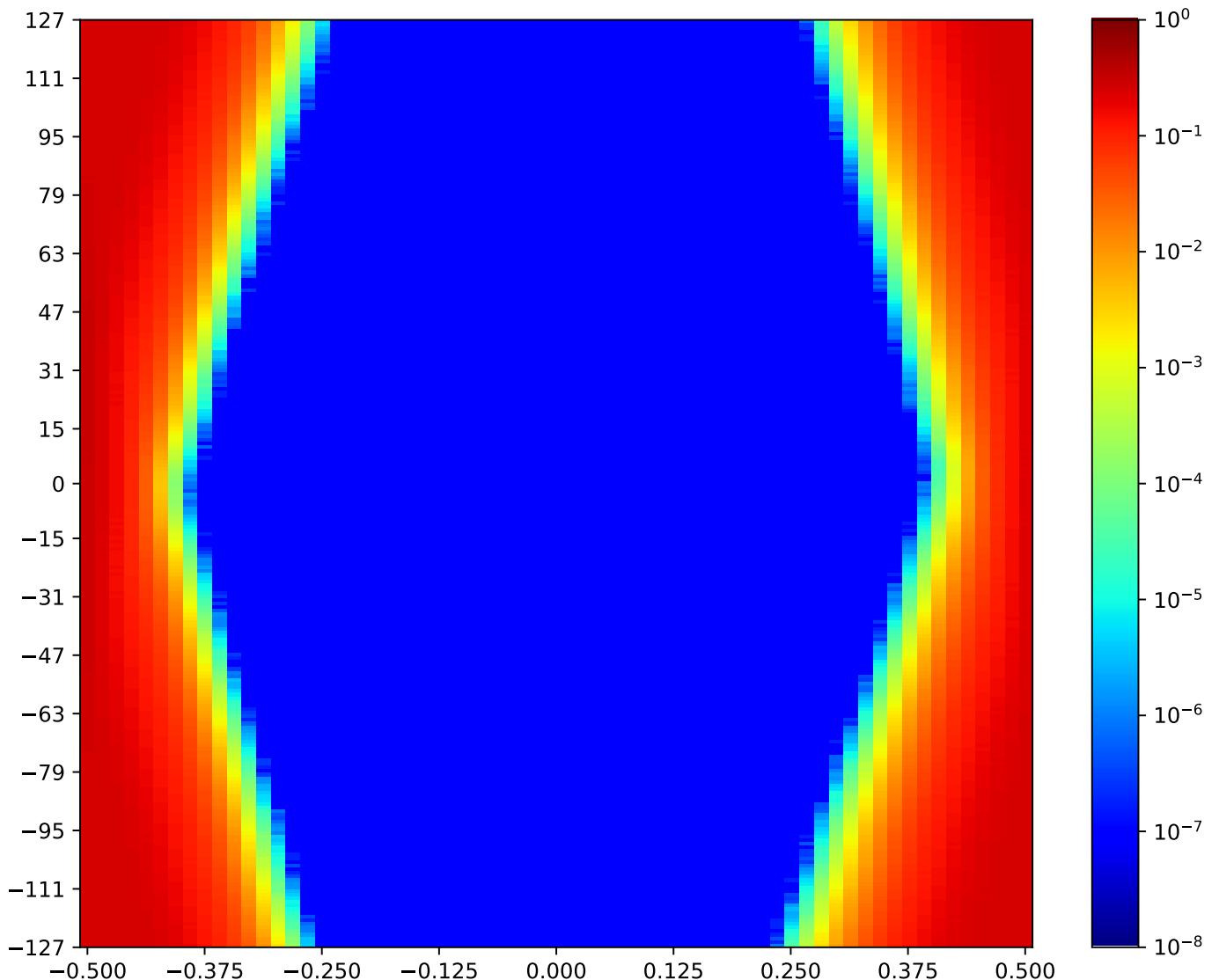


Figure 2.86: MSP\_A\_FPGA-IC39-16-IC4-16-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.18 MSP\_A\_FPGA-IC39-17-IC4-17-TRP\_FPGA

Table 2.79: MSP\_A\_FPGA-IC39-17-IC4-17-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:48:56		2018-Jan-24 19:49:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10219	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

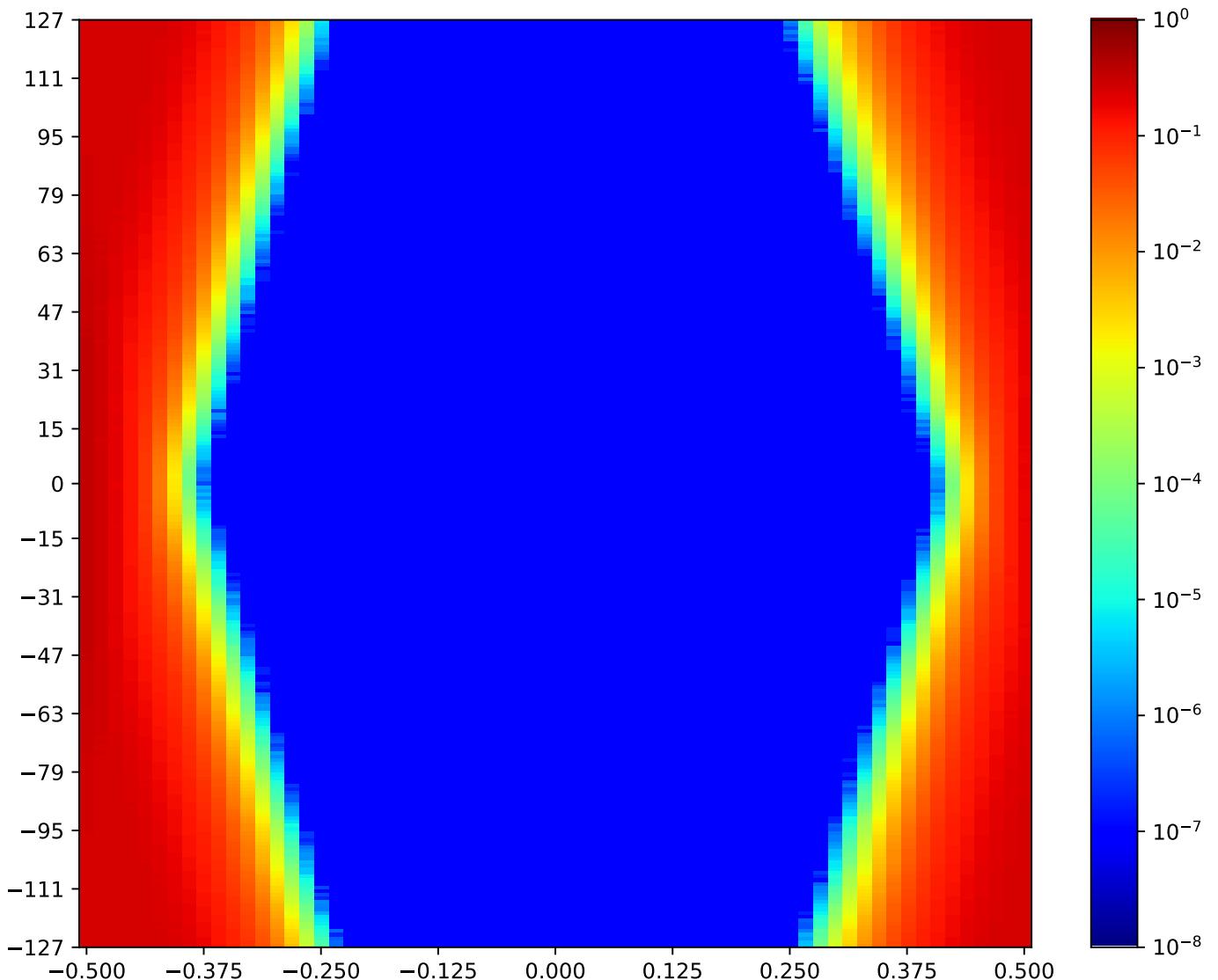


Figure 2.87: MSP\_A\_FPGA-IC39-17-IC4-17-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.19 MSP\_A\_FPGA-IC39-18-IC4-18-TRP\_FPGA

Table 2.80: MSP\_A\_FPGA-IC39-18-IC4-18-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:49:26		2018-Jan-24 19:49:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9838	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

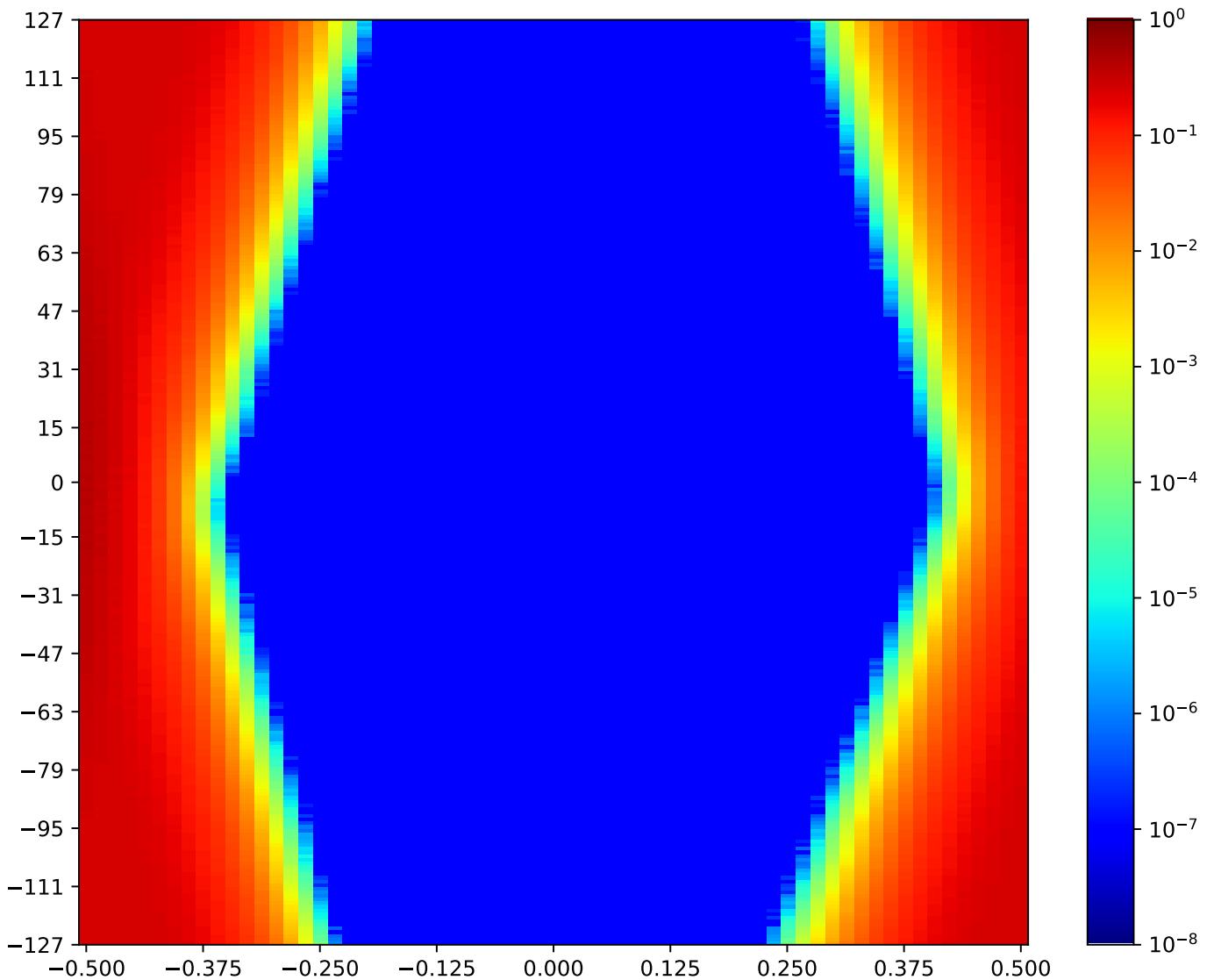


Figure 2.88: MSP\_A\_FPGA-IC39-18-IC4-18-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.20 MSP\_A\_FPGA-IC39-19-IC4-19-TRP\_FPGA

Table 2.81: MSP\_A\_FPGA-IC39-19-IC4-19-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:49:54		2018-Jan-24 19:50:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10690	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

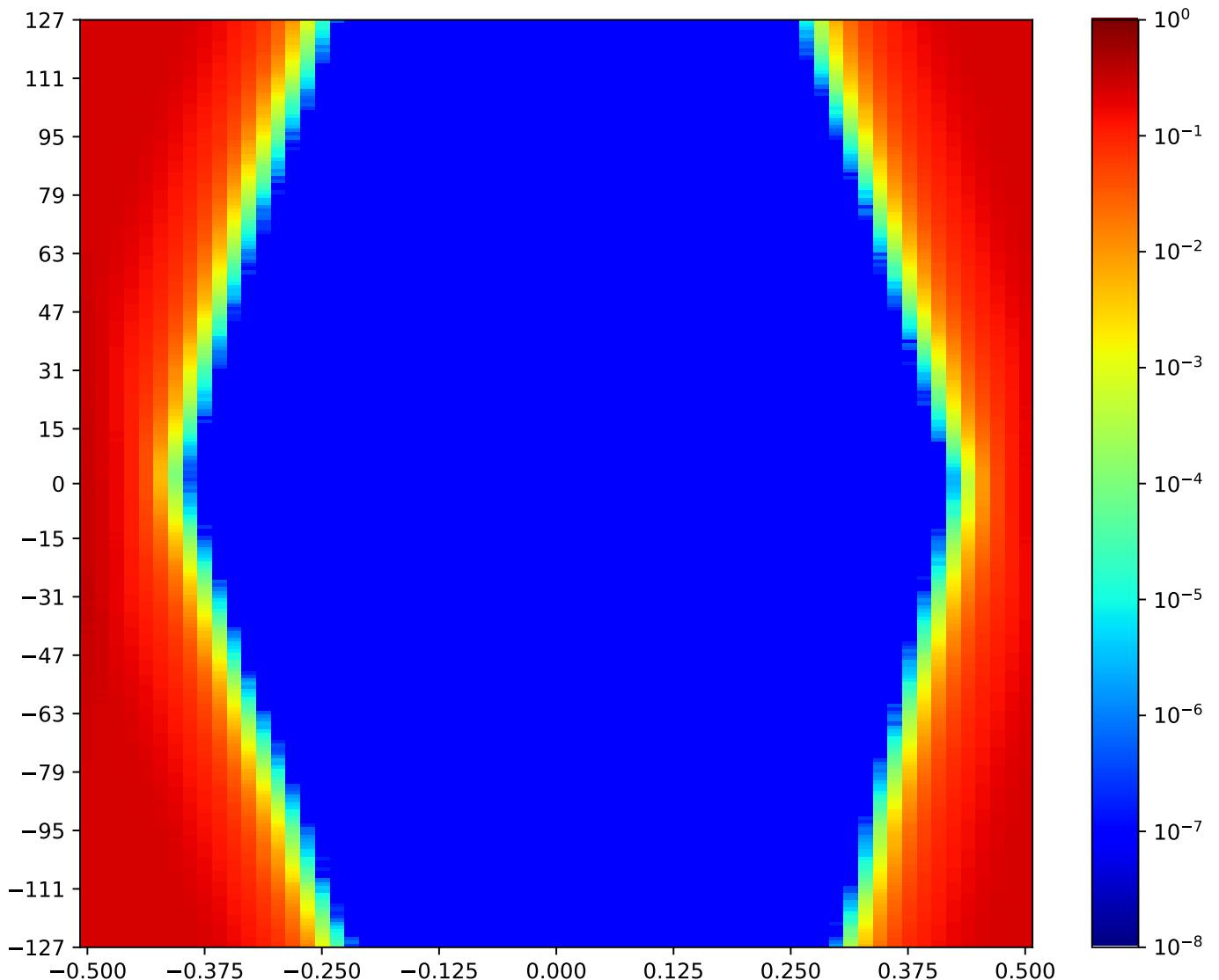


Figure 2.89: MSP\_A\_FPGA-IC39-19-IC4-19-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.21 MSP\_A\_FPGA-IC39-20-IC4-20-TRP\_FPGA

Table 2.82: MSP\_A\_FPGA-IC39-20-IC4-20-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:50:24		2018-Jan-24 19:50:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11262	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

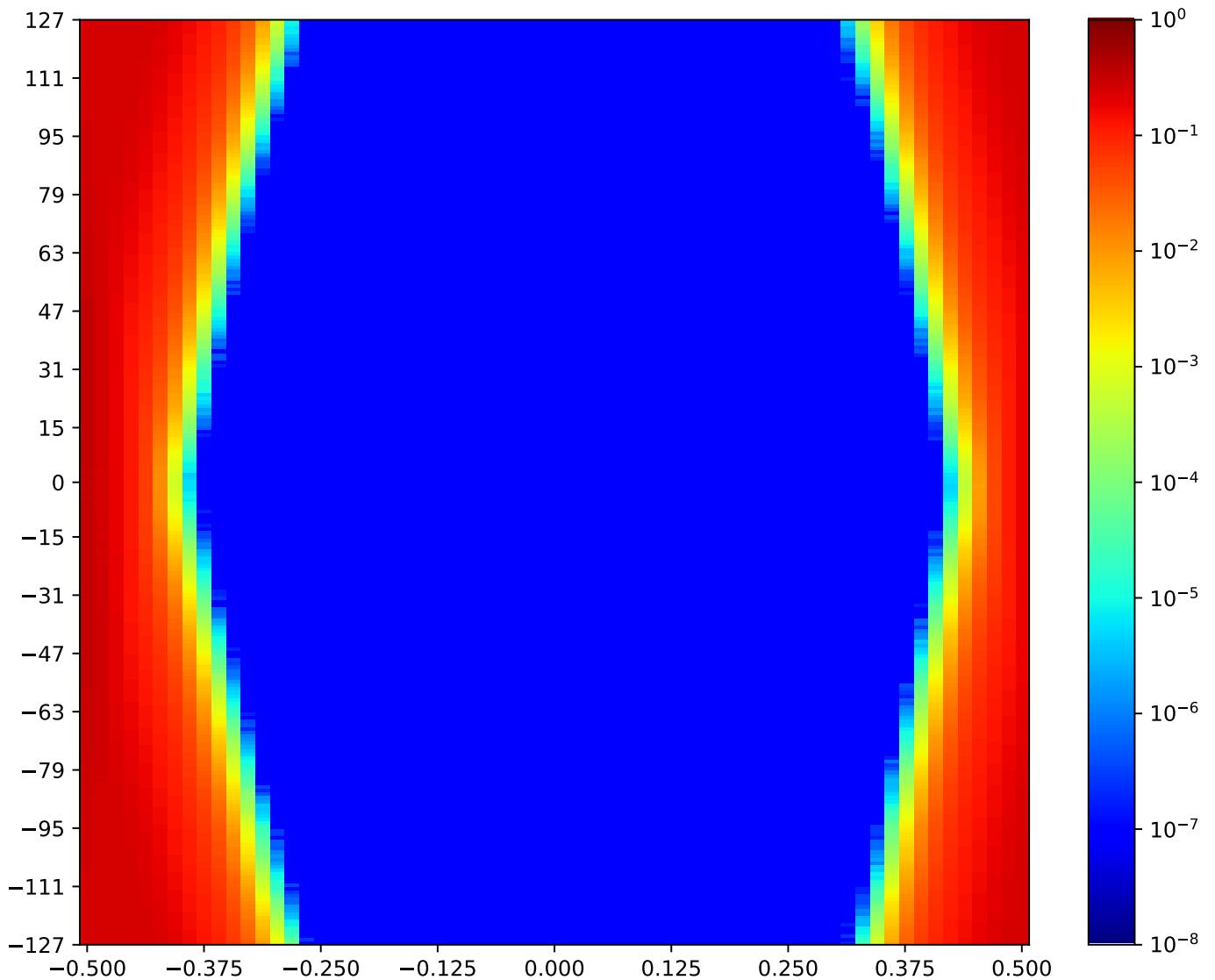


Figure 2.90: MSP\_A\_FPGA-IC39-20-IC4-20-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.22 MSP\_A\_FPGA-IC39-21-IC4-21-TRP\_FPGA

Table 2.83: MSP\_A\_FPGA-IC39-21-IC4-21-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:50:54		2018-Jan-24 19:51:23	
Reset RX	OA	HO		VO   VO (%)	
true	9448	49		75.38%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

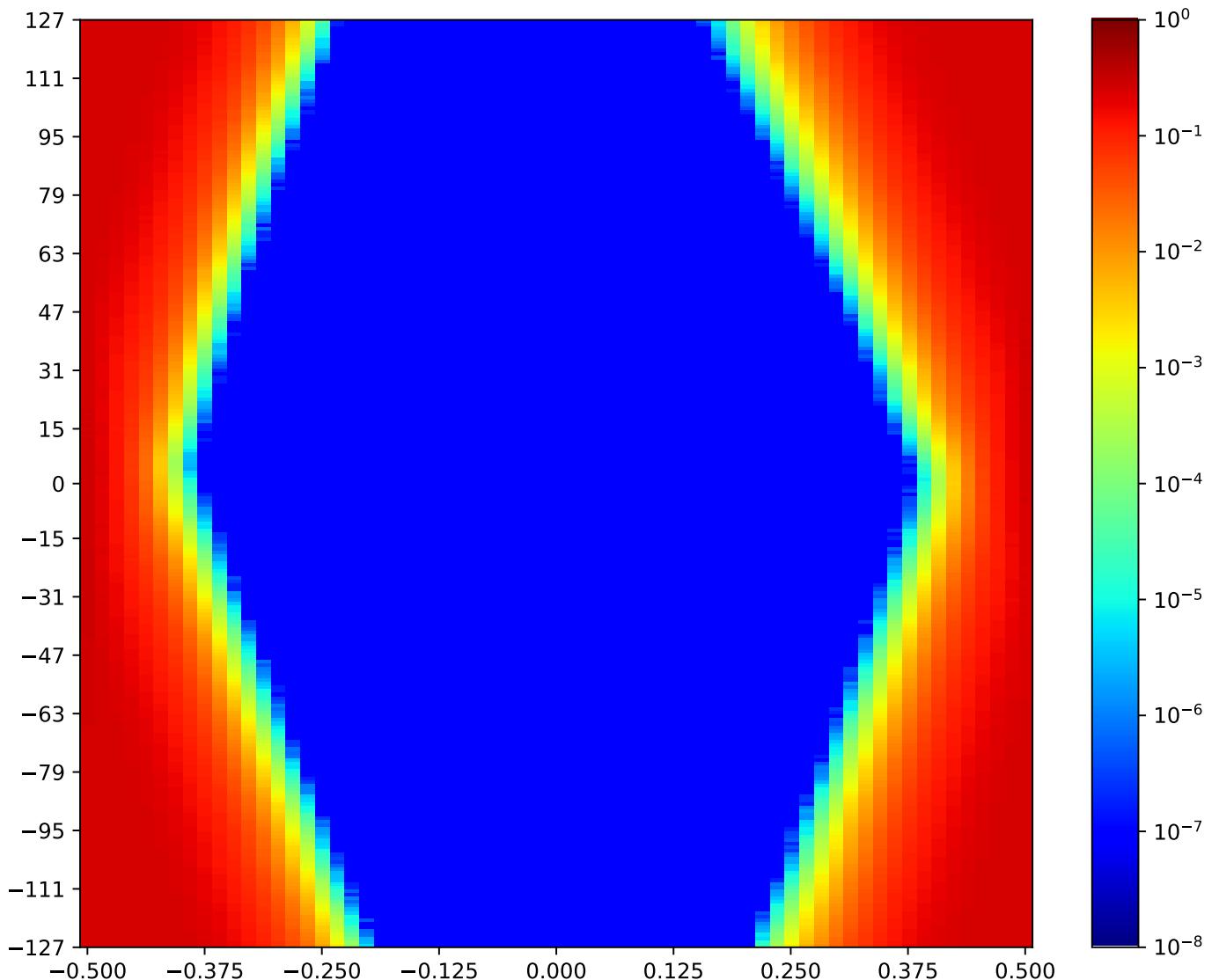


Figure 2.91: MSP\_A\_FPGA-IC39-21-IC4-21-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.23 MSP\_A\_FPGA-IC39-22-IC4-22-TRP\_FPGA

Table 2.84: MSP\_A\_FPGA-IC39-22-IC4-22-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:51:23		2018-Jan-24 19:51:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11199	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
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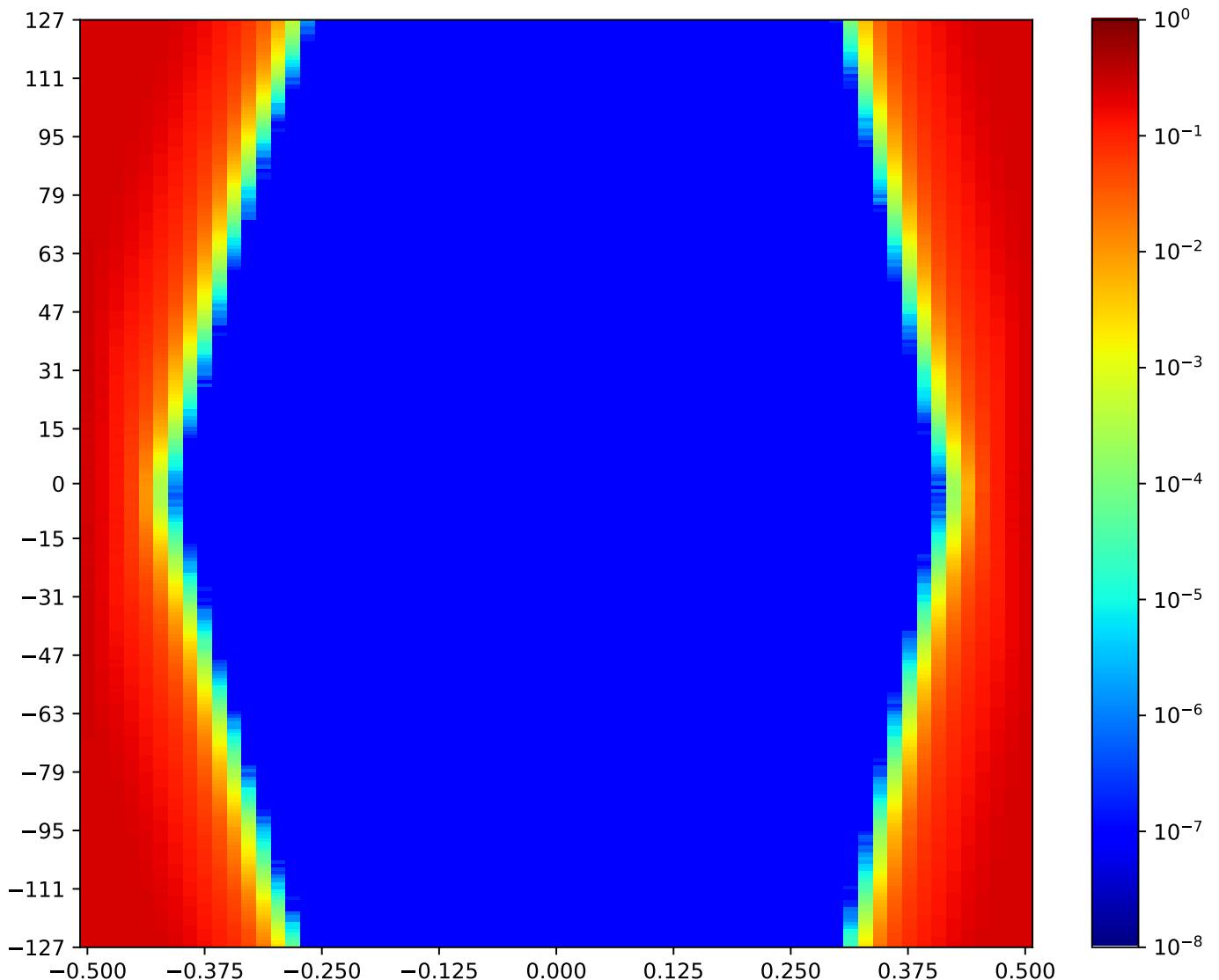


Figure 2.92: MSP\_A\_FPGA-IC39-22-IC4-22-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.24 MSP\_A\_FPGA-IC39-23-IC4-23-TRP\_FPGA

Table 2.85: MSP\_A\_FPGA-IC39-23-IC4-23-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:51:54		2018-Jan-24 19:52:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10877	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

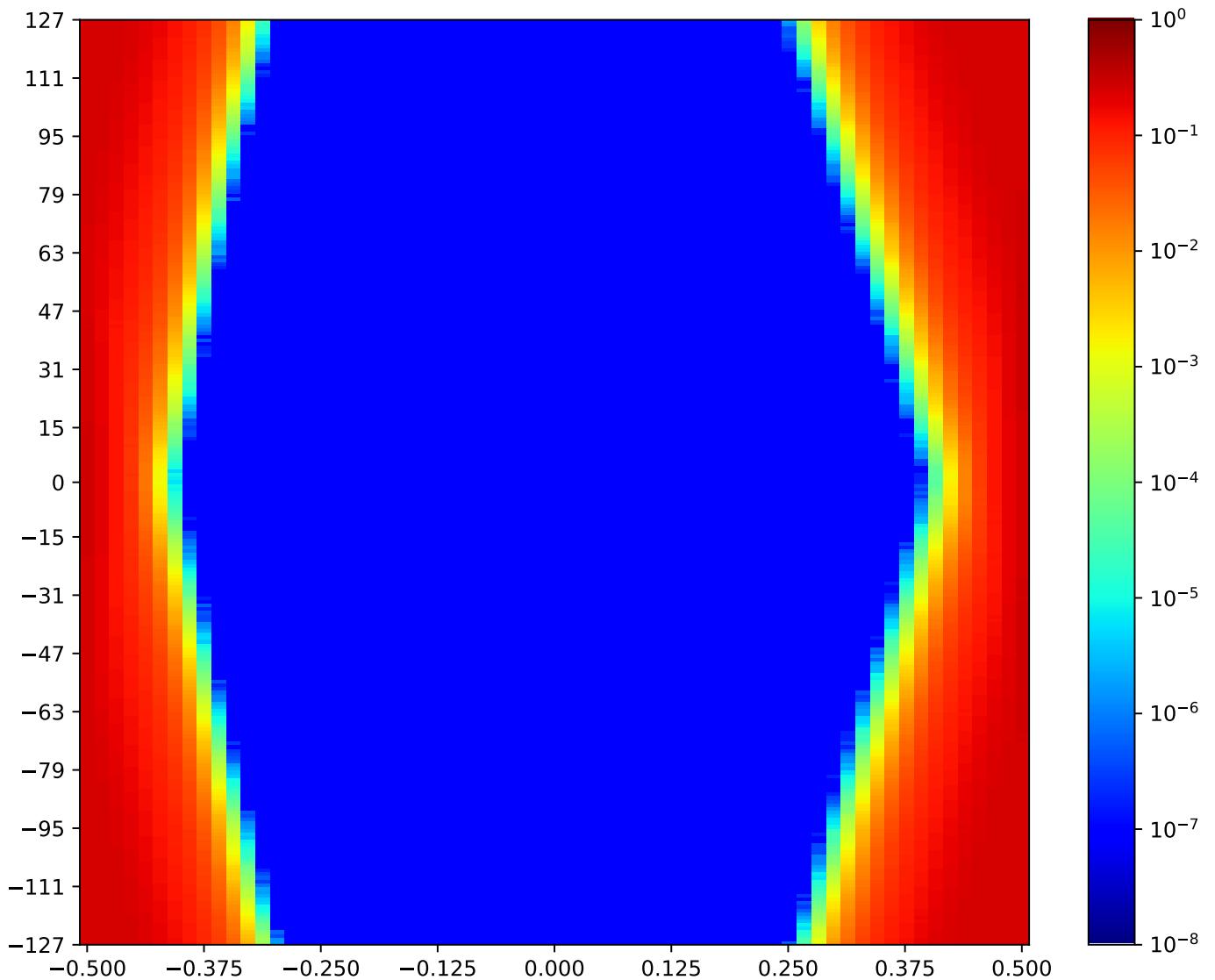


Figure 2.93: MSP\_A\_FPGA-IC39-23-IC4-23-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.25 MSP\_A\_FPGA-IC39-24-IC4-24-TRP\_FPGA

Table 2.86: MSP\_A\_FPGA-IC39-24-IC4-24-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:52:24		2018-Jan-24 19:52:53	
Reset RX	OA	HO		HO (%)	
true	10172	49		75.38%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

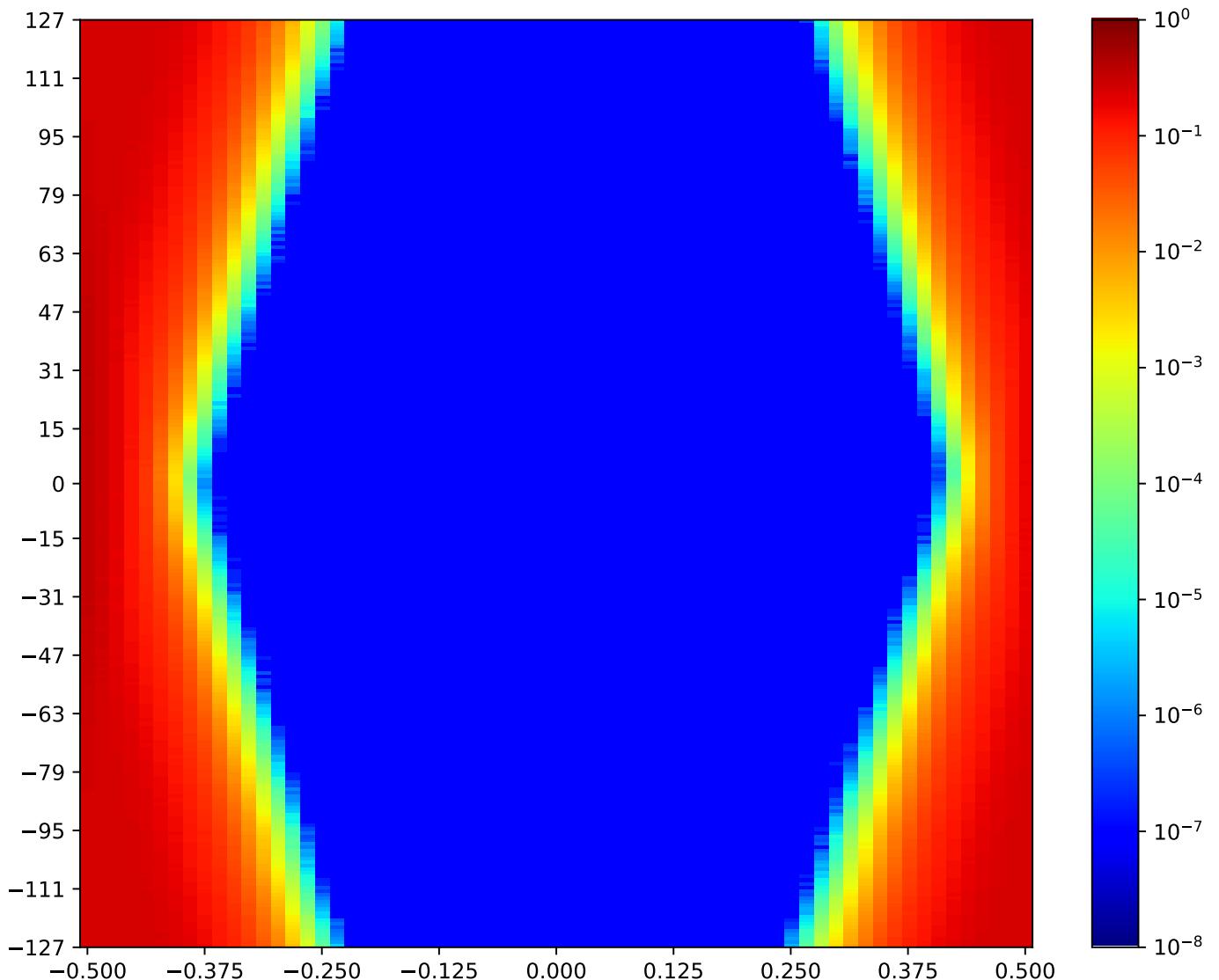


Figure 2.94: MSP\_A\_FPGA-IC39-24-IC4-24-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.26 MSP\_A\_FPGA-IC39-25-IC4-25-TRP\_FPGA

Table 2.87: MSP\_A\_FPGA-IC39-25-IC4-25-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:52:53		2018-Jan-24 19:53:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10692	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

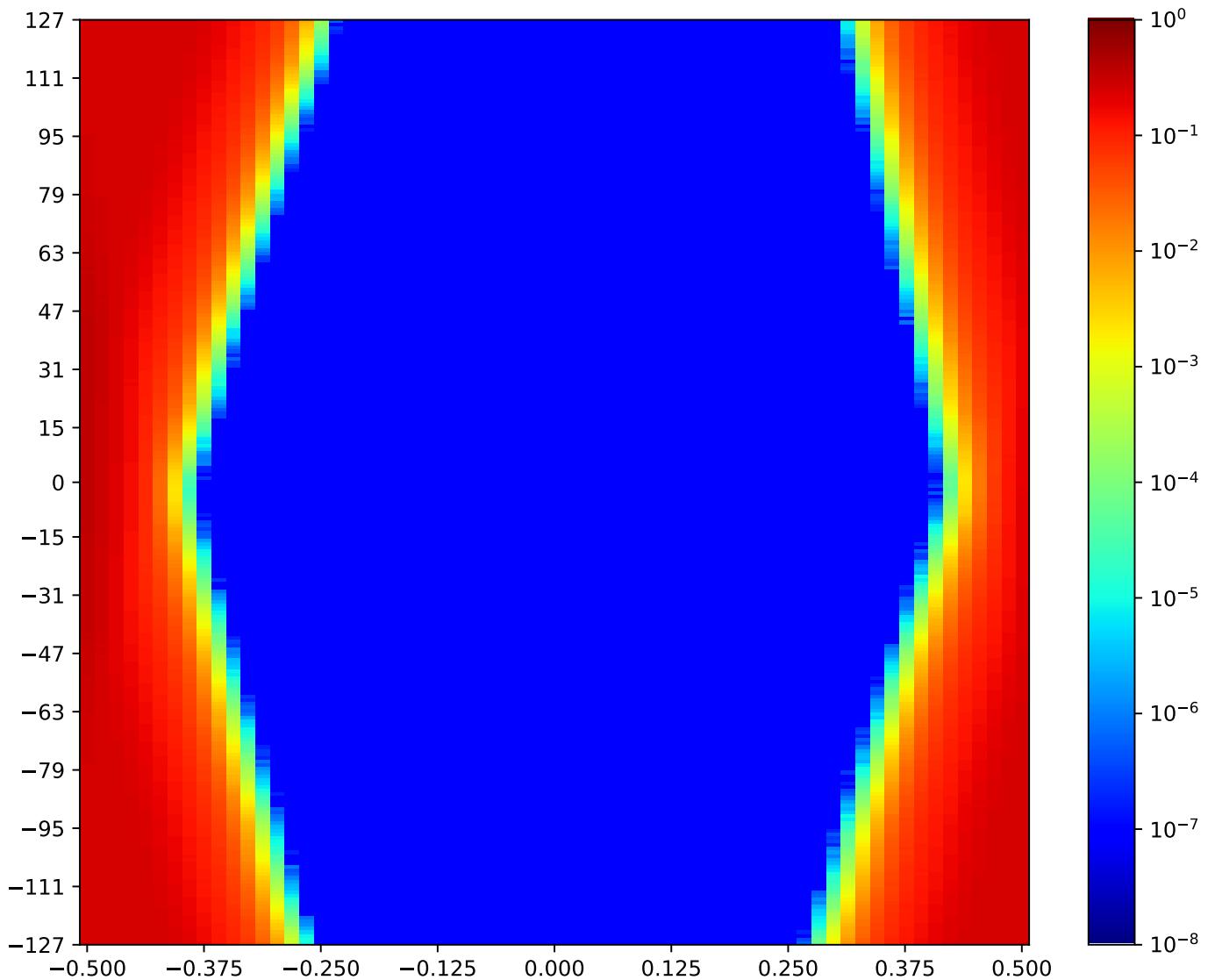


Figure 2.95: MSP\_A\_FPGA-IC39-25-IC4-25-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.8.27 MSP\_A\_FPGA-IC39-26-IC4-26-TRP\_FPGA

Table 2.88: MSP\_A\_FPGA-IC39-26-IC4-26-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:53:23		2018-Jan-24 19:53:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10254	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

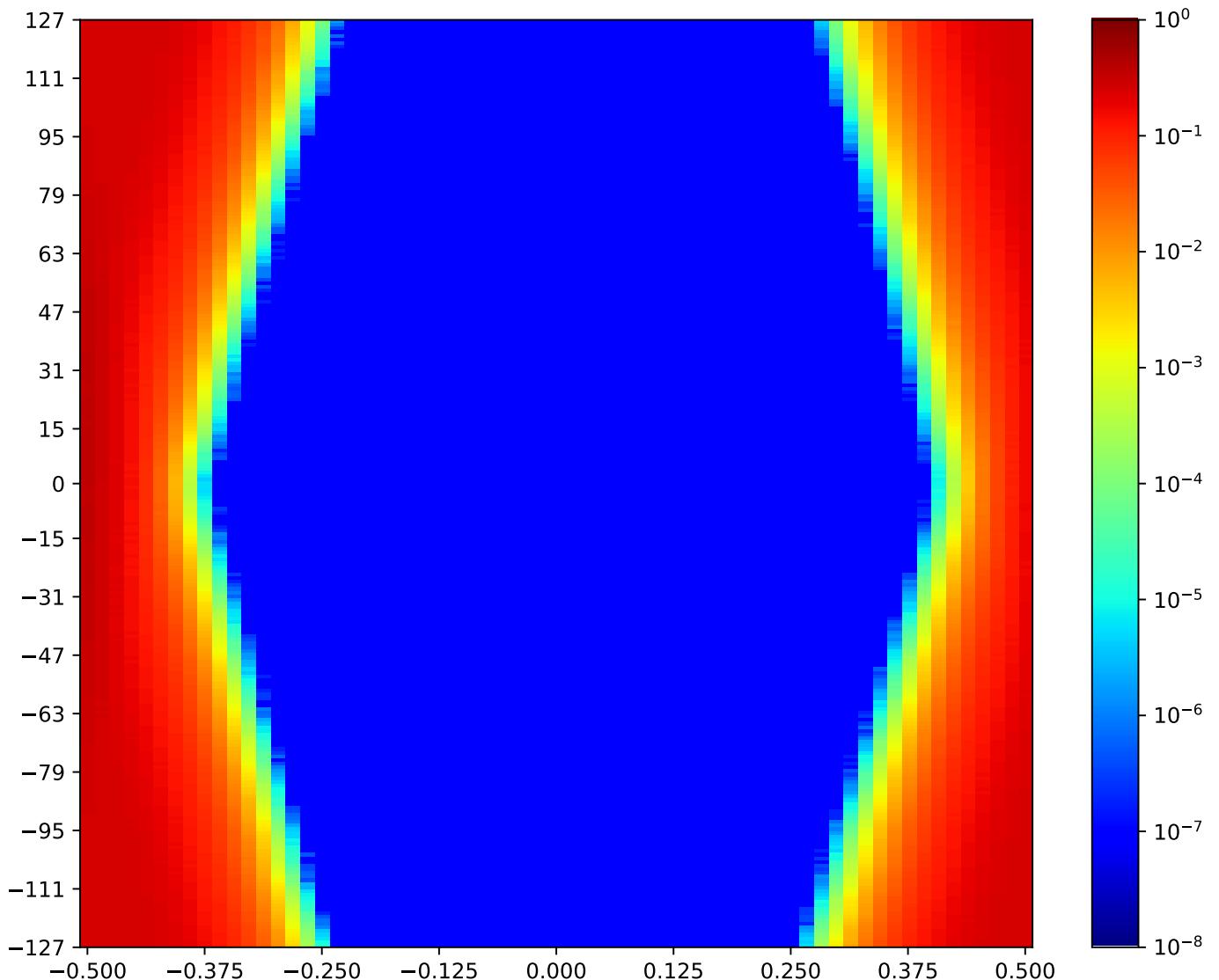


Figure 2.96: MSP\_A\_FPGA-IC39-26-IC4-26-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.8.28 MSP\_A\_FPGA-IC39-27-IC4-27-TRP\_FPGA

Table 2.89: MSP\_A\_FPGA-IC39-27-IC4-27-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 19:53:52		2018-Jan-24 19:54:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11072	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

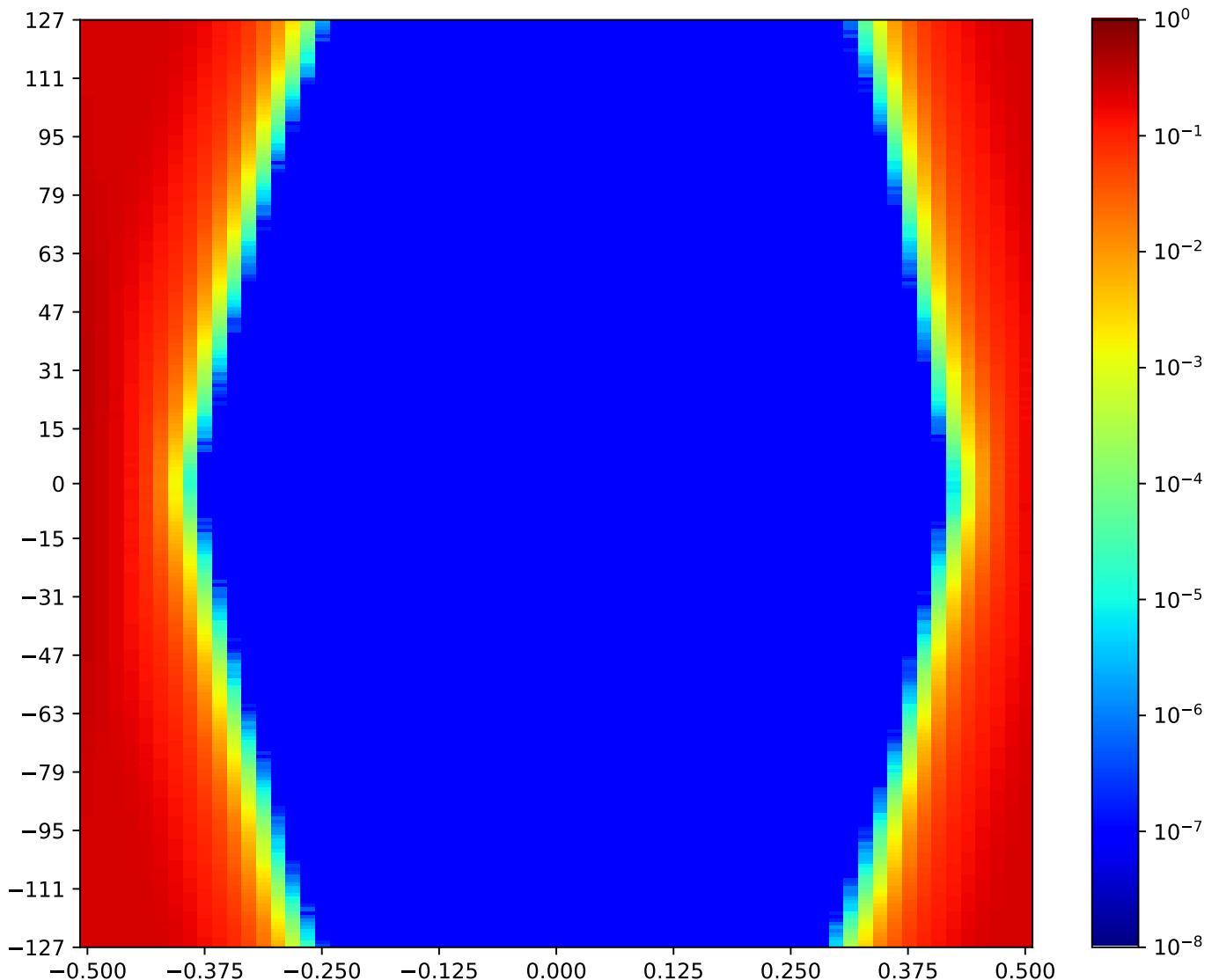


Figure 2.97: MSP\_A\_FPGA-IC39-27-IC4-27-TRP\_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9 MSP\_C TRP On board links

A cross-reference to Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.127.

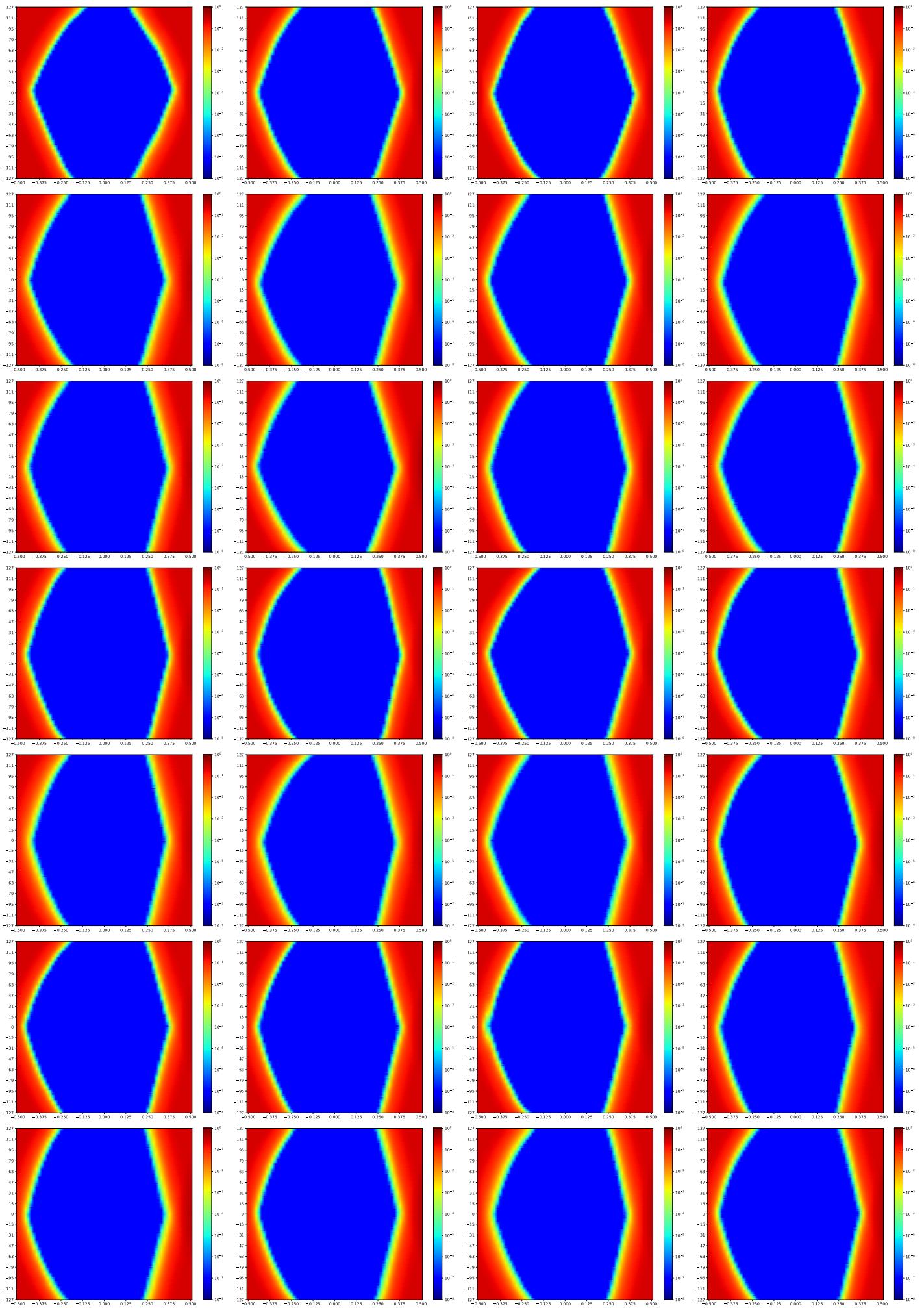


Figure 2.98: MSP\_C TRP On board links

### 2.9.1 MSP\_C\_FPGA-IC39-00-IC15-00-TRP\_FPGA

Table 2.90: MSP\_C\_FPGA-IC39-00-IC15-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:54:22		2018-Jan-24 19:54:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9068	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

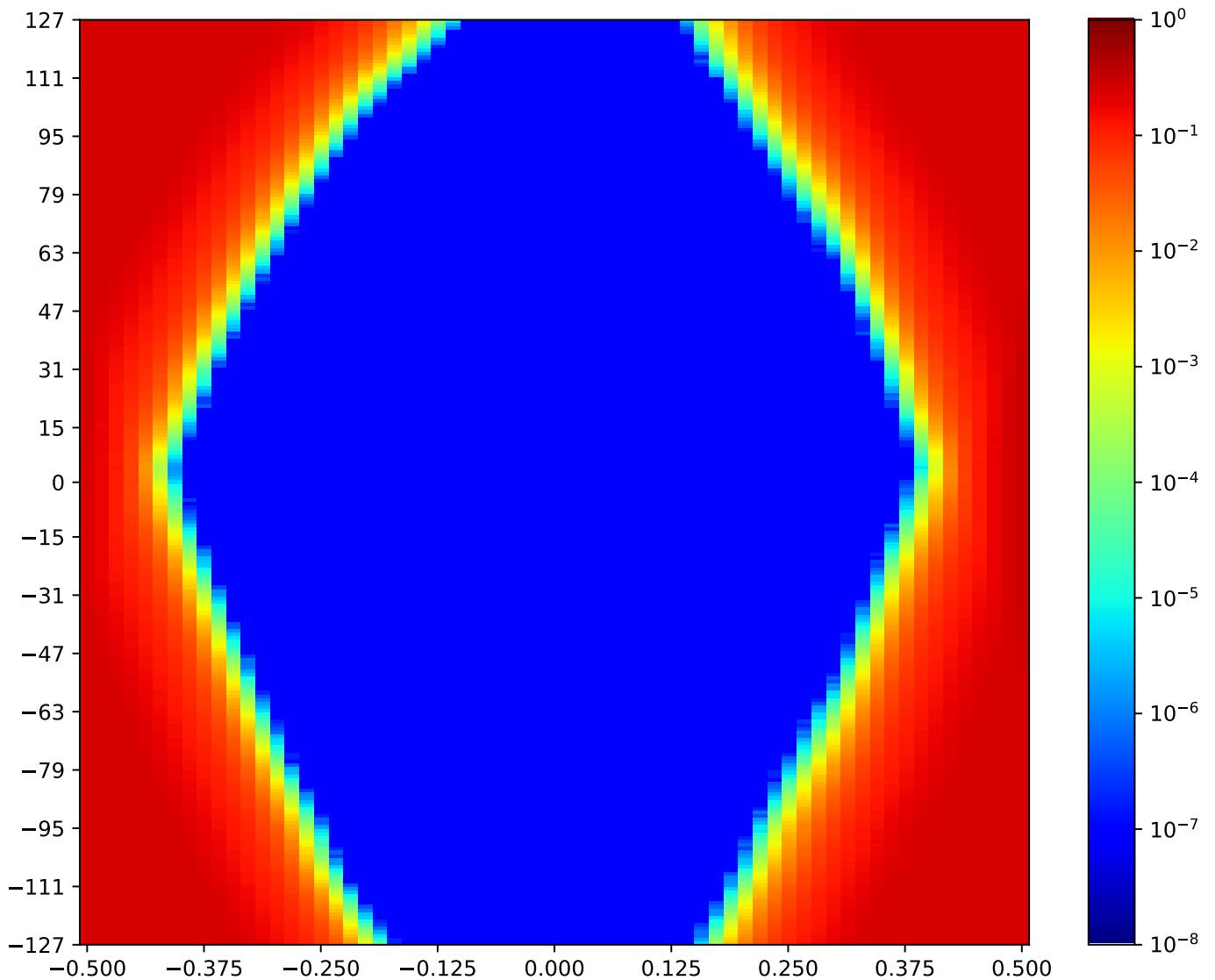


Figure 2.99: MSP\_C\_FPGA-IC39-00-IC15-00-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.2 MSP\_C\_FPGA-IC39-01-IC15-01-TRP\_FPGA

Table 2.91: MSP\_C\_FPGA-IC39-01-IC15-01-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:54:50		2018-Jan-24 19:55:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10067	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

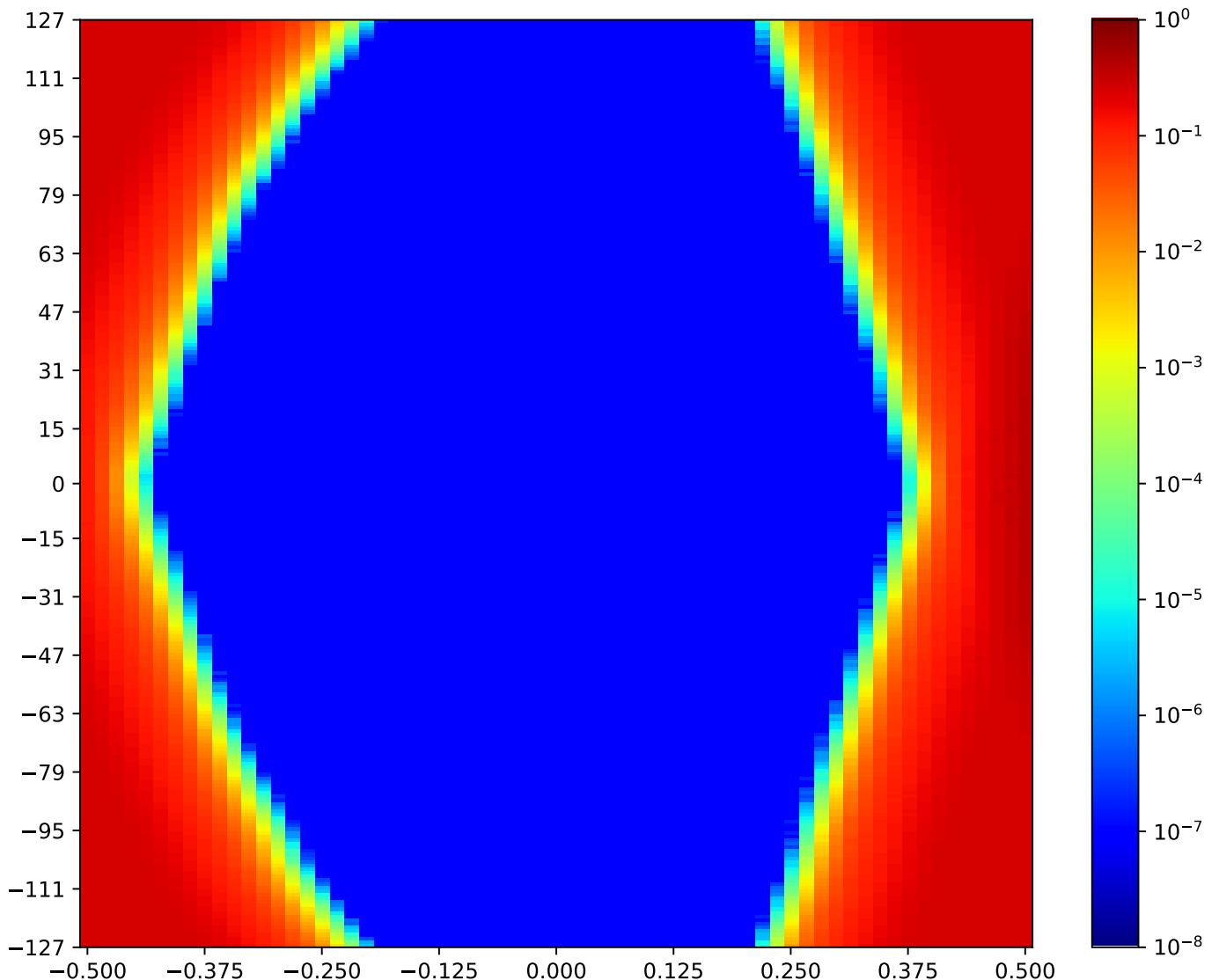


Figure 2.100: MSP\_C\_FPGA-IC39-01-IC15-01-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.3 MSP\_C\_FPGA-IC39-02-IC15-02-TRP\_FPGA

Table 2.92: MSP\_C\_FPGA-IC39-02-IC15-02-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:55:20		2018-Jan-24 19:55:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9819	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

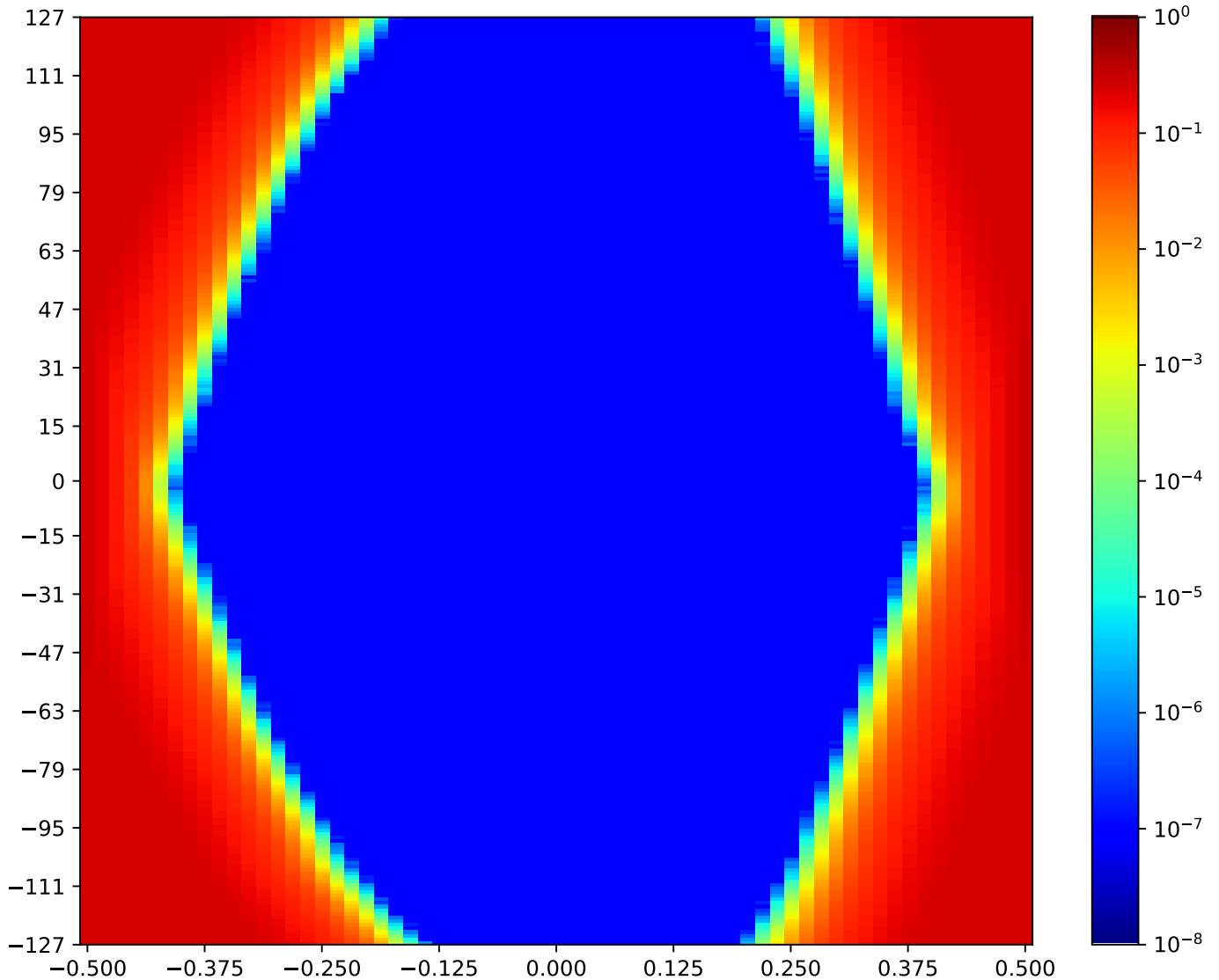


Figure 2.101: MSP\_C\_FPGA-IC39-02-IC15-02-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.4 MSP\_C\_FPGA-IC39-03-IC15-03-TRP\_FPGA

Table 2.93: MSP\_C\_FPGA-IC39-03-IC15-03-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:55:50		2018-Jan-24 19:56:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10451	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

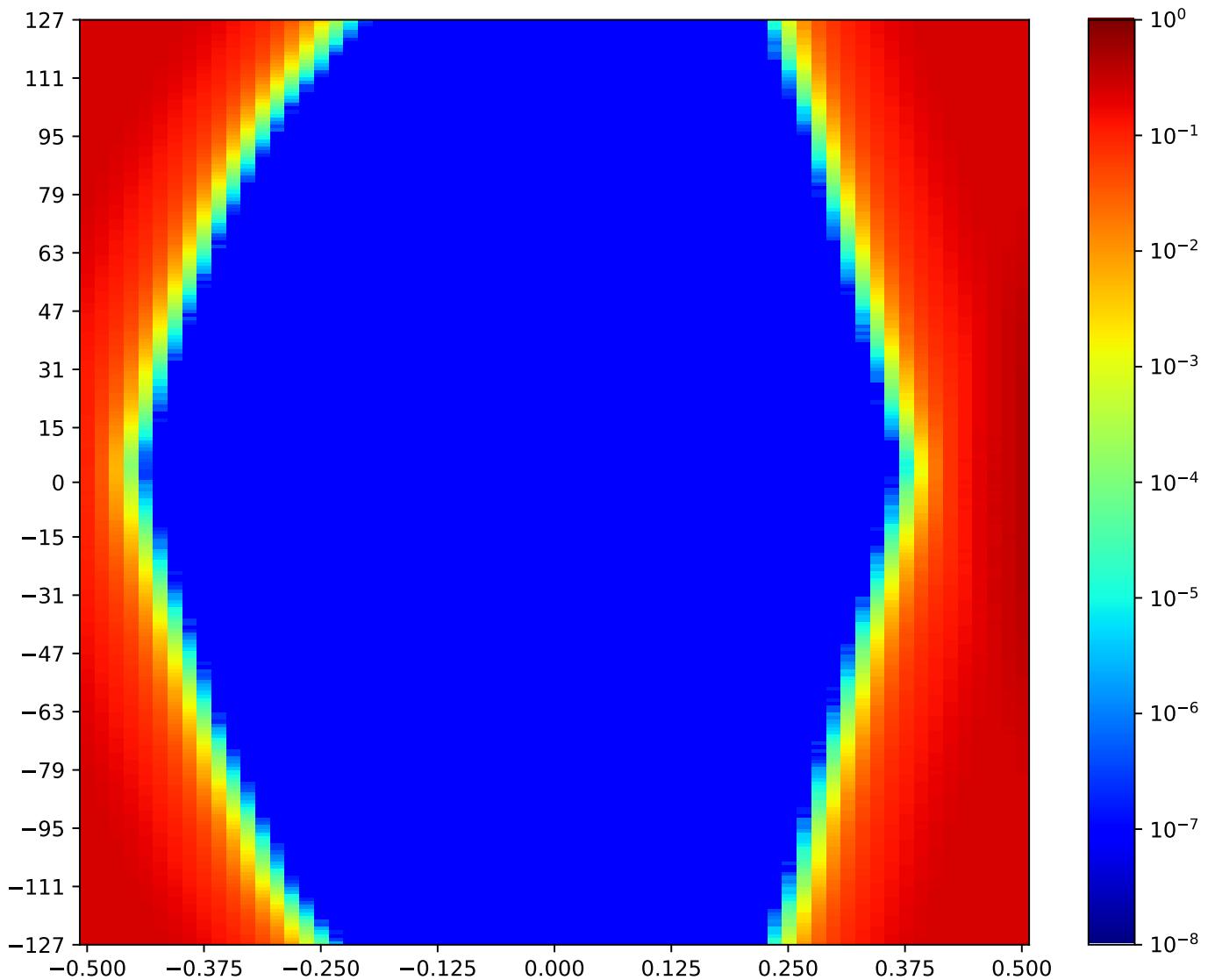


Figure 2.102: MSP\_C\_FPGA-IC39-03-IC15-03-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.5 MSP\_C\_FPGA-IC39-04-IC15-04-TRP\_FPGA

Table 2.94: MSP\_C\_FPGA-IC39-04-IC15-04-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:56:19		2018-Jan-24 19:56:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9507	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

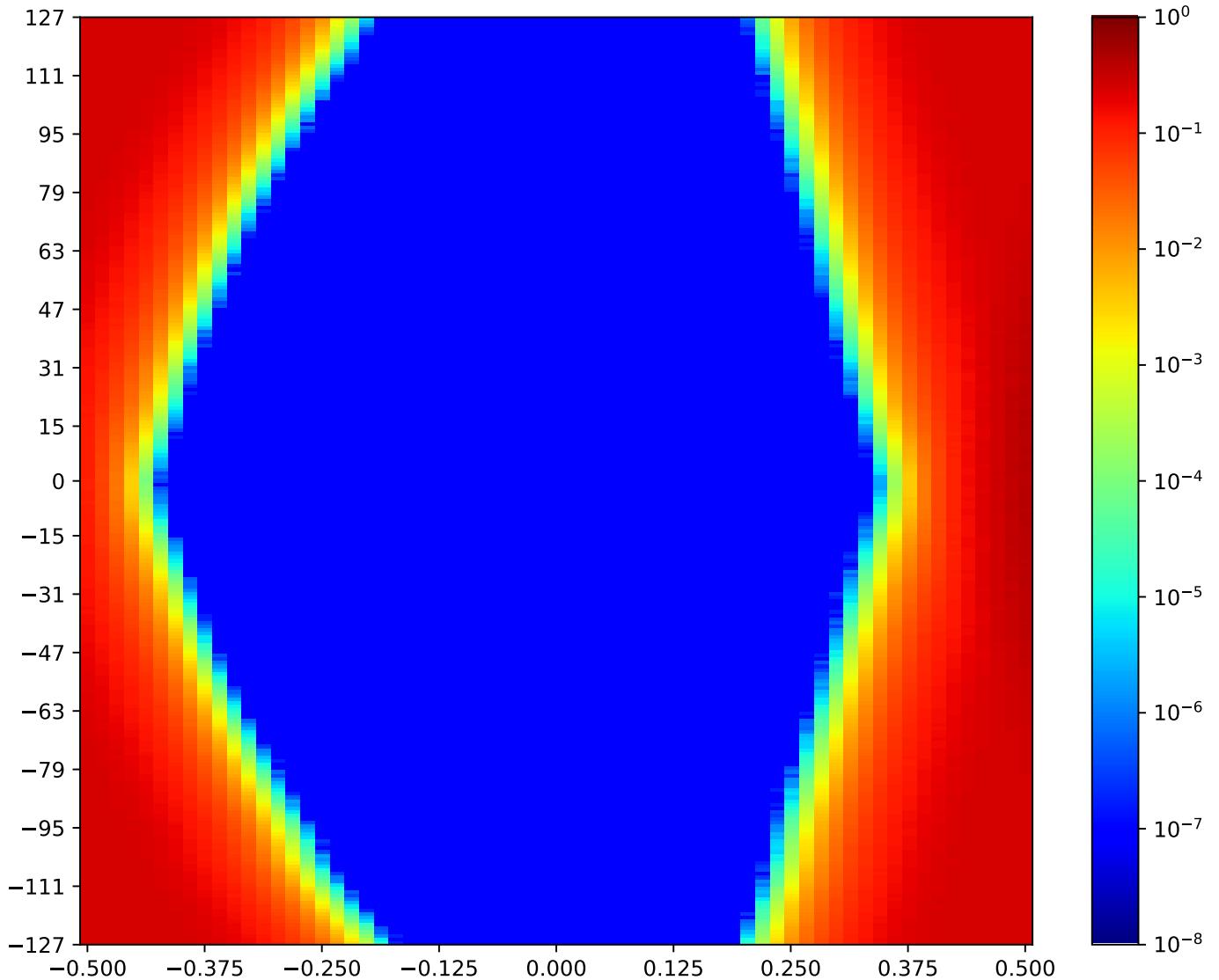


Figure 2.103: MSP\_C\_FPGA-IC39-04-IC15-04-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.6 MSP\_C\_FPGA-IC39-05-IC15-05-TRP\_FPGA

Table 2.95: MSP\_C\_FPGA-IC39-05-IC15-05-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:56:48		2018-Jan-24 19:57:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9567	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

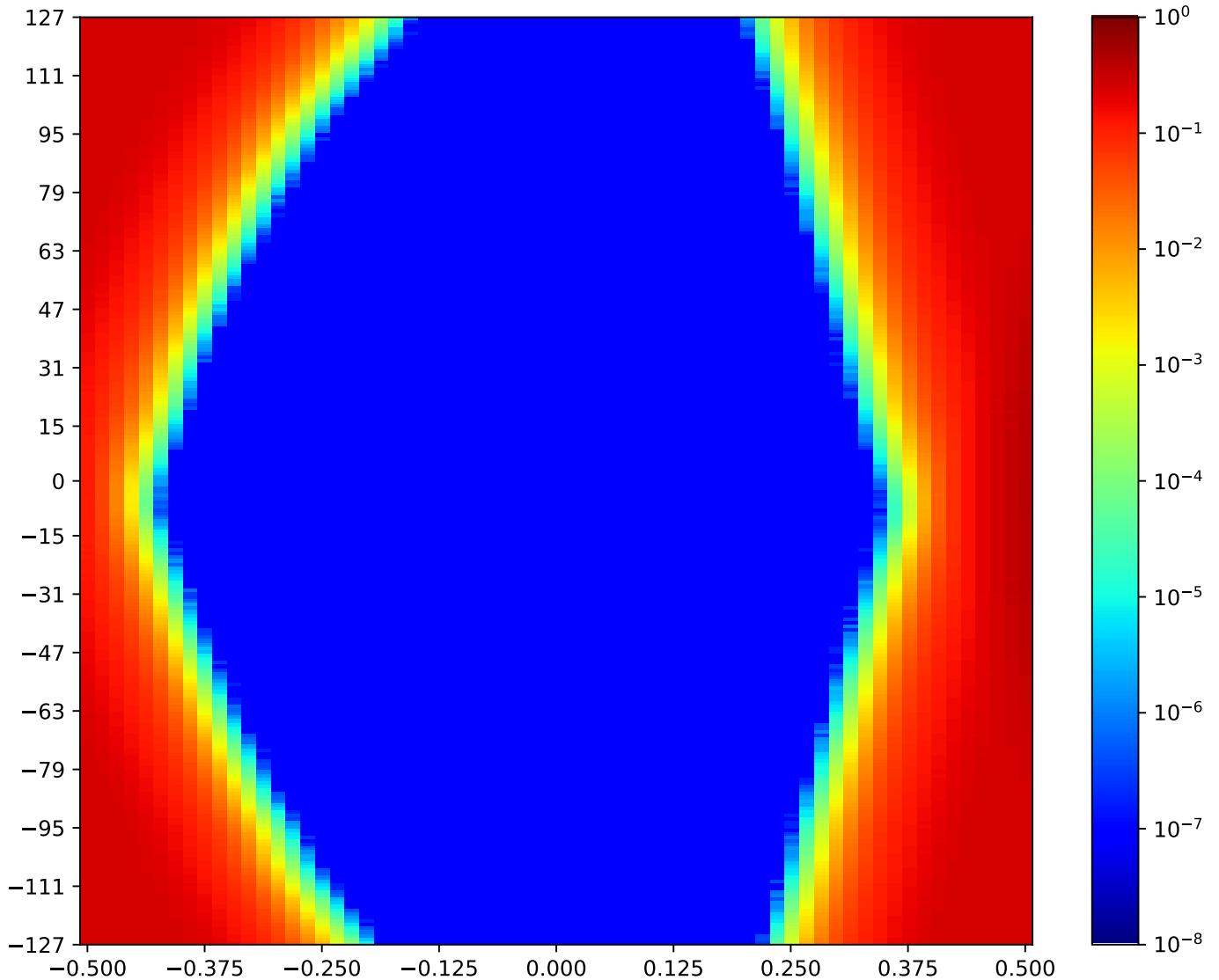


Figure 2.104: MSP\_C\_FPGA-IC39-05-IC15-05-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.7 MSP\_C\_FPGA-IC39-06-IC15-06-TRP\_FPGA

Table 2.96: MSP\_C\_FPGA-IC39-06-IC15-06-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:57:18		2018-Jan-24 19:57:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9893	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

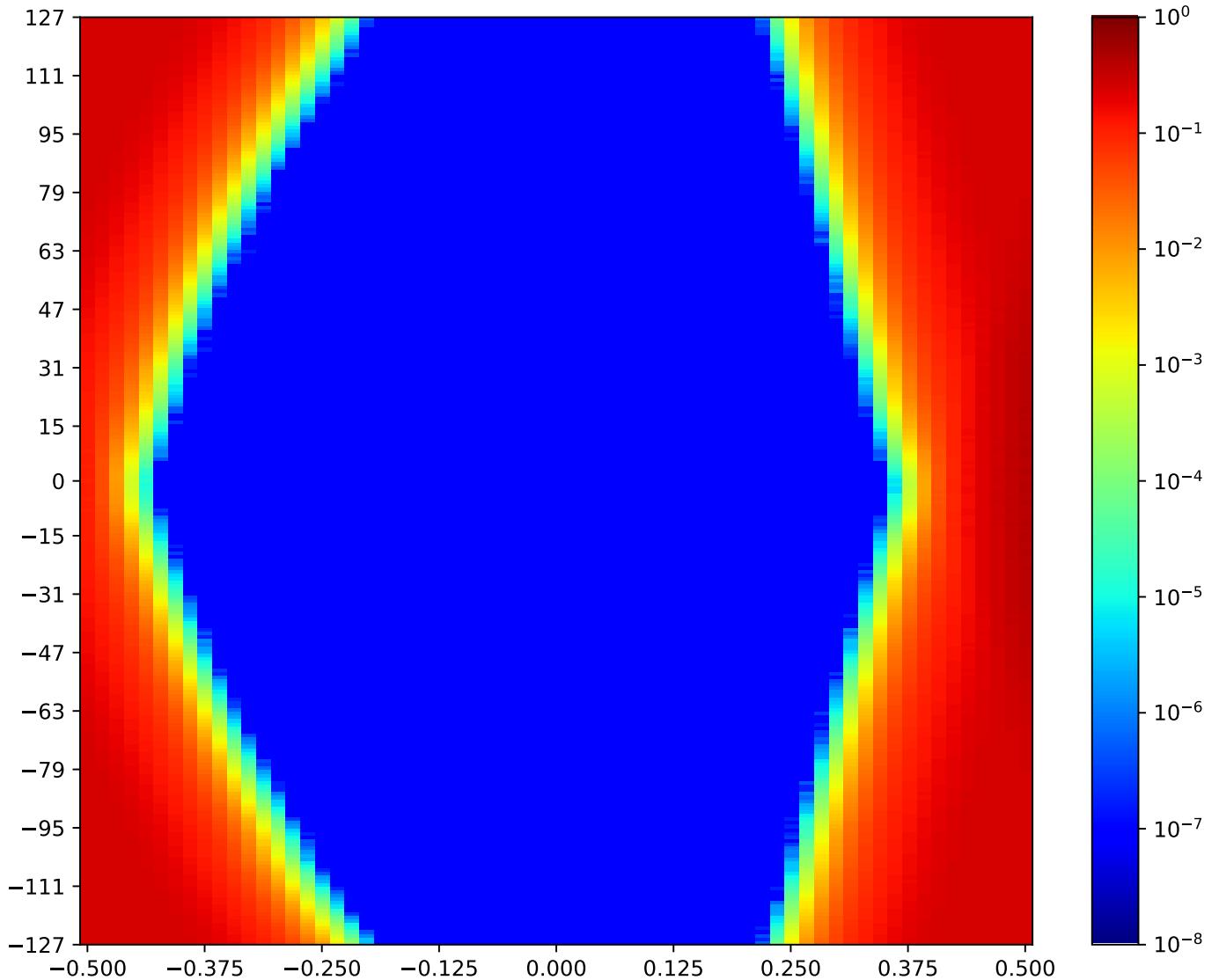


Figure 2.105: MSP\_C\_FPGA-IC39-06-IC15-06-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.8 MSP\_C\_FPGA-IC39-07-IC15-07-TRP\_FPGA

Table 2.97: MSP\_C\_FPGA-IC39-07-IC15-07-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:57:48		2018-Jan-24 19:58:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9693	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

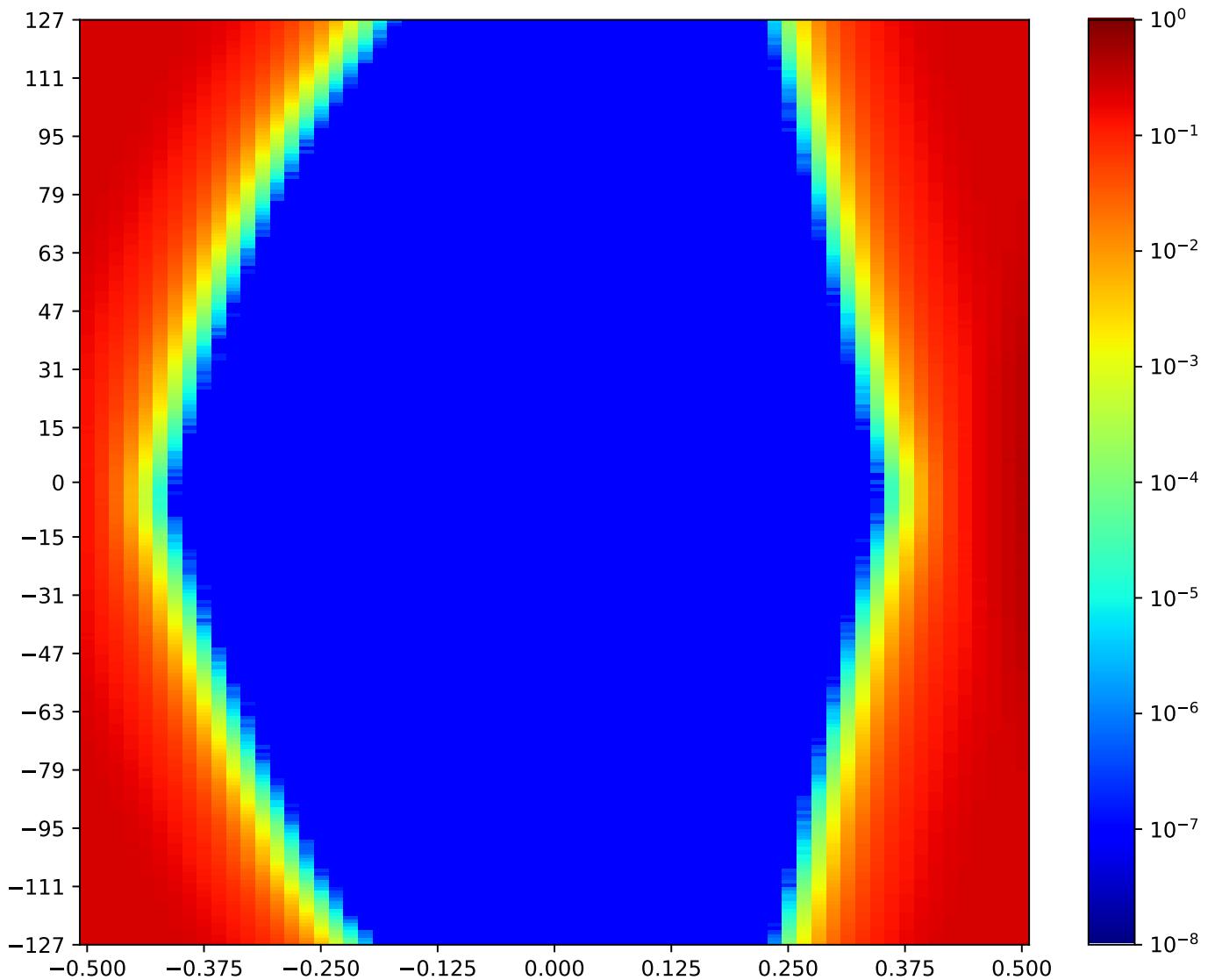


Figure 2.106: MSP\_C\_FPGA-IC39-07-IC15-07-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.9 MSP\_C\_FPGA-IC39-08-IC15-08-TRP\_FPGA

Table 2.98: MSP\_C\_FPGA-IC39-08-IC15-08-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:58:17		2018-Jan-24 19:58:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10032	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

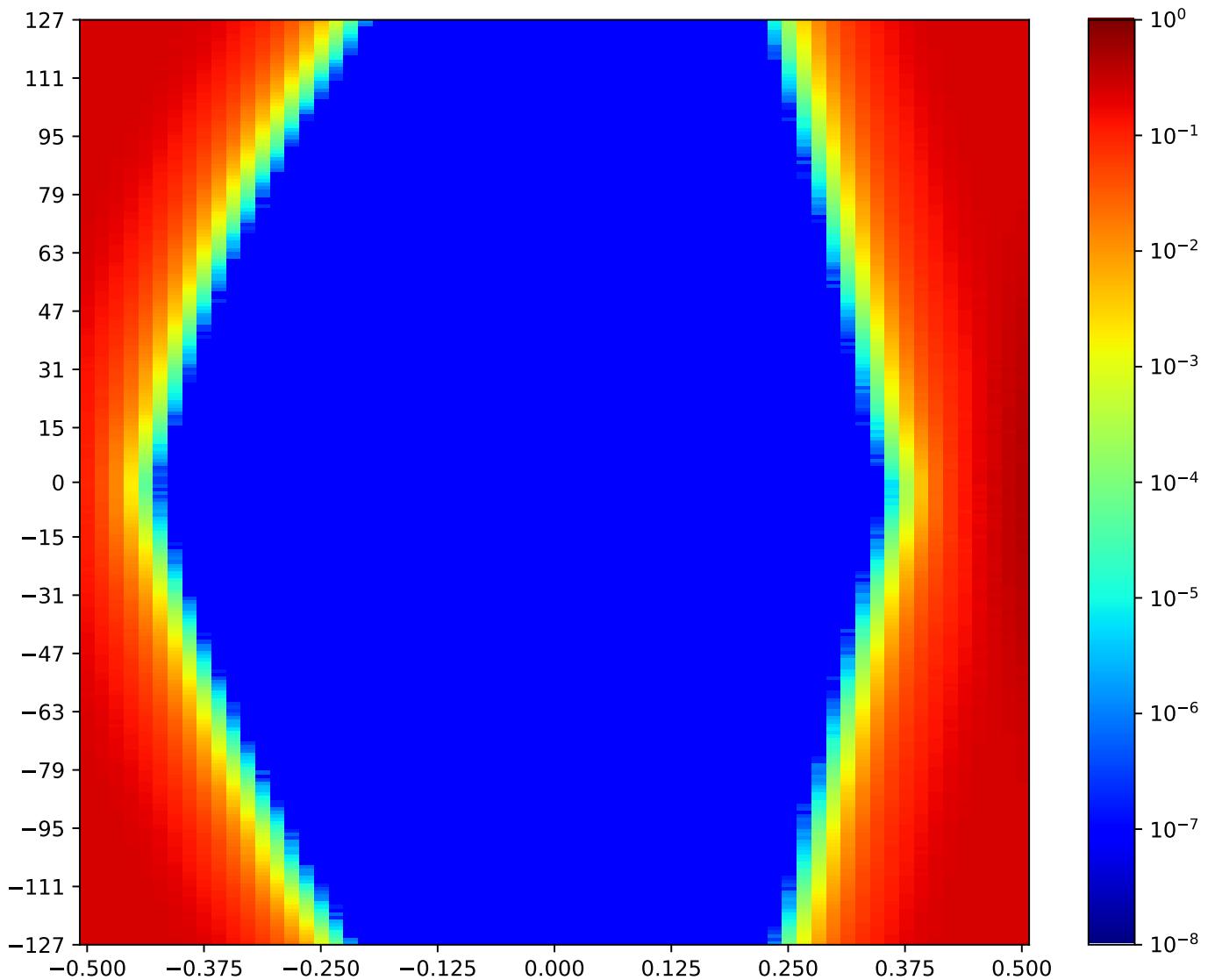


Figure 2.107: MSP\_C\_FPGA-IC39-08-IC15-08-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.10 MSP\_C\_FPGA-IC39-09-IC15-09-TRP\_FPGA

Table 2.99: MSP\_C\_FPGA-IC39-09-IC15-09-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:58:47		2018-Jan-24 19:59:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9503	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

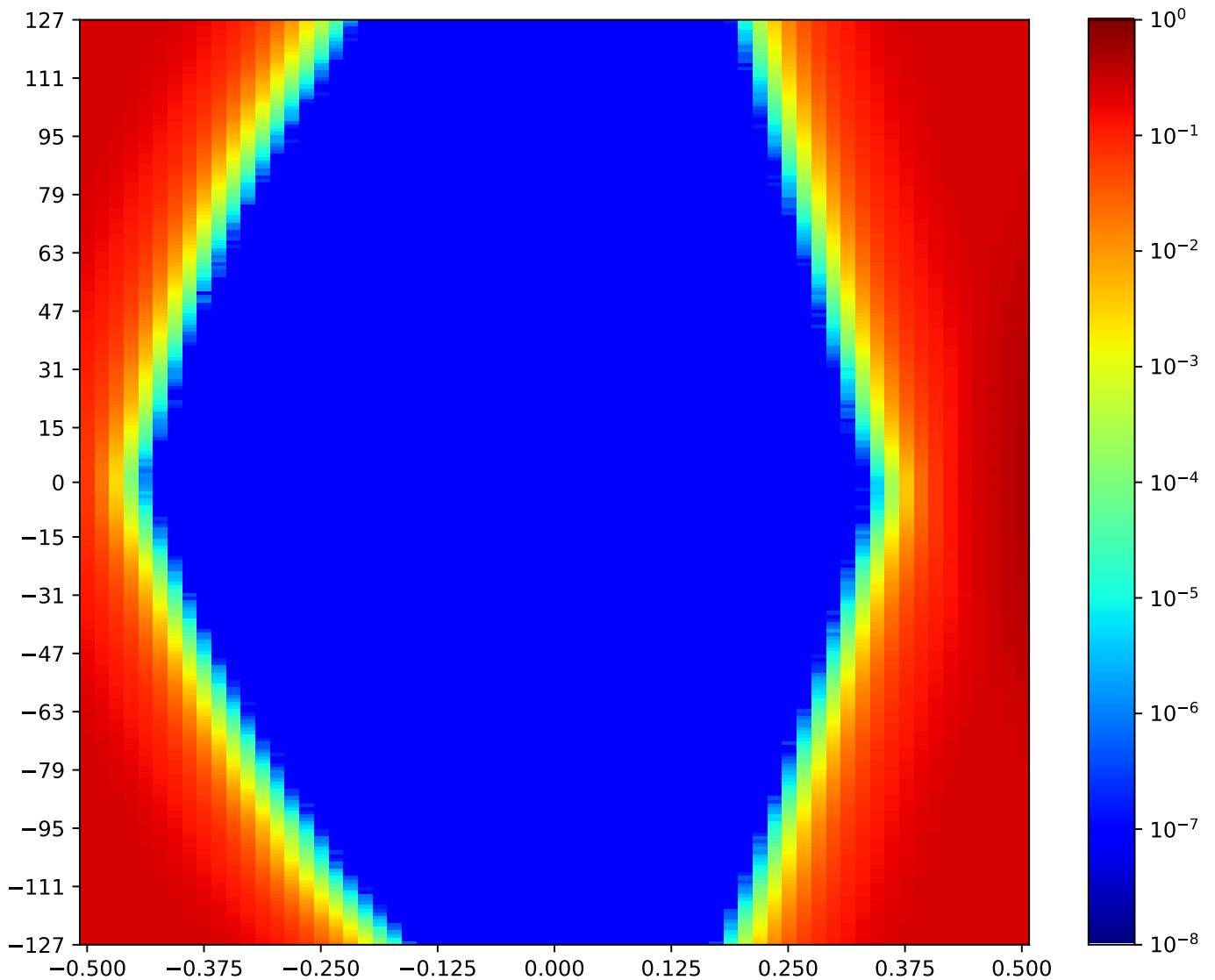


Figure 2.108: MSP\_C\_FPGA-IC39-09-IC15-09-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.11 MSP\_C\_FPGA-IC39-10-IC15-10-TRP\_FPGA

Table 2.100: MSP\_C\_FPGA-IC39-10-IC15-10-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:59:16		2018-Jan-24 19:59:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10108	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

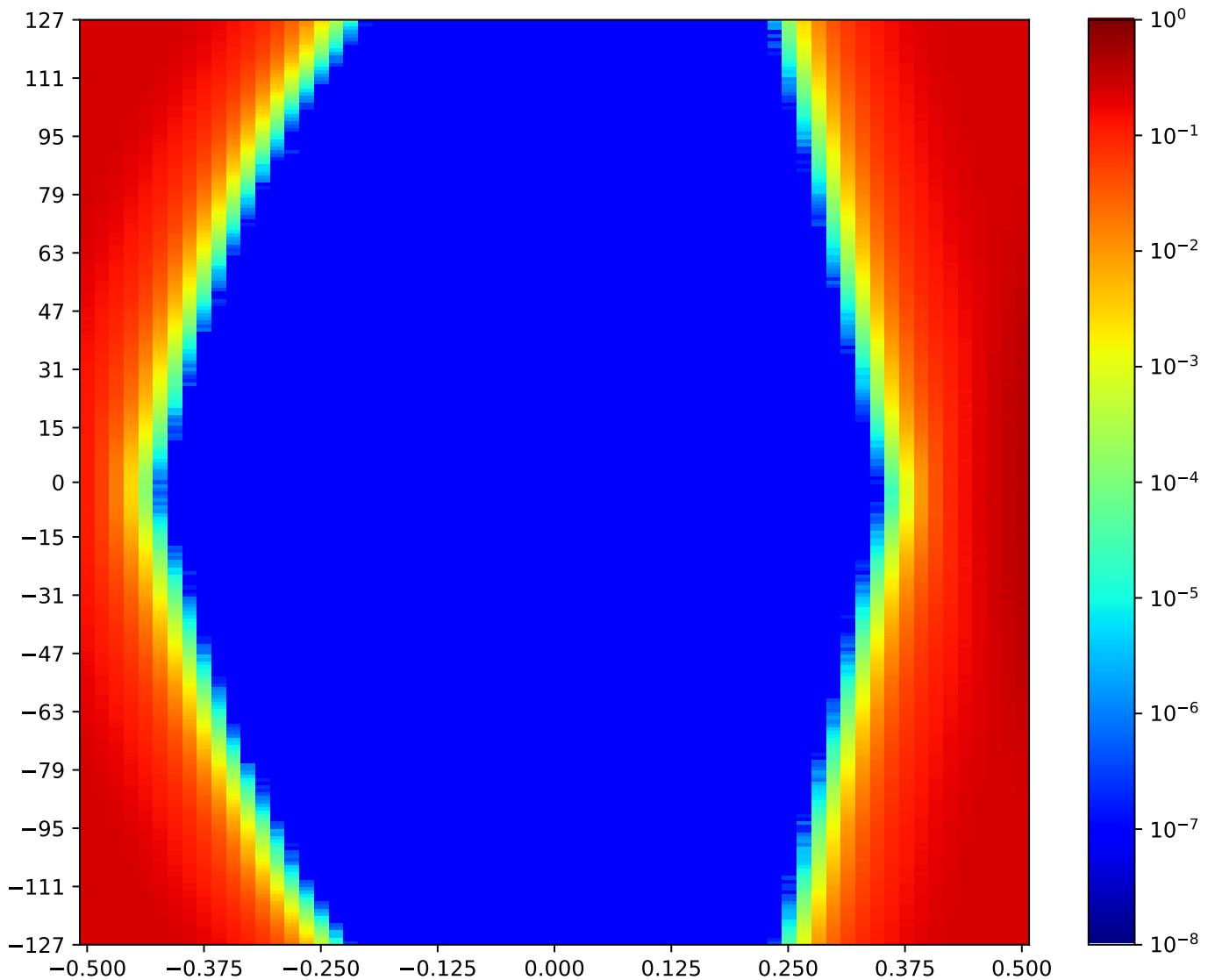


Figure 2.109: MSP\_C\_FPGA-IC39-10-IC15-10-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.12 MSP\_C\_FPGA-IC39-11-IC15-11-TRP\_FPGA

Table 2.101: MSP\_C\_FPGA-IC39-11-IC15-11-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 19:59:46		2018-Jan-24 20:00:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9926	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

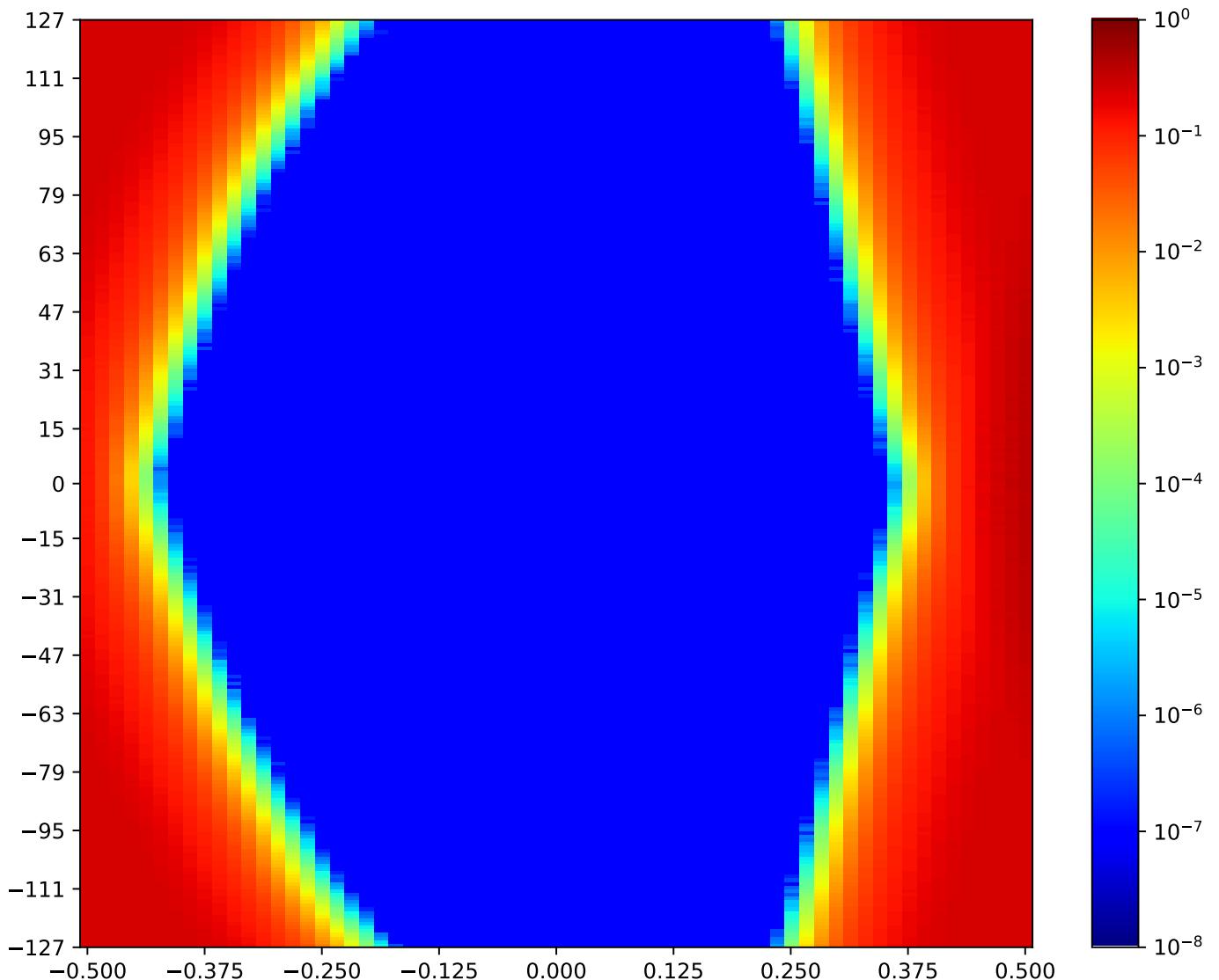


Figure 2.110: MSP\_C\_FPGA-IC39-11-IC15-11-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.13 MSP\_C\_FPGA-IC39-12-IC15-12-TRP\_FPGA

Table 2.102: MSP\_C\_FPGA-IC39-12-IC15-12-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:00:16		2018-Jan-24 20:00:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10441	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

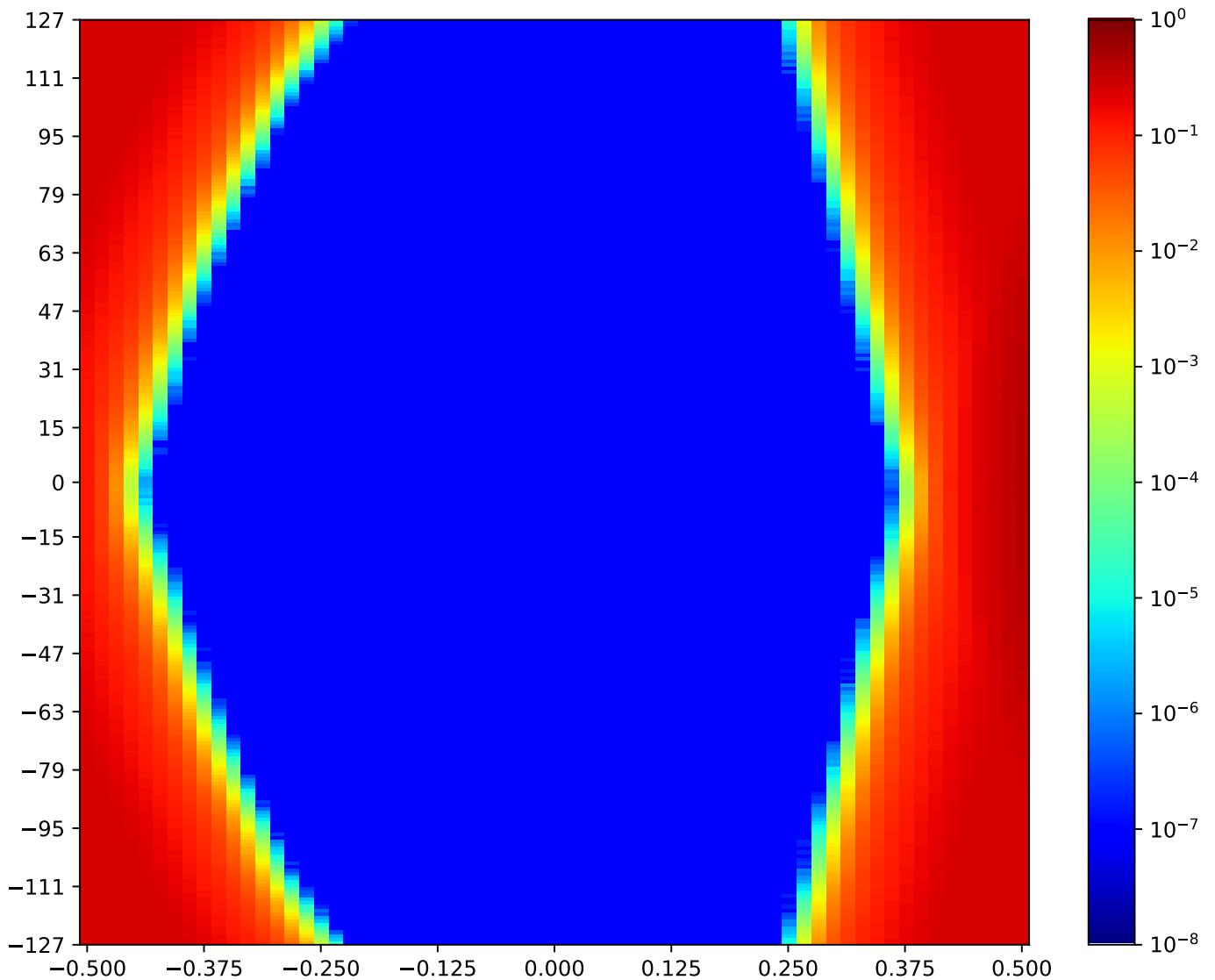


Figure 2.111: MSP\_C\_FPGA-IC39-12-IC15-12-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.14 MSP\_C\_FPGA-IC39-13-IC15-13-TRP\_FPGA

Table 2.103: MSP\_C\_FPGA-IC39-13-IC15-13-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:00:45		2018-Jan-24 20:01:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10623	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

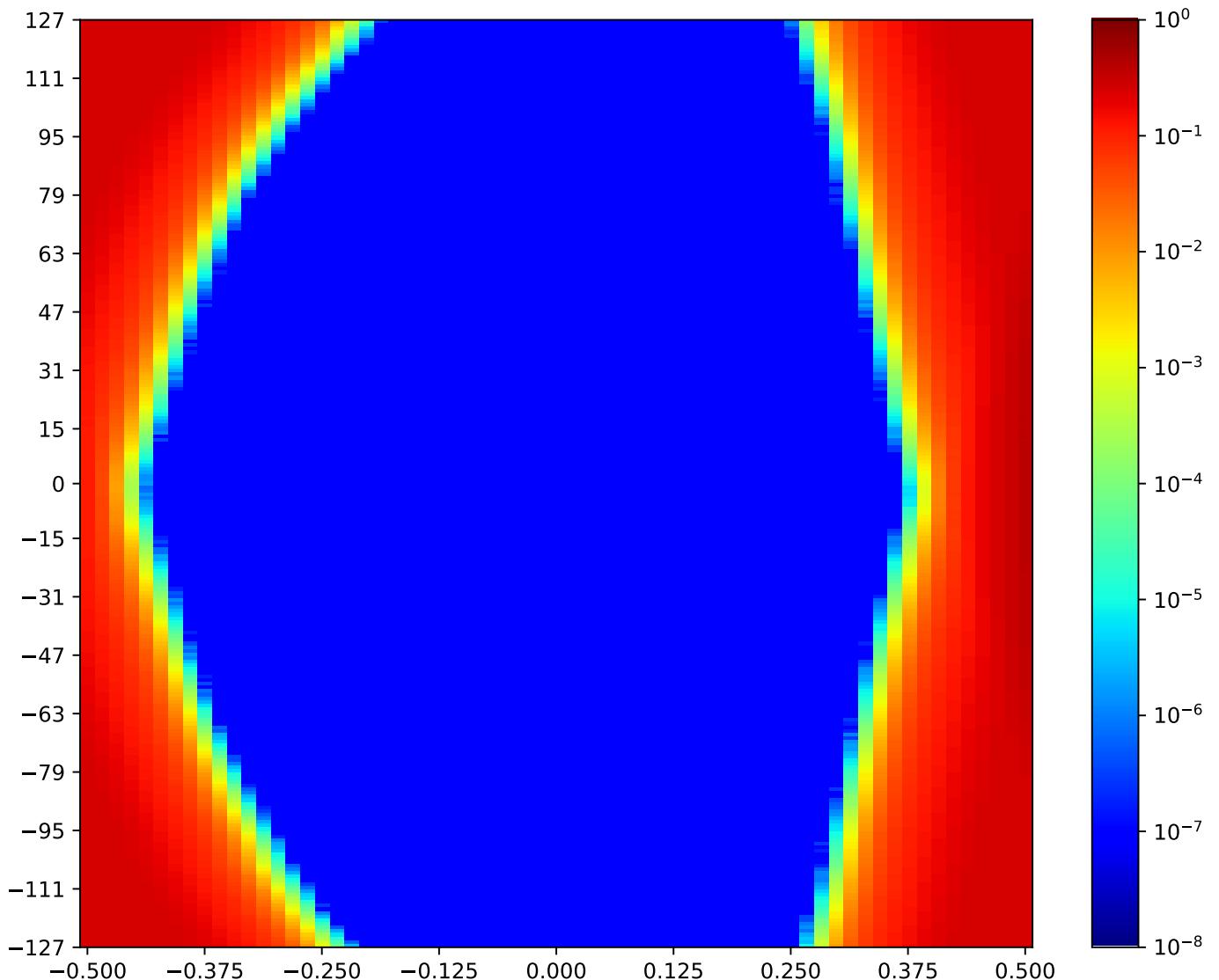


Figure 2.112: MSP\_C\_FPGA-IC39-13-IC15-13-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.15 MSP\_C\_FPGA-IC39-14-IC15-14-TRP\_FPGA

Table 2.104: MSP\_C\_FPGA-IC39-14-IC15-14-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:01:15		2018-Jan-24 20:01:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9945	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

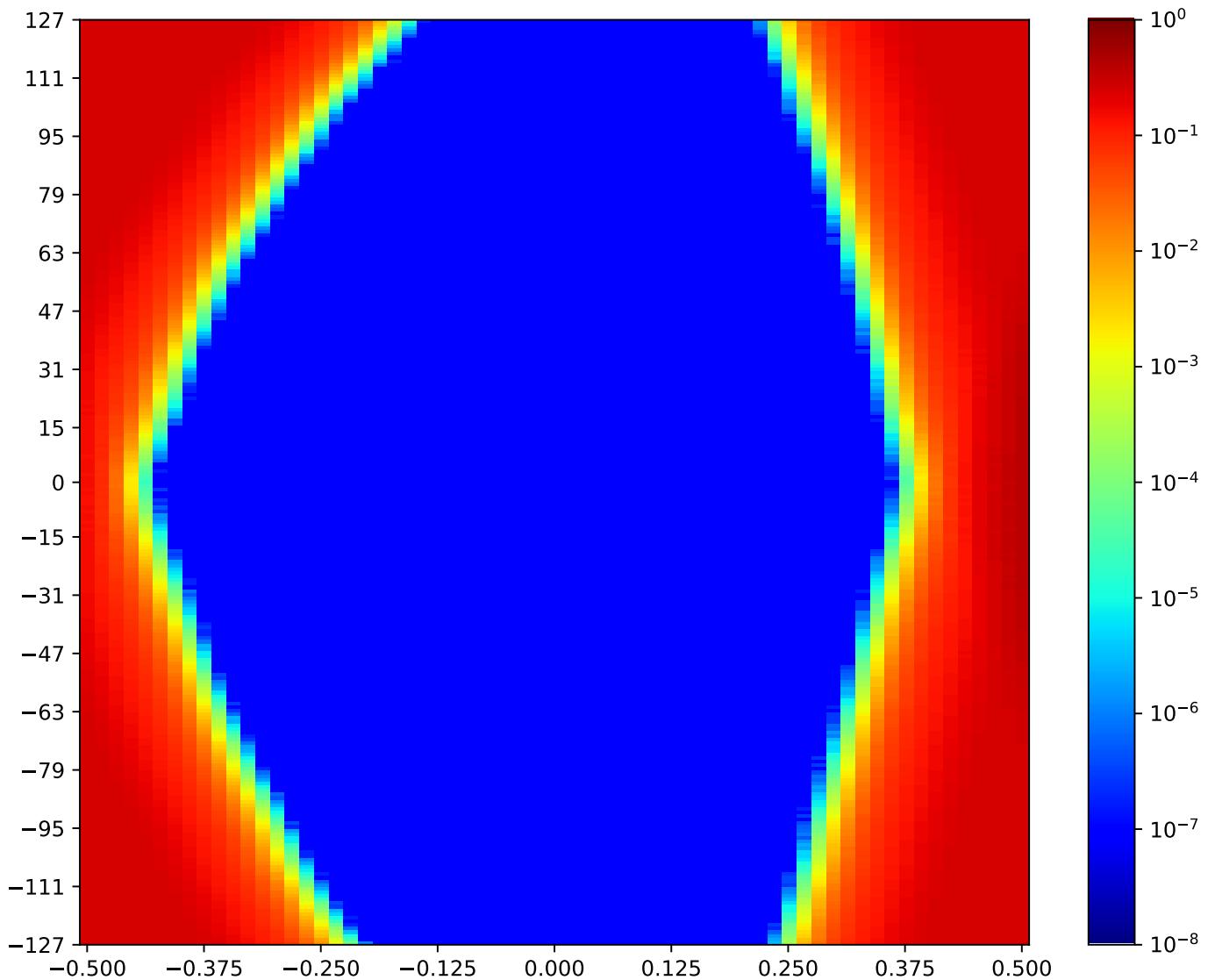


Figure 2.113: MSP\_C\_FPGA-IC39-14-IC15-14-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.16 MSP\_C\_FPGA-IC39-15-IC15-15-TRP\_FPGA

Table 2.105: MSP\_C\_FPGA-IC39-15-IC15-15-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:01:45		2018-Jan-24 20:02:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10372	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

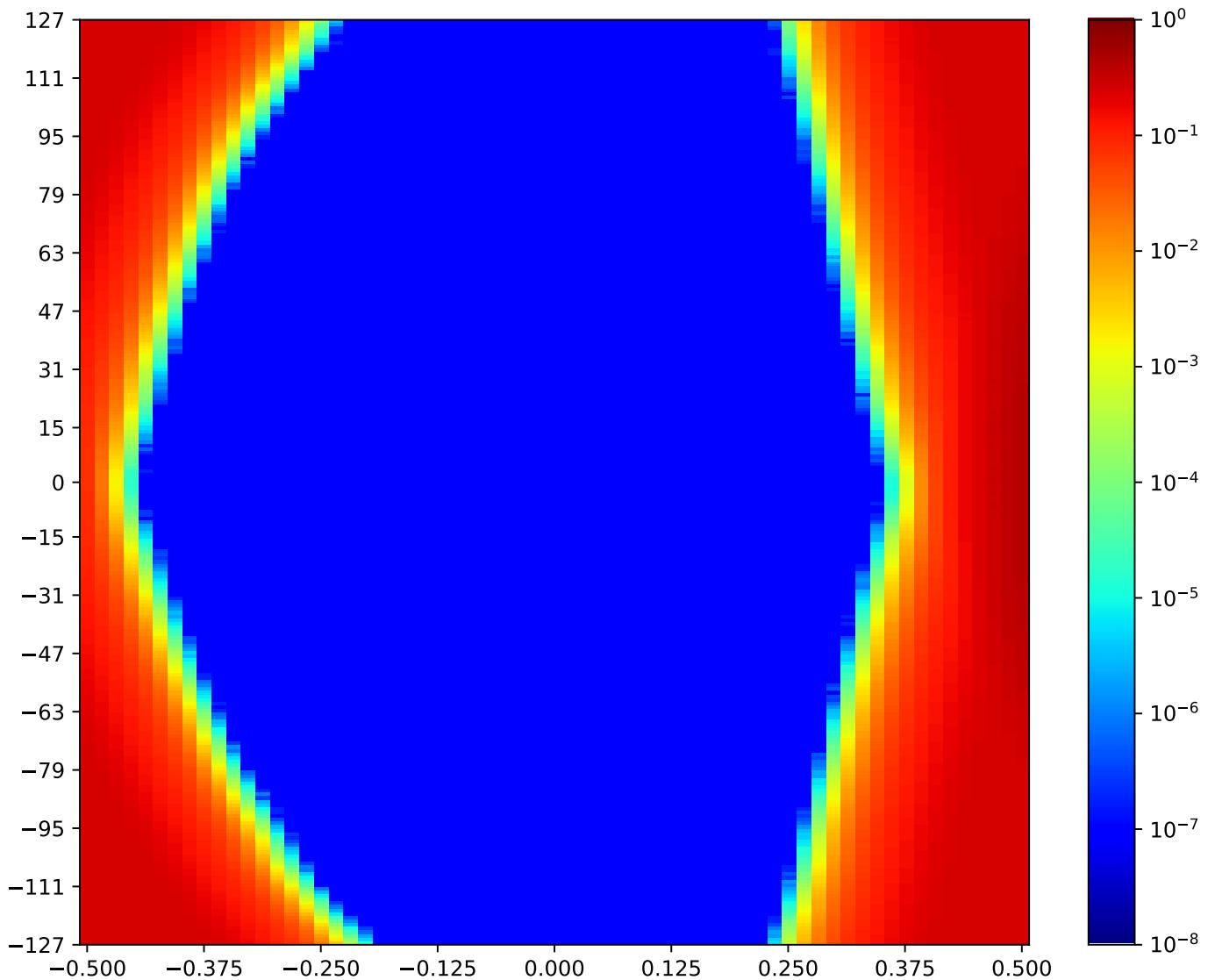


Figure 2.114: MSP\_C\_FPGA-IC39-15-IC15-15-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.17 MSP\_C\_FPGA-IC39-16-IC15-16-TRP\_FPGA

Table 2.106: MSP\_C\_FPGA-IC39-16-IC15-16-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:02:14		2018-Jan-24 20:02:44	
Reset RX	OA	HO		VO   VO (%)	
true	9789	47		72.31%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

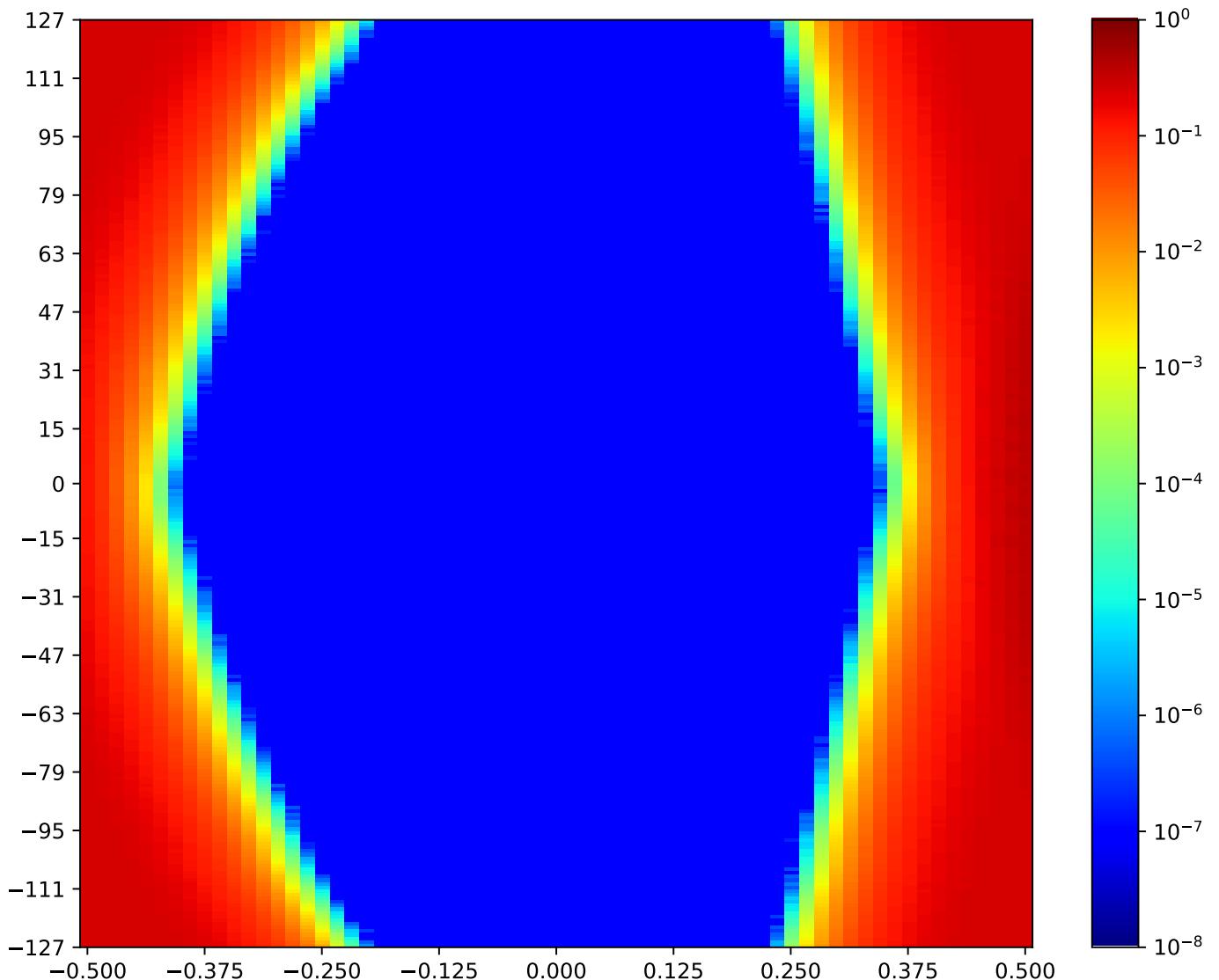


Figure 2.115: MSP\_C\_FPGA-IC39-16-IC15-16-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.18 MSP\_C\_FPGA-IC39-17-IC15-17-TRP\_FPGA

Table 2.107: MSP\_C\_FPGA-IC39-17-IC15-17-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:02:44		2018-Jan-24 20:03:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9420	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

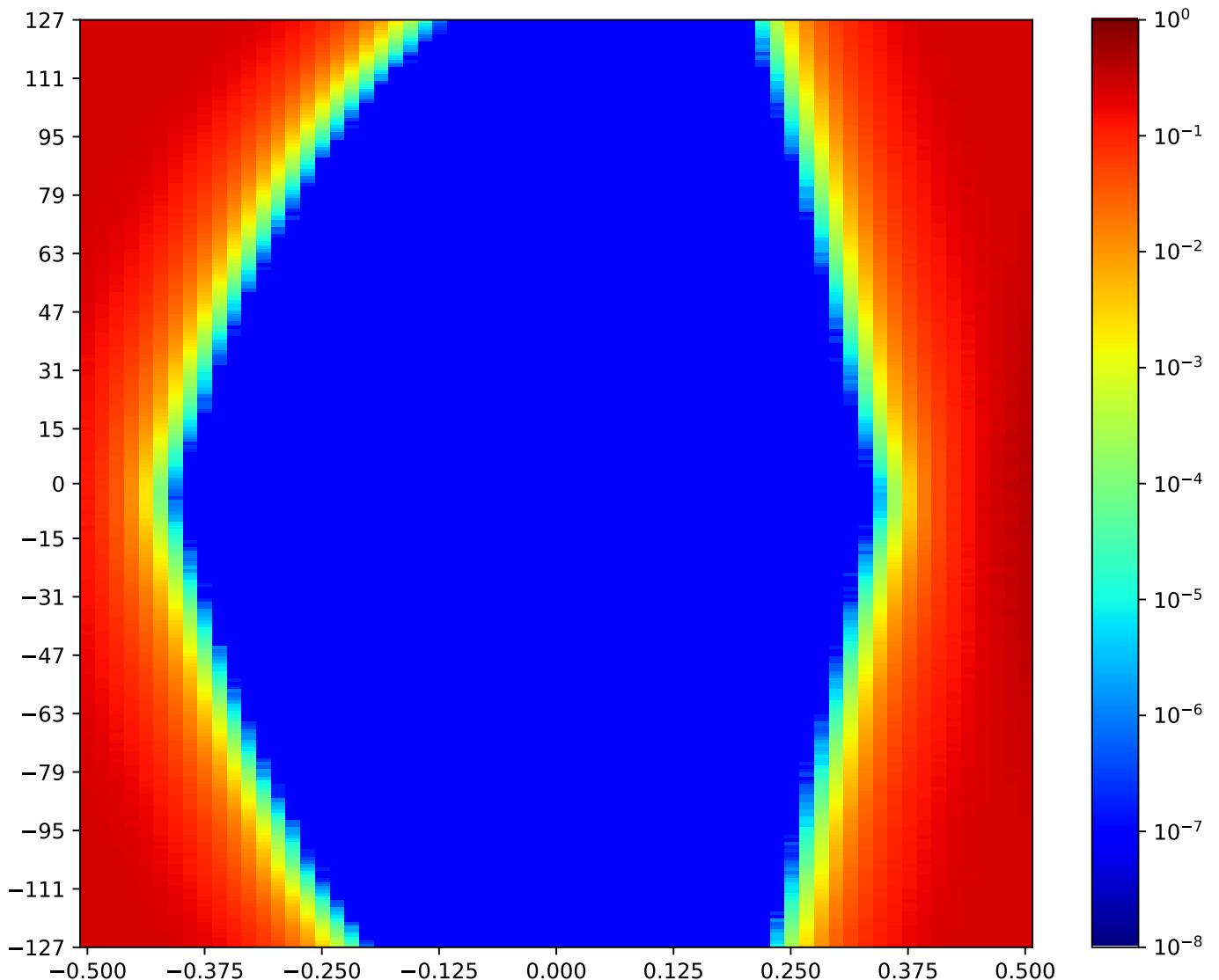


Figure 2.116: MSP\_C\_FPGA-IC39-17-IC15-17-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.19 MSP\_C\_FPGA-IC39-18-IC15-18-TRP\_FPGA

Table 2.108: MSP\_C\_FPGA-IC39-18-IC15-18-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:03:14		2018-Jan-24 20:03:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9709	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

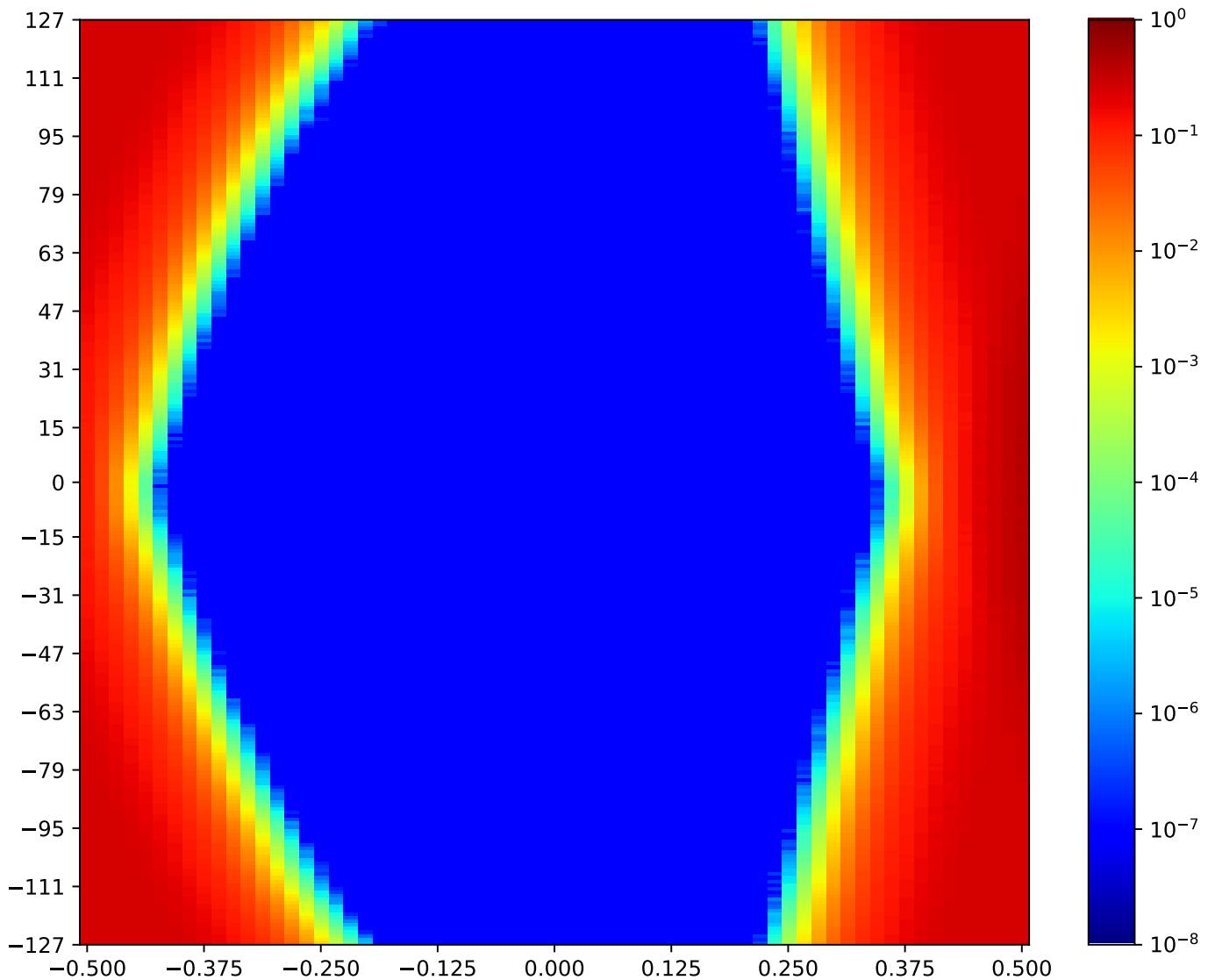


Figure 2.117: MSP\_C\_FPGA-IC39-18-IC15-18-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.20 MSP\_C\_FPGA-IC39-19-IC15-19-TRP\_FPGA

Table 2.109: MSP\_C\_FPGA-IC39-19-IC15-19-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:03:43		2018-Jan-24 20:04:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10262	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

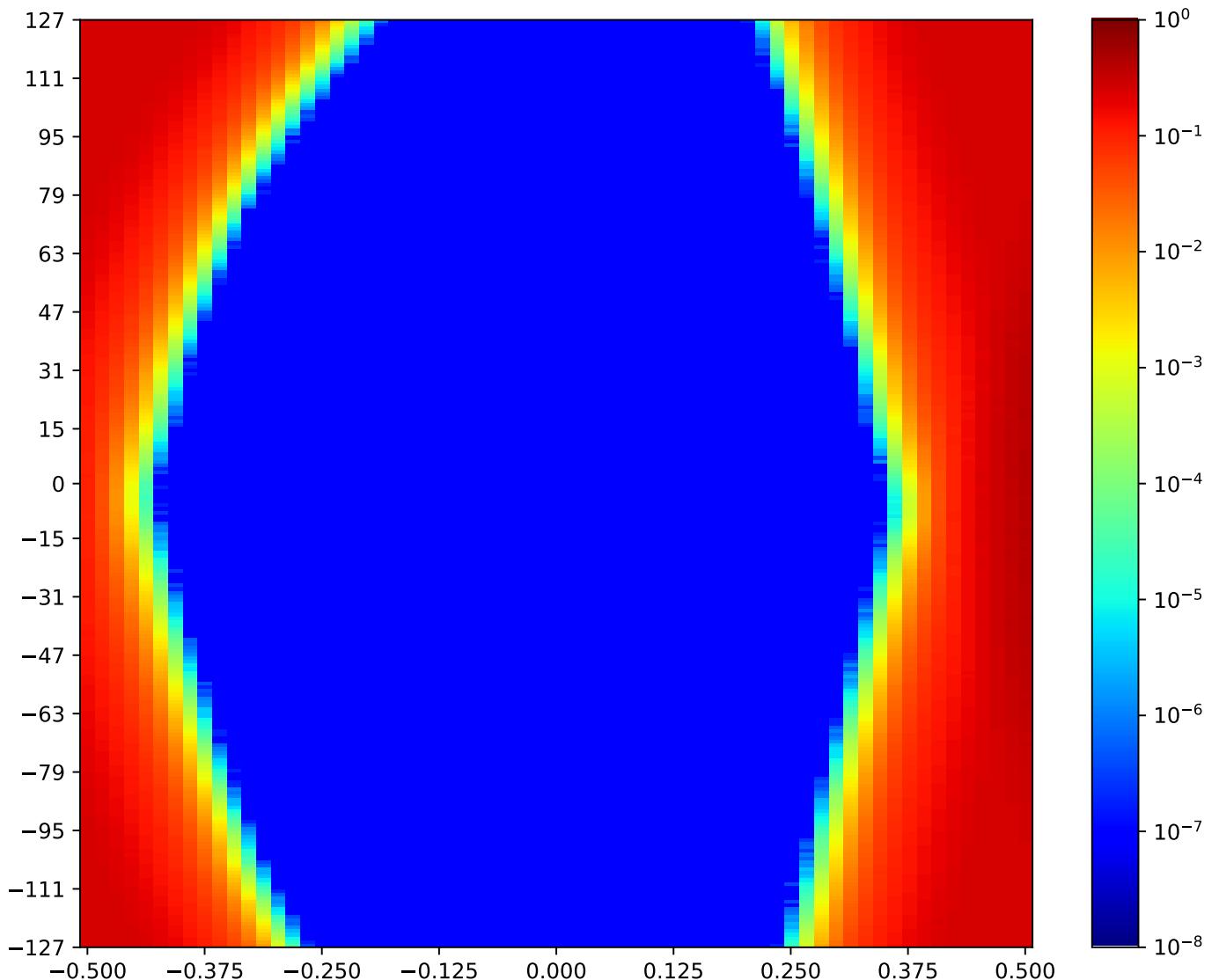


Figure 2.118: MSP\_C\_FPGA-IC39-19-IC15-19-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.21 MSP\_C\_FPGA-IC39-20-IC15-20-TRP\_FPGA

Table 2.110: MSP\_C\_FPGA-IC39-20-IC15-20-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:04:12		2018-Jan-24 20:04:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10423	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

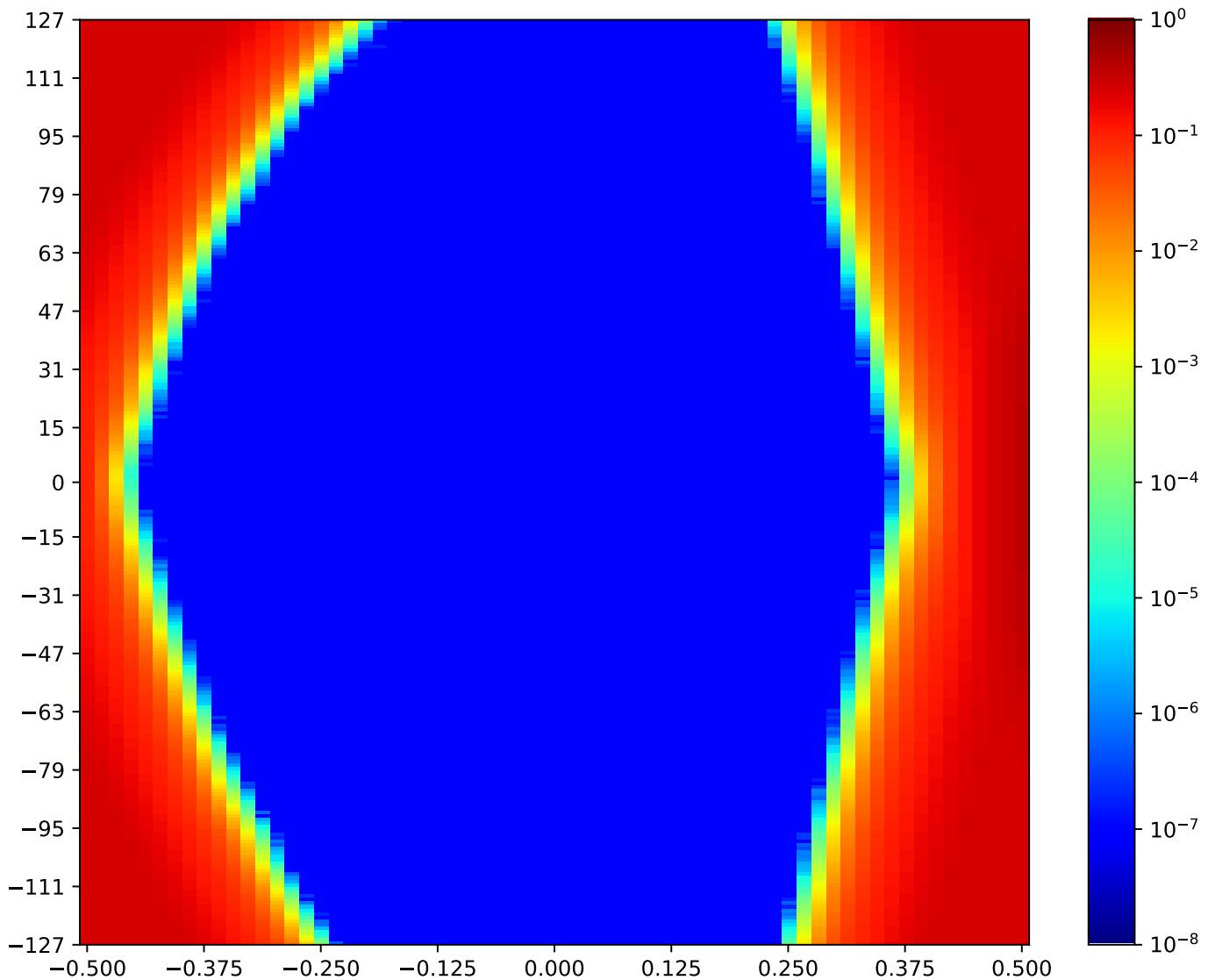


Figure 2.119: MSP\_C\_FPGA-IC39-20-IC15-20-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.22 MSP\_C\_FPGA-IC39-21-IC15-21-TRP\_FPGA

Table 2.111: MSP\_C\_FPGA-IC39-21-IC15-21-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:04:42		2018-Jan-24 20:05:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10459	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

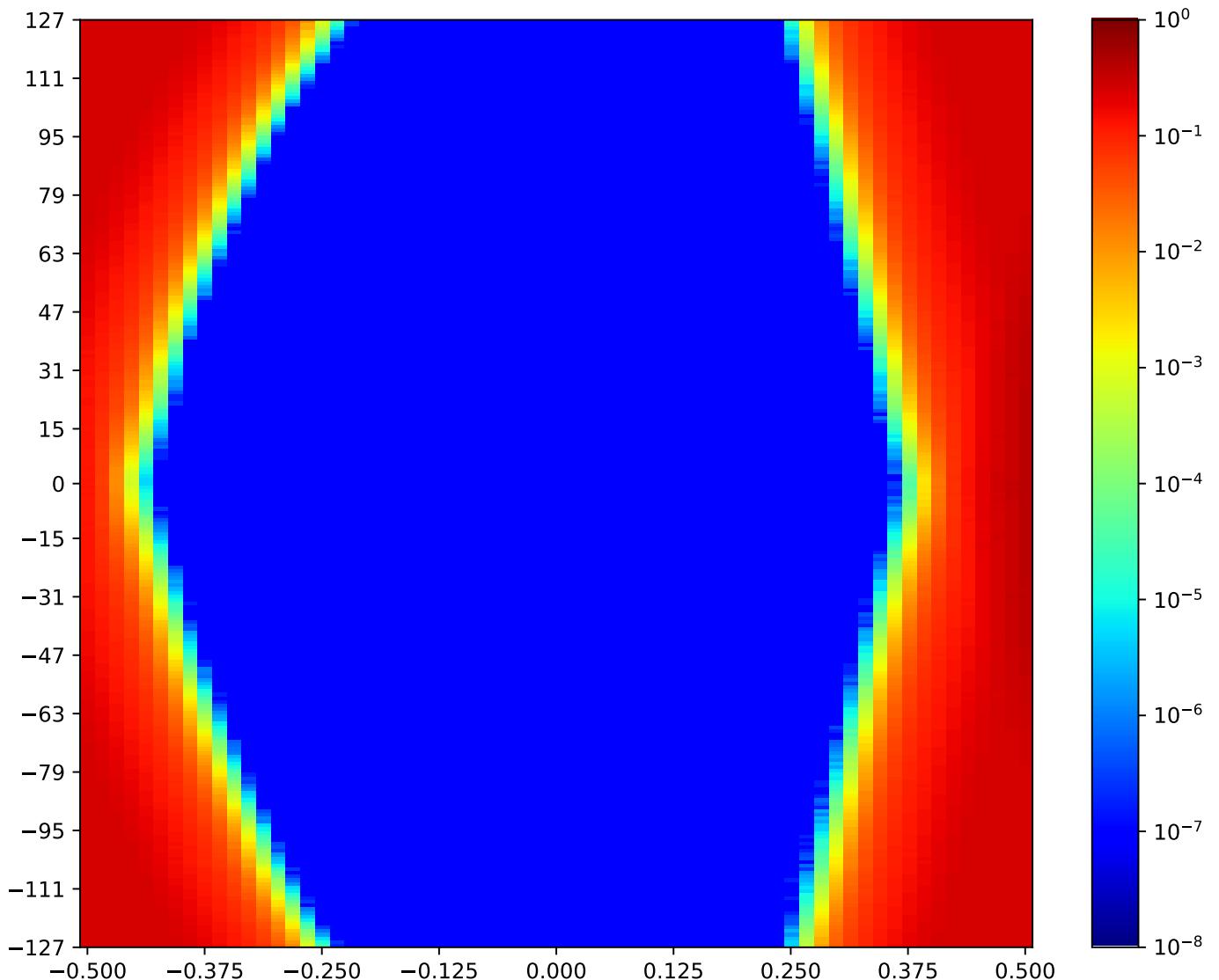


Figure 2.120: MSP\_C\_FPGA-IC39-21-IC15-21-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.23 MSP\_C\_FPGA-IC39-22-IC15-22-TRP\_FPGA

Table 2.112: MSP\_C\_FPGA-IC39-22-IC15-22-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:05:12		2018-Jan-24 20:05:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10053	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

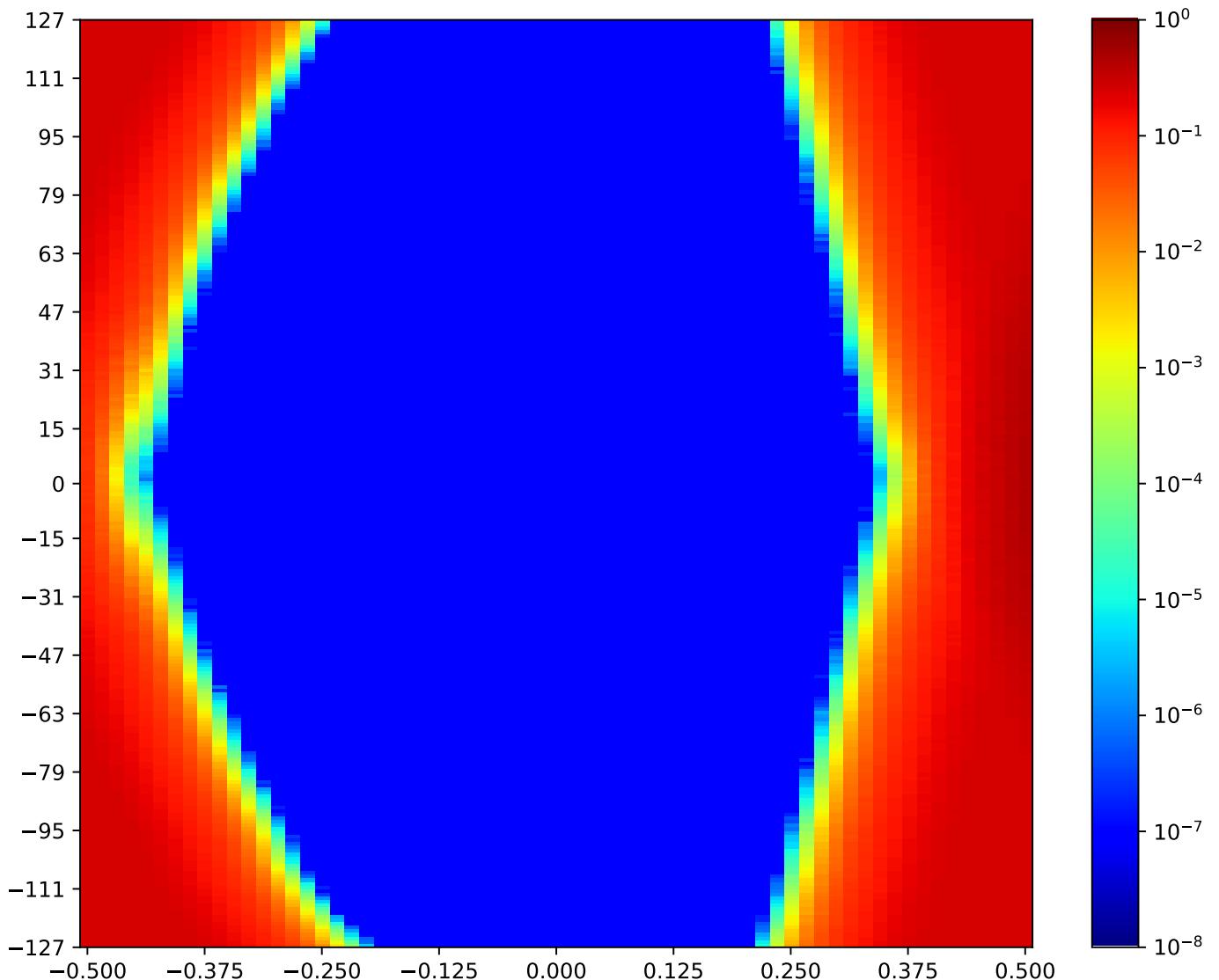


Figure 2.121: MSP\_C\_FPGA-IC39-22-IC15-22-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.24 MSP\_C\_FPGA-IC39-23-IC15-23-TRP\_FPGA

Table 2.113: MSP\_C\_FPGA-IC39-23-IC15-23-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:05:42		2018-Jan-24 20:06:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9950	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

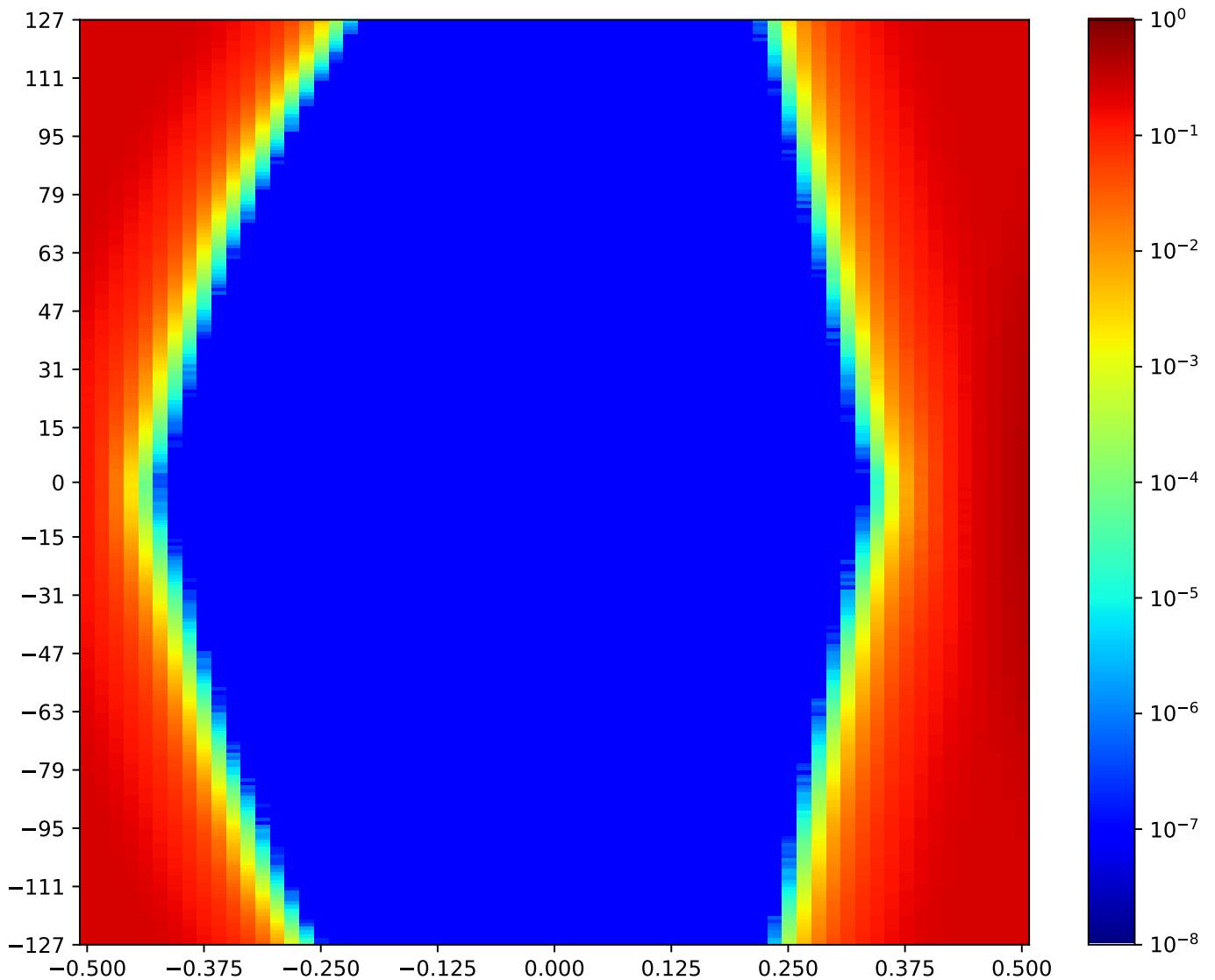


Figure 2.122: MSP\_C\_FPGA-IC39-23-IC15-23-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.25 MSP\_C\_FPGA-IC39-24-IC15-24-TRP\_FPGA

Table 2.114: MSP\_C\_FPGA-IC39-24-IC15-24-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:06:11		2018-Jan-24 20:06:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10126	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

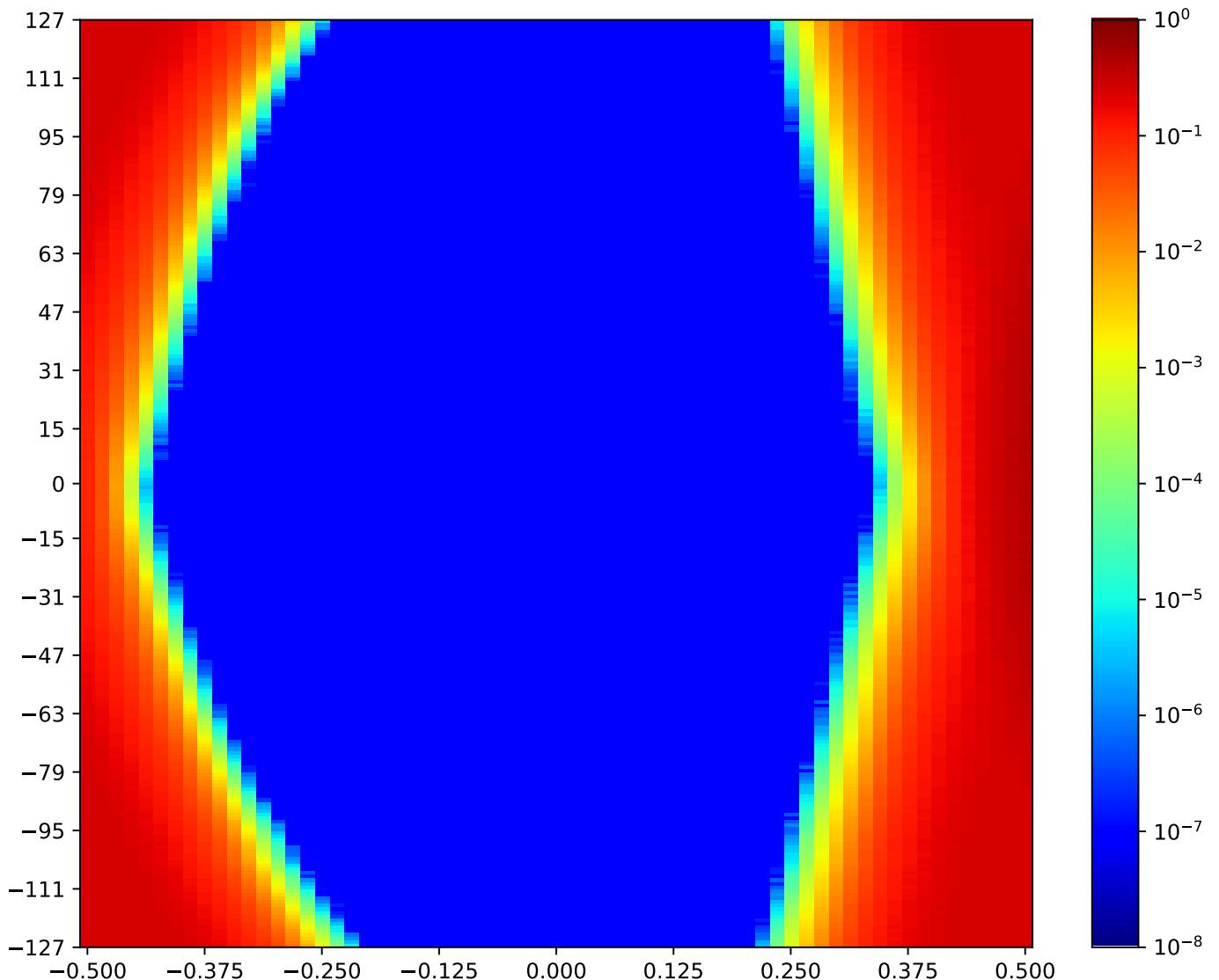


Figure 2.123: MSP\_C\_FPGA-IC39-24-IC15-24-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.26 MSP\_C\_FPGA-IC39-25-IC15-25-TRP\_FPGA

Table 2.115: MSP\_C\_FPGA-IC39-25-IC15-25-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:06:41		2018-Jan-24 20:07:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10221	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

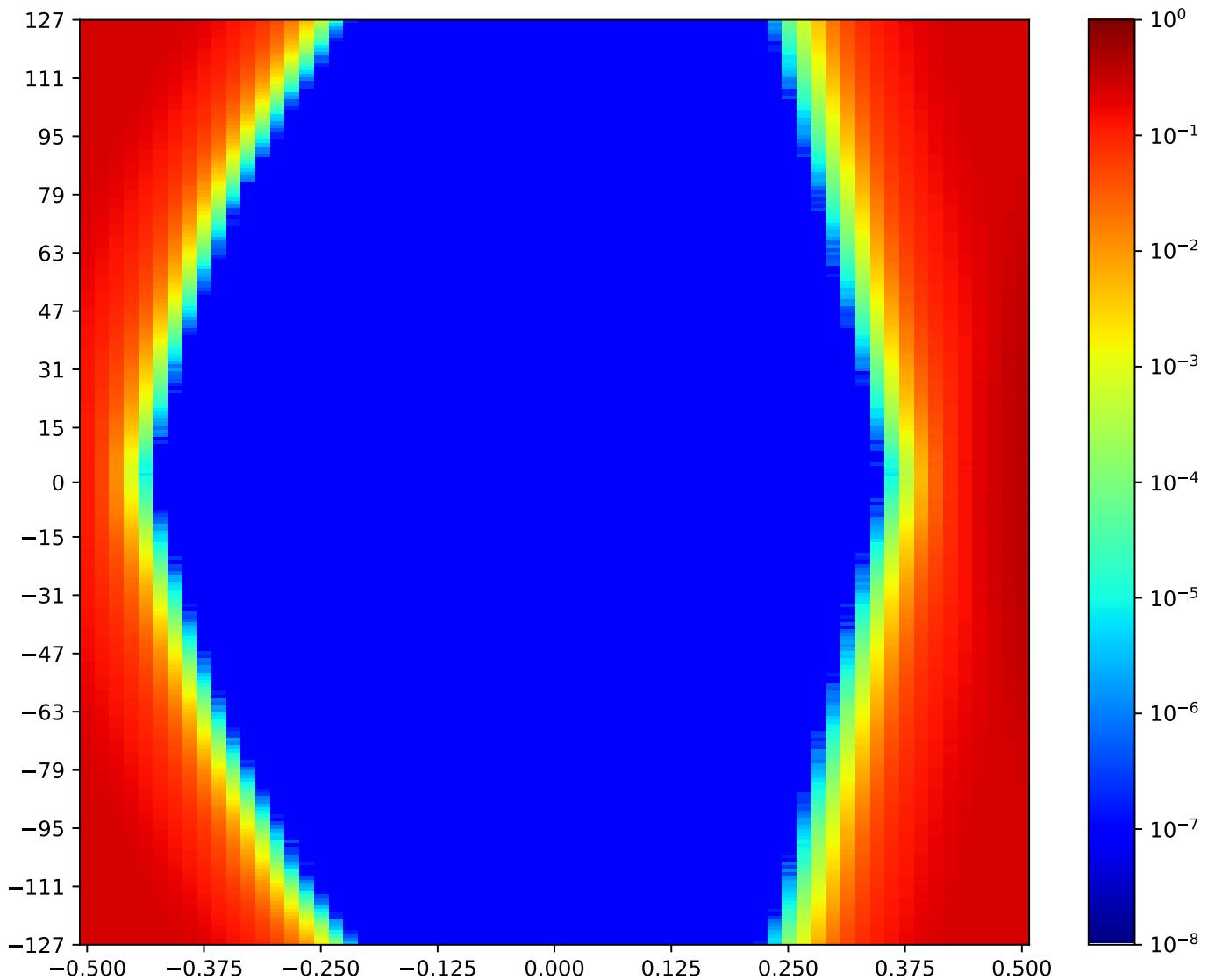


Figure 2.124: MSP\_C\_FPGA-IC39-25-IC15-25-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.9.27 MSP\_C\_FPGA-IC39-26-IC15-26-TRP\_FPGA

Table 2.116: MSP\_C\_FPGA-IC39-26-IC15-26-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:07:11		2018-Jan-24 20:07:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9684	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

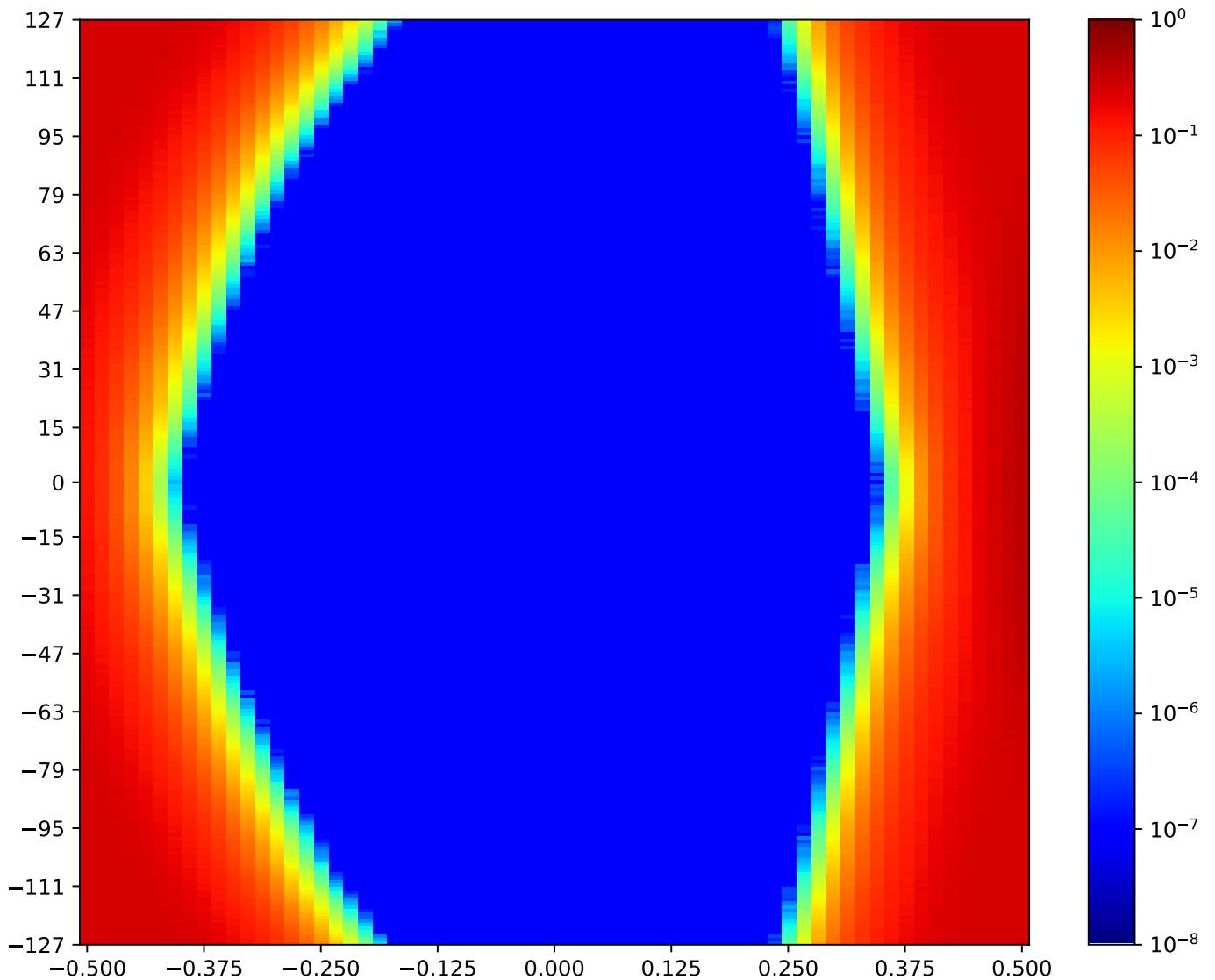


Figure 2.125: MSP\_C\_FPGA-IC39-26-IC15-26-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.9.28 MSP\_C\_FPGA-IC39-27-IC15-27-TRP\_FPGA

Table 2.117: MSP\_C\_FPGA-IC39-27-IC15-27-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 20:07:41		2018-Jan-24 20:08:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10391	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

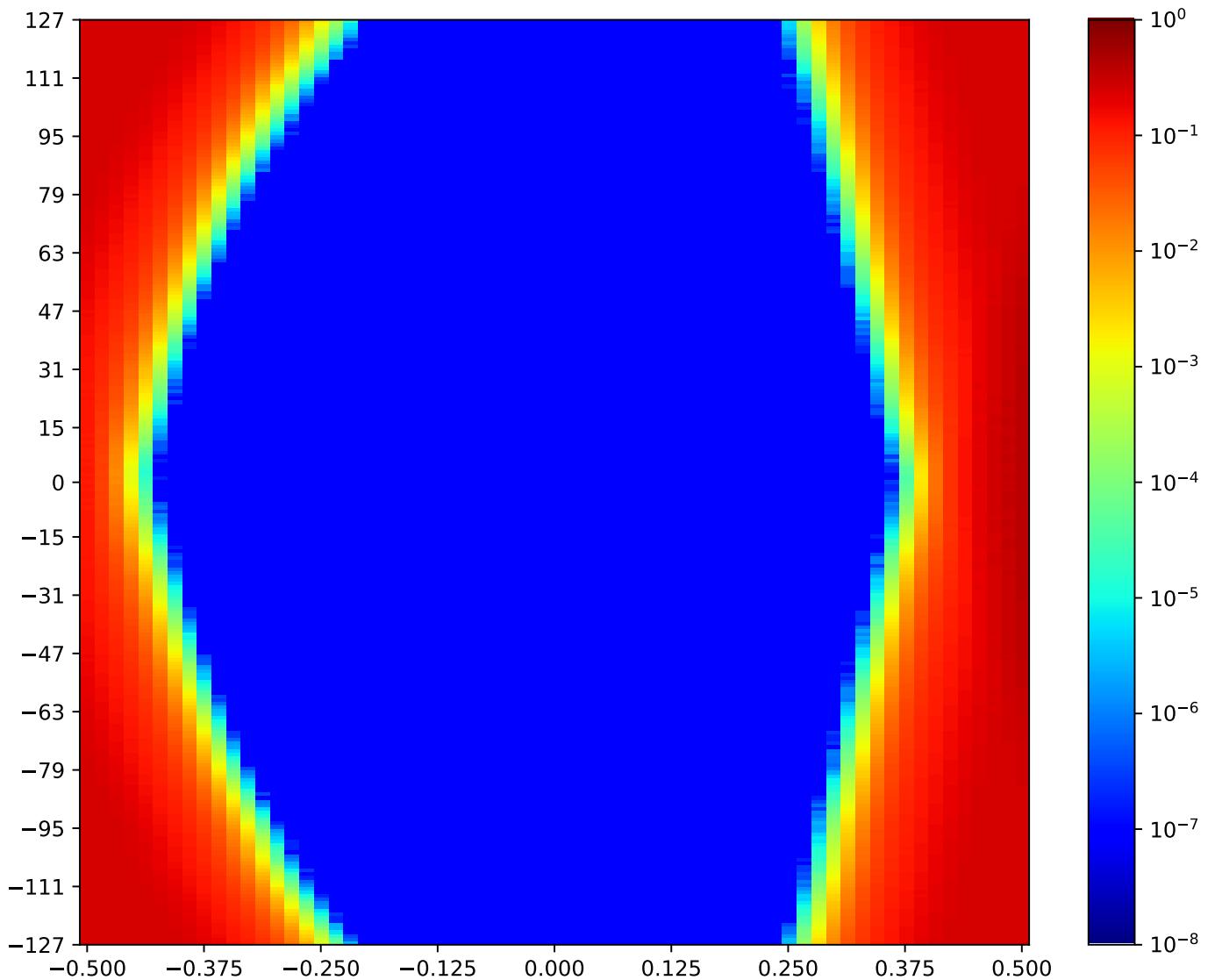


Figure 2.126: MSP\_C\_FPGA-IC39-27-IC15-27-TRP\_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10 MSP\_A TX1 MSP\_C RX18 Minipod Loopback

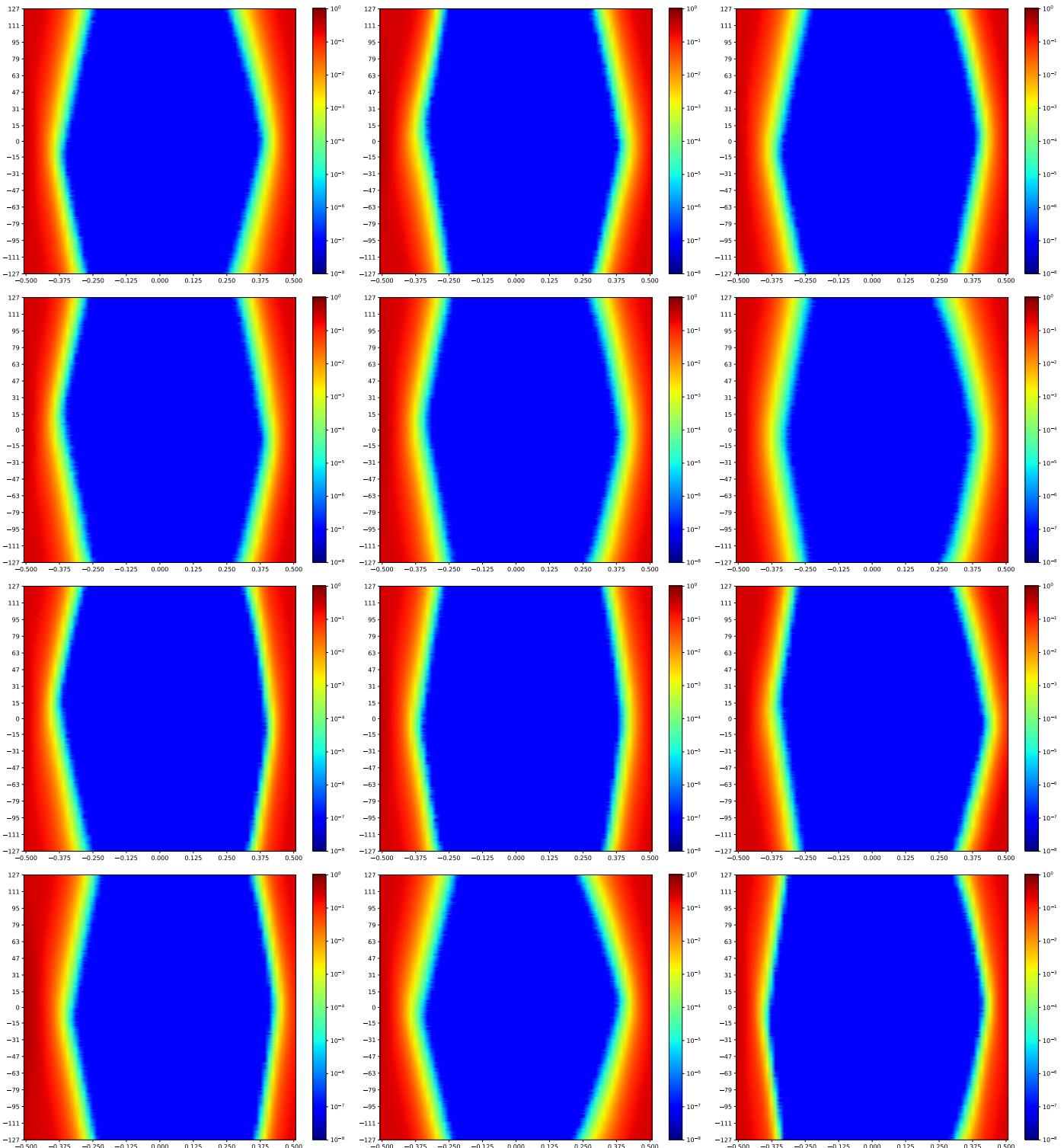


Figure 2.127: MSP\_A TX1 MSP\_C RX18 Minipod Loopback

A cross-reference to Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.140.

### 2.10.1 MSP\_A\_FPGA-TX1-00-RX18-00-MSP\_C\_FPGA

Table 2.118: MSP\_A\_FPGA-TX1-00-RX18-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:52:34		2018-Jan-24 20:53:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9900	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

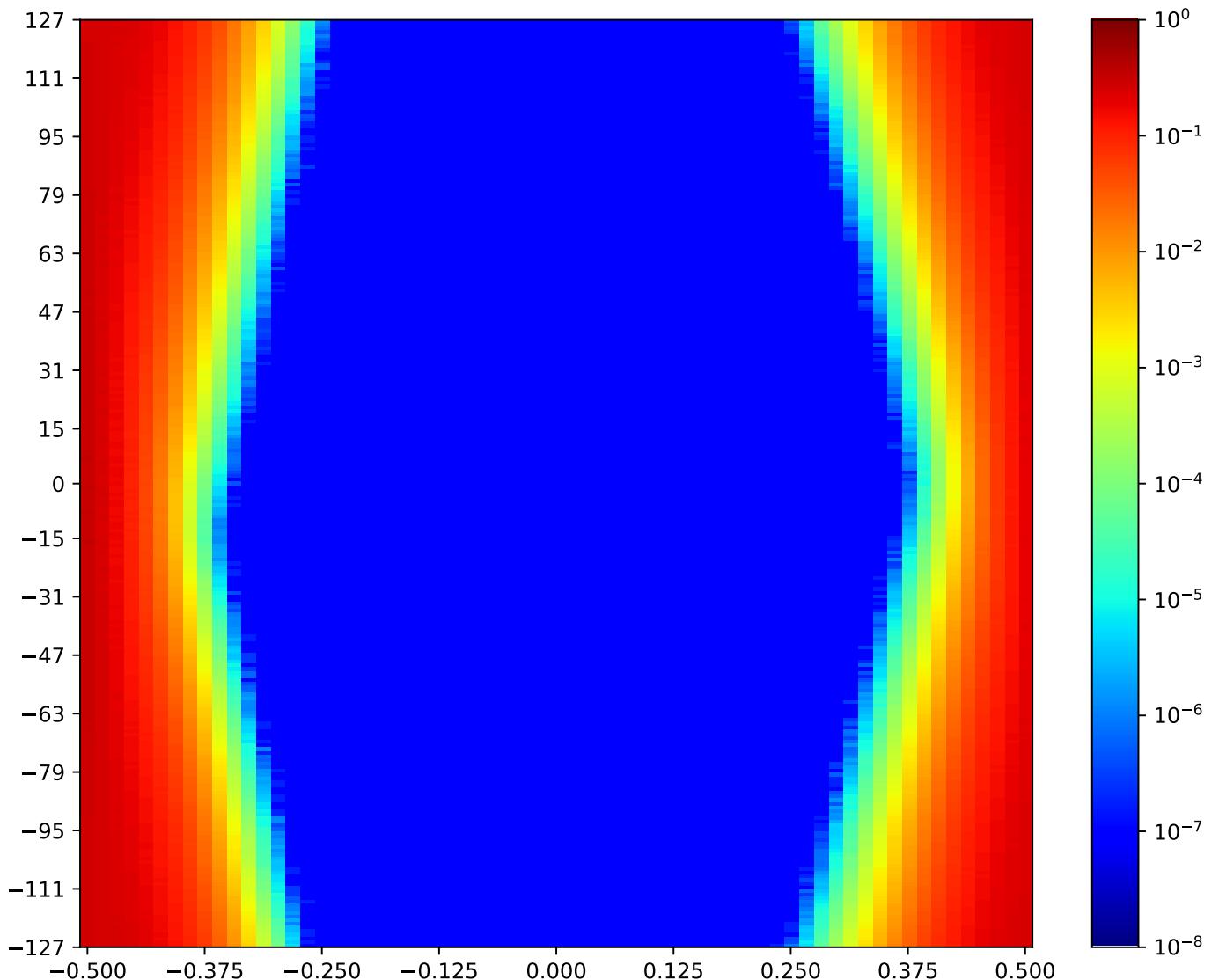


Figure 2.128: MSP\_A\_FPGA-TX1-00-RX18-00-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10.2 MSP\_A\_FPGA-TX1-01-RX18-01-MSP\_C\_FPGA

Table 2.119: MSP\_A\_FPGA-TX1-01-RX18-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:53:38		2018-Jan-24 20:54:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9851	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

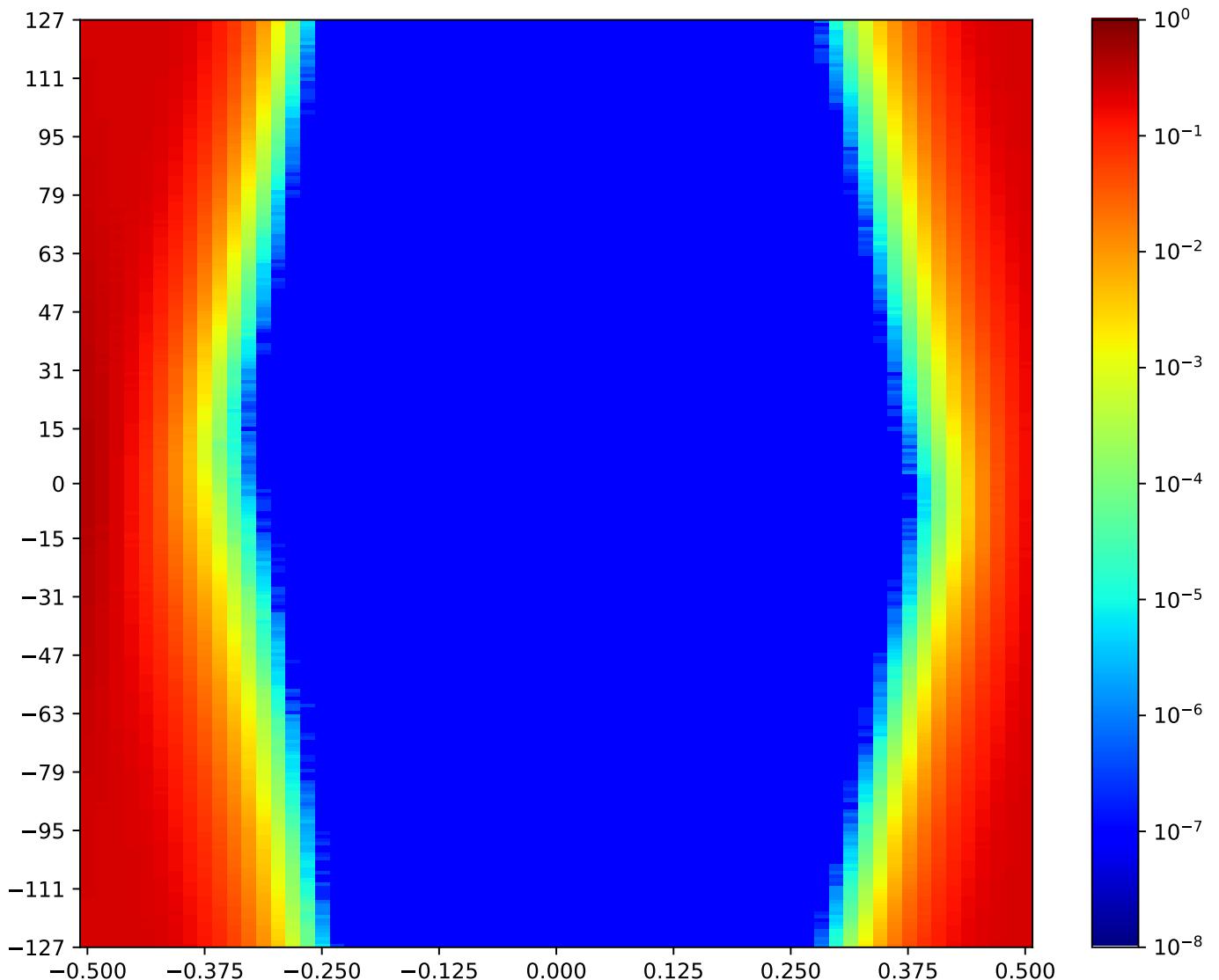


Figure 2.129: MSP\_A\_FPGA-TX1-01-RX18-01-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.10.3 MSP\_A\_FPGA-TX1-02-RX18-02-MSP\_C\_FPGA

Table 2.120: MSP\_A\_FPGA-TX1-02-RX18-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:54:10		2018-Jan-24 20:54:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9963	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

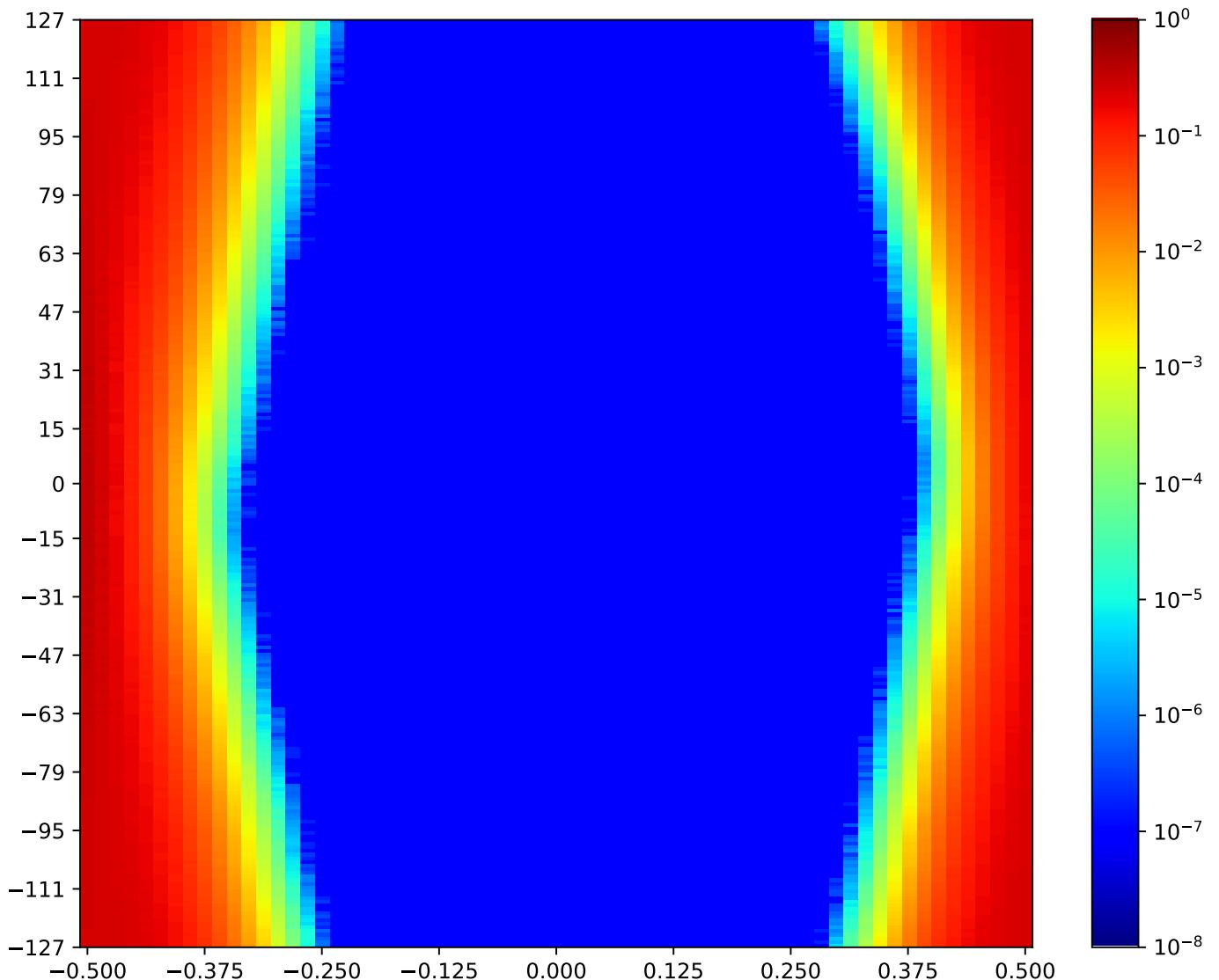


Figure 2.130: MSP\_A\_FPGA-TX1-02-RX18-02-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10.4 MSP\_A\_FPGA-TX1-03-RX18-03-MSP\_C\_FPGA

Table 2.121: MSP\_A\_FPGA-TX1-03-RX18-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:51:28		2018-Jan-24 20:52:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10104	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

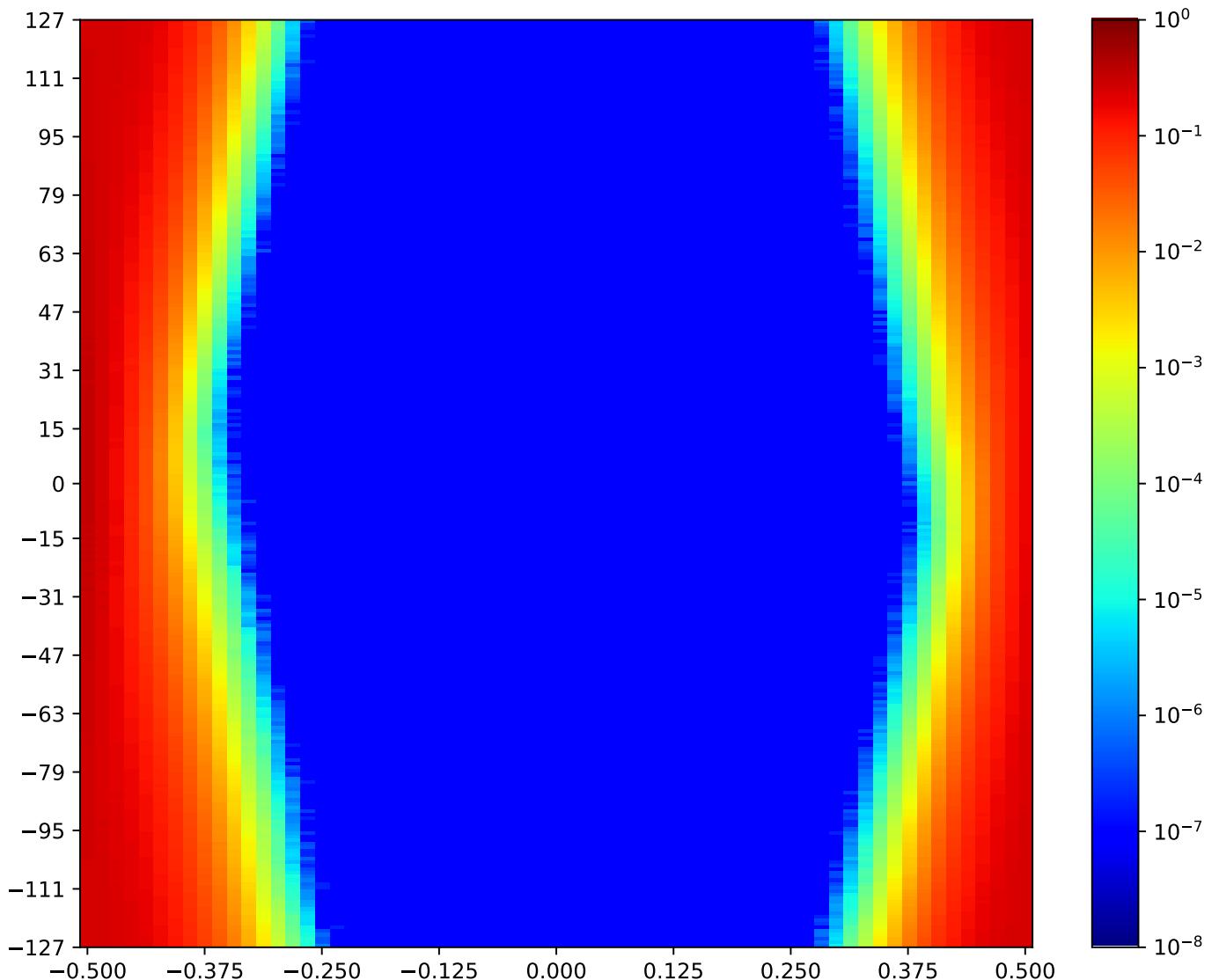


Figure 2.131: MSP\_A\_FPGA-TX1-03-RX18-03-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10.5 MSP\_A\_FPGA-TX1-04-RX18-04-MSP\_C\_FPGA

Table 2.122: MSP\_A\_FPGA-TX1-04-RX18-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:55:46		2018-Jan-24 20:56:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9627	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

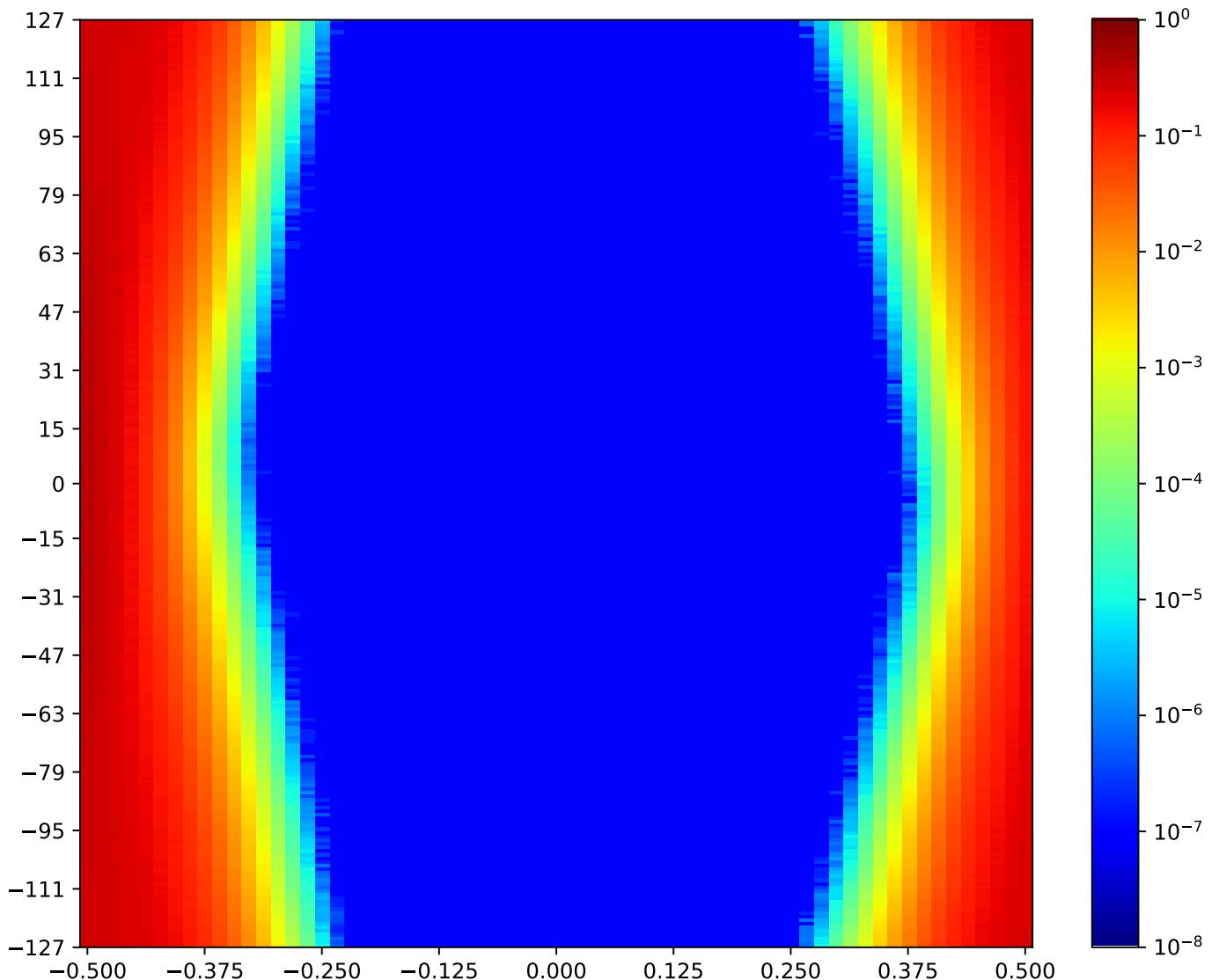


Figure 2.132: MSP\_A\_FPGA-TX1-04-RX18-04-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10.6 MSP\_A\_FPGA-TX1-05-RX18-05-MSP\_C\_FPGA

Table 2.123: MSP\_A\_FPGA-TX1-05-RX18-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:50:56		2018-Jan-24 20:51:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9172	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

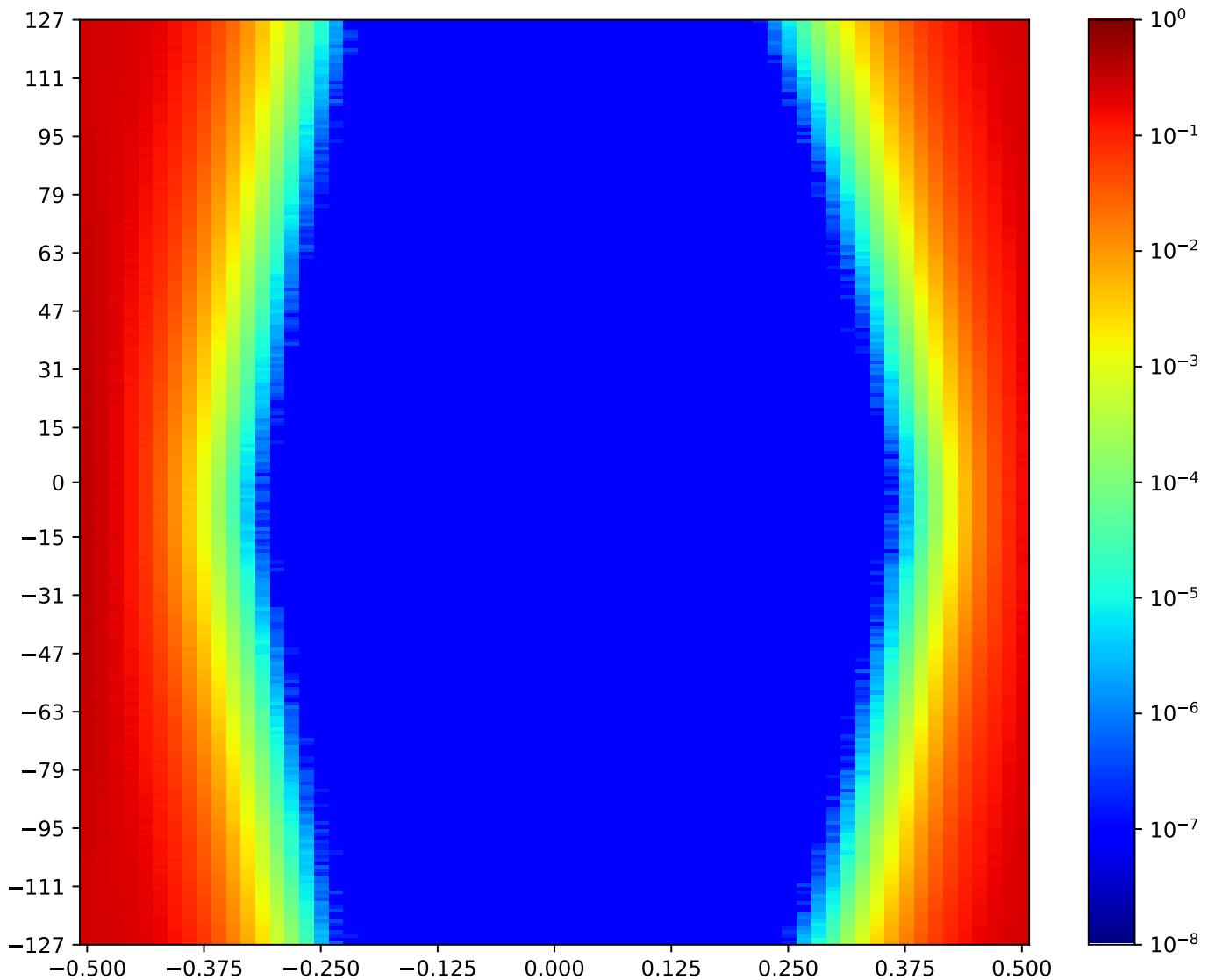


Figure 2.133: MSP\_A\_FPGA-TX1-05-RX18-05-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10.7 MSP\_A\_FPGA-TX1-06-RX18-06-MSP\_C\_FPGA

Table 2.124: MSP\_A\_FPGA-TX1-06-RX18-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:56:49		2018-Jan-24 20:57:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10839	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

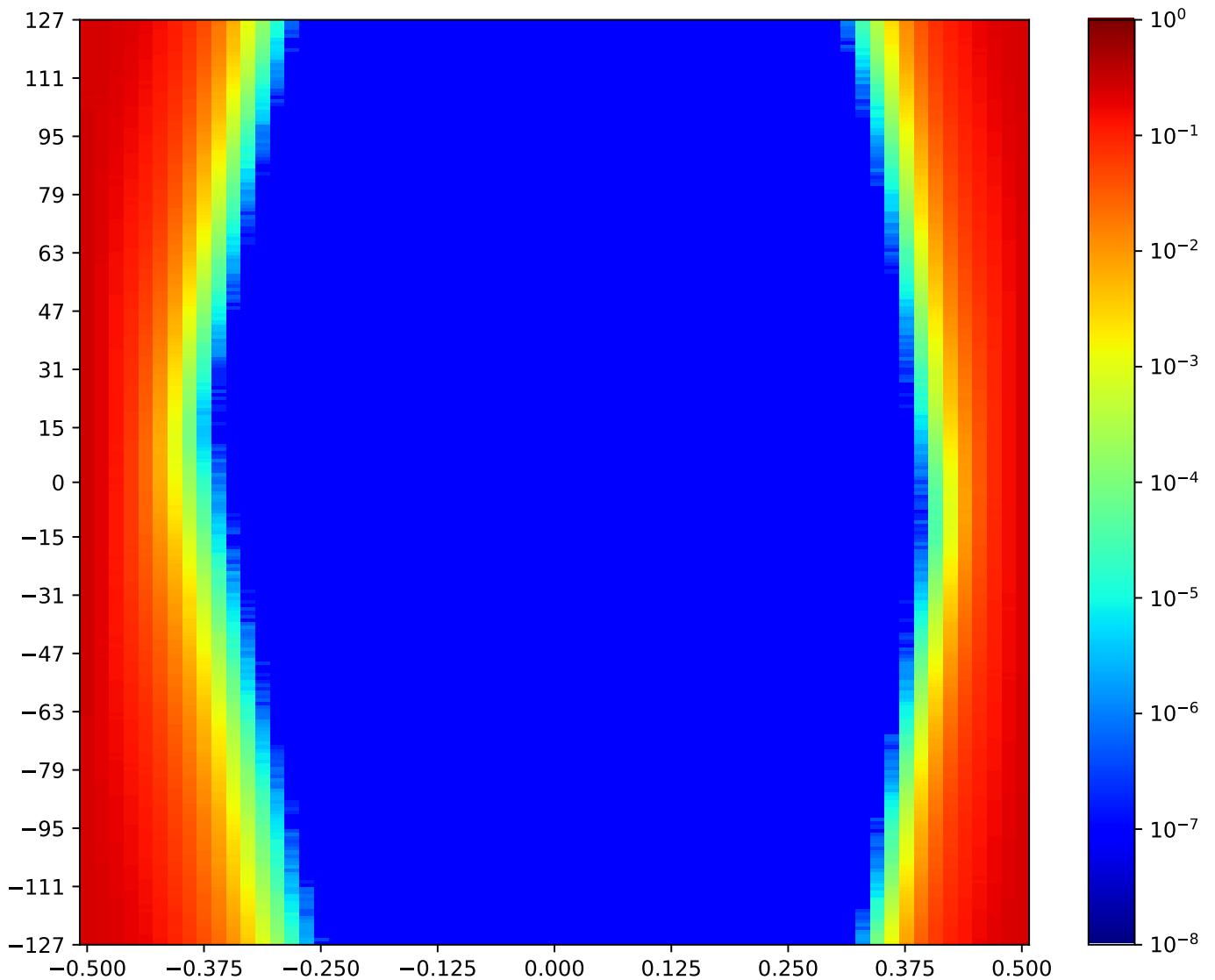


Figure 2.134: MSP\_A\_FPGA-TX1-06-RX18-06-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10.8 MSP\_A\_FPGA-TX1-07-RX18-07-MSP\_C\_FPGA

Table 2.125: MSP\_A\_FPGA-TX1-07-RX18-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:52:01		2018-Jan-24 20:52:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10640	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

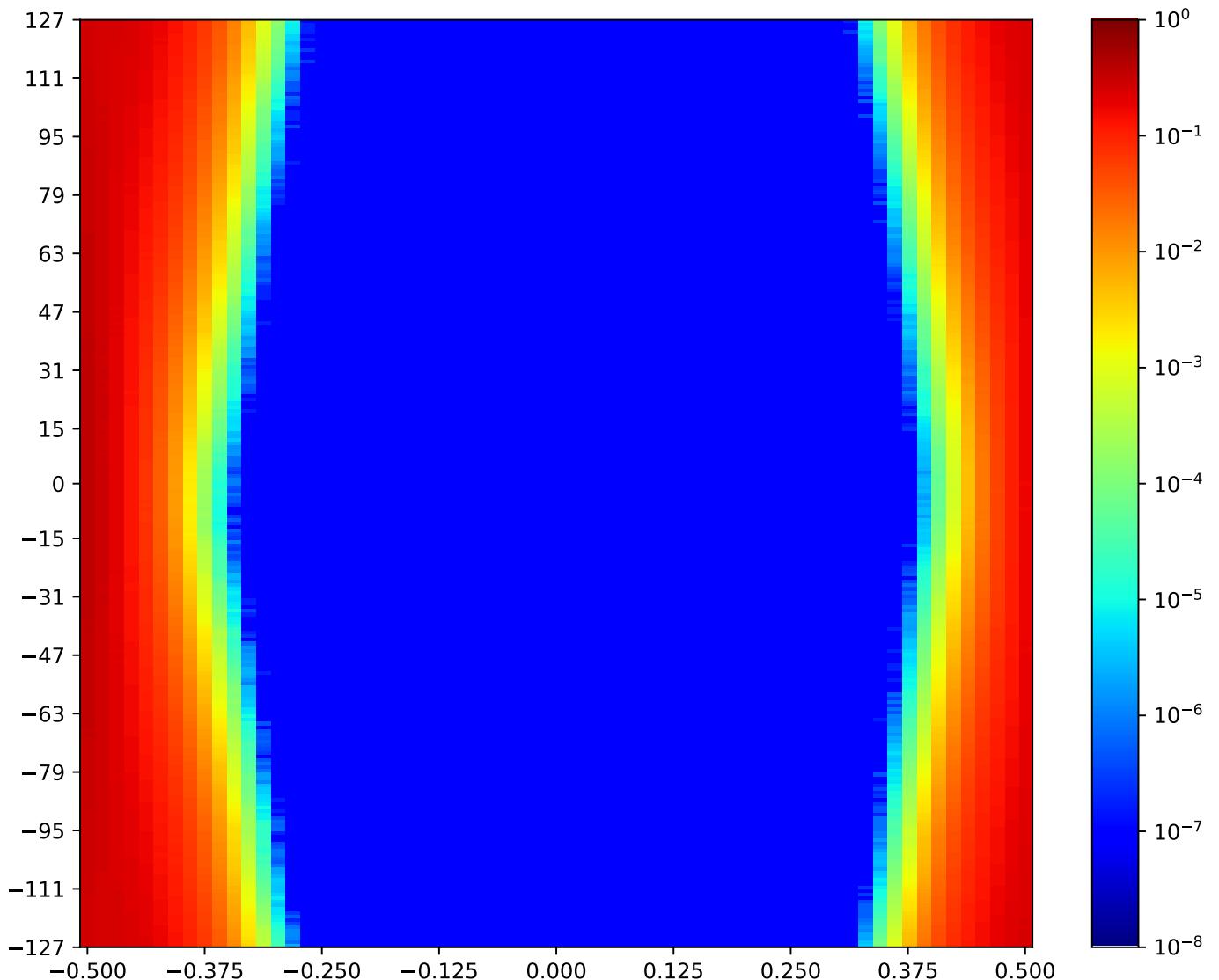


Figure 2.135: MSP\_A\_FPGA-TX1-07-RX18-07-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10.9 MSP\_A\_FPGA-TX1-08-RX18-08-MSP\_C\_FPGA

Table 2.126: MSP\_A\_FPGA-TX1-08-RX18-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:56:18		2018-Jan-24 20:56:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10512	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

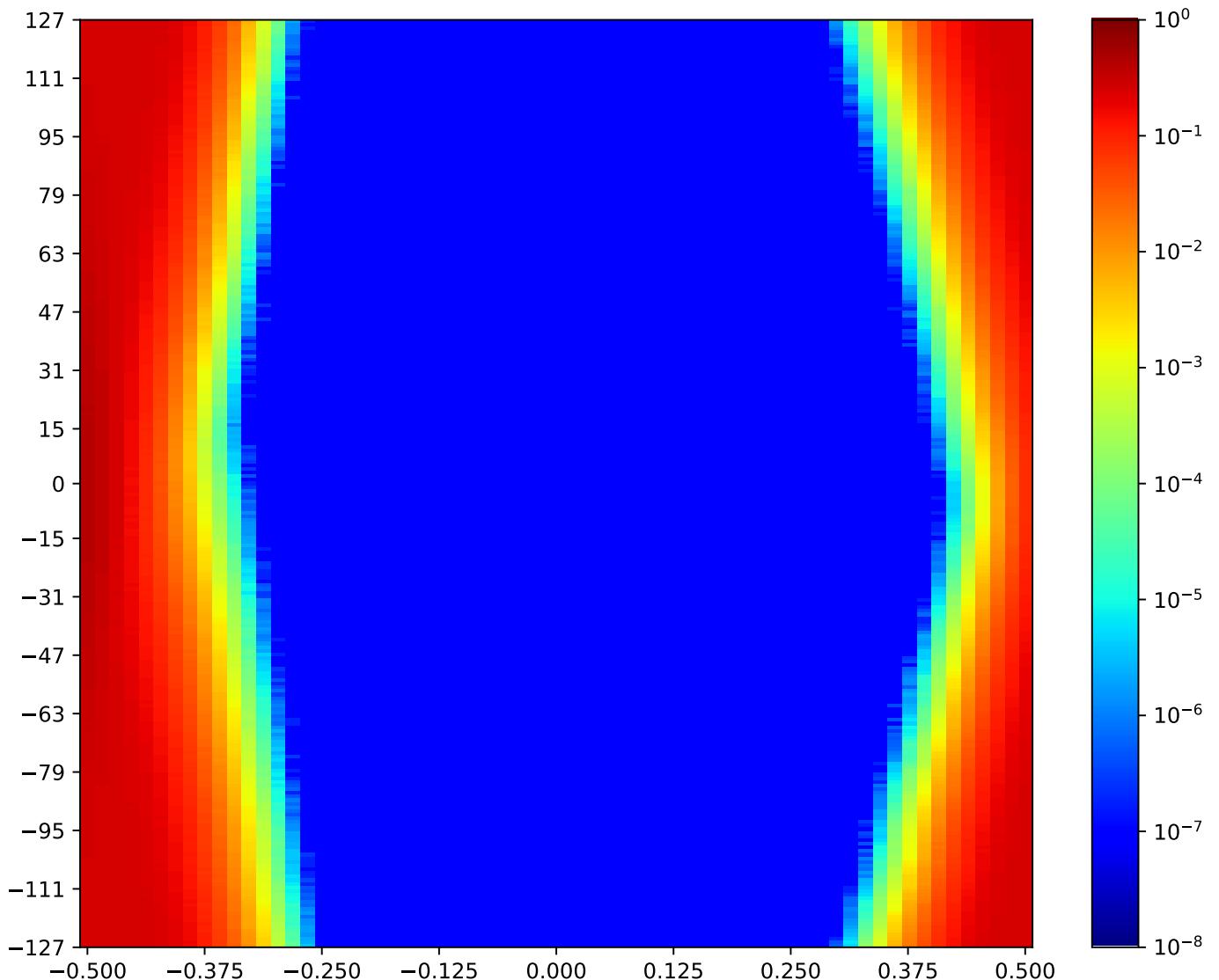


Figure 2.136: MSP\_A\_FPGA-TX1-08-RX18-08-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10.10 MSP\_A\_FPGA-TX1-09-RX18-09-MSP\_C\_FPGA

Table 2.127: MSP\_A\_FPGA-TX1-09-RX18-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:53:05		2018-Jan-24 20:53:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10479	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

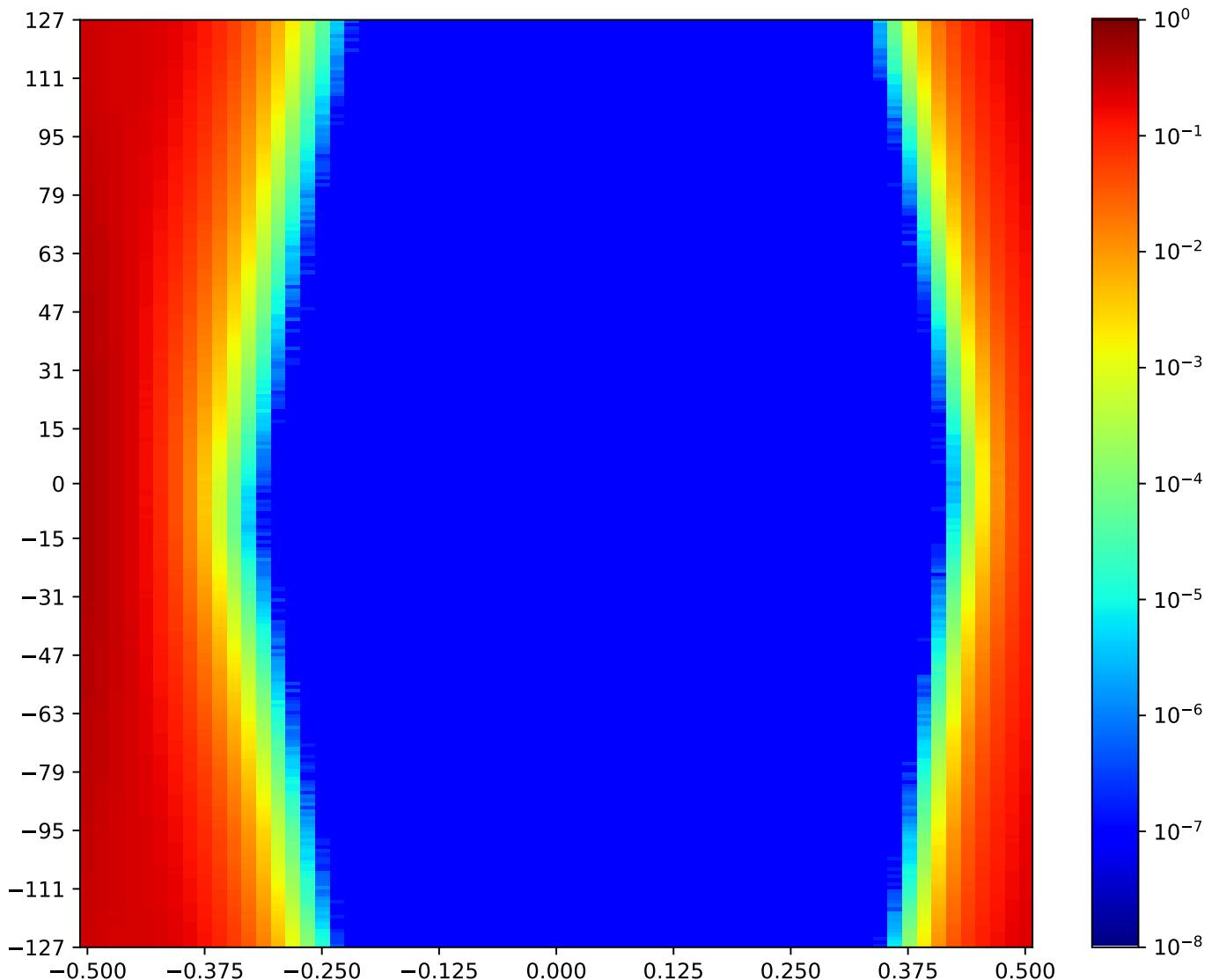


Figure 2.137: MSP\_A\_FPGA-TX1-09-RX18-09-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.10.11 MSP\_A\_FPGA-TX1-10-RX18-10-MSP\_C\_FPGA

Table 2.128: MSP\_A\_FPGA-TX1-10-RX18-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:55:16		2018-Jan-24 20:55:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9322	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

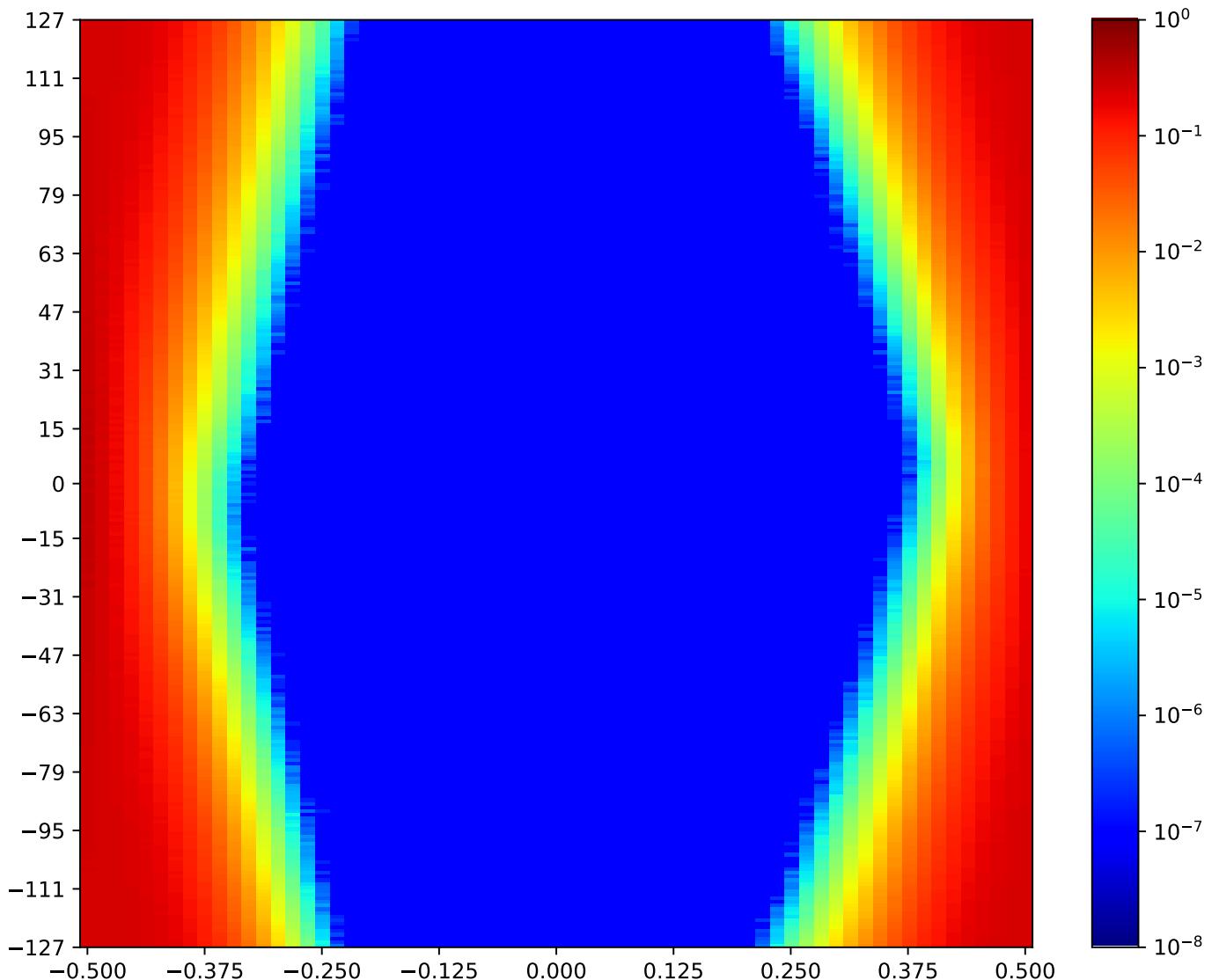


Figure 2.138: MSP\_A\_FPGA-TX1-10-RX18-10-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.10.12 MSP\_A\_FPGA-TX1-11-RX18-11-MSP\_C\_FPGA

Table 2.129: MSP\_A\_FPGA-TX1-11-RX18-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:54:42		2018-Jan-24 20:55:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11426	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

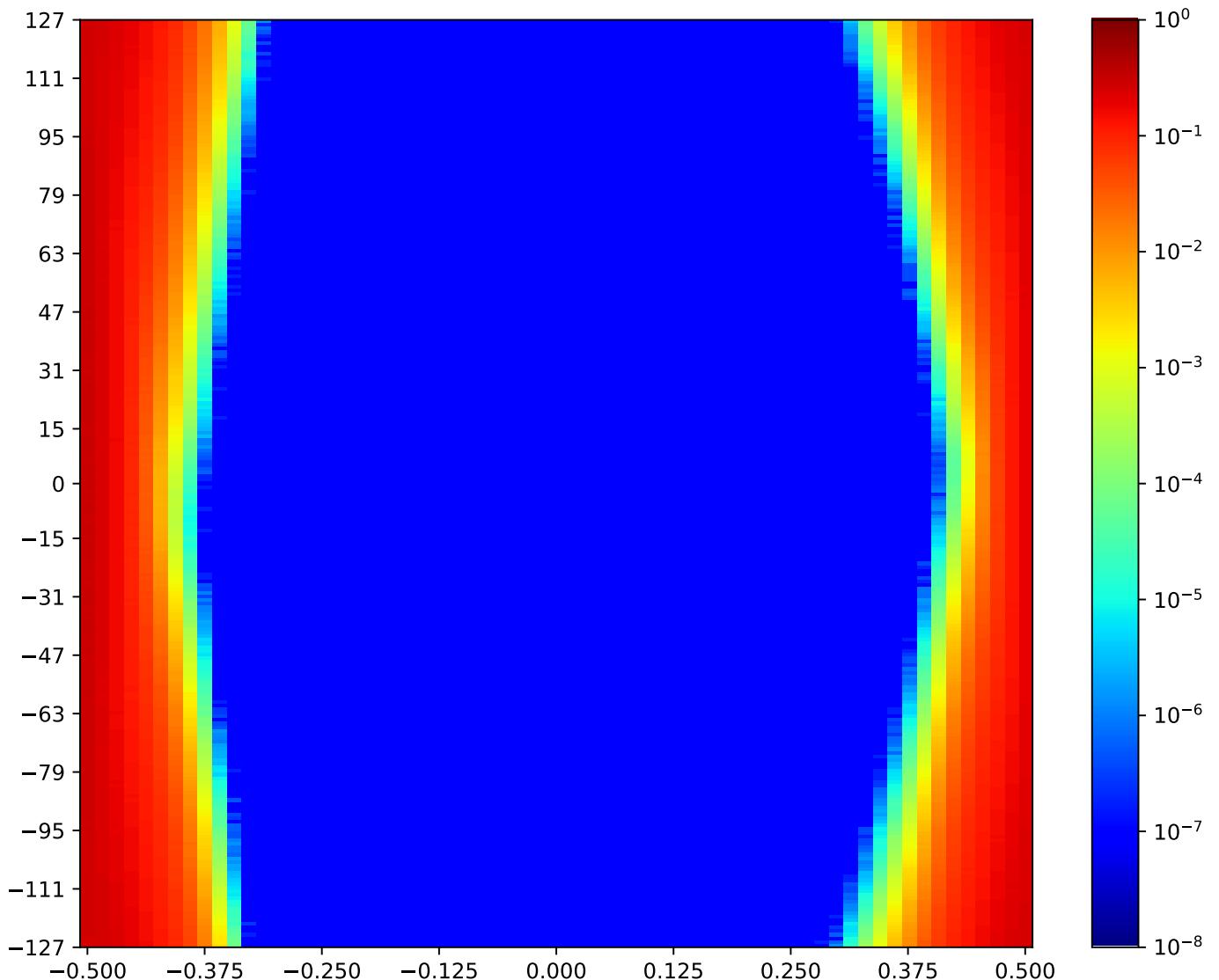


Figure 2.139: MSP\_A\_FPGA-TX1-11-RX18-11-MSP\_C\_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.11 MSP\_A TX2 MSP\_C RX17 Minipod Loopback

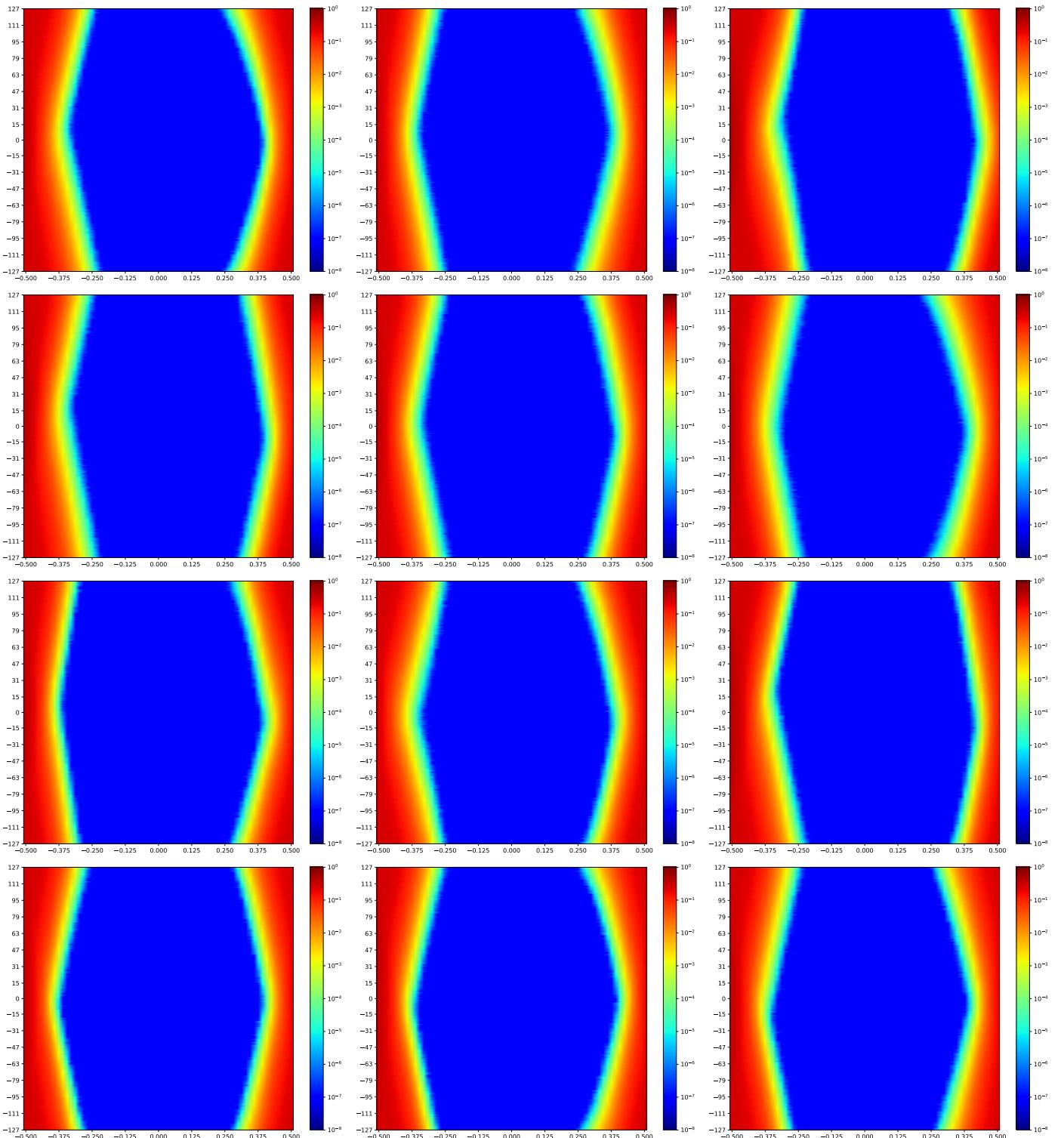


Figure 2.140: MSP\_A TX2 MSP\_C RX17 Minipod Loopback

A cross-reference to Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.153.

### 2.11.1 MSP\_A\_FPGA-TX2-00-RX17-00-MSP\_C\_FPGA

Table 2.130: MSP\_A\_FPGA-TX2-00-RX17-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:58:55		2018-Jan-24 20:59:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9626	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

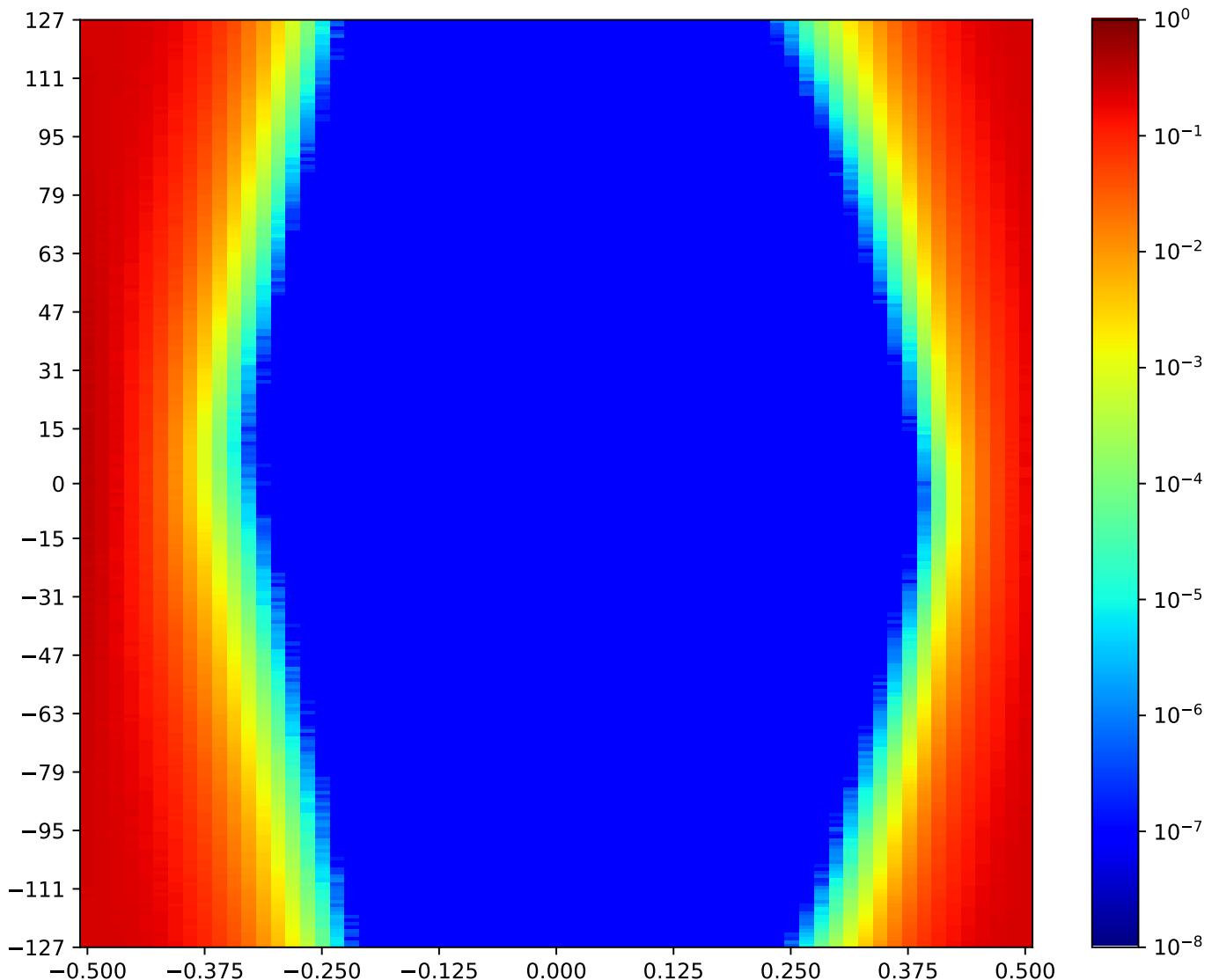


Figure 2.141: MSP\_A\_FPGA-TX2-00-RX17-00-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.11.2 MSP\_A\_FPGA-TX2-01-RX17-01-MSP\_C\_FPGA

Table 2.131: MSP\_A\_FPGA-TX2-01-RX17-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:57:53		2018-Jan-24 20:58:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9471	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

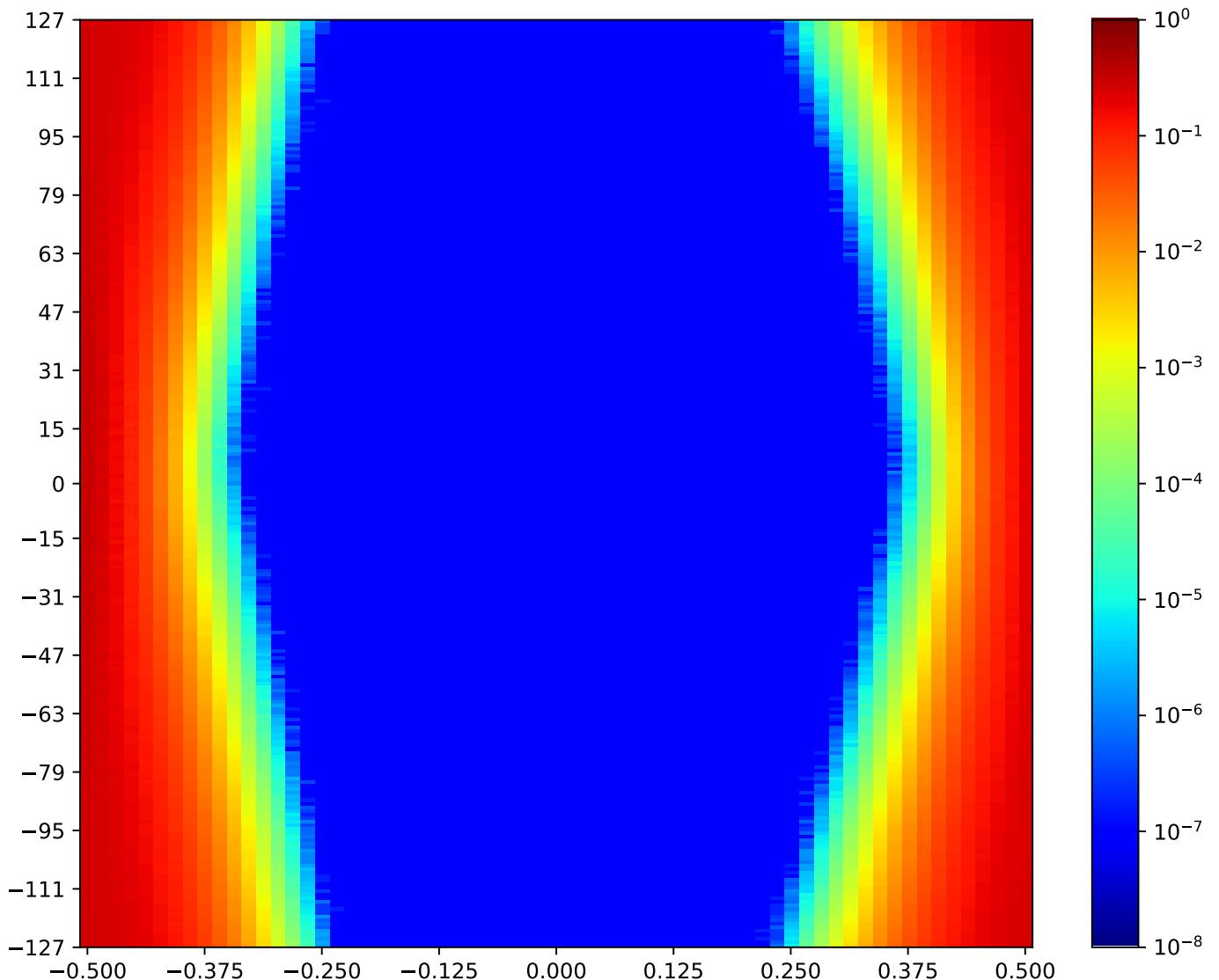


Figure 2.142: MSP\_A\_FPGA-TX2-01-RX17-01-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.11.3 MSP\_A\_FPGA-TX2-02-RX17-02-MSP\_C\_FPGA

Table 2.132: MSP\_A\_FPGA-TX2-02-RX17-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:00:24		2018-Jan-24 21:00:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9877	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

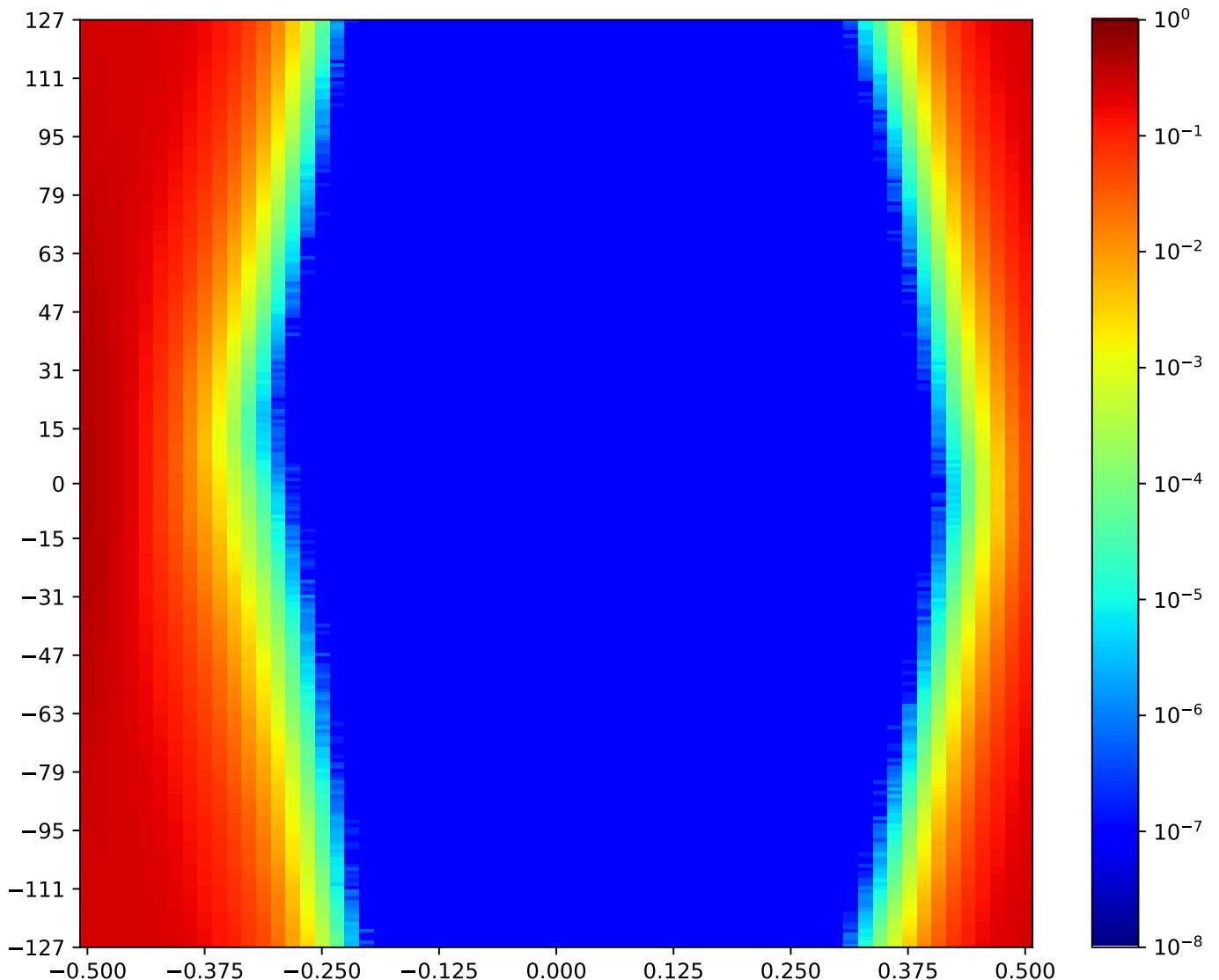


Figure 2.143: MSP\_A\_FPGA-TX2-02-RX17-02-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

#### 2.11.4 MSP\_A\_FPGA-TX2-03-RX17-03-MSP\_C\_FPGA

Table 2.133: MSP\_A\_FPGA-TX2-03-RX17-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:57:20		2018-Jan-24 20:57:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9841	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

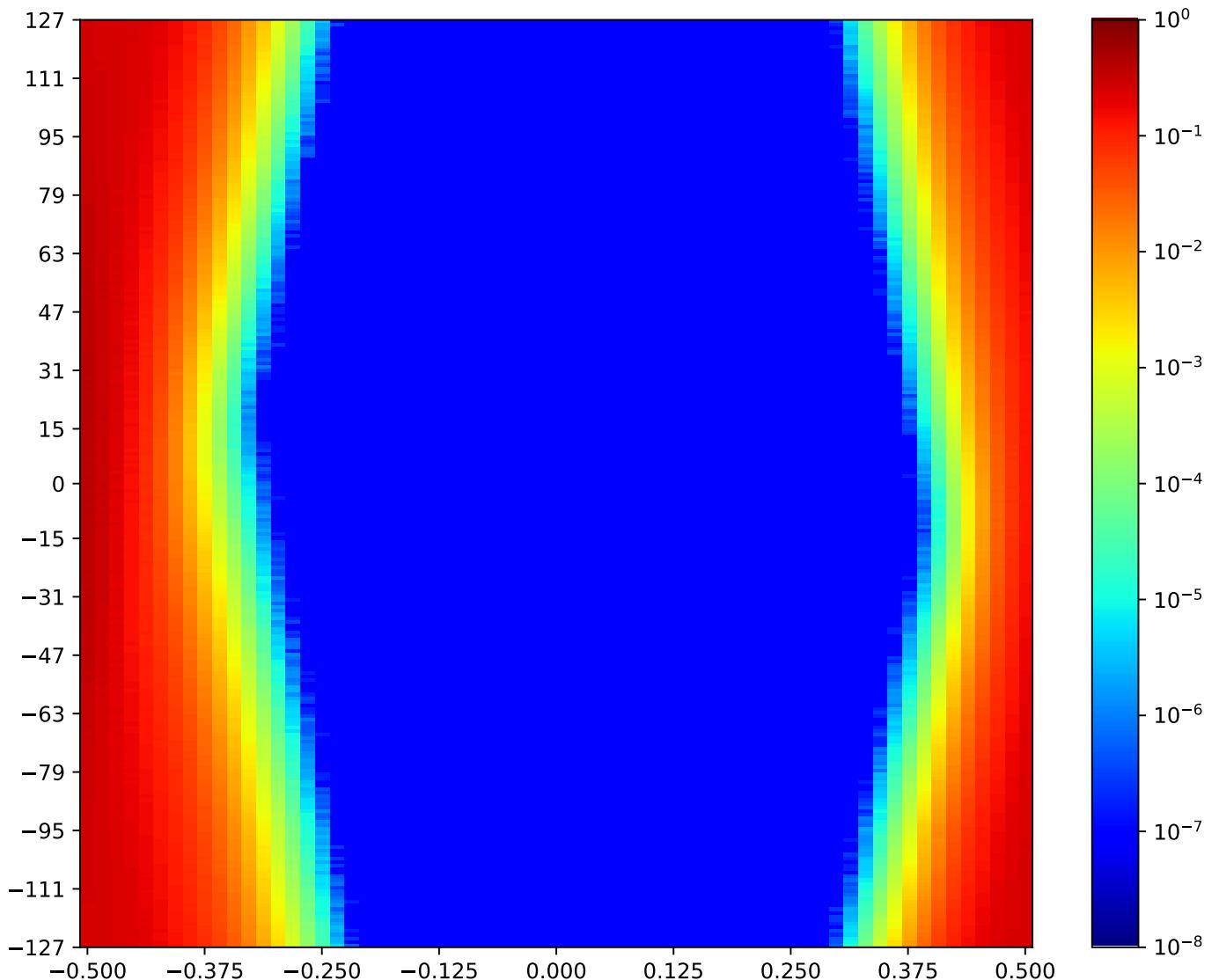


Figure 2.144: MSP\_A\_FPGA-TX2-03-RX17-03-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.11.5 MSP\_A\_FPGA-TX2-04-RX17-04-MSP\_C\_FPGA

Table 2.134: MSP\_A\_FPGA-TX2-04-RX17-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:01:56		2018-Jan-24 21:02:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9629	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

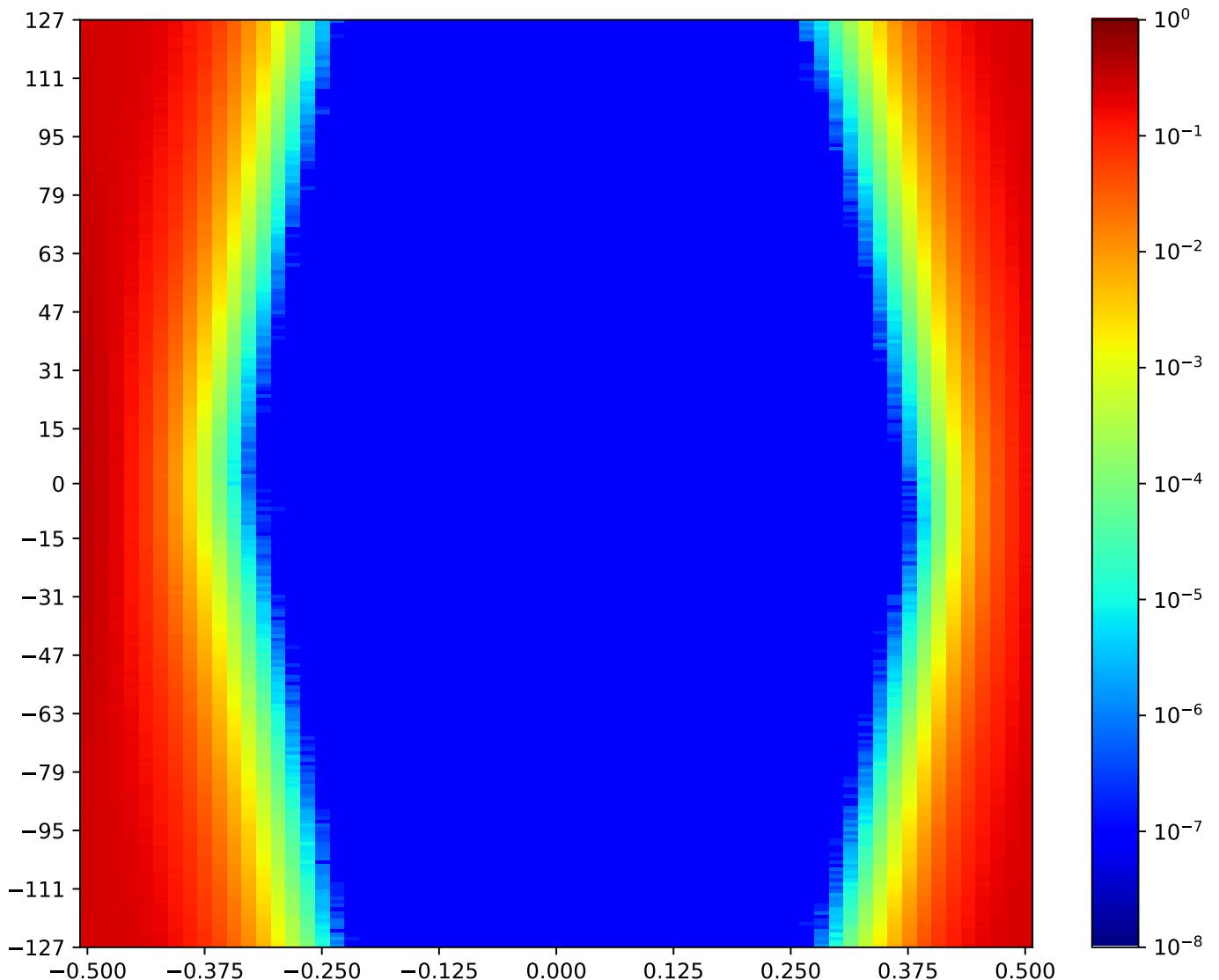


Figure 2.145: MSP\_A\_FPGA-TX2-04-RX17-04-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.11.6 MSP\_A\_FPGA-TX2-05-RX17-05-MSP\_C\_FPGA

Table 2.135: MSP\_A\_FPGA-TX2-05-RX17-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:58:25		2018-Jan-24 20:58:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8927	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

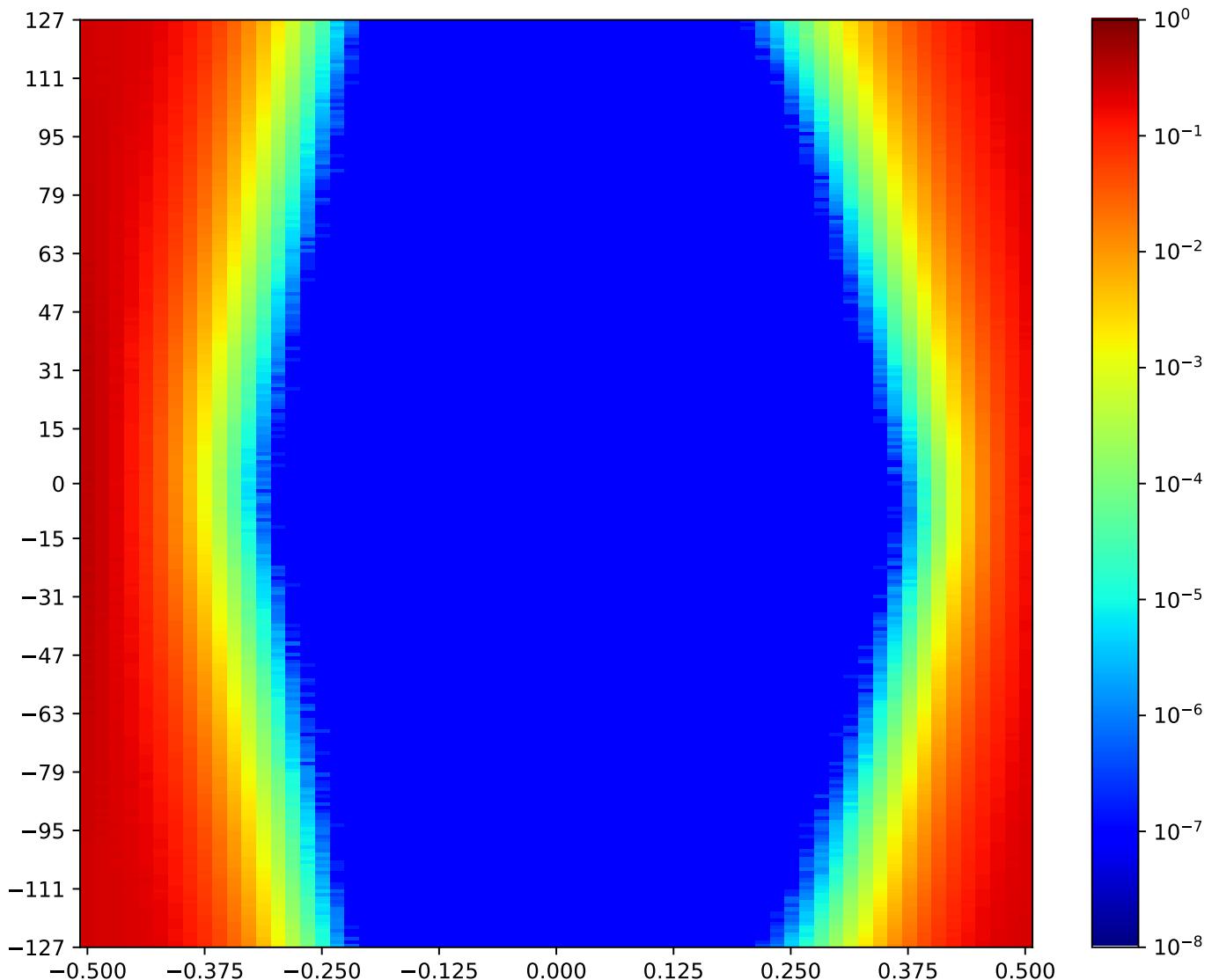


Figure 2.146: MSP\_A\_FPGA-TX2-05-RX17-05-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.11.7 MSP\_A\_FPGA-TX2-06-RX17-06-MSP\_C\_FPGA

Table 2.136: MSP\_A\_FPGA-TX2-06-RX17-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:02:56		2018-Jan-24 21:03:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10512	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

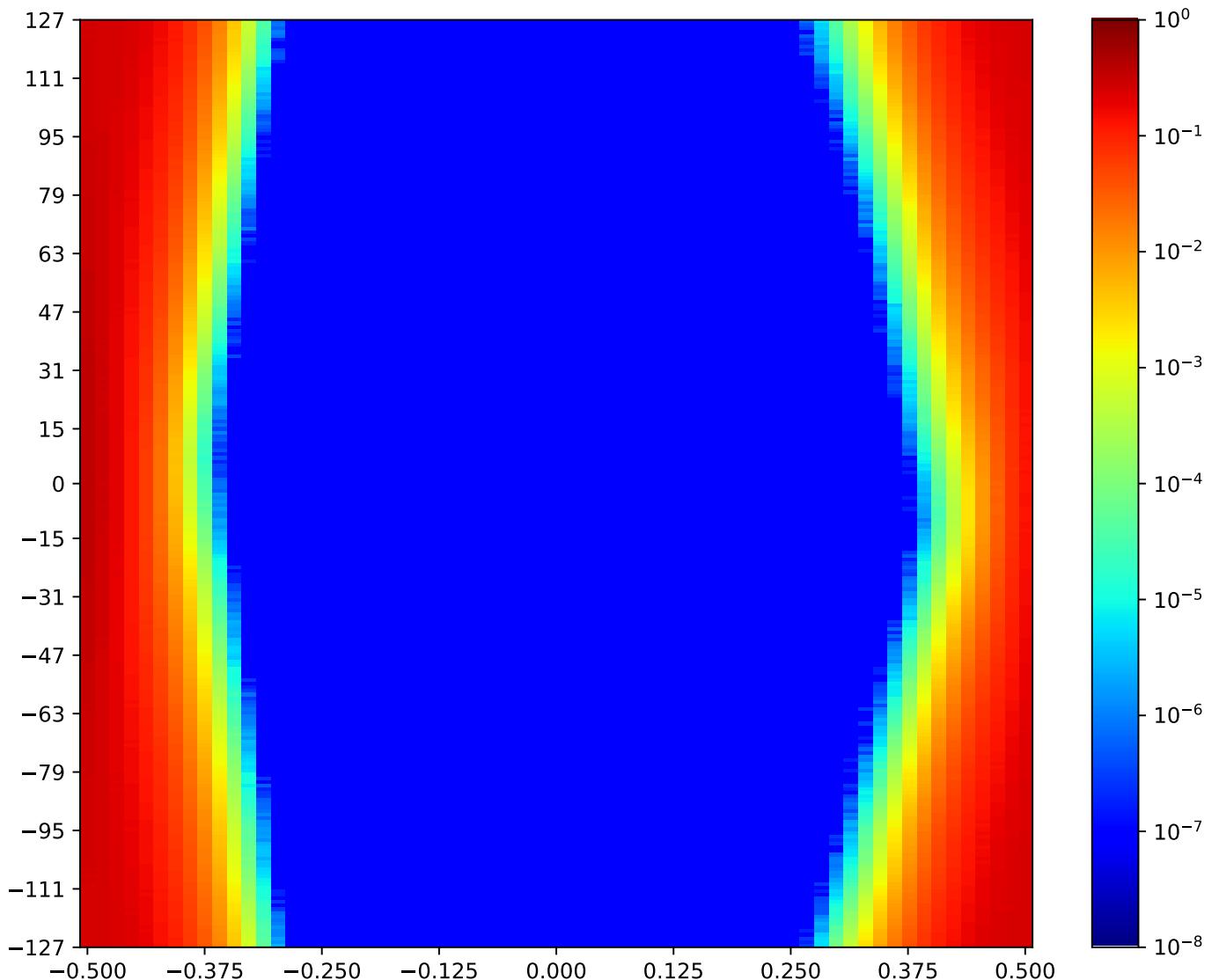


Figure 2.147: MSP\_A\_FPGA-TX2-06-RX17-06-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.11.8 MSP\_A\_FPGA-TX2-07-RX17-07-MSP\_C\_FPGA

Table 2.137: MSP\_A\_FPGA-TX2-07-RX17-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:59:25		2018-Jan-24 20:59:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9573	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

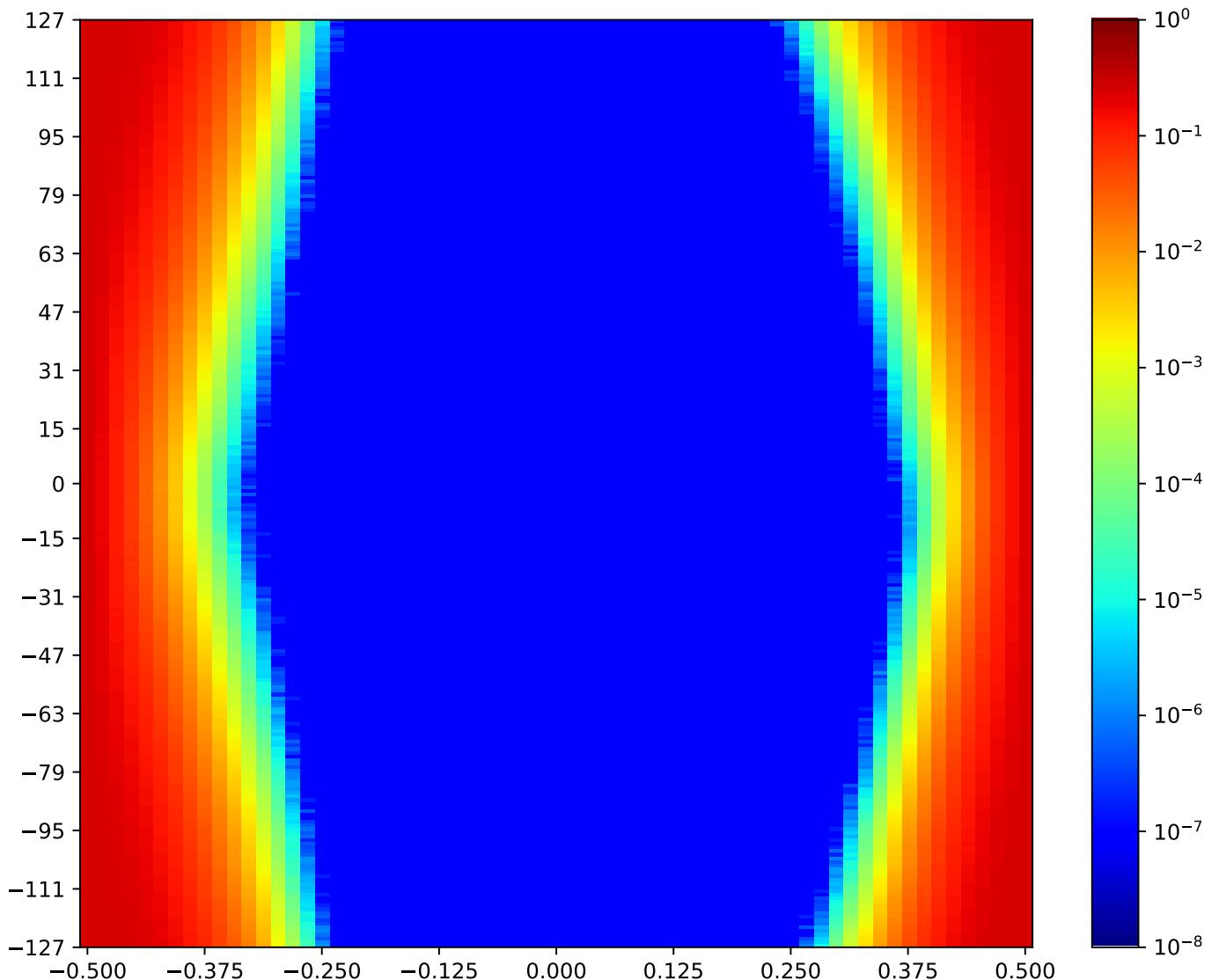


Figure 2.148: MSP\_A\_FPGA-TX2-07-RX17-07-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.11.9 MSP\_A\_FPGA-TX2-08-RX17-08-MSP\_C\_FPGA

Table 2.138: MSP\_A\_FPGA-TX2-08-RX17-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:02:26		2018-Jan-24 21:02:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10289	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

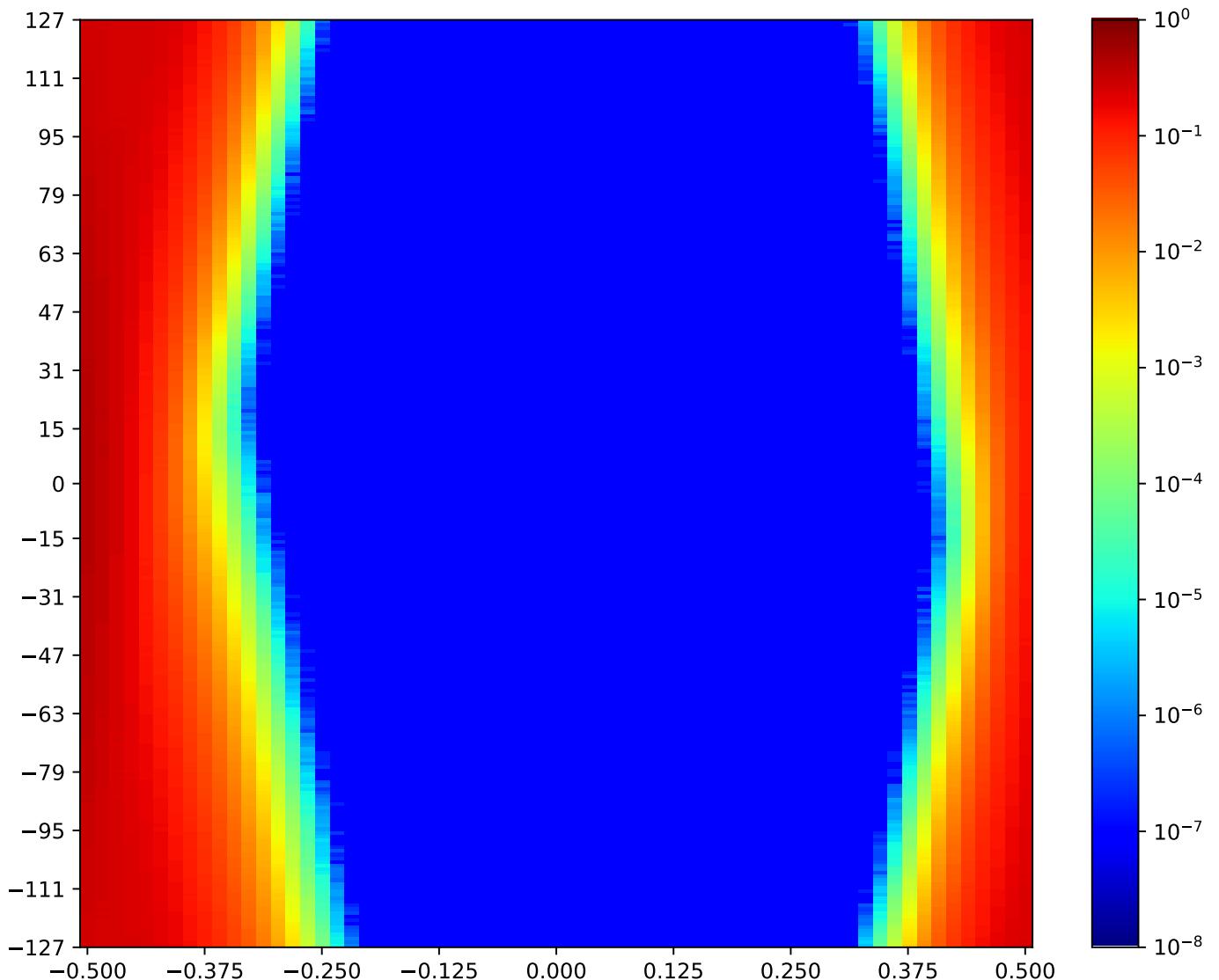


Figure 2.149: MSP\_A\_FPGA-TX2-08-RX17-08-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.11.10 MSP\_A\_FPGA-TX2-09-RX17-09-MSP\_C\_FPGA

Table 2.139: MSP\_A\_FPGA-TX2-09-RX17-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 20:59:54		2018-Jan-24 21:00:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10532	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

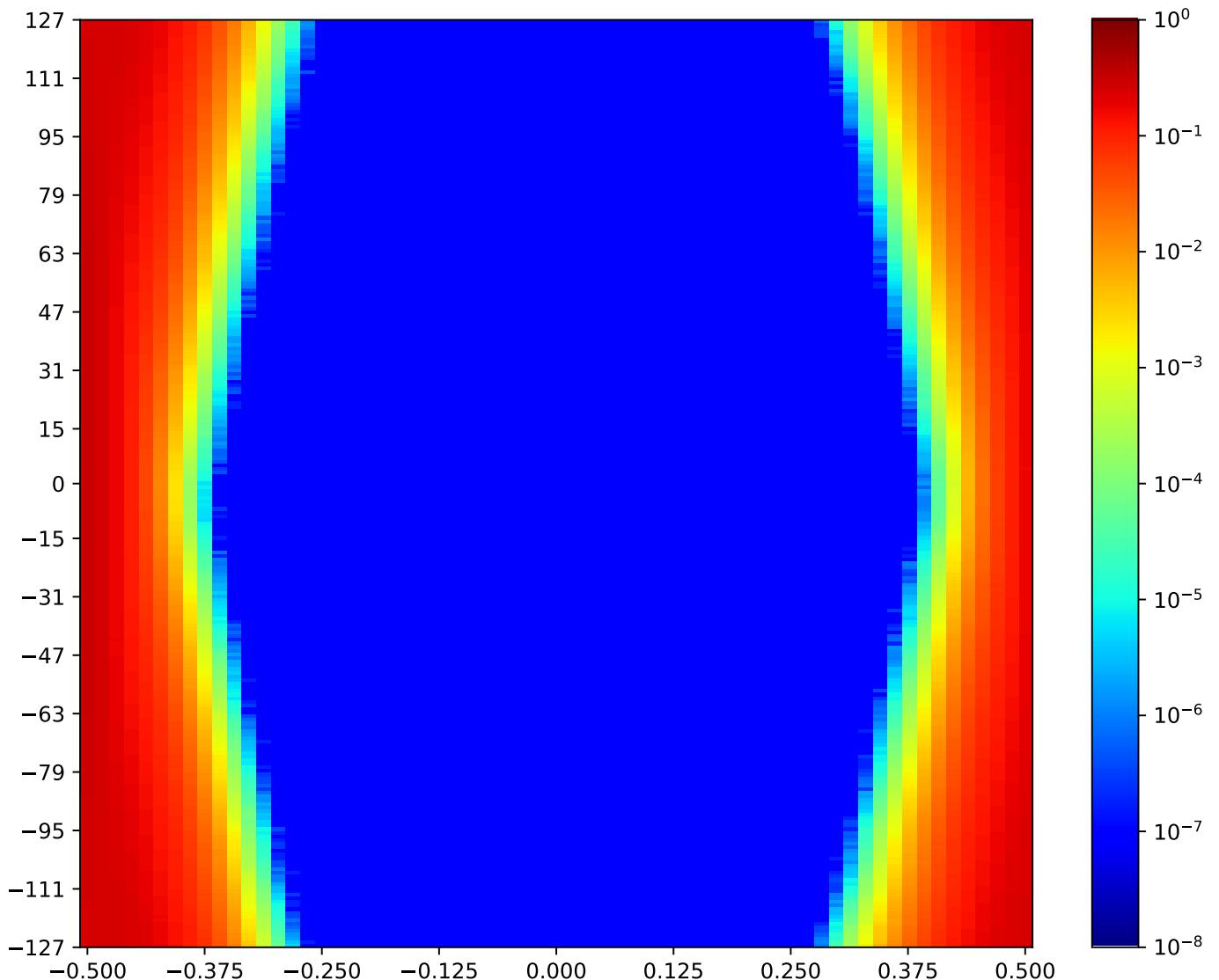


Figure 2.150: MSP\_A\_FPGA-TX2-09-RX17-09-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.11.11 MSP\_A\_FPGA-TX2-10-RX17-10-MSP\_C\_FPGA

Table 2.140: MSP\_A\_FPGA-TX2-10-RX17-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:01:26		2018-Jan-24 21:01:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10263	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

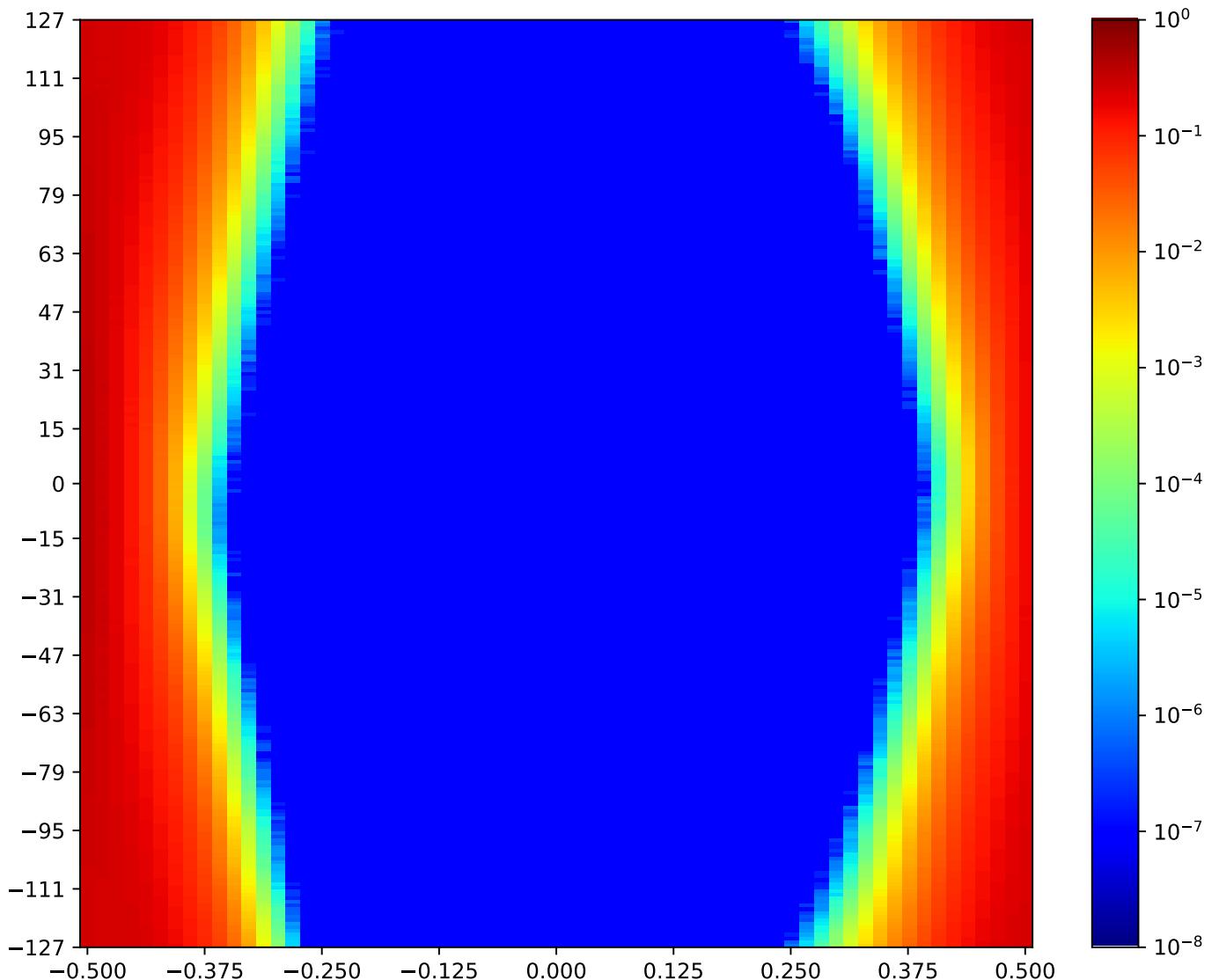


Figure 2.151: MSP\_A\_FPGA-TX2-10-RX17-10-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.11.12 MSP\_A\_FPGA-TX2-11-RX17-11-MSP\_C\_FPGA

Table 2.141: MSP\_A\_FPGA-TX2-11-RX17-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:00:54		2018-Jan-24 21:01:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9883	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

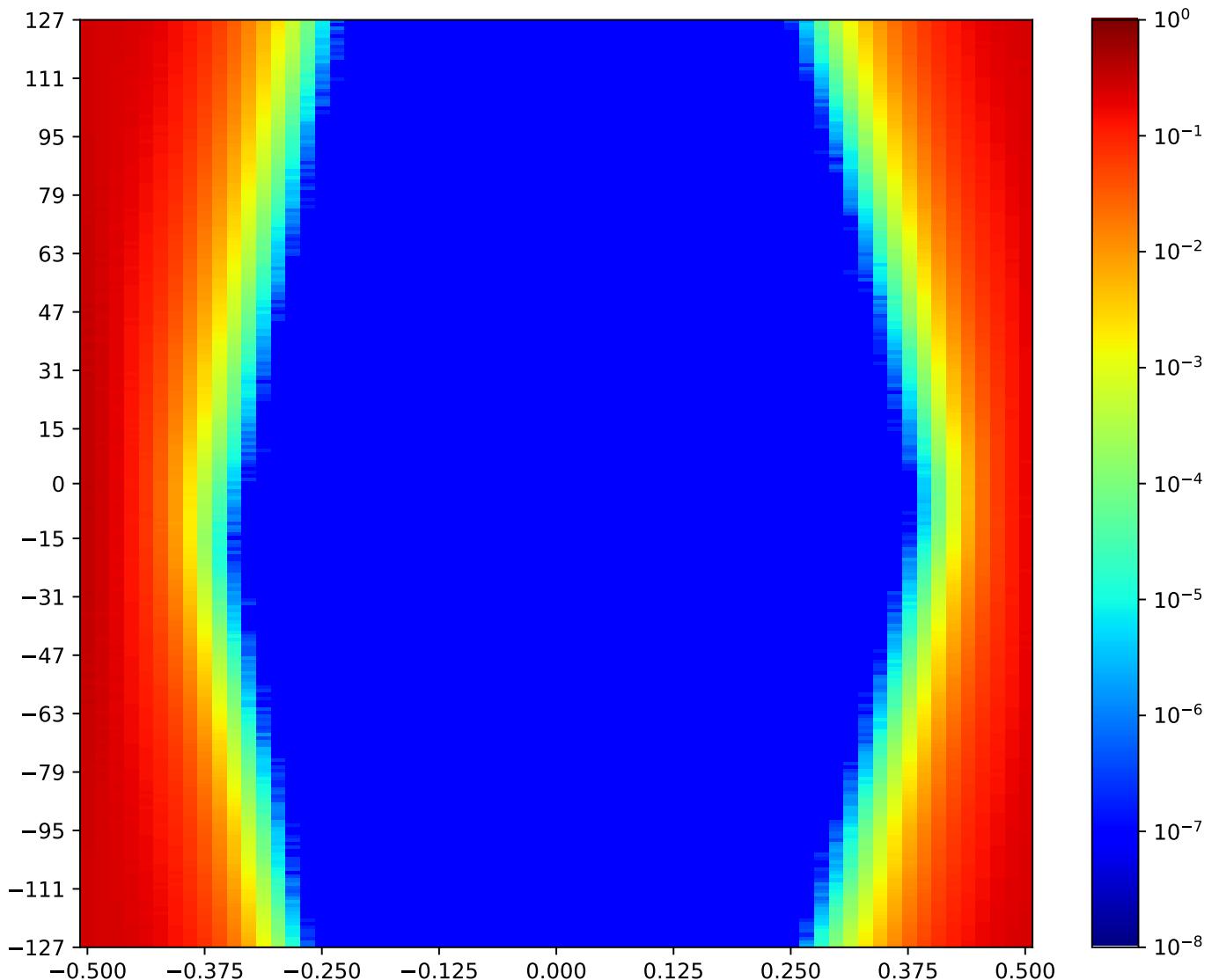


Figure 2.152: MSP\_A\_FPGA-TX2-11-RX17-11-MSP\_C\_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.12 MSP\_C TX3 MSP\_A RX9 Minipod Loopback

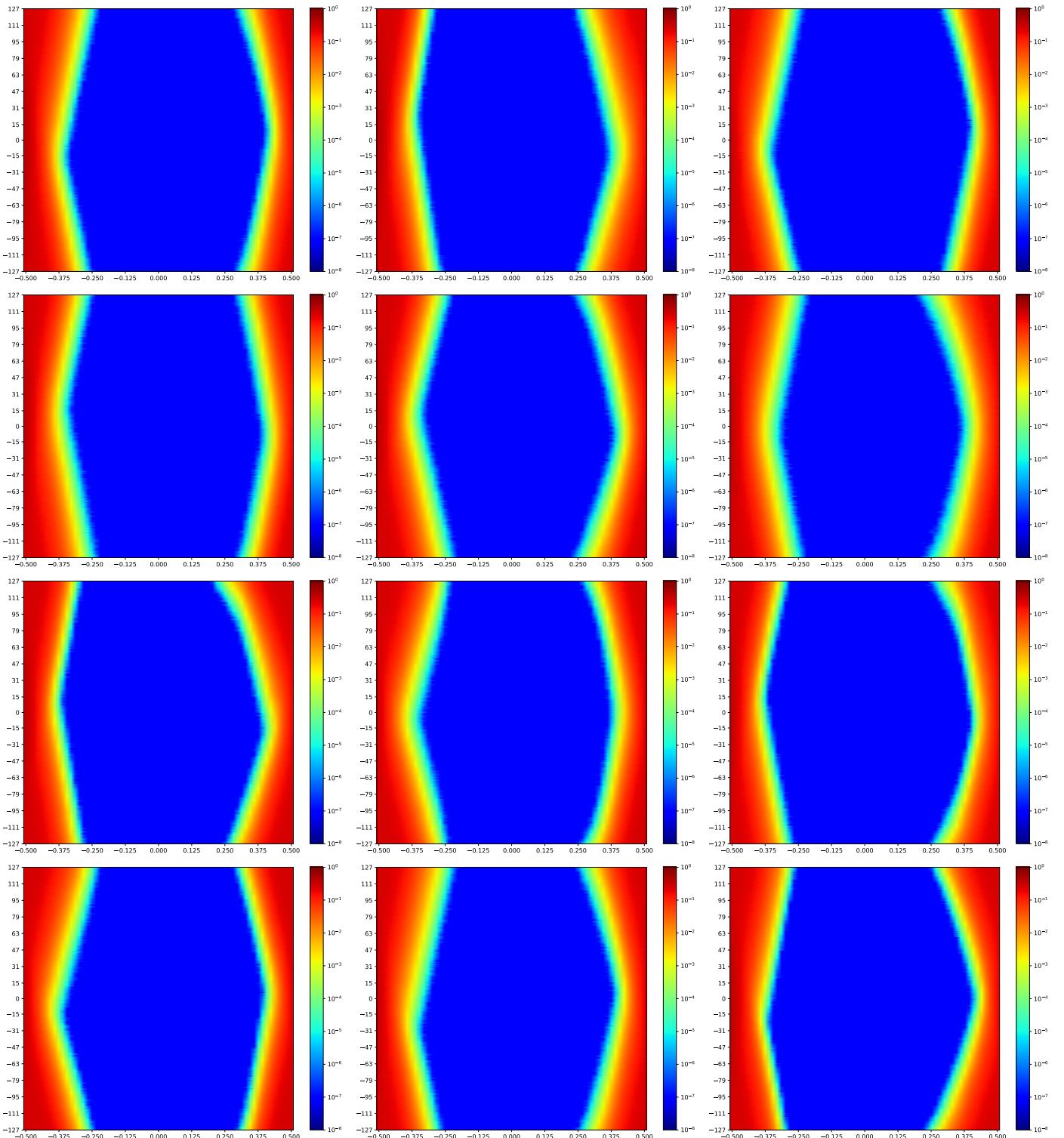


Figure 2.153: MSP\_C TX3 MSP\_A RX9 Minipod Loopback

A cross-reference to Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.166.

### 2.12.1 MSP\_C\_FPGA-TX3-00-RX9-00-MSP\_A\_FPGA

Table 2.142: MSP\_C\_FPGA-TX3-00-RX9-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:05:00		2018-Jan-24 21:05:29	
Reset RX	OA	HO		HO (%)	
true	10222	45		69.23%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

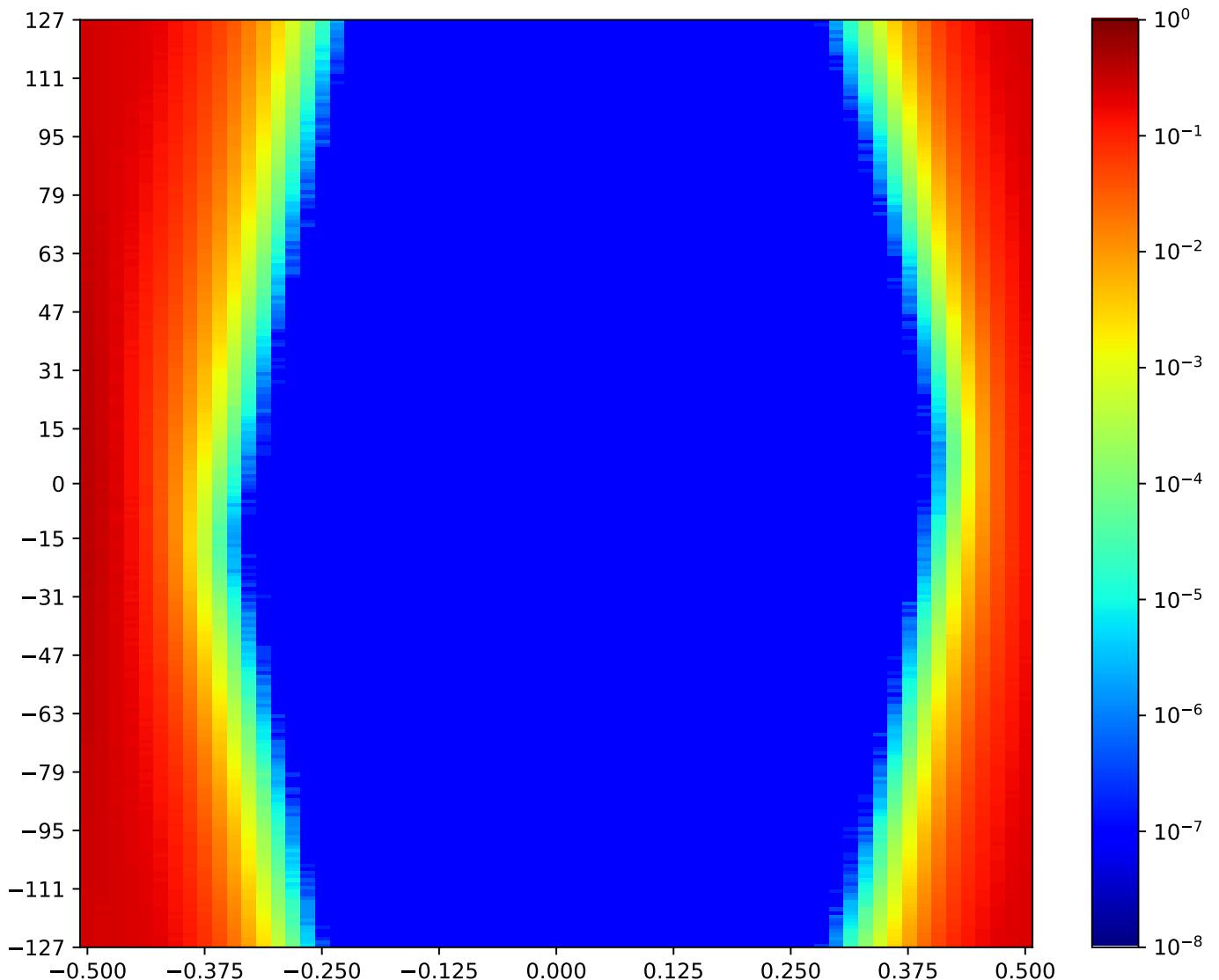


Figure 2.154: MSP\_C\_FPGA-TX3-00-RX9-00-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.12.2 MSP\_C\_FPGA-TX3-01-RX9-01-MSP\_A\_FPGA

Table 2.143: MSP\_C\_FPGA-TX3-01-RX9-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:06:03		2018-Jan-24 21:06:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9681	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

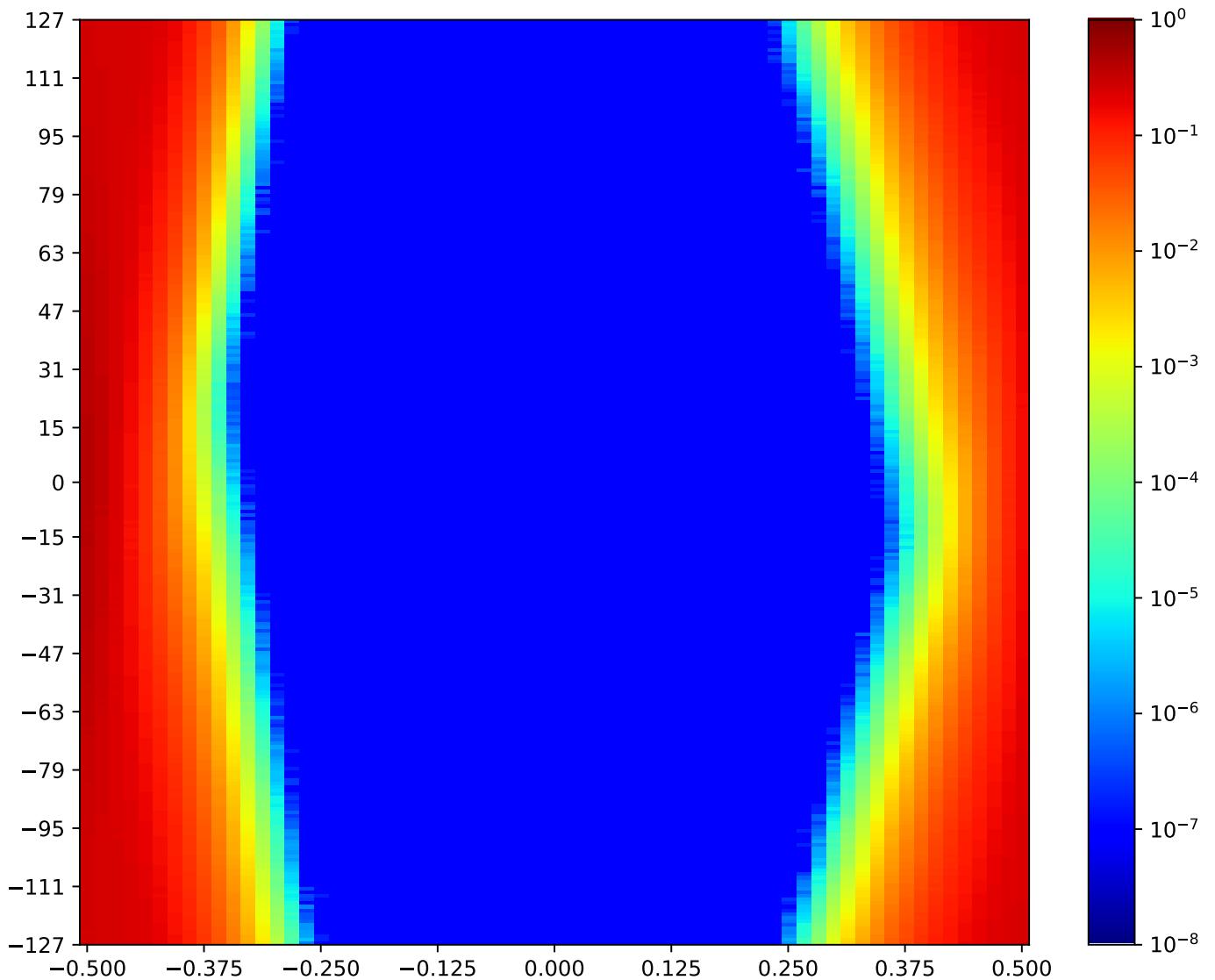


Figure 2.155: MSP\_C\_FPGA-TX3-01-RX9-01-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.12.3 MSP\_C\_FPGA-TX3-02-RX9-02-MSP\_A\_FPGA

Table 2.144: MSP\_C\_FPGA-TX3-02-RX9-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:06:32		2018-Jan-24 21:07:03	
Reset RX	OA	HO		HO (%)	
true	10021	44		67.69%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

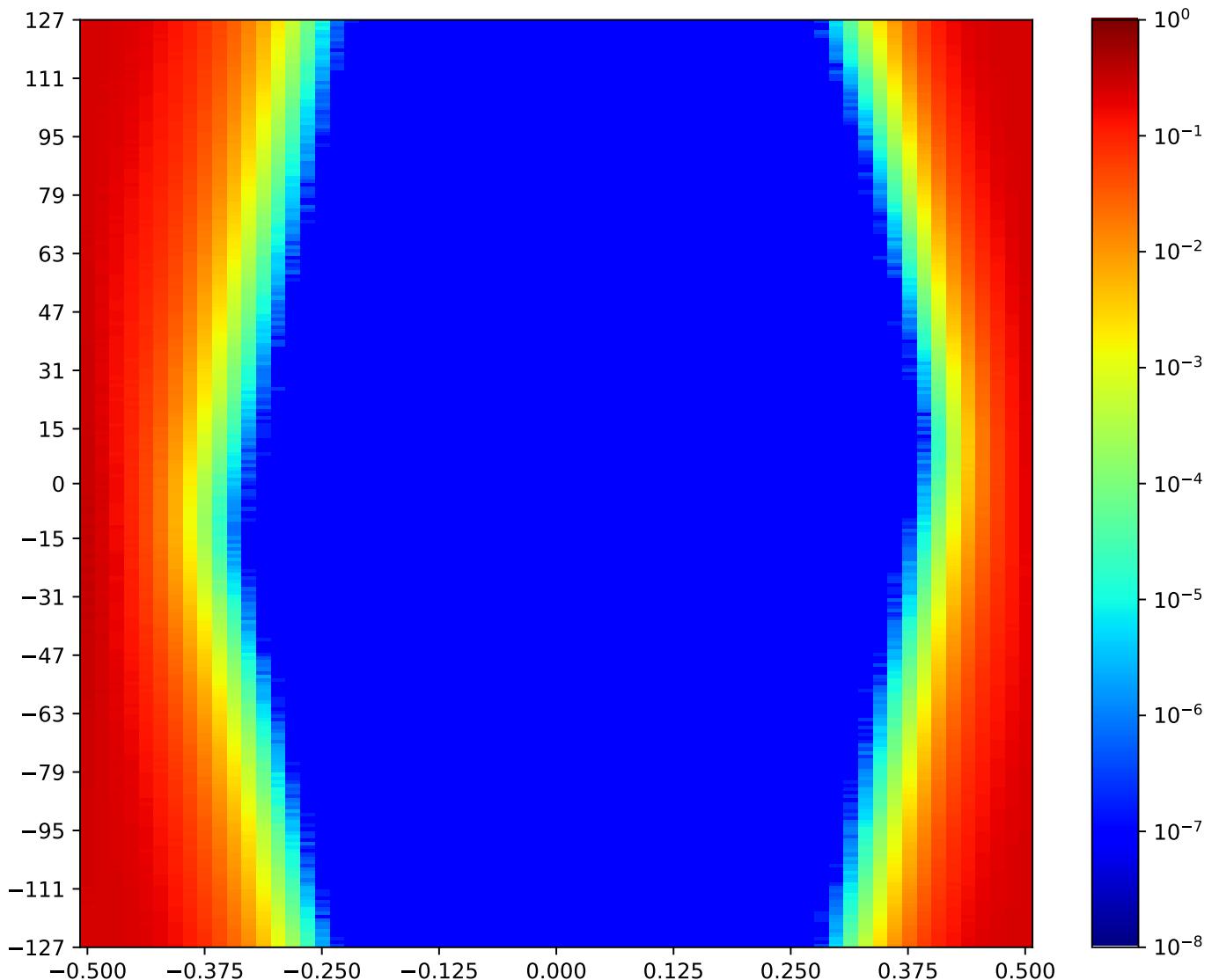


Figure 2.156: MSP\_C\_FPGA-TX3-02-RX9-02-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.12.4 MSP\_C\_FPGA-TX3-03-RX9-03-MSP\_A\_FPGA

Table 2.145: MSP\_C\_FPGA-TX3-03-RX9-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:03:58		2018-Jan-24 21:04:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9880	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

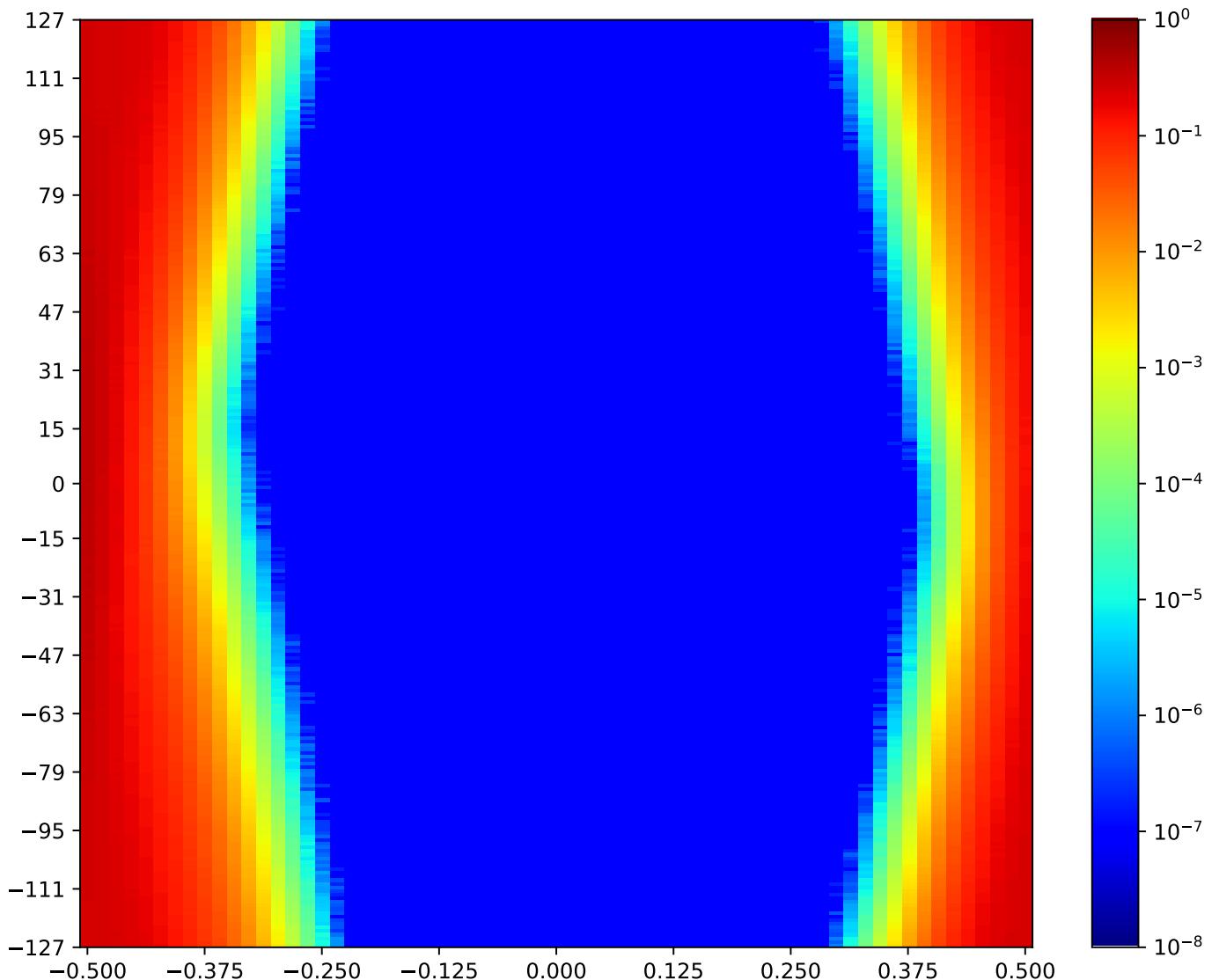


Figure 2.157: MSP\_C\_FPGA-TX3-03-RX9-03-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.12.5 MSP\_C\_FPGA-TX3-04-RX9-04-MSP\_A\_FPGA

Table 2.146: MSP\_C\_FPGA-TX3-04-RX9-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:08:02		2018-Jan-24 21:08:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9252	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

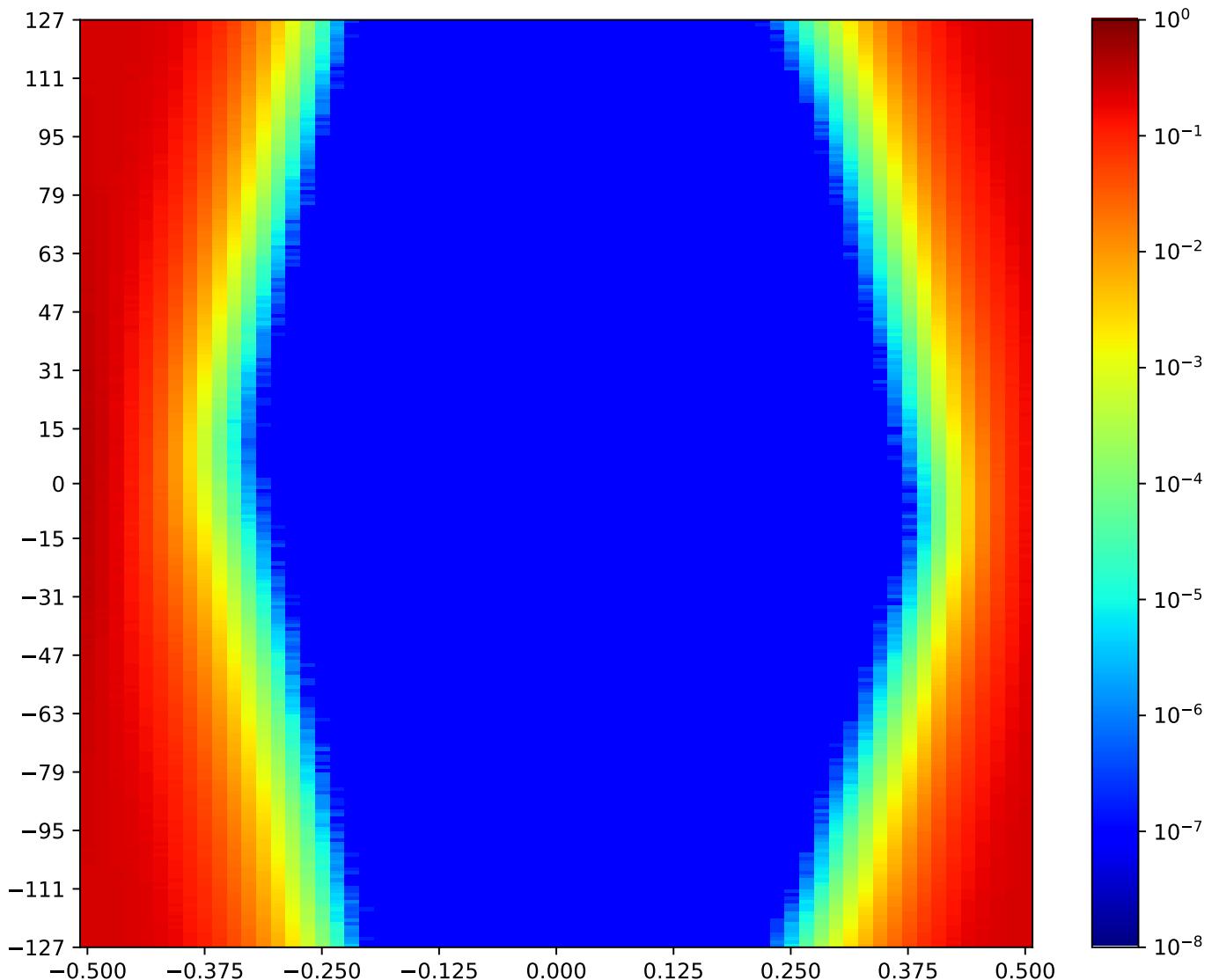


Figure 2.158: MSP\_C\_FPGA-TX3-04-RX9-04-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.12.6 MSP\_C\_FPGA-TX3-05-RX9-05-MSP\_A\_FPGA

Table 2.147: MSP\_C\_FPGA-TX3-05-RX9-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:03:26		2018-Jan-24 21:03:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8843	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

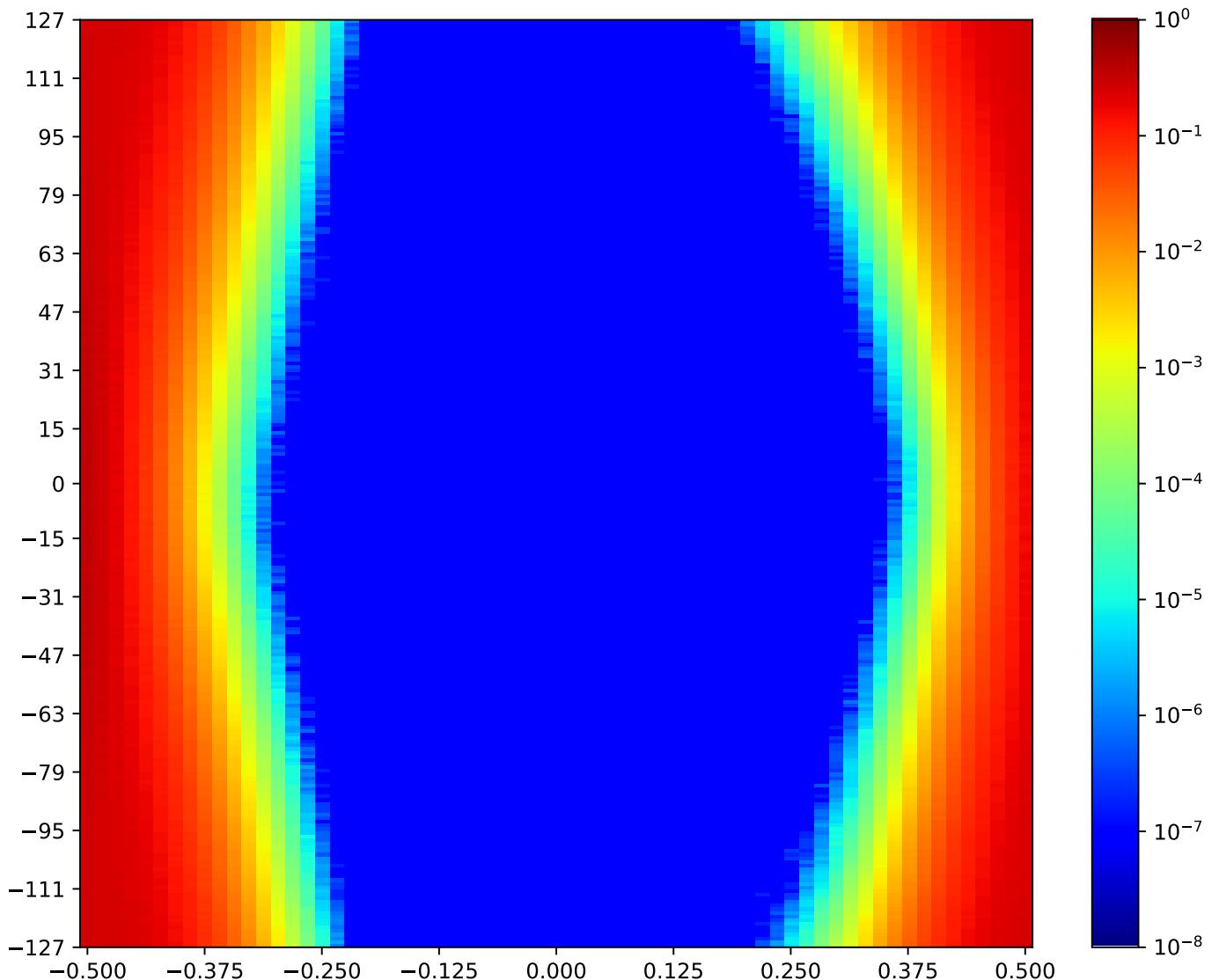


Figure 2.159: MSP\_C\_FPGA-TX3-05-RX9-05-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.12.7 MSP\_C\_FPGA-TX3-06-RX9-06-MSP\_A\_FPGA

Table 2.148: MSP\_C\_FPGA-TX3-06-RX9-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:09:01		2018-Jan-24 21:09:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10207	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

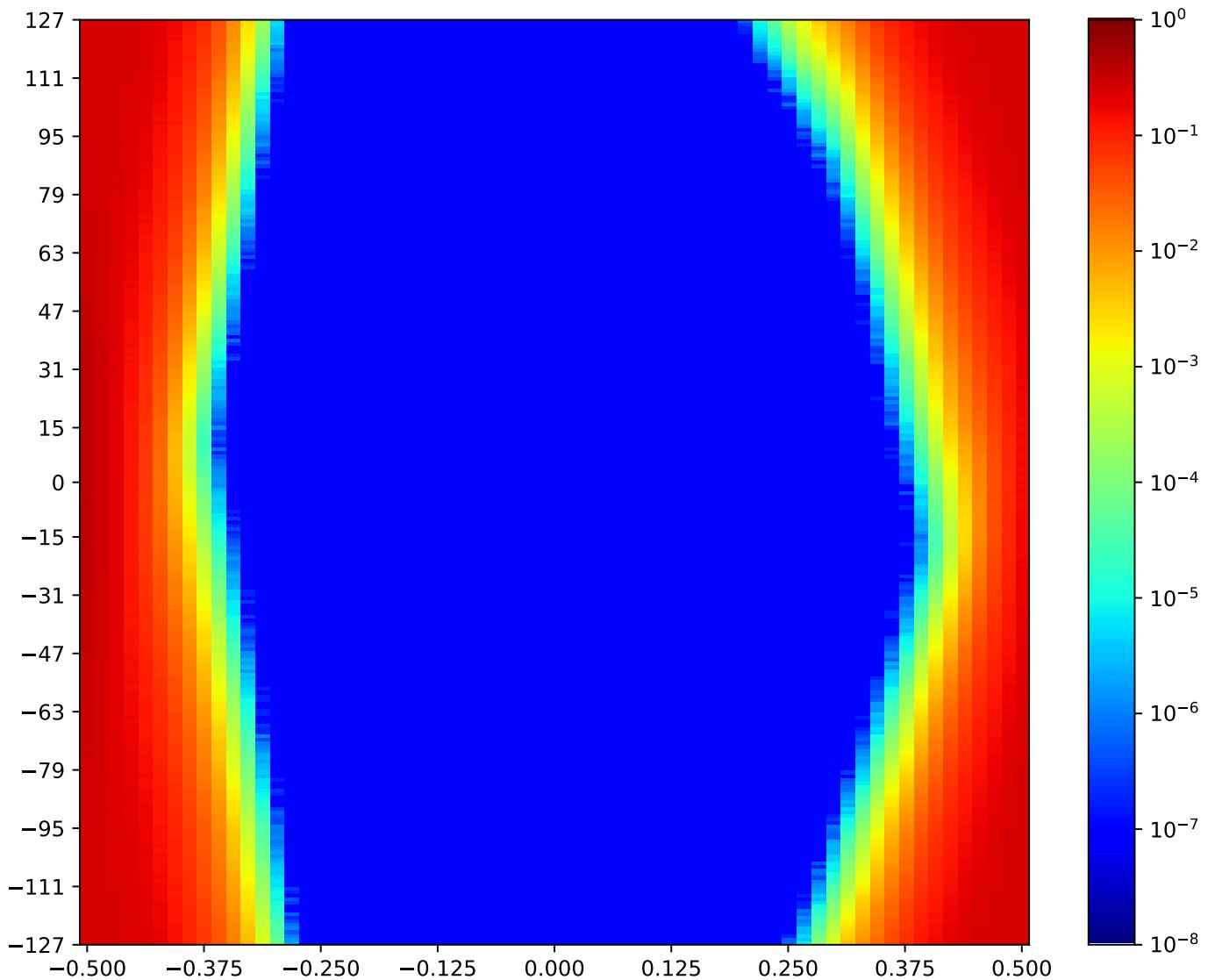


Figure 2.160: MSP\_C\_FPGA-TX3-06-RX9-06-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.12.8 MSP\_C\_FPGA-TX3-07-RX9-07-MSP\_A\_FPGA

Table 2.149: MSP\_C\_FPGA-TX3-07-RX9-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:04:29		2018-Jan-24 21:04:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9623	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

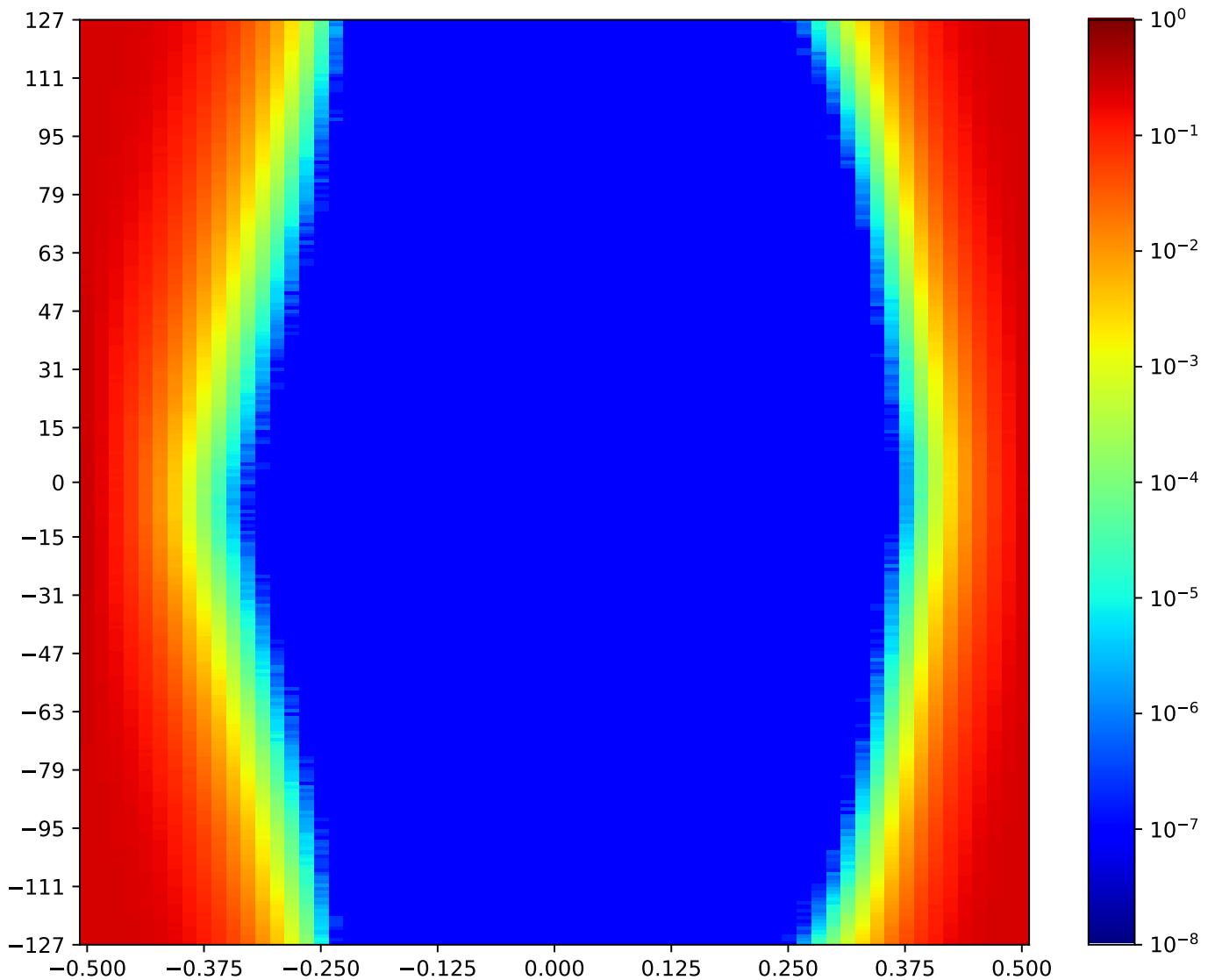


Figure 2.161: MSP\_C\_FPGA-TX3-07-RX9-07-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.12.9 MSP\_C\_FPGA-TX3-08-RX9-08-MSP\_A\_FPGA

Table 2.150: MSP\_C\_FPGA-TX3-08-RX9-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:08:31		2018-Jan-24 21:09:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10542	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

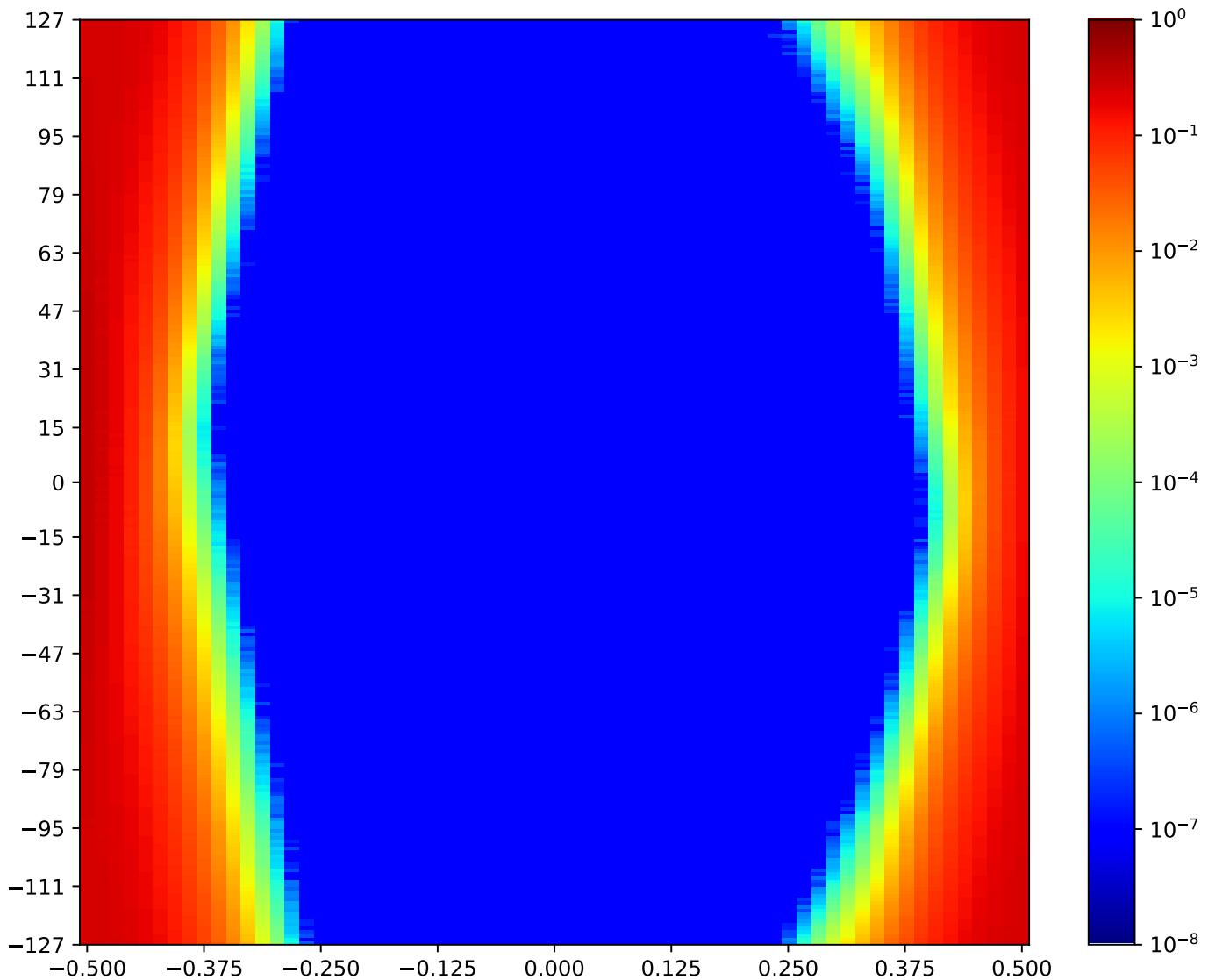


Figure 2.162: MSP\_C\_FPGA-TX3-08-RX9-08-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.12.10 MSP\_C\_FPGA-TX3-09-RX9-09-MSP\_A\_FPGA

Table 2.151: MSP\_C\_FPGA-TX3-09-RX9-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:05:29		2018-Jan-24 21:06:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10134	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

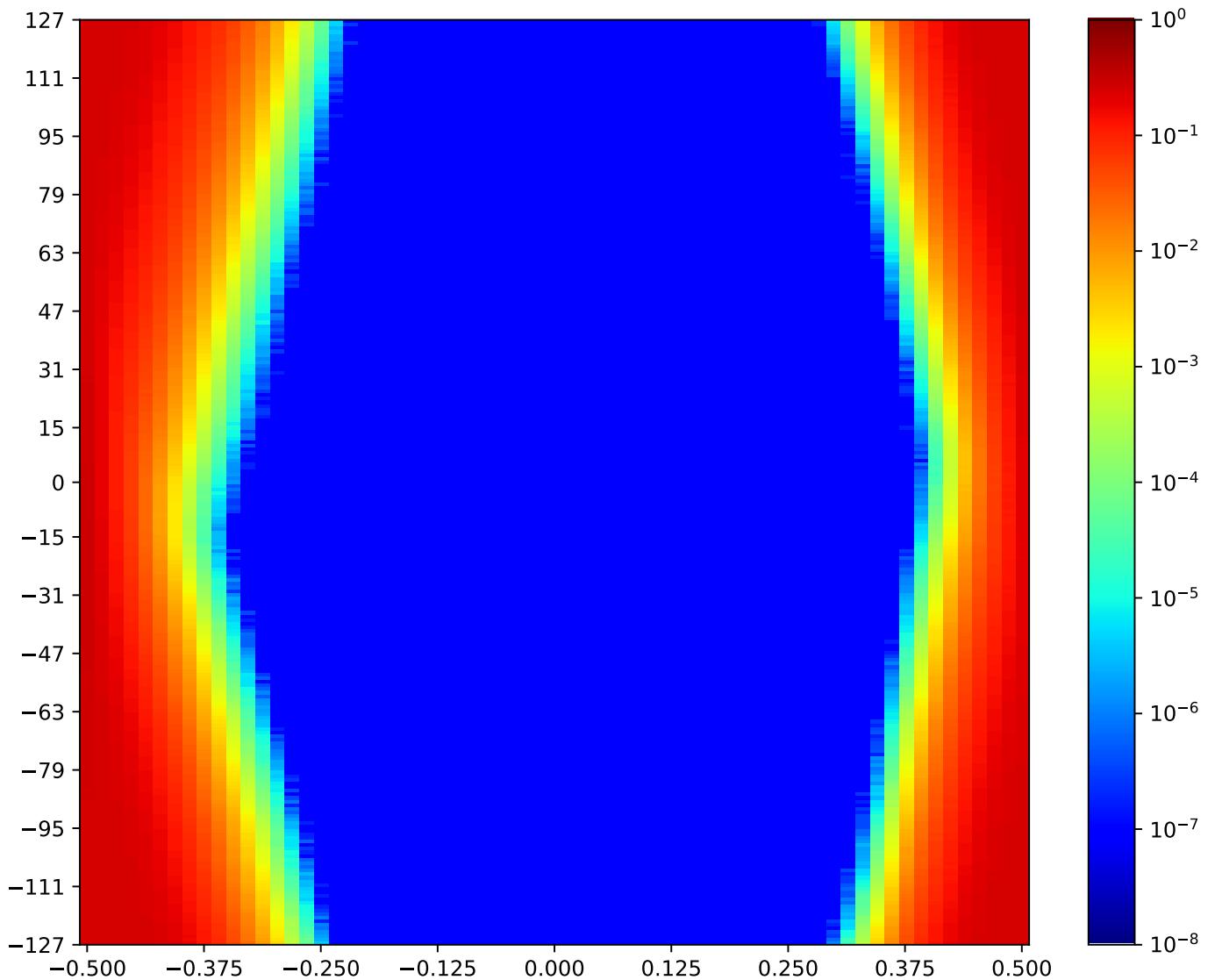


Figure 2.163: MSP\_C\_FPGA-TX3-09-RX9-09-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.12.11 MSP\_C\_FPGA-TX3-10-RX9-10-MSP\_A\_FPGA

Table 2.152: MSP\_C\_FPGA-TX3-10-RX9-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:07:33		2018-Jan-24 21:08:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9560	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
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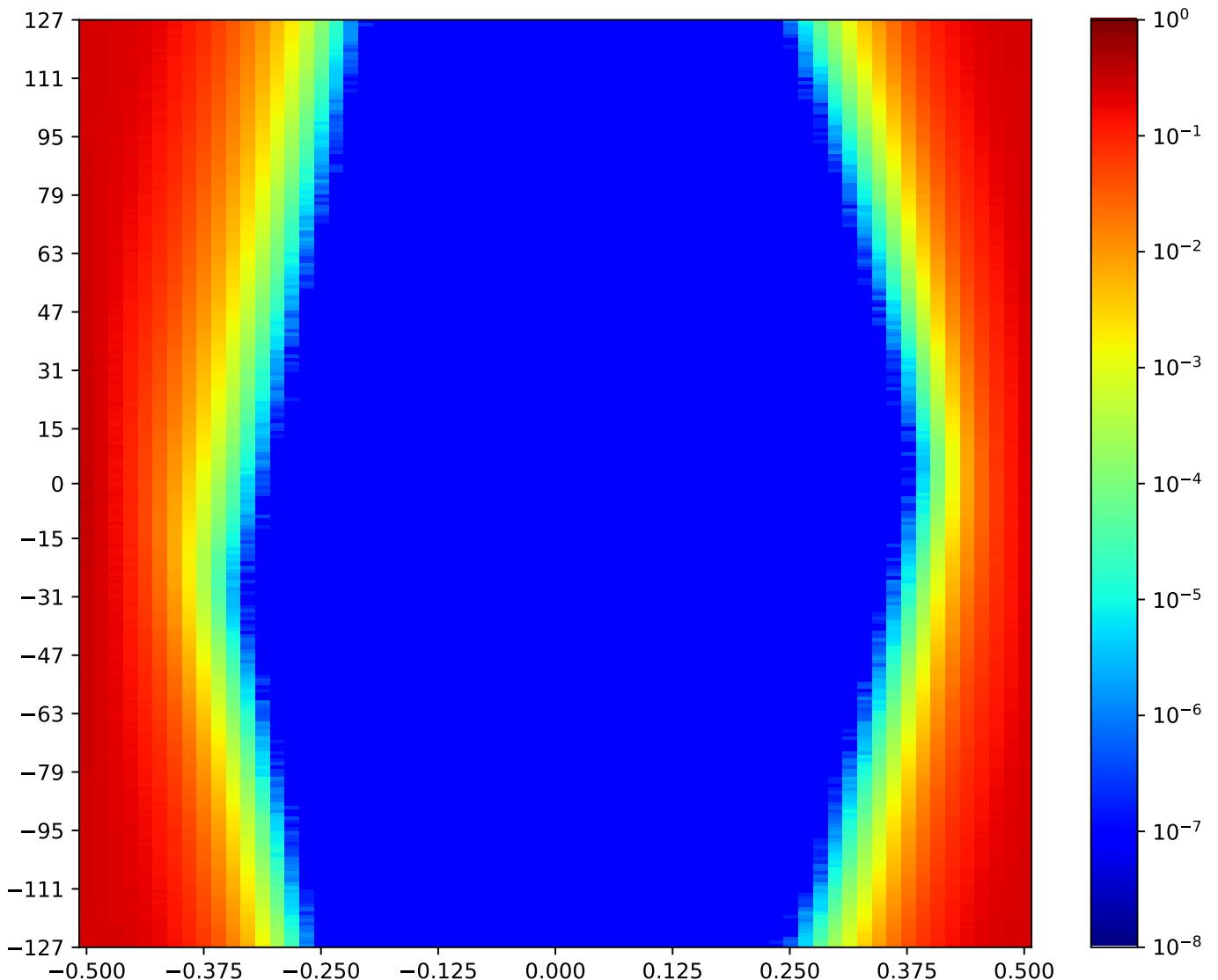


Figure 2.164: MSP\_C\_FPGA-TX3-10-RX9-10-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.12.12 MSP\_C\_FPGA-TX3-11-RX9-11-MSP\_A\_FPGA

Table 2.153: MSP\_C\_FPGA-TX3-11-RX9-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:07:03		2018-Jan-24 21:07:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10310	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

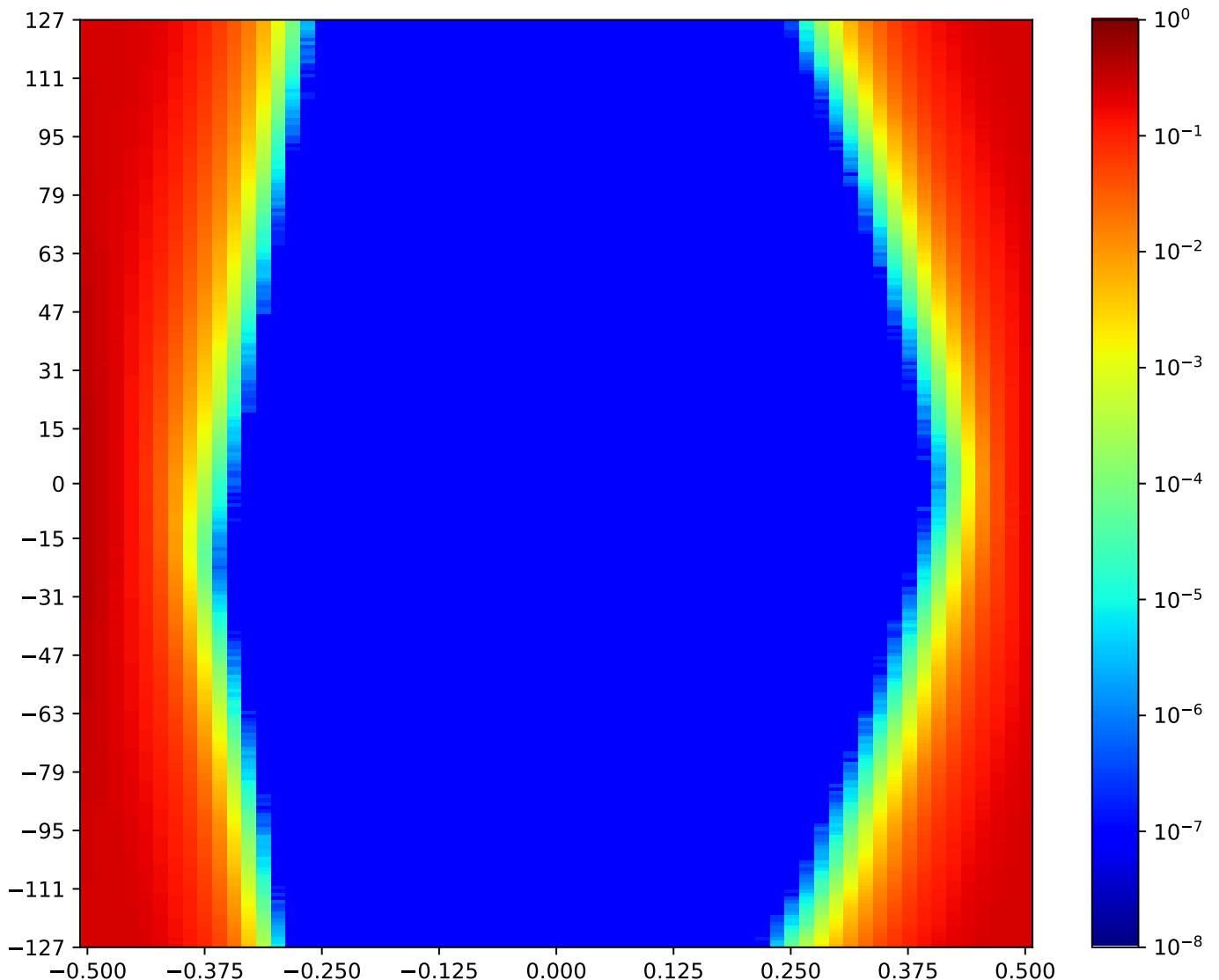


Figure 2.165: MSP\_C\_FPGA-TX3-11-RX9-11-MSP\_A\_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.13 MSP\_C TX4 MSP\_A RX8 Minipod Loopback

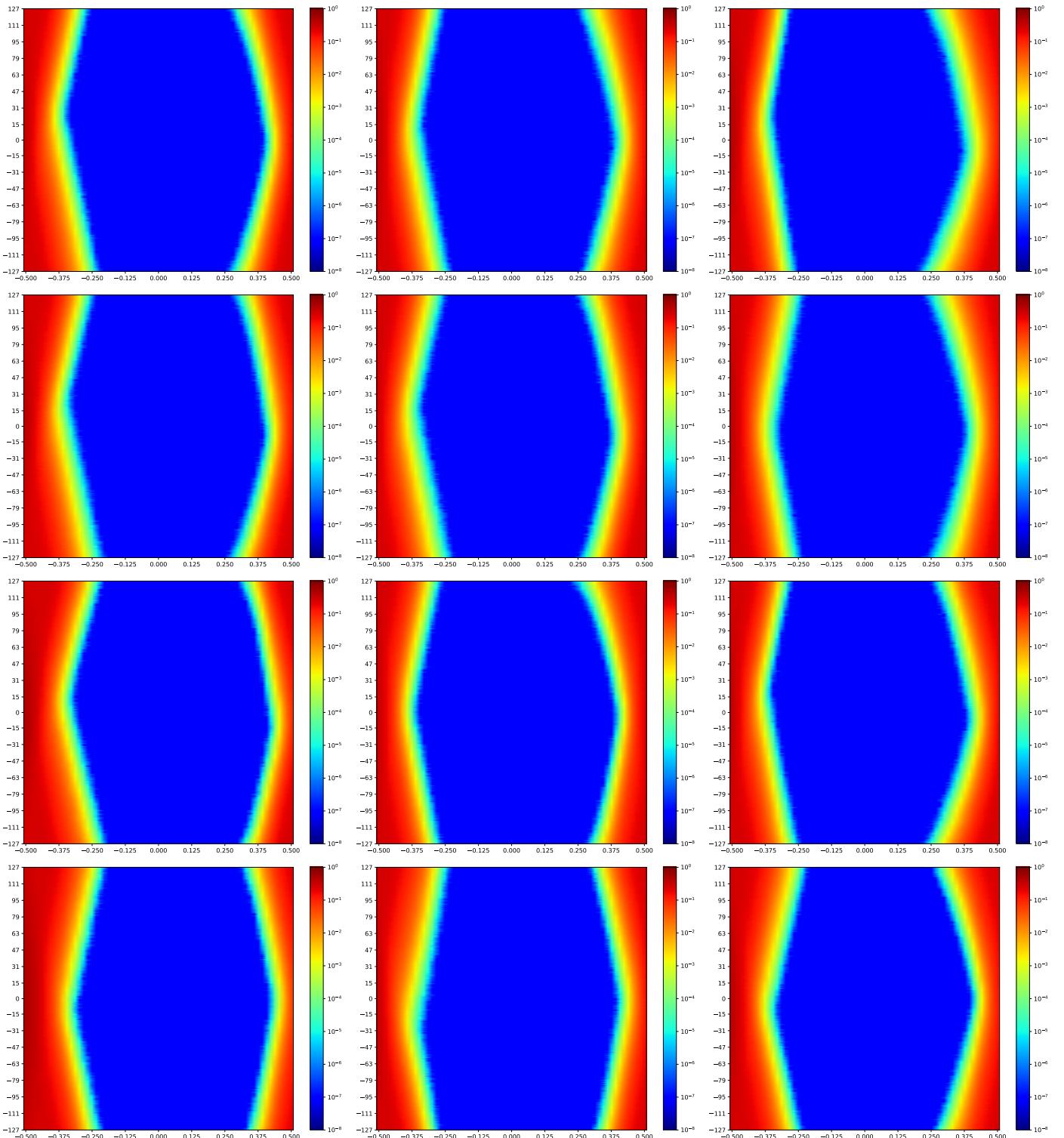


Figure 2.166: MSP\_C TX4 MSP\_A RX8 Minipod Loopback

A cross-reference to Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.179.

### 2.13.1 MSP\_C\_FPGA-TX4-00-RX8-00-MSP\_A\_FPGA

Table 2.154: MSP\_C\_FPGA-TX4-00-RX8-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:11:07		2018-Jan-24 21:11:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10027	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

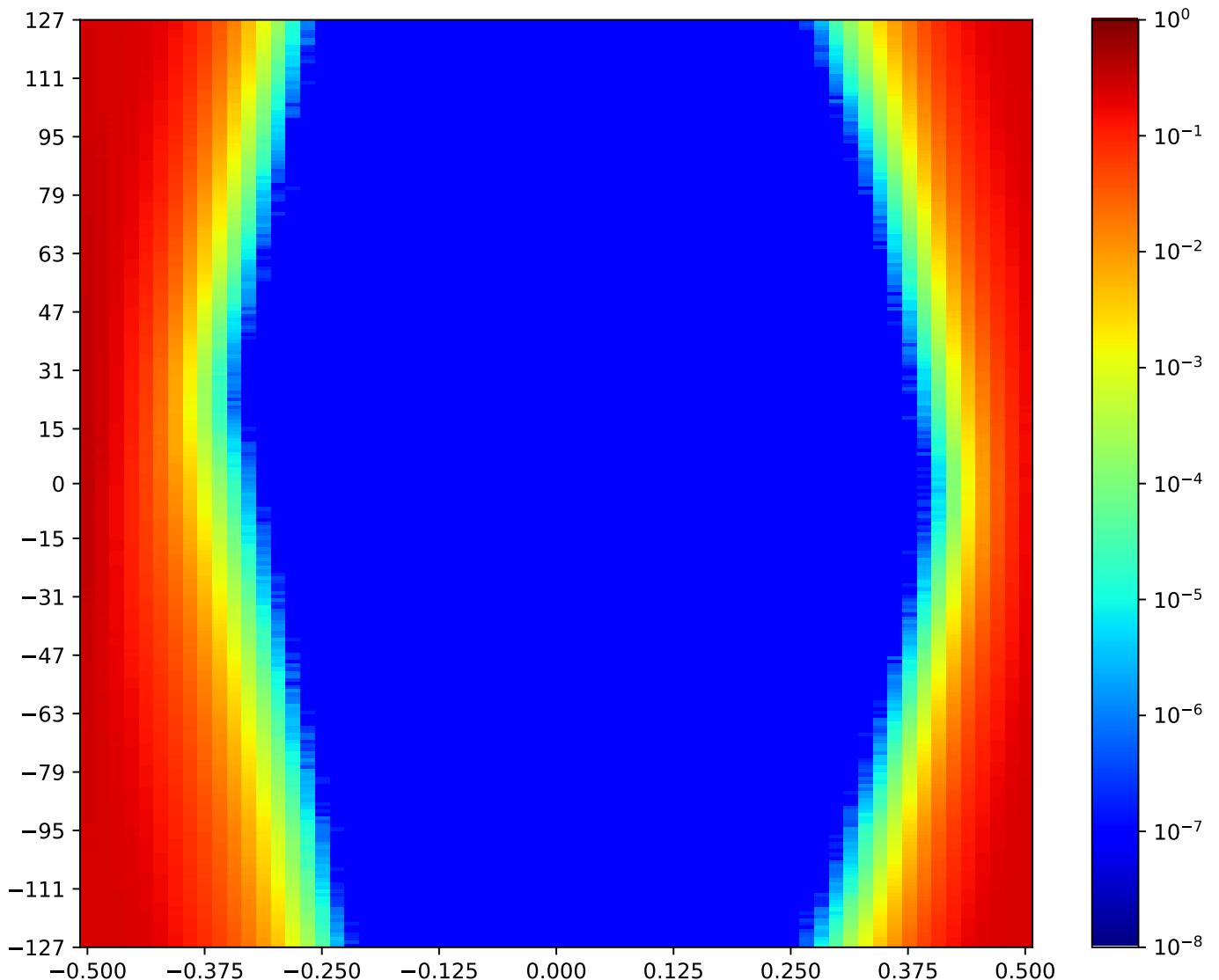


Figure 2.167: MSP\_C\_FPGA-TX4-00-RX8-00-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.13.2 MSP\_C\_FPGA-TX4-01-RX8-01-MSP\_A\_FPGA

Table 2.155: MSP\_C\_FPGA-TX4-01-RX8-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:10:04		2018-Jan-24 21:10:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9609	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

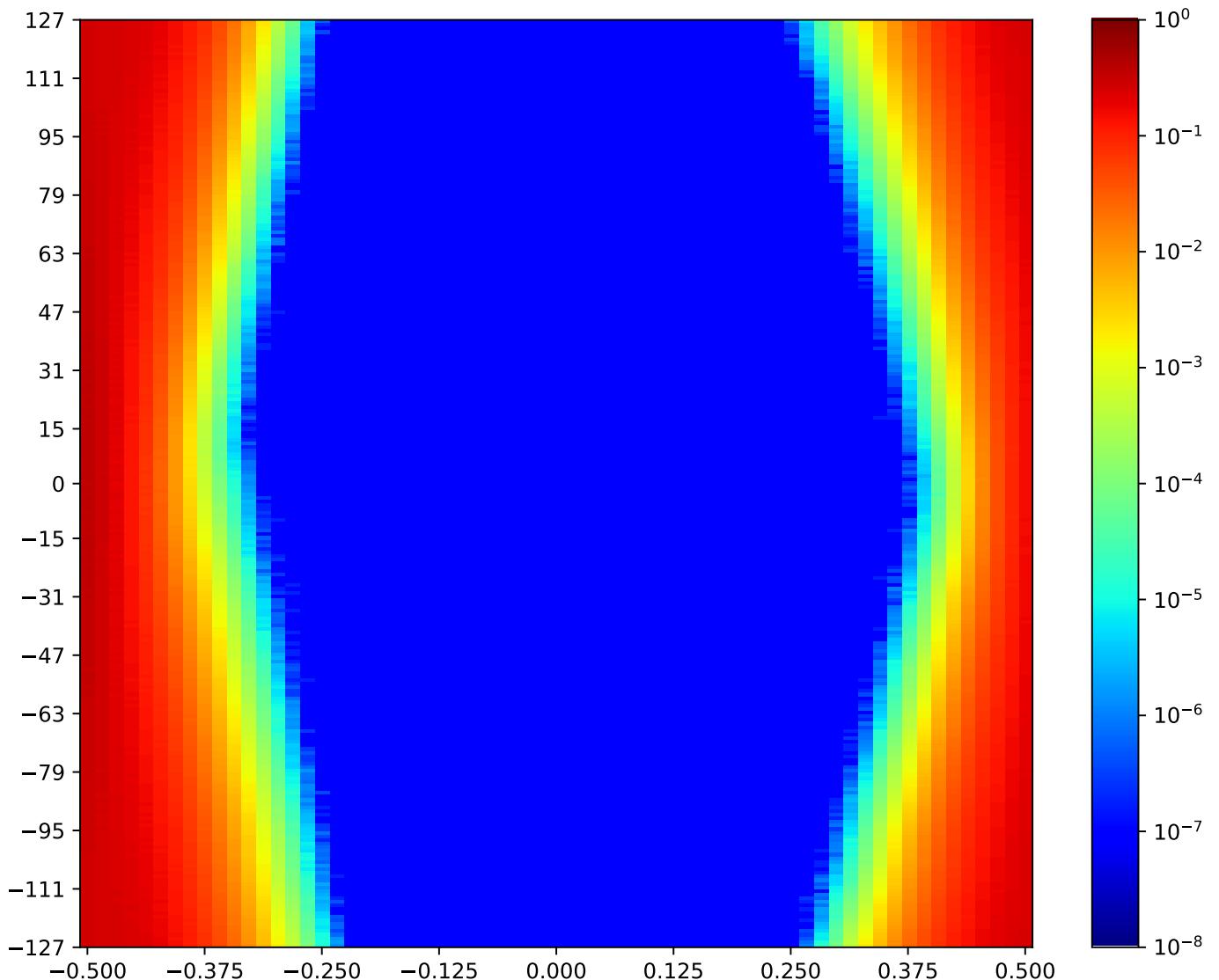


Figure 2.168: MSP\_C\_FPGA-TX4-01-RX8-01-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.13.3 MSP\_C\_FPGA-TX4-02-RX8-02-MSP\_A\_FPGA

Table 2.156: MSP\_C\_FPGA-TX4-02-RX8-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:12:37		2018-Jan-24 21:13:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9520	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

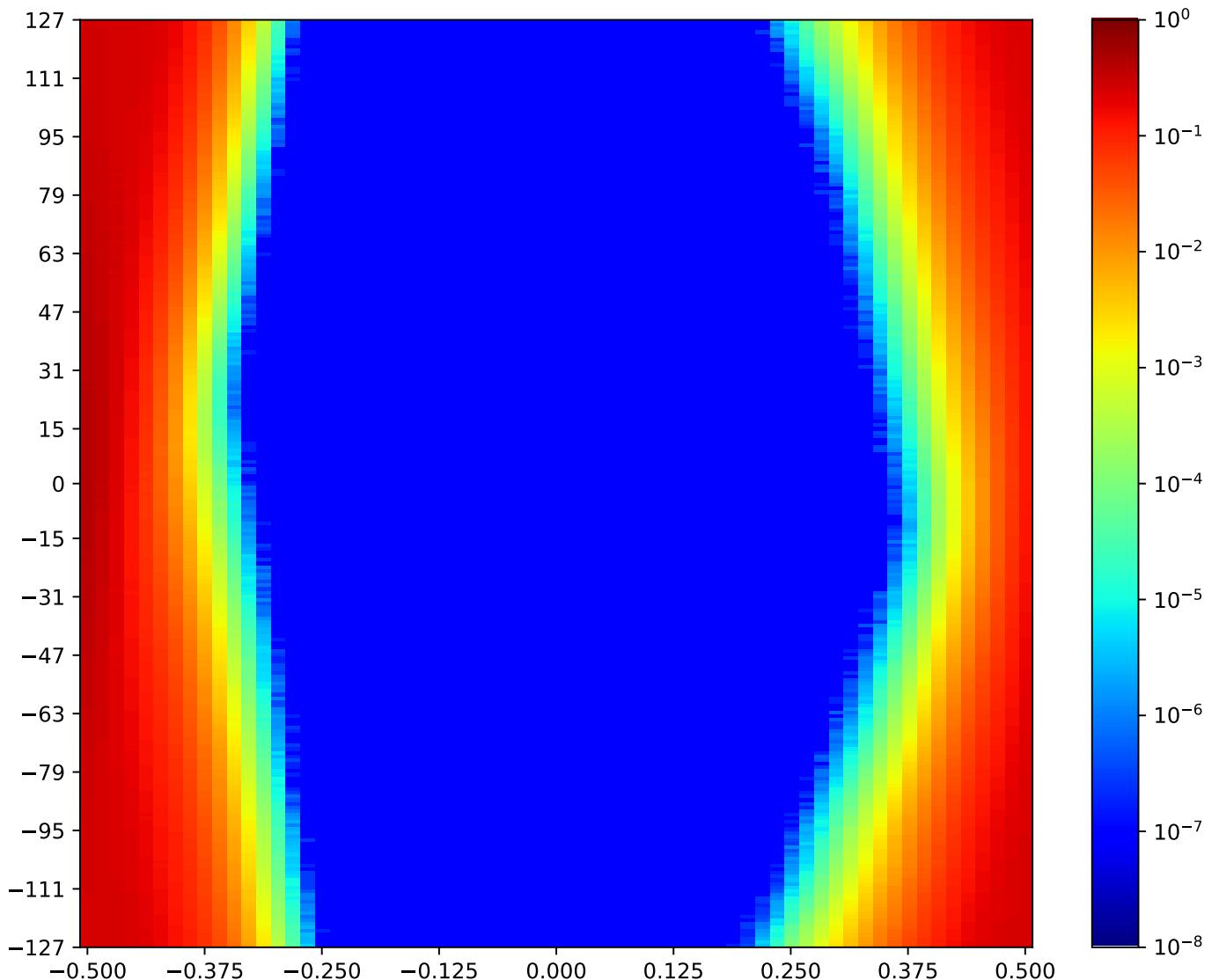


Figure 2.169: MSP\_C\_FPGA-TX4-02-RX8-02-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

#### 2.13.4 MSP\_C\_FPGA-TX4-03-RX8-03-MSP\_A\_FPGA

Table 2.157: MSP\_C\_FPGA-TX4-03-RX8-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:09:31		2018-Jan-24 21:10:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9772	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

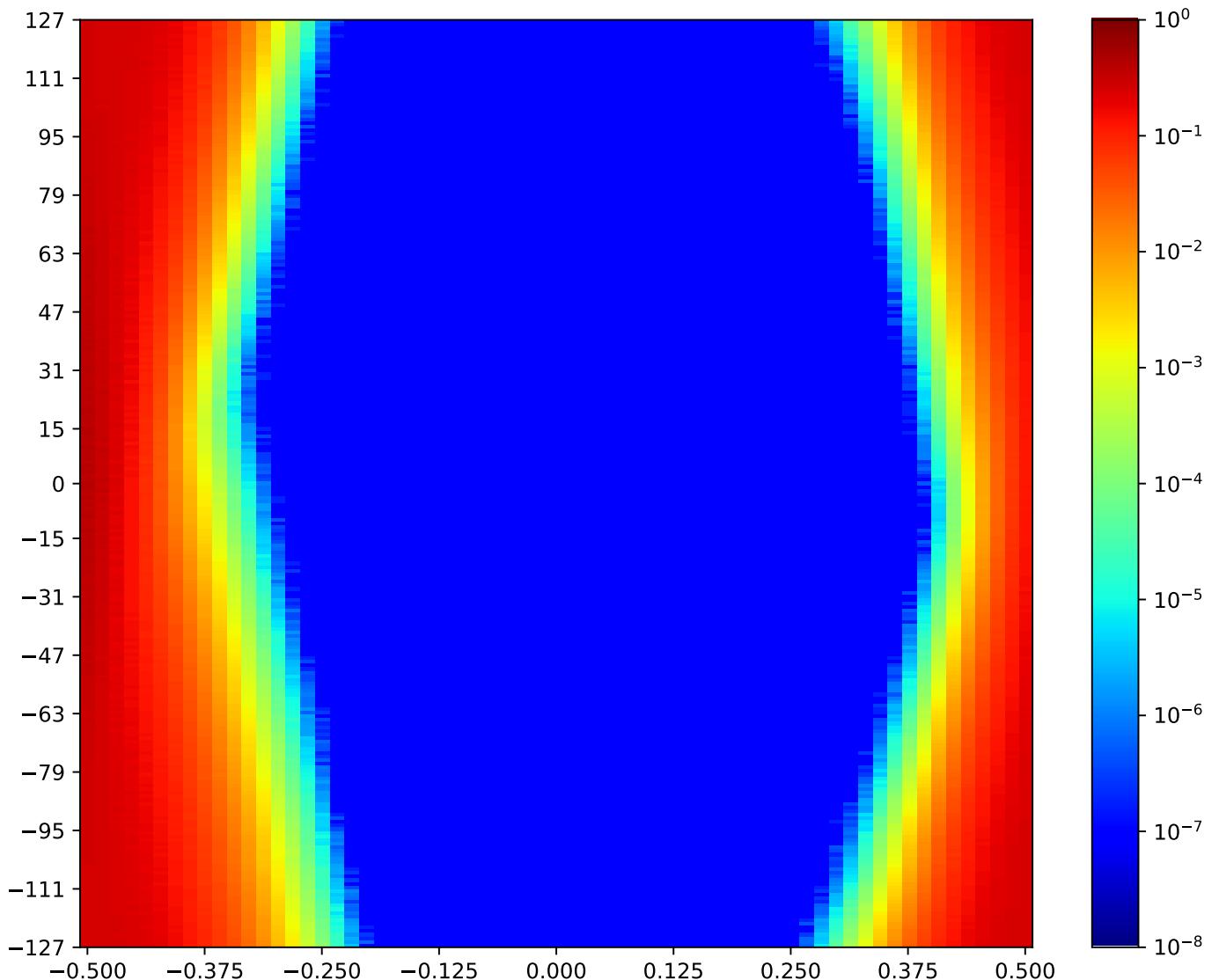


Figure 2.170: MSP\_C\_FPGA-TX4-03-RX8-03-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.13.5 MSP\_C\_FPGA-TX4-04-RX8-04-MSP\_A\_FPGA

Table 2.158: MSP\_C\_FPGA-TX4-04-RX8-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:14:08		2018-Jan-24 21:14:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9517	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

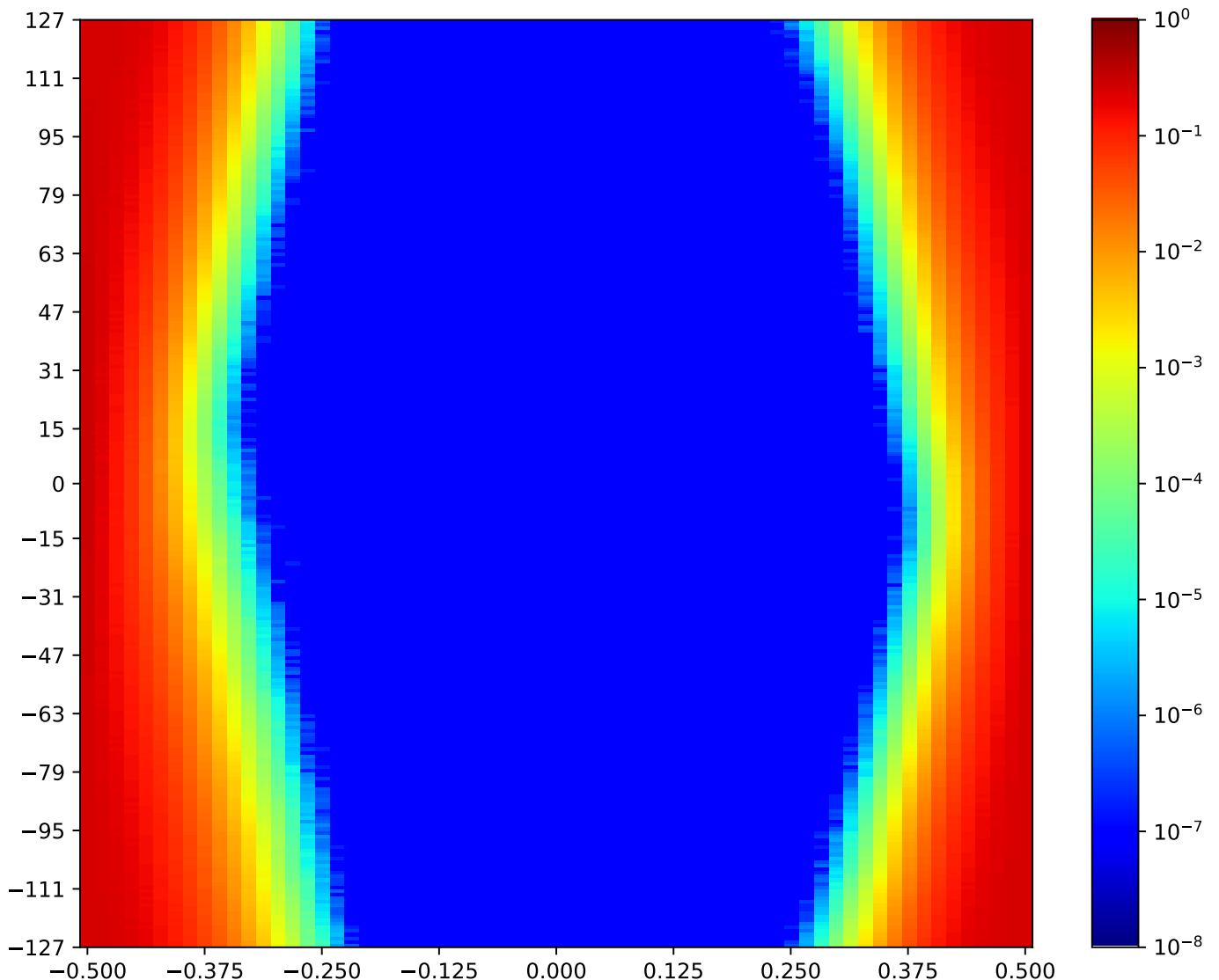


Figure 2.171: MSP\_C\_FPGA-TX4-04-RX8-04-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.13.6 MSP\_C\_FPGA-TX4-05-RX8-05-MSP\_A\_FPGA

Table 2.159: MSP\_C\_FPGA-TX4-05-RX8-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:10:37		2018-Jan-24 21:11:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9274	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

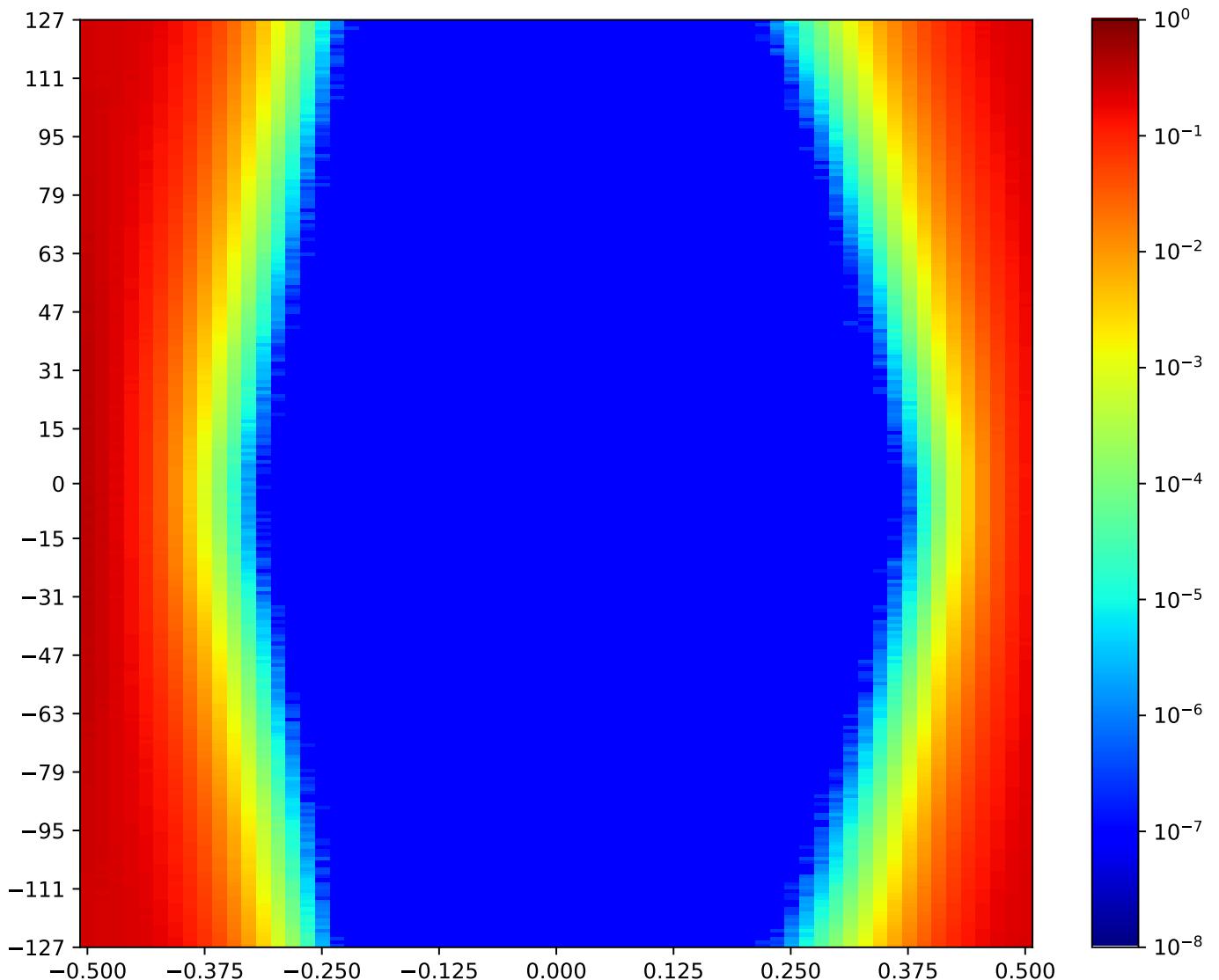


Figure 2.172: MSP\_C\_FPGA-TX4-05-RX8-05-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.13.7 MSP\_C\_FPGA-TX4-06-RX8-06-MSP\_A\_FPGA

Table 2.160: MSP\_C\_FPGA-TX4-06-RX8-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:15:07		2018-Jan-24 21:15:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10067	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

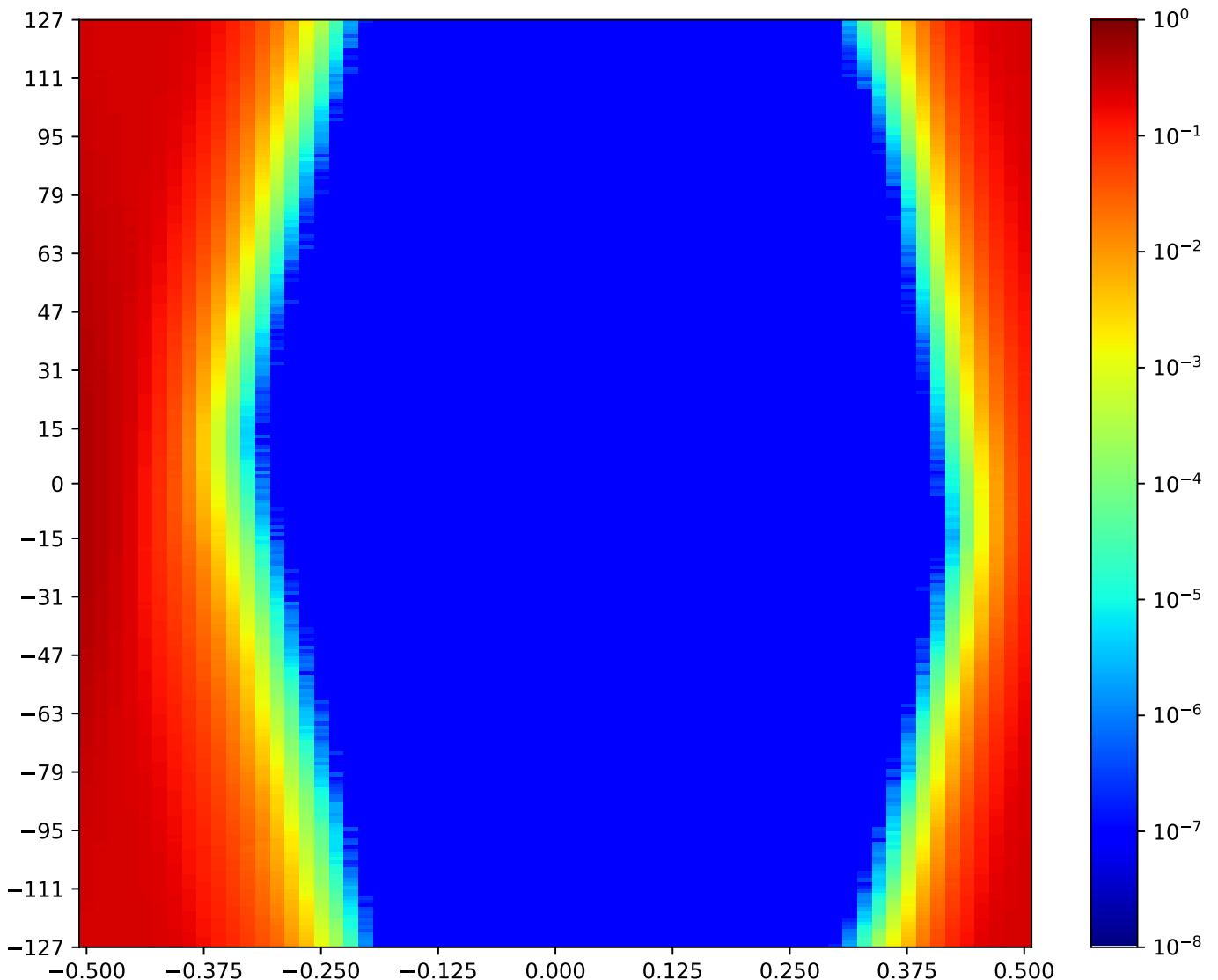


Figure 2.173: MSP\_C\_FPGA-TX4-06-RX8-06-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.13.8 MSP\_C\_FPGA-TX4-07-RX8-07-MSP\_A\_FPGA

Table 2.161: MSP\_C\_FPGA-TX4-07-RX8-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:11:37		2018-Jan-24 21:12:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10263	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

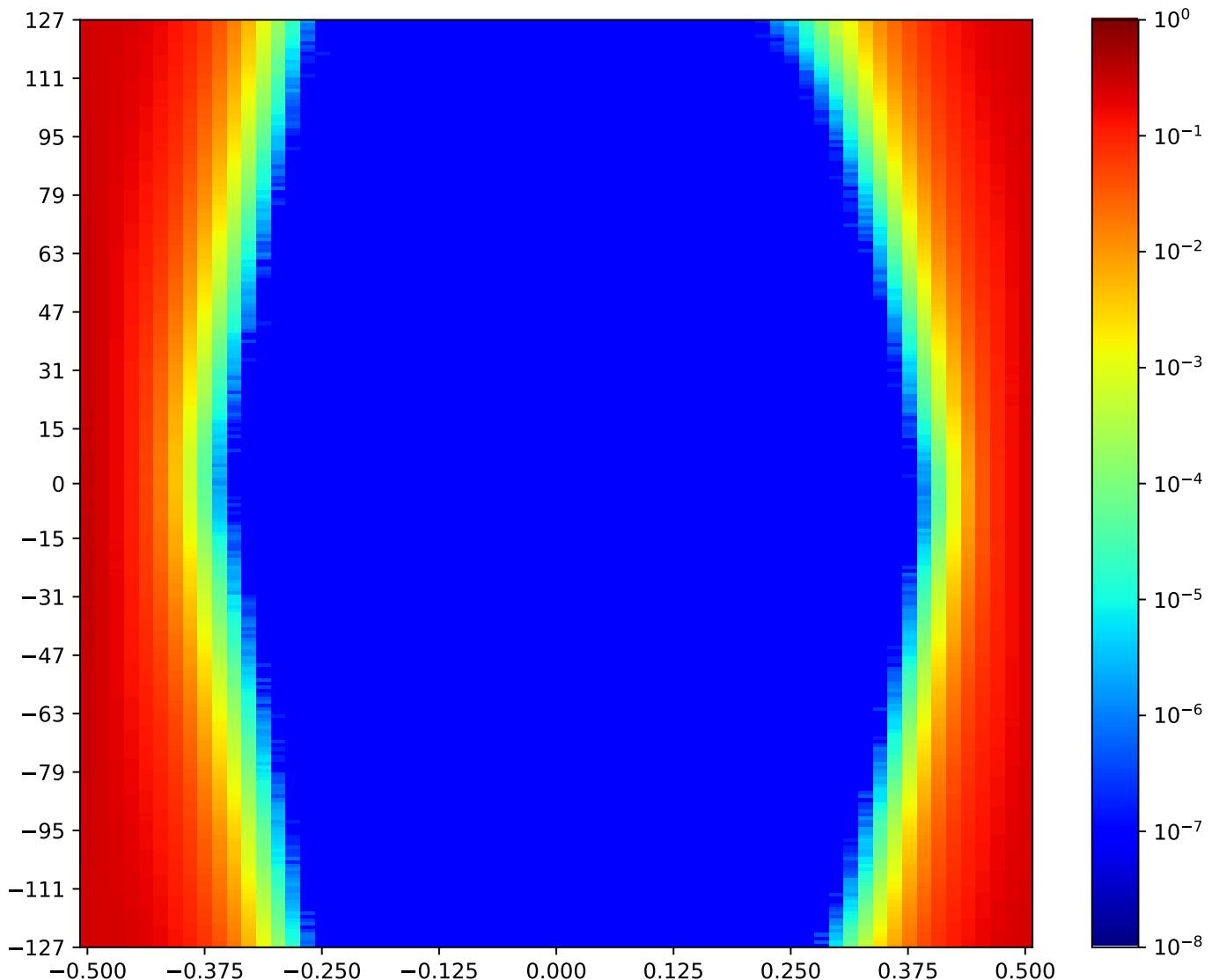


Figure 2.174: MSP\_C\_FPGA-TX4-07-RX8-07-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.13.9 MSP\_C\_FPGA-TX4-08-RX8-08-MSP\_A\_FPGA

Table 2.162: MSP\_C\_FPGA-TX4-08-RX8-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:14:37		2018-Jan-24 21:15:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9930	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

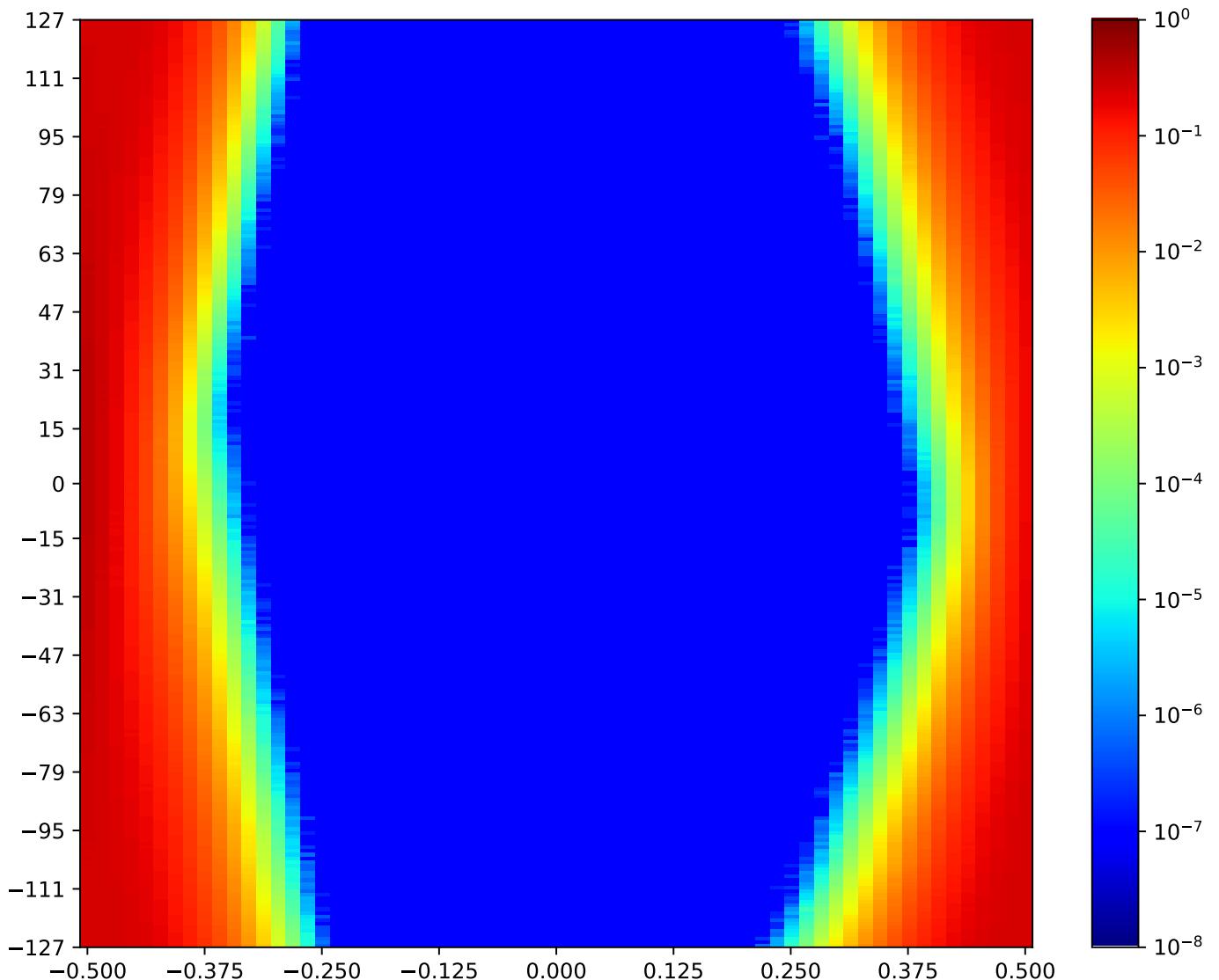


Figure 2.175: MSP\_C\_FPGA-TX4-08-RX8-08-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.13.10 MSP\_C\_FPGA-TX4-09-RX8-09-MSP\_A\_FPGA

Table 2.163: MSP\_C\_FPGA-TX4-09-RX8-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:12:07		2018-Jan-24 21:12:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10006	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

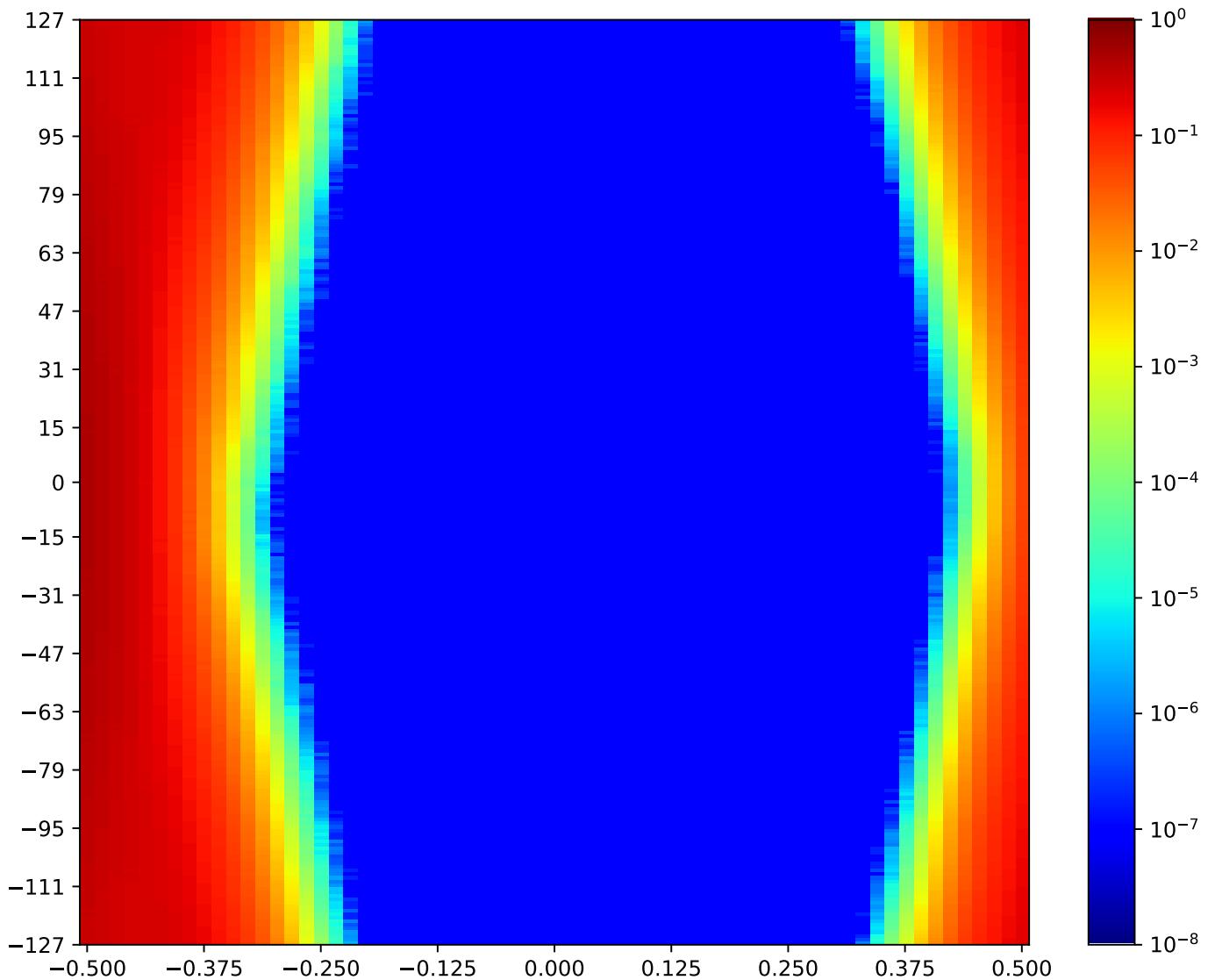


Figure 2.176: MSP\_C\_FPGA-TX4-09-RX8-09-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.13.11 MSP\_C\_FPGA-TX4-10-RX8-10-MSP\_A\_FPGA

Table 2.164: MSP\_C\_FPGA-TX4-10-RX8-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:13:38		2018-Jan-24 21:14:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10162	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

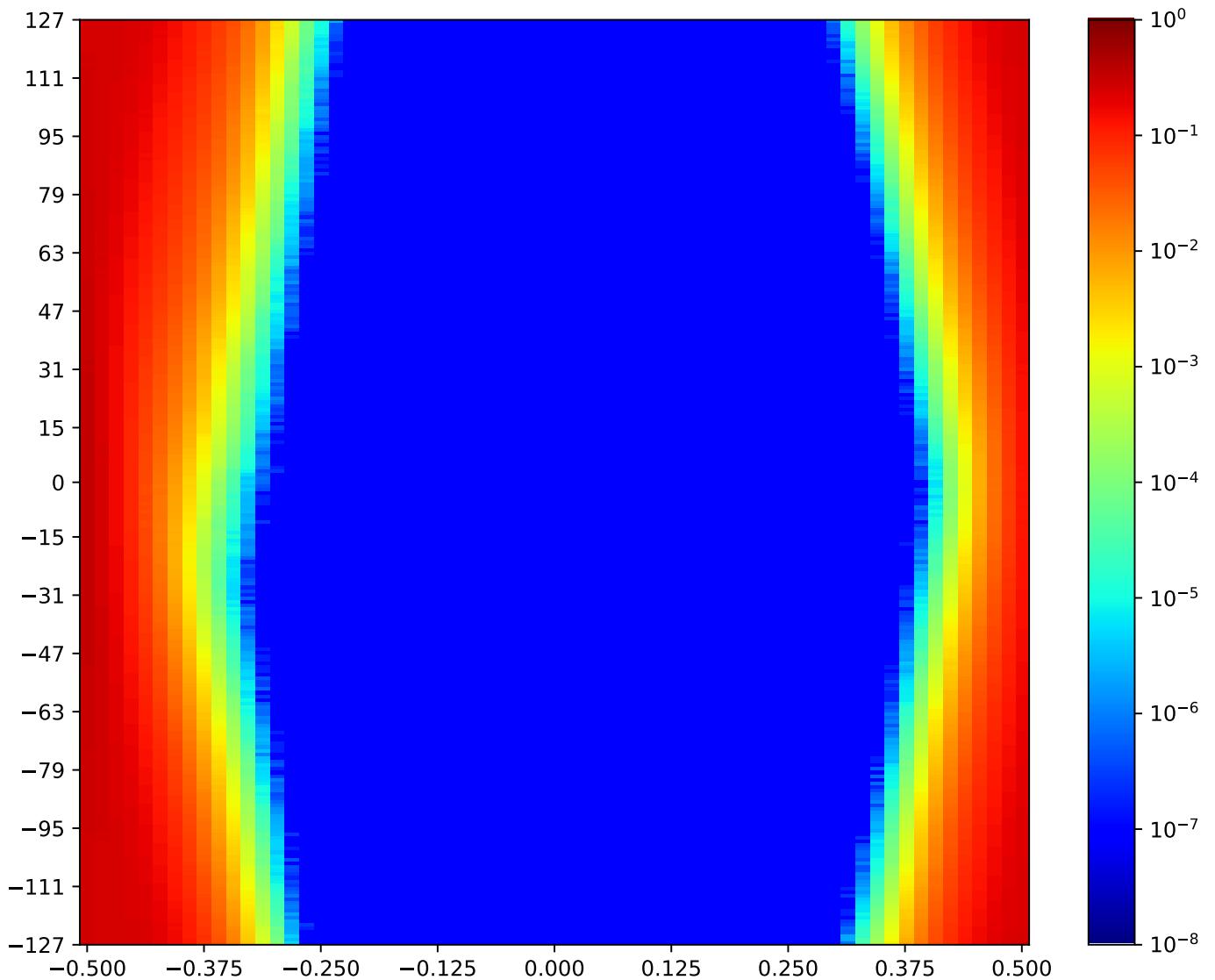


Figure 2.177: MSP\_C\_FPGA-TX4-10-RX8-10-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.13.12 MSP\_C\_FPGA-TX4-11-RX8-11-MSP\_A\_FPGA

Table 2.165: MSP\_C\_FPGA-TX4-11-RX8-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:13:06		2018-Jan-24 21:13:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9761	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

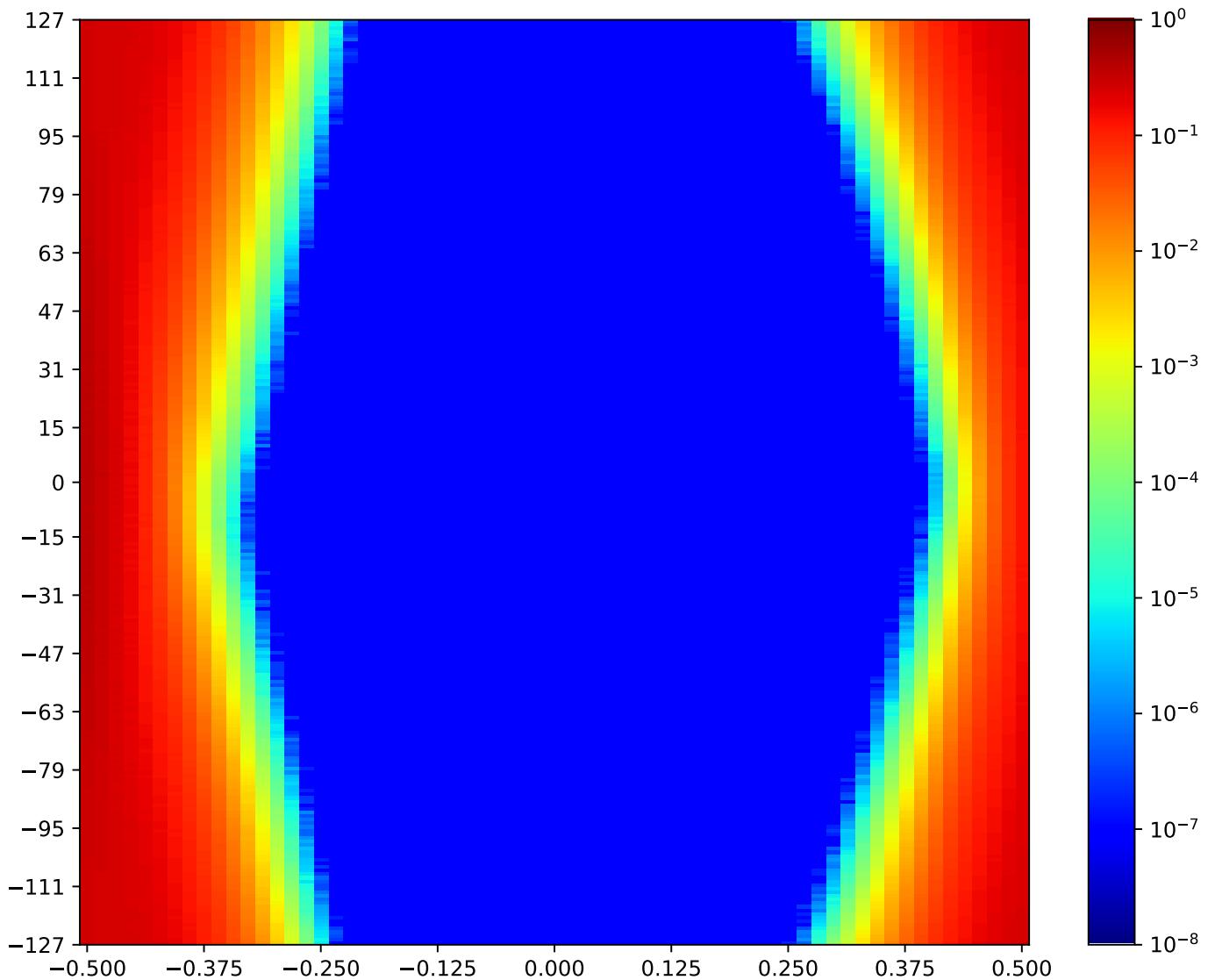


Figure 2.178: MSP\_C\_FPGA-TX4-11-RX8-11-MSP\_A\_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.14 Partial TRP TX5 MSP\_C RX14 Minipod Loopback

A cross-reference to Figure 2.179. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.188.

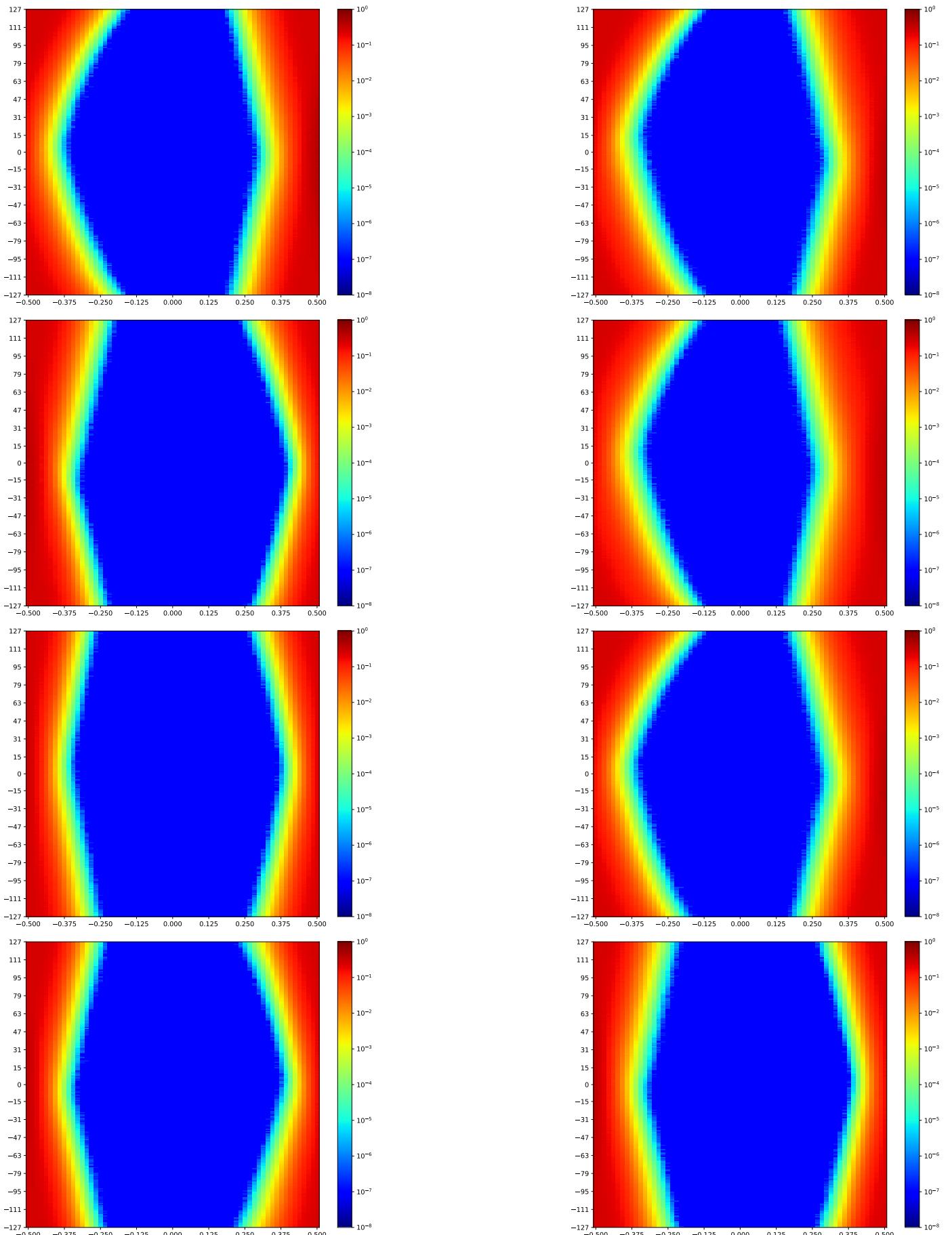


Figure 2.179: Partial TRP TX5 MSP\_C RX14 Minipod Loopback

### 2.14.1 TRP\_FPGA-TX5-00-RX14-00-MSP\_C\_FPGA

Table 2.166: TRP\_FPGA-TX5-00-RX14-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:17:07		2018-Jan-24 21:17:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8096	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

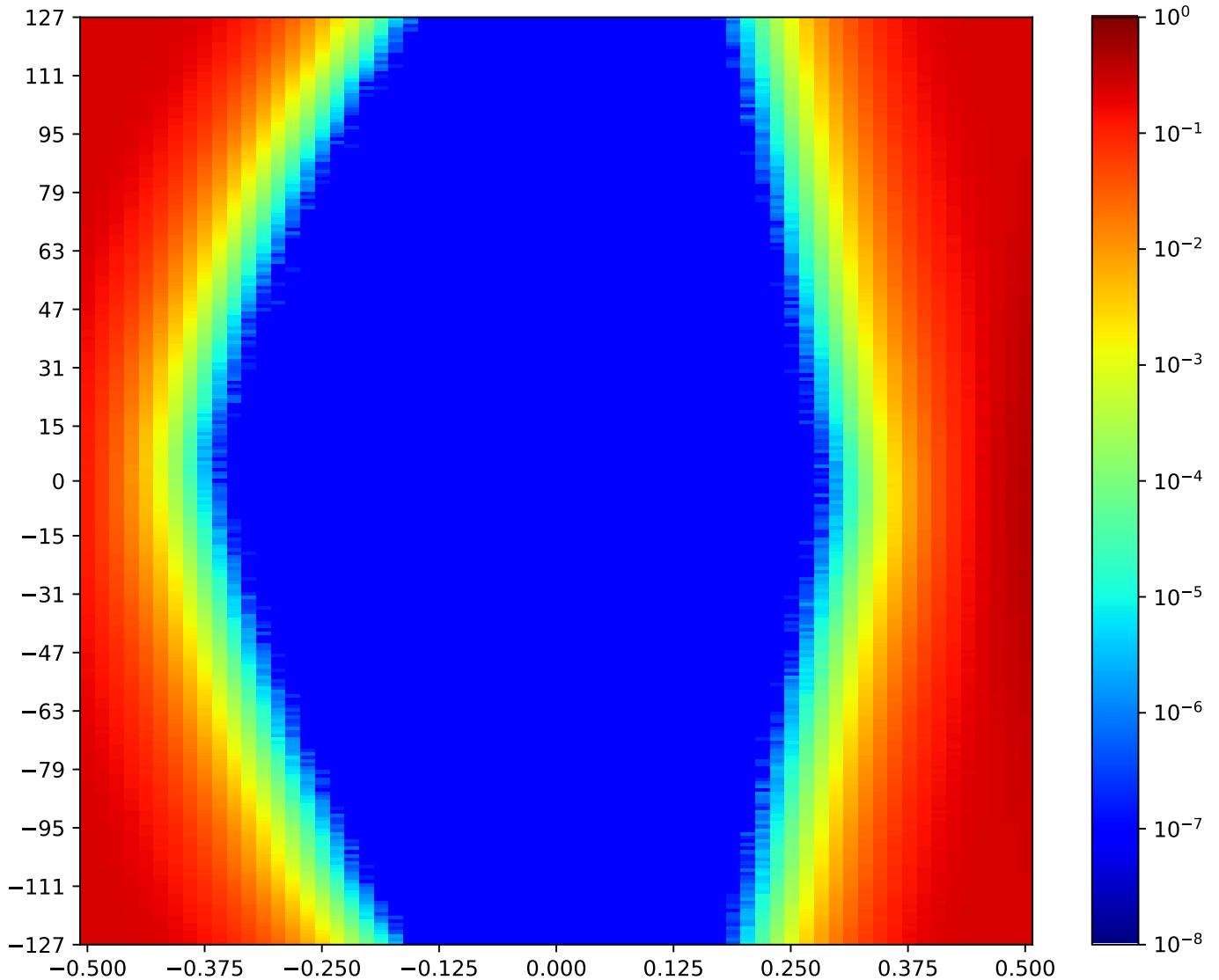


Figure 2.180: TRP\_FPGA-TX5-00-RX14-00-MSP\_C\_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.14.2 TRP\_FPGA-TX5-01-RX14-01-MSP\_C\_FPGA

Table 2.167: TRP\_FPGA-TX5-01-RX14-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:16:07		2018-Jan-24 21:16:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7246	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

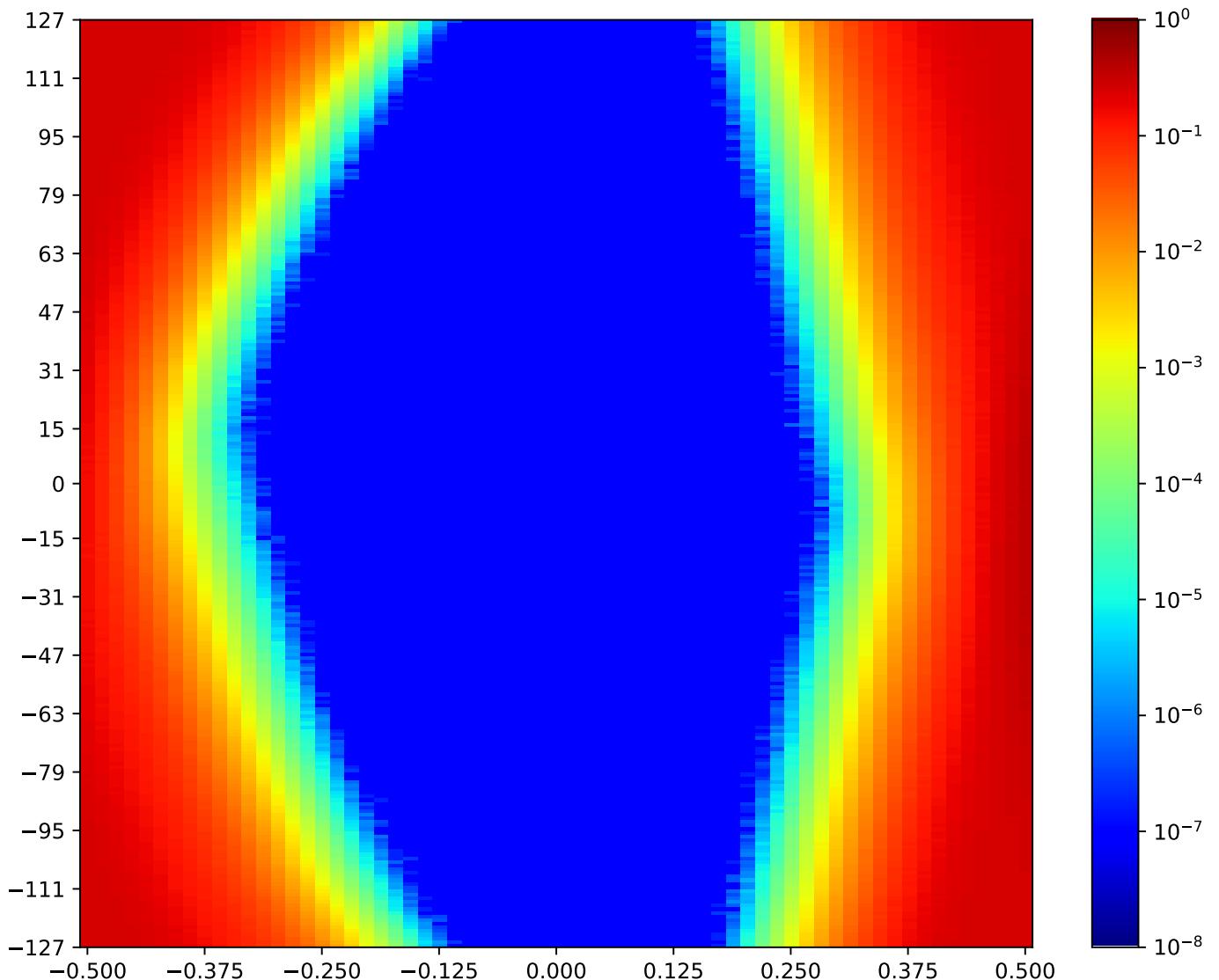


Figure 2.181: TRP\_FPGA-TX5-01-RX14-01-MSP\_C\_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.14.3 TRP\_FPGA-TX5-02-RX14-02-MSP\_C\_FPGA

Table 2.168: TRP\_FPGA-TX5-02-RX14-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:18:09		2018-Jan-24 21:18:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9361	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

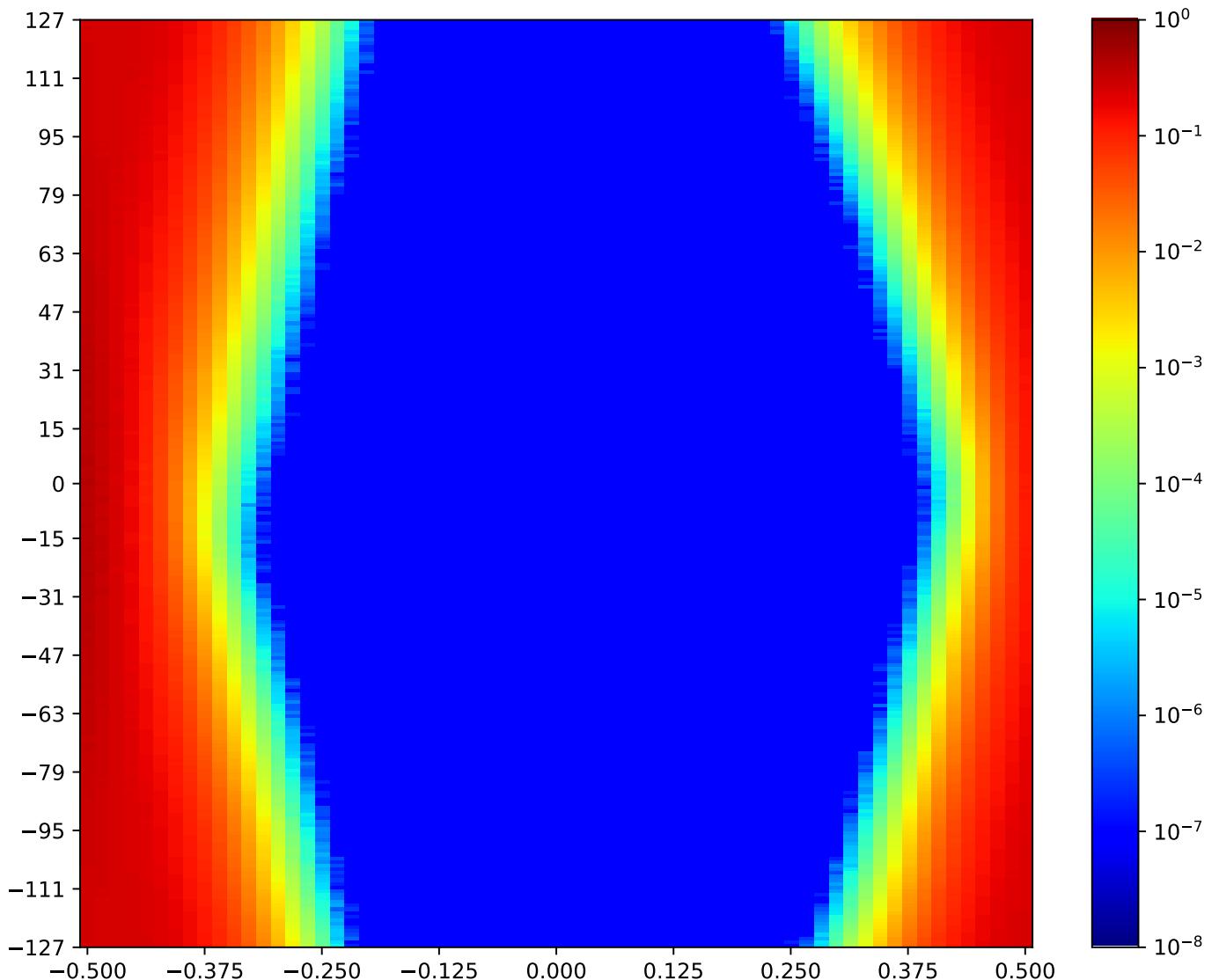


Figure 2.182: TRP\_FPGA-TX5-02-RX14-02-MSP\_C\_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

#### 2.14.4 TRP\_FPGA-TX5-03-RX14-03-MSP\_C\_FPGA

Table 2.169: TRP\_FPGA-TX5-03-RX14-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:16:37		2018-Jan-24 21:17:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6722	34	52.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

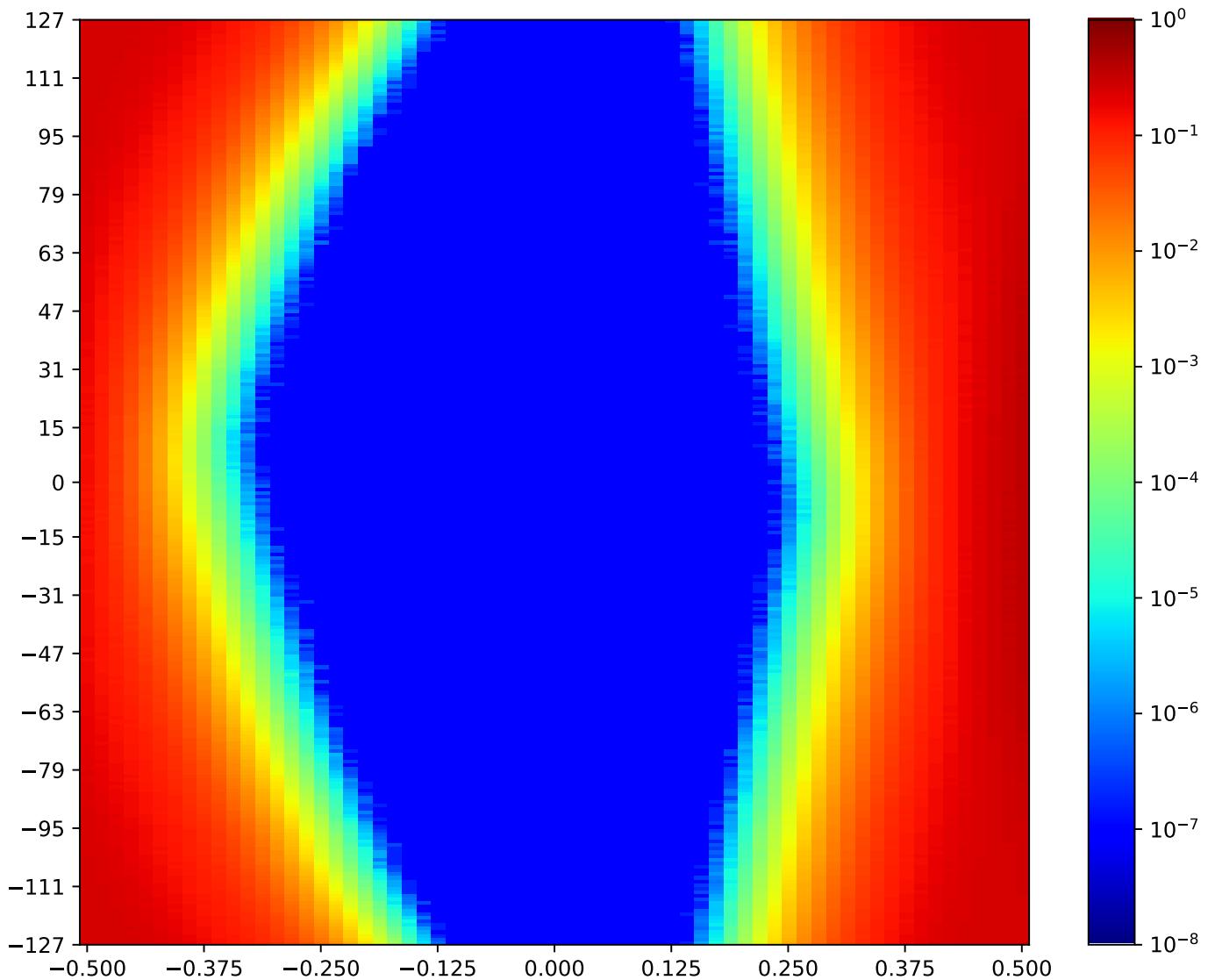


Figure 2.183: TRP\_FPGA-TX5-03-RX14-03-MSP\_C\_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.14.5 TRP\_FPGA-TX5-04-RX14-04-MSP\_C\_FPGA

Table 2.170: TRP\_FPGA-TX5-04-RX14-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:19:09		2018-Jan-24 21:19:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9767	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

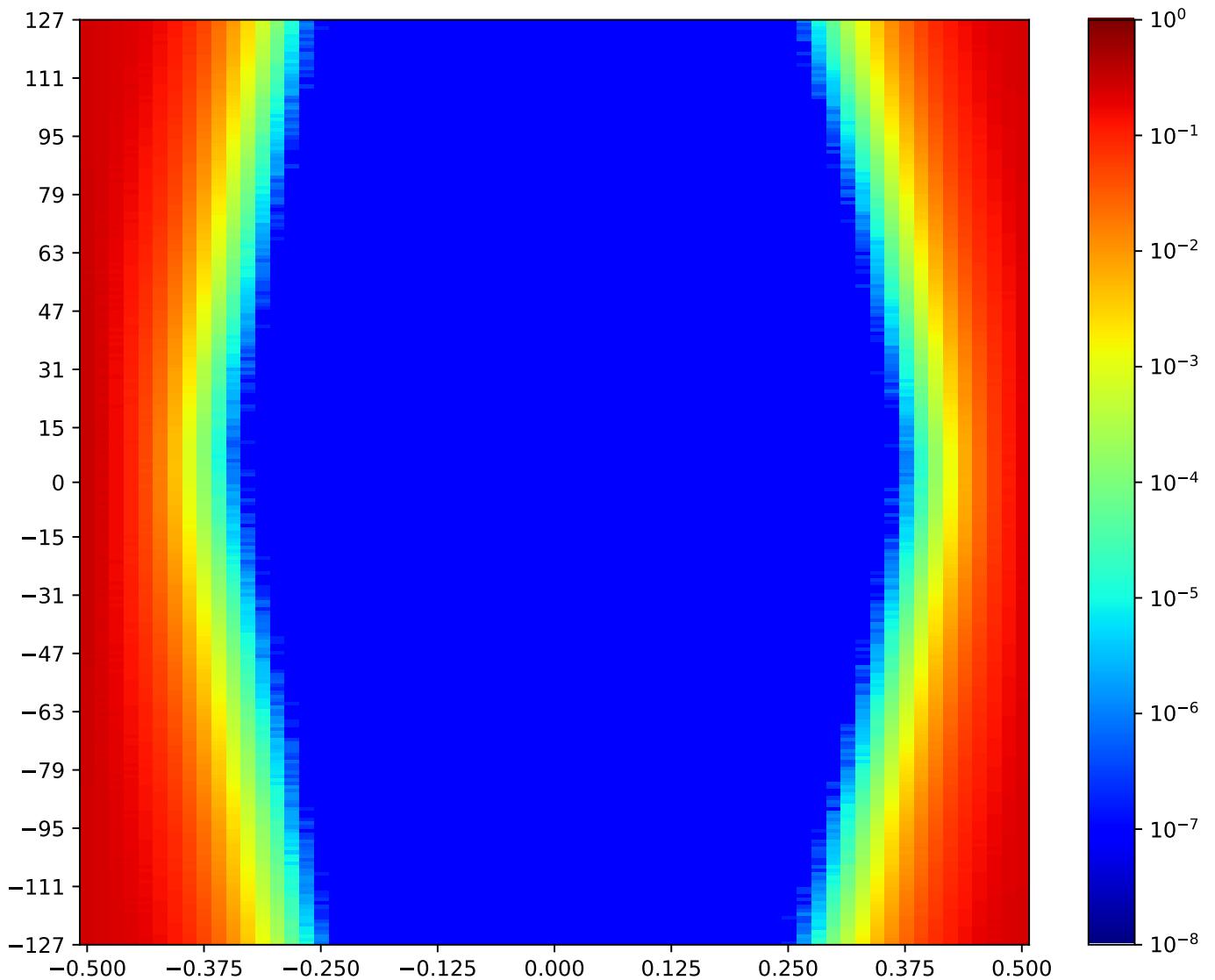


Figure 2.184: TRP\_FPGA-TX5-04-RX14-04-MSP\_C\_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.14.6 TRP\_FPGA-TX5-05-RX14-05-MSP\_C\_FPGA

Table 2.171: TRP\_FPGA-TX5-05-RX14-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:15:37		2018-Jan-24 21:16:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7573	39	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

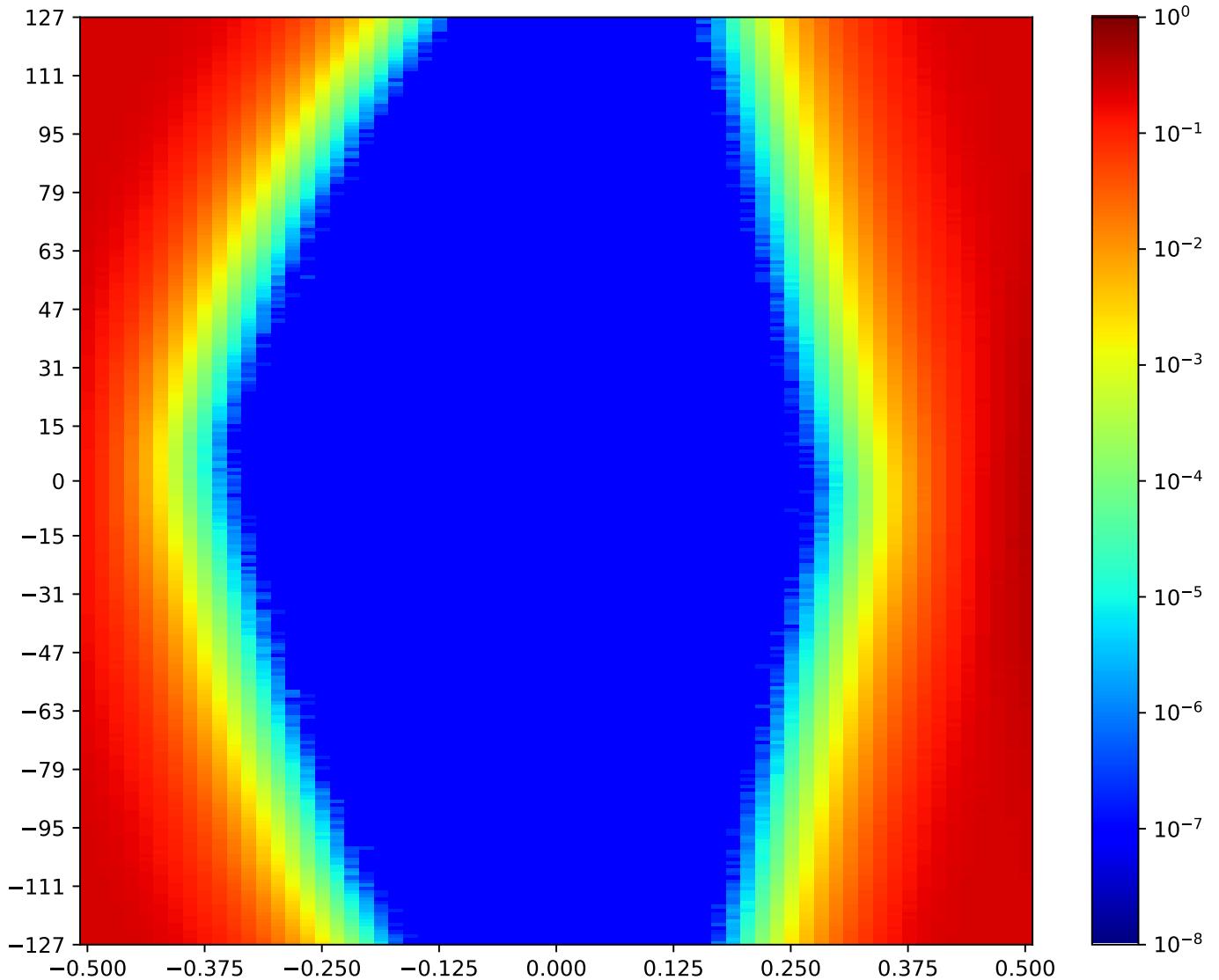


Figure 2.185: TRP\_FPGA-TX5-05-RX14-05-MSP\_C\_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.14.7 TRP\_FPGA-TX5-06-RX14-06-MSP\_C\_FPGA

Table 2.172: TRP\_FPGA-TX5-06-RX14-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:17:37		2018-Jan-24 21:18:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9332	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

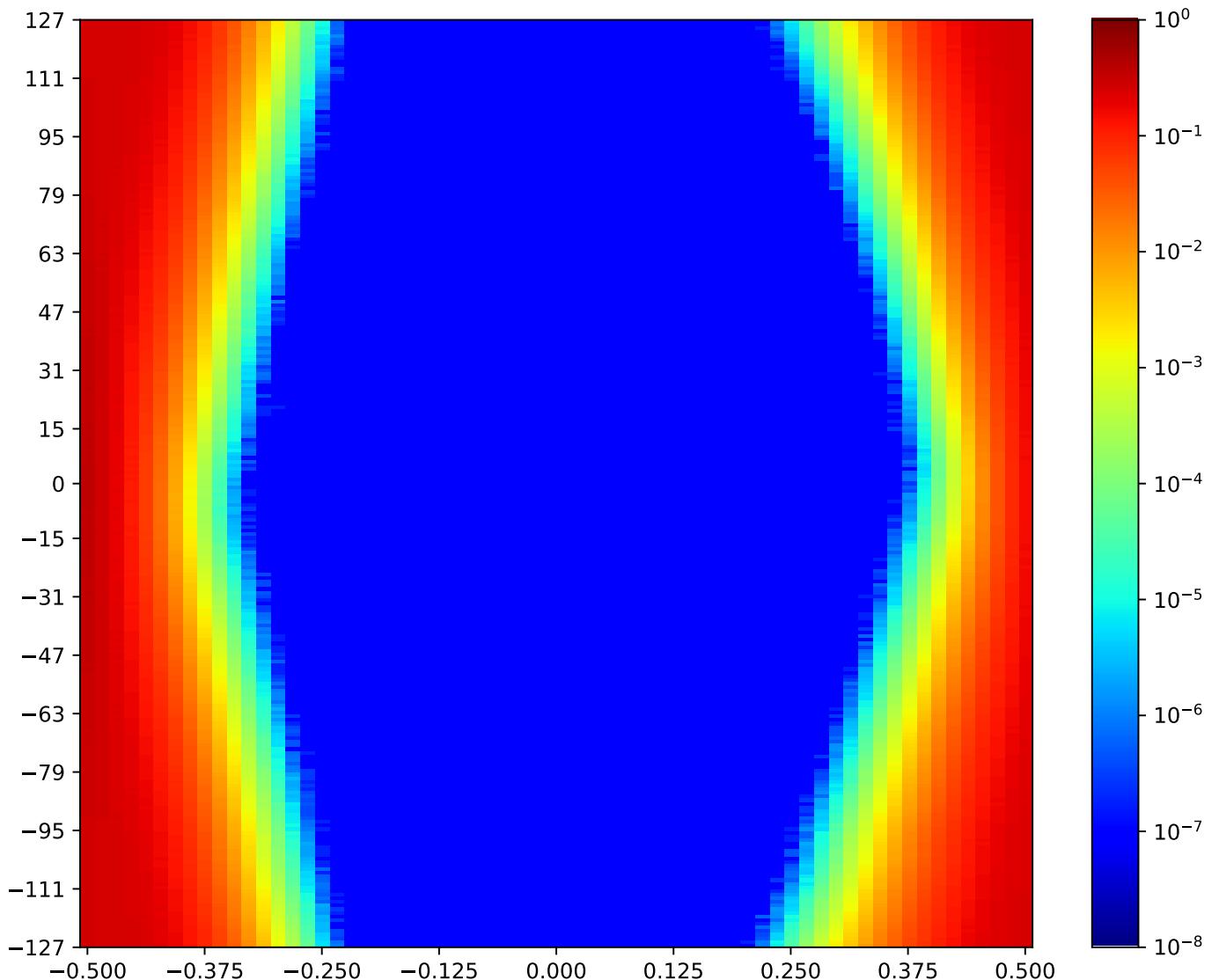


Figure 2.186: TRP\_FPGA-TX5-06-RX14-06-MSP\_C\_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.14.8 TRP\_FPGA-TX5-07-RX14-07-MSP\_C\_FPGA

Table 2.173: TRP\_FPGA-TX5-07-RX14-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 21:18:39		2018-Jan-24 21:19:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9273	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

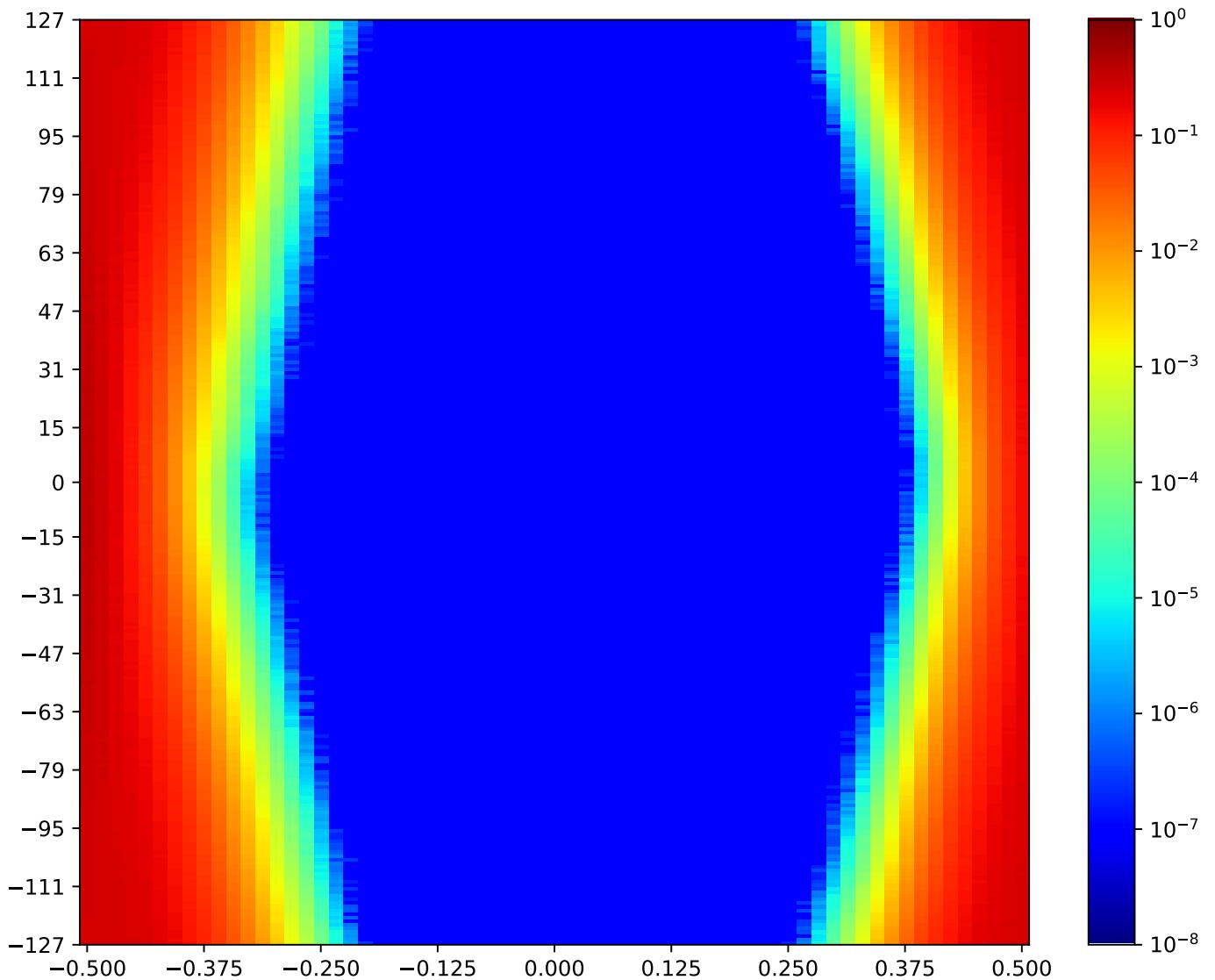


Figure 2.187: TRP\_FPGA-TX5-07-RX14-07-MSP\_C\_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15 MSP\_A TX1 MSP\_C RX11 Minipod Loopback

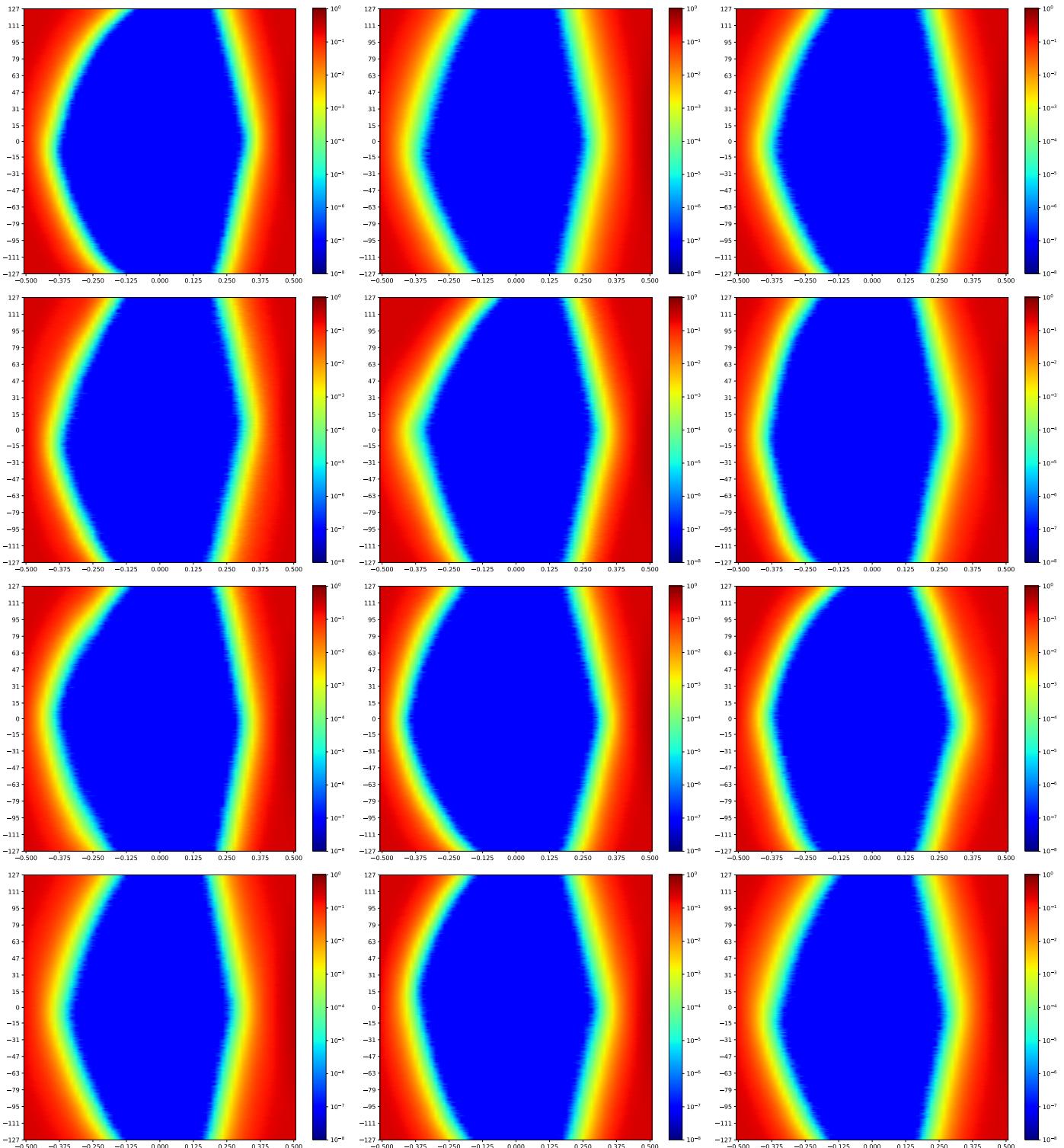


Figure 2.188: MSP\_A TX1 MSP\_C RX11 Minipod Loopback

A cross-reference to Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.201.

### 2.15.1 MSP\_A\_FPGA-TX1-00-RX11-00-MSP\_C\_FPGA

Table 2.174: MSP\_A\_FPGA-TX1-00-RX11-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:28:04		2018-Jan-24 21:28:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8386	43	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

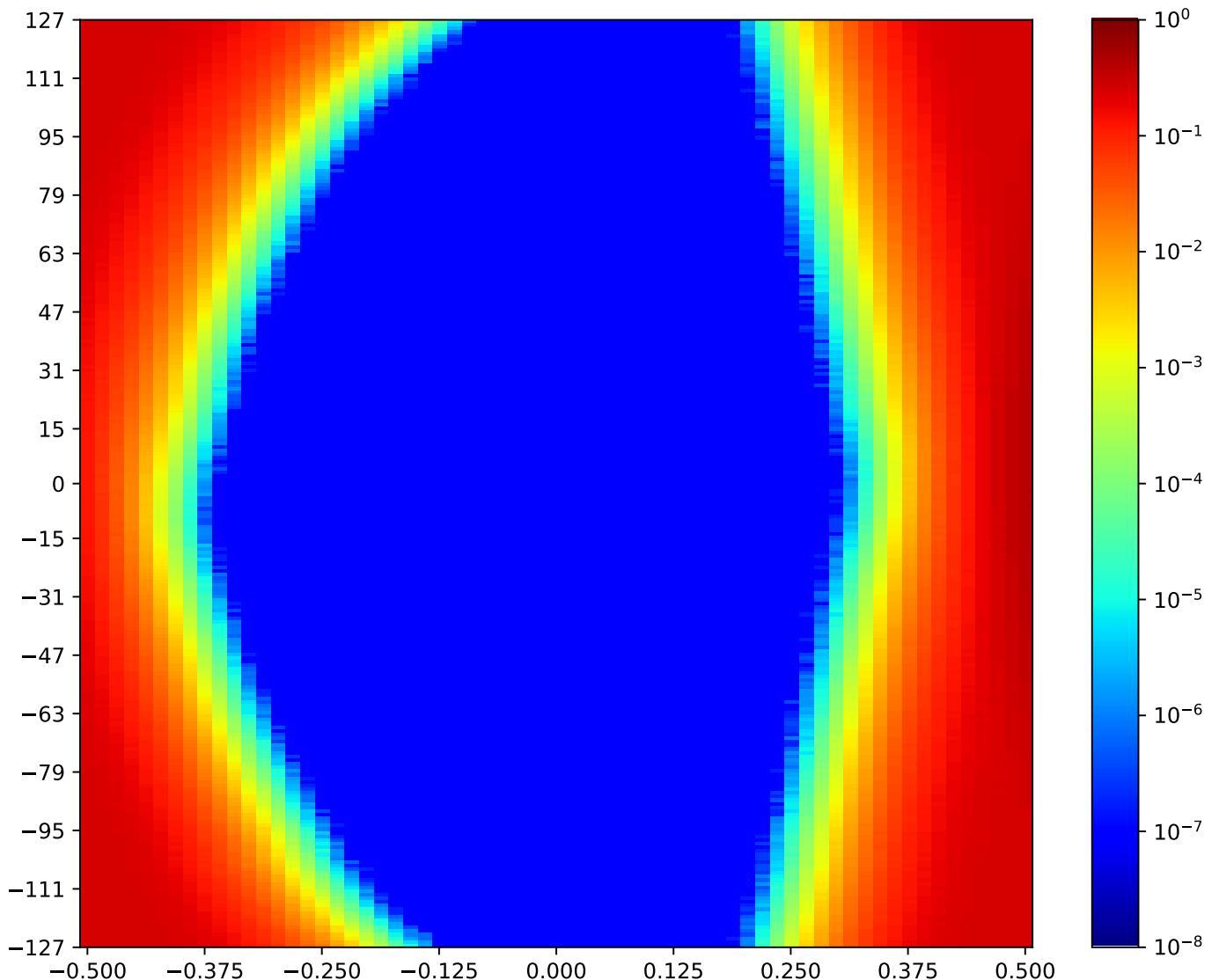


Figure 2.189: MSP\_A\_FPGA-TX1-00-RX11-00-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.2 MSP\_A\_FPGA-TX1-01-RX11-01-MSP\_C\_FPGA

Table 2.175: MSP\_A\_FPGA-TX1-01-RX11-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:29:07		2018-Jan-24 21:29:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6912	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

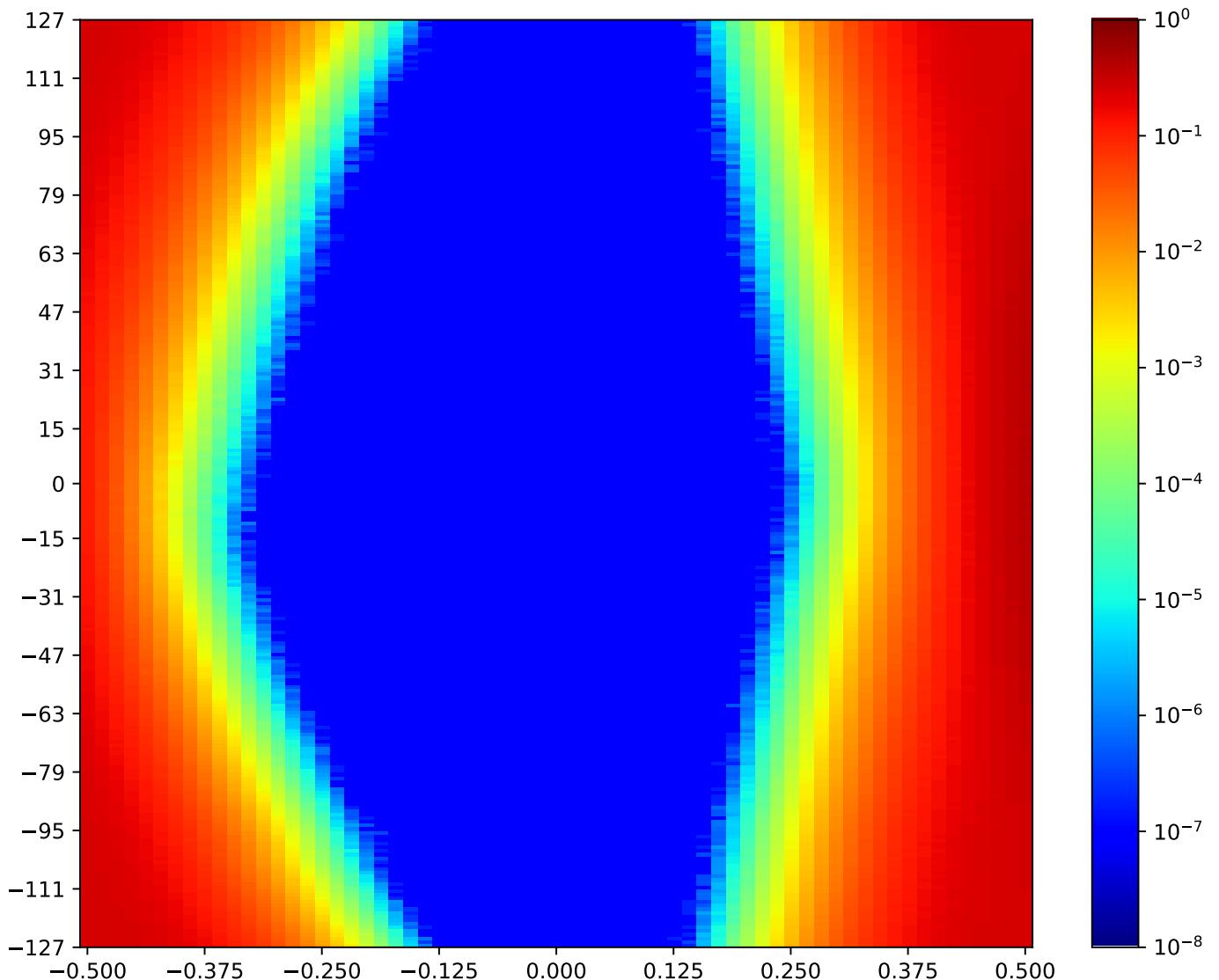


Figure 2.190: MSP\_A\_FPGA-TX1-01-RX11-01-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.15.3 MSP\_A\_FPGA-TX1-02-RX11-02-MSP\_C\_FPGA

Table 2.176: MSP\_A\_FPGA-TX1-02-RX11-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:29:39		2018-Jan-24 21:30:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7593	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

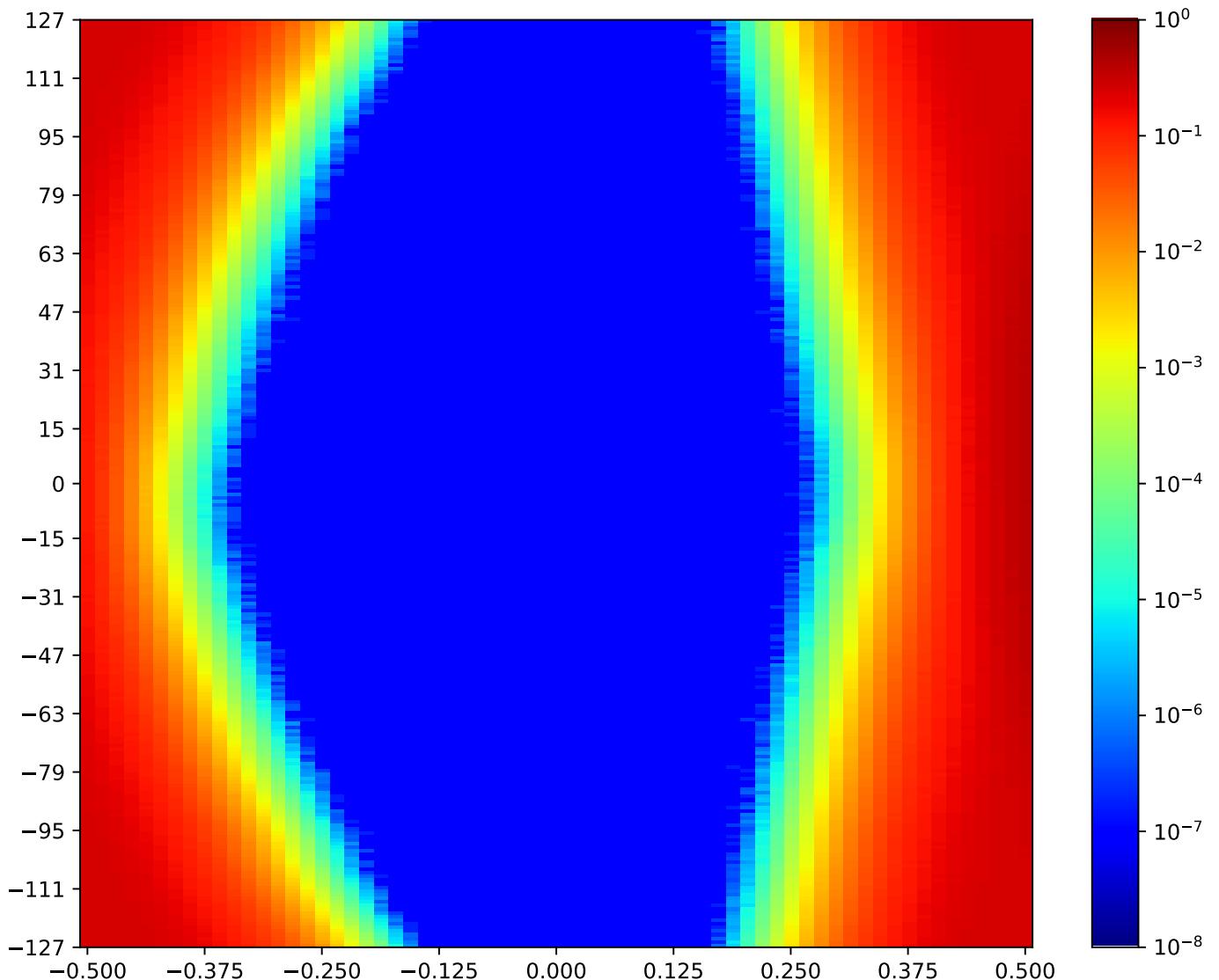


Figure 2.191: MSP\_A\_FPGA-TX1-02-RX11-02-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.4 MSP\_A\_FPGA-TX1-03-RX11-03-MSP\_C\_FPGA

Table 2.177: MSP\_A\_FPGA-TX1-03-RX11-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:27:00		2018-Jan-24 21:27:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7890	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

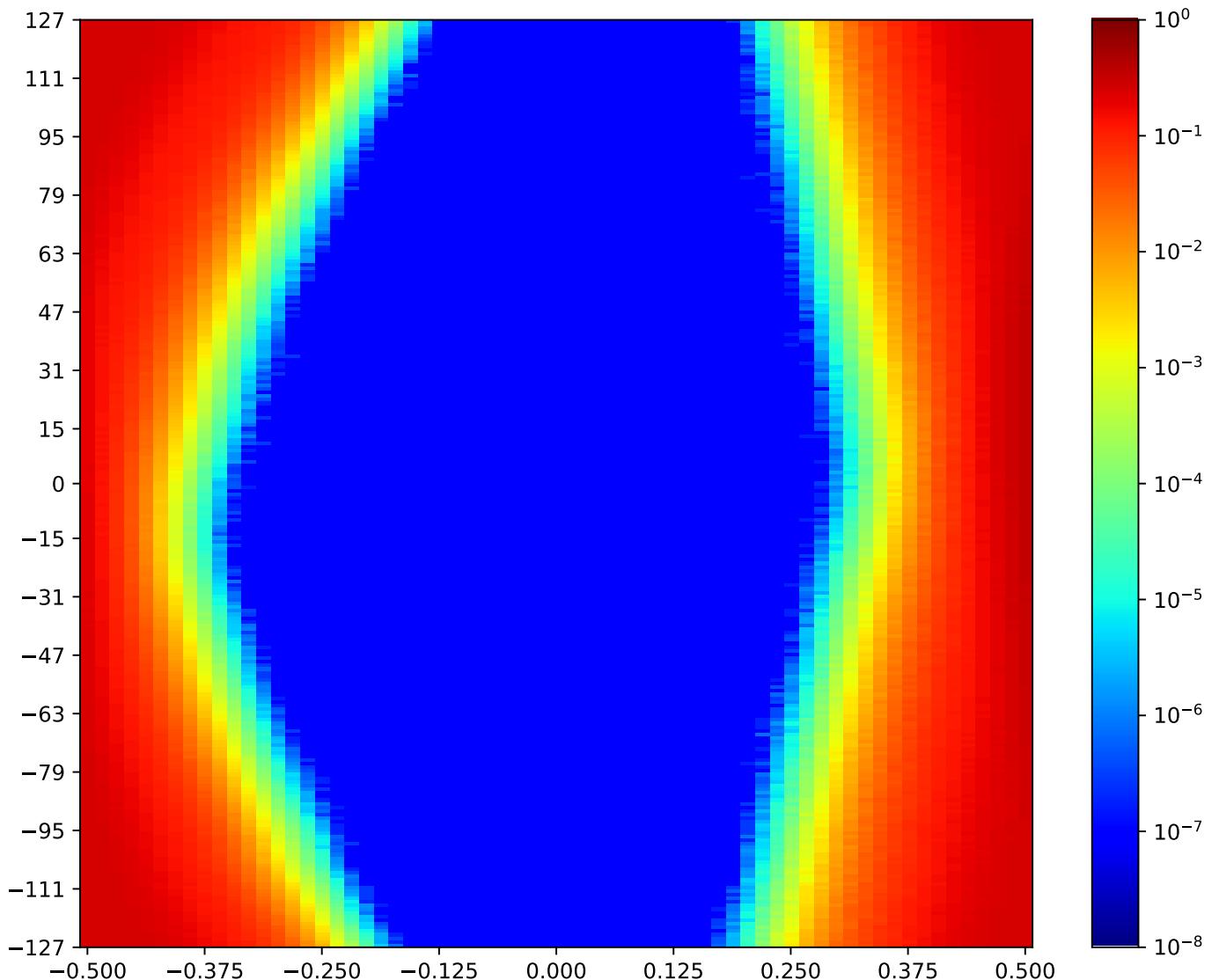


Figure 2.192: MSP\_A\_FPGA-TX1-03-RX11-03-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.5 MSP\_A\_FPGA-TX1-04-RX11-04-MSP\_C\_FPGA

Table 2.178: MSP\_A\_FPGA-TX1-04-RX11-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:31:15		2018-Jan-24 21:31:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7136	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

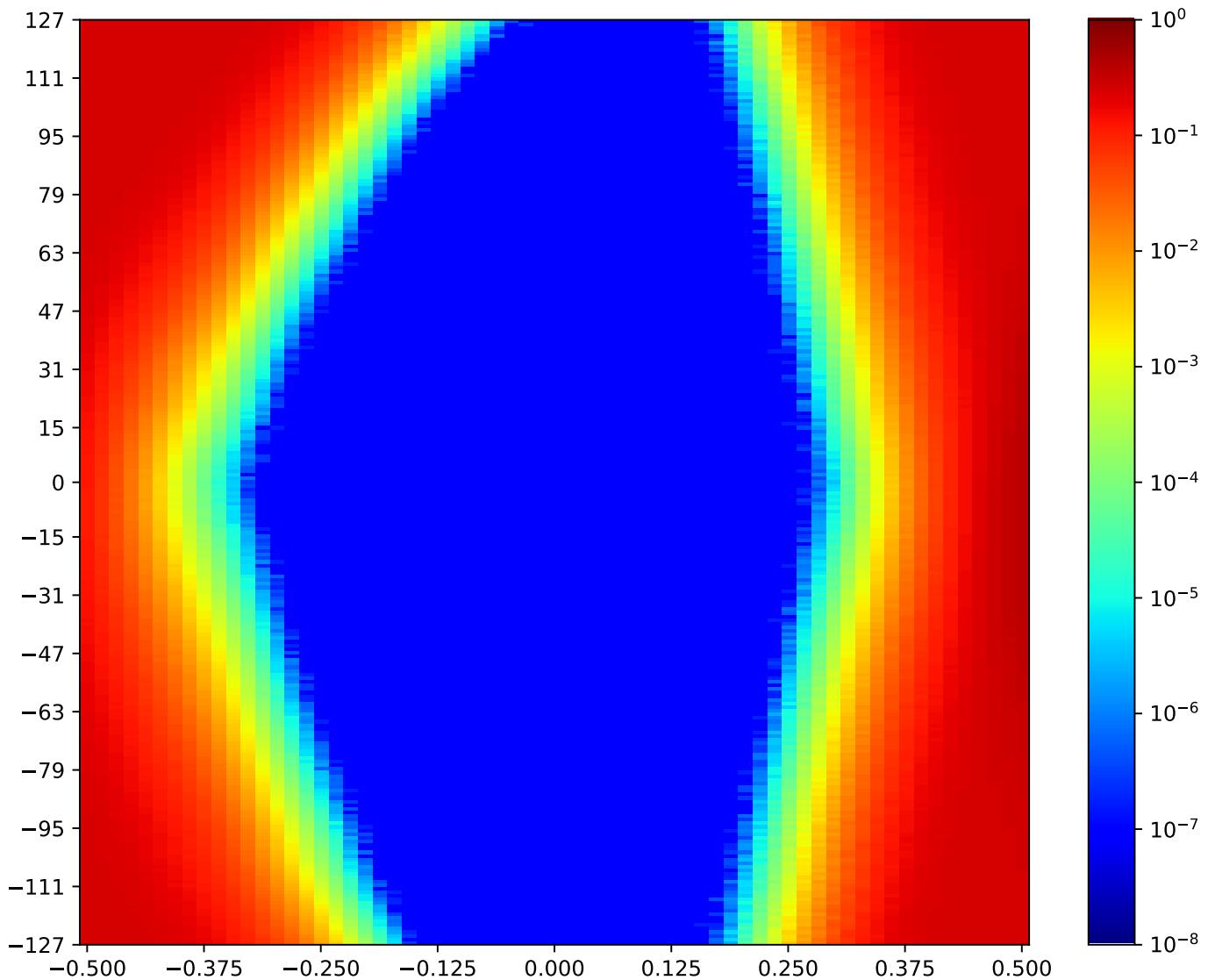


Figure 2.193: MSP\_A\_FPGA-TX1-04-RX11-04-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.6 MSP\_A\_FPGA-TX1-05-RX11-05-MSP\_C\_FPGA

Table 2.179: MSP\_A\_FPGA-TX1-05-RX11-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:26:28		2018-Jan-24 21:27:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7795	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

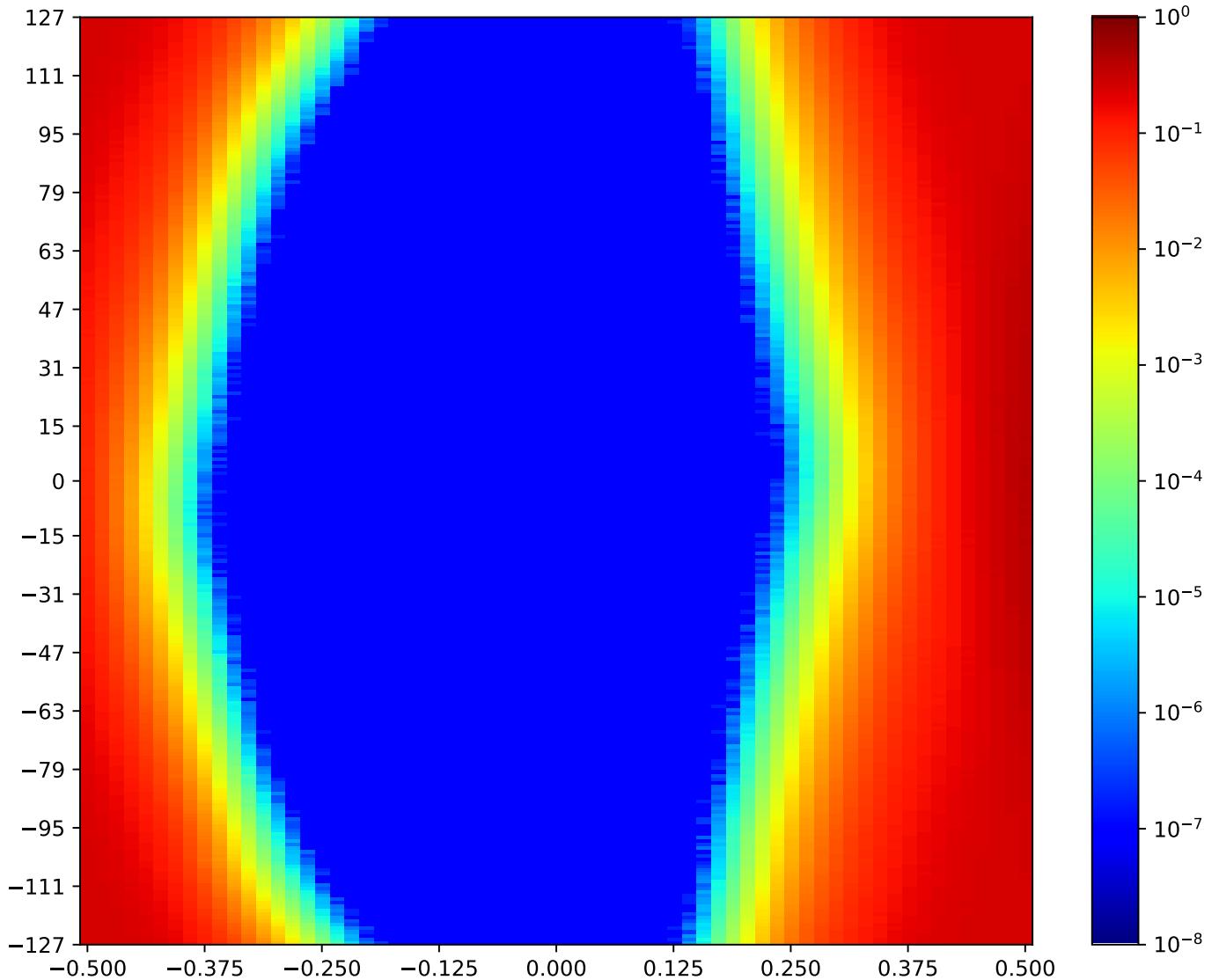


Figure 2.194: MSP\_A\_FPGA-TX1-05-RX11-05-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.7 MSP\_A\_FPGA-TX1-06-RX11-06-MSP\_C\_FPGA

Table 2.180: MSP\_A\_FPGA-TX1-06-RX11-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:32:17		2018-Jan-24 21:32:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8195	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

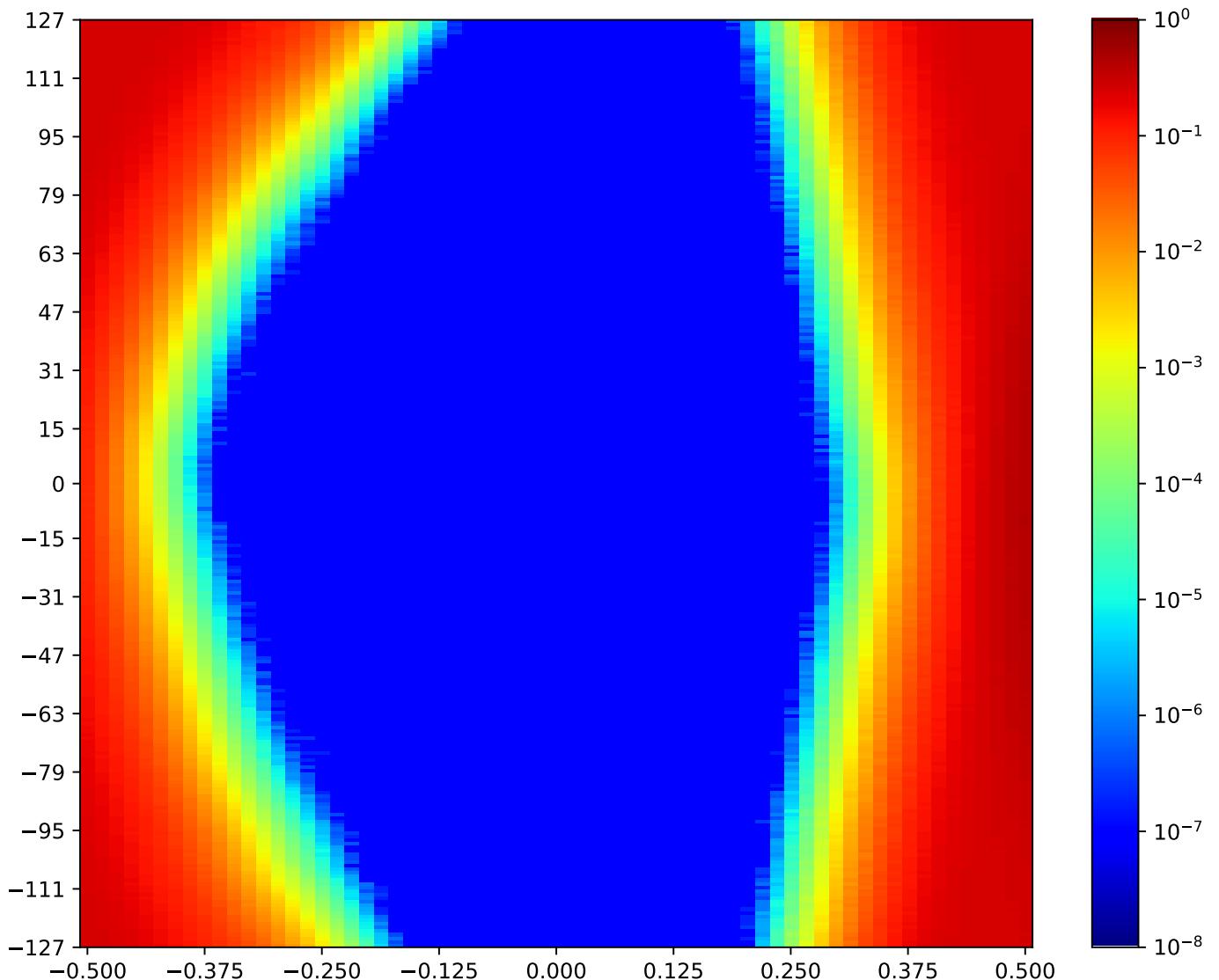


Figure 2.195: MSP\_A\_FPGA-TX1-06-RX11-06-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.8 MSP\_A\_FPGA-TX1-07-RX11-07-MSP\_C\_FPGA

Table 2.181: MSP\_A\_FPGA-TX1-07-RX11-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:27:32		2018-Jan-24 21:28:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8496	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

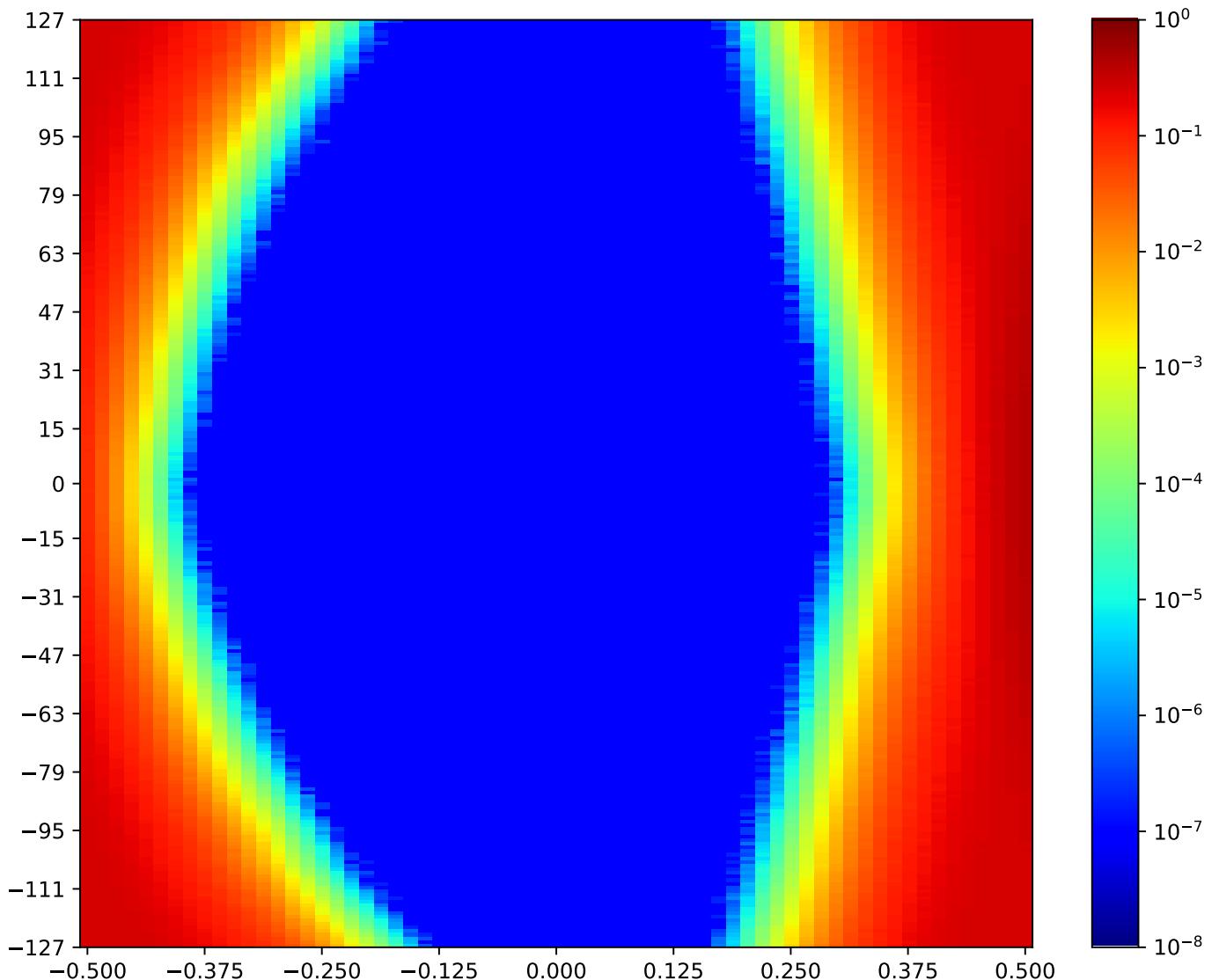


Figure 2.196: MSP\_A\_FPGA-TX1-07-RX11-07-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.9 MSP\_A\_FPGA-TX1-08-RX11-08-MSP\_C\_FPGA

Table 2.182: MSP\_A\_FPGA-TX1-08-RX11-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:31:46		2018-Jan-24 21:32:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7720	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

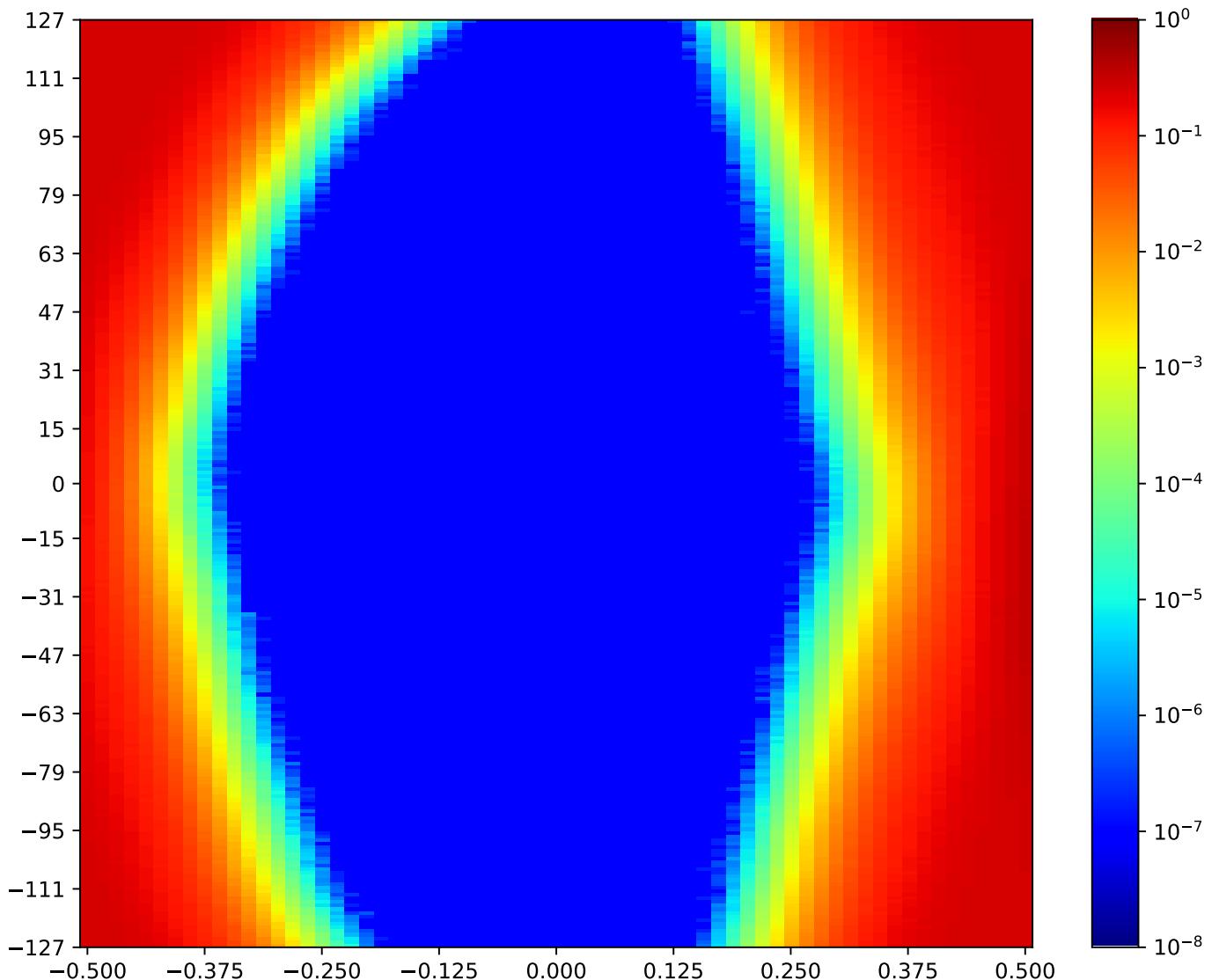


Figure 2.197: MSP\_A\_FPGA-TX1-08-RX11-08-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.10 MSP\_A\_FPGA-TX1-09-RX11-09-MSP\_C\_FPGA

Table 2.183: MSP\_A\_FPGA-TX1-09-RX11-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:28:36		2018-Jan-24 21:29:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7127	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

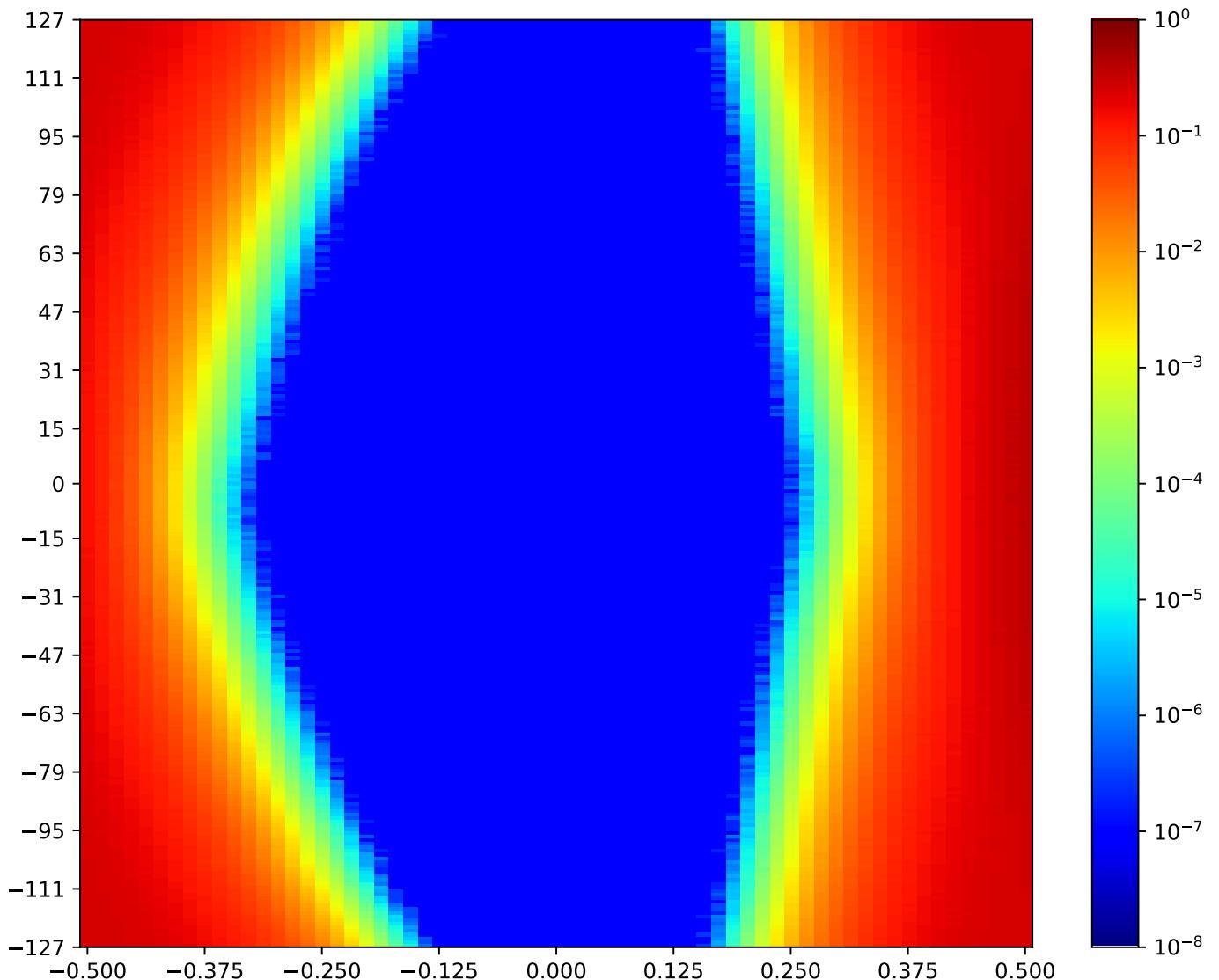


Figure 2.198: MSP\_A\_FPGA-TX1-09-RX11-09-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.11 MSP\_A\_FPGA-TX1-10-RX11-10-MSP\_C\_FPGA

Table 2.184: MSP\_A\_FPGA-TX1-10-RX11-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:30:43		2018-Jan-24 21:31:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7936	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

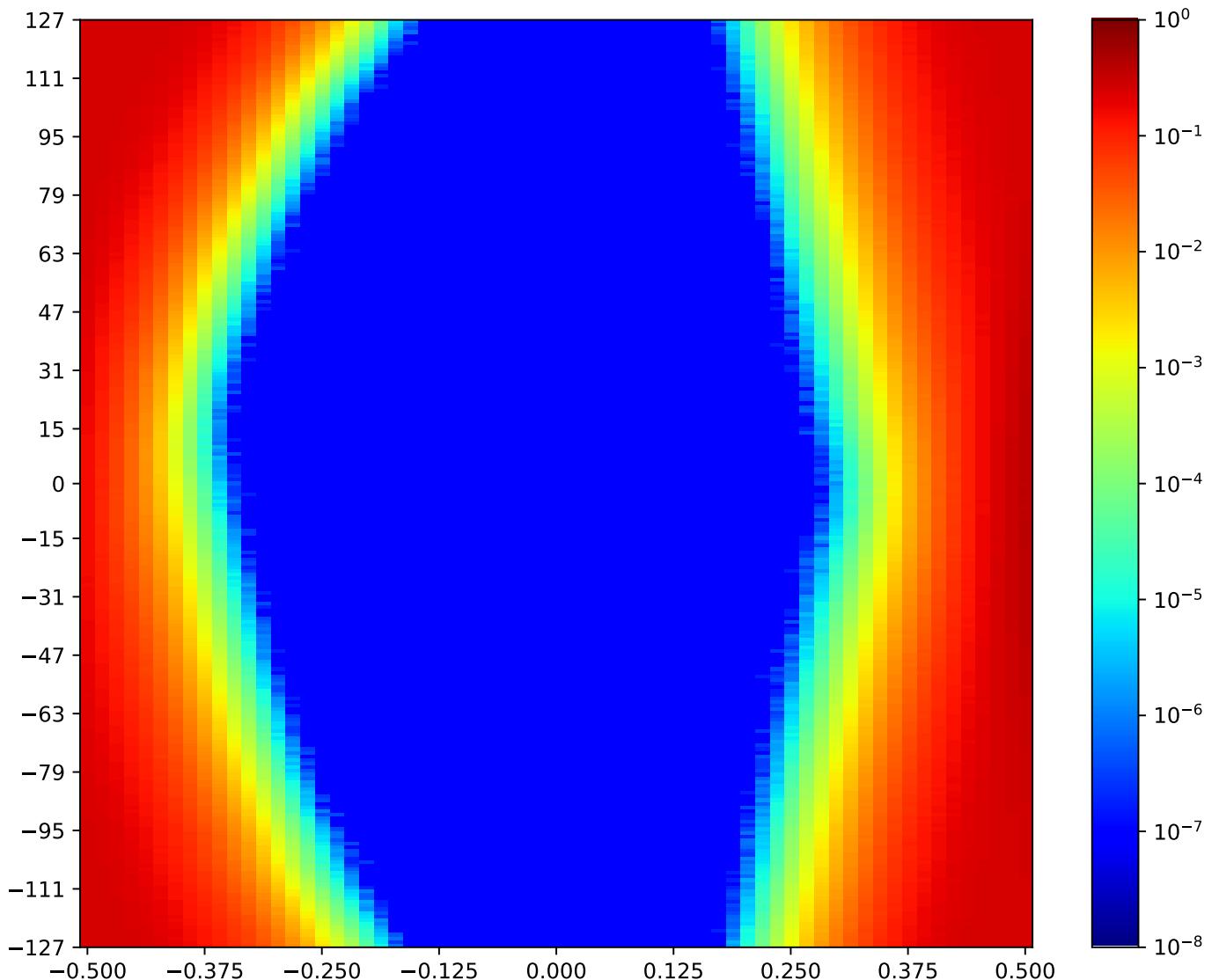


Figure 2.199: MSP\_A\_FPGA-TX1-10-RX11-10-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.15.12 MSP\_A\_FPGA-TX1-11-RX11-11-MSP\_C\_FPGA

Table 2.185: MSP\_A\_FPGA-TX1-11-RX11-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:30:11		2018-Jan-24 21:30:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7239	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

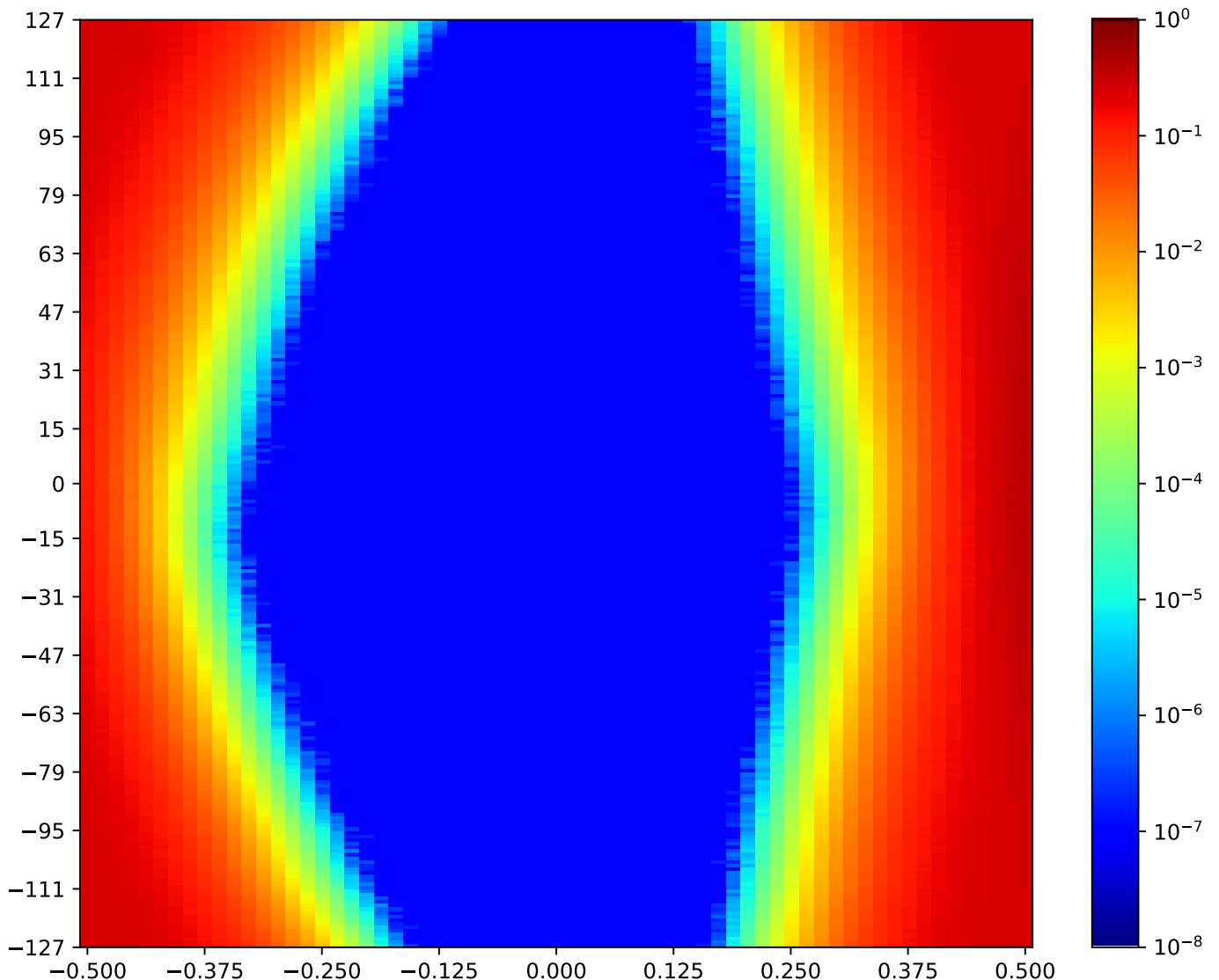


Figure 2.200: MSP\_A\_FPGA-TX1-11-RX11-11-MSP\_C\_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16 MSP\_A TX2 MSP\_C RX10 Minipod Loopback

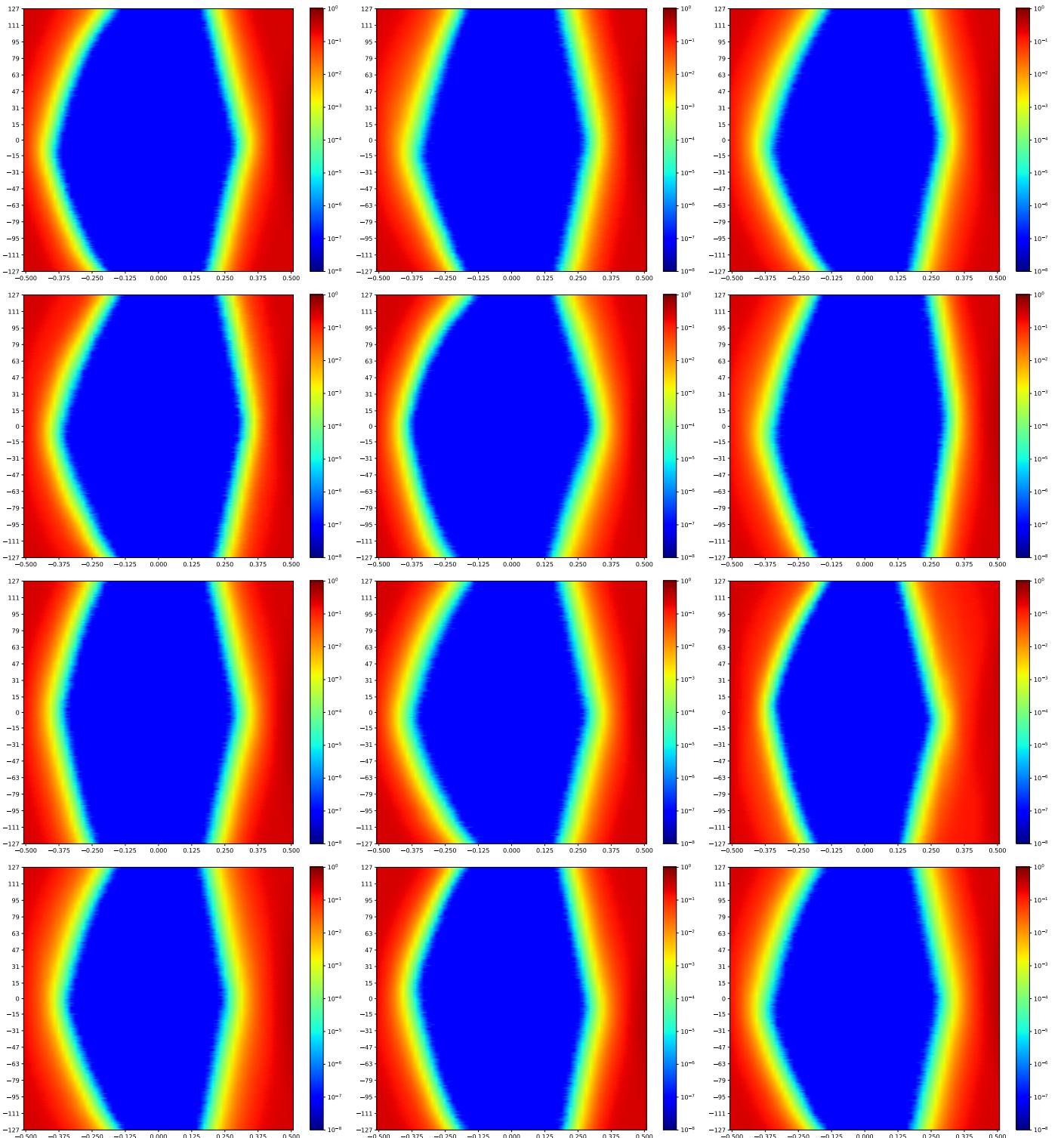


Figure 2.201: MSP\_A TX2 MSP\_C RX10 Minipod Loopback

A cross-reference to Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.214.

### 2.16.1 MSP\_A\_FPGA-TX2-00-RX10-00-MSP\_C\_FPGA

Table 2.186: MSP\_A\_FPGA-TX2-00-RX10-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:34:23		2018-Jan-24 21:34:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8087	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

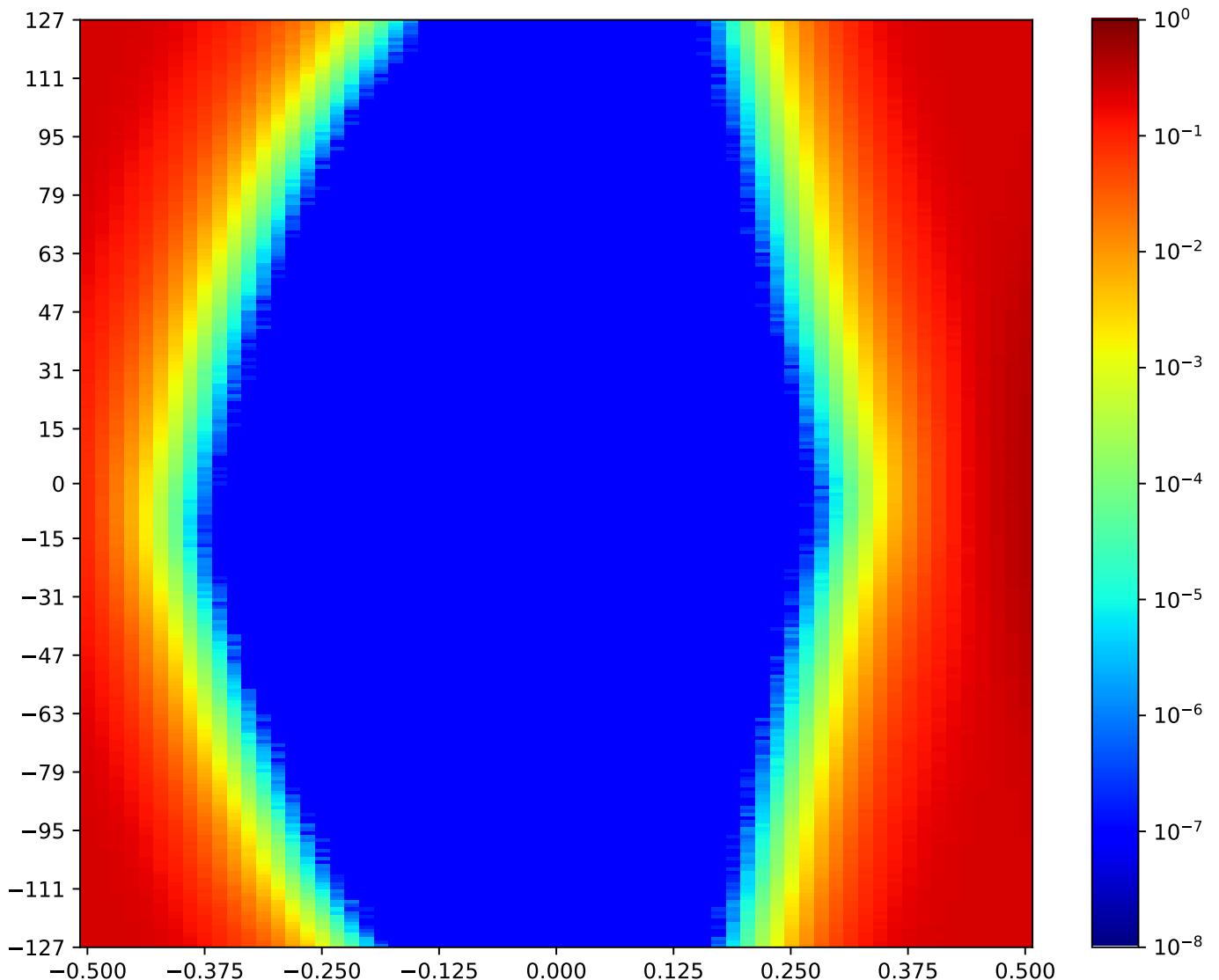


Figure 2.202: MSP\_A\_FPGA-TX2-00-RX10-00-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.2 MSP\_A\_FPGA-TX2-01-RX10-01-MSP\_C\_FPGA

Table 2.187: MSP\_A\_FPGA-TX2-01-RX10-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:33:18		2018-Jan-24 21:33:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7312	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

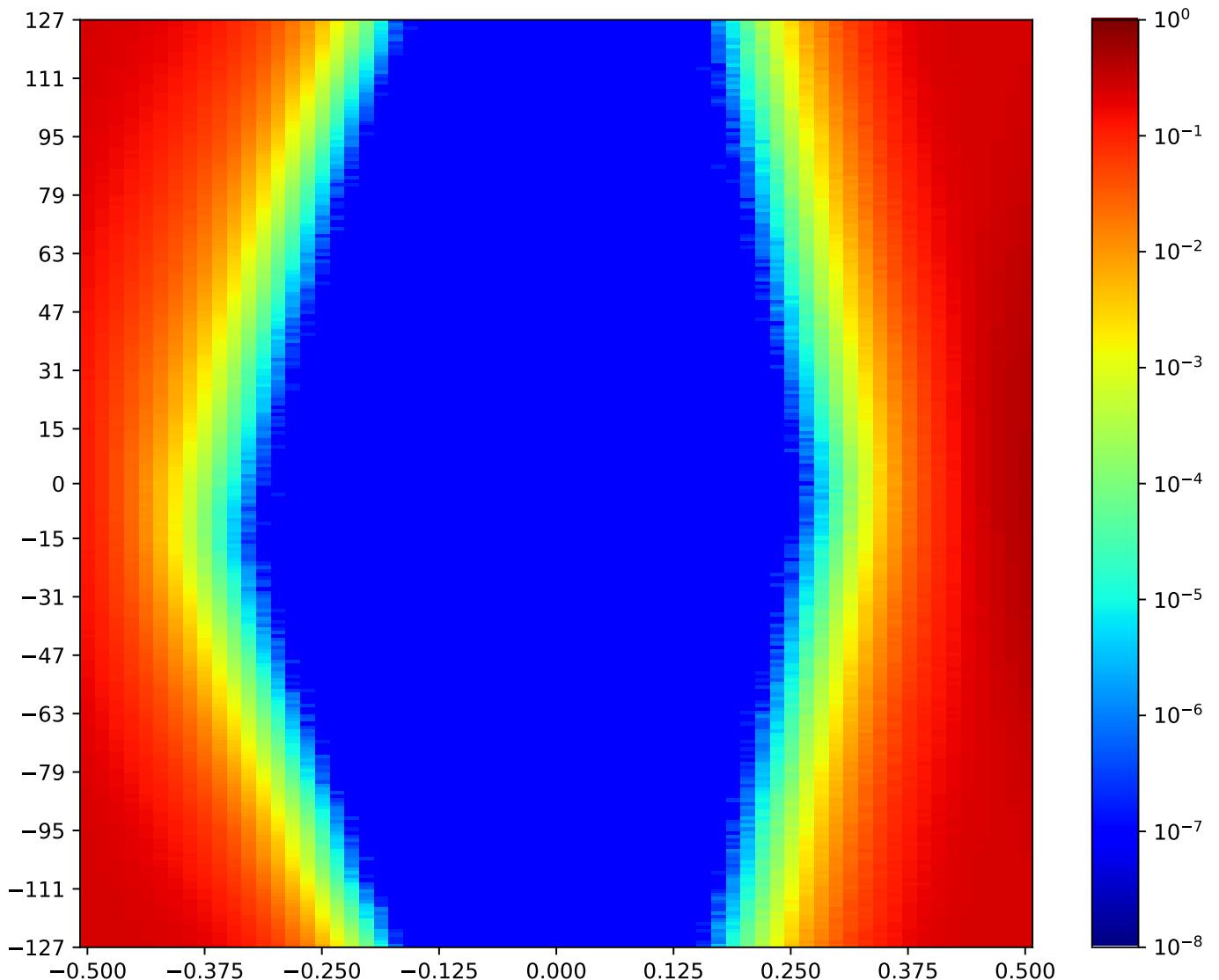


Figure 2.203: MSP\_A\_FPGA-TX2-01-RX10-01-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.16.3 MSP\_A\_FPGA-TX2-02-RX10-02-MSP\_C\_FPGA

Table 2.188: MSP\_A\_FPGA-TX2-02-RX10-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:35:56		2018-Jan-24 21:36:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7147	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

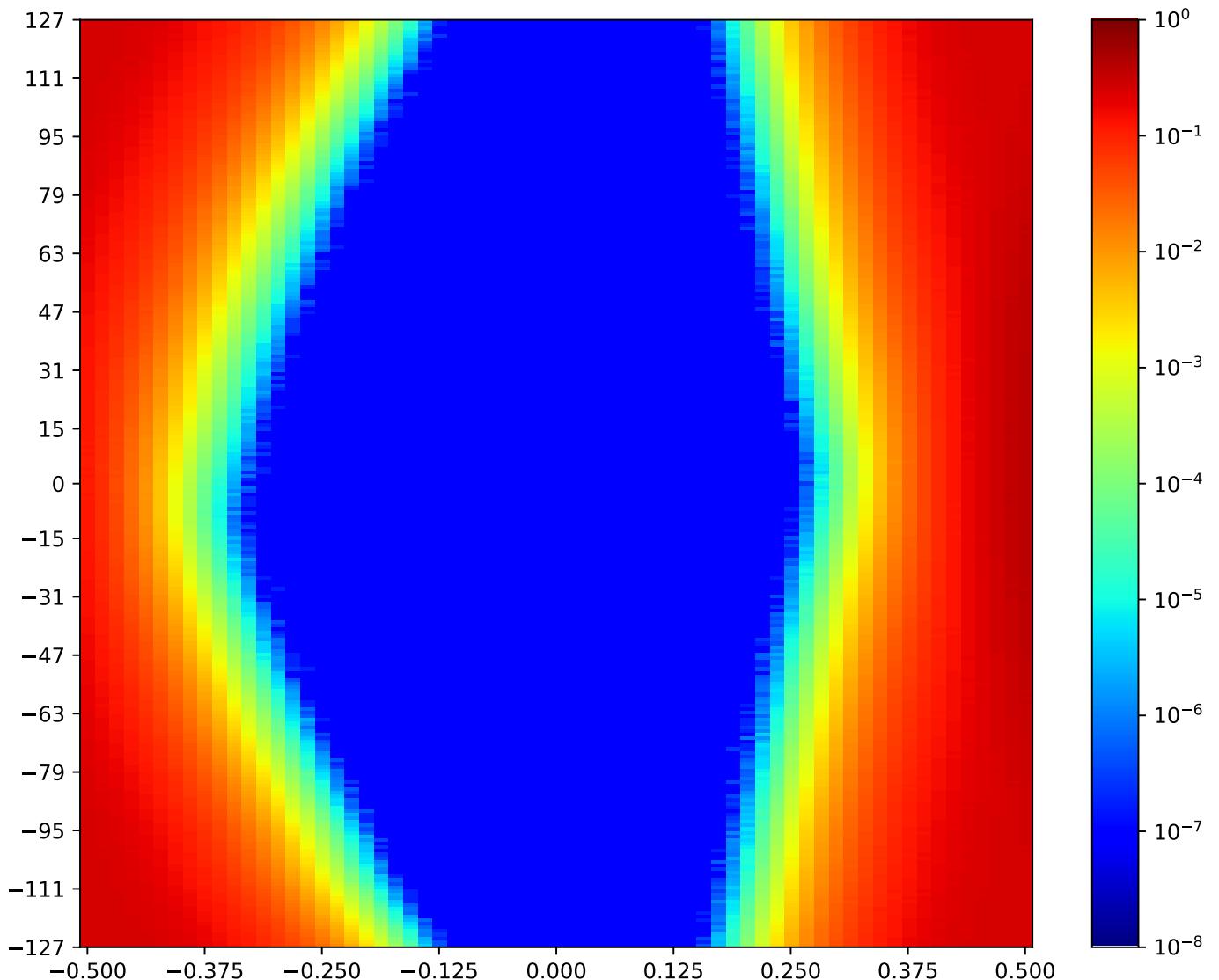


Figure 2.204: MSP\_A\_FPGA-TX2-02-RX10-02-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.4 MSP\_A\_FPGA-TX2-03-RX10-03-MSP\_C\_FPGA

Table 2.189: MSP\_A\_FPGA-TX2-03-RX10-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:32:47		2018-Jan-24 21:33:18	
Reset RX	OA	HO		VO   VO (%)	
true	8179	39		60.00%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

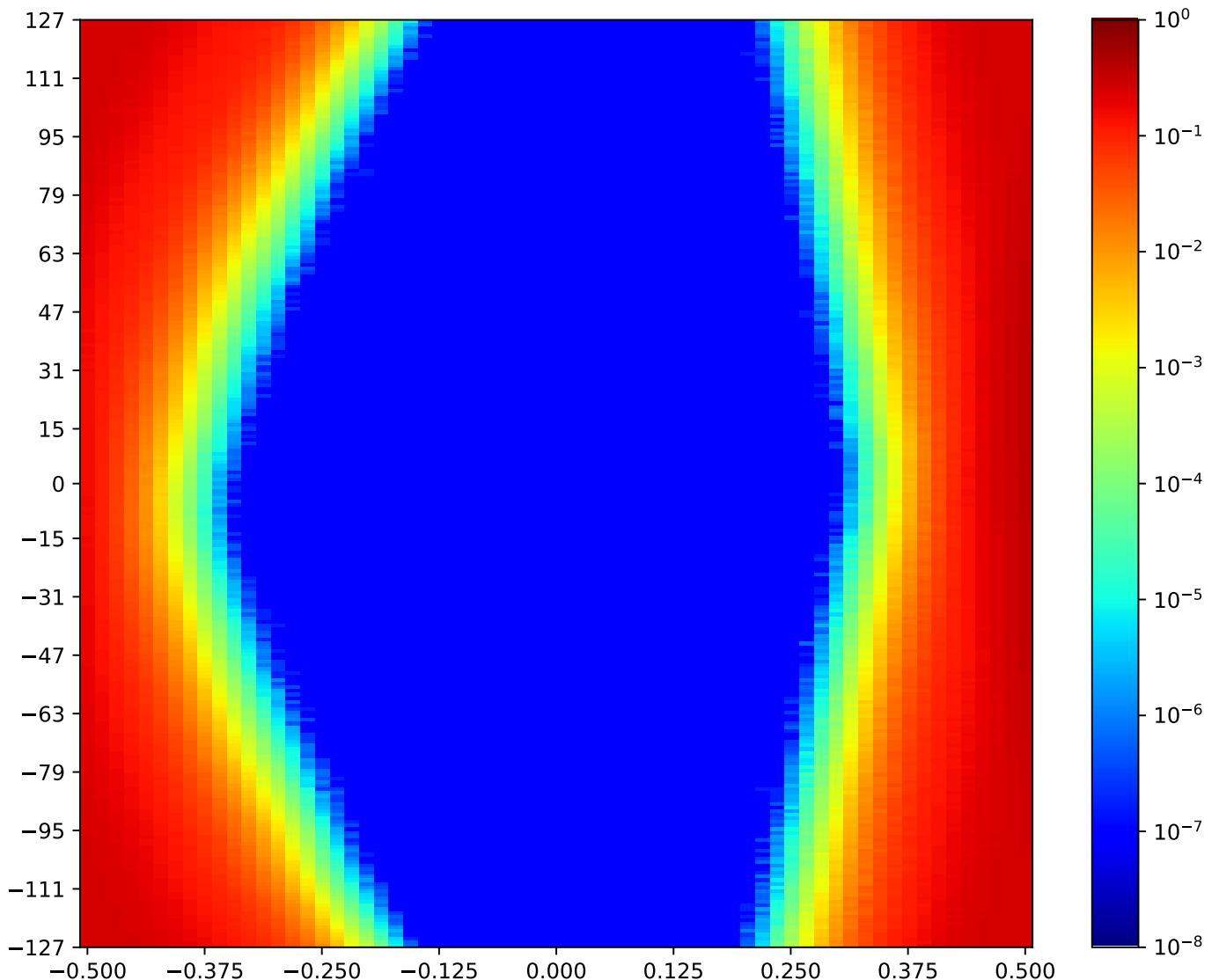


Figure 2.205: MSP\_A\_FPGA-TX2-03-RX10-03-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.5 MSP\_A\_FPGA-TX2-04-RX10-04-MSP\_C\_FPGA

Table 2.190: MSP\_A\_FPGA-TX2-04-RX10-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:37:28		2018-Jan-24 21:37:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7897	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

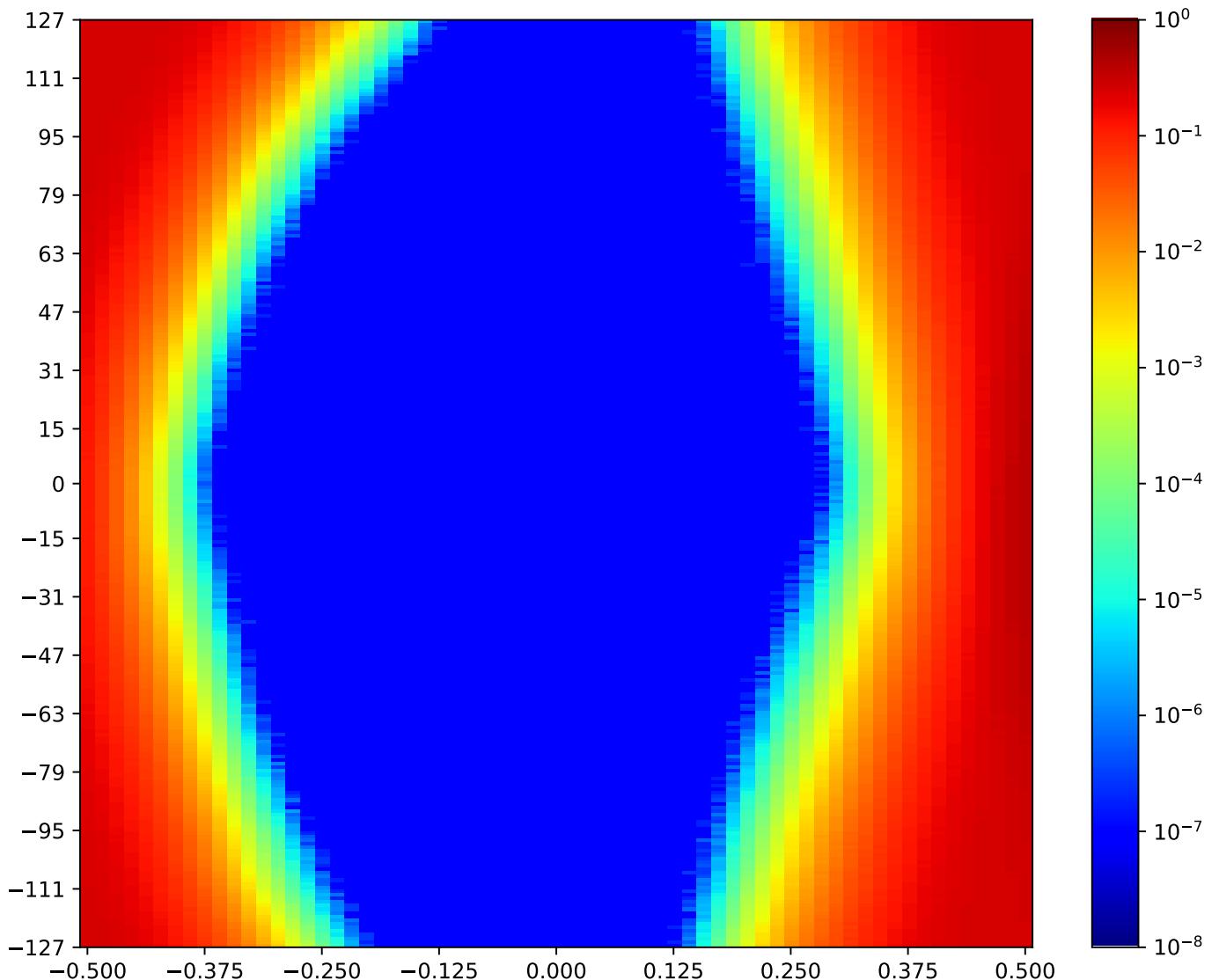


Figure 2.206: MSP\_A\_FPGA-TX2-04-RX10-04-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.6 MSP\_A\_FPGA-TX2-05-RX10-05-MSP\_C\_FPGA

Table 2.191: MSP\_A\_FPGA-TX2-05-RX10-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:33:50		2018-Jan-24 21:34:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8051	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

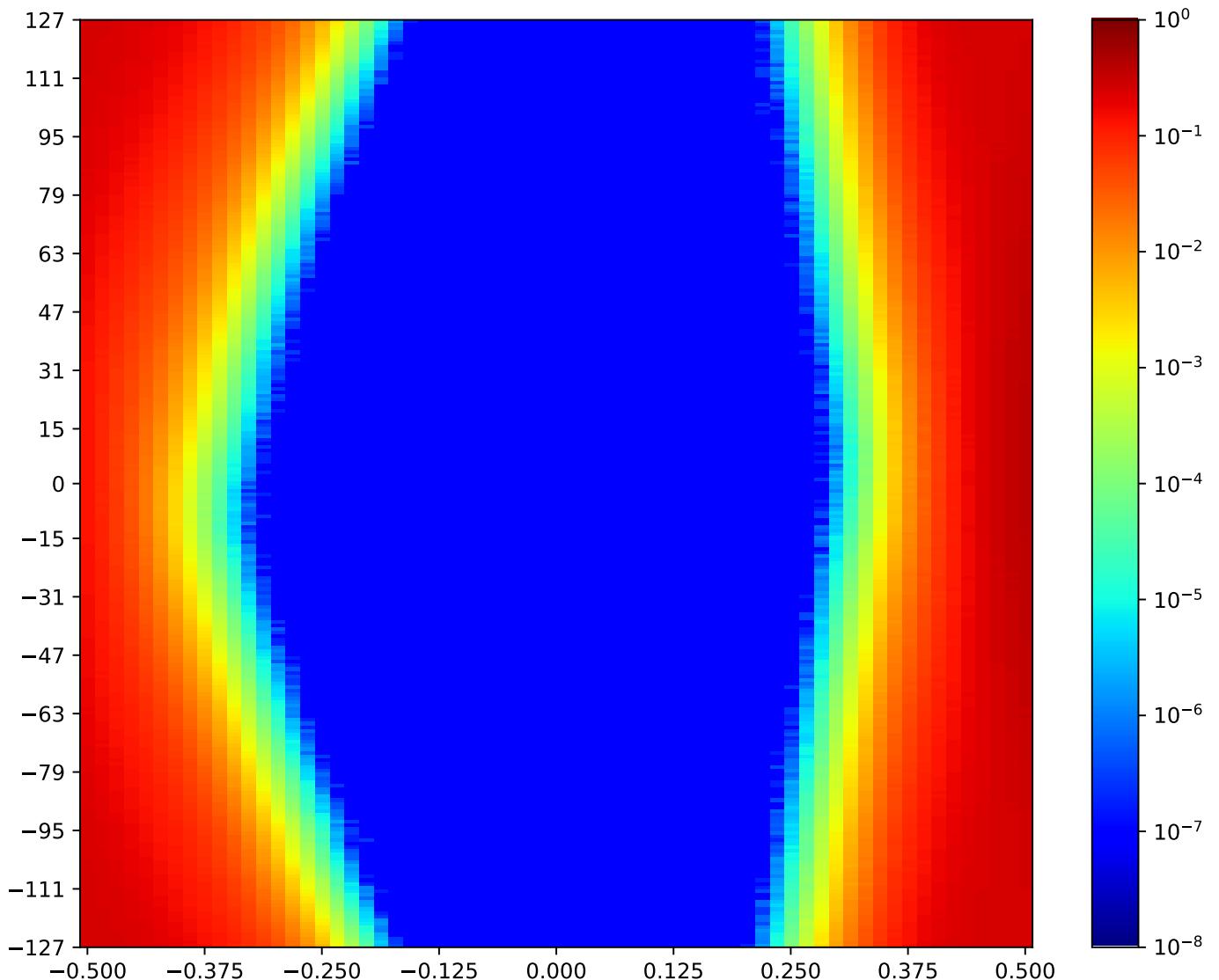


Figure 2.207: MSP\_A\_FPGA-TX2-05-RX10-05-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.7 MSP\_A\_FPGA-TX2-06-RX10-06-MSP\_C\_FPGA

Table 2.192: MSP\_A\_FPGA-TX2-06-RX10-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:38:27		2018-Jan-24 21:38:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8080	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

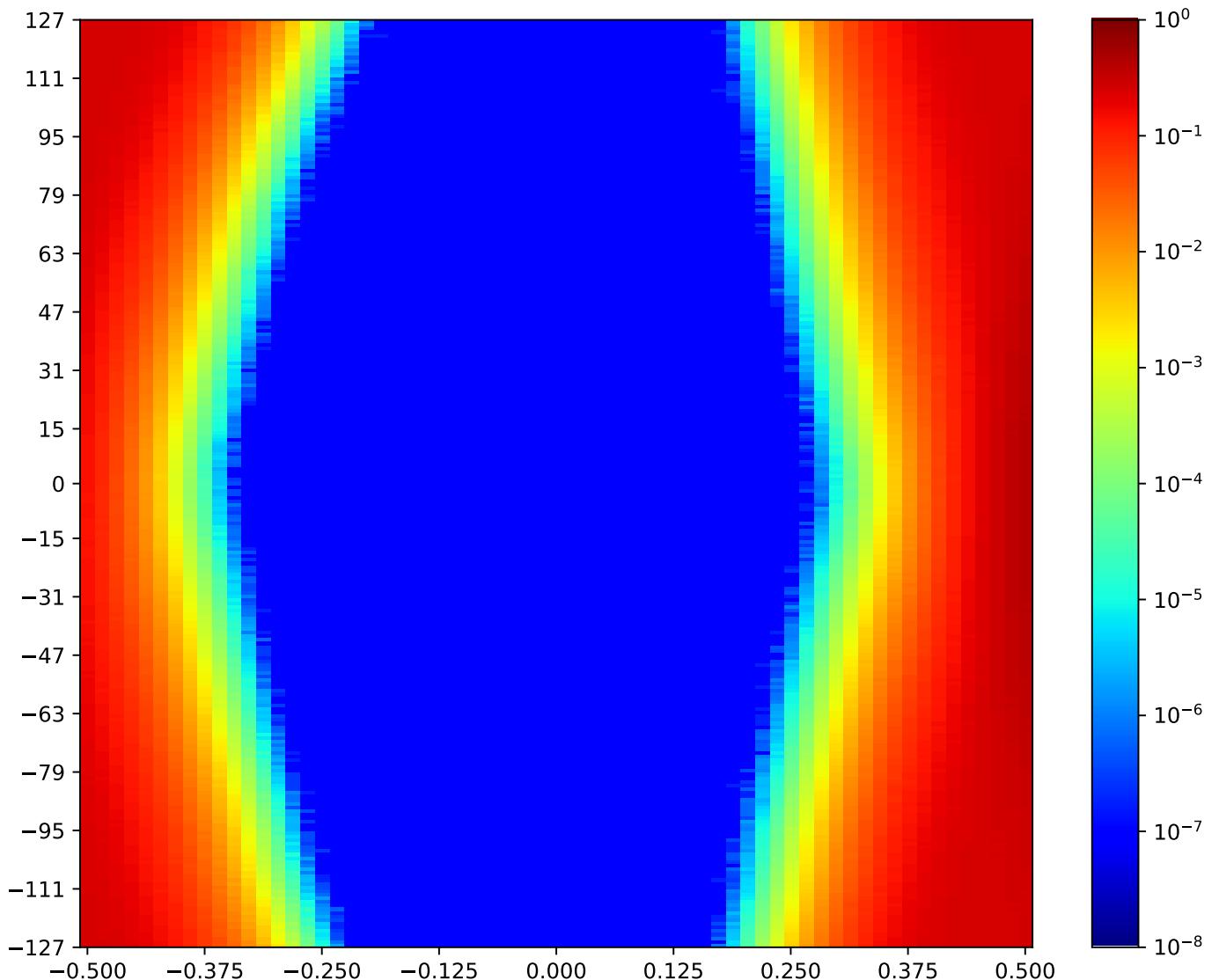


Figure 2.208: MSP\_A\_FPGA-TX2-06-RX10-06-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.8 MSP\_A\_FPGA-TX2-07-RX10-07-MSP\_C\_FPGA

Table 2.193: MSP\_A\_FPGA-TX2-07-RX10-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:34:54		2018-Jan-24 21:35:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7396	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

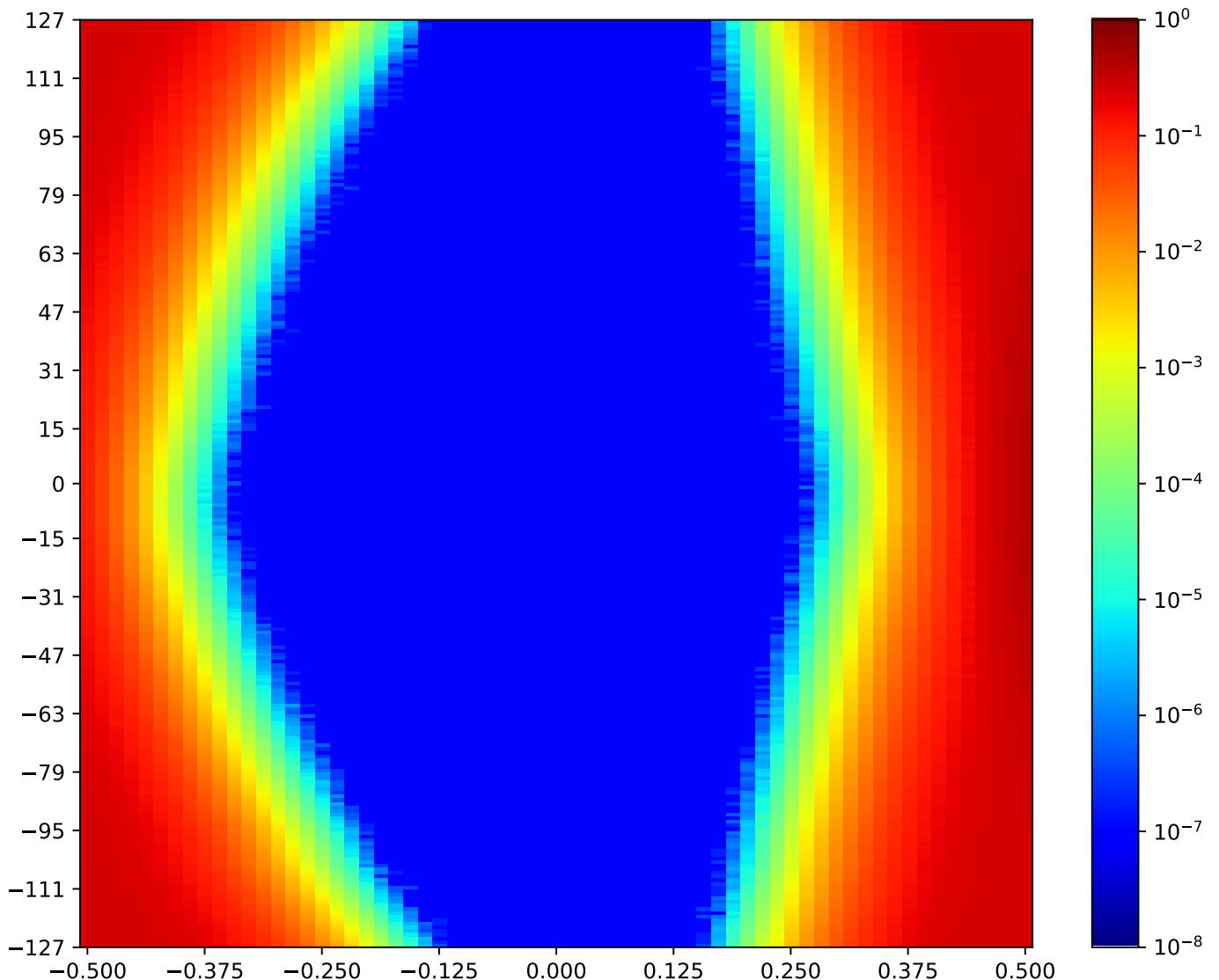


Figure 2.209: MSP\_A\_FPGA-TX2-07-RX10-07-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.9 MSP\_A\_FPGA-TX2-08-RX10-08-MSP\_C\_FPGA

Table 2.194: MSP\_A\_FPGA-TX2-08-RX10-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:37:59		2018-Jan-24 21:38:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6799	35	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

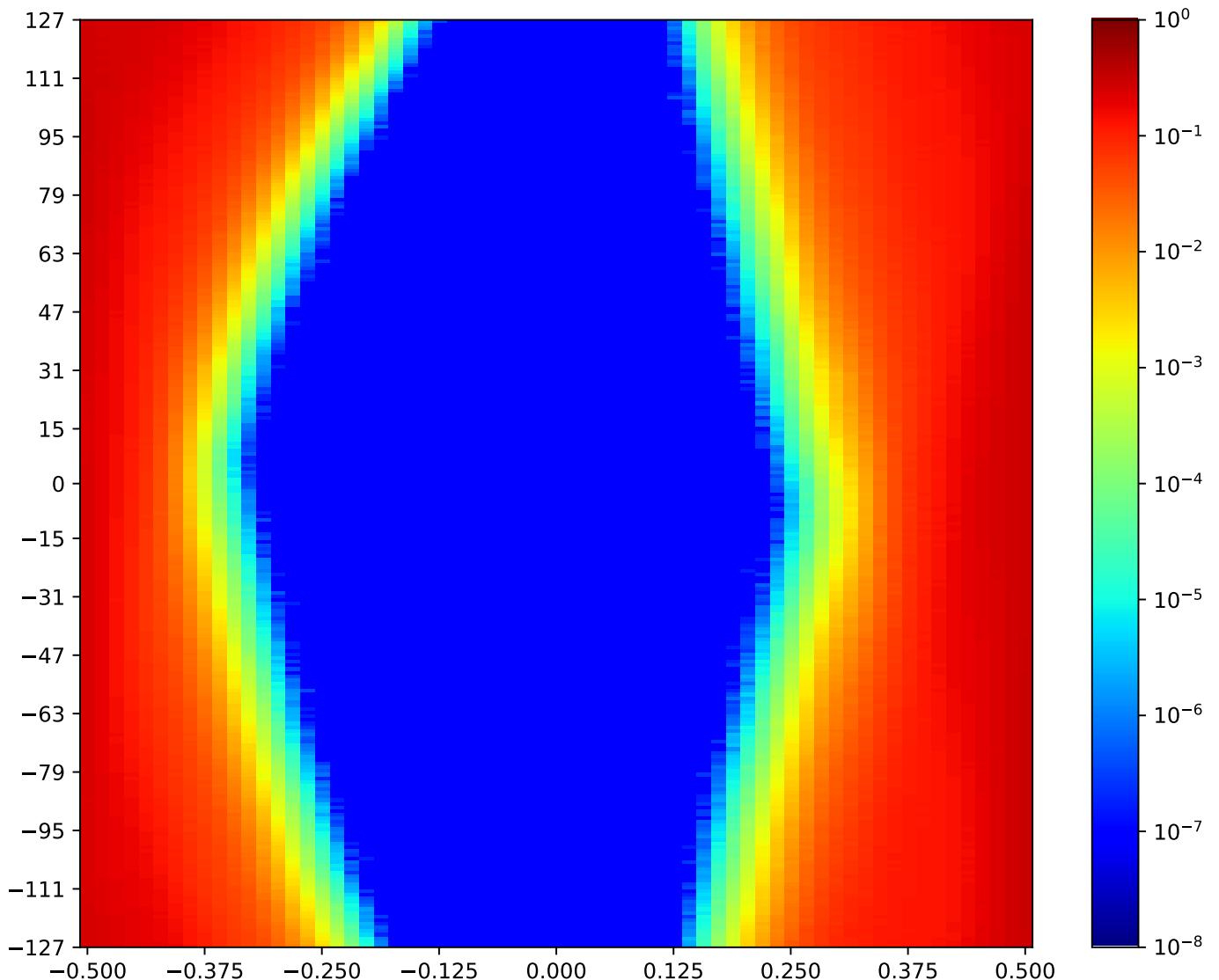


Figure 2.210: MSP\_A\_FPGA-TX2-08-RX10-08-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.10 MSP\_A\_FPGA-TX2-09-RX10-09-MSP\_C\_FPGA

Table 2.195: MSP\_A\_FPGA-TX2-09-RX10-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:35:27		2018-Jan-24 21:35:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7011	34	52.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

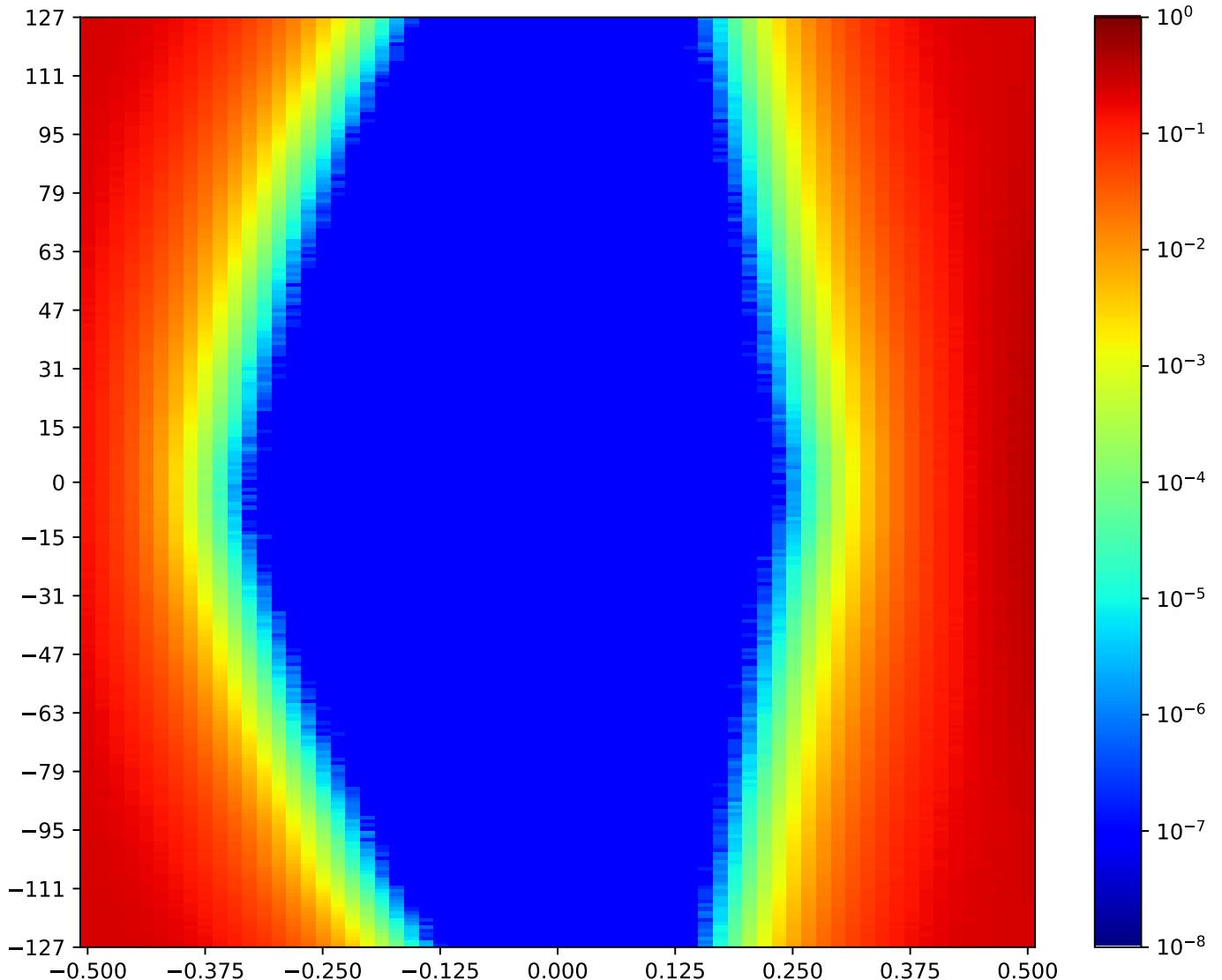


Figure 2.211: MSP\_A\_FPGA-TX2-09-RX10-09-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.11 MSP\_A\_FPGA-TX2-10-RX10-10-MSP\_C\_FPGA

Table 2.196: MSP\_A\_FPGA-TX2-10-RX10-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:36:58		2018-Jan-24 21:37:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7756	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
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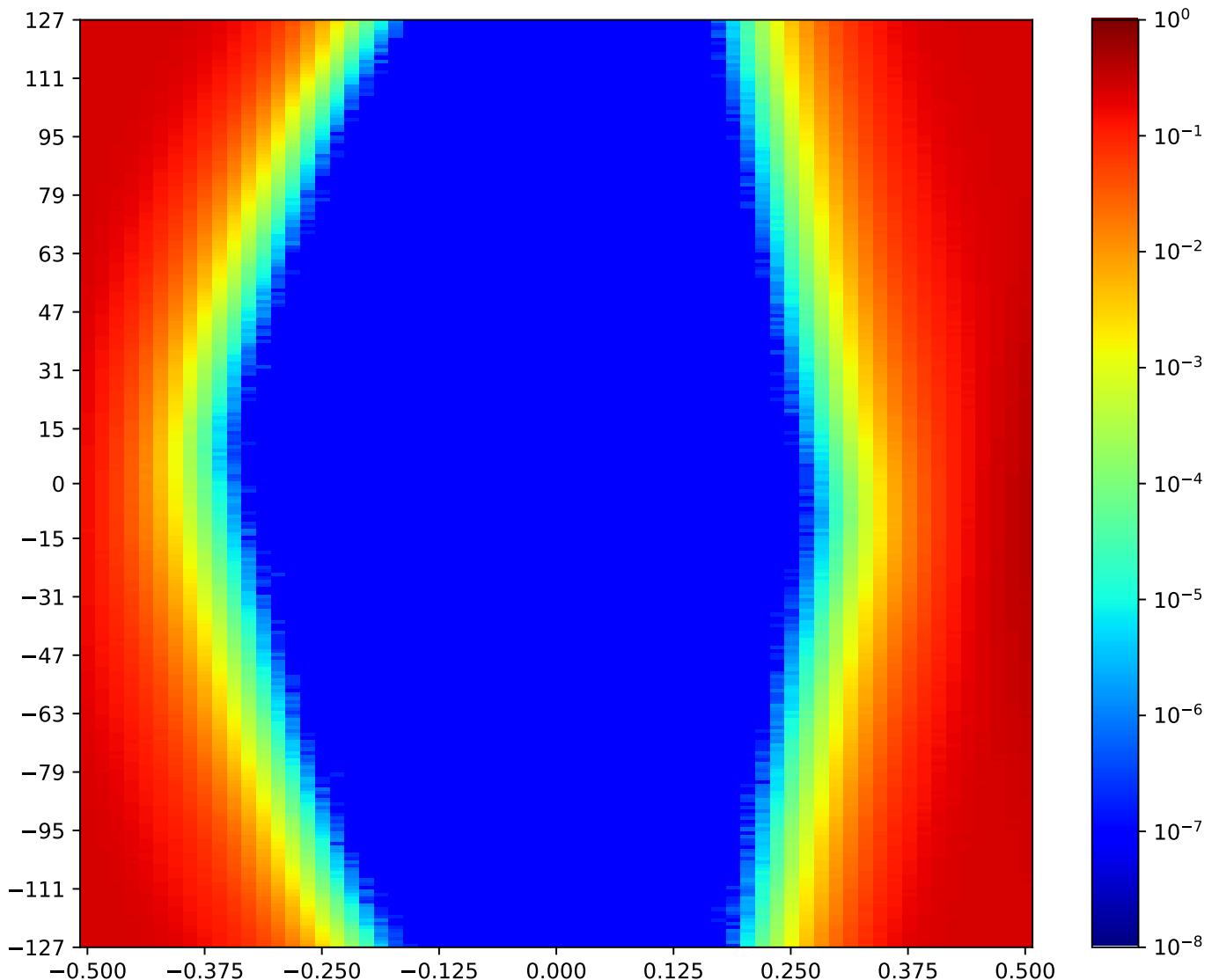


Figure 2.212: MSP\_A\_FPGA-TX2-10-RX10-10-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.16.12 MSP\_A\_FPGA-TX2-11-RX10-11-MSP\_C\_FPGA

Table 2.197: MSP\_A\_FPGA-TX2-11-RX10-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:36:29		2018-Jan-24 21:36:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7435	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

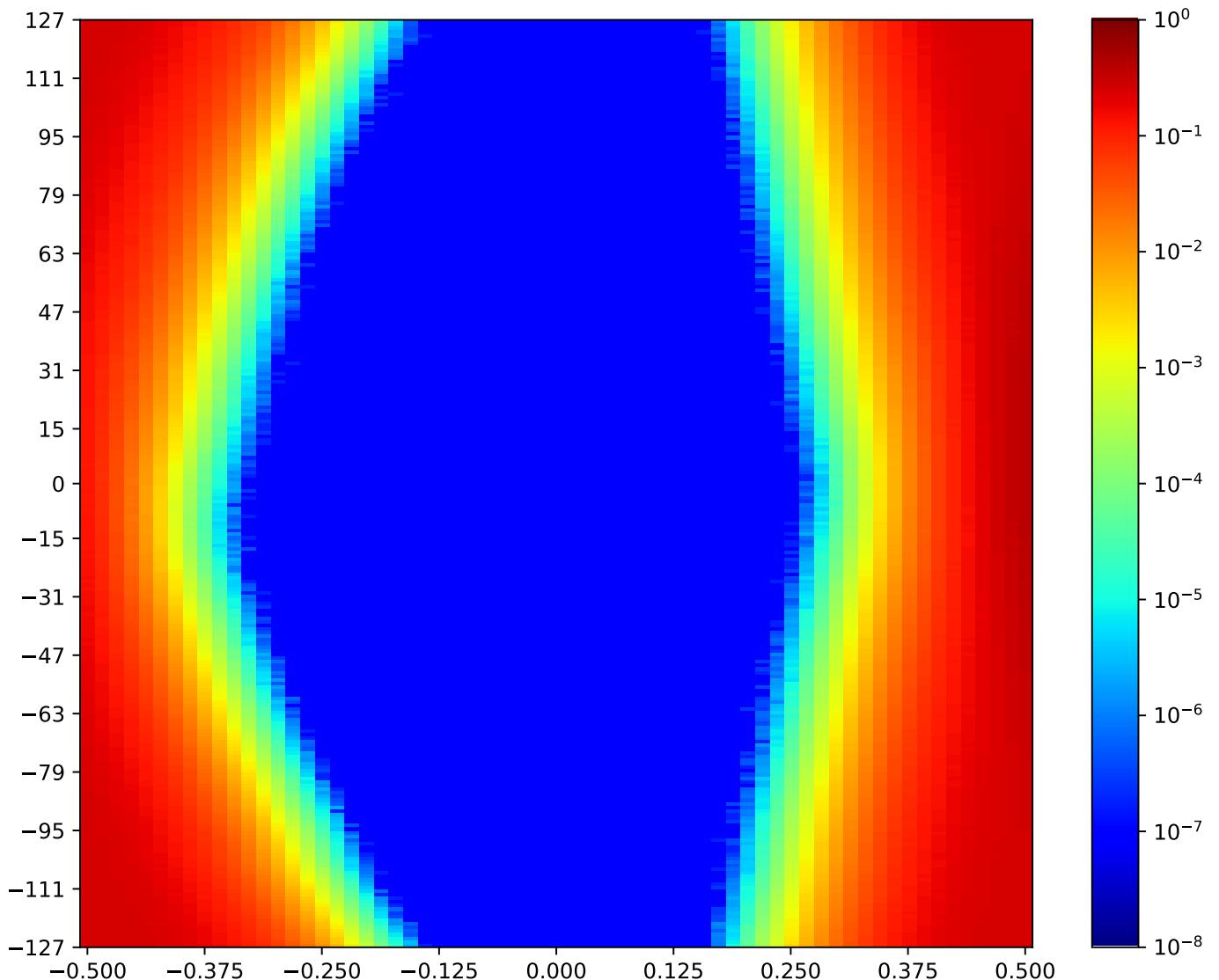


Figure 2.213: MSP\_A\_FPGA-TX2-11-RX10-11-MSP\_C\_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17 MSP\_C TX3 MSP\_A RX2 Minipod Loopback

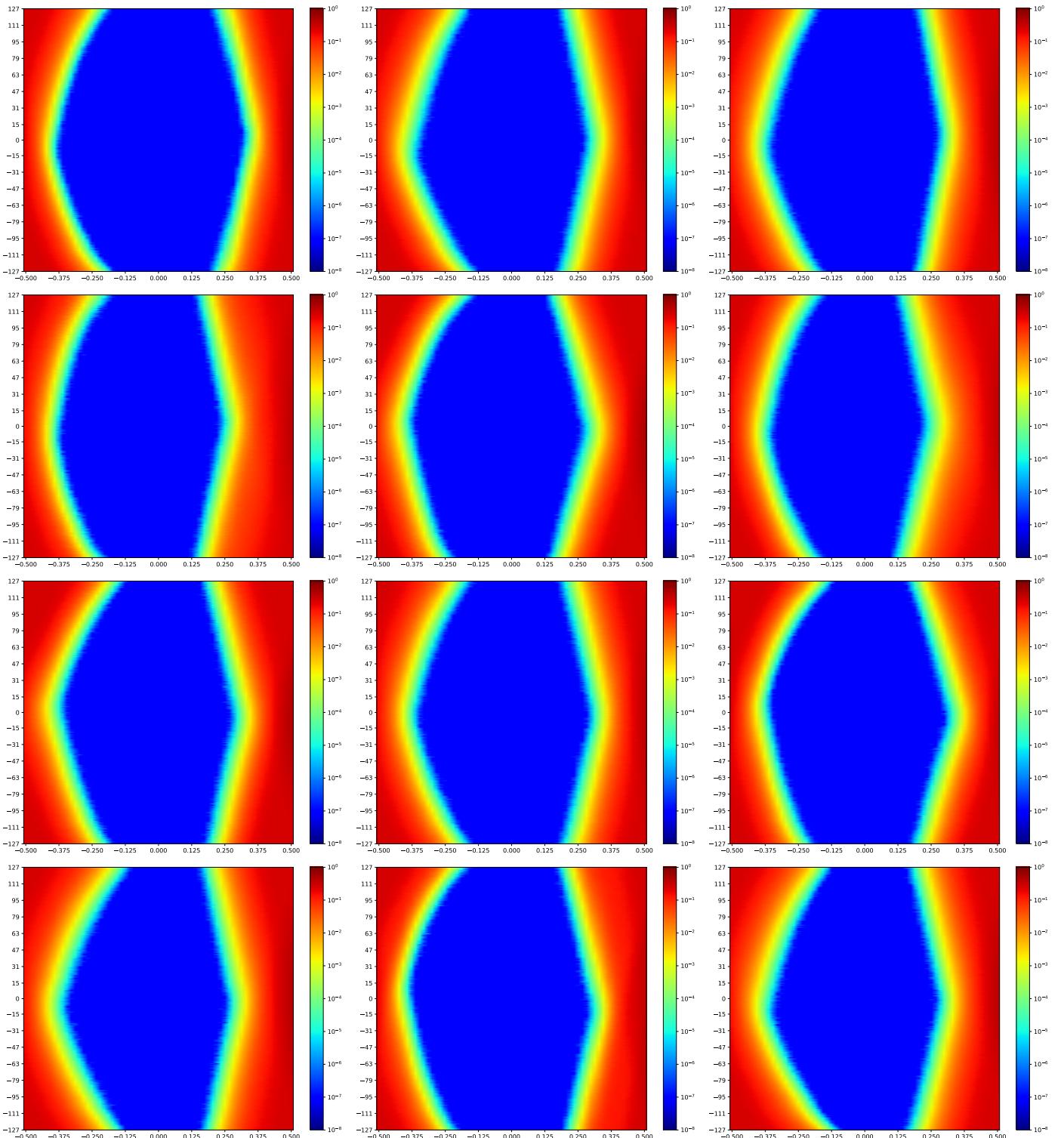


Figure 2.214: MSP\_C TX3 MSP\_A RX2 Minipod Loopback

A cross-reference to Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.227.

### 2.17.1 MSP\_C\_FPGA-TX3-00-RX2-00-MSP\_A\_FPGA

Table 2.198: MSP\_C\_FPGA-TX3-00-RX2-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:40:27		2018-Jan-24 21:40:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8878	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

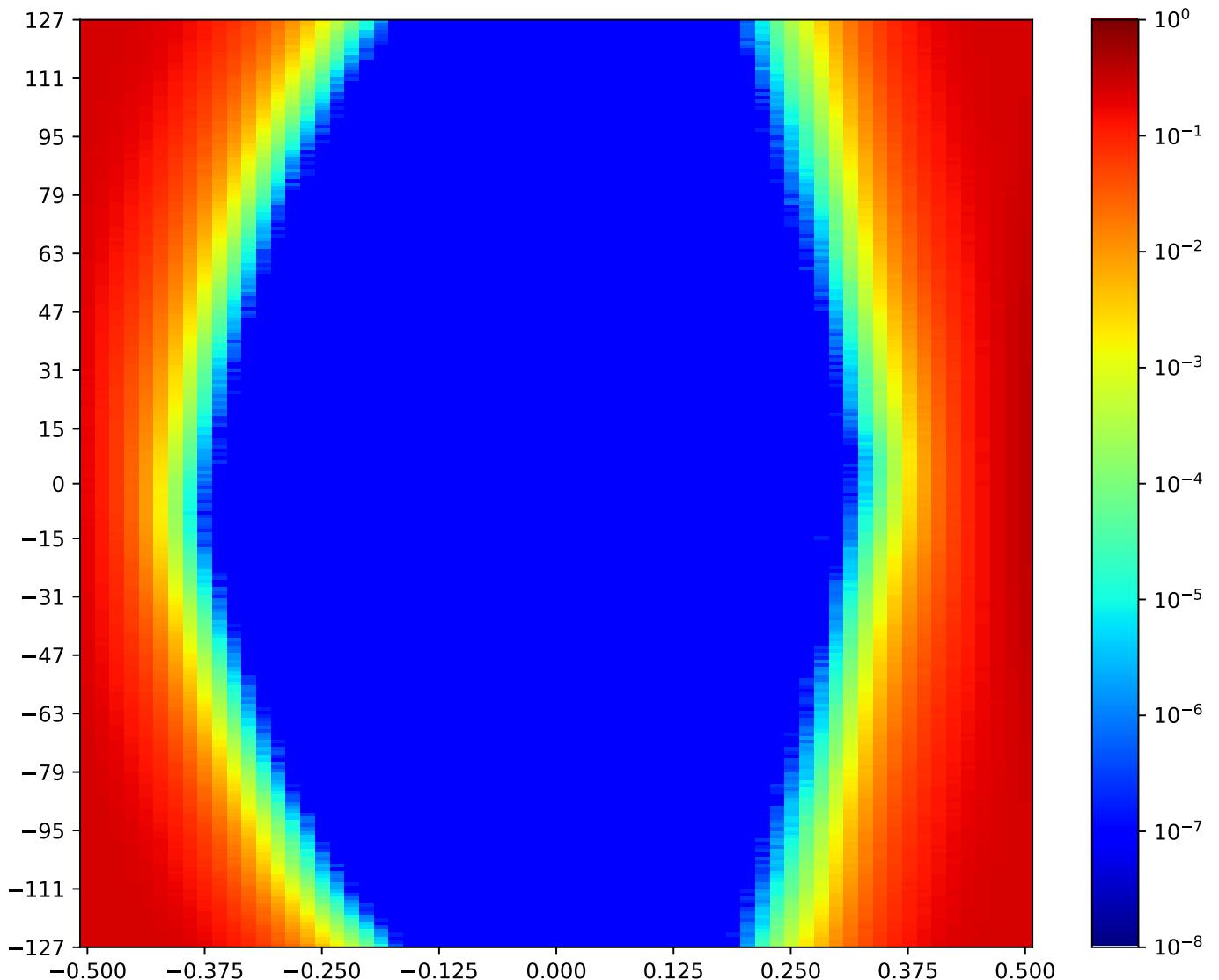


Figure 2.215: MSP\_C\_FPGA-TX3-00-RX2-00-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.2 MSP\_C\_FPGA-TX3-01-RX2-01-MSP\_A\_FPGA

Table 2.199: MSP\_C\_FPGA-TX3-01-RX2-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:41:30		2018-Jan-24 21:41:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7520	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

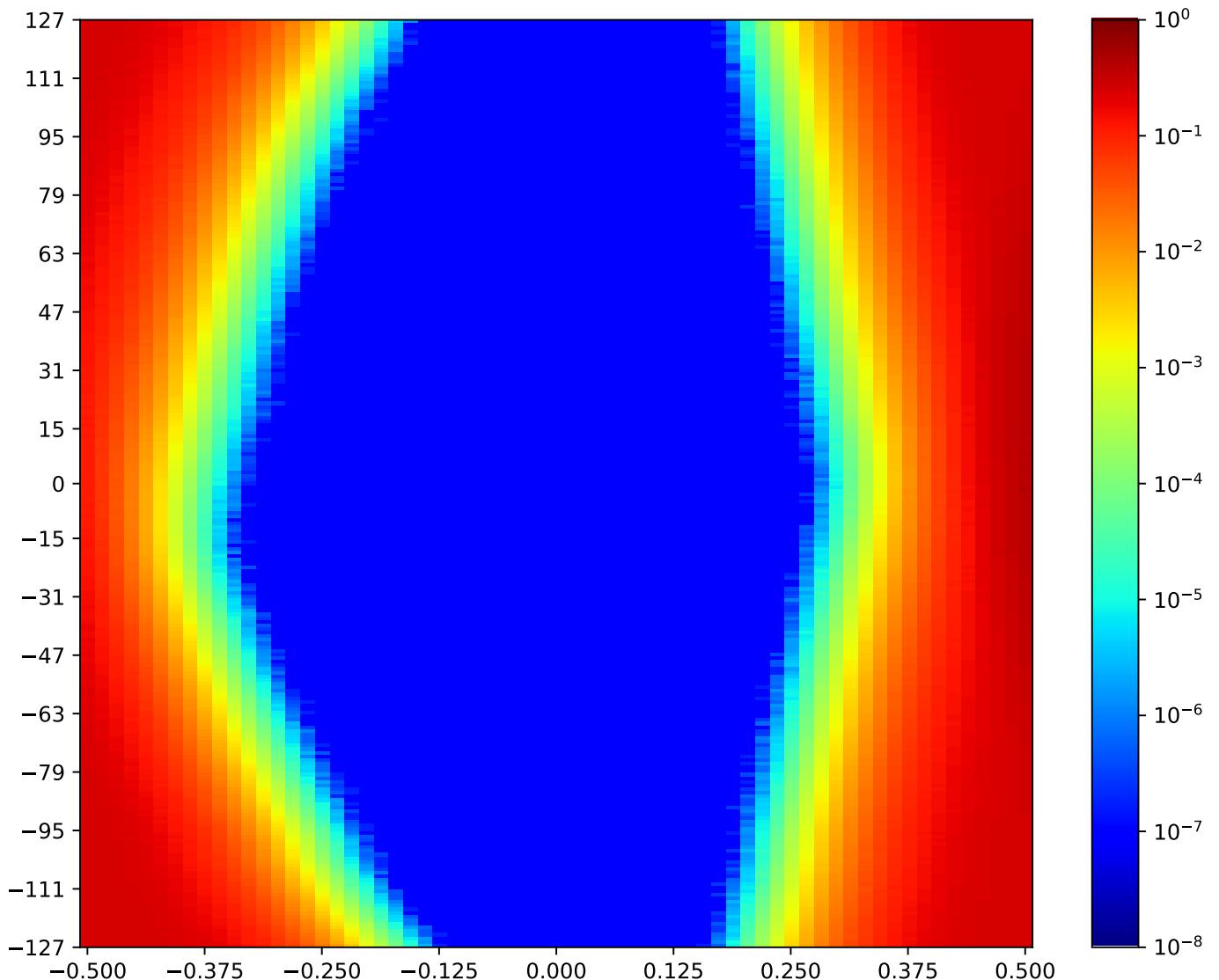


Figure 2.216: MSP\_C\_FPGA-TX3-01-RX2-01-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.17.3 MSP\_C\_FPGA-TX3-02-RX2-02-MSP\_A\_FPGA

Table 2.200: MSP\_C\_FPGA-TX3-02-RX2-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:42:00		2018-Jan-24 21:42:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7817	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

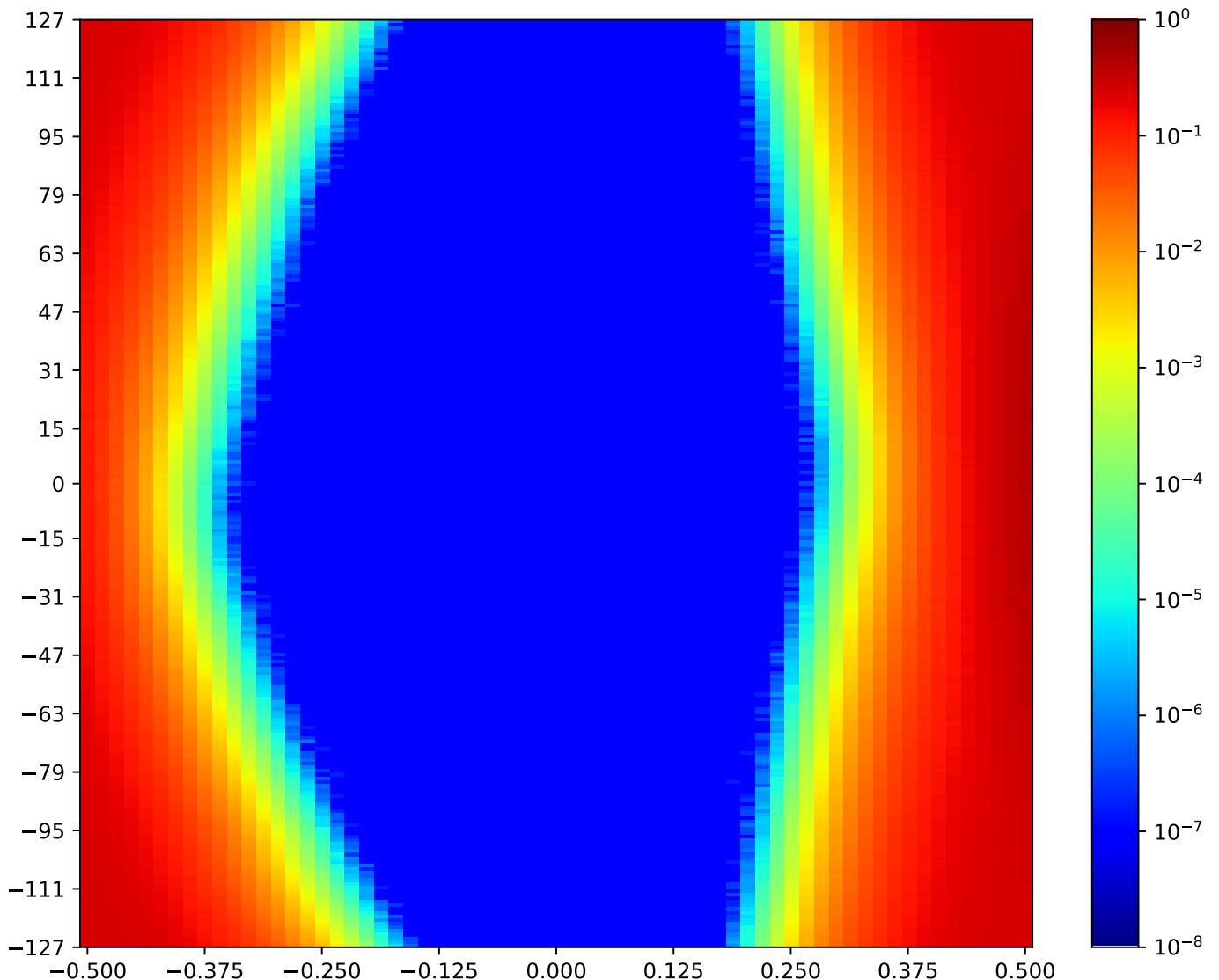


Figure 2.217: MSP\_C\_FPGA-TX3-02-RX2-02-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.4 MSP\_C\_FPGA-TX3-03-RX2-03-MSP\_A\_FPGA

Table 2.201: MSP\_C\_FPGA-TX3-03-RX2-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:39:27		2018-Jan-24 21:39:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7563	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

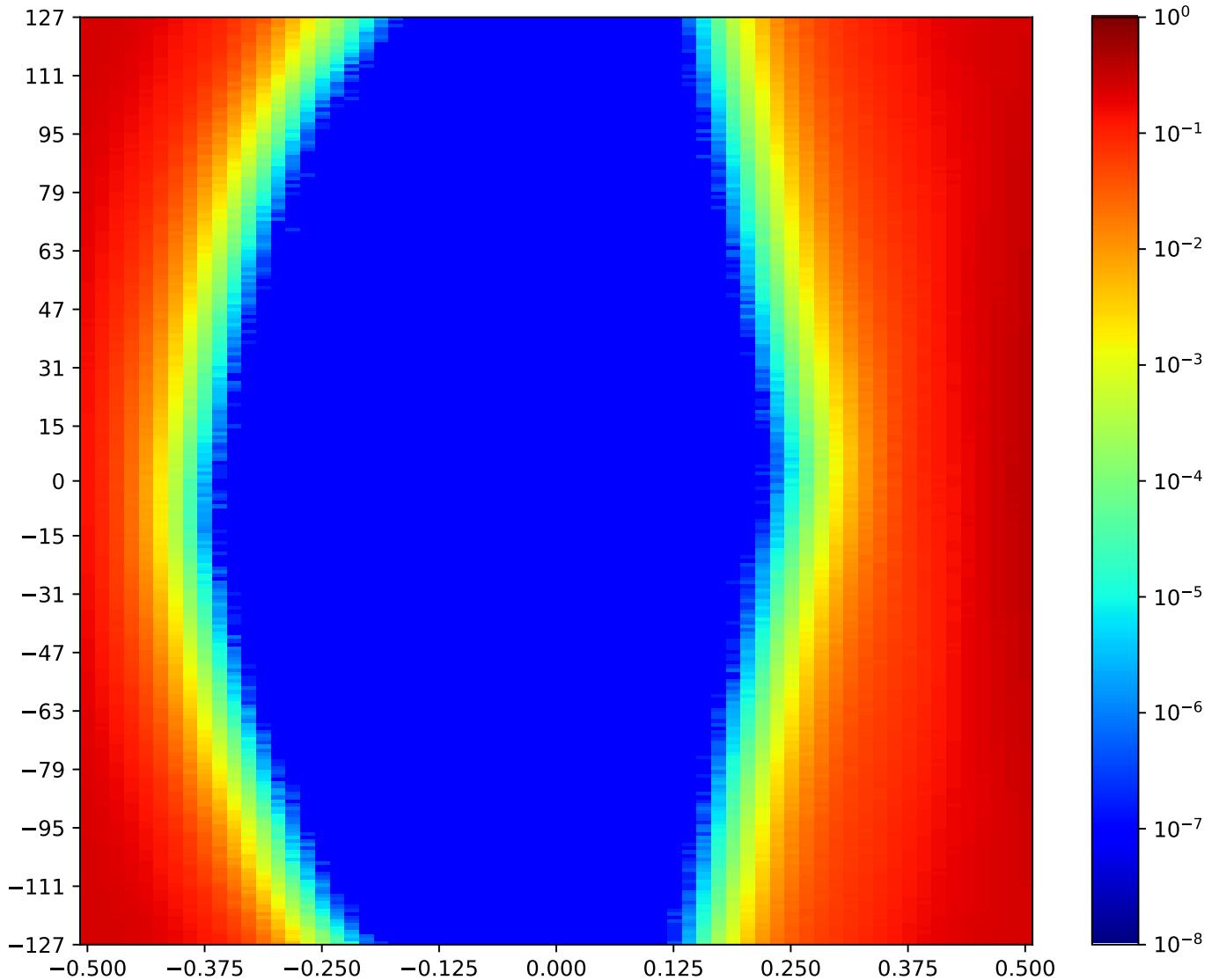


Figure 2.218: MSP\_C\_FPGA-TX3-03-RX2-03-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.5 MSP\_C\_FPGA-TX3-04-RX2-04-MSP\_A\_FPGA

Table 2.202: MSP\_C\_FPGA-TX3-04-RX2-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:43:28		2018-Jan-24 21:44:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7720	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

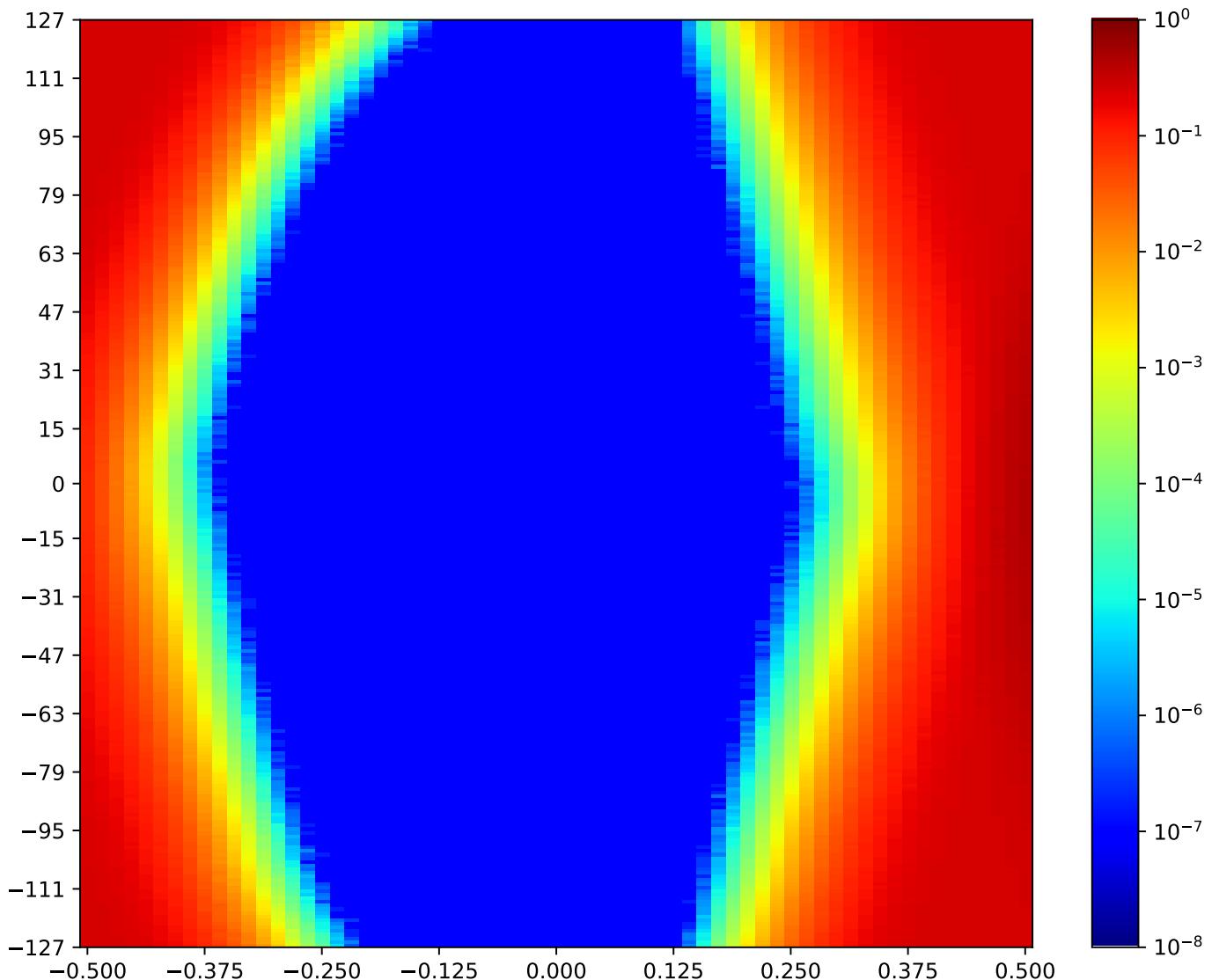


Figure 2.219: MSP\_C\_FPGA-TX3-04-RX2-04-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.6 MSP\_C\_FPGA-TX3-05-RX2-05-MSP\_A\_FPGA

Table 2.203: MSP\_C\_FPGA-TX3-05-RX2-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:38:57		2018-Jan-24 21:39:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6636	34	52.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

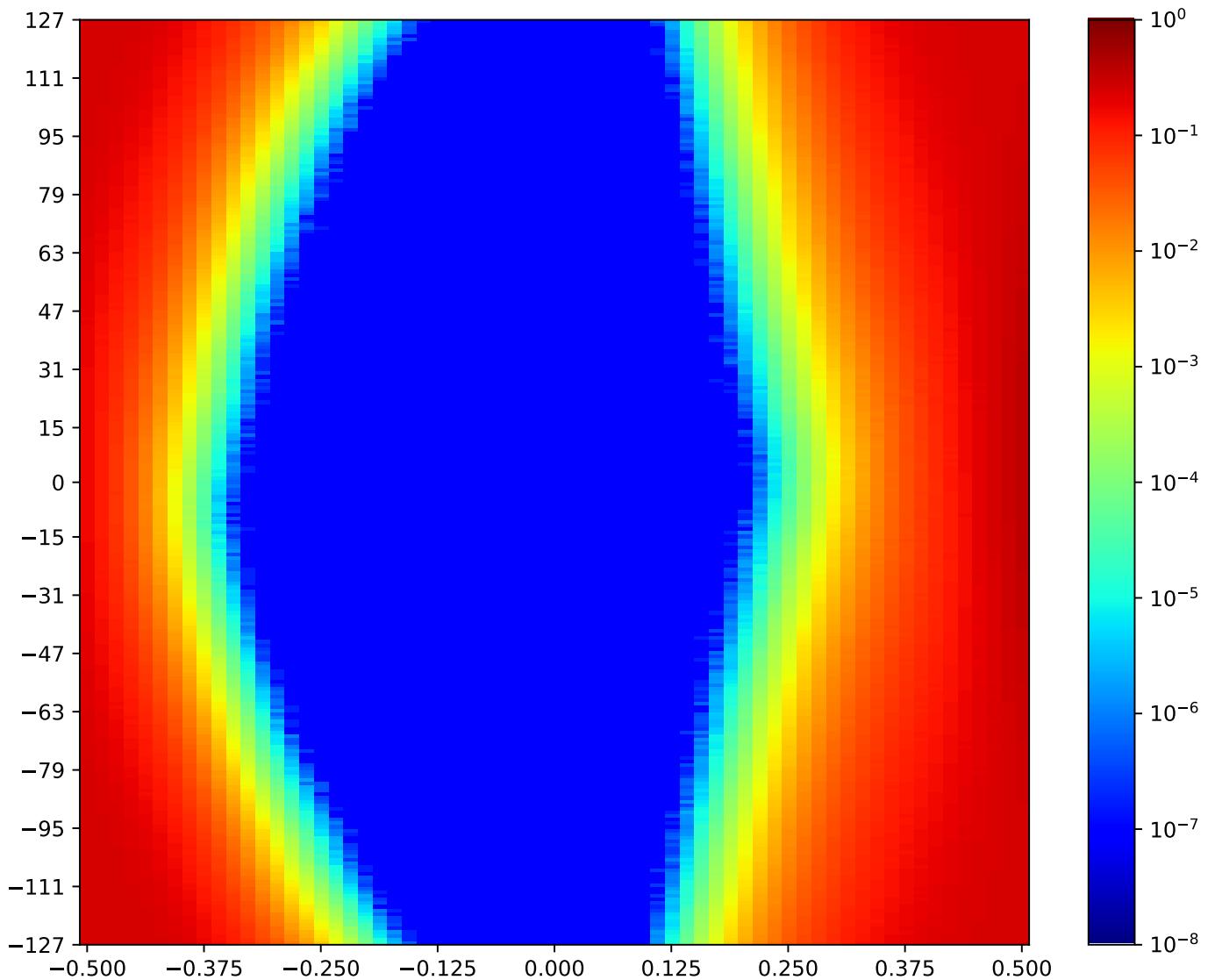


Figure 2.220: MSP\_C\_FPGA-TX3-05-RX2-05-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.7 MSP\_C\_FPGA-TX3-06-RX2-06-MSP\_A\_FPGA

Table 2.204: MSP\_C\_FPGA-TX3-06-RX2-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:44:31		2018-Jan-24 21:45:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7681	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

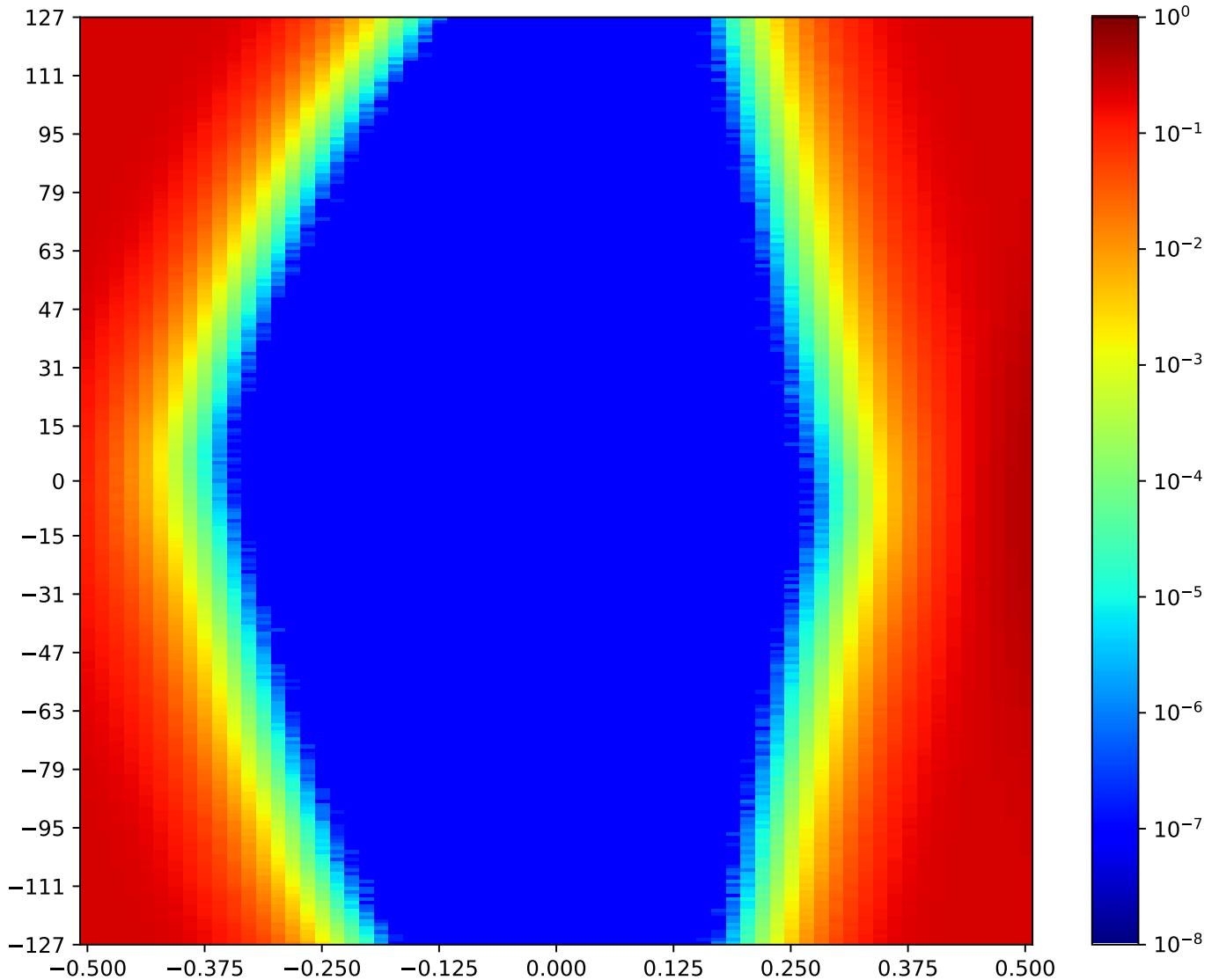


Figure 2.221: MSP\_C\_FPGA-TX3-06-RX2-06-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.8 MSP\_C\_FPGA-TX3-07-RX2-07-MSP\_A\_FPGA

Table 2.205: MSP\_C\_FPGA-TX3-07-RX2-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:39:56		2018-Jan-24 21:40:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7809	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

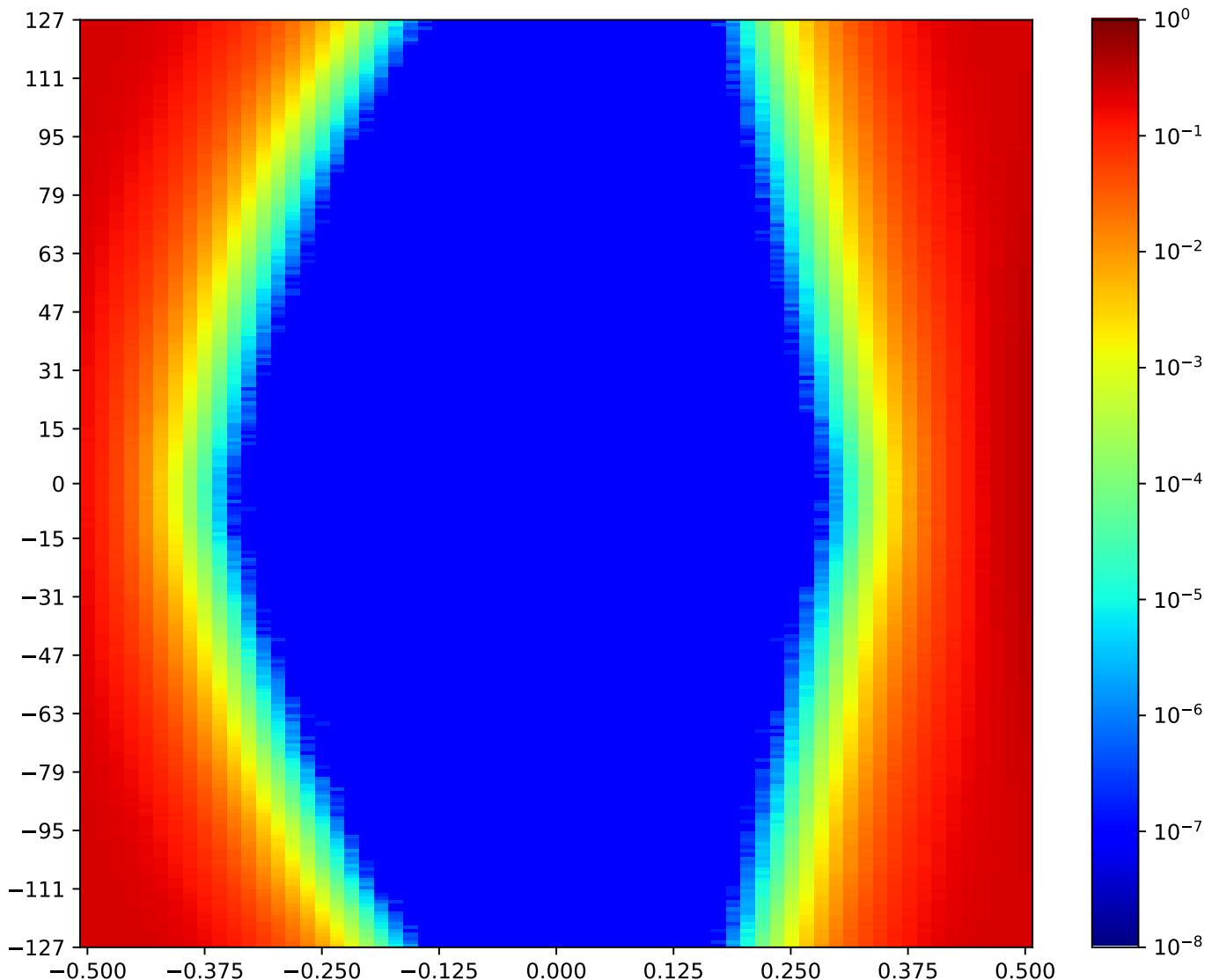


Figure 2.222: MSP\_C\_FPGA-TX3-07-RX2-07-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.9 MSP\_C\_FPGA-TX3-08-RX2-08-MSP\_A\_FPGA

Table 2.206: MSP\_C\_FPGA-TX3-08-RX2-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:44:01		2018-Jan-24 21:44:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8000	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

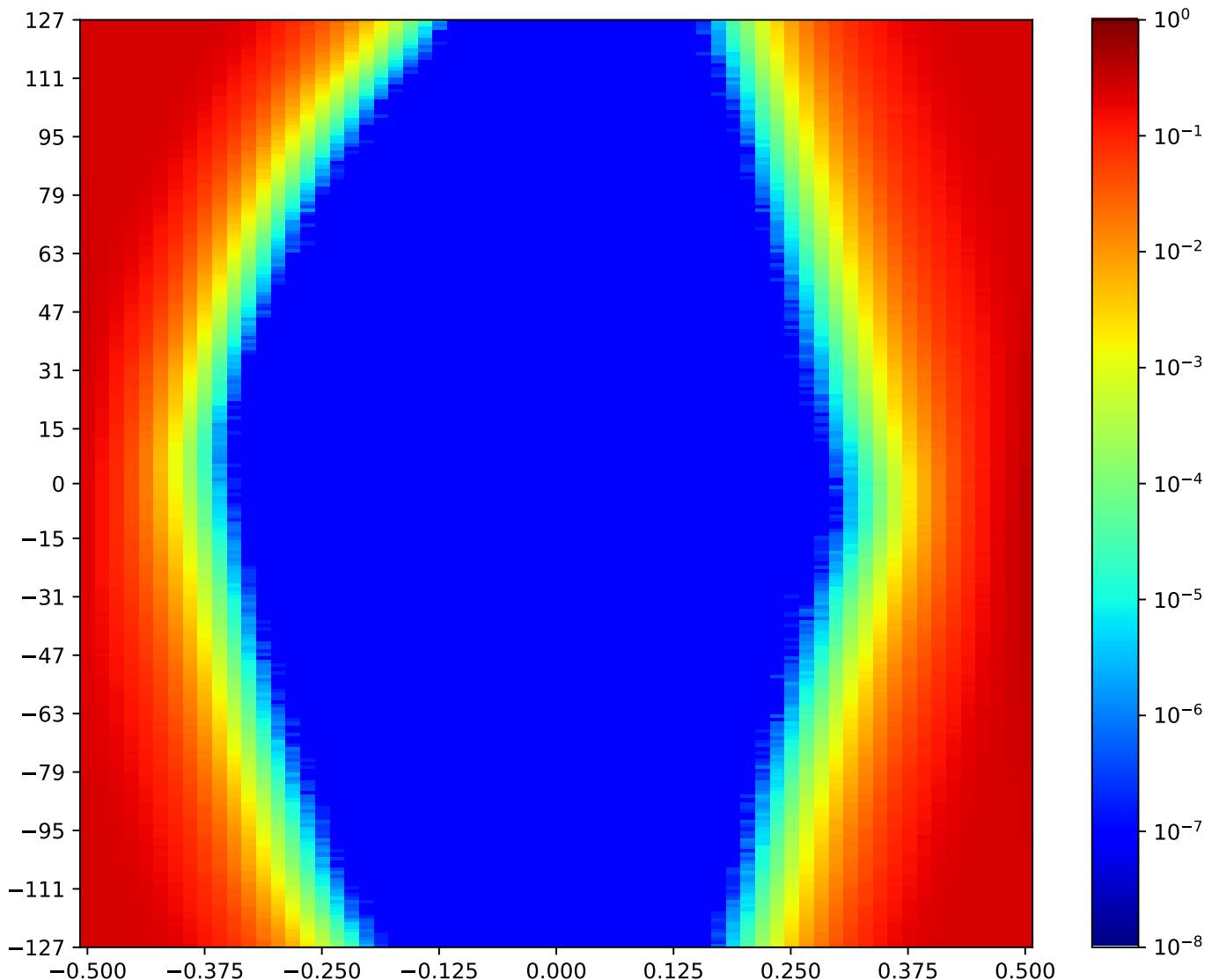


Figure 2.223: MSP\_C\_FPGA-TX3-08-RX2-08-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.10 MSP\_C\_FPGA-TX3-09-RX2-09-MSP\_A\_FPGA

Table 2.207: MSP\_C\_FPGA-TX3-09-RX2-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:40:57		2018-Jan-24 21:41:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7046	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

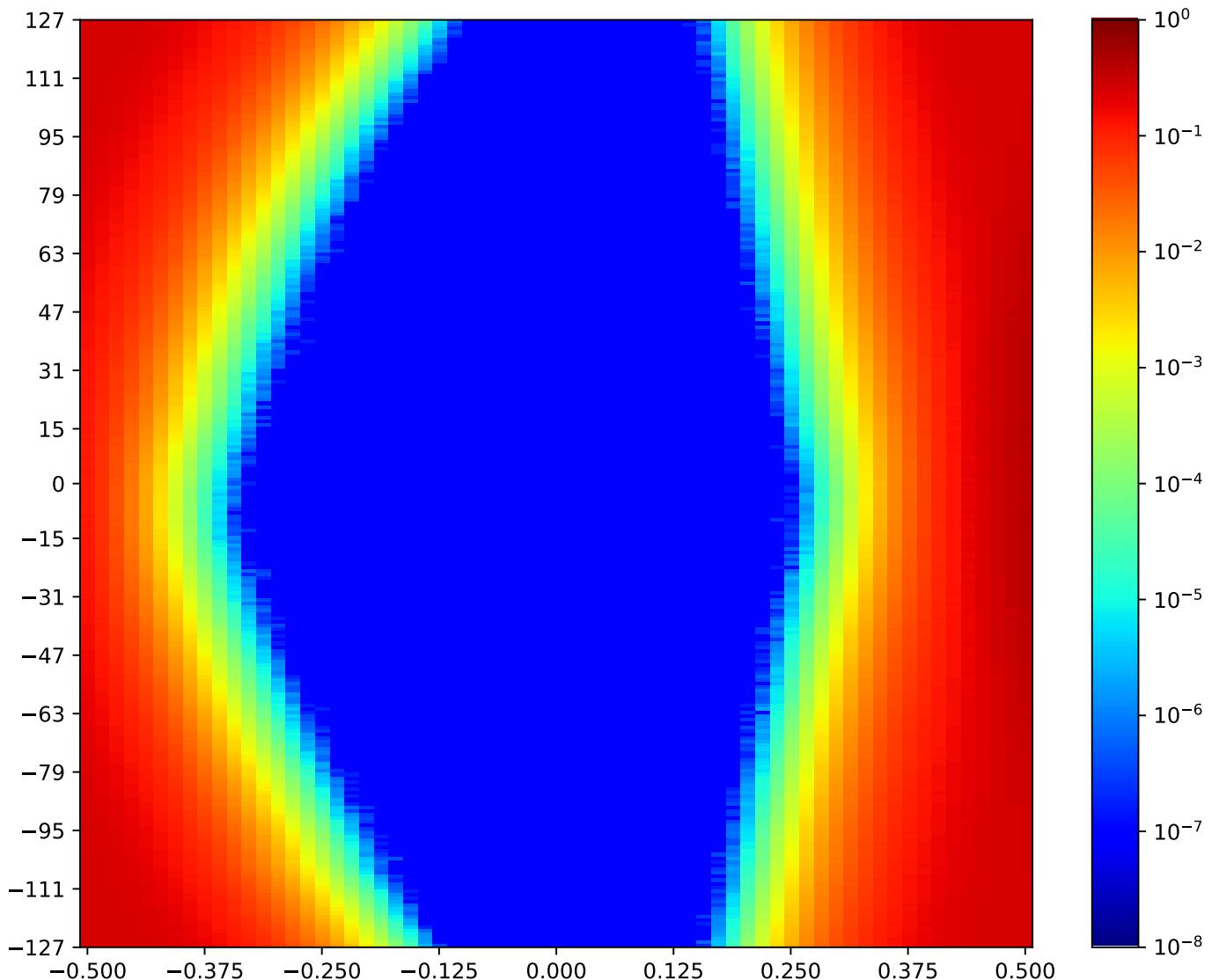


Figure 2.224: MSP\_C\_FPGA-TX3-09-RX2-09-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.11 MSP\_C\_FPGA-TX3-10-RX2-10-MSP\_A\_FPGA

Table 2.208: MSP\_C\_FPGA-TX3-10-RX2-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:42:59		2018-Jan-24 21:43:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8412	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

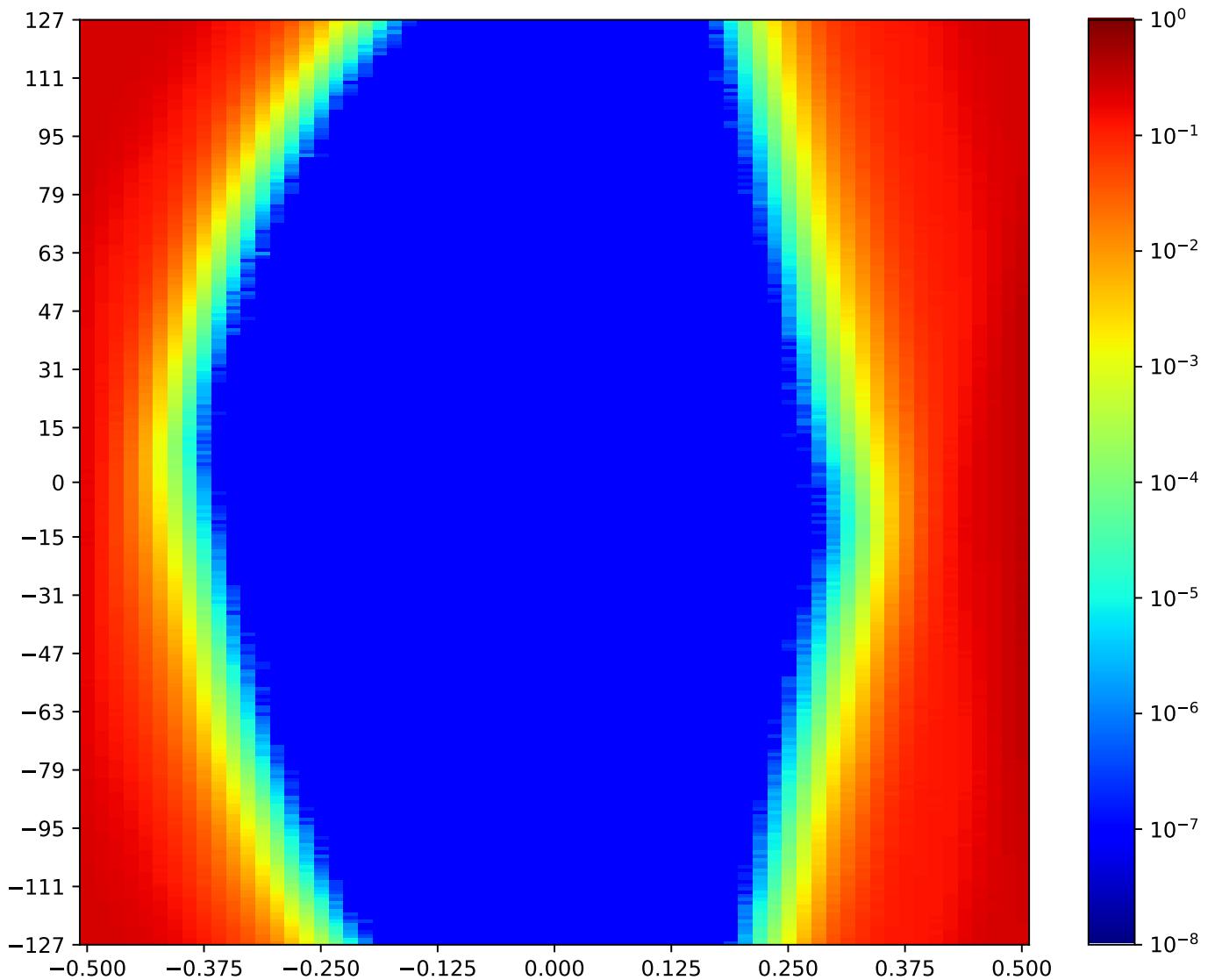


Figure 2.225: MSP\_C\_FPGA-TX3-10-RX2-10-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.17.12 MSP\_C\_FPGA-TX3-11-RX2-11-MSP\_A\_FPGA

Table 2.209: MSP\_C\_FPGA-TX3-11-RX2-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:42:30		2018-Jan-24 21:42:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7187	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

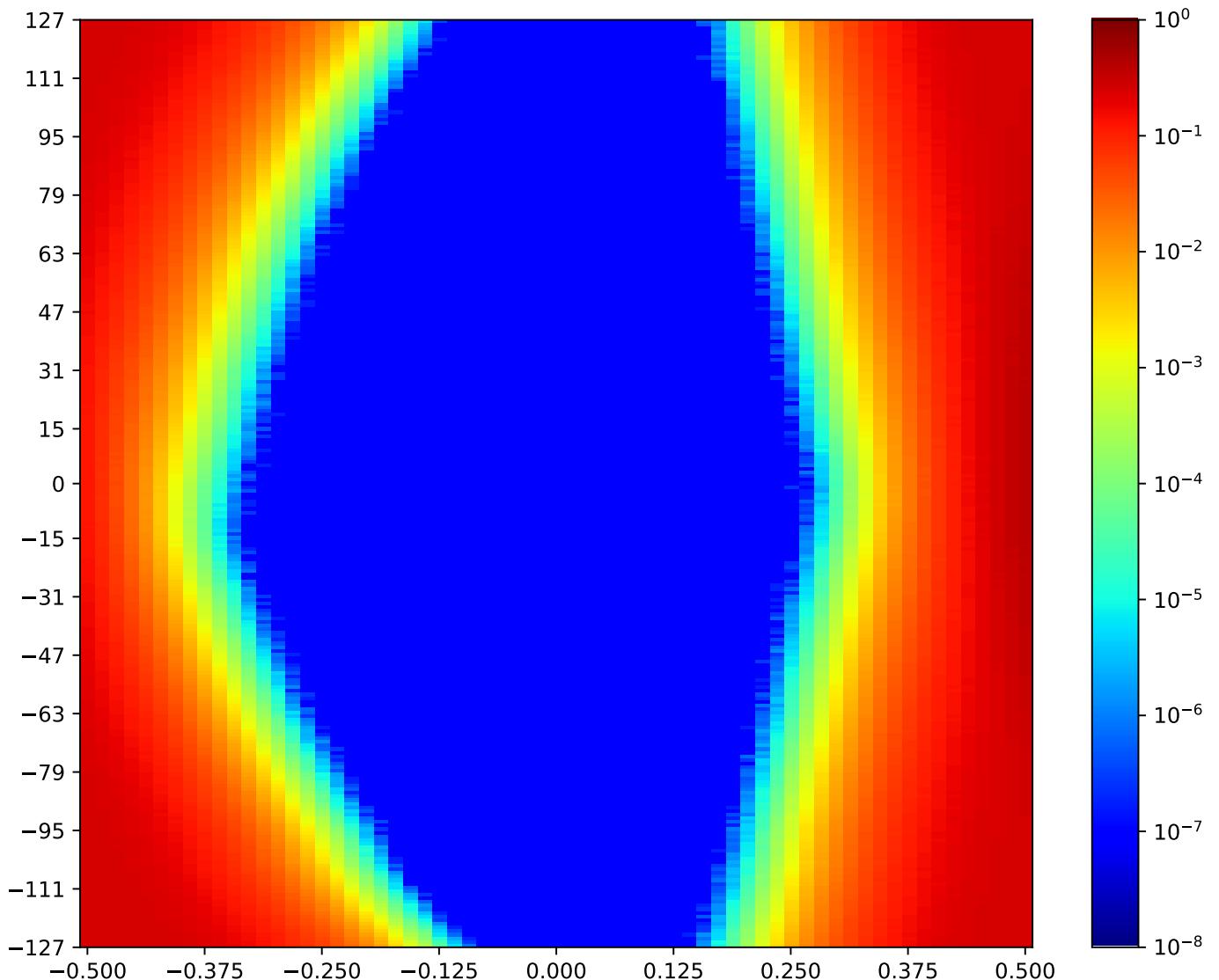


Figure 2.226: MSP\_C\_FPGA-TX3-11-RX2-11-MSP\_A\_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18 MSP\_C TX4 MSP\_A RX1 Minipod Loopback

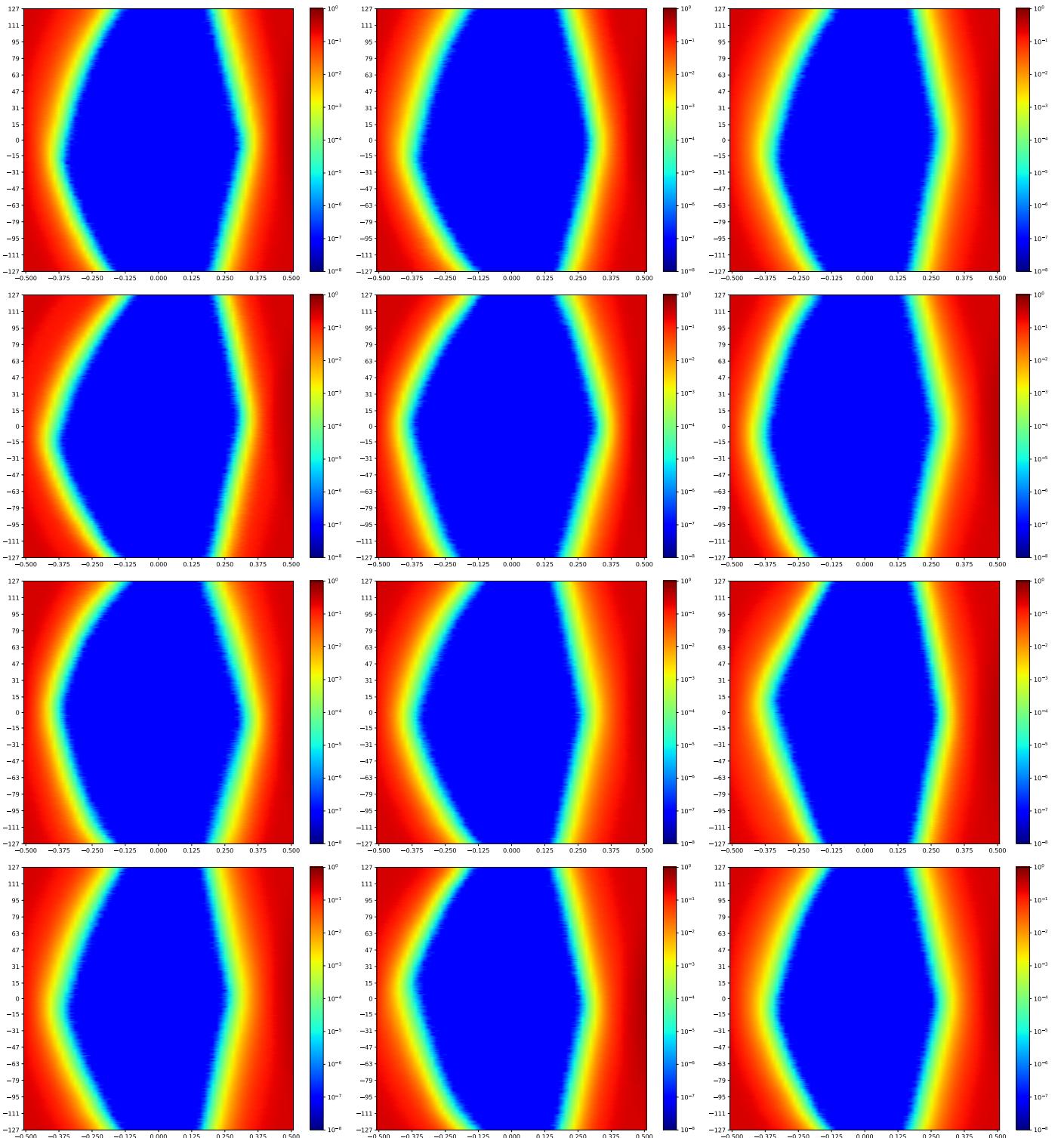


Figure 2.227: MSP\_C TX4 MSP\_A RX1 Minipod Loopback

A cross-reference to Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.240.

### 2.18.1 MSP\_C\_FPGA-TX4-00-RX1-00-MSP\_A\_FPGA

Table 2.210: MSP\_C\_FPGA-TX4-00-RX1-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:46:30		2018-Jan-24 21:46:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7944	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

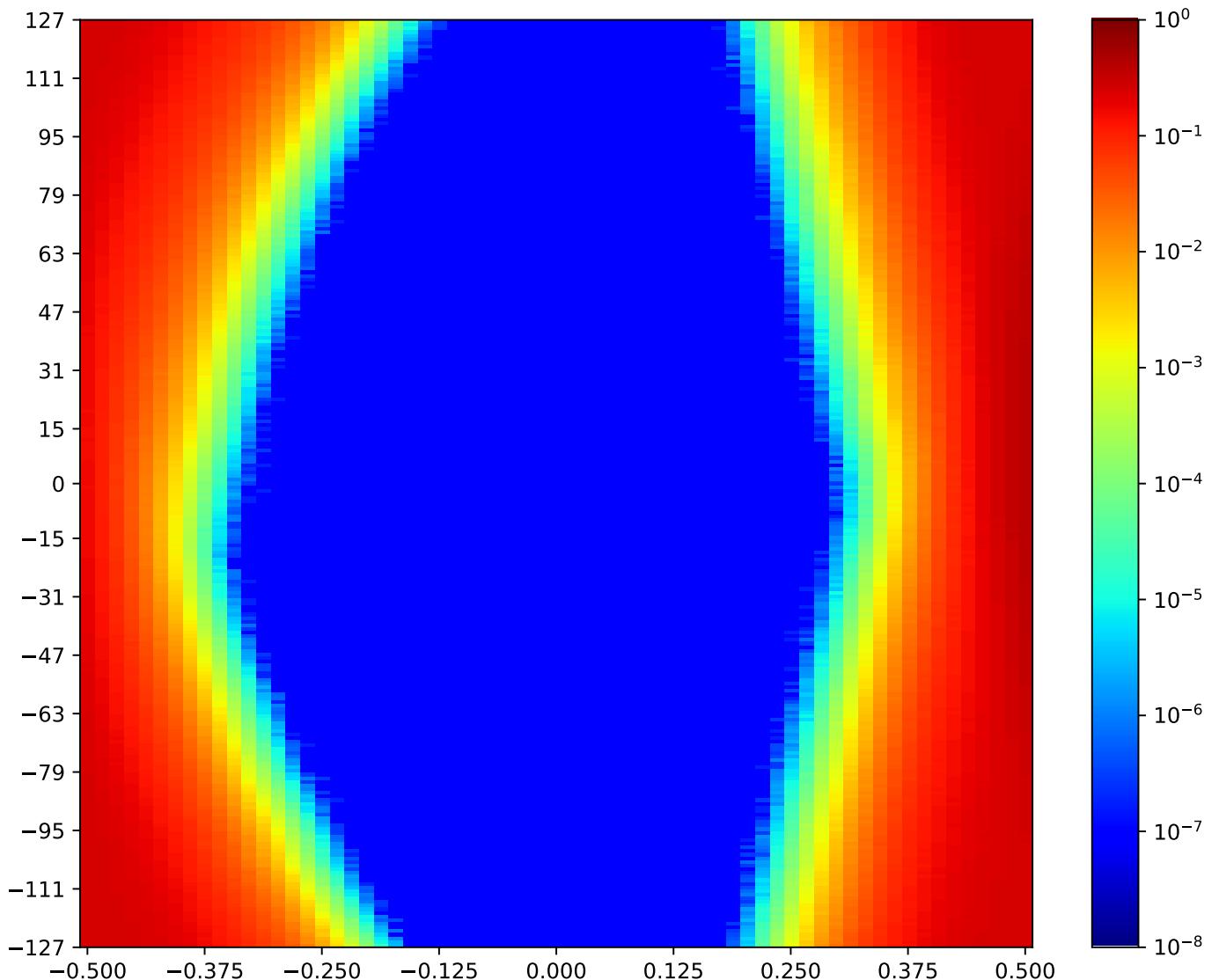


Figure 2.228: MSP\_C\_FPGA-TX4-00-RX1-00-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.2 MSP\_C\_FPGA-TX4-01-RX1-01-MSP\_A\_FPGA

Table 2.211: MSP\_C\_FPGA-TX4-01-RX1-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:45:30		2018-Jan-24 21:45:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7555	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

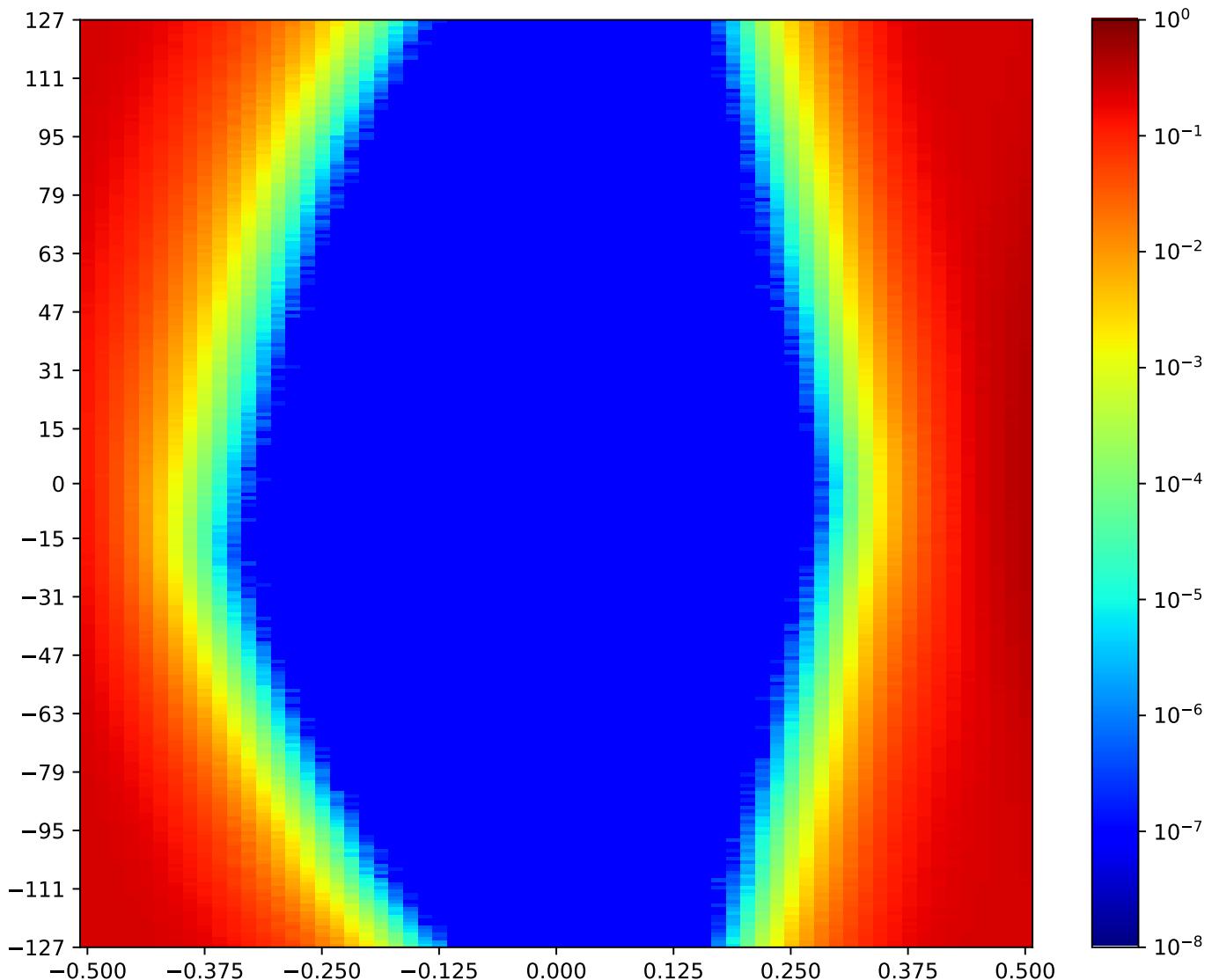


Figure 2.229: MSP\_C\_FPGA-TX4-01-RX1-01-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.18.3 MSP\_C\_FPGA-TX4-02-RX1-02-MSP\_A\_FPGA

Table 2.212: MSP\_C\_FPGA-TX4-02-RX1-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:47:59		2018-Jan-24 21:48:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6964	34	52.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

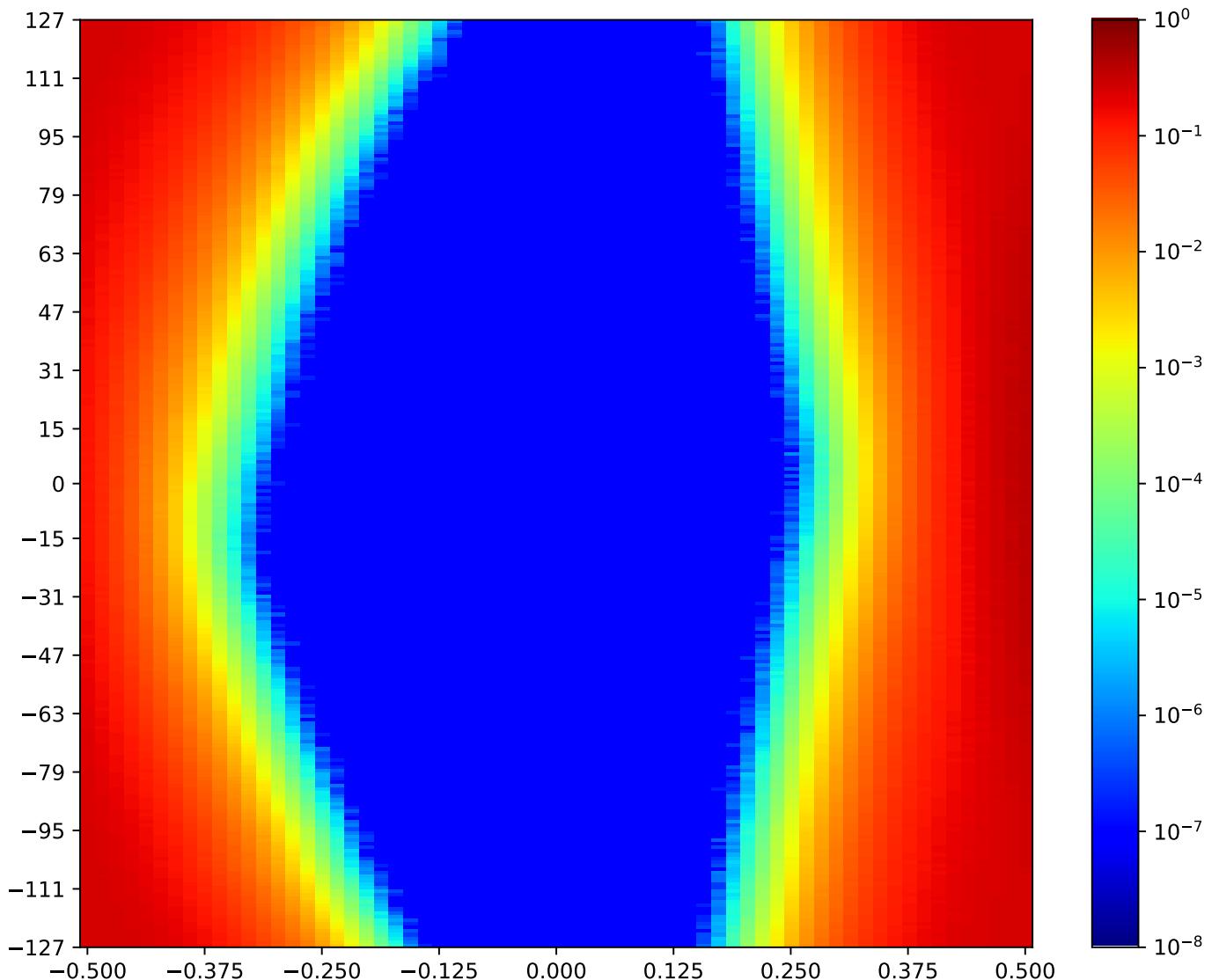


Figure 2.230: MSP\_C\_FPGA-TX4-02-RX1-02-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.4 MSP\_C\_FPGA-TX4-03-RX1-03-MSP\_A\_FPGA

Table 2.213: MSP\_C\_FPGA-TX4-03-RX1-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:45:00		2018-Jan-24 21:45:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7828	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

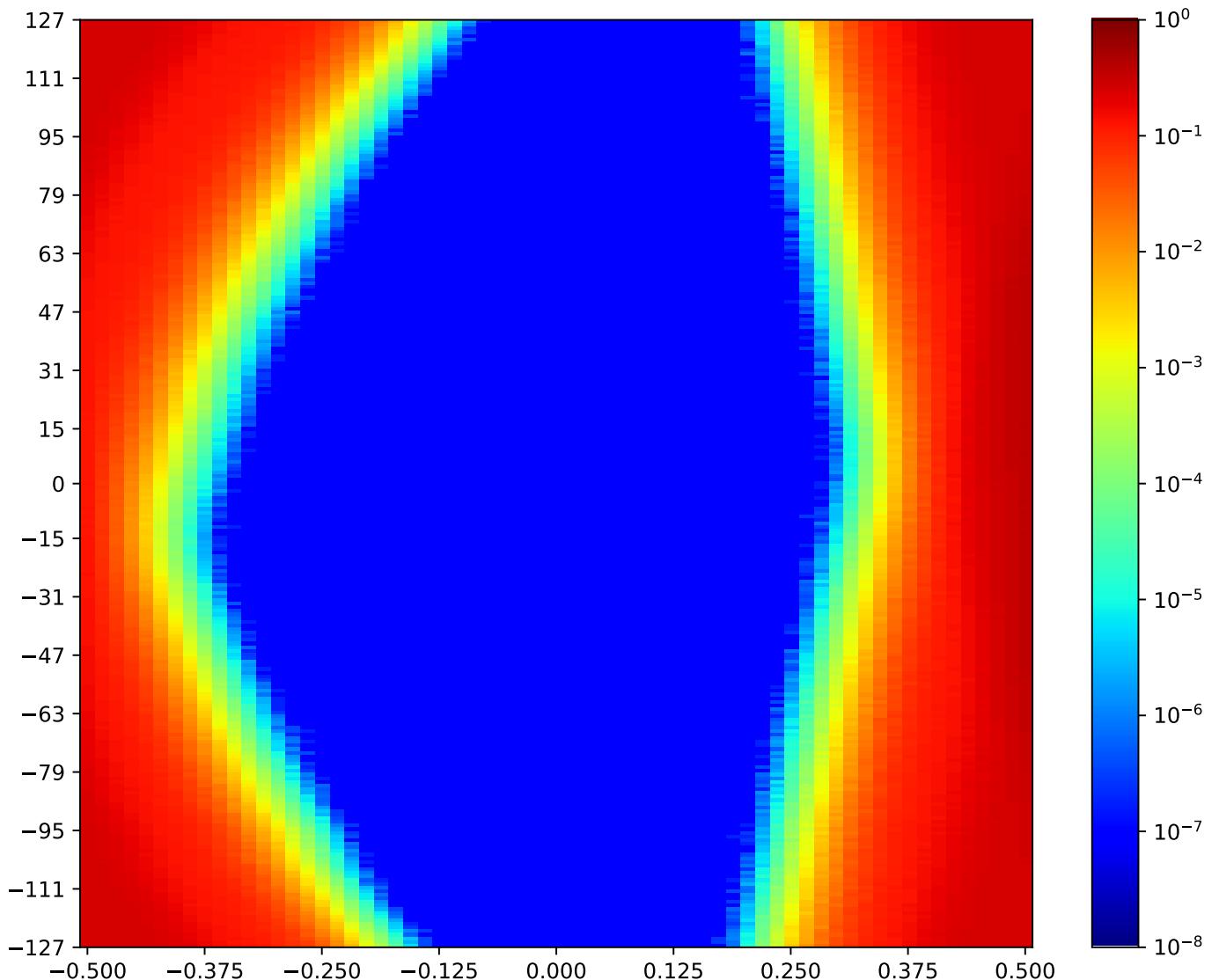


Figure 2.231: MSP\_C\_FPGA-TX4-03-RX1-03-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.5 MSP\_C\_FPGA-TX4-04-RX1-04-MSP\_A\_FPGA

Table 2.214: MSP\_C\_FPGA-TX4-04-RX1-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:49:27		2018-Jan-24 21:49:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7982	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

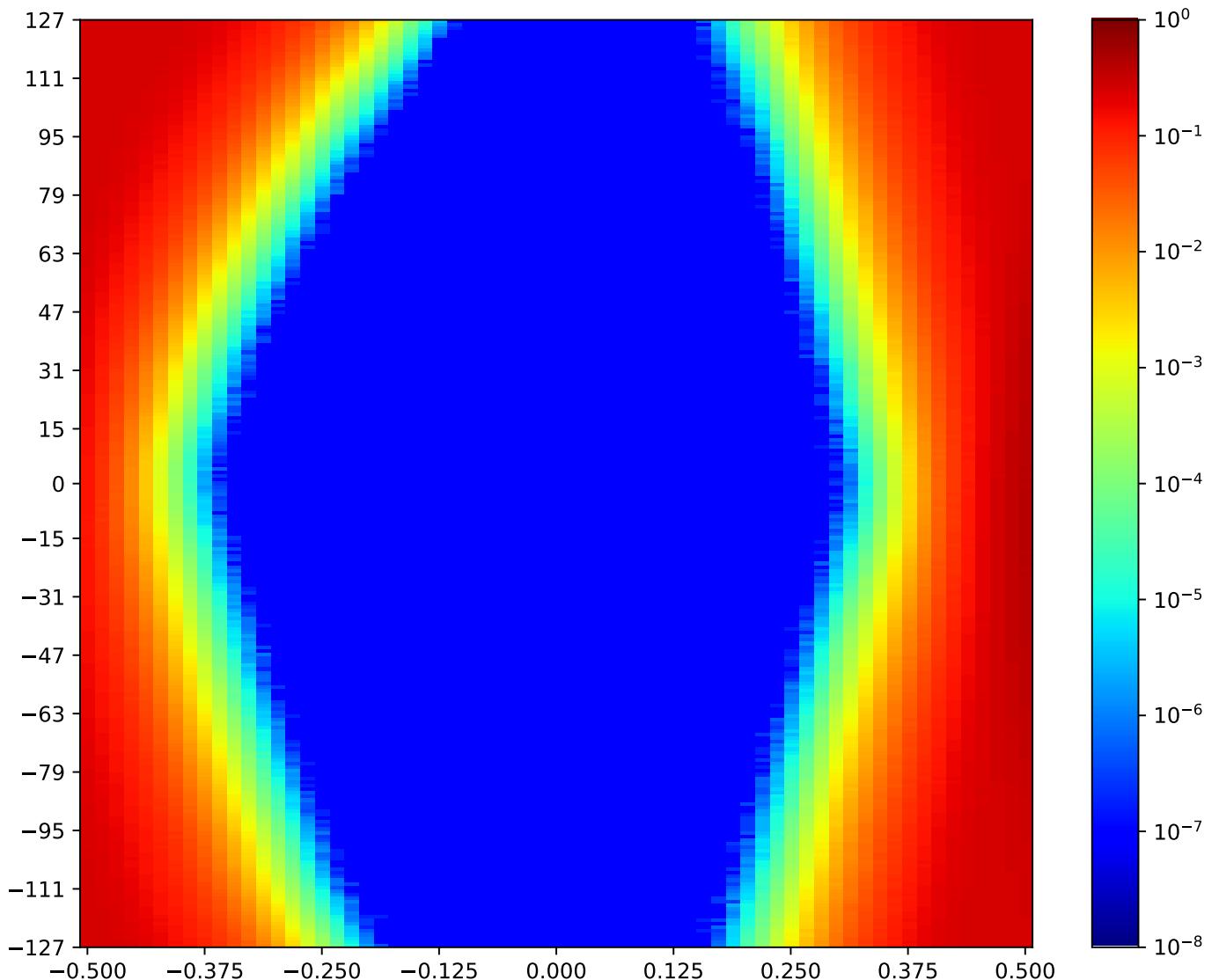


Figure 2.232: MSP\_C\_FPGA-TX4-04-RX1-04-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.6 MSP\_C\_FPGA-TX4-05-RX1-05-MSP\_A\_FPGA

Table 2.215: MSP\_C\_FPGA-TX4-05-RX1-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:46:00		2018-Jan-24 21:46:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7380	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

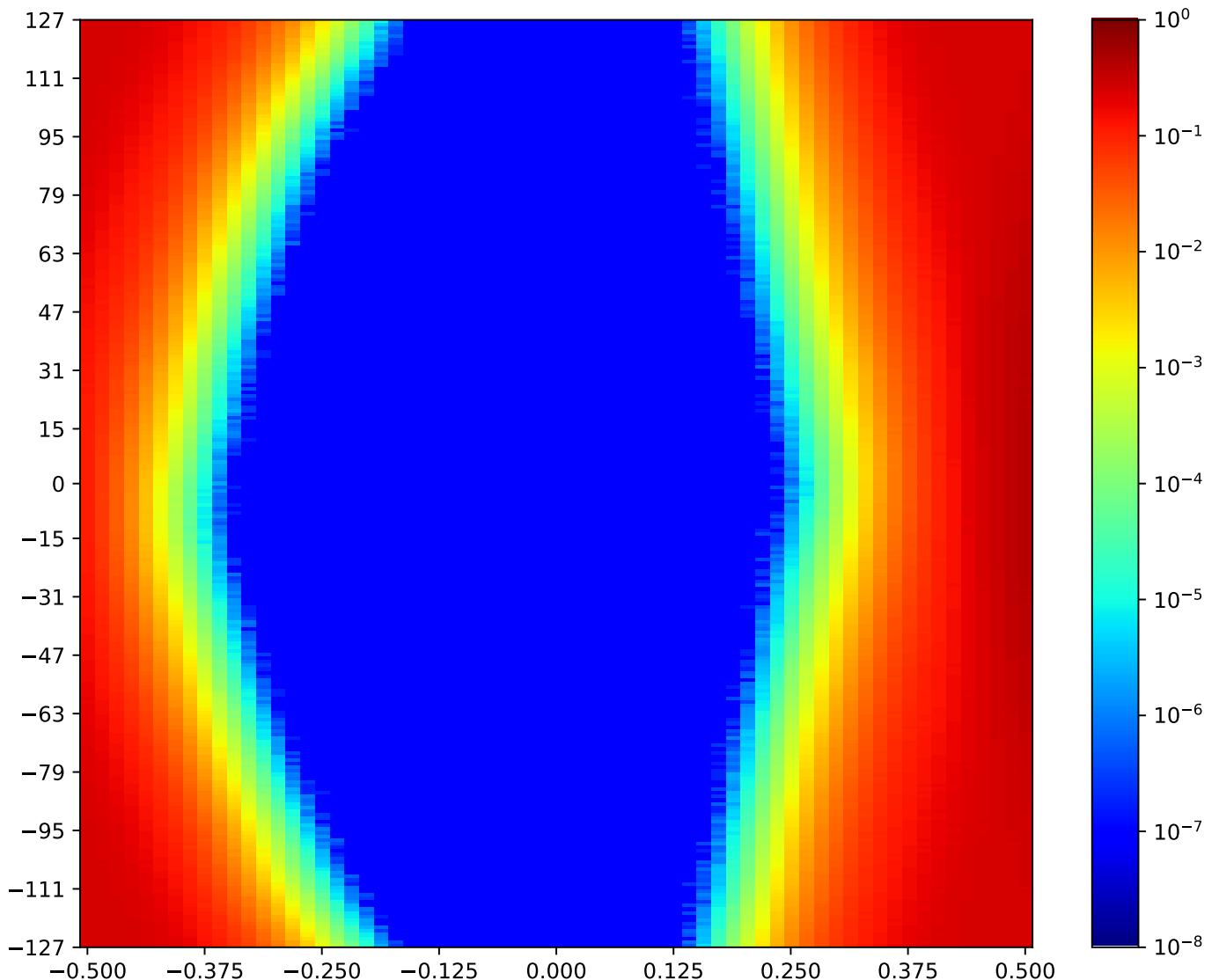


Figure 2.233: MSP\_C\_FPGA-TX4-05-RX1-05-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.7 MSP\_C\_FPGA-TX4-06-RX1-06-MSP\_A\_FPGA

Table 2.216: MSP\_C\_FPGA-TX4-06-RX1-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:50:27		2018-Jan-24 21:50:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7864	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

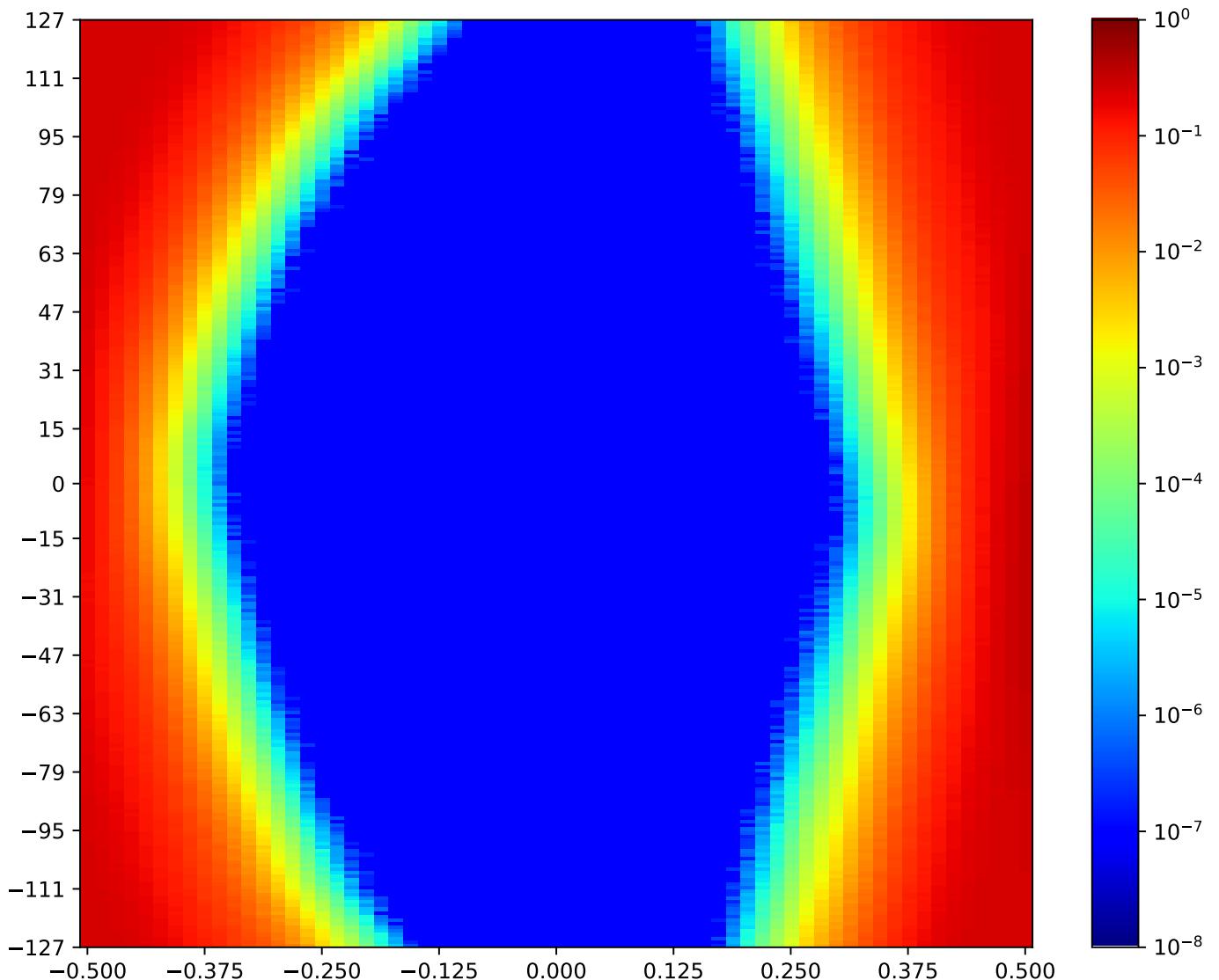


Figure 2.234: MSP\_C\_FPGA-TX4-06-RX1-06-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.8 MSP\_C\_FPGA-TX4-07-RX1-07-MSP\_A\_FPGA

Table 2.217: MSP\_C\_FPGA-TX4-07-RX1-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:46:59		2018-Jan-24 21:47:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6877	35	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

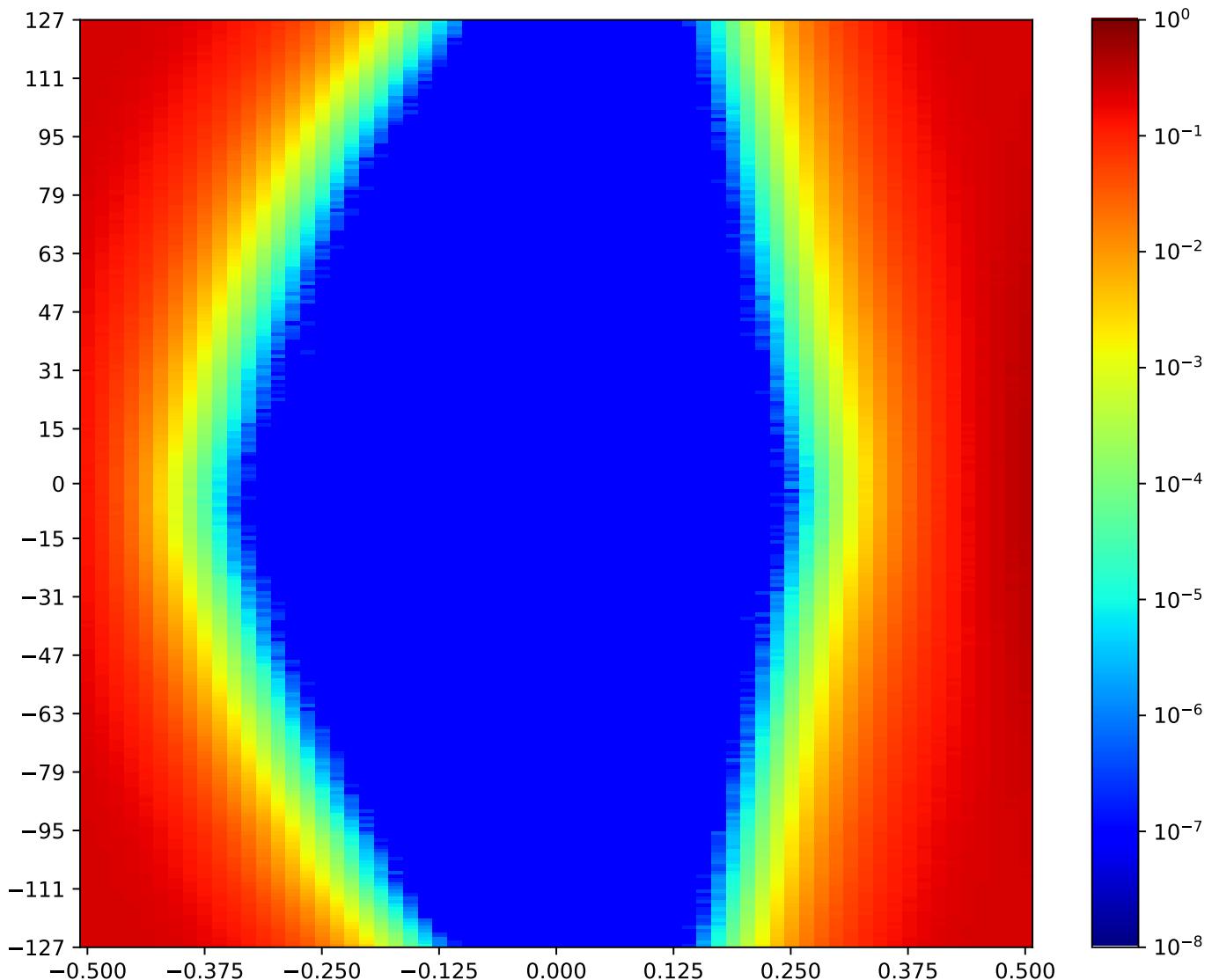


Figure 2.235: MSP\_C\_FPGA-TX4-07-RX1-07-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.9 MSP\_C\_FPGA-TX4-08-RX1-08-MSP\_A\_FPGA

Table 2.218: MSP\_C\_FPGA-TX4-08-RX1-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:49:57		2018-Jan-24 21:50:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7067	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

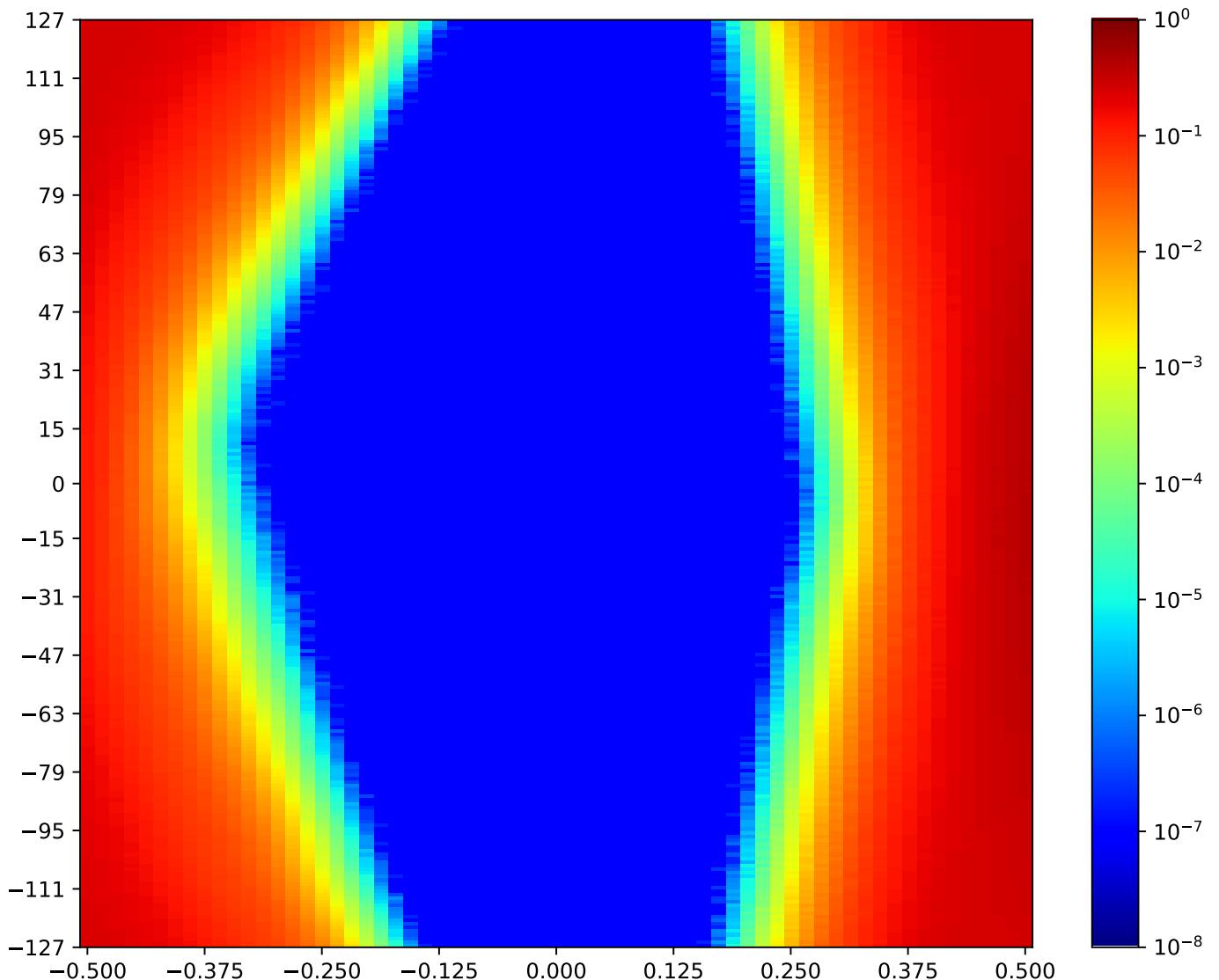


Figure 2.236: MSP\_C\_FPGA-TX4-08-RX1-08-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.10 MSP\_C\_FPGA-TX4-09-RX1-09-MSP\_A\_FPGA

Table 2.219: MSP\_C\_FPGA-TX4-09-RX1-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:47:29		2018-Jan-24 21:47:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6979	34	52.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

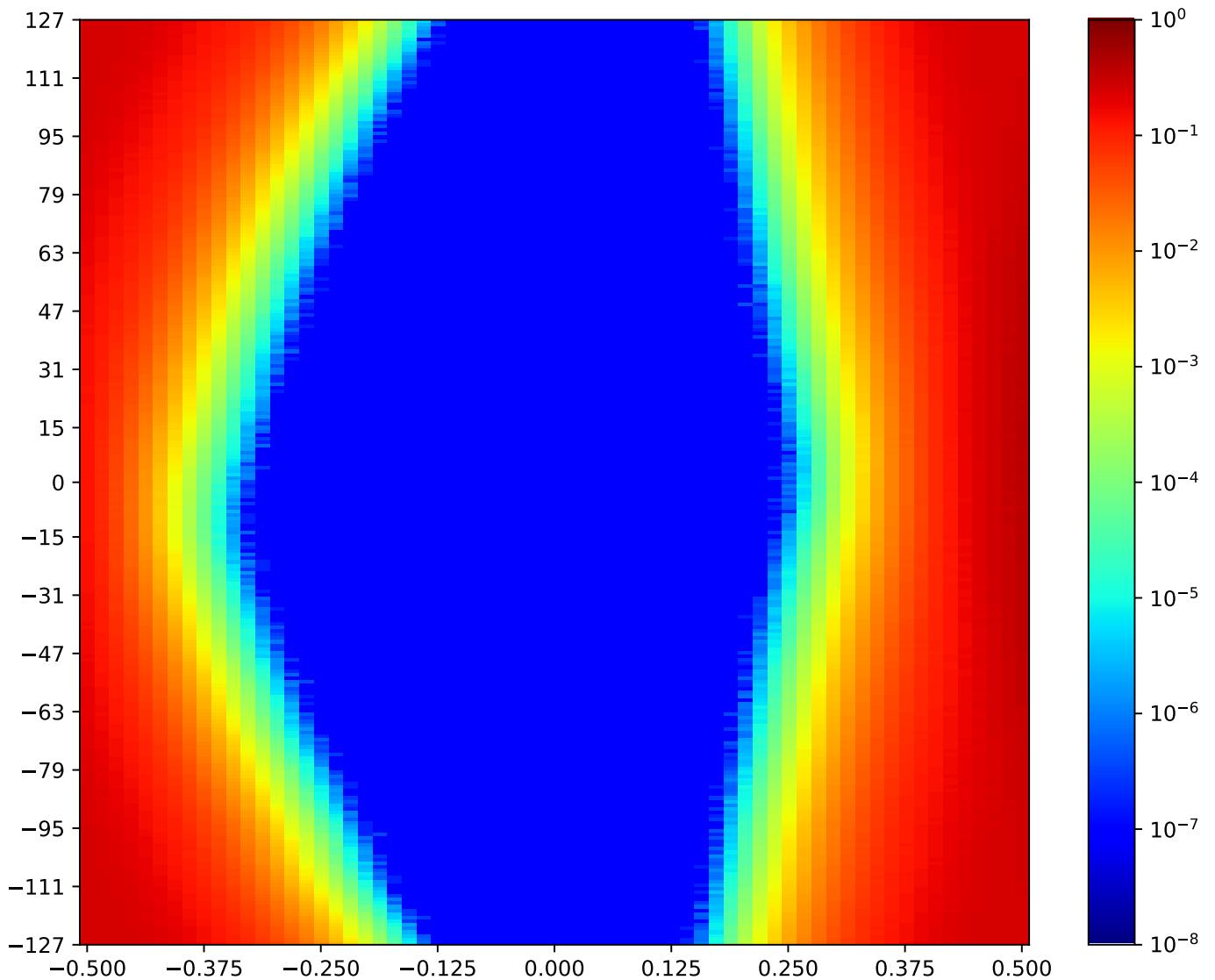


Figure 2.237: MSP\_C\_FPGA-TX4-09-RX1-09-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.11 MSP\_C\_FPGA-TX4-10-RX1-10-MSP\_A\_FPGA

Table 2.220: MSP\_C\_FPGA-TX4-10-RX1-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:48:58		2018-Jan-24 21:49:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7213	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

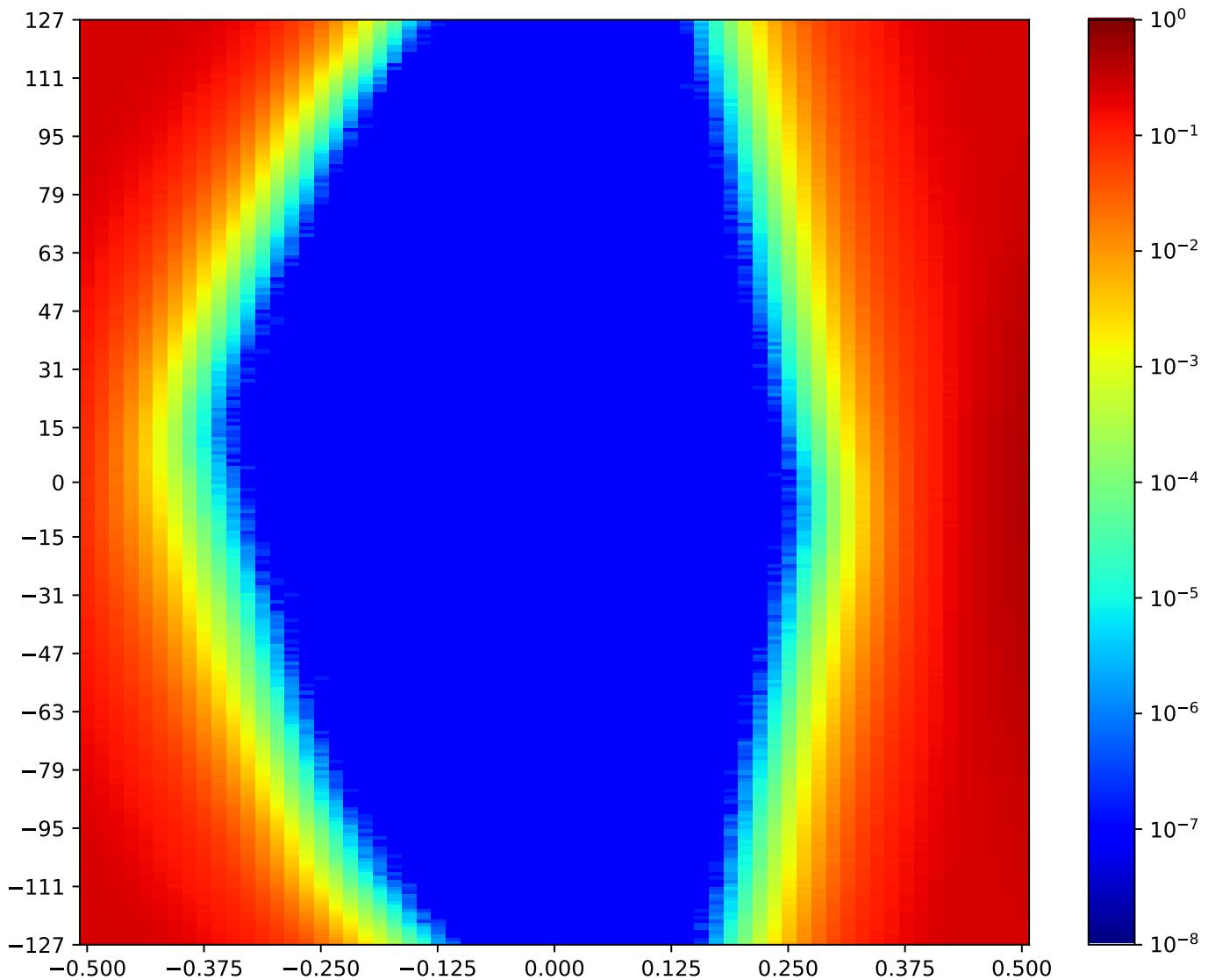


Figure 2.238: MSP\_C\_FPGA-TX4-10-RX1-10-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.18.12 MSP\_C\_FPGA-TX4-11-RX1-11-MSP\_A\_FPGA

Table 2.221: MSP\_C\_FPGA-TX4-11-RX1-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:48:28		2018-Jan-24 21:48:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6935	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

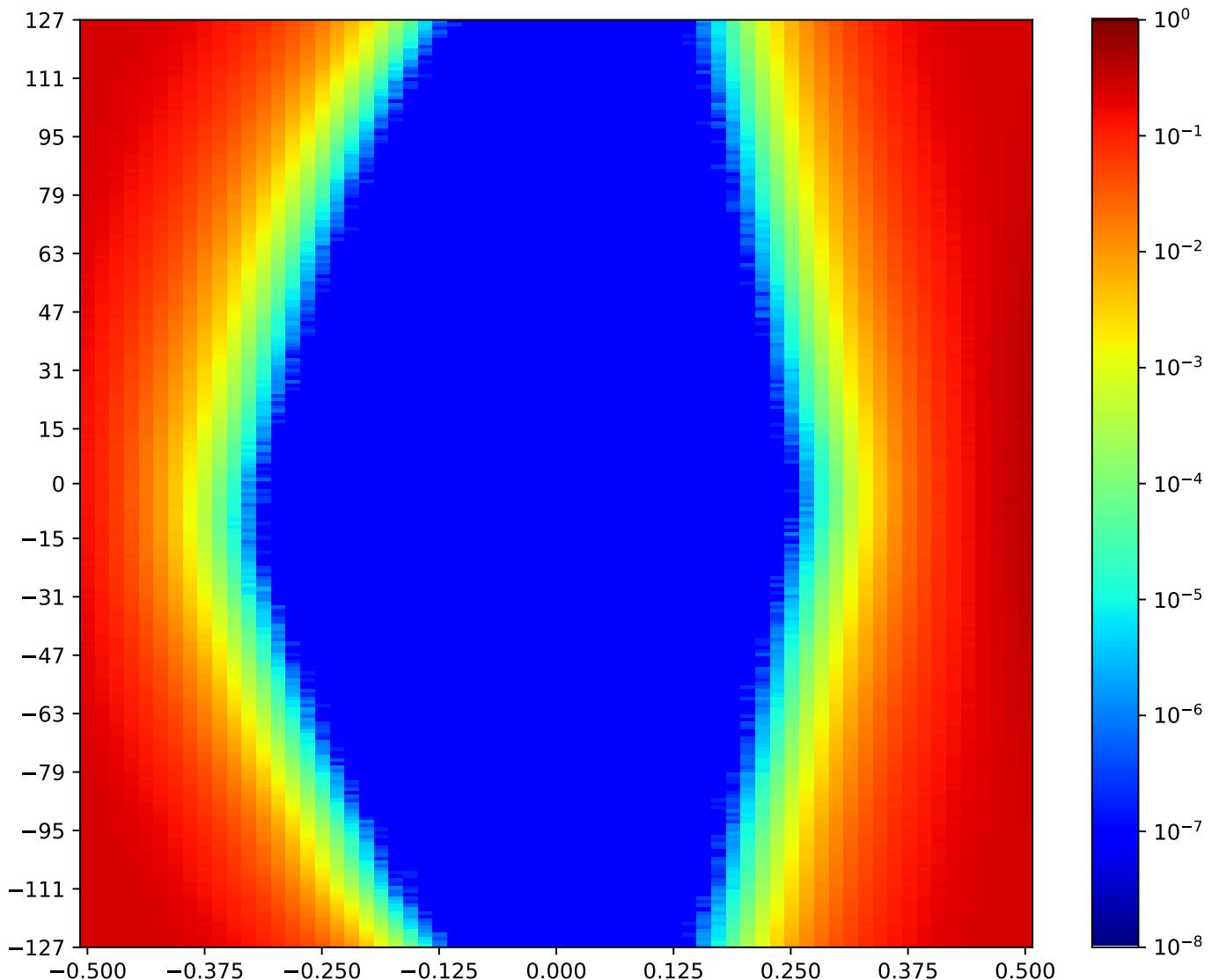


Figure 2.239: MSP\_C\_FPGA-TX4-11-RX1-11-MSP\_A\_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19 MSP\_A TX1 MSP\_C RX13 Minipod Loopback

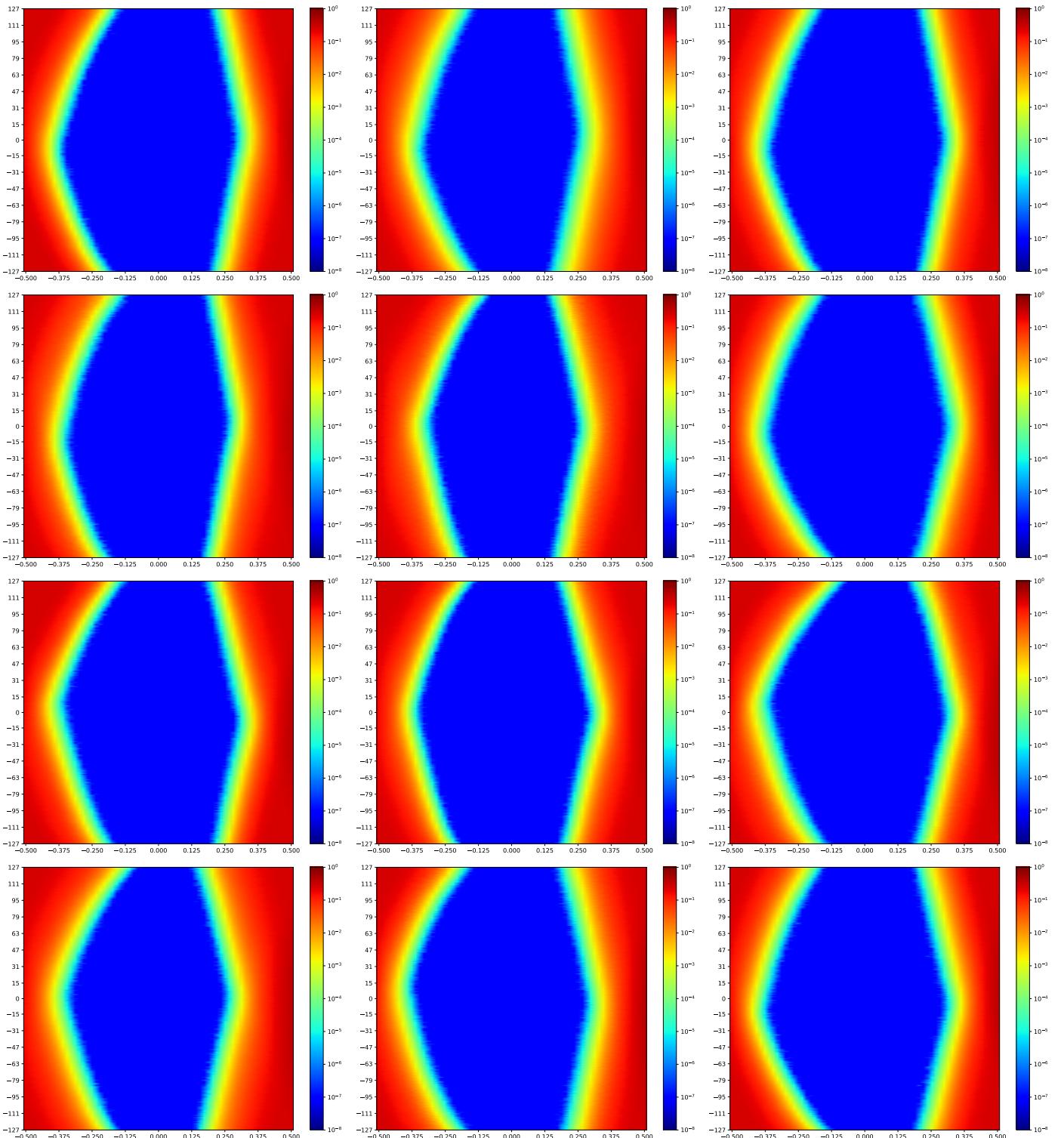


Figure 2.240: MSP\_A TX1 MSP\_C RX13 Minipod Loopback

A cross-reference to Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.253.

### 2.19.1 MSP\_A\_FPGA-TX1-00-RX13-00-MSP\_C\_FPGA

Table 2.222: MSP\_A\_FPGA-TX1-00-RX13-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:00:33		2018-Jan-24 22:01:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8029	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

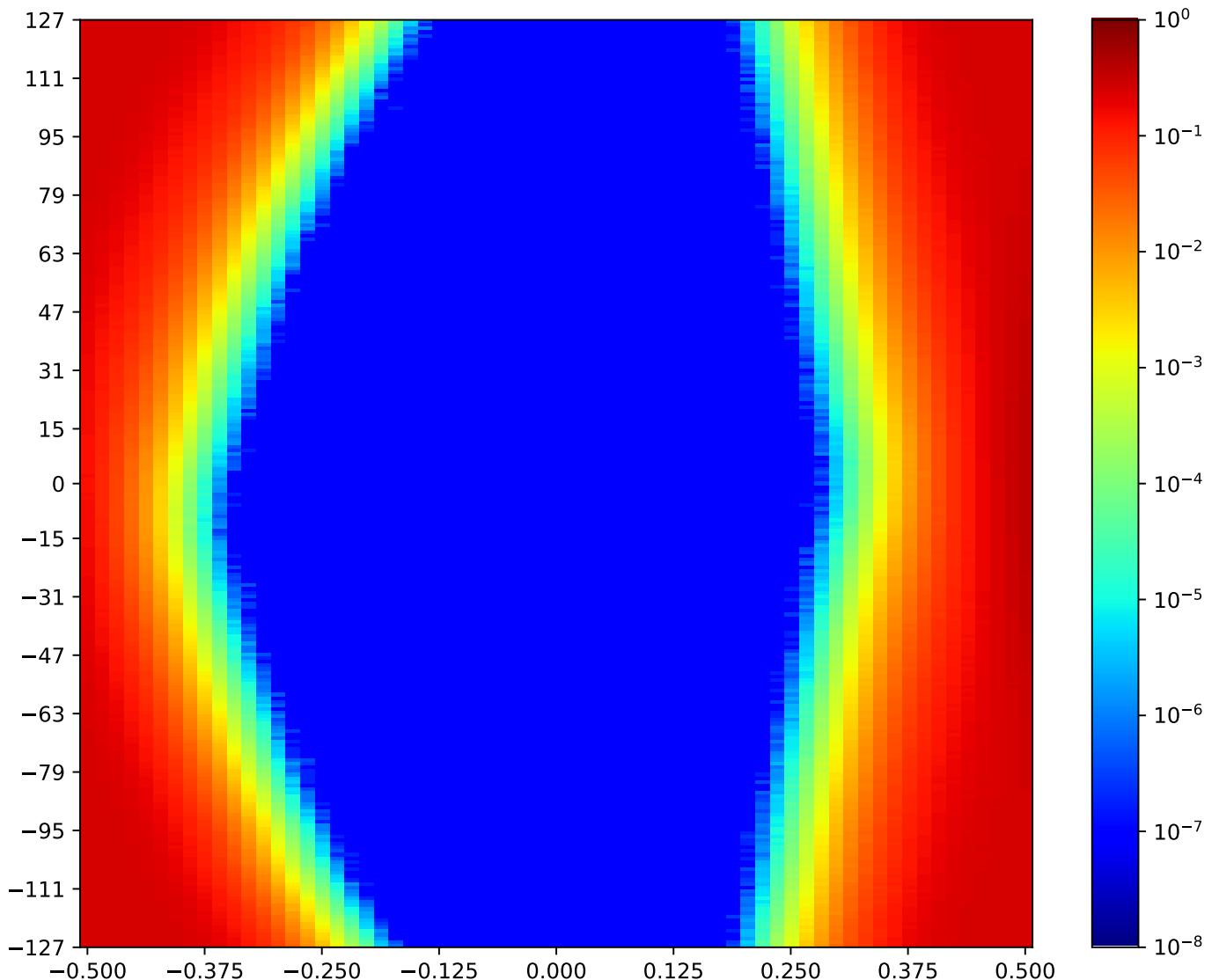


Figure 2.241: MSP\_A\_FPGA-TX1-00-RX13-00-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.2 MSP\_A\_FPGA-TX1-01-RX13-01-MSP\_C\_FPGA

Table 2.223: MSP\_A\_FPGA-TX1-01-RX13-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:01:36		2018-Jan-24 22:02:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6715	34	52.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

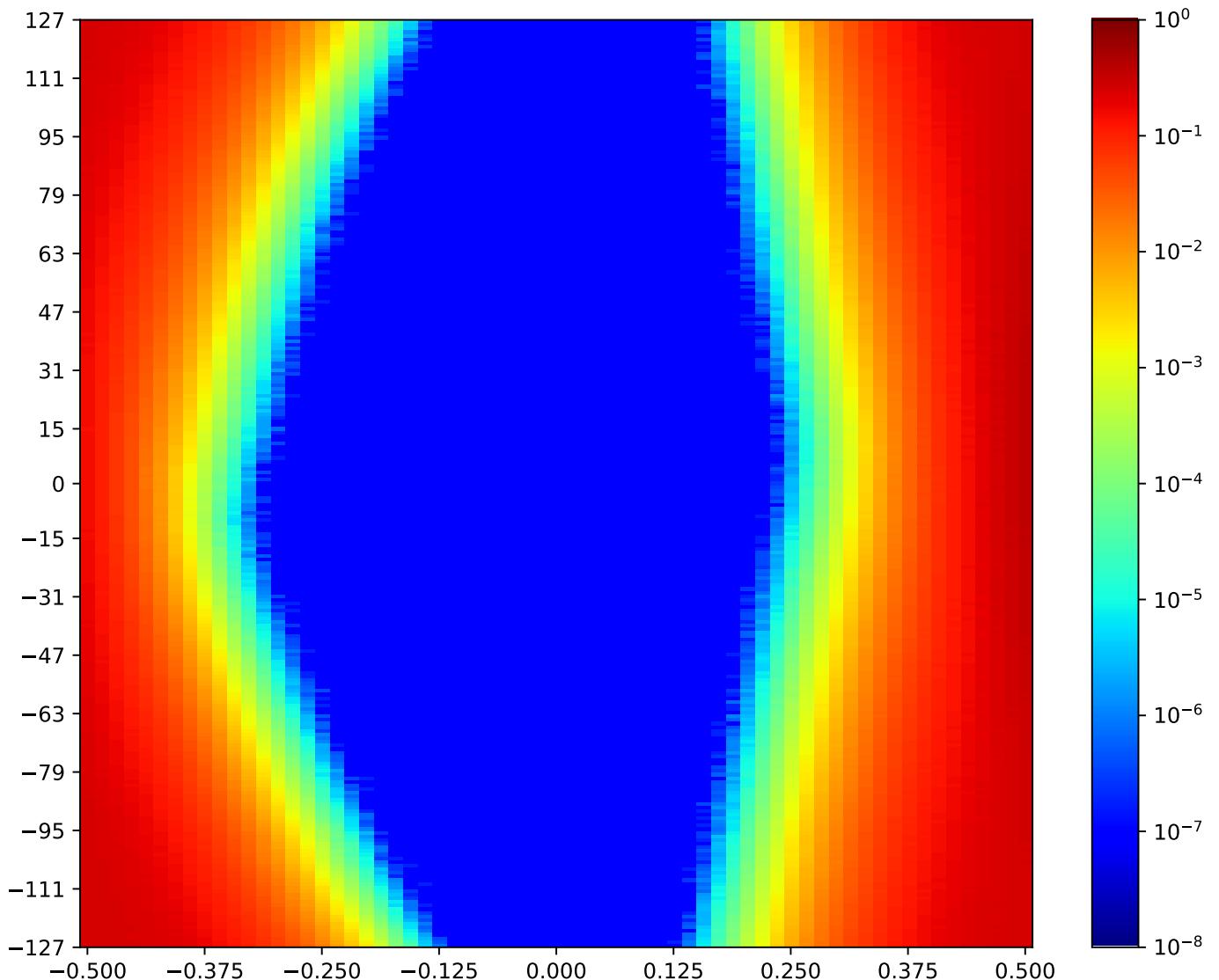


Figure 2.242: MSP\_A\_FPGA-TX1-01-RX13-01-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.19.3 MSP\_A\_FPGA-TX1-02-RX13-02-MSP\_C\_FPGA

Table 2.224: MSP\_A\_FPGA-TX1-02-RX13-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:02:07		2018-Jan-24 22:02:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7933	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

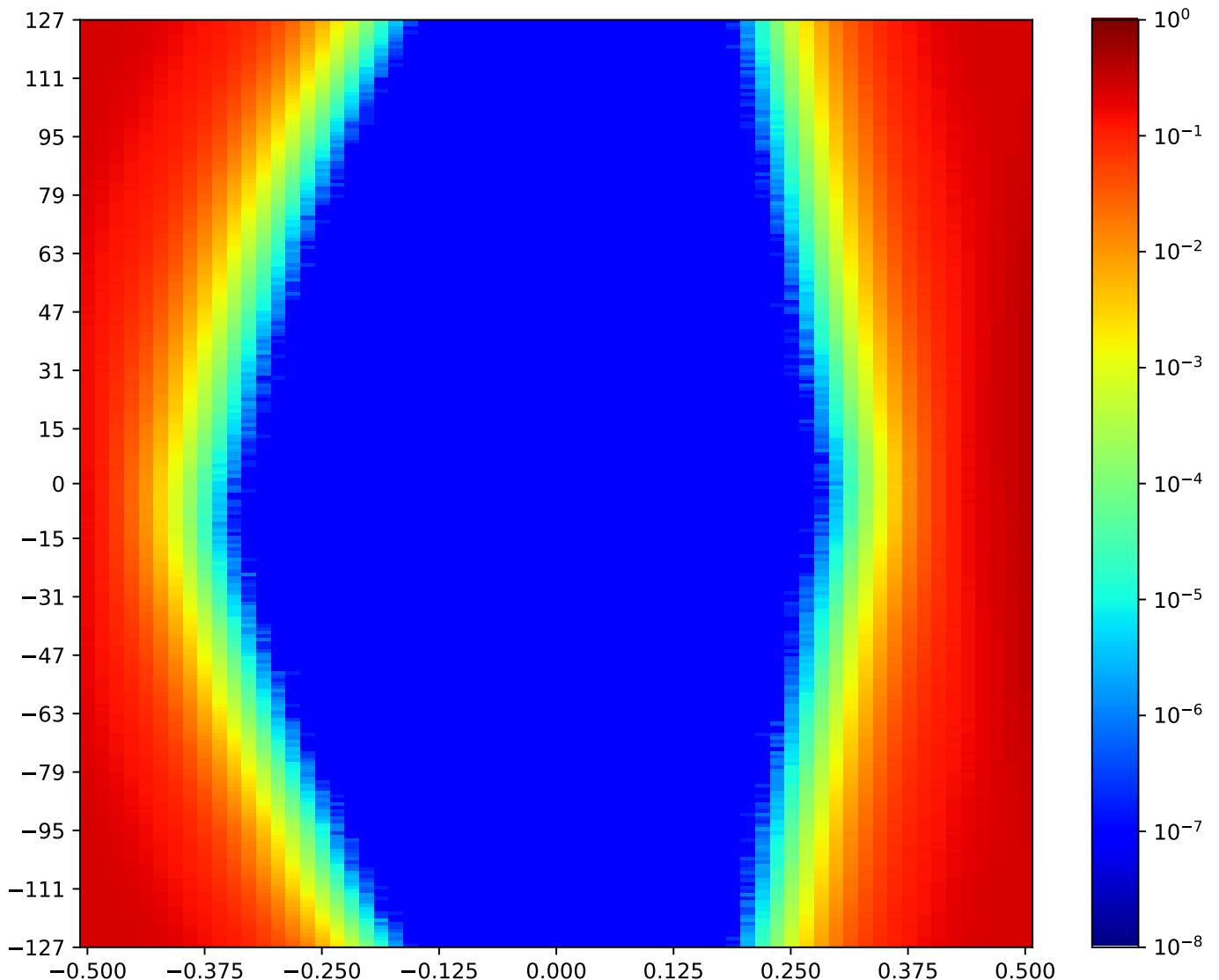


Figure 2.243: MSP\_A\_FPGA-TX1-02-RX13-02-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.4 MSP\_A\_FPGA-TX1-03-RX13-03-MSP\_C\_FPGA

Table 2.225: MSP\_A\_FPGA-TX1-03-RX13-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:59:31		2018-Jan-24 22:00:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7300	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

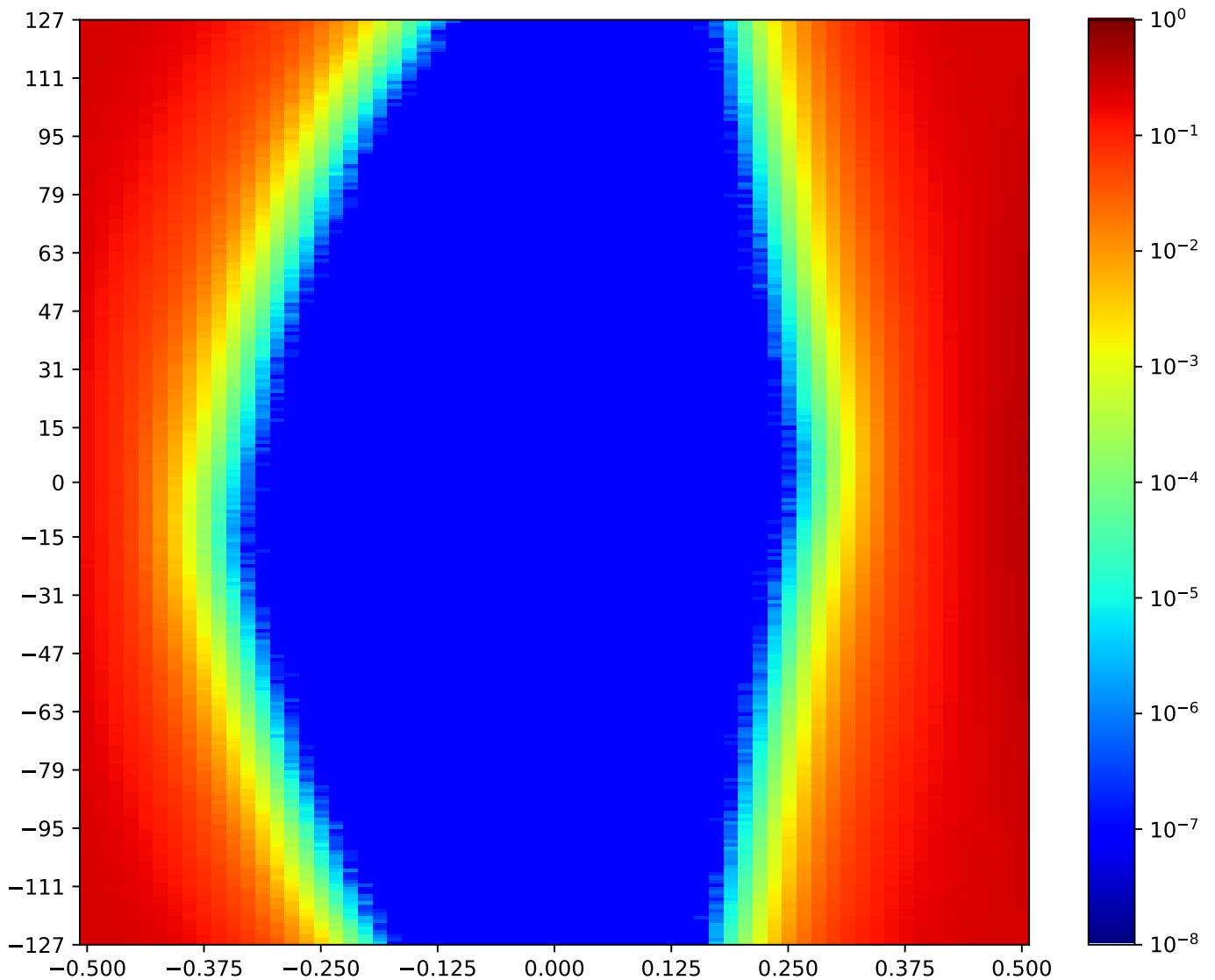


Figure 2.244: MSP\_A\_FPGA-TX1-03-RX13-03-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.5 MSP\_A\_FPGA-TX1-04-RX13-04-MSP\_C\_FPGA

Table 2.226: MSP\_A\_FPGA-TX1-04-RX13-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:03:43		2018-Jan-24 22:04:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6454	32	49.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

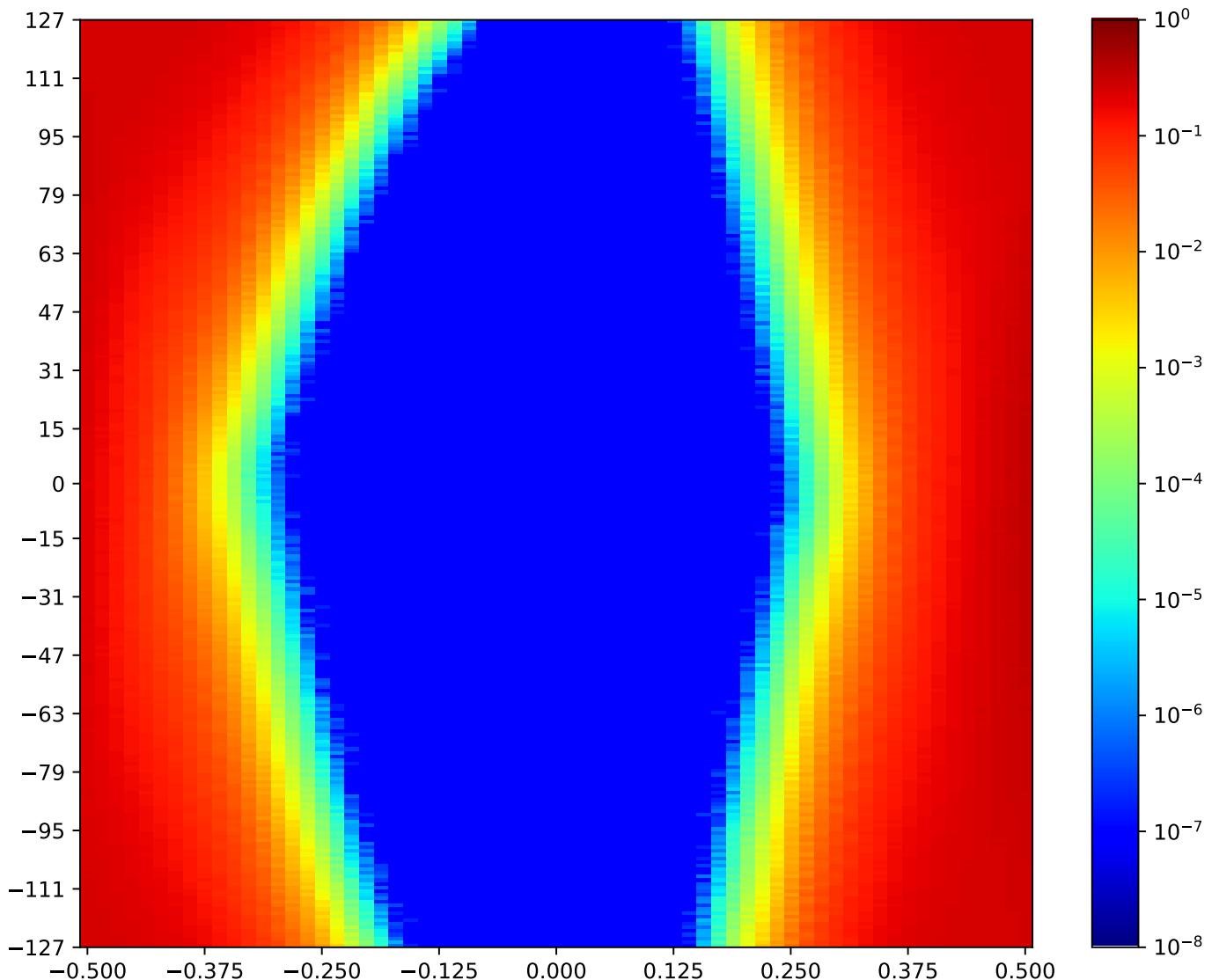


Figure 2.245: MSP\_A\_FPGA-TX1-04-RX13-04-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.6 MSP\_A\_FPGA-TX1-05-RX13-05-MSP\_C\_FPGA

Table 2.227: MSP\_A\_FPGA-TX1-05-RX13-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 21:58:58		2018-Jan-24 21:59:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7780	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

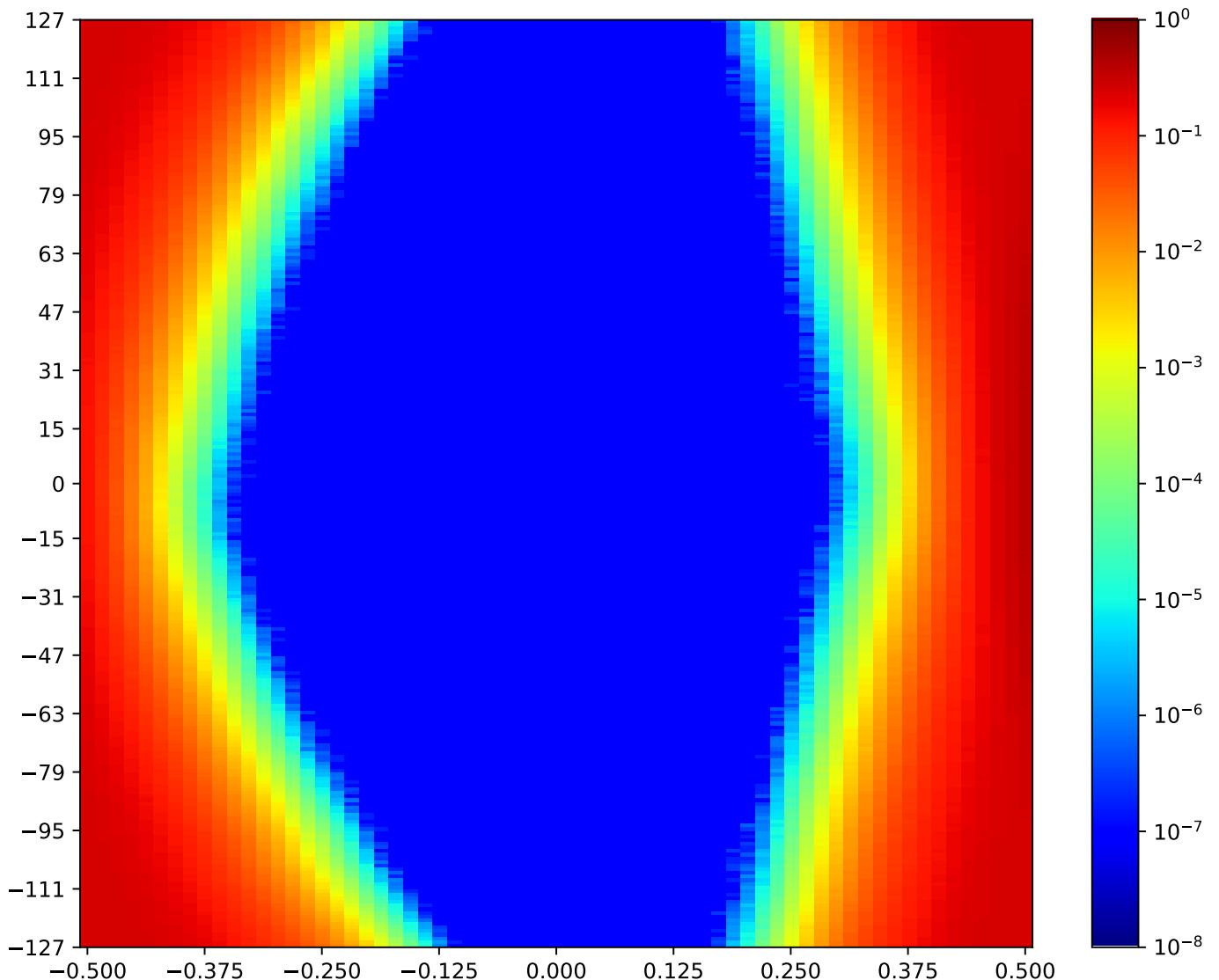


Figure 2.246: MSP\_A\_FPGA-TX1-05-RX13-05-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.7 MSP\_A\_FPGA-TX1-06-RX13-06-MSP\_C\_FPGA

Table 2.228: MSP\_A\_FPGA-TX1-06-RX13-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:04:44		2018-Jan-24 22:05:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7807	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

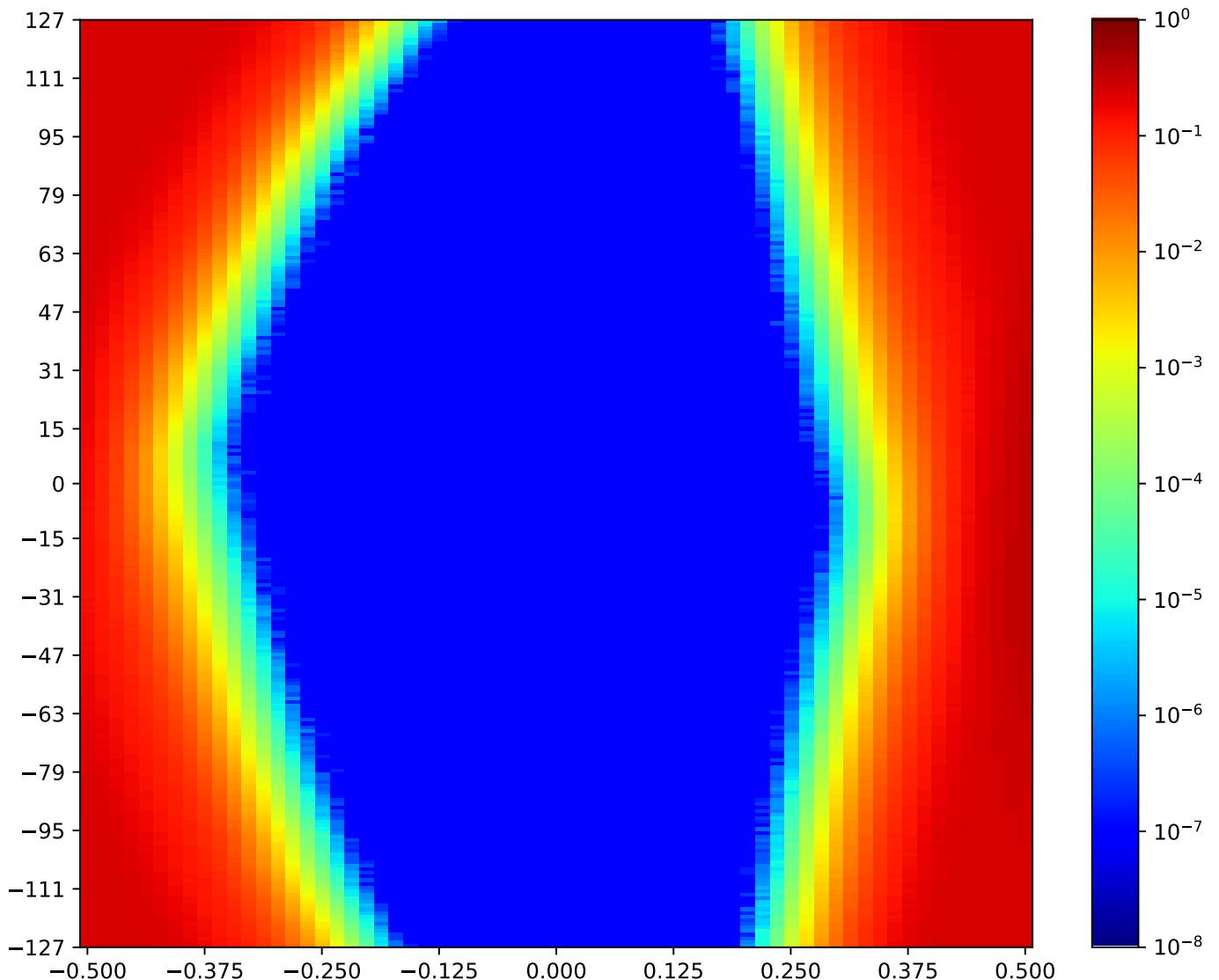


Figure 2.247: MSP\_A\_FPGA-TX1-06-RX13-06-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.8 MSP\_A\_FPGA-TX1-07-RX13-07-MSP\_C\_FPGA

Table 2.229: MSP\_A\_FPGA-TX1-07-RX13-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:00:02		2018-Jan-24 22:00:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7857	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

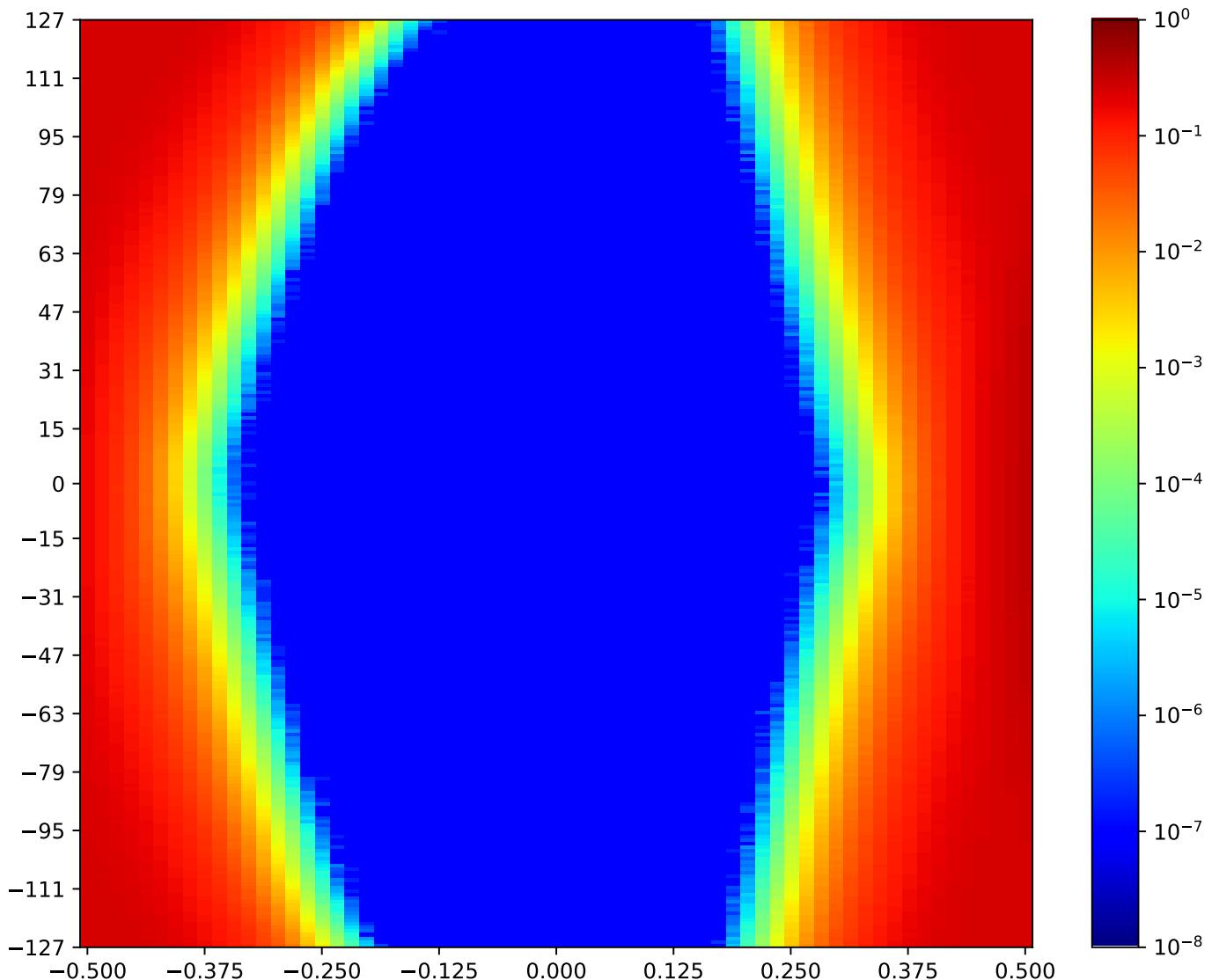


Figure 2.248: MSP\_A\_FPGA-TX1-07-RX13-07-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.9 MSP\_A\_FPGA-TX1-08-RX13-08-MSP\_C\_FPGA

Table 2.230: MSP\_A\_FPGA-TX1-08-RX13-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:04:13		2018-Jan-24 22:04:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7494	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

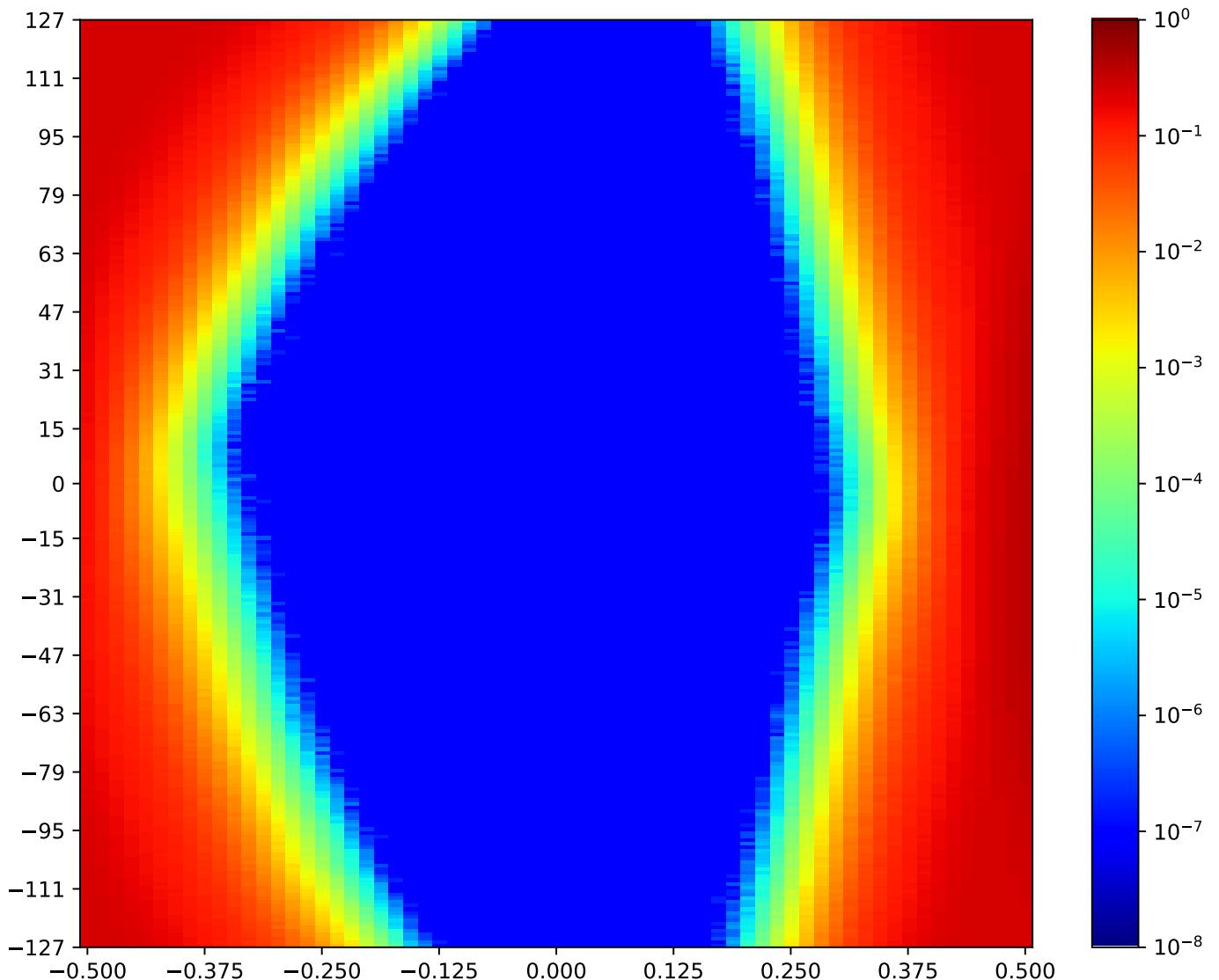


Figure 2.249: MSP\_A\_FPGA-TX1-08-RX13-08-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.10 MSP\_A\_FPGA-TX1-09-RX13-09-MSP\_C\_FPGA

Table 2.231: MSP\_A\_FPGA-TX1-09-RX13-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:01:05		2018-Jan-24 22:01:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6729	35	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

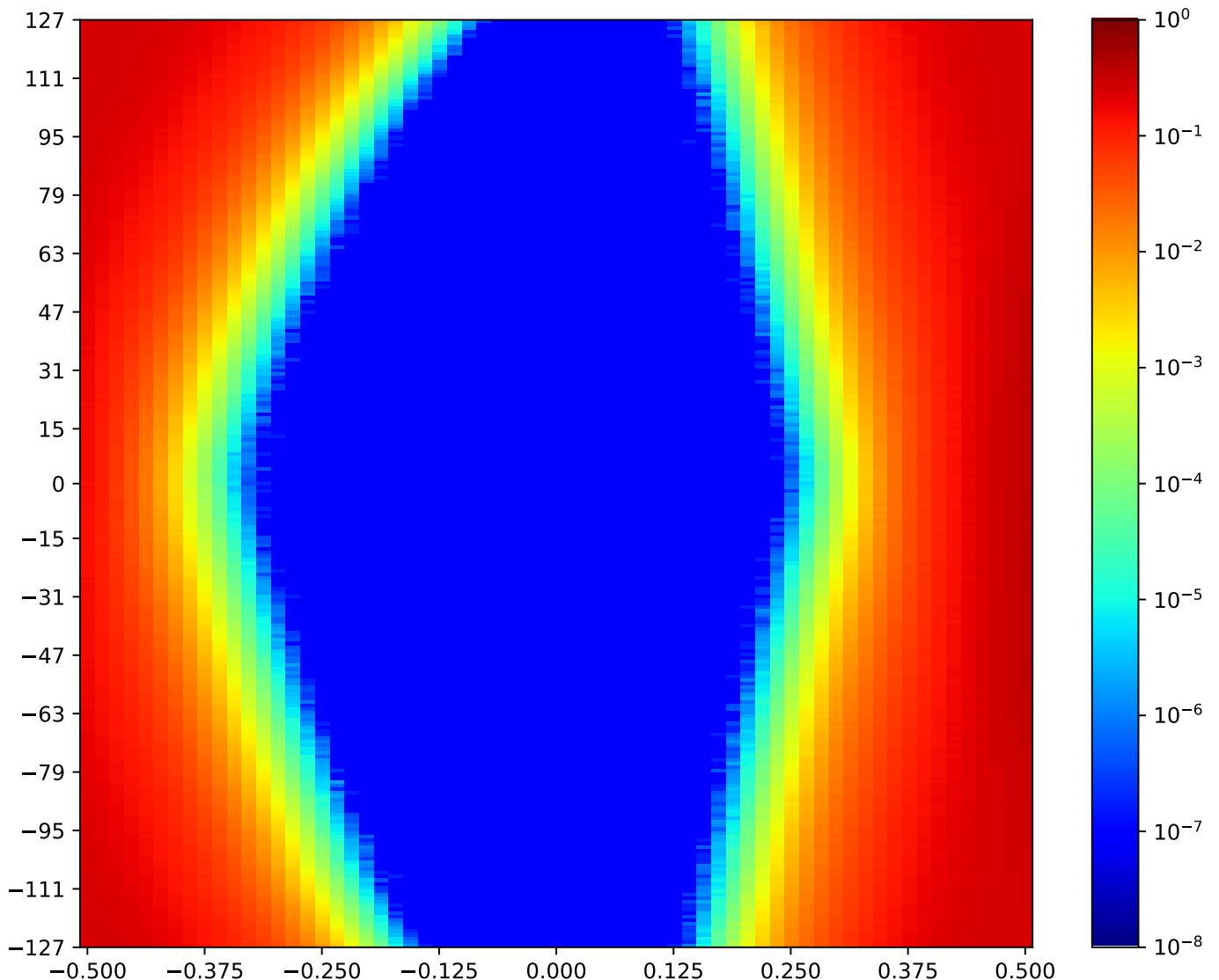


Figure 2.250: MSP\_A\_FPGA-TX1-09-RX13-09-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.11 MSP\_A\_FPGA-TX1-10-RX13-10-MSP\_C\_FPGA

Table 2.232: MSP\_A\_FPGA-TX1-10-RX13-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:03:11		2018-Jan-24 22:03:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7912	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

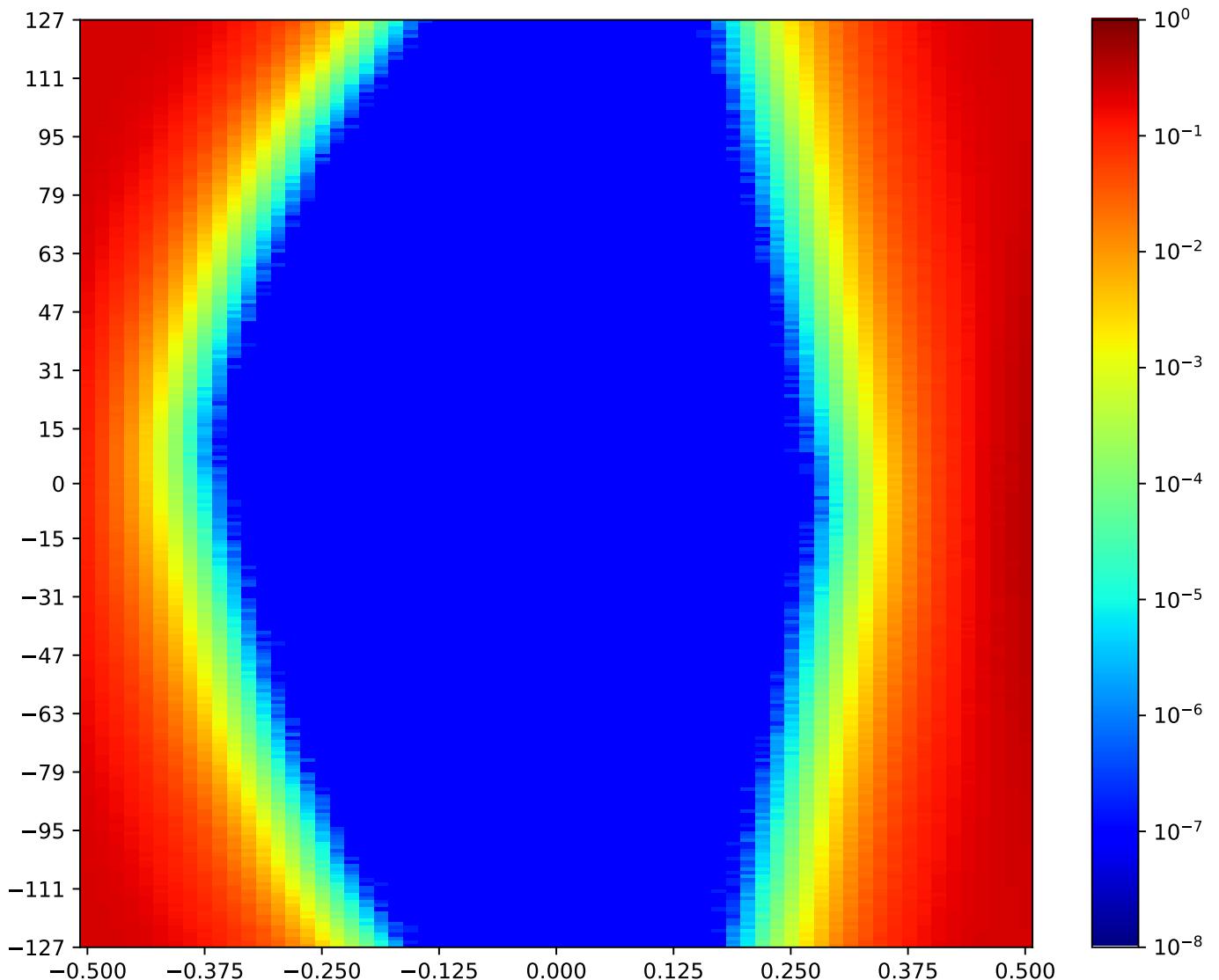


Figure 2.251: MSP\_A\_FPGA-TX1-10-RX13-10-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.19.12 MSP\_A\_FPGA-TX1-11-RX13-11-MSP\_C\_FPGA

Table 2.233: MSP\_A\_FPGA-TX1-11-RX13-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:02:39		2018-Jan-24 22:03:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7990	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

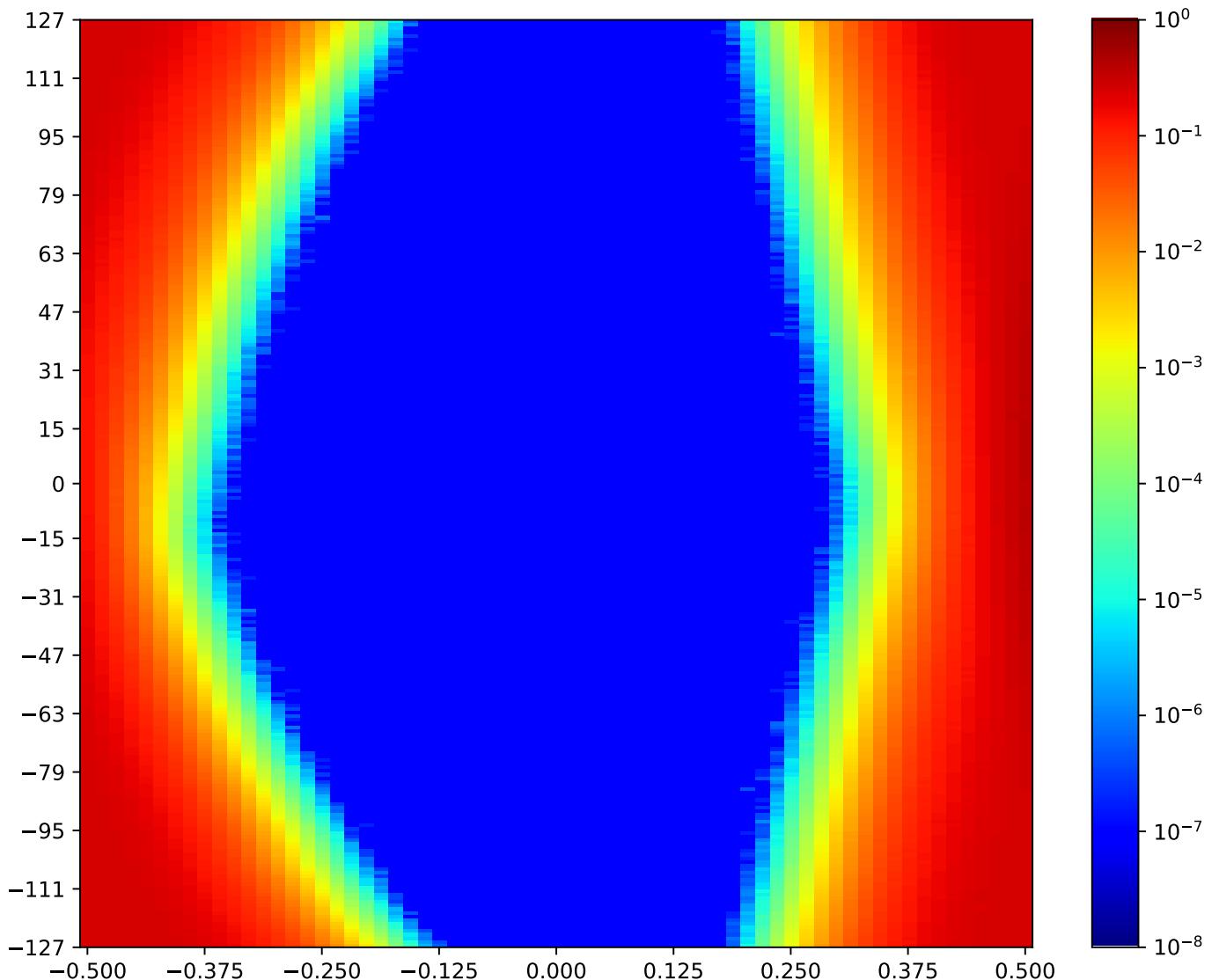


Figure 2.252: MSP\_A\_FPGA-TX1-11-RX13-11-MSP\_C\_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20 MSP\_A TX2 MSP\_C RX12 Minipod Loopback

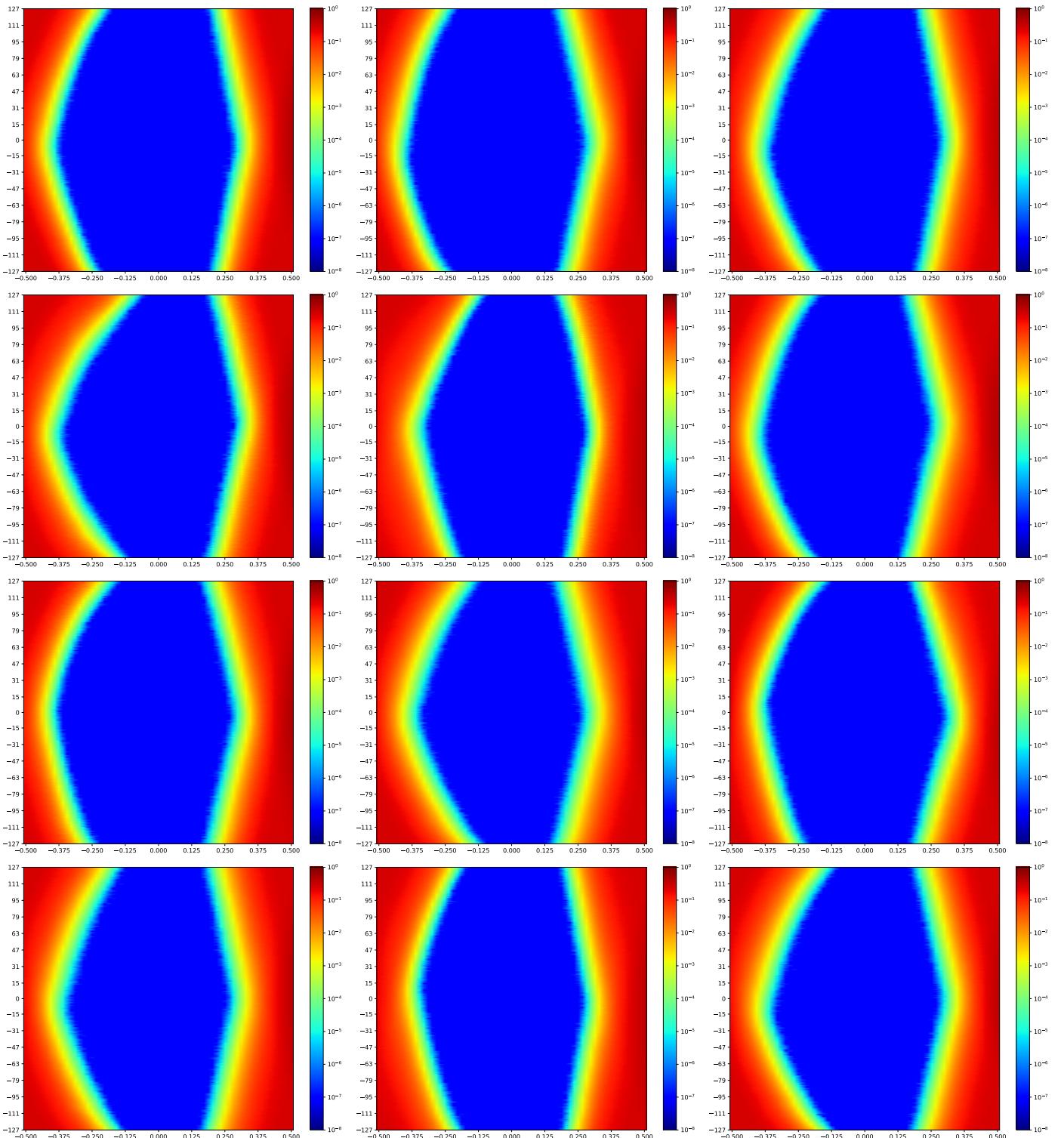


Figure 2.253: MSP\_A TX2 MSP\_C RX12 Minipod Loopback

A cross-reference to Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.266.

### 2.20.1 MSP\_A\_FPGA-TX2-00-RX12-00-MSP\_C\_FPGA

Table 2.234: MSP\_A\_FPGA-TX2-00-RX12-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:06:45		2018-Jan-24 22:07:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8422	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

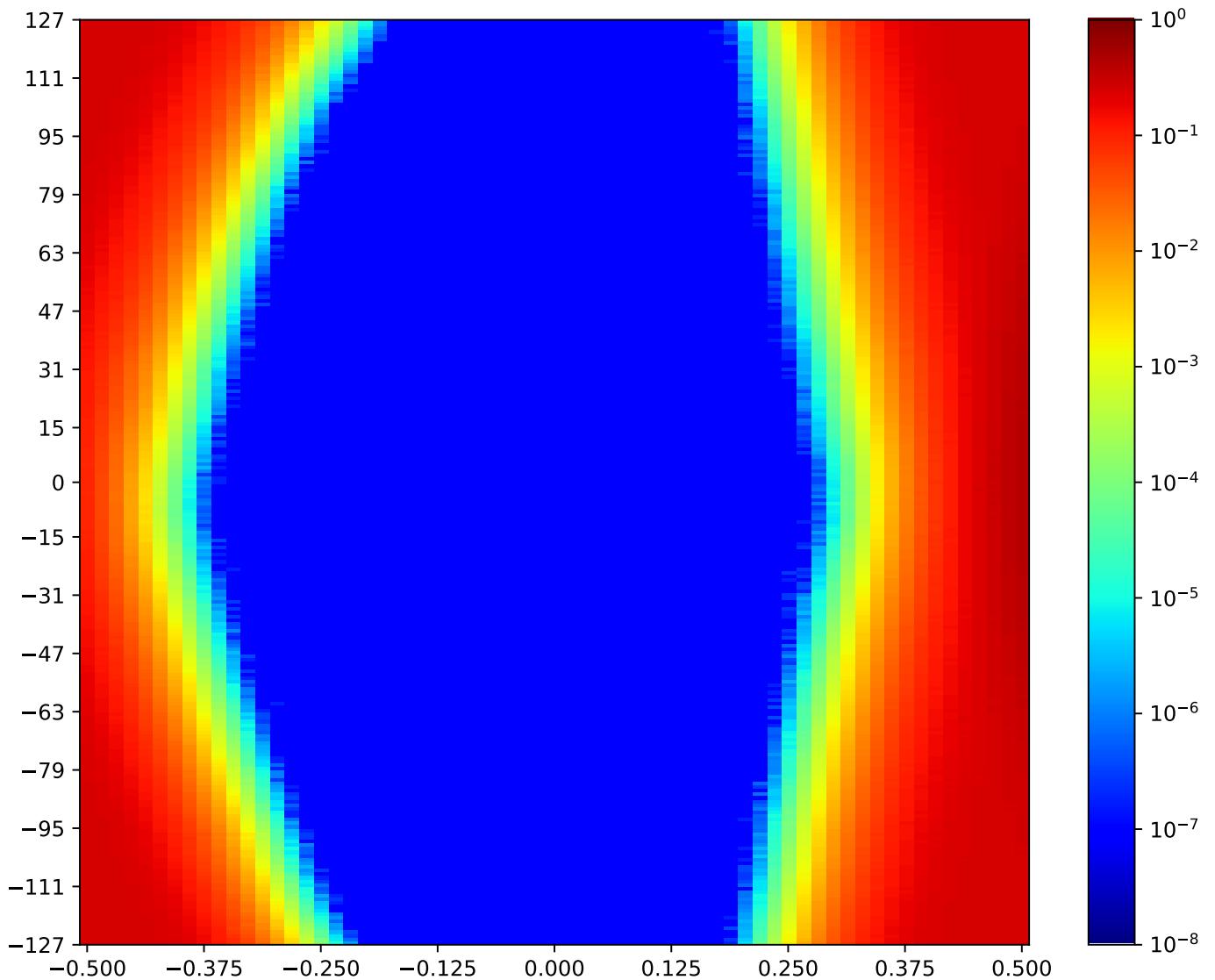


Figure 2.254: MSP\_A\_FPGA-TX2-00-RX12-00-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.2 MSP\_A\_FPGA-TX2-01-RX12-01-MSP\_C\_FPGA

Table 2.235: MSP\_A\_FPGA-TX2-01-RX12-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:05:46		2018-Jan-24 22:06:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8309	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

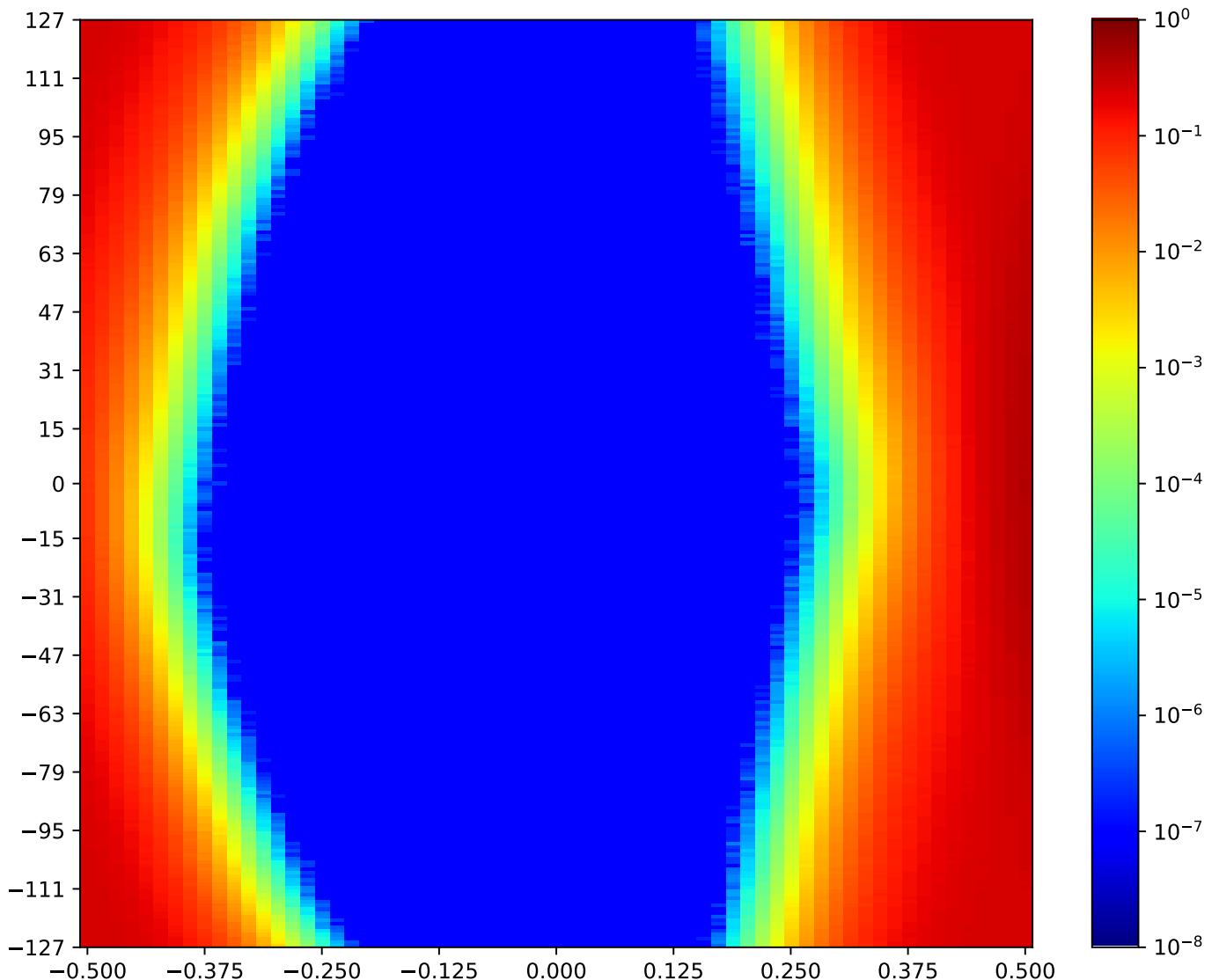


Figure 2.255: MSP\_A\_FPGA-TX2-01-RX12-01-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.20.3 MSP\_A\_FPGA-TX2-02-RX12-02-MSP\_C\_FPGA

Table 2.236: MSP\_A\_FPGA-TX2-02-RX12-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:08:17		2018-Jan-24 22:08:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7769	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

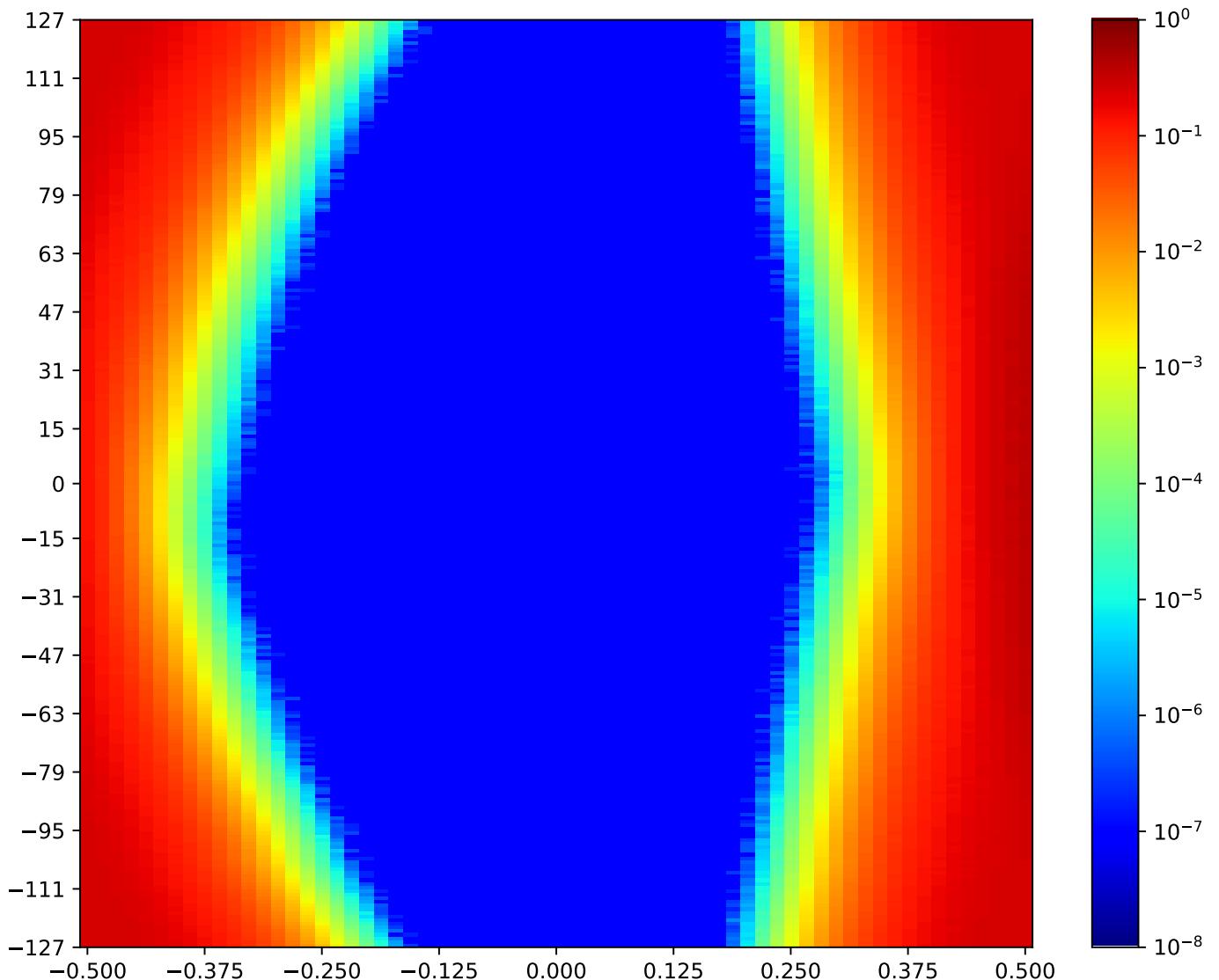


Figure 2.256: MSP\_A\_FPGA-TX2-02-RX12-02-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.4 MSP\_A\_FPGA-TX2-03-RX12-03-MSP\_C\_FPGA

Table 2.237: MSP\_A\_FPGA-TX2-03-RX12-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:05:15		2018-Jan-24 22:05:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7404	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

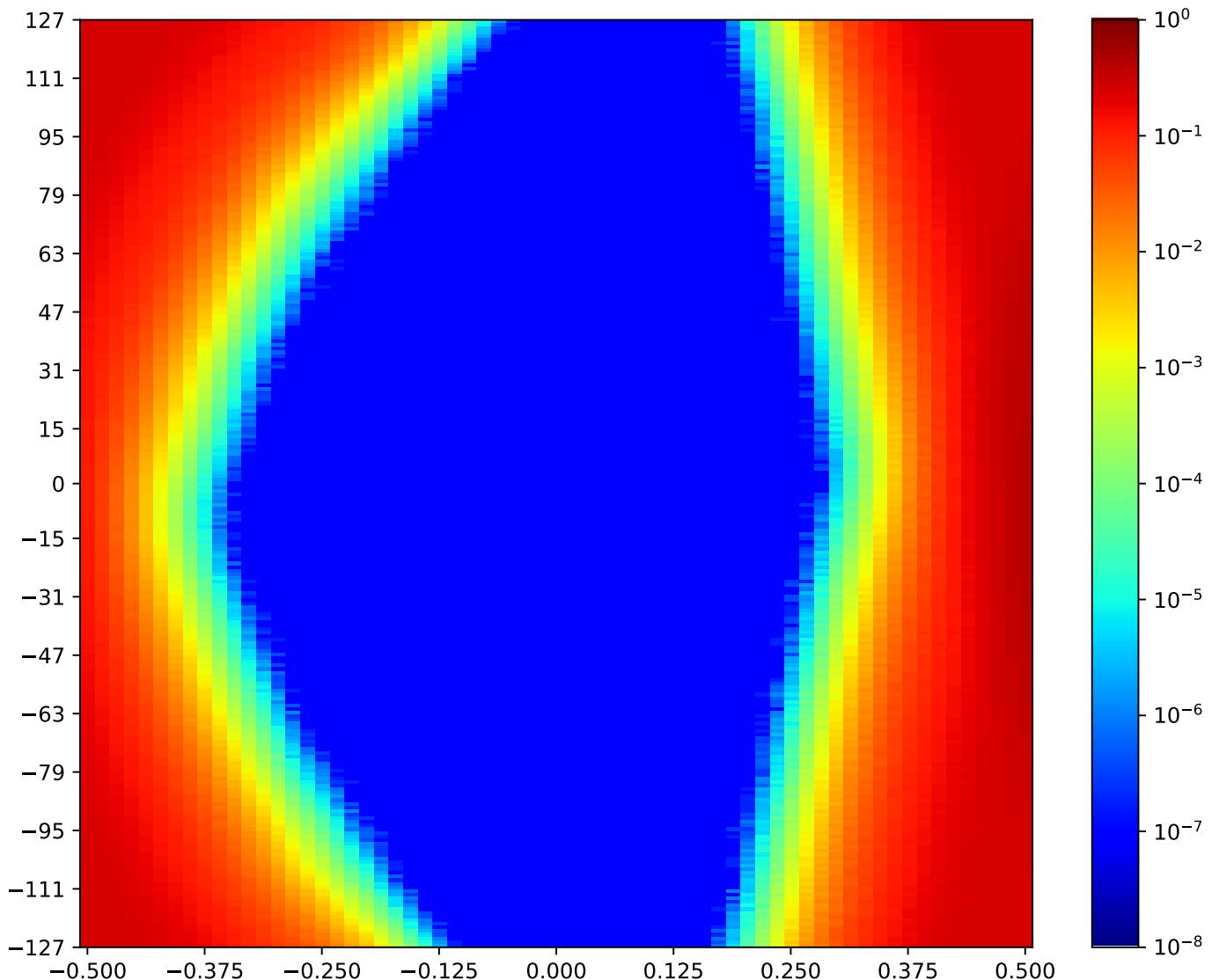


Figure 2.257: MSP\_A\_FPGA-TX2-03-RX12-03-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.5 MSP\_A\_FPGA-TX2-04-RX12-04-MSP\_C\_FPGA

Table 2.238: MSP\_A\_FPGA-TX2-04-RX12-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:09:45		2018-Jan-24 22:10:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7294	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

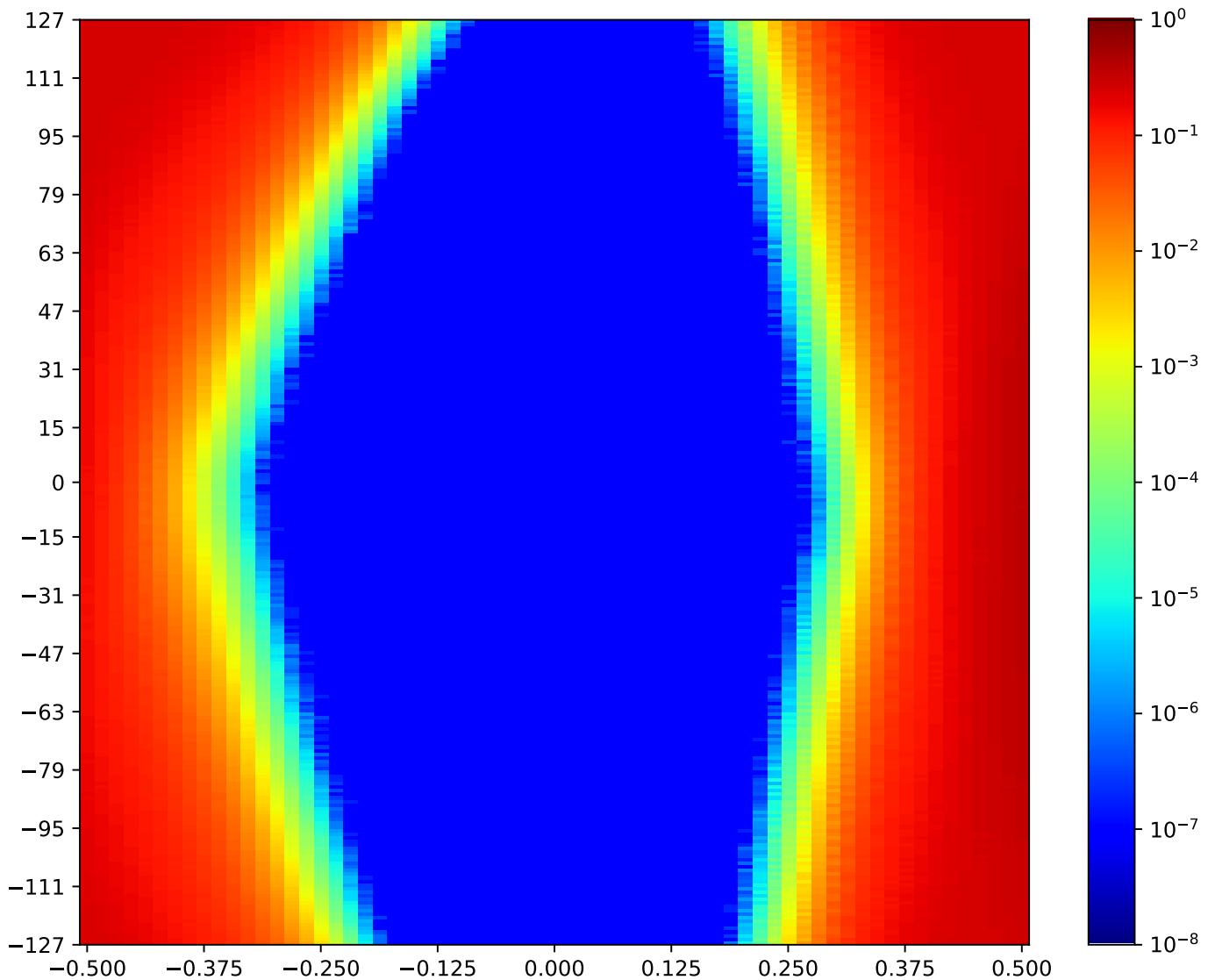


Figure 2.258: MSP\_A\_FPGA-TX2-04-RX12-04-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.6 MSP\_A\_FPGA-TX2-05-RX12-05-MSP\_C\_FPGA

Table 2.239: MSP\_A\_FPGA-TX2-05-RX12-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:06:16		2018-Jan-24 22:06:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7423	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

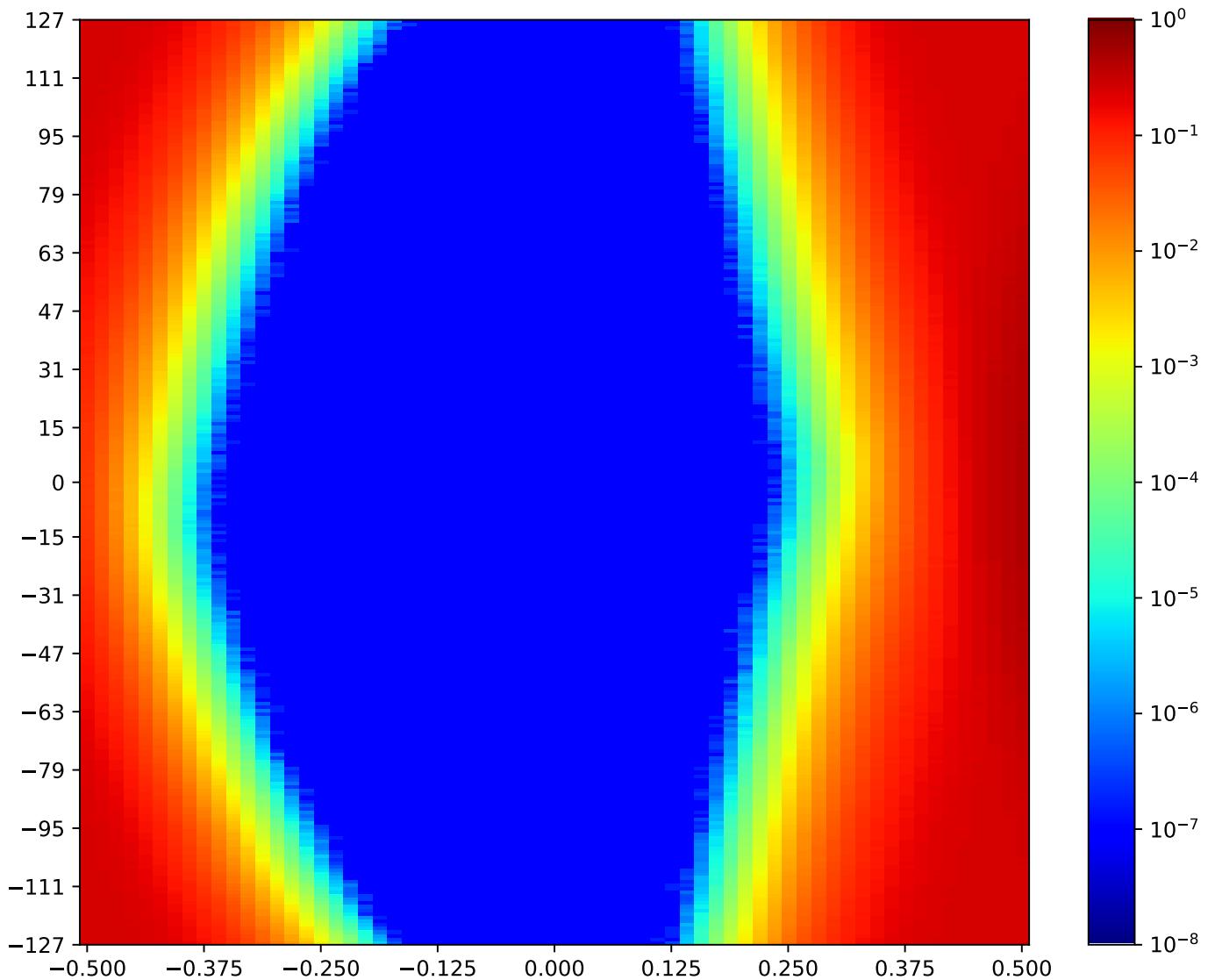


Figure 2.259: MSP\_A\_FPGA-TX2-05-RX12-05-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.7 MSP\_A\_FPGA-TX2-06-RX12-06-MSP\_C\_FPGA

Table 2.240: MSP\_A\_FPGA-TX2-06-RX12-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:10:44		2018-Jan-24 22:11:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8168	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

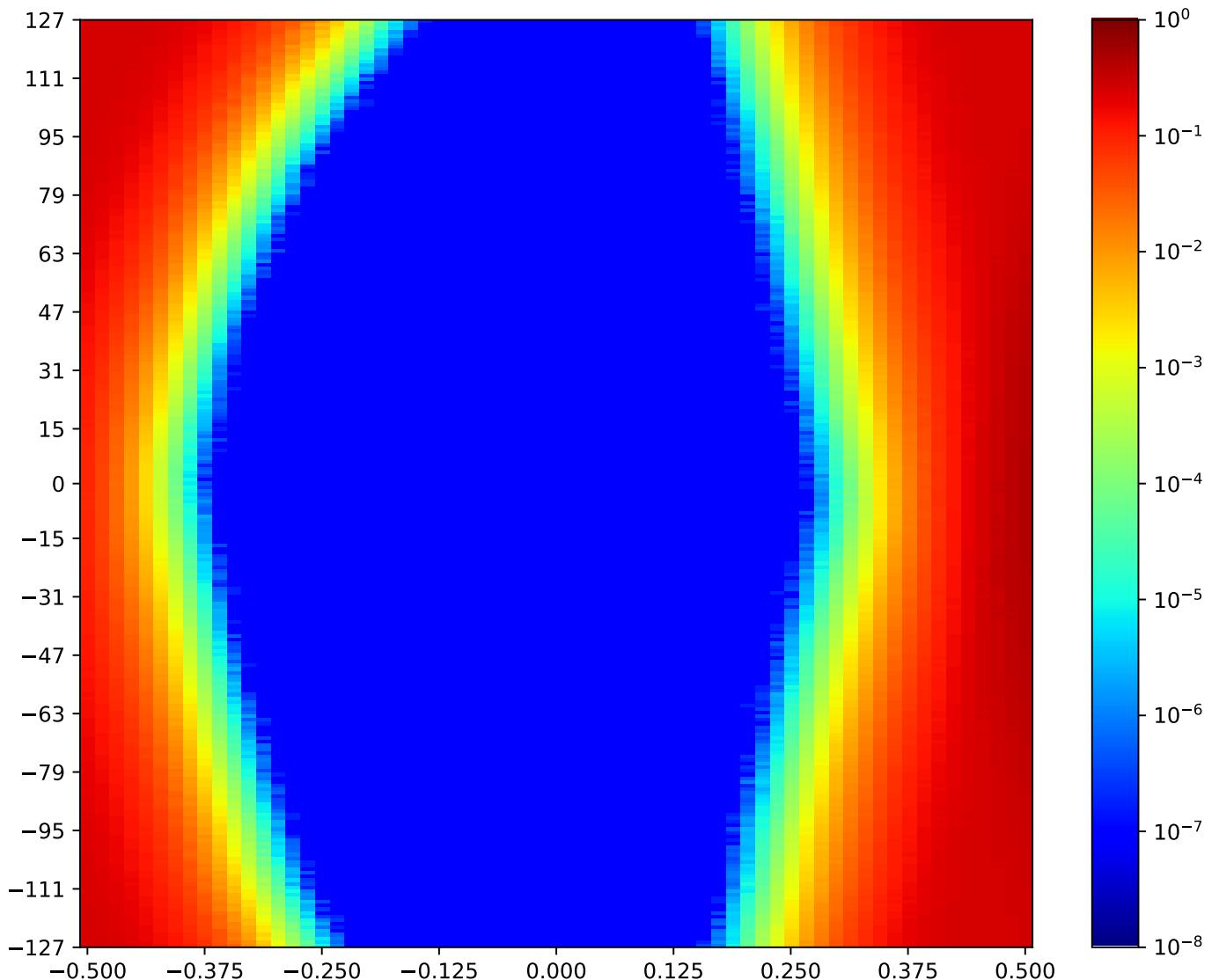


Figure 2.260: MSP\_A\_FPGA-TX2-06-RX12-06-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.8 MSP\_A\_FPGA-TX2-07-RX12-07-MSP\_C\_FPGA

Table 2.241: MSP\_A\_FPGA-TX2-07-RX12-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:07:15		2018-Jan-24 22:07:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6913	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

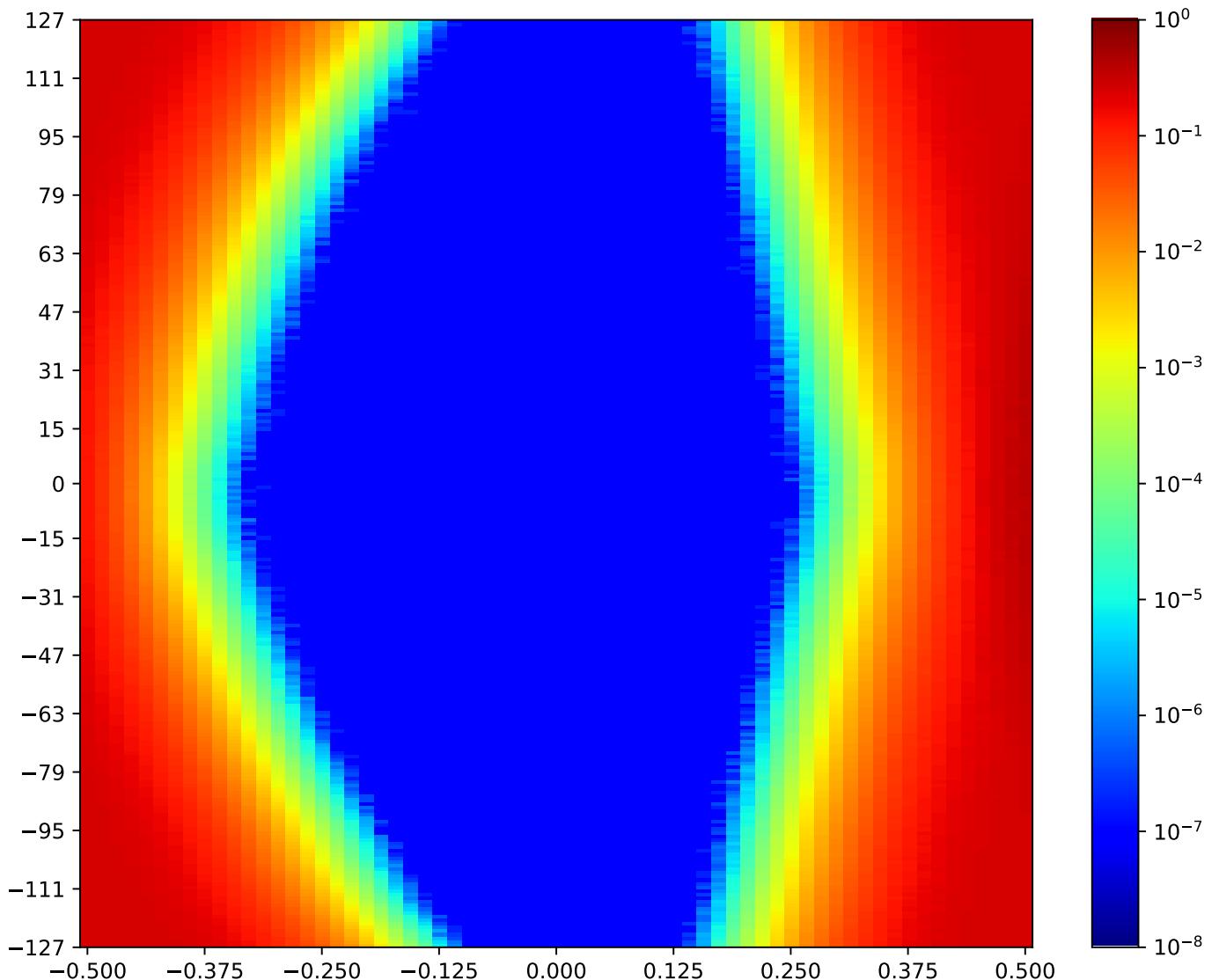


Figure 2.261: MSP\_A\_FPGA-TX2-07-RX12-07-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.9 MSP\_A\_FPGA-TX2-08-RX12-08-MSP\_C\_FPGA

Table 2.242: MSP\_A\_FPGA-TX2-08-RX12-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:10:15		2018-Jan-24 22:10:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8019	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

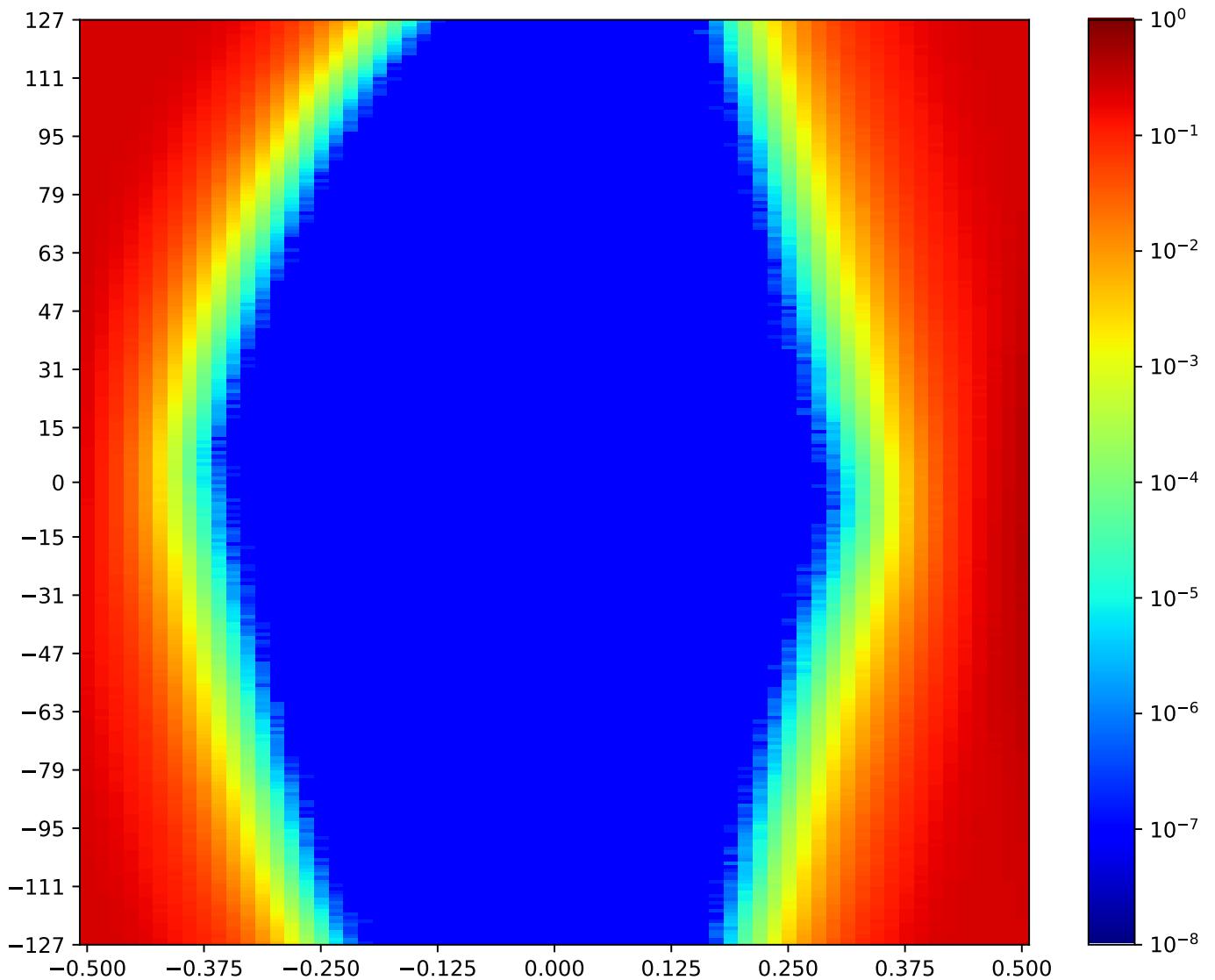


Figure 2.262: MSP\_A\_FPGA-TX2-08-RX12-08-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.10 MSP\_A\_FPGA-TX2-09-RX12-09-MSP\_C\_FPGA

Table 2.243: MSP\_A\_FPGA-TX2-09-RX12-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:07:44		2018-Jan-24 22:08:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7175	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

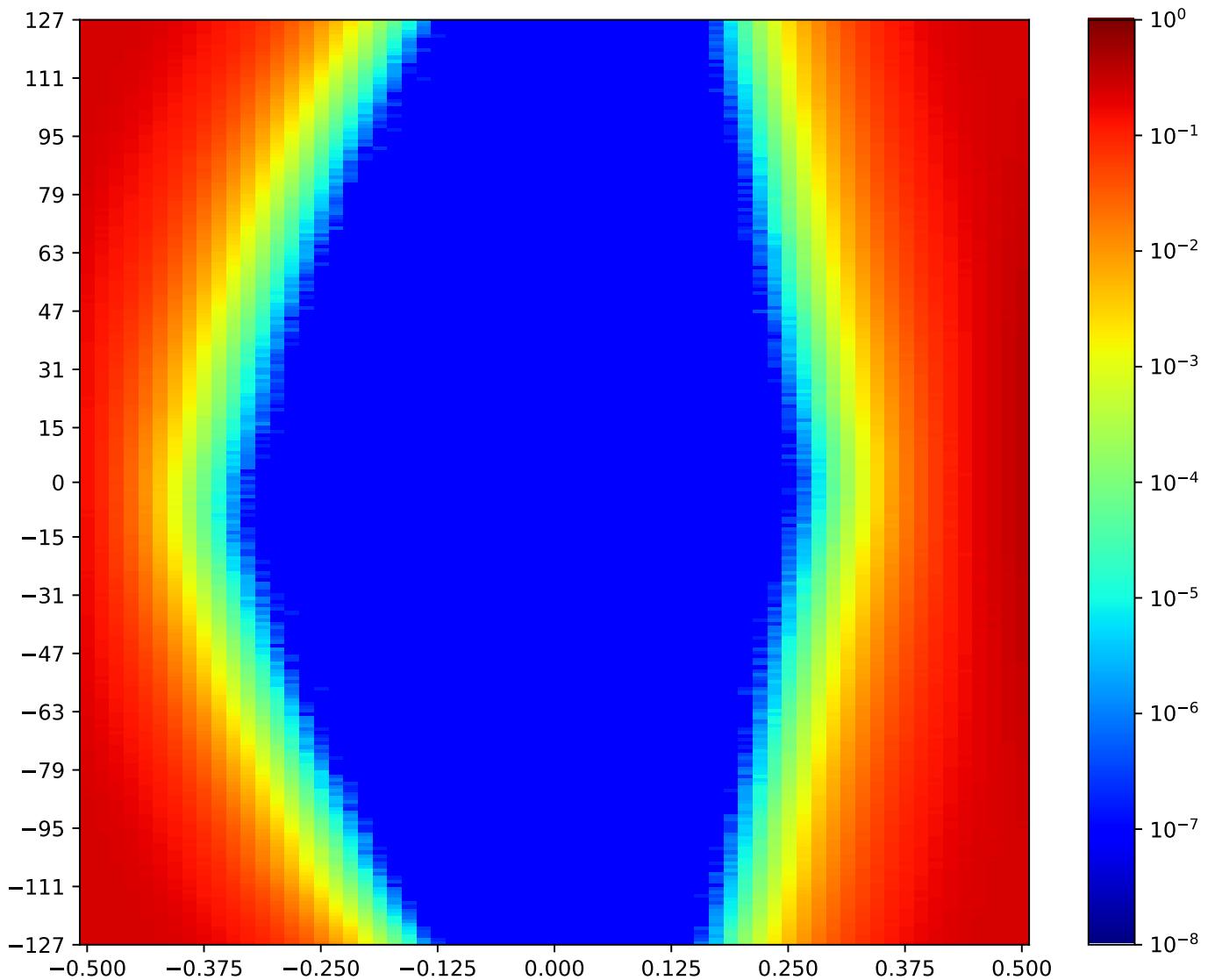


Figure 2.263: MSP\_A\_FPGA-TX2-09-RX12-09-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.11 MSP\_A\_FPGA-TX2-10-RX12-10-MSP\_C\_FPGA

Table 2.244: MSP\_A\_FPGA-TX2-10-RX12-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:09:16		2018-Jan-24 22:09:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7757	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

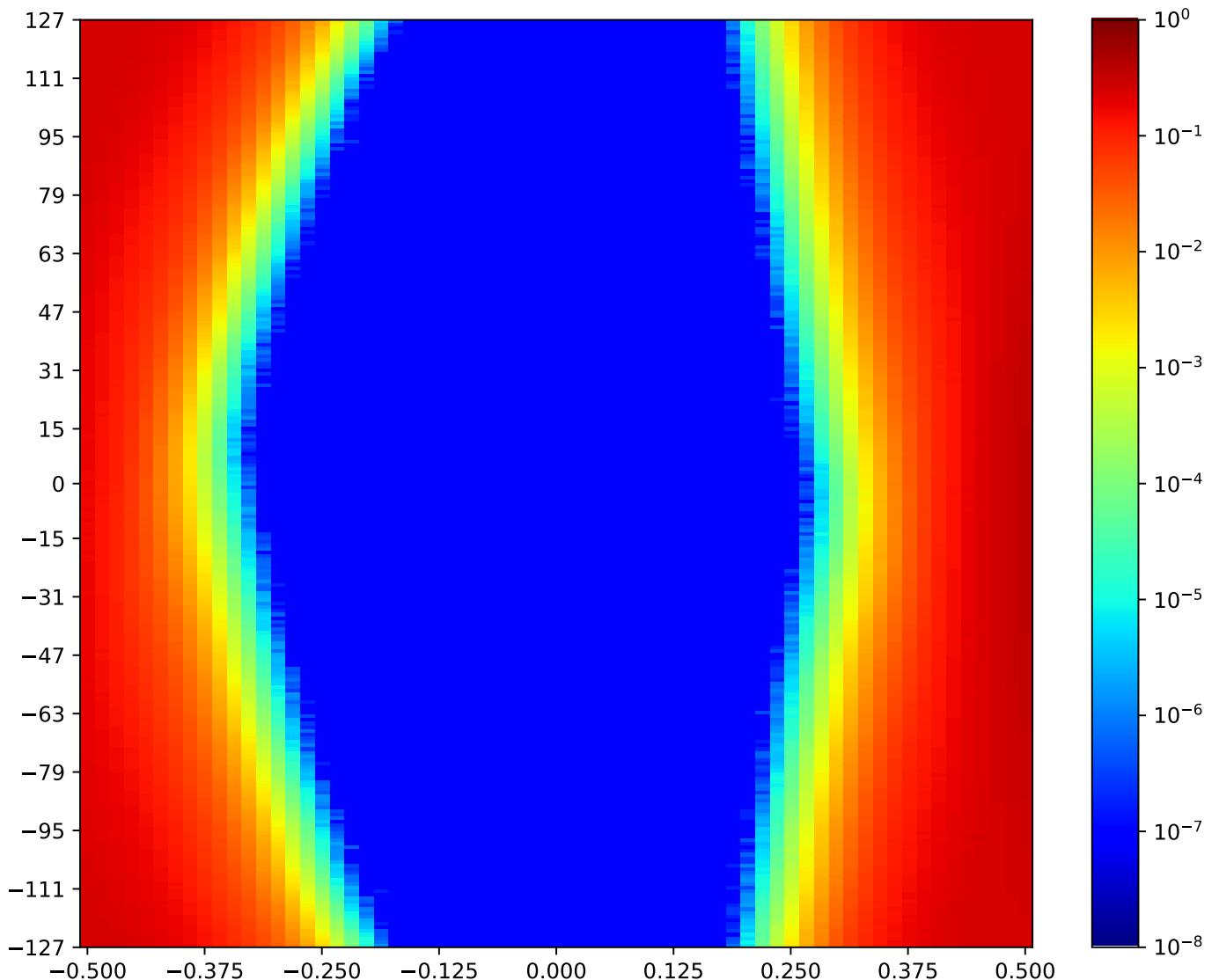


Figure 2.264: MSP\_A\_FPGA-TX2-10-RX12-10-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.20.12 MSP\_A\_FPGA-TX2-11-RX12-11-MSP\_C\_FPGA

Table 2.245: MSP\_A\_FPGA-TX2-11-RX12-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:08:47		2018-Jan-24 22:09:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7360	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

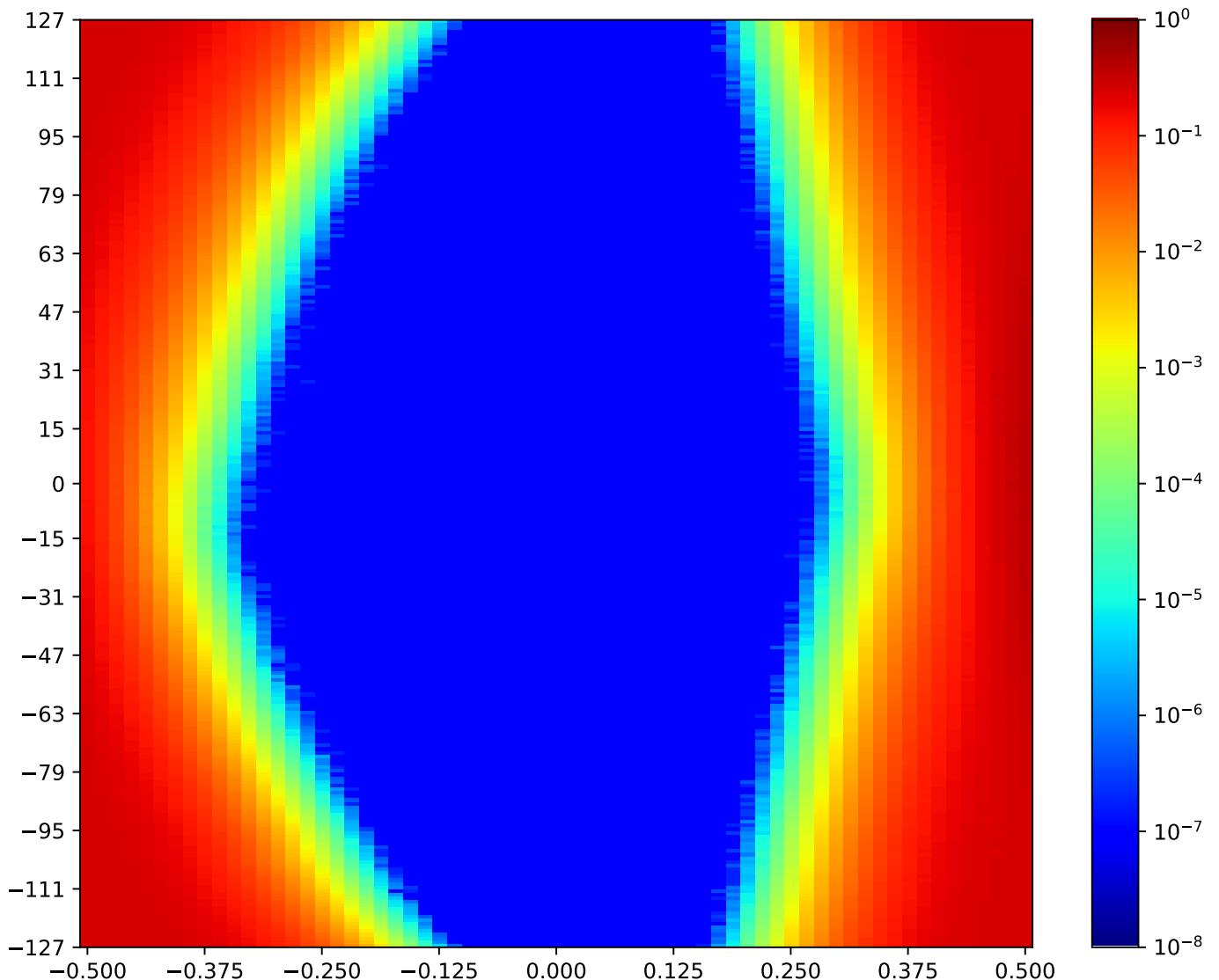


Figure 2.265: MSP\_A\_FPGA-TX2-11-RX12-11-MSP\_C\_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21 MSP\_C TX3 MSP\_A RX4 Minipod Loopback

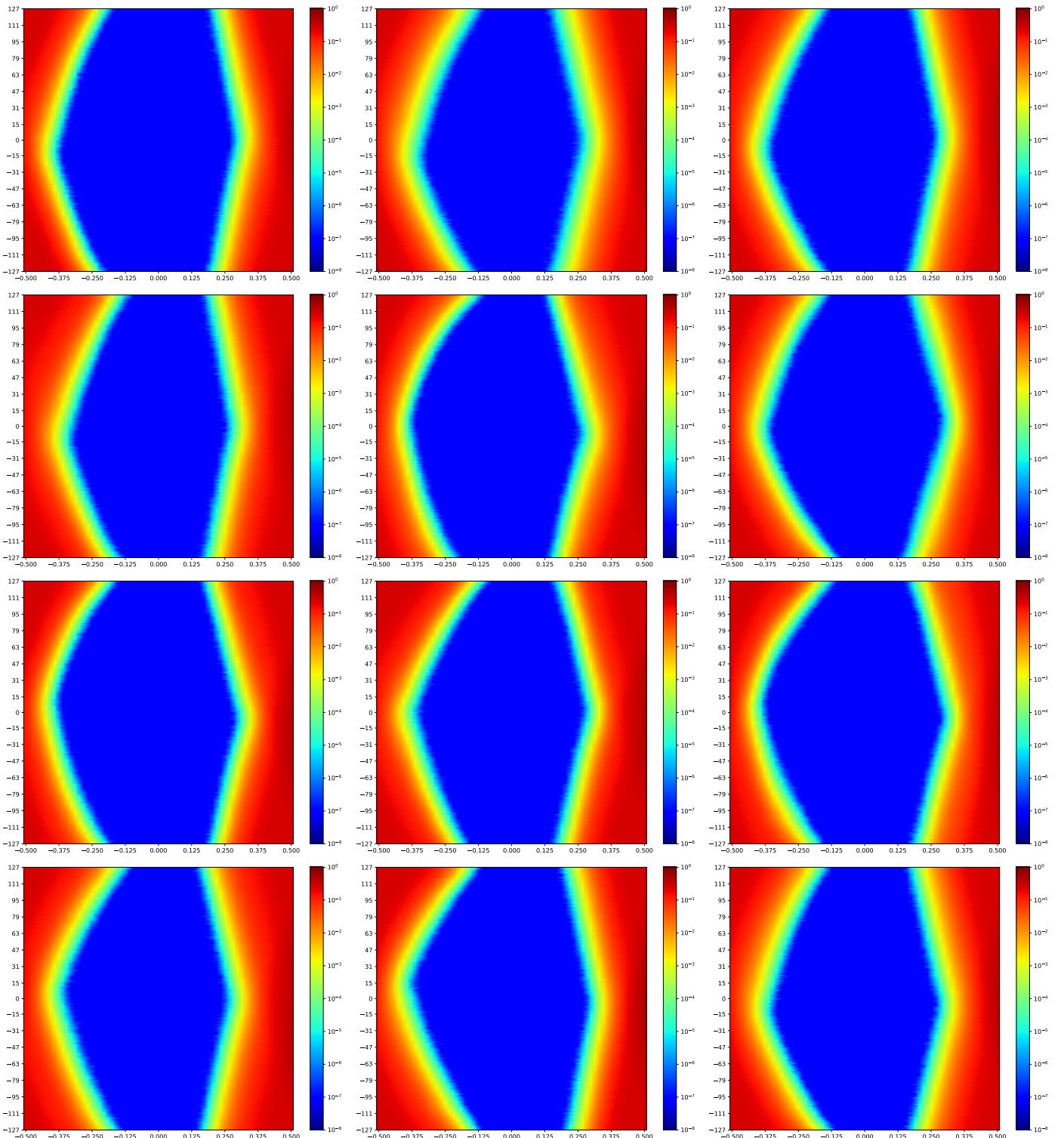


Figure 2.266: MSP\_C TX3 MSP\_A RX4 Minipod Loopback

A cross-reference to Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 2.279.

### 2.21.1 MSP\_C\_FPGA-TX3-00-RX4-00-MSP\_A\_FPGA

Table 2.246: MSP\_C\_FPGA-TX3-00-RX4-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:12:42		2018-Jan-24 22:13:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8227	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

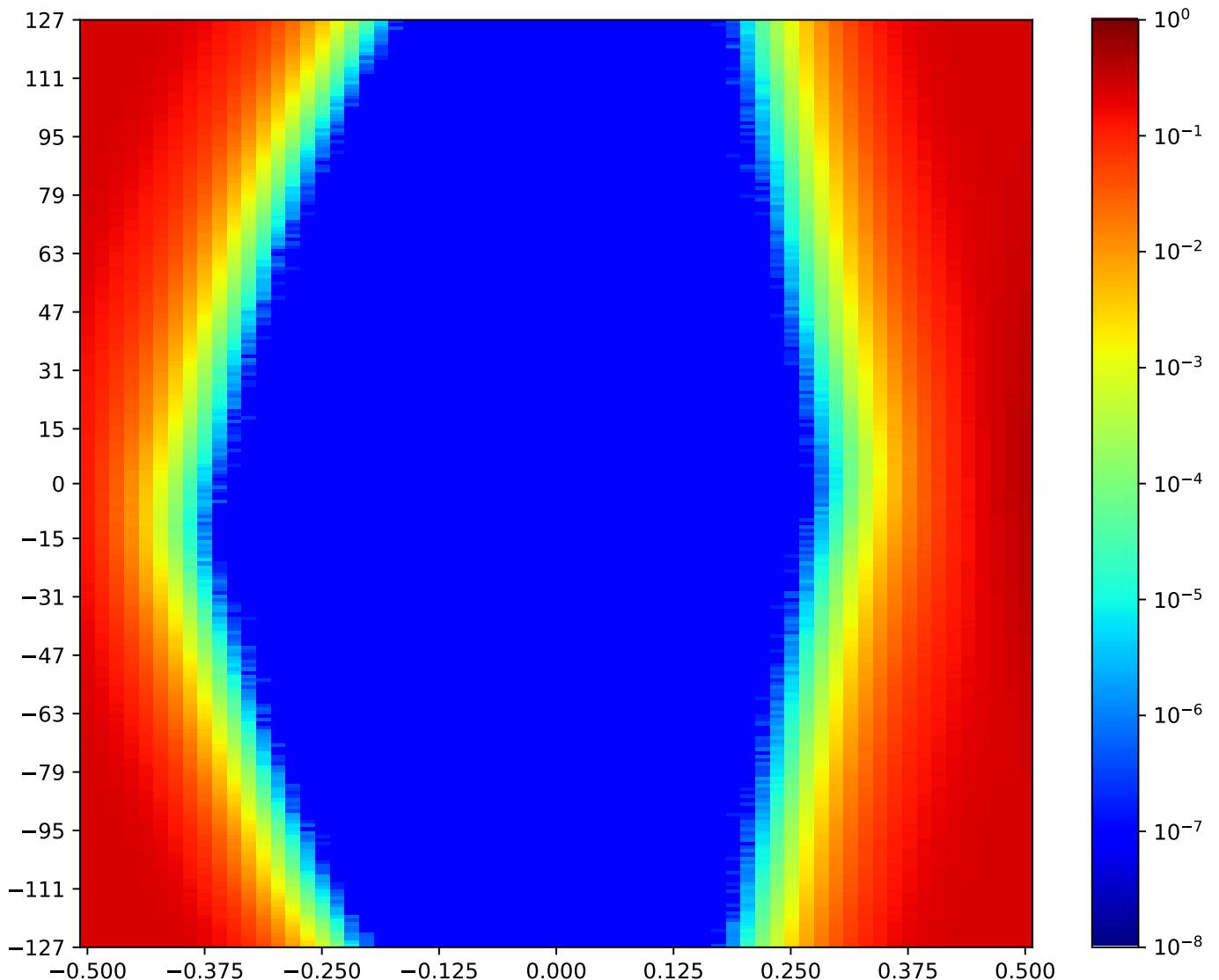


Figure 2.267: MSP\_C\_FPGA-TX3-00-RX4-00-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.2 MSP\_C\_FPGA-TX3-01-RX4-01-MSP\_A\_FPGA

Table 2.247: MSP\_C\_FPGA-TX3-01-RX4-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:13:42		2018-Jan-24 22:14:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6620	35	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

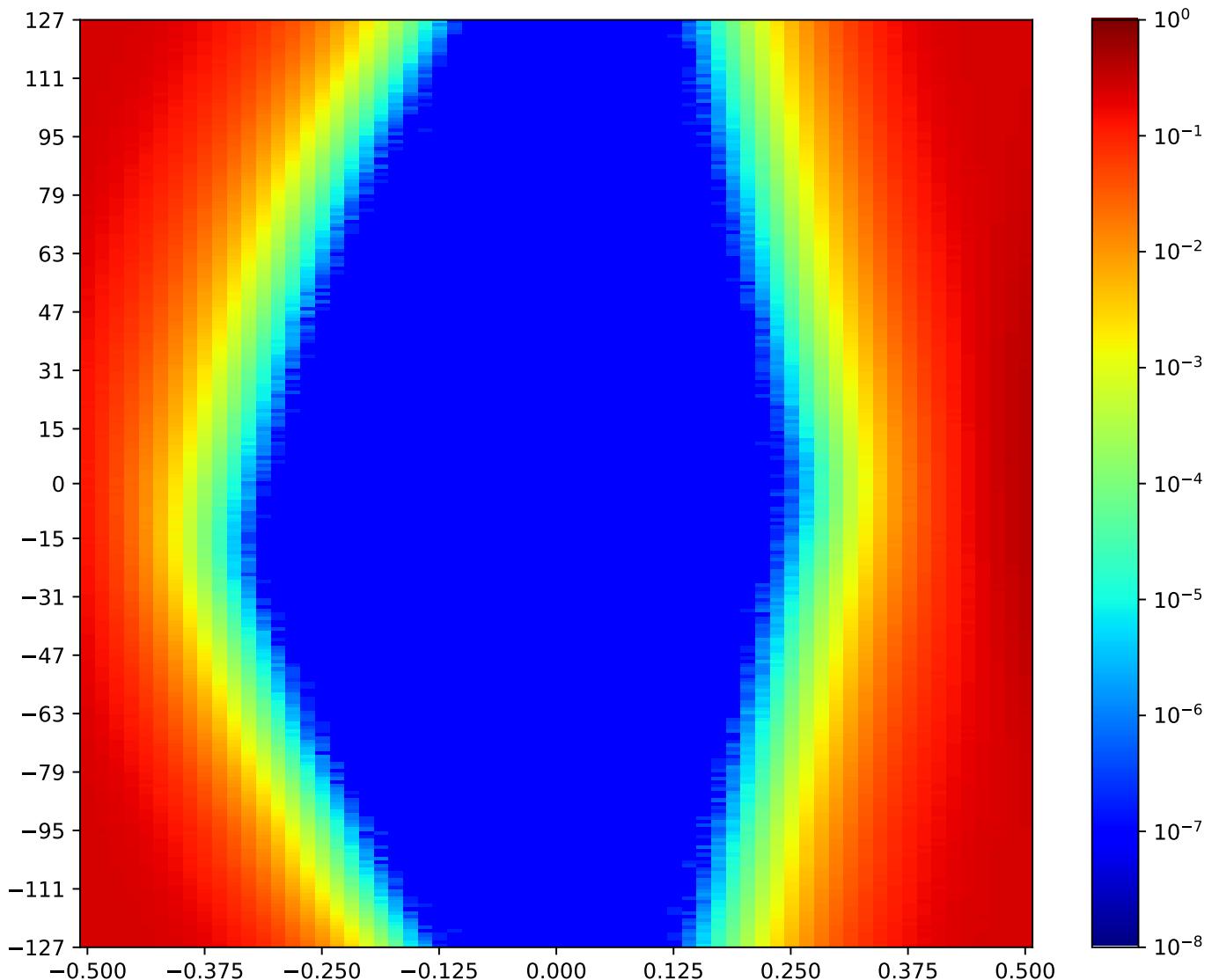


Figure 2.268: MSP\_C\_FPGA-TX3-01-RX4-01-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.21.3 MSP\_C\_FPGA-TX3-02-RX4-02-MSP\_A\_FPGA

Table 2.248: MSP\_C\_FPGA-TX3-02-RX4-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:14:12		2018-Jan-24 22:14:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7275	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

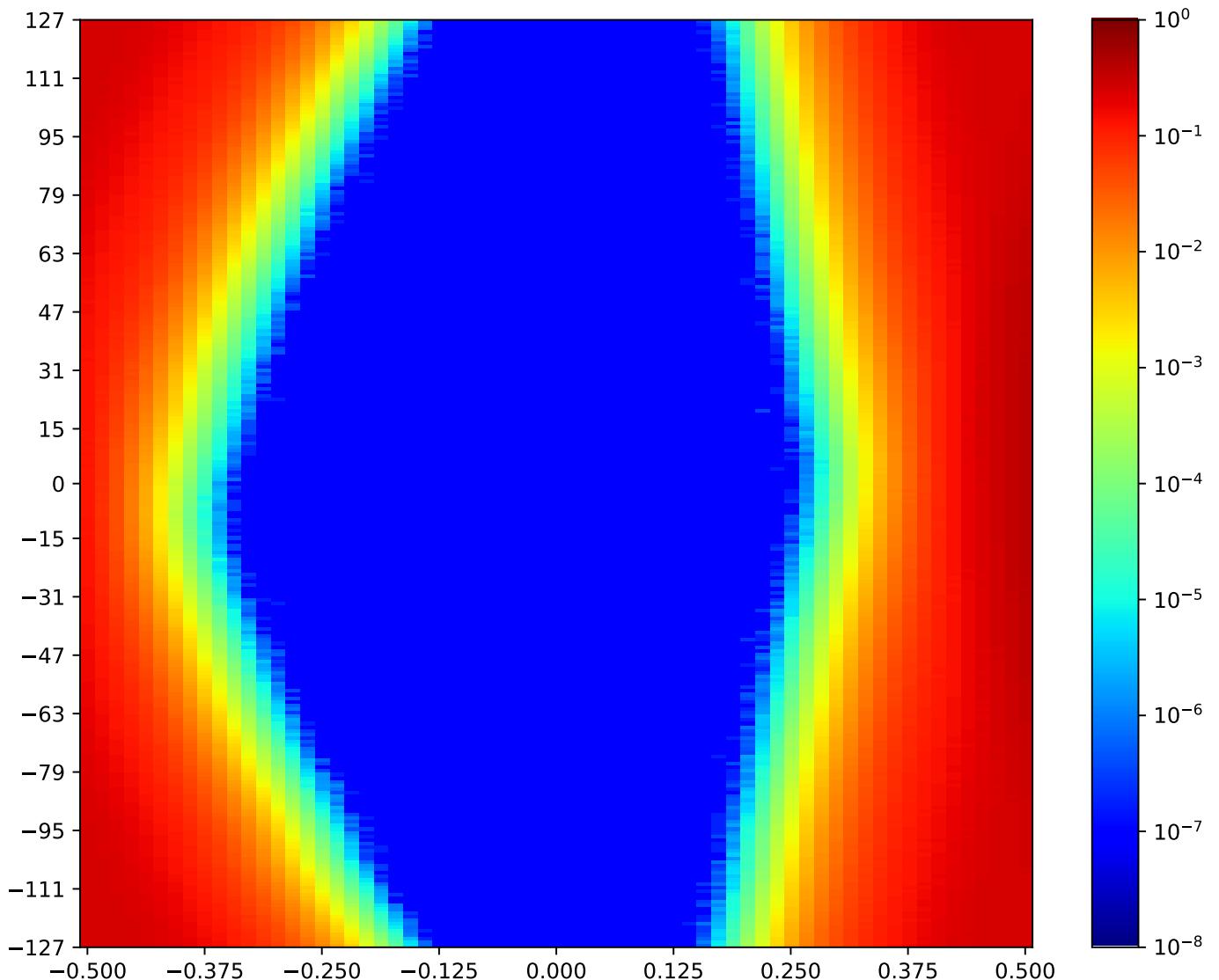


Figure 2.269: MSP\_C\_FPGA-TX3-02-RX4-02-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.4 MSP\_C\_FPGA-TX3-03-RX4-03-MSP\_A\_FPGA

Table 2.249: MSP\_C\_FPGA-TX3-03-RX4-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:11:44		2018-Jan-24 22:12:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6924	35	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

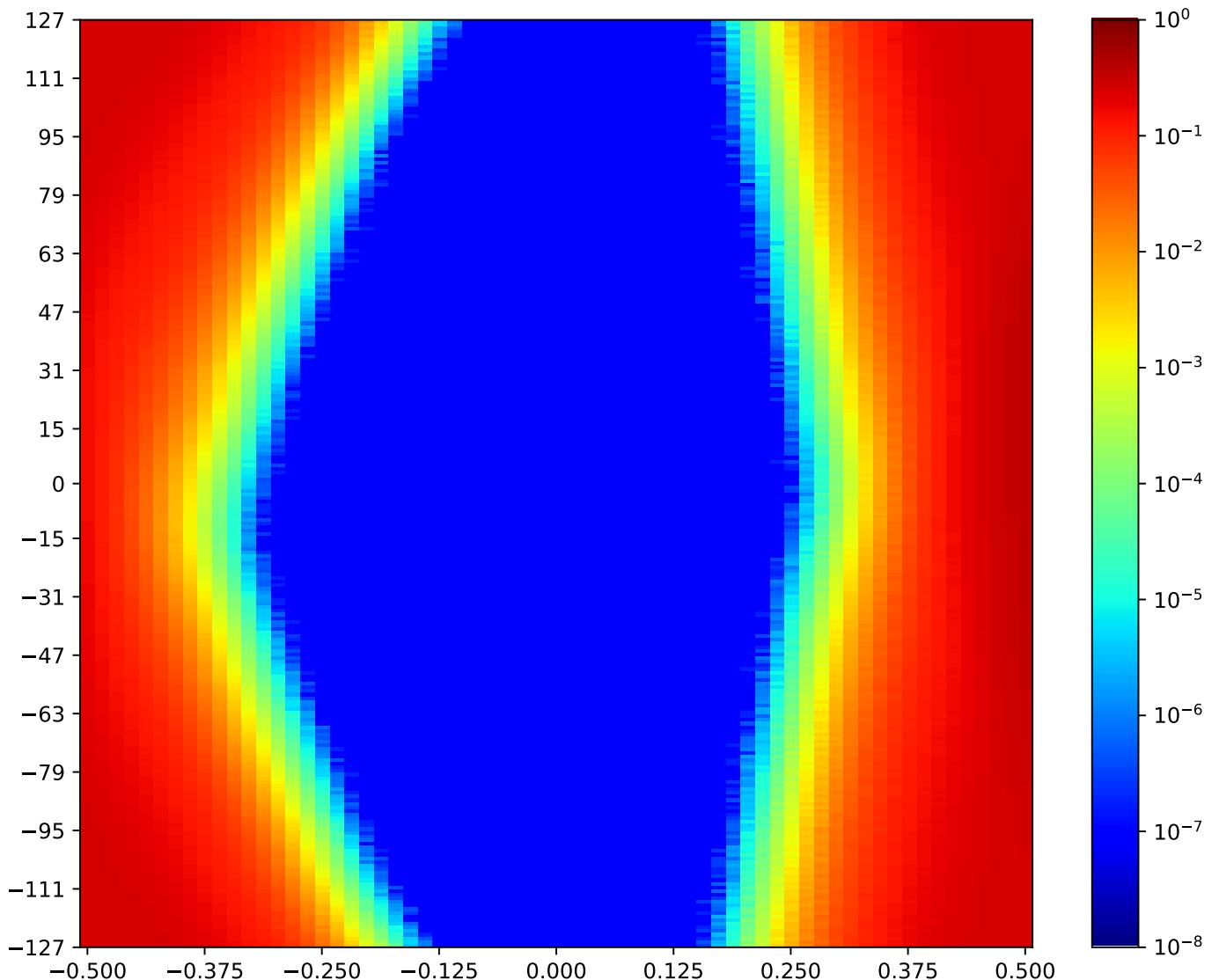


Figure 2.270: MSP\_C\_FPGA-TX3-03-RX4-03-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.5 MSP\_C\_FPGA-TX3-04-RX4-04-MSP\_A\_FPGA

Table 2.250: MSP\_C\_FPGA-TX3-04-RX4-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:15:43		2018-Jan-24 22:16:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7393	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

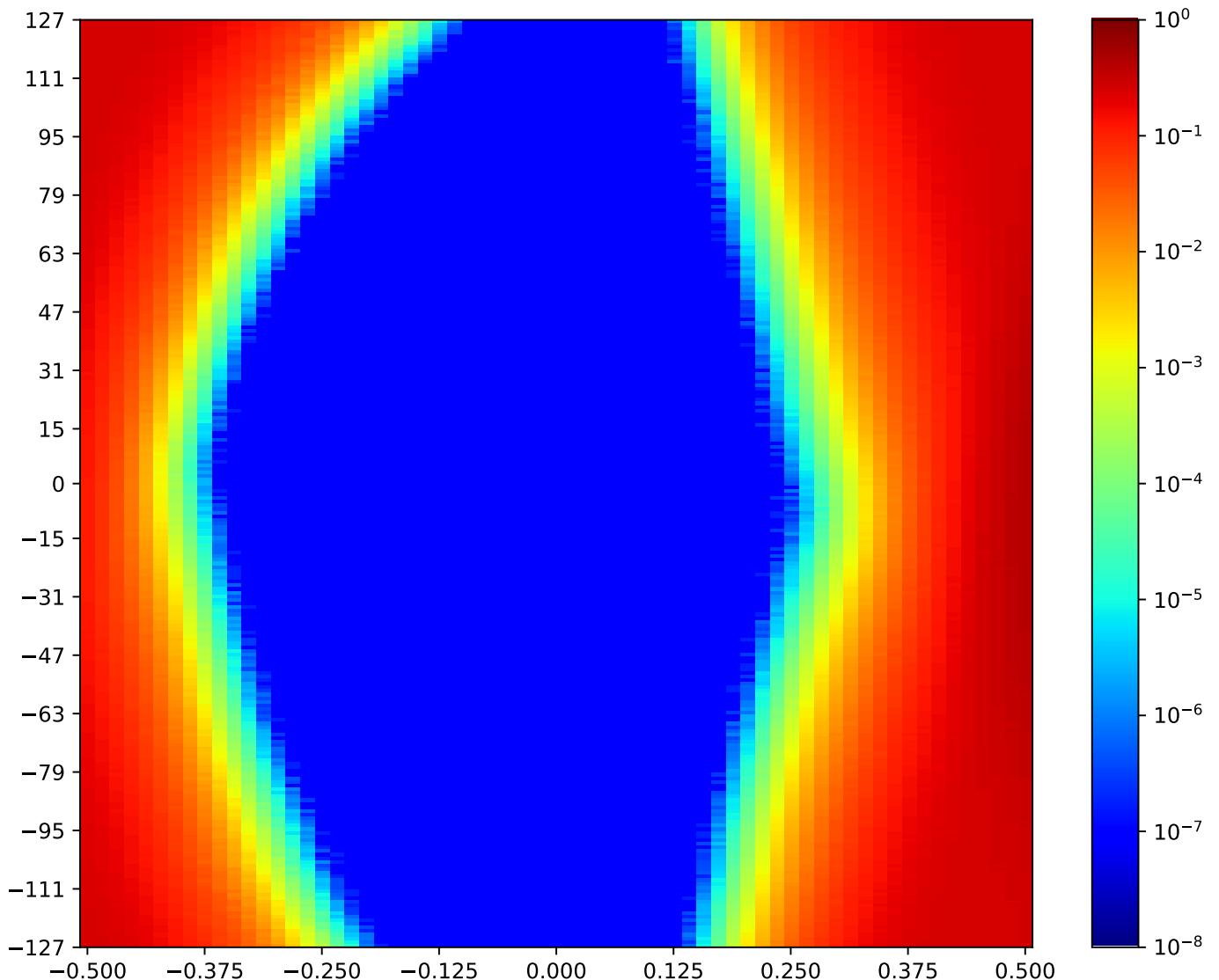


Figure 2.271: MSP\_C\_FPGA-TX3-04-RX4-04-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.6 MSP\_C\_FPGA-TX3-05-RX4-05-MSP\_A\_FPGA

Table 2.251: MSP\_C\_FPGA-TX3-05-RX4-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:11:14		2018-Jan-24 22:11:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7236	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

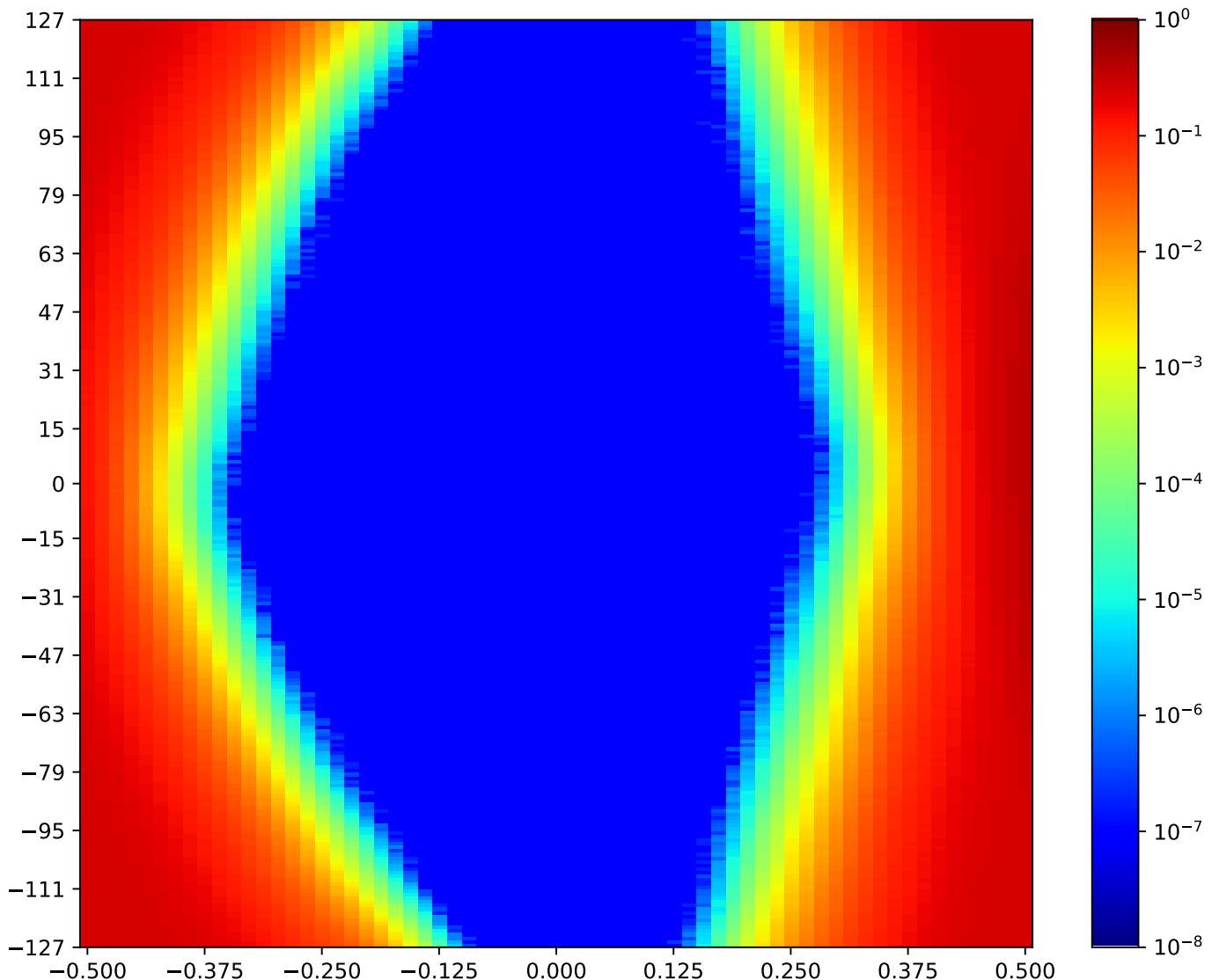


Figure 2.272: MSP\_C\_FPGA-TX3-05-RX4-05-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.7 MSP\_C\_FPGA-TX3-06-RX4-06-MSP\_A\_FPGA

Table 2.252: MSP\_C\_FPGA-TX3-06-RX4-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:16:43		2018-Jan-24 22:17:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8183	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

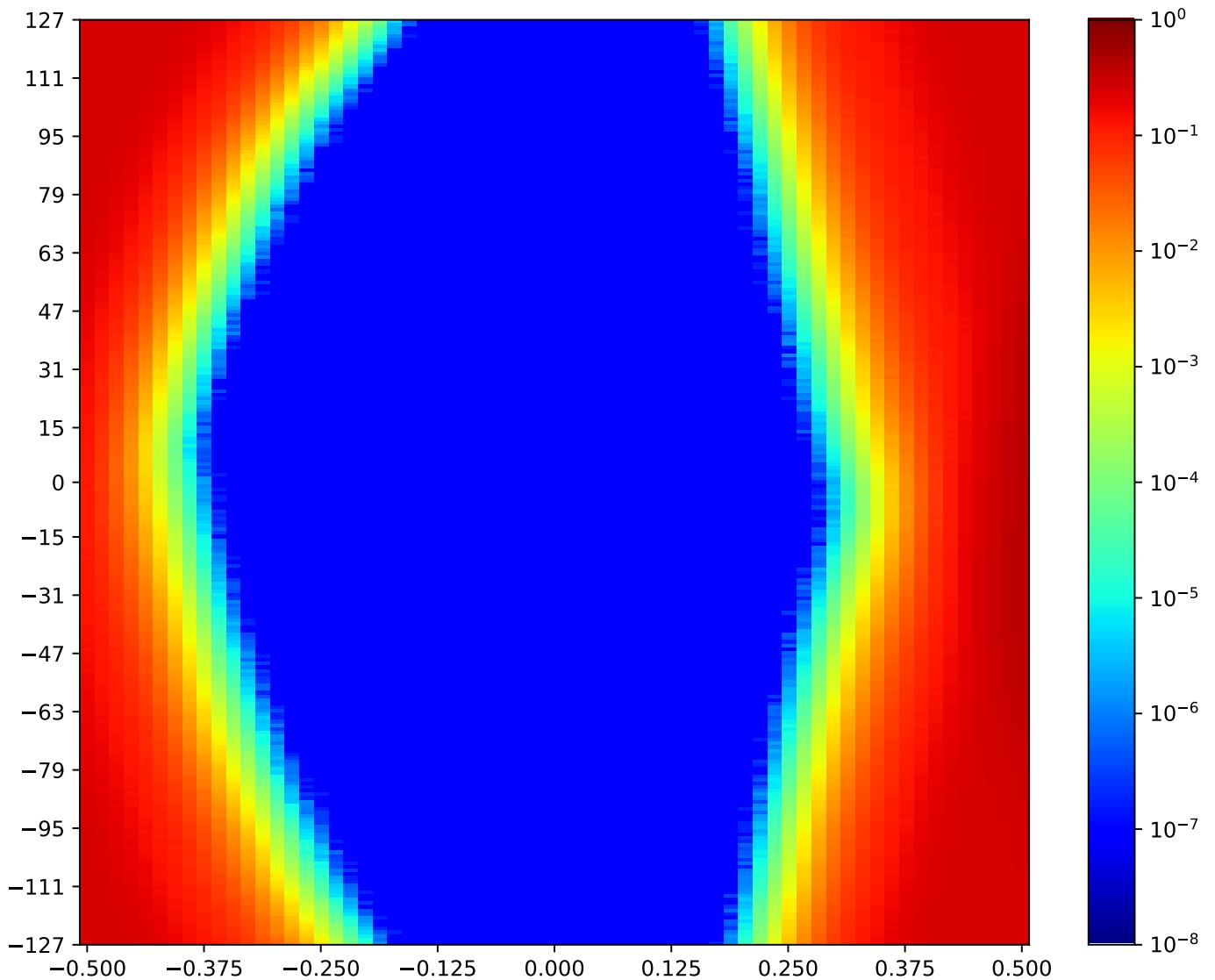


Figure 2.273: MSP\_C\_FPGA-TX3-06-RX4-06-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.8 MSP\_C\_FPGA-TX3-07-RX4-07-MSP\_A\_FPGA

Table 2.253: MSP\_C\_FPGA-TX3-07-RX4-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:12:13		2018-Jan-24 22:12:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7214	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

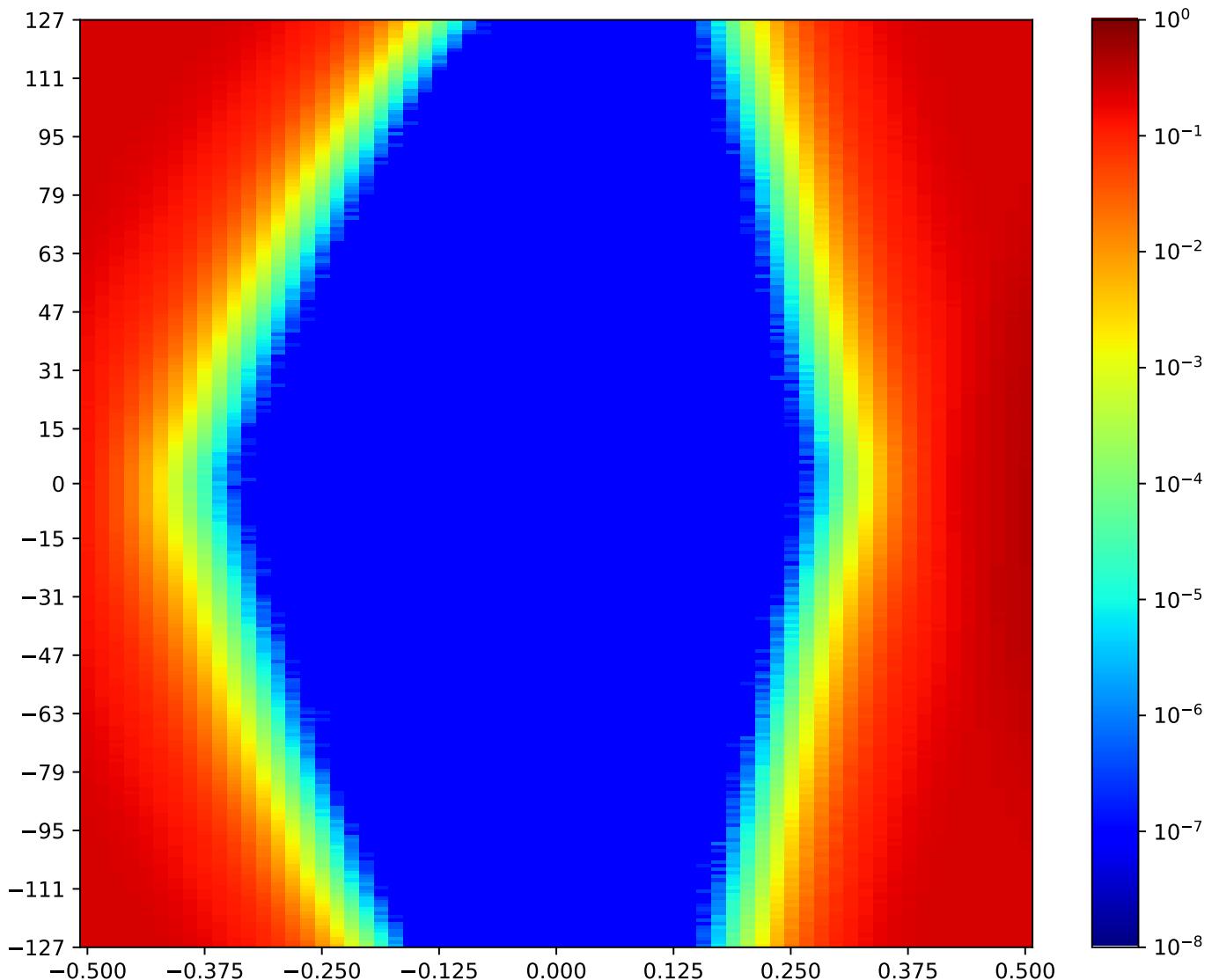


Figure 2.274: MSP\_C\_FPGA-TX3-07-RX4-07-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.9 MSP\_C\_FPGA-TX3-08-RX4-08-MSP\_A\_FPGA

Table 2.254: MSP\_C\_FPGA-TX3-08-RX4-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:16:13		2018-Jan-24 22:16:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7860	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

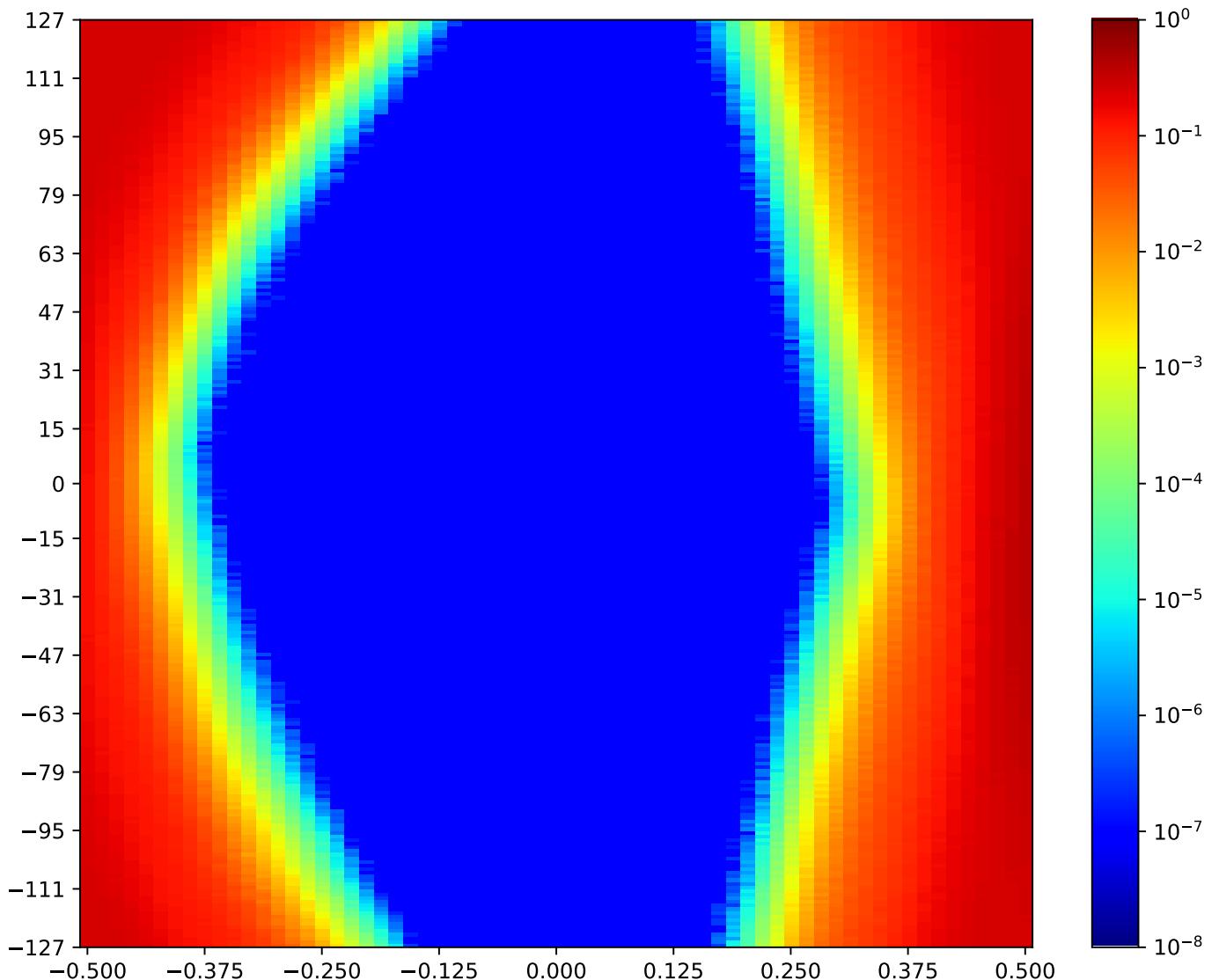


Figure 2.275: MSP\_C\_FPGA-TX3-08-RX4-08-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.10 MSP\_C\_FPGA-TX3-09-RX4-09-MSP\_A\_FPGA

Table 2.255: MSP\_C\_FPGA-TX3-09-RX4-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:13:12		2018-Jan-24 22:13:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6980	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

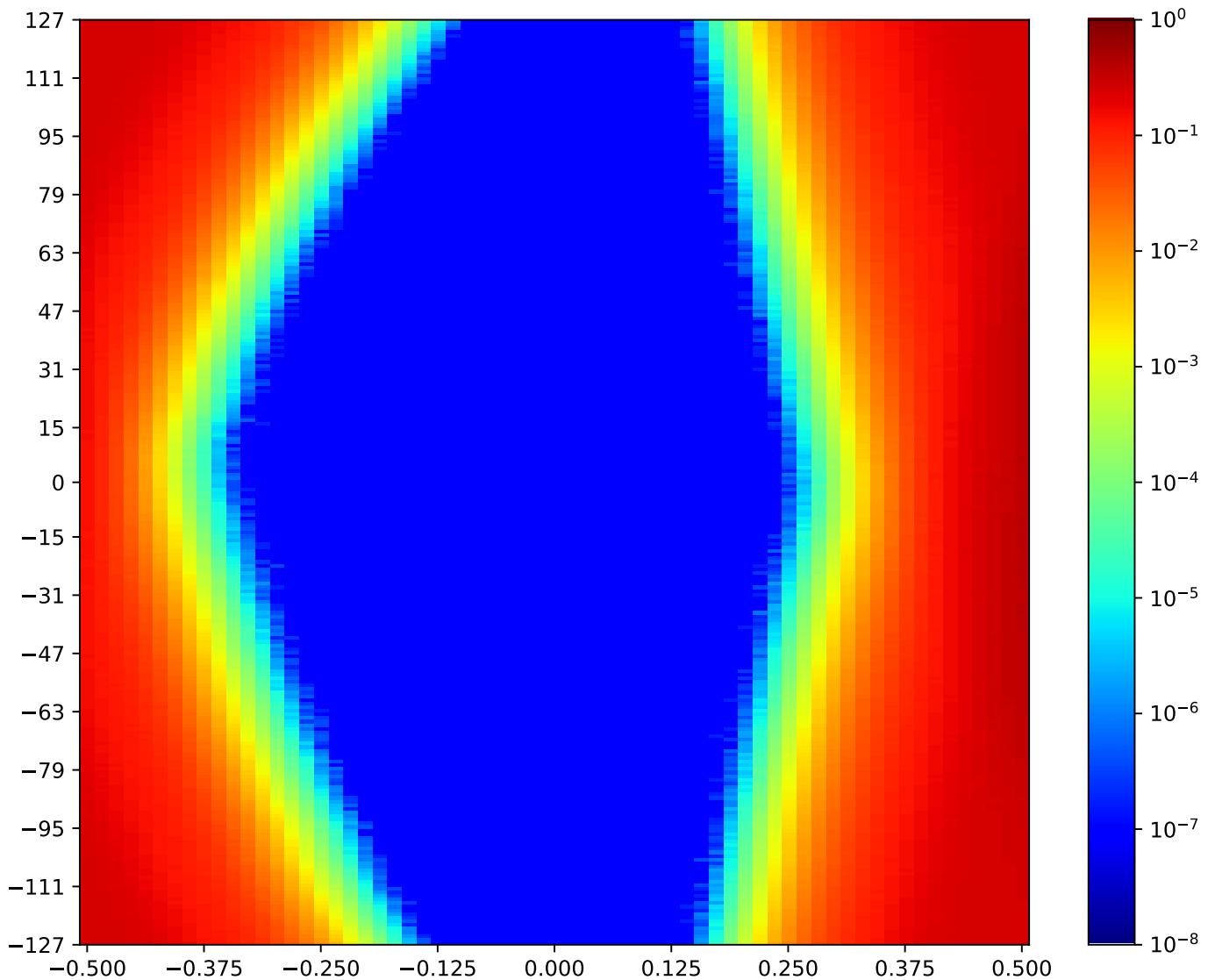


Figure 2.276: MSP\_C\_FPGA-TX3-09-RX4-09-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.11 MSP\_C\_FPGA-TX3-10-RX4-10-MSP\_A\_FPGA

Table 2.256: MSP\_C\_FPGA-TX3-10-RX4-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:15:12		2018-Jan-24 22:15:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7695	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

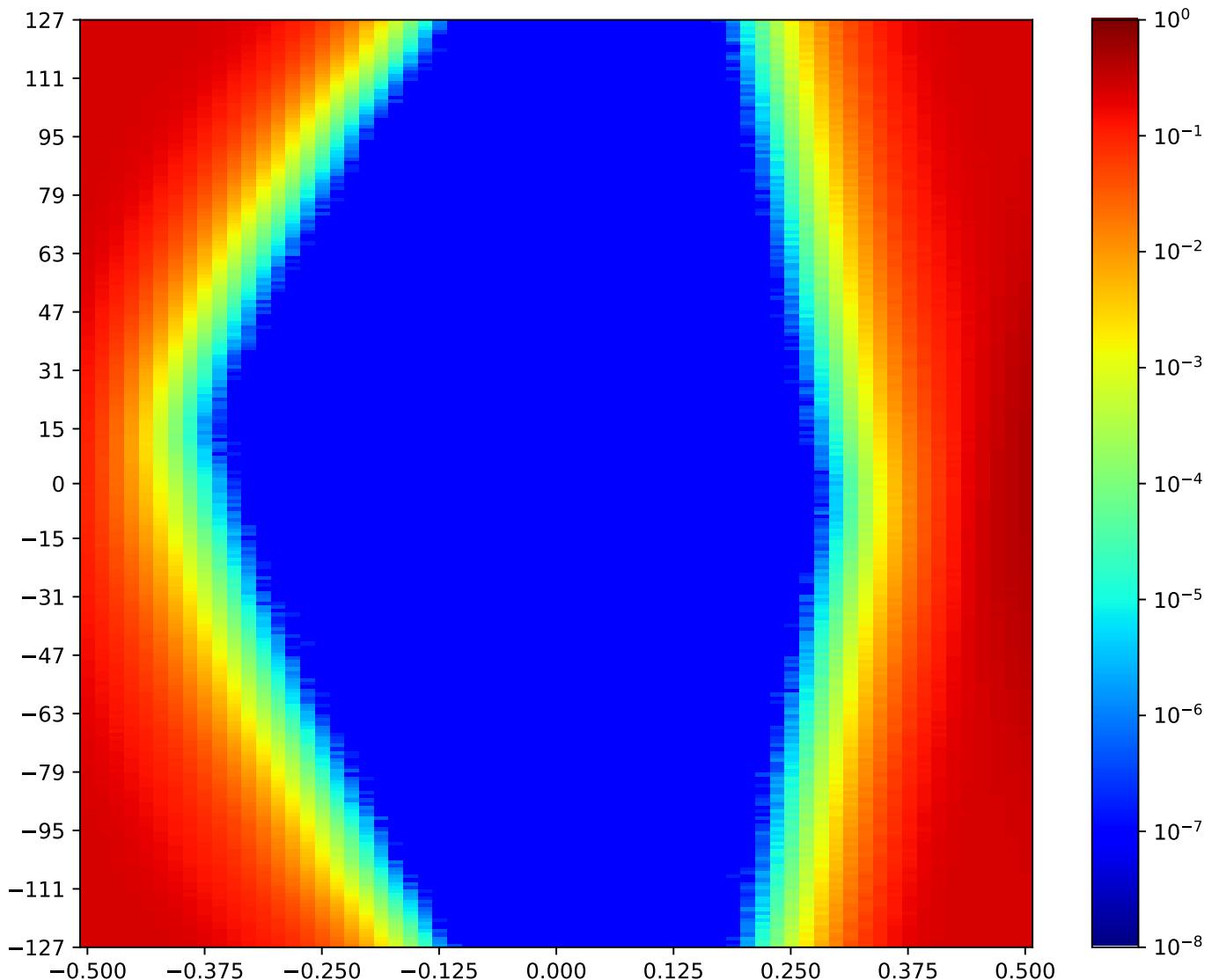


Figure 2.277: MSP\_C\_FPGA-TX3-10-RX4-10-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.21.12 MSP\_C\_FPGA-TX3-11-RX4-11-MSP\_A\_FPGA

Table 2.257: MSP\_C\_FPGA-TX3-11-RX4-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:14:42		2018-Jan-24 22:15:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7257	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

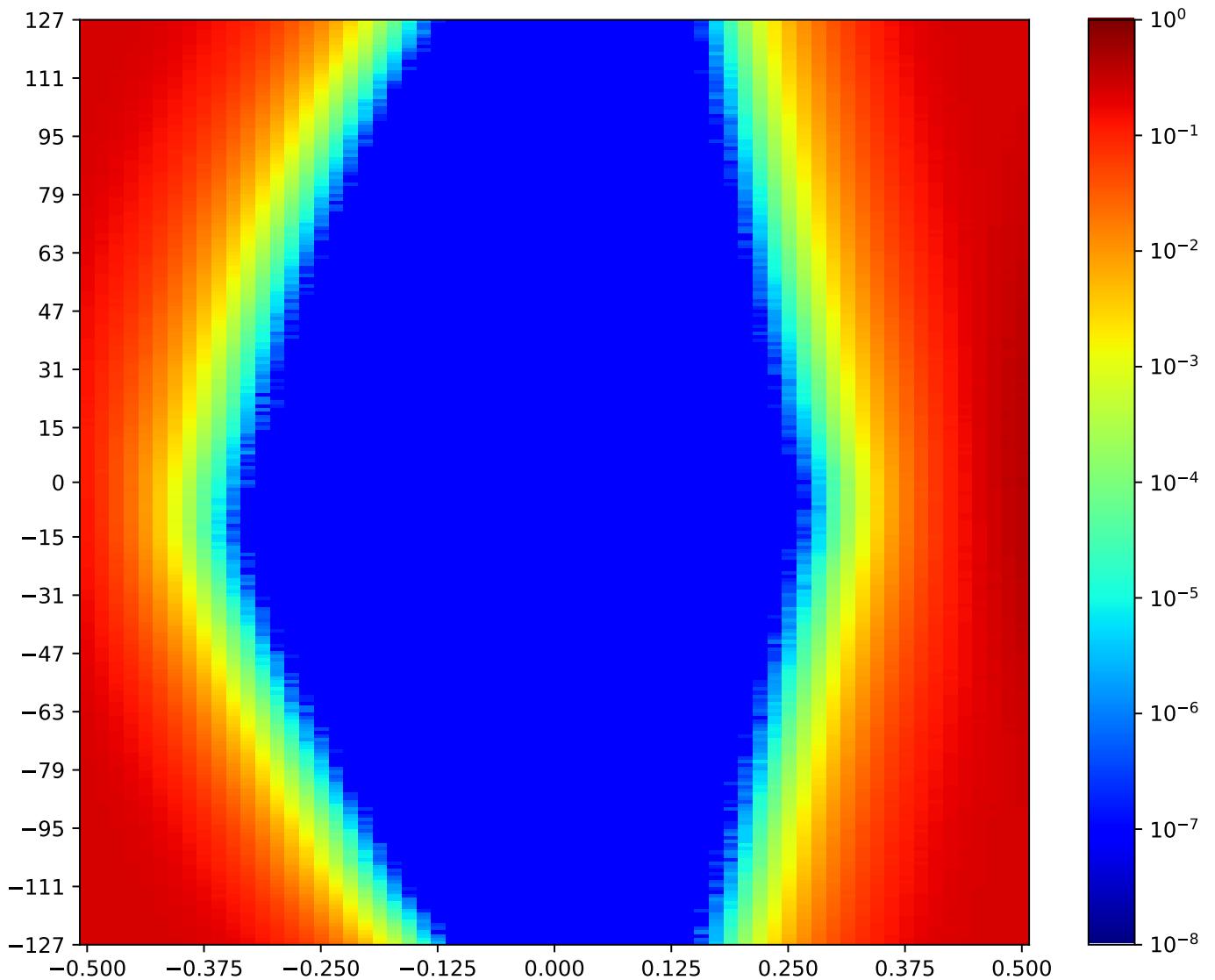


Figure 2.278: MSP\_C\_FPGA-TX3-11-RX4-11-MSP\_A\_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22 MSP\_C TX4 MSP\_A RX3 Minipod Loopback

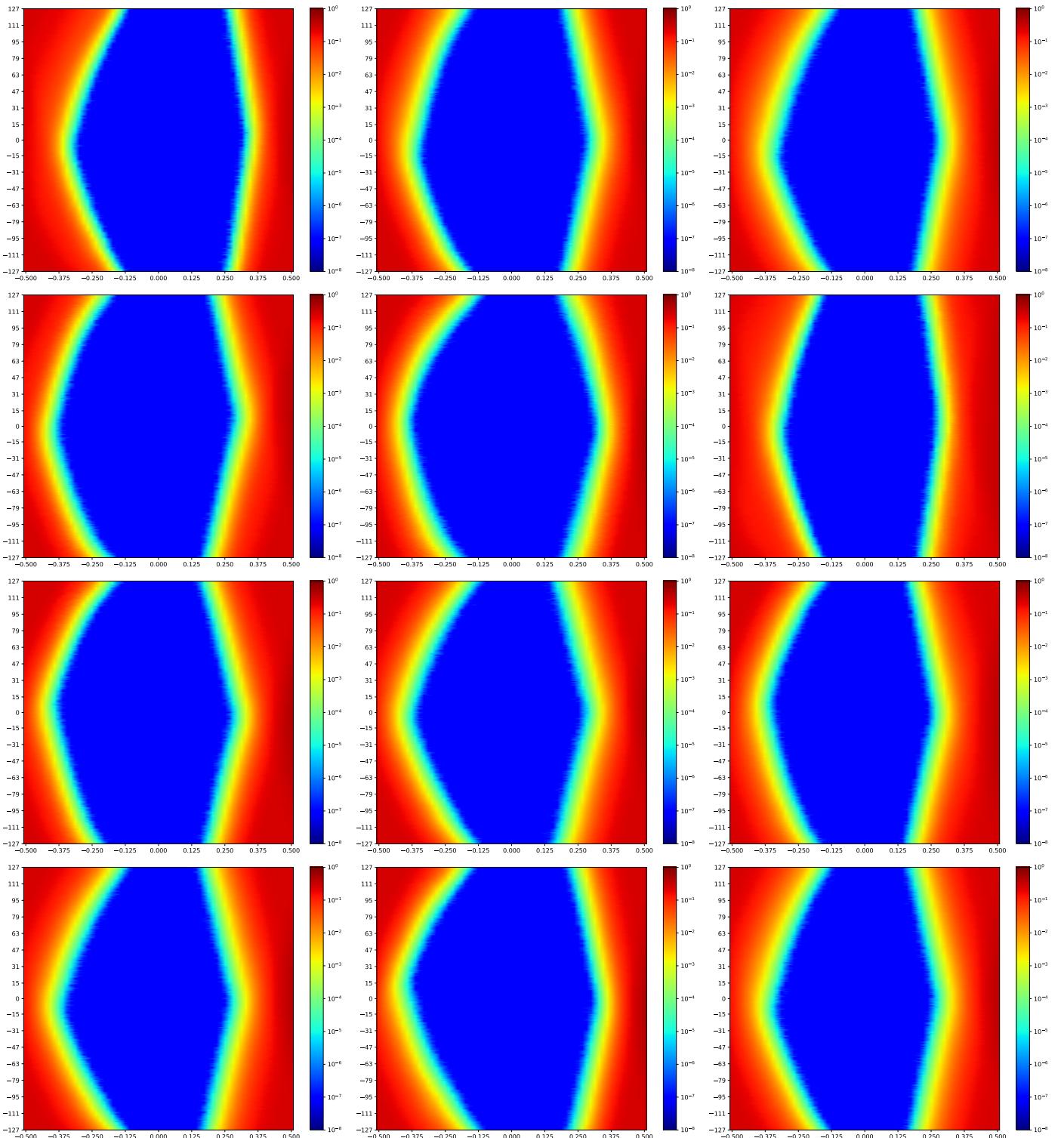


Figure 2.279: MSP\_C TX4 MSP\_A RX3 Minipod Loopback

A cross-reference to Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.  
Next summary Figure 3.1.

### 2.22.1 MSP\_C\_FPGA-TX4-00-RX3-00-MSP\_A\_FPGA

Table 2.258: MSP\_C\_FPGA-TX4-00-RX3-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:18:42		2018-Jan-24 22:19:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8018	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

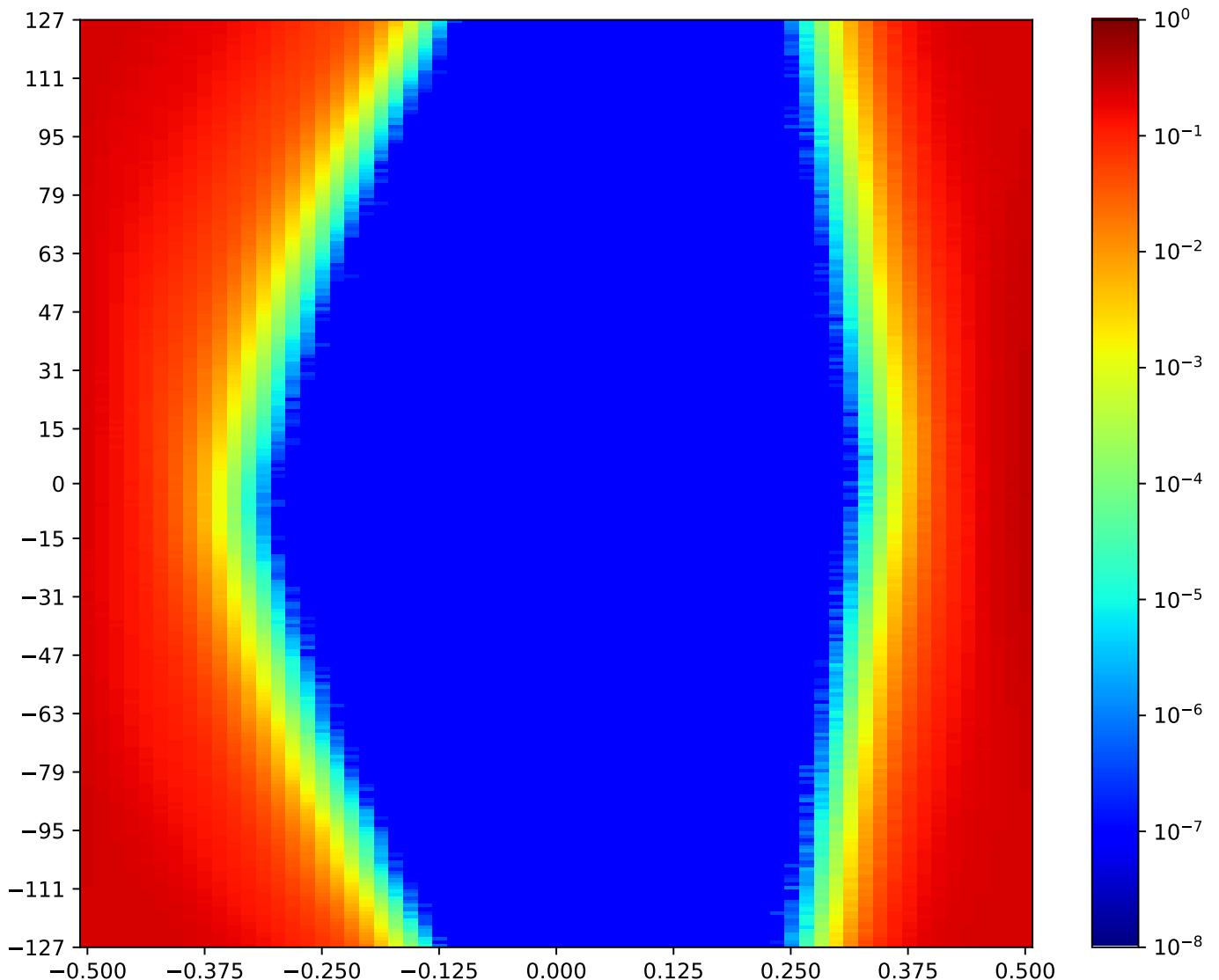


Figure 2.280: MSP\_C\_FPGA-TX4-00-RX3-00-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.2 MSP\_C\_FPGA-TX4-01-RX3-01-MSP\_A\_FPGA

Table 2.259: MSP\_C\_FPGA-TX4-01-RX3-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:17:42		2018-Jan-24 22:18:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7591	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

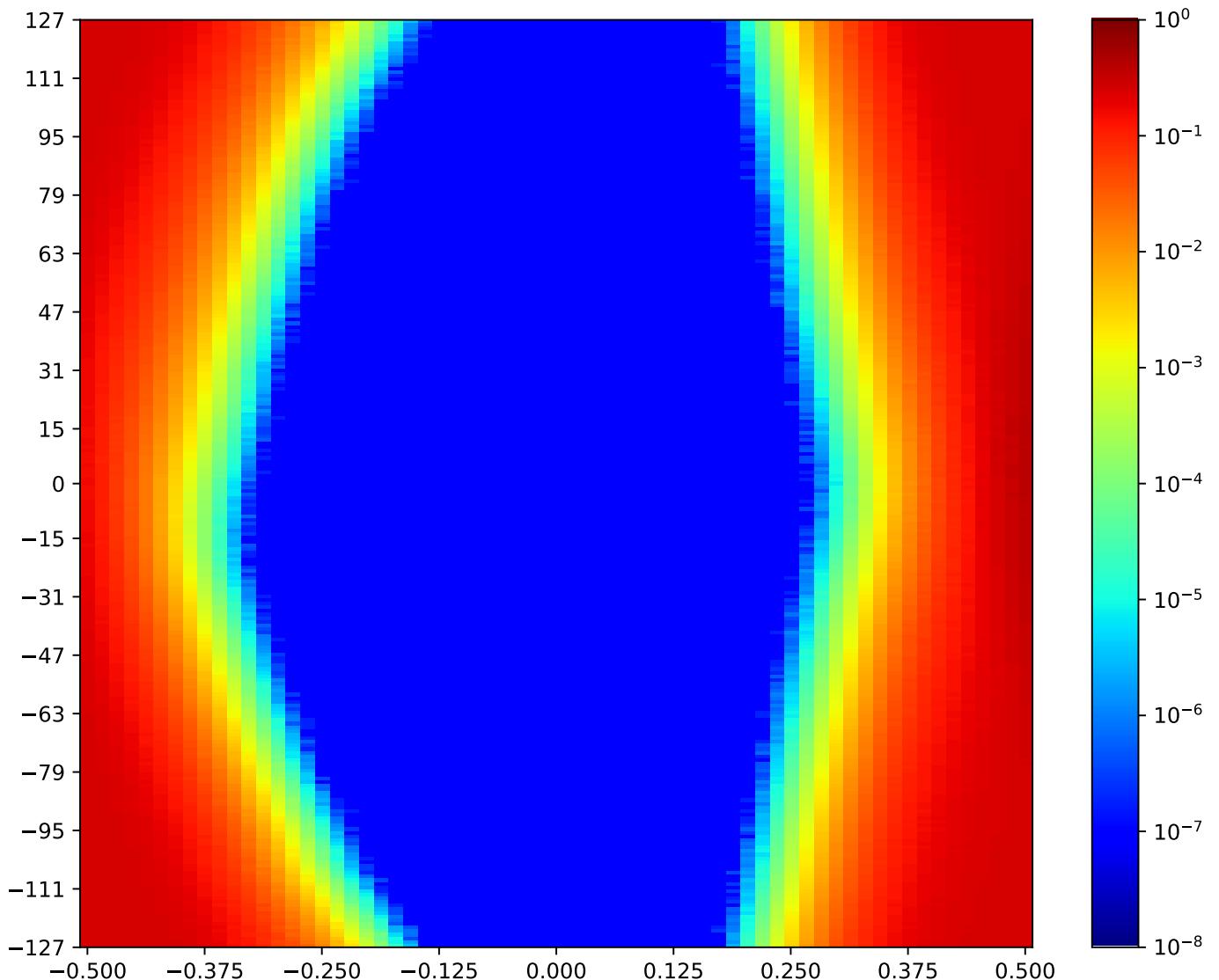


Figure 2.281: MSP\_C\_FPGA-TX4-01-RX3-01-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

### 2.22.3 MSP\_C\_FPGA-TX4-02-RX3-02-MSP\_A\_FPGA

Table 2.260: MSP\_C\_FPGA-TX4-02-RX3-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:20:11		2018-Jan-24 22:20:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6881	35	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

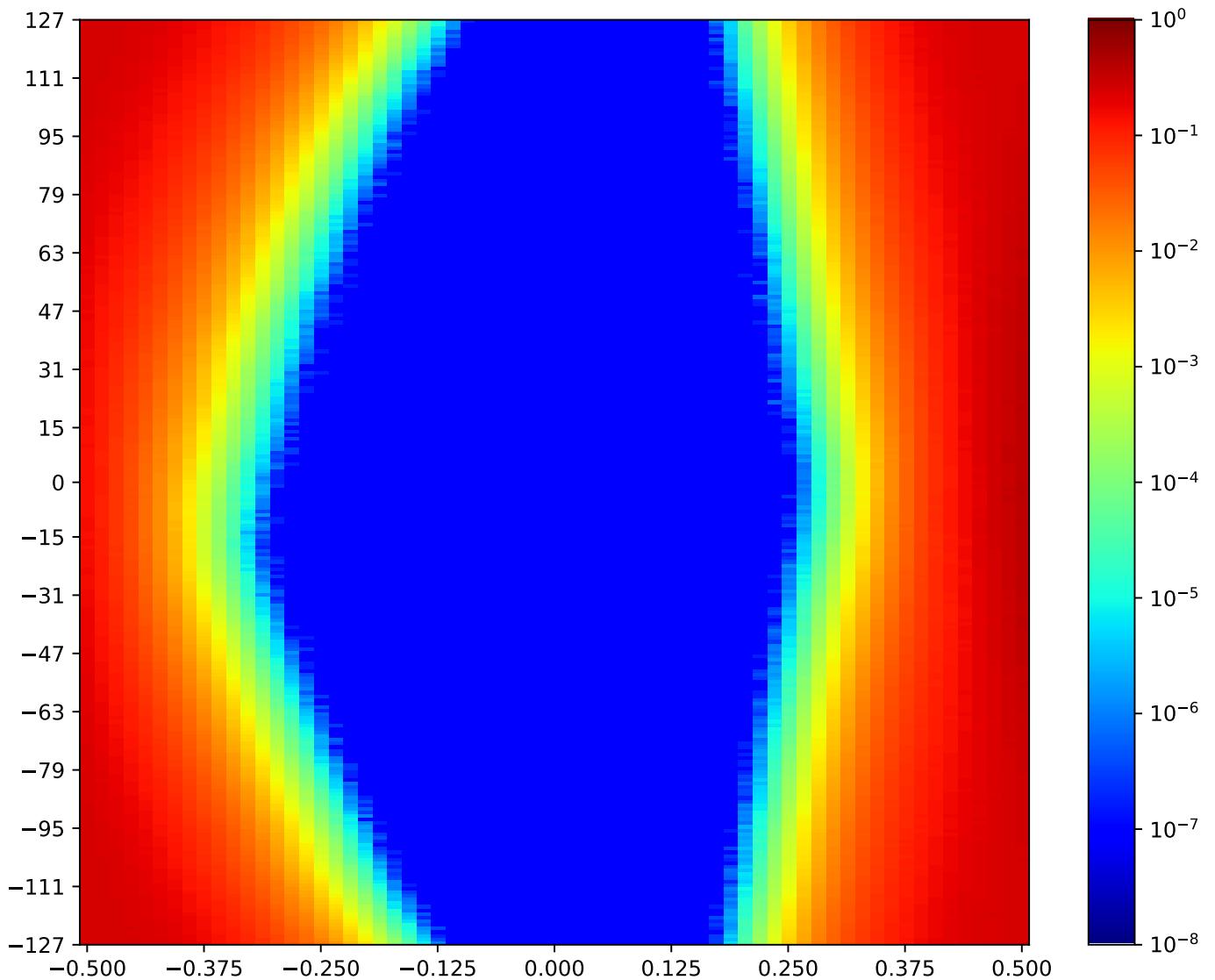


Figure 2.282: MSP\_C\_FPGA-TX4-02-RX3-02-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.4 MSP\_C\_FPGA-TX4-03-RX3-03-MSP\_A\_FPGA

Table 2.261: MSP\_C\_FPGA-TX4-03-RX3-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:17:13		2018-Jan-24 22:17:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7993	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

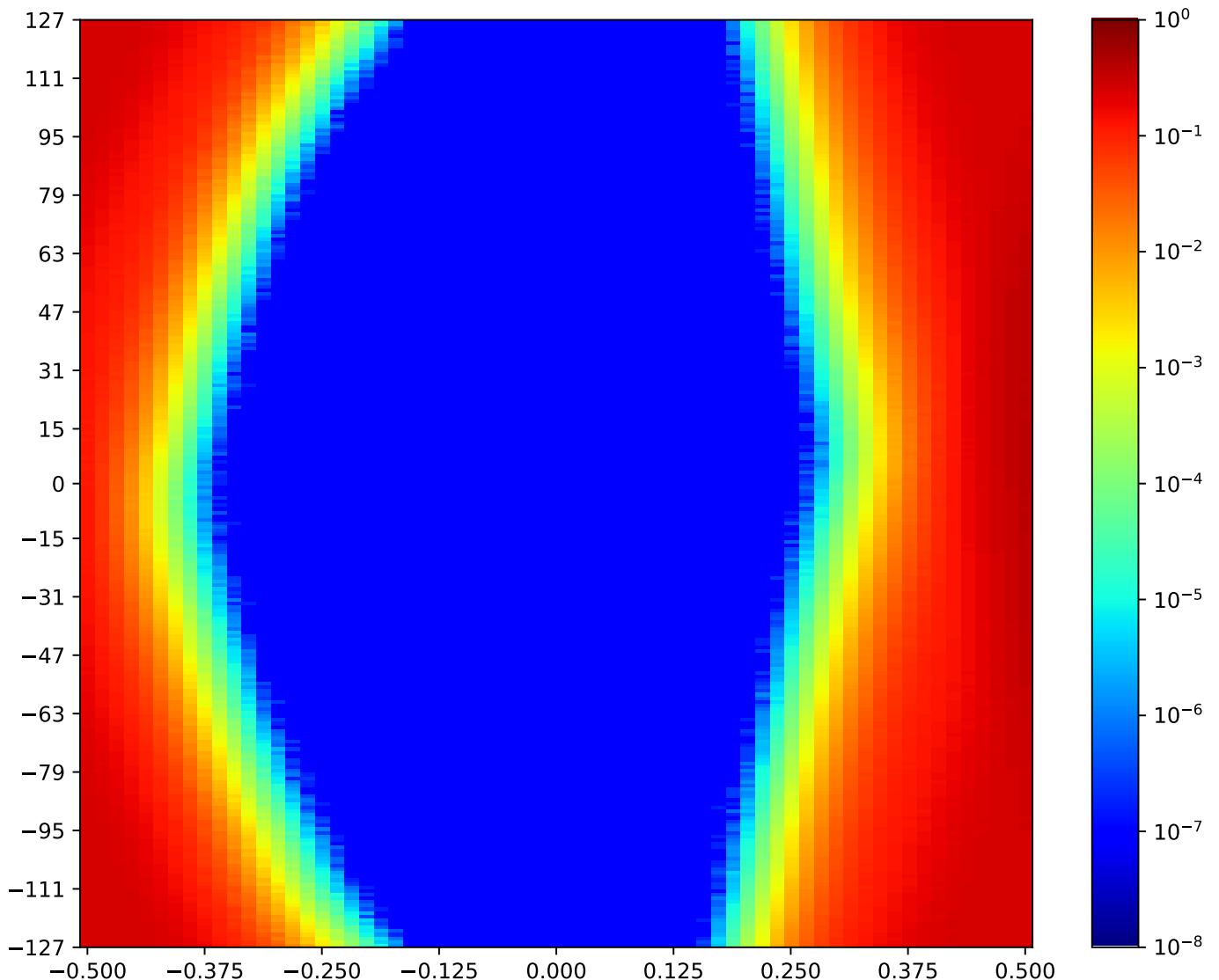


Figure 2.283: MSP\_C\_FPGA-TX4-03-RX3-03-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.5 MSP\_C\_FPGA-TX4-04-RX3-04-MSP\_A\_FPGA

Table 2.262: MSP\_C\_FPGA-TX4-04-RX3-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:21:40		2018-Jan-24 22:22:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8154	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

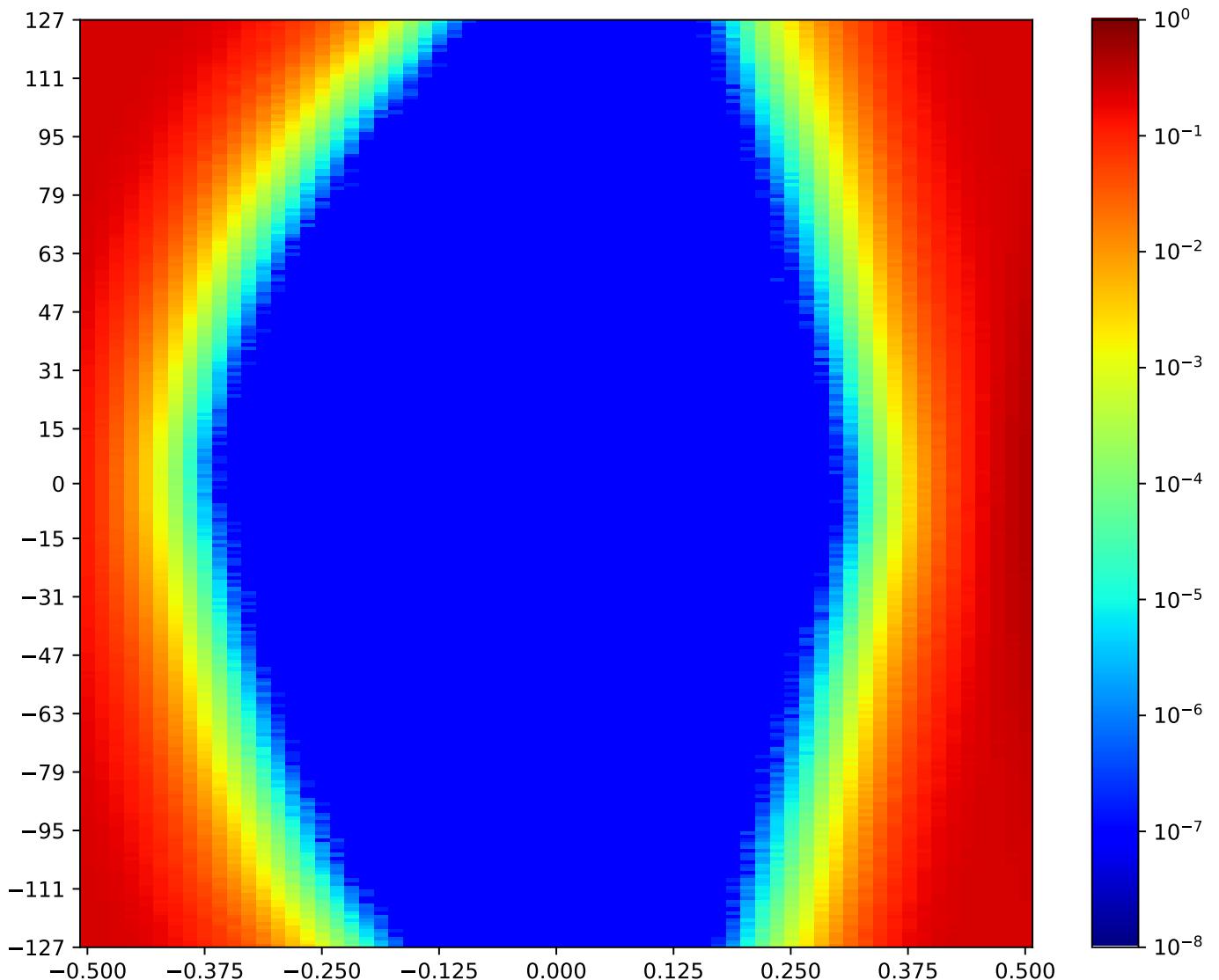


Figure 2.284: MSP\_C\_FPGA-TX4-04-RX3-04-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.6 MSP\_C\_FPGA-TX4-05-RX3-05-MSP\_A\_FPGA

Table 2.263: MSP\_C\_FPGA-TX4-05-RX3-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:18:12		2018-Jan-24 22:18:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7222	33	50.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

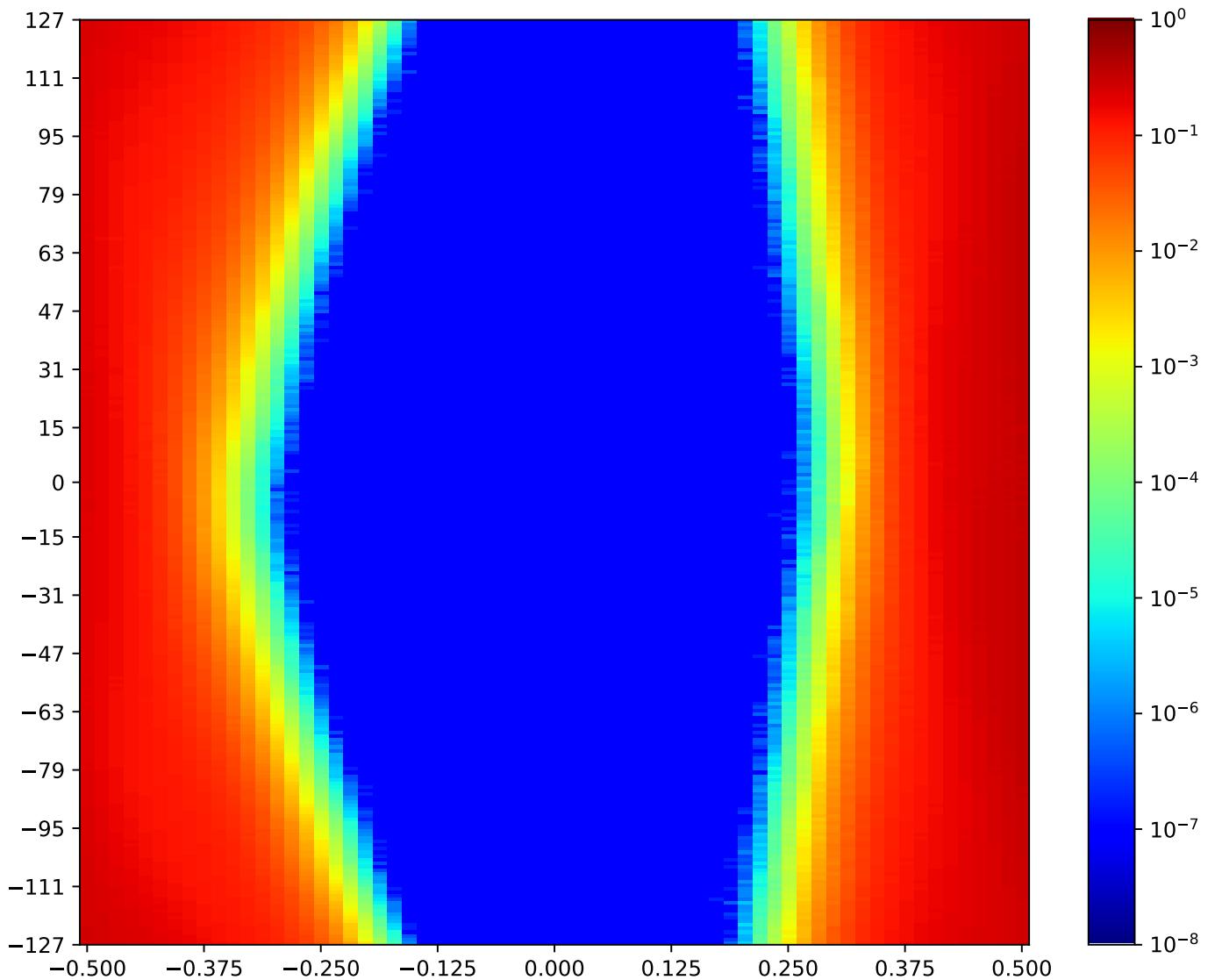


Figure 2.285: MSP\_C\_FPGA-TX4-05-RX3-05-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.7 MSP\_C\_FPGA-TX4-06-RX3-06-MSP\_A\_FPGA

Table 2.264: MSP\_C\_FPGA-TX4-06-RX3-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:22:40		2018-Jan-24 22:23:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7860	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

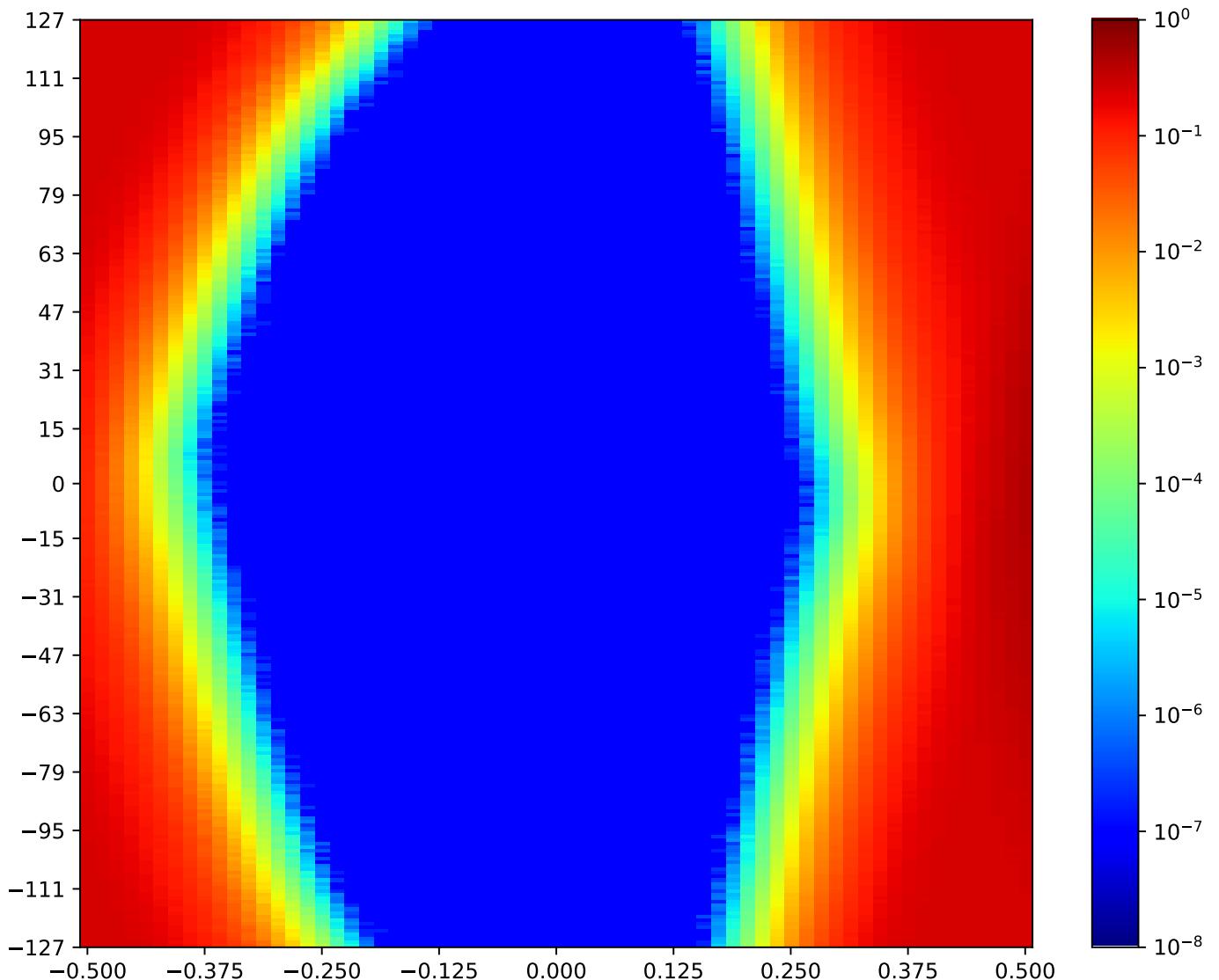


Figure 2.286: MSP\_C\_FPGA-TX4-06-RX3-06-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.8 MSP\_C\_FPGA-TX4-07-RX3-07-MSP\_A\_FPGA

Table 2.265: MSP\_C\_FPGA-TX4-07-RX3-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:19:12		2018-Jan-24 22:19:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7064	38	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

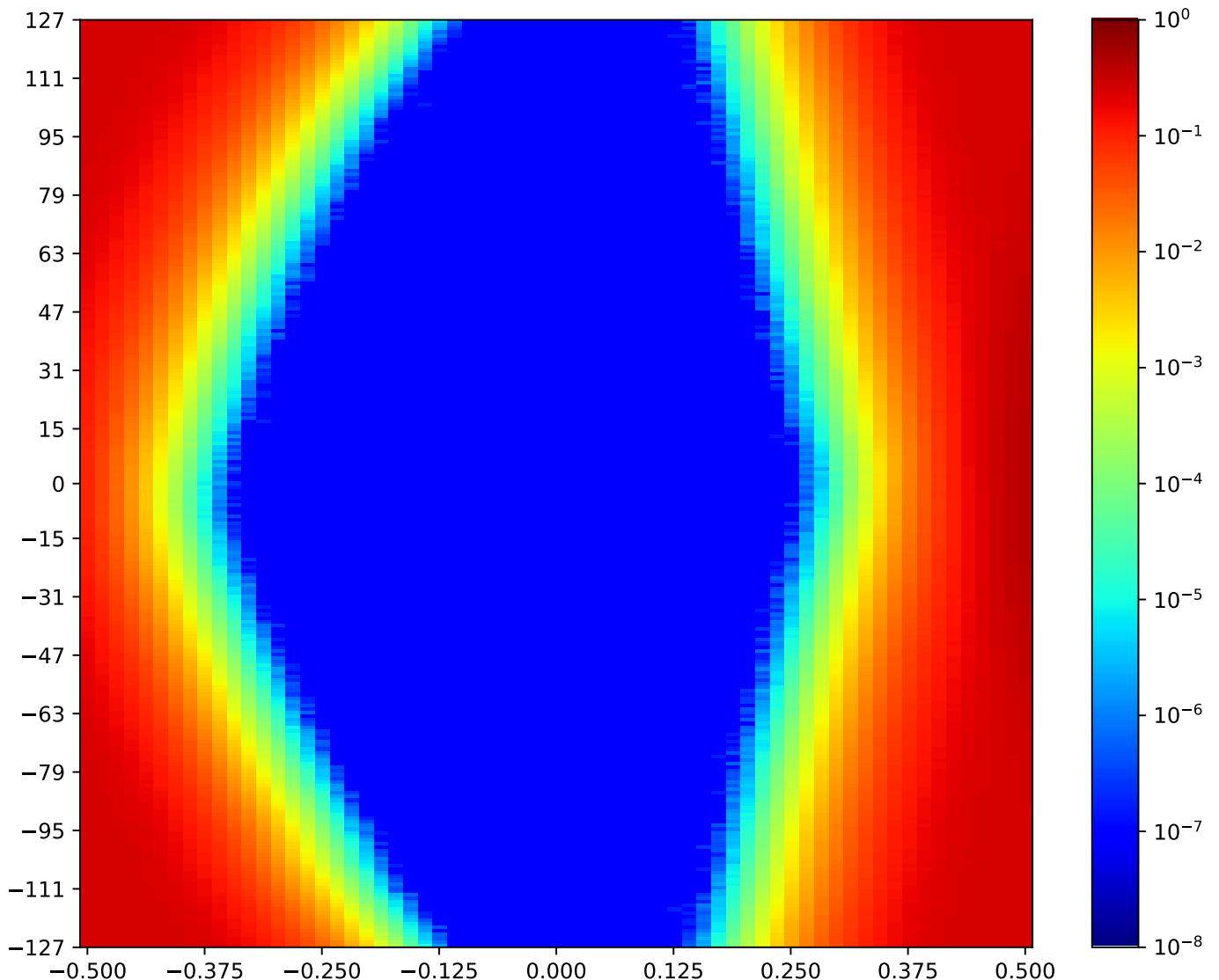


Figure 2.287: MSP\_C\_FPGA-TX4-07-RX3-07-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.9 MSP\_C\_FPGA-TX4-08-RX3-08-MSP\_A\_FPGA

Table 2.266: MSP\_C\_FPGA-TX4-08-RX3-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:22:11		2018-Jan-24 22:22:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7128	36	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

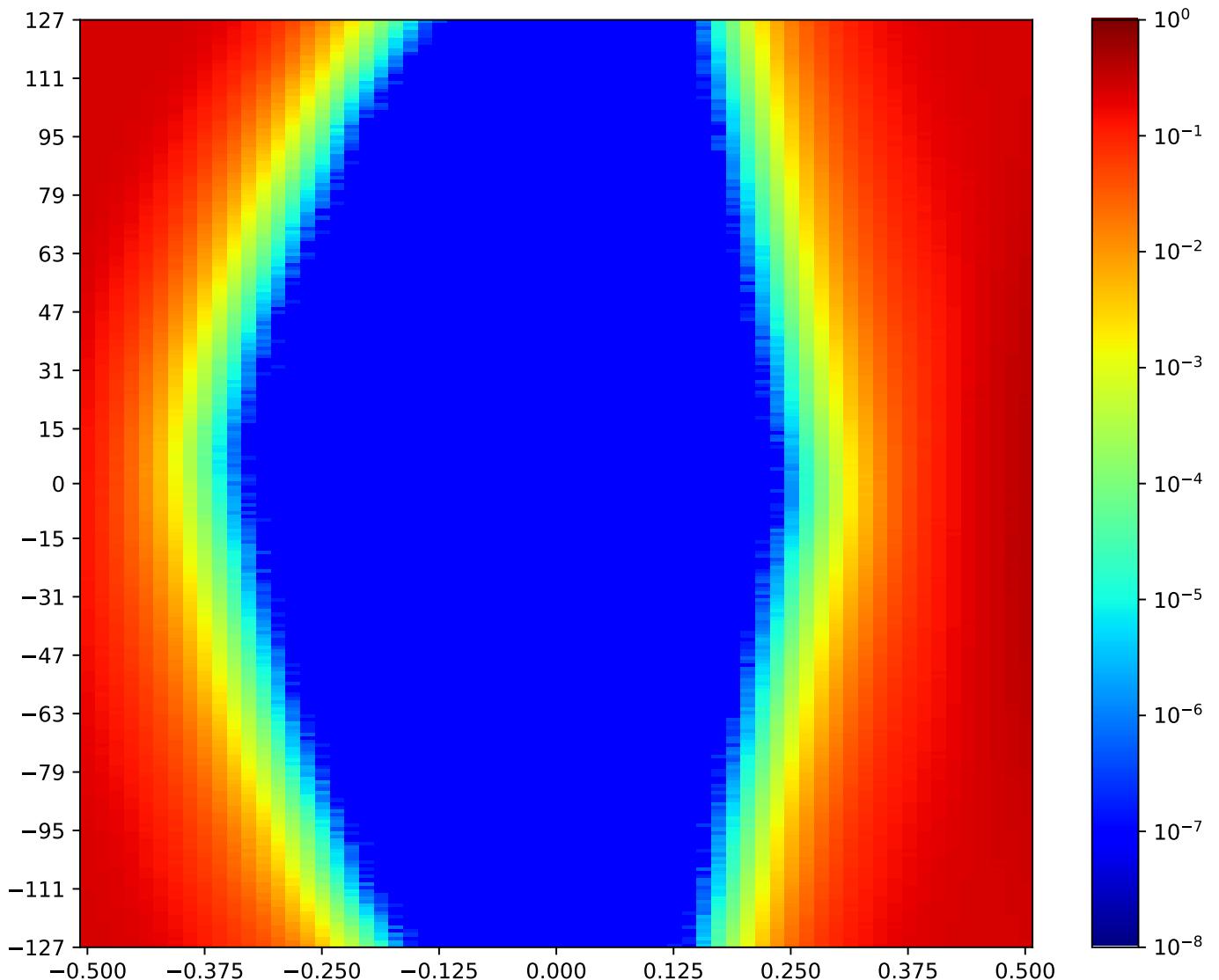


Figure 2.288: MSP\_C\_FPGA-TX4-08-RX3-08-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.10 MSP\_C\_FPGA-TX4-09-RX3-09-MSP\_A\_FPGA

Table 2.267: MSP\_C\_FPGA-TX4-09-RX3-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:19:41		2018-Jan-24 22:20:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6929	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

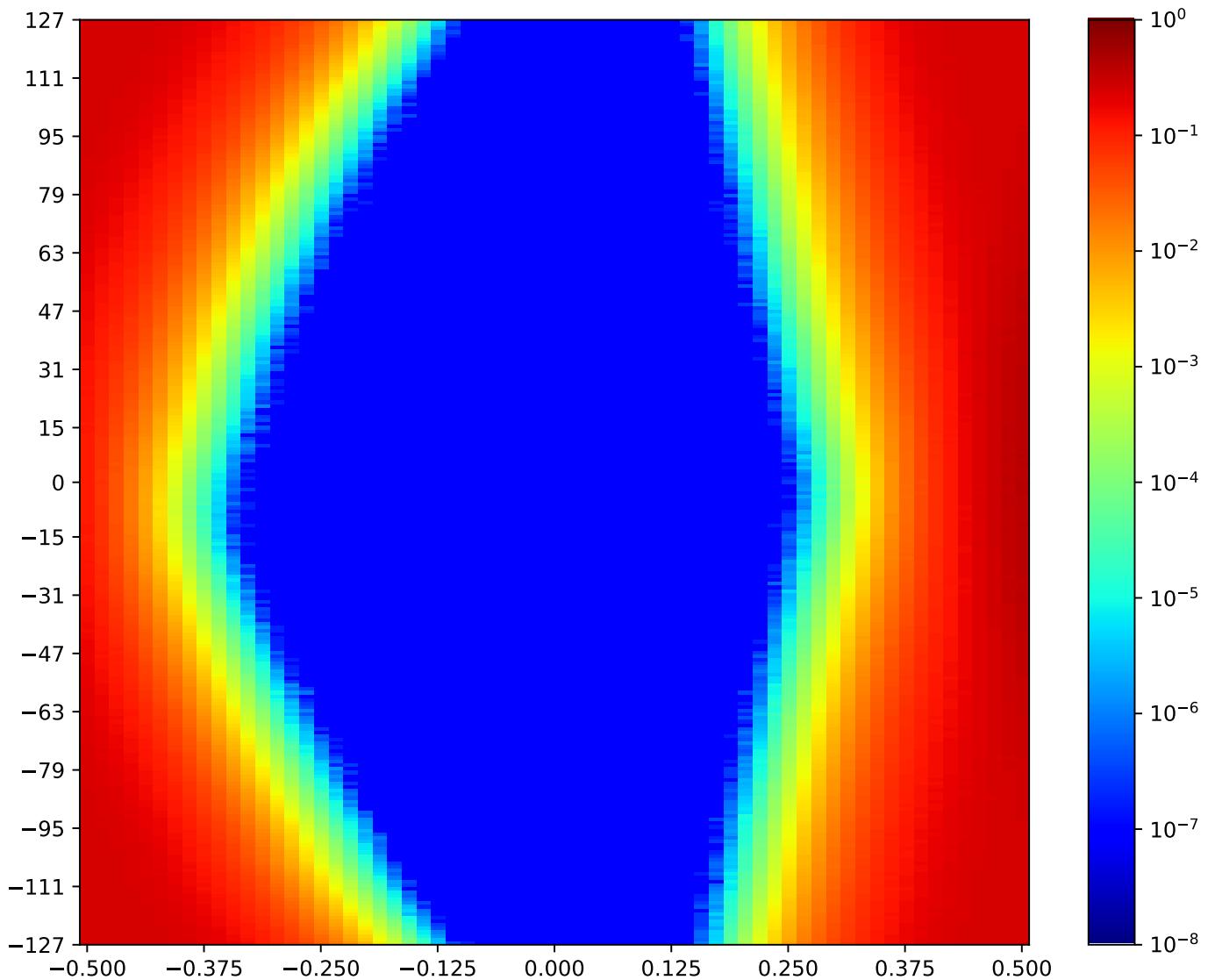


Figure 2.289: MSP\_C\_FPGA-TX4-09-RX3-09-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.11 MSP\_C\_FPGA-TX4-10-RX3-10-MSP\_A\_FPGA

Table 2.268: MSP\_C\_FPGA-TX4-10-RX3-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:21:10		2018-Jan-24 22:21:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8103	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

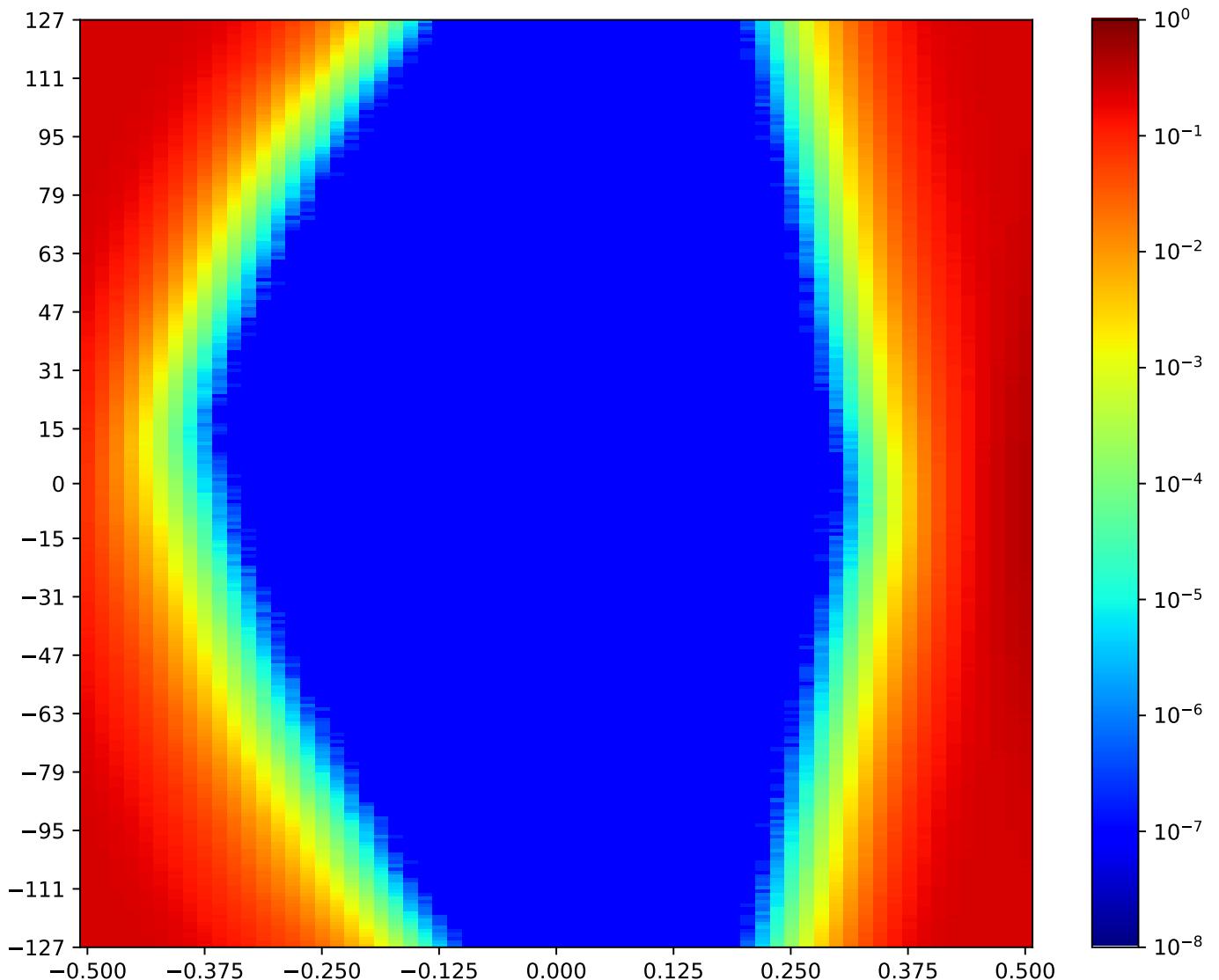


Figure 2.290: MSP\_C\_FPGA-TX4-10-RX3-10-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## 2.22.12 MSP\_C\_FPGA-TX4-11-RX3-11-MSP\_A\_FPGA

Table 2.269: MSP\_C\_FPGA-TX4-11-RX3-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 22:20:41		2018-Jan-24 22:21:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6888	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

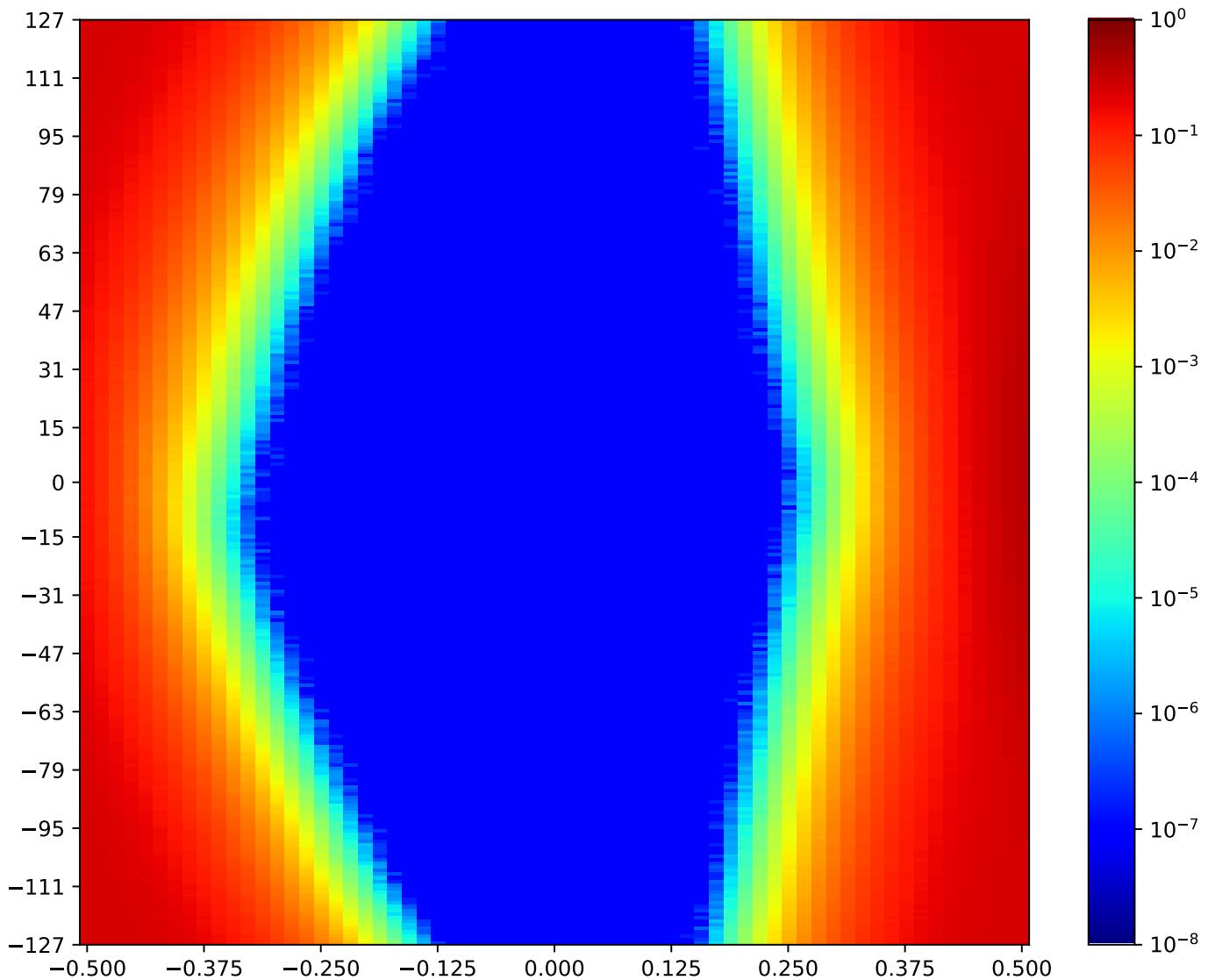


Figure 2.291: MSP\_C\_FPGA-TX4-11-RX3-11-MSP\_A\_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: 6.4-optimized, 12.8-optimized.

## **Chapter 3**

### **12.8 Gbps**

### 3.1 MSP\_A TX1 MSP\_C RX16 Minipod Loopback

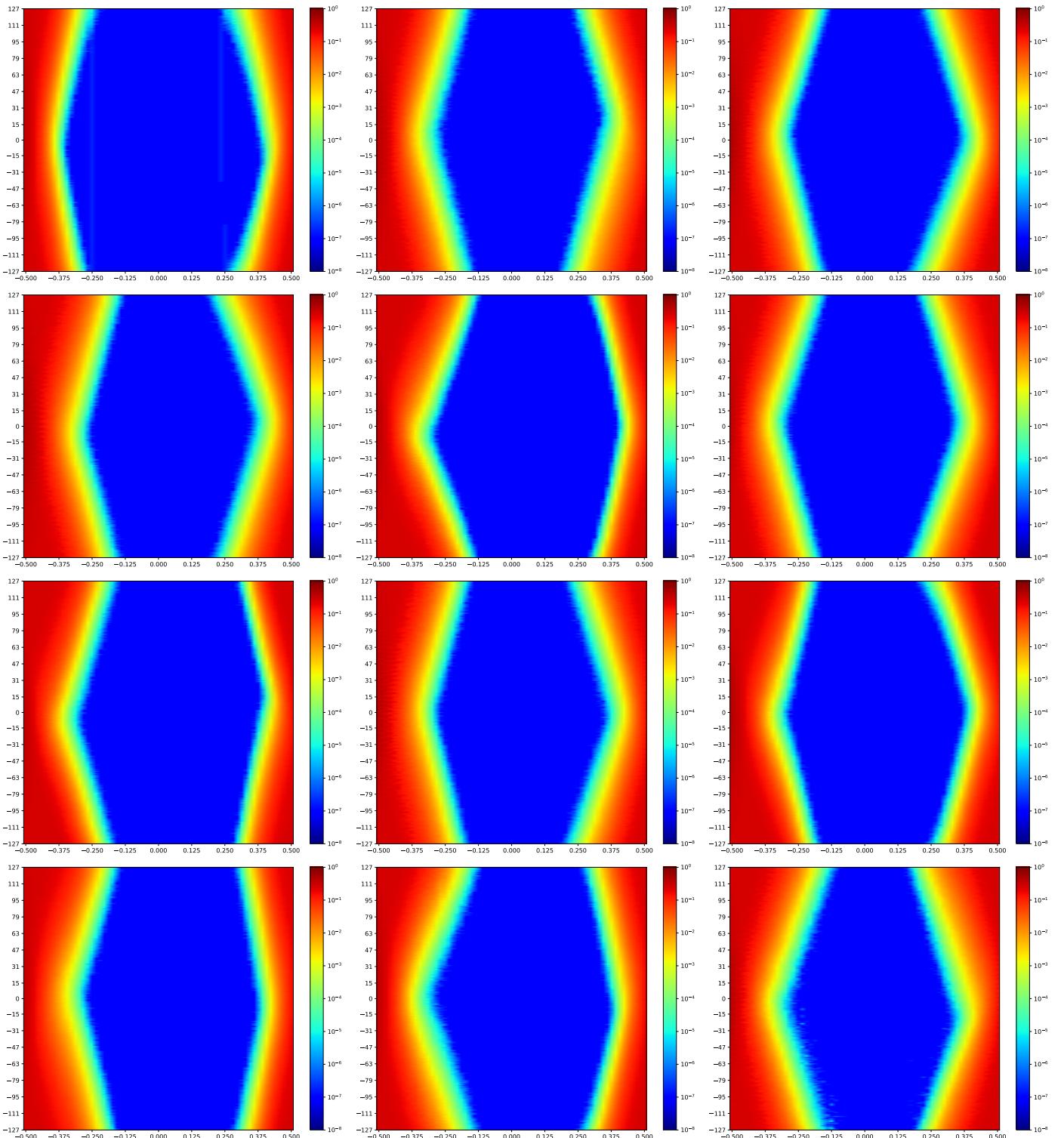


Figure 3.1: MSP\_A TX1 MSP\_C RX16 Minipod Loopback

A cross-reference to Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.14.

### 3.1.1 MSP\_A\_FPGA-TX1-00-RX16-00-MSP\_C\_FPGA

Table 3.1: MSP\_A\_FPGA-TX1-00-RX16-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:29:15		2018-Jan-23 23:29:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9912	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

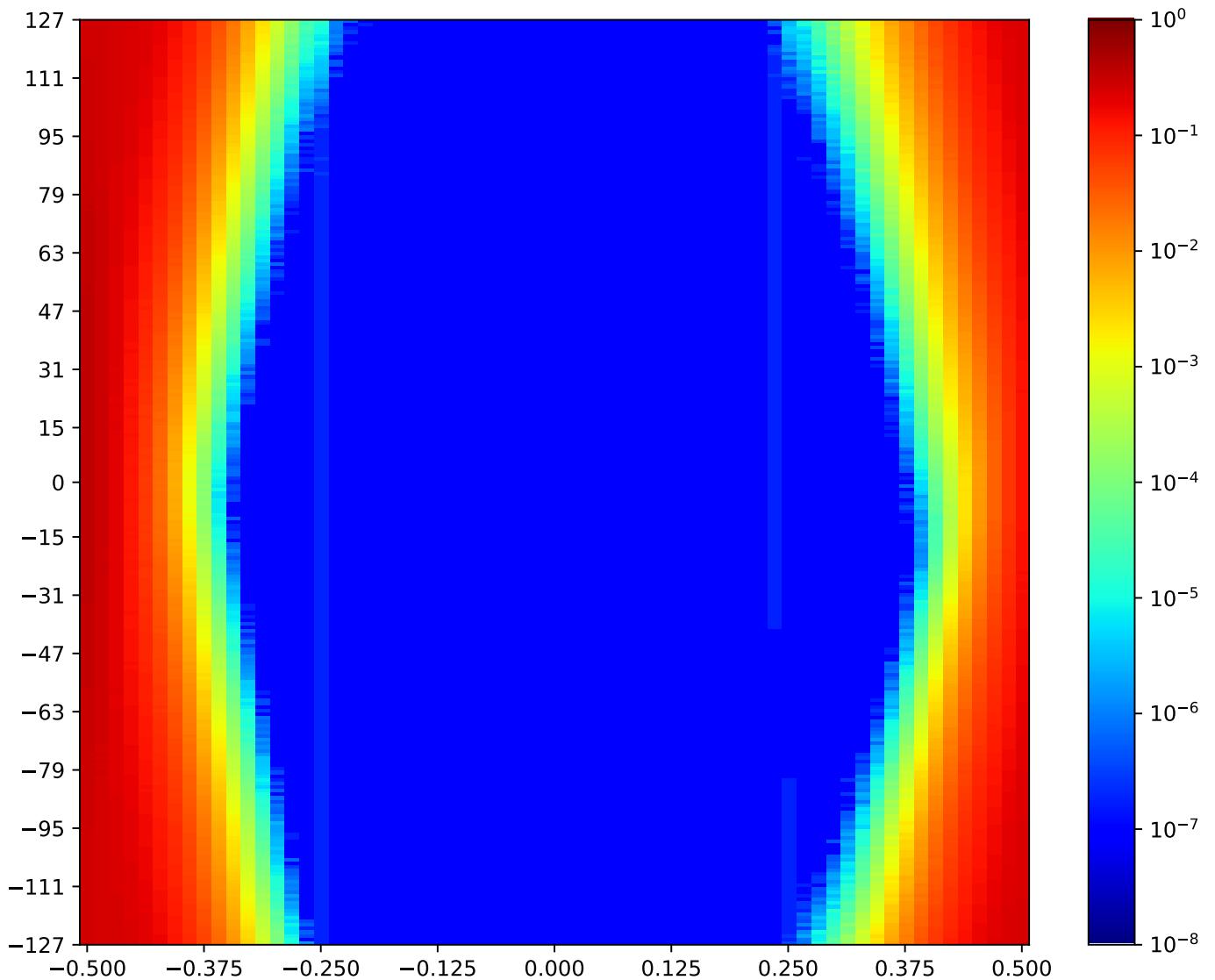


Figure 3.2: MSP\_A\_FPGA-TX1-00-RX16-00-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.2 MSP\_A\_FPGA-TX1-01-RX16-01-MSP\_C\_FPGA

Table 3.2: MSP\_A\_FPGA-TX1-01-RX16-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:29:57		2018-Jan-23 23:30:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7286	34	52.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

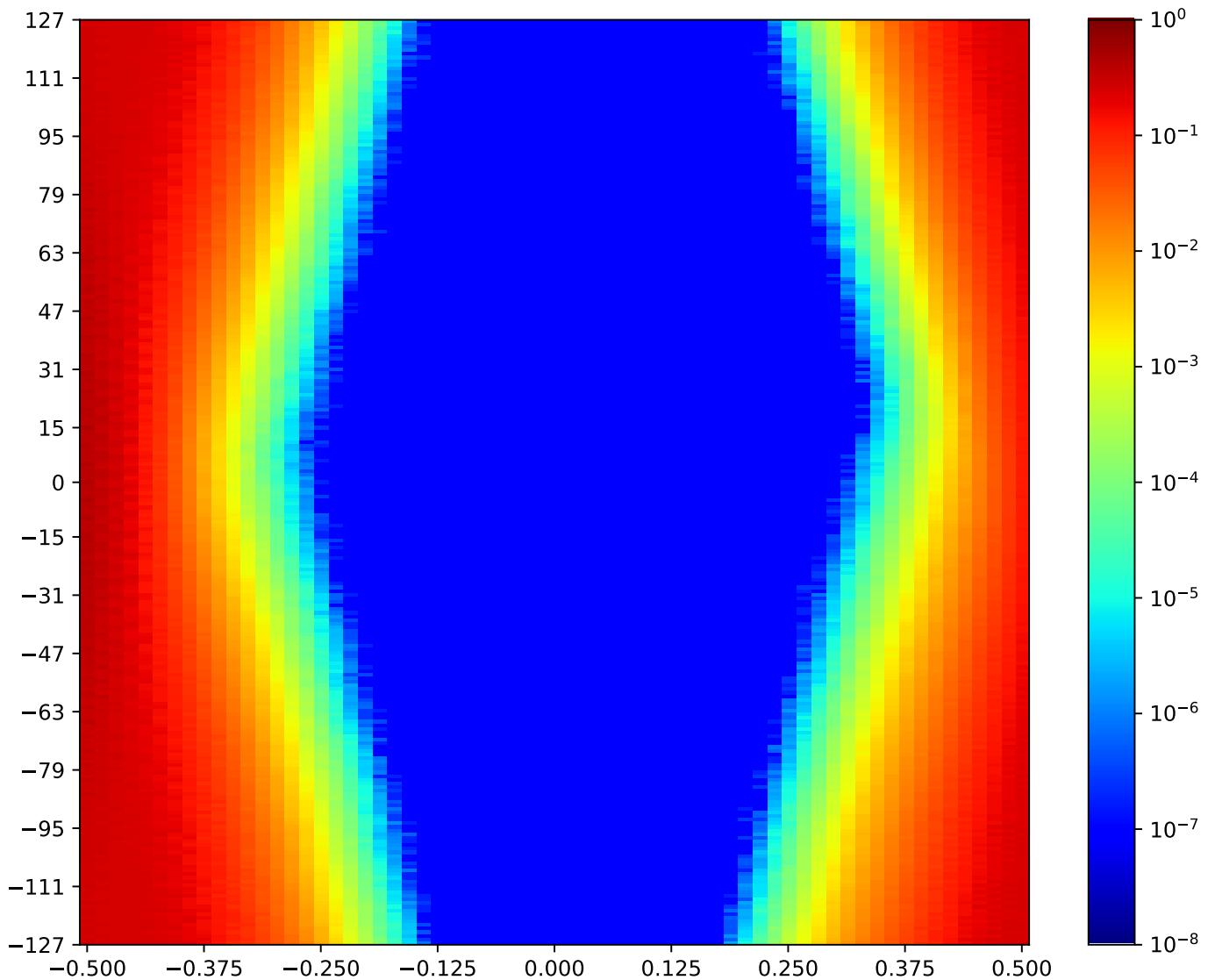


Figure 3.3: MSP\_A\_FPGA-TX1-01-RX16-01-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.3 MSP\_A\_FPGA-TX1-02-RX16-02-MSP\_C\_FPGA

Table 3.3: MSP\_A\_FPGA-TX1-02-RX16-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:30:17		2018-Jan-23 23:30:38	
Reset RX	OA	HO		HO (%)	
true	7392	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

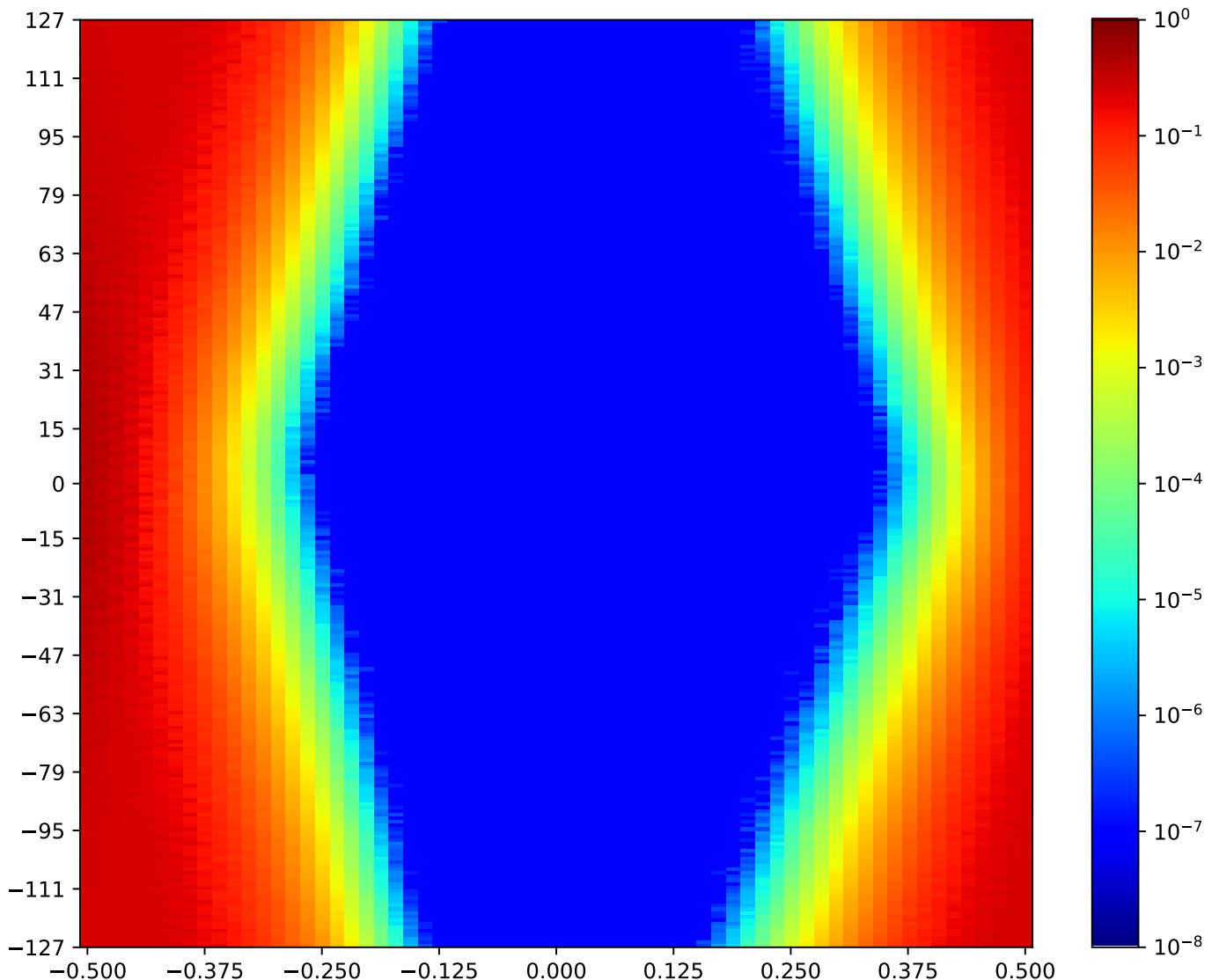


Figure 3.4: MSP\_A\_FPGA-TX1-02-RX16-02-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.4 MSP\_A\_FPGA-TX1-03-RX16-03-MSP\_C\_FPGA

Table 3.4: MSP\_A\_FPGA-TX1-03-RX16-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:28:33		2018-Jan-23 23:28:54	
Reset RX	OA	HO		HO (%)	
true	7363	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

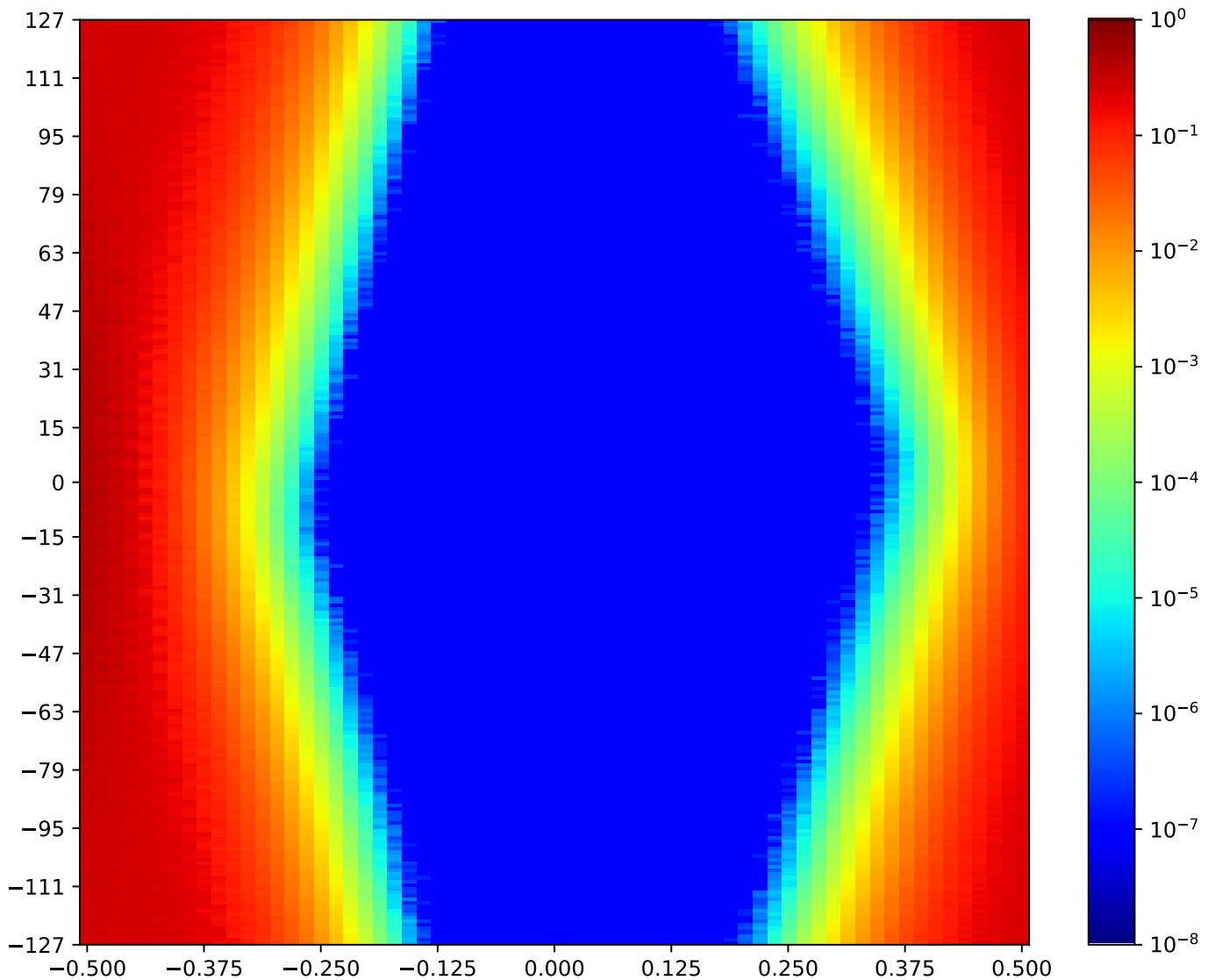


Figure 3.5: MSP\_A\_FPGA-TX1-03-RX16-03-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.5 MSP\_A\_FPGA-TX1-04-RX16-04-MSP\_C\_FPGA

Table 3.5: MSP\_A\_FPGA-TX1-04-RX16-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:31:18		2018-Jan-23 23:31:39	
Reset RX	OA	HO		VO   VO (%)	
true	8744	41		63.08%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

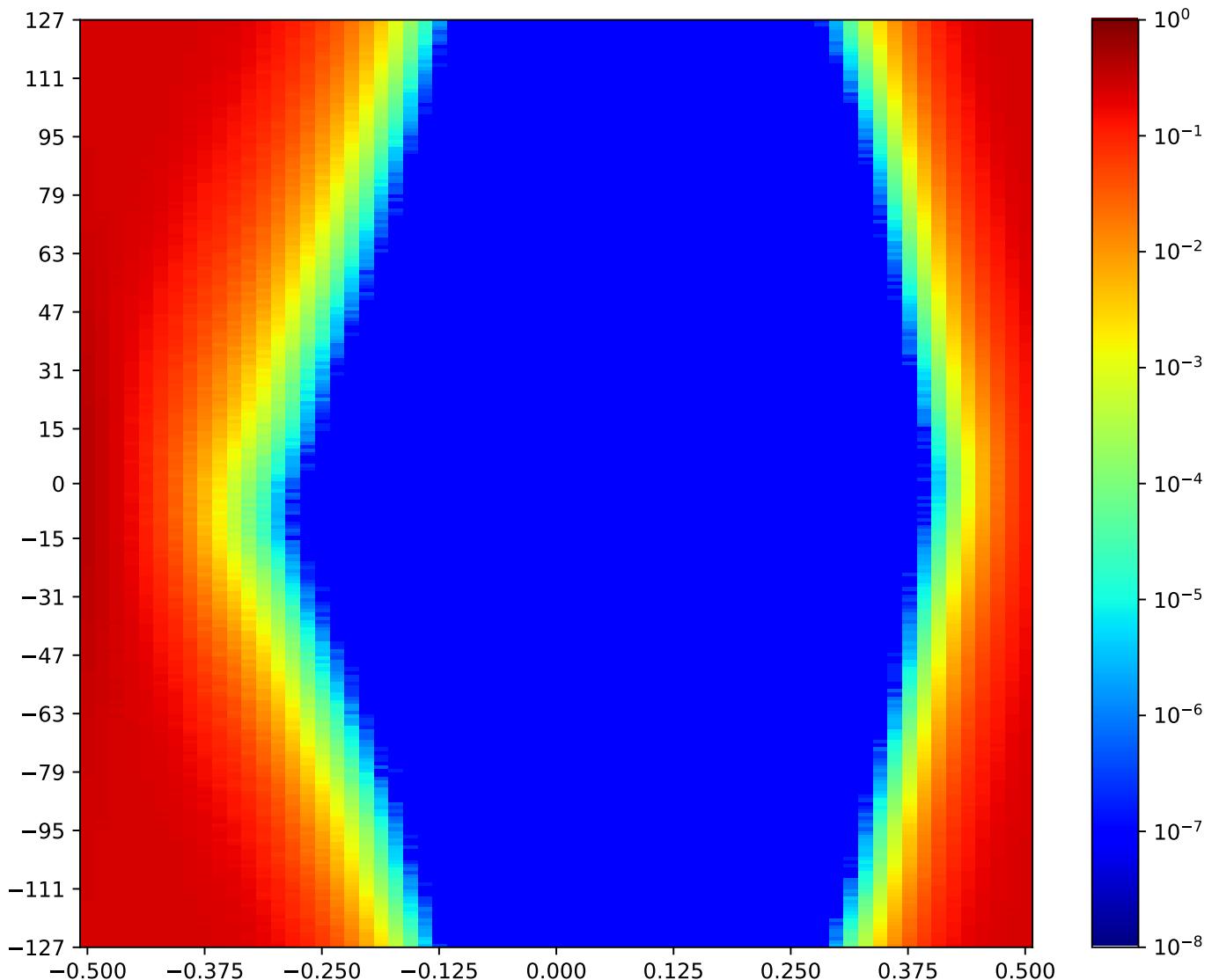


Figure 3.6: MSP\_A\_FPGA-TX1-04-RX16-04-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.6 MSP\_A\_FPGA-TX1-05-RX16-05-MSP\_C\_FPGA

Table 3.6: MSP\_A\_FPGA-TX1-05-RX16-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:28:13		2018-Jan-23 23:28:33	
Reset RX	OA	HO		HO (%)	
true	7387	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

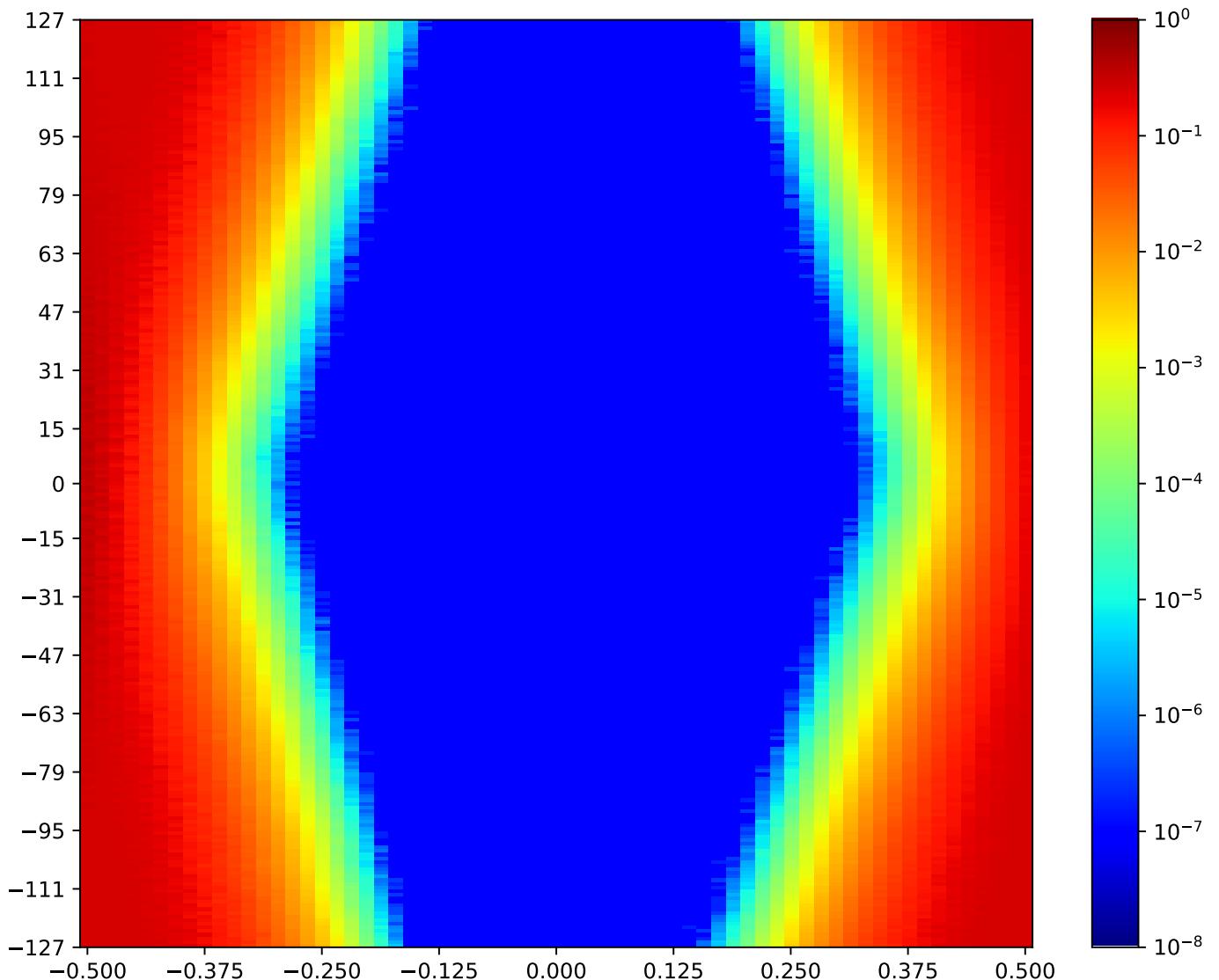


Figure 3.7: MSP\_A\_FPGA-TX1-05-RX16-05-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.7 MSP\_A\_FPGA-TX1-06-RX16-06-MSP\_C\_FPGA

Table 3.7: MSP\_A\_FPGA-TX1-06-RX16-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:31:59		2018-Jan-23 23:32:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8842	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

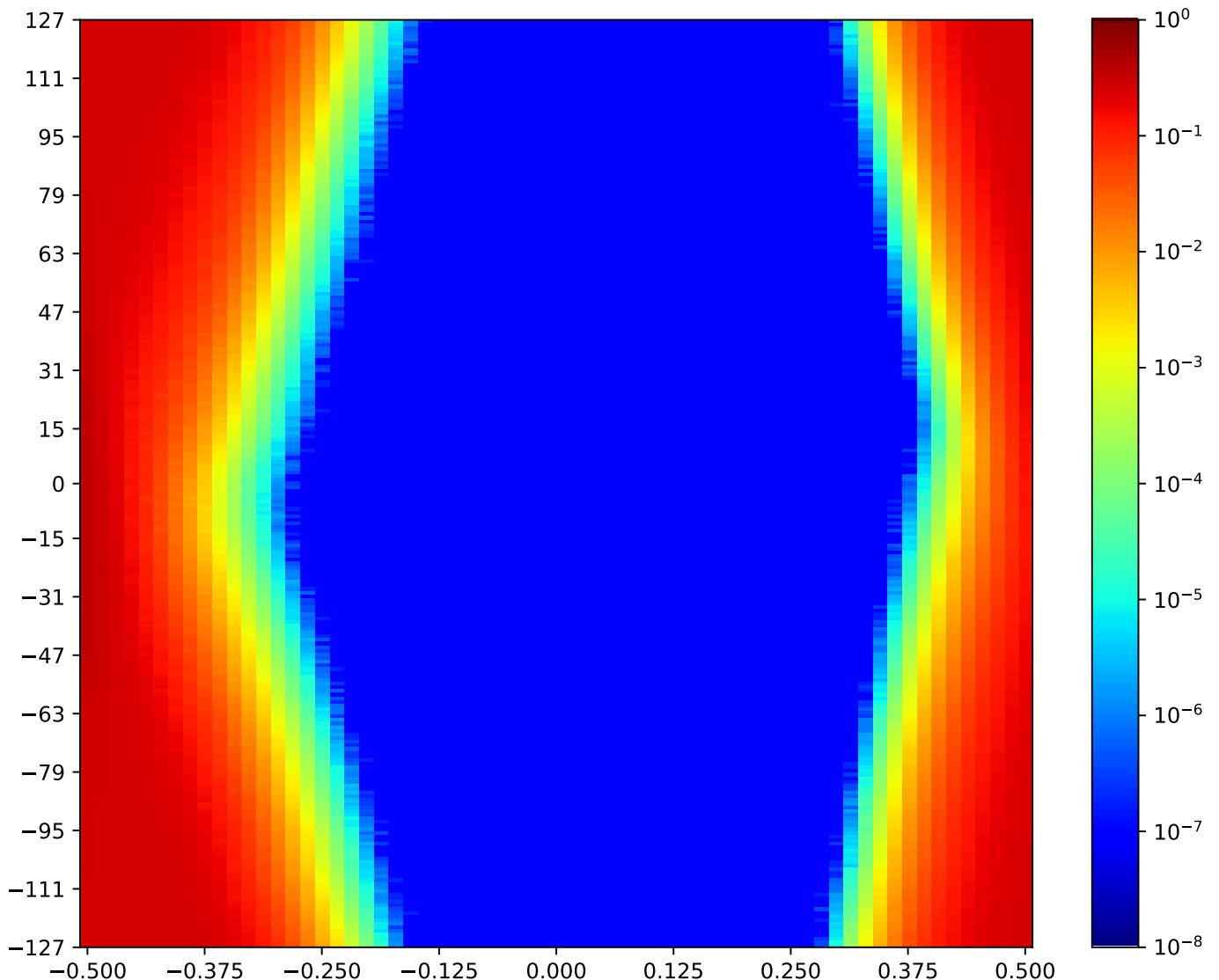


Figure 3.8: MSP\_A\_FPGA-TX1-06-RX16-06-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.8 MSP\_A\_FPGA-TX1-07-RX16-07-MSP\_C\_FPGA

Table 3.8: MSP\_A\_FPGA-TX1-07-RX16-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:28:54		2018-Jan-23 23:29:15	
Reset RX	OA	HO		HO (%)	
true	7642	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

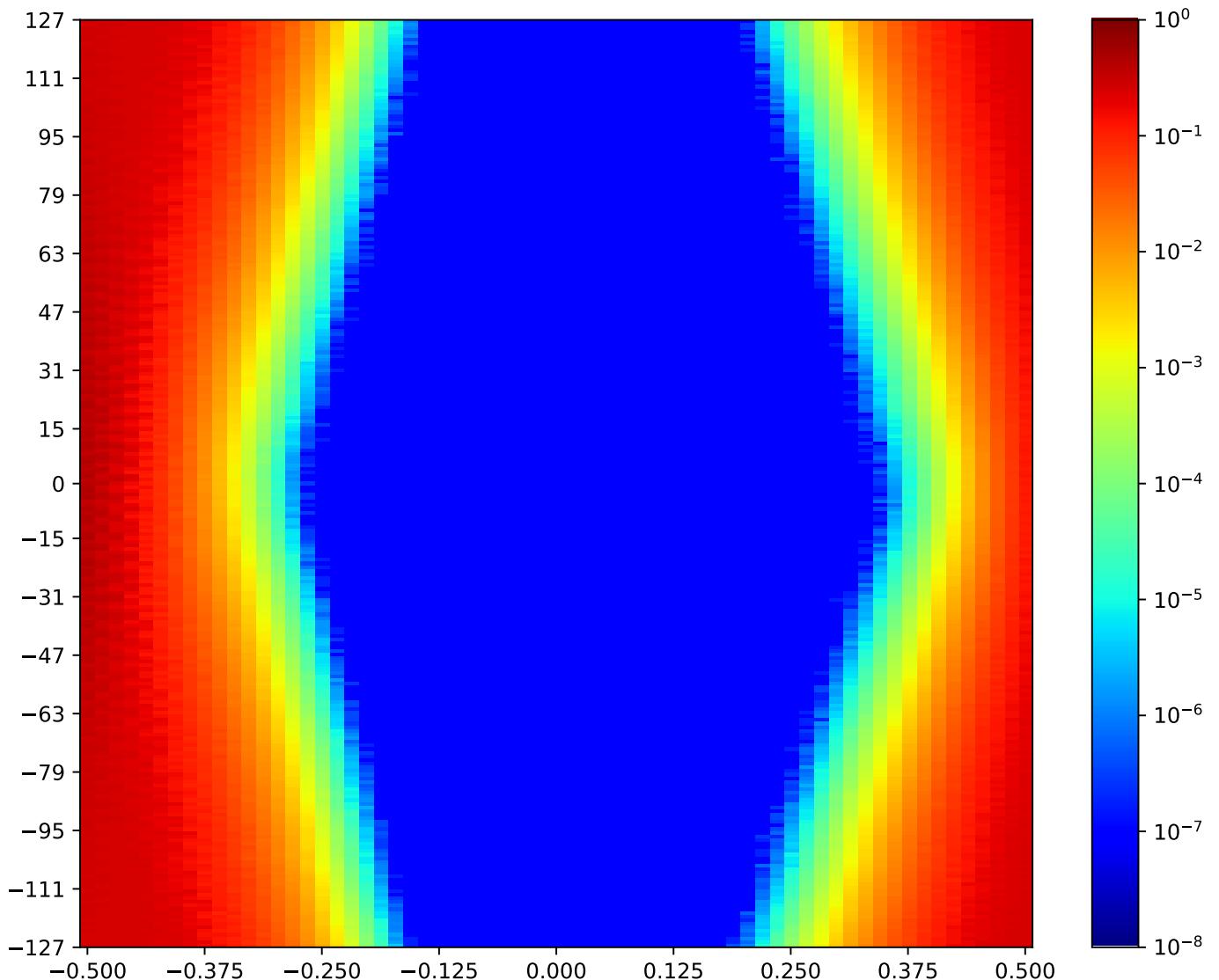


Figure 3.9: MSP\_A\_FPGA-TX1-07-RX16-07-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.9 MSP\_A\_FPGA-TX1-08-RX16-08-MSP\_C\_FPGA

Table 3.9: MSP\_A\_FPGA-TX1-08-RX16-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:31:39		2018-Jan-23 23:31:59	
Reset RX	OA	HO		HO (%)	
true	8316	41		63.08%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

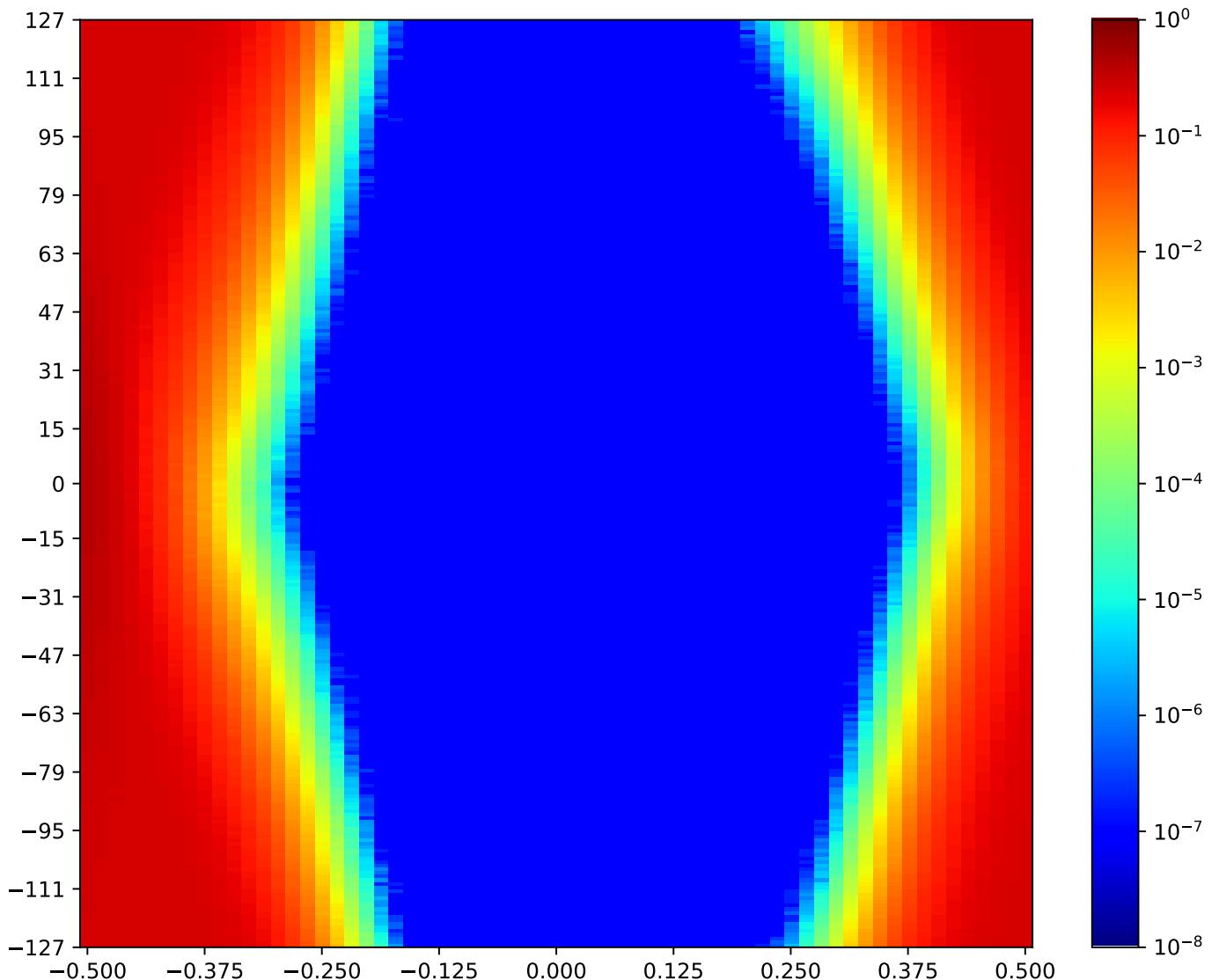


Figure 3.10: MSP\_A\_FPGA-TX1-08-RX16-08-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.10 MSP\_A\_FPGA-TX1-09-RX16-09-MSP\_C\_FPGA

Table 3.10: MSP\_A\_FPGA-TX1-09-RX16-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:29:36		2018-Jan-23 23:29:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8464	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

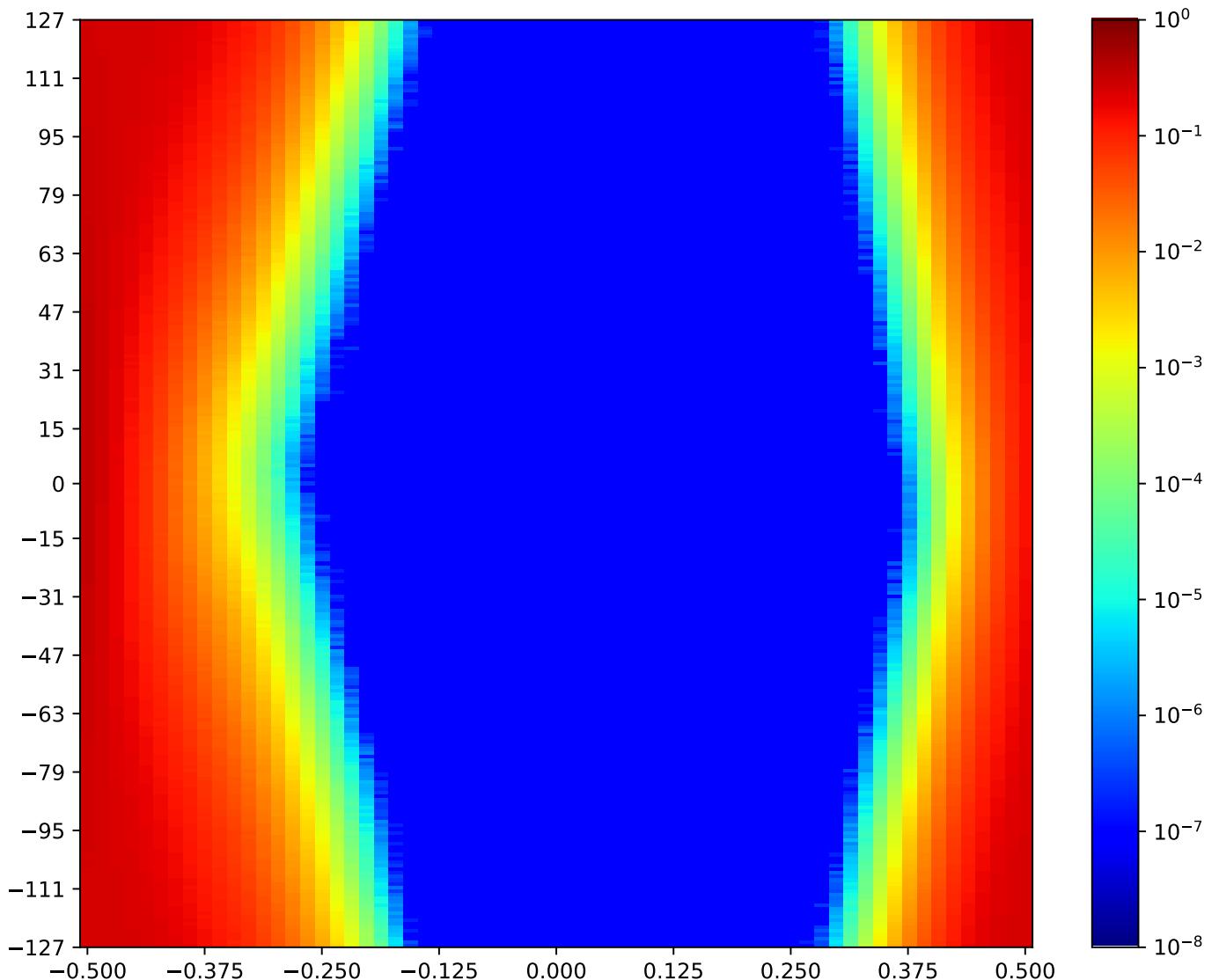


Figure 3.11: MSP\_A\_FPGA-TX1-09-RX16-09-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.11 MSP\_A\_FPGA-TX1-10-RX16-10-MSP\_C\_FPGA

Table 3.11: MSP\_A\_FPGA-TX1-10-RX16-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:30:58		2018-Jan-23 23:31:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8137	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

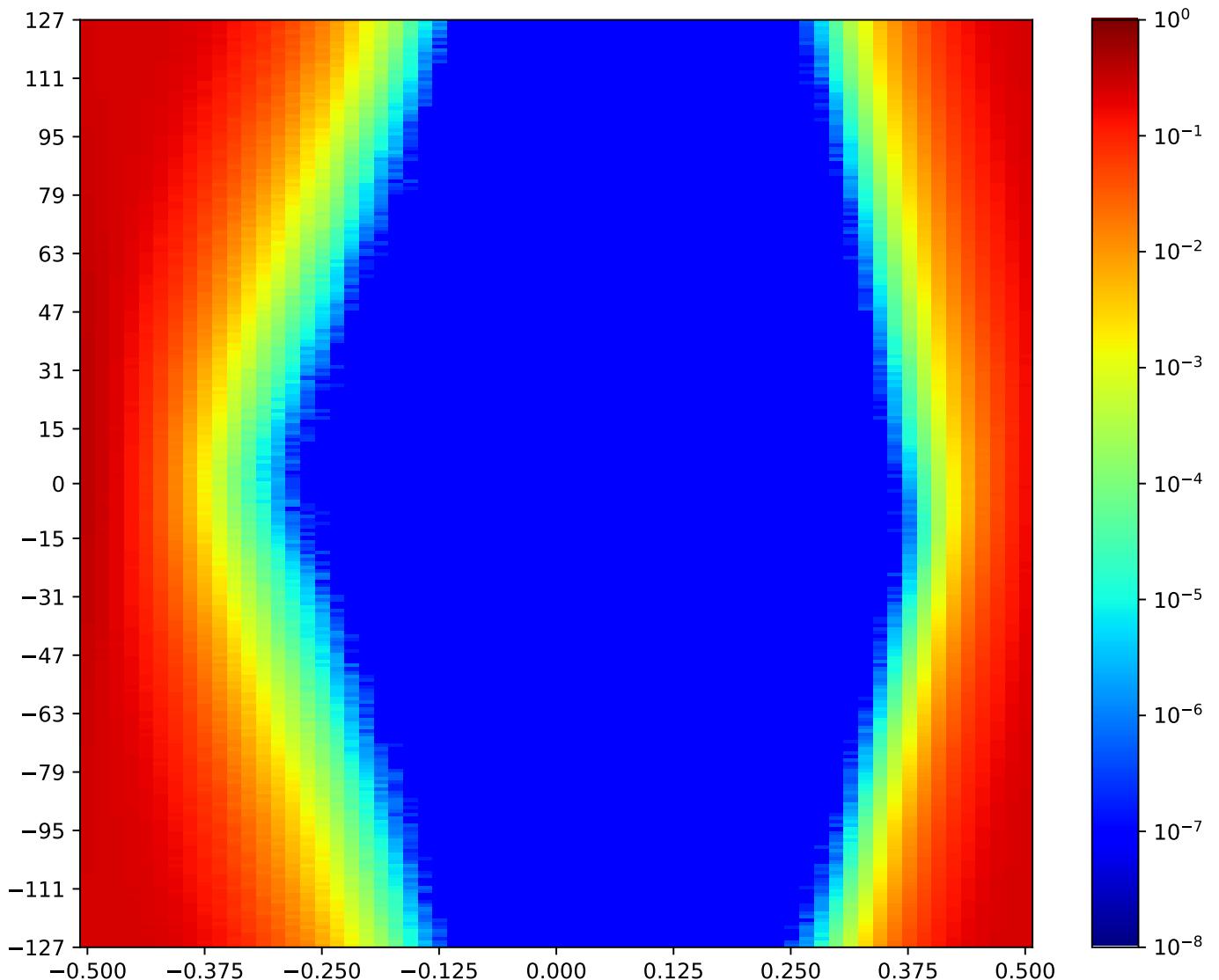


Figure 3.12: MSP\_A\_FPGA-TX1-10-RX16-10-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.1.12 MSP\_A\_FPGA-TX1-11-RX16-11-MSP\_C\_FPGA

Table 3.12: MSP\_A\_FPGA-TX1-11-RX16-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:30:38			2018-Jan-23 23:30:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	6656	34	52.31%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

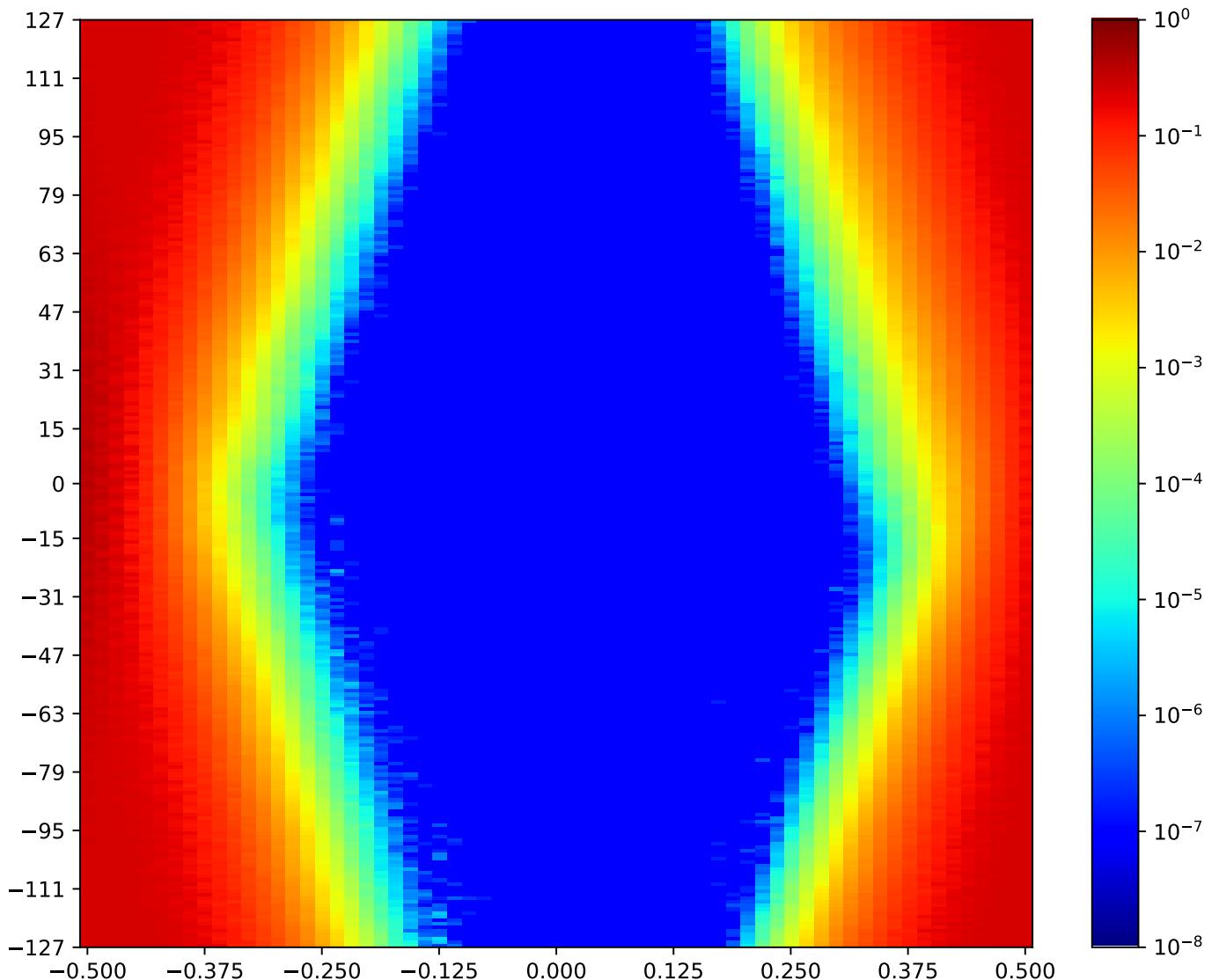


Figure 3.13: MSP\_A\_FPGA-TX1-11-RX16-11-MSP\_C\_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2 MSP\_A TX2 MSP\_C RX15 Minipod Loopback

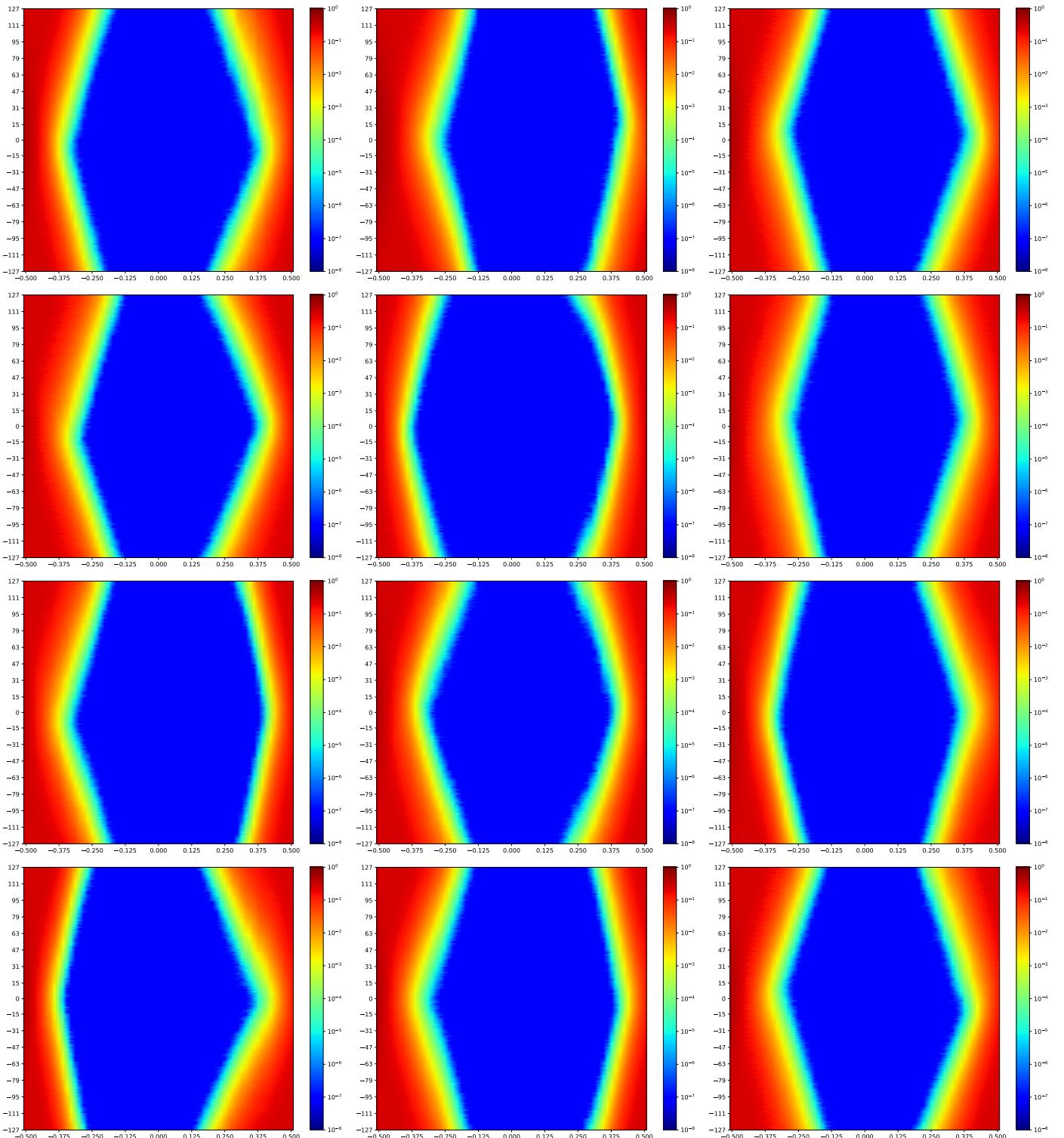


Figure 3.14: MSP\_A TX2 MSP\_C RX15 Minipod Loopback

A cross-reference to Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.27.

### 3.2.1 MSP\_A\_FPGA-TX2-00-RX15-00-MSP\_C\_FPGA

Table 3.13: MSP\_A\_FPGA-TX2-00-RX15-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:33:20		2018-Jan-23 23:33:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8099	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

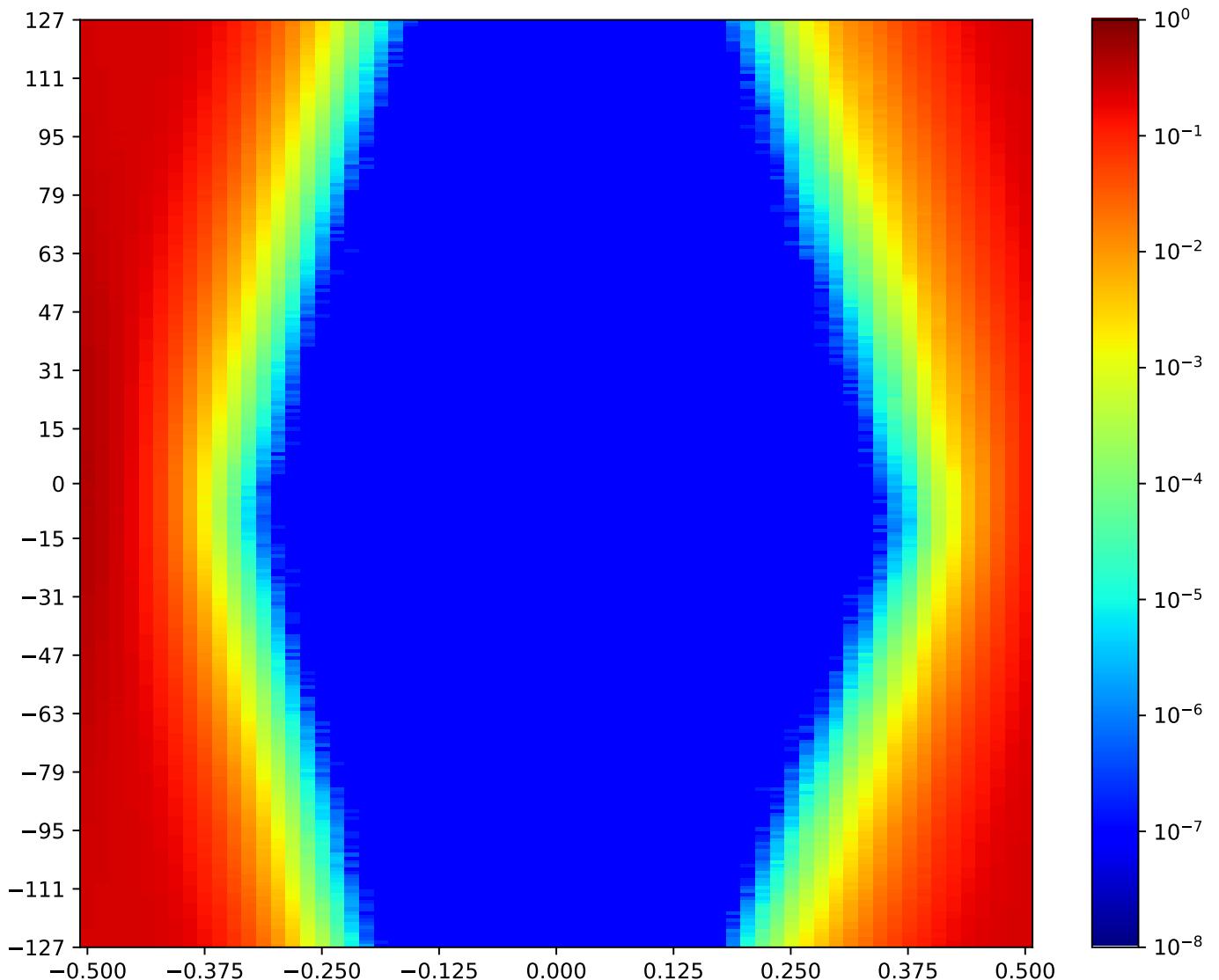


Figure 3.15: MSP\_A\_FPGA-TX2-00-RX15-00-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.2 MSP\_A\_FPGA-TX2-01-RX15-01-MSP\_C\_FPGA

Table 3.14: MSP\_A\_FPGA-TX2-01-RX15-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:32:39		2018-Jan-23 23:33:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8220	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

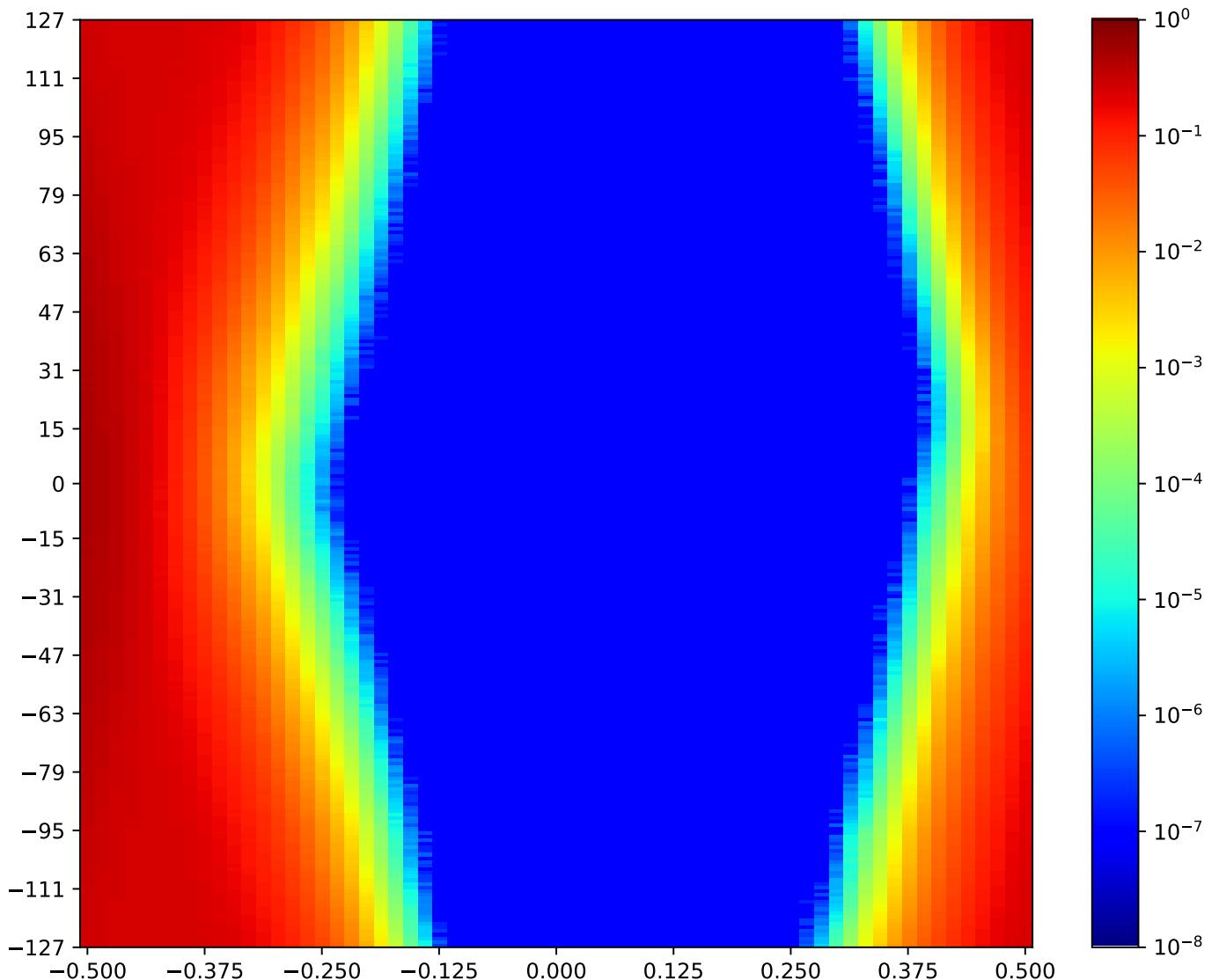


Figure 3.16: MSP\_A\_FPGA-TX2-01-RX15-01-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.3 MSP\_A\_FPGA-TX2-02-RX15-02-MSP\_C\_FPGA

Table 3.15: MSP\_A\_FPGA-TX2-02-RX15-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:34:20		2018-Jan-23 23:34:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7526	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

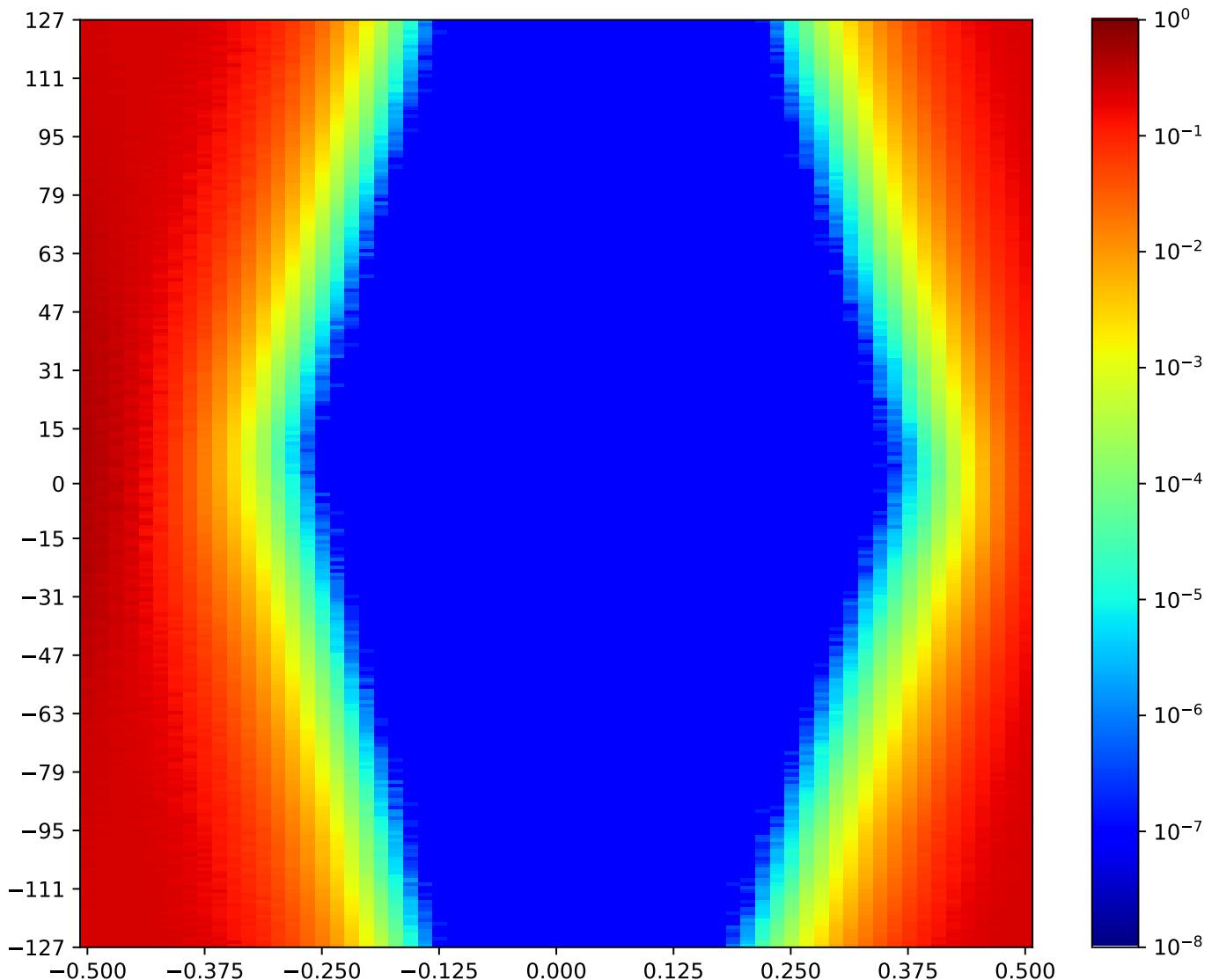


Figure 3.17: MSP\_A\_FPGA-TX2-02-RX15-02-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.4 MSP\_A\_FPGA-TX2-03-RX15-03-MSP\_C\_FPGA

Table 3.16: MSP\_A\_FPGA-TX2-03-RX15-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:32:19		2018-Jan-23 23:32:39	
Reset RX	OA	HO		HO (%)	
true	7300	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

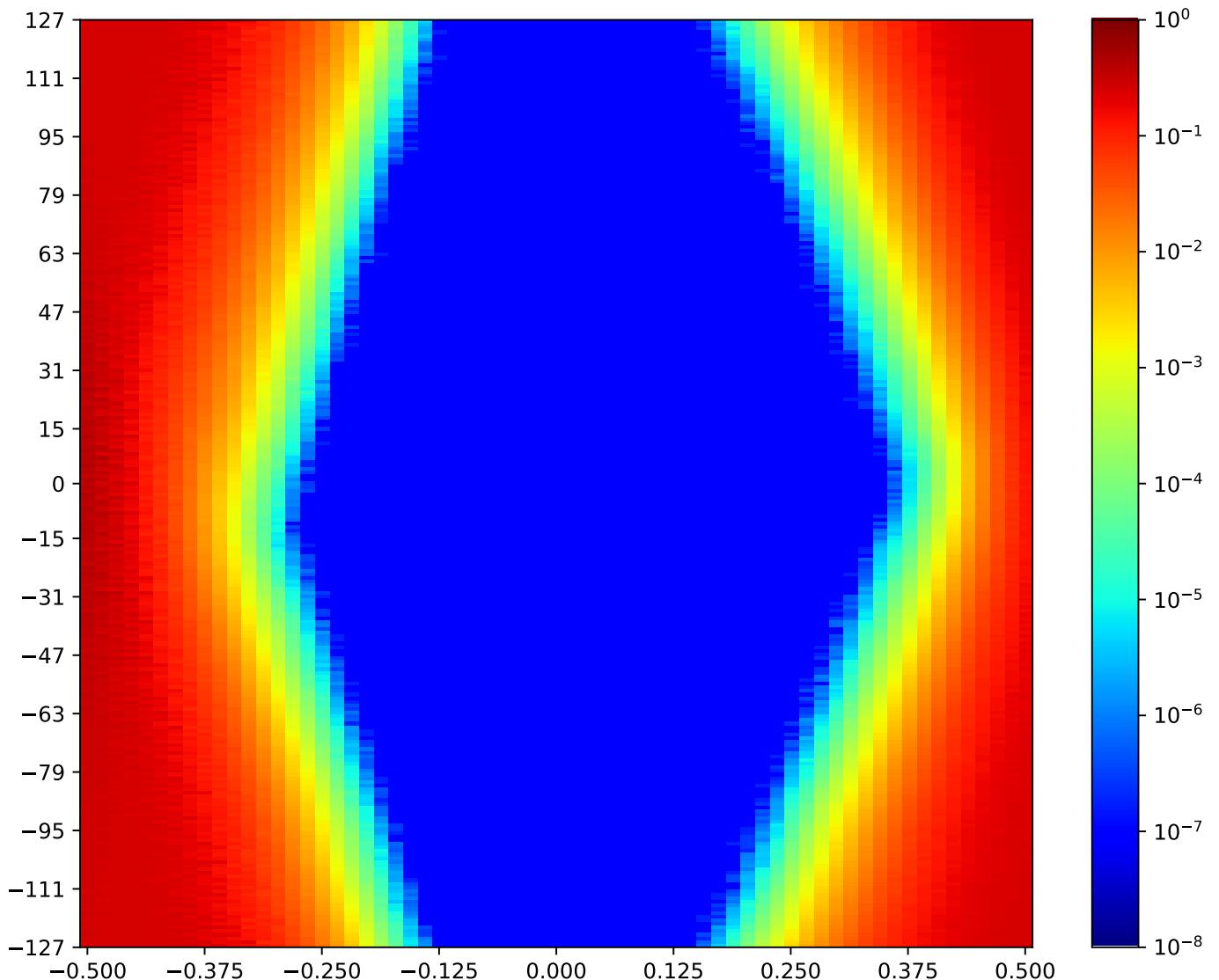


Figure 3.18: MSP\_A\_FPGA-TX2-03-RX15-03-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.5 MSP\_A\_FPGA-TX2-04-RX15-04-MSP\_C\_FPGA

Table 3.17: MSP\_A\_FPGA-TX2-04-RX15-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:35:22		2018-Jan-23 23:35:42	
Reset RX	OA	HO		HO (%)	
true	9666	46		70.77%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

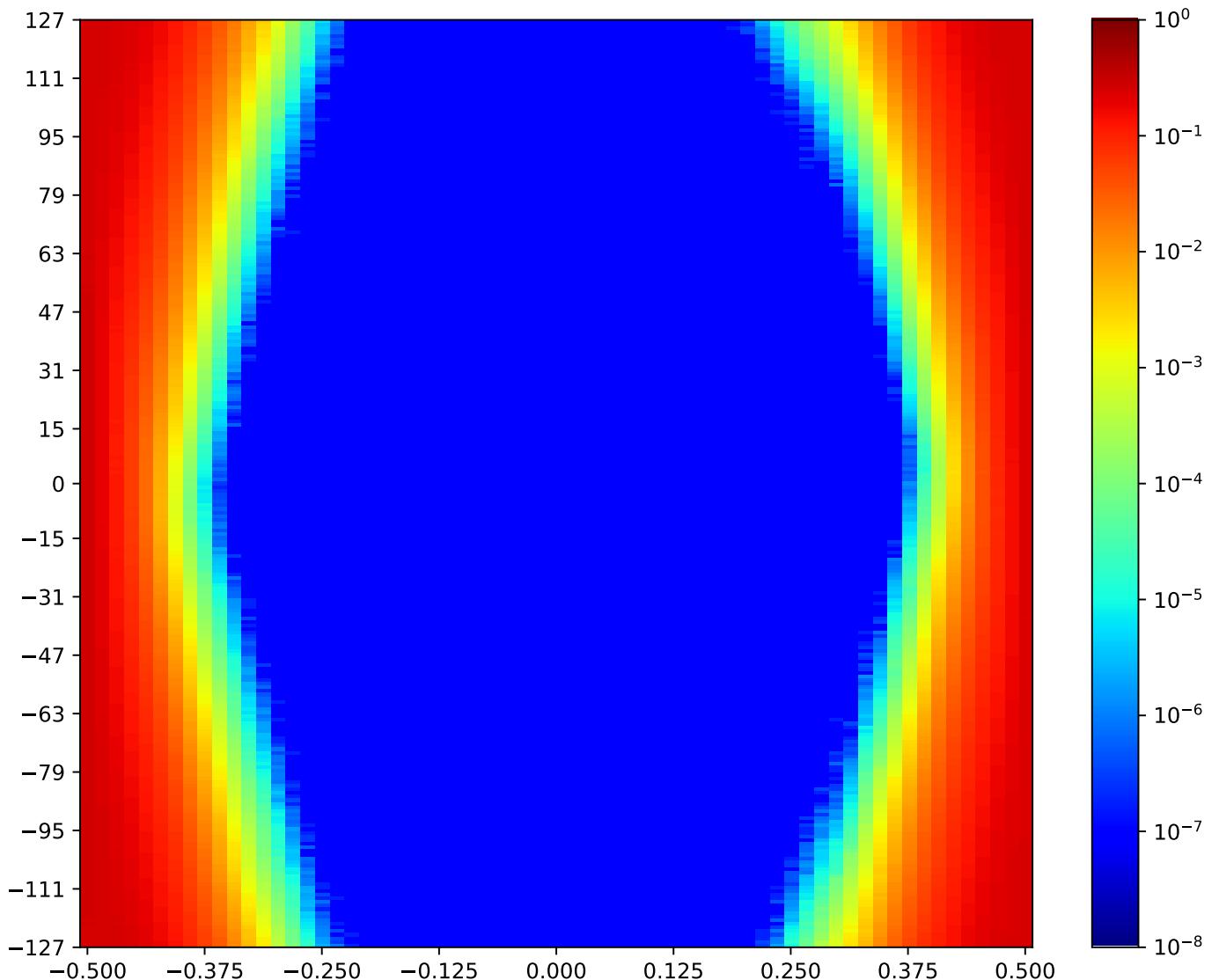


Figure 3.19: MSP\_A\_FPGA-TX2-04-RX15-04-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.6 MSP\_A\_FPGA-TX2-05-RX15-05-MSP\_C\_FPGA

Table 3.18: MSP\_A\_FPGA-TX2-05-RX15-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:33:00		2018-Jan-23 23:33:20	
Reset RX	OA	HO		HO (%)	
true	7204	36		55.38%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

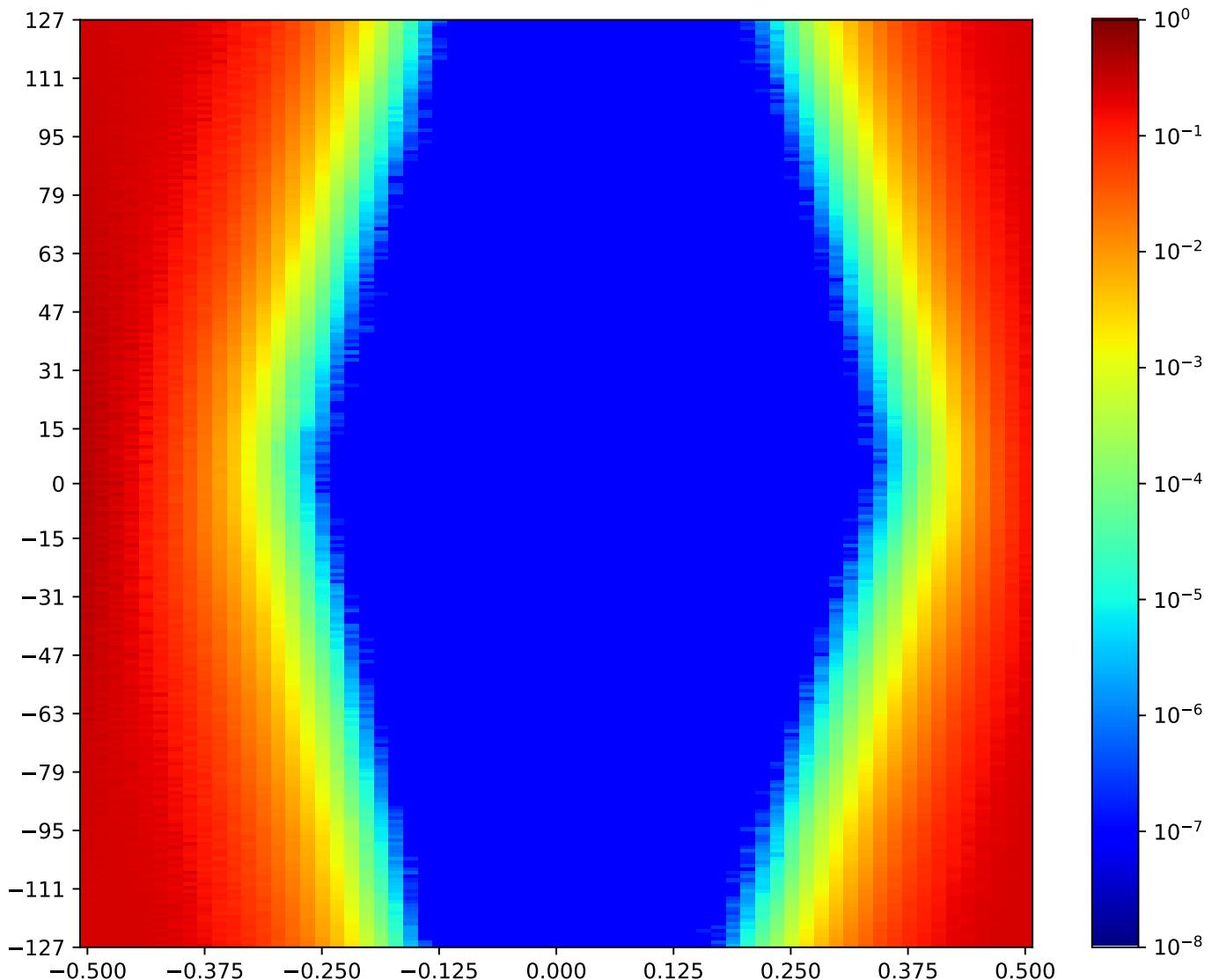


Figure 3.20: MSP\_A\_FPGA-TX2-05-RX15-05-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.7 MSP\_A\_FPGA-TX2-06-RX15-06-MSP\_C\_FPGA

Table 3.19: MSP\_A\_FPGA-TX2-06-RX15-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:36:03		2018-Jan-23 23:36:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9151	44	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

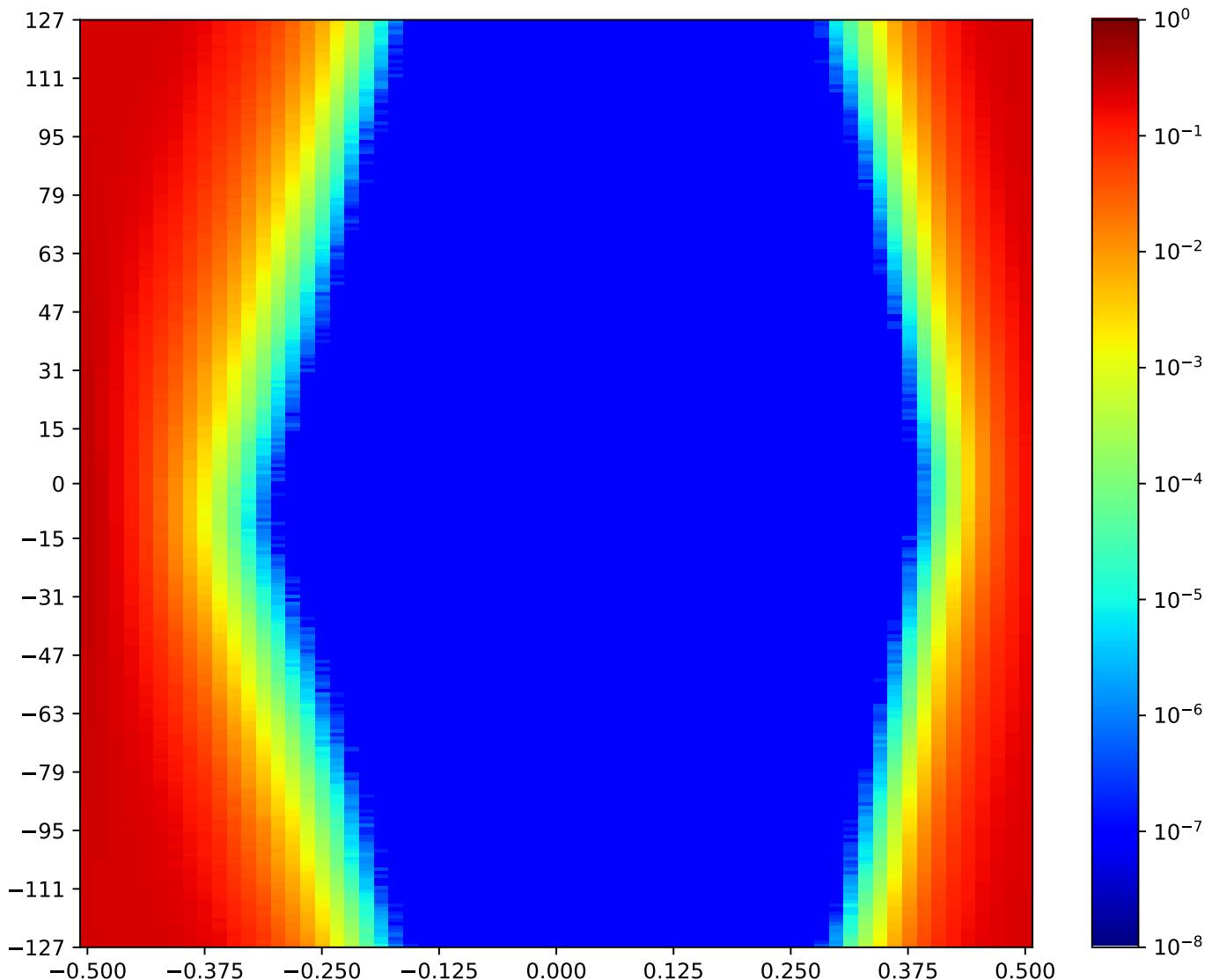


Figure 3.21: MSP\_A\_FPGA-TX2-06-RX15-06-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.8 MSP\_A\_FPGA-TX2-07-RX15-07-MSP\_C\_FPGA

Table 3.20: MSP\_A\_FPGA-TX2-07-RX15-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:33:40		2018-Jan-23 23:34:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7917	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

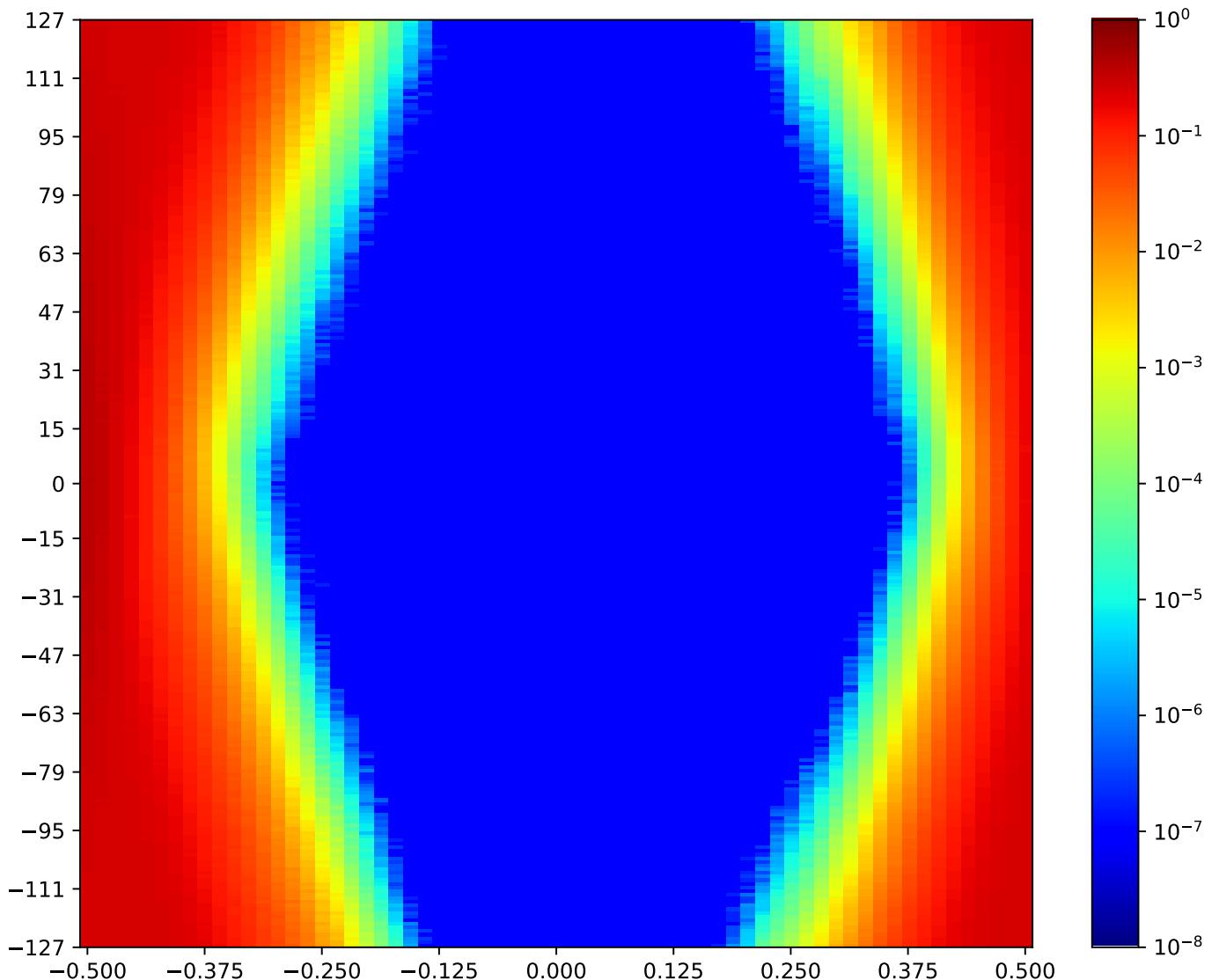


Figure 3.22: MSP\_A\_FPGA-TX2-07-RX15-07-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.9 MSP\_A\_FPGA-TX2-08-RX15-08-MSP\_C\_FPGA

Table 3.21: MSP\_A\_FPGA-TX2-08-RX15-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:35:42		2018-Jan-23 23:36:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8277	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

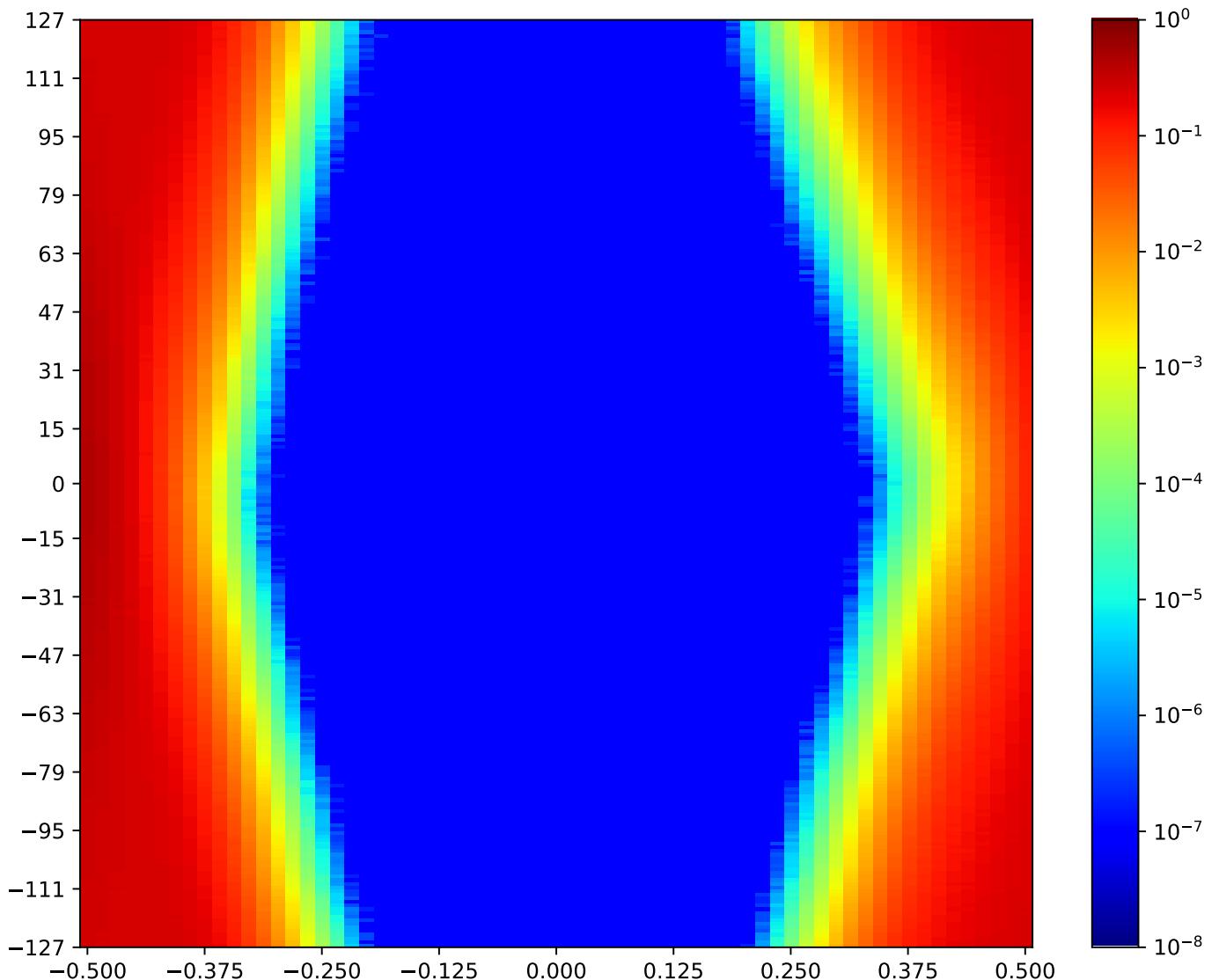


Figure 3.23: MSP\_A\_FPGA-TX2-08-RX15-08-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.10 MSP\_A\_FPGA-TX2-09-RX15-09-MSP\_C\_FPGA

Table 3.22: MSP\_A\_FPGA-TX2-09-RX15-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:34:00		2018-Jan-23 23:34:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8683	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

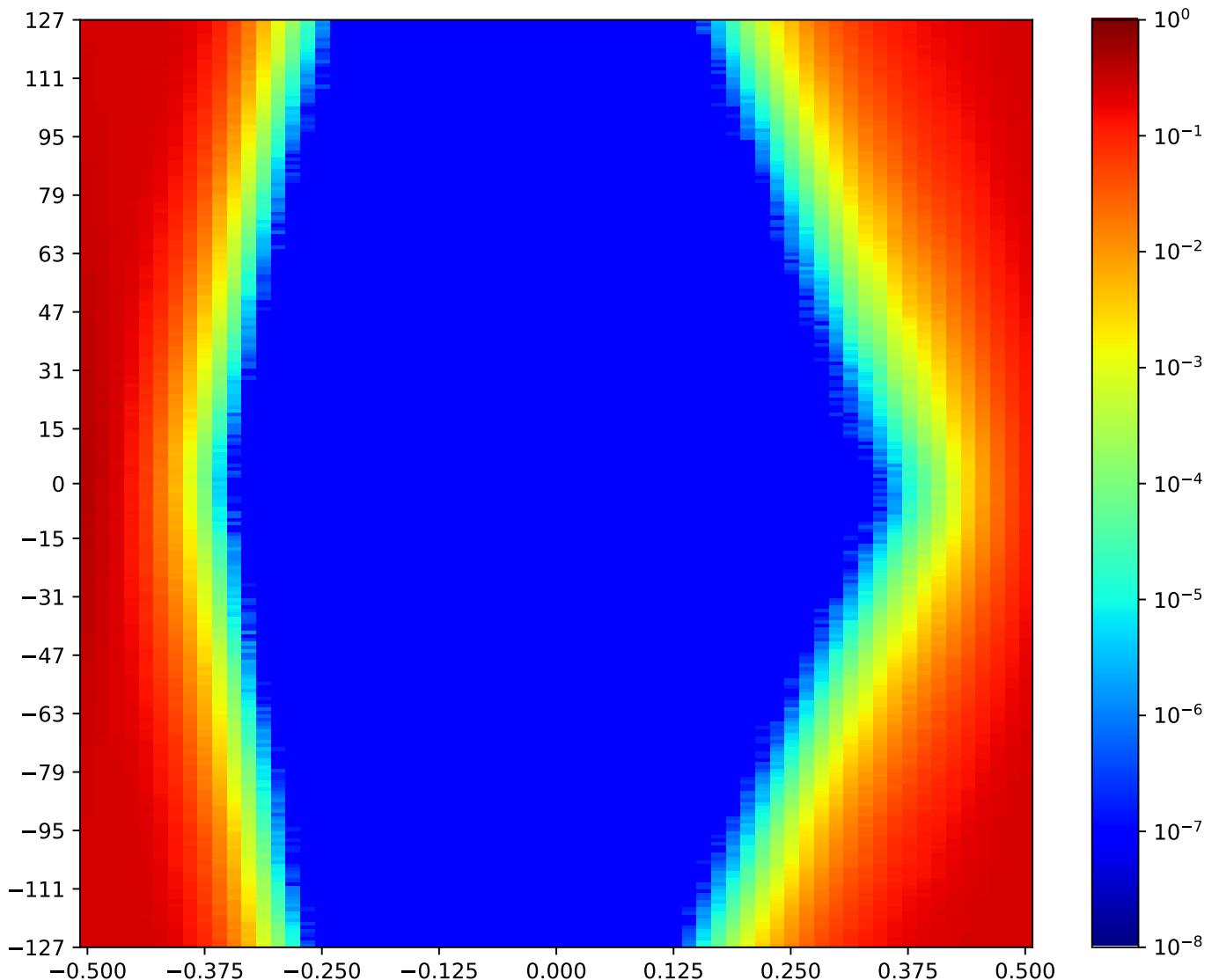


Figure 3.24: MSP\_A\_FPGA-TX2-09-RX15-09-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.11 MSP\_A\_FPGA-TX2-10-RX15-10-MSP\_C\_FPGA

Table 3.23: MSP\_A\_FPGA-TX2-10-RX15-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:35:01		2018-Jan-23 23:35:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8711	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

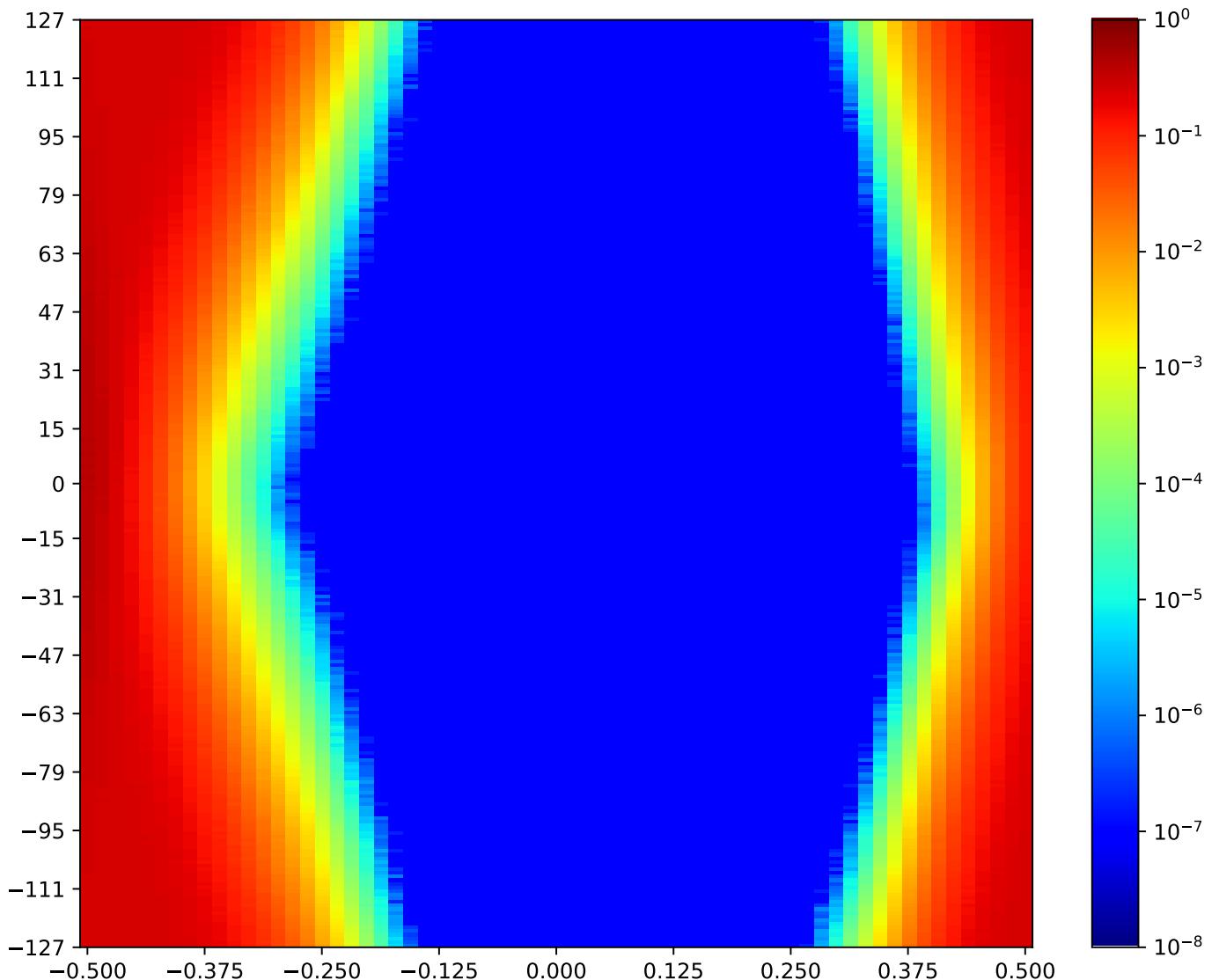


Figure 3.25: MSP\_A\_FPGA-TX2-10-RX15-10-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.2.12 MSP\_A\_FPGA-TX2-11-RX15-11-MSP\_C\_FPGA

Table 3.24: MSP\_A\_FPGA-TX2-11-RX15-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:34:41		2018-Jan-23 23:35:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7588	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

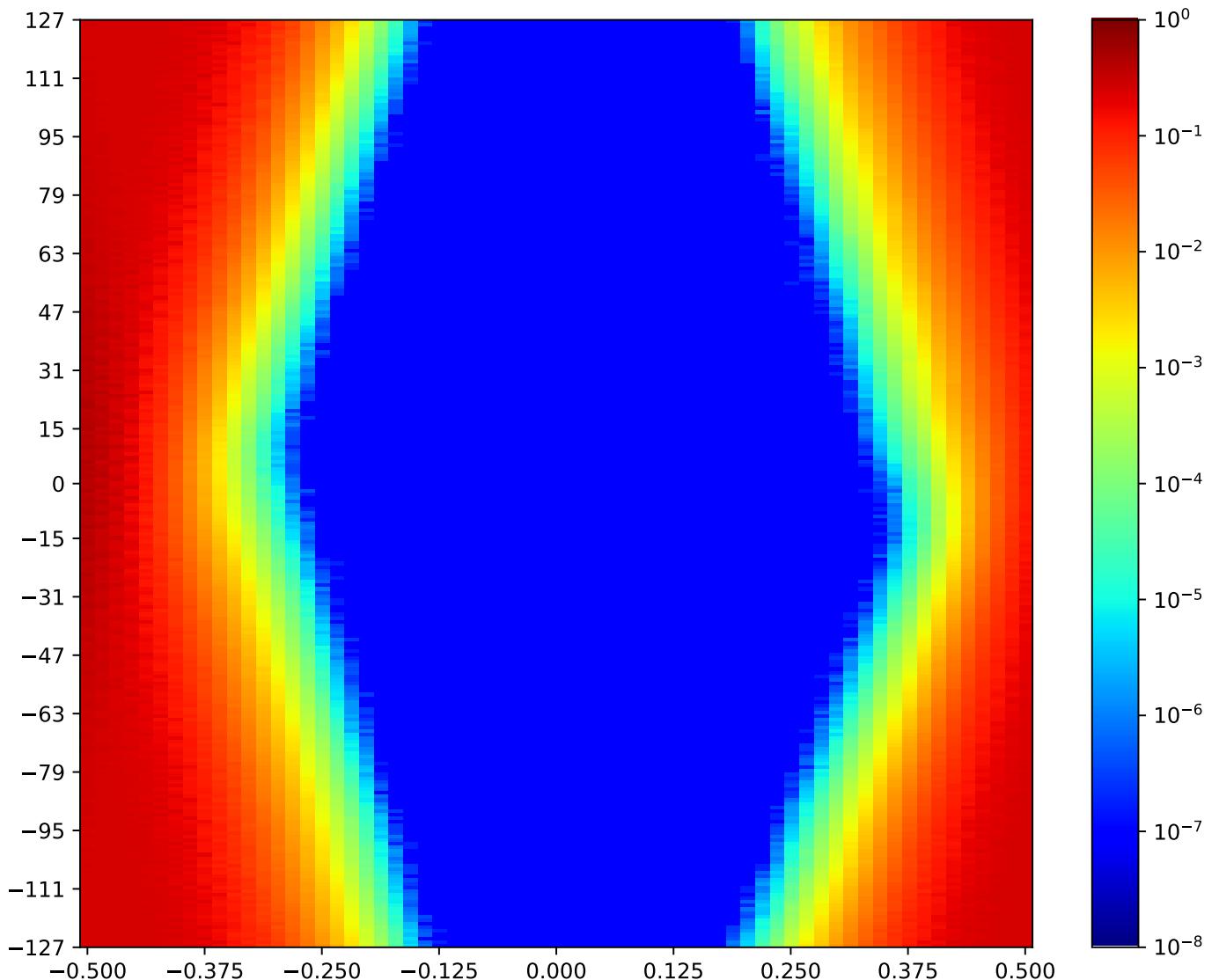


Figure 3.26: MSP\_A\_FPGA-TX2-11-RX15-11-MSP\_C\_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3 MSP\_C TX3 MSP\_A RX7 Minipod Loopback

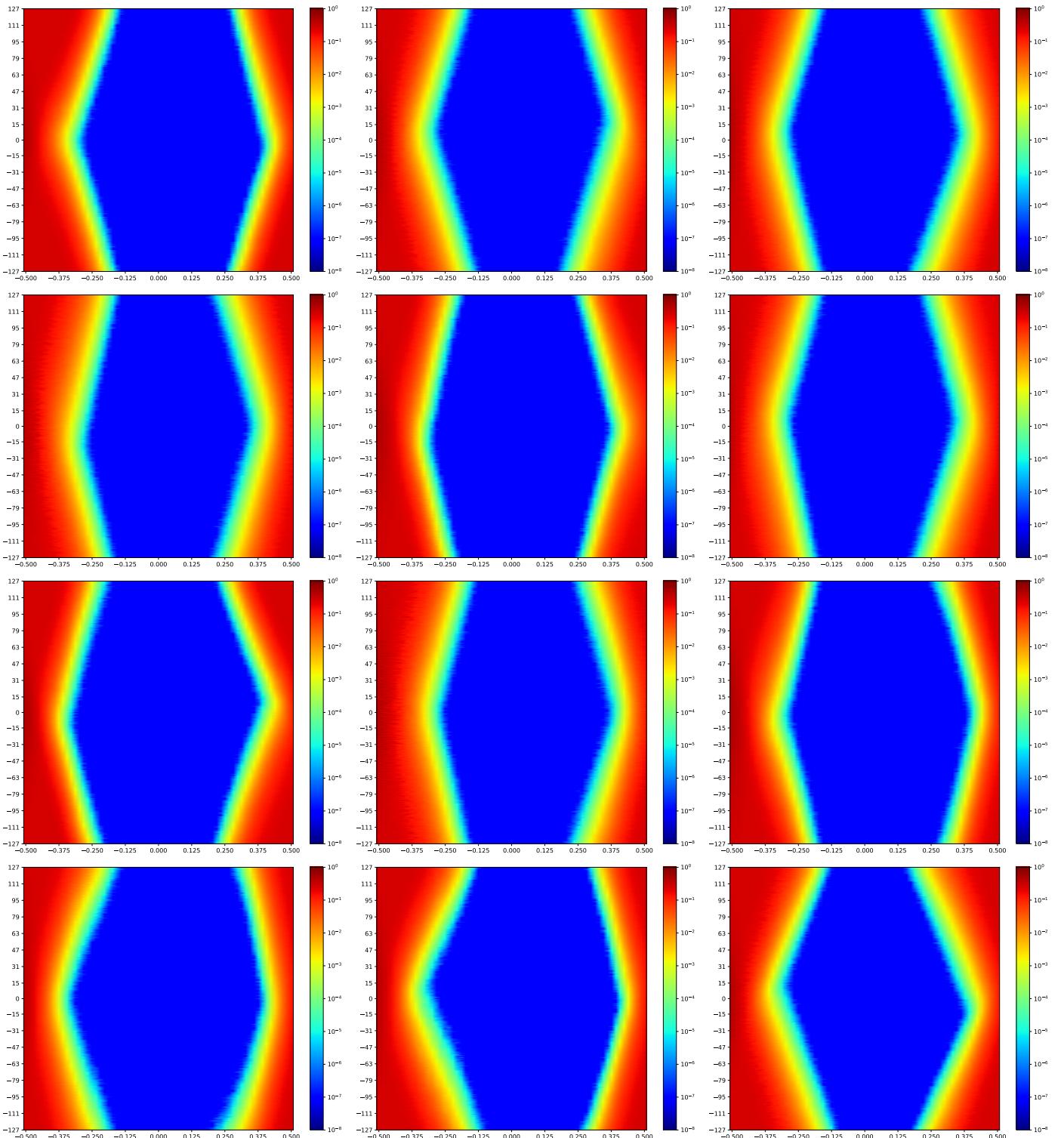


Figure 3.27: MSP\_C TX3 MSP\_A RX7 Minipod Loopback

A cross-reference to Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.40.

### 3.3.1 MSP\_C\_FPGA-TX3-00-RX7-00-MSP\_A\_FPGA

Table 3.25: MSP\_C\_FPGA-TX3-00-RX7-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:37:26		2018-Jan-23 23:37:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8461	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

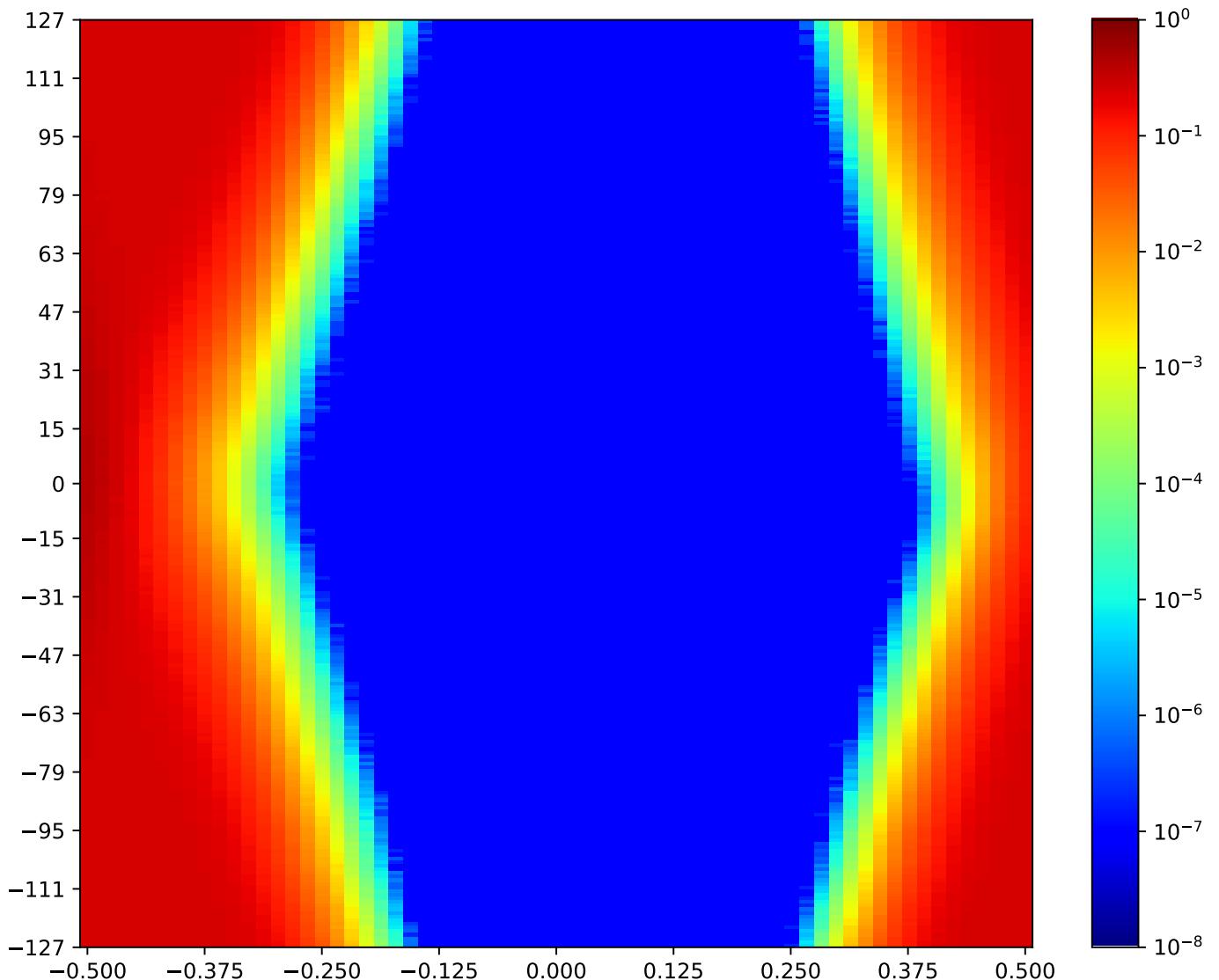


Figure 3.28: MSP\_C\_FPGA-TX3-00-RX7-00-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.2 MSP\_C\_FPGA-TX3-01-RX7-01-MSP\_A\_FPGA

Table 3.26: MSP\_C\_FPGA-TX3-01-RX7-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:38:07		2018-Jan-23 23:38:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7348	36	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

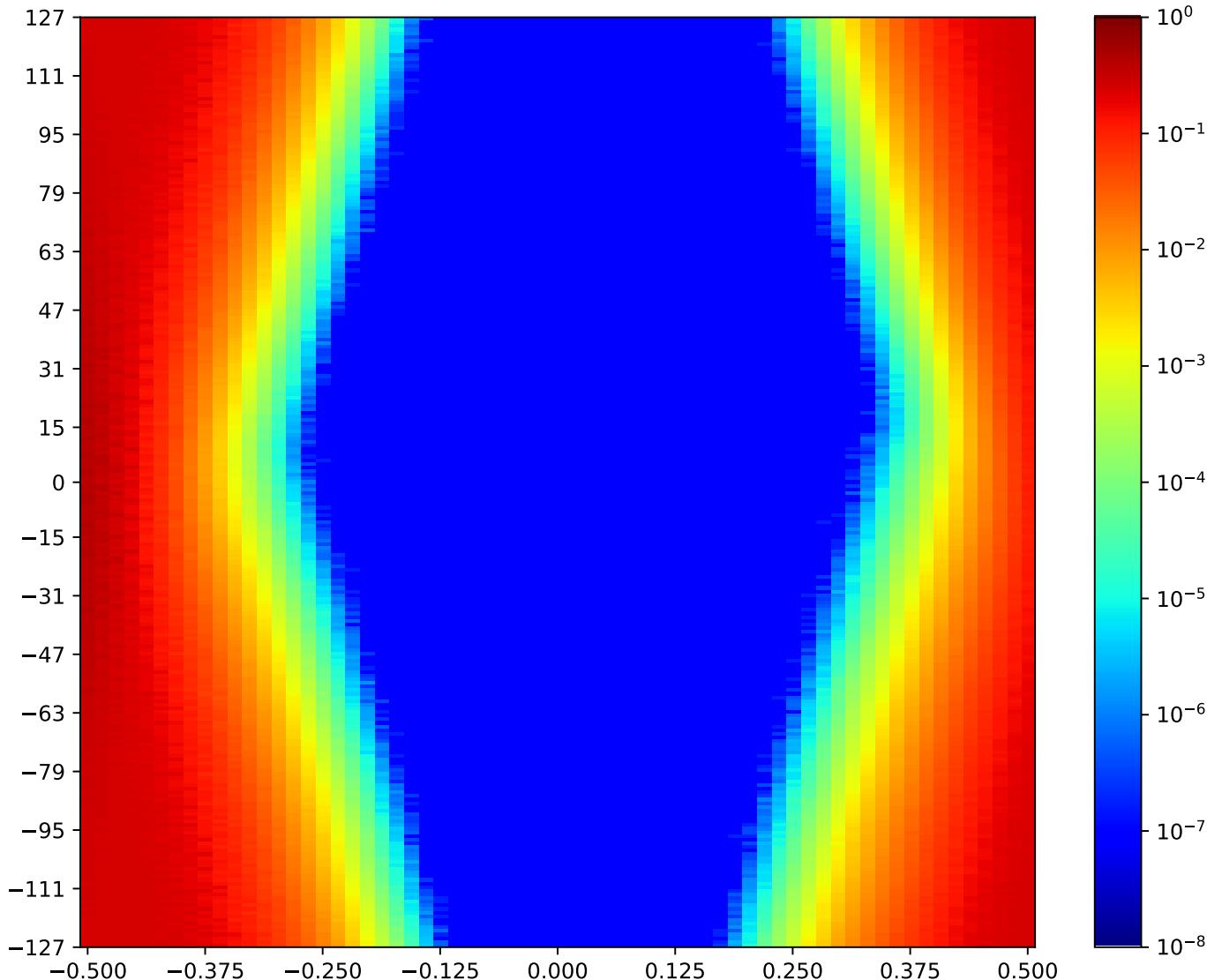


Figure 3.29: MSP\_C\_FPGA-TX3-01-RX7-01-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.3 MSP\_C\_FPGA-TX3-02-RX7-02-MSP\_A\_FPGA

Table 3.27: MSP\_C\_FPGA-TX3-02-RX7-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:38:27		2018-Jan-23 23:38:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7455	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

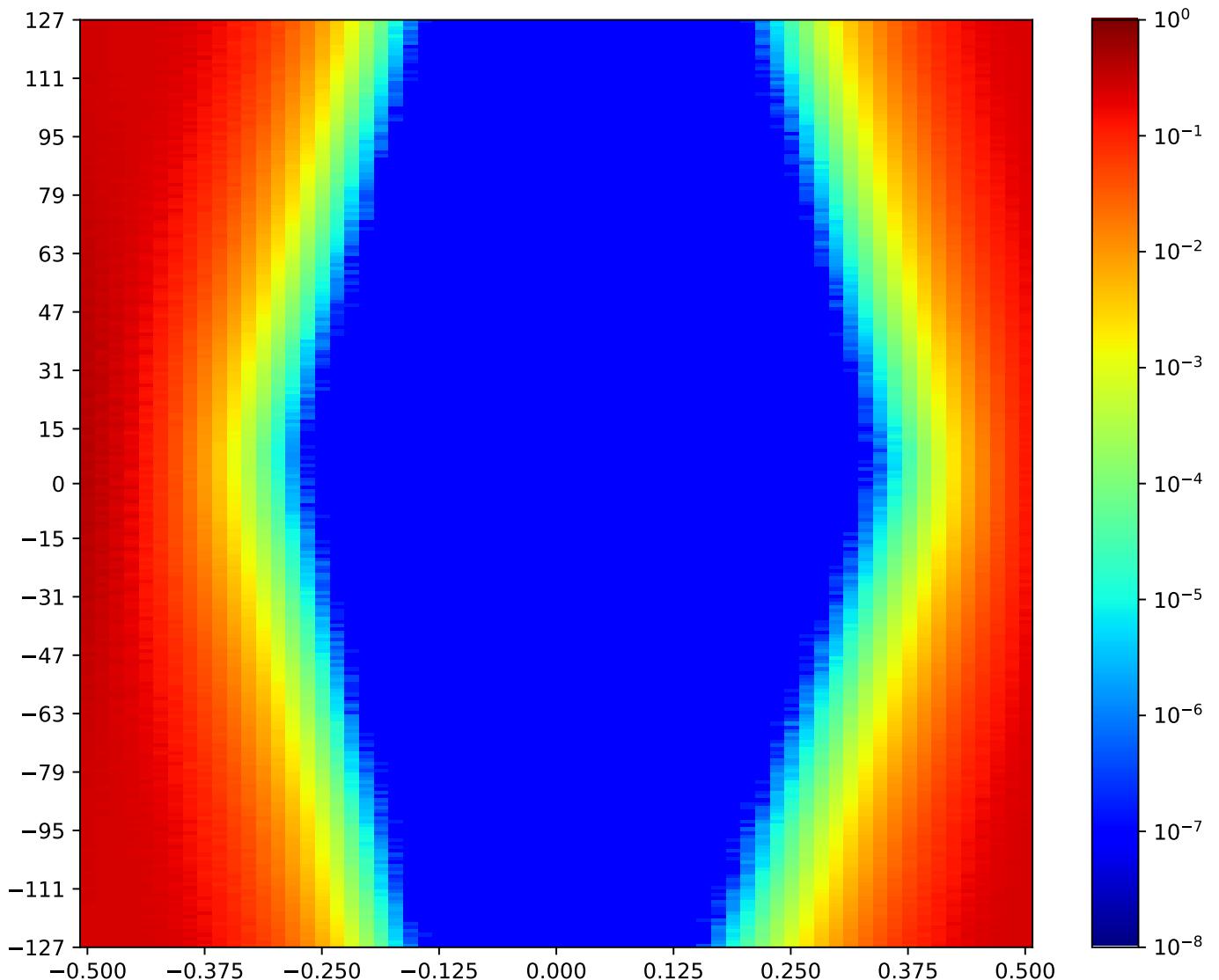


Figure 3.30: MSP\_C\_FPGA-TX3-02-RX7-02-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.4 MSP\_C\_FPGA-TX3-03-RX7-03-MSP\_A\_FPGA

Table 3.28: MSP\_C\_FPGA-TX3-03-RX7-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:36:45		2018-Jan-23 23:37:05	
Reset RX	OA	HO		HO (%)	
true	7479	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

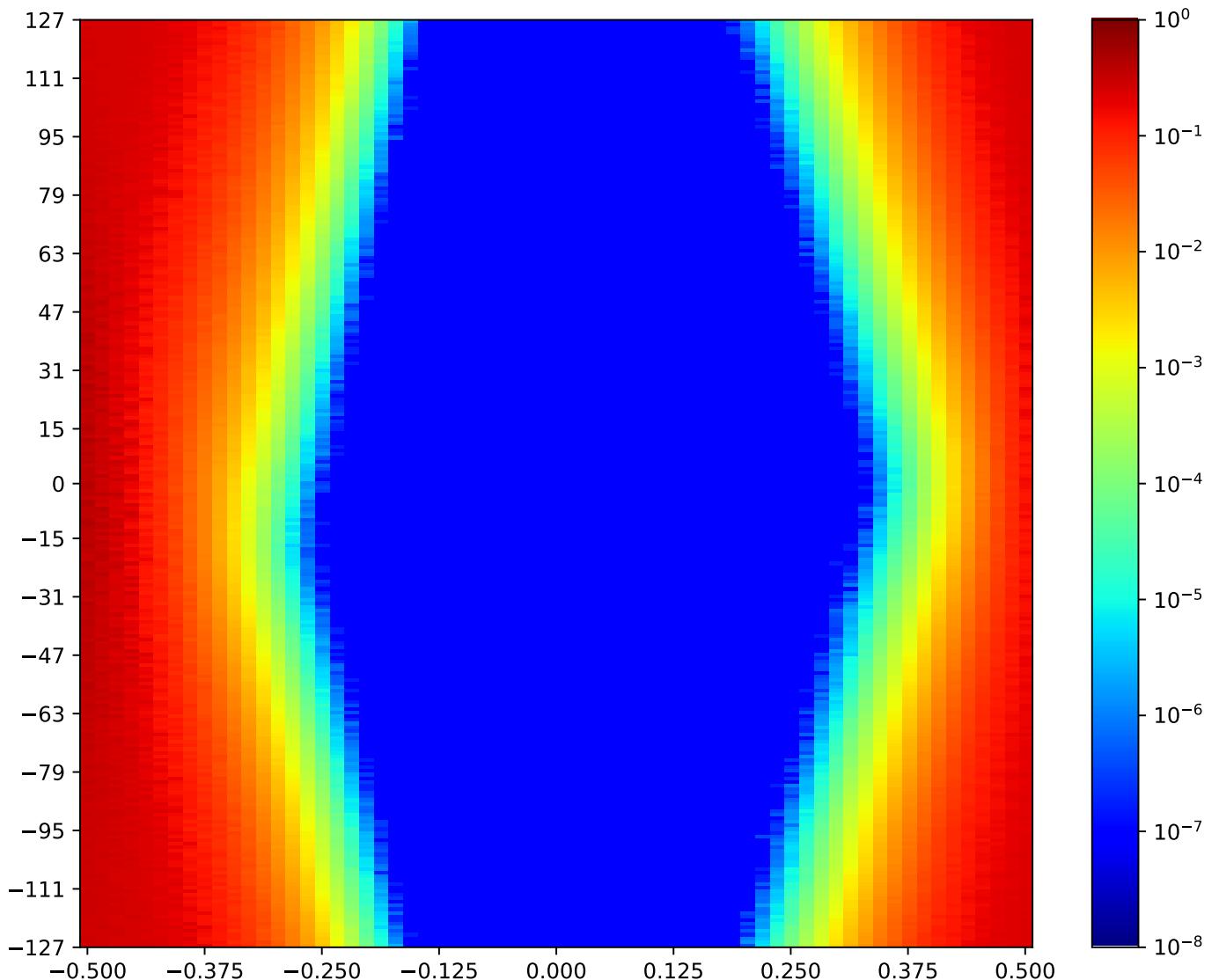


Figure 3.31: MSP\_C\_FPGA-TX3-03-RX7-03-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.5 MSP\_C\_FPGA-TX3-04-RX7-04-MSP\_A\_FPGA

Table 3.29: MSP\_C\_FPGA-TX3-04-RX7-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:39:28		2018-Jan-23 23:39:48	
Reset RX	OA	HO		VO   VO (%)	
true	8625	41		63.08%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

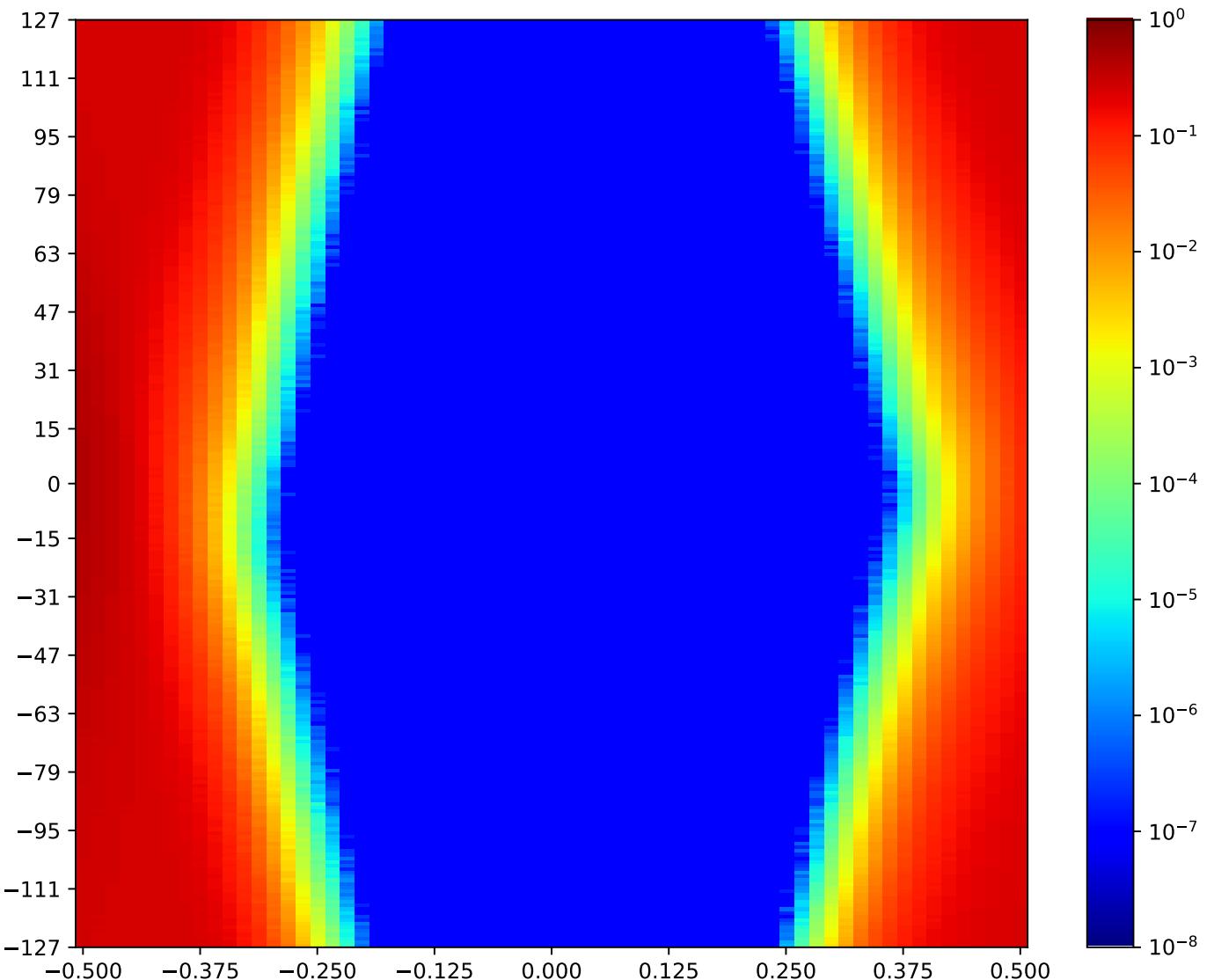


Figure 3.32: MSP\_C\_FPGA-TX3-04-RX7-04-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.6 MSP\_C\_FPGA-TX3-05-RX7-05-MSP\_A\_FPGA

Table 3.30: MSP\_C\_FPGA-TX3-05-RX7-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:36:24		2018-Jan-23 23:36:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7365	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

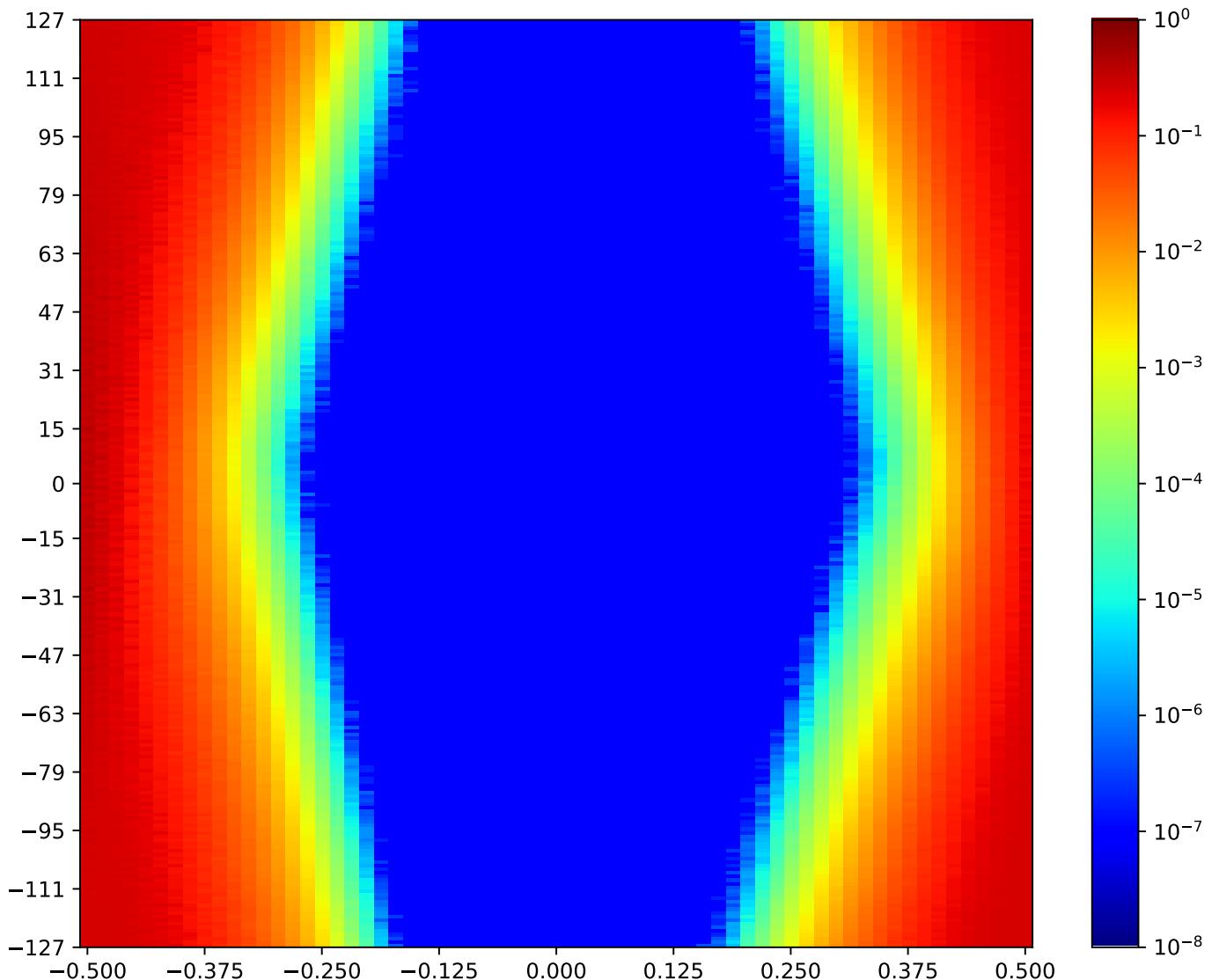


Figure 3.33: MSP\_C\_FPGA-TX3-05-RX7-05-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.7 MSP\_C\_FPGA-TX3-06-RX7-06-MSP\_A\_FPGA

Table 3.31: MSP\_C\_FPGA-TX3-06-RX7-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:40:08		2018-Jan-23 23:40:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8644	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

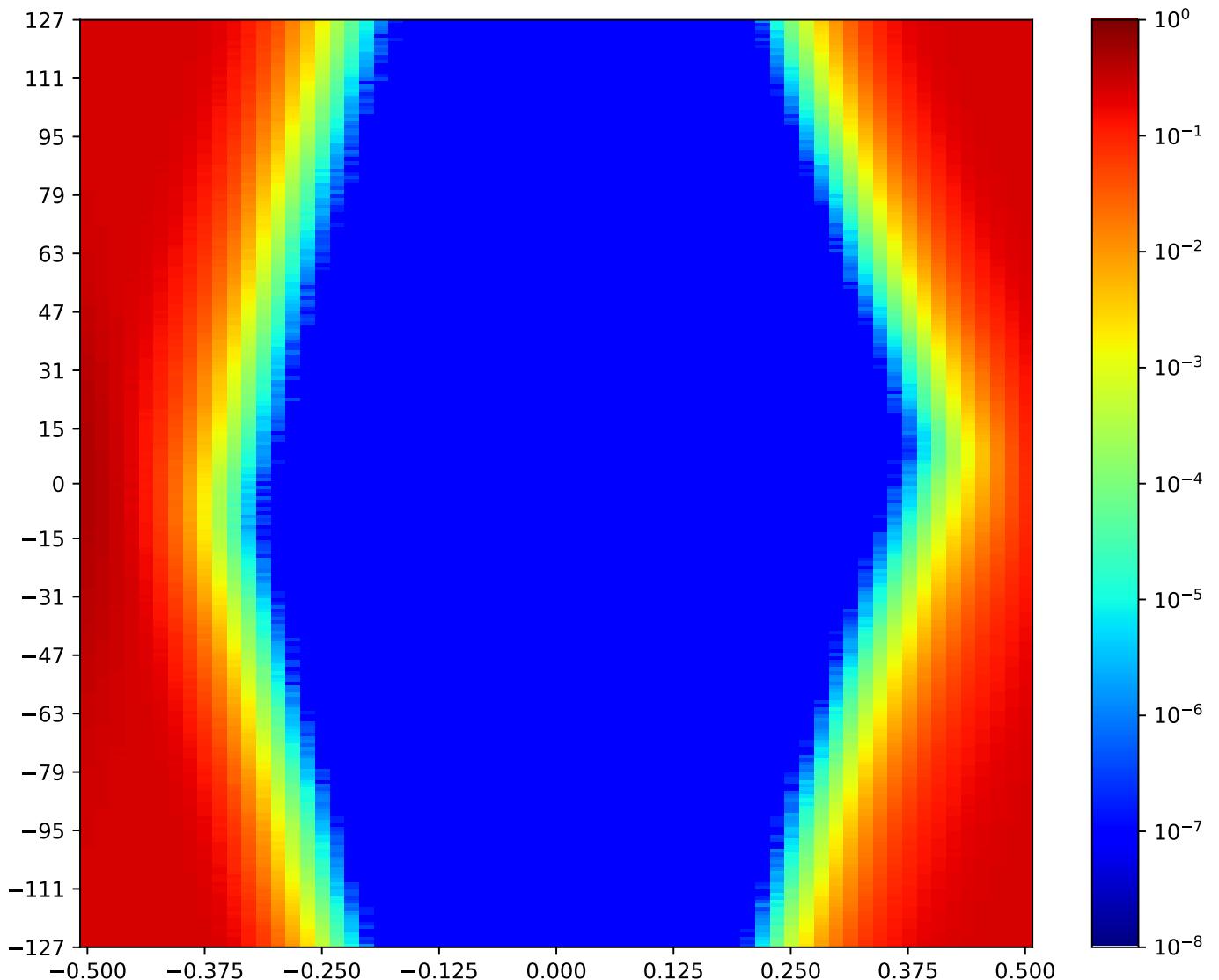


Figure 3.34: MSP\_C\_FPGA-TX3-06-RX7-06-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.8 MSP\_C\_FPGA-TX3-07-RX7-07-MSP\_A\_FPGA

Table 3.32: MSP\_C\_FPGA-TX3-07-RX7-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:37:06		2018-Jan-23 23:37:26	
Reset RX	OA	HO		HO (%)	
true	7651	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

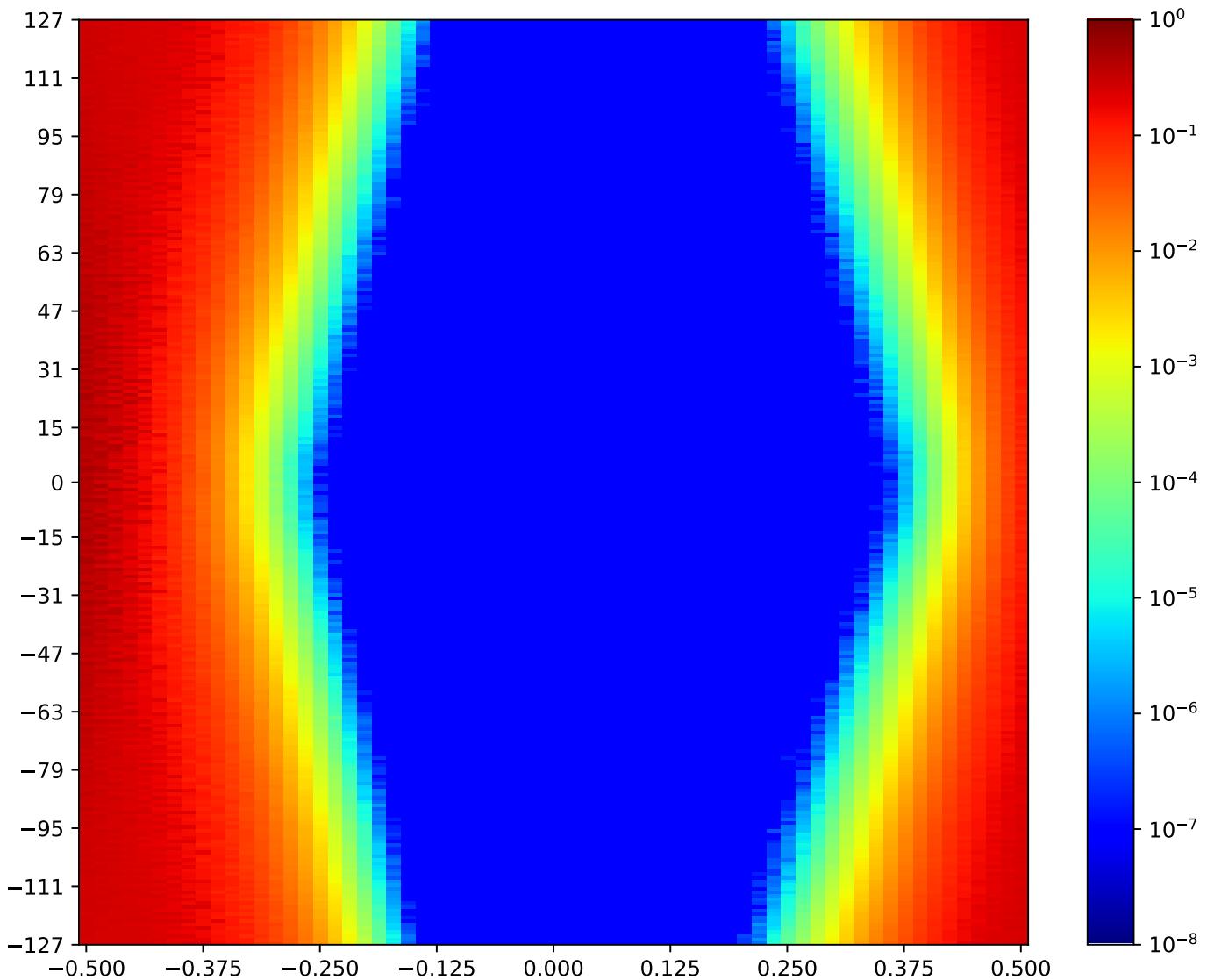


Figure 3.35: MSP\_C\_FPGA-TX3-07-RX7-07-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.9 MSP\_C\_FPGA-TX3-08-RX7-08-MSP\_A\_FPGA

Table 3.33: MSP\_C\_FPGA-TX3-08-RX7-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:39:48		2018-Jan-23 23:40:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8655	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

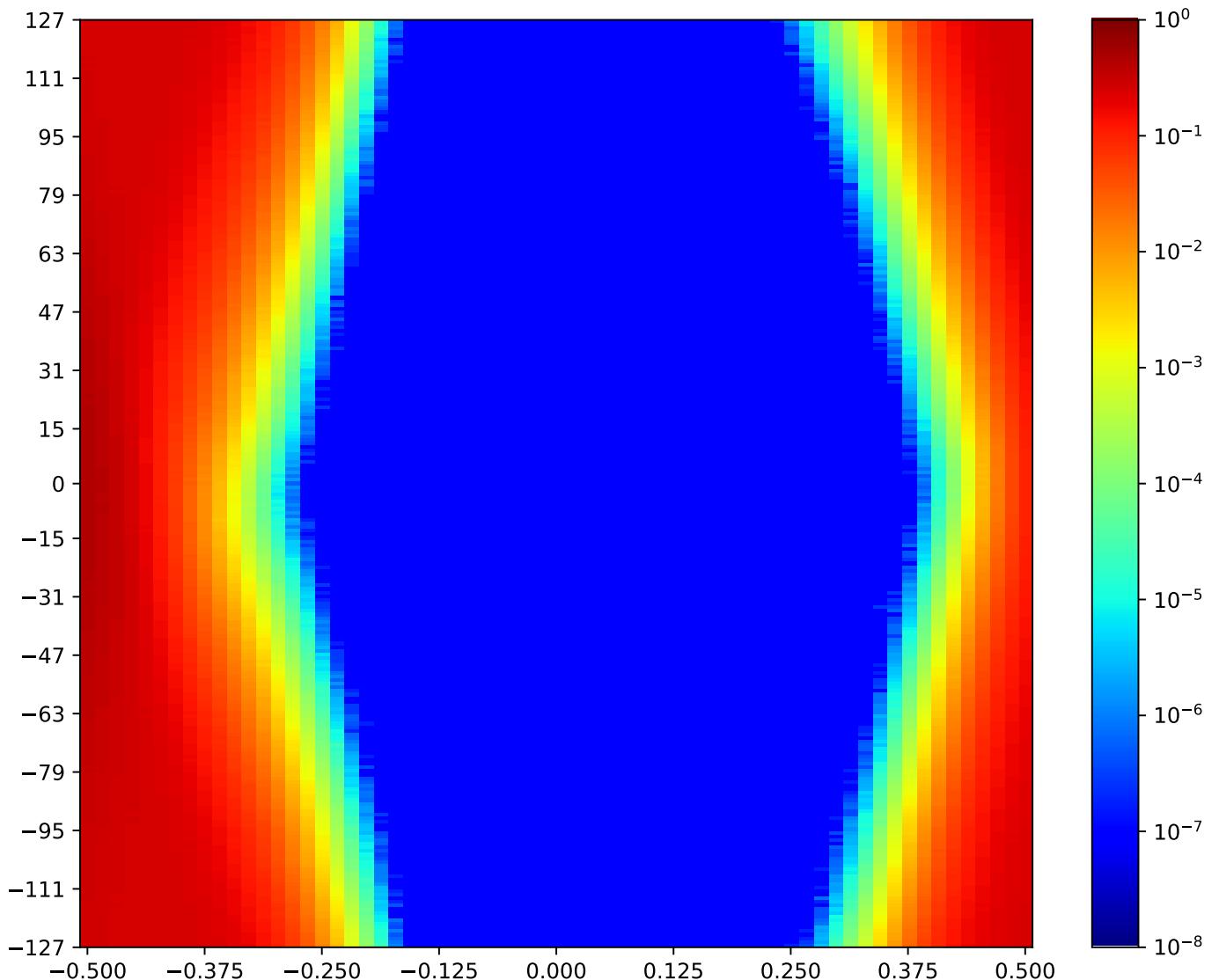


Figure 3.36: MSP\_C\_FPGA-TX3-08-RX7-08-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.10 MSP\_C\_FPGA-TX3-09-RX7-09-MSP\_A\_FPGA

Table 3.34: MSP\_C\_FPGA-TX3-09-RX7-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:37:46		2018-Jan-23 23:38:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8835	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

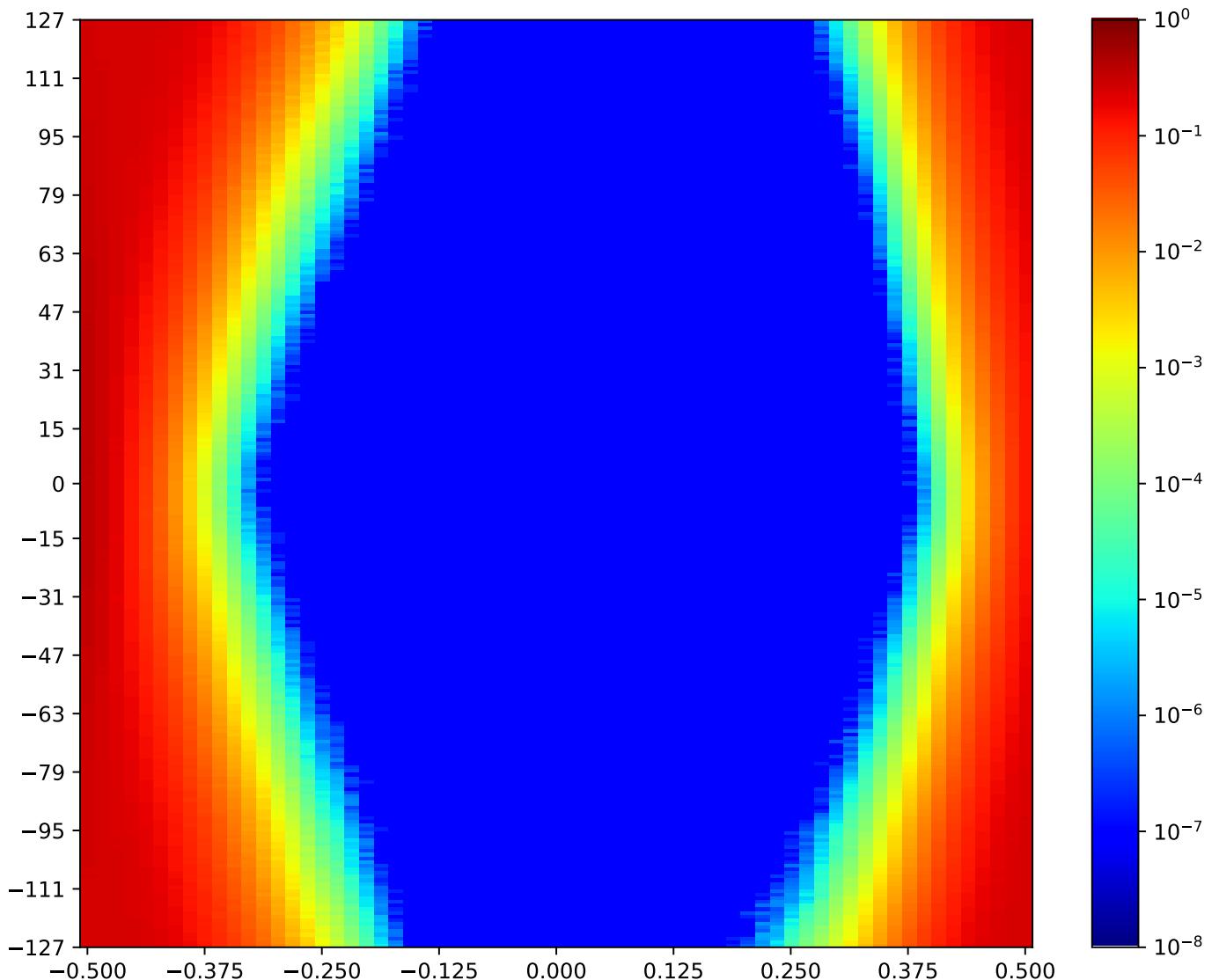


Figure 3.37: MSP\_C\_FPGA-TX3-09-RX7-09-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.11 MSP\_C\_FPGA-TX3-10-RX7-10-MSP\_A\_FPGA

Table 3.35: MSP\_C\_FPGA-TX3-10-RX7-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:39:07		2018-Jan-23 23:39:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8522	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

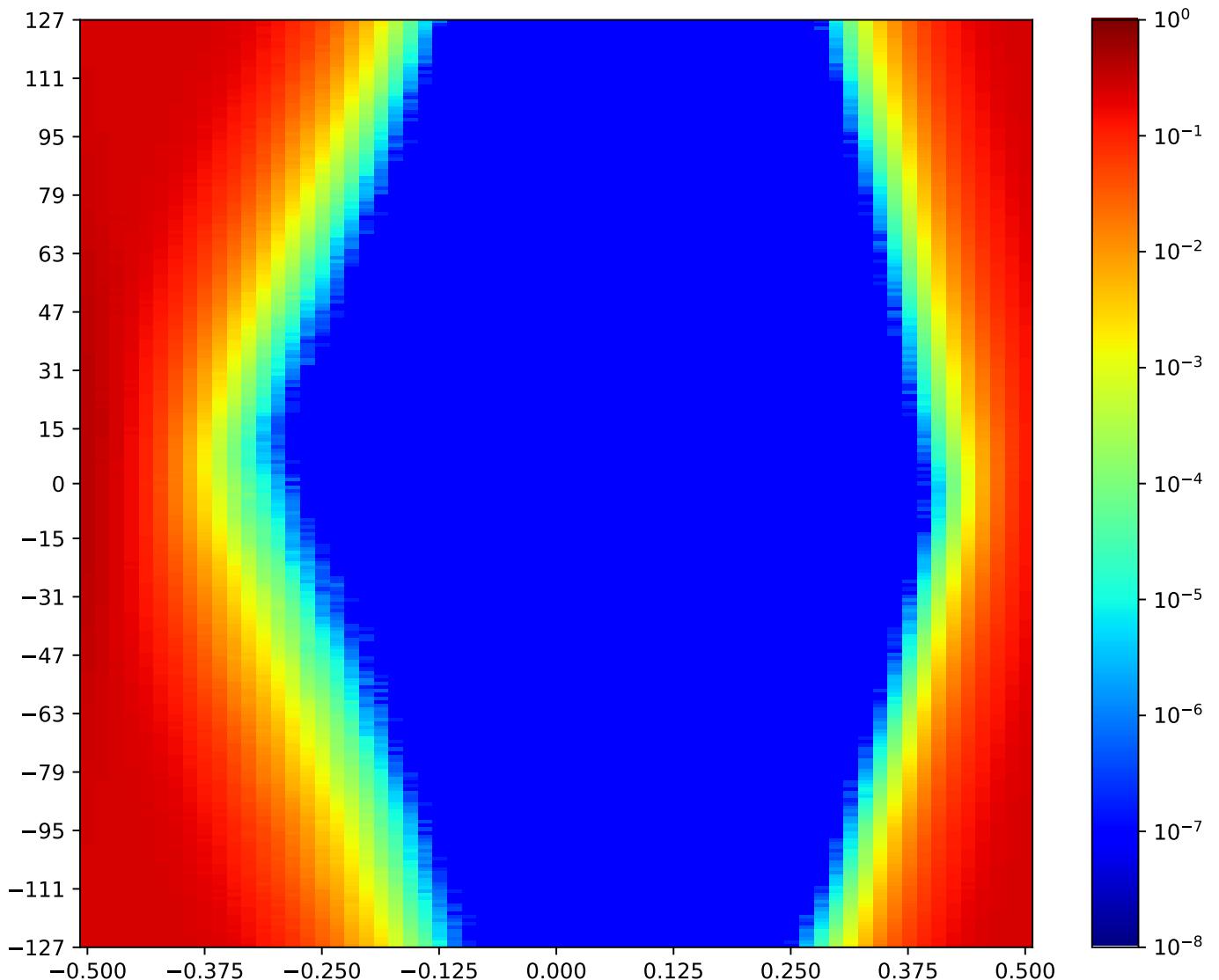


Figure 3.38: MSP\_C\_FPGA-TX3-10-RX7-10-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.3.12 MSP\_C\_FPGA-TX3-11-RX7-11-MSP\_A\_FPGA

Table 3.36: MSP\_C\_FPGA-TX3-11-RX7-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:38:47		2018-Jan-23 23:39:07	
Reset RX	OA	HO		HO (%)	
true	7328	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

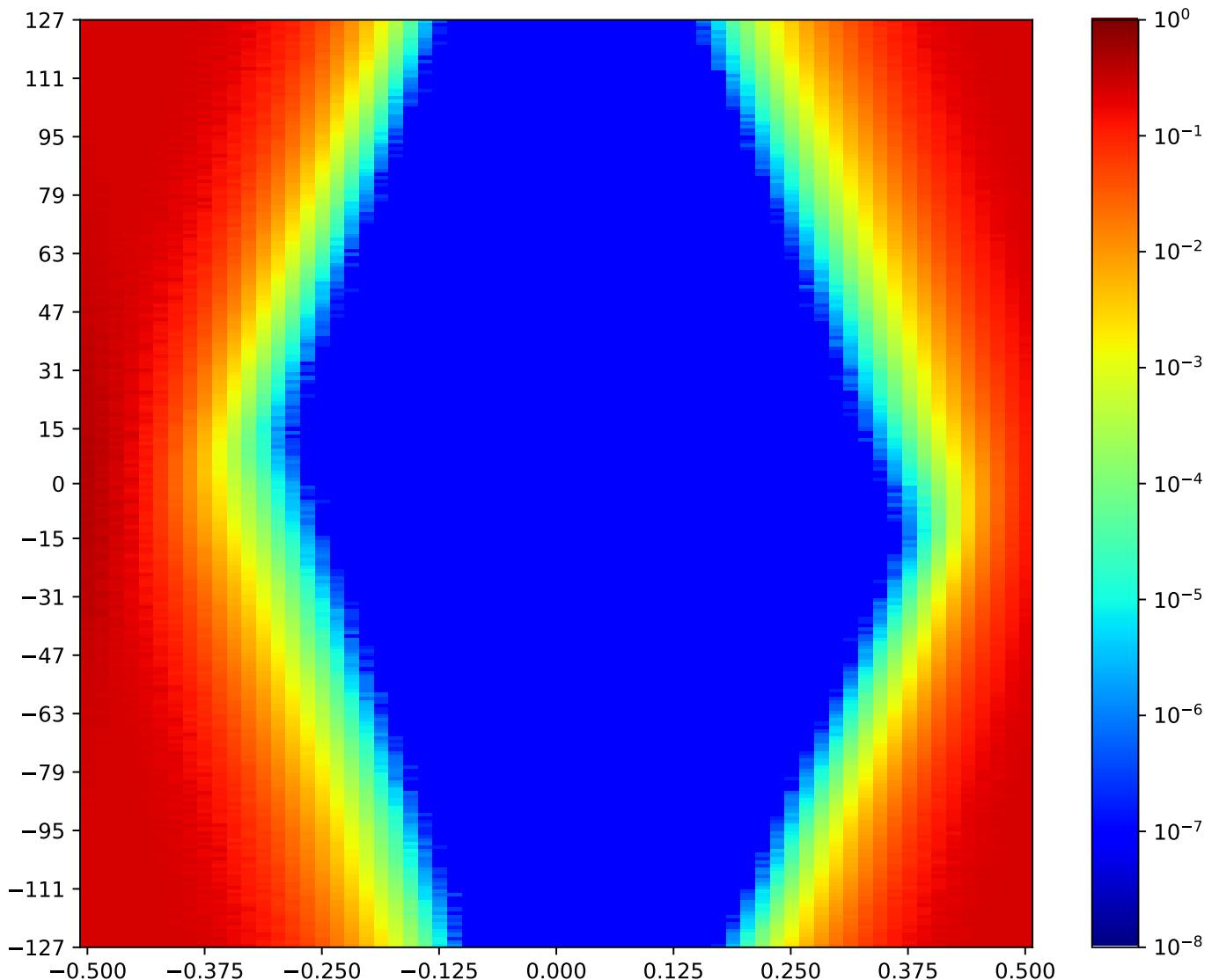


Figure 3.39: MSP\_C\_FPGA-TX3-11-RX7-11-MSP\_A\_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4 MSP\_C TX4 MSP\_A RX6 Minipod Loopback

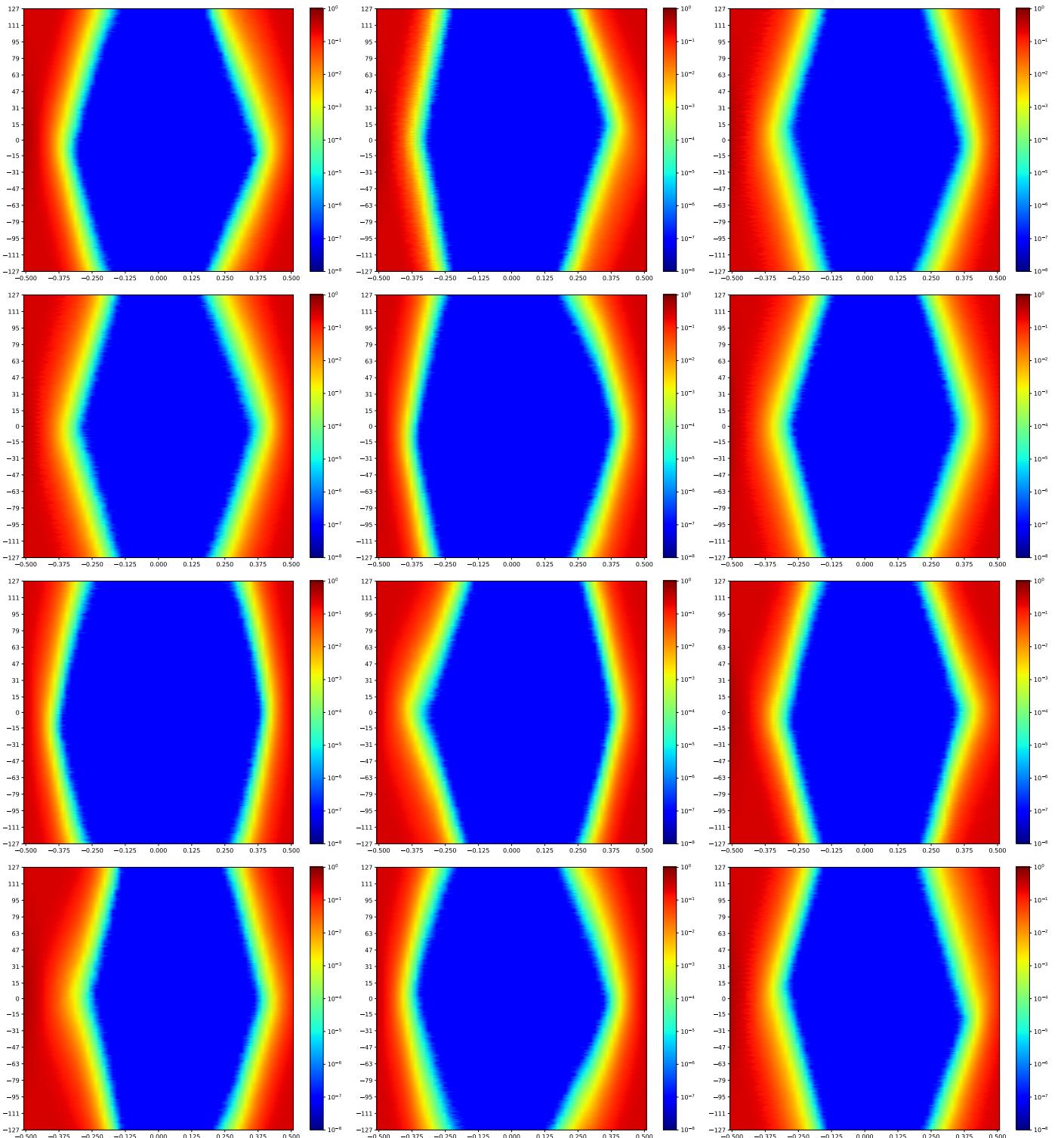


Figure 3.40: MSP\_C TX4 MSP\_A RX6 Minipod Loopback

A cross-reference to Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.53.

### 3.4.1 MSP\_C\_FPGA-TX4-00-RX6-00-MSP\_A\_FPGA

Table 3.37: MSP\_C\_FPGA-TX4-00-RX6-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:41:29		2018-Jan-23 23:41:49	
Reset RX	OA	HO		HO (%)	
true	8049	40		61.54%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

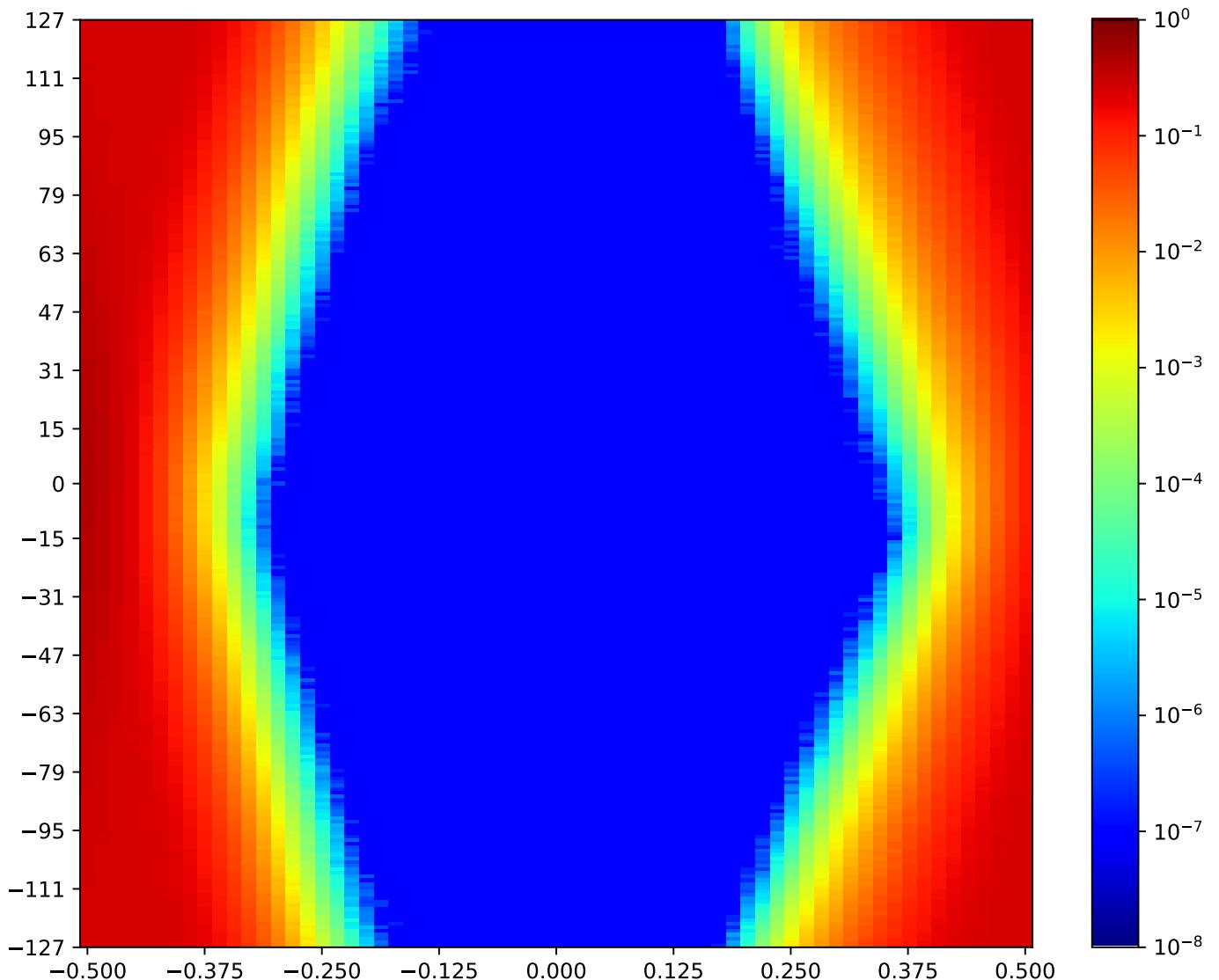


Figure 3.41: MSP\_C\_FPGA-TX4-00-RX6-00-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.2 MSP\_C\_FPGA-TX4-01-RX6-01-MSP\_A\_FPGA

Table 3.38: MSP\_C\_FPGA-TX4-01-RX6-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:40:49		2018-Jan-23 23:41:09	
Reset RX	OA	HO		HO (%)	
true	8514	40		61.54%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

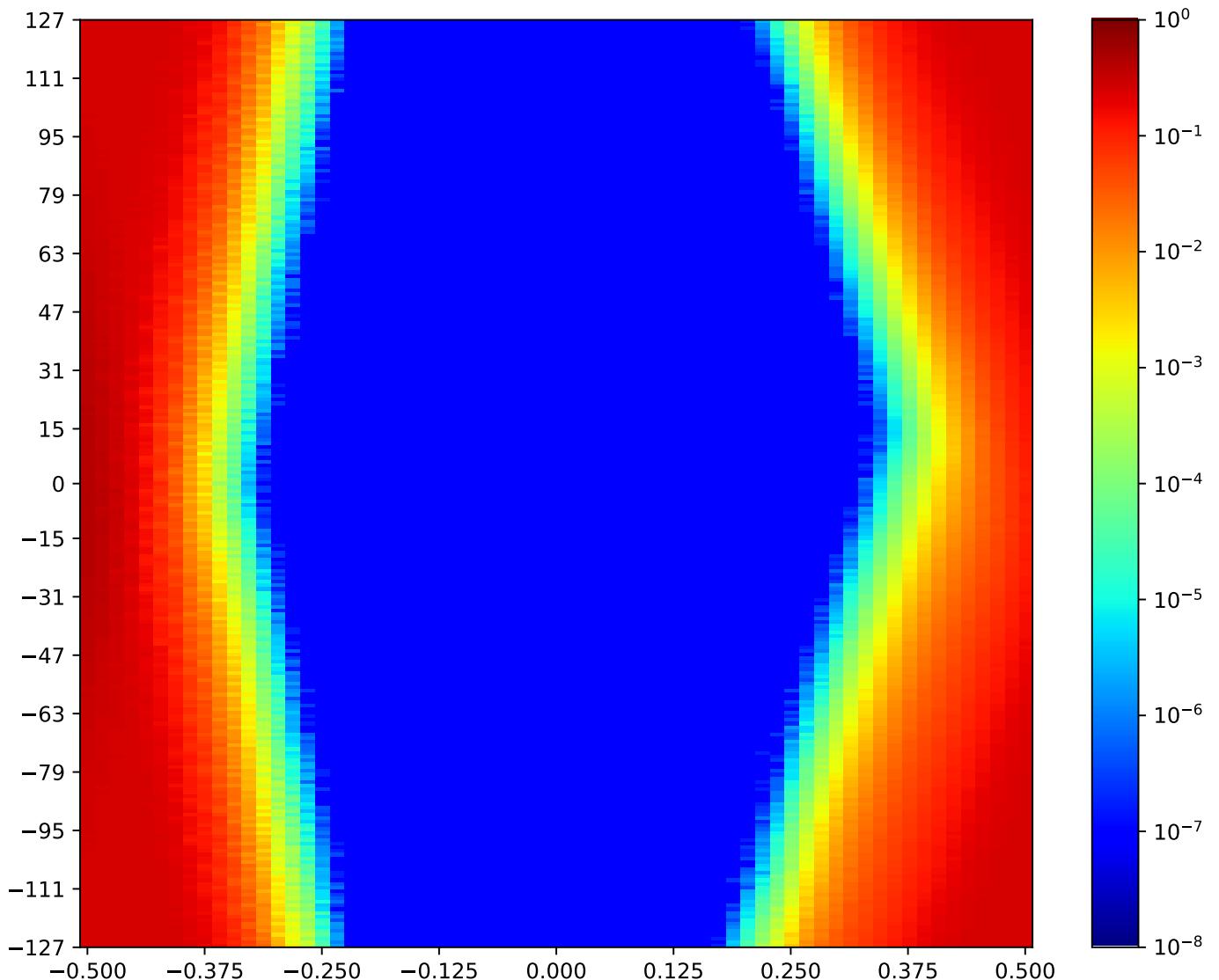


Figure 3.42: MSP\_C\_FPGA-TX4-01-RX6-01-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.3 MSP\_C\_FPGA-TX4-02-RX6-02-MSP\_A\_FPGA

Table 3.39: MSP\_C\_FPGA-TX4-02-RX6-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:42:30		2018-Jan-23 23:42:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7417	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

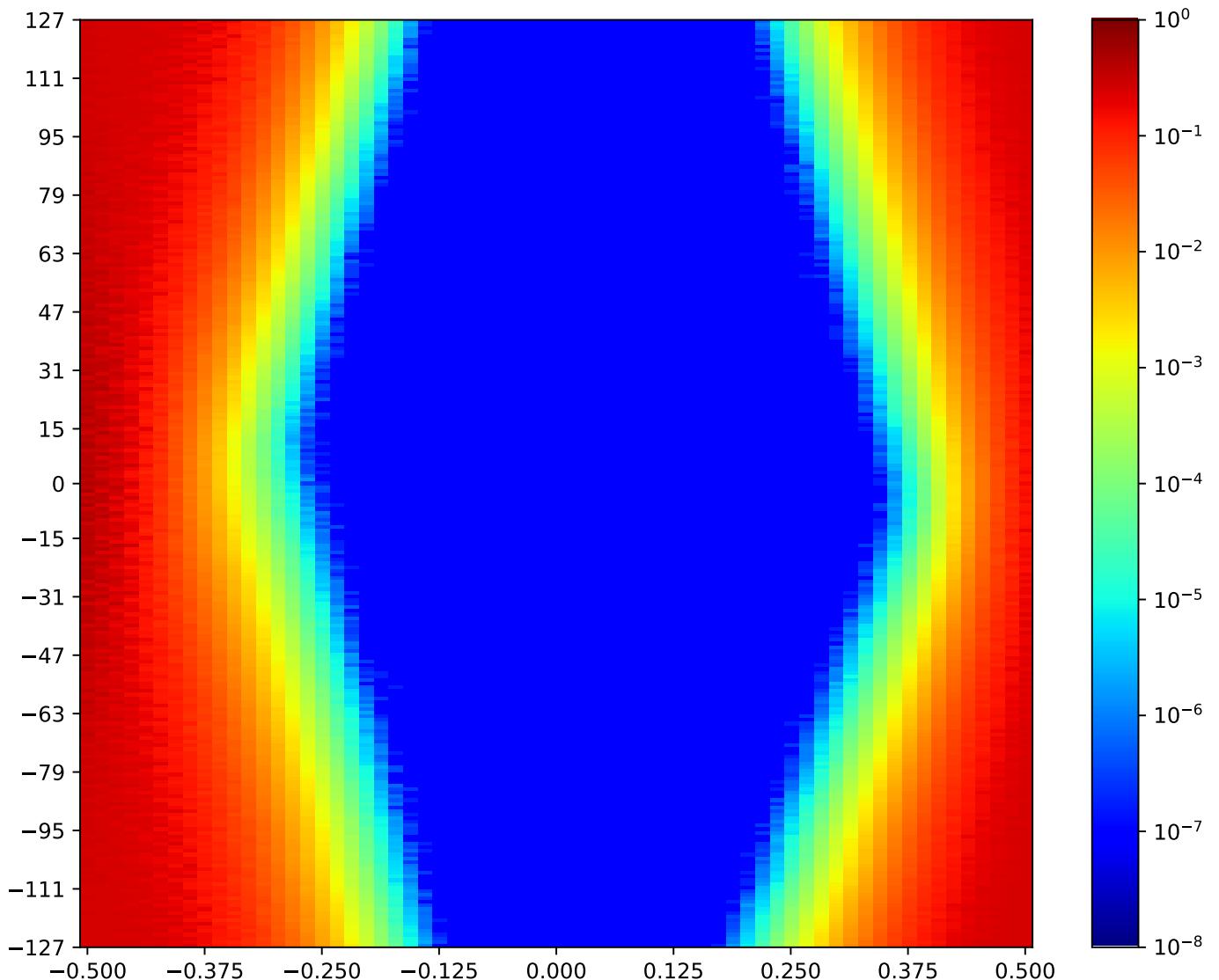


Figure 3.43: MSP\_C\_FPGA-TX4-02-RX6-02-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.4 MSP\_C\_FPGA-TX4-03-RX6-03-MSP\_A\_FPGA

Table 3.40: MSP\_C\_FPGA-TX4-03-RX6-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:40:29		2018-Jan-23 23:40:49	
Reset RX	OA	HO		HO (%)	
true	7328	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

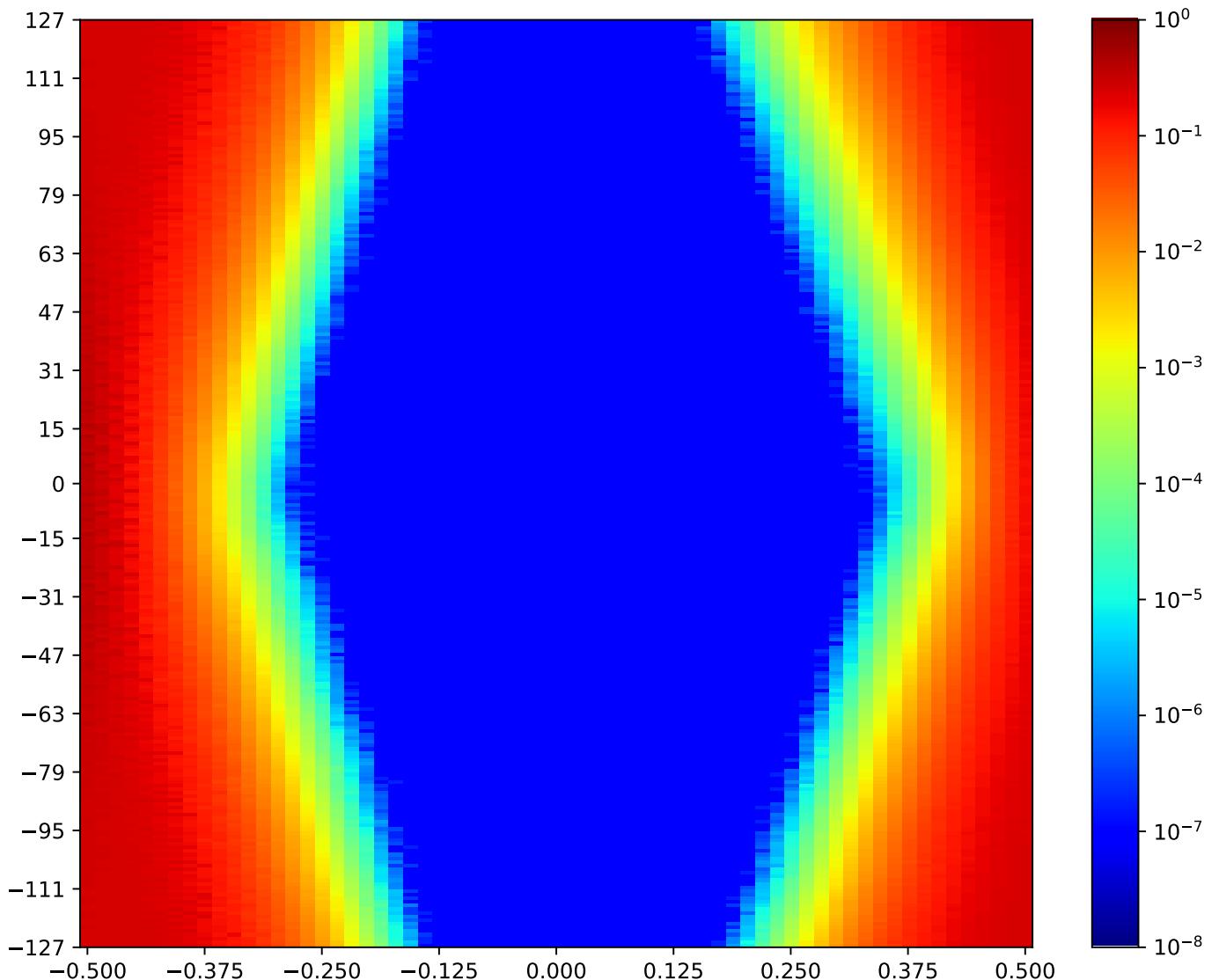


Figure 3.44: MSP\_C\_FPGA-TX4-03-RX6-03-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.5 MSP\_C\_FPGA-TX4-04-RX6-04-MSP\_A\_FPGA

Table 3.41: MSP\_C\_FPGA-TX4-04-RX6-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:43:31		2018-Jan-23 23:43:51	
Reset RX	OA	HO		HO (%)	
true	9465	46		70.77%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

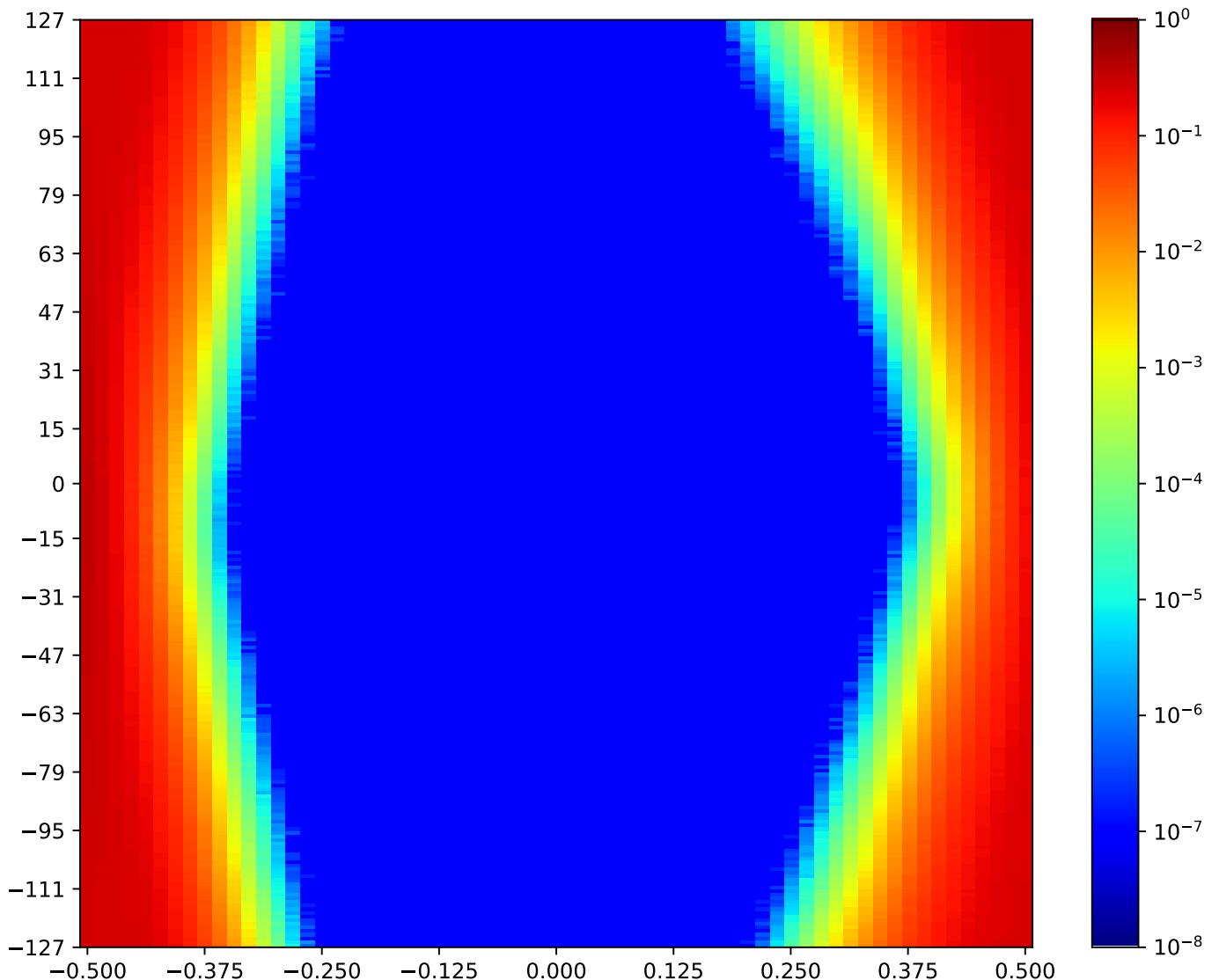


Figure 3.45: MSP\_C\_FPGA-TX4-04-RX6-04-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.6 MSP\_C\_FPGA-TX4-05-RX6-05-MSP\_A\_FPGA

Table 3.42: MSP\_C\_FPGA-TX4-05-RX6-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:41:09		2018-Jan-23 23:41:29	
Reset RX	OA	HO		HO (%)	
true	7266	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

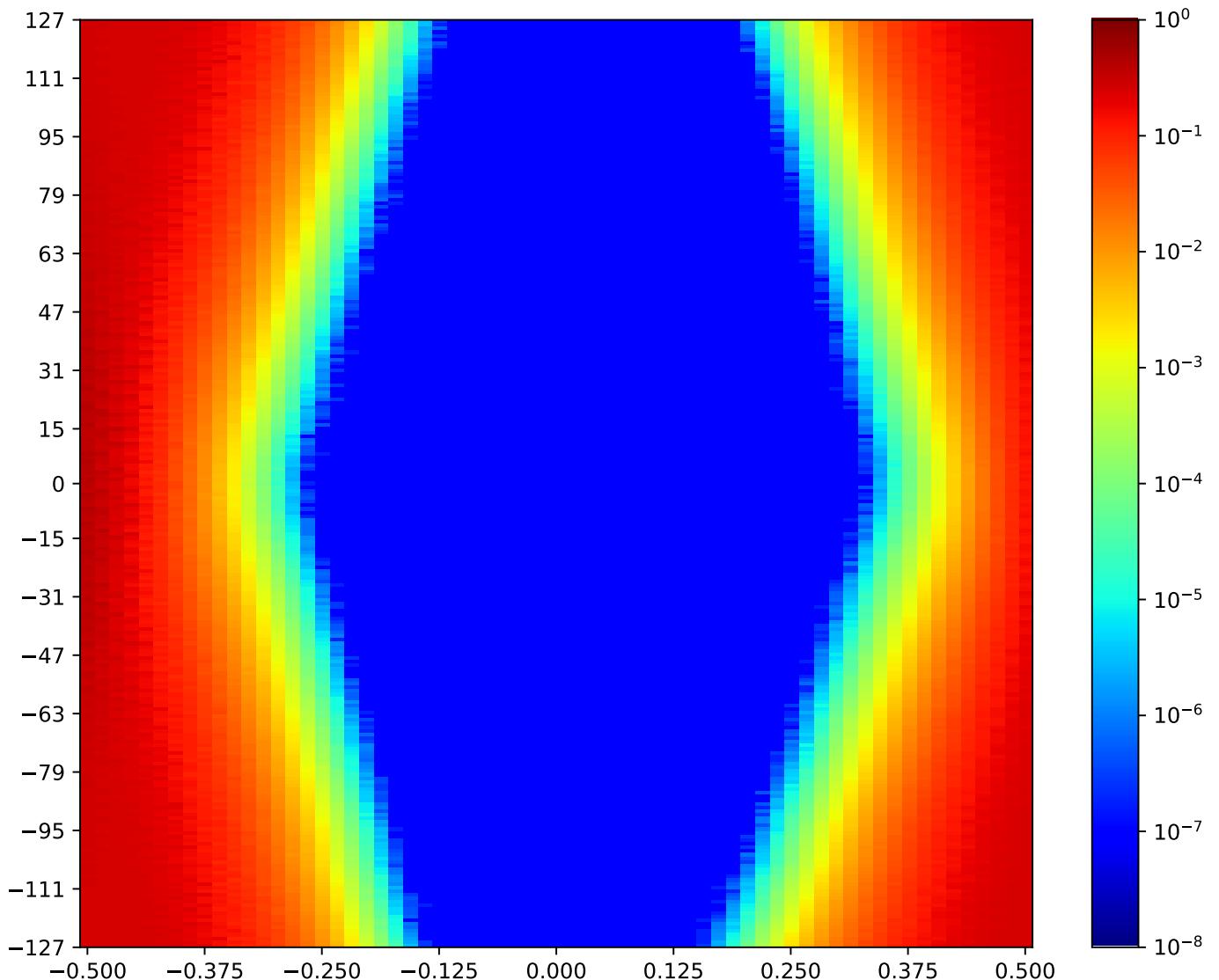


Figure 3.46: MSP\_C\_FPGA-TX4-05-RX6-05-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.7 MSP\_C\_FPGA-TX4-06-RX6-06-MSP\_A\_FPGA

Table 3.43: MSP\_C\_FPGA-TX4-06-RX6-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:44:12		2018-Jan-23 23:44:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10205	47	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

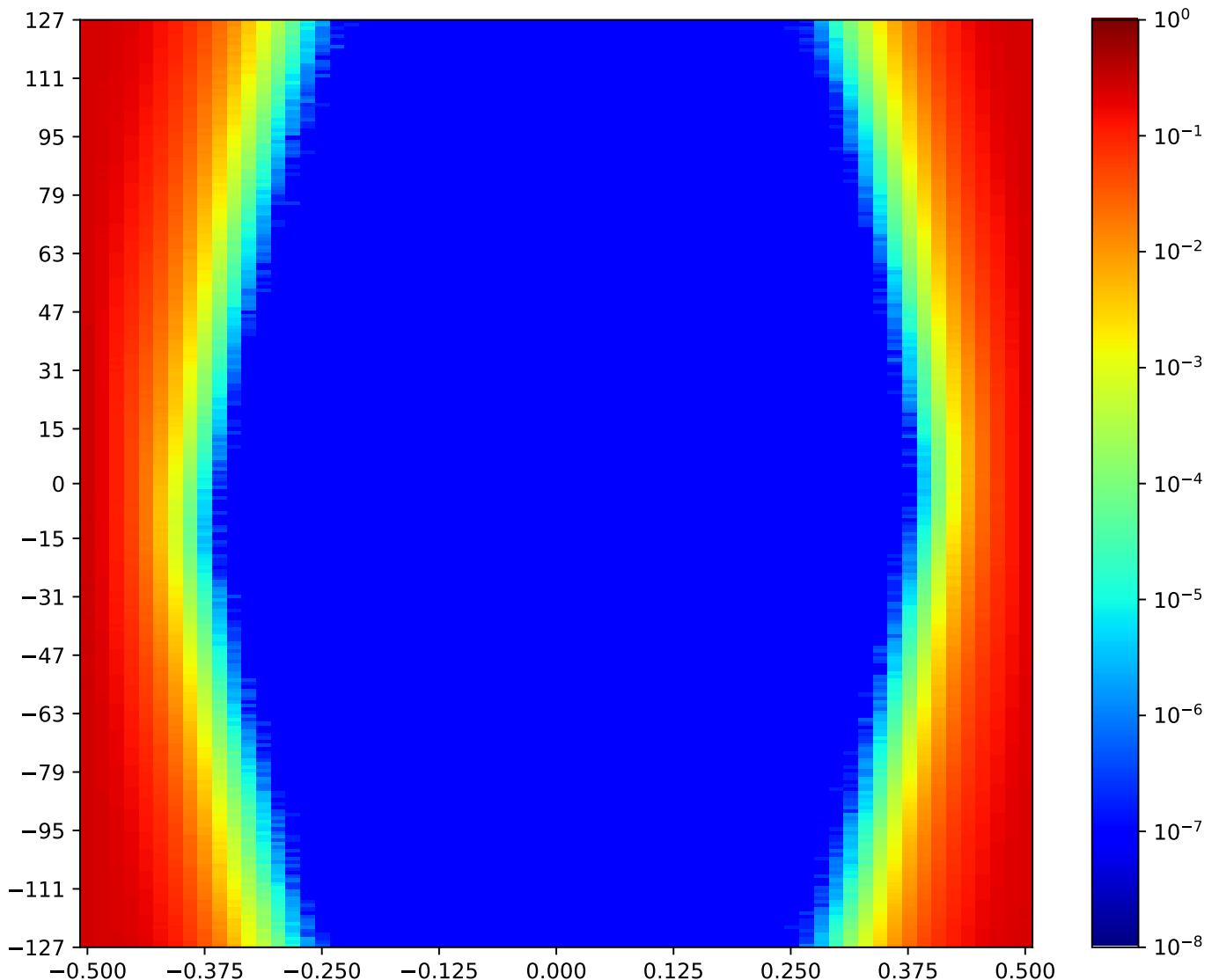


Figure 3.47: MSP\_C\_FPGA-TX4-06-RX6-06-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.8 MSP\_C\_FPGA-TX4-07-RX6-07-MSP\_A\_FPGA

Table 3.44: MSP\_C\_FPGA-TX4-07-RX6-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:41:49		2018-Jan-23 23:42:09	
Reset RX	OA	HO		HO (%)	
true	8571	42		64.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

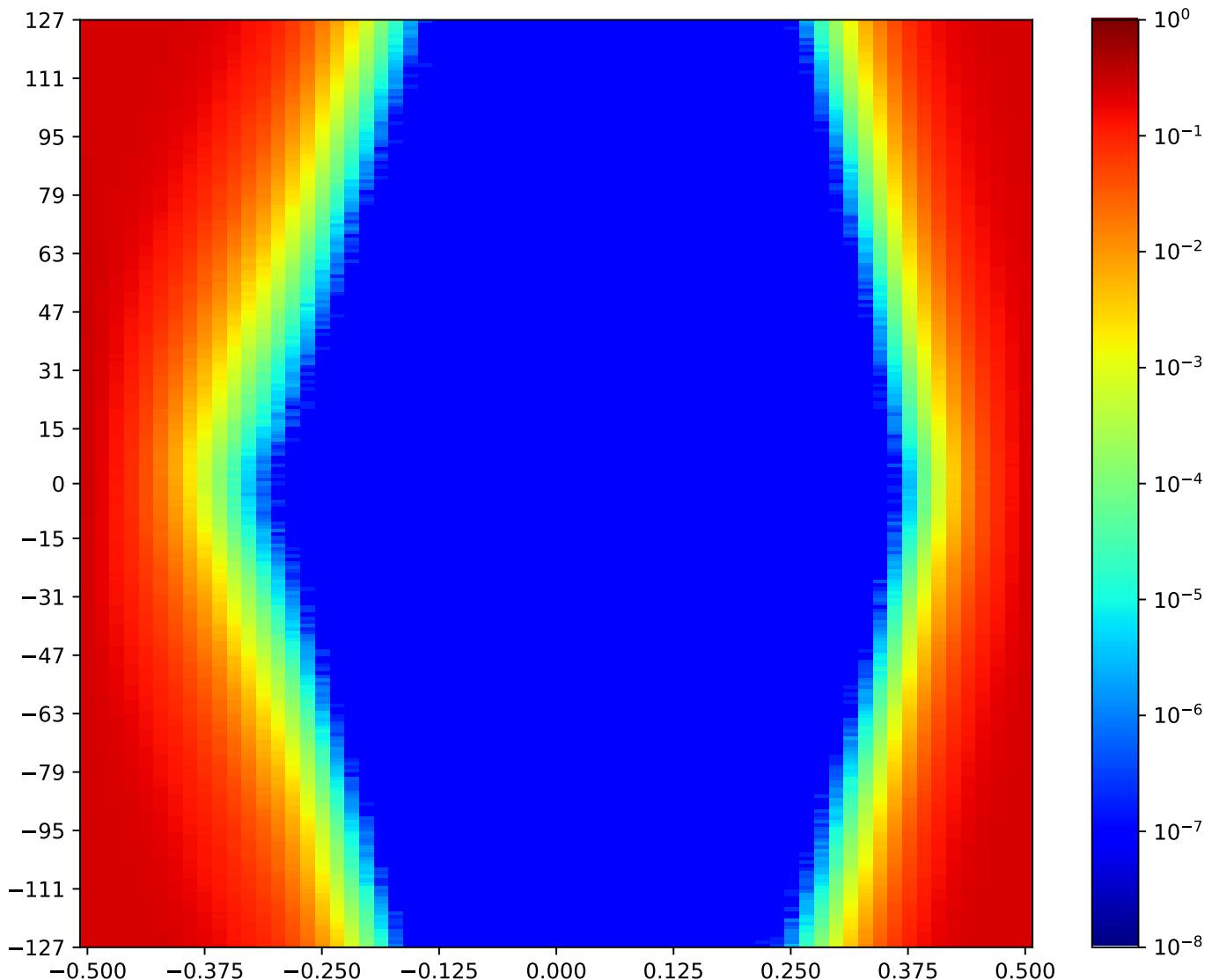


Figure 3.48: MSP\_C\_FPGA-TX4-07-RX6-07-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.9 MSP\_C\_FPGA-TX4-08-RX6-08-MSP\_A\_FPGA

Table 3.45: MSP\_C\_FPGA-TX4-08-RX6-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:43:52		2018-Jan-23 23:44:12	
Reset RX	OA	HO		HO (%)	
true	7631	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

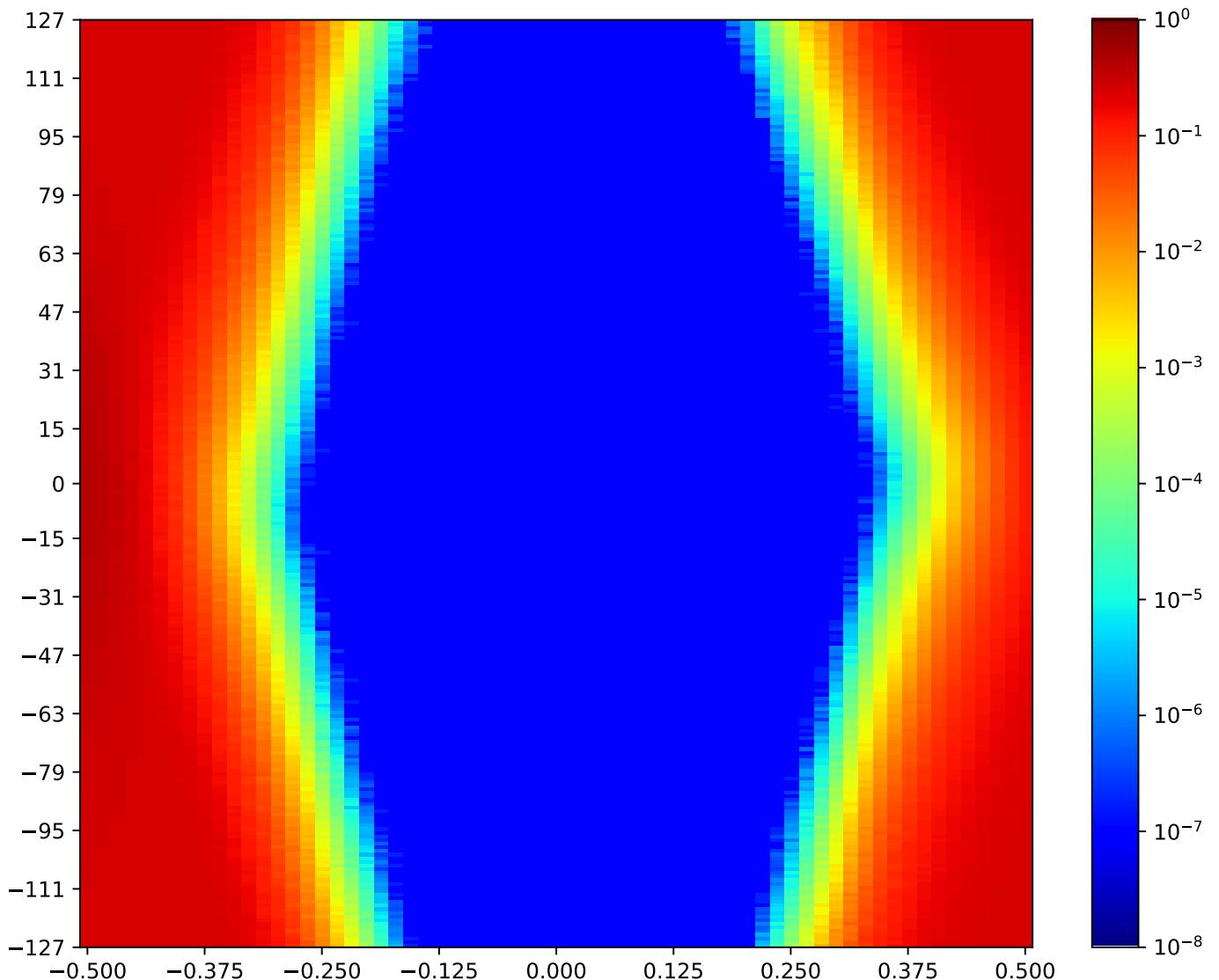


Figure 3.49: MSP\_C\_FPGA-TX4-08-RX6-08-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.10 MSP\_C\_FPGA-TX4-09-RX6-09-MSP\_A\_FPGA

Table 3.46: MSP\_C\_FPGA-TX4-09-RX6-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:42:10		2018-Jan-23 23:42:30	
Reset RX	OA	HO		HO (%)	
true	7727	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

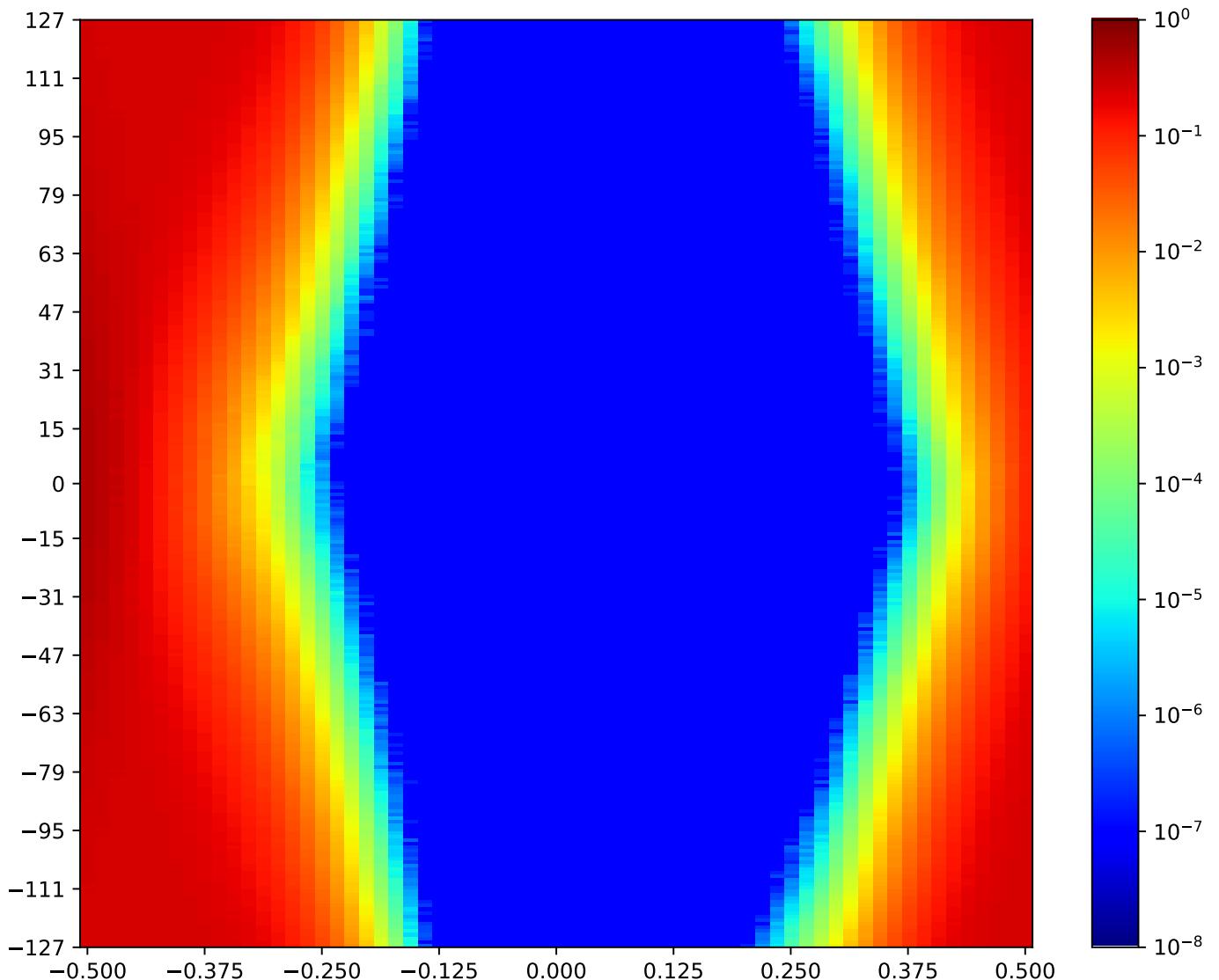


Figure 3.50: MSP\_C\_FPGA-TX4-09-RX6-09-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.11 MSP\_C\_FPGA-TX4-10-RX6-10-MSP\_A\_FPGA

Table 3.47: MSP\_C\_FPGA-TX4-10-RX6-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:43:11		2018-Jan-23 23:43:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8491	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

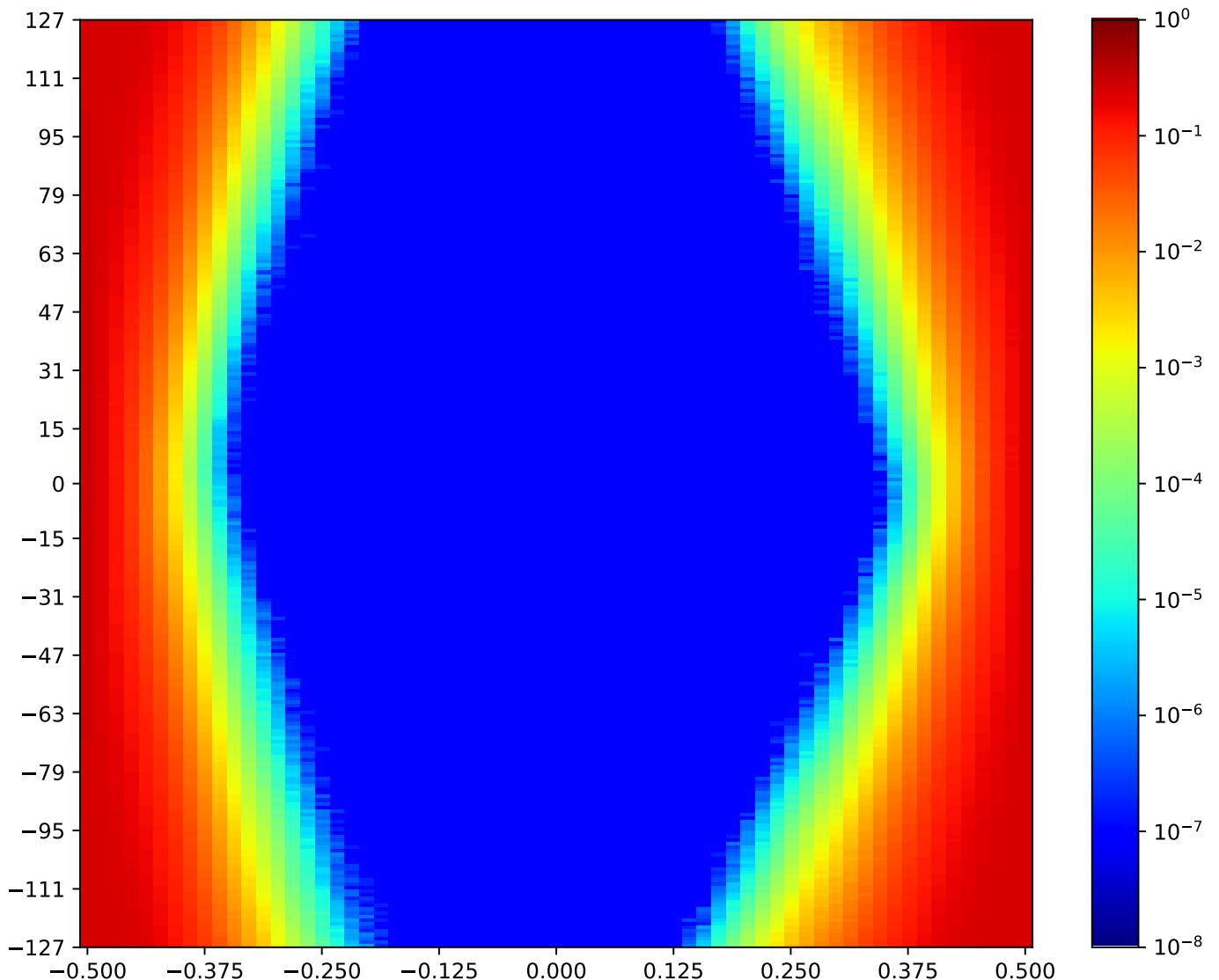


Figure 3.51: MSP\_C\_FPGA-TX4-10-RX6-10-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.4.12 MSP\_C\_FPGA-TX4-11-RX6-11-MSP\_A\_FPGA

Table 3.48: MSP\_C\_FPGA-TX4-11-RX6-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:42:50		2018-Jan-23 23:43:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7853	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

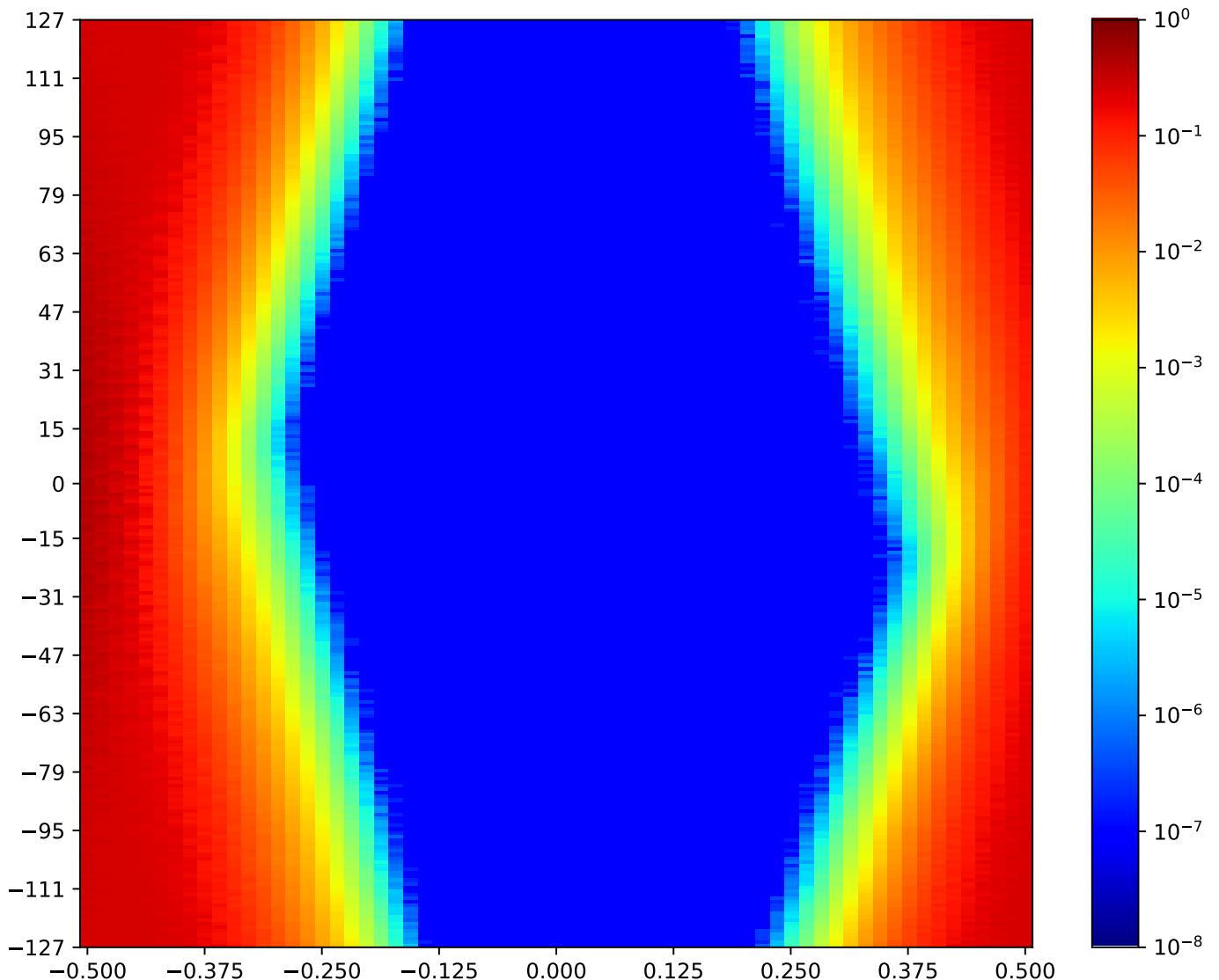


Figure 3.52: MSP\_C\_FPGA-TX4-11-RX6-11-MSP\_A\_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.5 Partial TRP TX5 MSP\_A RX5 Minipod Loopback

A cross-reference to Figure 3.53. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.62.

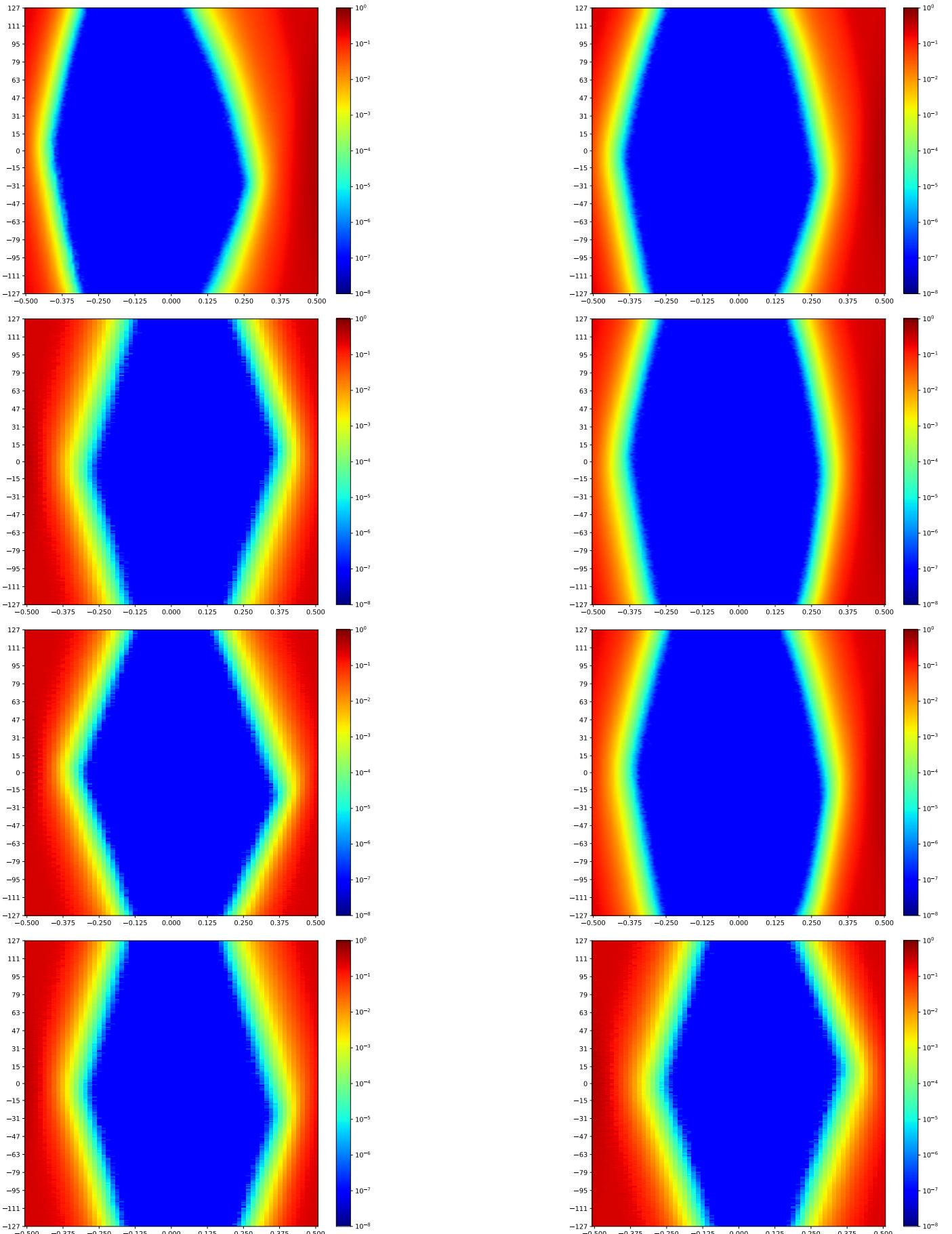


Figure 3.53: Partial TRP TX5 MSP\_A RX5 Minipod Loopback

### 3.5.1 TRP\_FPGA-TX5-00-RX5-00-MSP\_A\_FPGA

Table 3.49: TRP\_FPGA-TX5-00-RX5-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:46:35		2018-Jan-23 23:47:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16281	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

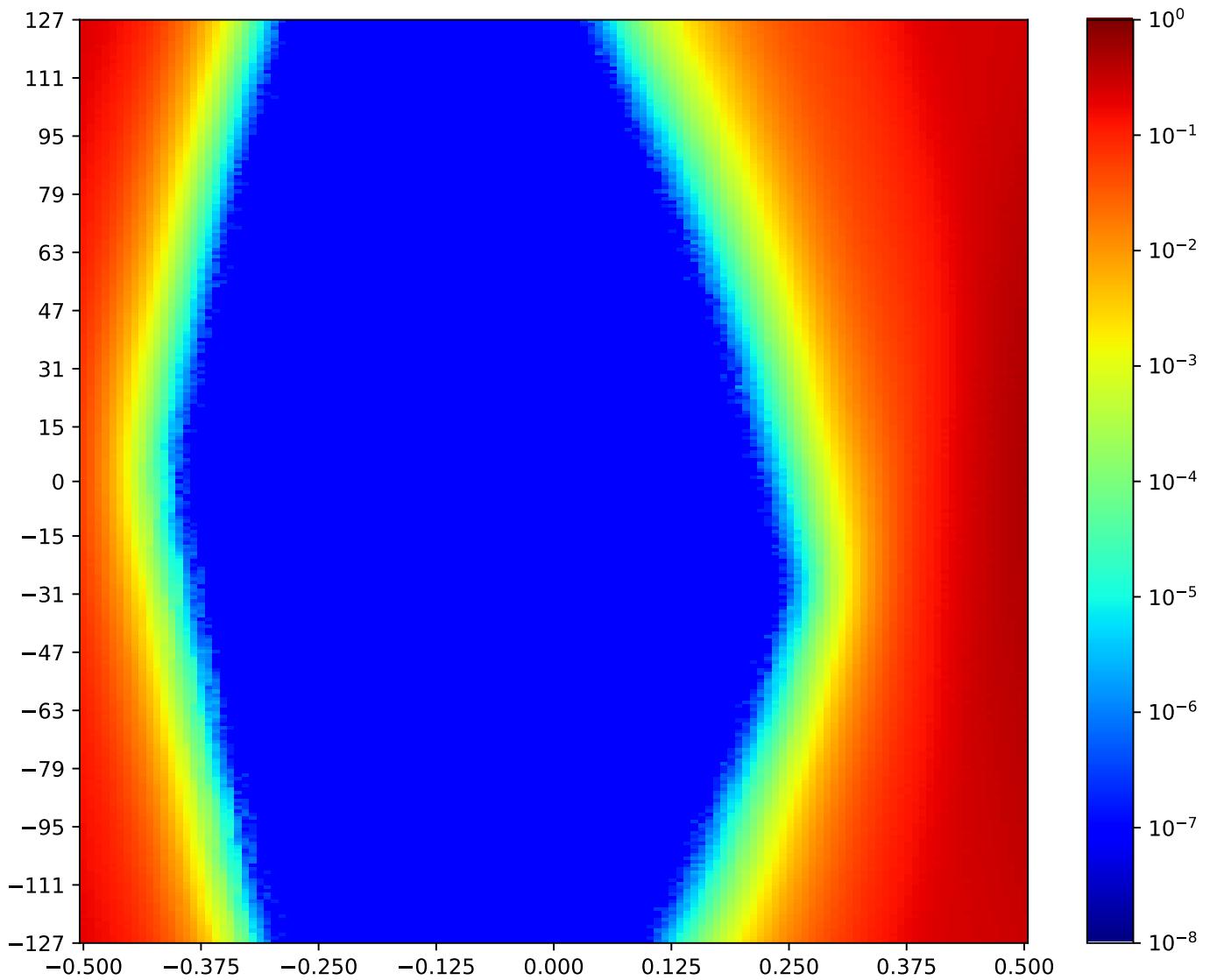


Figure 3.54: TRP\_FPGA-TX5-00-RX5-00-MSP\_A\_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.5.2 TRP\_FPGA-TX5-01-RX5-01-MSP\_A\_FPGA

Table 3.50: TRP\_FPGA-TX5-01-RX5-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:45:13		2018-Jan-23 23:45:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16378	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

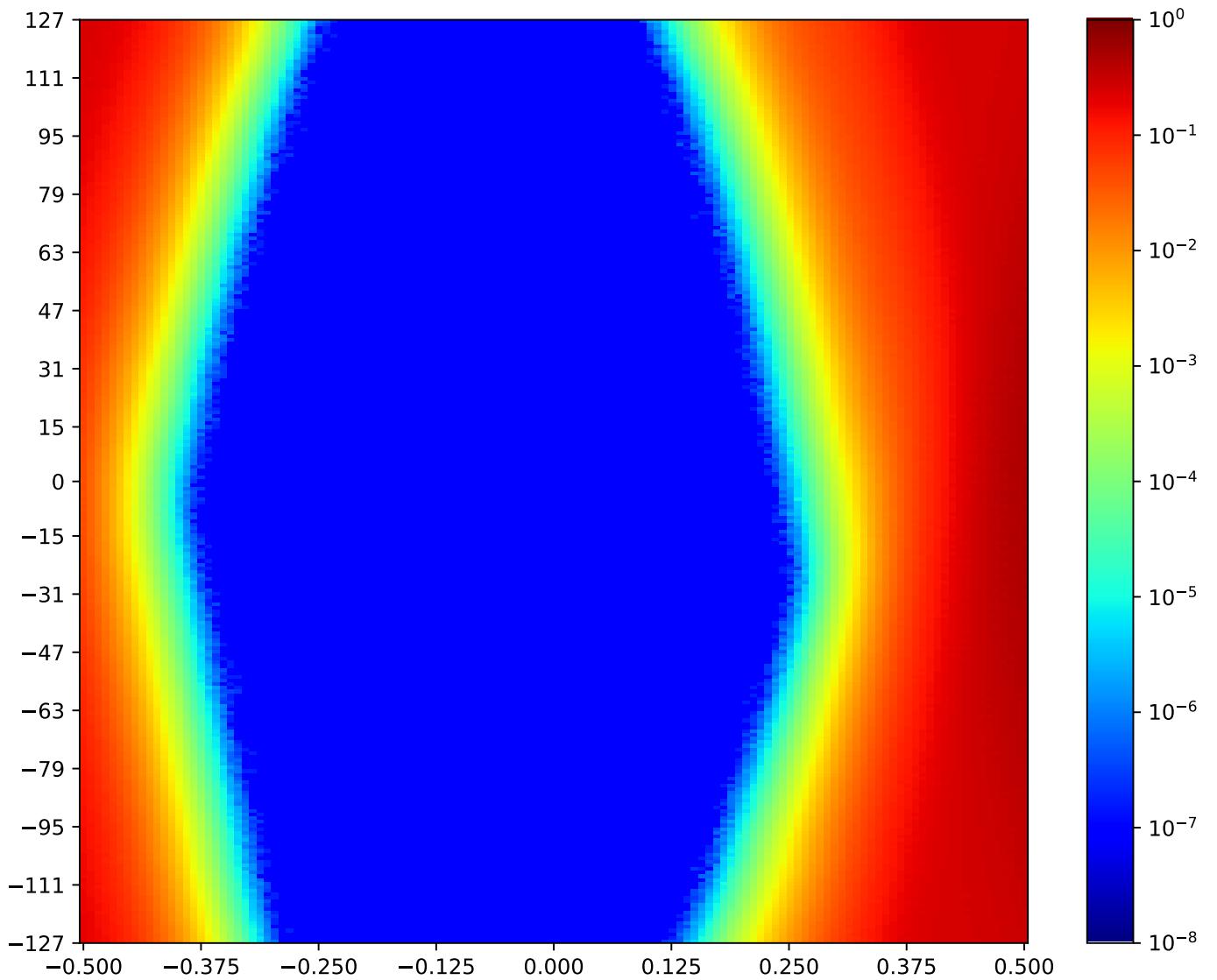


Figure 3.55: TRP\_FPGA-TX5-01-RX5-01-MSP\_A\_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.5.3 TRP\_FPGA-TX5-02-RX5-02-MSP\_A\_FPGA

Table 3.51: TRP\_FPGA-TX5-02-RX5-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:47:36		2018-Jan-23 23:47:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7243	38	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

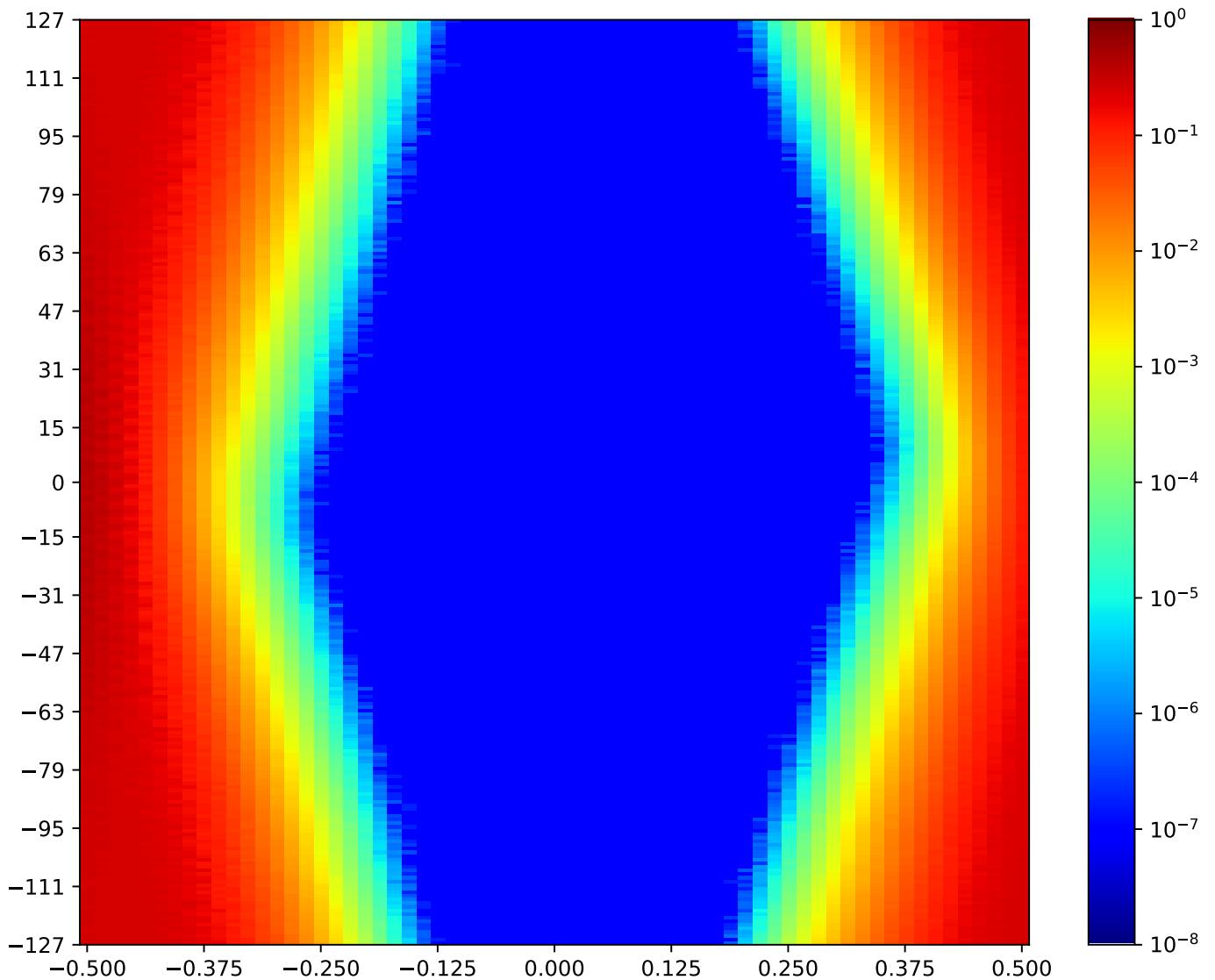


Figure 3.56: TRP\_FPGA-TX5-02-RX5-02-MSP\_A\_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.5.4 TRP\_FPGA-TX5-03-RX5-03-MSP\_A\_FPGA

Table 3.52: TRP\_FPGA-TX5-03-RX5-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:45:54		2018-Jan-23 23:46:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17293	79	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

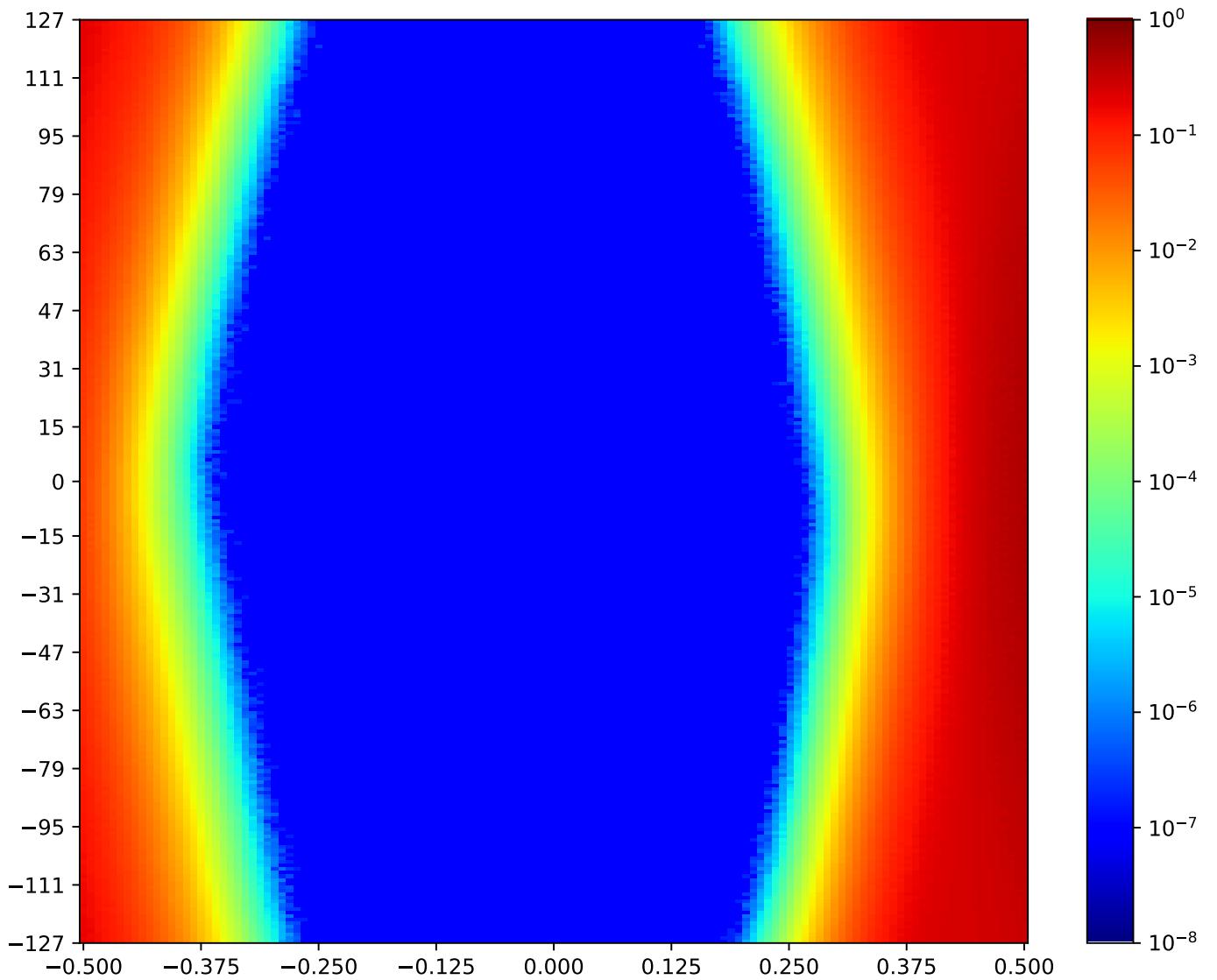


Figure 3.57: TRP\_FPGA-TX5-03-RX5-03-MSP\_A\_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.5.5 TRP\_FPGA-TX5-04-RX5-04-MSP\_A\_FPGA

Table 3.53: TRP\_FPGA-TX5-04-RX5-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:48:17		2018-Jan-23 23:48:38	
Reset RX	OA	HO		HO (%)	
true	7196	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

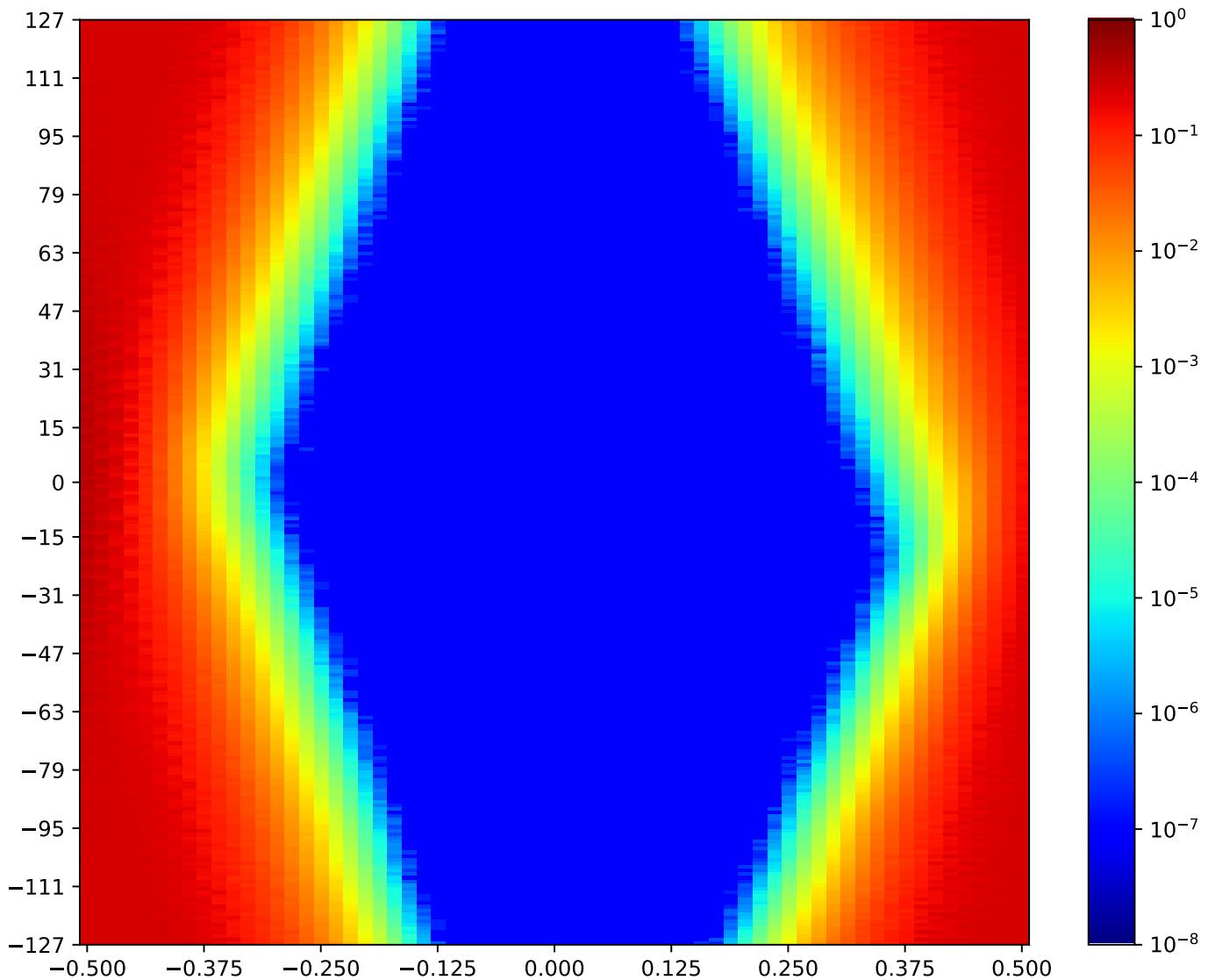


Figure 3.58: TRP\_FPGA-TX5-04-RX5-04-MSP\_A\_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.5.6 TRP\_FPGA-TX5-05-RX5-05-MSP\_A\_FPGA

Table 3.54: TRP\_FPGA-TX5-05-RX5-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:44:33		2018-Jan-23 23:45:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16667	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

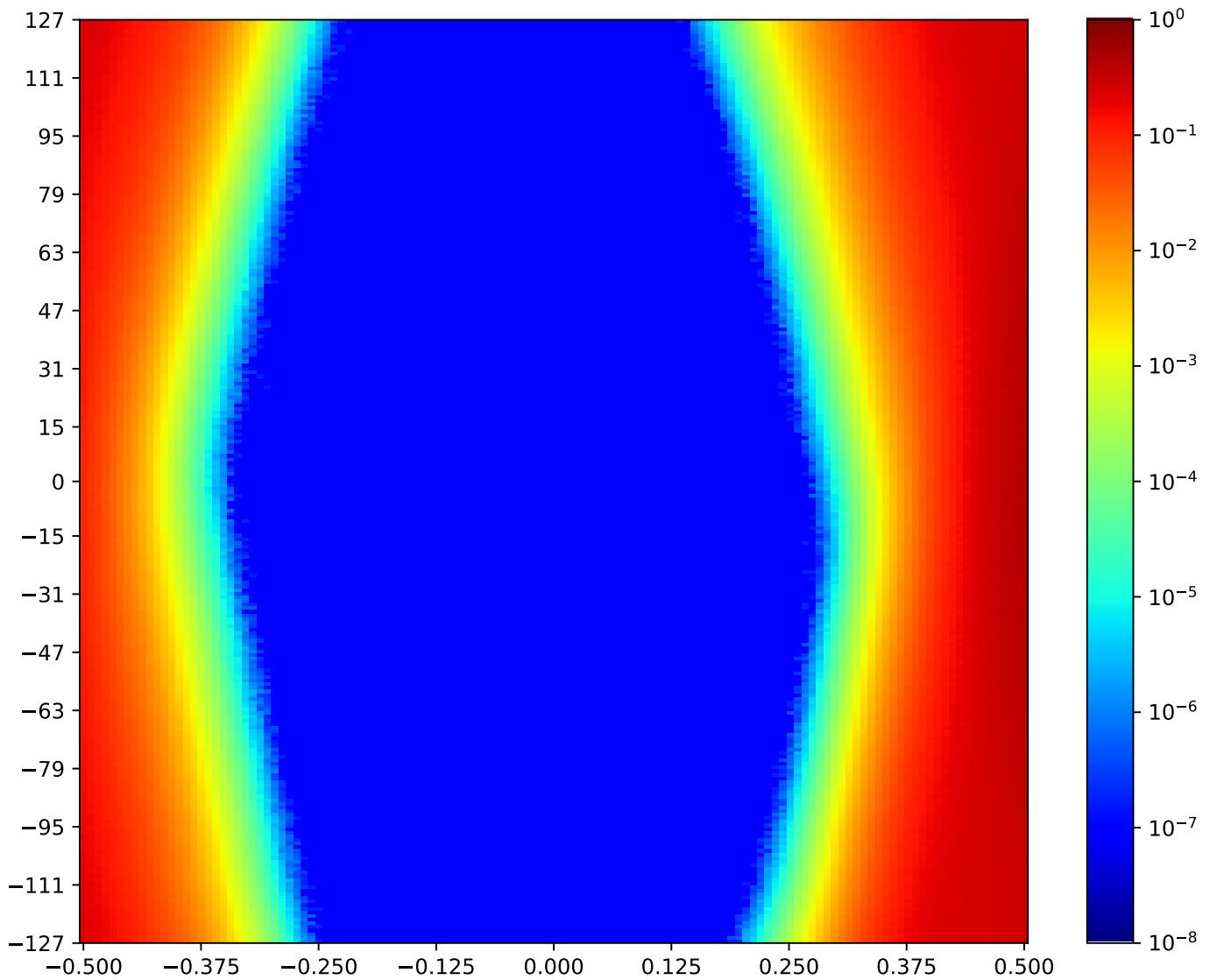


Figure 3.59: TRP\_FPGA-TX5-05-RX5-05-MSP\_A\_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.5.7 TRP\_FPGA-TX5-06-RX5-06-MSP\_A\_FPGA

Table 3.55: TRP\_FPGA-TX5-06-RX5-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:47:16		2018-Jan-23 23:47:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7449	35	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

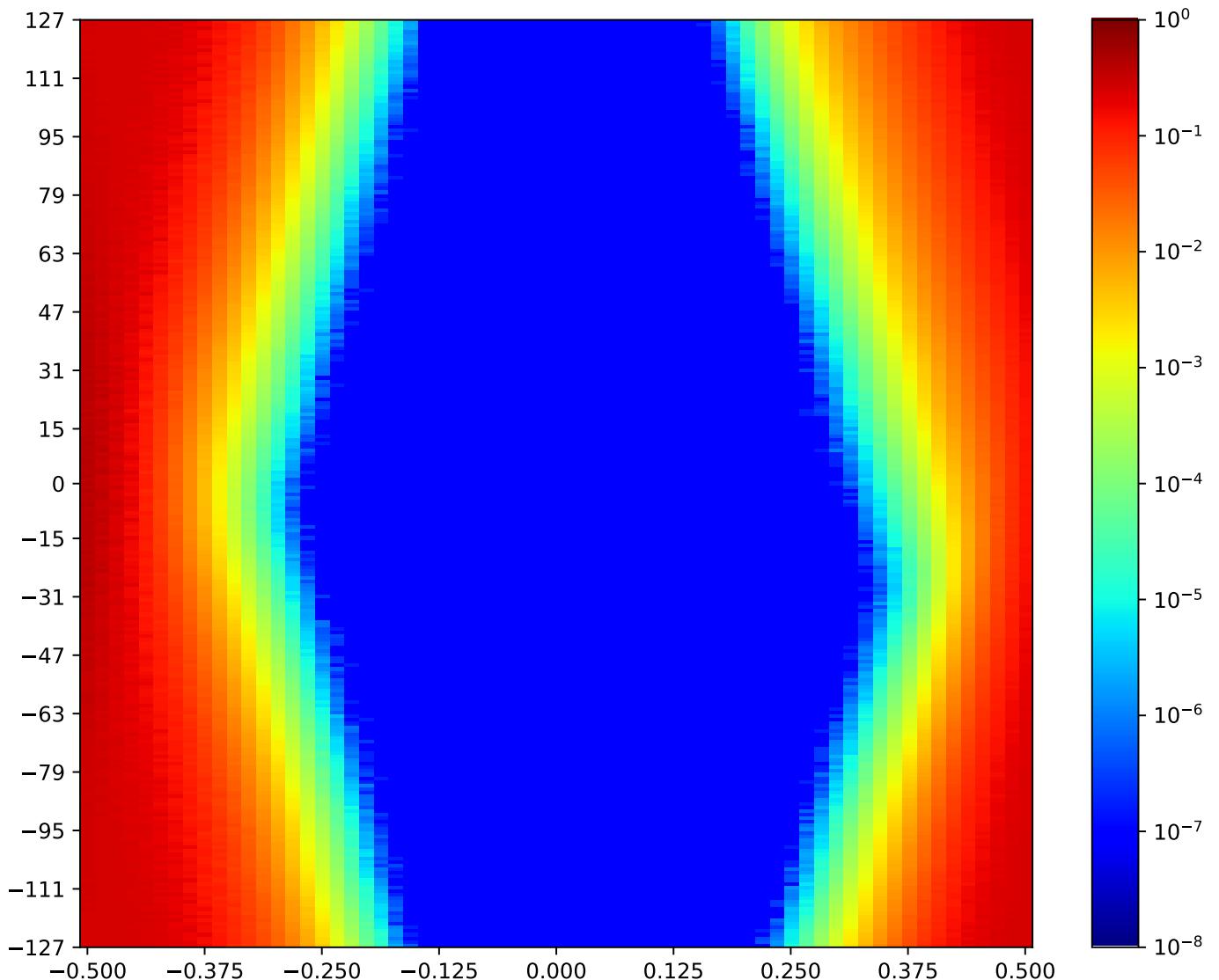


Figure 3.60: TRP\_FPGA-TX5-06-RX5-06-MSP\_A\_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.5.8 TRP\_FPGA-TX5-07-RX5-07-MSP\_A\_FPGA

Table 3.56: TRP\_FPGA-TX5-07-RX5-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:47:57		2018-Jan-23 23:48:17	
Reset RX	OA	HO		HO (%)	
true	6612	35		53.85%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

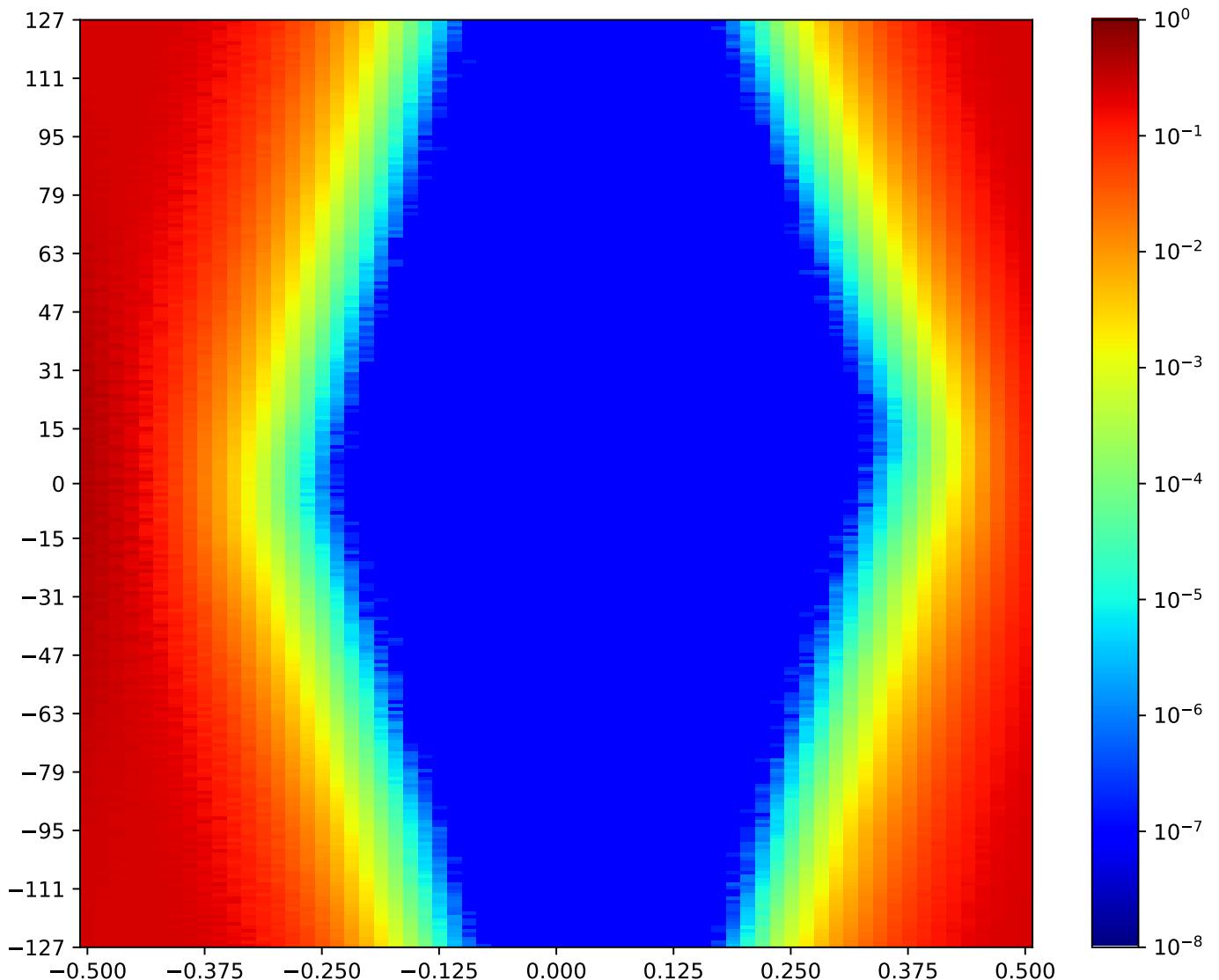


Figure 3.61: TRP\_FPGA-TX5-07-RX5-07-MSP\_A\_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.6 TRP J1 QSFP Loopback

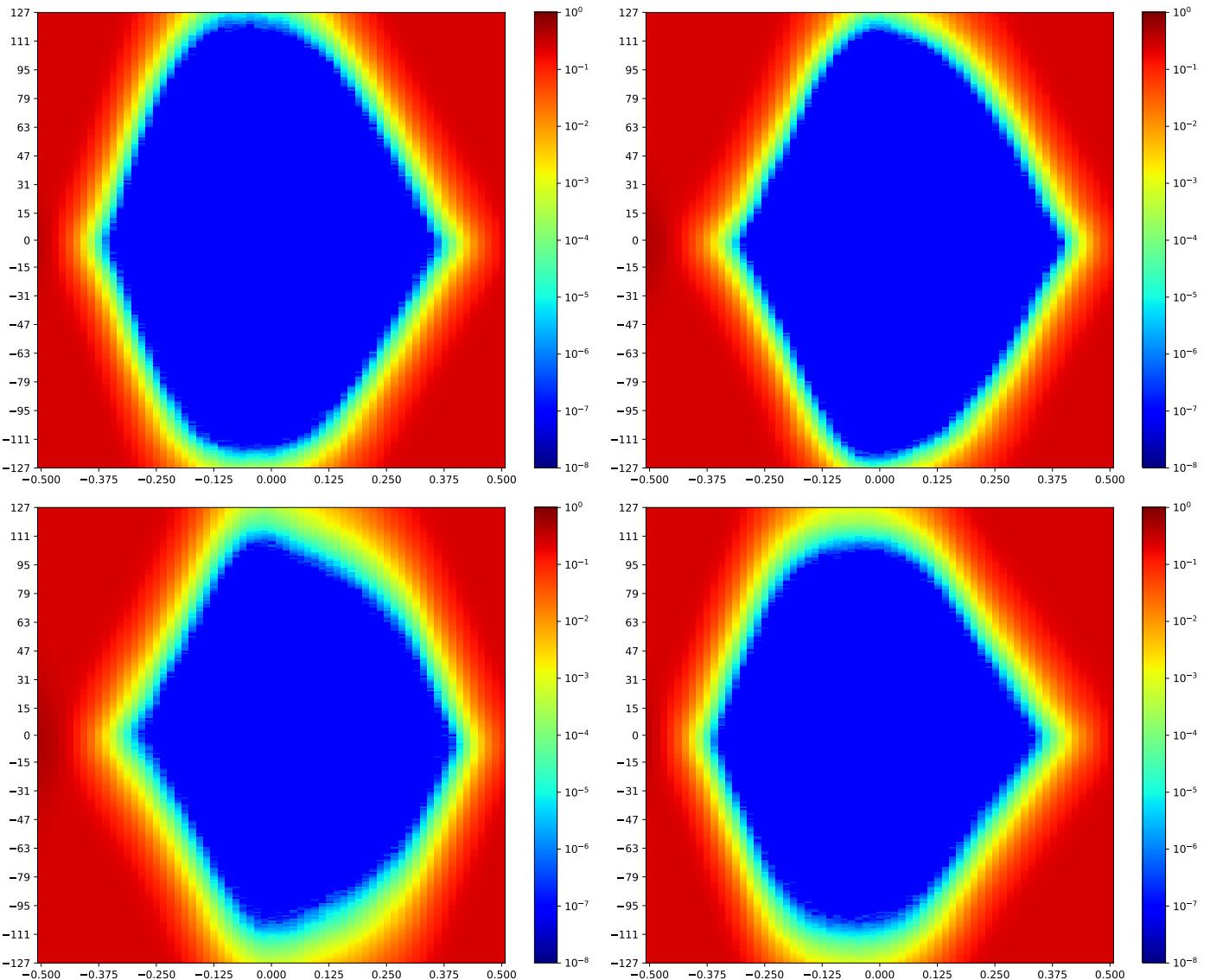


Figure 3.62: TRP J1 QSFP Loopback

A cross-reference to Figure 3.62. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.67.

### 3.6.1 TRP\_FPGA-J1-00–J1-00-TRP\_FPGA

Table 3.57: TRP\_FPGA-J1-00–J1-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:48:38		2018-Jan-23 23:48:58	
Reset RX	OA	HO		HO (%)	
true	6960	45		69.23%	228   89.41%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

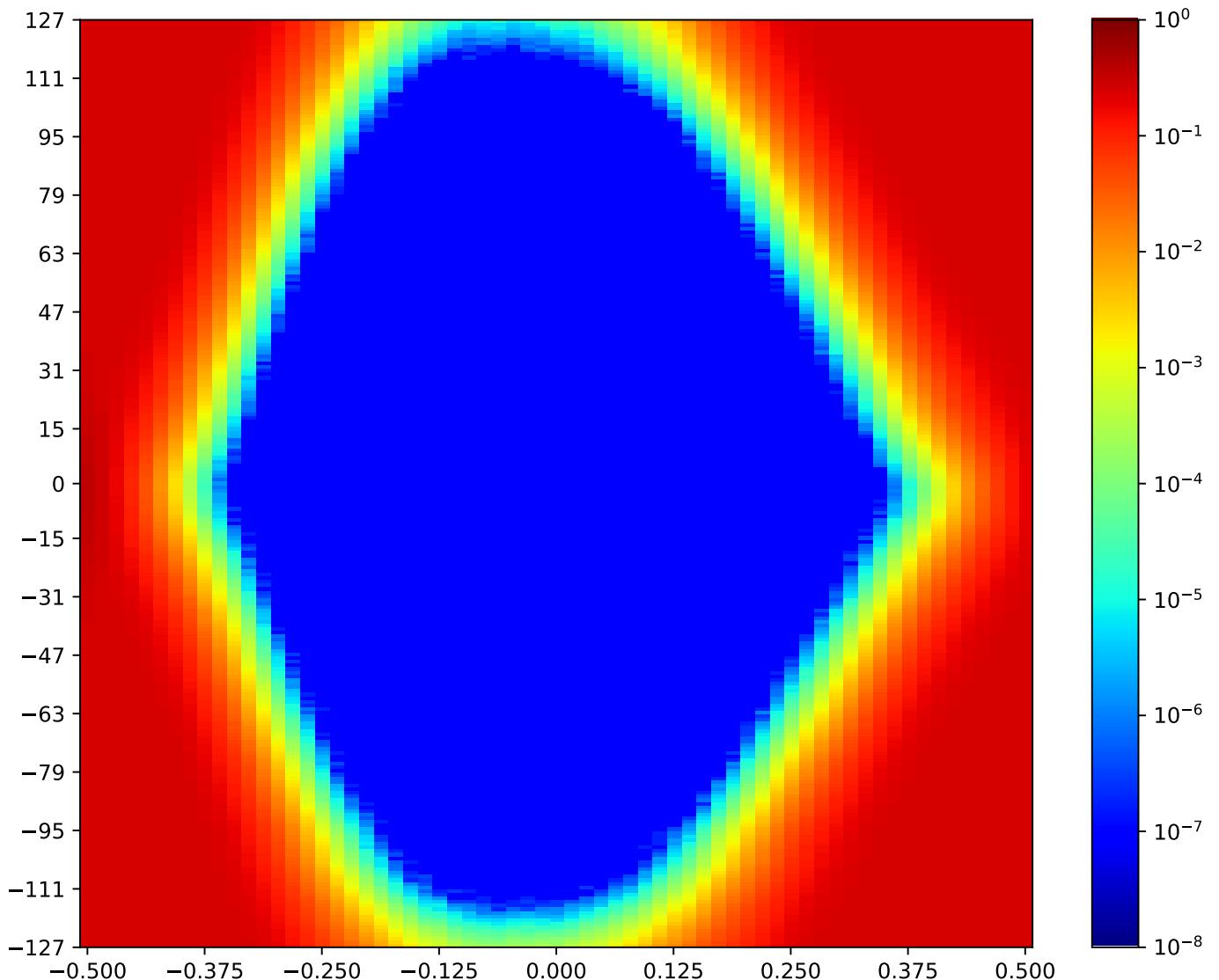


Figure 3.63: TRP\_FPGA-J1-00–J1-00-TRP\_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.6.2 TRP\_FPGA-J1-01–J1-01-TRP\_FPGA

Table 3.58: TRP\_FPGA-J1-01–J1-01-TRP\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:48:58			2018-Jan-23 23:49:19	
Reset RX	OA	HO	HO (%)		VO	VO (%)
true	6437	44	67.69%		237	92.55%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

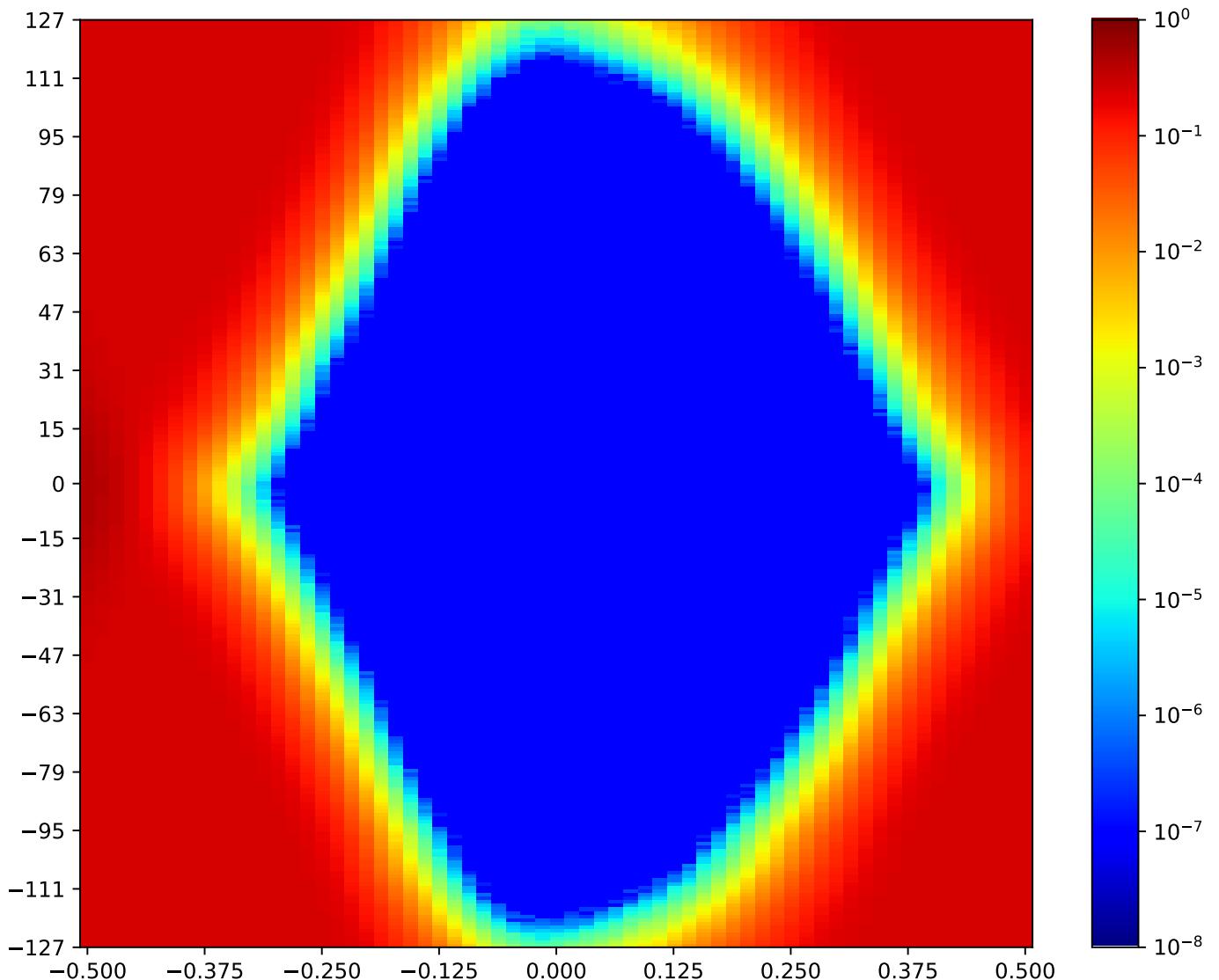


Figure 3.64: TRP\_FPGA-J1-01–J1-01-TRP\_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.6.3 TRP\_FPGA-J1-02–J1-02-TRP\_FPGA

Table 3.59: TRP\_FPGA-J1-02–J1-02-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:49:19		2018-Jan-23 23:49:39	
Reset RX	OA	HO		HO (%)	
true	5563	41		63.08%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

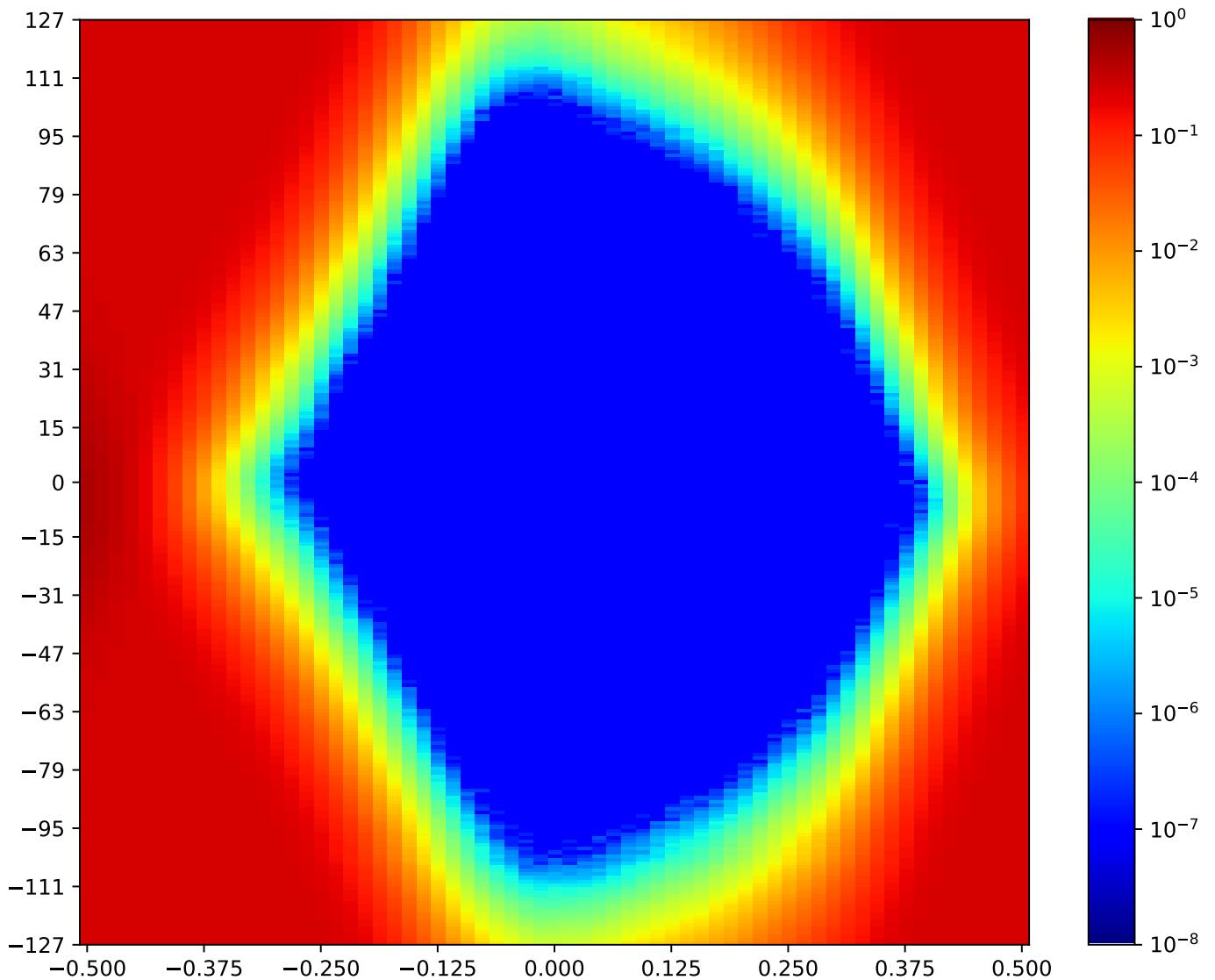


Figure 3.65: TRP\_FPGA-J1-02–J1-02-TRP\_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.6.4 TRP\_FPGA-J1-03–J1-03-TRP\_FPGA

Table 3.60: TRP\_FPGA-J1-03–J1-03-TRP\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:49:40			2018-Jan-23 23:50:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	5864	42	64.62%	201	78.43%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

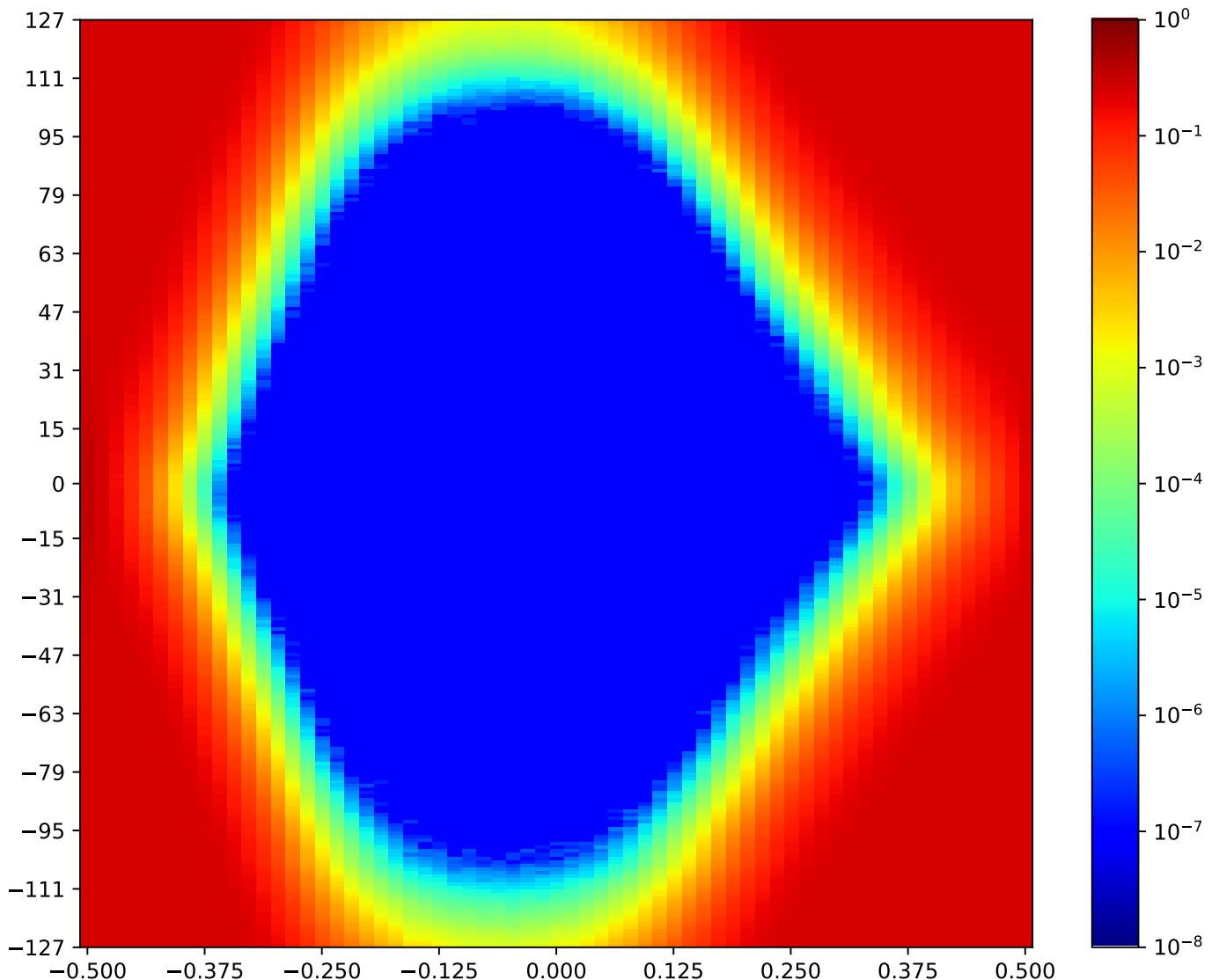


Figure 3.66: TRP\_FPGA-J1-03–J1-03-TRP\_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.7 TRP J3 SFP Loopback

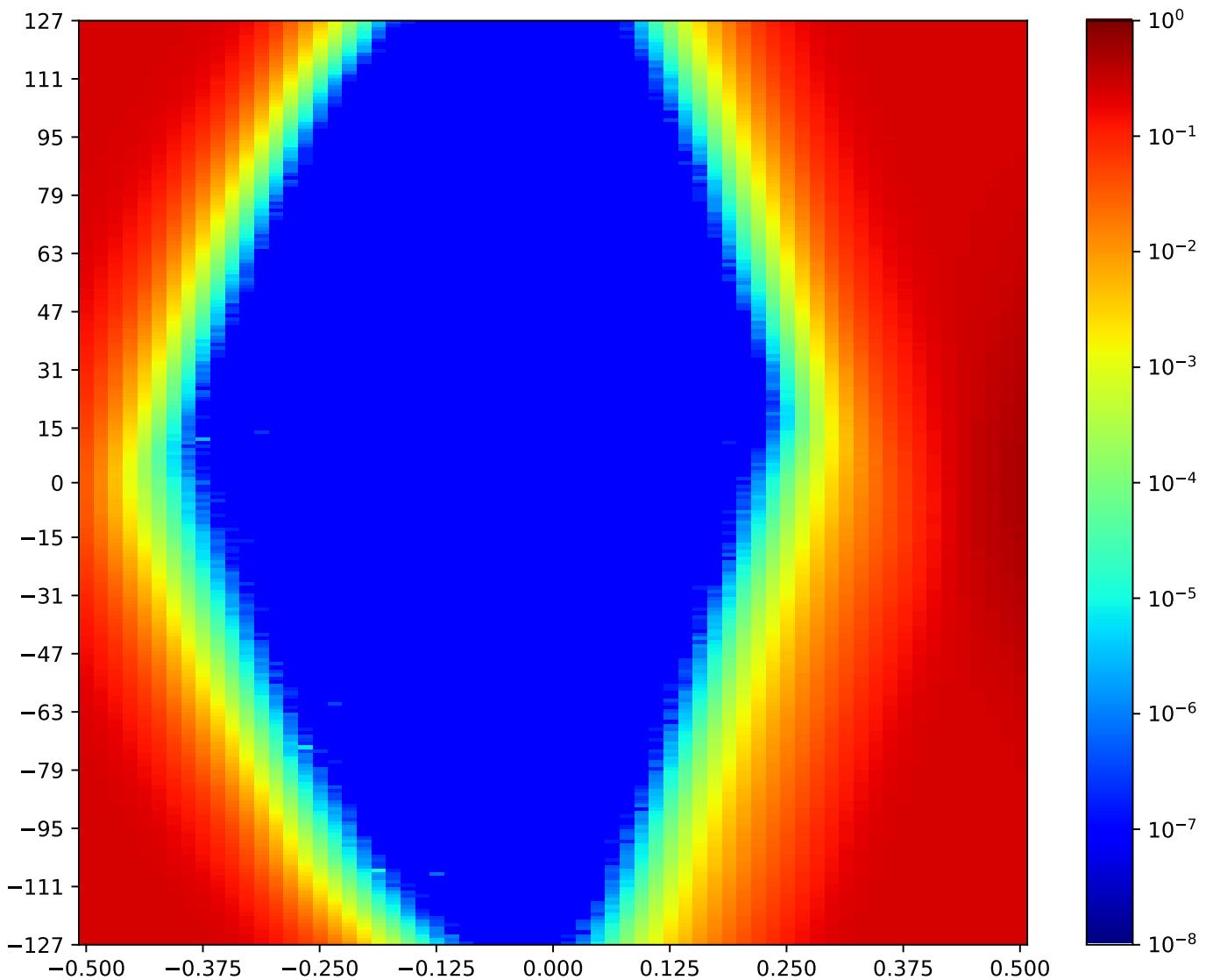


Figure 3.67: TRP J3 SFP Loopback

A cross-reference to Figure 3.67. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.69.

### 3.7.1 TRP\_FPGA-J3-00–J3-00-TRP\_FPGA

Table 3.61: TRP\_FPGA-J3-00–J3-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:50:00		2018-Jan-23 23:50:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6766	36	55.38%	255	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

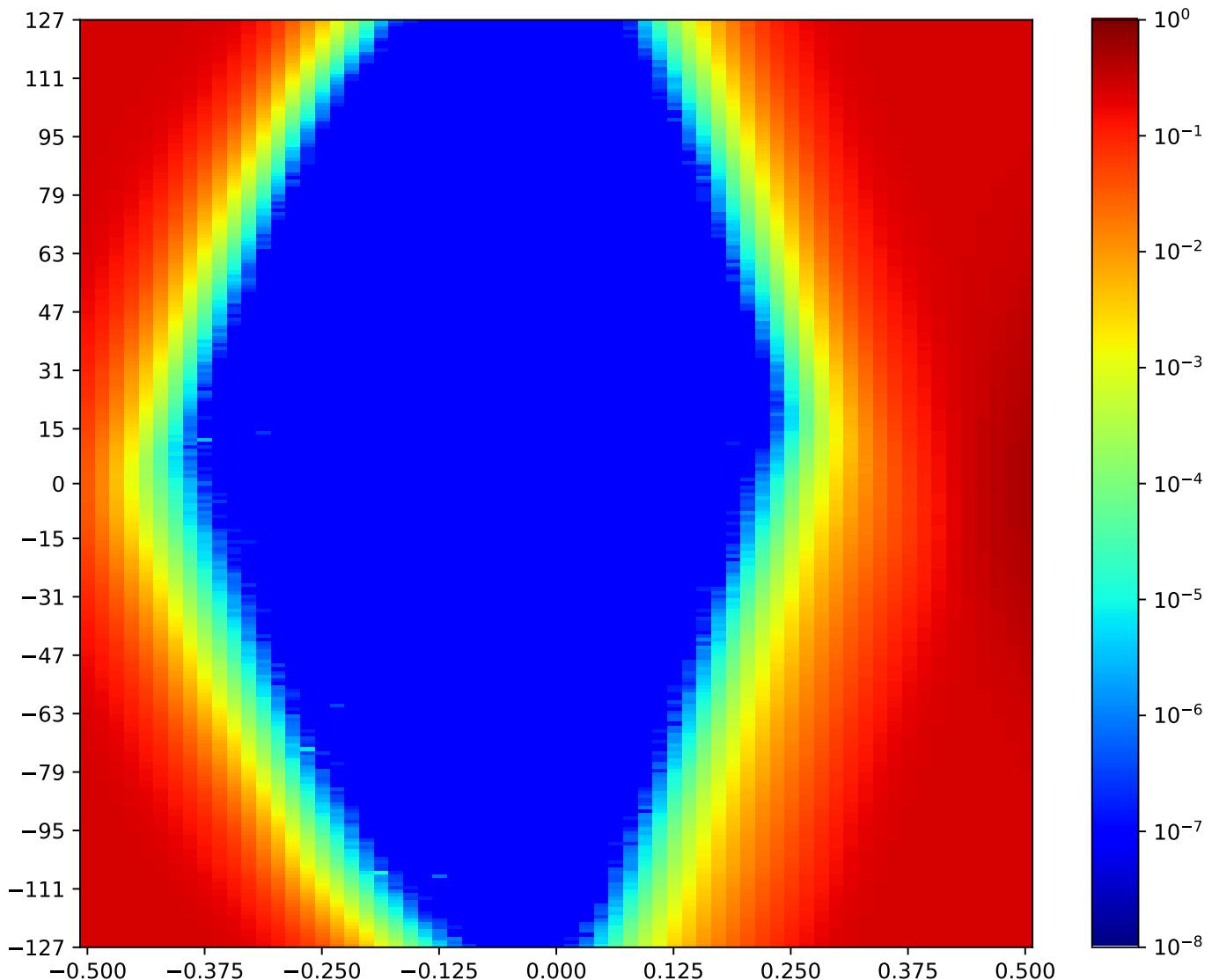


Figure 3.68: TRP\_FPGA-J3-00–J3-00-TRP\_FPGA

Call back to summary Figure 3.67. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### **3.8 MSP\_A TRP On board links**

A cross-reference to Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.98.

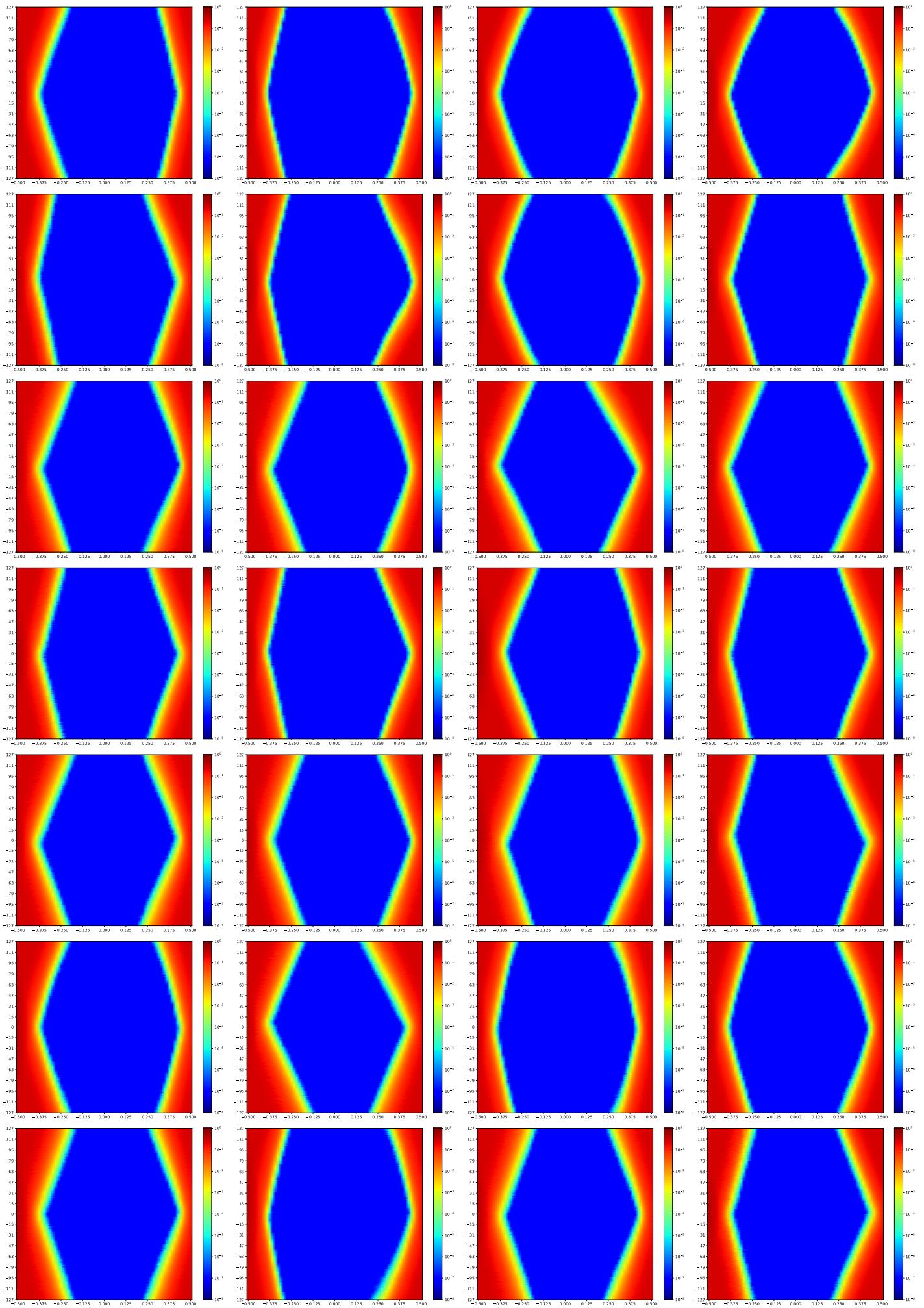


Figure 3.69: MSP\_A TRP On board links

### 3.8.1 MSP\_A\_FPGA-IC39-00-IC4-00-TRP\_FPGA

Table 3.62: MSP\_A\_FPGA-IC39-00-IC4-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:50:21		2018-Jan-23 23:50:41	
Reset RX	OA	HO		HO (%)	
true	10247	48		73.85%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

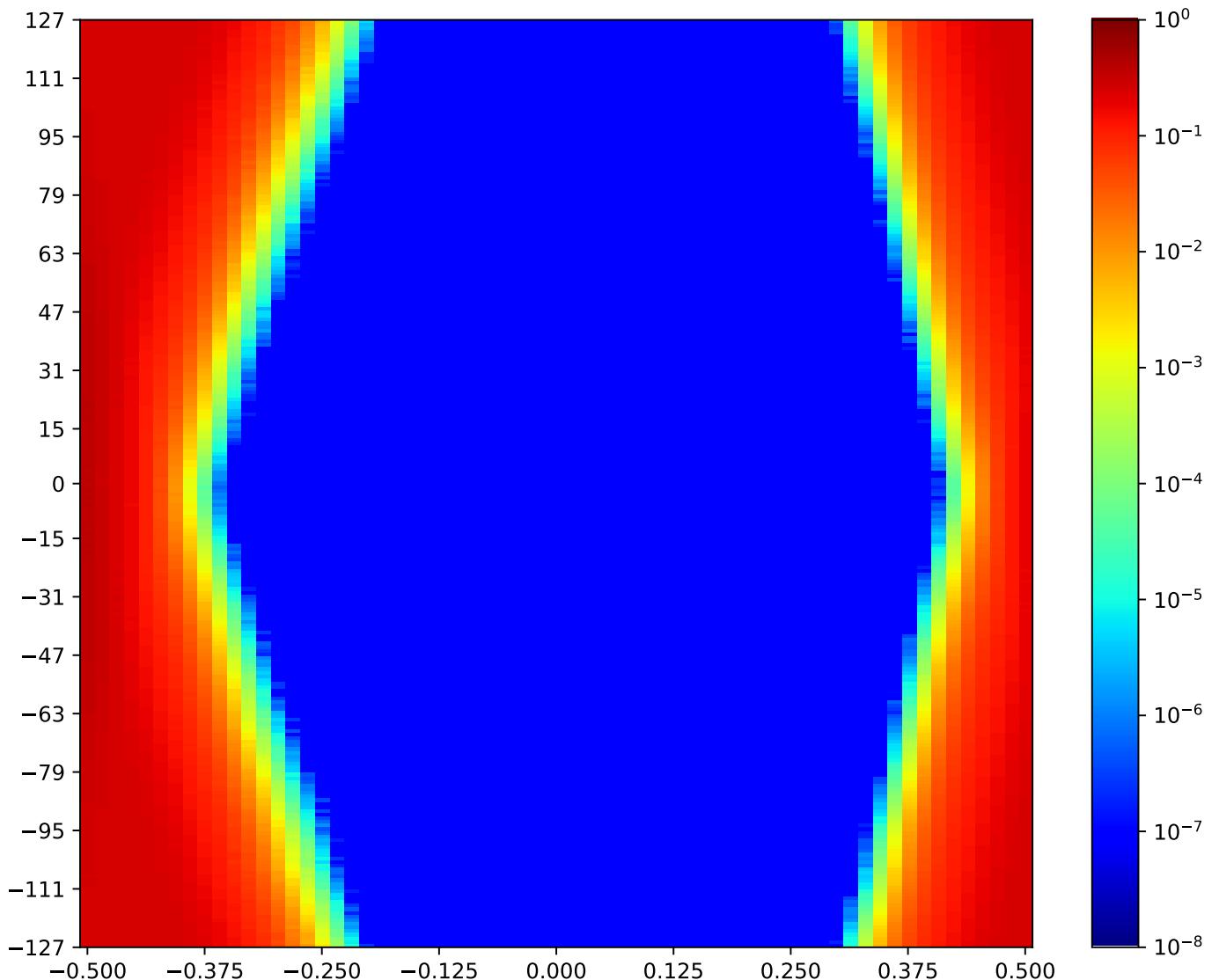


Figure 3.70: MSP\_A\_FPGA-IC39-00-IC4-00-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.2 MSP\_A\_FPGA-IC39-01-IC4-01-TRP\_FPGA

Table 3.63: MSP\_A\_FPGA-IC39-01-IC4-01-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:50:41		2018-Jan-23 23:51:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11305	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

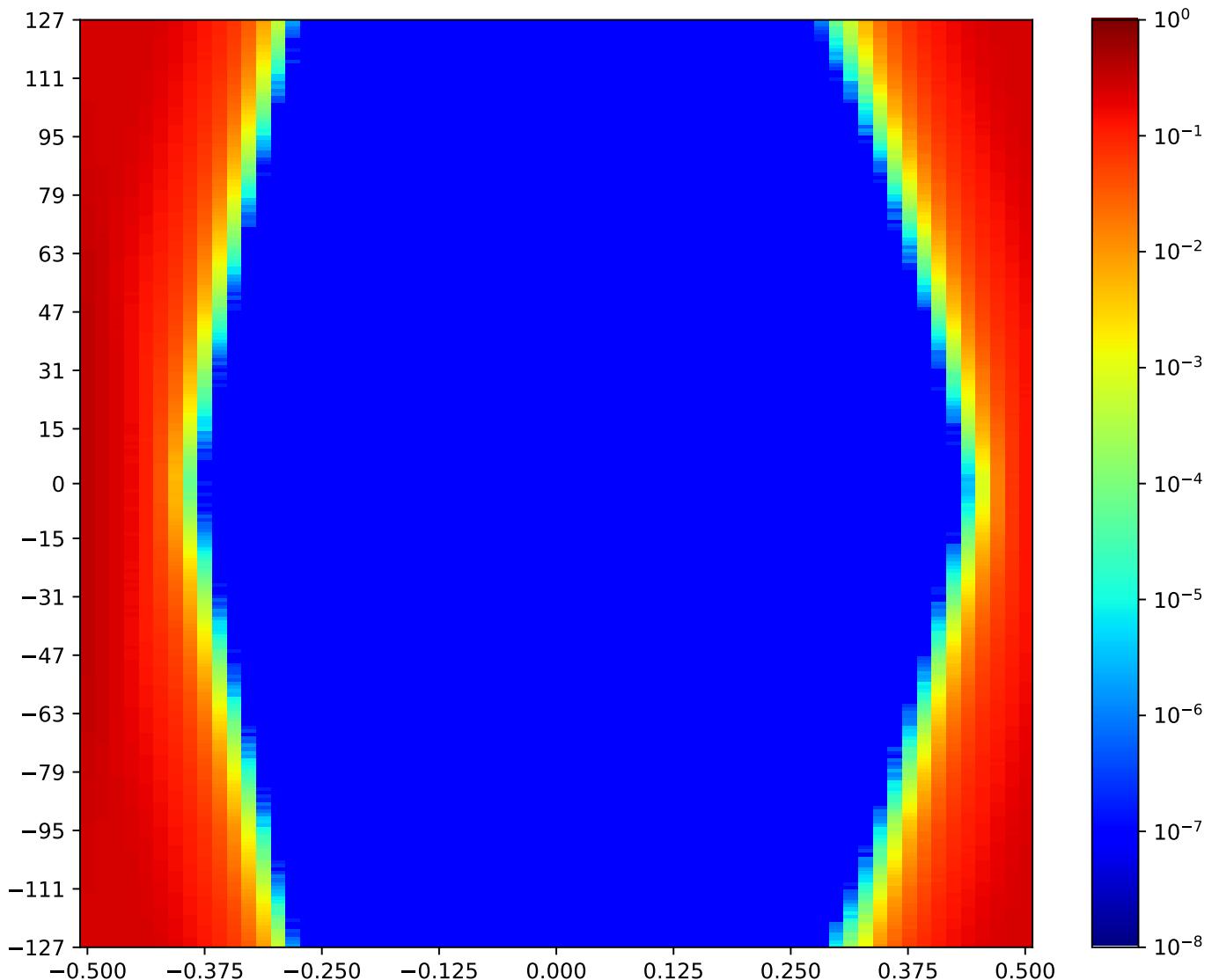


Figure 3.71: MSP\_A\_FPGA-IC39-01-IC4-01-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.3 MSP\_A\_FPGA-IC39-02-IC4-02-TRP\_FPGA

Table 3.64: MSP\_A\_FPGA-IC39-02-IC4-02-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:51:02		2018-Jan-23 23:51:22	
Reset RX	OA	HO		HO (%)	
true	10054	49		75.38%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

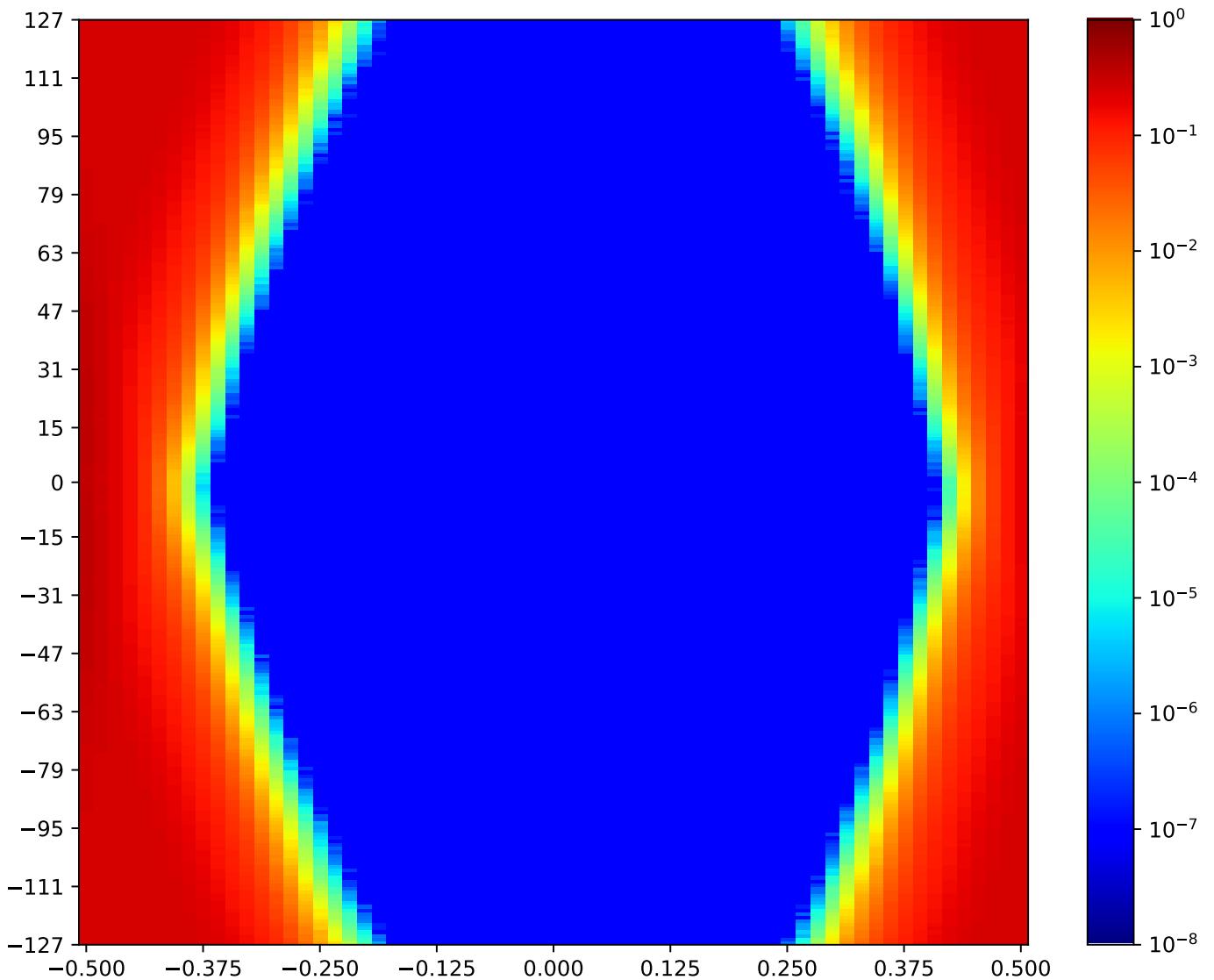


Figure 3.72: MSP\_A\_FPGA-IC39-02-IC4-02-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.4 MSP\_A\_FPGA-IC39-03-IC4-03-TRP\_FPGA

Table 3.65: MSP\_A\_FPGA-IC39-03-IC4-03-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:51:22		2018-Jan-23 23:51:43	
Reset RX	OA	HO		HO (%)	
true	9717	51		78.46%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

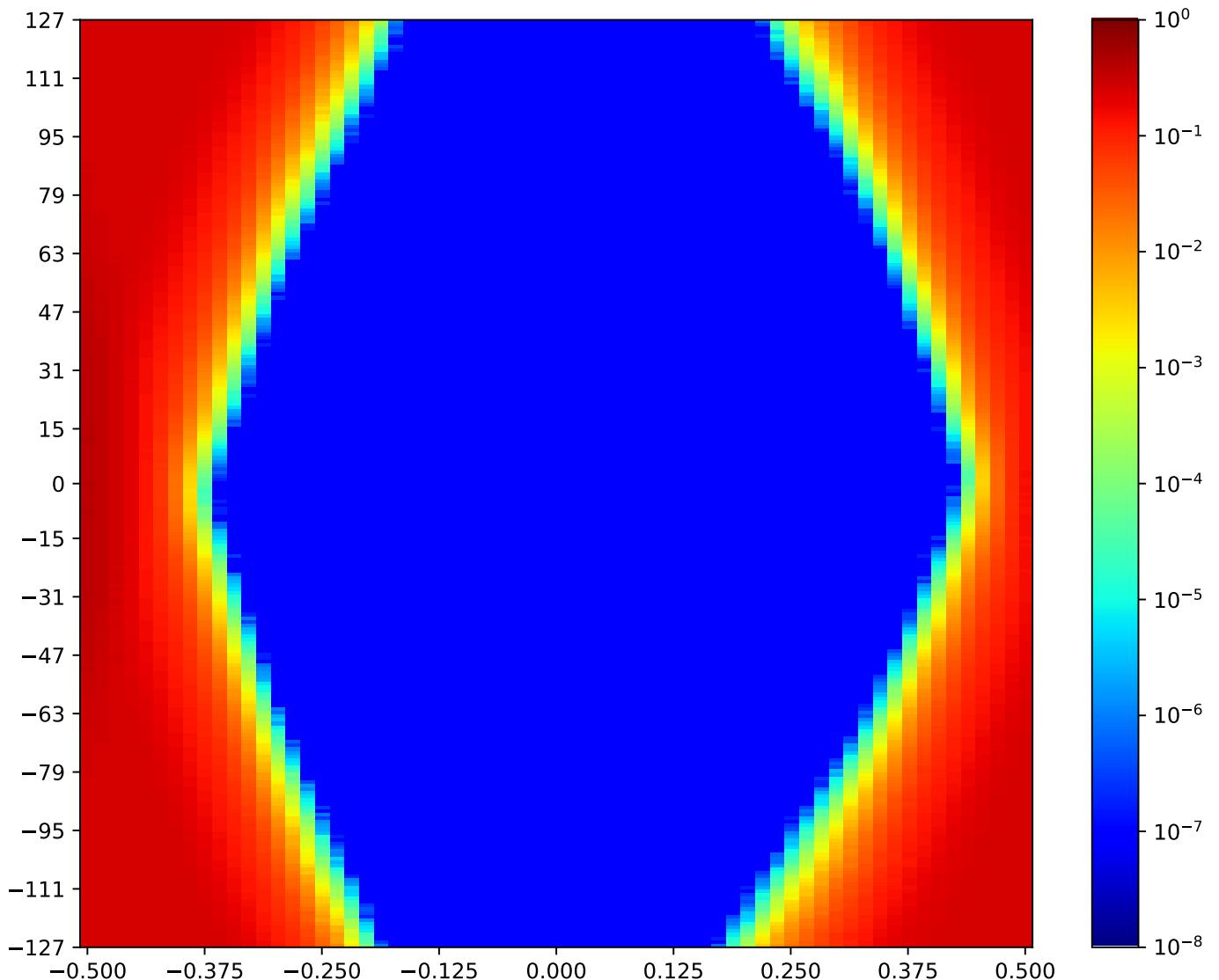


Figure 3.73: MSP\_A\_FPGA-IC39-03-IC4-03-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.5 MSP\_A\_FPGA-IC39-04-IC4-04-TRP\_FPGA

Table 3.66: MSP\_A\_FPGA-IC39-04-IC4-04-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:51:43		2018-Jan-23 23:52:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10095	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

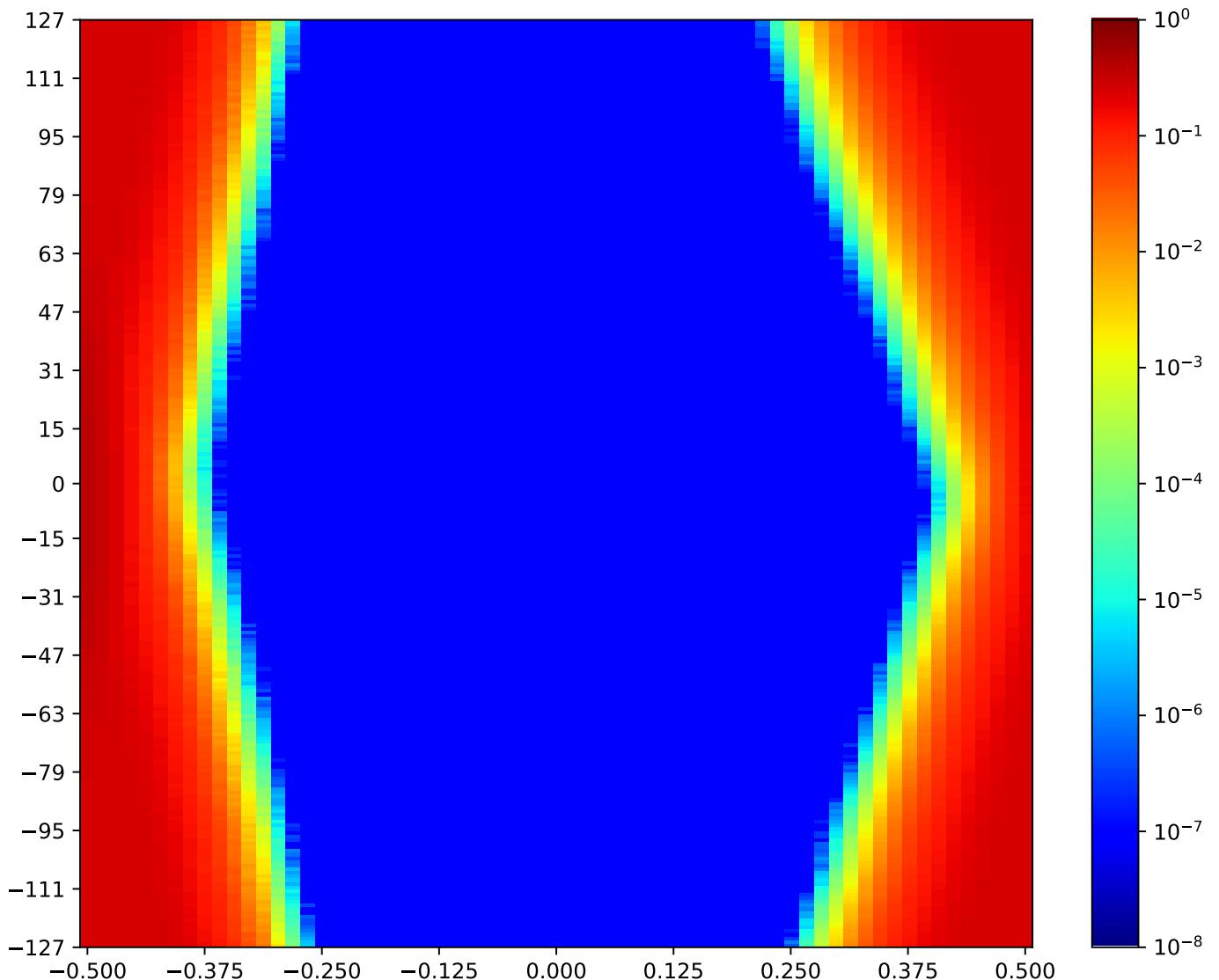


Figure 3.74: MSP\_A\_FPGA-IC39-04-IC4-04-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.6 MSP\_A\_FPGA-IC39-05-IC4-05-TRP\_FPGA

Table 3.67: MSP\_A\_FPGA-IC39-05-IC4-05-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:52:03		2018-Jan-23 23:52:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10464	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

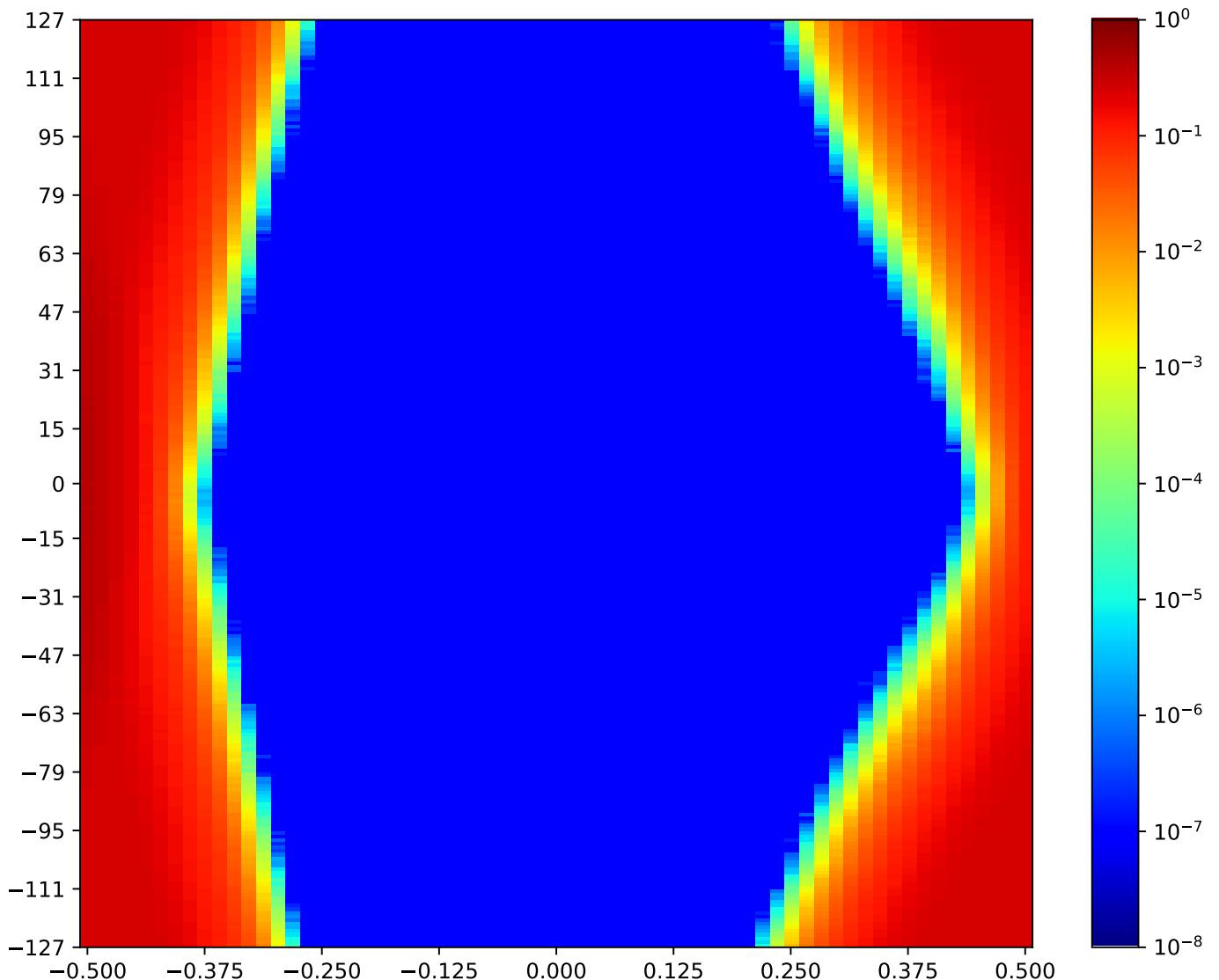


Figure 3.75: MSP\_A\_FPGA-IC39-05-IC4-05-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.7 MSP\_A\_FPGA-IC39-06-IC4-06-TRP\_FPGA

Table 3.68: MSP\_A\_FPGA-IC39-06-IC4-06-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:52:24		2018-Jan-23 23:52:45	
Reset RX	OA	HO		HO (%)	
true	9795	49		75.38%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

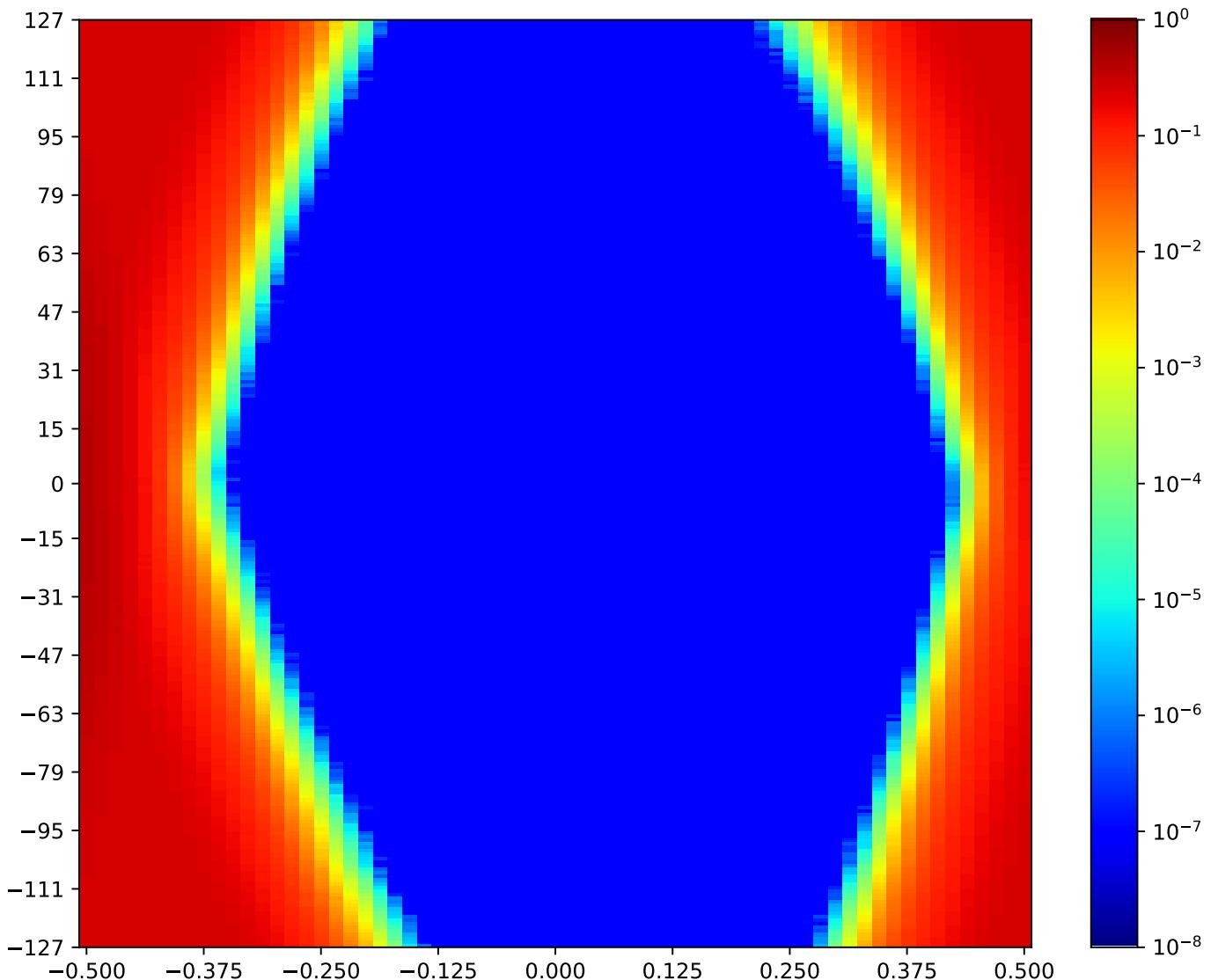


Figure 3.76: MSP\_A\_FPGA-IC39-06-IC4-06-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.8 MSP\_A\_FPGA-IC39-07-IC4-07-TRP\_FPGA

Table 3.69: MSP\_A\_FPGA-IC39-07-IC4-07-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:52:45		2018-Jan-23 23:53:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9901	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

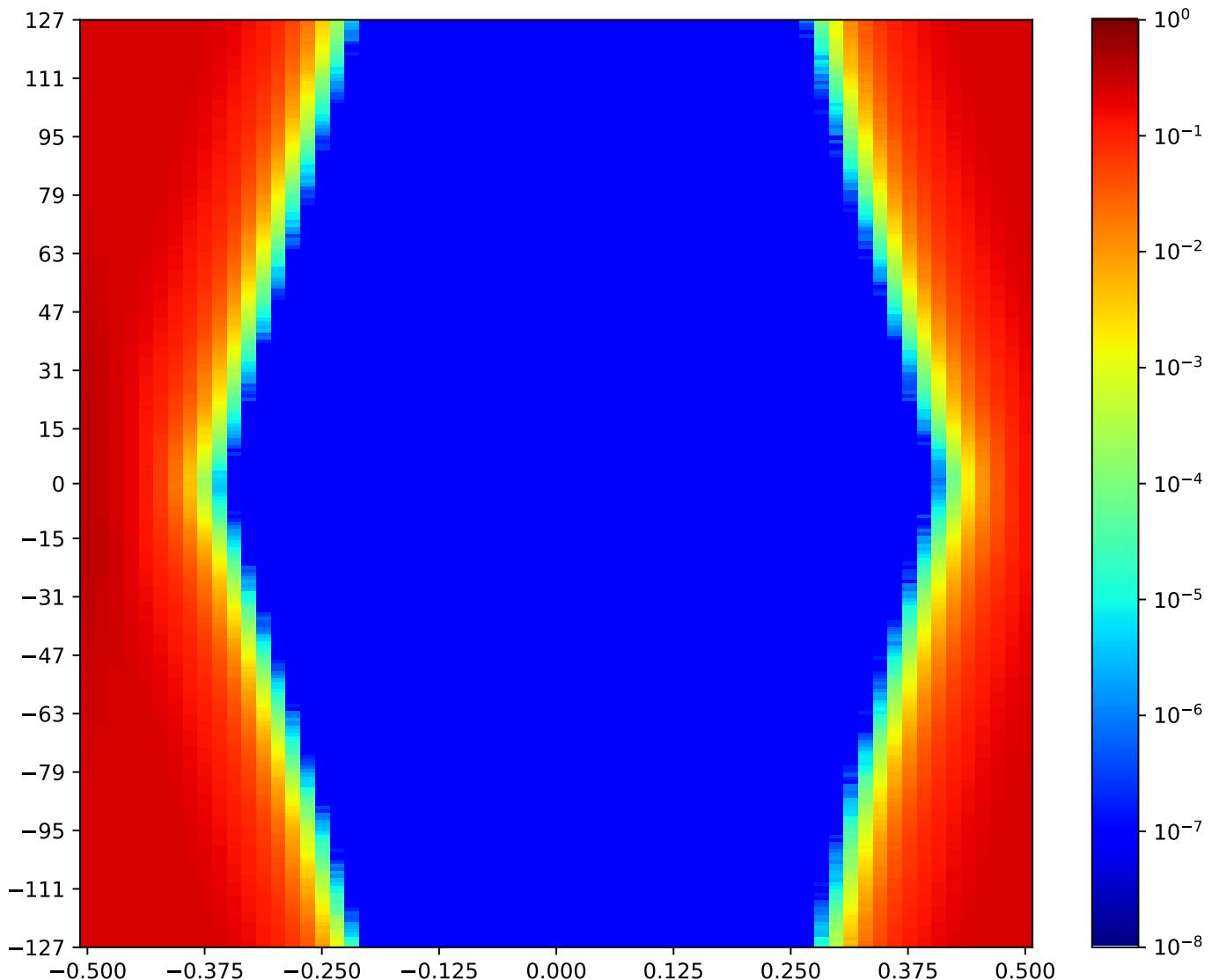


Figure 3.77: MSP\_A\_FPGA-IC39-07-IC4-07-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.9 MSP\_A\_FPGA-IC39-08-IC4-08-TRP\_FPGA

Table 3.70: MSP\_A\_FPGA-IC39-08-IC4-08-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:53:05		2018-Jan-23 23:53:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9364	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

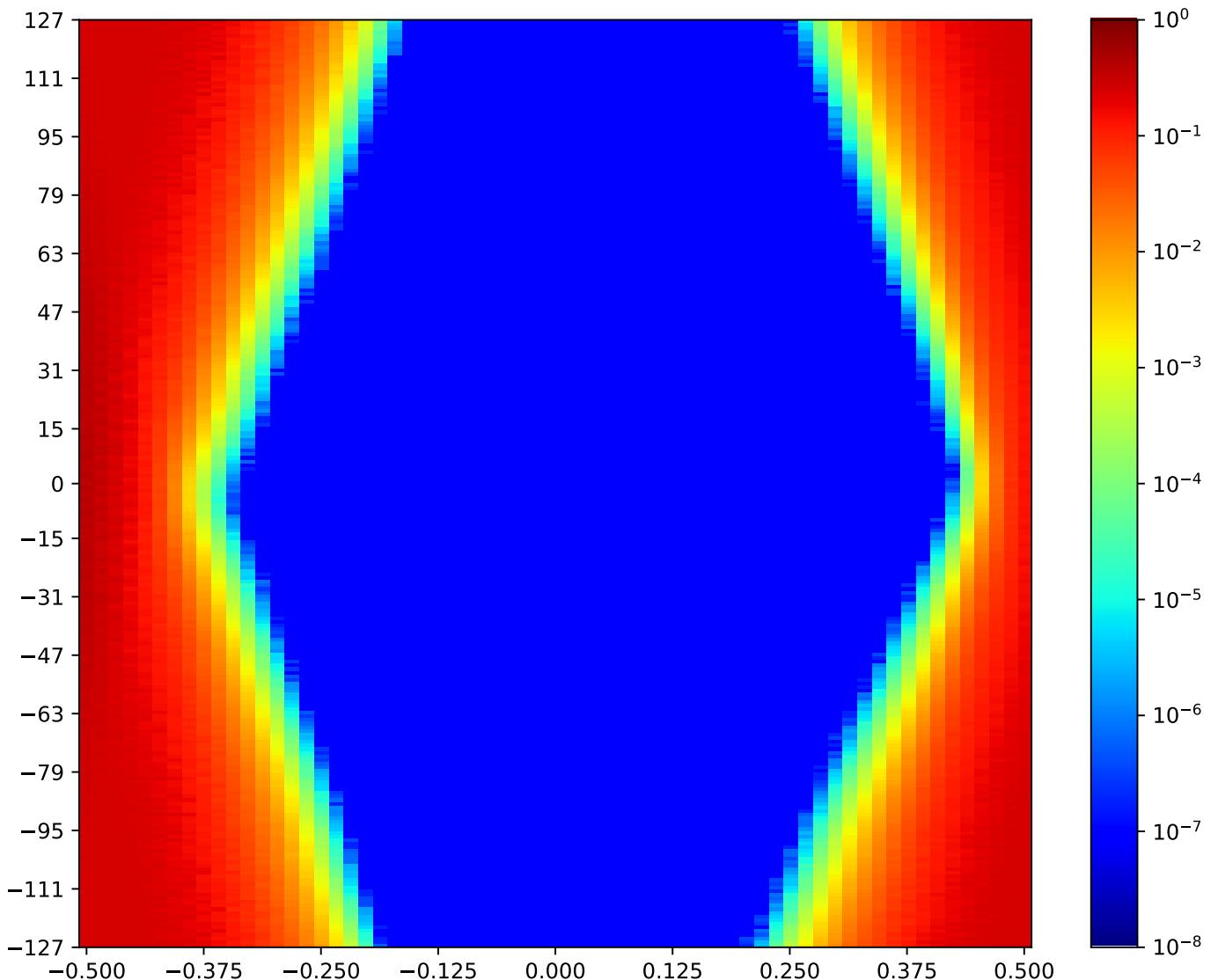


Figure 3.78: MSP\_A\_FPGA-IC39-08-IC4-08-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.10 MSP\_A\_FPGA-IC39-09-IC4-09-TRP\_FPGA

Table 3.71: MSP\_A\_FPGA-IC39-09-IC4-09-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:53:26		2018-Jan-23 23:53:47	
Reset RX	OA	HO		HO (%)	
true	9277	47		72.31%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

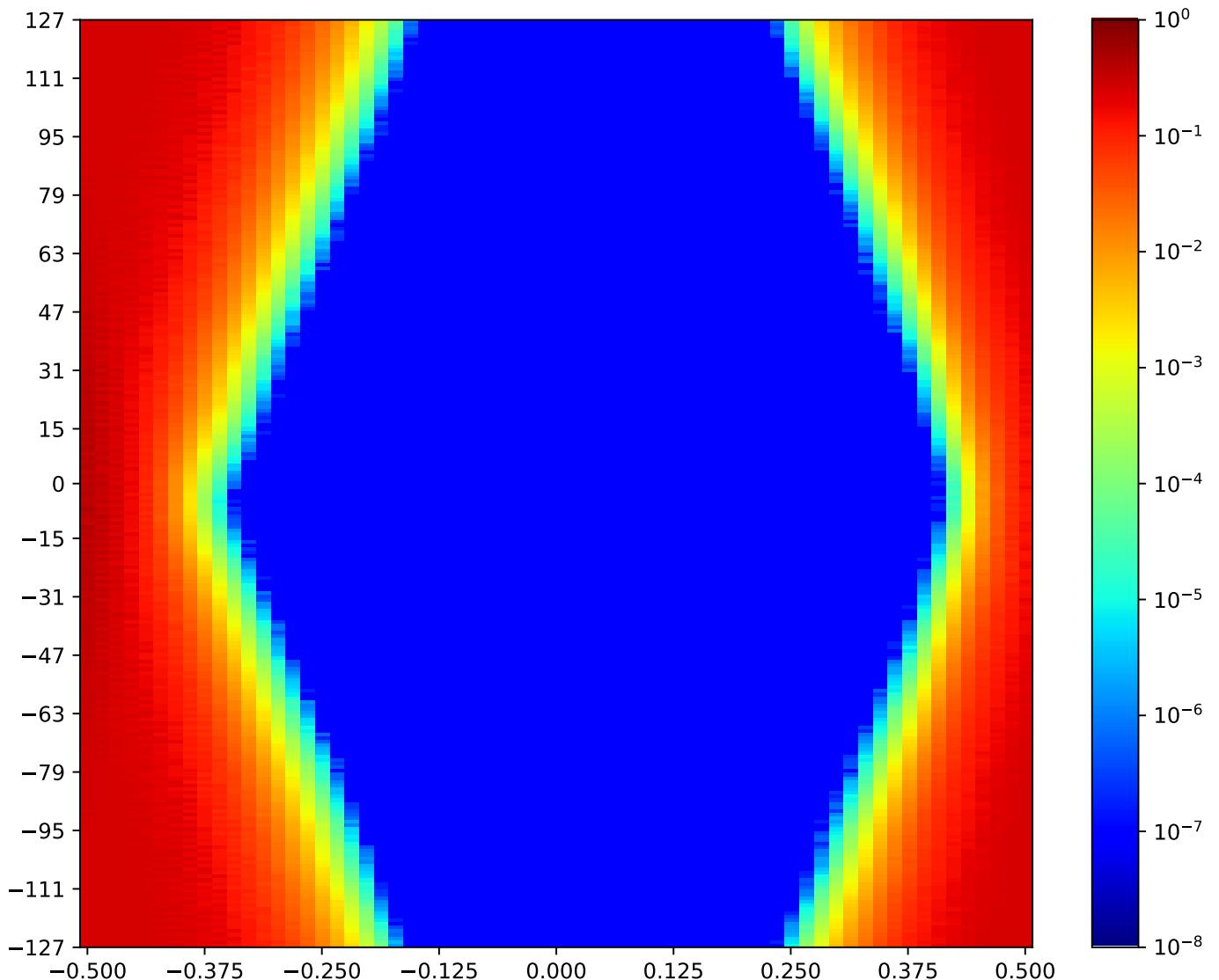


Figure 3.79: MSP\_A\_FPGA-IC39-09-IC4-09-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.11 MSP\_A\_FPGA-IC39-10-IC4-10-TRP\_FPGA

Table 3.72: MSP\_A\_FPGA-IC39-10-IC4-10-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:53:47		2018-Jan-23 23:54:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8367	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

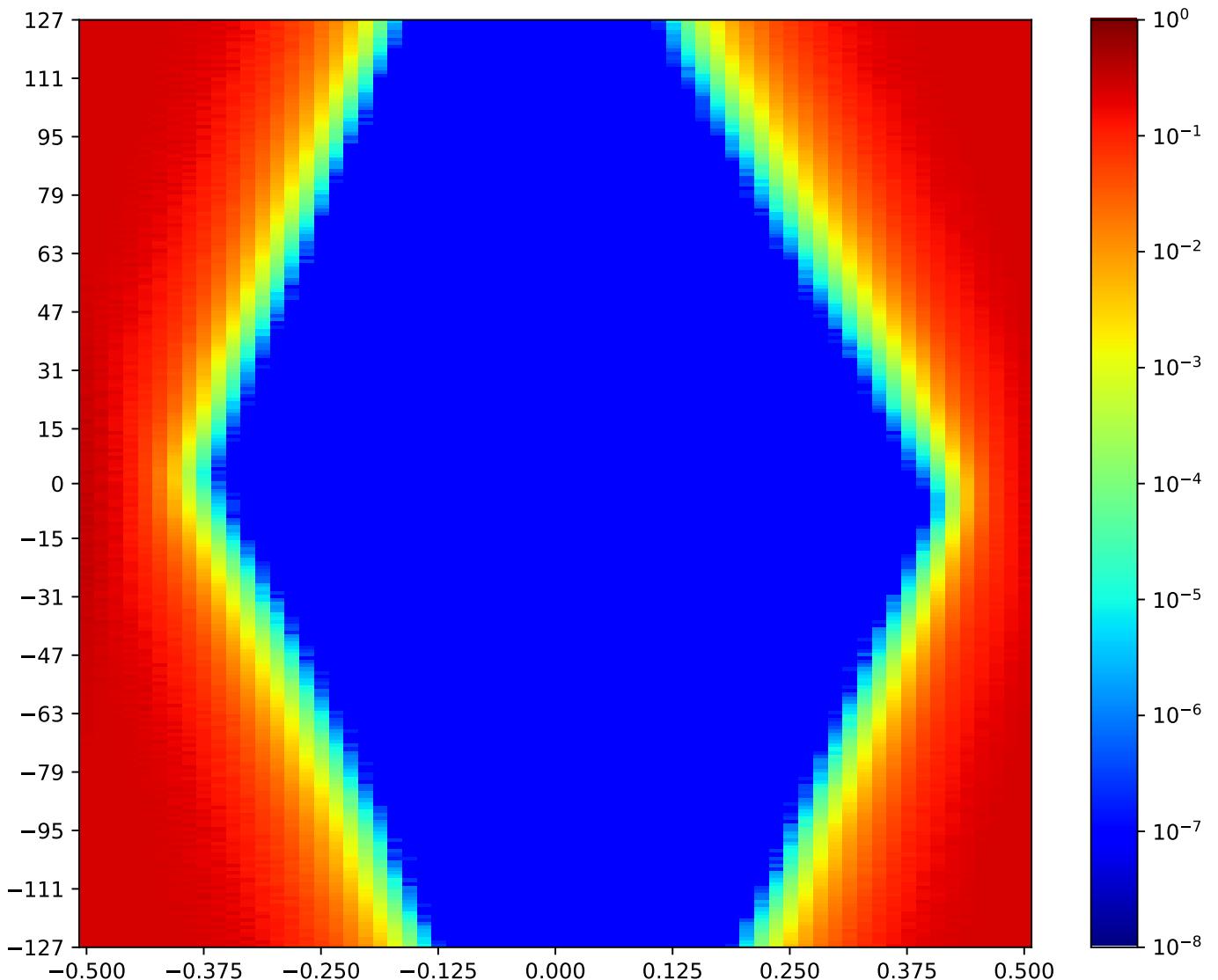


Figure 3.80: MSP\_A\_FPGA-IC39-10-IC4-10-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.12 MSP\_A\_FPGA-IC39-11-IC4-11-TRP\_FPGA

Table 3.73: MSP\_A\_FPGA-IC39-11-IC4-11-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:54:07		2018-Jan-23 23:54:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9246	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
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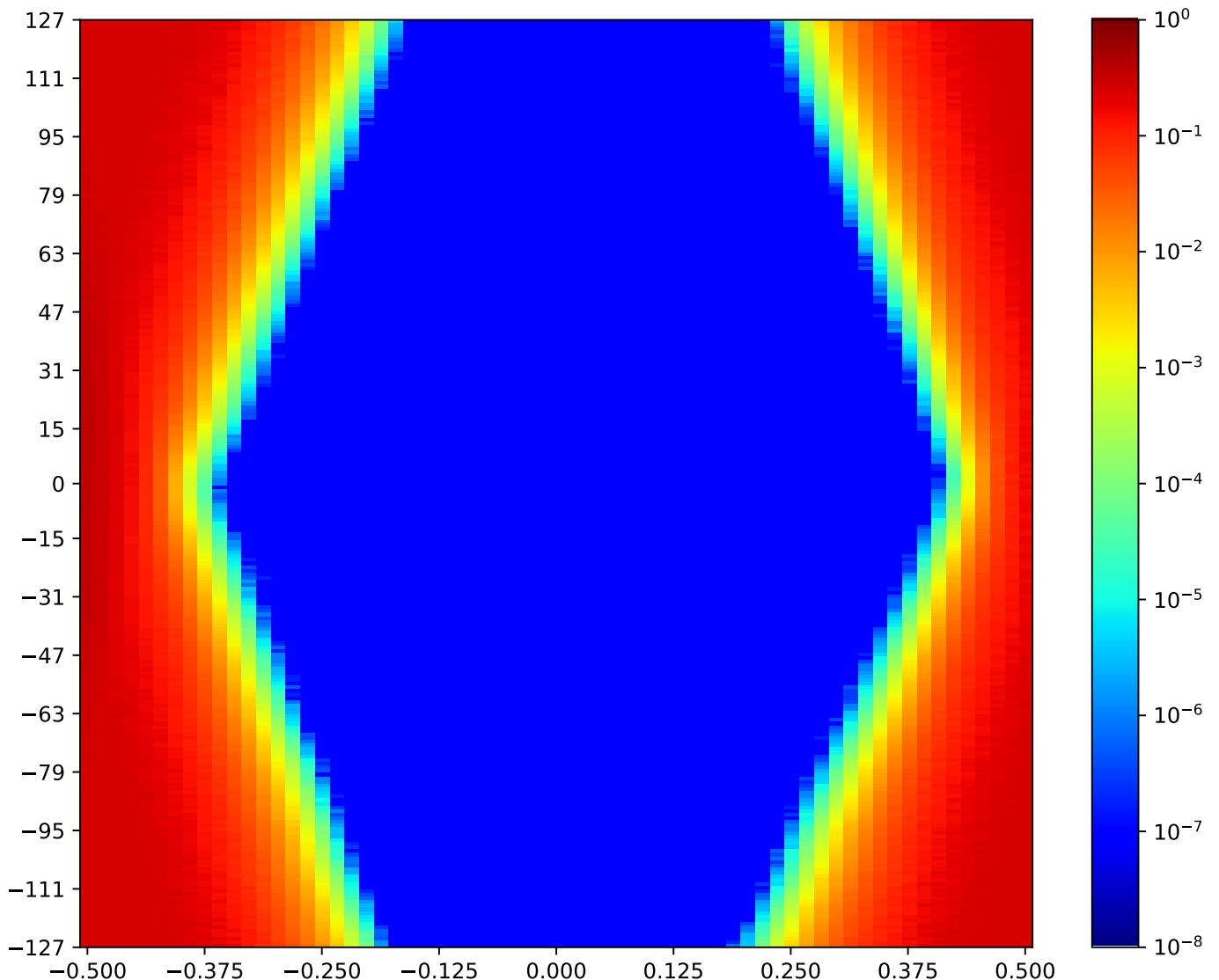


Figure 3.81: MSP\_A\_FPGA-IC39-11-IC4-11-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.13 MSP\_A\_FPGA-IC39-12-IC4-12-TRP\_FPGA

Table 3.74: MSP\_A\_FPGA-IC39-12-IC4-12-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:54:28		2018-Jan-23 23:54:48	
Reset RX	OA	HO		VO   VO (%)	
true	9712	47		72.31%	255   100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

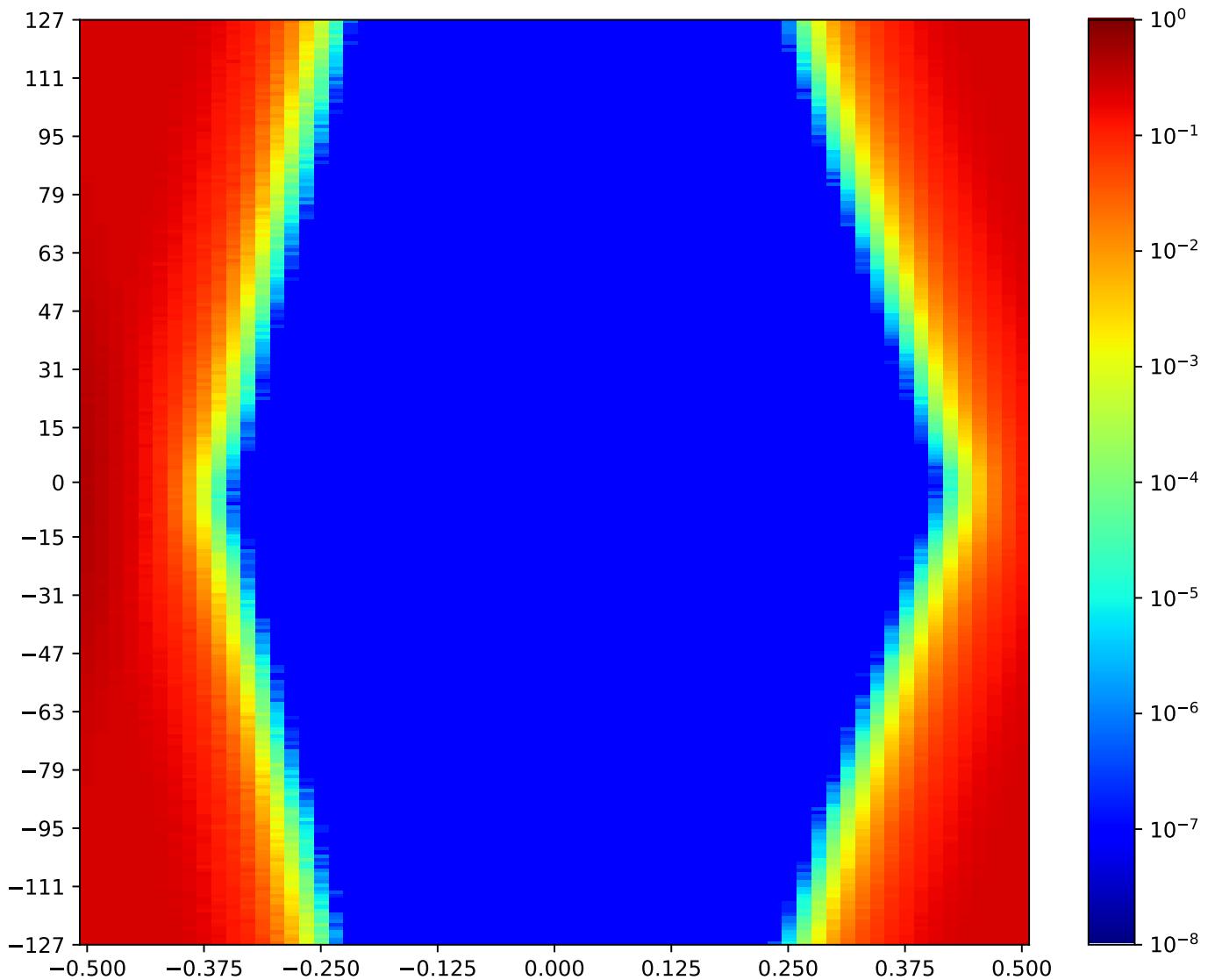


Figure 3.82: MSP\_A\_FPGA-IC39-12-IC4-12-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.14 MSP\_A\_FPGA-IC39-13-IC4-13-TRP\_FPGA

Table 3.75: MSP\_A\_FPGA-IC39-13-IC4-13-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:54:49		2018-Jan-23 23:55:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10451	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

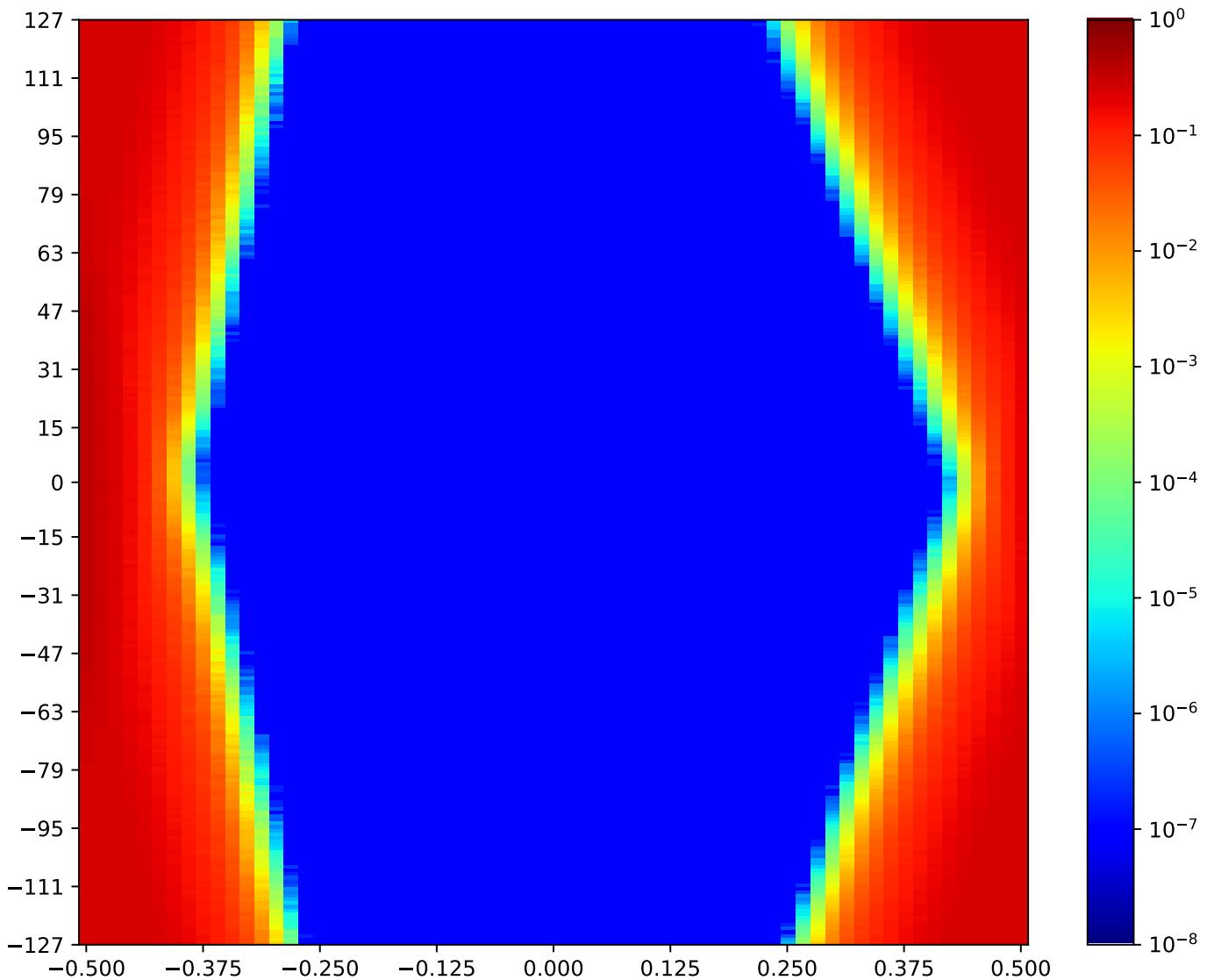


Figure 3.83: MSP\_A\_FPGA-IC39-13-IC4-13-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.15 MSP\_A\_FPGA-IC39-14-IC4-14-TRP\_FPGA

Table 3.76: MSP\_A\_FPGA-IC39-14-IC4-14-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:55:09		2018-Jan-23 23:55:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9526	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

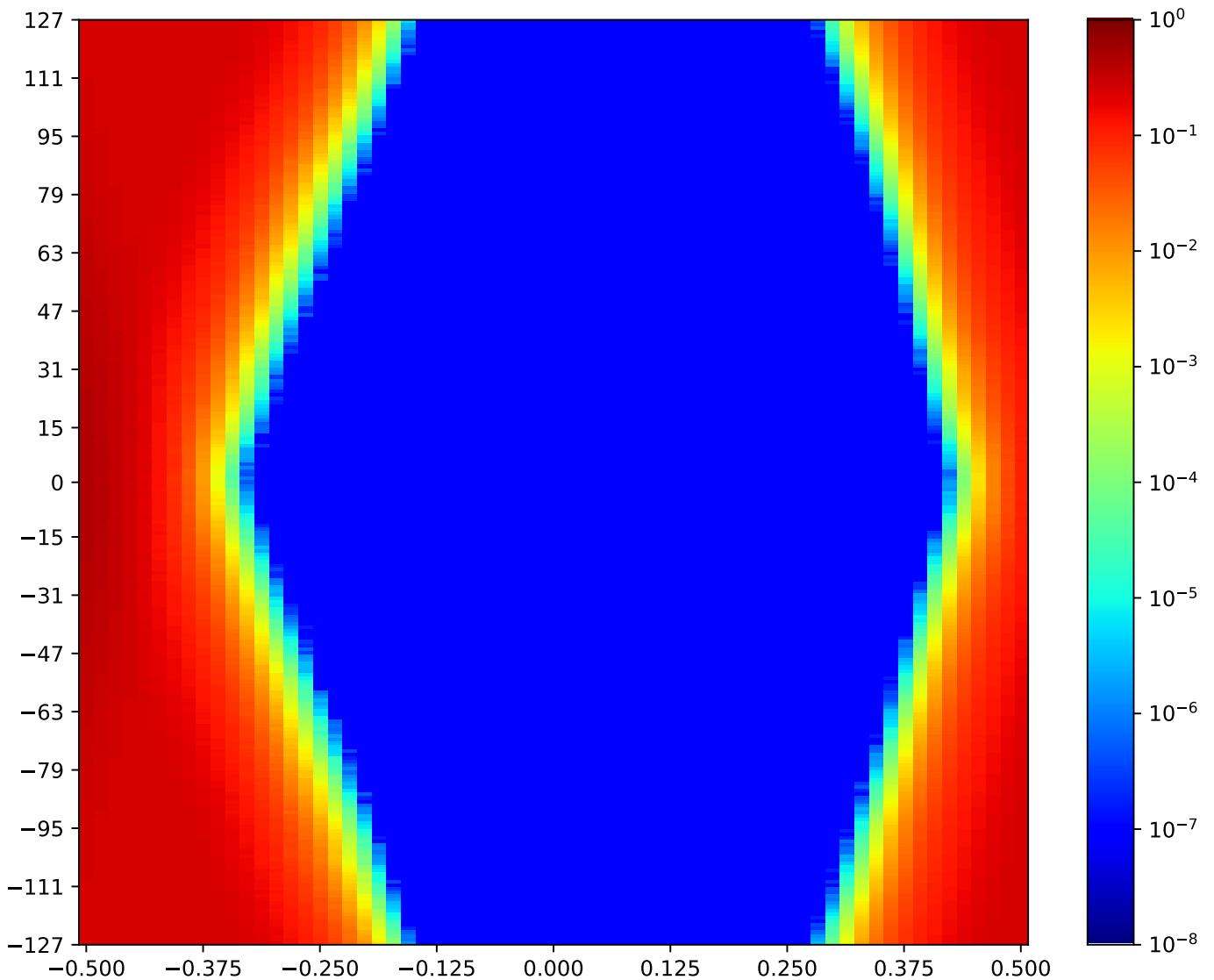


Figure 3.84: MSP\_A\_FPGA-IC39-14-IC4-14-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.16 MSP\_A\_FPGA-IC39-15-IC4-15-TRP\_FPGA

Table 3.77: MSP\_A\_FPGA-IC39-15-IC4-15-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:55:30		2018-Jan-23 23:55:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9962	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

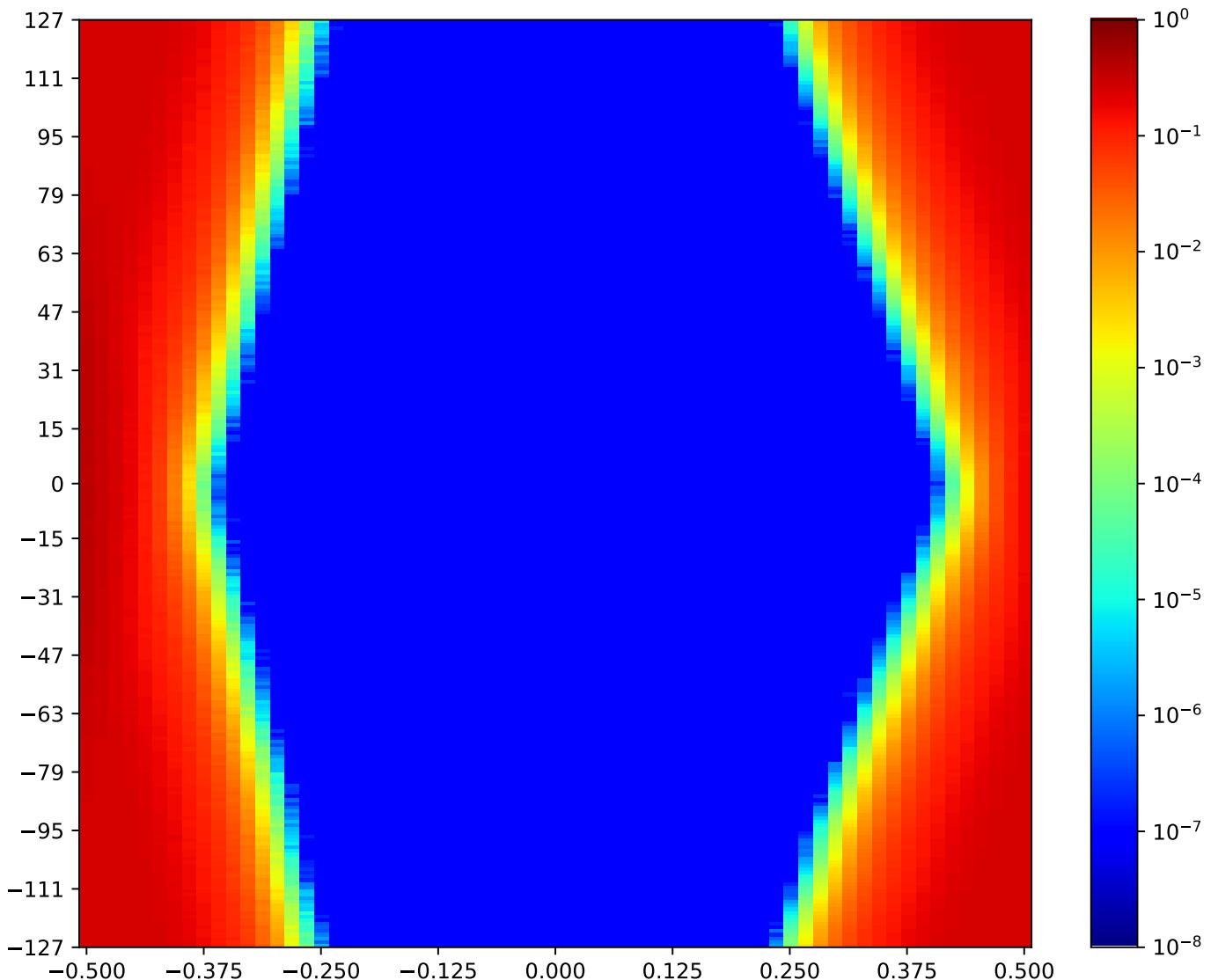


Figure 3.85: MSP\_A\_FPGA-IC39-15-IC4-15-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.17 MSP\_A\_FPGA-IC39-16-IC4-16-TRP\_FPGA

Table 3.78: MSP\_A\_FPGA-IC39-16-IC4-16-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:55:51		2018-Jan-23 23:56:11	
Reset RX	OA	HO		HO (%)	
true	9035	47		72.31%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

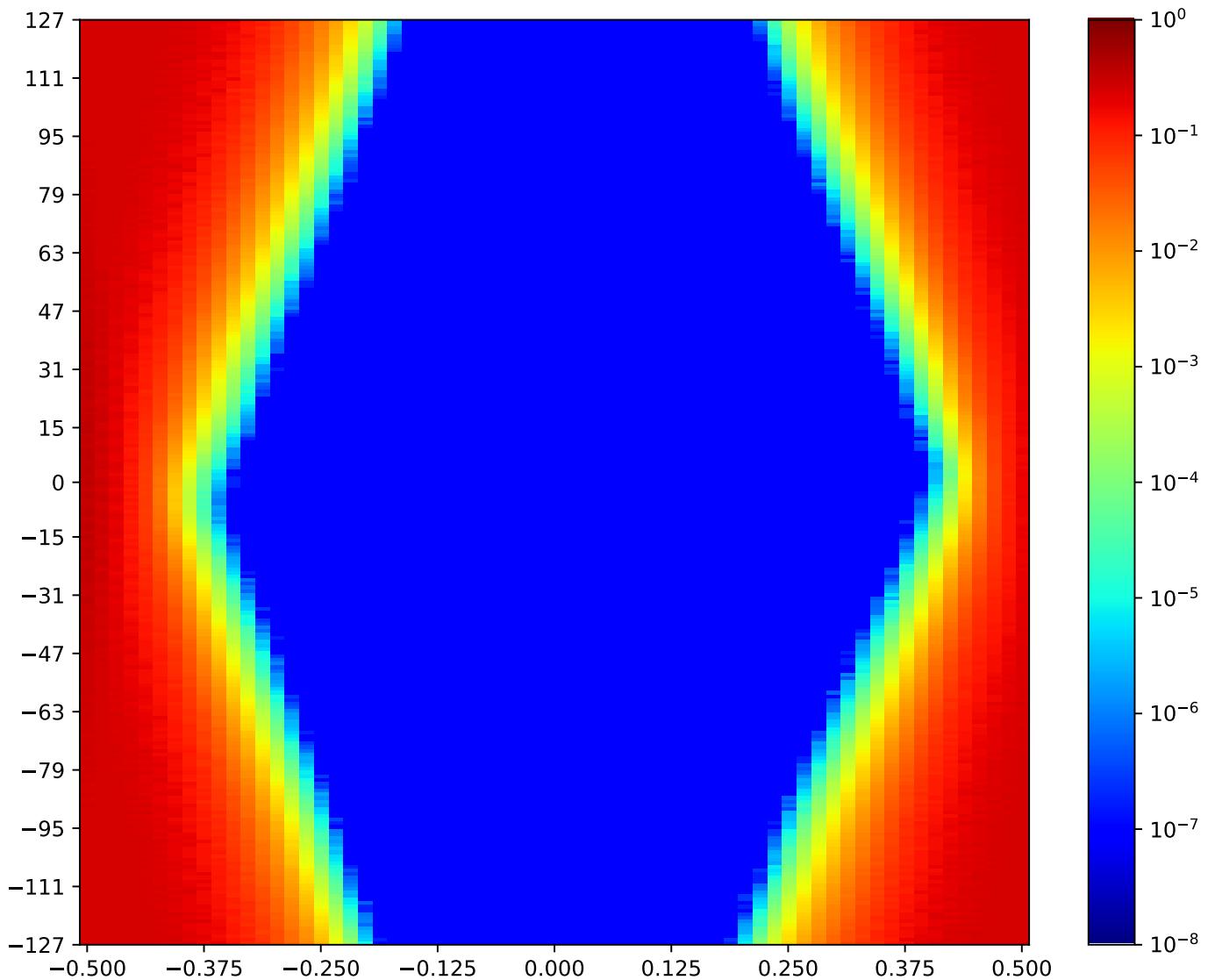


Figure 3.86: MSP\_A\_FPGA-IC39-16-IC4-16-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.18 MSP\_A\_FPGA-IC39-17-IC4-17-TRP\_FPGA

Table 3.79: MSP\_A\_FPGA-IC39-17-IC4-17-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:56:11		2018-Jan-23 23:56:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9399	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

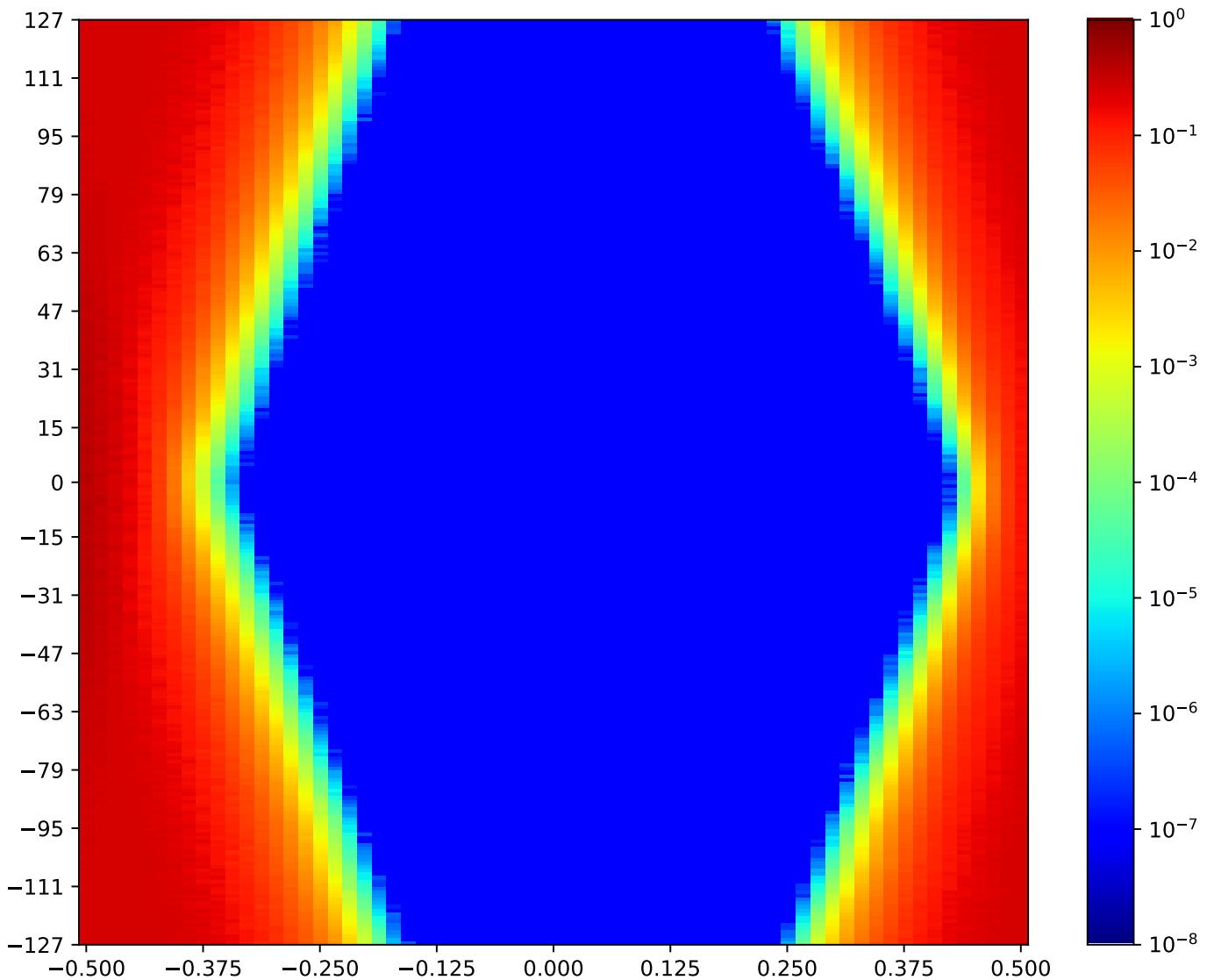


Figure 3.87: MSP\_A\_FPGA-IC39-17-IC4-17-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.19 MSP\_A\_FPGA-IC39-18-IC4-18-TRP\_FPGA

Table 3.80: MSP\_A\_FPGA-IC39-18-IC4-18-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:56:31		2018-Jan-23 23:56:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9075	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

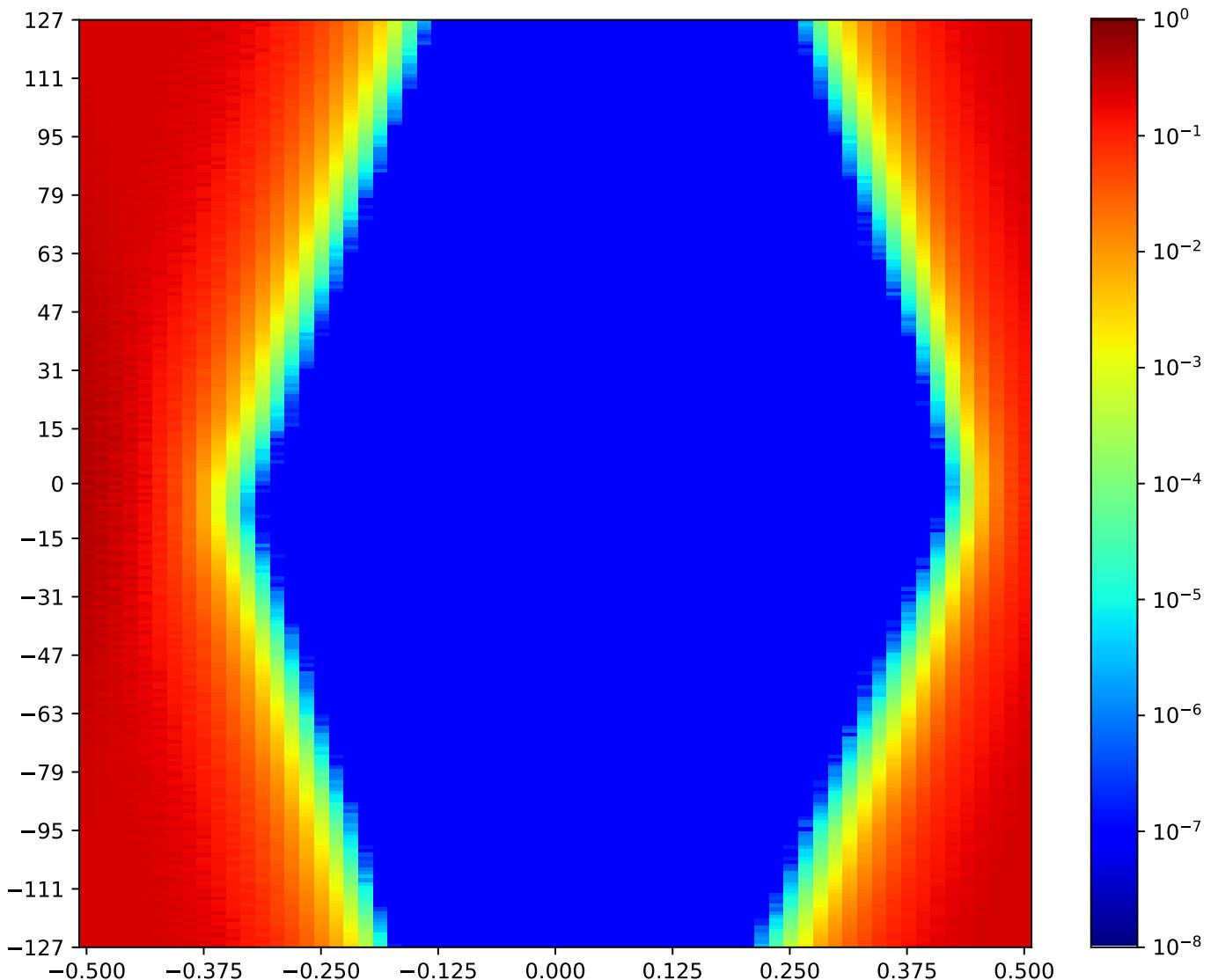


Figure 3.88: MSP\_A\_FPGA-IC39-18-IC4-18-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.20 MSP\_A\_FPGA-IC39-19-IC4-19-TRP\_FPGA

Table 3.81: MSP\_A\_FPGA-IC39-19-IC4-19-TRP\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:56:51			2018-Jan-23 23:57:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	9084	44	67.69%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

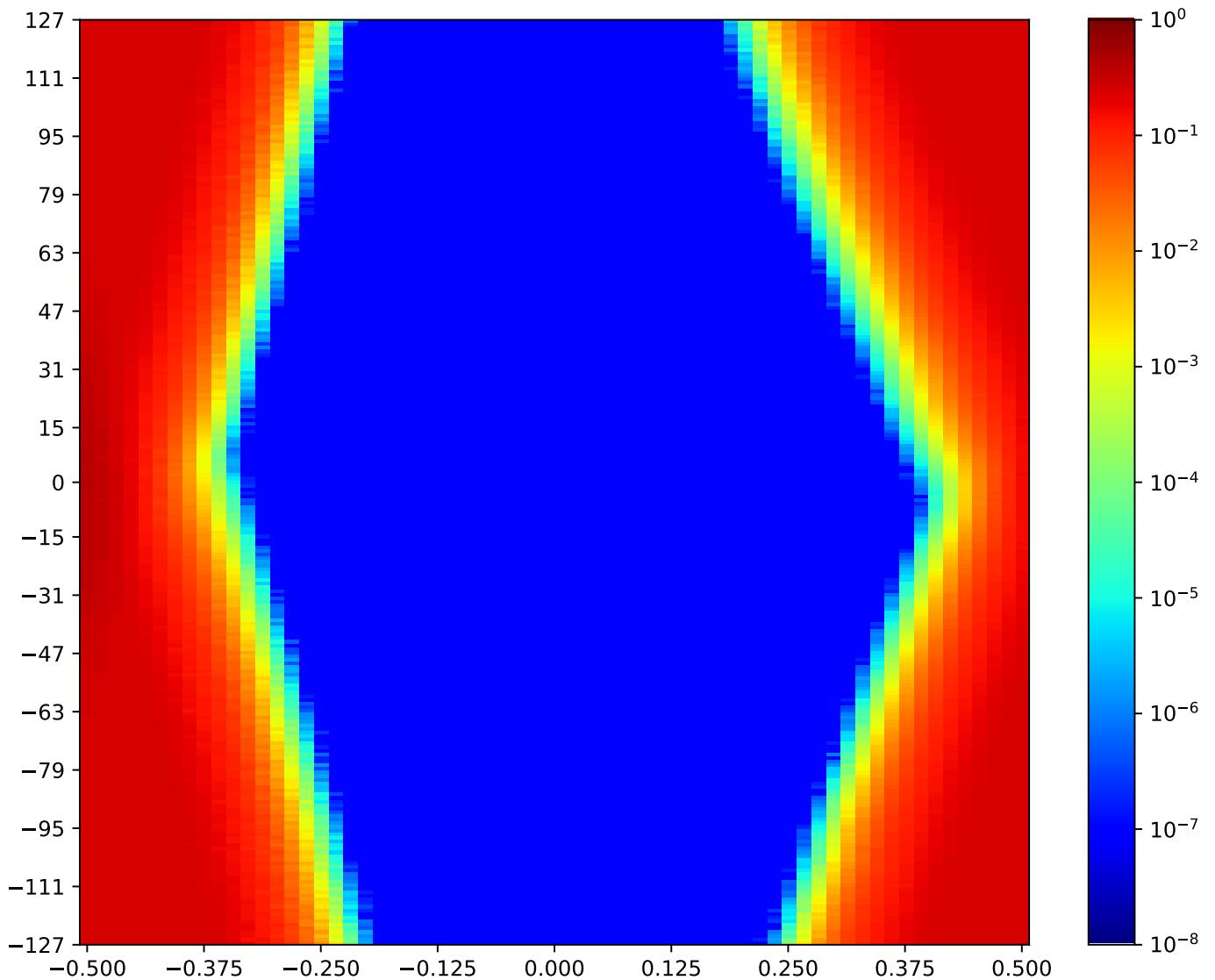


Figure 3.89: MSP\_A\_FPGA-IC39-19-IC4-19-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.21 MSP\_A\_FPGA-IC39-20-IC4-20-TRP\_FPGA

Table 3.82: MSP\_A\_FPGA-IC39-20-IC4-20-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:57:11		2018-Jan-23 23:57:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10245	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

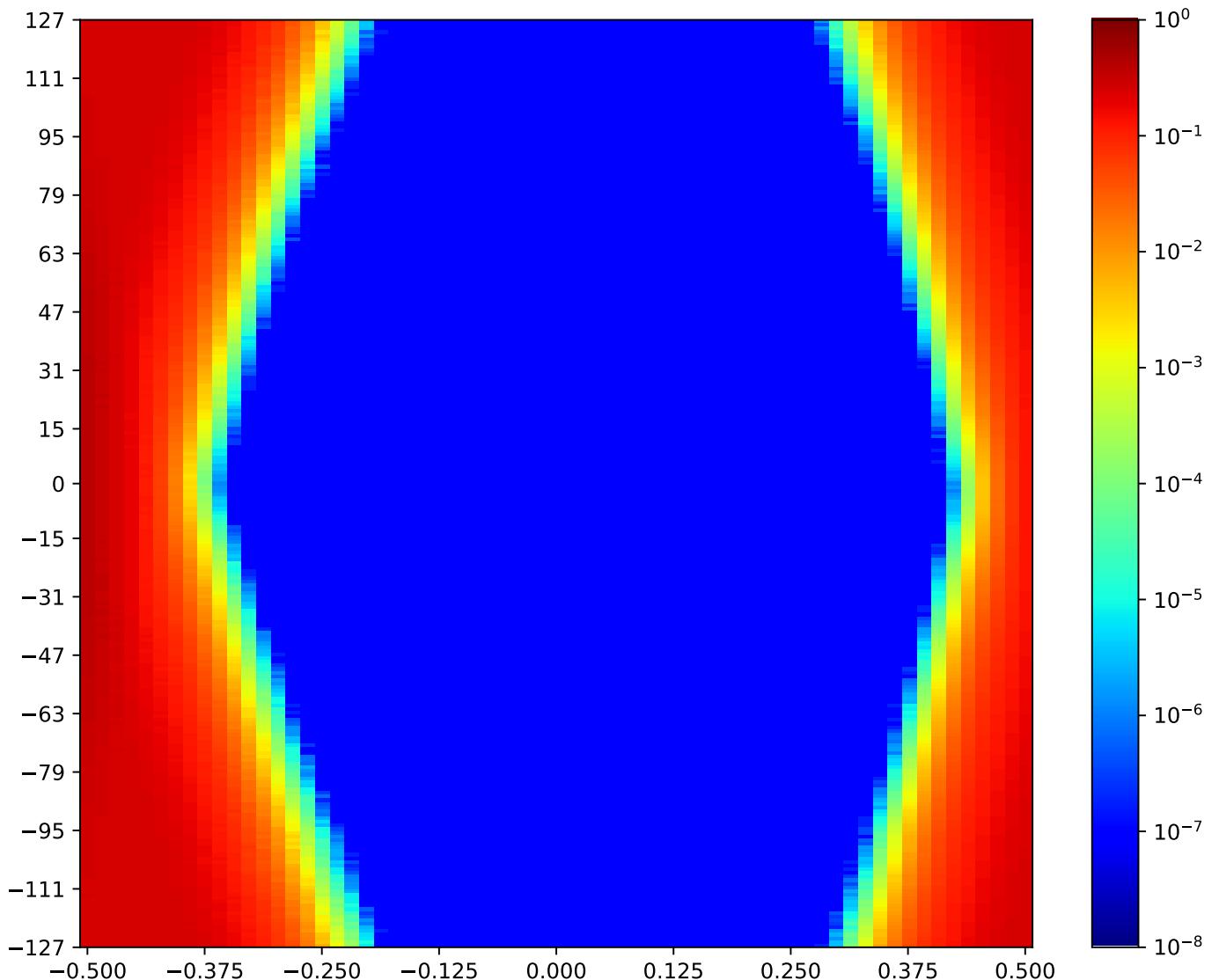


Figure 3.90: MSP\_A\_FPGA-IC39-20-IC4-20-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.22 MSP\_A\_FPGA-IC39-21-IC4-21-TRP\_FPGA

Table 3.83: MSP\_A\_FPGA-IC39-21-IC4-21-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:57:32		2018-Jan-23 23:57:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8343	46	70.77%	255	100.00%
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BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

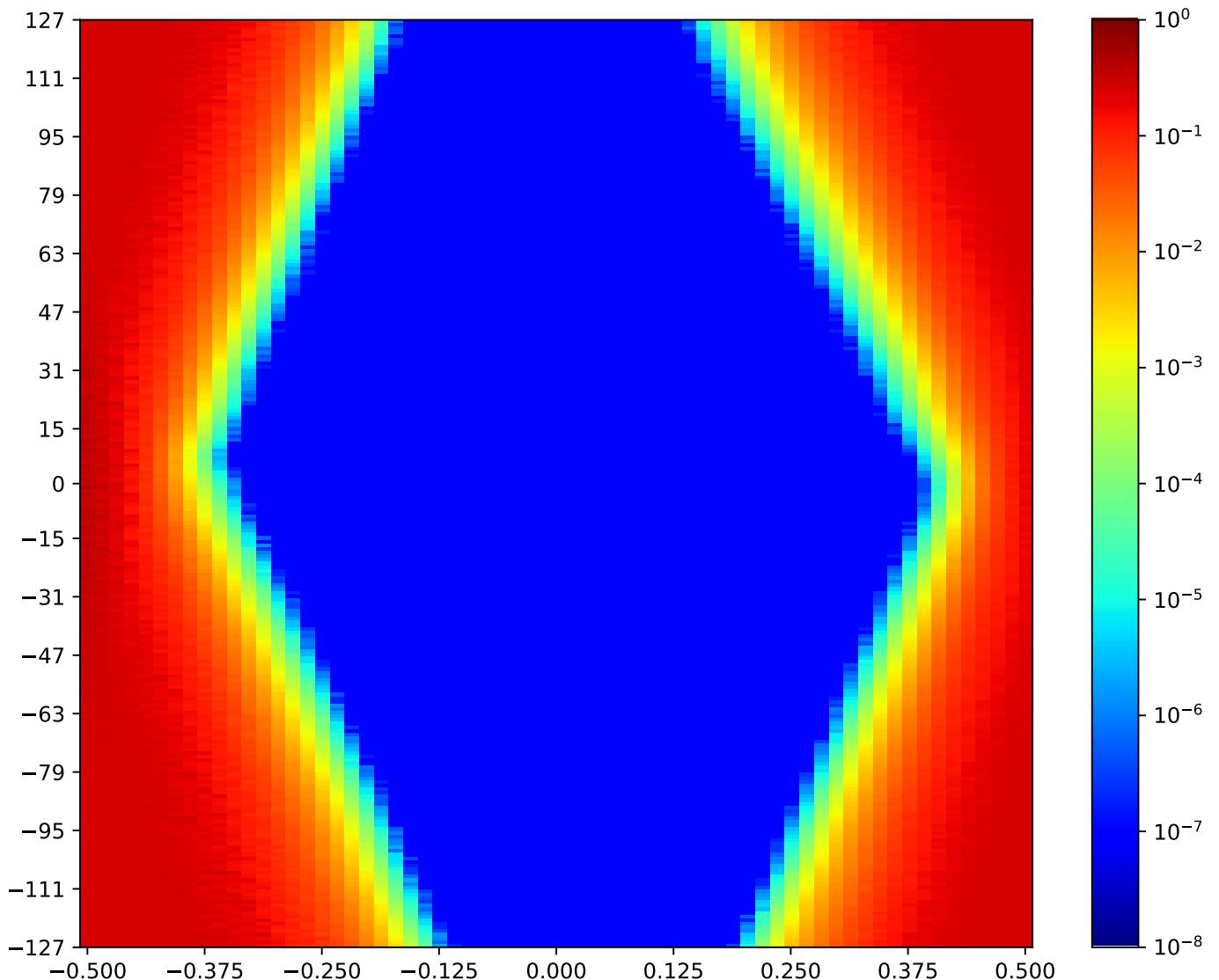


Figure 3.91: MSP\_A\_FPGA-IC39-21-IC4-21-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.23 MSP\_A\_FPGA-IC39-22-IC4-22-TRP\_FPGA

Table 3.84: MSP\_A\_FPGA-IC39-22-IC4-22-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:57:52		2018-Jan-23 23:58:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10865	50	76.92%	255	100.00%
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BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

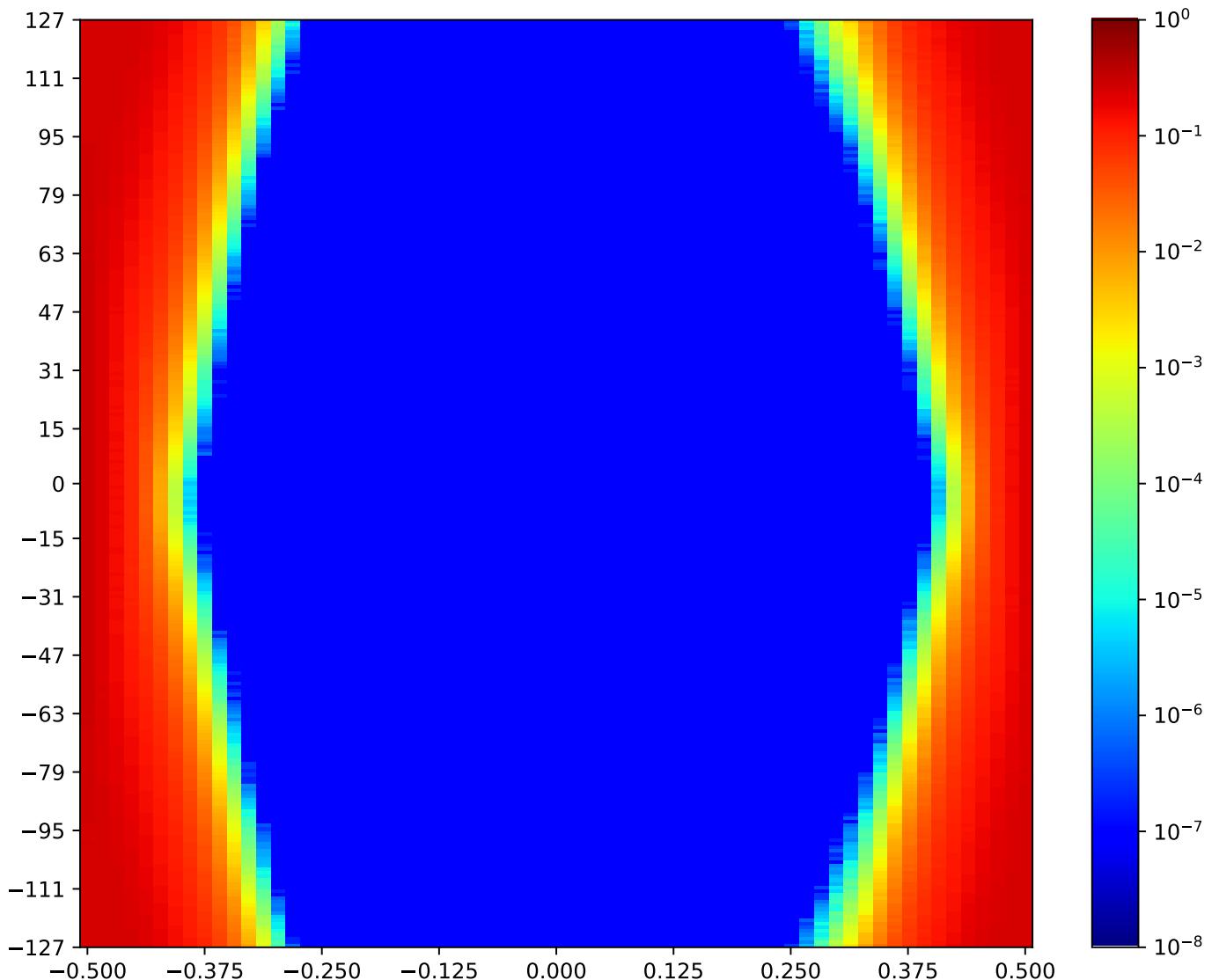


Figure 3.92: MSP\_A\_FPGA-IC39-22-IC4-22-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.24 MSP\_A\_FPGA-IC39-23-IC4-23-TRP\_FPGA

Table 3.85: MSP\_A\_FPGA-IC39-23-IC4-23-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:58:12		2018-Jan-23 23:58:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10234	49	75.38%	255	100.00%
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BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

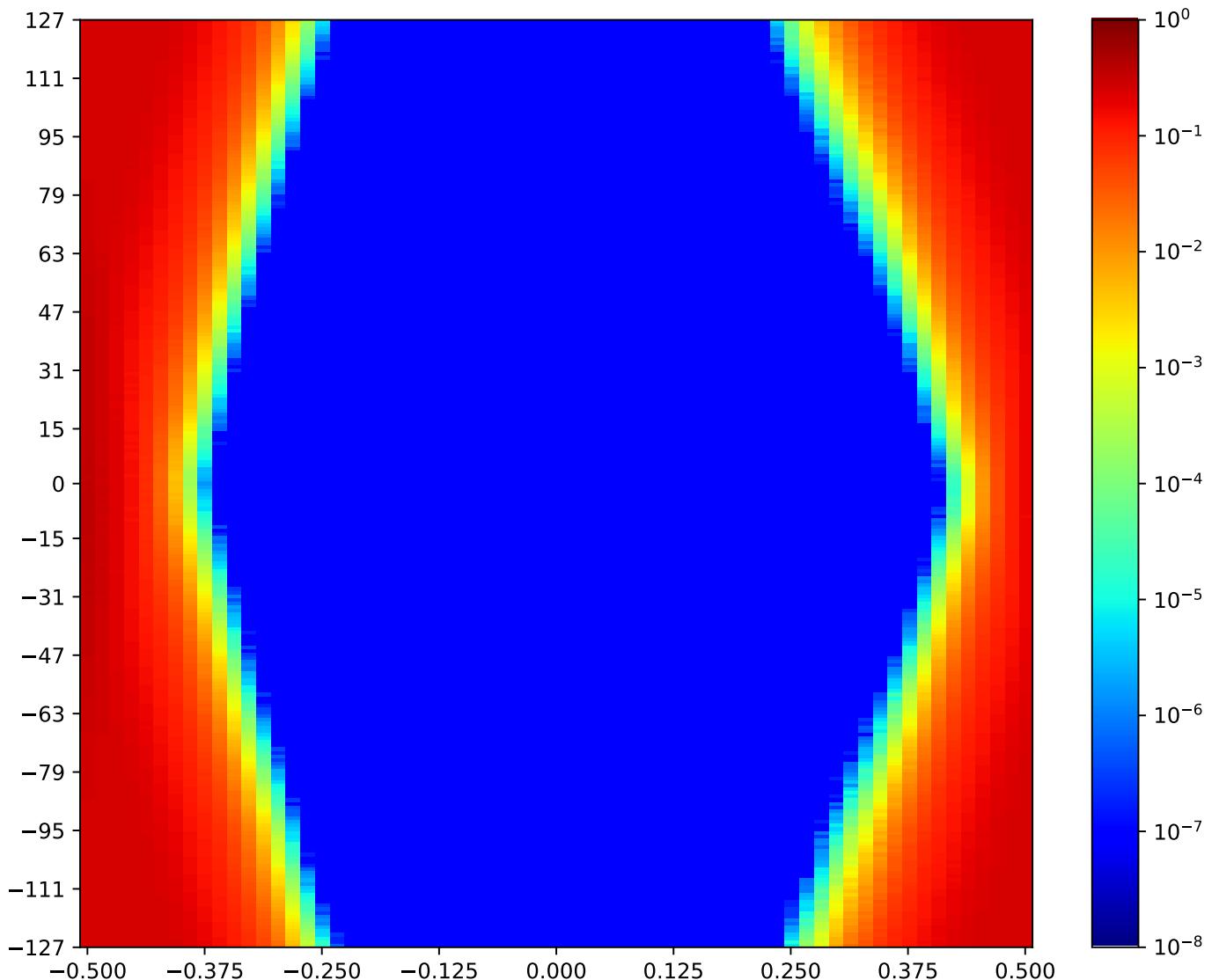


Figure 3.93: MSP\_A\_FPGA-IC39-23-IC4-23-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.25 MSP\_A\_FPGA-IC39-24-IC4-24-TRP\_FPGA

Table 3.86: MSP\_A\_FPGA-IC39-24-IC4-24-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:58:33		2018-Jan-23 23:58:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9128	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

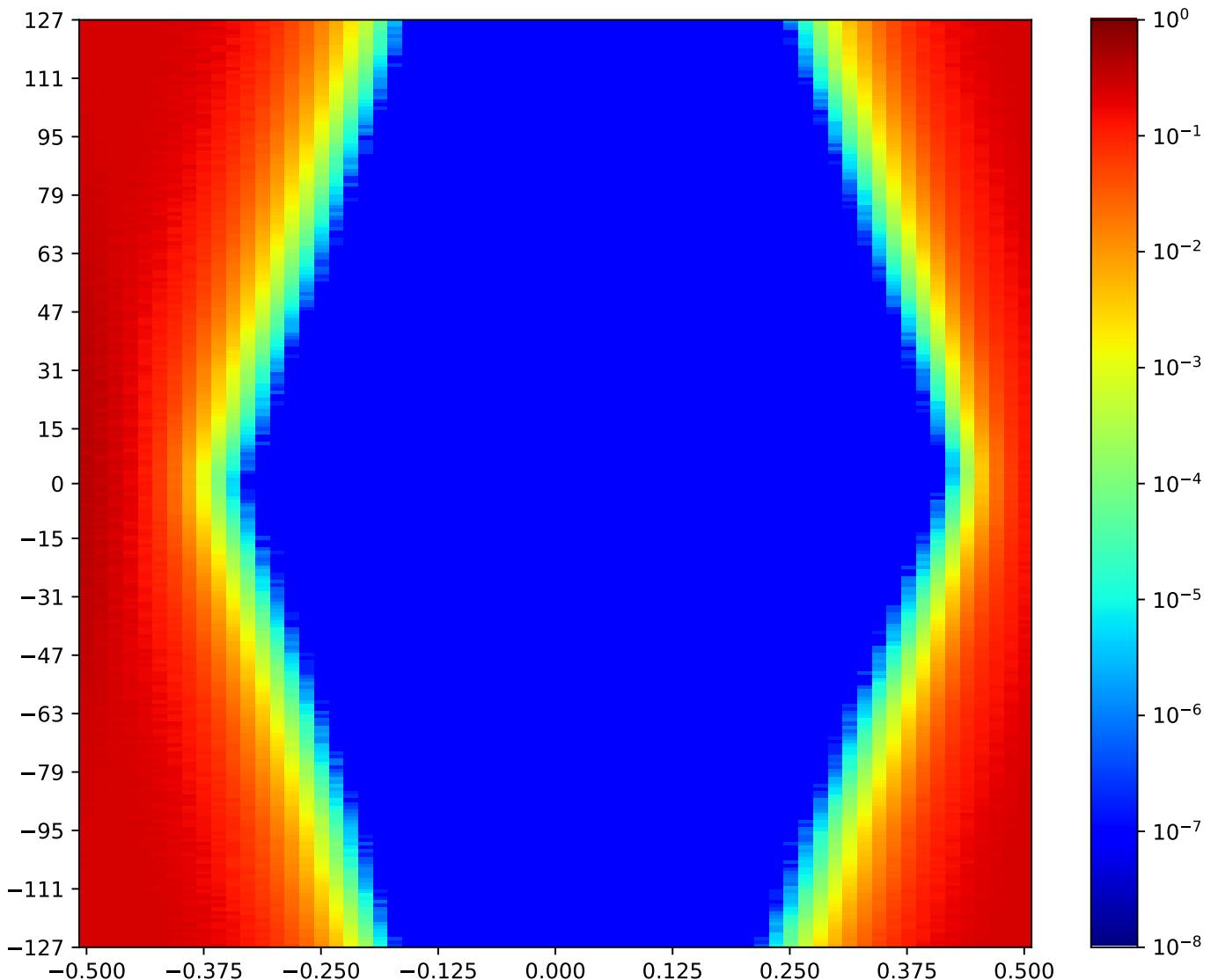


Figure 3.94: MSP\_A\_FPGA-IC39-24-IC4-24-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.26 MSP\_A\_FPGA-IC39-25-IC4-25-TRP\_FPGA

Table 3.87: MSP\_A\_FPGA-IC39-25-IC4-25-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:58:53		2018-Jan-23 23:59:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10753	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

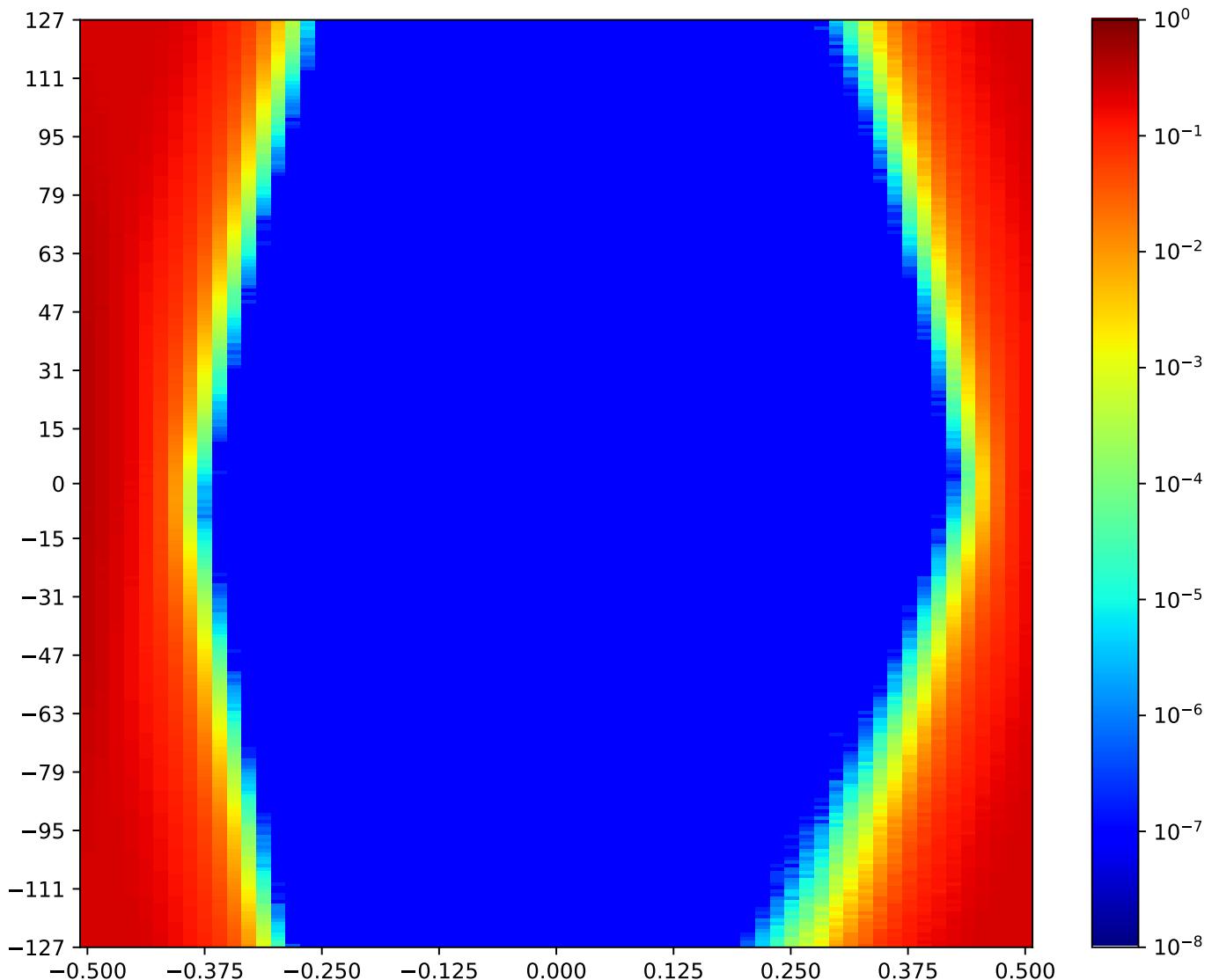


Figure 3.95: MSP\_A\_FPGA-IC39-25-IC4-25-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.27 MSP\_A\_FPGA-IC39-26-IC4-26-TRP\_FPGA

Table 3.88: MSP\_A\_FPGA-IC39-26-IC4-26-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:59:13		2018-Jan-23 23:59:34	
Reset RX	OA	HO		HO (%)	
true	9141	46		70.77%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

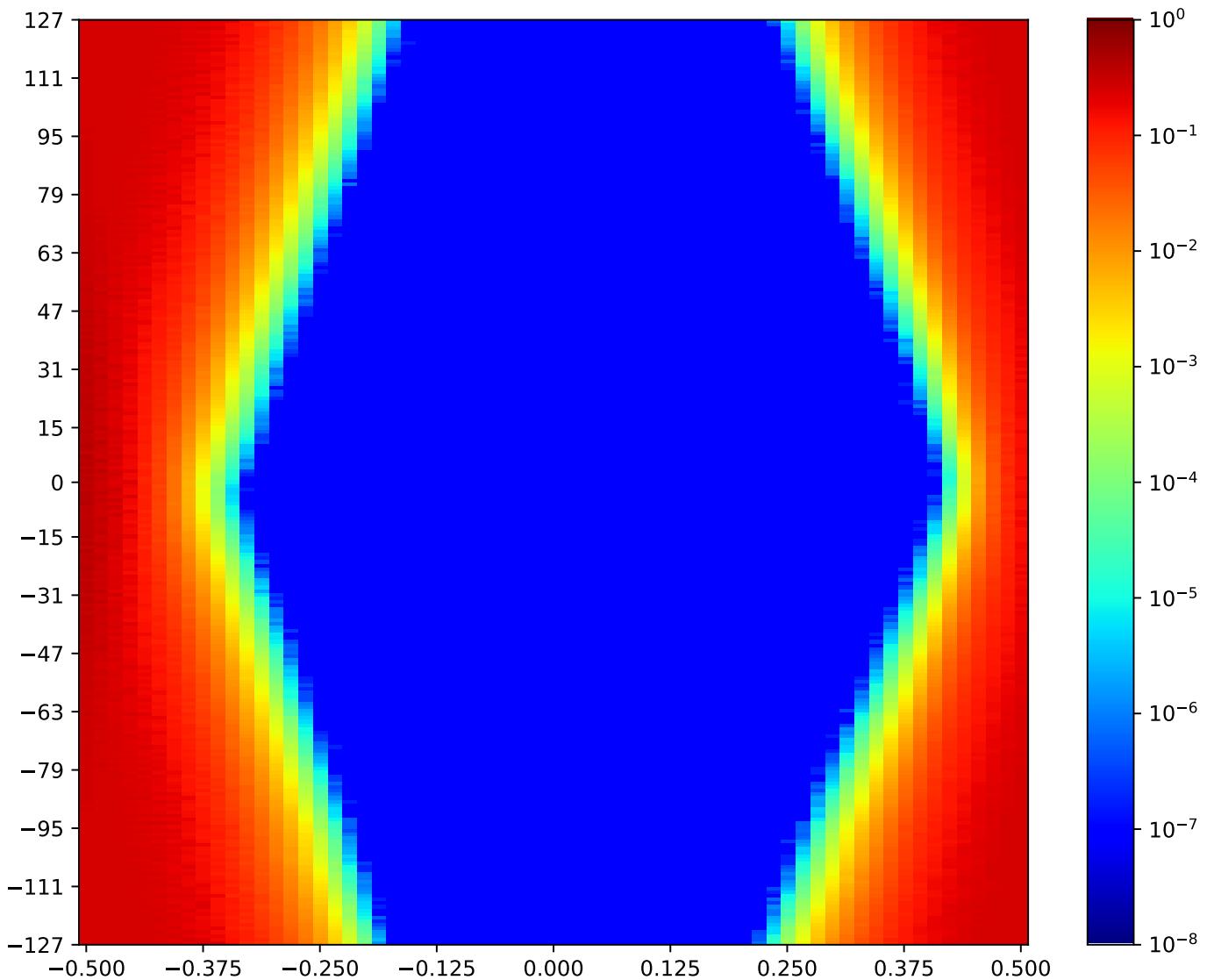


Figure 3.96: MSP\_A\_FPGA-IC39-26-IC4-26-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.8.28 MSP\_A\_FPGA-IC39-27-IC4-27-TRP\_FPGA

Table 3.89: MSP\_A\_FPGA-IC39-27-IC4-27-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:59:34		2018-Jan-23 23:59:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9552	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

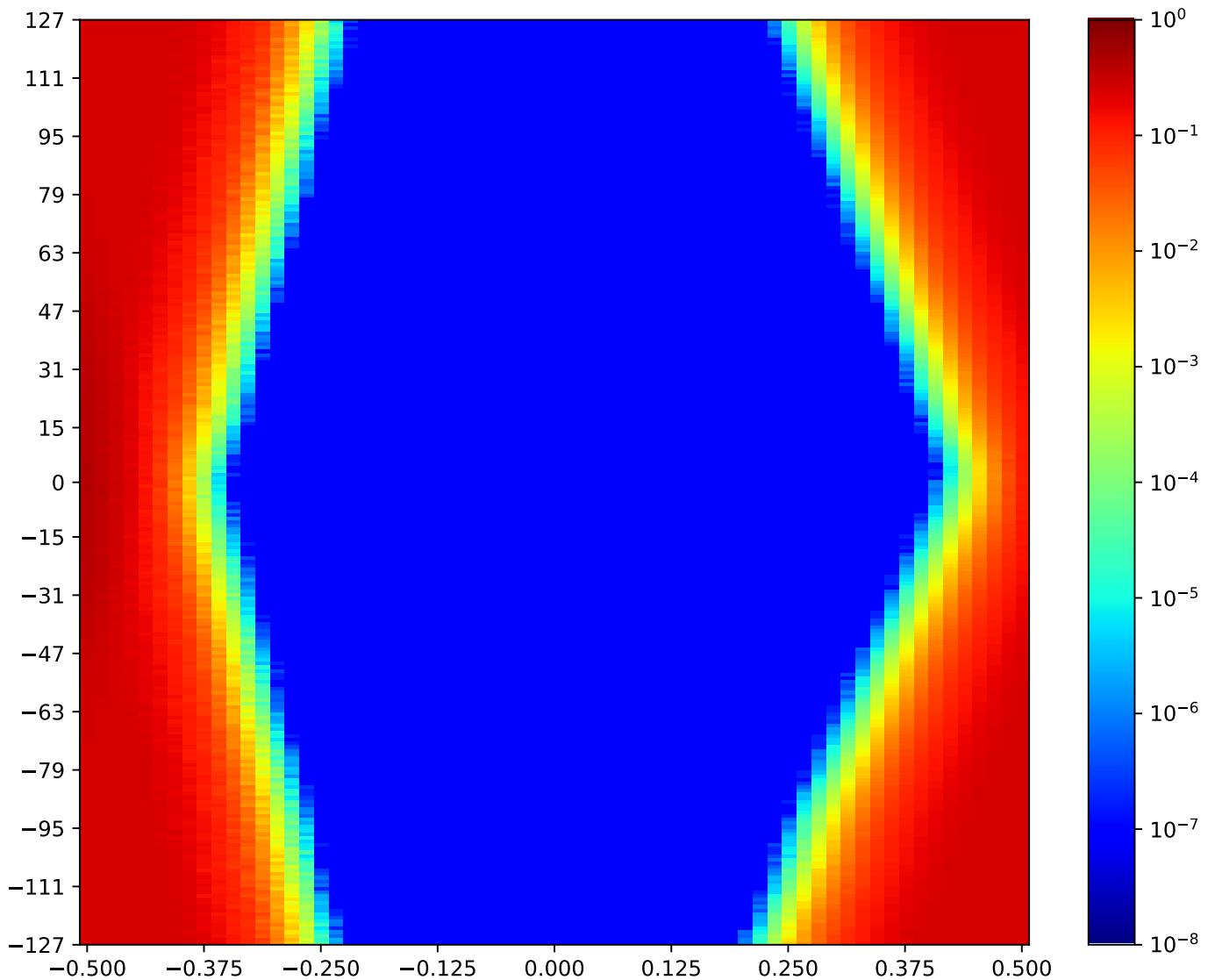


Figure 3.97: MSP\_A\_FPGA-IC39-27-IC4-27-TRP\_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9 MSP\_C TRP On board links

A cross-reference to Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.127.

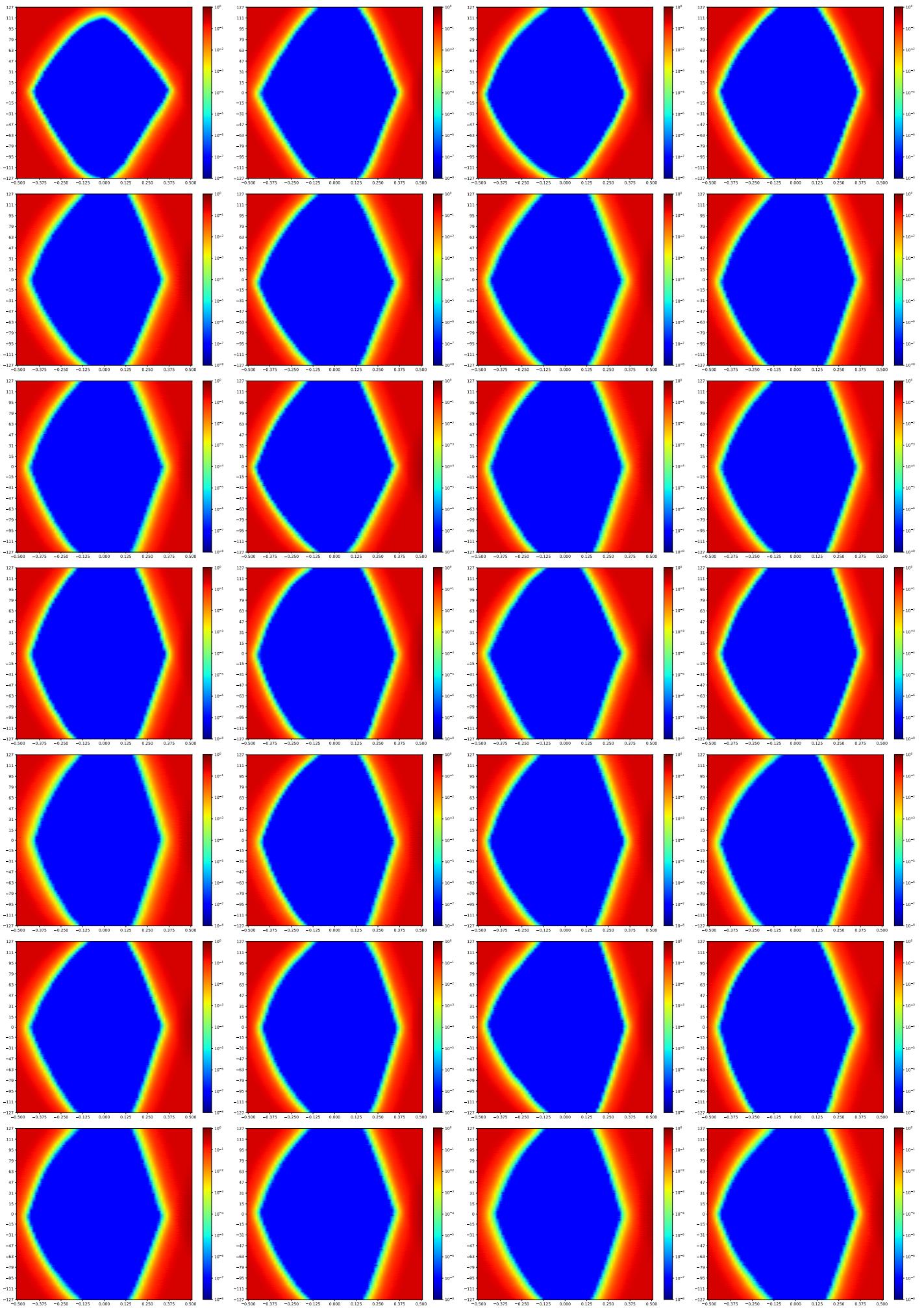


Figure 3.98: MSP\_C TRP On board links

### 3.9.1 MSP\_C\_FPGA-IC39-00-IC15-00-TRP\_FPGA

Table 3.90: MSP\_C\_FPGA-IC39-00-IC15-00-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:59:54		2018-Jan-24 00:00:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6936	48	73.85%	236	92.55%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

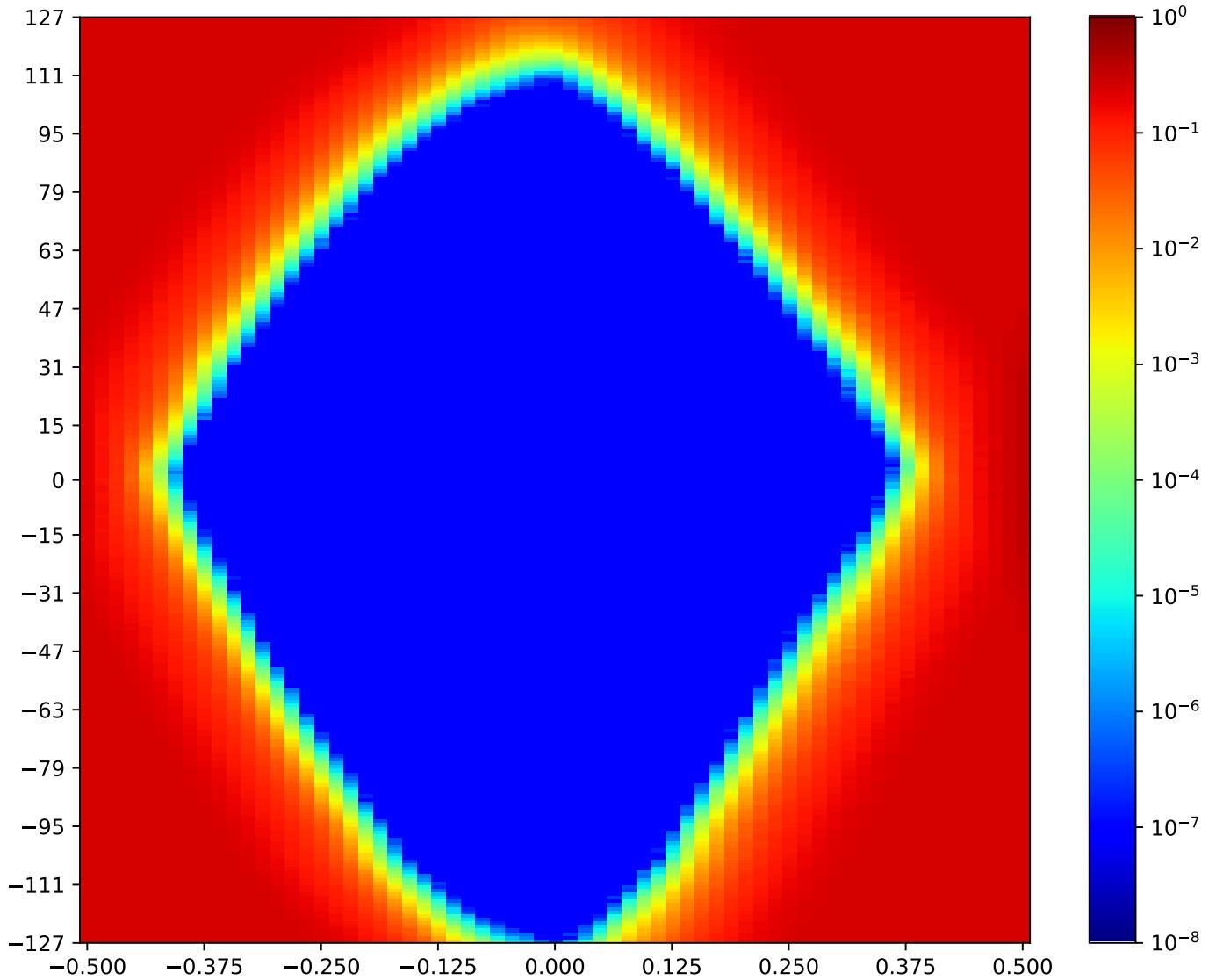


Figure 3.99: MSP\_C\_FPGA-IC39-00-IC15-00-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.2 MSP\_C\_FPGA-IC39-01-IC15-01-TRP\_FPGA

Table 3.91: MSP\_C\_FPGA-IC39-01-IC15-01-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:00:14		2018-Jan-24 00:00:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8472	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

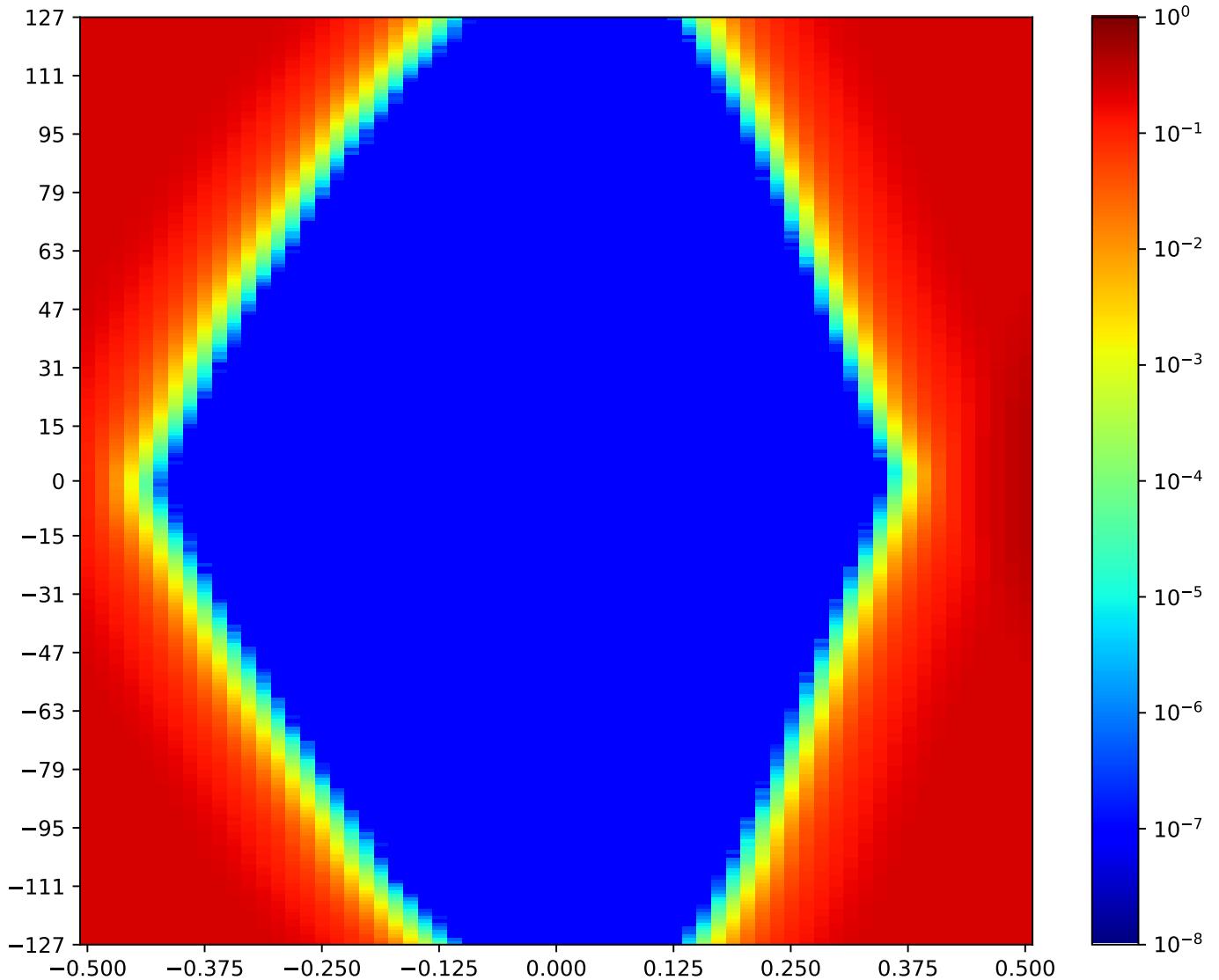


Figure 3.100: MSP\_C\_FPGA-IC39-01-IC15-01-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.3 MSP\_C\_FPGA-IC39-02-IC15-02-TRP\_FPGA

Table 3.92: MSP\_C\_FPGA-IC39-02-IC15-02-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:00:35		2018-Jan-24 00:00:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8267	49	75.38%	255	99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

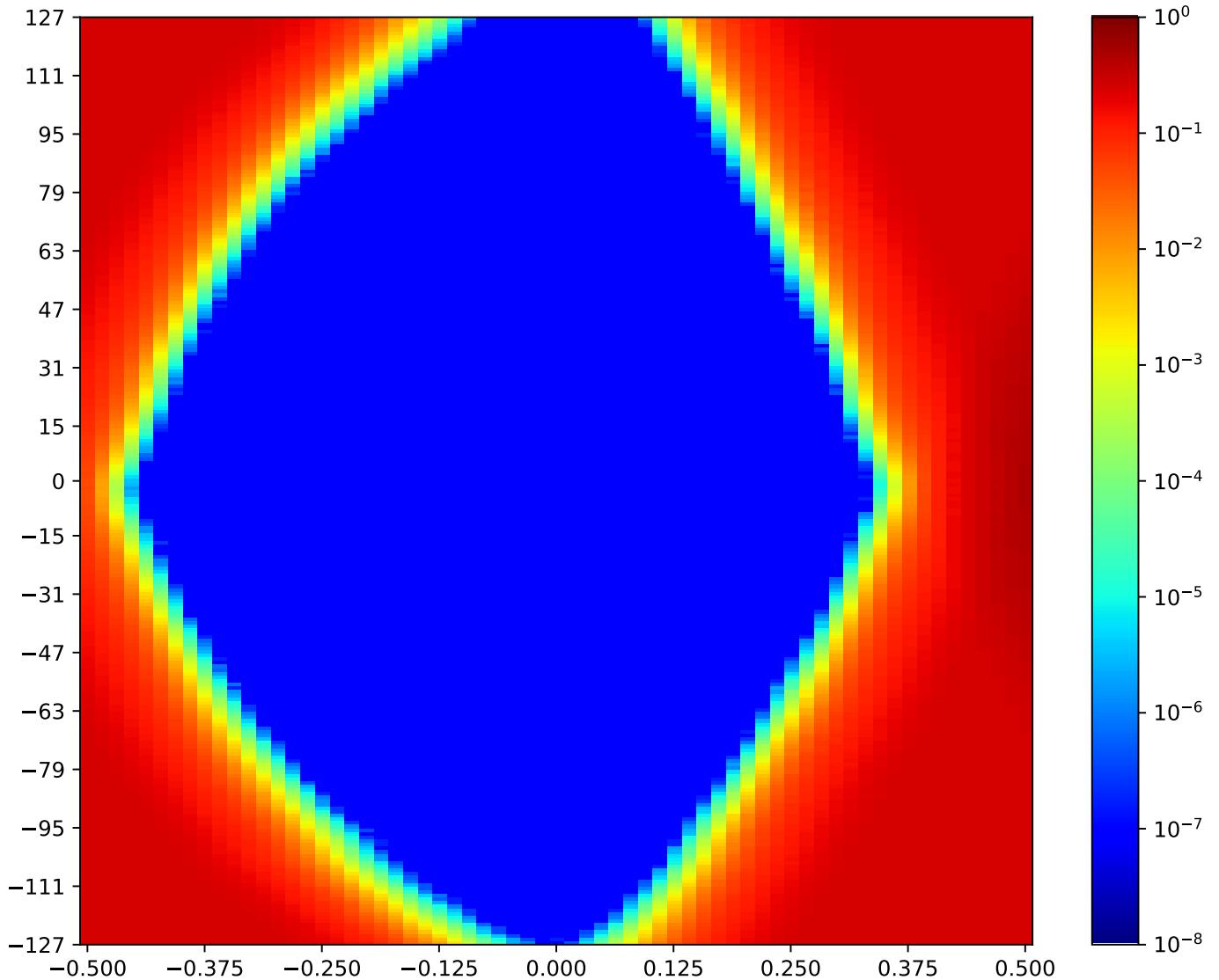


Figure 3.101: MSP\_C\_FPGA-IC39-02-IC15-02-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.4 MSP\_C\_FPGA-IC39-03-IC15-03-TRP\_FPGA

Table 3.93: MSP\_C\_FPGA-IC39-03-IC15-03-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:00:55		2018-Jan-24 00:01:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8849	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

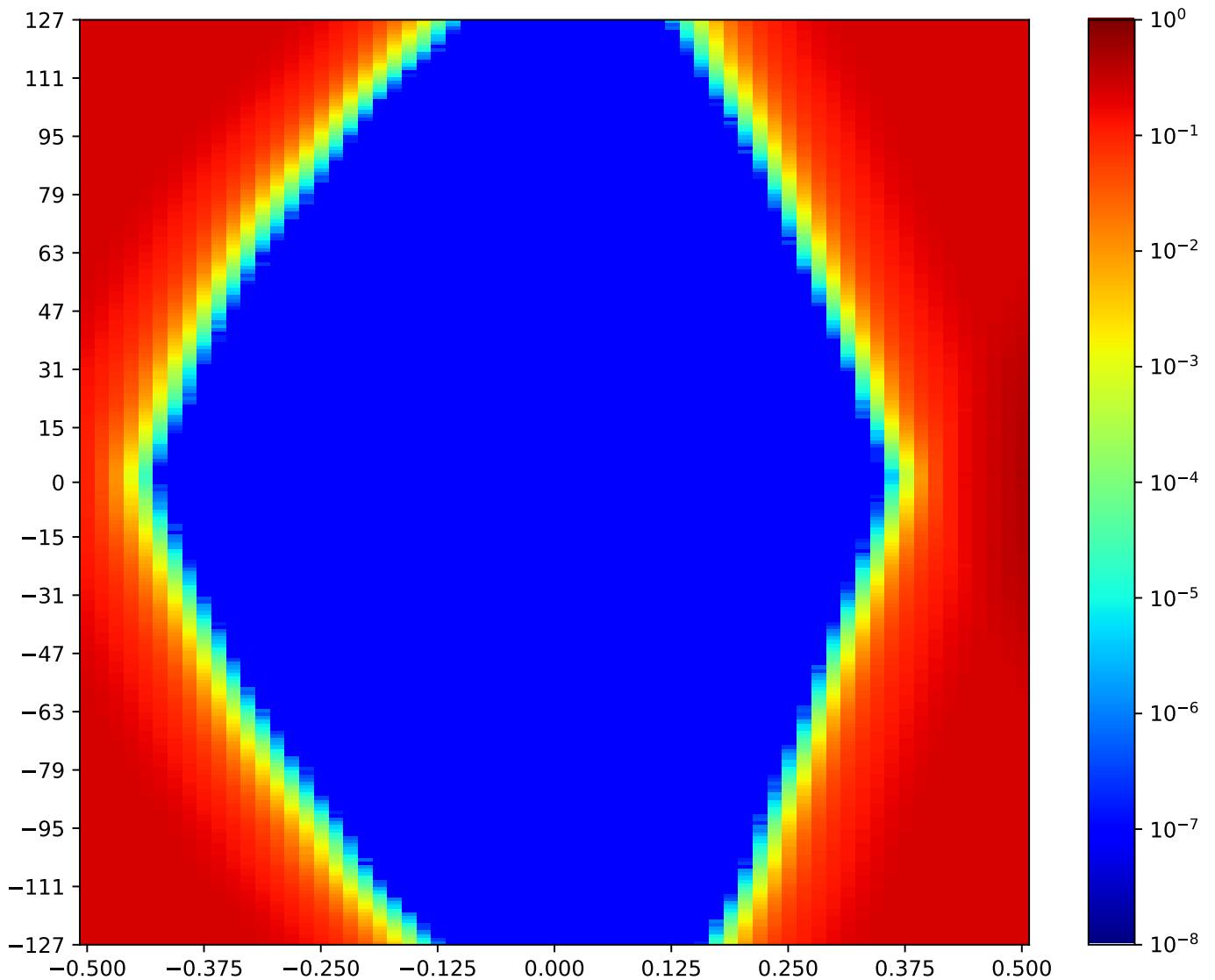


Figure 3.102: MSP\_C\_FPGA-IC39-03-IC15-03-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.5 MSP\_C\_FPGA-IC39-04-IC15-04-TRP\_FPGA

Table 3.94: MSP\_C\_FPGA-IC39-04-IC15-04-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:01:15		2018-Jan-24 00:01:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8153	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

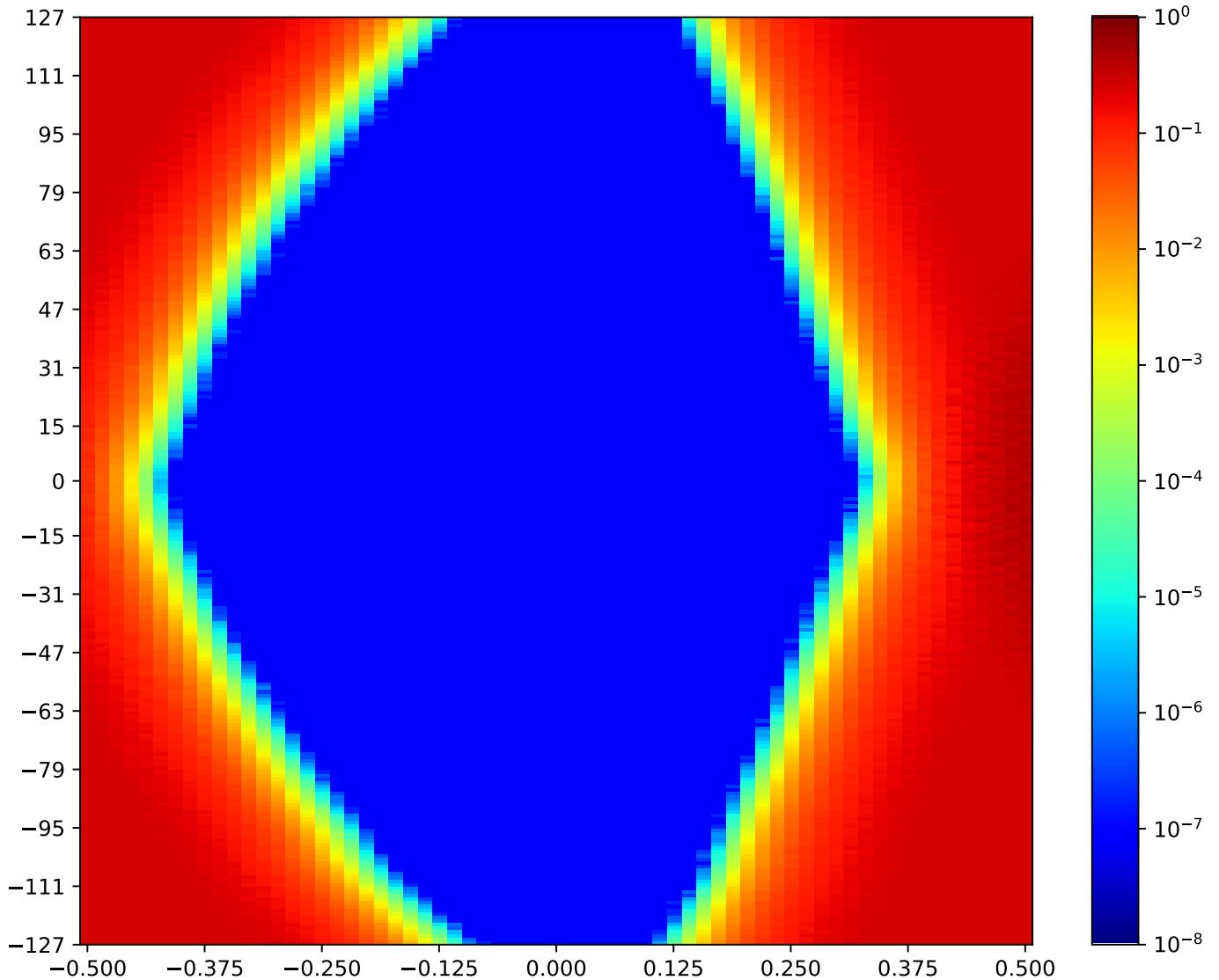


Figure 3.103: MSP\_C\_FPGA-IC39-04-IC15-04-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.6 MSP\_C\_FPGA-IC39-05-IC15-05-TRP\_FPGA

Table 3.95: MSP\_C\_FPGA-IC39-05-IC15-05-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:01:36		2018-Jan-24 00:01:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8441	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

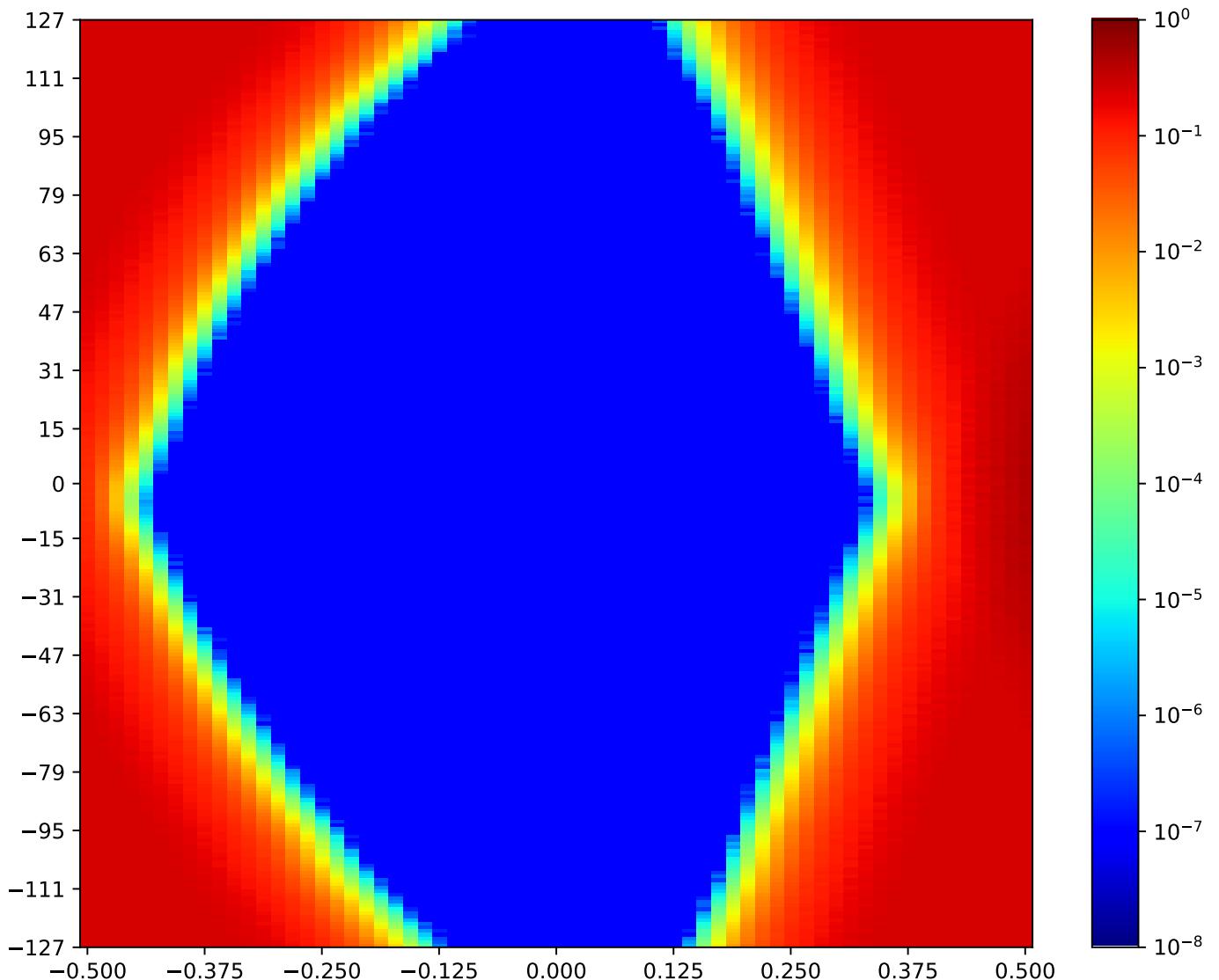


Figure 3.104: MSP\_C\_FPGA-IC39-05-IC15-05-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.7 MSP\_C\_FPGA-IC39-06-IC15-06-TRP\_FPGA

Table 3.96: MSP\_C\_FPGA-IC39-06-IC15-06-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:01:57		2018-Jan-24 00:02:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8404	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

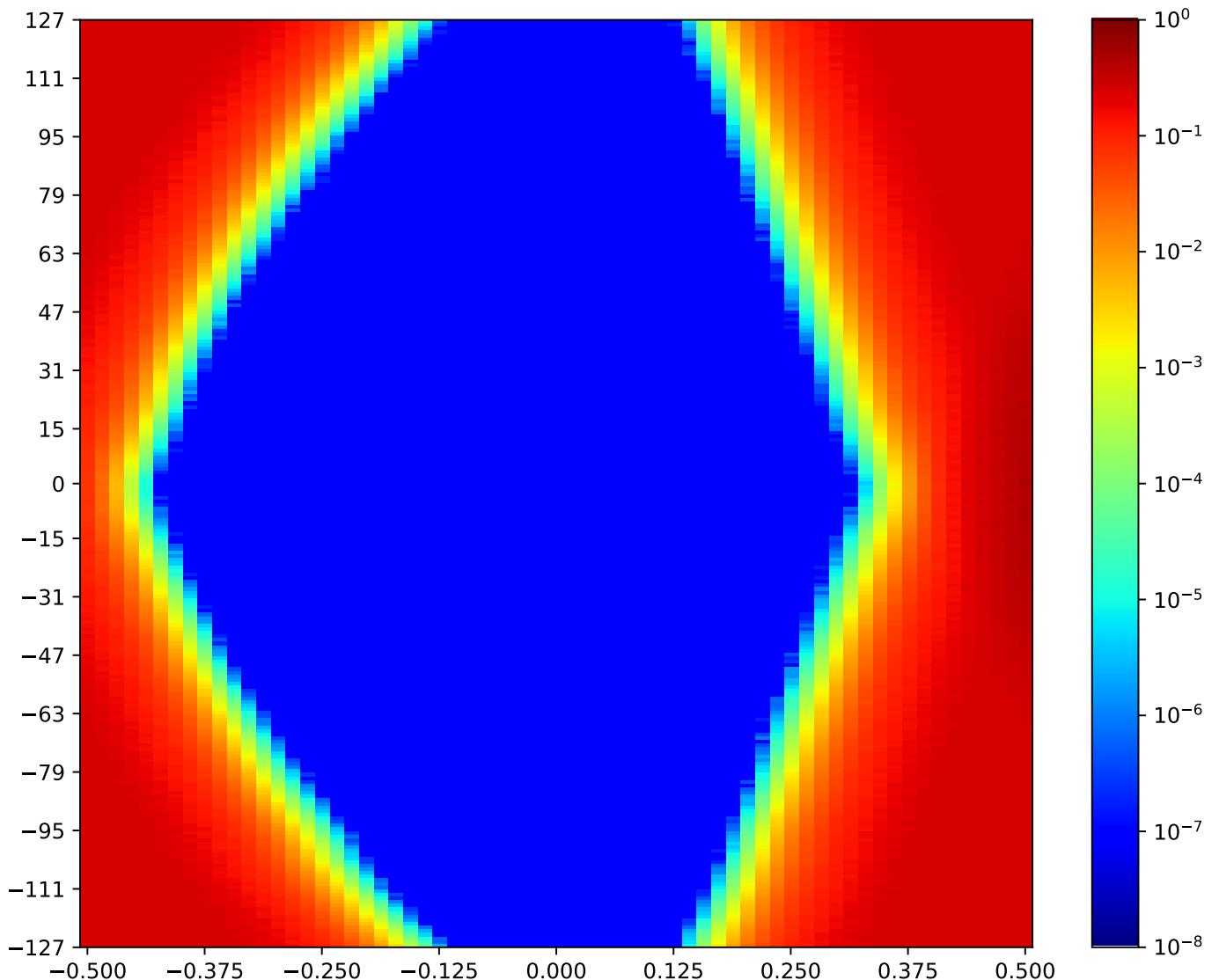


Figure 3.105: MSP\_C\_FPGA-IC39-06-IC15-06-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.8 MSP\_C\_FPGA-IC39-07-IC15-07-TRP\_FPGA

Table 3.97: MSP\_C\_FPGA-IC39-07-IC15-07-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:02:17		2018-Jan-24 00:02:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8945	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

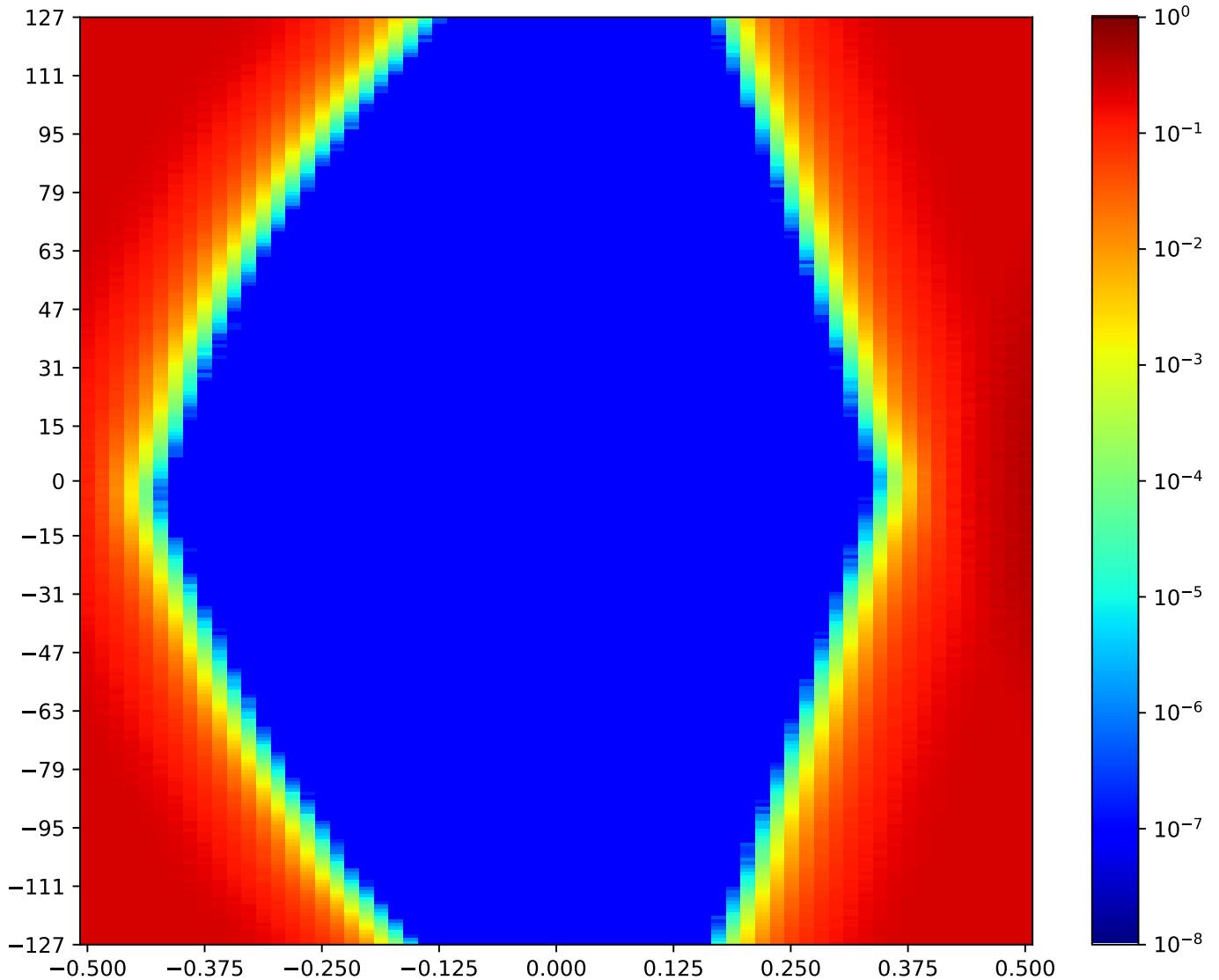


Figure 3.106: MSP\_C\_FPGA-IC39-07-IC15-07-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.9 MSP\_C\_FPGA-IC39-08-IC15-08-TRP\_FPGA

Table 3.98: MSP\_C\_FPGA-IC39-08-IC15-08-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:02:38		2018-Jan-24 00:02:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8660	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

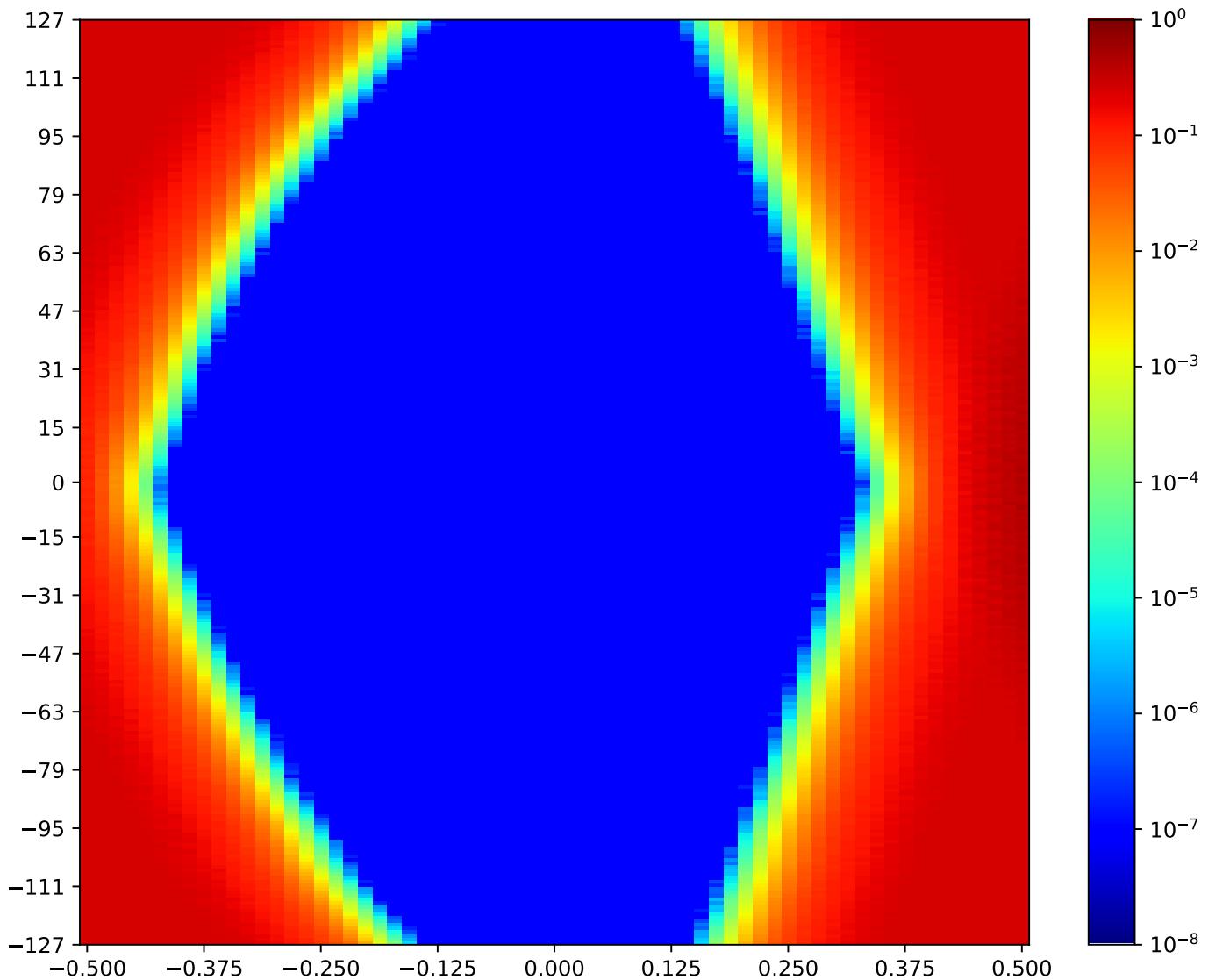


Figure 3.107: MSP\_C\_FPGA-IC39-08-IC15-08-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.10 MSP\_C\_FPGA-IC39-09-IC15-09-TRP\_FPGA

Table 3.99: MSP\_C\_FPGA-IC39-09-IC15-09-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:02:58		2018-Jan-24 00:03:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8523	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

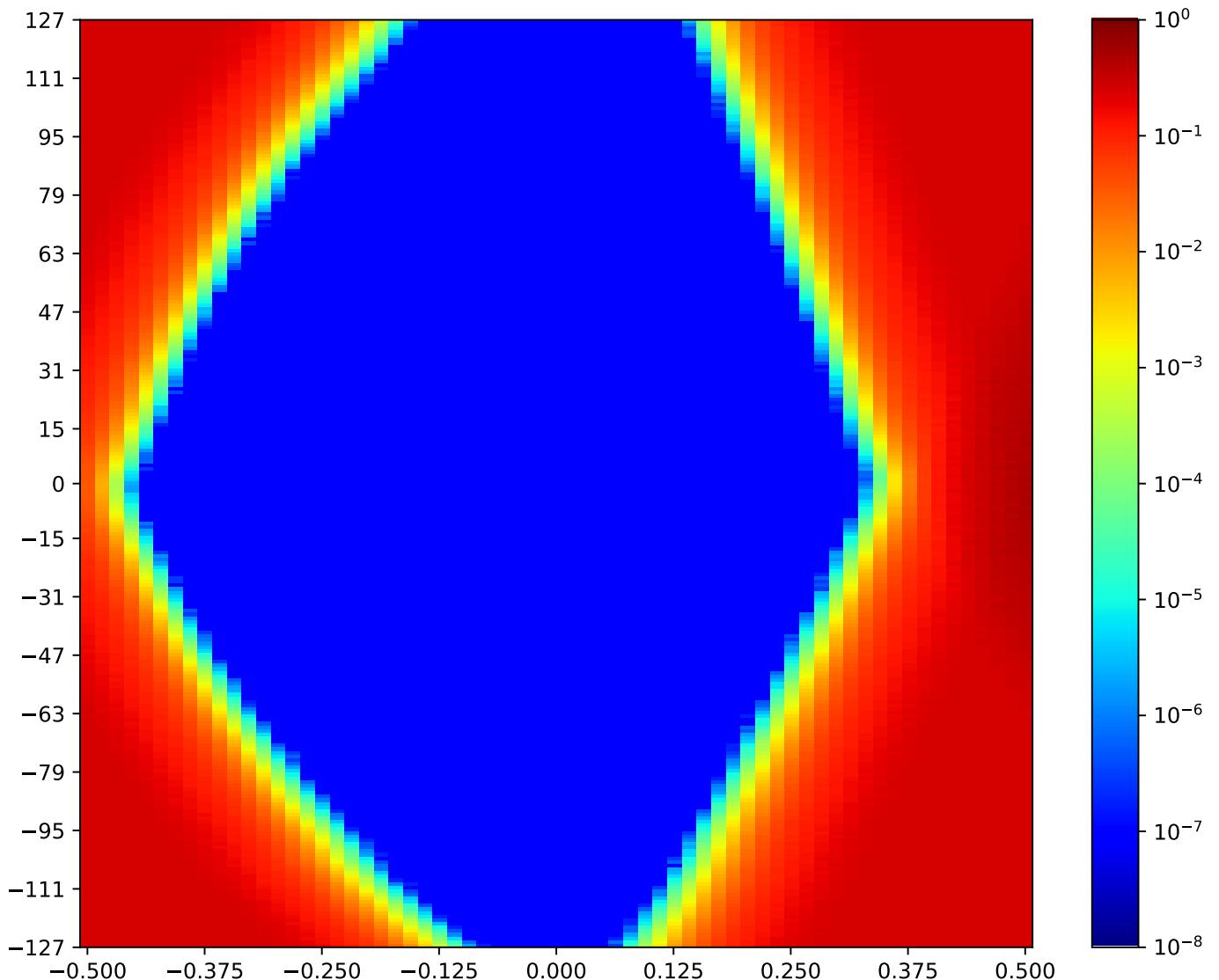


Figure 3.108: MSP\_C\_FPGA-IC39-09-IC15-09-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.11 MSP\_C\_FPGA-IC39-10-IC15-10-TRP\_FPGA

Table 3.100: MSP\_C\_FPGA-IC39-10-IC15-10-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:03:19		2018-Jan-24 00:03:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8845	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

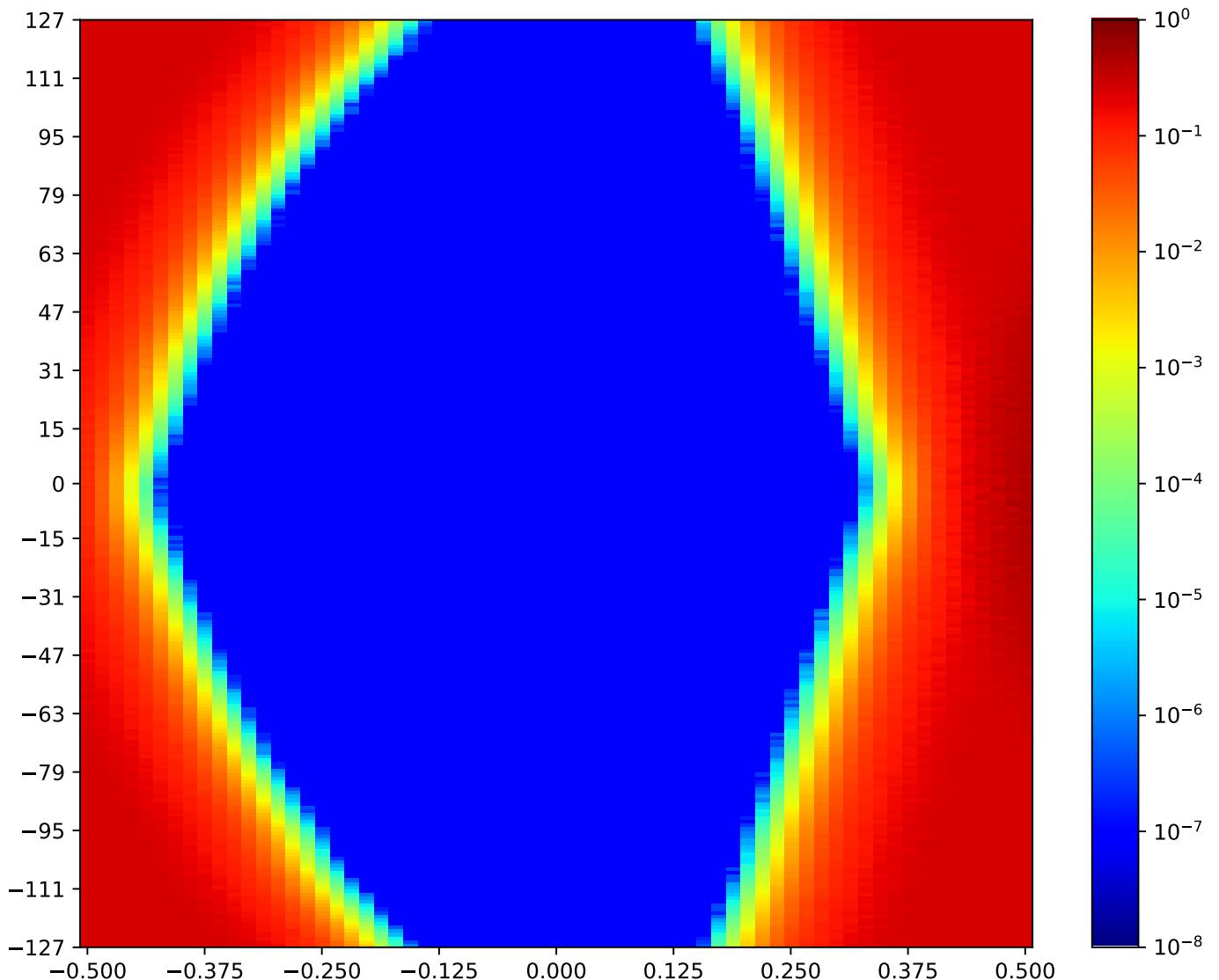


Figure 3.109: MSP\_C\_FPGA-IC39-10-IC15-10-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.12 MSP\_C\_FPGA-IC39-11-IC15-11-TRP\_FPGA

Table 3.101: MSP\_C\_FPGA-IC39-11-IC15-11-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:03:39		2018-Jan-24 00:04:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8967	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

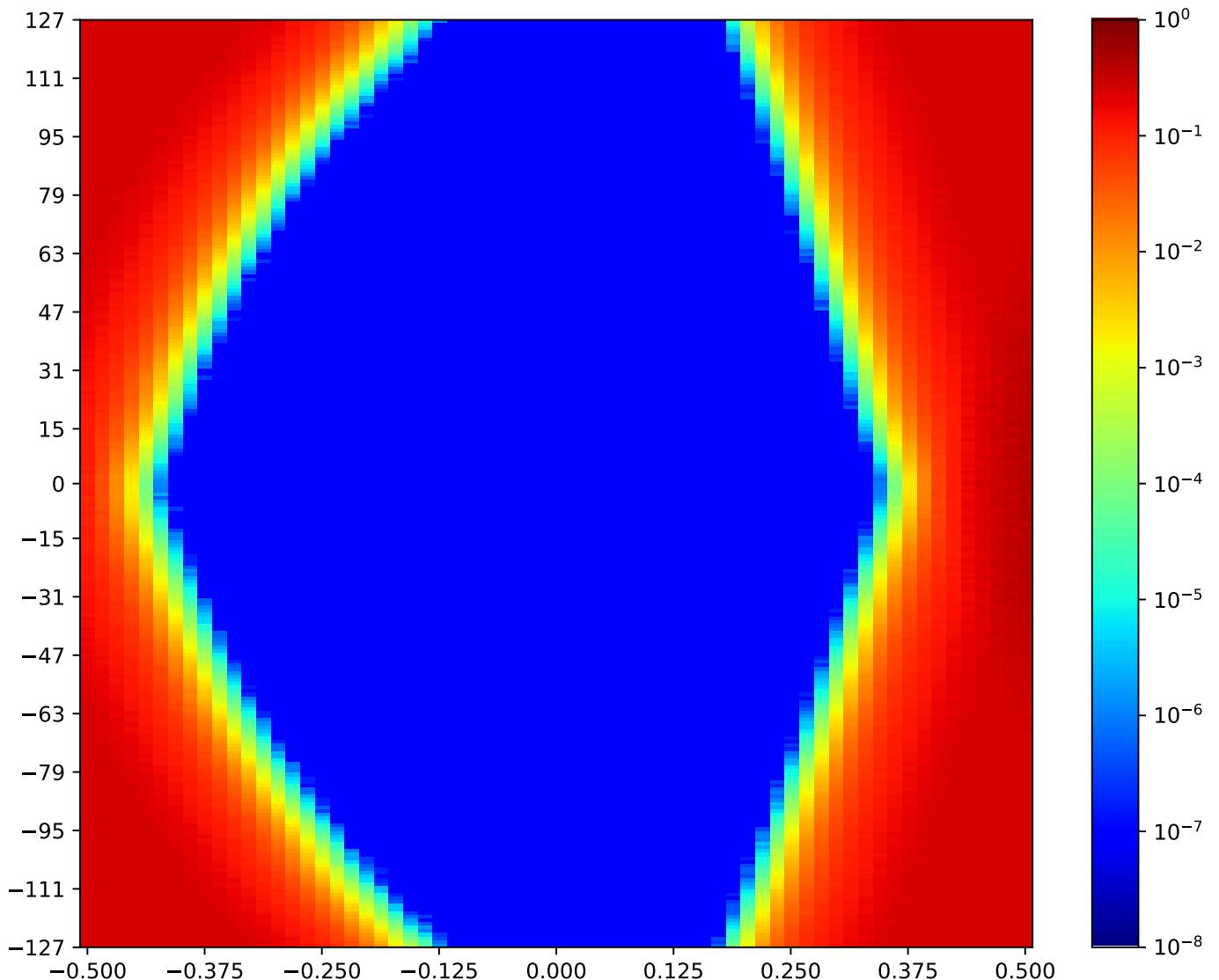


Figure 3.110: MSP\_C\_FPGA-IC39-11-IC15-11-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.13 MSP\_C\_FPGA-IC39-12-IC15-12-TRP\_FPGA

Table 3.102: MSP\_C\_FPGA-IC39-12-IC15-12-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:04:00		2018-Jan-24 00:04:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9229	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

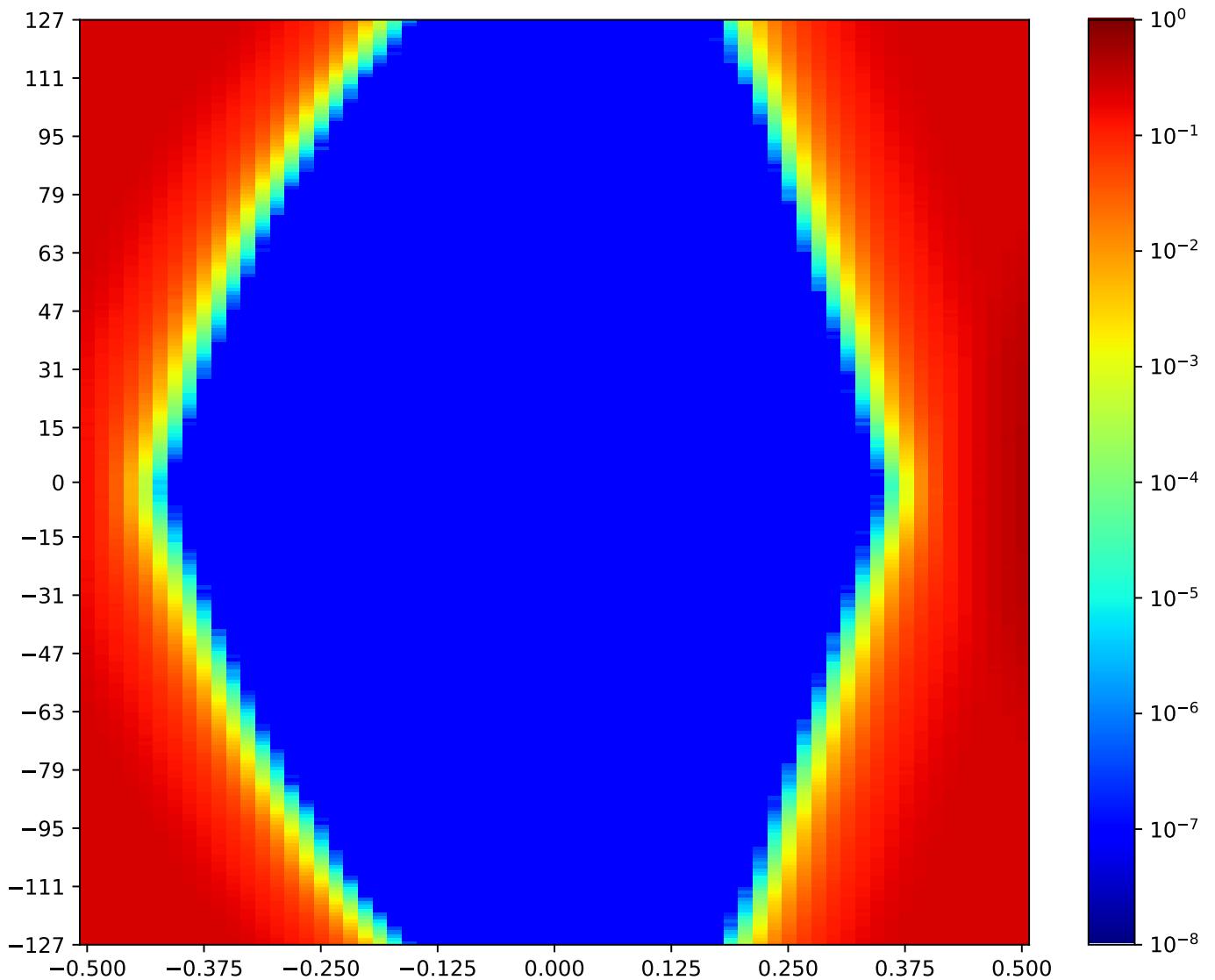


Figure 3.111: MSP\_C\_FPGA-IC39-12-IC15-12-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.14 MSP\_C\_FPGA-IC39-13-IC15-13-TRP\_FPGA

Table 3.103: MSP\_C\_FPGA-IC39-13-IC15-13-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:04:21		2018-Jan-24 00:04:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9284	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

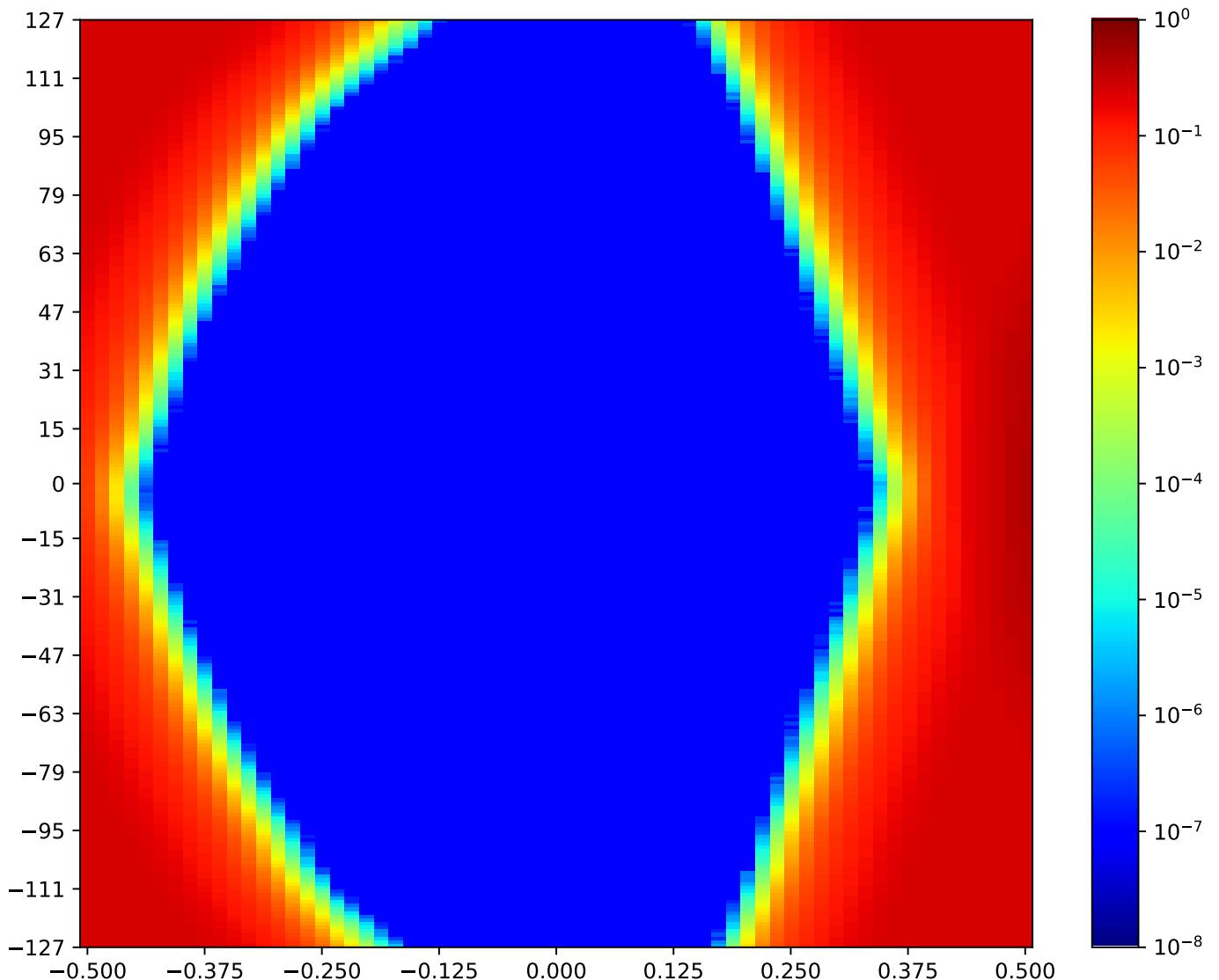


Figure 3.112: MSP\_C\_FPGA-IC39-13-IC15-13-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.15 MSP\_C\_FPGA-IC39-14-IC15-14-TRP\_FPGA

Table 3.104: MSP\_C\_FPGA-IC39-14-IC15-14-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:04:41		2018-Jan-24 00:05:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8387	47	72.31%	255	100.00%
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BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

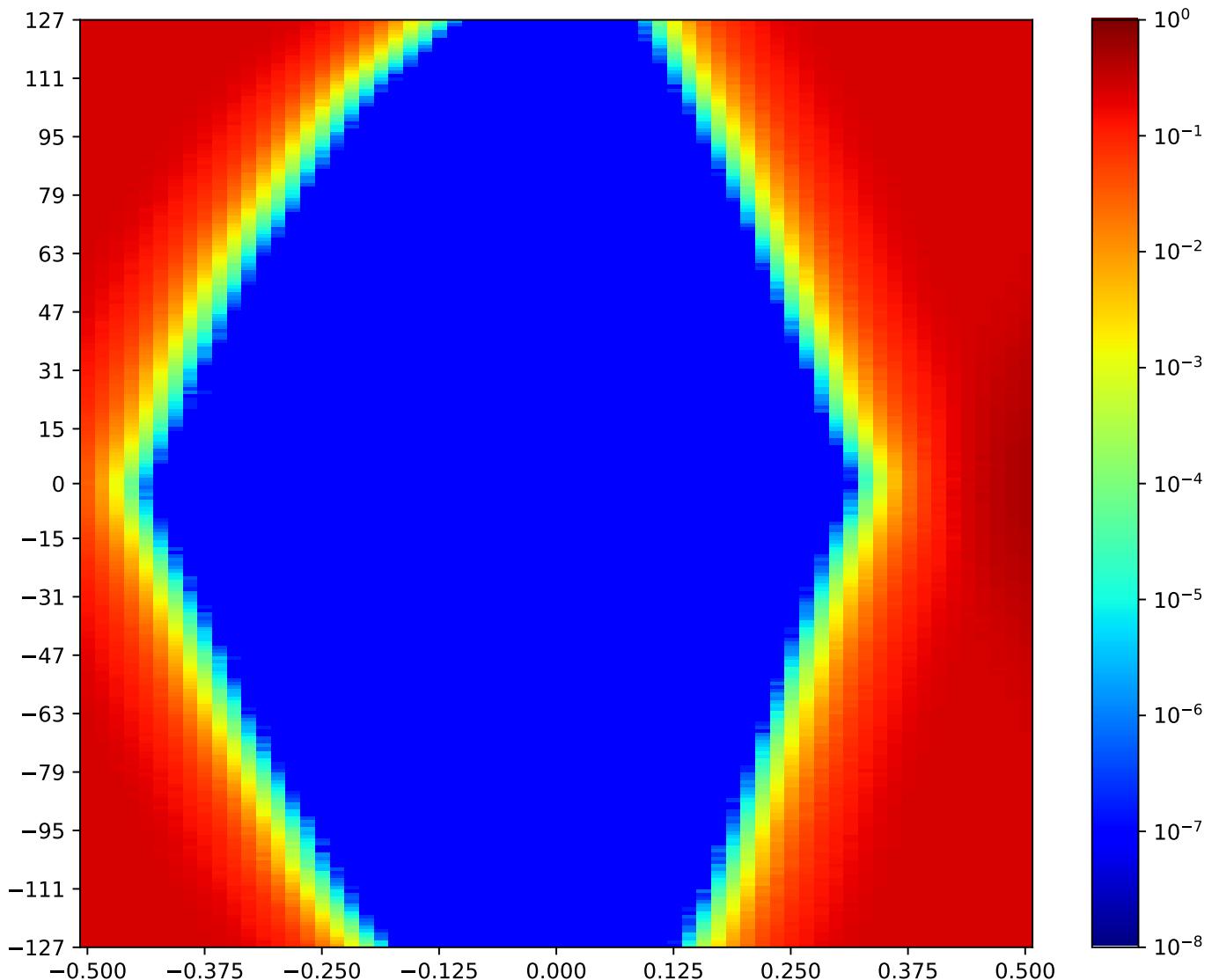


Figure 3.113: MSP\_C\_FPGA-IC39-14-IC15-14-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.16 MSP\_C\_FPGA-IC39-15-IC15-15-TRP\_FPGA

Table 3.105: MSP\_C\_FPGA-IC39-15-IC15-15-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:05:02		2018-Jan-24 00:05:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9189	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

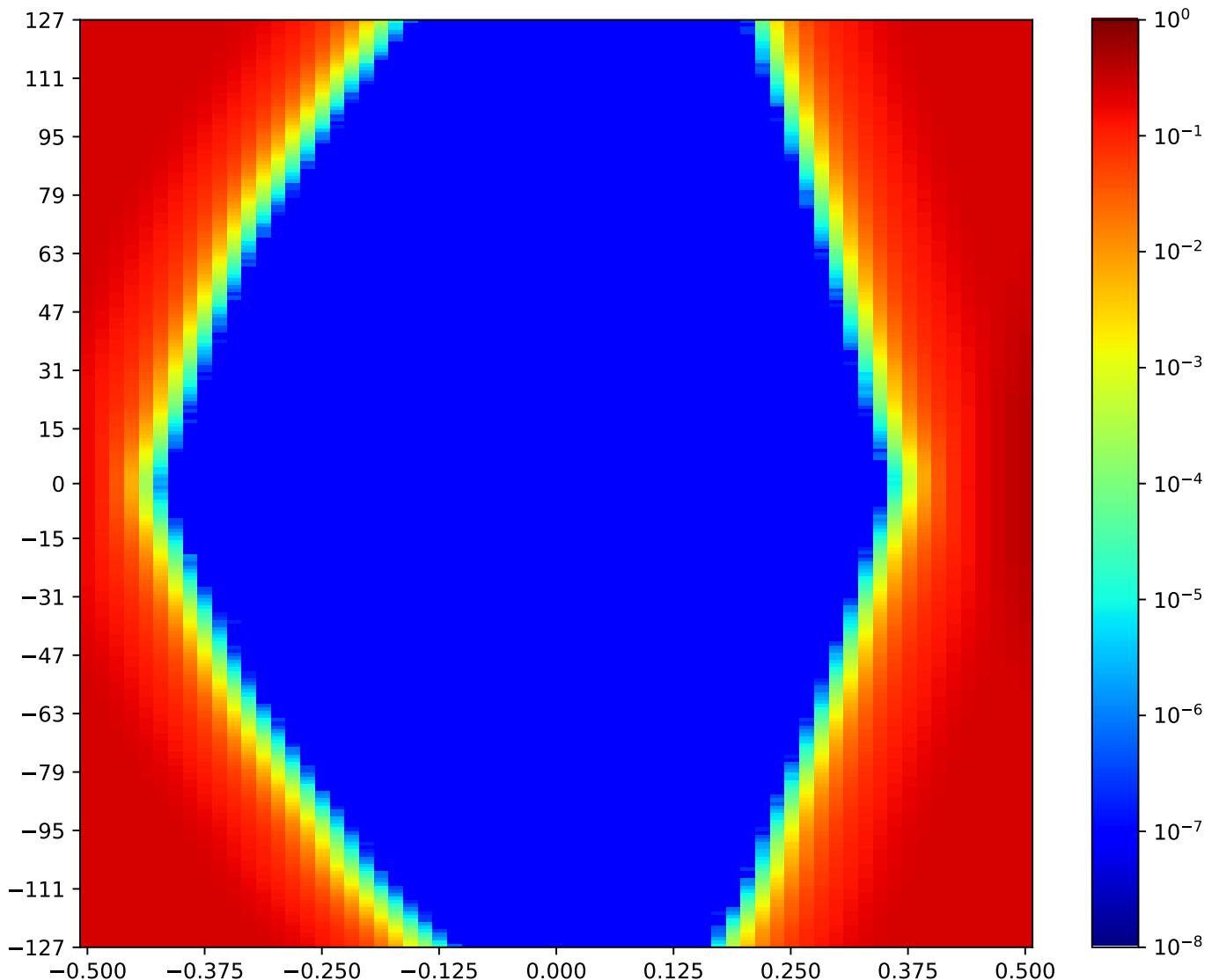


Figure 3.114: MSP\_C\_FPGA-IC39-15-IC15-15-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.17 MSP\_C\_FPGA-IC39-16-IC15-16-TRP\_FPGA

Table 3.106: MSP\_C\_FPGA-IC39-16-IC15-16-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:05:23		2018-Jan-24 00:05:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8458	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

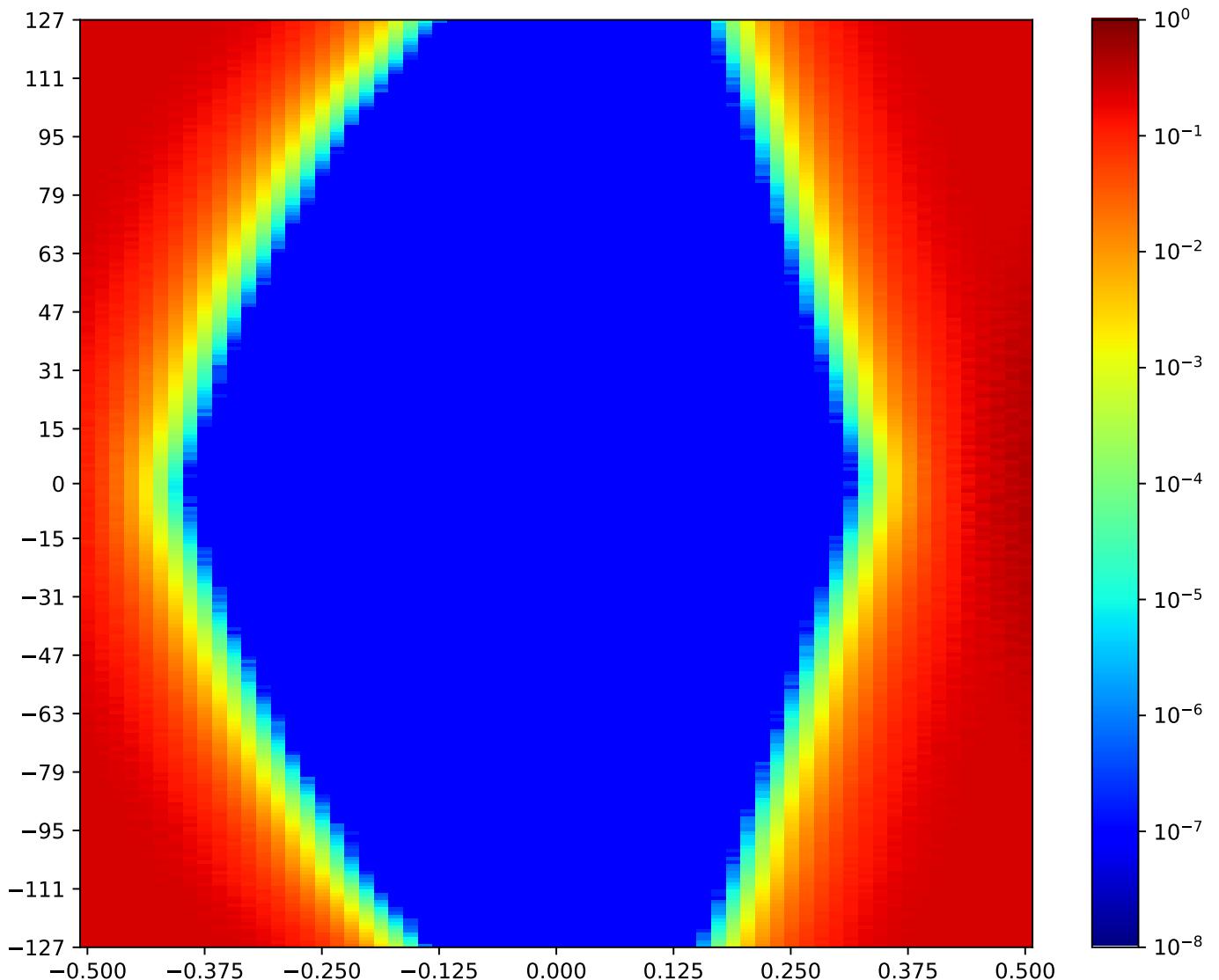


Figure 3.115: MSP\_C\_FPGA-IC39-16-IC15-16-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.18 MSP\_C\_FPGA-IC39-17-IC15-17-TRP\_FPGA

Table 3.107: MSP\_C\_FPGA-IC39-17-IC15-17-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:05:43		2018-Jan-24 00:06:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8769	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

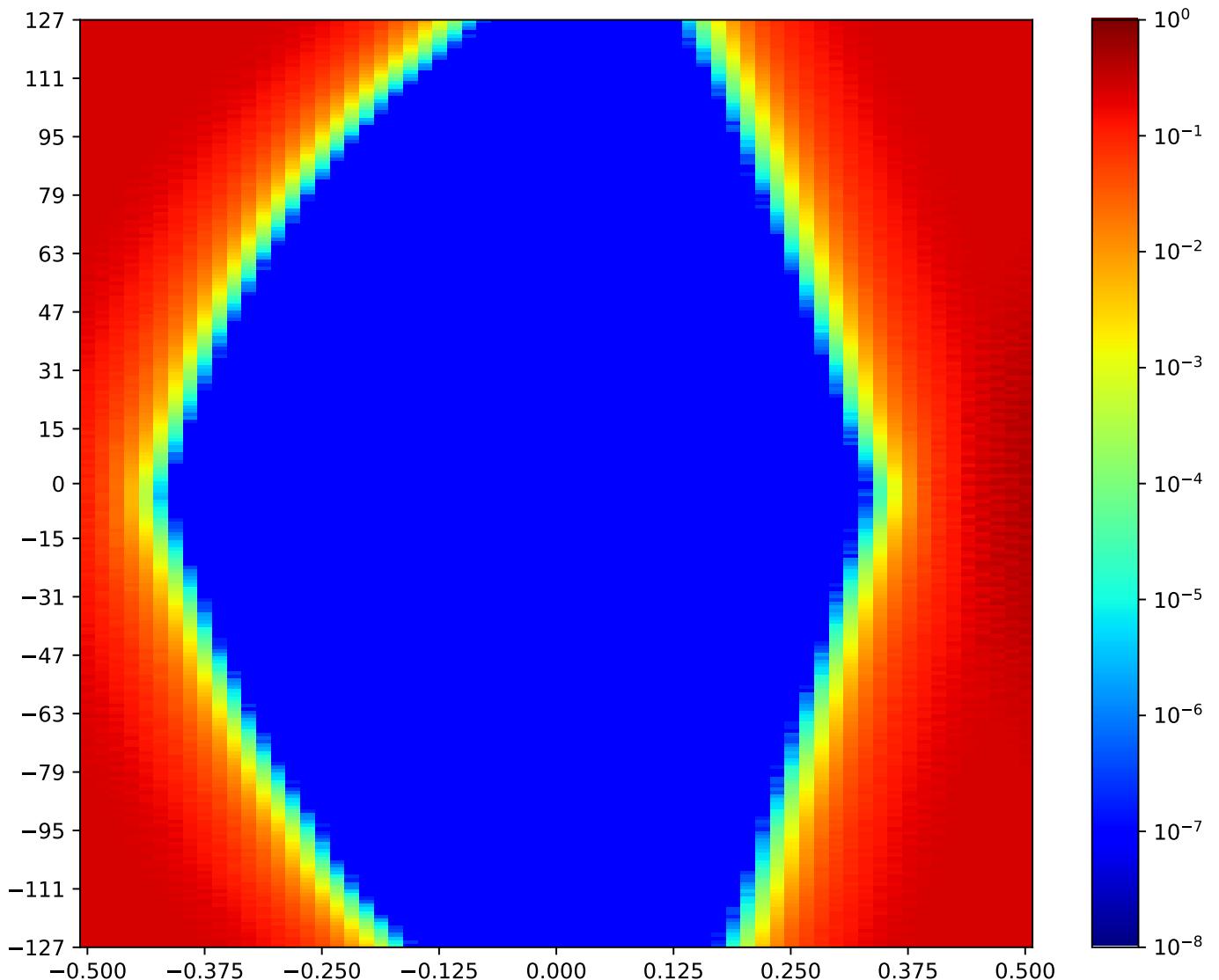


Figure 3.116: MSP\_C\_FPGA-IC39-17-IC15-17-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.19 MSP\_C\_FPGA-IC39-18-IC15-18-TRP\_FPGA

Table 3.108: MSP\_C\_FPGA-IC39-18-IC15-18-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:06:04		2018-Jan-24 00:06:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9060	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

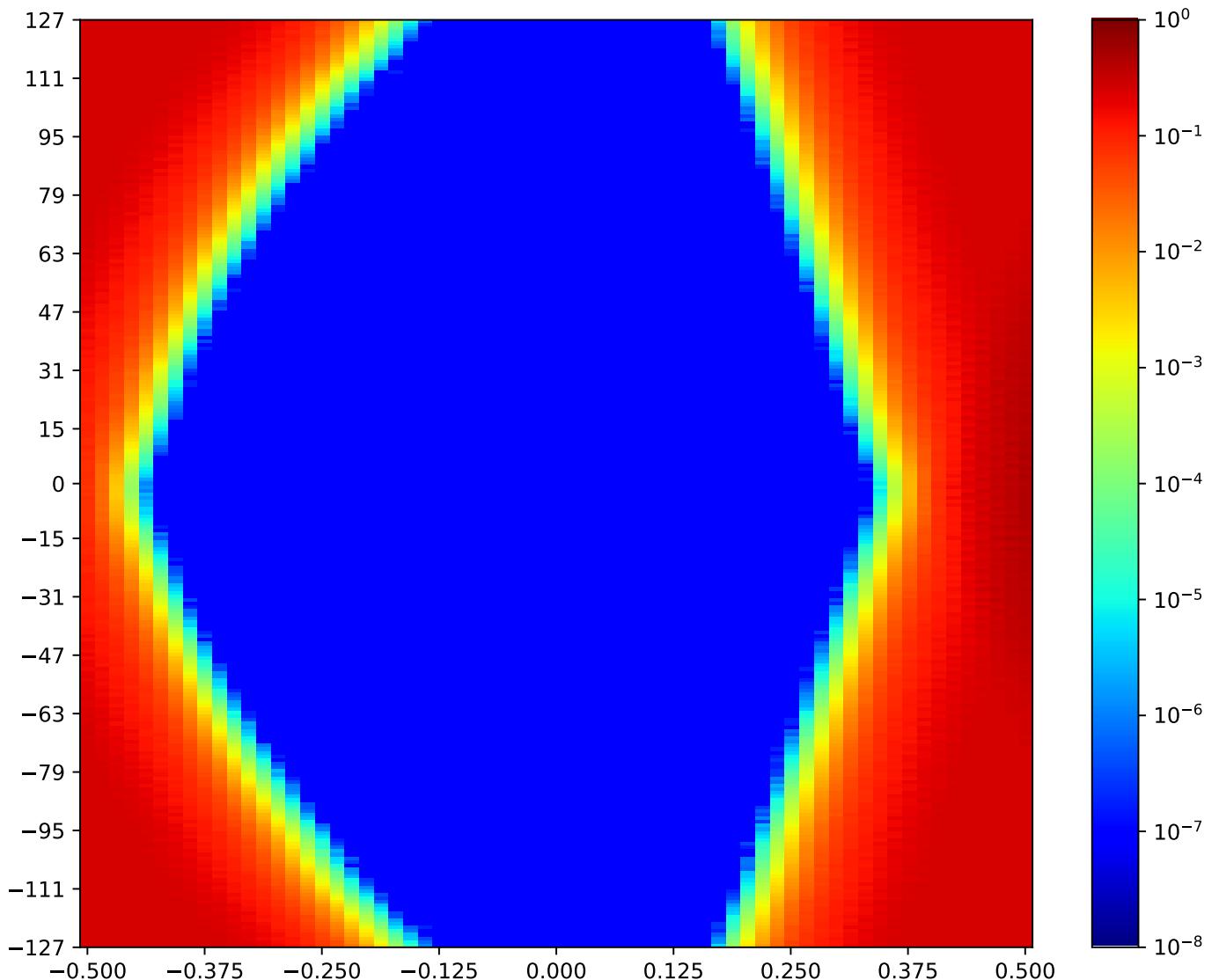


Figure 3.117: MSP\_C\_FPGA-IC39-18-IC15-18-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.20 MSP\_C\_FPGA-IC39-19-IC15-19-TRP\_FPGA

Table 3.109: MSP\_C\_FPGA-IC39-19-IC15-19-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:06:24		2018-Jan-24 00:06:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8752	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

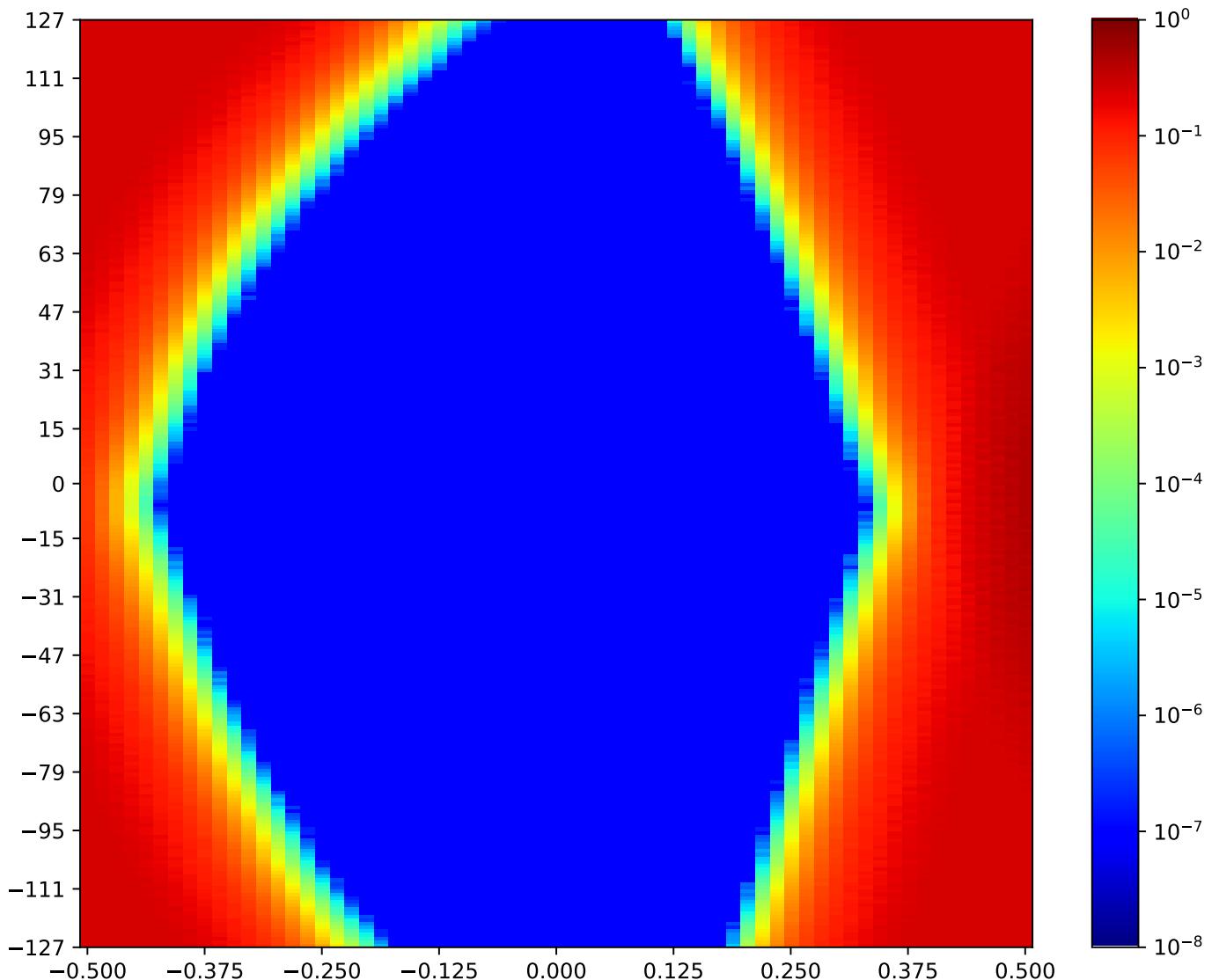


Figure 3.118: MSP\_C\_FPGA-IC39-19-IC15-19-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.21 MSP\_C\_FPGA-IC39-20-IC15-20-TRP\_FPGA

Table 3.110: MSP\_C\_FPGA-IC39-20-IC15-20-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:06:45		2018-Jan-24 00:07:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8468	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

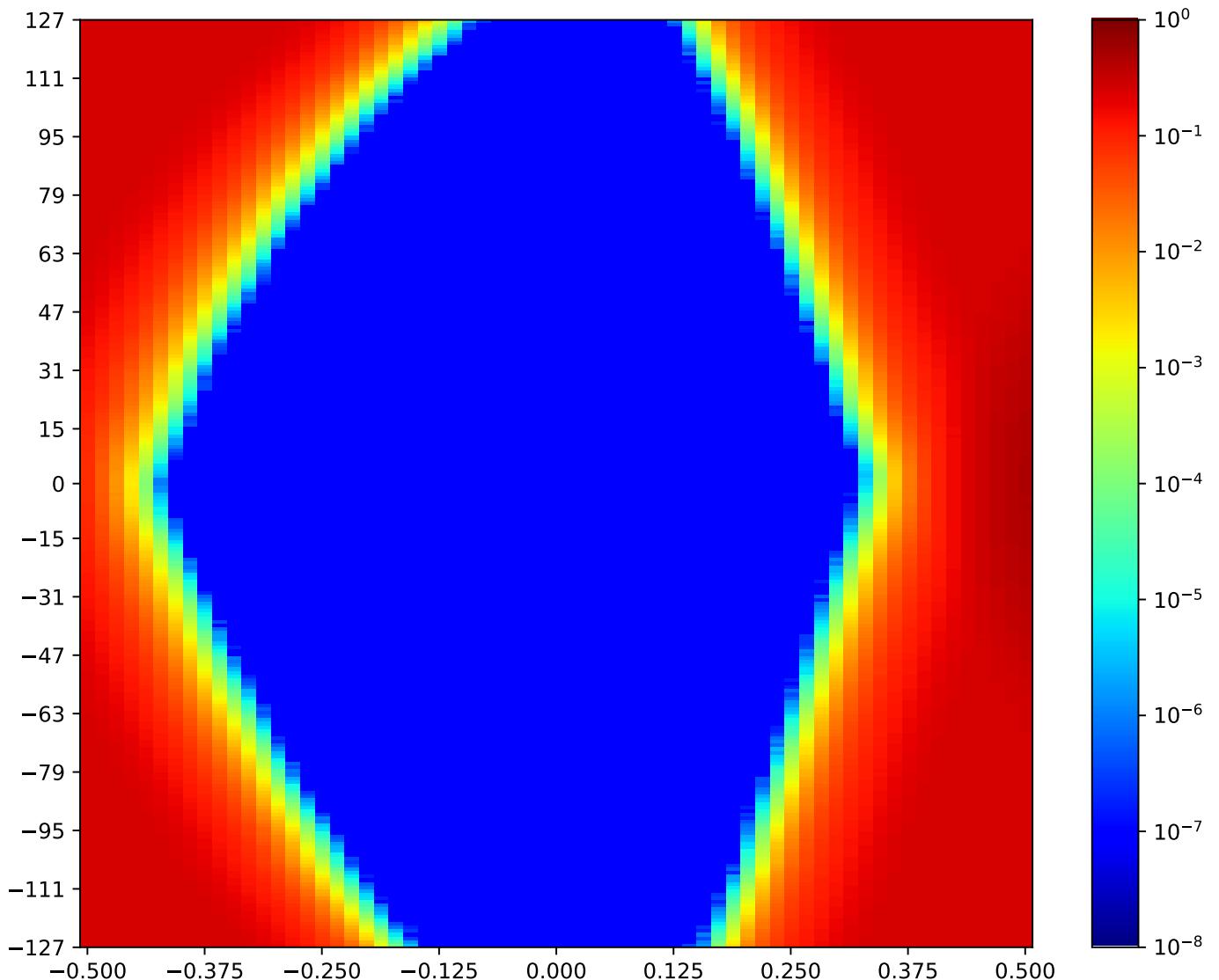


Figure 3.119: MSP\_C\_FPGA-IC39-20-IC15-20-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.22 MSP\_C\_FPGA-IC39-21-IC15-21-TRP\_FPGA

Table 3.111: MSP\_C\_FPGA-IC39-21-IC15-21-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:07:06		2018-Jan-24 00:07:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9158	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

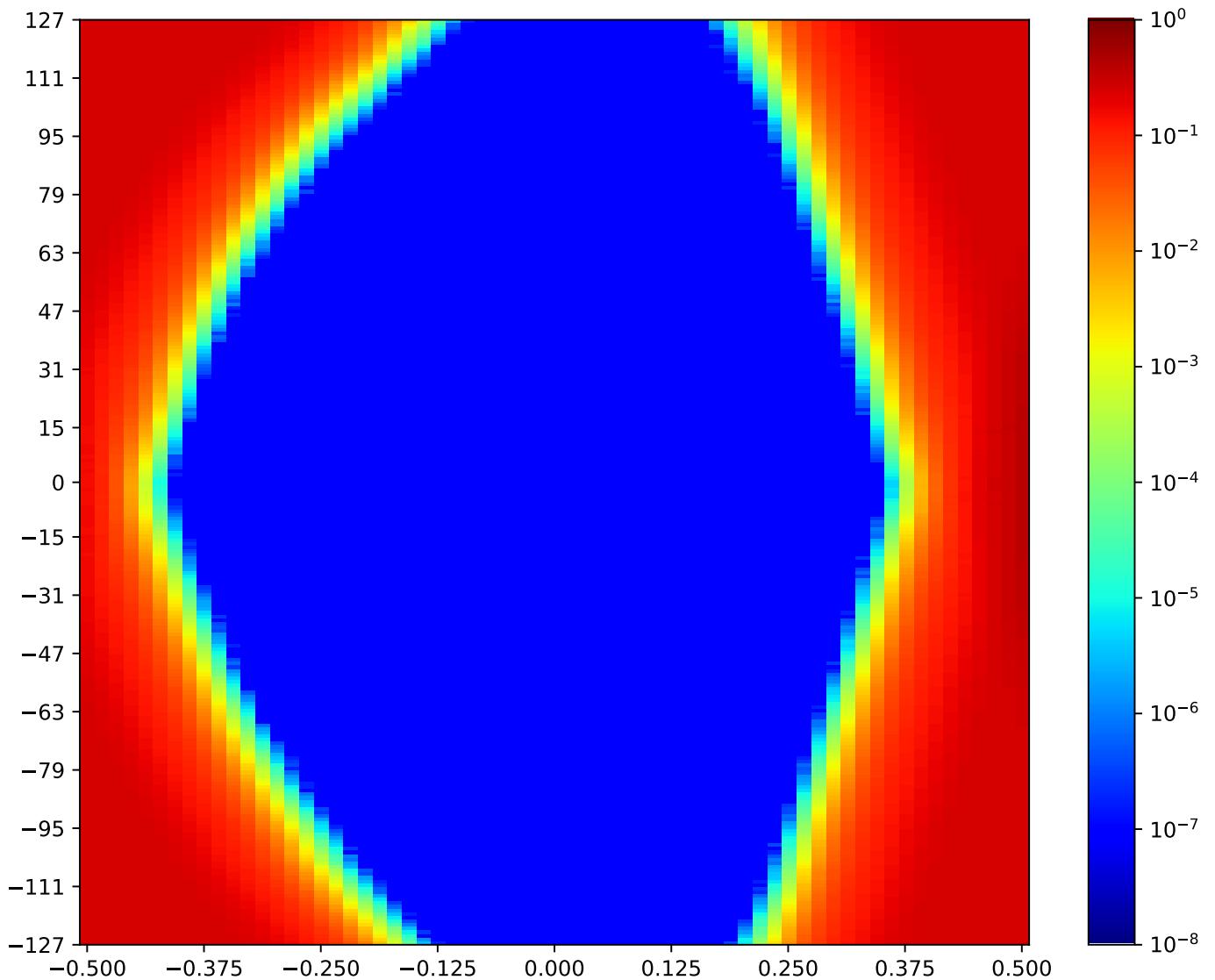


Figure 3.120: MSP\_C\_FPGA-IC39-21-IC15-21-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.23 MSP\_C\_FPGA-IC39-22-IC15-22-TRP\_FPGA

Table 3.112: MSP\_C\_FPGA-IC39-22-IC15-22-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:07:26		2018-Jan-24 00:07:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9139	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

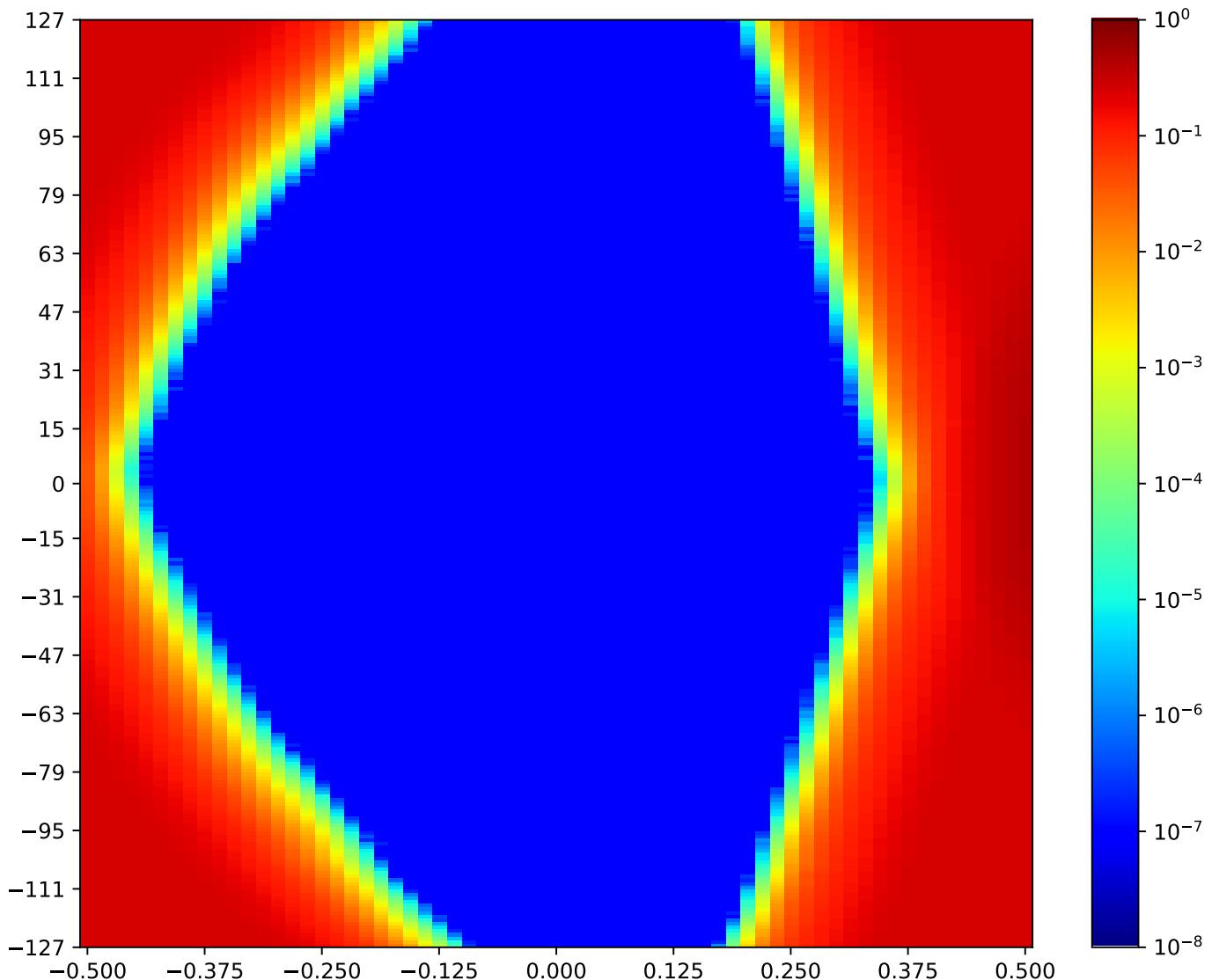


Figure 3.121: MSP\_C\_FPGA-IC39-22-IC15-22-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.24 MSP\_C\_FPGA-IC39-23-IC15-23-TRP\_FPGA

Table 3.113: MSP\_C\_FPGA-IC39-23-IC15-23-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:07:46		2018-Jan-24 00:08:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9312	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

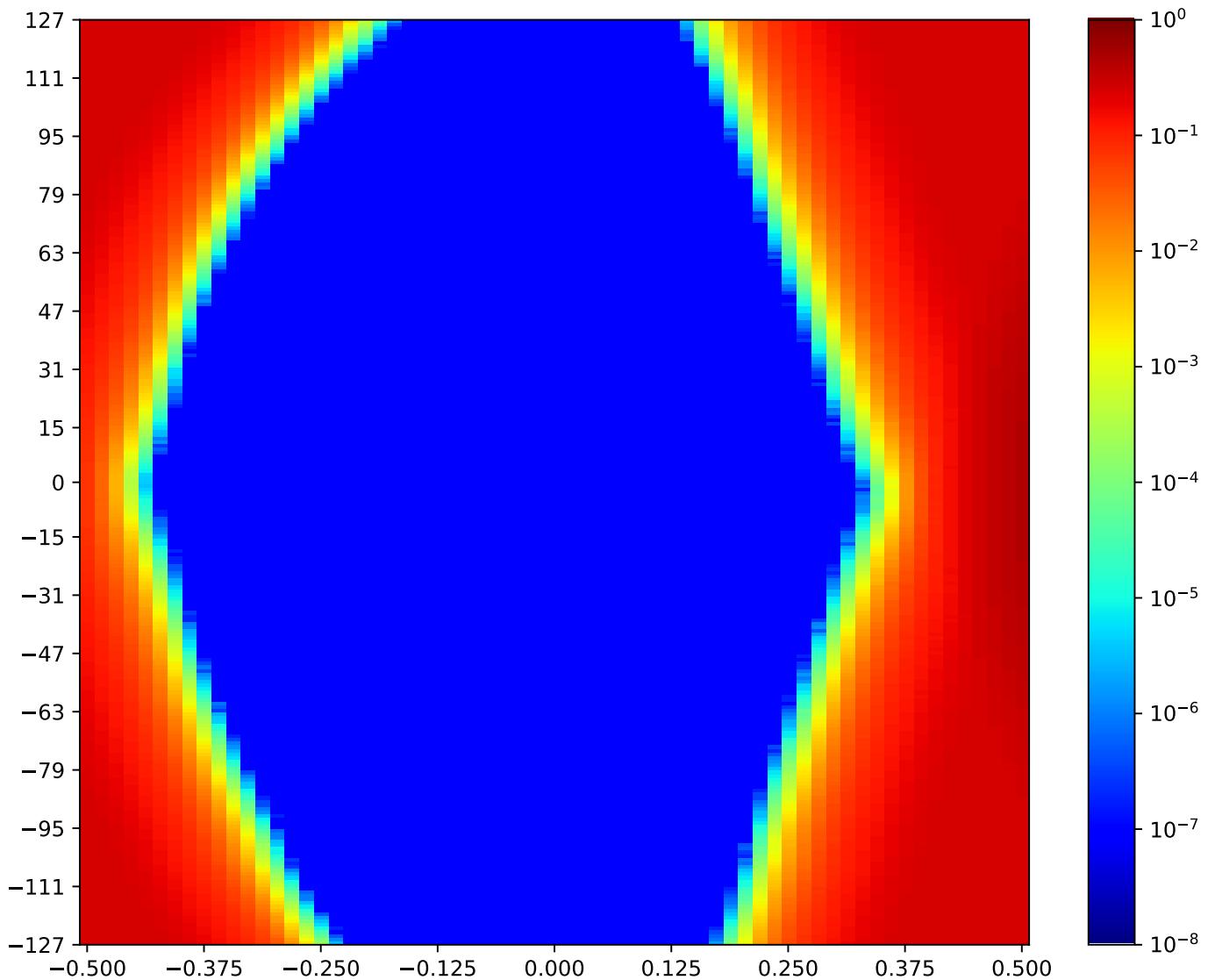


Figure 3.122: MSP\_C\_FPGA-IC39-23-IC15-23-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.25 MSP\_C\_FPGA-IC39-24-IC15-24-TRP\_FPGA

Table 3.114: MSP\_C\_FPGA-IC39-24-IC15-24-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:08:07		2018-Jan-24 00:08:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8866	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

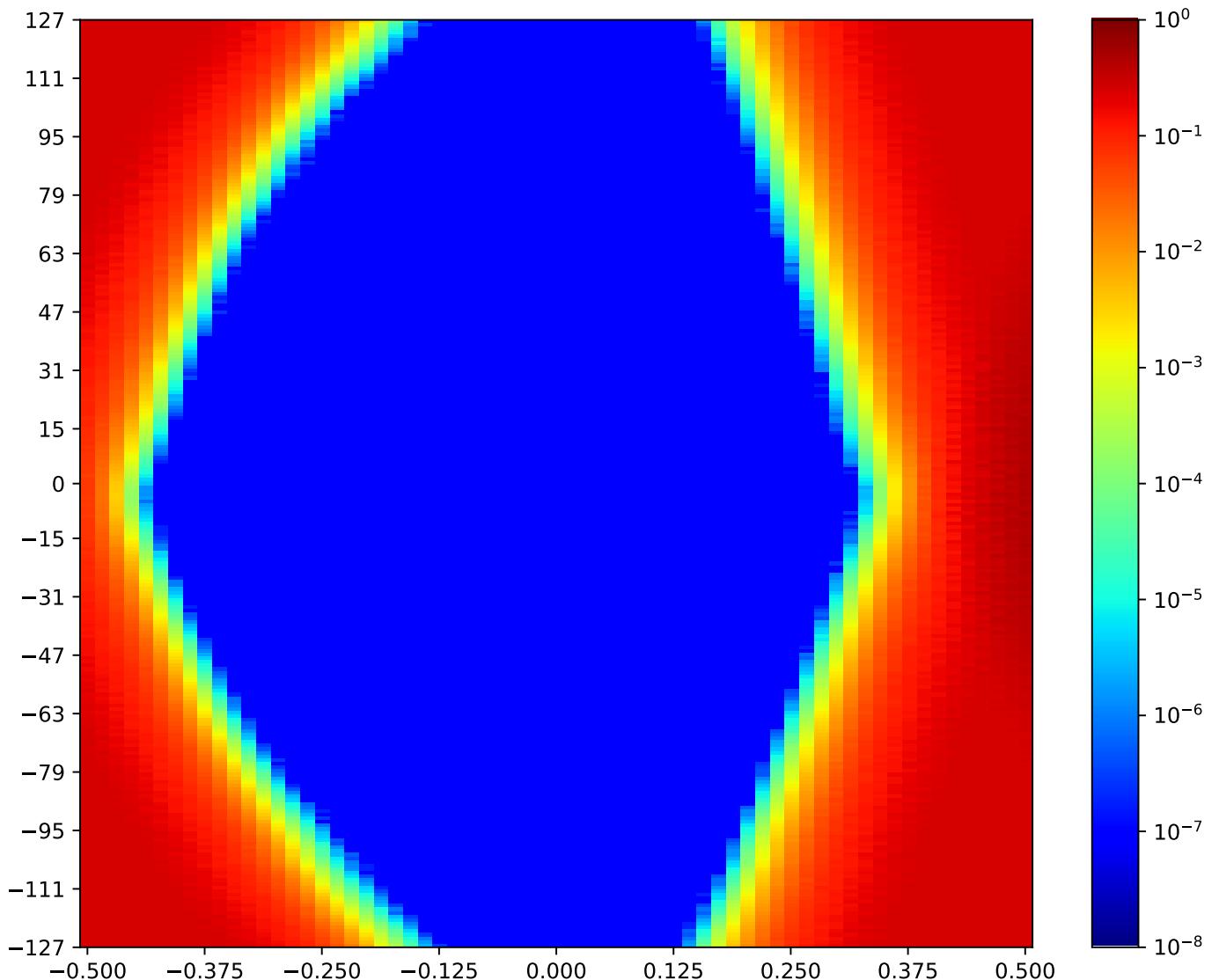


Figure 3.123: MSP\_C\_FPGA-IC39-24-IC15-24-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.26 MSP\_C\_FPGA-IC39-25-IC15-25-TRP\_FPGA

Table 3.115: MSP\_C\_FPGA-IC39-25-IC15-25-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:08:27		2018-Jan-24 00:08:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8985	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

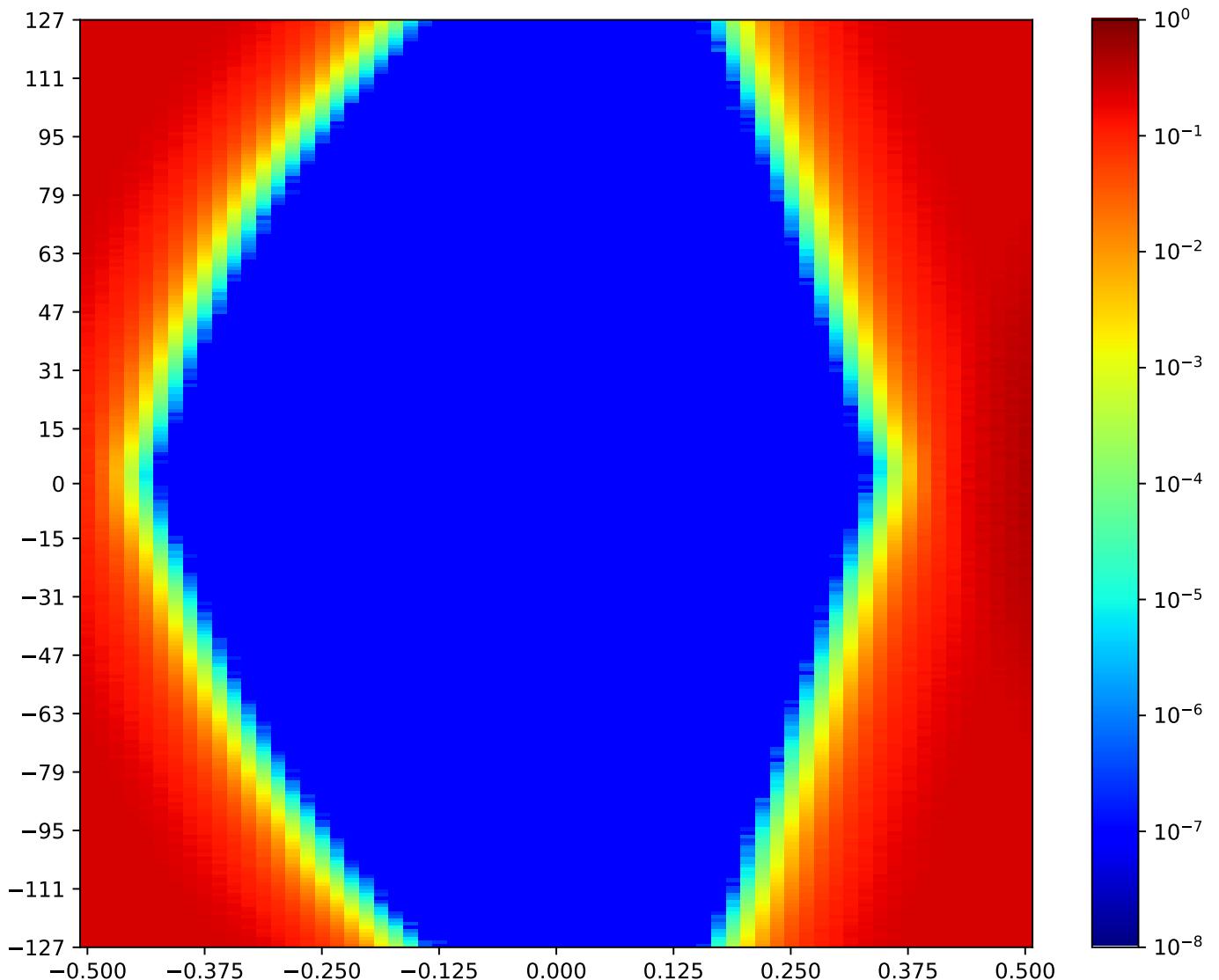


Figure 3.124: MSP\_C\_FPGA-IC39-25-IC15-25-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.27 MSP\_C\_FPGA-IC39-26-IC15-26-TRP\_FPGA

Table 3.116: MSP\_C\_FPGA-IC39-26-IC15-26-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:08:48		2018-Jan-24 00:09:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8382	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

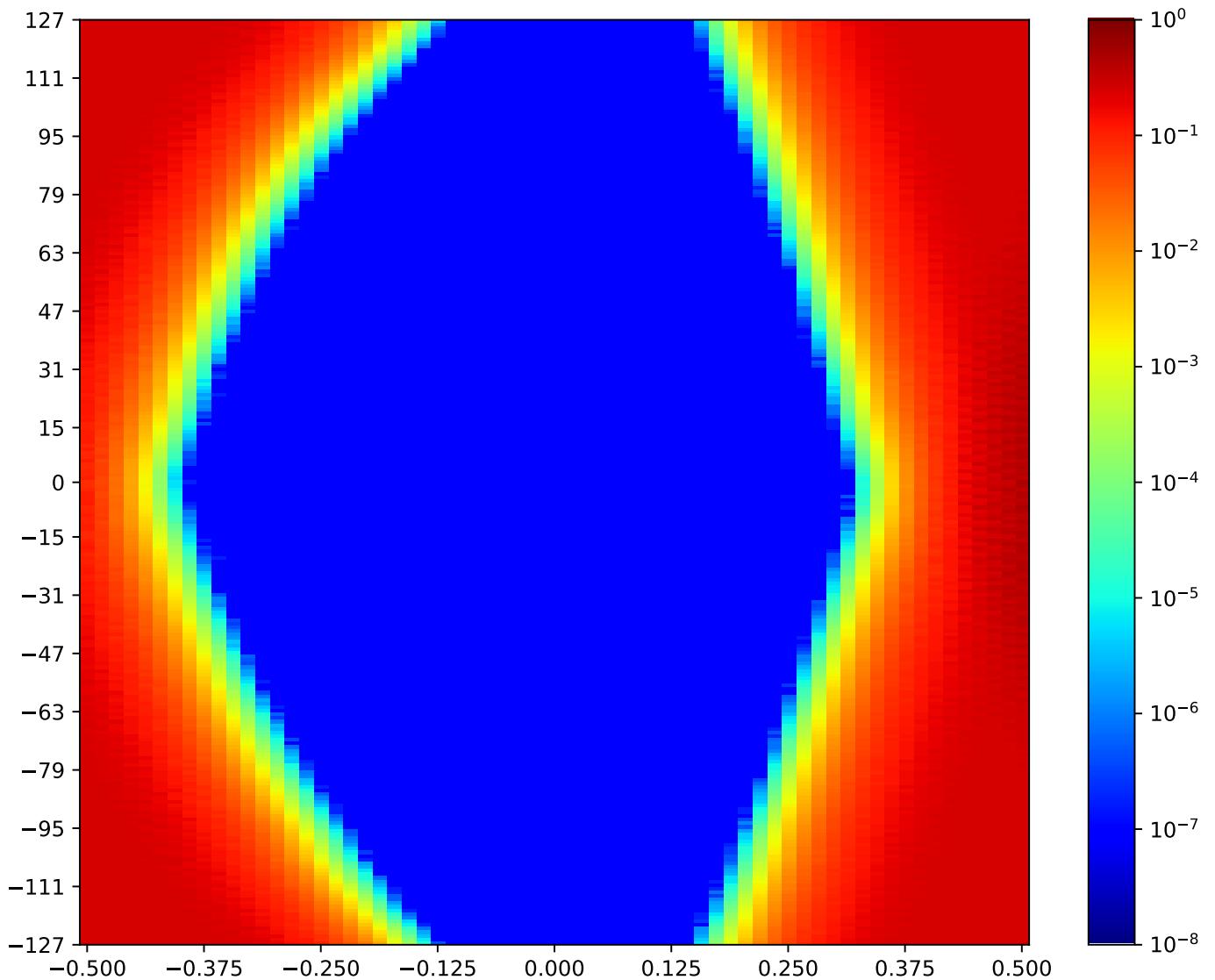


Figure 3.125: MSP\_C\_FPGA-IC39-26-IC15-26-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.9.28 MSP\_C\_FPGA-IC39-27-IC15-27-TRP\_FPGA

Table 3.117: MSP\_C\_FPGA-IC39-27-IC15-27-TRP\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:09:08		2018-Jan-24 00:09:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8954	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

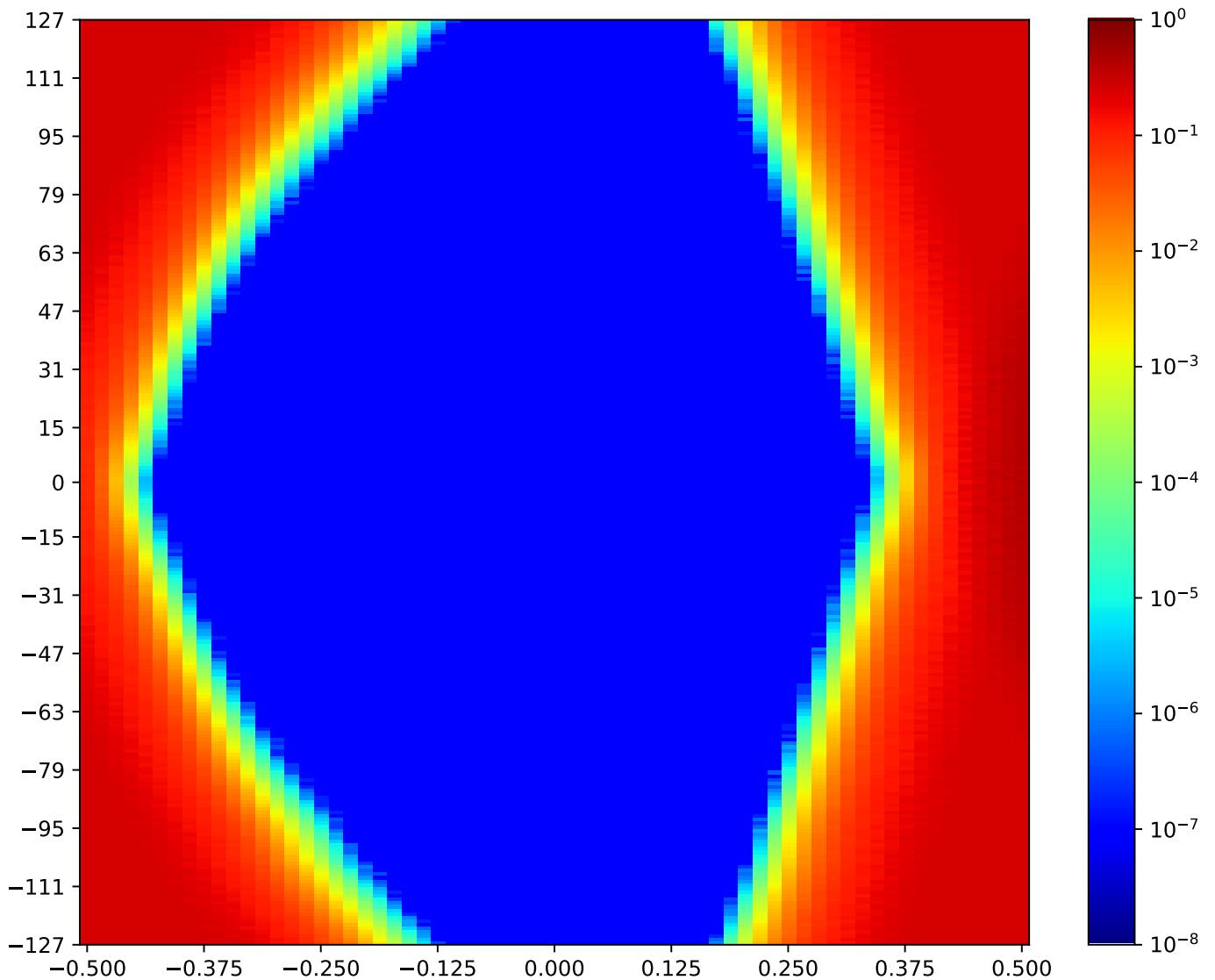


Figure 3.126: MSP\_C\_FPGA-IC39-27-IC15-27-TRP\_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10 MSP\_A TX1 MSP\_C RX18 Minipod Loopback

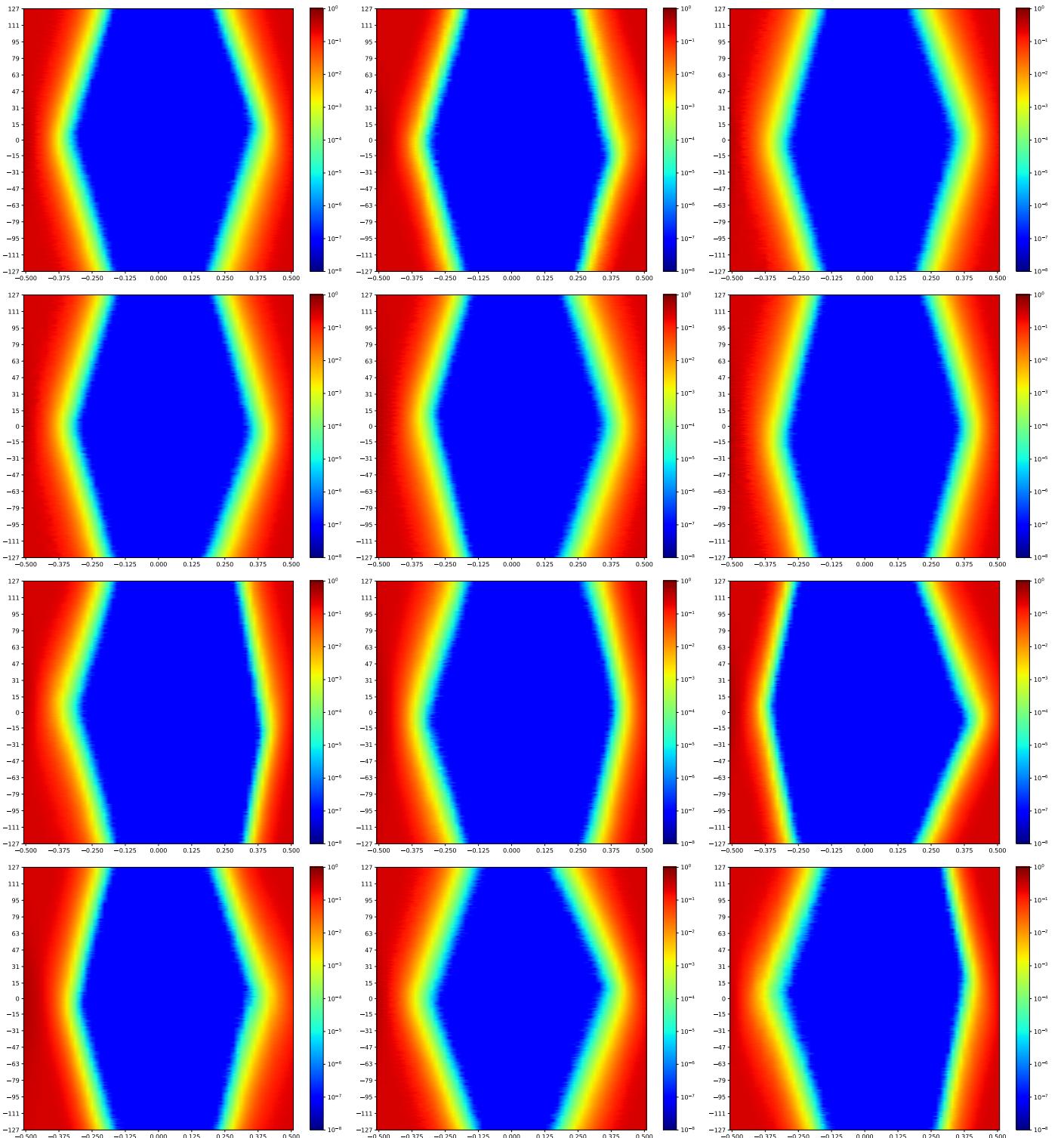


Figure 3.127: MSP\_A TX1 MSP\_C RX18 Minipod Loopback

A cross-reference to Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.140.

### 3.10.1 MSP\_A\_FPGA-TX1-00-RX18-00-MSP\_C\_FPGA

Table 3.118: MSP\_A\_FPGA-TX1-00-RX18-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:28:06		2018-Jan-24 00:28:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7939	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

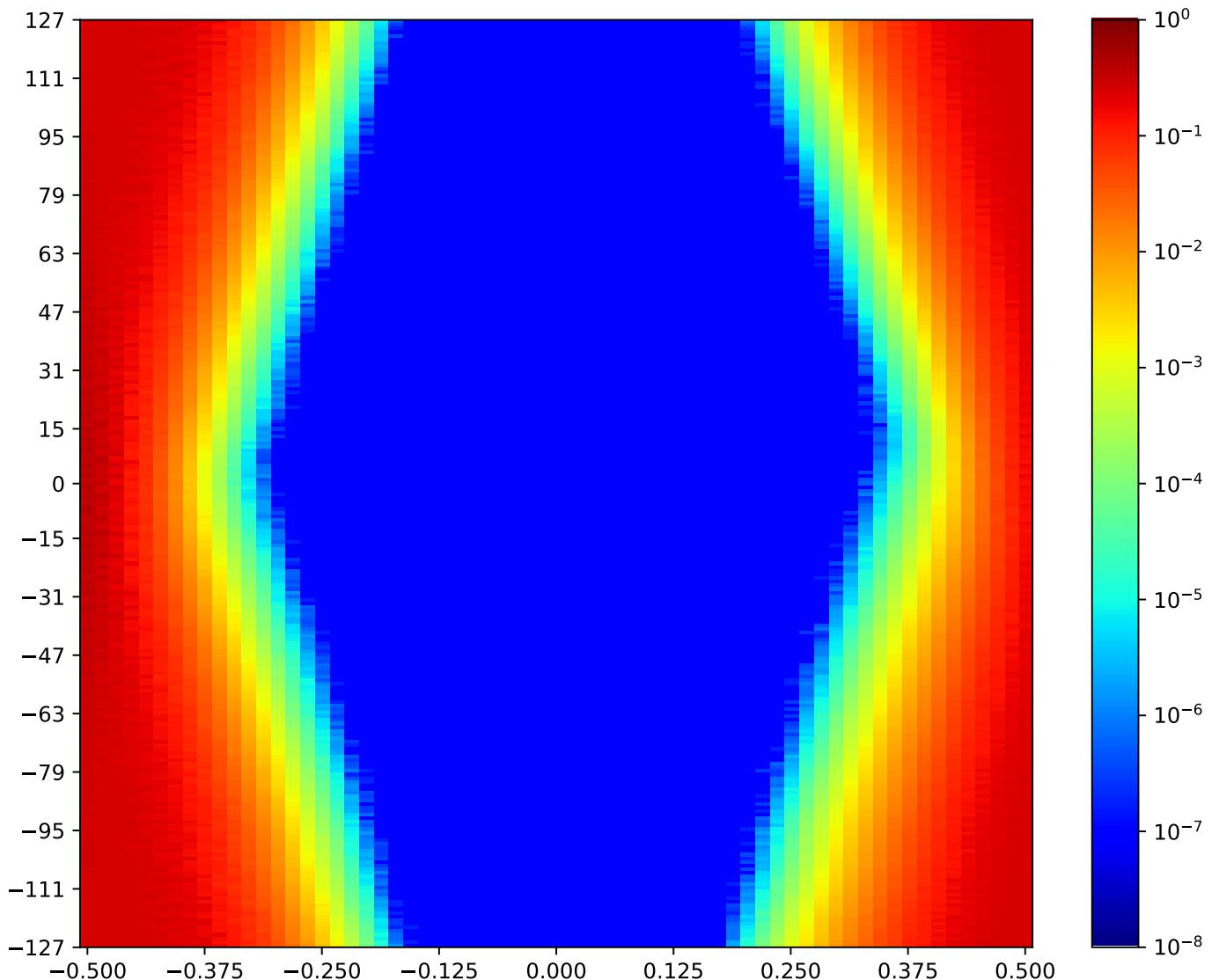


Figure 3.128: MSP\_A\_FPGA-TX1-00-RX18-00-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.2 MSP\_A\_FPGA-TX1-01-RX18-01-MSP\_C\_FPGA

Table 3.119: MSP\_A\_FPGA-TX1-01-RX18-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:28:49		2018-Jan-24 00:29:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8212	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

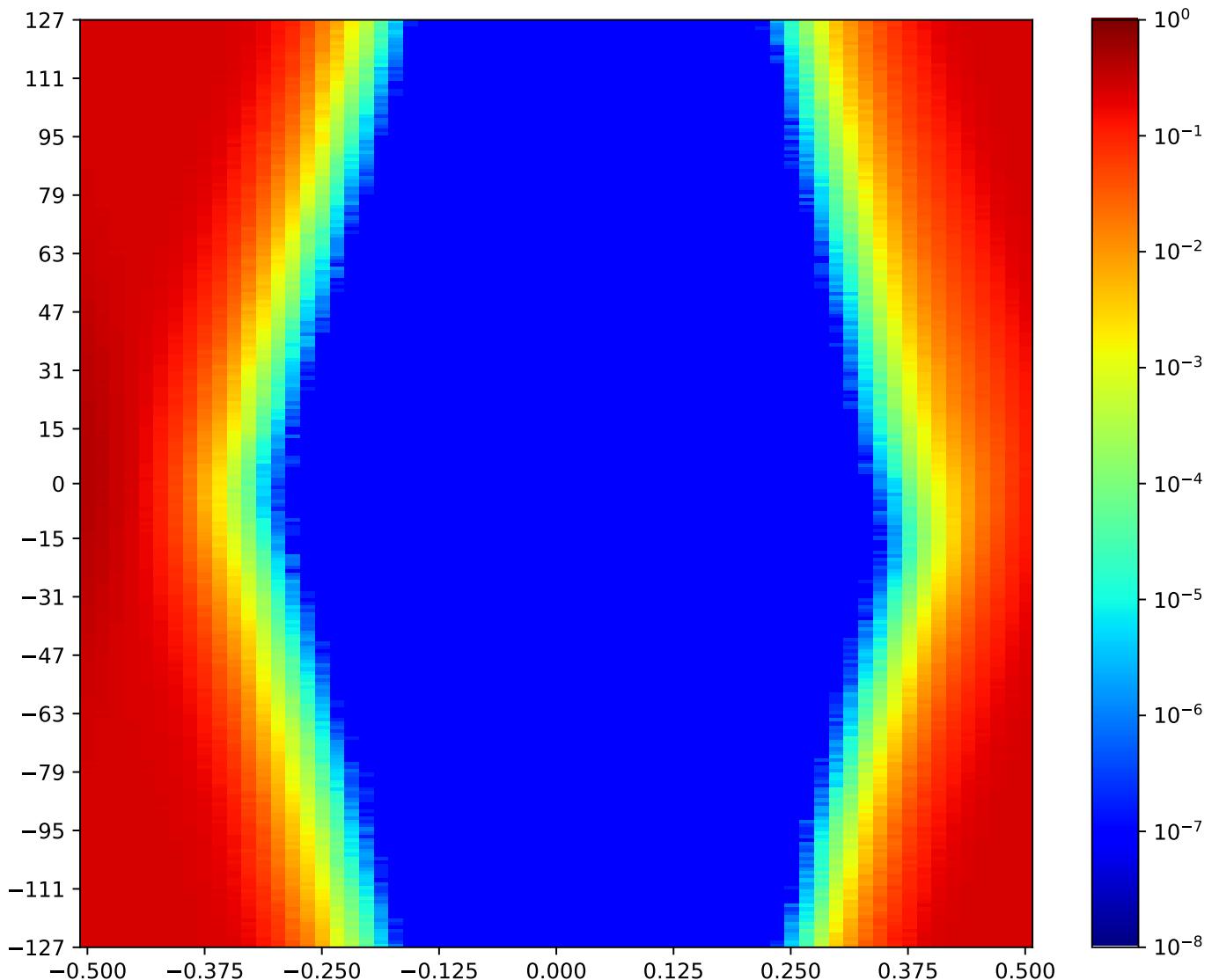


Figure 3.129: MSP\_A\_FPGA-TX1-01-RX18-01-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.3 MSP\_A\_FPGA-TX1-02-RX18-02-MSP\_C\_FPGA

Table 3.120: MSP\_A\_FPGA-TX1-02-RX18-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:29:10			2018-Jan-24 00:29:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7156	36	55.38%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

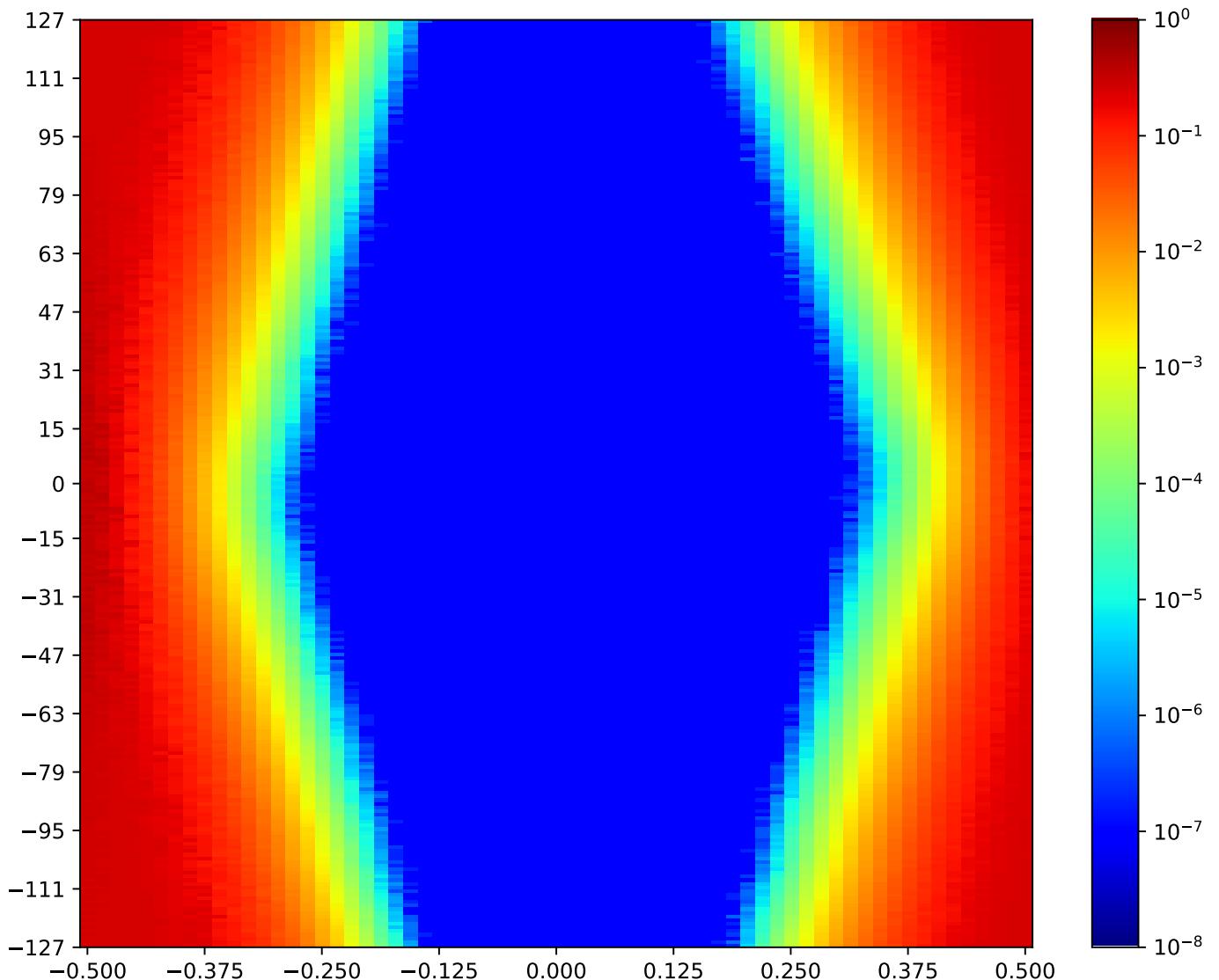


Figure 3.130: MSP\_A\_FPGA-TX1-02-RX18-02-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.4 MSP\_A\_FPGA-TX1-03-RX18-03-MSP\_C\_FPGA

Table 3.121: MSP\_A\_FPGA-TX1-03-RX18-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:27:23			2018-Jan-24 00:27:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7661	39	60.00%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

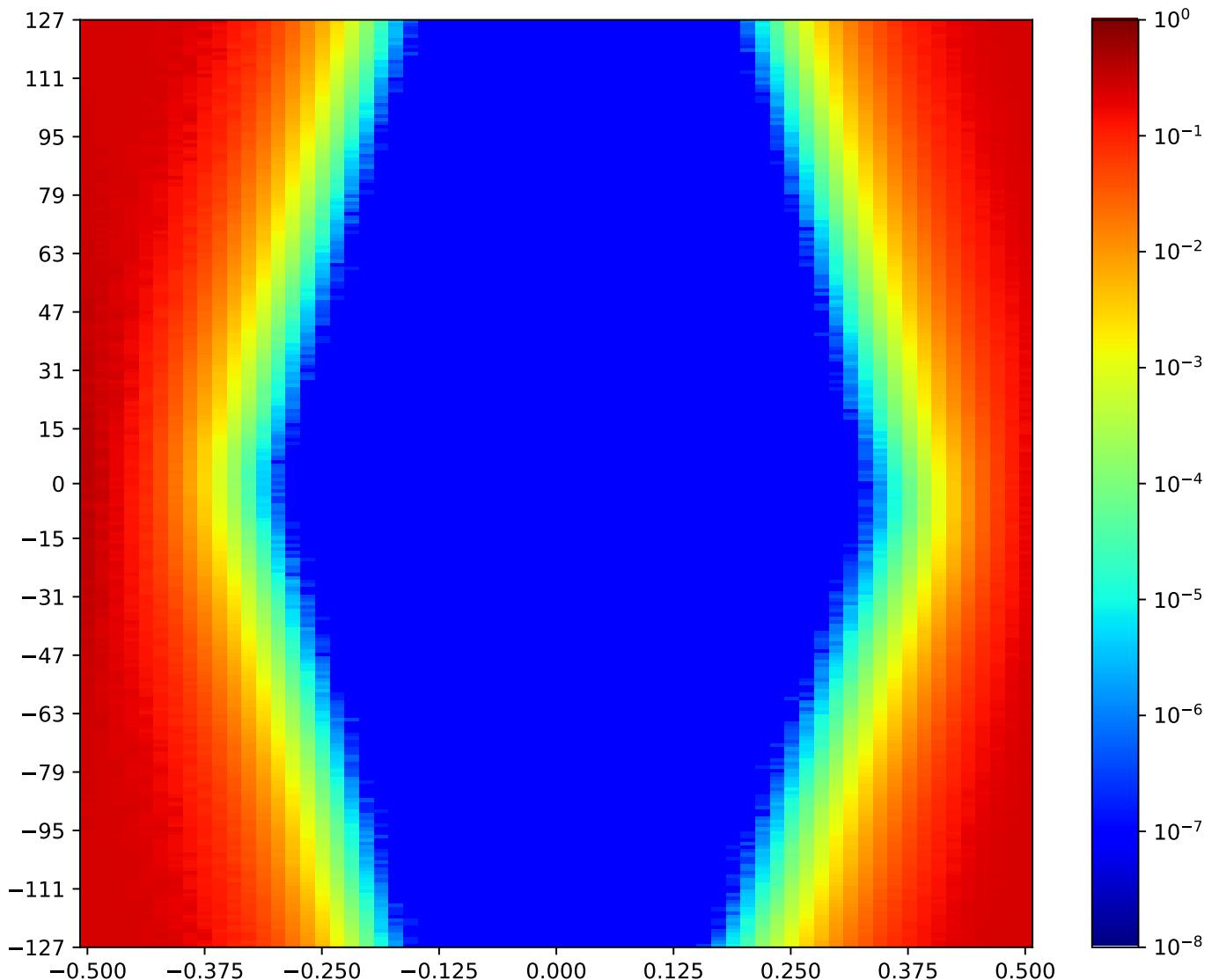


Figure 3.131: MSP\_A\_FPGA-TX1-03-RX18-03-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.5 MSP\_A\_FPGA-TX1-04-RX18-04-MSP\_C\_FPGA

Table 3.122: MSP\_A\_FPGA-TX1-04-RX18-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:30:15		2018-Jan-24 00:30:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7359	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

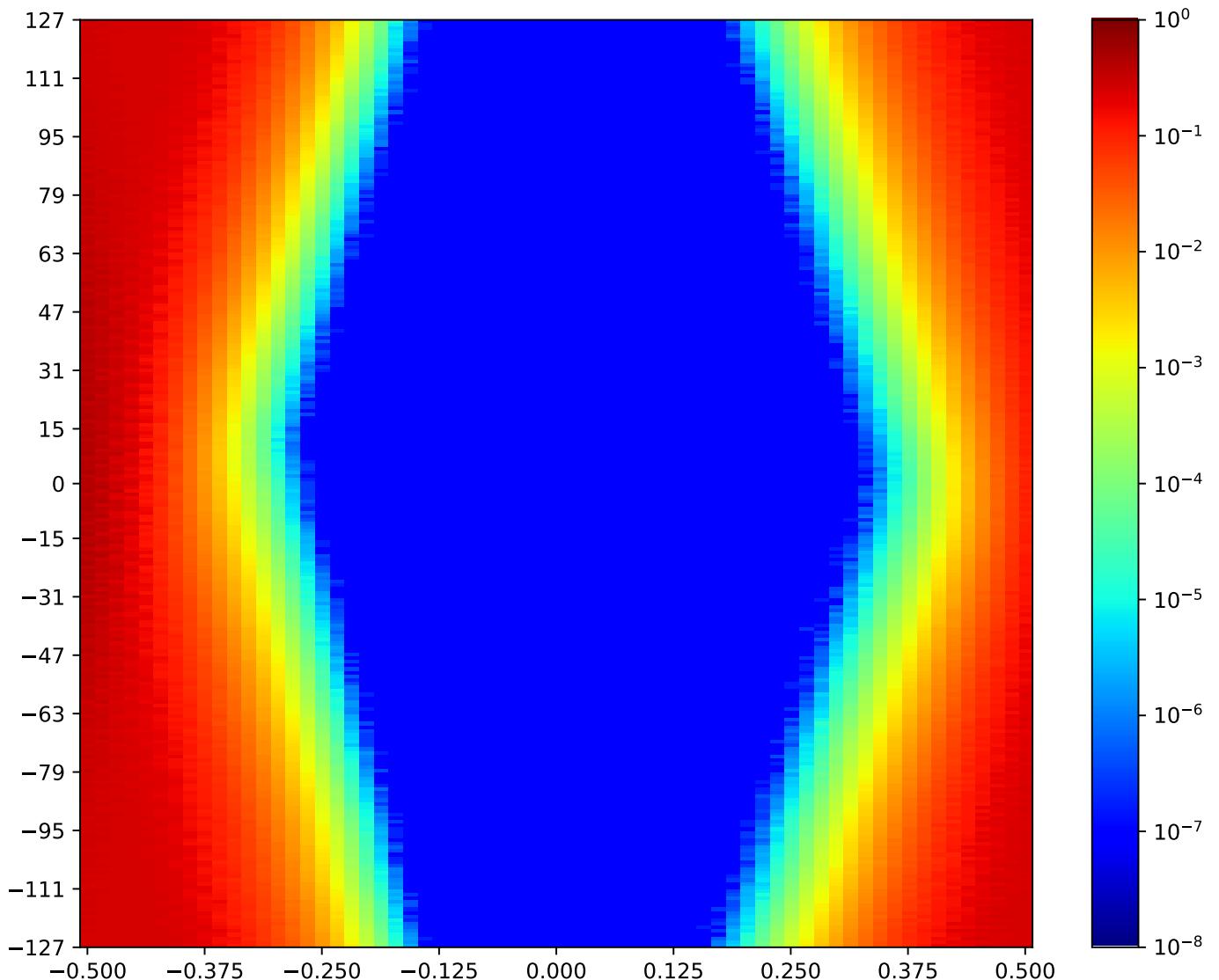


Figure 3.132: MSP\_A\_FPGA-TX1-04-RX18-04-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.6 MSP\_A\_FPGA-TX1-05-RX18-05-MSP\_C\_FPGA

Table 3.123: MSP\_A\_FPGA-TX1-05-RX18-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:27:02		2018-Jan-24 00:27:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7940	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

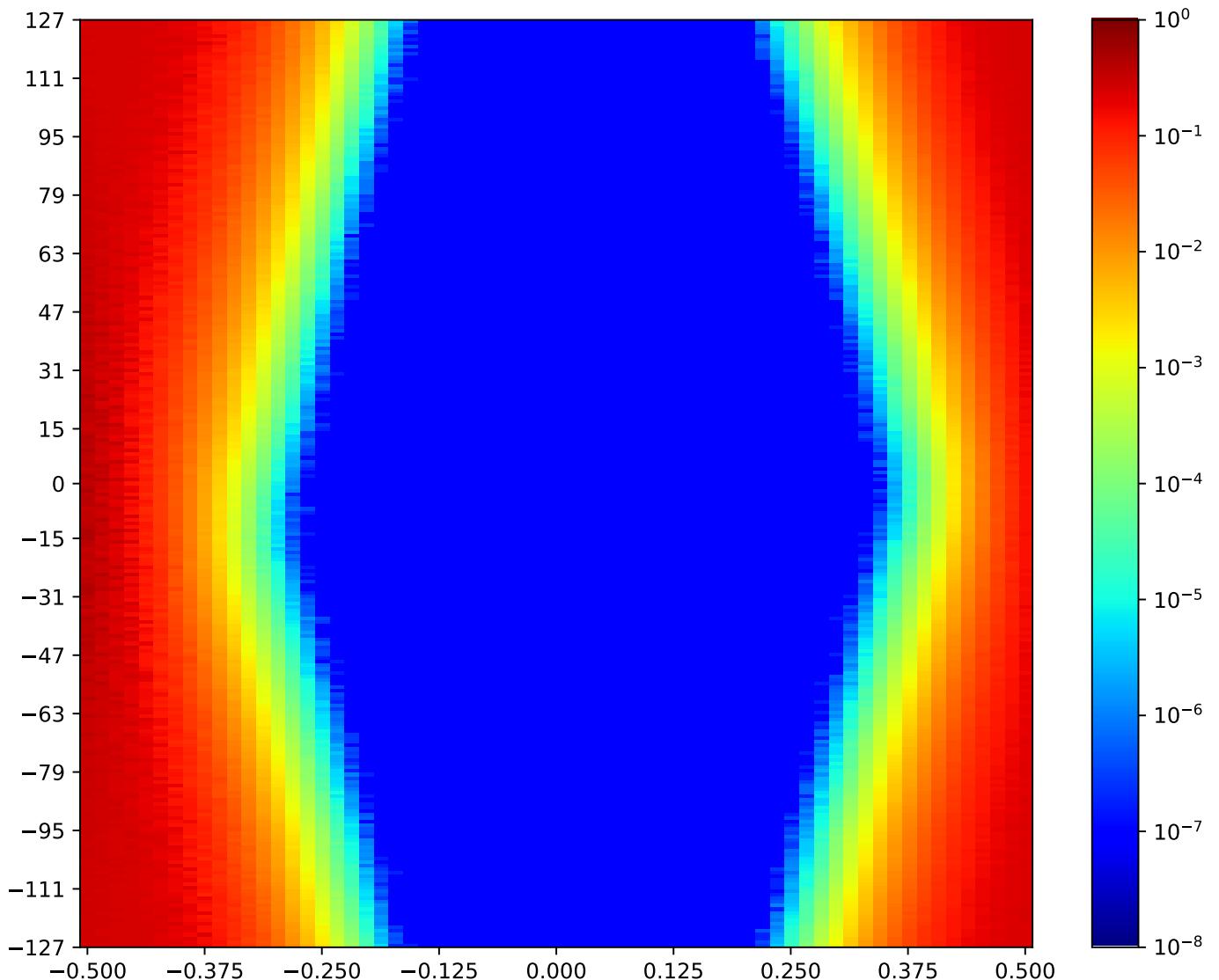


Figure 3.133: MSP\_A\_FPGA-TX1-05-RX18-05-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.7 MSP\_A\_FPGA-TX1-06-RX18-06-MSP\_C\_FPGA

Table 3.124: MSP\_A\_FPGA-TX1-06-RX18-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:30:58		2018-Jan-24 00:31:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8863	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

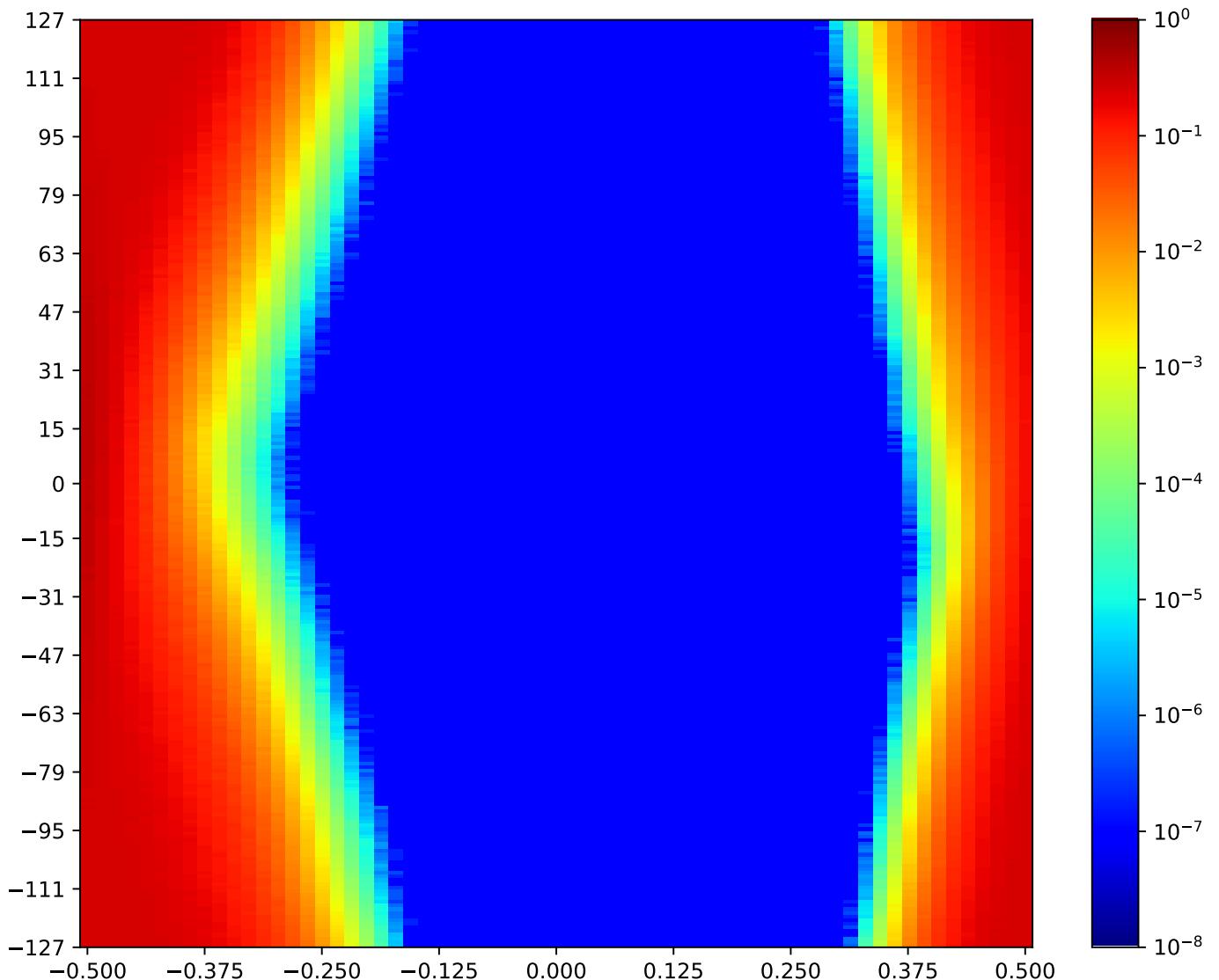


Figure 3.134: MSP\_A\_FPGA-TX1-06-RX18-06-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.8 MSP\_A\_FPGA-TX1-07-RX18-07-MSP\_C\_FPGA

Table 3.125: MSP\_A\_FPGA-TX1-07-RX18-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:27:44		2018-Jan-24 00:28:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8630	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

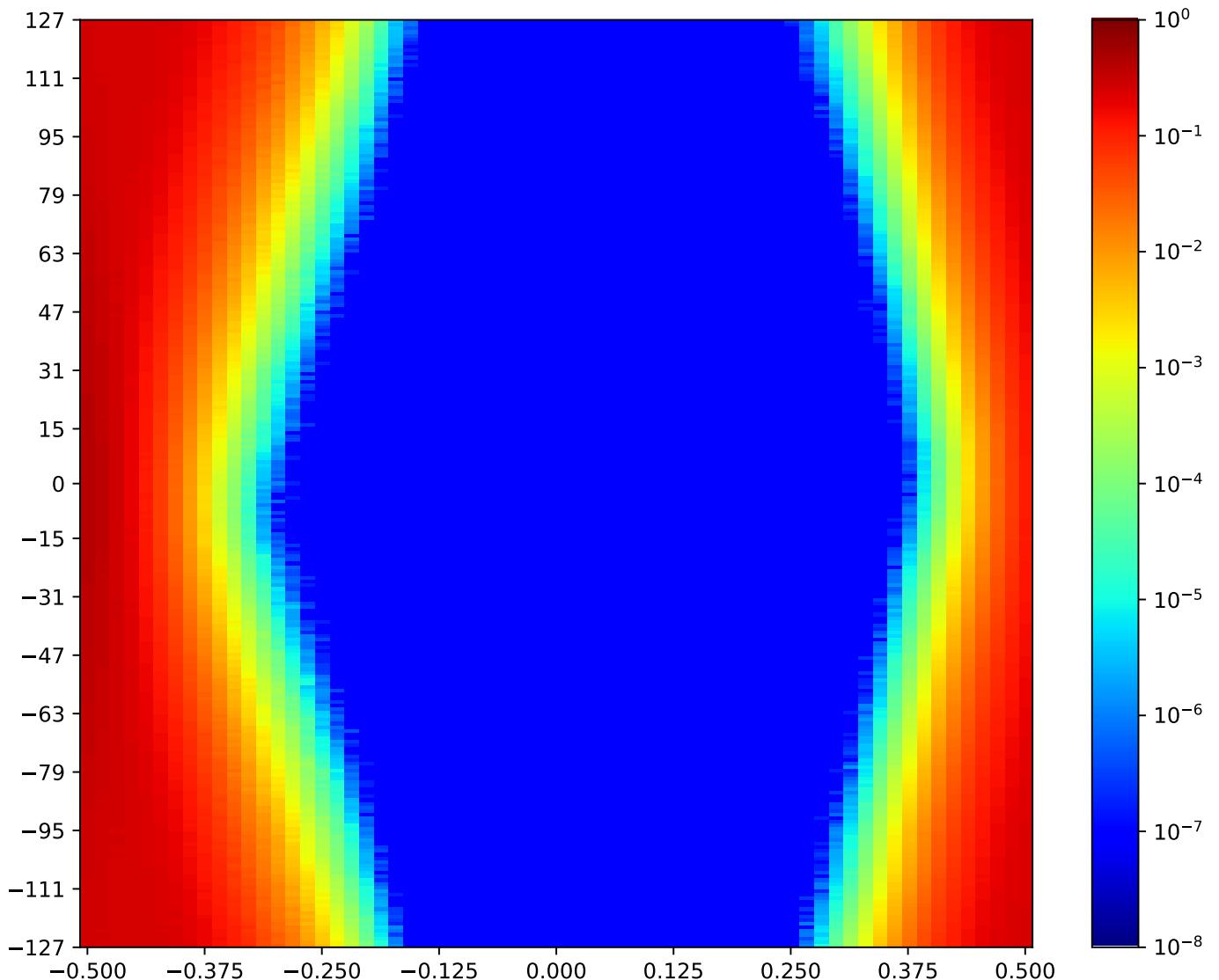


Figure 3.135: MSP\_A\_FPGA-TX1-07-RX18-07-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.9 MSP\_A\_FPGA-TX1-08-RX18-08-MSP\_C\_FPGA

Table 3.126: MSP\_A\_FPGA-TX1-08-RX18-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:30:37		2018-Jan-24 00:30:58	
Reset RX	OA	HO		HO (%)	
true	9062	44		67.69%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

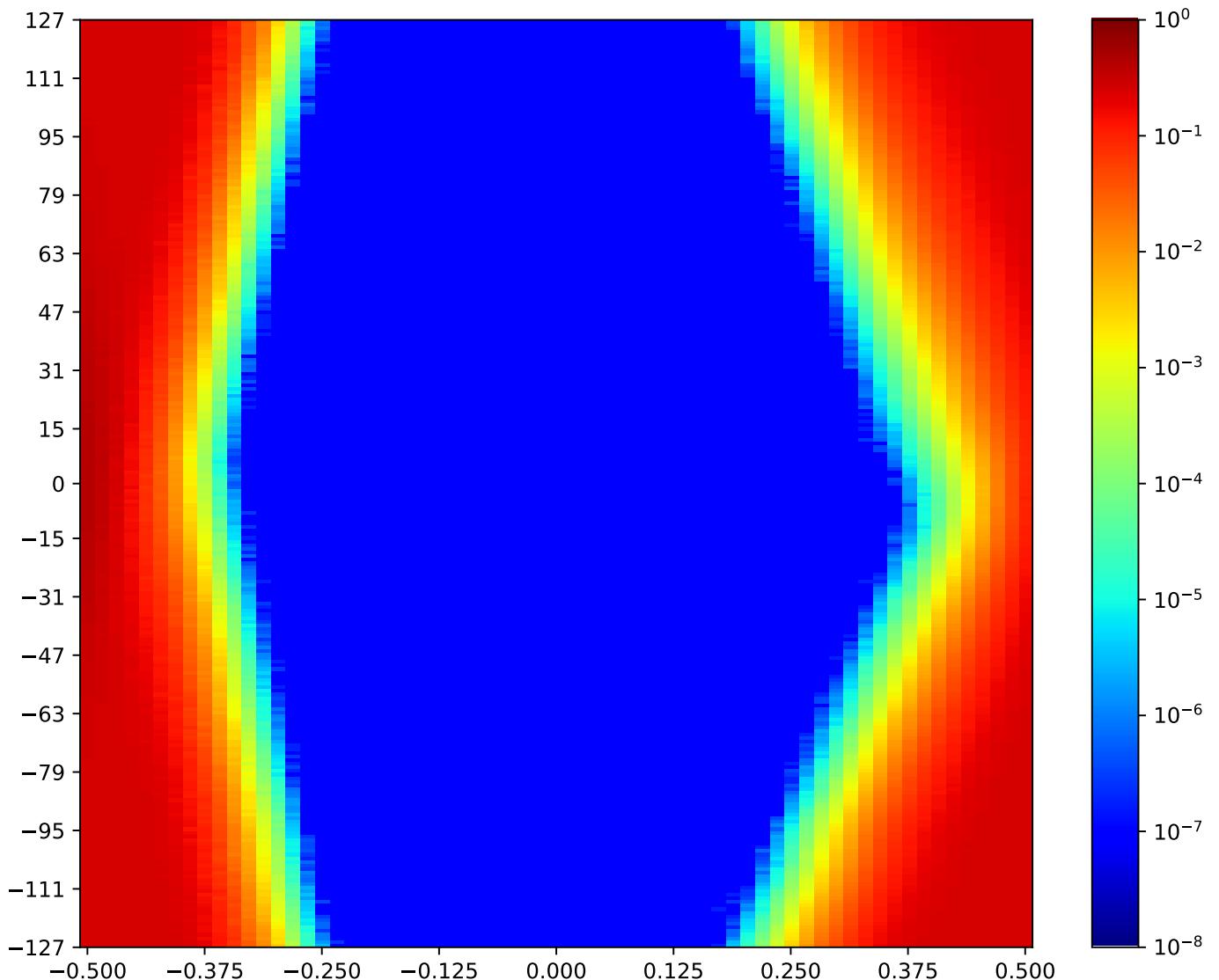


Figure 3.136: MSP\_A\_FPGA-TX1-08-RX18-08-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.10 MSP\_A\_FPGA-TX1-09-RX18-09-MSP\_C\_FPGA

Table 3.127: MSP\_A\_FPGA-TX1-09-RX18-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:28:27		2018-Jan-24 00:28:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7722	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

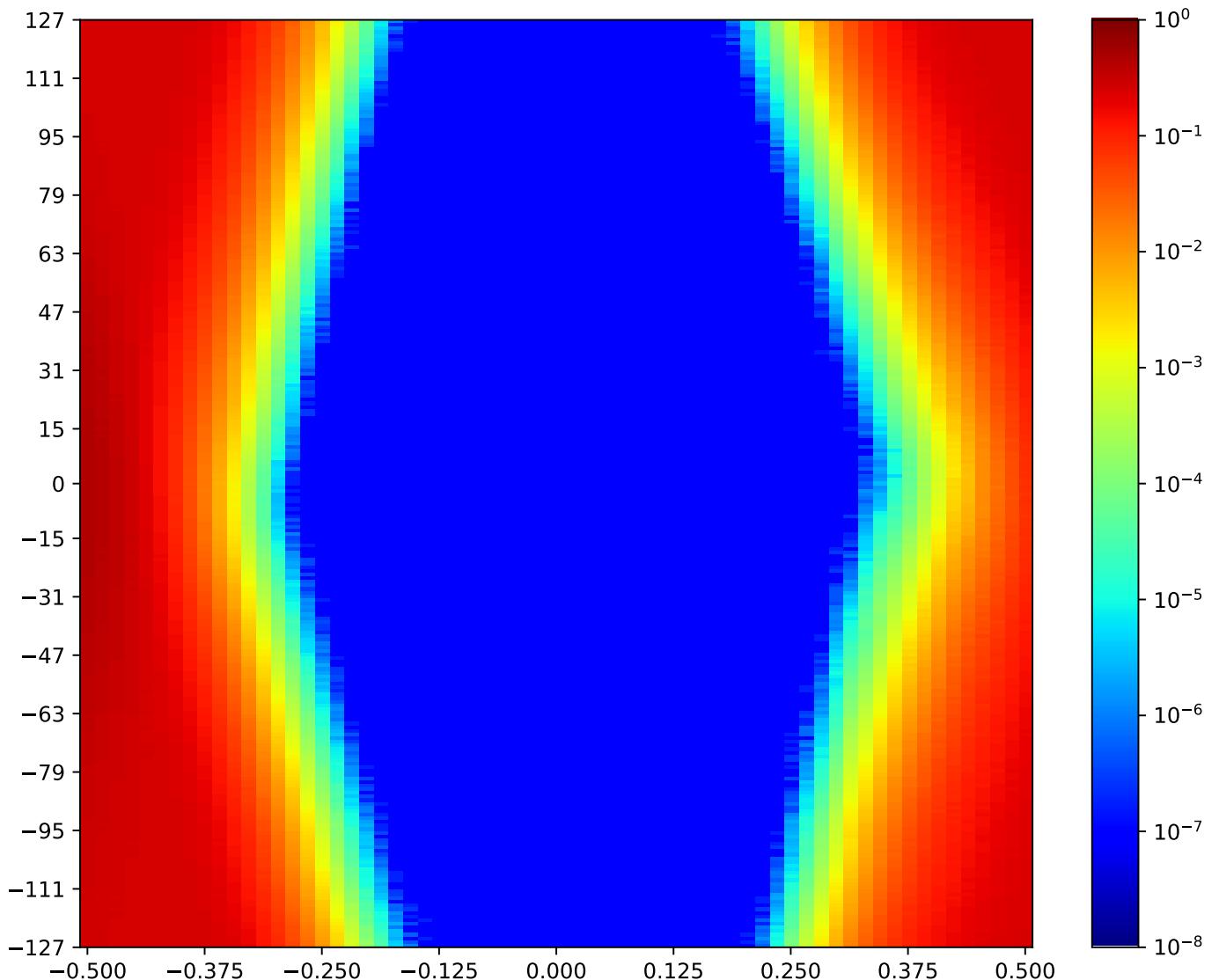


Figure 3.137: MSP\_A\_FPGA-TX1-09-RX18-09-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.11 MSP\_A\_FPGA-TX1-10-RX18-10-MSP\_C\_FPGA

Table 3.128: MSP\_A\_FPGA-TX1-10-RX18-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:29:54		2018-Jan-24 00:30:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6686	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

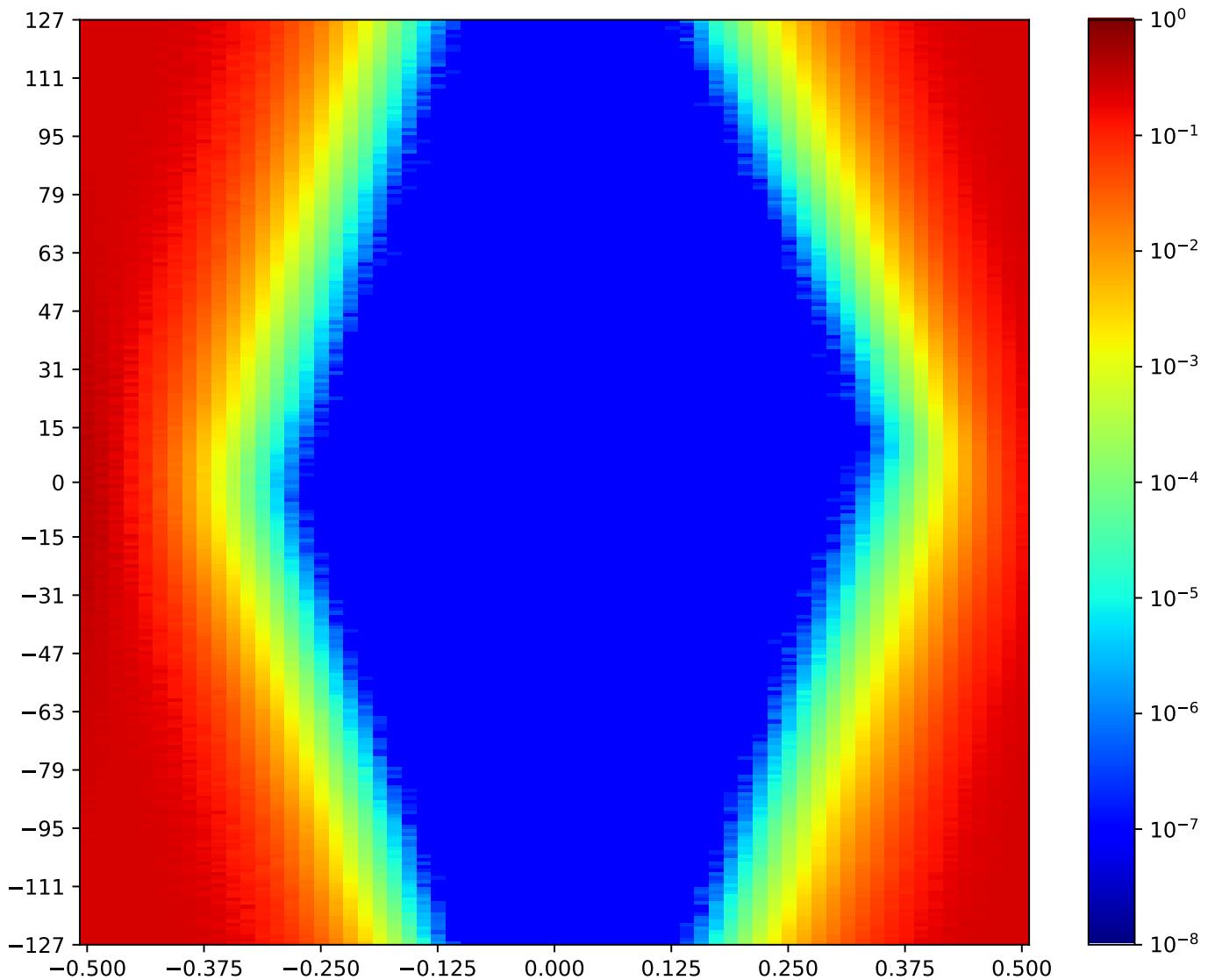


Figure 3.138: MSP\_A\_FPGA-TX1-10-RX18-10-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.10.12 MSP\_A\_FPGA-TX1-11-RX18-11-MSP\_C\_FPGA

Table 3.129: MSP\_A\_FPGA-TX1-11-RX18-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:29:32		2018-Jan-24 00:29:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8265	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

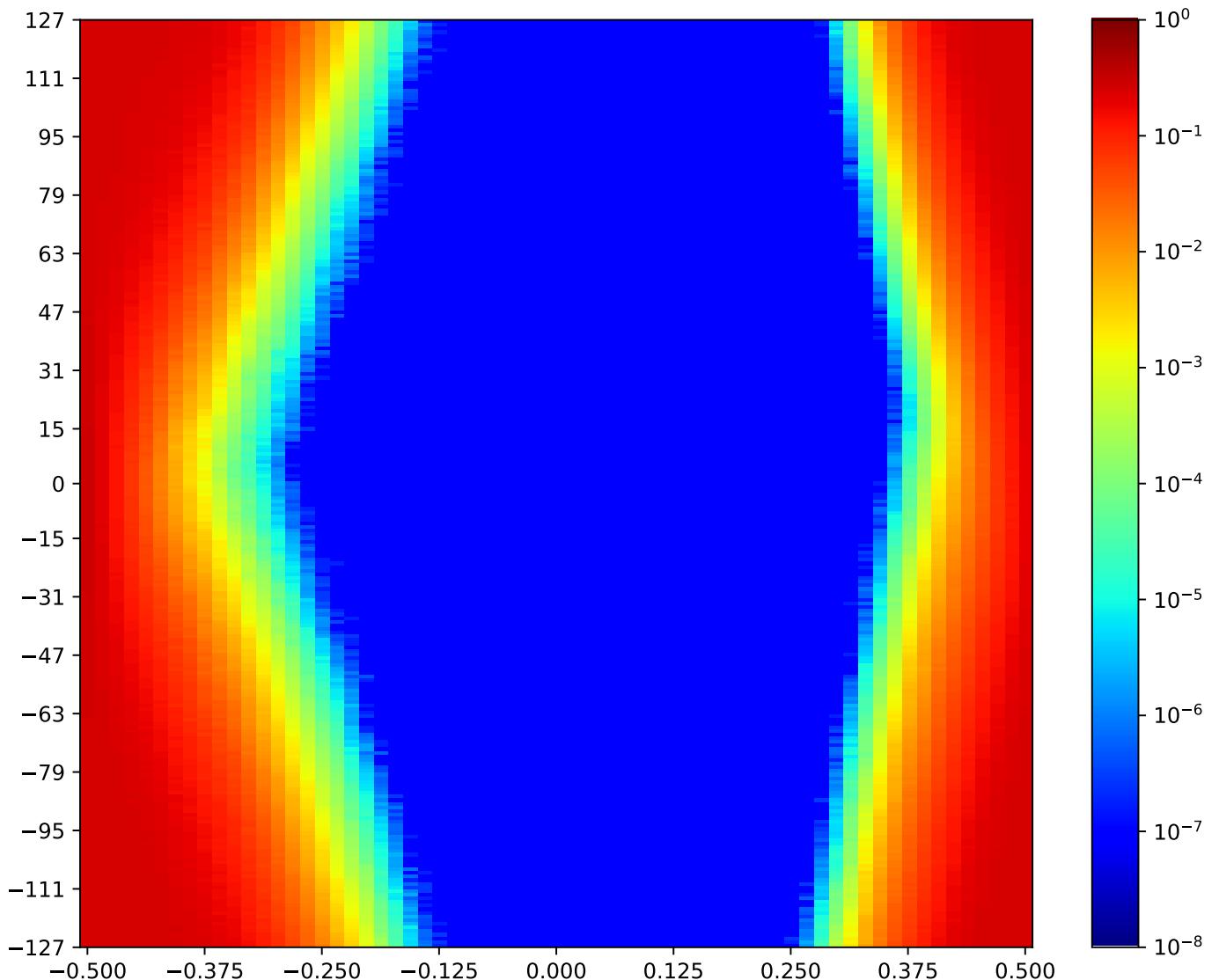


Figure 3.139: MSP\_A\_FPGA-TX1-11-RX18-11-MSP\_C\_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11 MSP\_A TX2 MSP\_C RX17 Minipod Loopback

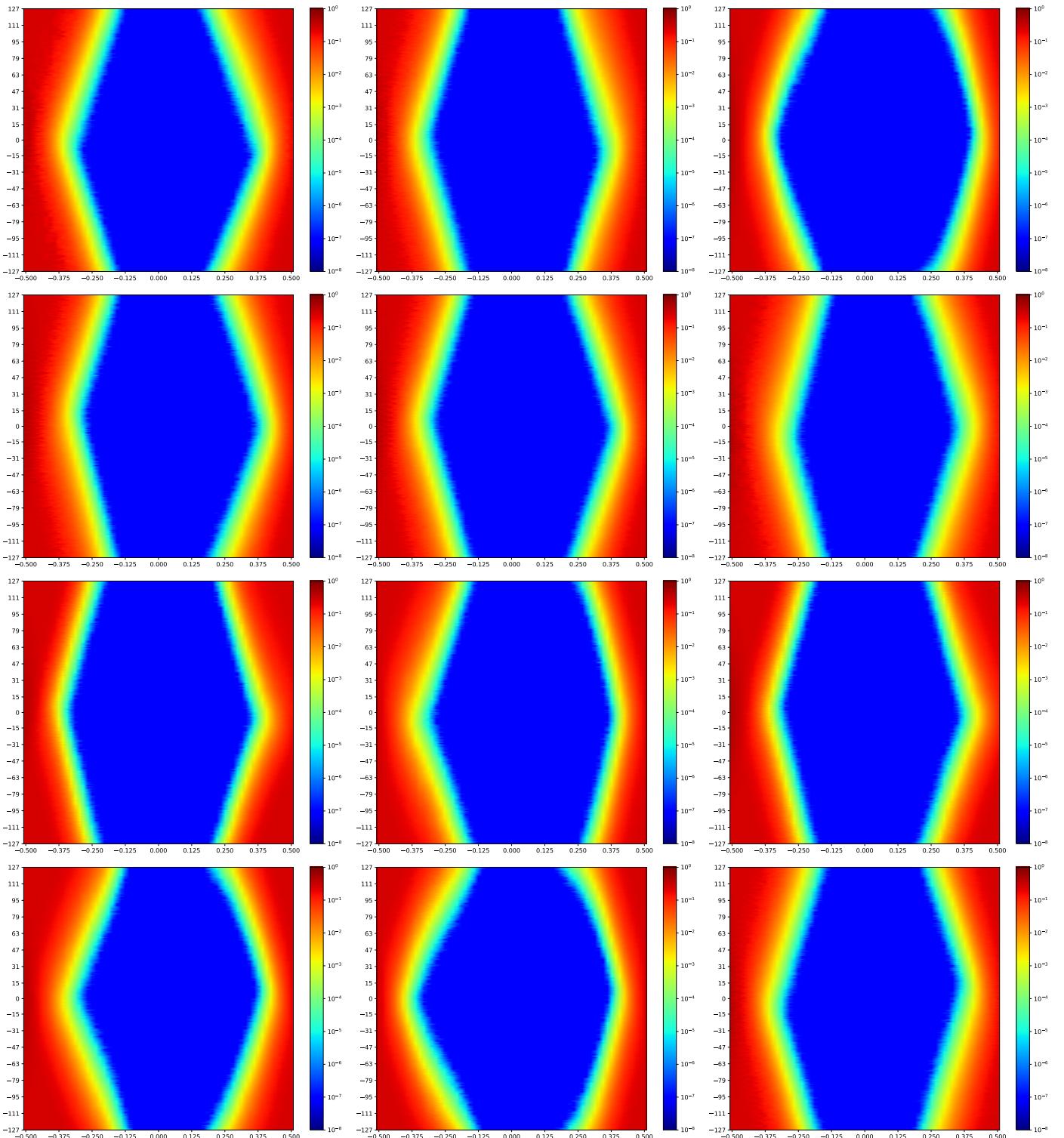


Figure 3.140: MSP\_A TX2 MSP\_C RX17 Minipod Loopback

A cross-reference to Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.153.

### 3.11.1 MSP\_A\_FPGA-TX2-00-RX17-00-MSP\_C\_FPGA

Table 3.130: MSP\_A\_FPGA-TX2-00-RX17-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:32:23			2018-Jan-24 00:32:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7332	35	53.85%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

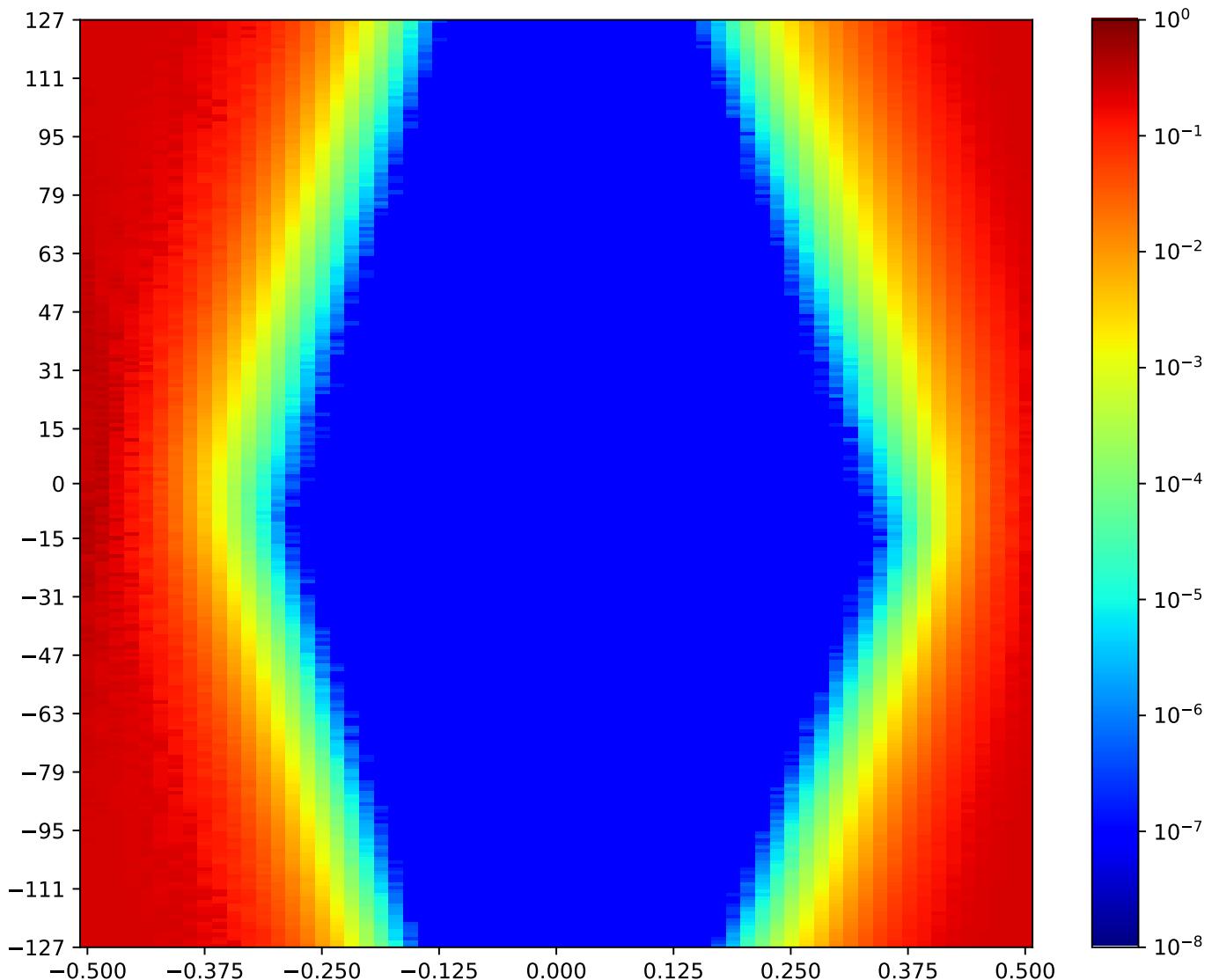


Figure 3.141: MSP\_A\_FPGA-TX2-00-RX17-00-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.2 MSP\_A\_FPGA-TX2-01-RX17-01-MSP\_C\_FPGA

Table 3.131: MSP\_A\_FPGA-TX2-01-RX17-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:31:40			2018-Jan-24 00:32:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7452	37	56.92%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

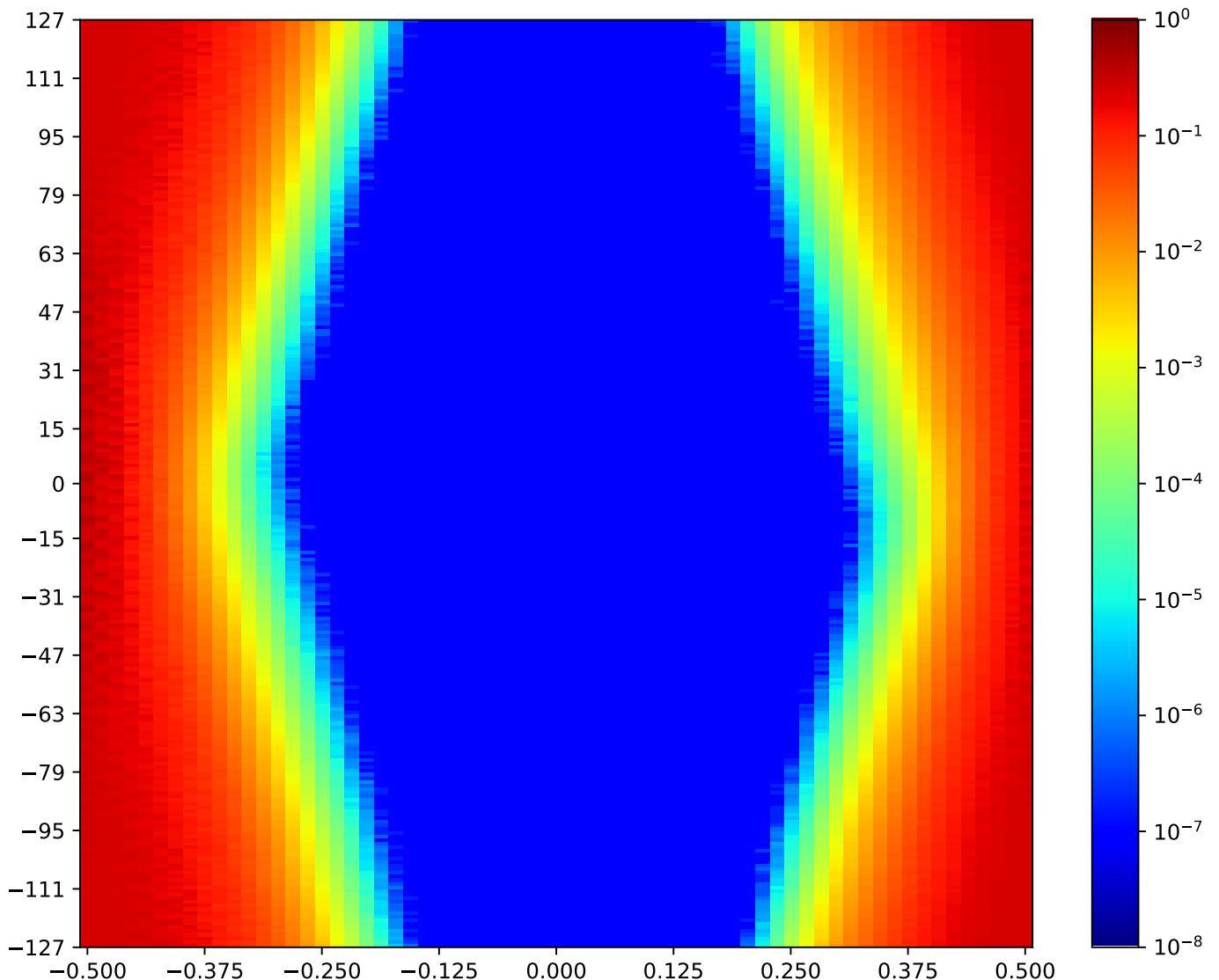


Figure 3.142: MSP\_A\_FPGA-TX2-01-RX17-01-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.3 MSP\_A\_FPGA-TX2-02-RX17-02-MSP\_C\_FPGA

Table 3.132: MSP\_A\_FPGA-TX2-02-RX17-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:33:27		2018-Jan-24 00:33:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8905	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

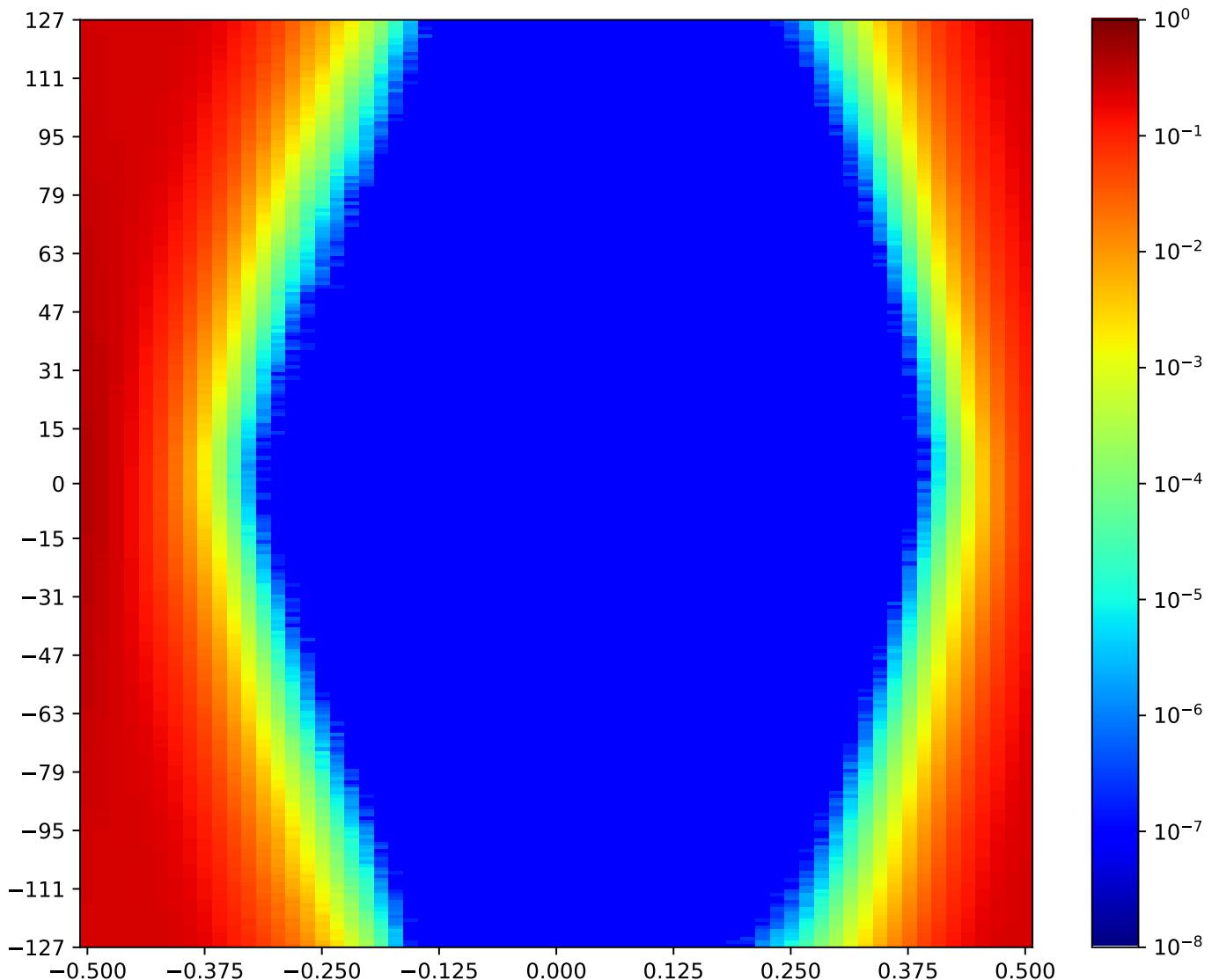


Figure 3.143: MSP\_A\_FPGA-TX2-02-RX17-02-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.4 MSP\_A\_FPGA-TX2-03-RX17-03-MSP\_C\_FPGA

Table 3.133: MSP\_A\_FPGA-TX2-03-RX17-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:31:19		2018-Jan-24 00:31:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7659	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

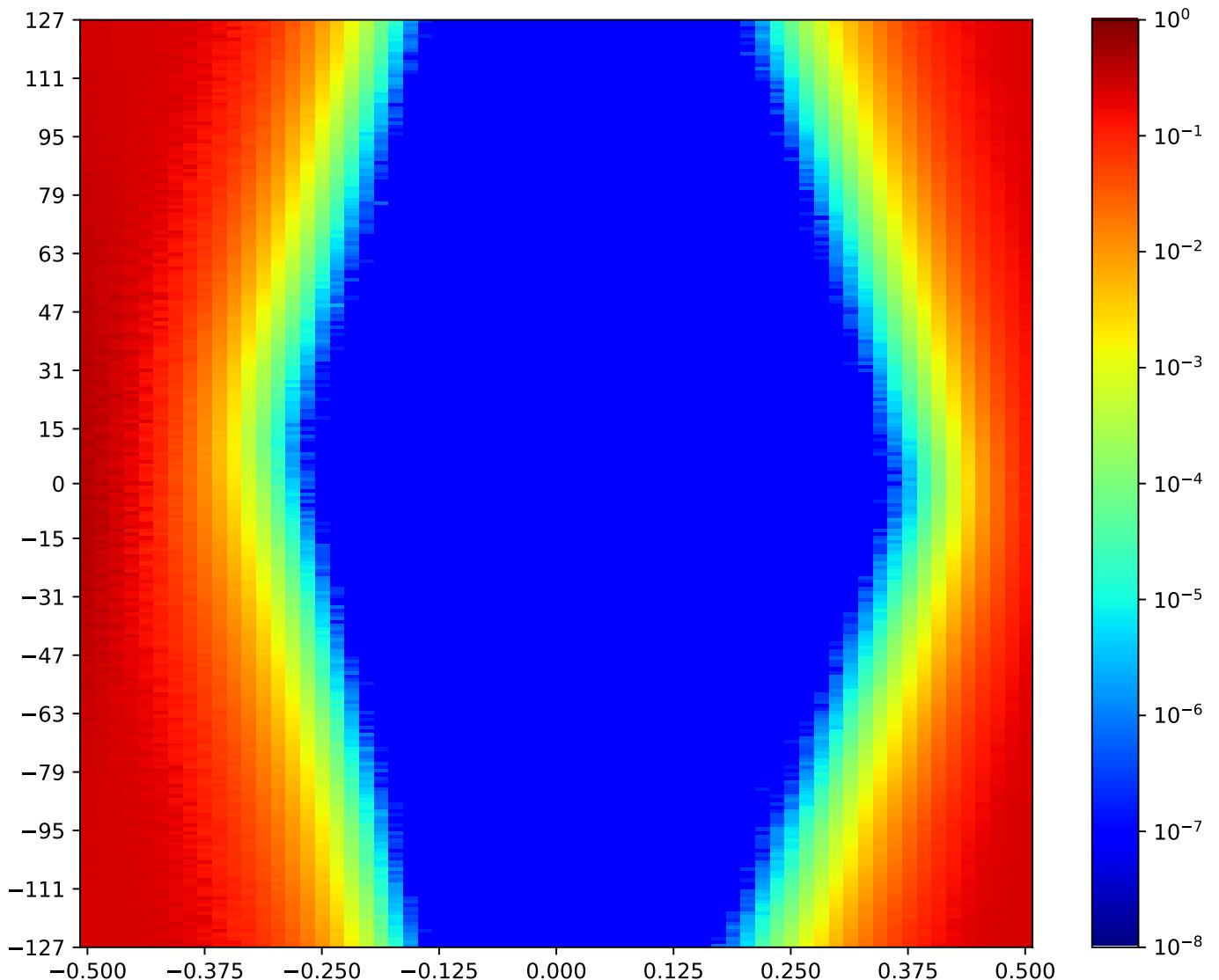


Figure 3.144: MSP\_A\_FPGA-TX2-03-RX17-03-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.5 MSP\_A\_FPGA-TX2-04-RX17-04-MSP\_C\_FPGA

Table 3.134: MSP\_A\_FPGA-TX2-04-RX17-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:34:31		2018-Jan-24 00:34:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7748	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

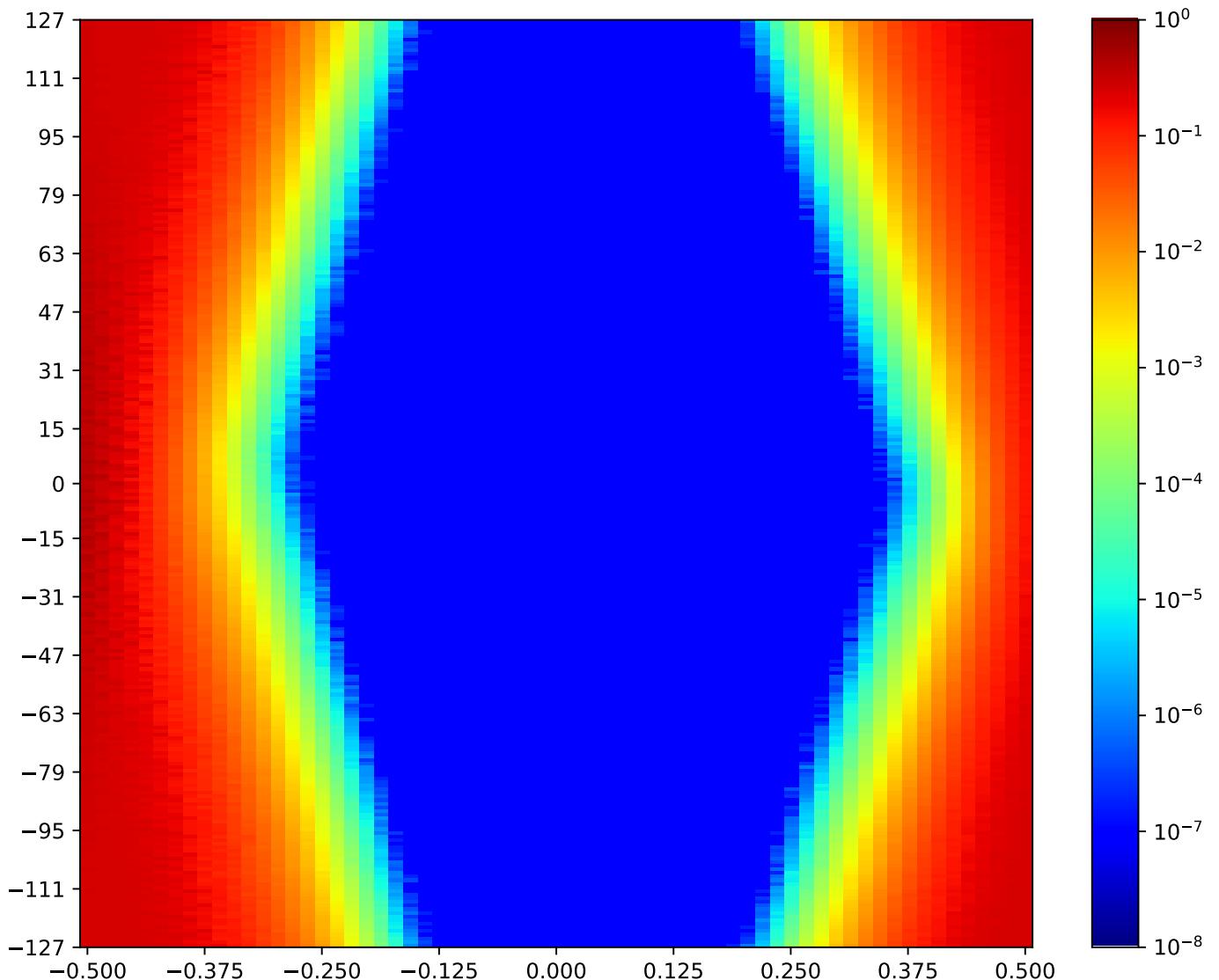


Figure 3.145: MSP\_A\_FPGA-TX2-04-RX17-04-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.6 MSP\_A\_FPGA-TX2-05-RX17-05-MSP\_C\_FPGA

Table 3.135: MSP\_A\_FPGA-TX2-05-RX17-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:32:02			2018-Jan-24 00:32:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	6852	35	53.85%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

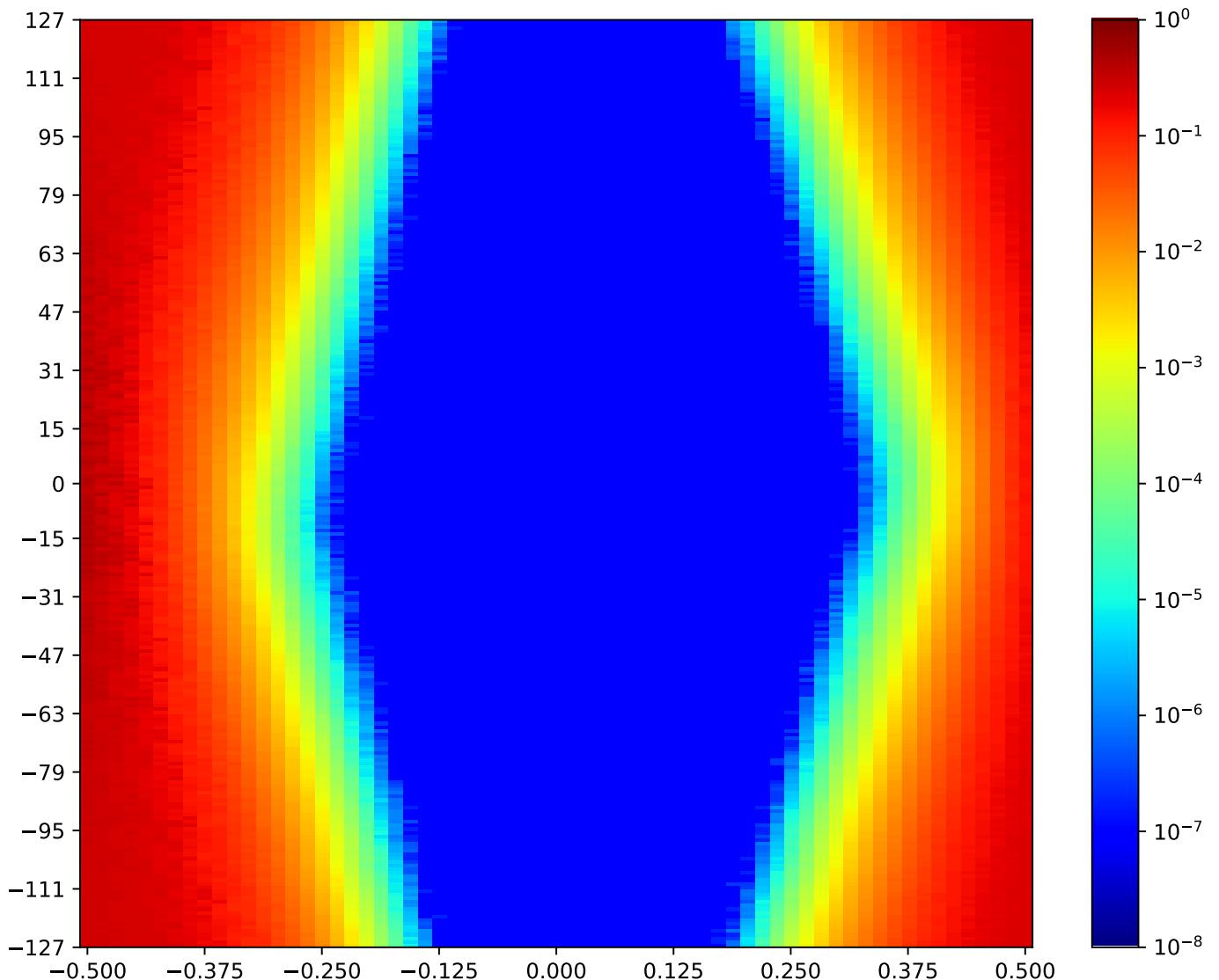


Figure 3.146: MSP\_A\_FPGA-TX2-05-RX17-05-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.7 MSP\_A\_FPGA-TX2-06-RX17-06-MSP\_C\_FPGA

Table 3.136: MSP\_A\_FPGA-TX2-06-RX17-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:35:13		2018-Jan-24 00:35:34	
Reset RX	OA	HO		HO (%)	
true	8502	41		63.08%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

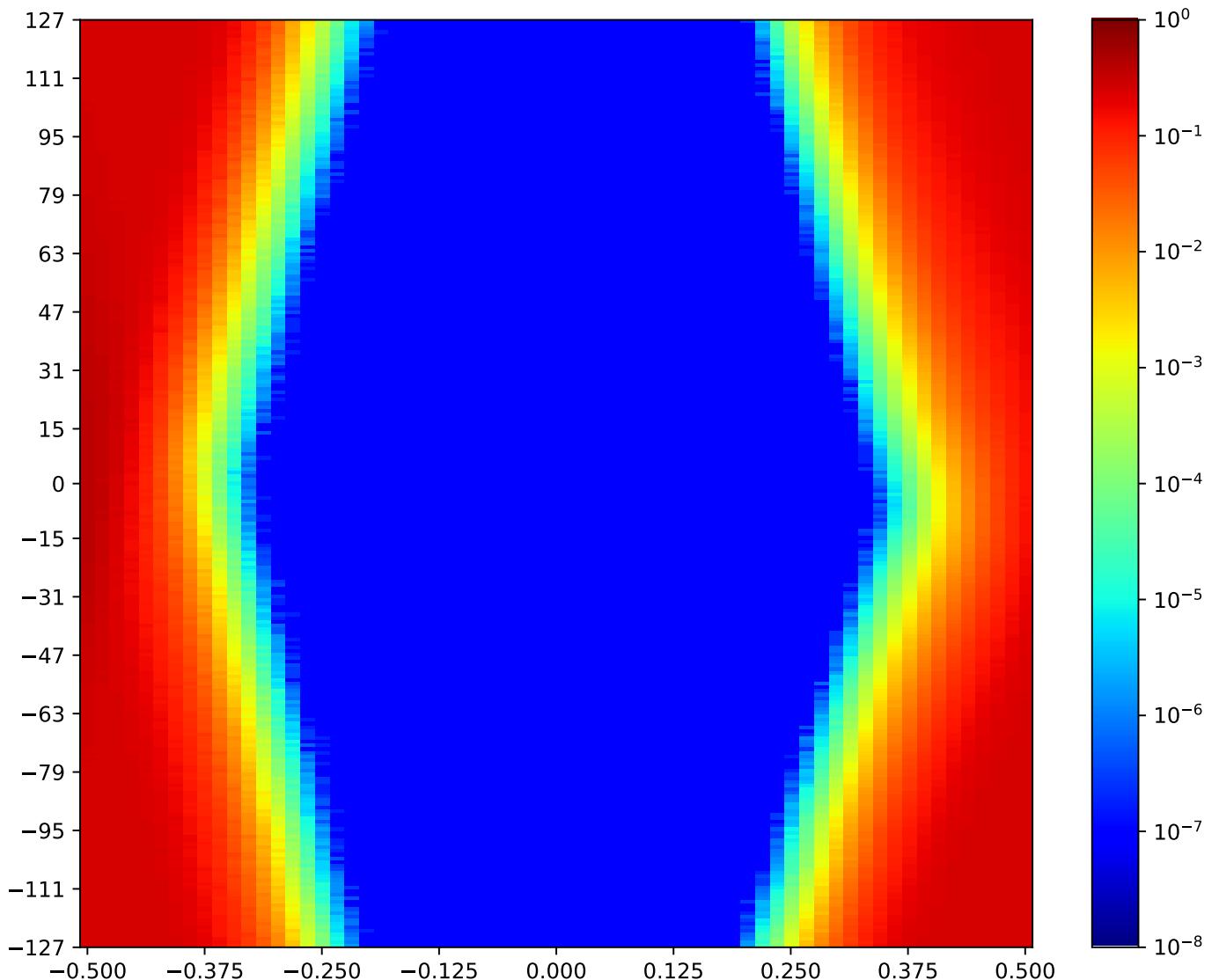


Figure 3.147: MSP\_A\_FPGA-TX2-06-RX17-06-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.8 MSP\_A\_FPGA-TX2-07-RX17-07-MSP\_C\_FPGA

Table 3.137: MSP\_A\_FPGA-TX2-07-RX17-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:32:44		2018-Jan-24 00:33:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8269	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

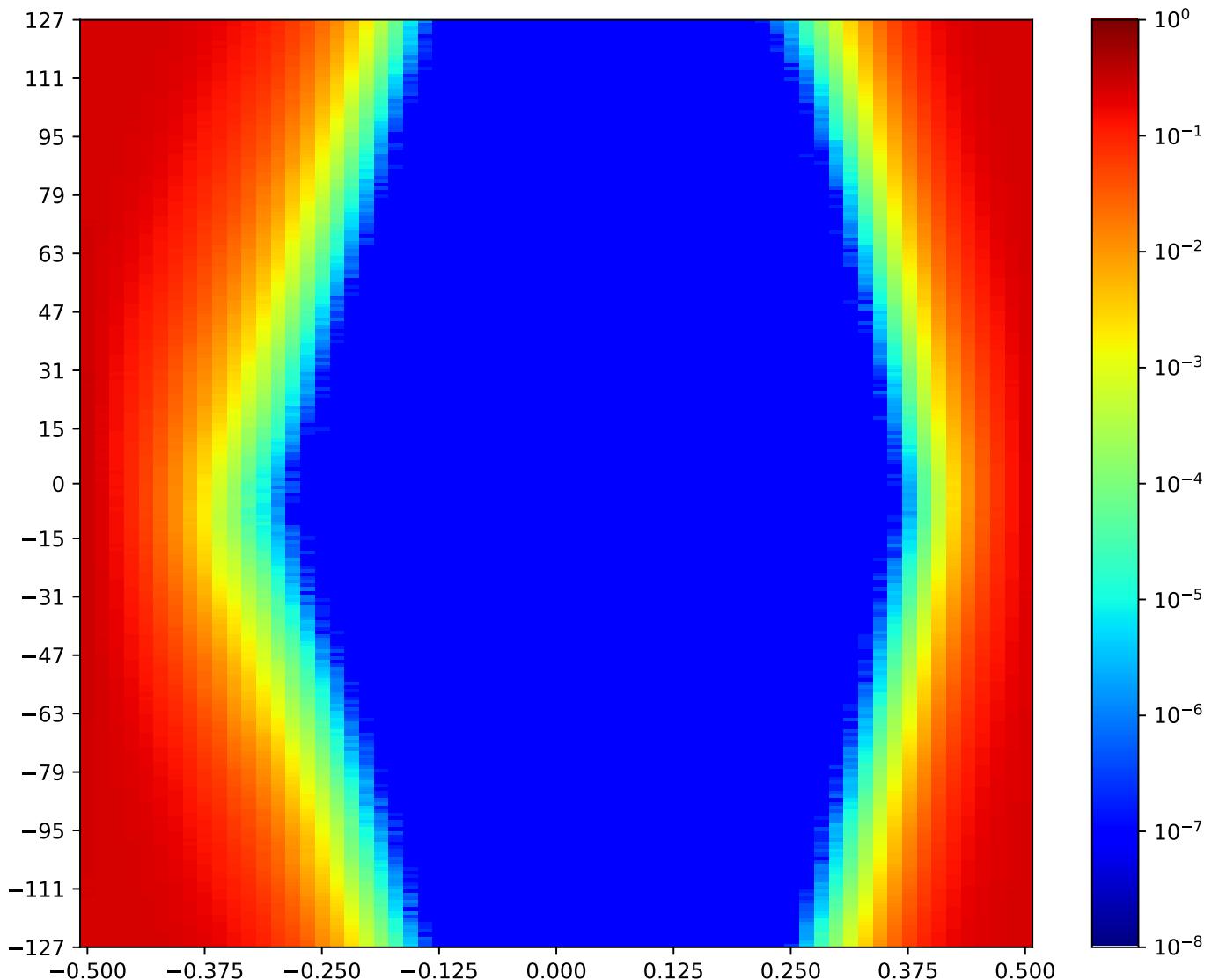


Figure 3.148: MSP\_A\_FPGA-TX2-07-RX17-07-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.9 MSP\_A\_FPGA-TX2-08-RX17-08-MSP\_C\_FPGA

Table 3.138: MSP\_A\_FPGA-TX2-08-RX17-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:34:52			2018-Jan-24 00:35:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	8119	40	61.54%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

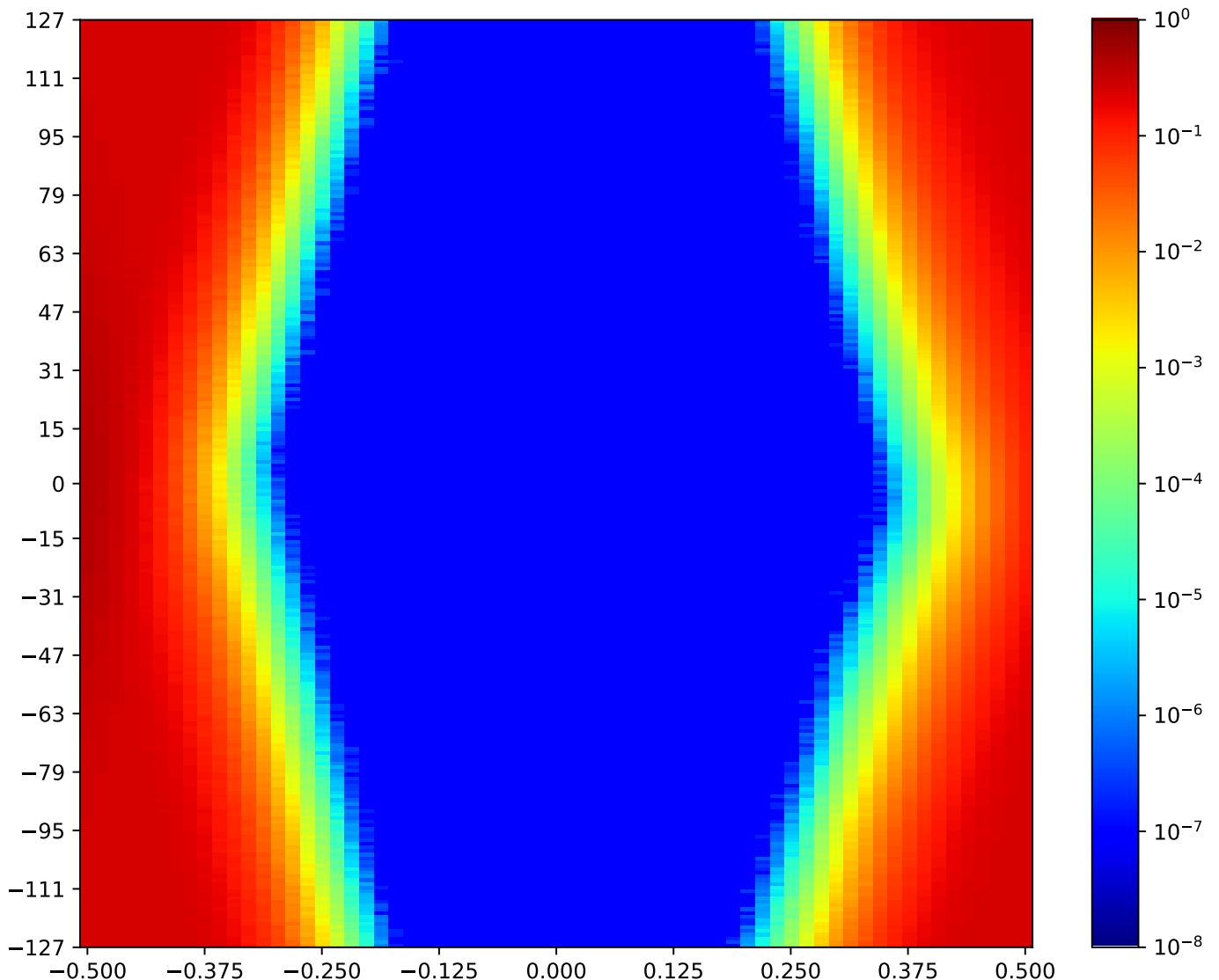


Figure 3.149: MSP\_A\_FPGA-TX2-08-RX17-08-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.10 MSP\_A\_FPGA-TX2-09-RX17-09-MSP\_C\_FPGA

Table 3.139: MSP\_A\_FPGA-TX2-09-RX17-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:33:05		2018-Jan-24 00:33:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7437	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

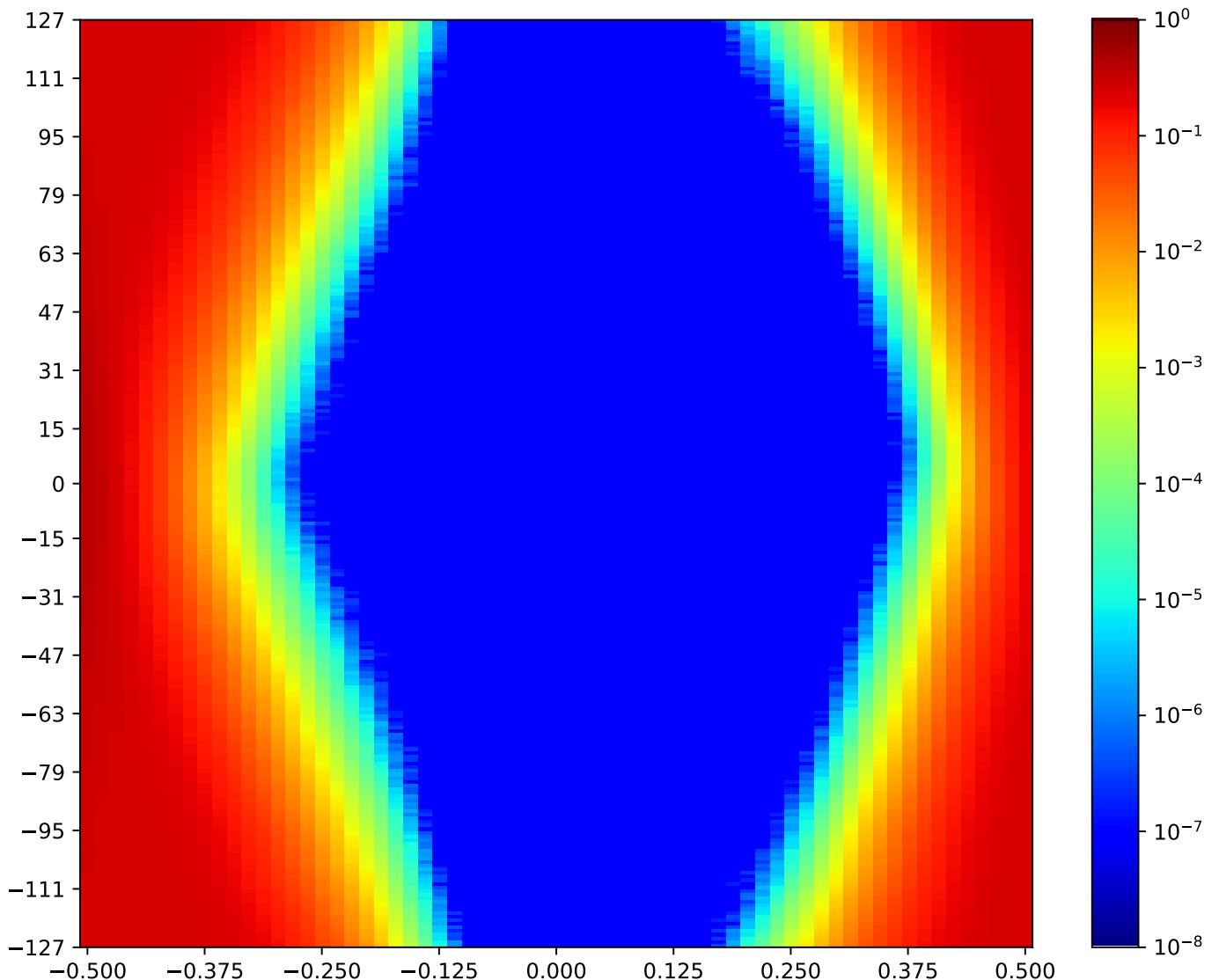


Figure 3.150: MSP\_A\_FPGA-TX2-09-RX17-09-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.11 MSP\_A\_FPGA-TX2-10-RX17-10-MSP\_C\_FPGA

Table 3.140: MSP\_A\_FPGA-TX2-10-RX17-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:34:09		2018-Jan-24 00:34:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8210	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

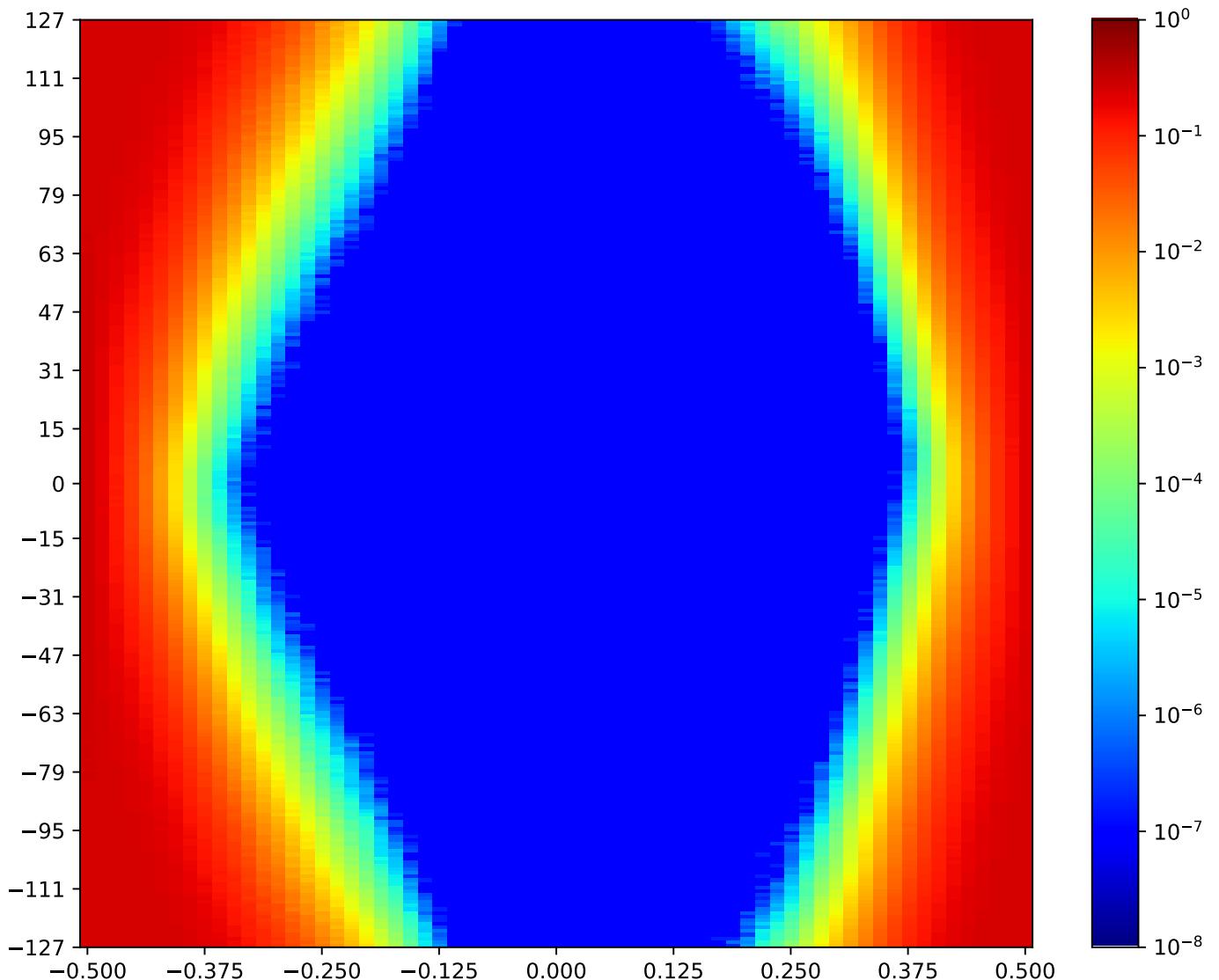


Figure 3.151: MSP\_A\_FPGA-TX2-10-RX17-10-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.11.12 MSP\_A\_FPGA-TX2-11-RX17-11-MSP\_C\_FPGA

Table 3.141: MSP\_A\_FPGA-TX2-11-RX17-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:33:48			2018-Jan-24 00:34:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7682	38	58.46%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

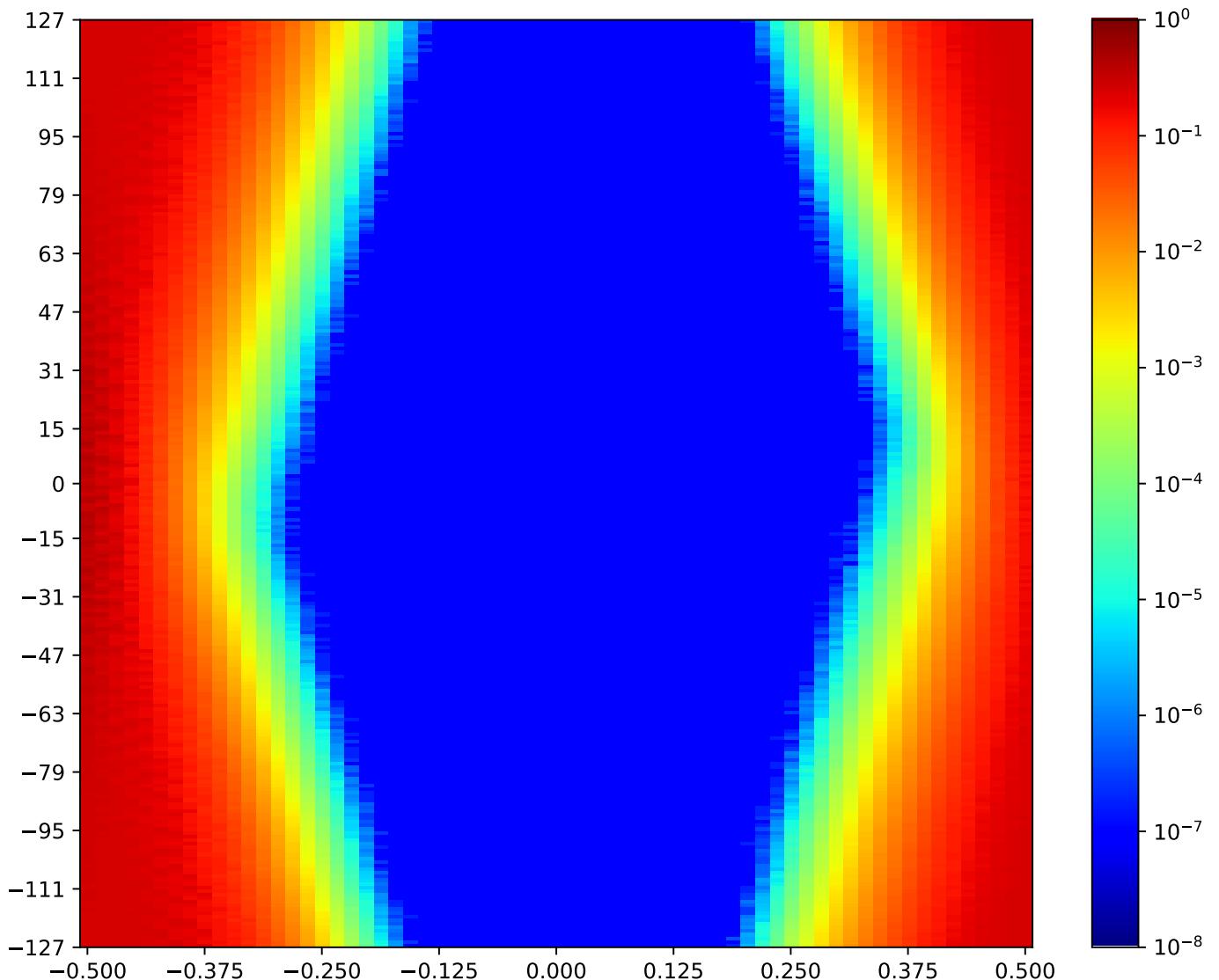


Figure 3.152: MSP\_A\_FPGA-TX2-11-RX17-11-MSP\_C\_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12 MSP\_C TX3 MSP\_A RX9 Minipod Loopback

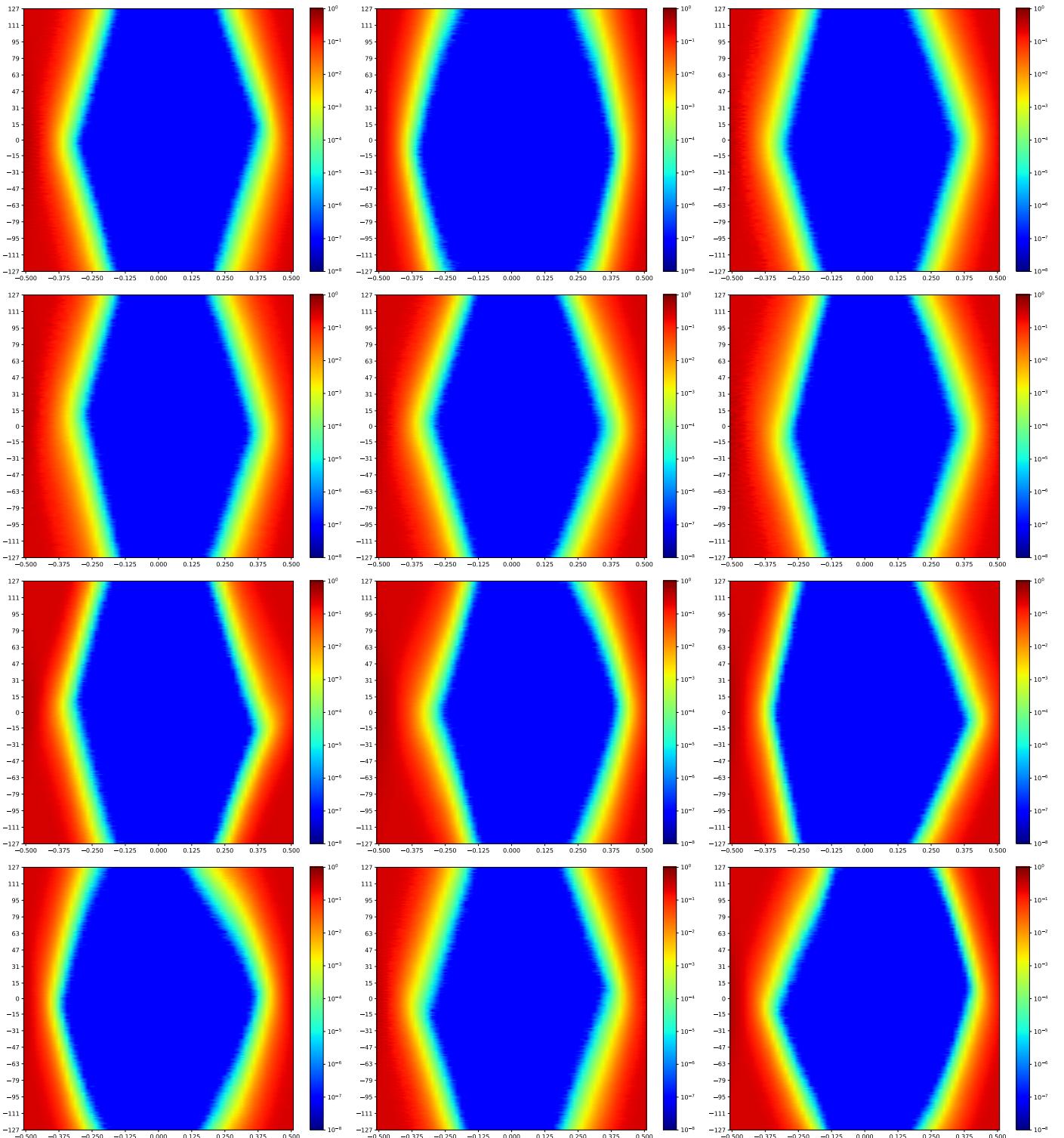


Figure 3.153: MSP\_C TX3 MSP\_A RX9 Minipod Loopback

A cross-reference to Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.166.

### 3.12.1 MSP\_C\_FPGA-TX3-00-RX9-00-MSP\_A\_FPGA

Table 3.142: MSP\_C\_FPGA-TX3-00-RX9-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:36:39		2018-Jan-24 00:37:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8023	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

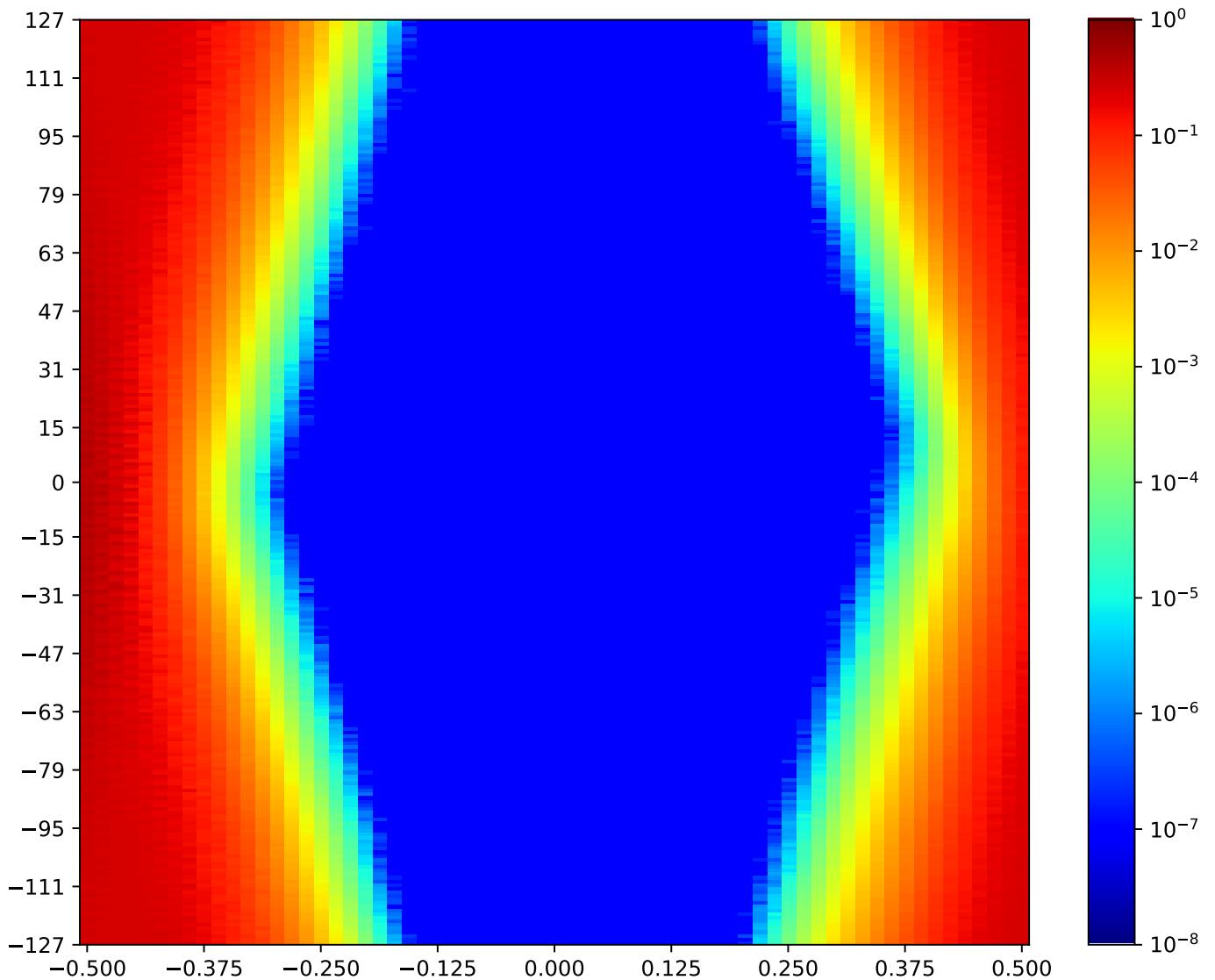


Figure 3.154: MSP\_C\_FPGA-TX3-00-RX9-00-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.2 MSP\_C\_FPGA-TX3-01-RX9-01-MSP\_A\_FPGA

Table 3.143: MSP\_C\_FPGA-TX3-01-RX9-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:37:22		2018-Jan-24 00:37:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9246	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

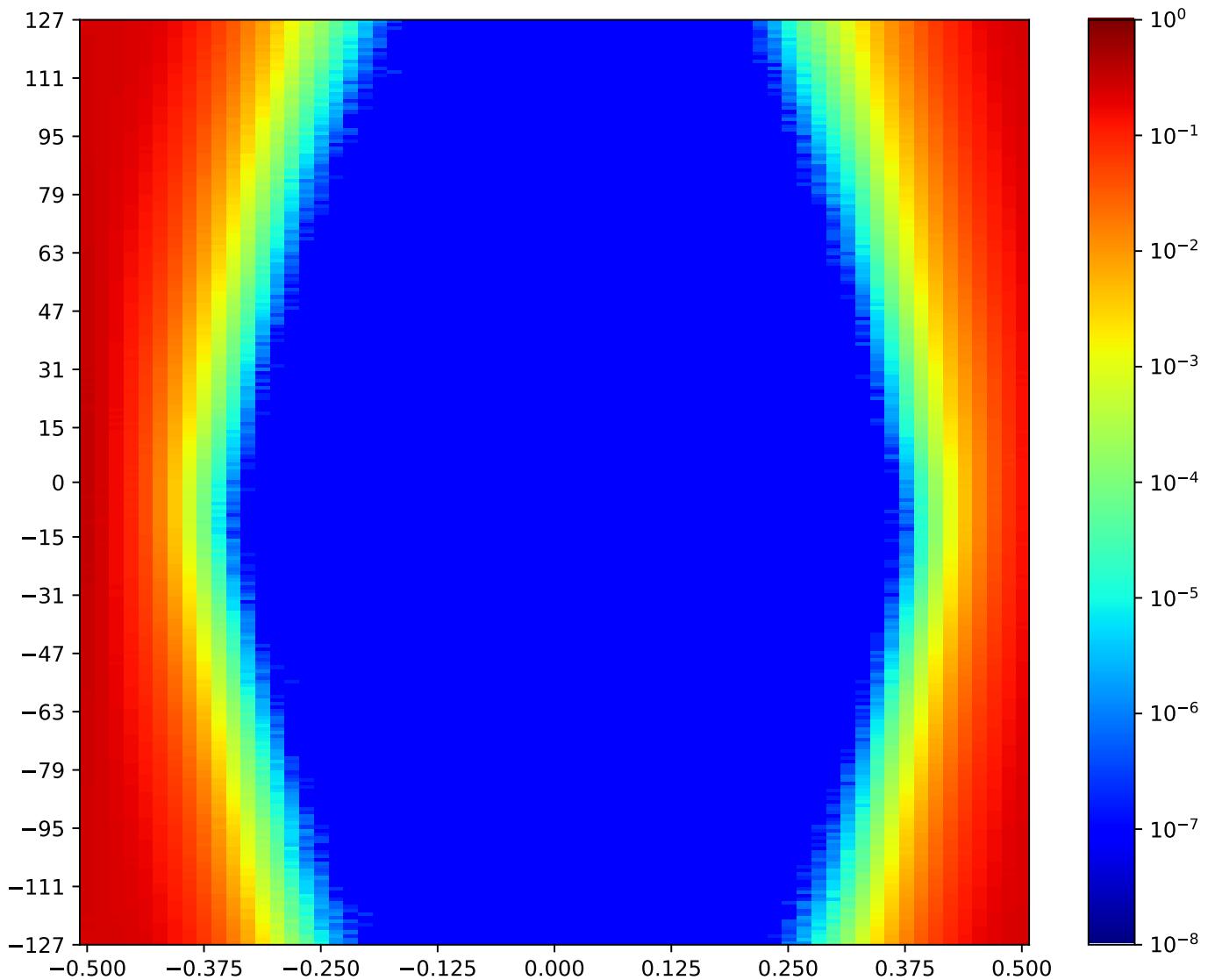


Figure 3.155: MSP\_C\_FPGA-TX3-01-RX9-01-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.3 MSP\_C\_FPGA-TX3-02-RX9-02-MSP\_A\_FPGA

Table 3.144: MSP\_C\_FPGA-TX3-02-RX9-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:37:43		2018-Jan-24 00:38:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7399	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

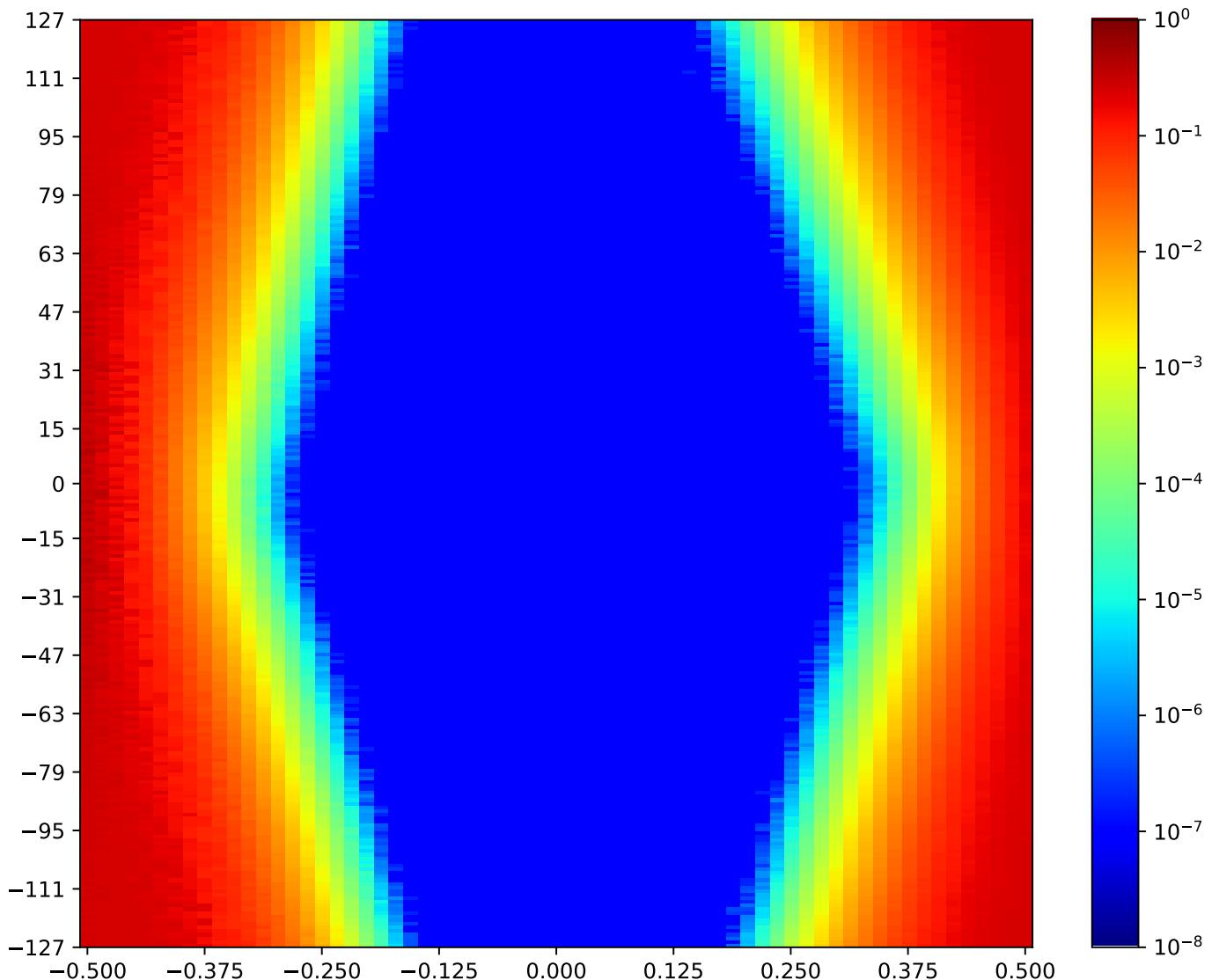


Figure 3.156: MSP\_C\_FPGA-TX3-02-RX9-02-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.4 MSP\_C\_FPGA-TX3-03-RX9-03-MSP\_A\_FPGA

Table 3.145: MSP\_C\_FPGA-TX3-03-RX9-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:35:56		2018-Jan-24 00:36:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7275	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

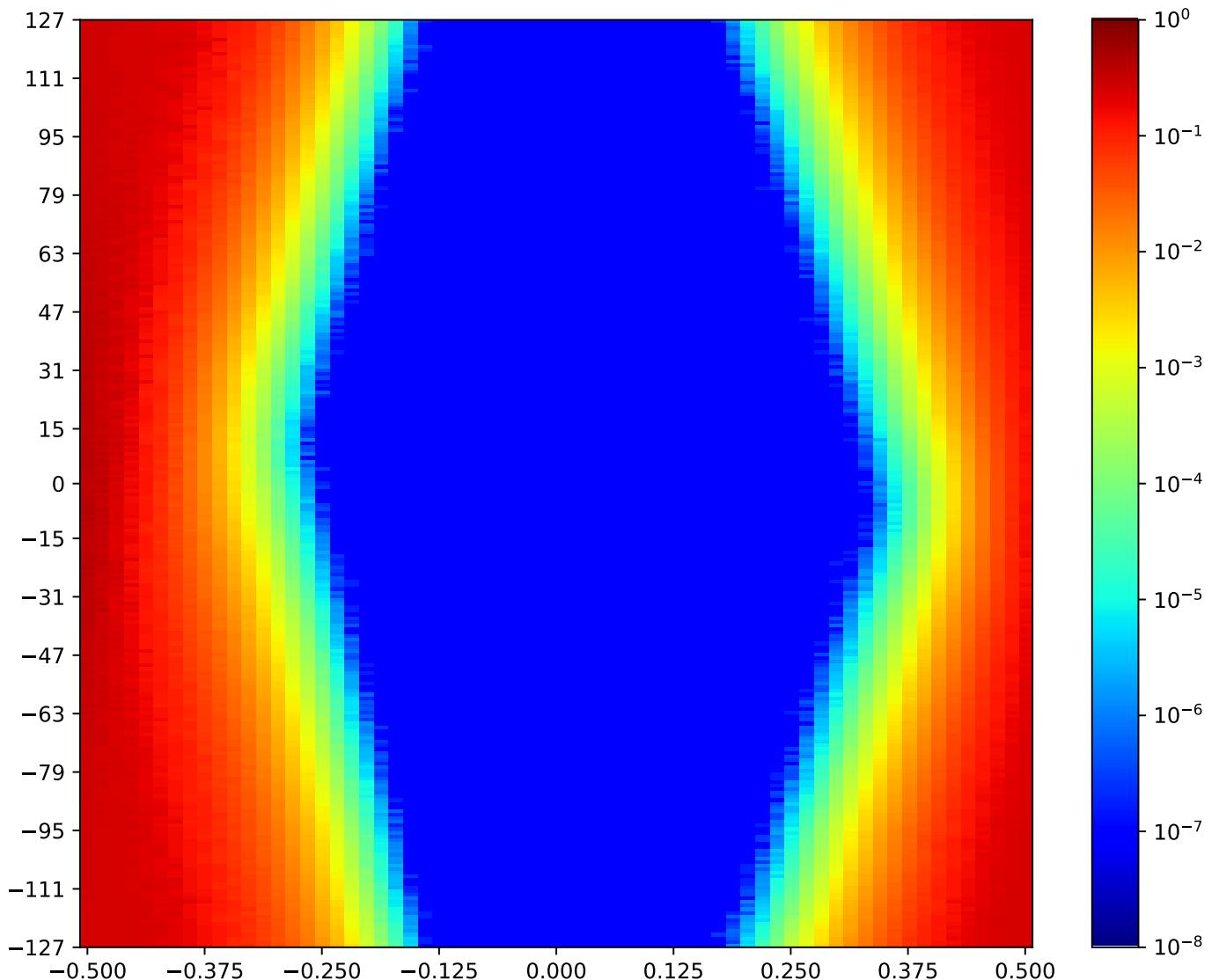


Figure 3.157: MSP\_C\_FPGA-TX3-03-RX9-03-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.5 MSP\_C\_FPGA-TX3-04-RX9-04-MSP\_A\_FPGA

Table 3.146: MSP\_C\_FPGA-TX3-04-RX9-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:38:47		2018-Jan-24 00:39:08	
Reset RX	OA	HO		HO (%)	
true	7015	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

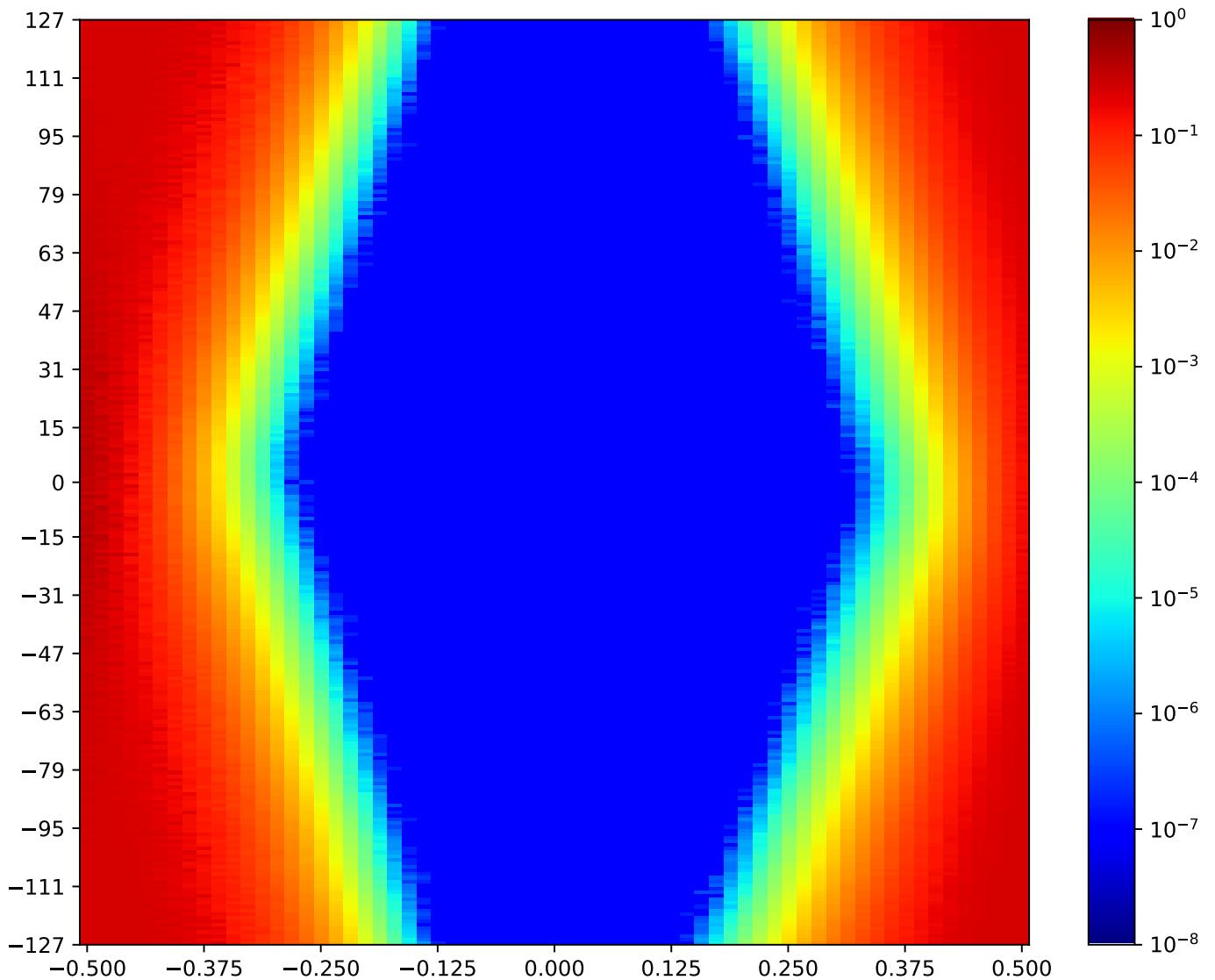


Figure 3.158: MSP\_C\_FPGA-TX3-04-RX9-04-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.6 MSP\_C\_FPGA-TX3-05-RX9-05-MSP\_A\_FPGA

Table 3.147: MSP\_C\_FPGA-TX3-05-RX9-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:35:35		2018-Jan-24 00:35:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6980	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

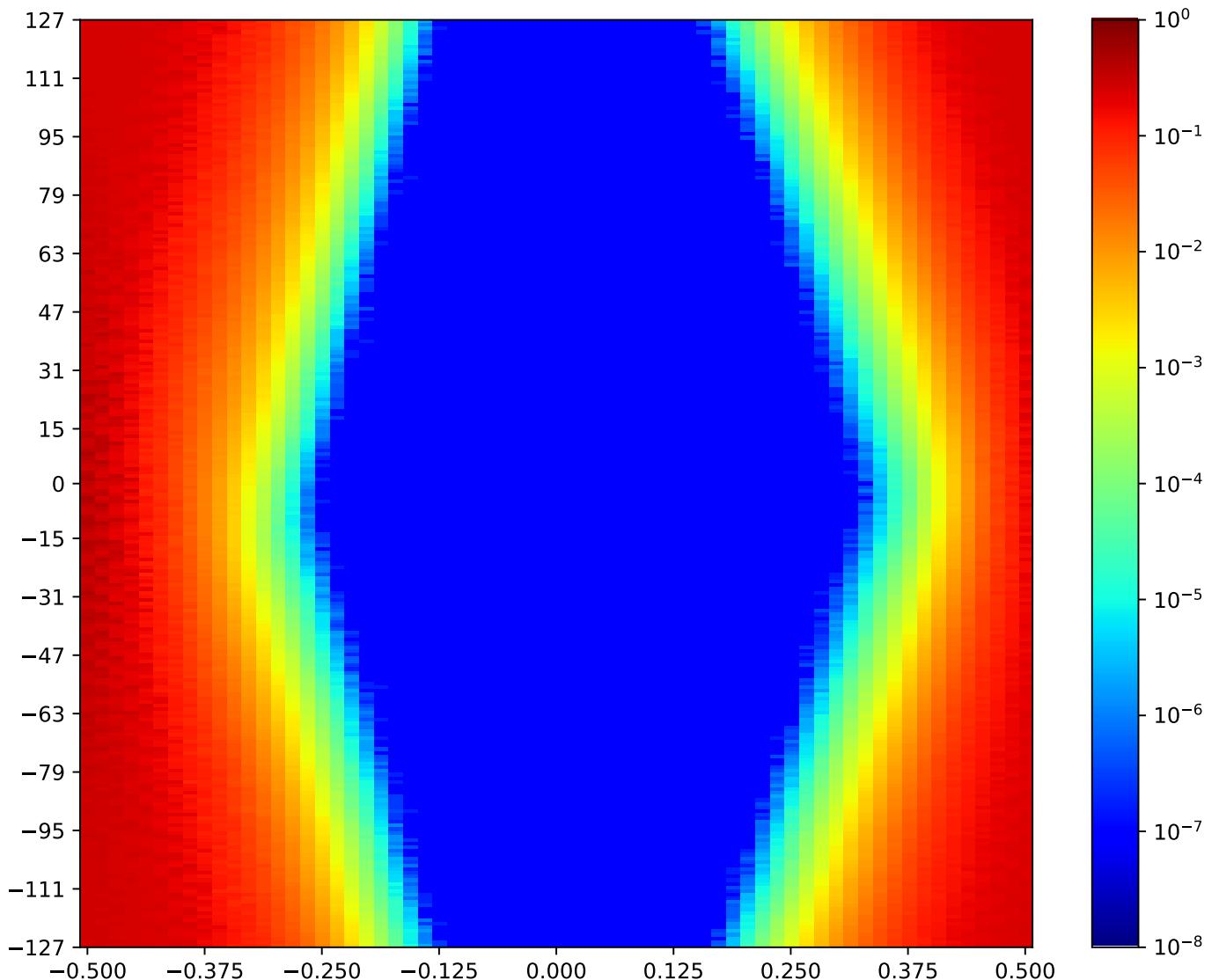


Figure 3.159: MSP\_C\_FPGA-TX3-05-RX9-05-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.7 MSP\_C\_FPGA-TX3-06-RX9-06-MSP\_A\_FPGA

Table 3.148: MSP\_C\_FPGA-TX3-06-RX9-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:39:30		2018-Jan-24 00:39:52	
Reset RX	OA	HO		HO (%)	
true	7974	40		61.54%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

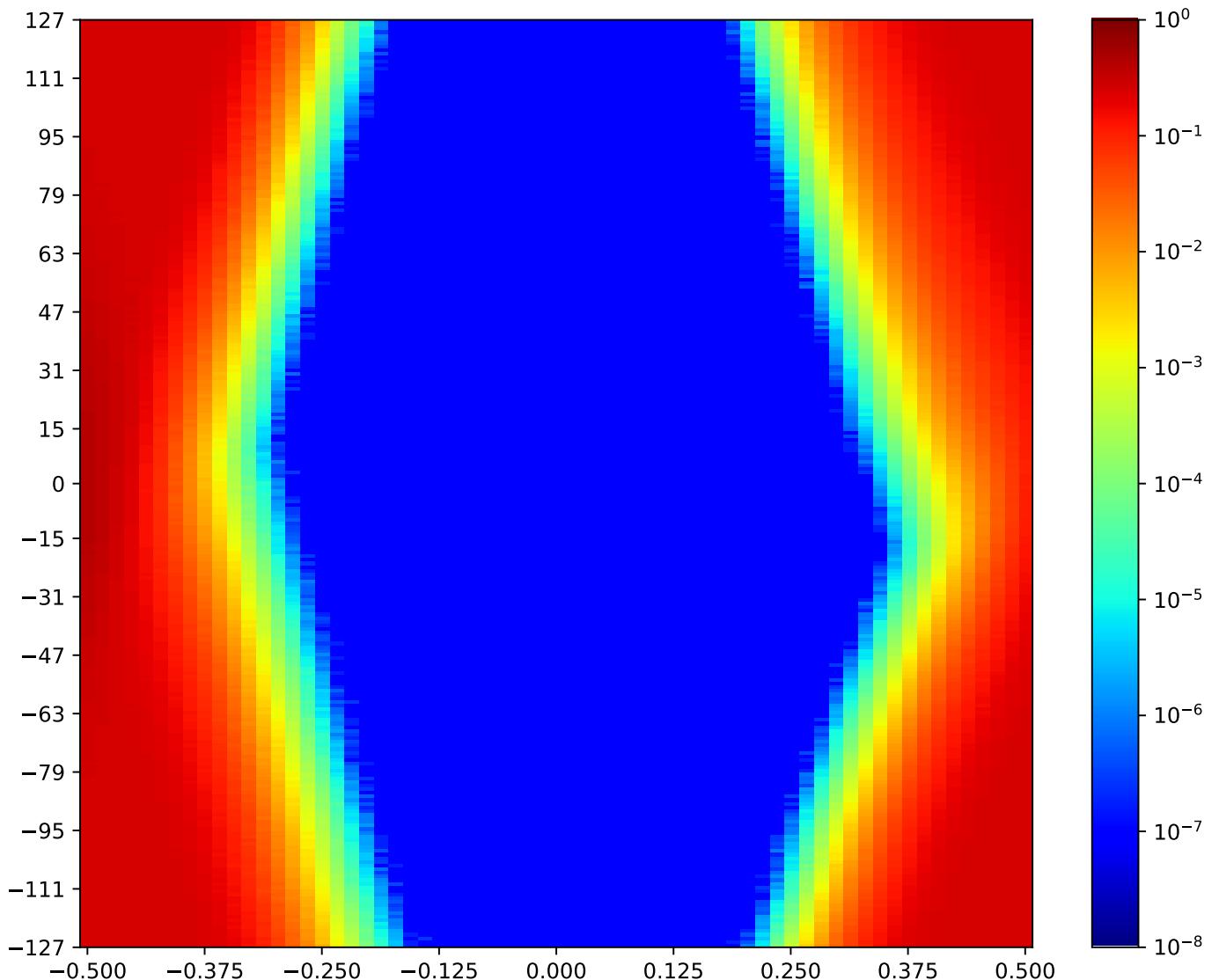


Figure 3.160: MSP\_C\_FPGA-TX3-06-RX9-06-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.8 MSP\_C\_FPGA-TX3-07-RX9-07-MSP\_A\_FPGA

Table 3.149: MSP\_C\_FPGA-TX3-07-RX9-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:36:18		2018-Jan-24 00:36:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7712	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

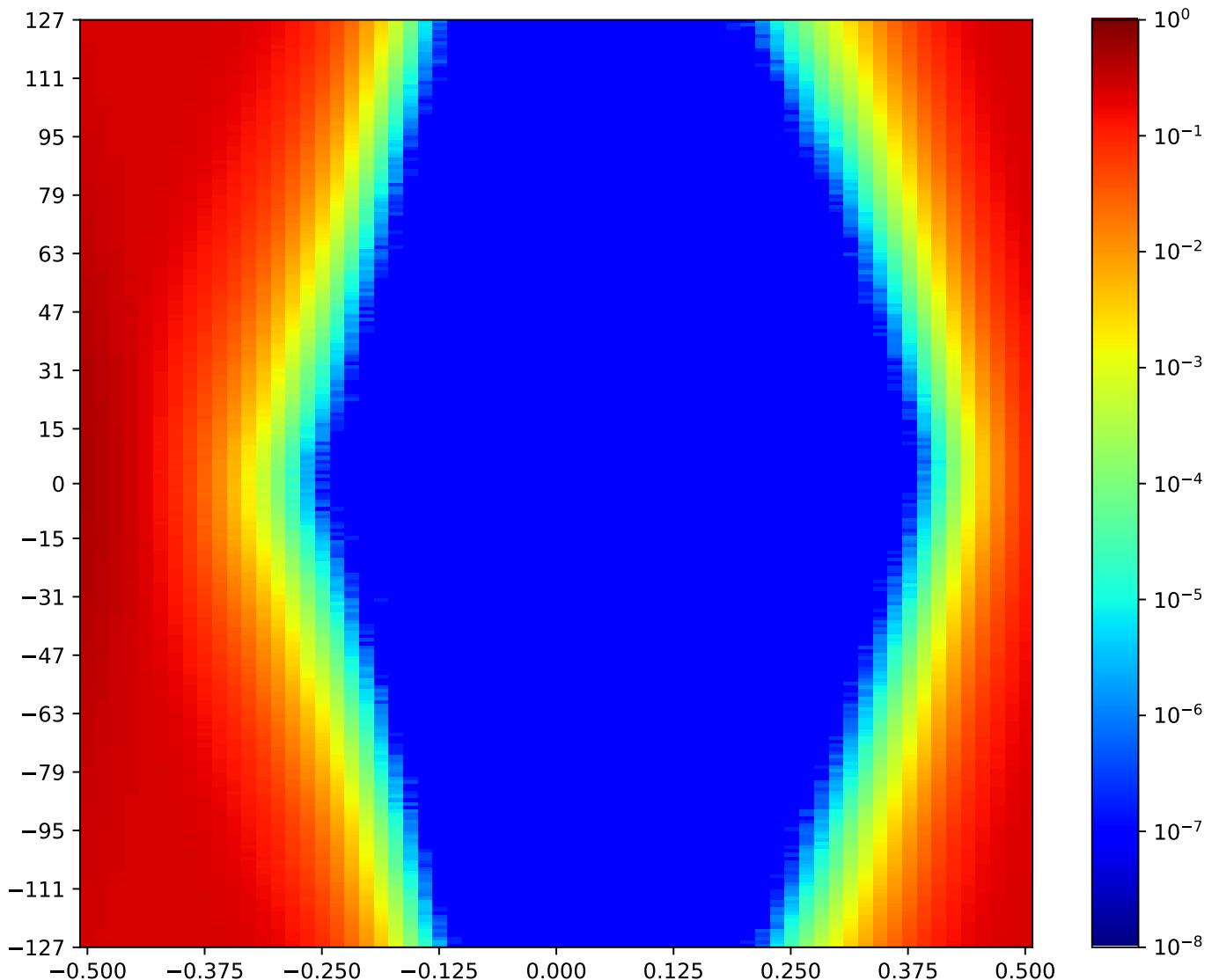


Figure 3.161: MSP\_C\_FPGA-TX3-07-RX9-07-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.9 MSP\_C\_FPGA-TX3-08-RX9-08-MSP\_A\_FPGA

Table 3.150: MSP\_C\_FPGA-TX3-08-RX9-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:39:09		2018-Jan-24 00:39:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8819	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

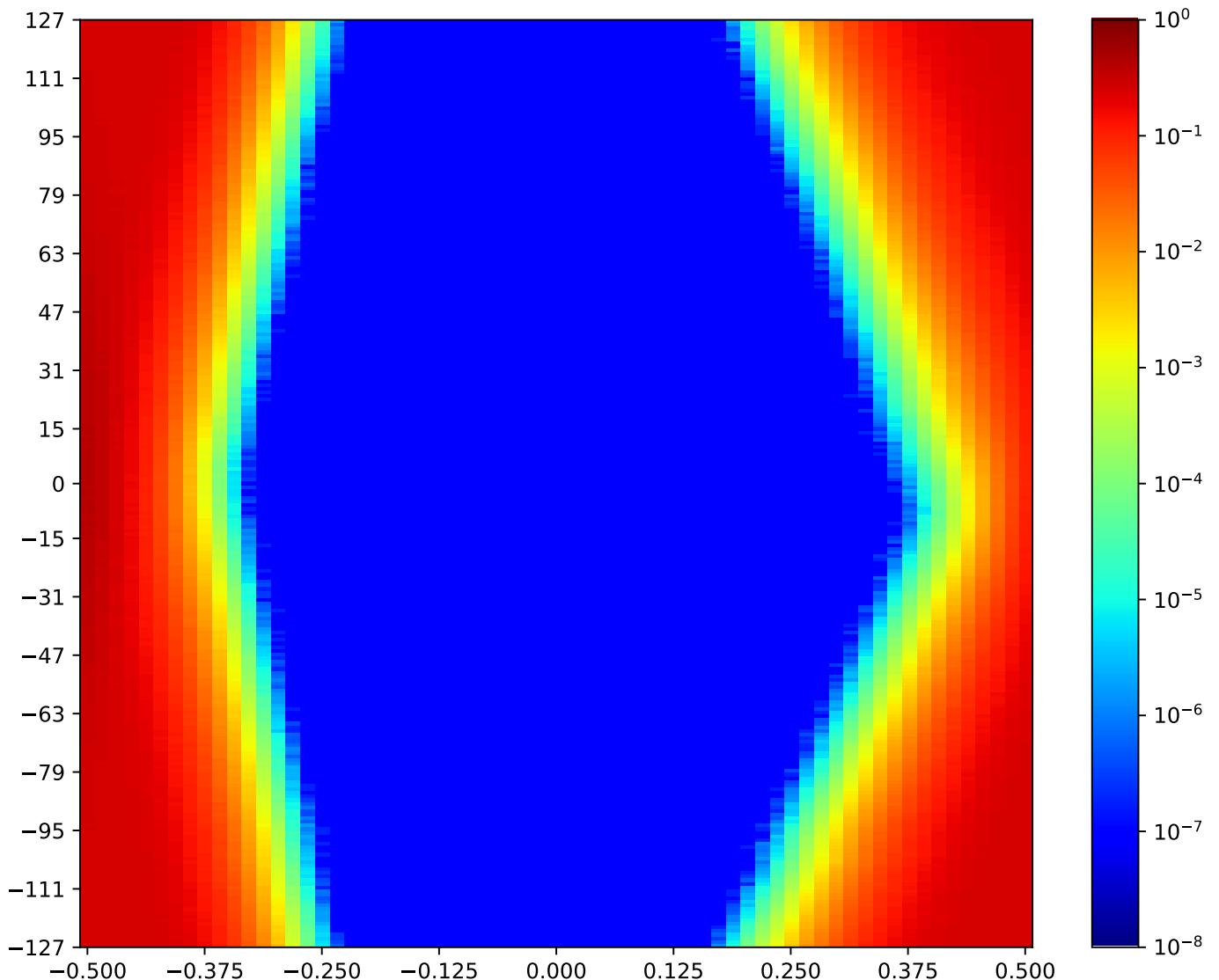


Figure 3.162: MSP\_C\_FPGA-TX3-08-RX9-08-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.10 MSP\_C\_FPGA-TX3-09-RX9-09-MSP\_A\_FPGA

Table 3.151: MSP\_C\_FPGA-TX3-09-RX9-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:37:01		2018-Jan-24 00:37:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8423	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

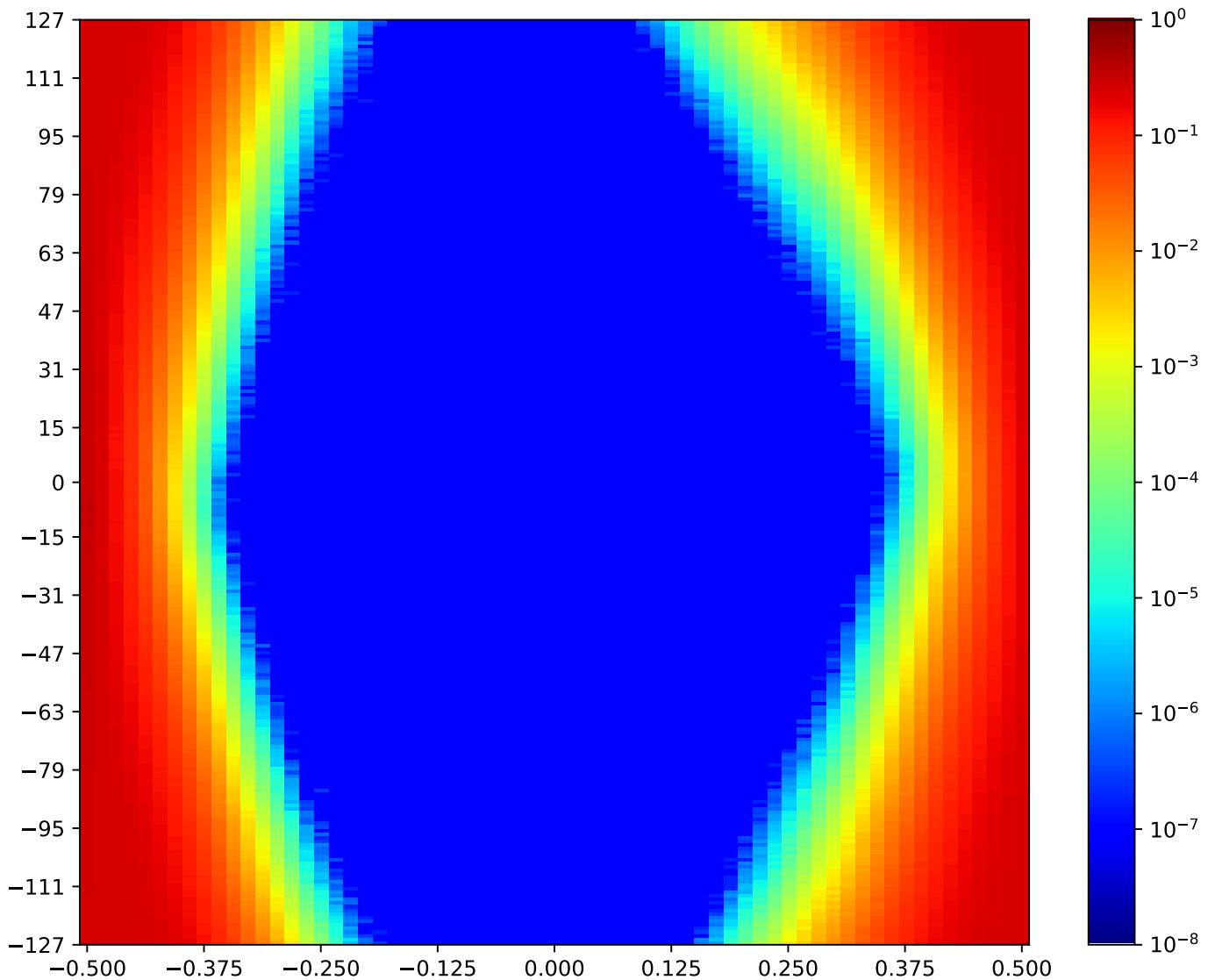


Figure 3.163: MSP\_C\_FPGA-TX3-09-RX9-09-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.11 MSP\_C\_FPGA-TX3-10-RX9-10-MSP\_A\_FPGA

Table 3.152: MSP\_C\_FPGA-TX3-10-RX9-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:38:26		2018-Jan-24 00:38:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7521	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

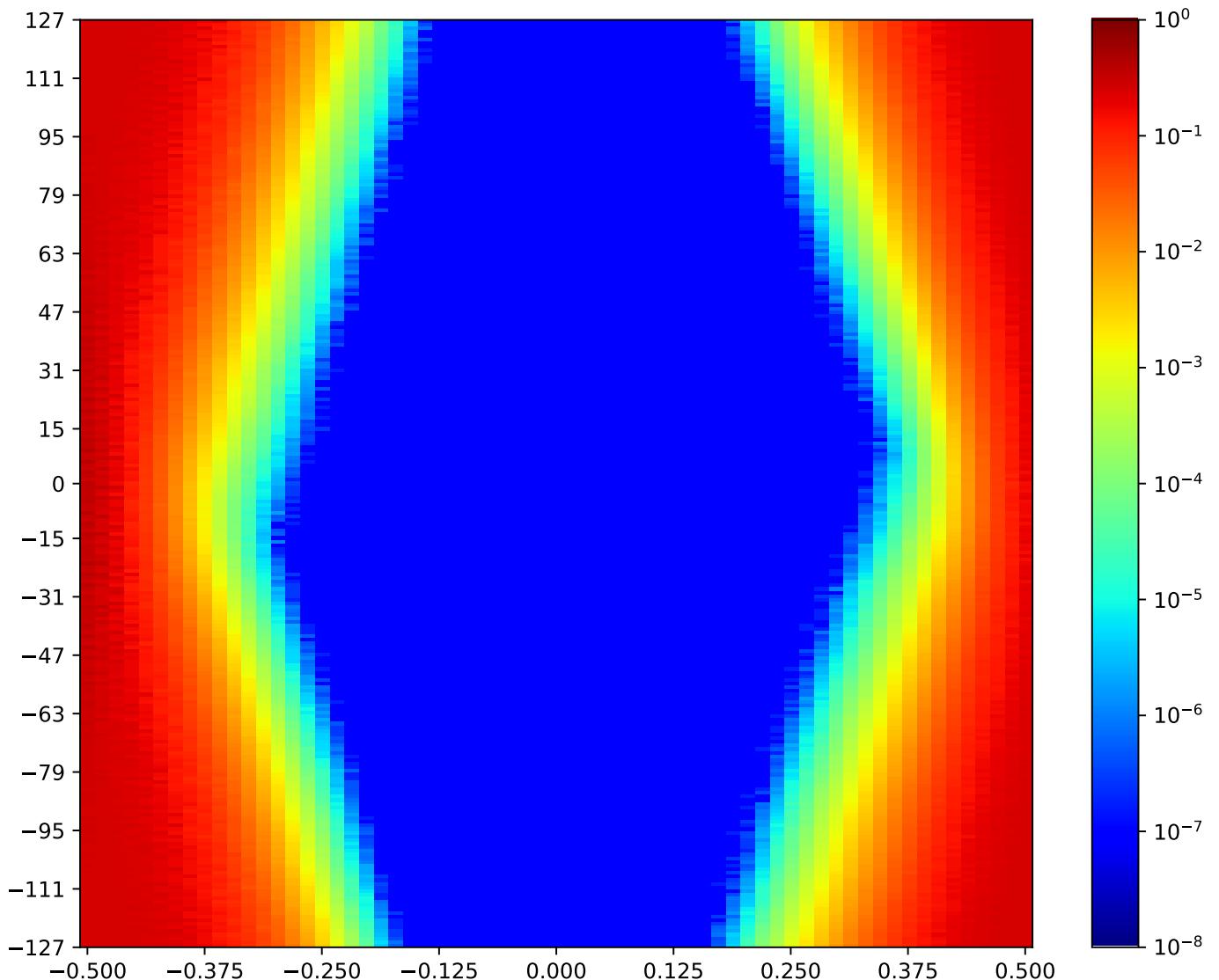


Figure 3.164: MSP\_C\_FPGA-TX3-10-RX9-10-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.12.12 MSP\_C\_FPGA-TX3-11-RX9-11-MSP\_A\_FPGA

Table 3.153: MSP\_C\_FPGA-TX3-11-RX9-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:38:05		2018-Jan-24 00:38:26	
Reset RX	OA	HO		HO (%)	
true	8226	42		64.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

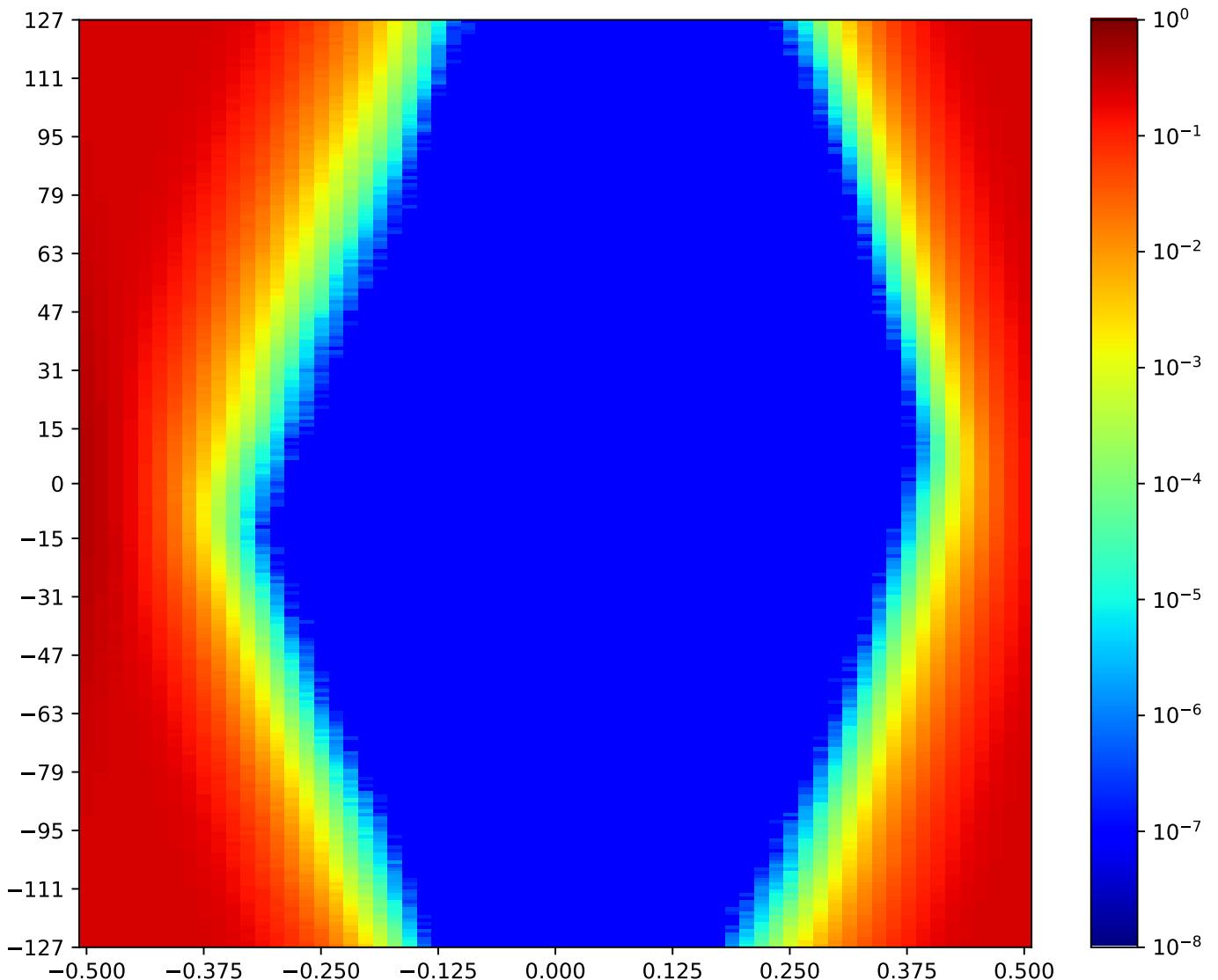


Figure 3.165: MSP\_C\_FPGA-TX3-11-RX9-11-MSP\_A\_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13 MSP\_C TX4 MSP\_A RX8 Minipod Loopback

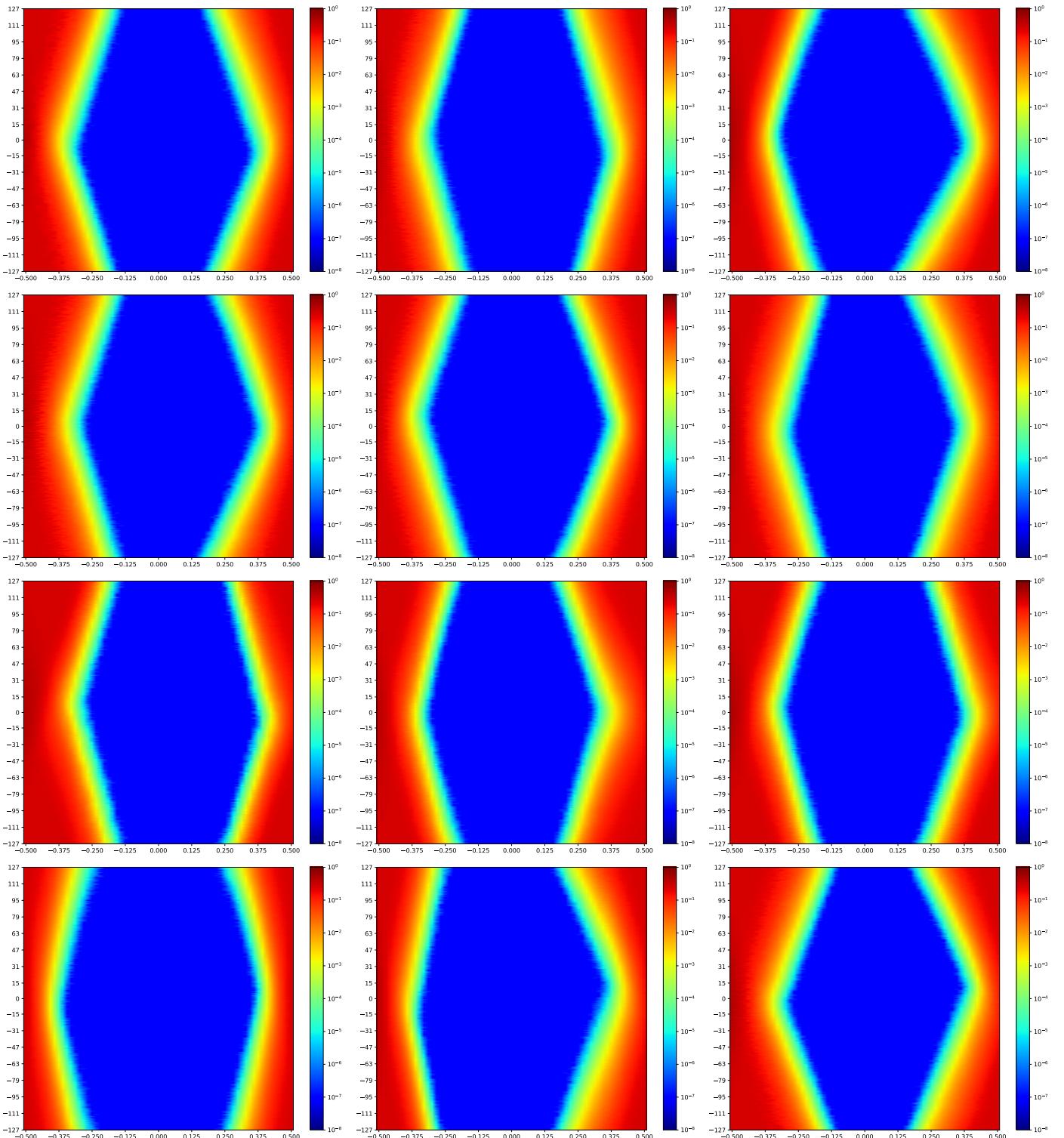


Figure 3.166: MSP\_C TX4 MSP\_A RX8 Minipod Loopback

A cross-reference to Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.179.

### 3.13.1 MSP\_C\_FPGA-TX4-00-RX8-00-MSP\_A\_FPGA

Table 3.154: MSP\_C\_FPGA-TX4-00-RX8-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:40:55		2018-Jan-24 00:41:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7377	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

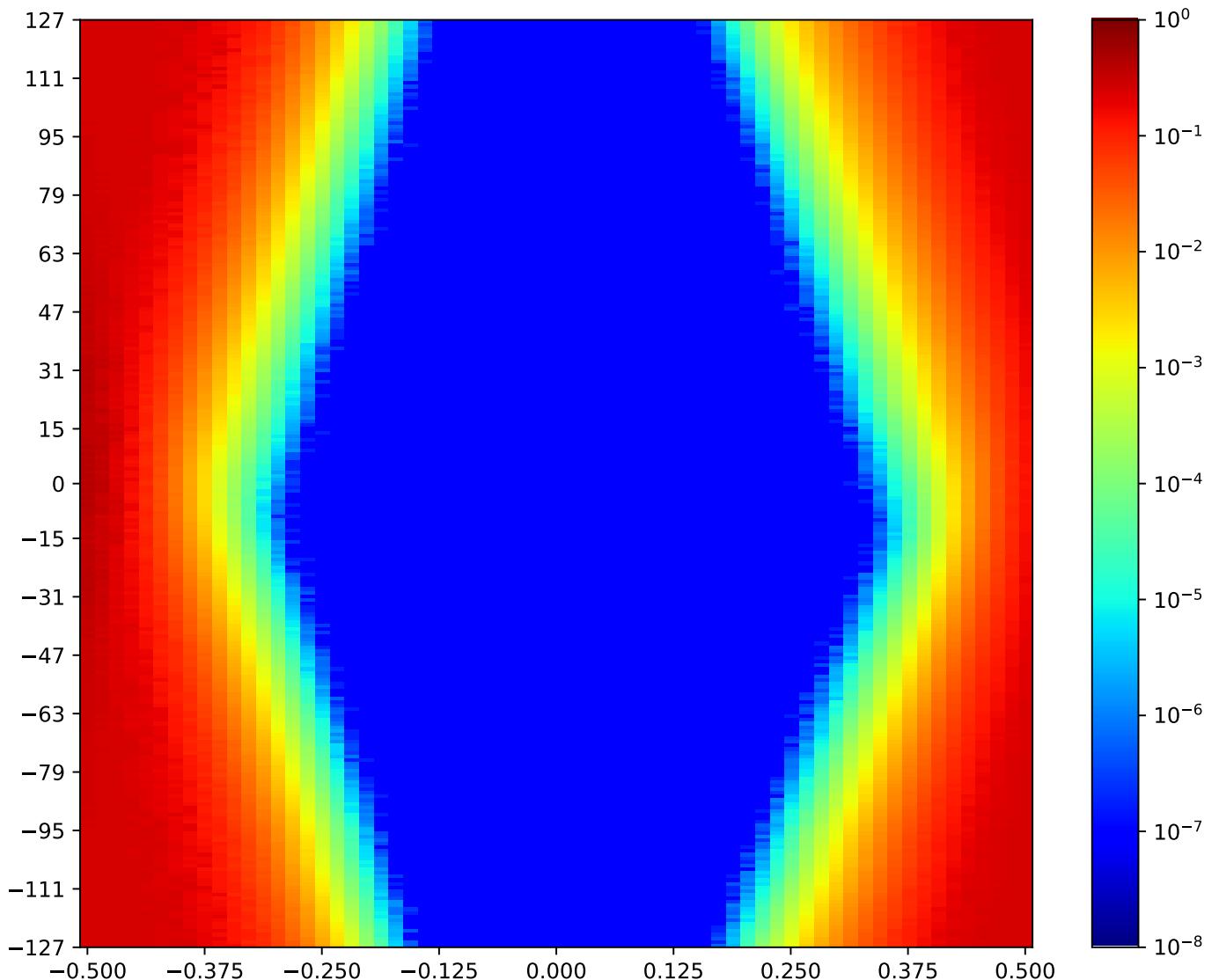


Figure 3.167: MSP\_C\_FPGA-TX4-00-RX8-00-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.2 MSP\_C\_FPGA-TX4-01-RX8-01-MSP\_A\_FPGA

Table 3.155: MSP\_C\_FPGA-TX4-01-RX8-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:40:13		2018-Jan-24 00:40:34	
Reset RX	OA	HO		HO (%)	
true	7590	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

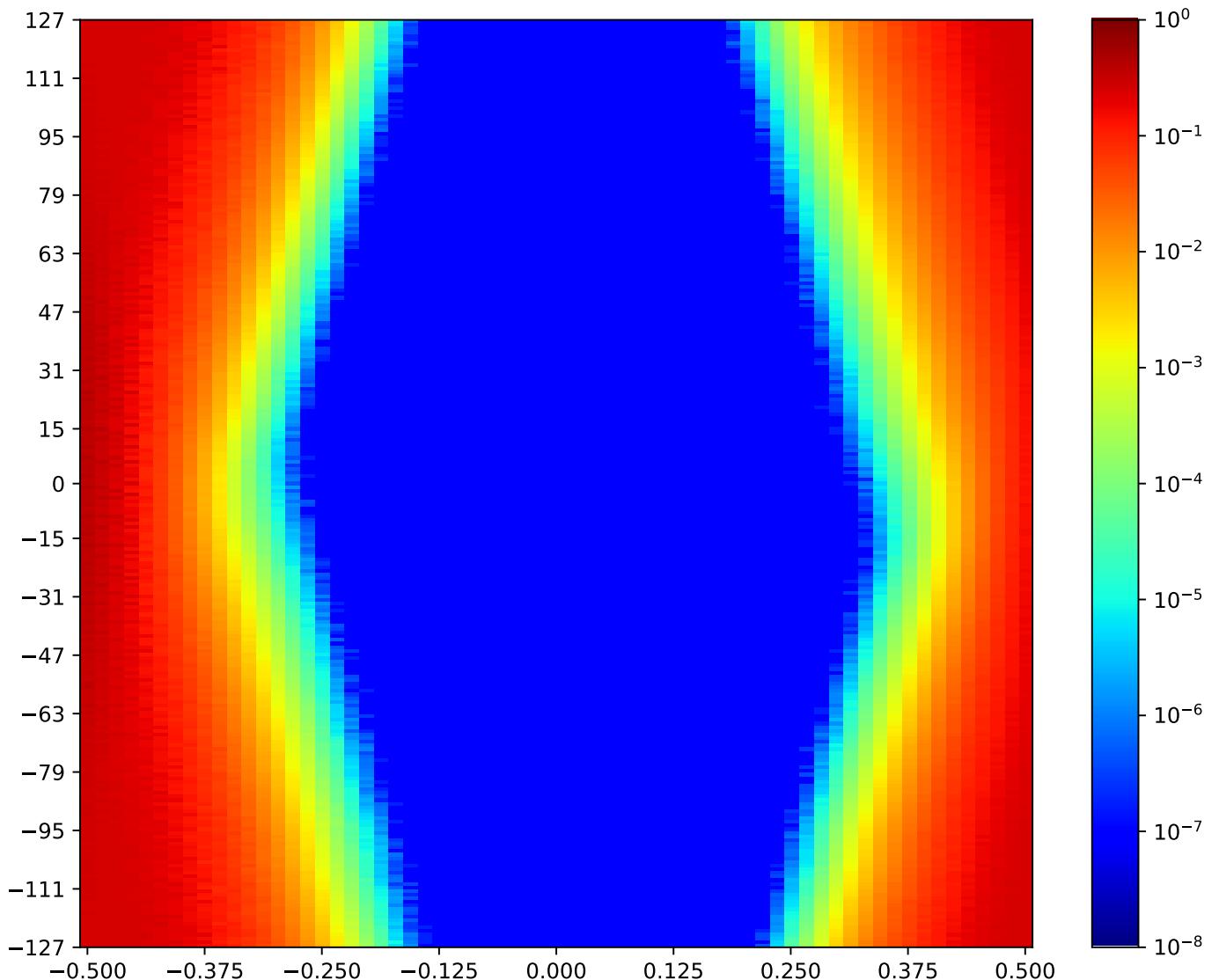


Figure 3.168: MSP\_C\_FPGA-TX4-01-RX8-01-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.3 MSP\_C\_FPGA-TX4-02-RX8-02-MSP\_A\_FPGA

Table 3.156: MSP\_C\_FPGA-TX4-02-RX8-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:41:59		2018-Jan-24 00:42:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7354	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

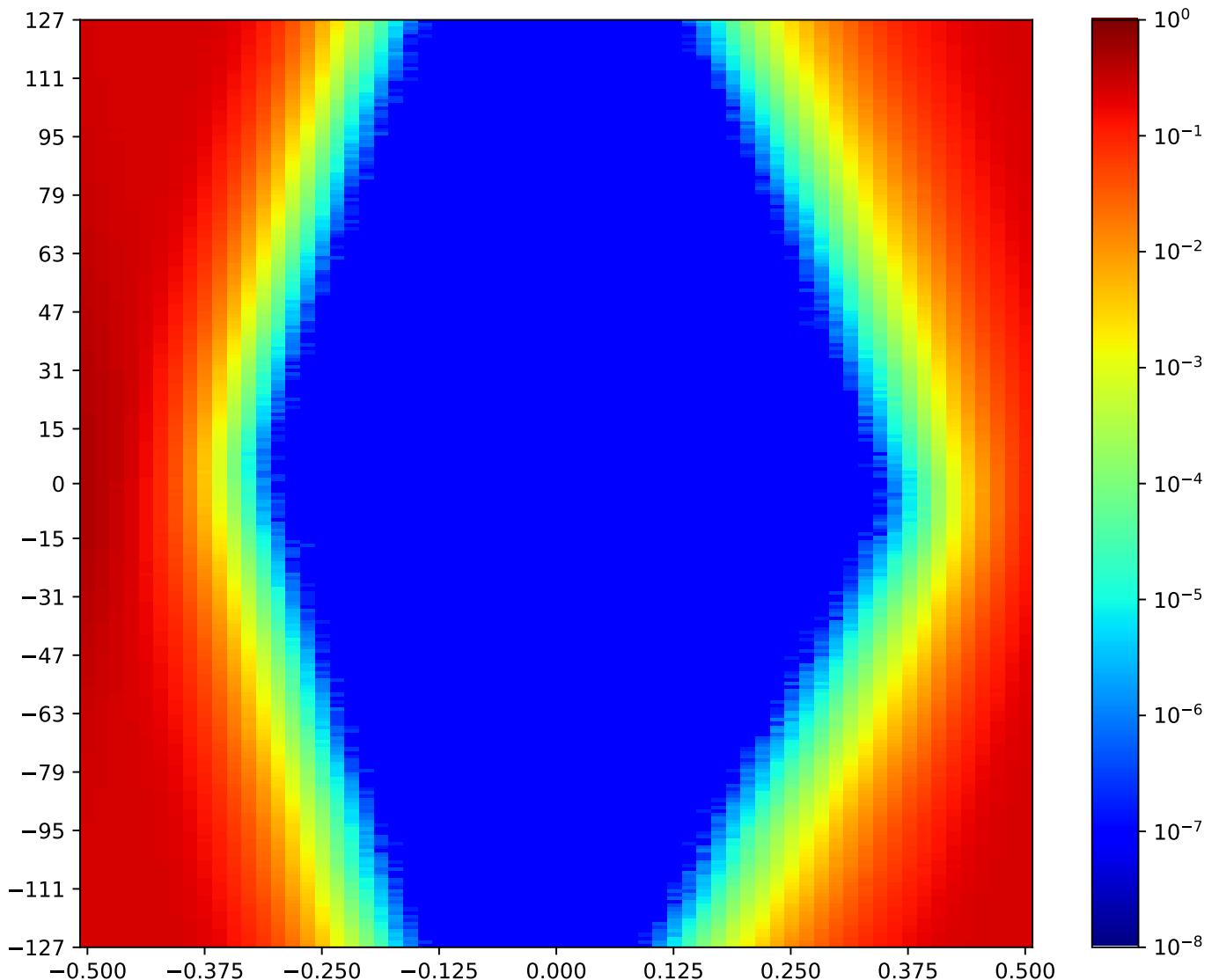


Figure 3.169: MSP\_C\_FPGA-TX4-02-RX8-02-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.4 MSP\_C\_FPGA-TX4-03-RX8-03-MSP\_A\_FPGA

Table 3.157: MSP\_C\_FPGA-TX4-03-RX8-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:39:52		2018-Jan-24 00:40:13	
Reset RX	OA	HO		HO (%)	
true	7256	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

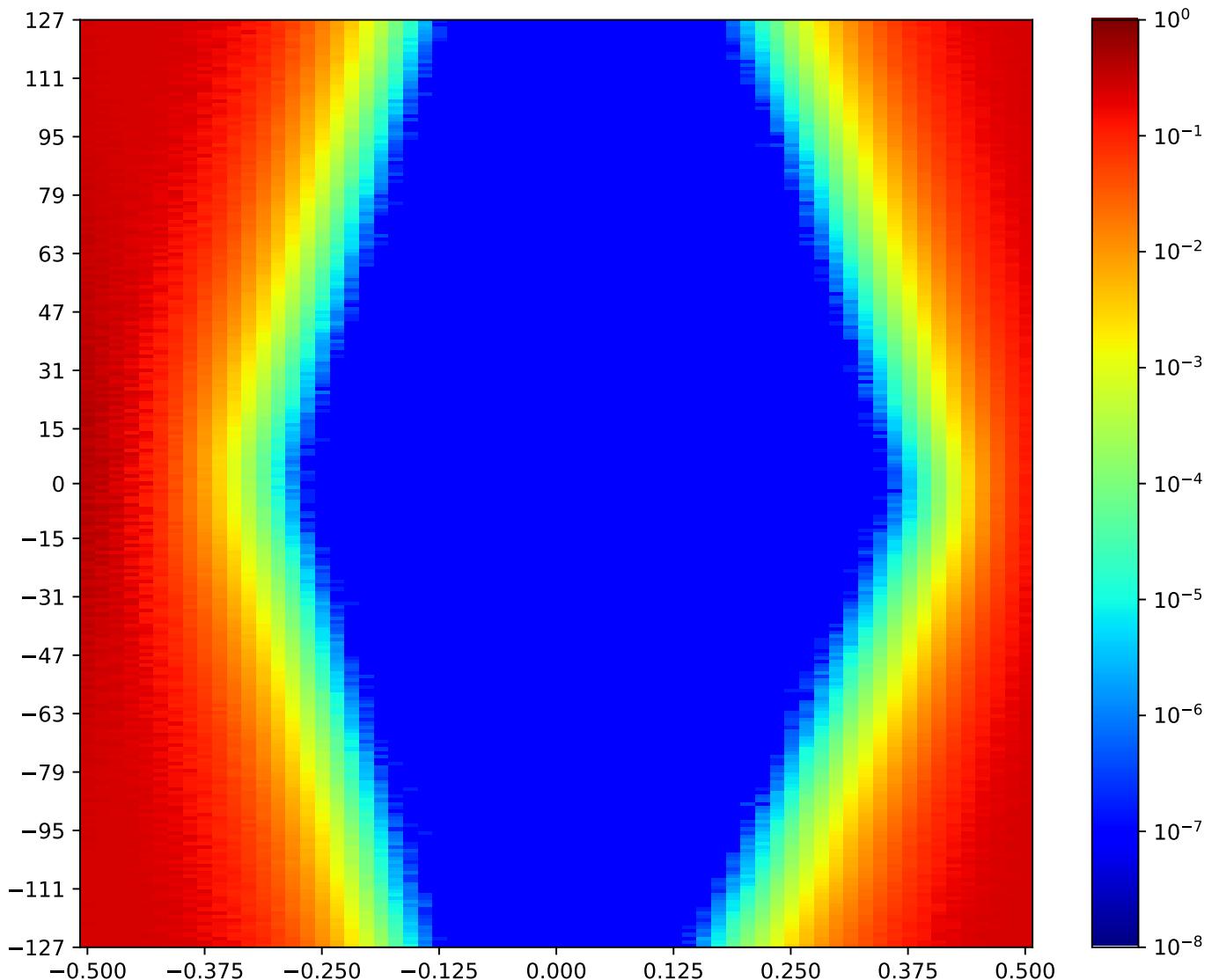


Figure 3.170: MSP\_C\_FPGA-TX4-03-RX8-03-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.5 MSP\_C\_FPGA-TX4-04-RX8-04-MSP\_A\_FPGA

Table 3.158: MSP\_C\_FPGA-TX4-04-RX8-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:43:03		2018-Jan-24 00:43:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7584	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

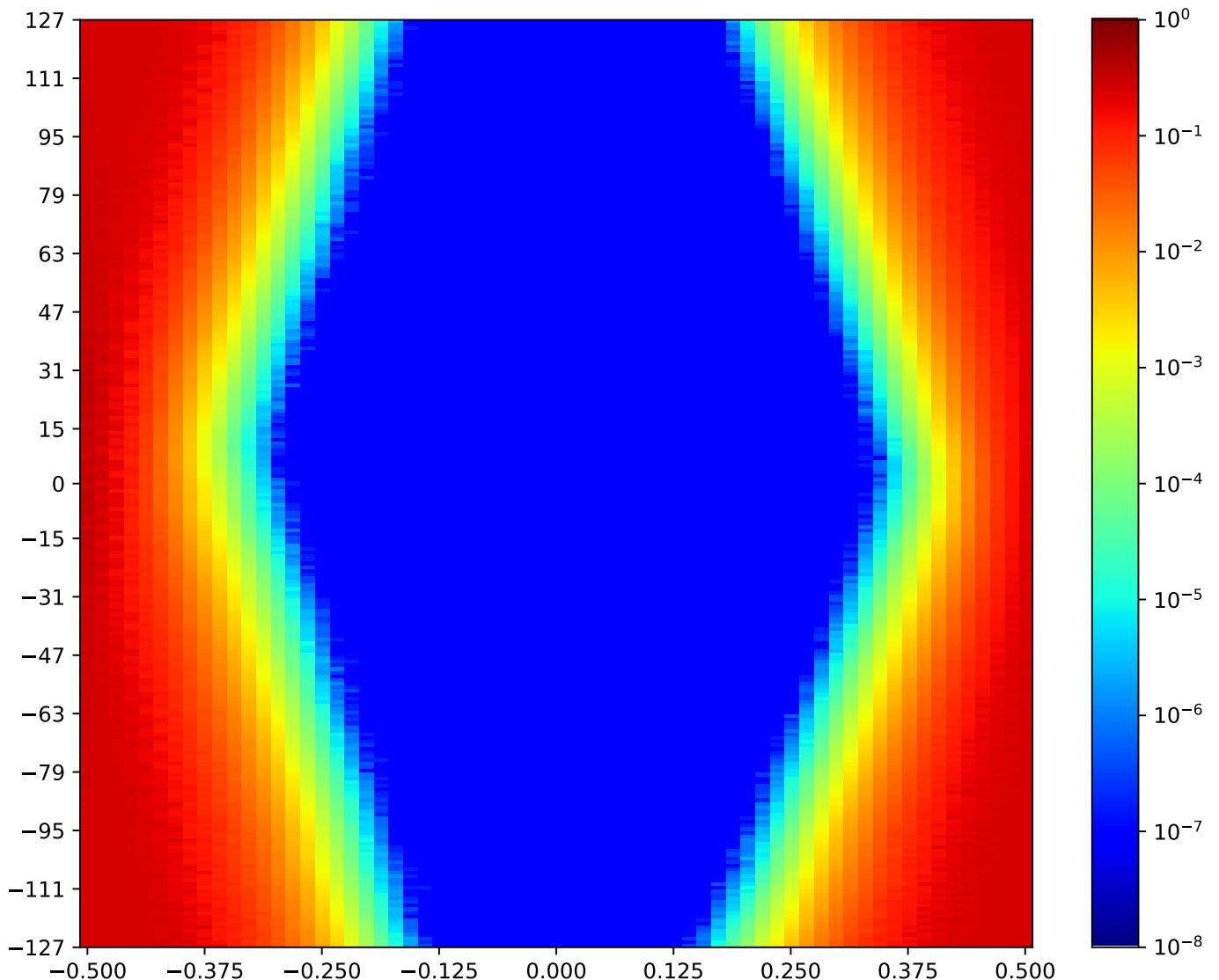


Figure 3.171: MSP\_C\_FPGA-TX4-04-RX8-04-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.6 MSP\_C\_FPGA-TX4-05-RX8-05-MSP\_A\_FPGA

Table 3.159: MSP\_C\_FPGA-TX4-05-RX8-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:40:34		2018-Jan-24 00:40:55	
Reset RX	OA	HO		HO (%)	
true	6895	36		55.38%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

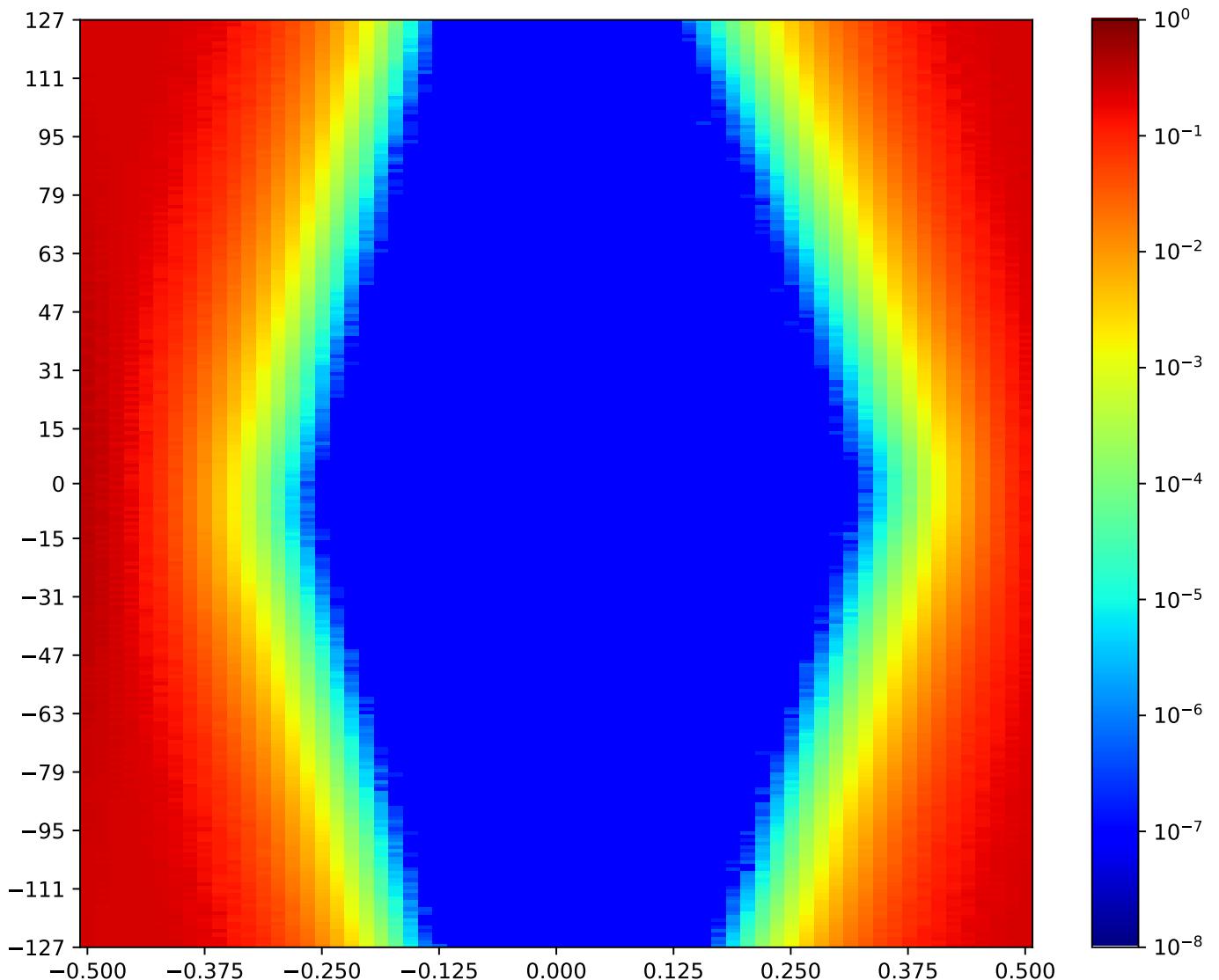


Figure 3.172: MSP\_C\_FPGA-TX4-05-RX8-05-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.7 MSP\_C\_FPGA-TX4-06-RX8-06-MSP\_A\_FPGA

Table 3.160: MSP\_C\_FPGA-TX4-06-RX8-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:43:46		2018-Jan-24 00:44:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7888	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

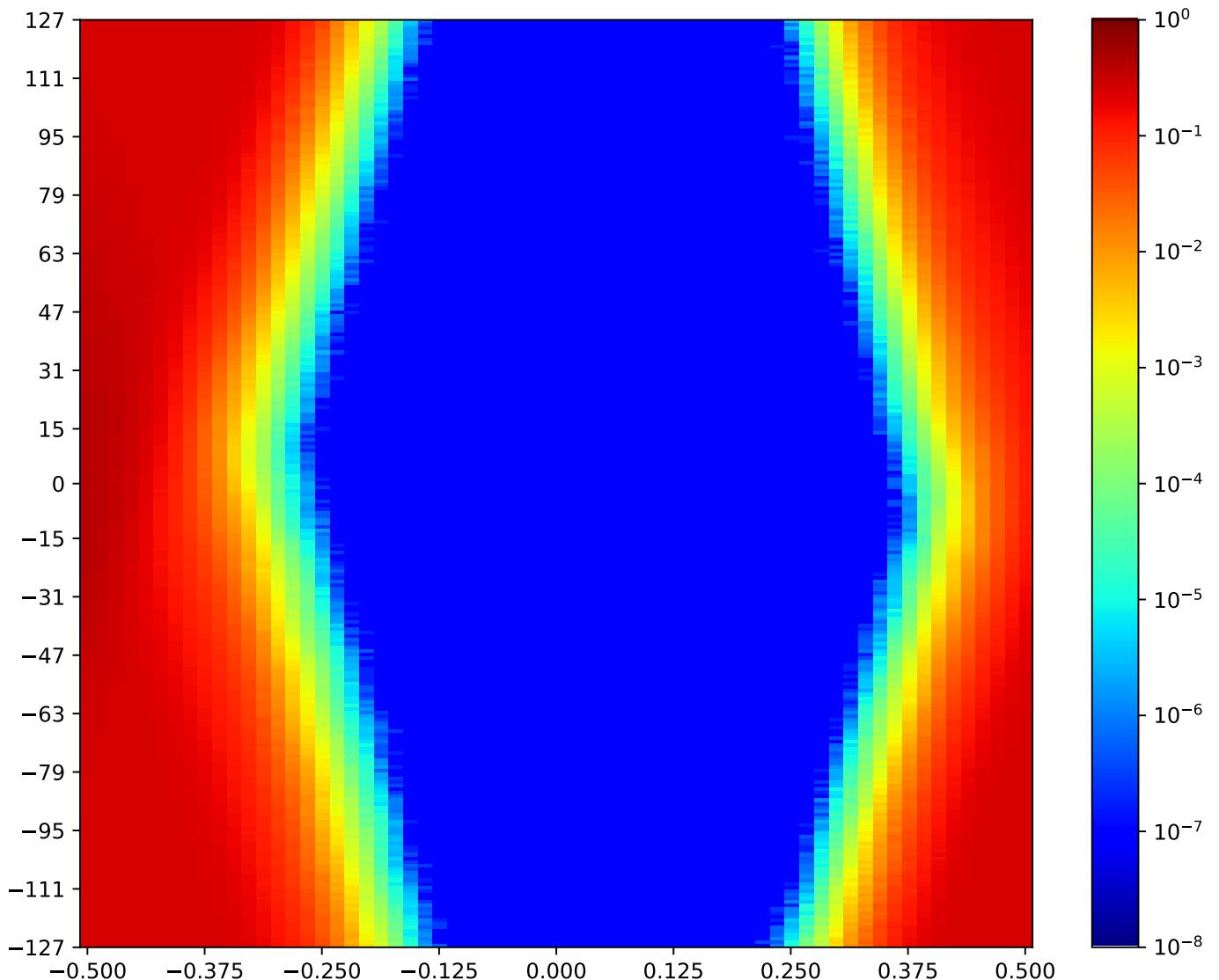


Figure 3.173: MSP\_C\_FPGA-TX4-06-RX8-06-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.8 MSP\_C\_FPGA-TX4-07-RX8-07-MSP\_A\_FPGA

Table 3.161: MSP\_C\_FPGA-TX4-07-RX8-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:41:17		2018-Jan-24 00:41:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7517	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

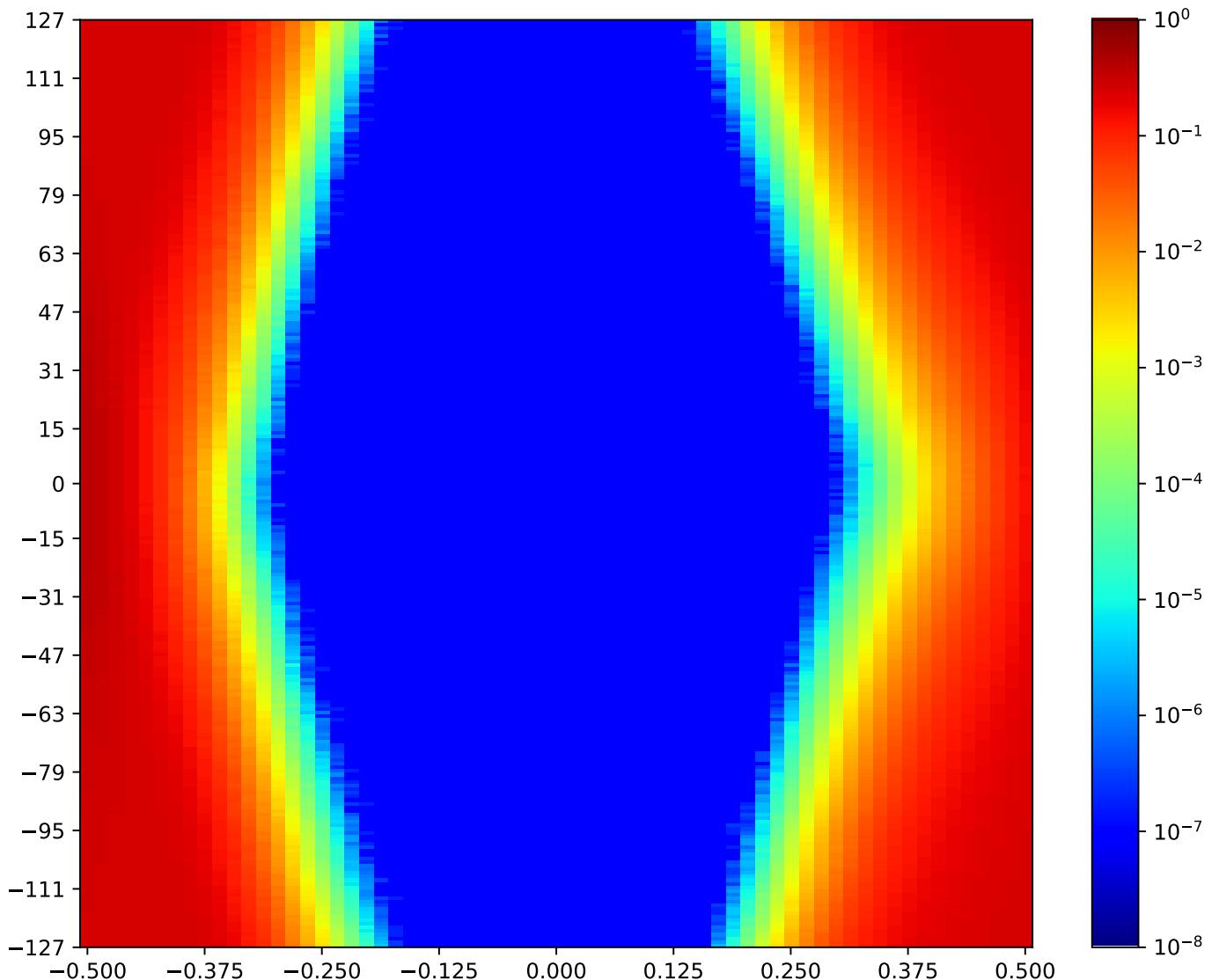


Figure 3.174: MSP\_C\_FPGA-TX4-07-RX8-07-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.9 MSP\_C\_FPGA-TX4-08-RX8-08-MSP\_A\_FPGA

Table 3.162: MSP\_C\_FPGA-TX4-08-RX8-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:43:24		2018-Jan-24 00:43:45	
Reset RX	OA	HO		HO (%)	
true	7816	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

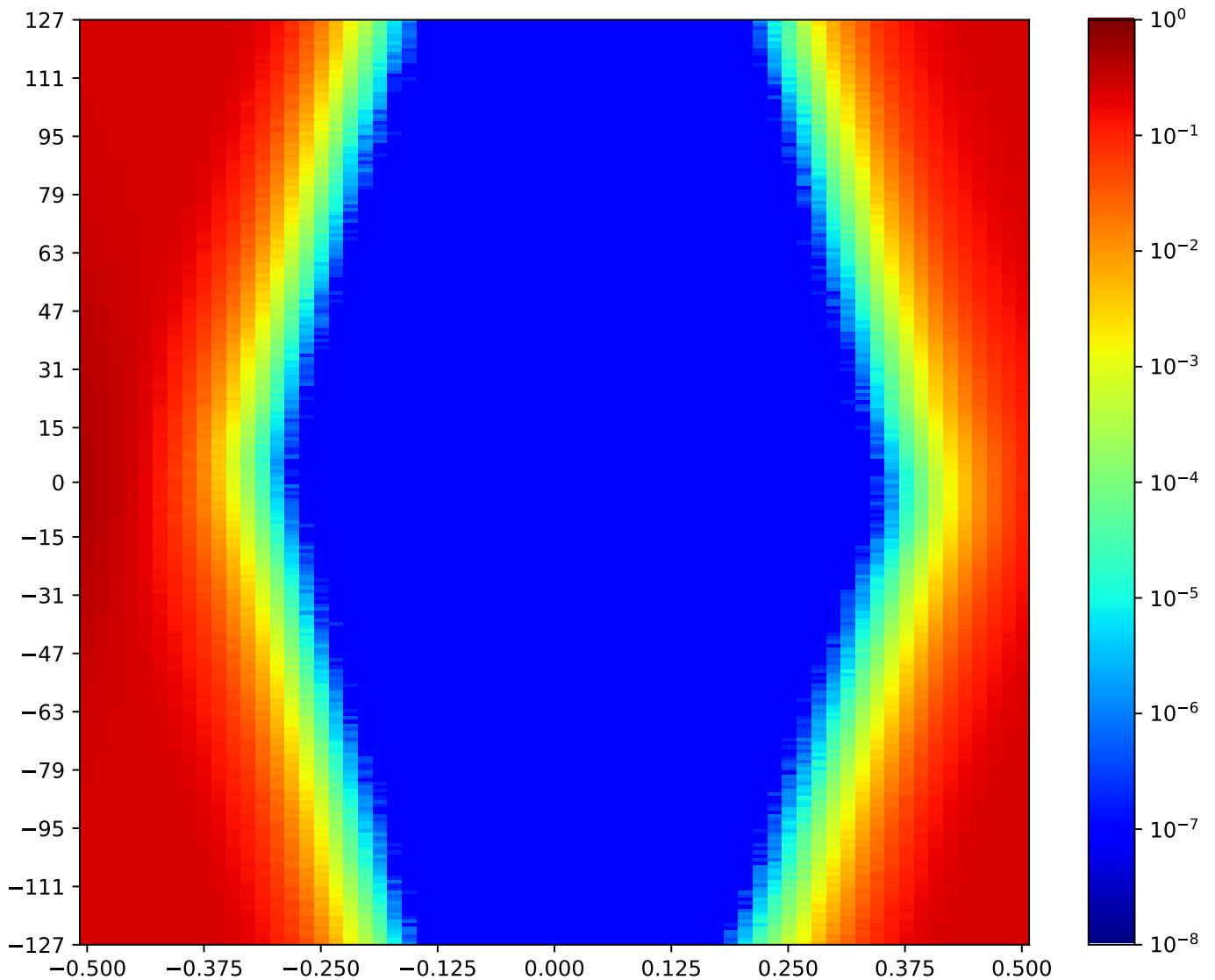


Figure 3.175: MSP\_C\_FPGA-TX4-08-RX8-08-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.10 MSP\_C\_FPGA-TX4-09-RX8-09-MSP\_A\_FPGA

Table 3.163: MSP\_C\_FPGA-TX4-09-RX8-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:41:38		2018-Jan-24 00:41:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9428	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

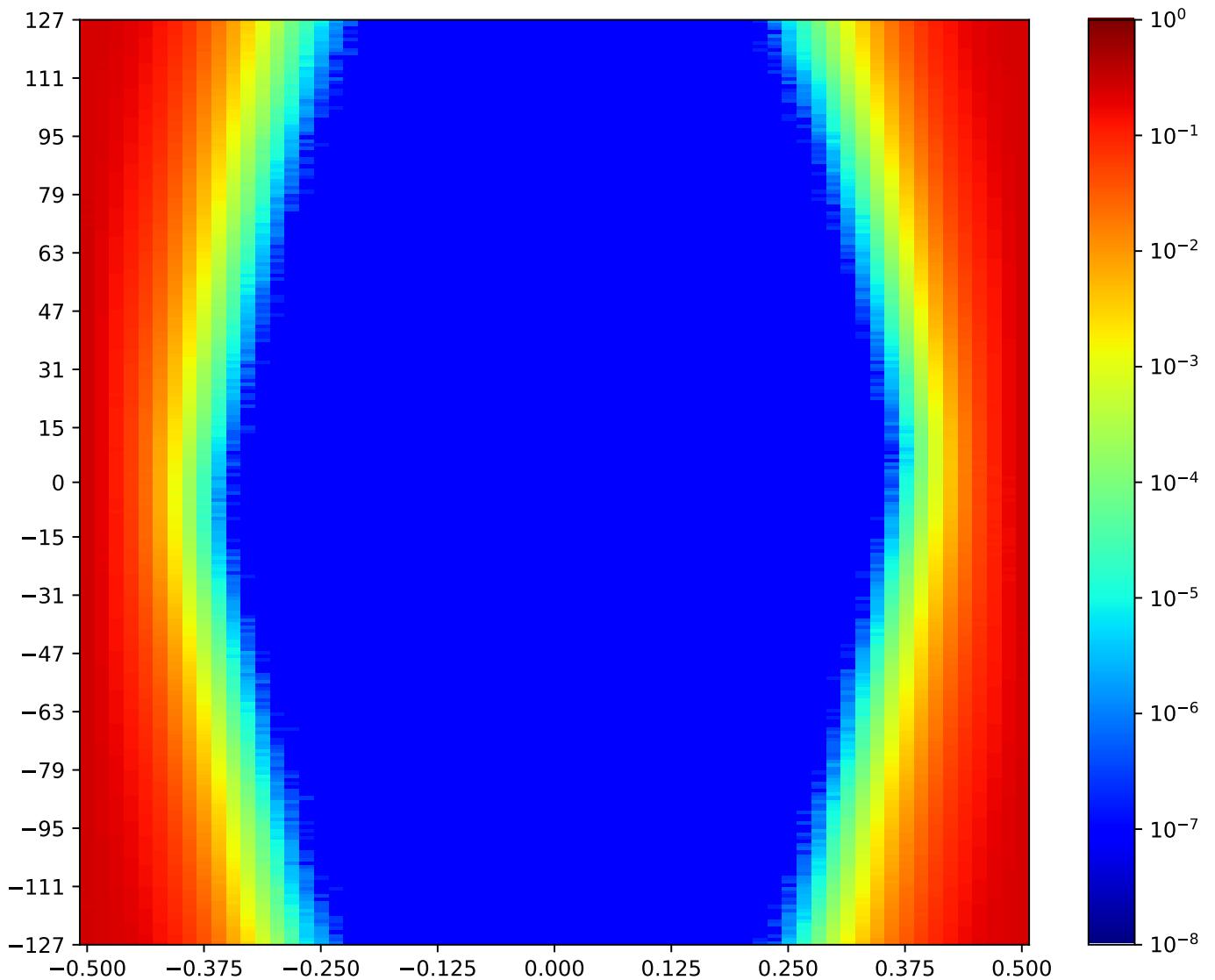


Figure 3.176: MSP\_C\_FPGA-TX4-09-RX8-09-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.11 MSP\_C\_FPGA-TX4-10-RX8-10-MSP\_A\_FPGA

Table 3.164: MSP\_C\_FPGA-TX4-10-RX8-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:42:42		2018-Jan-24 00:43:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8564	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

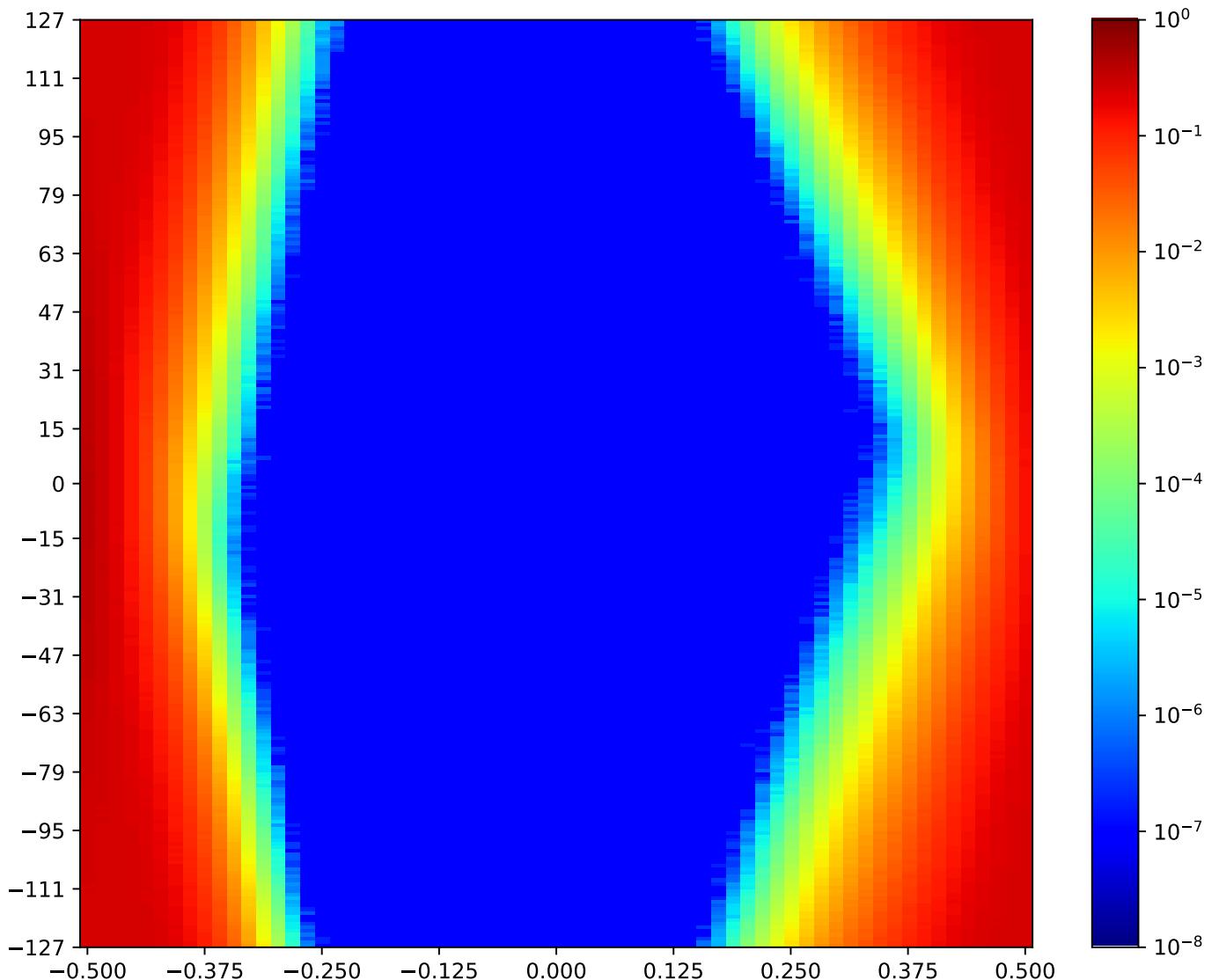


Figure 3.177: MSP\_C\_FPGA-TX4-10-RX8-10-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.13.12 MSP\_C\_FPGA-TX4-11-RX8-11-MSP\_A\_FPGA

Table 3.165: MSP\_C\_FPGA-TX4-11-RX8-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:42:21		2018-Jan-24 00:42:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7103	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

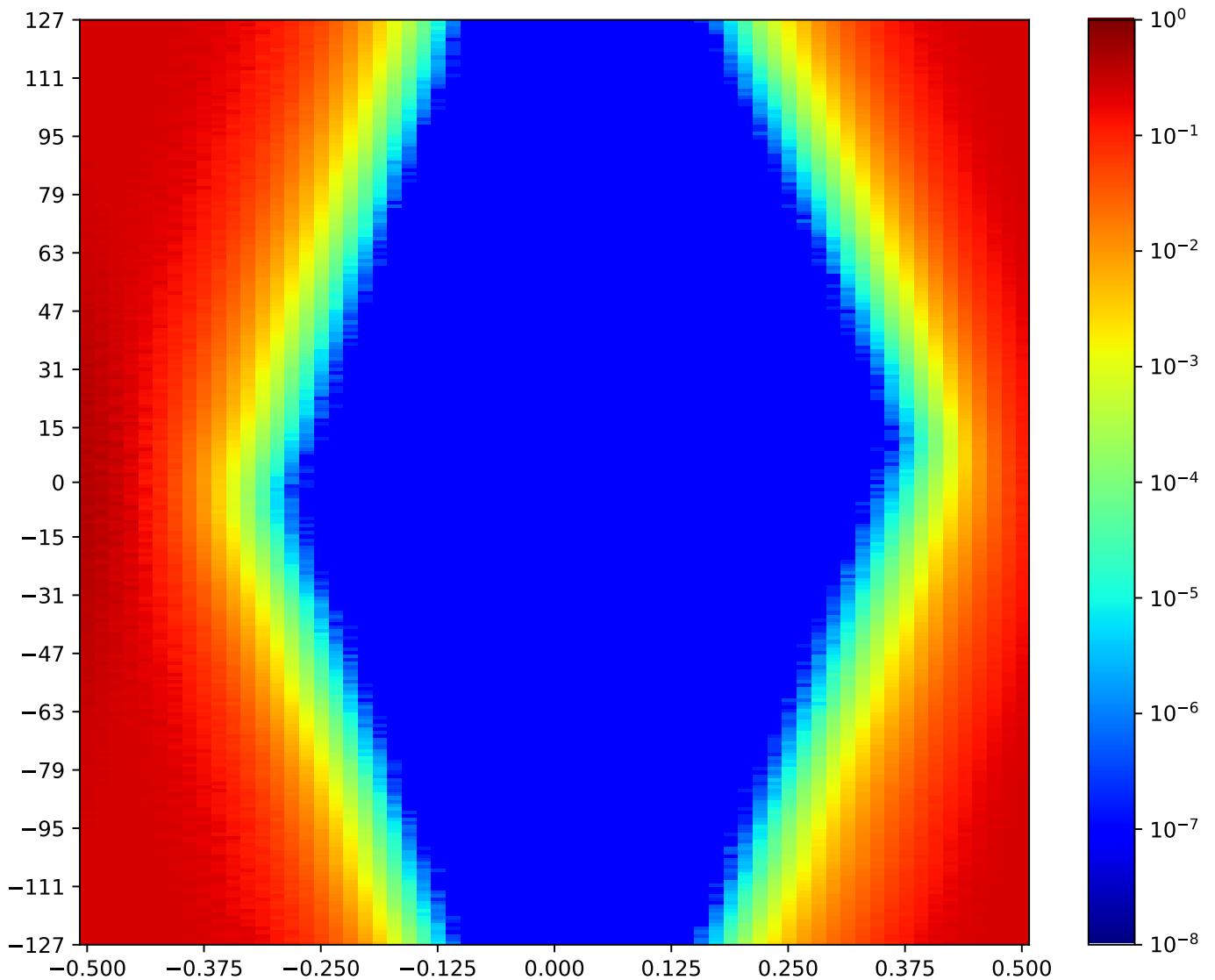


Figure 3.178: MSP\_C\_FPGA-TX4-11-RX8-11-MSP\_A\_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### **3.14 Partial TRP TX5 MSP\_C RX14 Minipod Loopback**

A cross-reference to Figure 3.179. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

Next summary Figure 3.188.

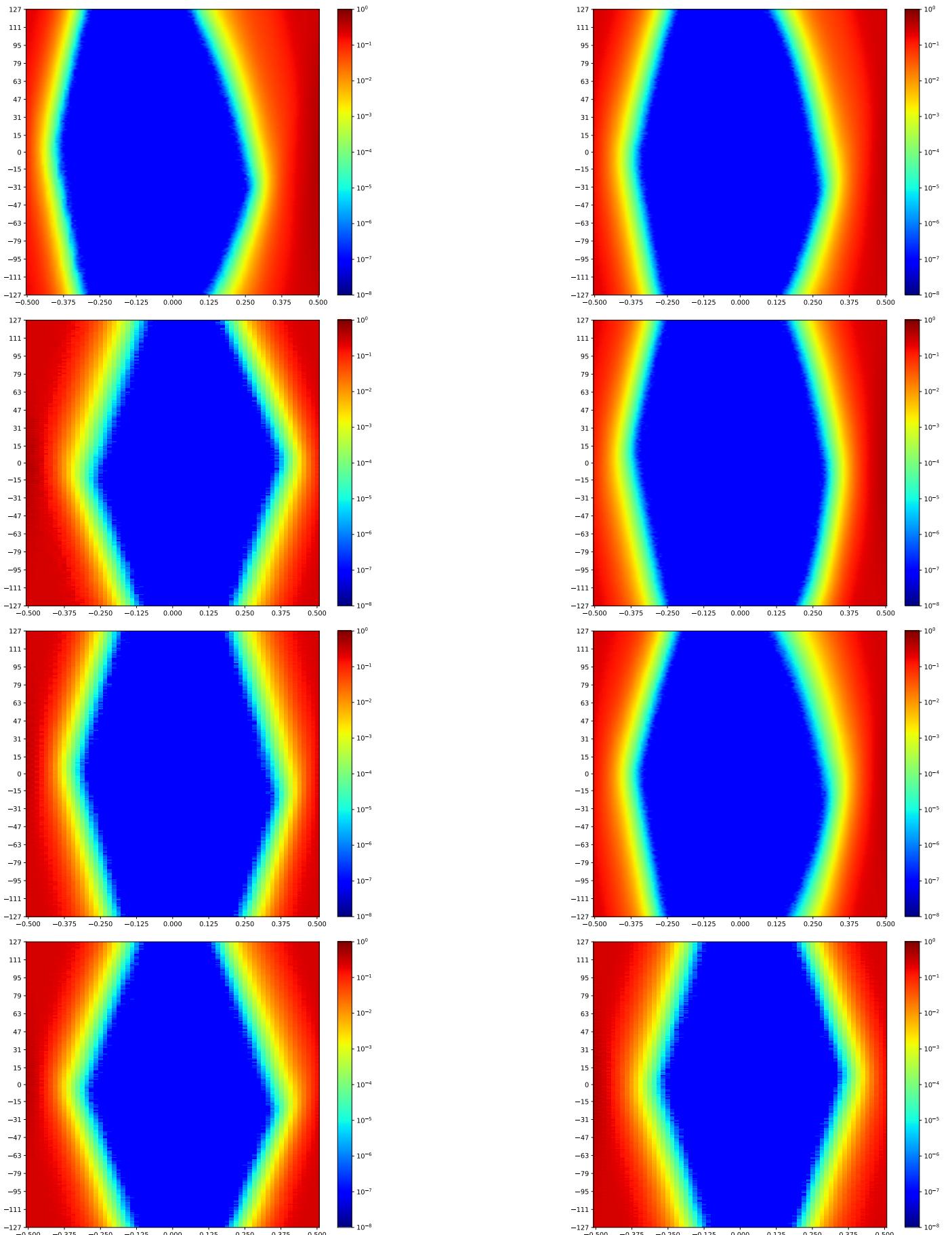


Figure 3.179: Partial TRP TX5 MSP\_C RX14 Minipod Loopback

### 3.14.1 TRP\_FPGA-TX5-00-RX14-00-MSP\_C\_FPGA

Table 3.166: TRP\_FPGA-TX5-00-RX14-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:46:15		2018-Jan-24 00:46:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16345	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

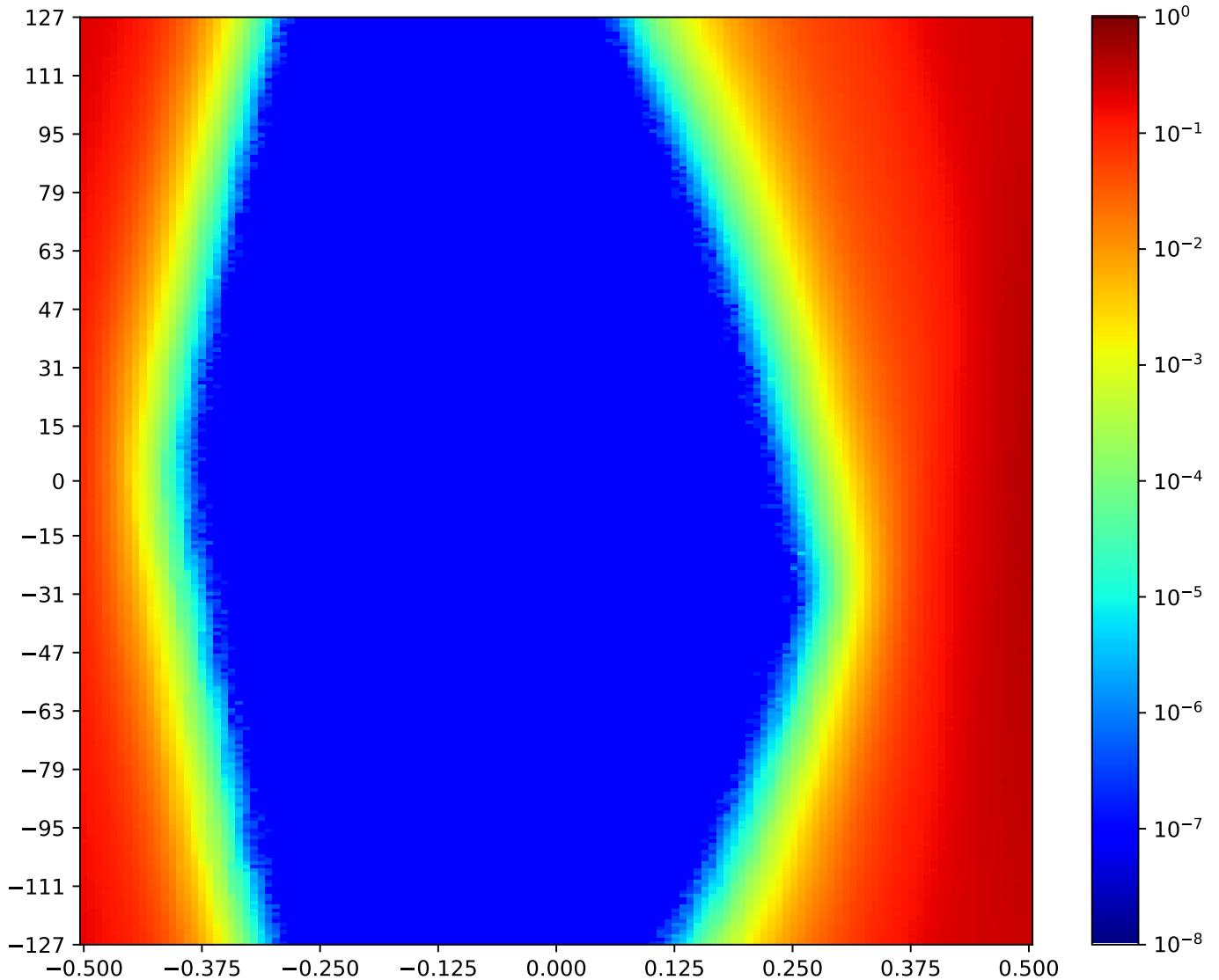


Figure 3.180: TRP\_FPGA-TX5-00-RX14-00-MSP\_C\_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.14.2 TRP\_FPGA-TX5-01-RX14-01-MSP\_C\_FPGA

Table 3.167: TRP\_FPGA-TX5-01-RX14-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:44:50		2018-Jan-24 00:45:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15685	73	56.59%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

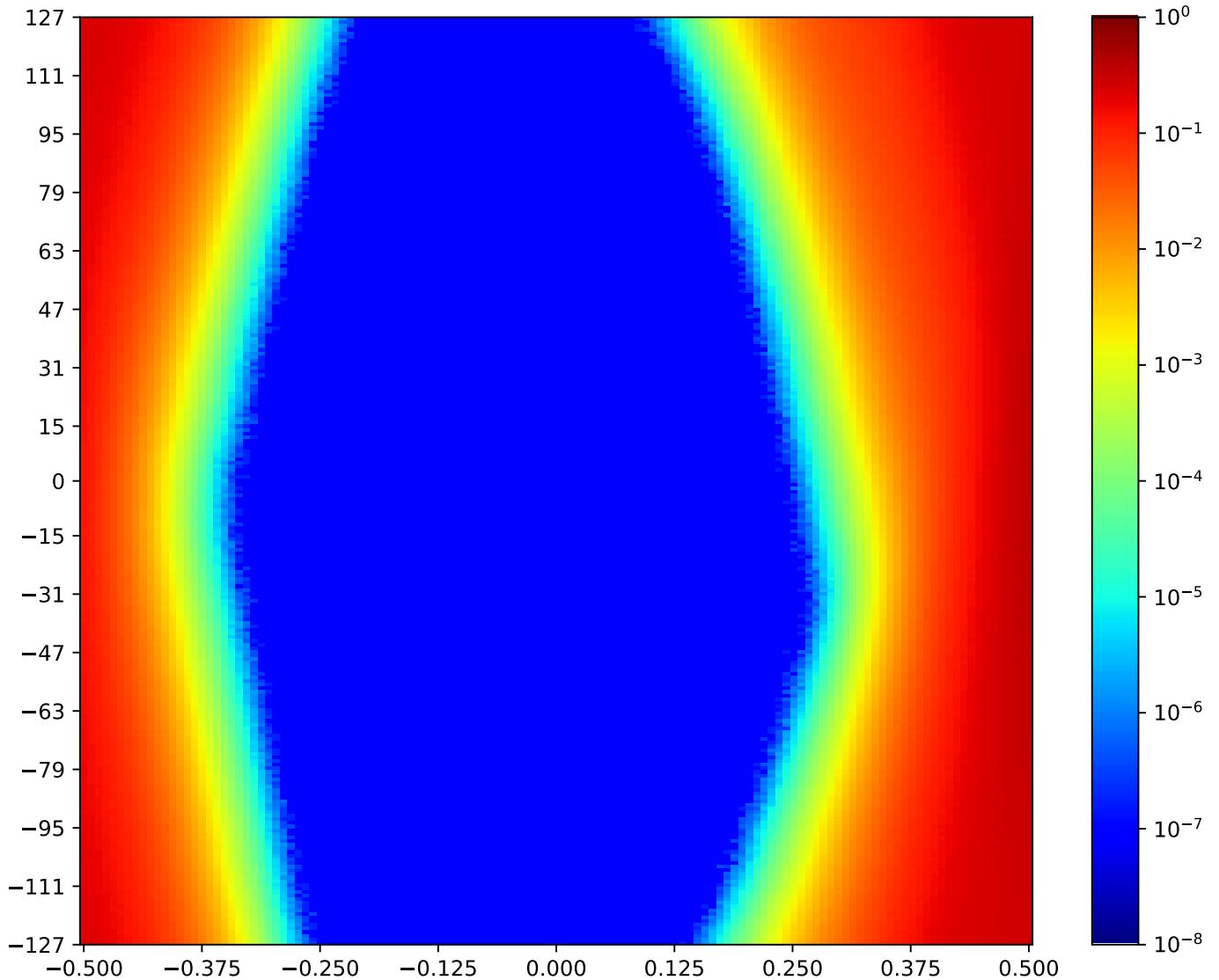


Figure 3.181: TRP\_FPGA-TX5-01-RX14-01-MSP\_C\_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.14.3 TRP\_FPGA-TX5-02-RX14-02-MSP\_C\_FPGA

Table 3.168: TRP\_FPGA-TX5-02-RX14-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:47:19		2018-Jan-24 00:47:40	
Reset RX	OA	HO		HO (%)	
true	6915	36		55.38%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

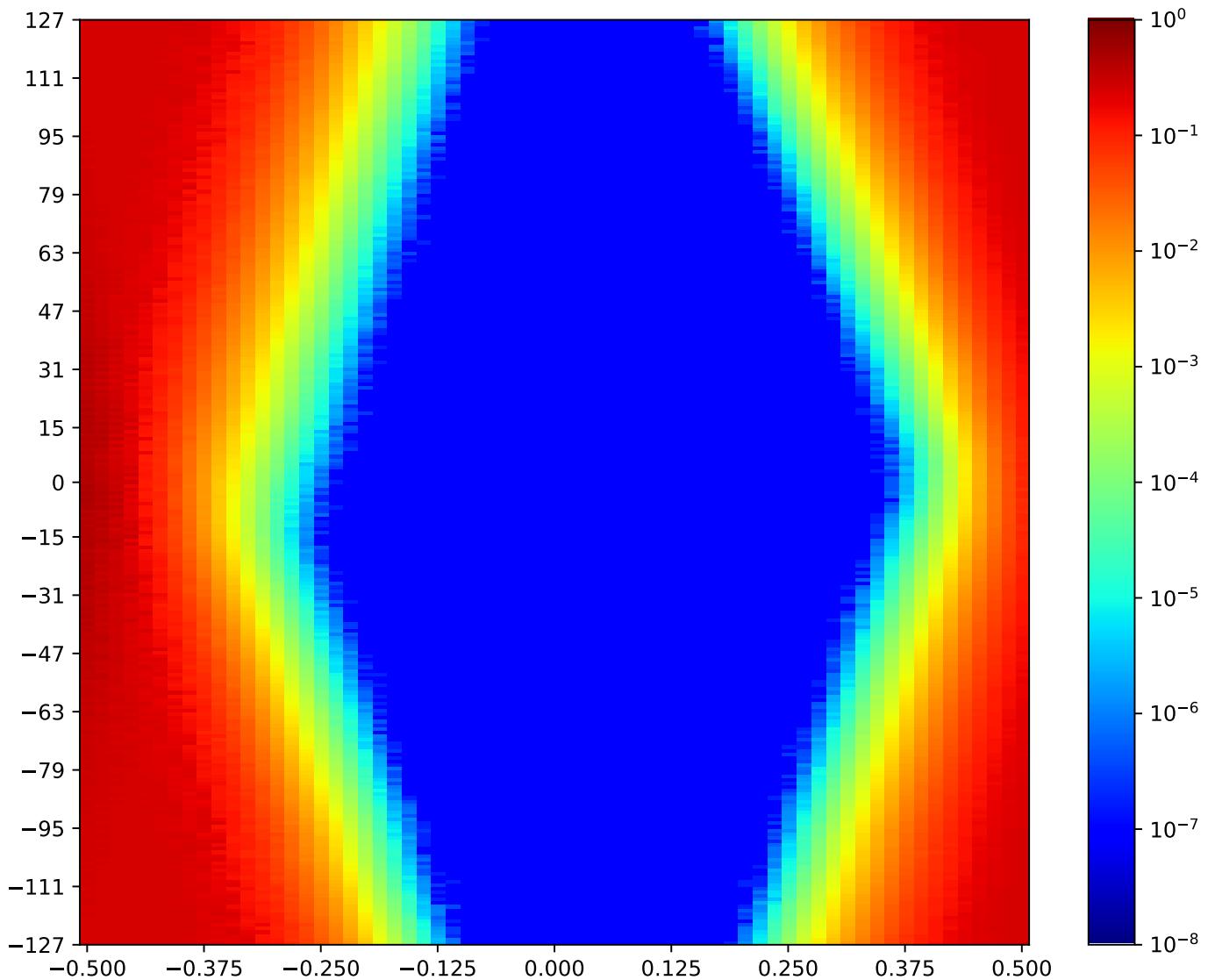


Figure 3.182: TRP\_FPGA-TX5-02-RX14-02-MSP\_C\_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.14.4 TRP\_FPGA-TX5-03-RX14-03-MSP\_C\_FPGA

Table 3.169: TRP\_FPGA-TX5-03-RX14-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:45:33		2018-Jan-24 00:46:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17179	79	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

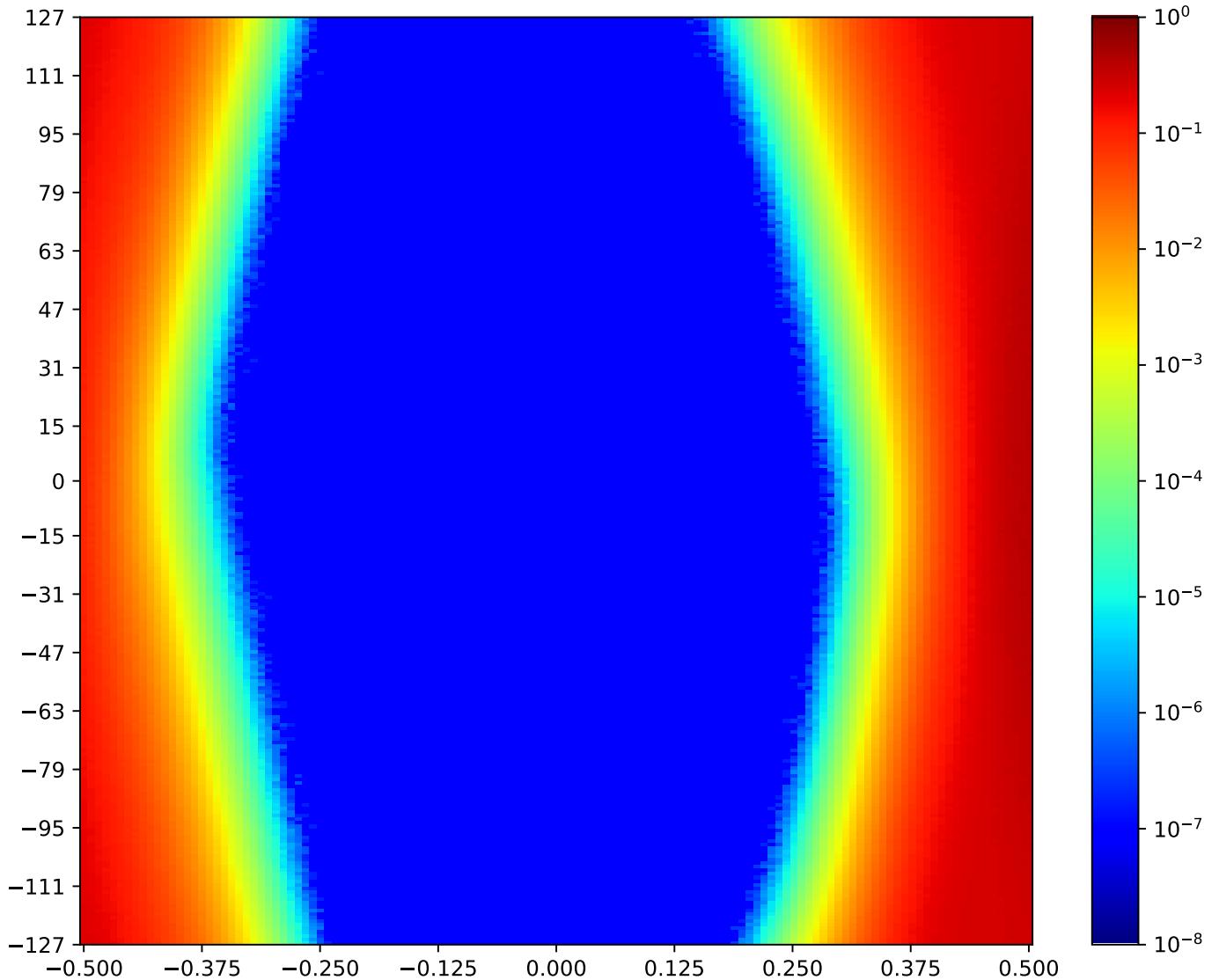


Figure 3.183: TRP\_FPGA-TX5-03-RX14-03-MSP\_C\_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.14.5 TRP\_FPGA-TX5-04-RX14-04-MSP\_C\_FPGA

Table 3.170: TRP\_FPGA-TX5-04-RX14-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:48:02		2018-Jan-24 00:48:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8057	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

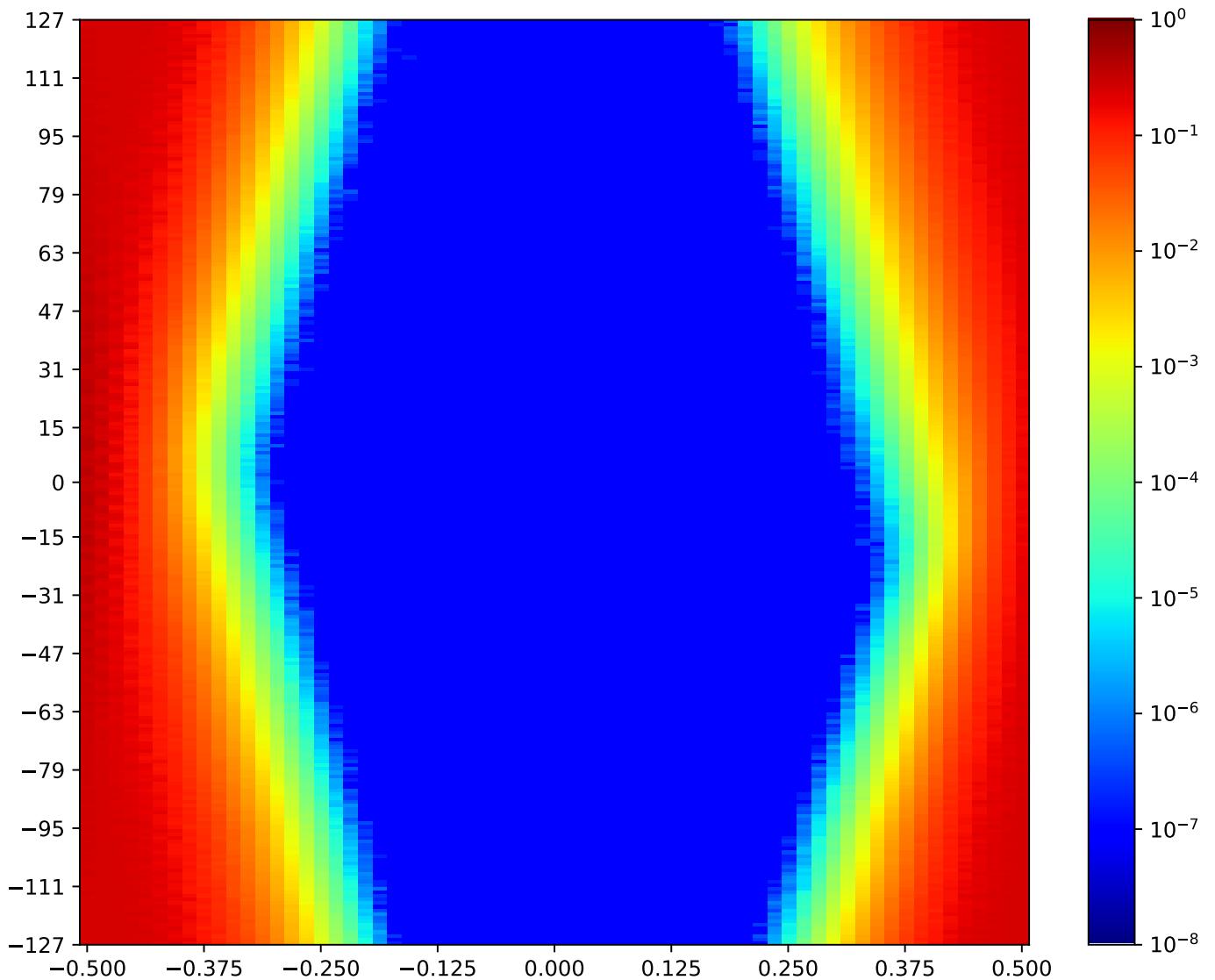


Figure 3.184: TRP\_FPGA-TX5-04-RX14-04-MSP\_C\_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.14.6 TRP\_FPGA-TX5-05-RX14-05-MSP\_C\_FPGA

Table 3.171: TRP\_FPGA-TX5-05-RX14-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:44:07		2018-Jan-24 00:44:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15909	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

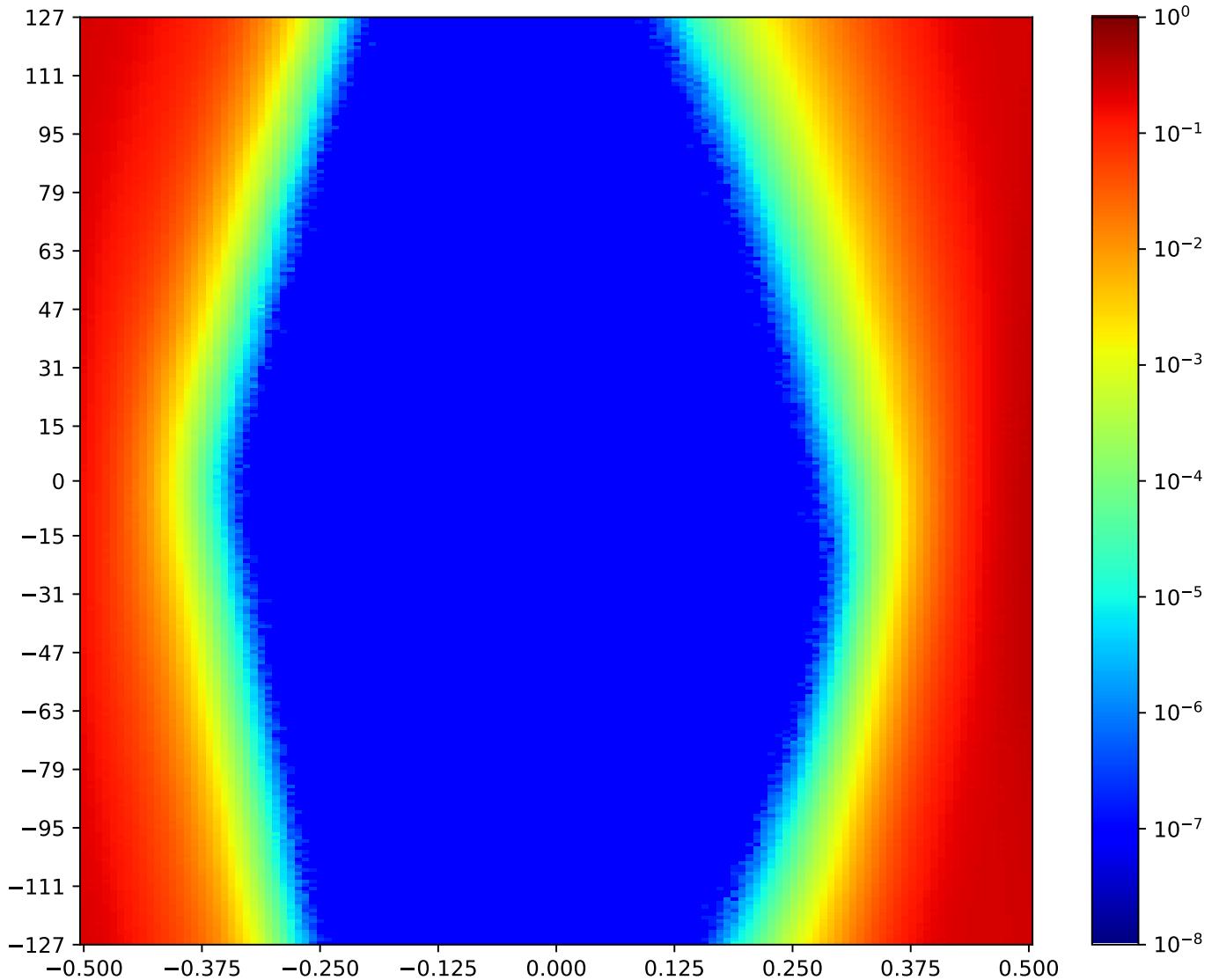


Figure 3.185: TRP\_FPGA-TX5-05-RX14-05-MSP\_C\_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.14.7 TRP\_FPGA-TX5-06-RX14-06-MSP\_C\_FPGA

Table 3.172: TRP\_FPGA-TX5-06-RX14-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:46:57		2018-Jan-24 00:47:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6982	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

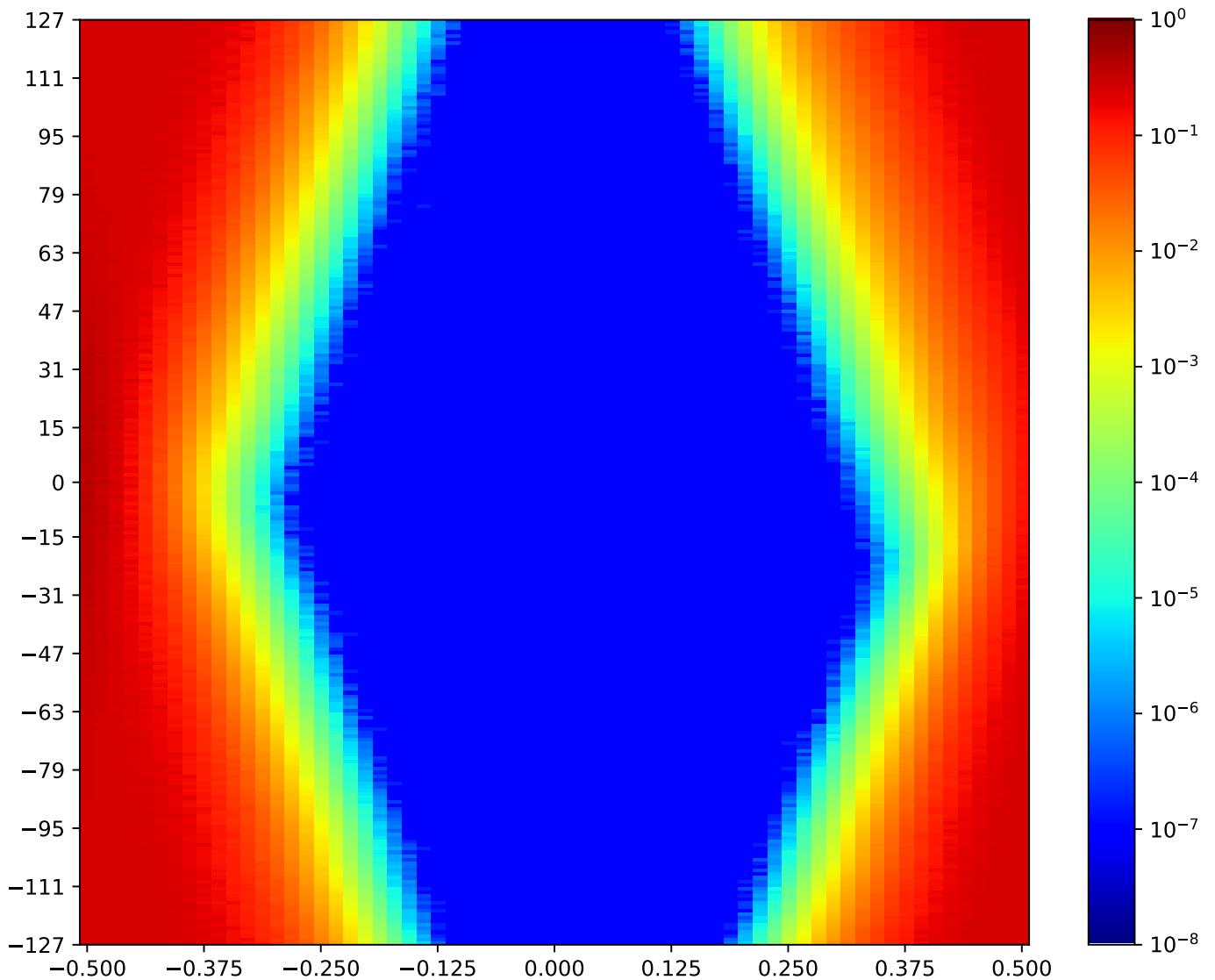


Figure 3.186: TRP\_FPGA-TX5-06-RX14-06-MSP\_C\_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.14.8 TRP\_FPGA-TX5-07-RX14-07-MSP\_C\_FPGA

Table 3.173: TRP\_FPGA-TX5-07-RX14-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:47:40		2018-Jan-24 00:48:02	
Reset RX	OA	HO		VO   VO (%)	
true	7070	37		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

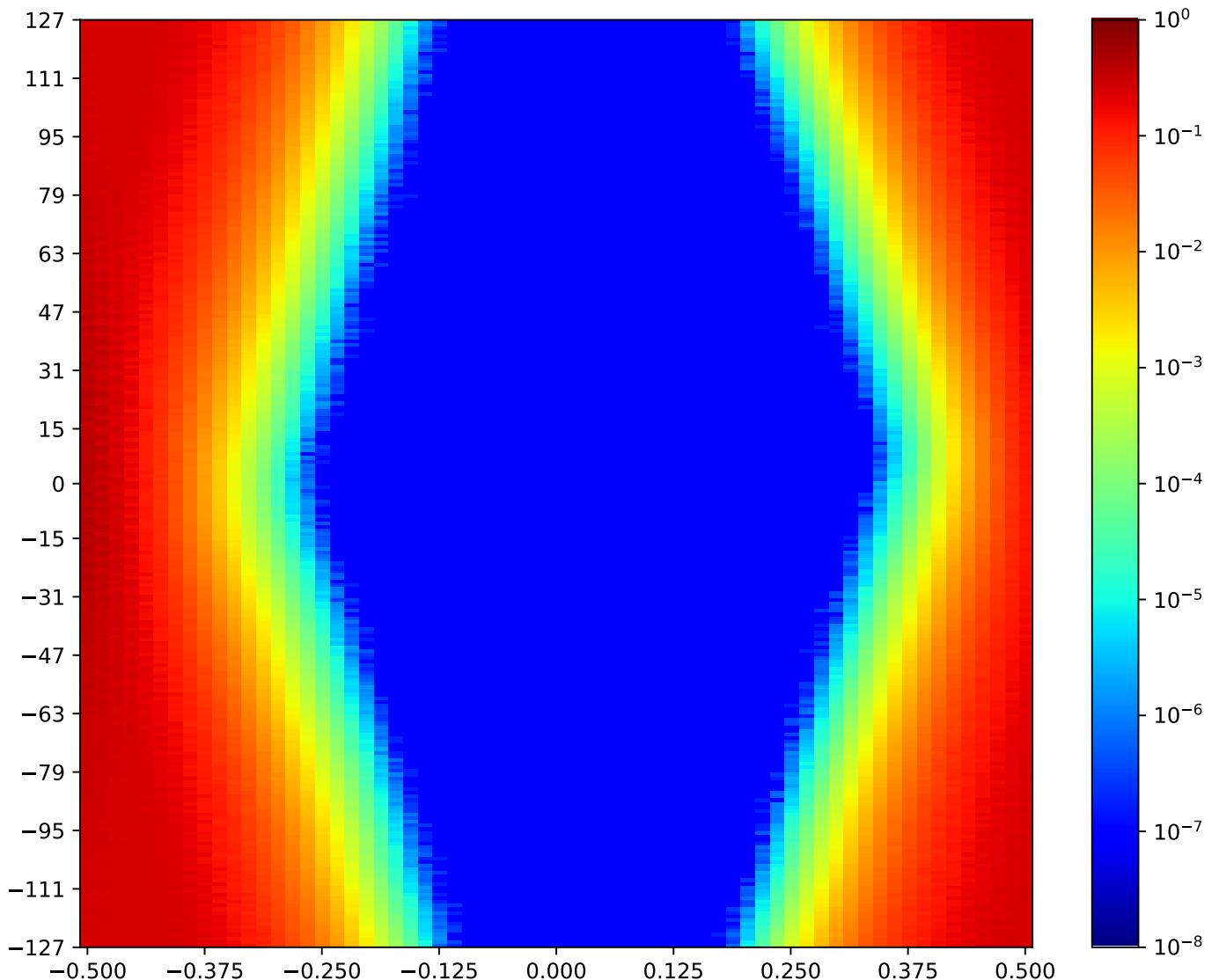


Figure 3.187: TRP\_FPGA-TX5-07-RX14-07-MSP\_C\_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15 MSP\_A TX1 MSP\_C RX11 Minipod Loopback

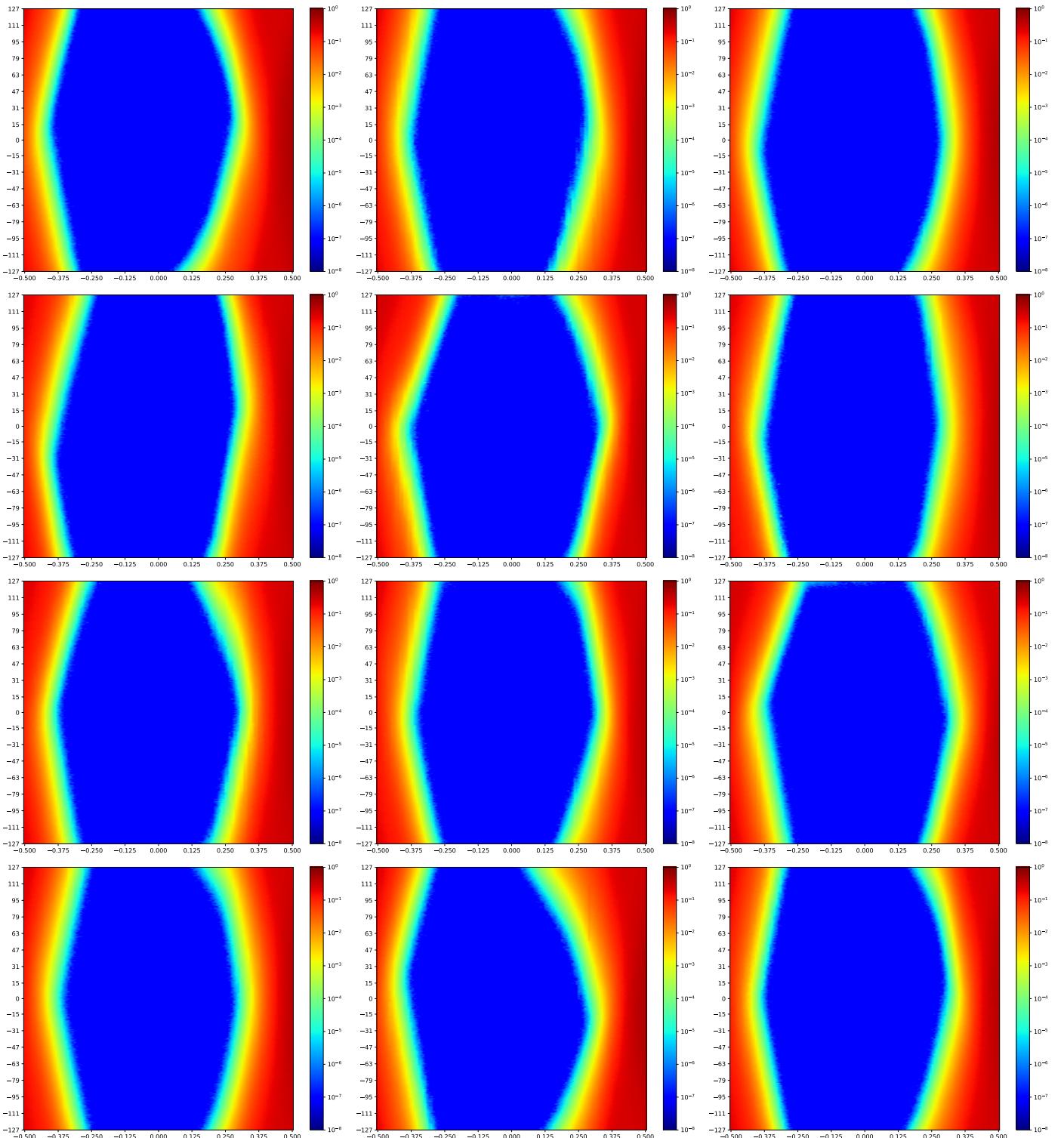


Figure 3.188: MSP\_A TX1 MSP\_C RX11 Minipod Loopback

A cross-reference to Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.201.

### 3.15.1 MSP\_A\_FPGA-TX1-00-RX11-00-MSP\_C\_FPGA

Table 3.174: MSP\_A\_FPGA-TX1-00-RX11-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:57:58		2018-Jan-24 00:58:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17249	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

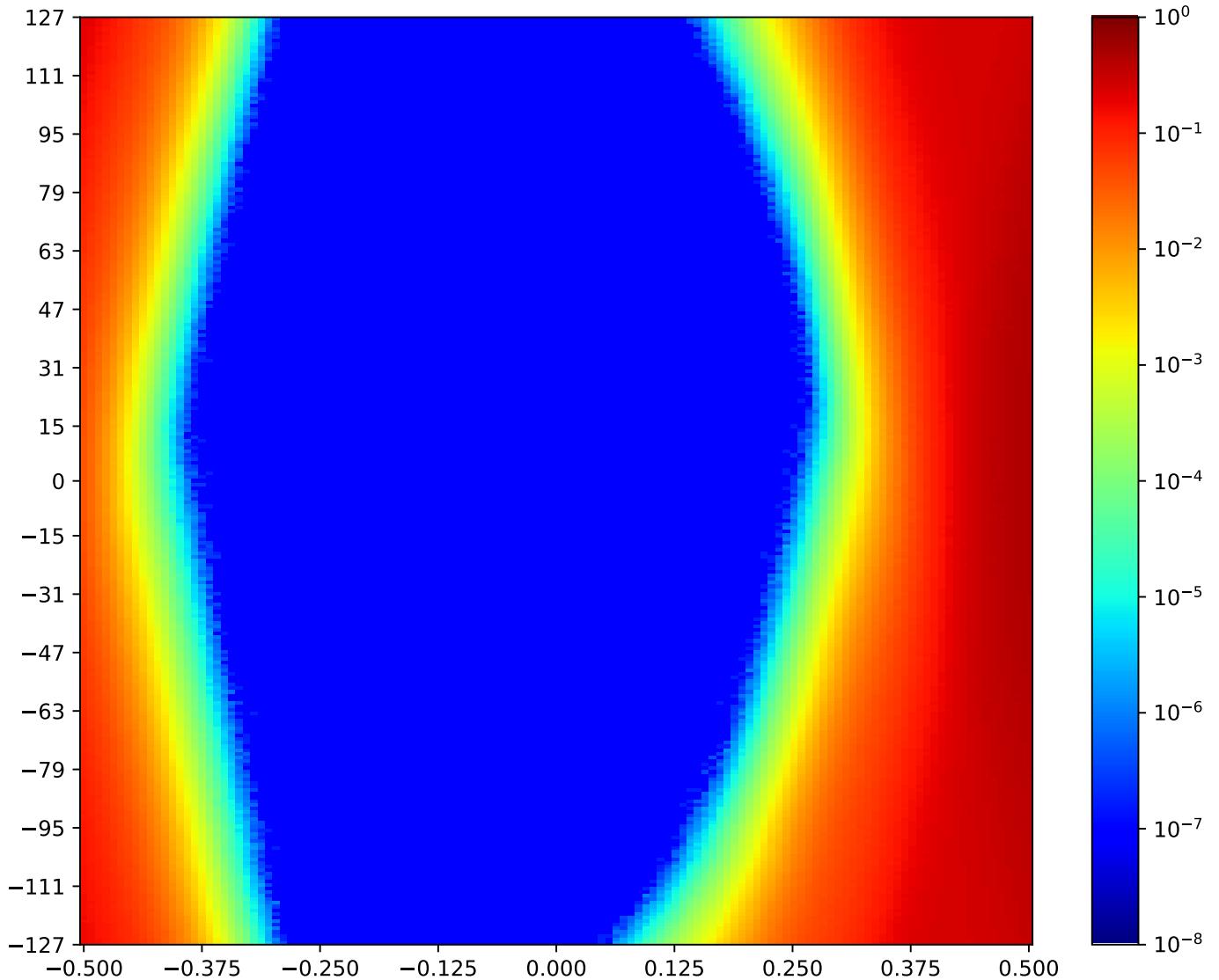


Figure 3.189: MSP\_A\_FPGA-TX1-00-RX11-00-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.2 MSP\_A\_FPGA-TX1-01-RX11-01-MSP\_C\_FPGA

Table 3.175: MSP\_A\_FPGA-TX1-01-RX11-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:59:22		2018-Jan-24 01:00:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16714	75	57.36%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

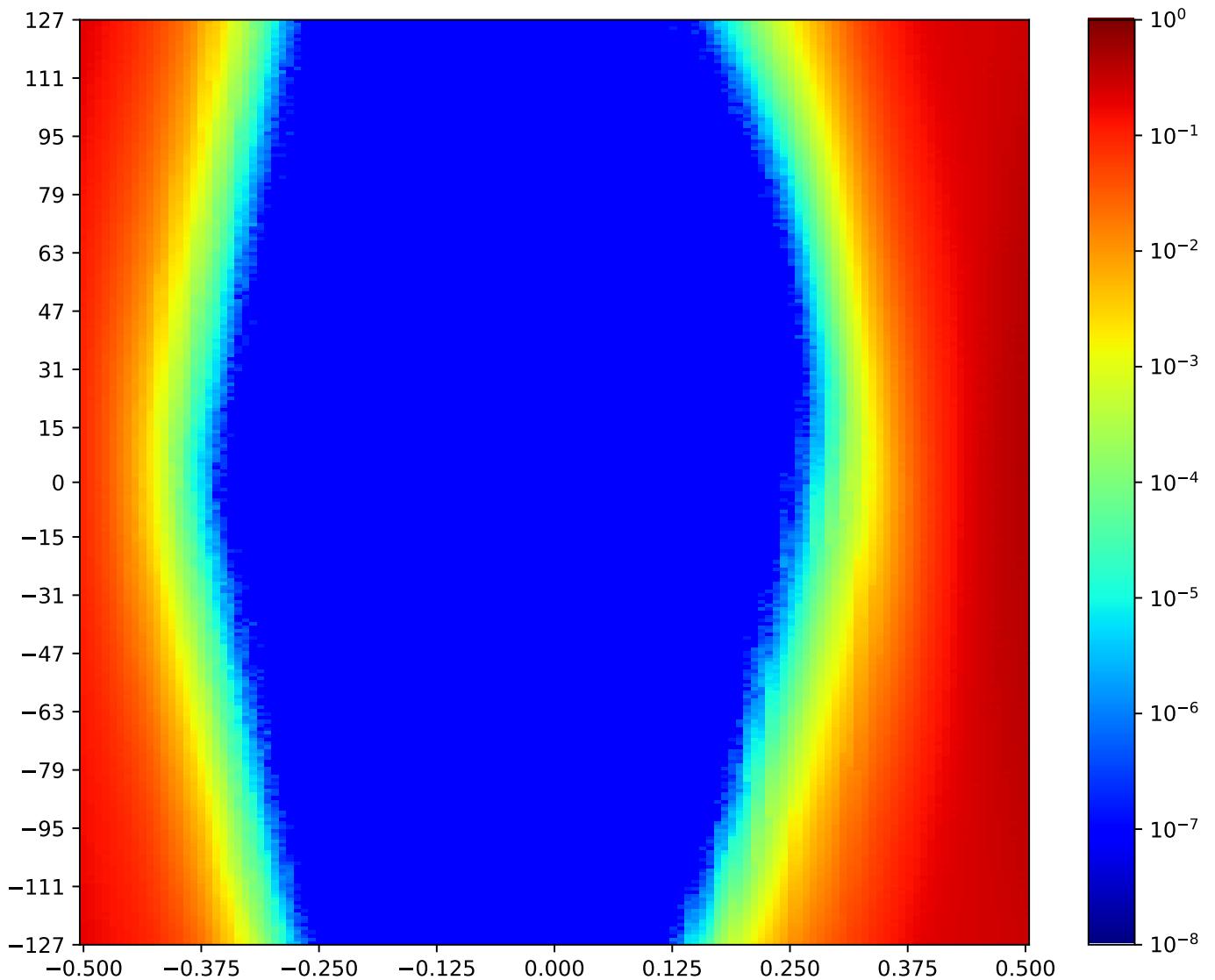


Figure 3.190: MSP\_A\_FPGA-TX1-01-RX11-01-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.3 MSP\_A\_FPGA-TX1-02-RX11-02-MSP\_C\_FPGA

Table 3.176: MSP\_A\_FPGA-TX1-02-RX11-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:00:03		2018-Jan-24 01:00:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17537	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

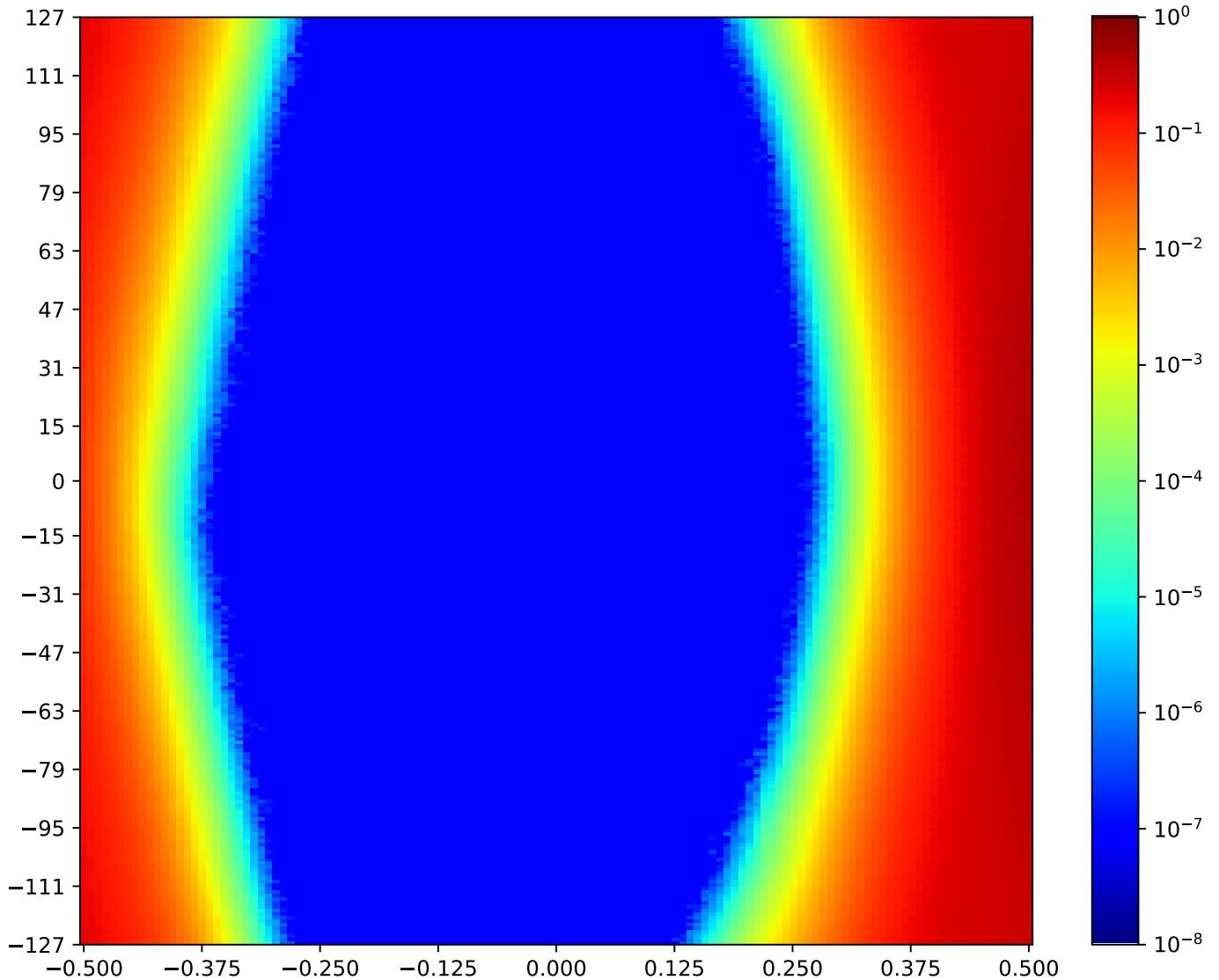


Figure 3.191: MSP\_A\_FPGA-TX1-02-RX11-02-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.4 MSP\_A\_FPGA-TX1-03-RX11-03-MSP\_C\_FPGA

Table 3.177: MSP\_A\_FPGA-TX1-03-RX11-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:56:34		2018-Jan-24 00:57:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17809	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

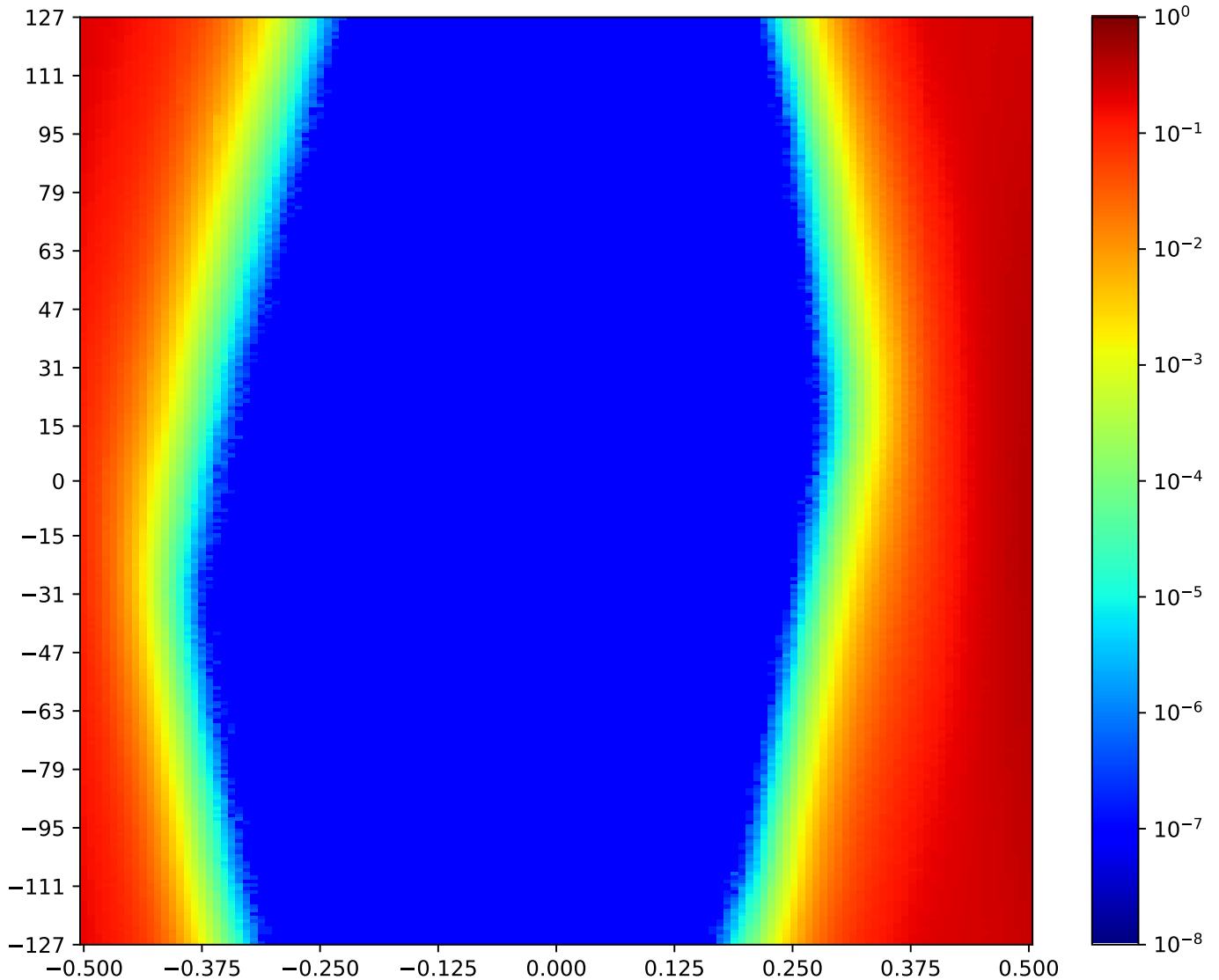


Figure 3.192: MSP\_A\_FPGA-TX1-03-RX11-03-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.5 MSP\_A\_FPGA-TX1-04-RX11-04-MSP\_C\_FPGA

Table 3.178: MSP\_A\_FPGA-TX1-04-RX11-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:02:08		2018-Jan-24 01:02:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17296	83	64.34%	250	97.65%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

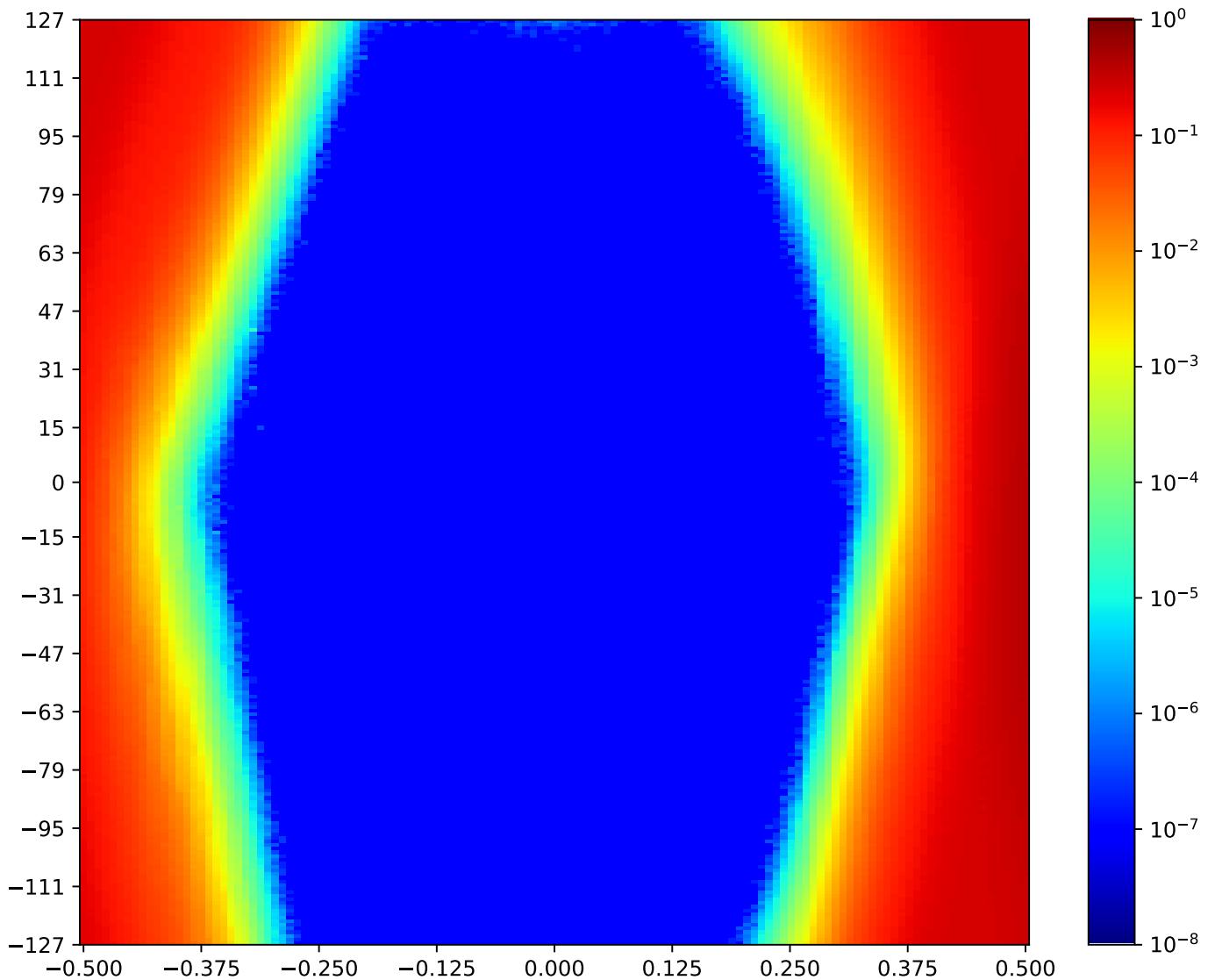


Figure 3.193: MSP\_A\_FPGA-TX1-04-RX11-04-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.6 MSP\_A\_FPGA-TX1-05-RX11-05-MSP\_C\_FPGA

Table 3.179: MSP\_A\_FPGA-TX1-05-RX11-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:55:52		2018-Jan-24 00:56:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17106	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

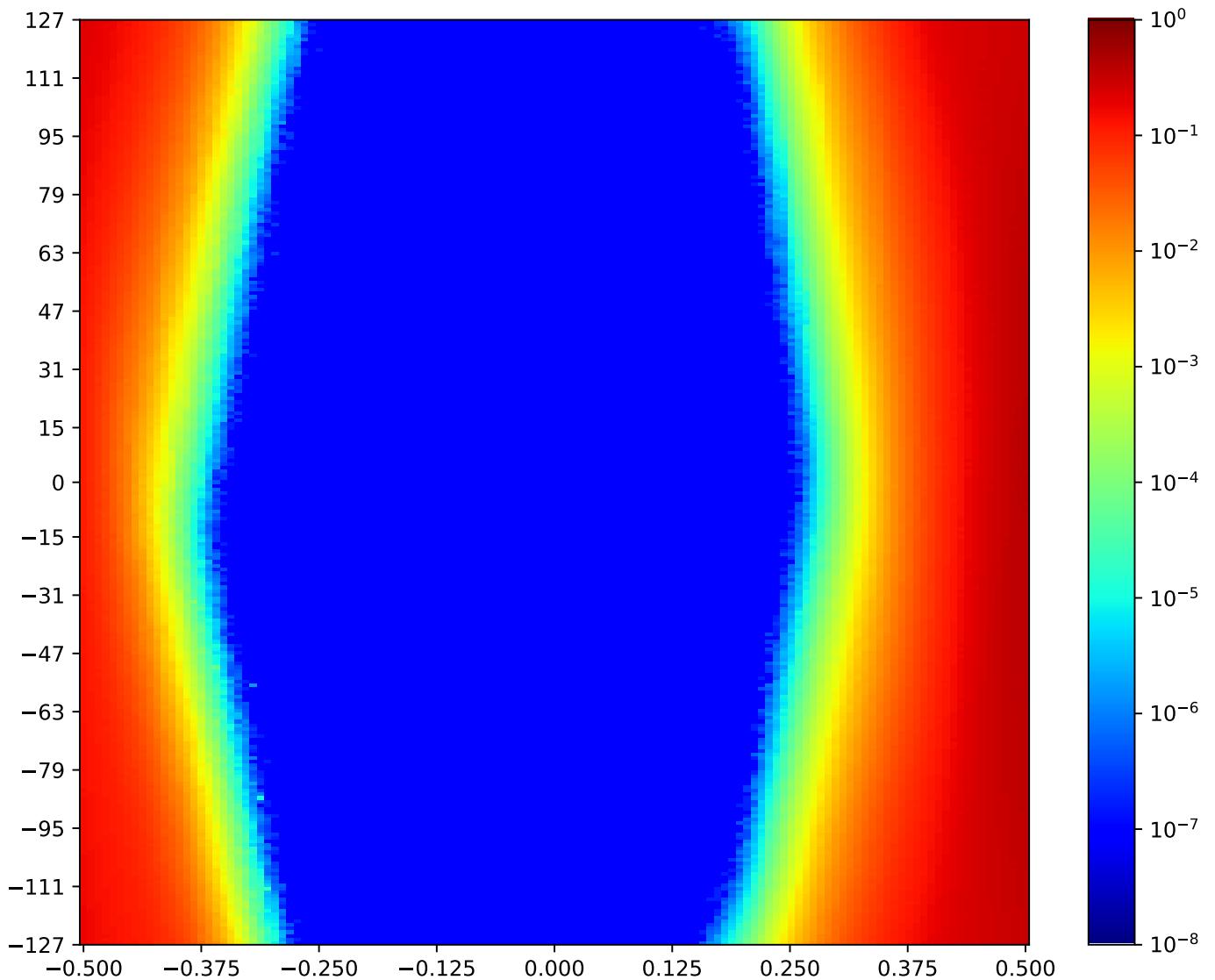


Figure 3.194: MSP\_A\_FPGA-TX1-05-RX11-05-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.7 MSP\_A\_FPGA-TX1-06-RX11-06-MSP\_C\_FPGA

Table 3.180: MSP\_A\_FPGA-TX1-06-RX11-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:03:31		2018-Jan-24 01:04:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16989	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

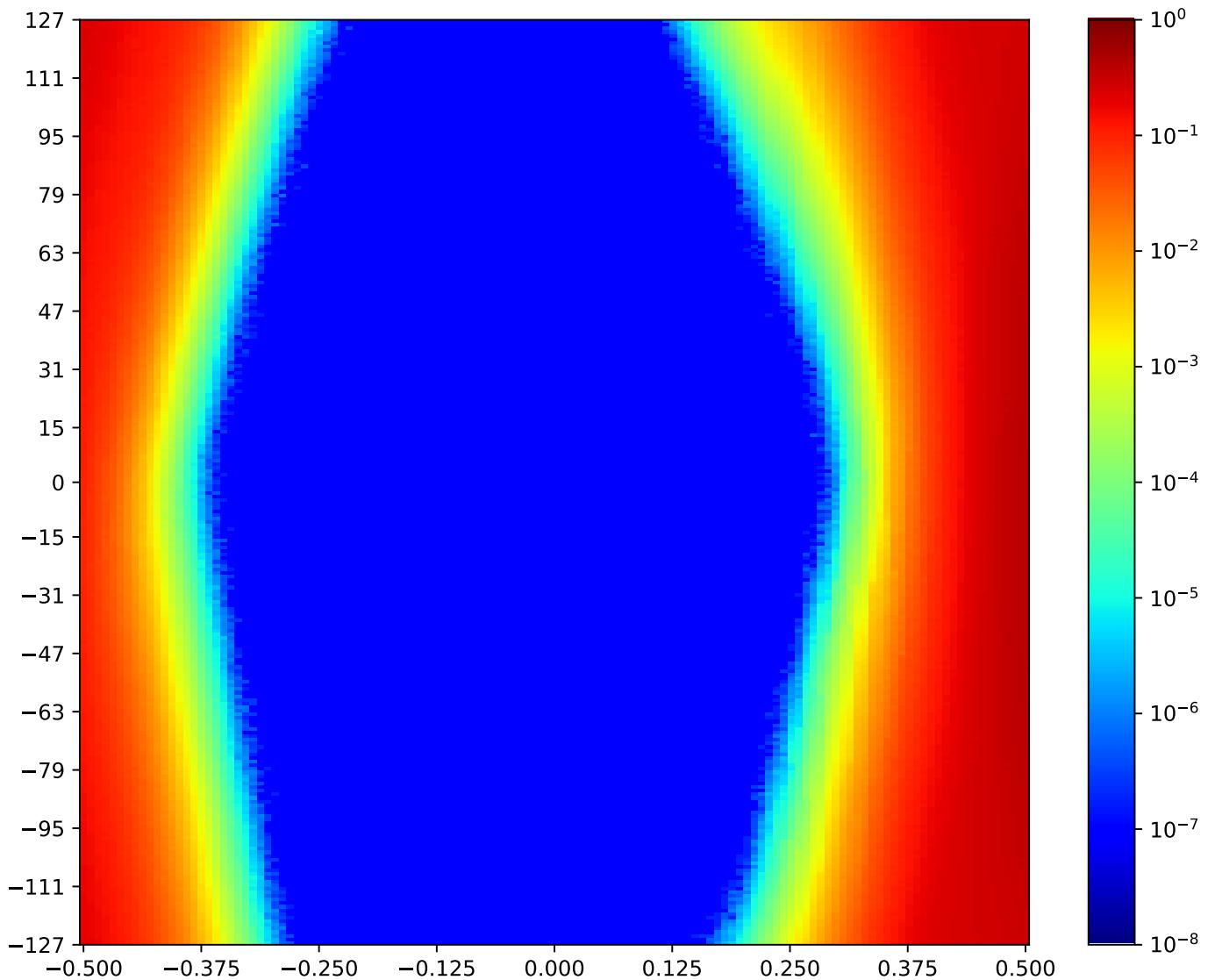


Figure 3.195: MSP\_A\_FPGA-TX1-06-RX11-06-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.8 MSP\_A\_FPGA-TX1-07-RX11-07-MSP\_C\_FPGA

Table 3.181: MSP\_A\_FPGA-TX1-07-RX11-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:57:16		2018-Jan-24 00:57:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17159	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

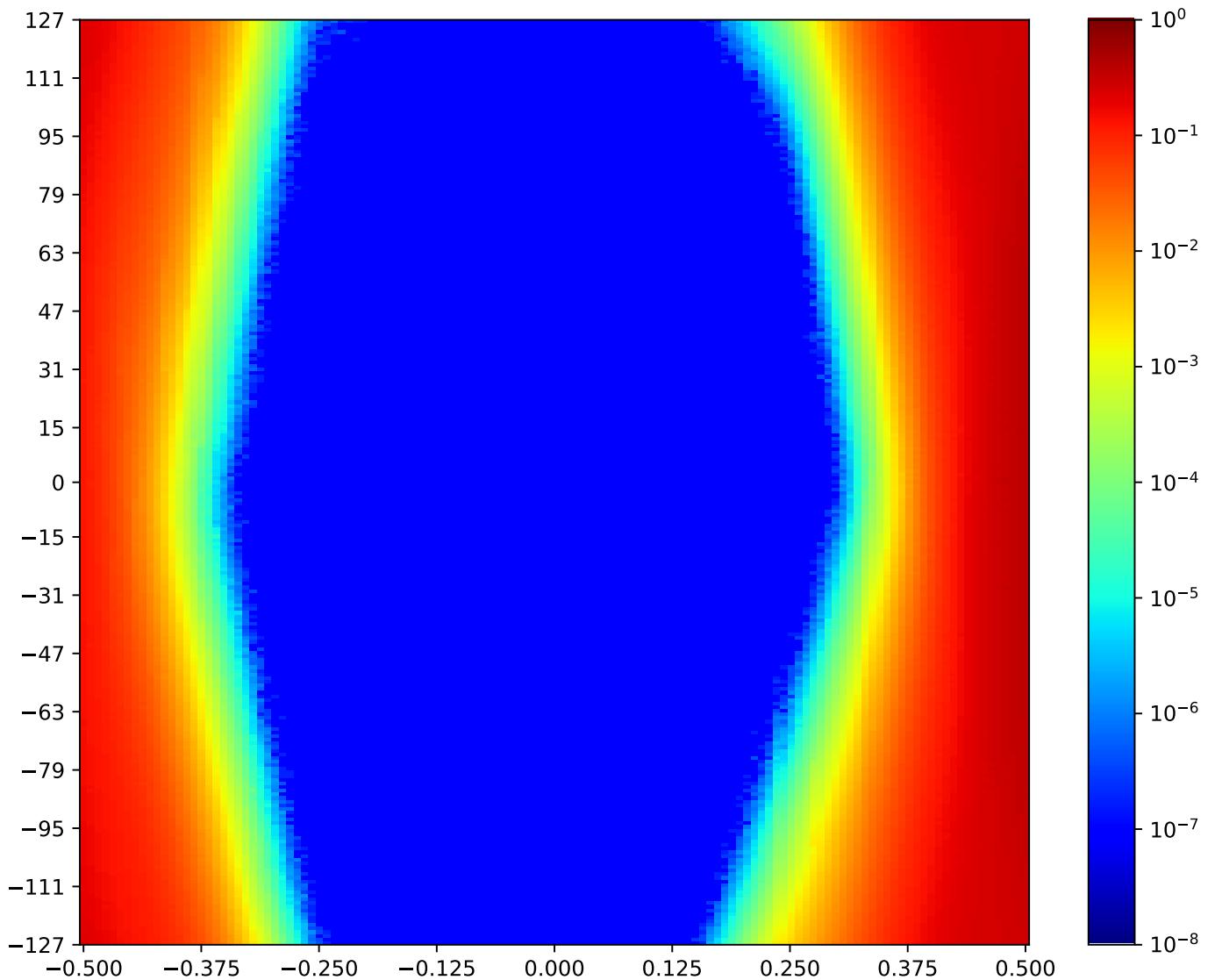


Figure 3.196: MSP\_A\_FPGA-TX1-07-RX11-07-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.9 MSP\_A\_FPGA-TX1-08-RX11-08-MSP\_C\_FPGA

Table 3.182: MSP\_A\_FPGA-TX1-08-RX11-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:02:50		2018-Jan-24 01:03:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16678	79	61.24%	248	97.25%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

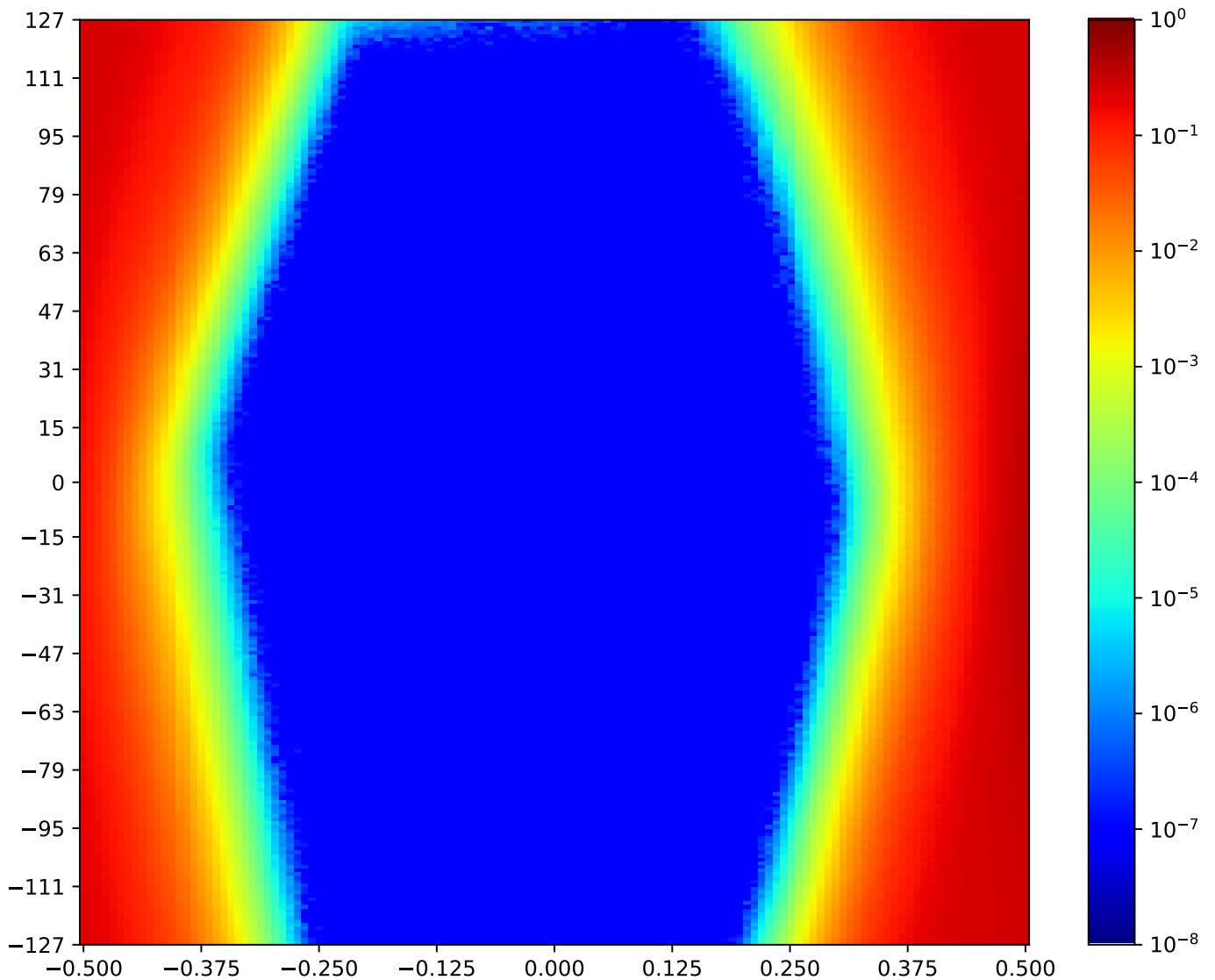


Figure 3.197: MSP\_A\_FPGA-TX1-08-RX11-08-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.10 MSP\_A\_FPGA-TX1-09-RX11-09-MSP\_C\_FPGA

Table 3.183: MSP\_A\_FPGA-TX1-09-RX11-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:58:40		2018-Jan-24 00:59:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16654	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

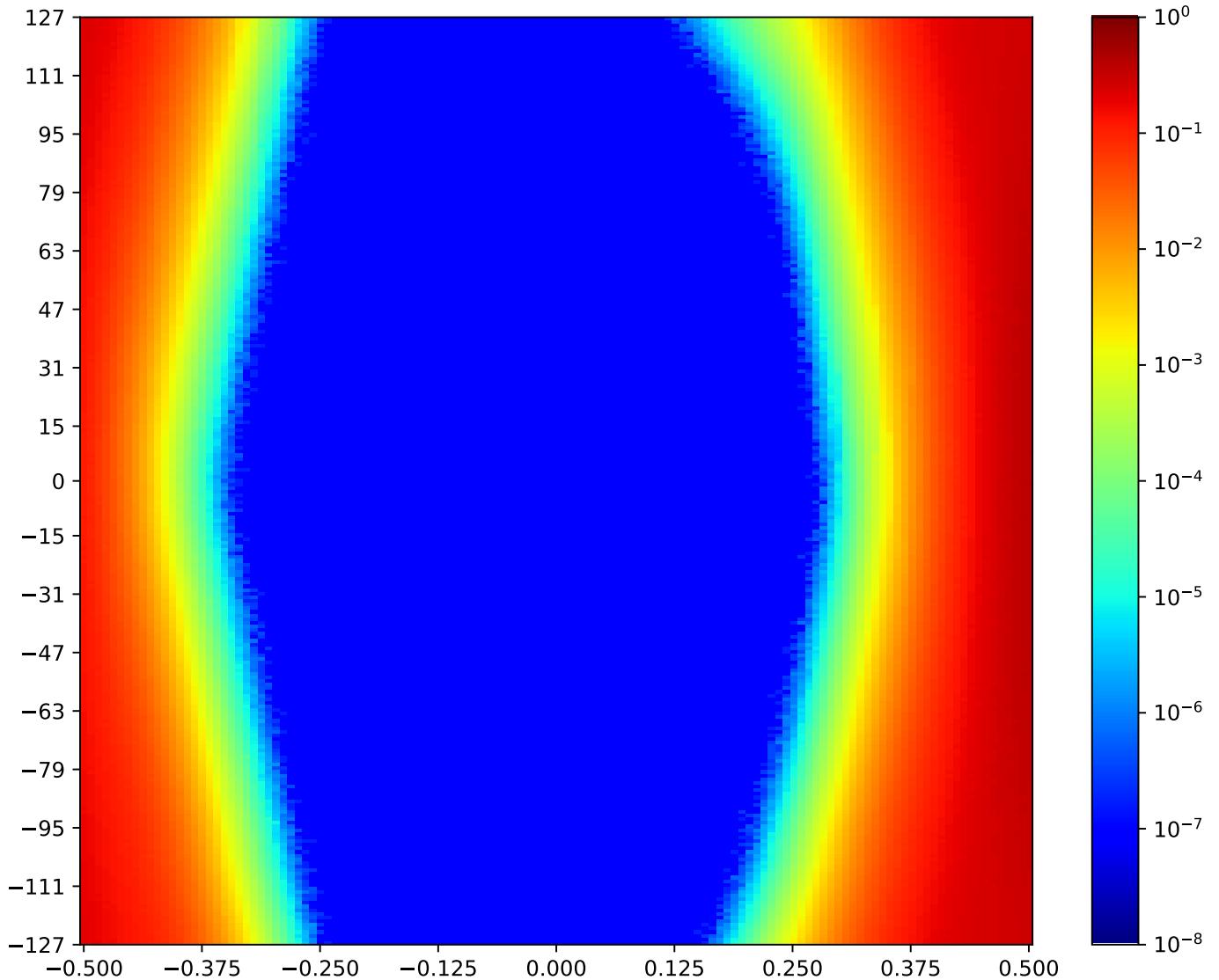


Figure 3.198: MSP\_A\_FPGA-TX1-09-RX11-09-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.11 MSP\_A\_FPGA-TX1-10-RX11-10-MSP\_C\_FPGA

Table 3.184: MSP\_A\_FPGA-TX1-10-RX11-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:01:27		2018-Jan-24 01:02:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16396	77	59.69%	255	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

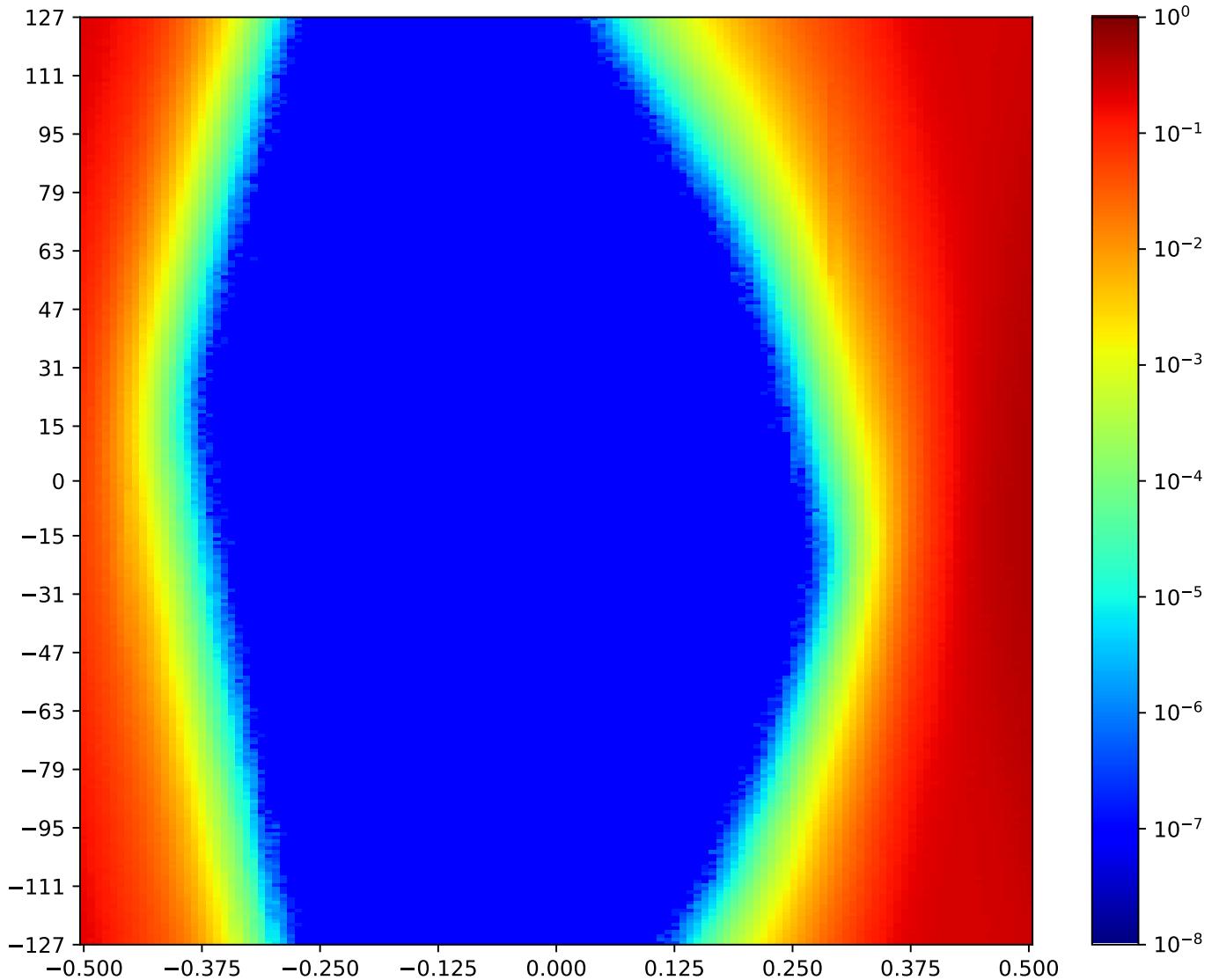


Figure 3.199: MSP\_A\_FPGA-TX1-10-RX11-10-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.15.12 MSP\_A\_FPGA-TX1-11-RX11-11-MSP\_C\_FPGA

Table 3.185: MSP\_A\_FPGA-TX1-11-RX11-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:00:45		2018-Jan-24 01:01:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17919	81	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

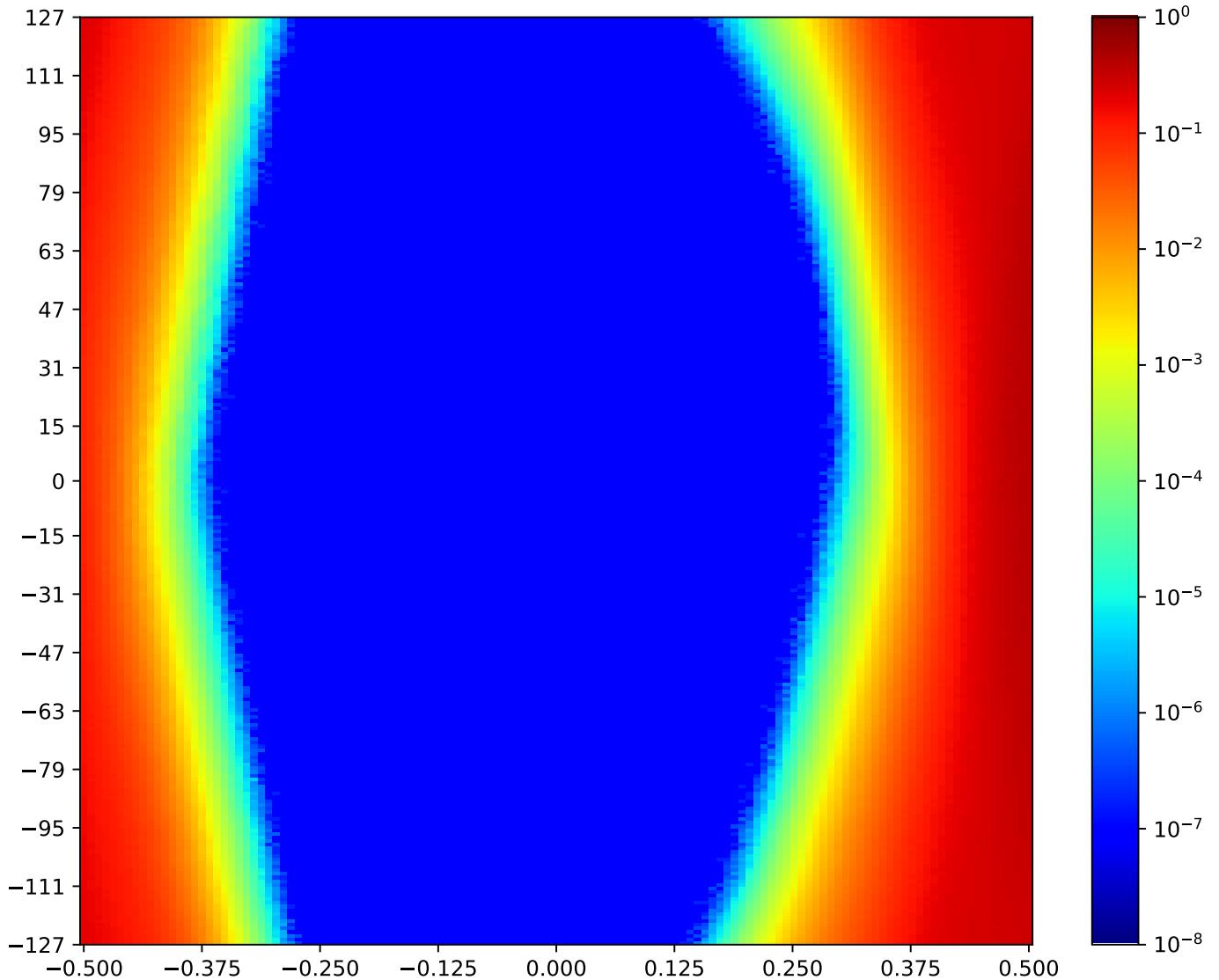


Figure 3.200: MSP\_A\_FPGA-TX1-11-RX11-11-MSP\_C\_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16 MSP\_A TX2 MSP\_C RX10 Minipod Loopback

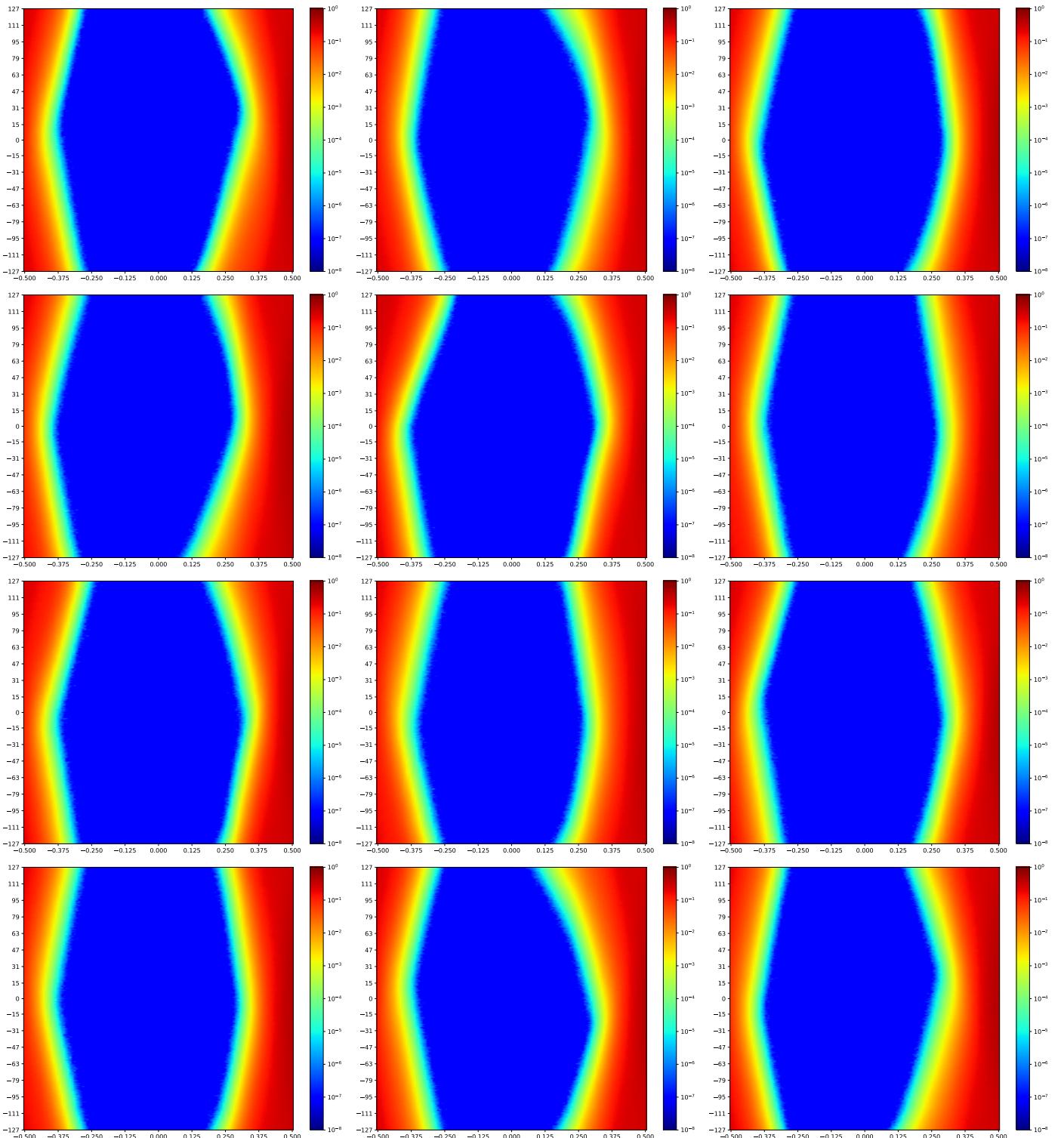


Figure 3.201: MSP\_A TX2 MSP\_C RX10 Minipod Loopback

A cross-reference to Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.214.

### 3.16.1 MSP\_A\_FPGA-TX2-00-RX10-00-MSP\_C\_FPGA

Table 3.186: MSP\_A\_FPGA-TX2-00-RX10-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:06:19		2018-Jan-24 01:07:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17317	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

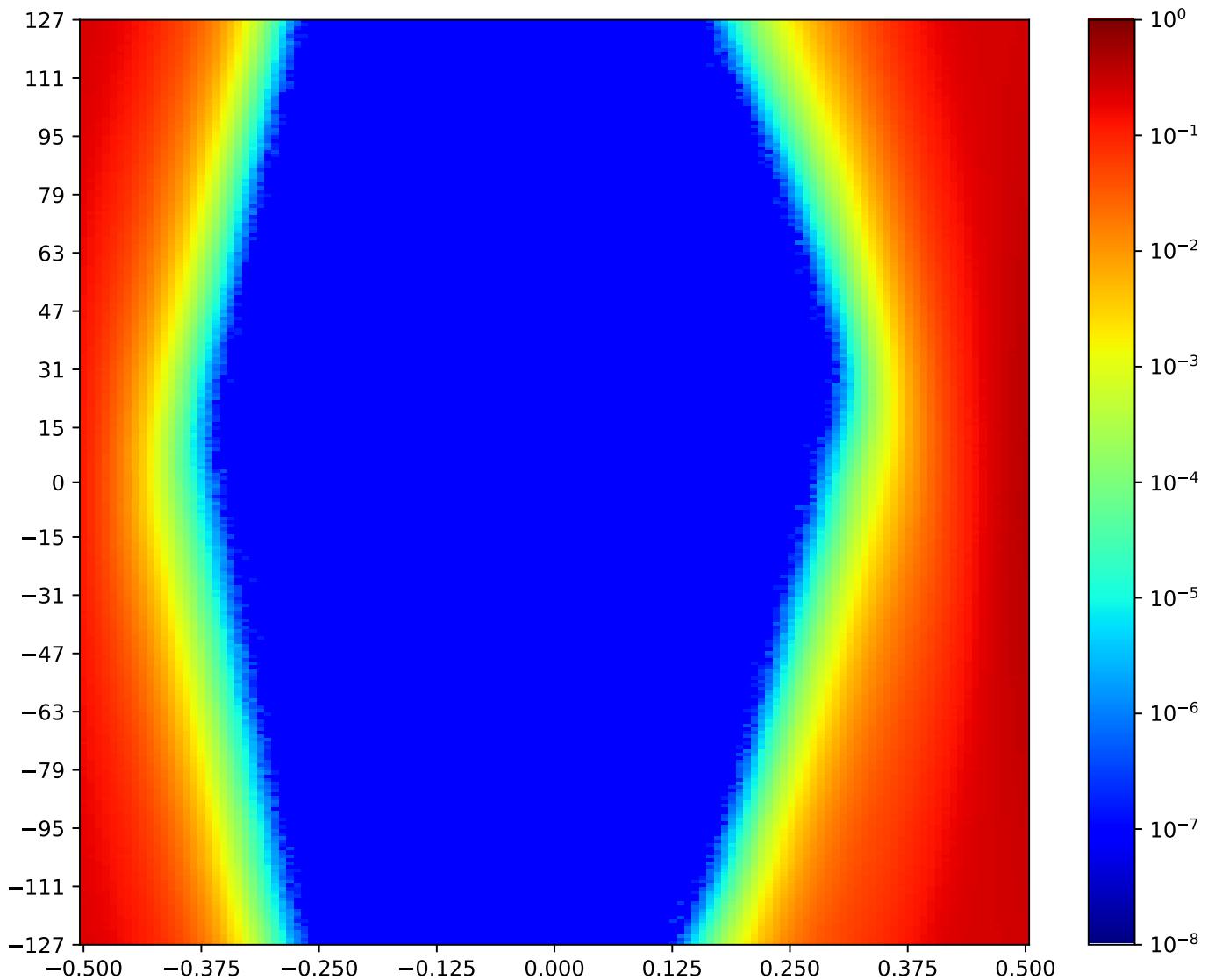


Figure 3.202: MSP\_A\_FPGA-TX2-00-RX10-00-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.2 MSP\_A\_FPGA-TX2-01-RX10-01-MSP\_C\_FPGA

Table 3.187: MSP\_A\_FPGA-TX2-01-RX10-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:04:55		2018-Jan-24 01:05:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16212	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

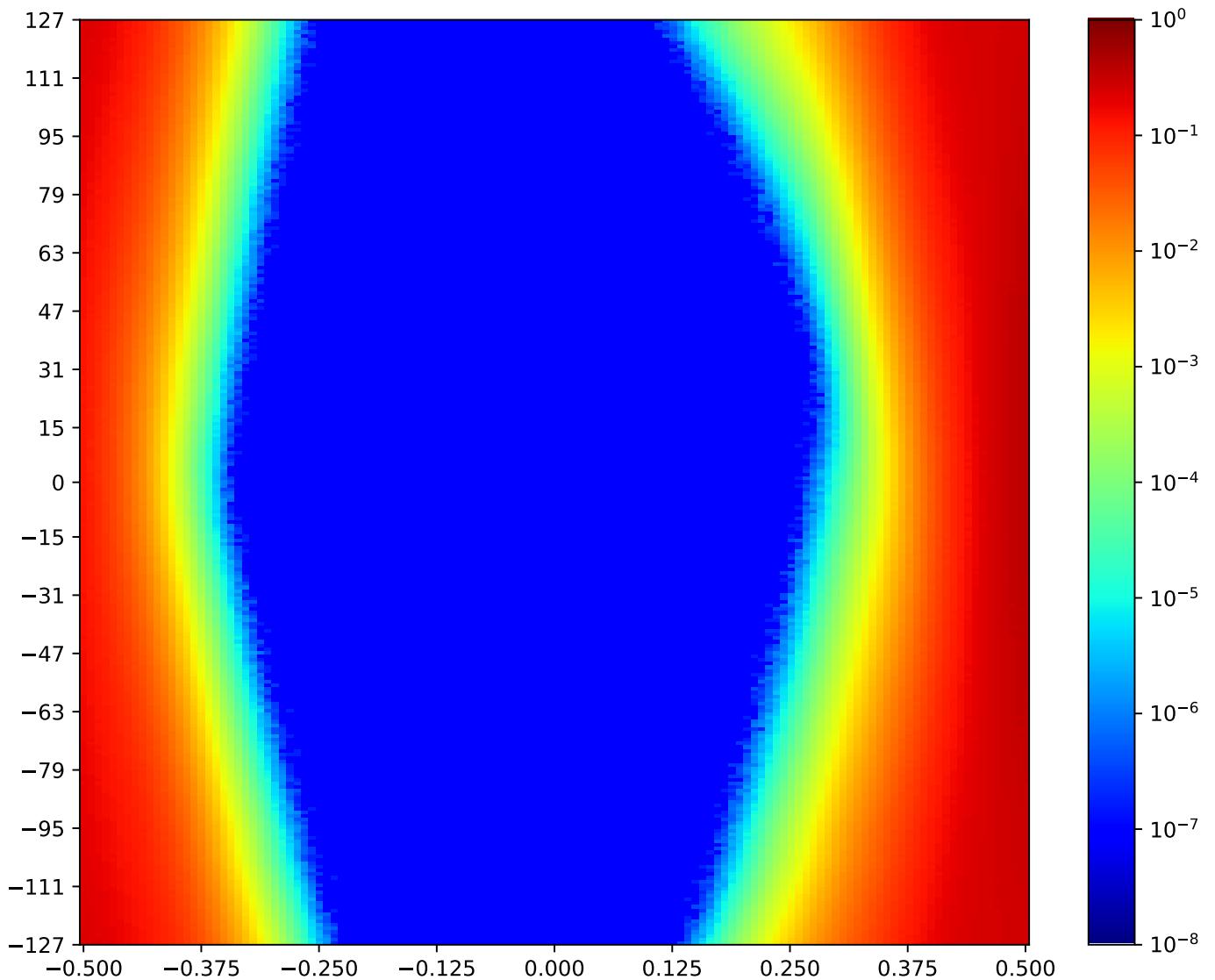


Figure 3.203: MSP\_A\_FPGA-TX2-01-RX10-01-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.3 MSP\_A\_FPGA-TX2-02-RX10-02-MSP\_C\_FPGA

Table 3.188: MSP\_A\_FPGA-TX2-02-RX10-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:08:27		2018-Jan-24 01:09:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17974	83	64.34%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

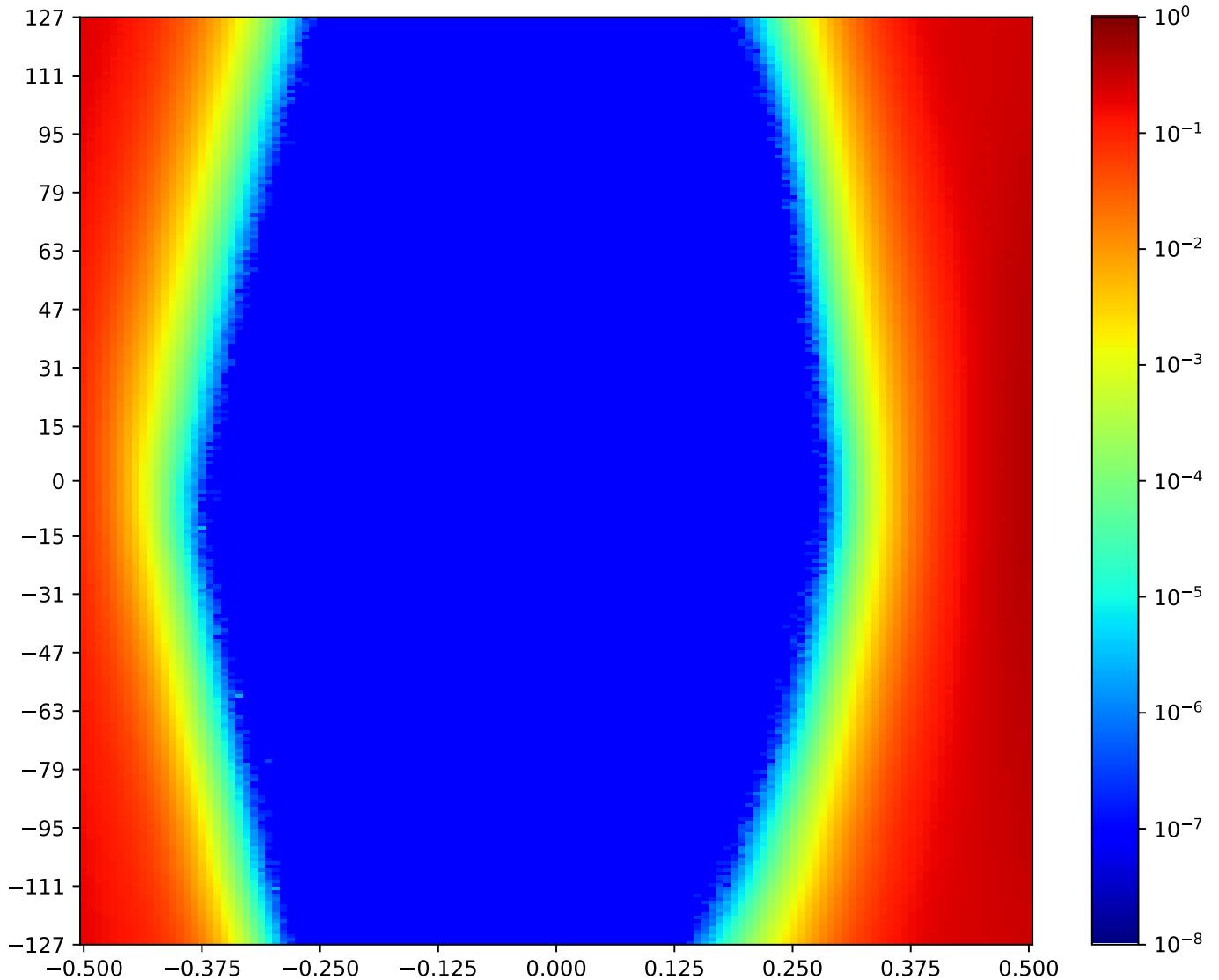


Figure 3.204: MSP\_A\_FPGA-TX2-02-RX10-02-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.4 MSP\_A\_FPGA-TX2-03-RX10-03-MSP\_C\_FPGA

Table 3.189: MSP\_A\_FPGA-TX2-03-RX10-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:04:13		2018-Jan-24 01:04:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16942	83	64.34%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

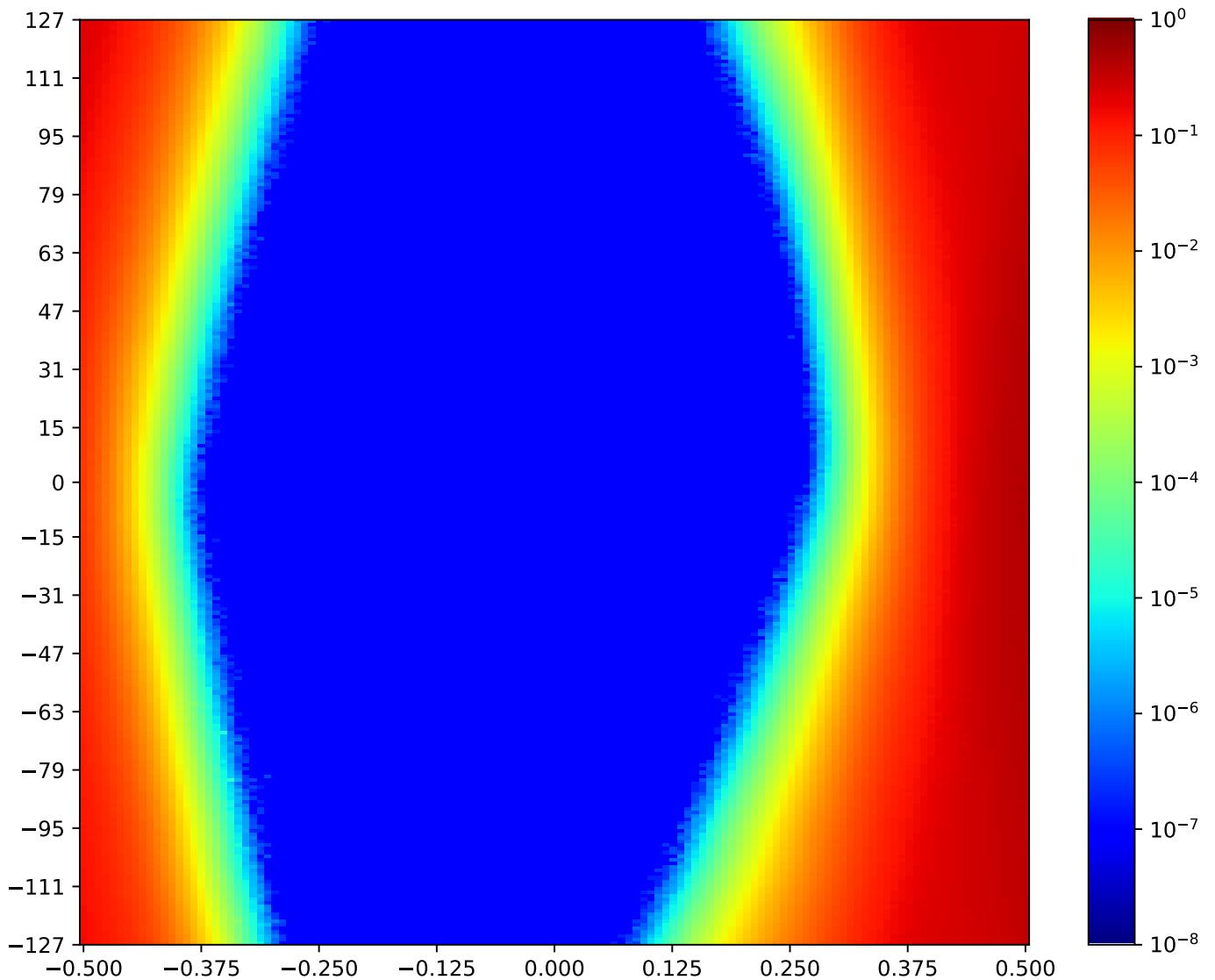


Figure 3.205: MSP\_A\_FPGA-TX2-03-RX10-03-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.5 MSP\_A\_FPGA-TX2-04-RX10-04-MSP\_C\_FPGA

Table 3.190: MSP\_A\_FPGA-TX2-04-RX10-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:10:35		2018-Jan-24 01:11:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17434	84	65.12%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

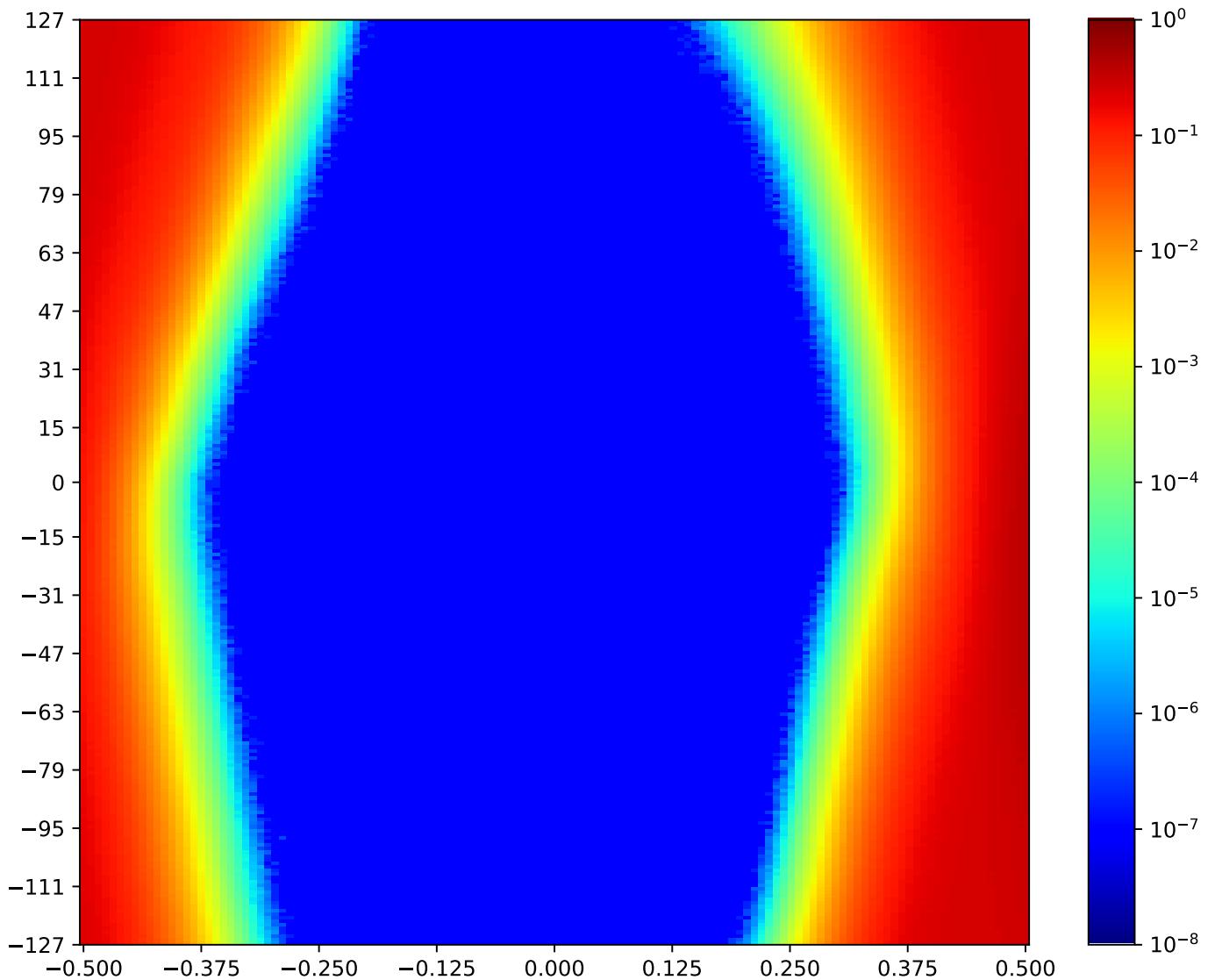


Figure 3.206: MSP\_A\_FPGA-TX2-04-RX10-04-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.6 MSP\_A\_FPGA-TX2-05-RX10-05-MSP\_C\_FPGA

Table 3.191: MSP\_A\_FPGA-TX2-05-RX10-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:05:37		2018-Jan-24 01:06:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16786	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

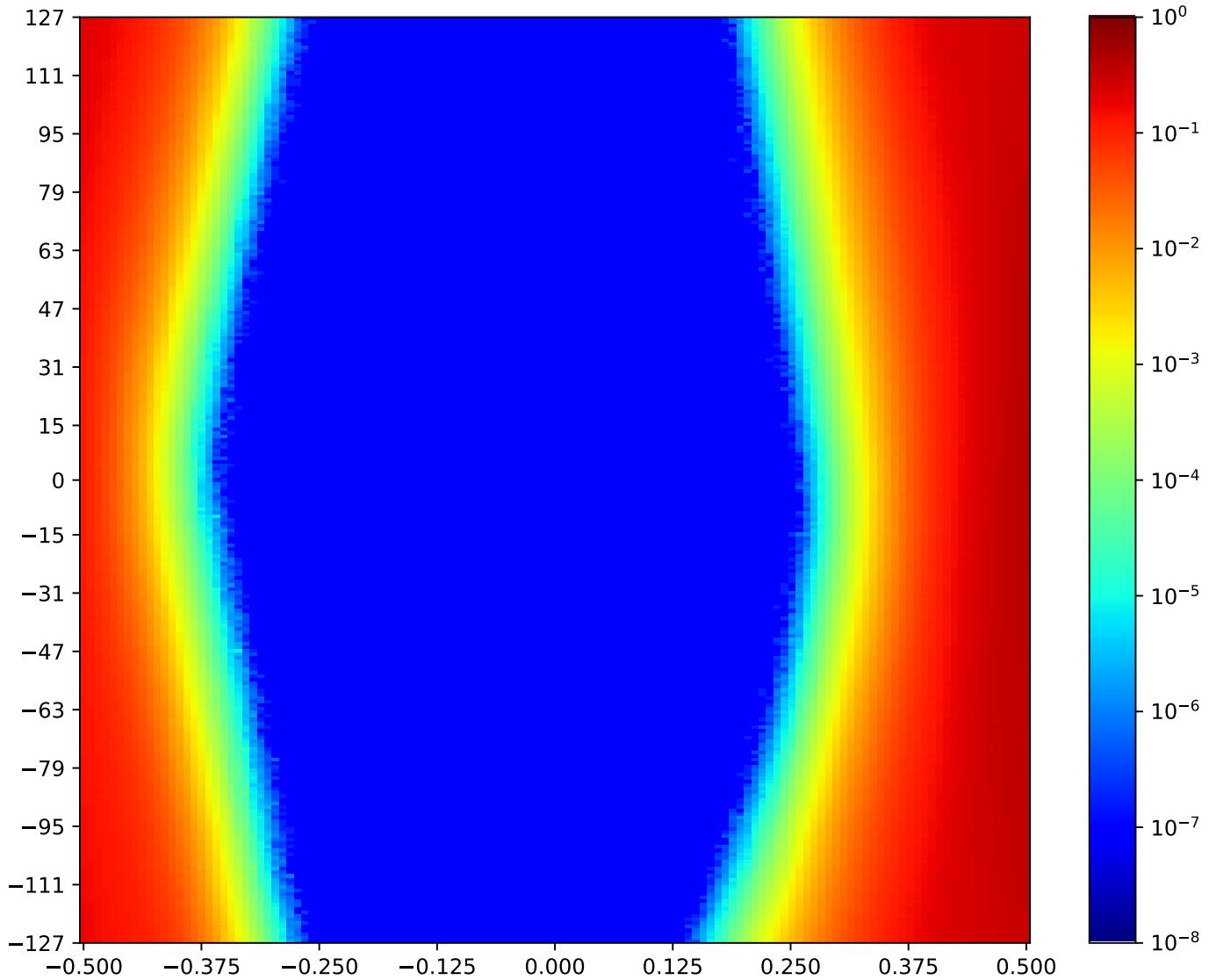


Figure 3.207: MSP\_A\_FPGA-TX2-05-RX10-05-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.7 MSP\_A\_FPGA-TX2-06-RX10-06-MSP\_C\_FPGA

Table 3.192: MSP\_A\_FPGA-TX2-06-RX10-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:12:00		2018-Jan-24 01:12:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17901	83	64.34%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

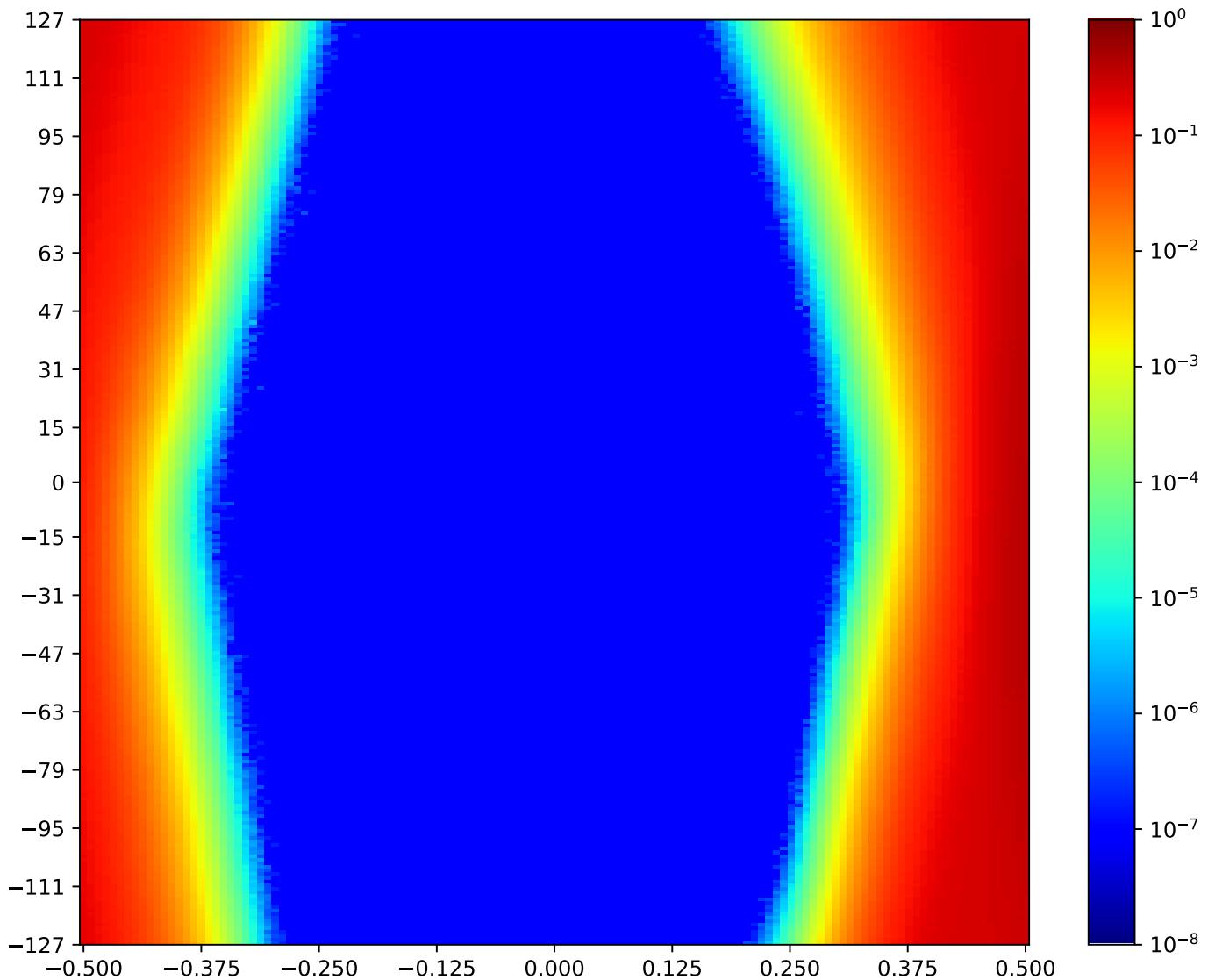


Figure 3.208: MSP\_A\_FPGA-TX2-06-RX10-06-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.8 MSP\_A\_FPGA-TX2-07-RX10-07-MSP\_C\_FPGA

Table 3.193: MSP\_A\_FPGA-TX2-07-RX10-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:07:02		2018-Jan-24 01:07:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16150	74	56.59%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

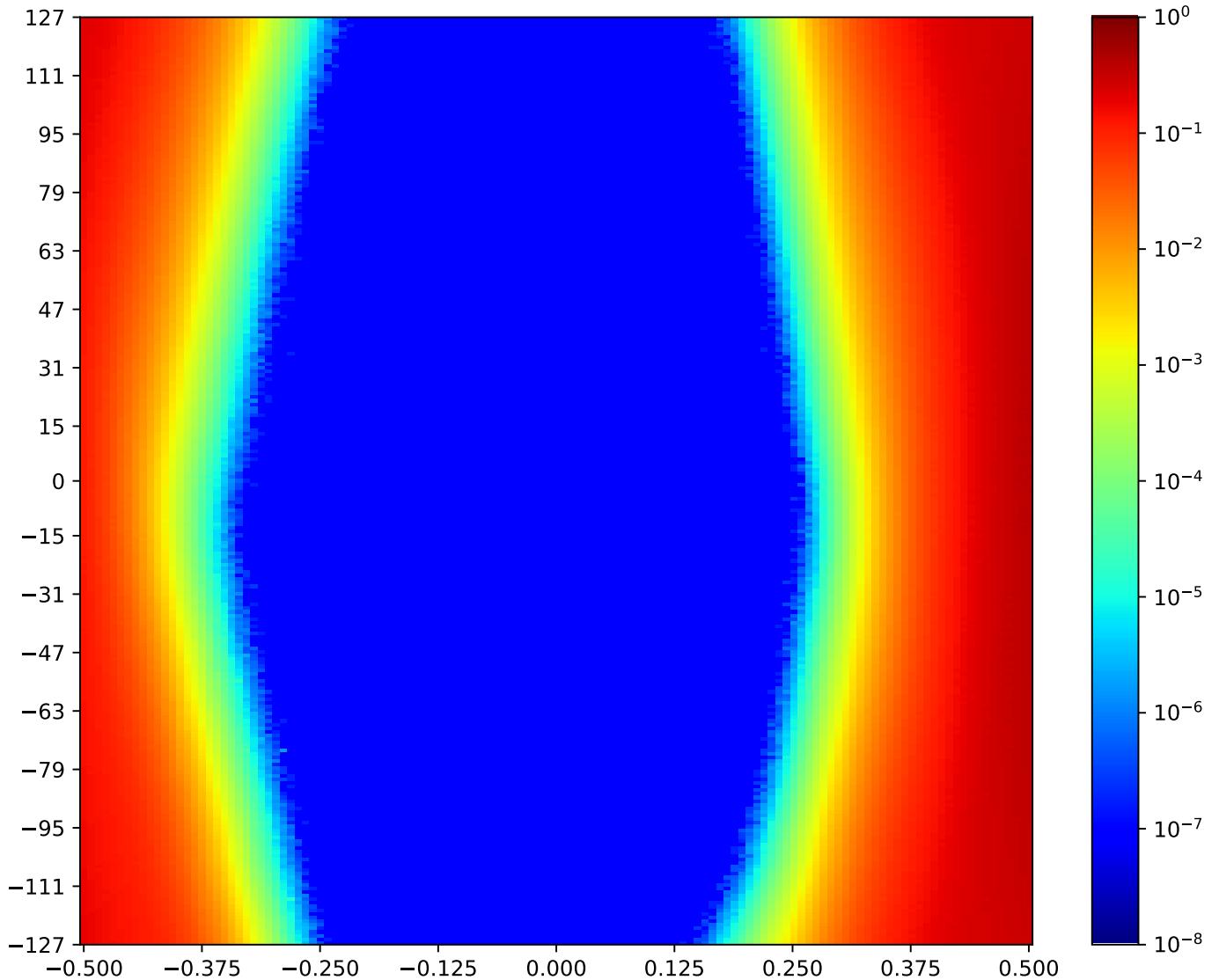


Figure 3.209: MSP\_A\_FPGA-TX2-07-RX10-07-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.9 MSP\_A\_FPGA-TX2-08-RX10-08-MSP\_C\_FPGA

Table 3.194: MSP\_A\_FPGA-TX2-08-RX10-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:11:17		2018-Jan-24 01:12:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17522	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

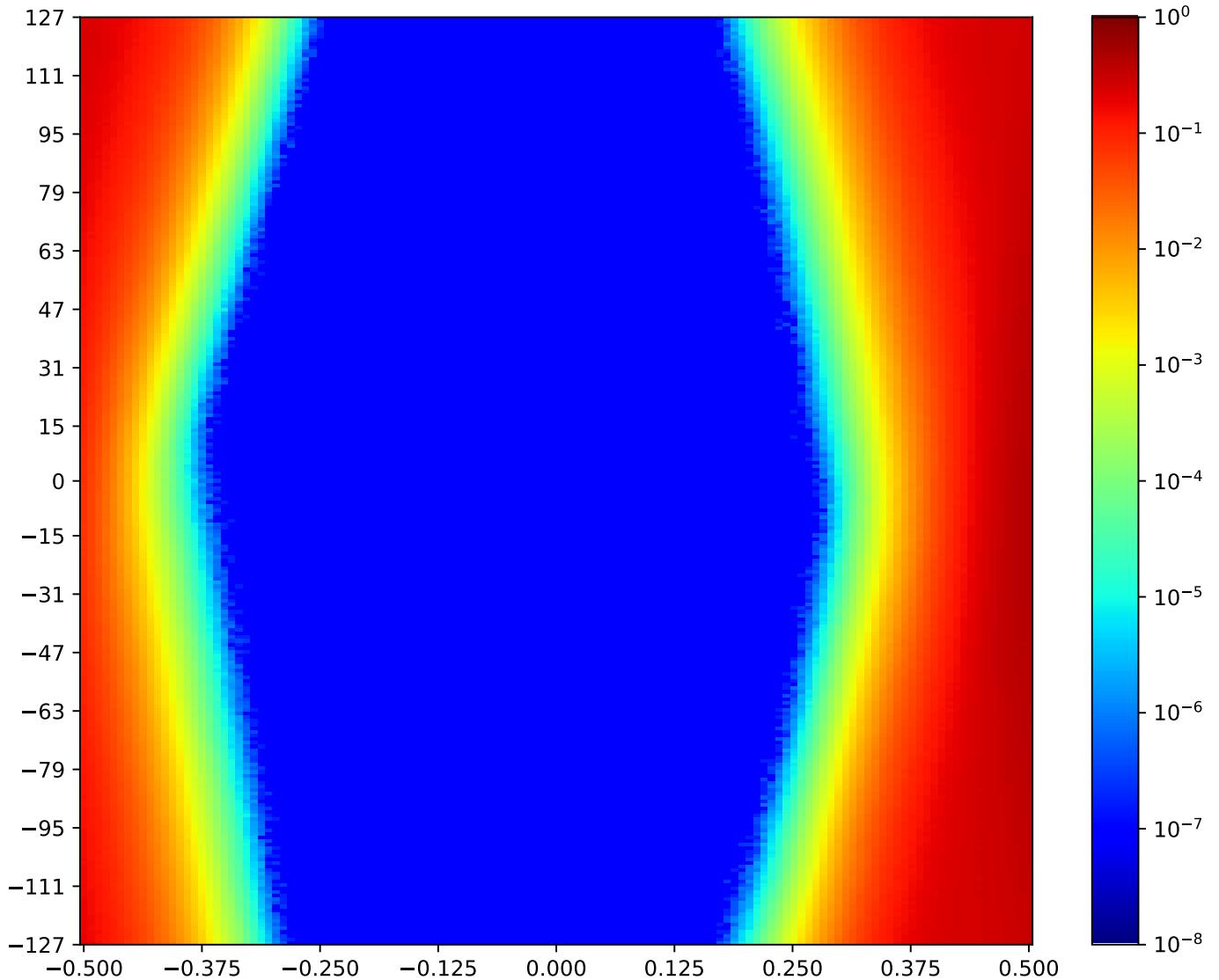


Figure 3.210: MSP\_A\_FPGA-TX2-08-RX10-08-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.10 MSP\_A\_FPGA-TX2-09-RX10-09-MSP\_C\_FPGA

Table 3.195: MSP\_A\_FPGA-TX2-09-RX10-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:07:44		2018-Jan-24 01:08:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17951	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

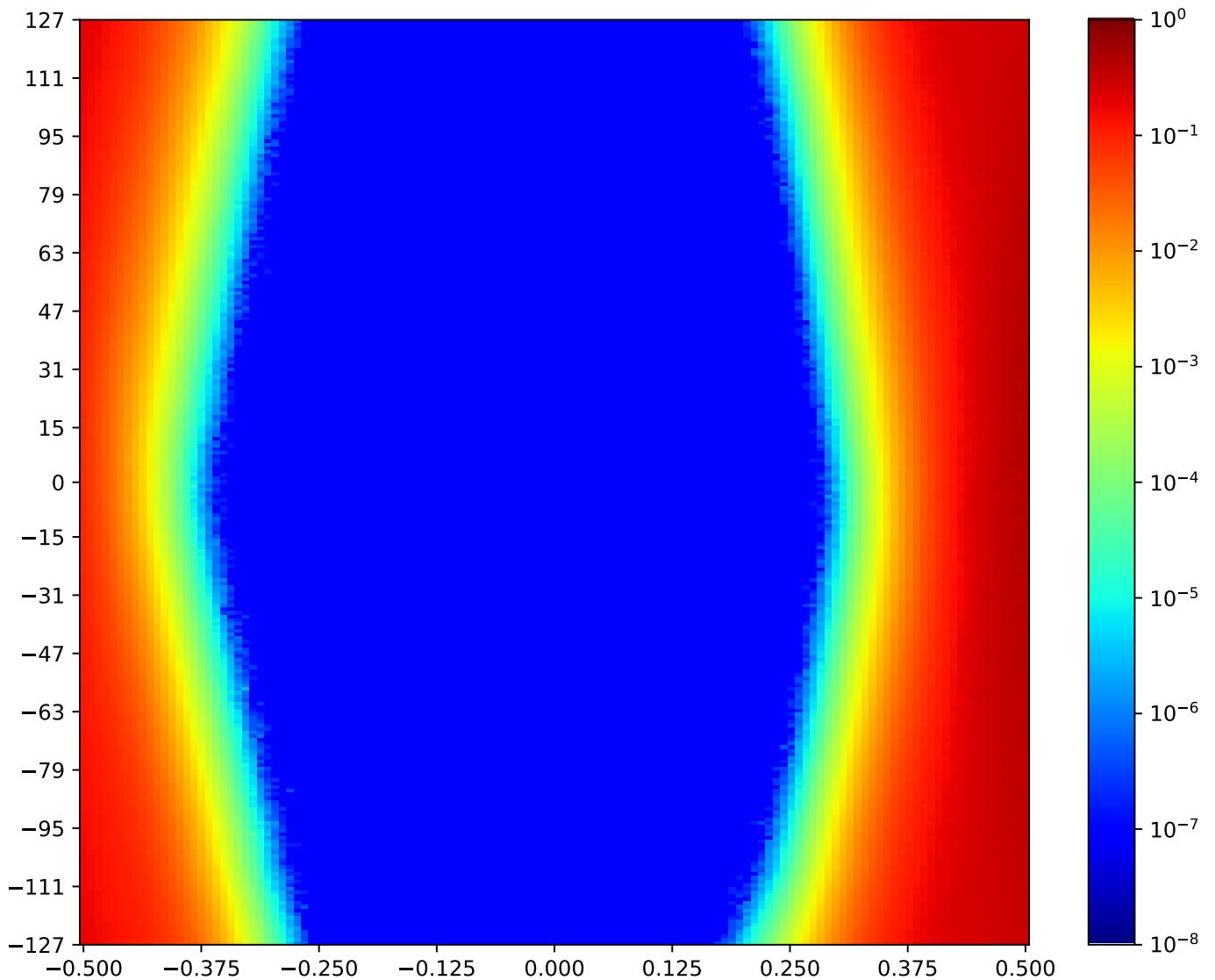


Figure 3.211: MSP\_A\_FPGA-TX2-09-RX10-09-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.11 MSP\_A\_FPGA-TX2-10-RX10-10-MSP\_C\_FPGA

Table 3.196: MSP\_A\_FPGA-TX2-10-RX10-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:09:52		2018-Jan-24 01:10:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16343	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

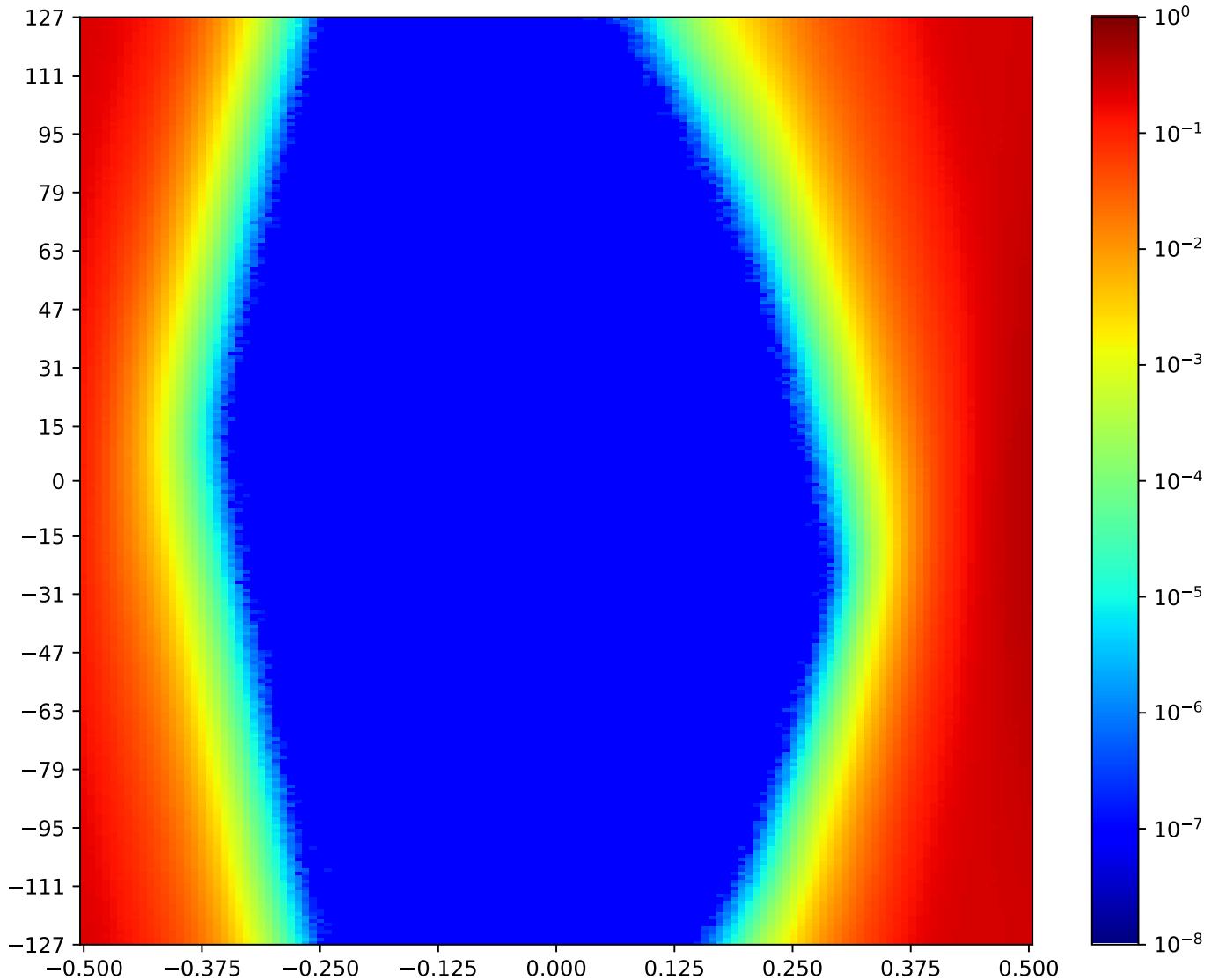


Figure 3.212: MSP\_A\_FPGA-TX2-10-RX10-10-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.16.12 MSP\_A\_FPGA-TX2-11-RX10-11-MSP\_C\_FPGA

Table 3.197: MSP\_A\_FPGA-TX2-11-RX10-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:09:10		2018-Jan-24 01:09:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16534	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

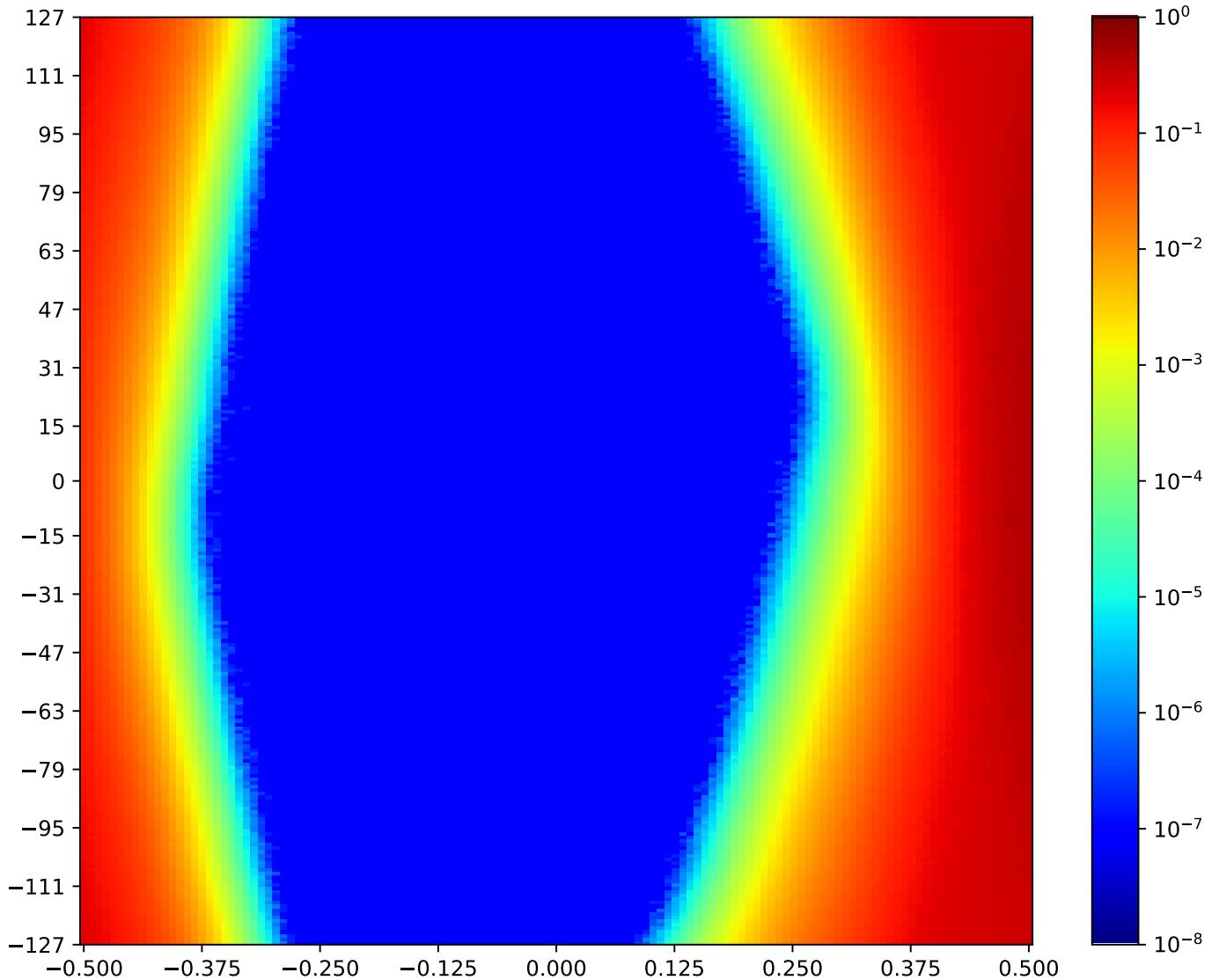


Figure 3.213: MSP\_A\_FPGA-TX2-11-RX10-11-MSP\_C\_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17 MSP\_C TX3 MSP\_A RX2 Minipod Loopback

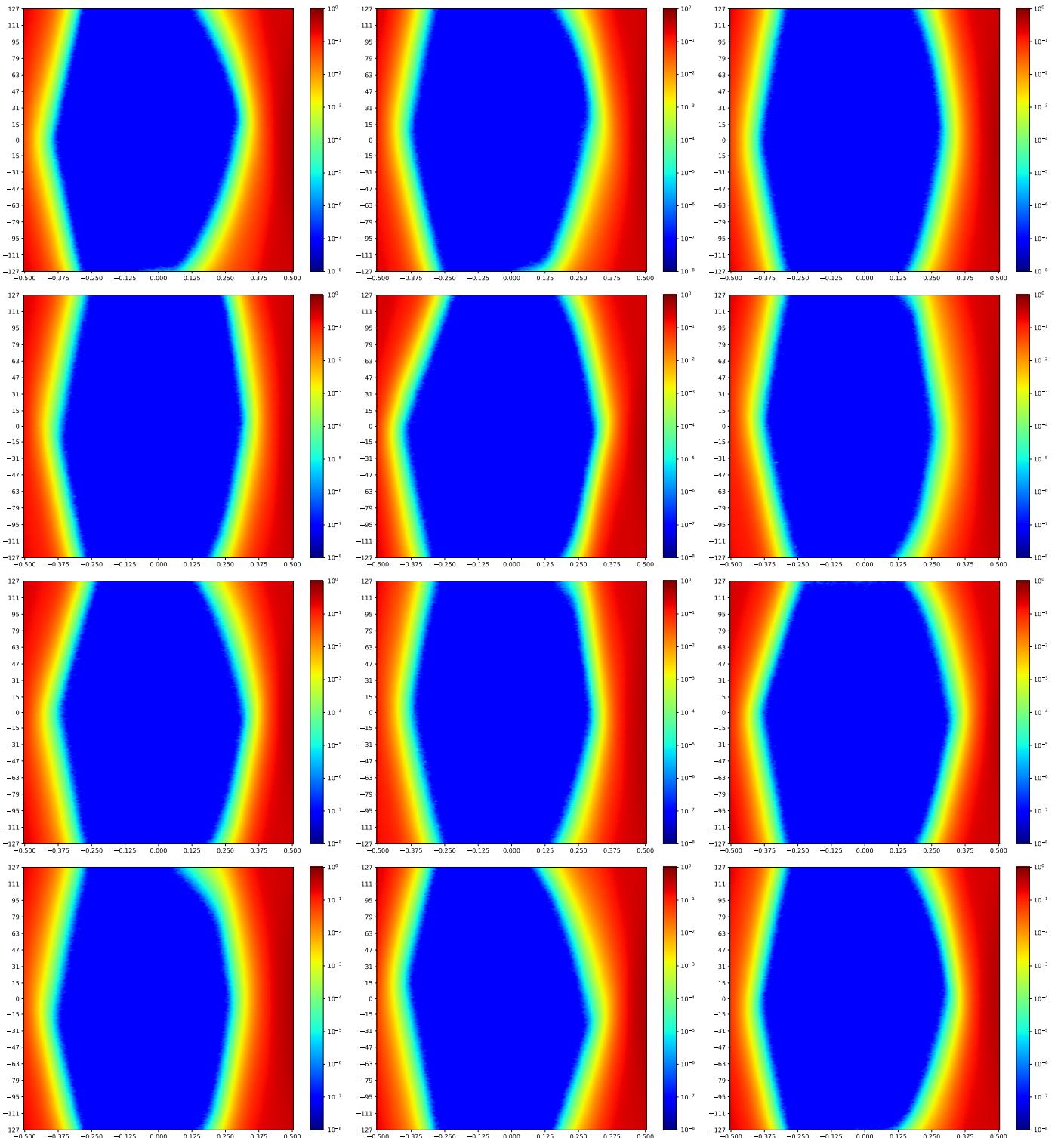


Figure 3.214: MSP\_C TX3 MSP\_A RX2 Minipod Loopback

A cross-reference to Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.227.

### 3.17.1 MSP\_C\_FPGA-TX3-00-RX2-00-MSP\_A\_FPGA

Table 3.198: MSP\_C\_FPGA-TX3-00-RX2-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:14:51		2018-Jan-24 01:15:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17145	82	63.57%	249	97.65%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

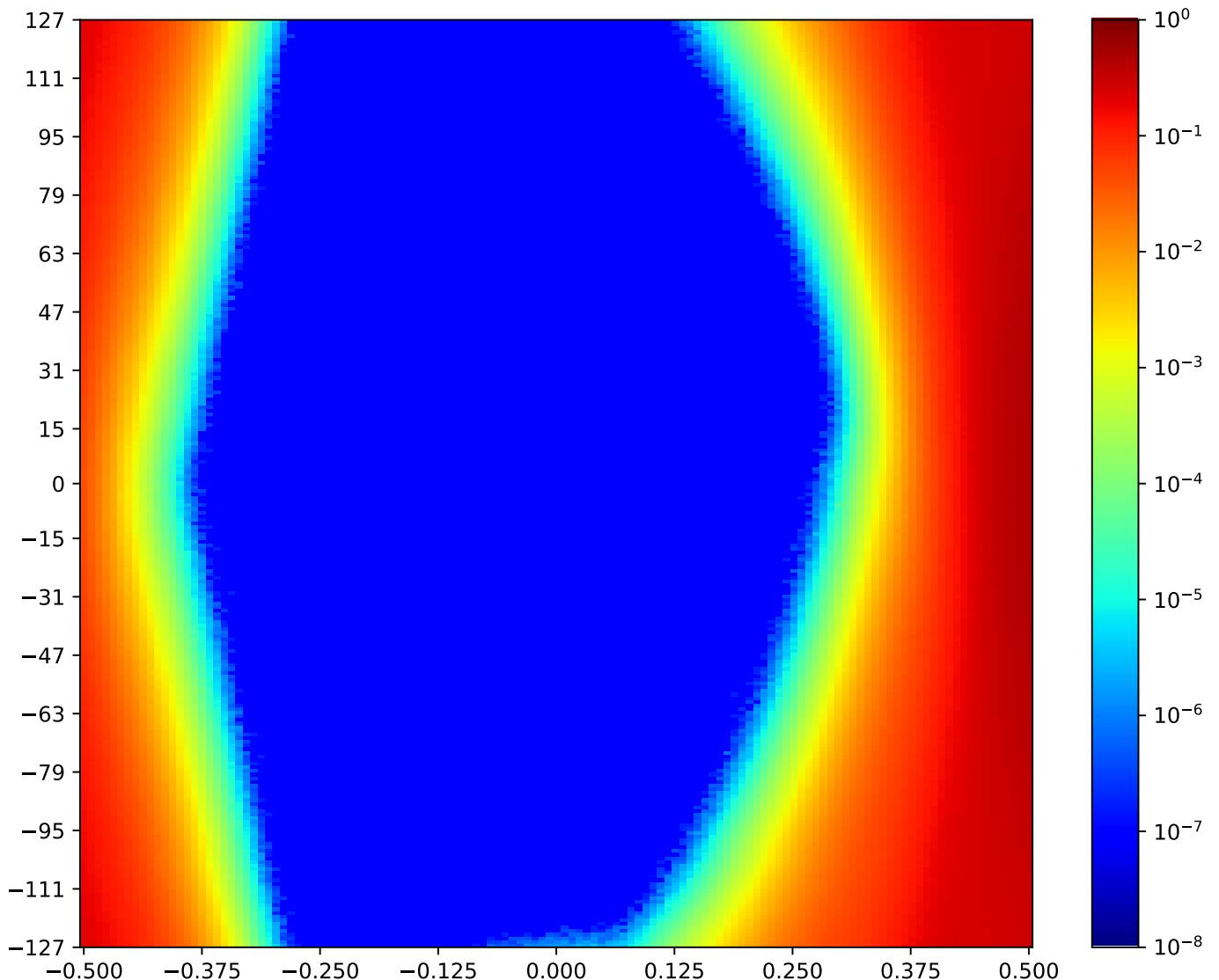


Figure 3.215: MSP\_C\_FPGA-TX3-00-RX2-00-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.2 MSP\_C\_FPGA-TX3-01-RX2-01-MSP\_A\_FPGA

Table 3.199: MSP\_C\_FPGA-TX3-01-RX2-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:16:16		2018-Jan-24 01:16:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16708	78	60.47%	251	98.04%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

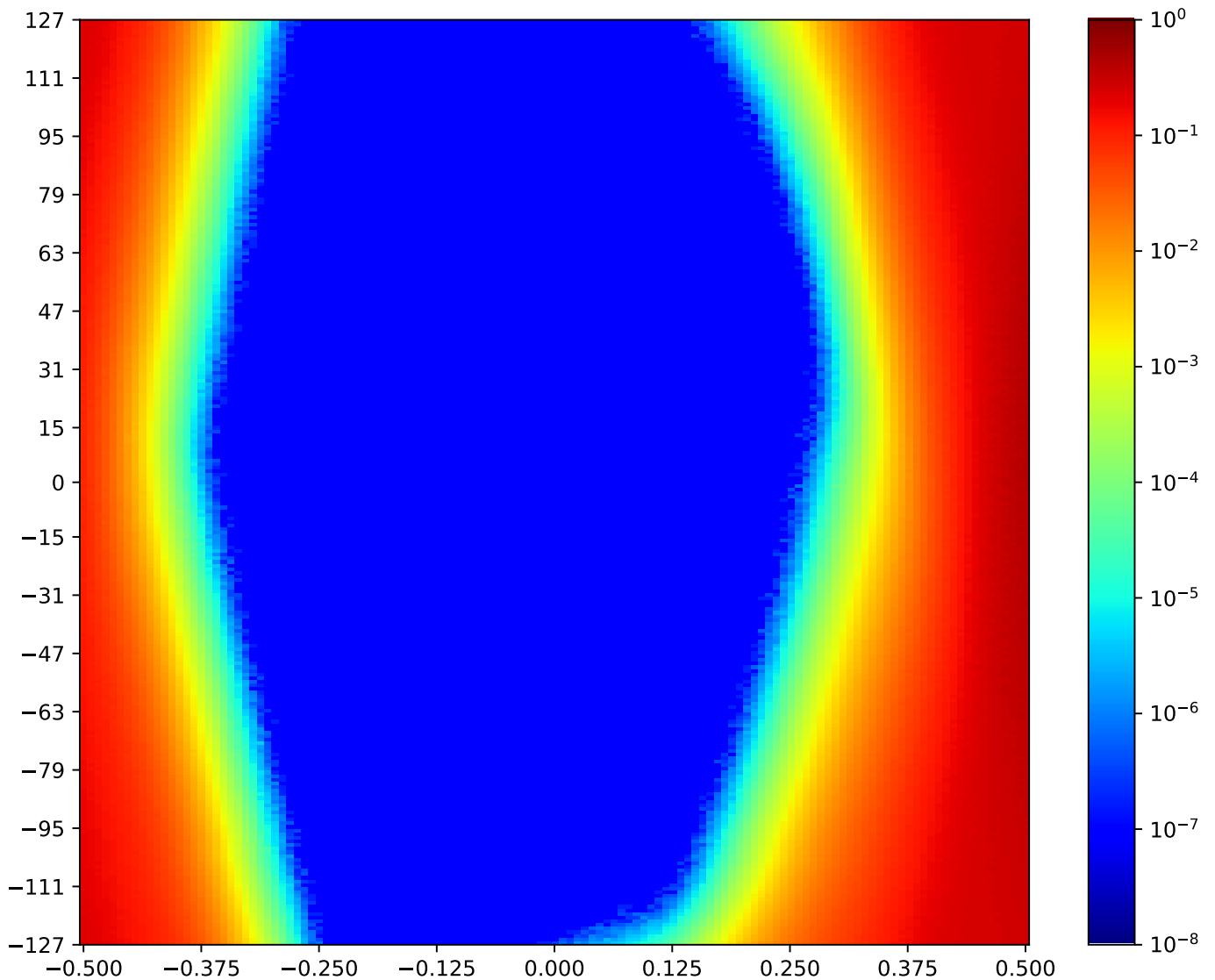


Figure 3.216: MSP\_C\_FPGA-TX3-01-RX2-01-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.3 MSP\_C\_FPGA-TX3-02-RX2-02-MSP\_A\_FPGA

Table 3.200: MSP\_C\_FPGA-TX3-02-RX2-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:16:58		2018-Jan-24 01:17:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17918	83	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

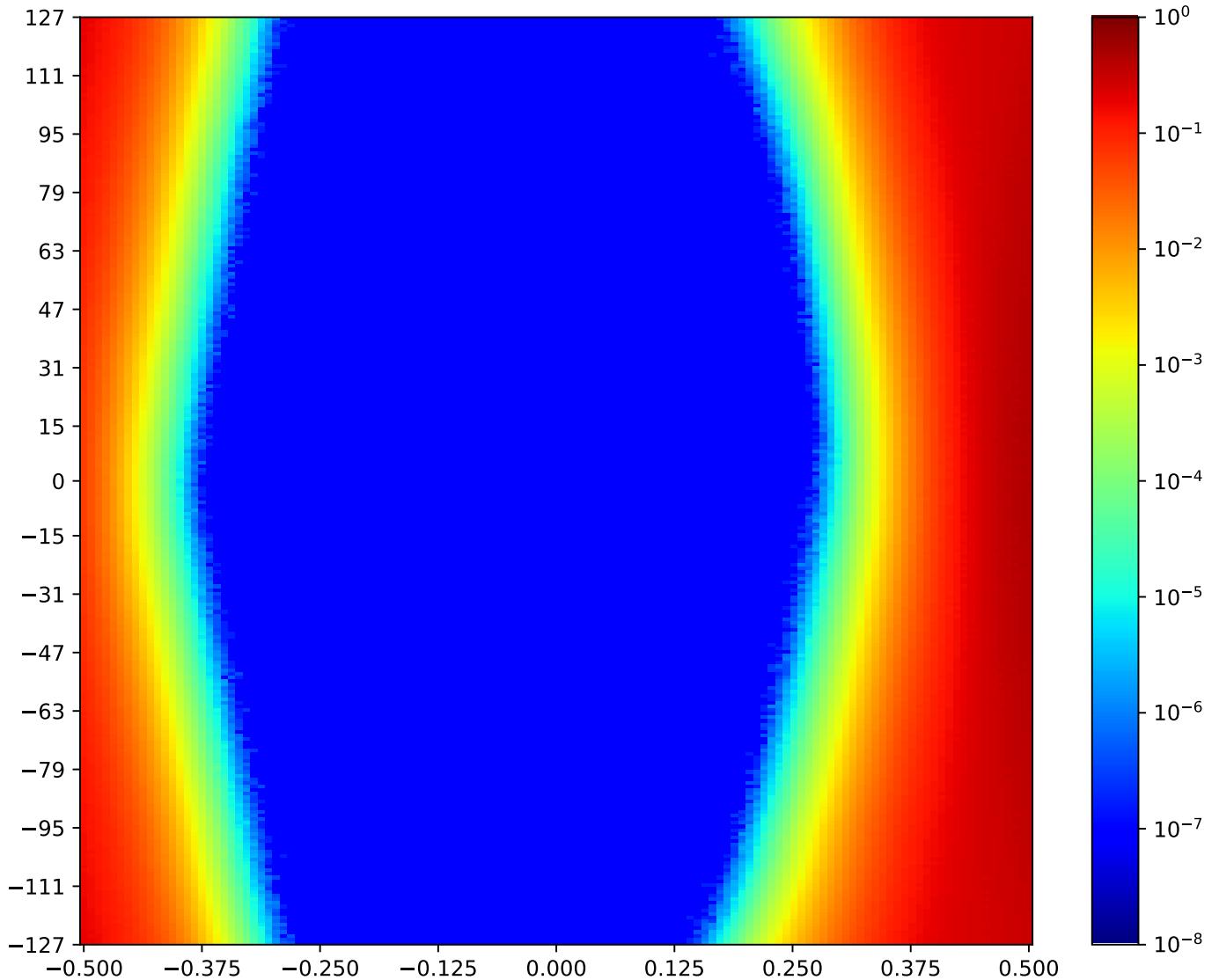


Figure 3.217: MSP\_C\_FPGA-TX3-02-RX2-02-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.4 MSP\_C\_FPGA-TX3-03-RX2-03-MSP\_A\_FPGA

Table 3.201: MSP\_C\_FPGA-TX3-03-RX2-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:13:25		2018-Jan-24 01:14:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18307	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

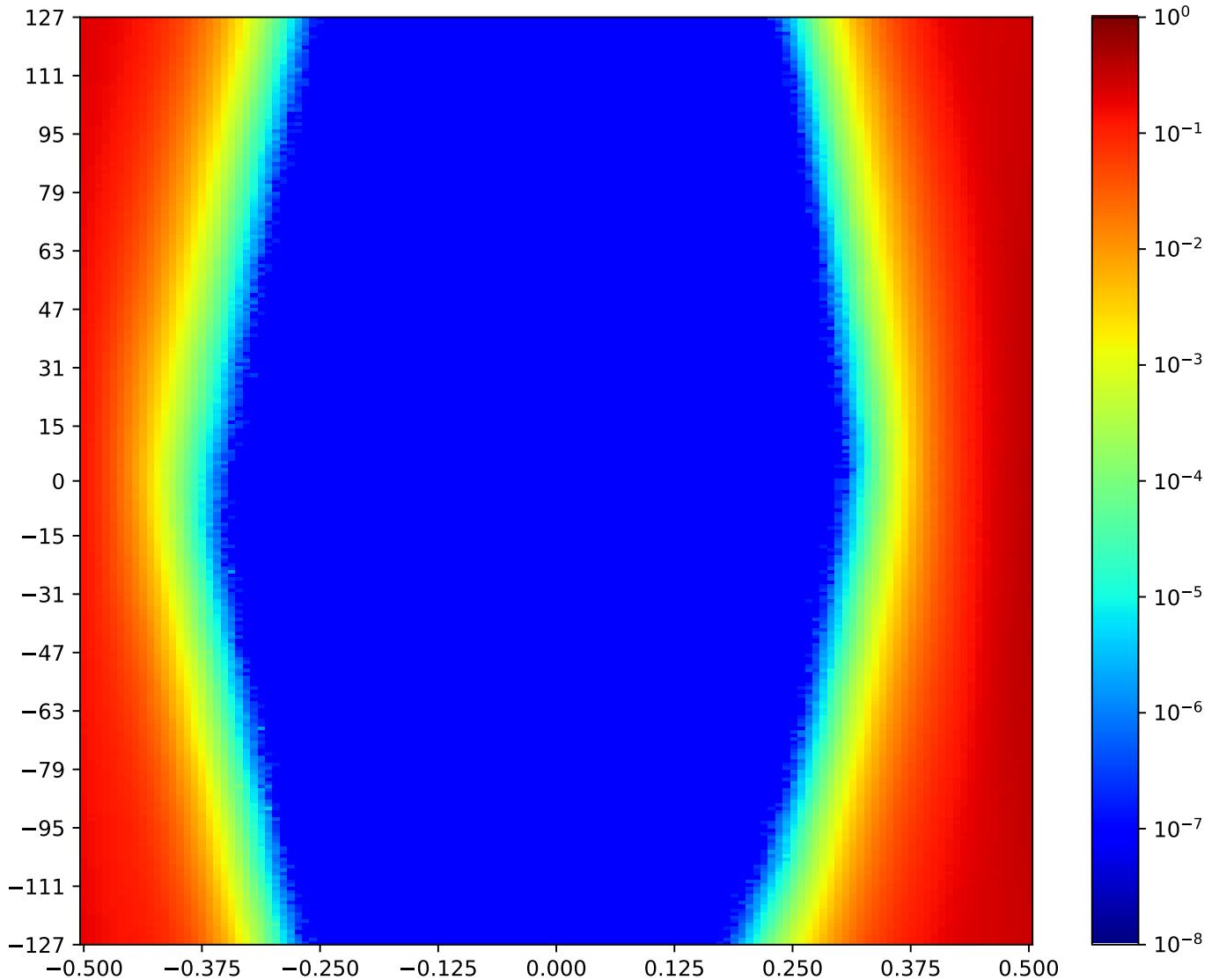


Figure 3.218: MSP\_C\_FPGA-TX3-03-RX2-03-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.5 MSP\_C\_FPGA-TX3-04-RX2-04-MSP\_A\_FPGA

Table 3.202: MSP\_C\_FPGA-TX3-04-RX2-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:19:06		2018-Jan-24 01:19:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18110	85	65.89%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

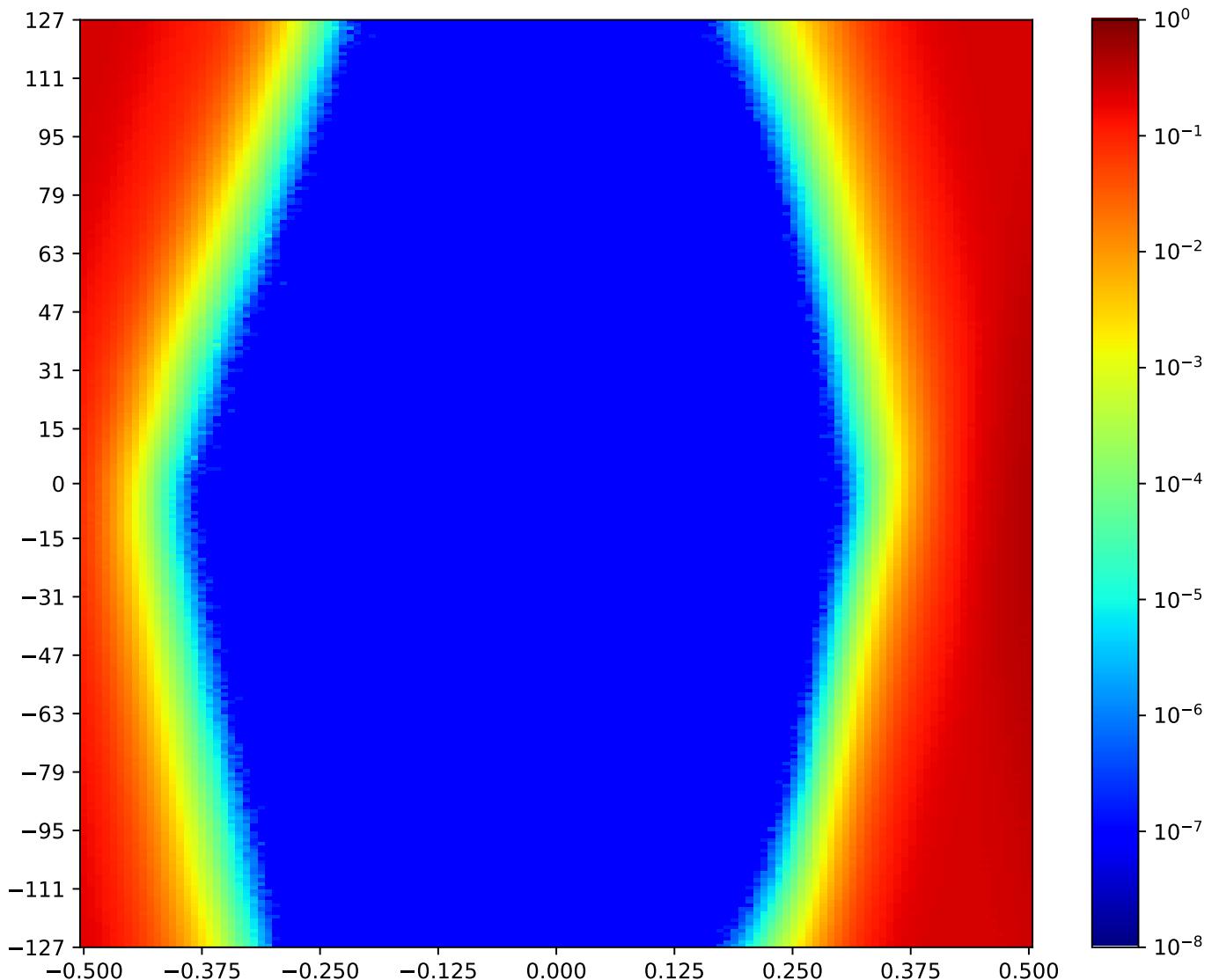


Figure 3.219: MSP\_C\_FPGA-TX3-04-RX2-04-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.6 MSP\_C\_FPGA-TX3-05-RX2-05-MSP\_A\_FPGA

Table 3.203: MSP\_C\_FPGA-TX3-05-RX2-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:12:42		2018-Jan-24 01:13:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16217	77	58.14%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

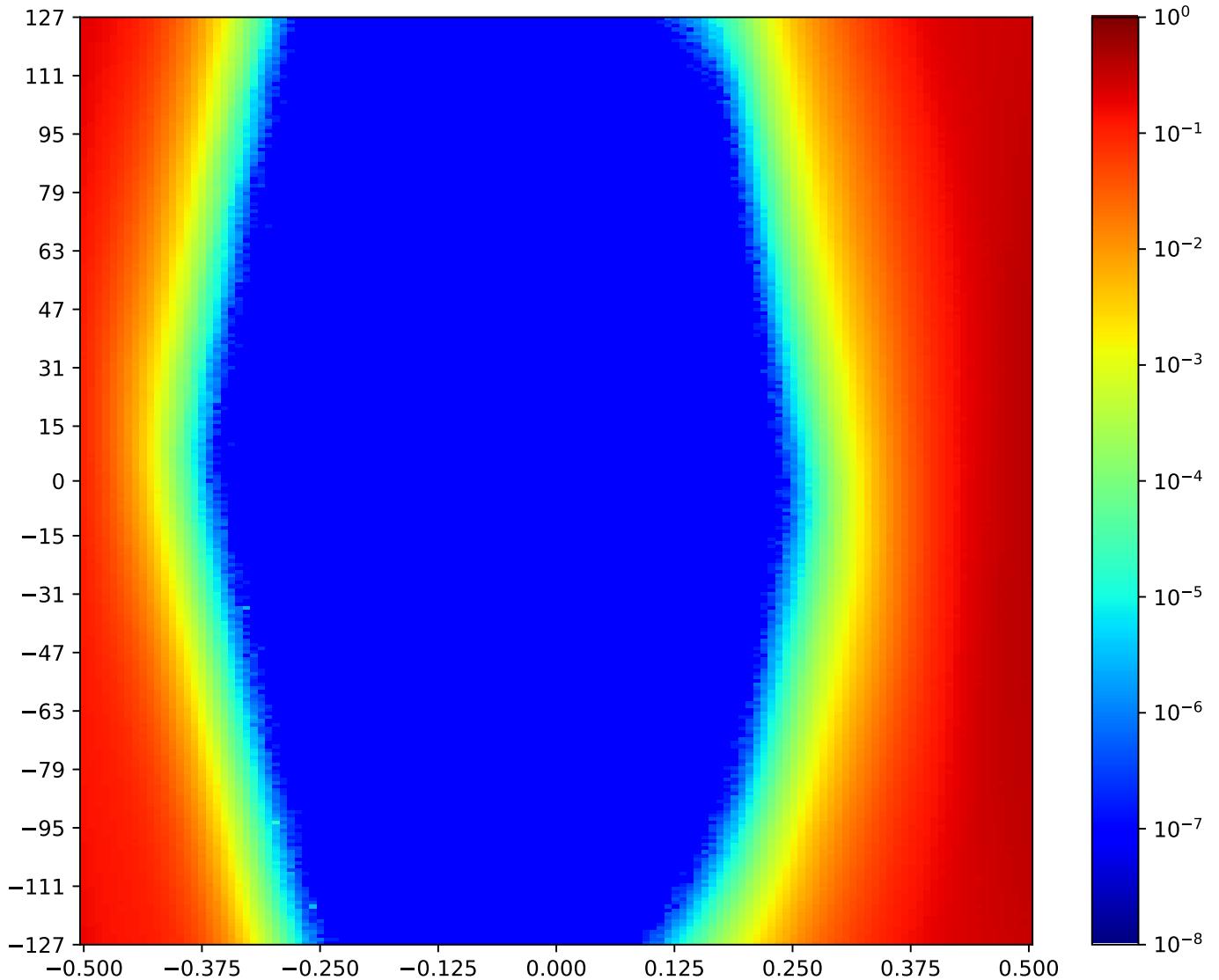


Figure 3.220: MSP\_C\_FPGA-TX3-05-RX2-05-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.7 MSP\_C\_FPGA-TX3-06-RX2-06-MSP\_A\_FPGA

Table 3.204: MSP\_C\_FPGA-TX3-06-RX2-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:20:32		2018-Jan-24 01:21:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17423	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

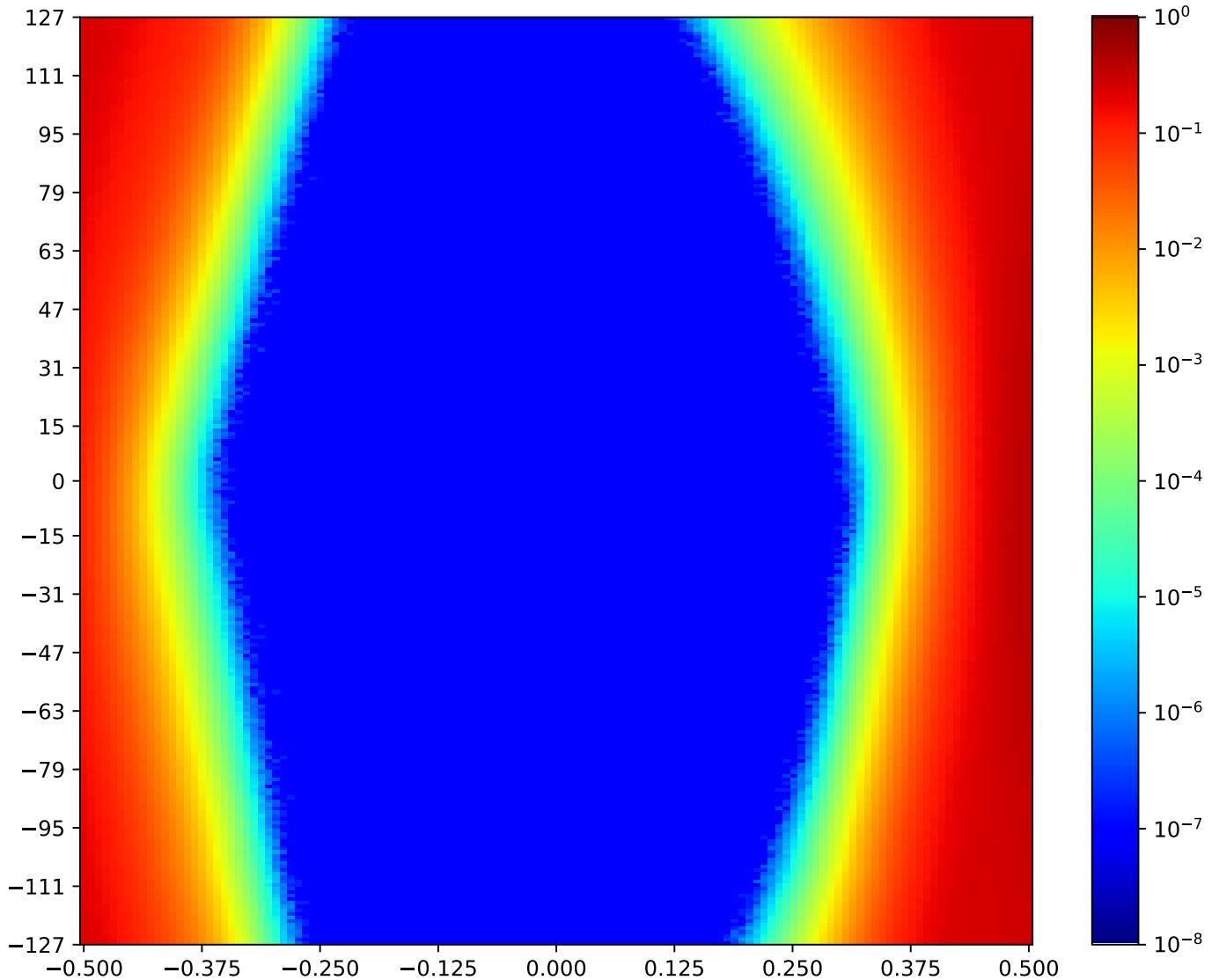


Figure 3.221: MSP\_C\_FPGA-TX3-06-RX2-06-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.8 MSP\_C\_FPGA-TX3-07-RX2-07-MSP\_A\_FPGA

Table 3.205: MSP\_C\_FPGA-TX3-07-RX2-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:14:07		2018-Jan-24 01:14:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17349	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

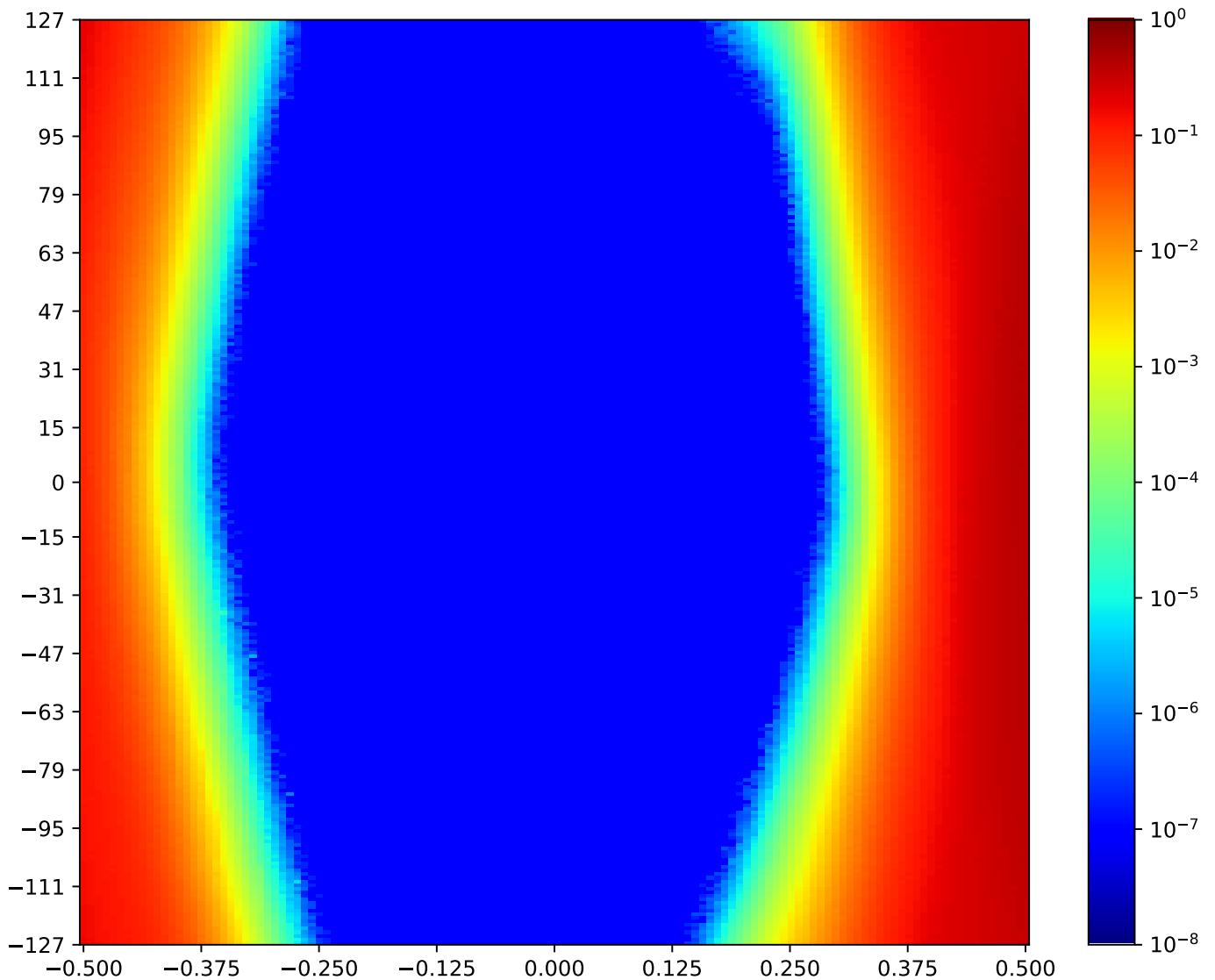


Figure 3.222: MSP\_C\_FPGA-TX3-07-RX2-07-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.9 MSP\_C\_FPGA-TX3-08-RX2-08-MSP\_A\_FPGA

Table 3.206: MSP\_C\_FPGA-TX3-08-RX2-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:19:49		2018-Jan-24 01:20:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17708	86	65.12%	252	97.25%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

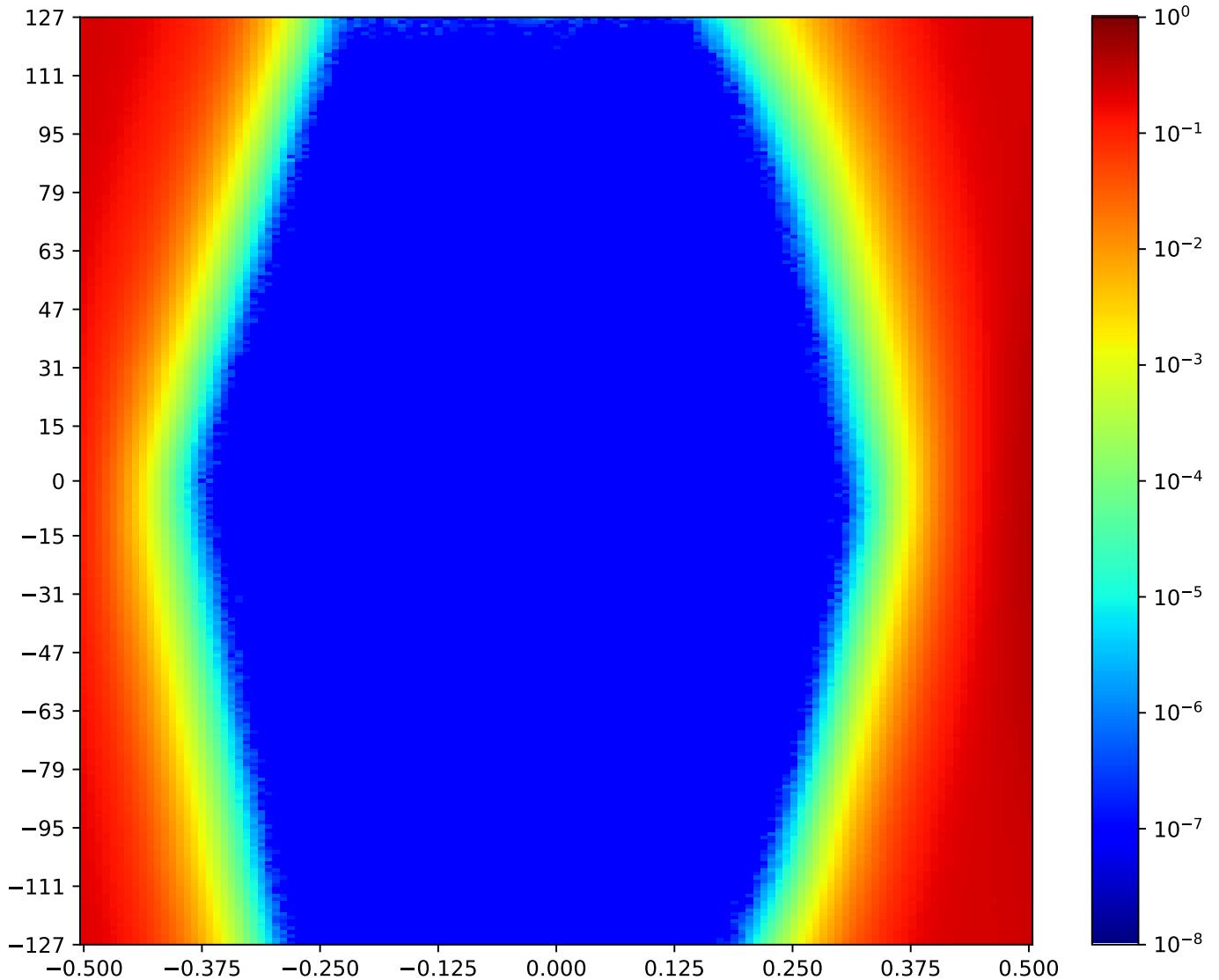


Figure 3.223: MSP\_C\_FPGA-TX3-08-RX2-08-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.10 MSP\_C\_FPGA-TX3-09-RX2-09-MSP\_A\_FPGA

Table 3.207: MSP\_C\_FPGA-TX3-09-RX2-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:15:33		2018-Jan-24 01:16:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16793	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

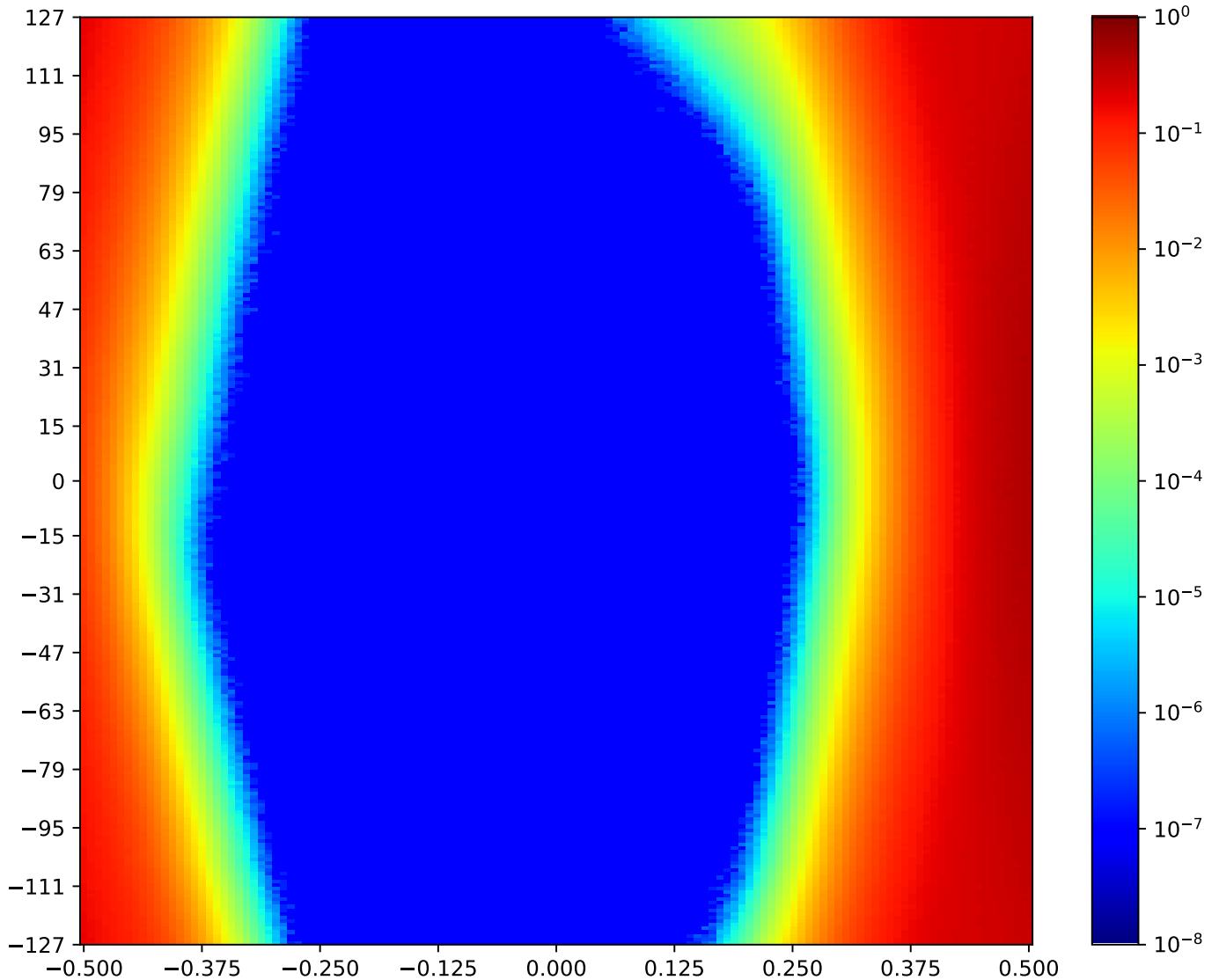


Figure 3.224: MSP\_C\_FPGA-TX3-09-RX2-09-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.11 MSP\_C\_FPGA-TX3-10-RX2-10-MSP\_A\_FPGA

Table 3.208: MSP\_C\_FPGA-TX3-10-RX2-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:18:23		2018-Jan-24 01:19:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16894	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

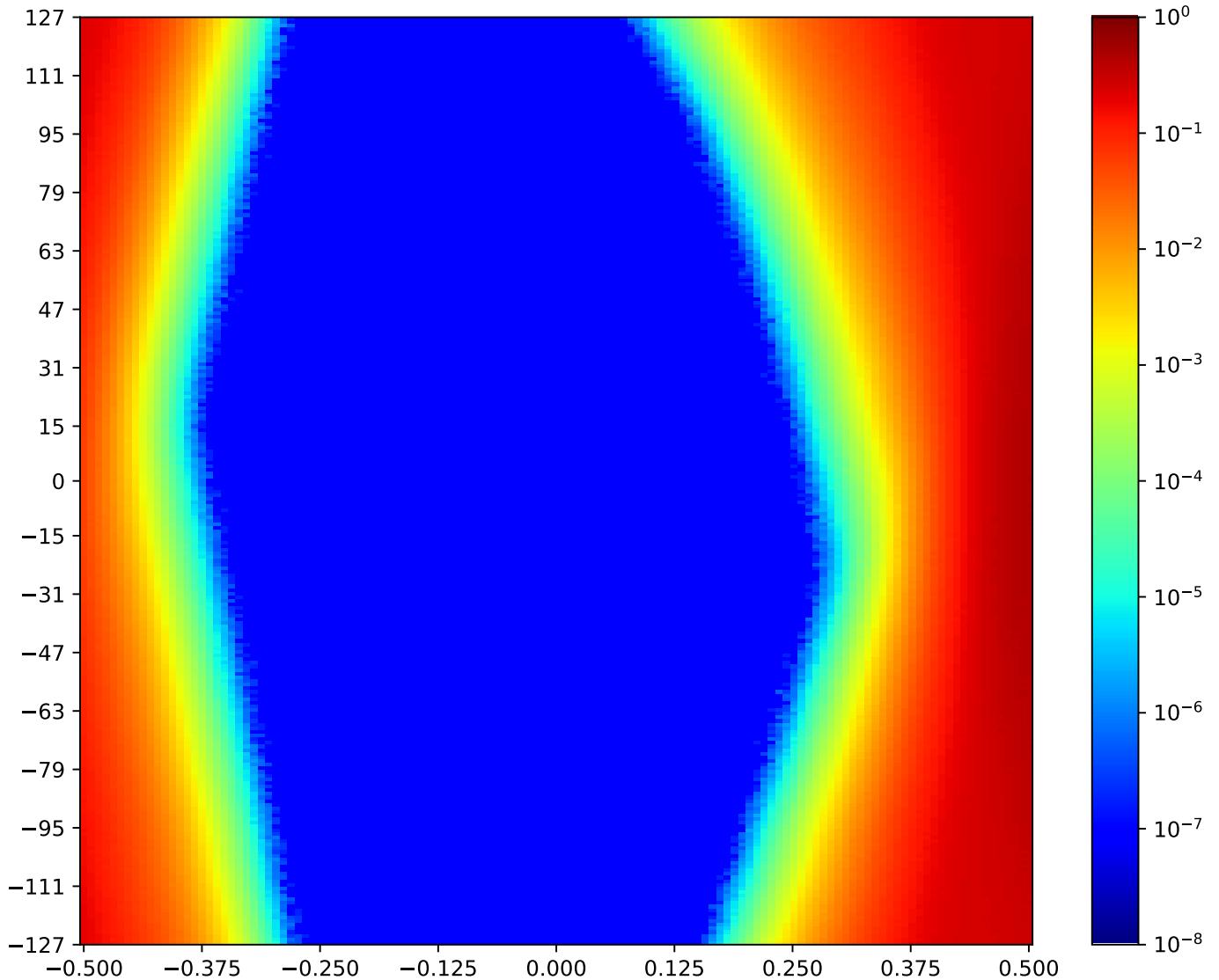


Figure 3.225: MSP\_C\_FPGA-TX3-10-RX2-10-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.17.12 MSP\_C\_FPGA-TX3-11-RX2-11-MSP\_A\_FPGA

Table 3.209: MSP\_C\_FPGA-TX3-11-RX2-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:17:41		2018-Jan-24 01:18:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17792	83	64.34%	254	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

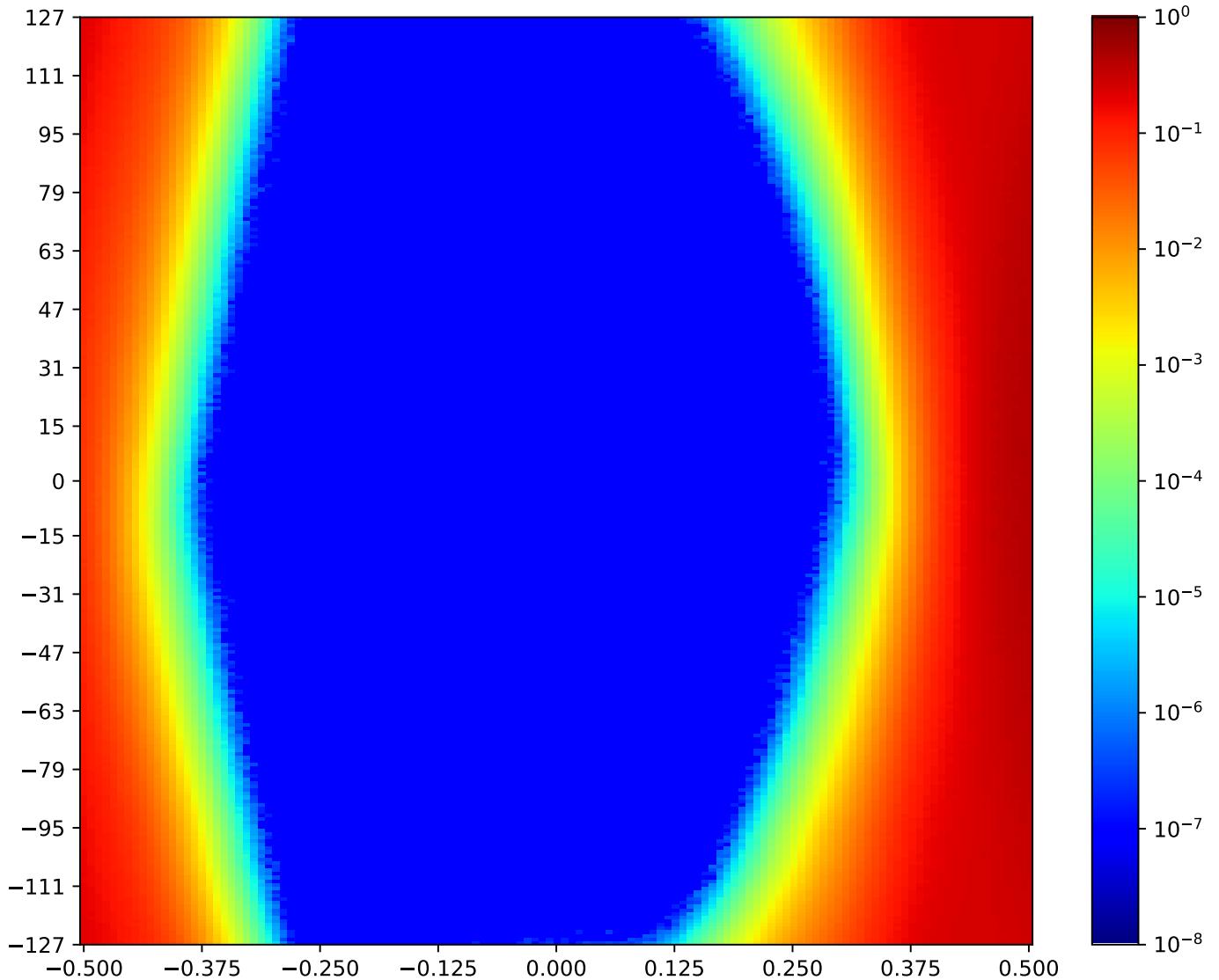


Figure 3.226: MSP\_C\_FPGA-TX3-11-RX2-11-MSP\_A\_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18 MSP\_C TX4 MSP\_A RX1 Minipod Loopback

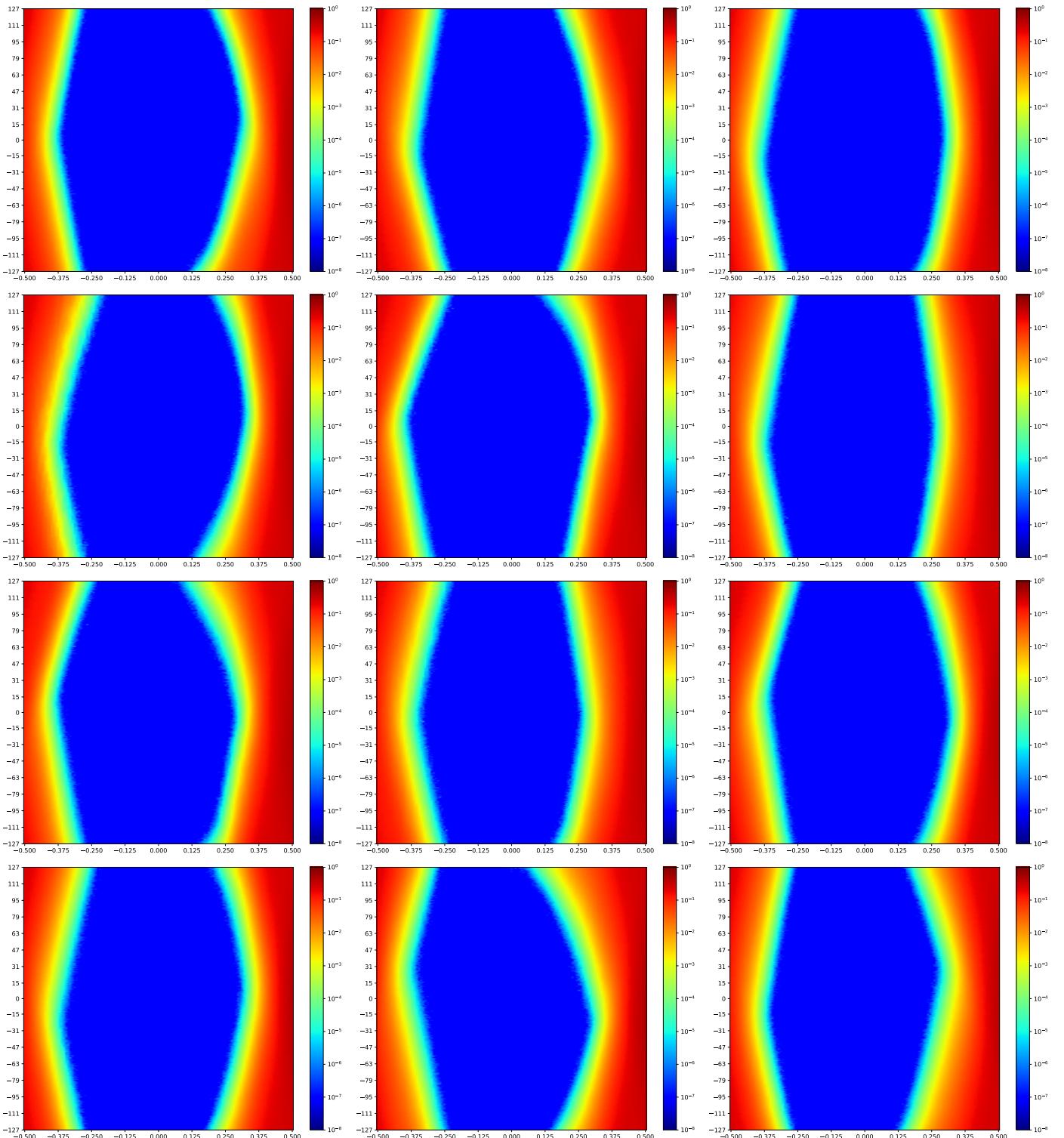


Figure 3.227: MSP\_C TX4 MSP\_A RX1 Minipod Loopback

A cross-reference to Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.240.

### 3.18.1 MSP\_C\_FPGA-TX4-00-RX1-00-MSP\_A\_FPGA

Table 3.210: MSP\_C\_FPGA-TX4-00-RX1-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:23:23		2018-Jan-24 01:24:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17729	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

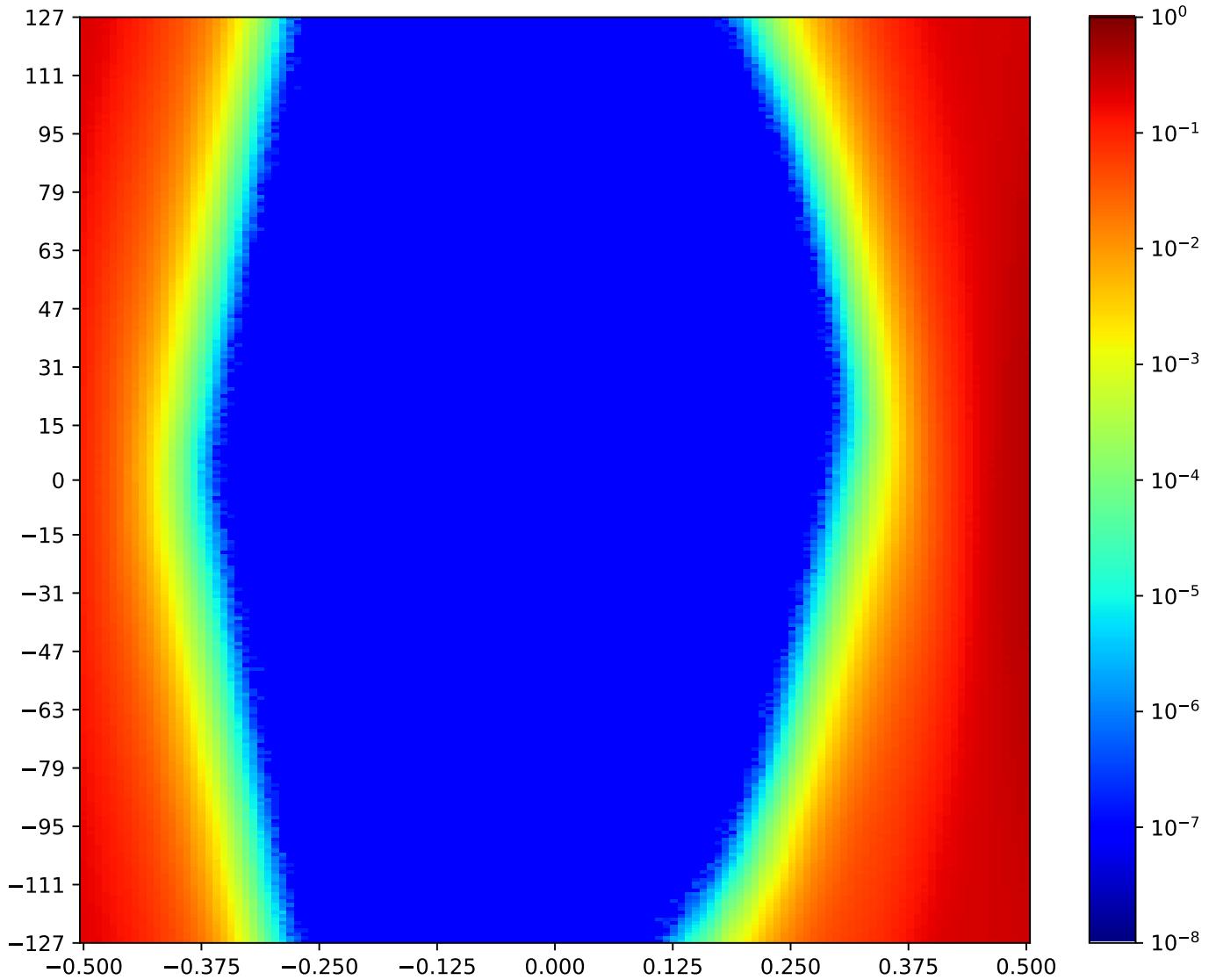


Figure 3.228: MSP\_C\_FPGA-TX4-00-RX1-00-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.2 MSP\_C\_FPGA-TX4-01-RX1-01-MSP\_A\_FPGA

Table 3.211: MSP\_C\_FPGA-TX4-01-RX1-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:21:57		2018-Jan-24 01:22:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16237	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

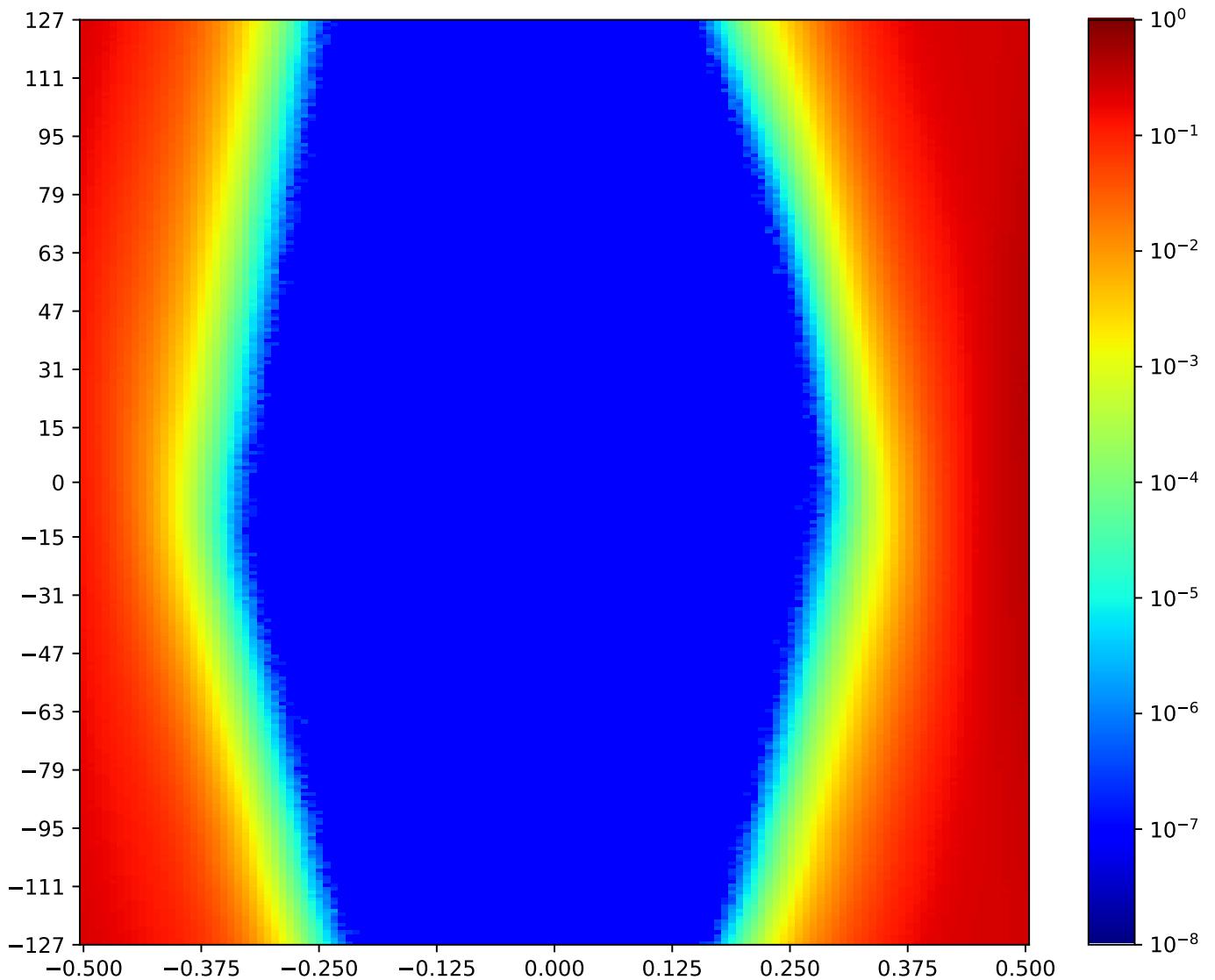


Figure 3.229: MSP\_C\_FPGA-TX4-01-RX1-01-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.3 MSP\_C\_FPGA-TX4-02-RX1-02-MSP\_A\_FPGA

Table 3.212: MSP\_C\_FPGA-TX4-02-RX1-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:25:30		2018-Jan-24 01:26:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17892	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

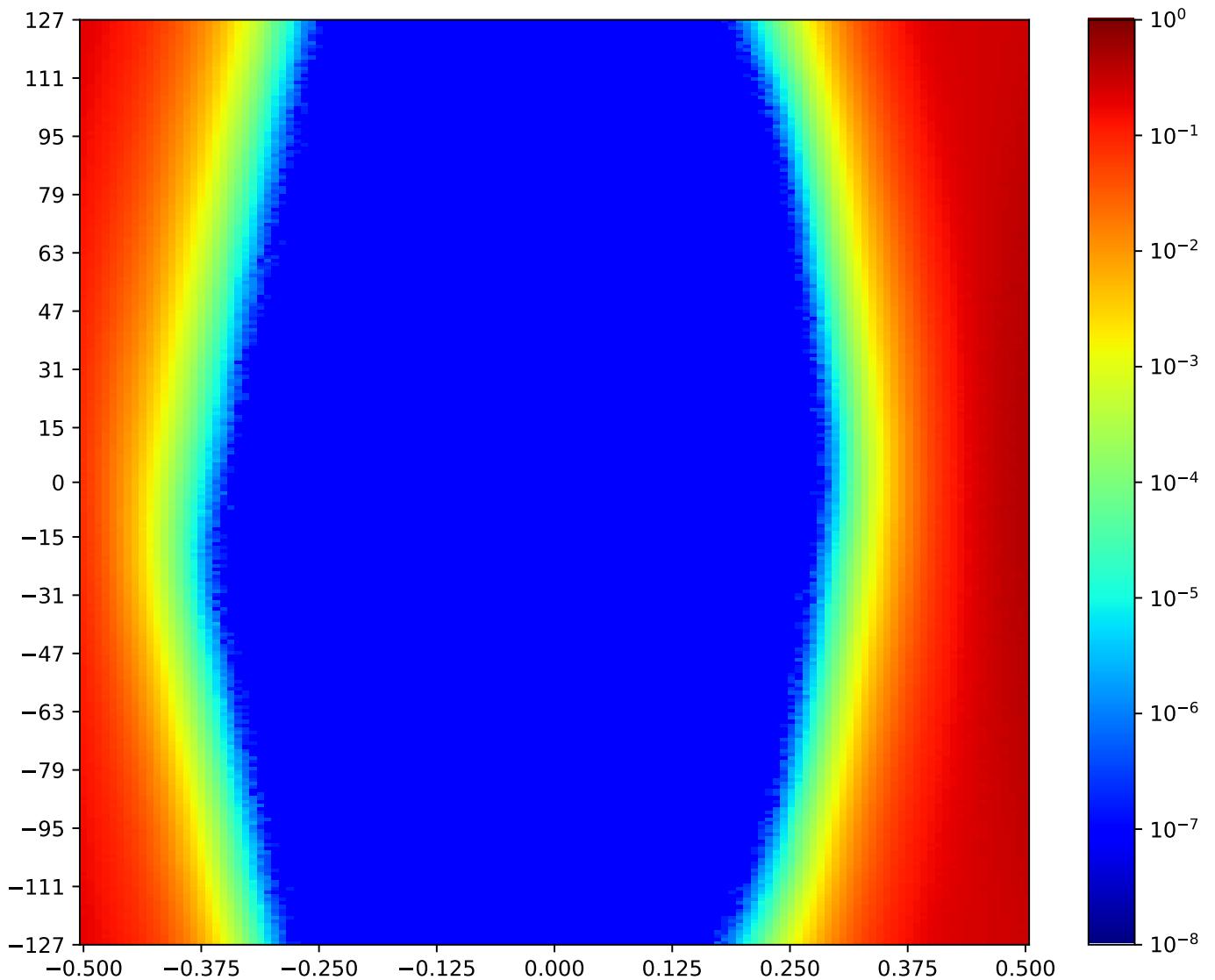


Figure 3.230: MSP\_C\_FPGA-TX4-02-RX1-02-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.4 MSP\_C\_FPGA-TX4-03-RX1-03-MSP\_A\_FPGA

Table 3.213: MSP\_C\_FPGA-TX4-03-RX1-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:21:15		2018-Jan-24 01:21:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17150	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

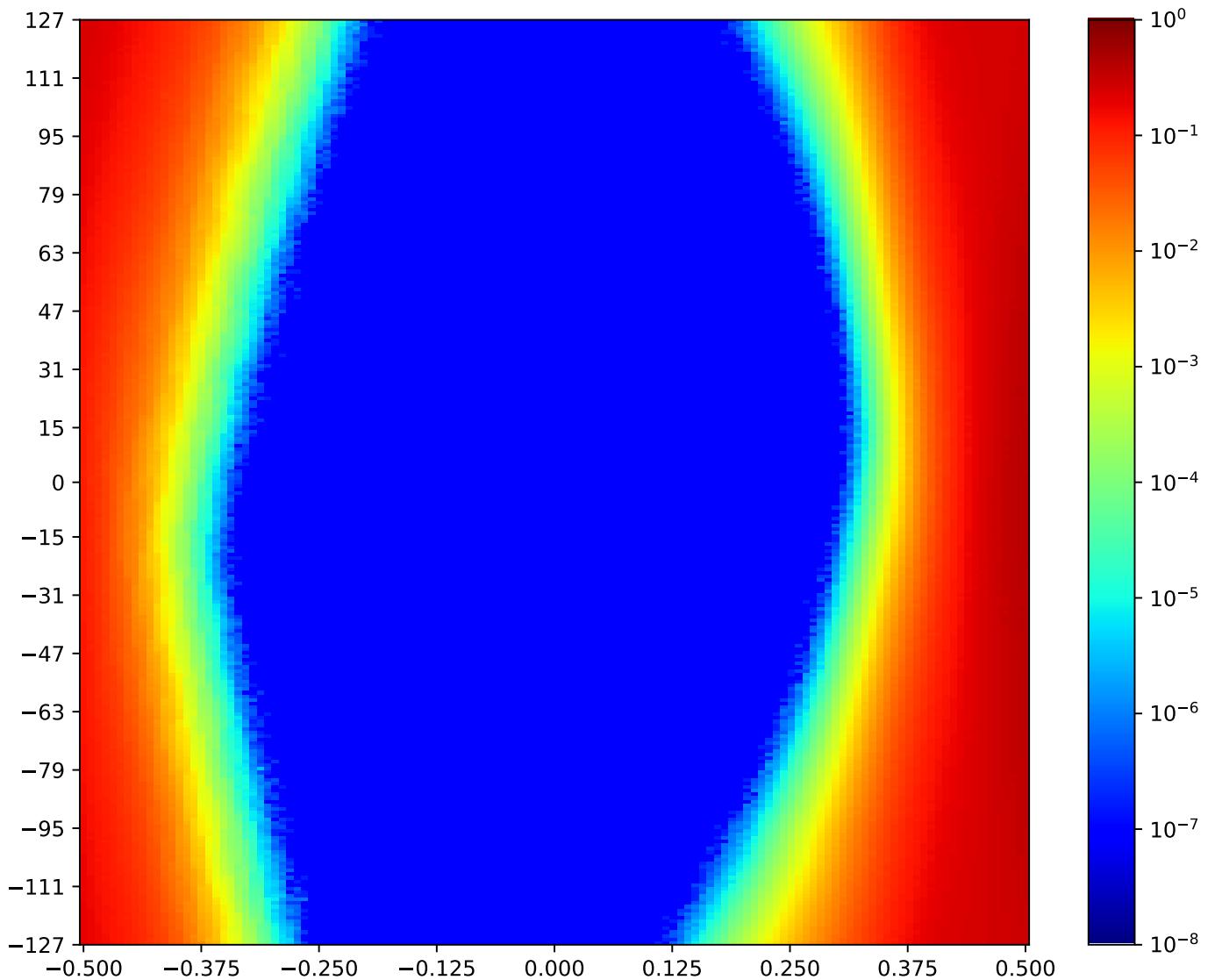


Figure 3.231: MSP\_C\_FPGA-TX4-03-RX1-03-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.5 MSP\_C\_FPGA-TX4-04-RX1-04-MSP\_A\_FPGA

Table 3.214: MSP\_C\_FPGA-TX4-04-RX1-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:27:37		2018-Jan-24 01:28:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17181	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

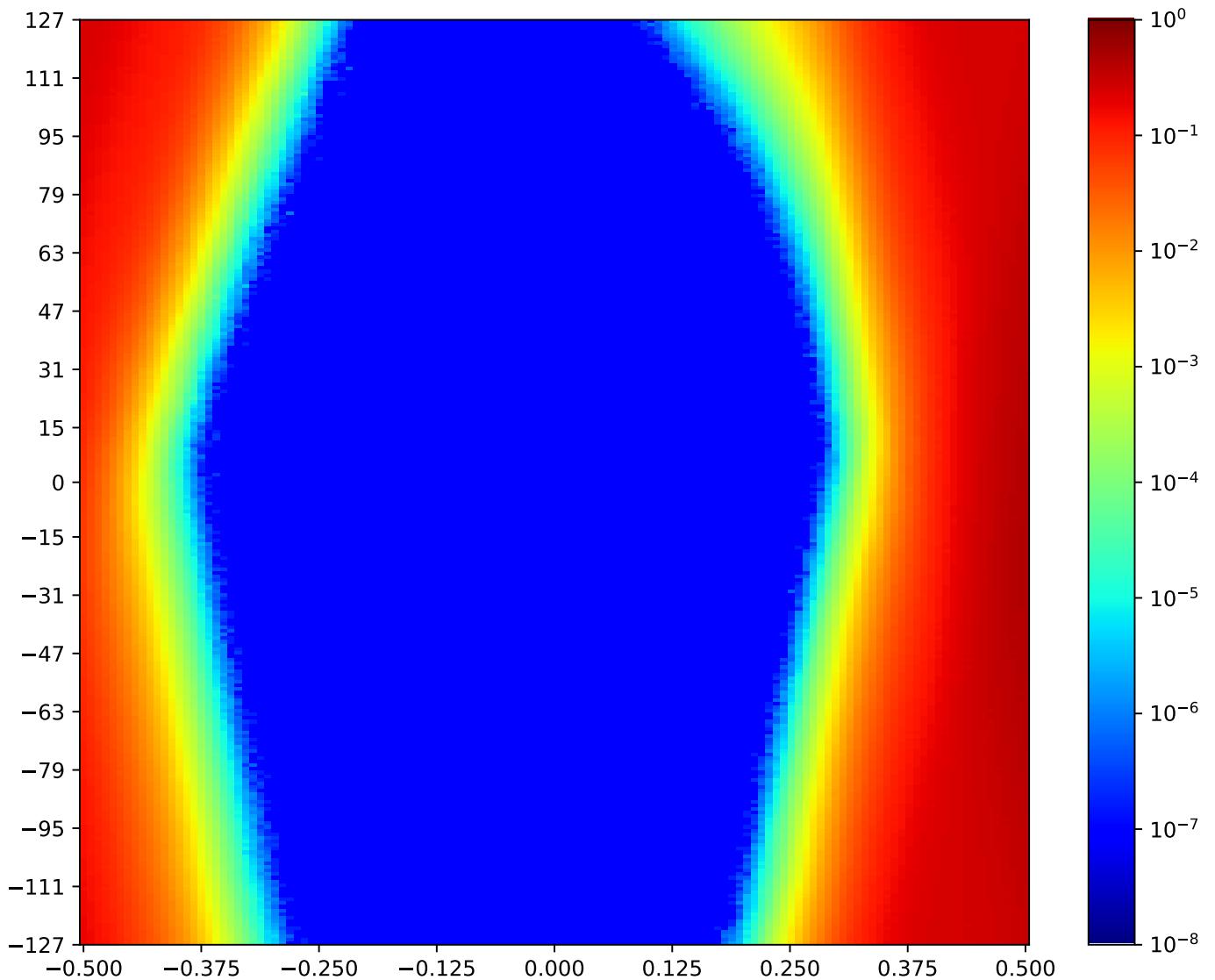


Figure 3.232: MSP\_C\_FPGA-TX4-04-RX1-04-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.6 MSP\_C\_FPGA-TX4-05-RX1-05-MSP\_A\_FPGA

Table 3.215: MSP\_C\_FPGA-TX4-05-RX1-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:22:40		2018-Jan-24 01:23:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16407	72	55.81%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

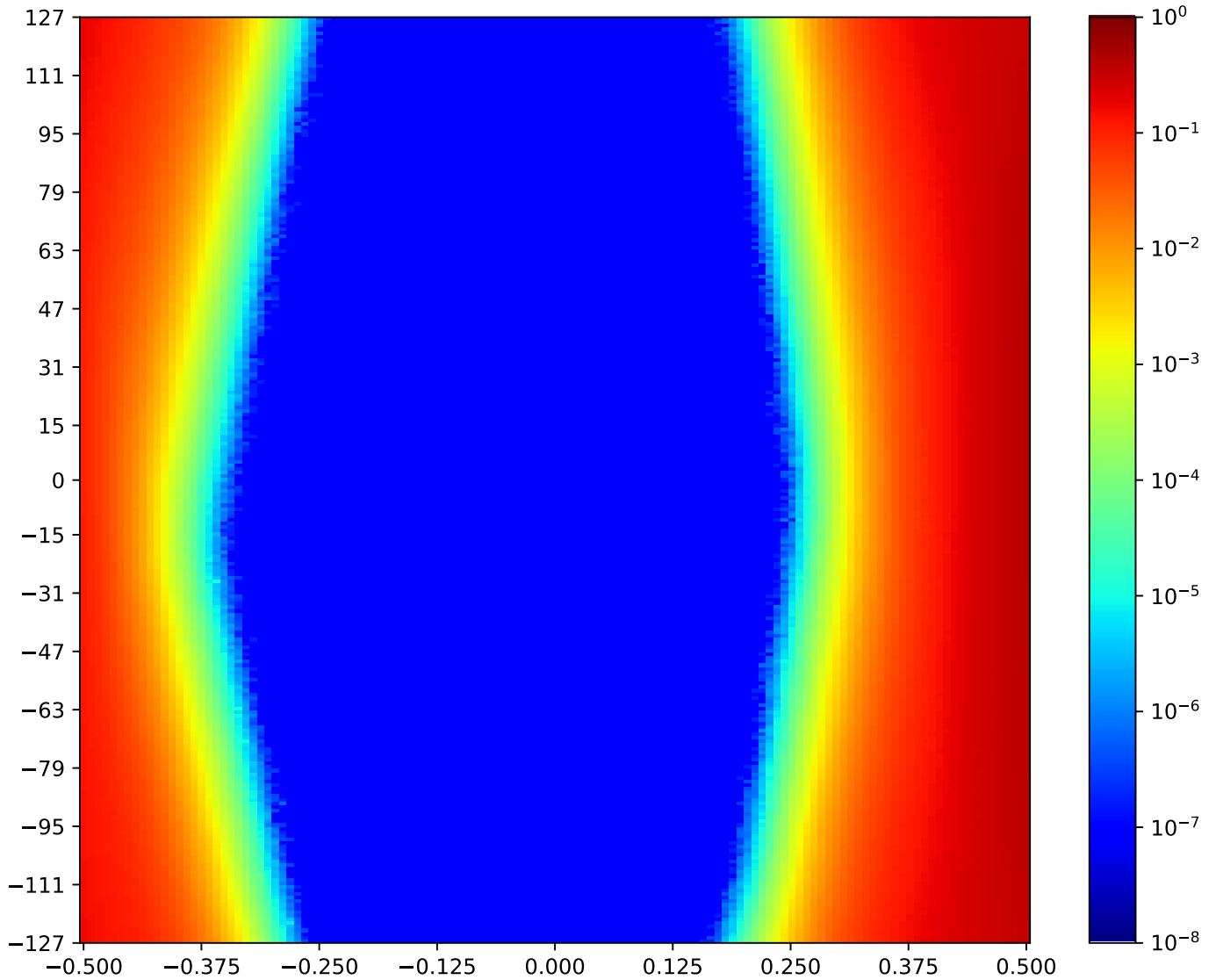


Figure 3.233: MSP\_C\_FPGA-TX4-05-RX1-05-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.7 MSP\_C\_FPGA-TX4-06-RX1-06-MSP\_A\_FPGA

Table 3.216: MSP\_C\_FPGA-TX4-06-RX1-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:29:02		2018-Jan-24 01:29:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16495	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

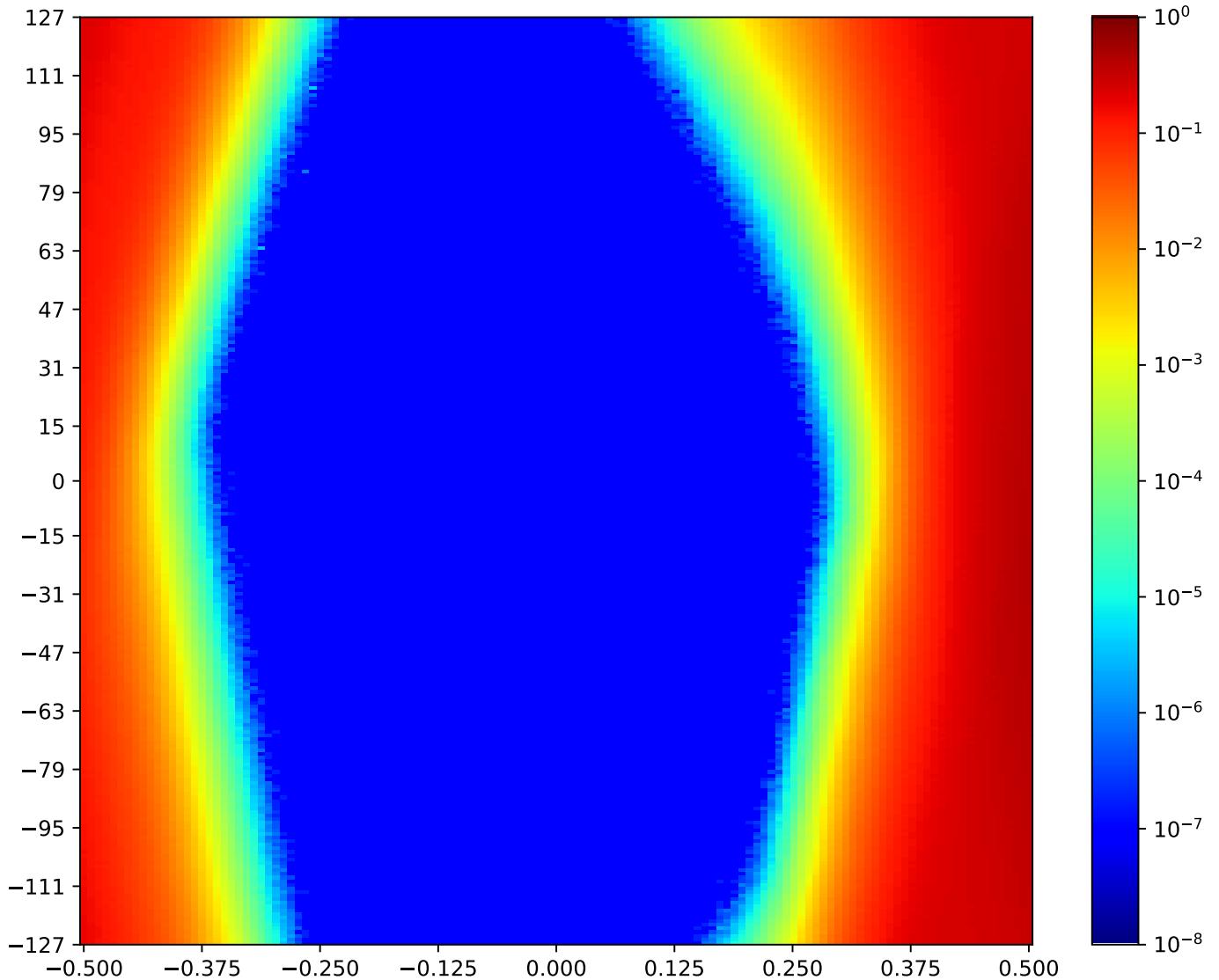


Figure 3.234: MSP\_C\_FPGA-TX4-06-RX1-06-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.8 MSP\_C\_FPGA-TX4-07-RX1-07-MSP\_A\_FPGA

Table 3.217: MSP\_C\_FPGA-TX4-07-RX1-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:24:05		2018-Jan-24 01:24:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15499	72	55.81%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

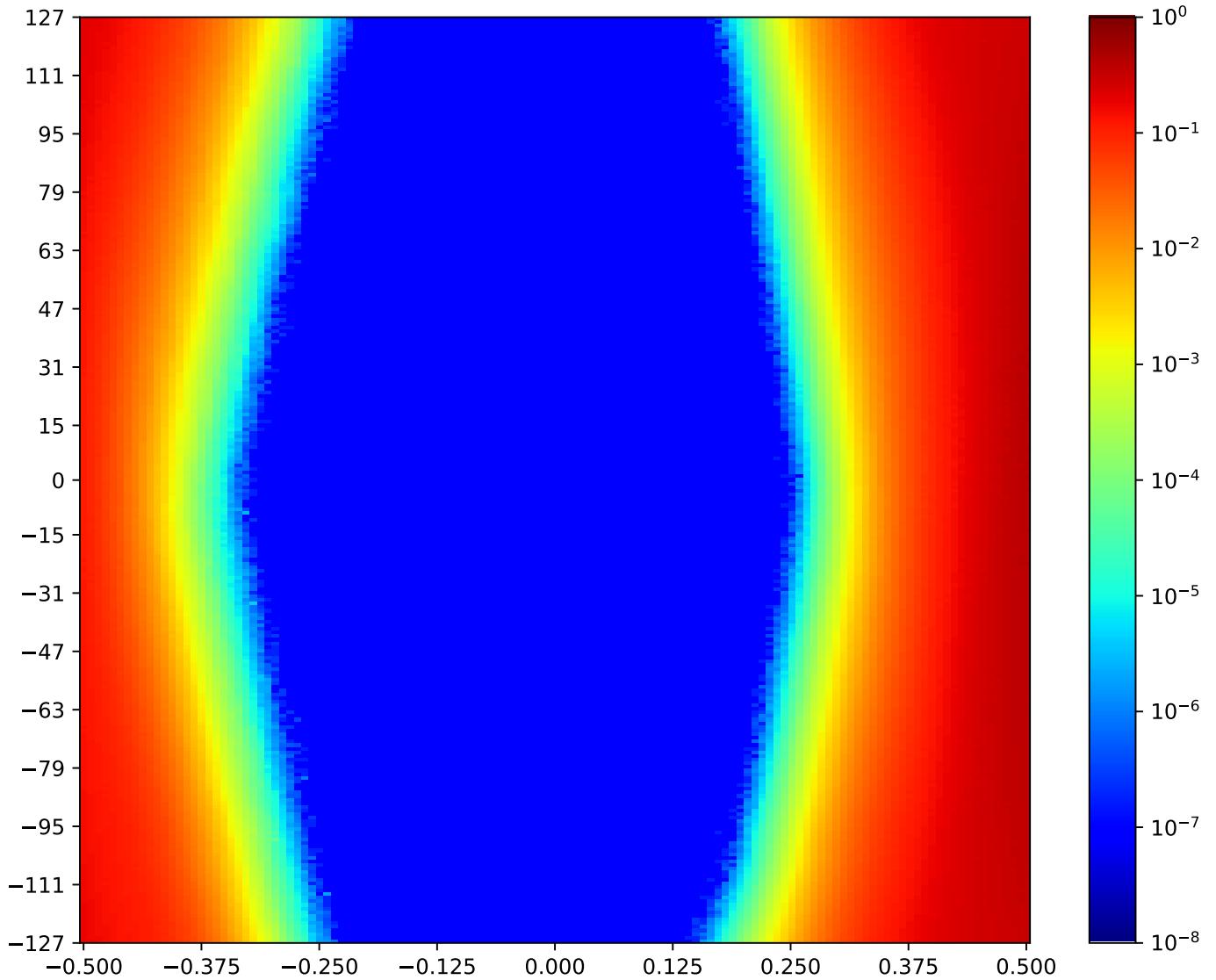


Figure 3.235: MSP\_C\_FPGA-TX4-07-RX1-07-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.9 MSP\_C\_FPGA-TX4-08-RX1-08-MSP\_A\_FPGA

Table 3.218: MSP\_C\_FPGA-TX4-08-RX1-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:28:19		2018-Jan-24 01:29:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17418	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

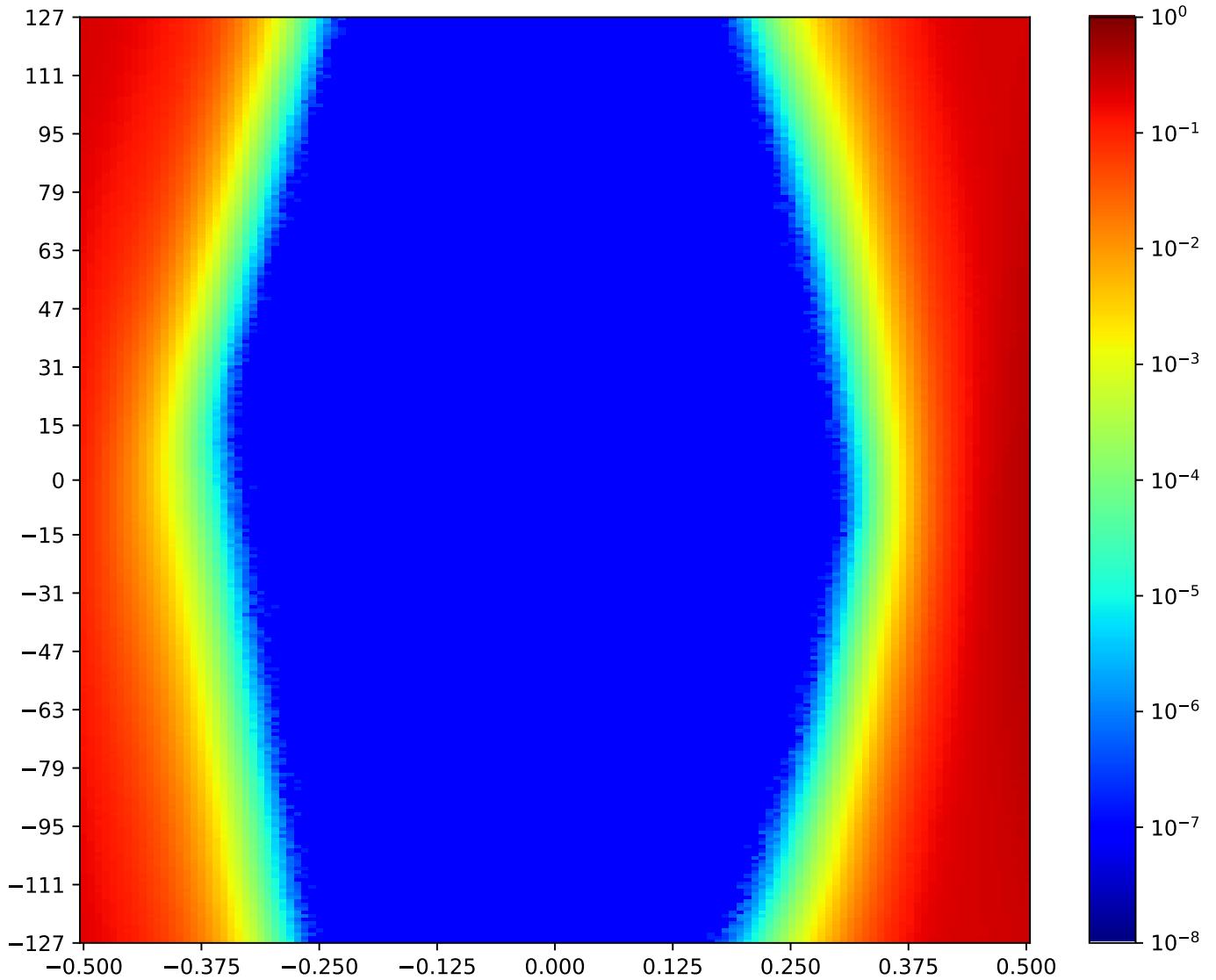


Figure 3.236: MSP\_C\_FPGA-TX4-08-RX1-08-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.10 MSP\_C\_FPGA-TX4-09-RX1-09-MSP\_A\_FPGA

Table 3.219: MSP\_C\_FPGA-TX4-09-RX1-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:24:48		2018-Jan-24 01:25:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17442	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

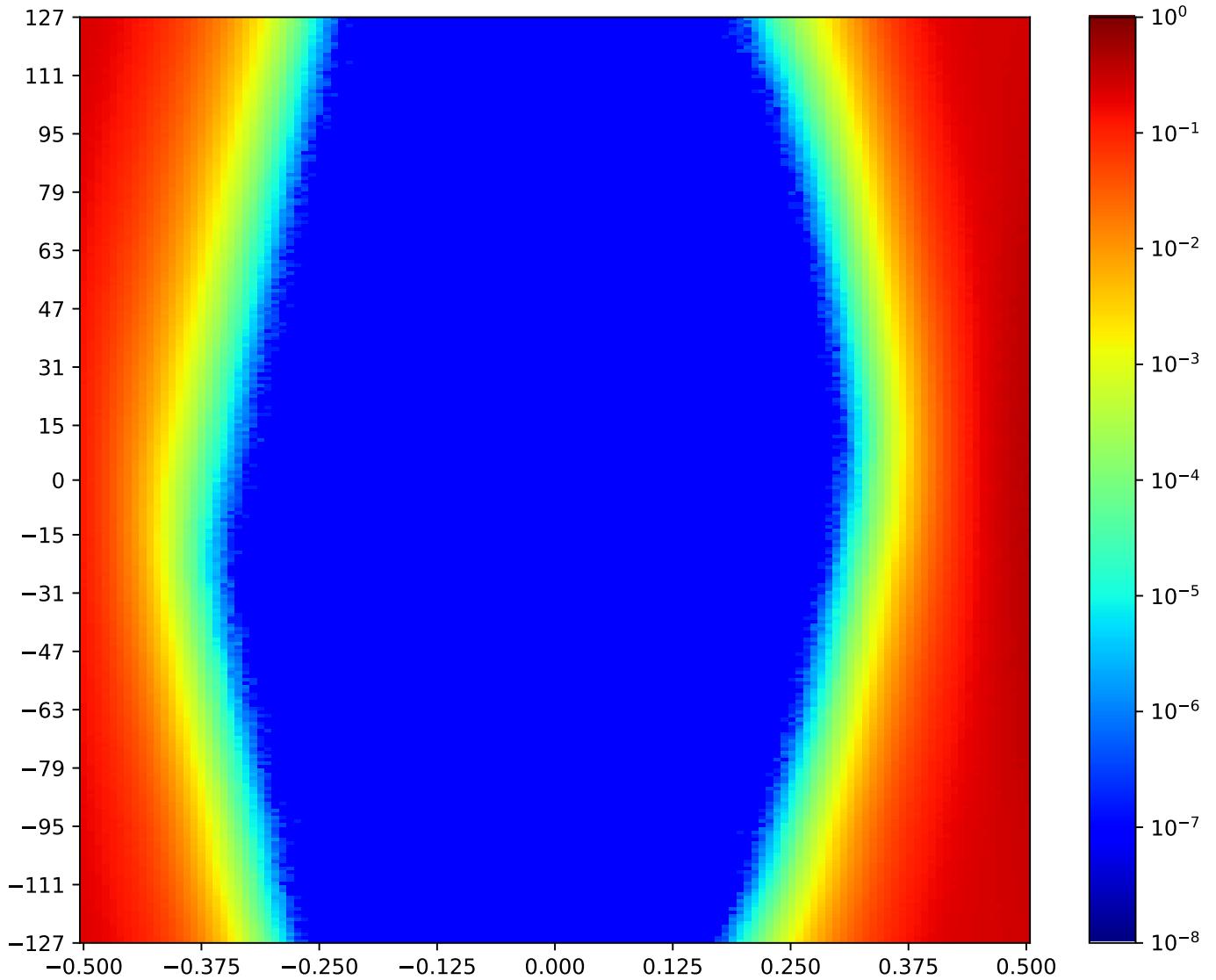


Figure 3.237: MSP\_C\_FPGA-TX4-09-RX1-09-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.11 MSP\_C\_FPGA-TX4-10-RX1-10-MSP\_A\_FPGA

Table 3.220: MSP\_C\_FPGA-TX4-10-RX1-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:26:55		2018-Jan-24 01:27:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15751	74	55.81%	250	98.04%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

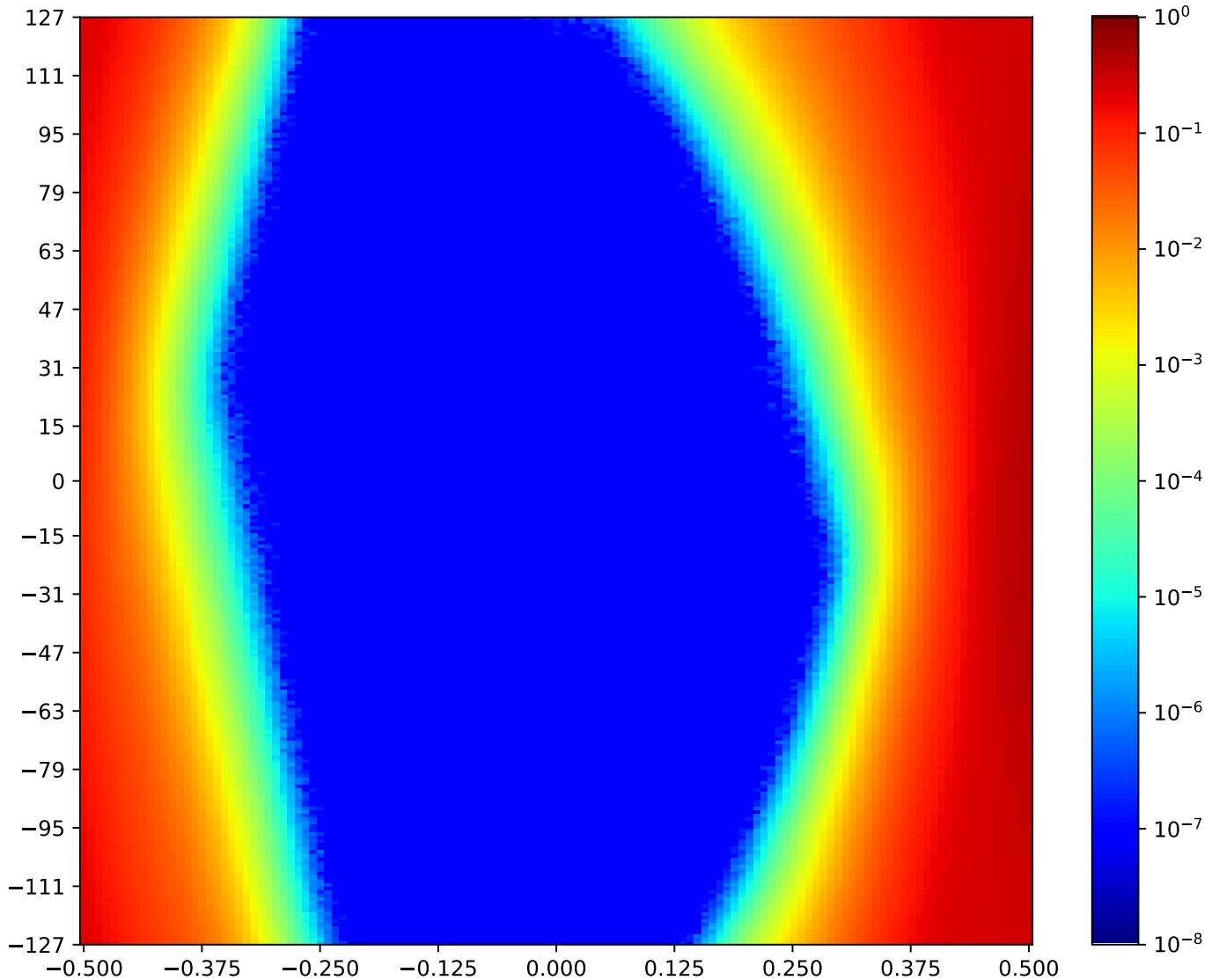


Figure 3.238: MSP\_C\_FPGA-TX4-10-RX1-10-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.18.12 MSP\_C\_FPGA-TX4-11-RX1-11-MSP\_A\_FPGA

Table 3.221: MSP\_C\_FPGA-TX4-11-RX1-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:26:12		2018-Jan-24 01:26:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16183	72	55.81%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

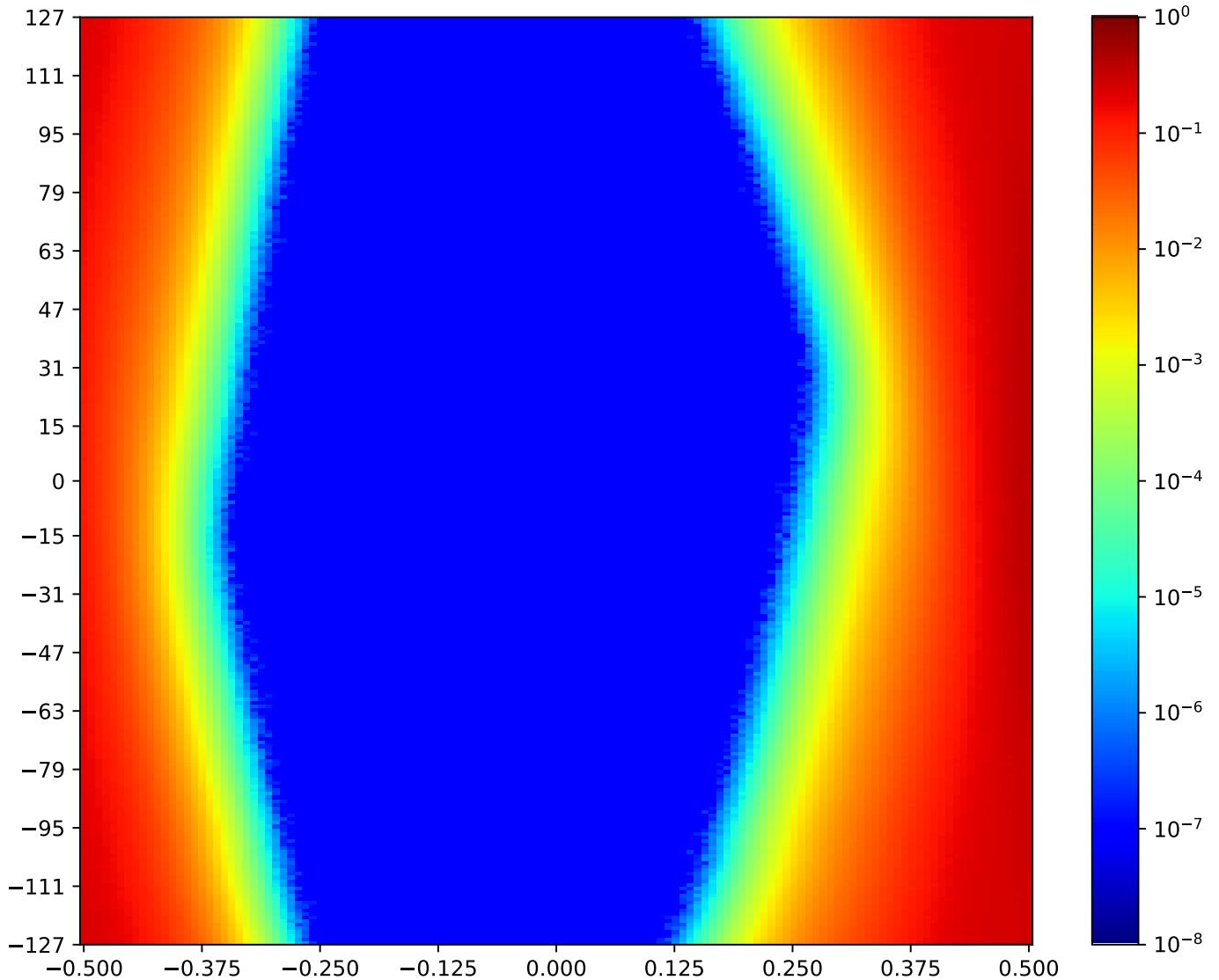


Figure 3.239: MSP\_C\_FPGA-TX4-11-RX1-11-MSP\_A\_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19 MSP\_A TX1 MSP\_C RX13 Minipod Loopback

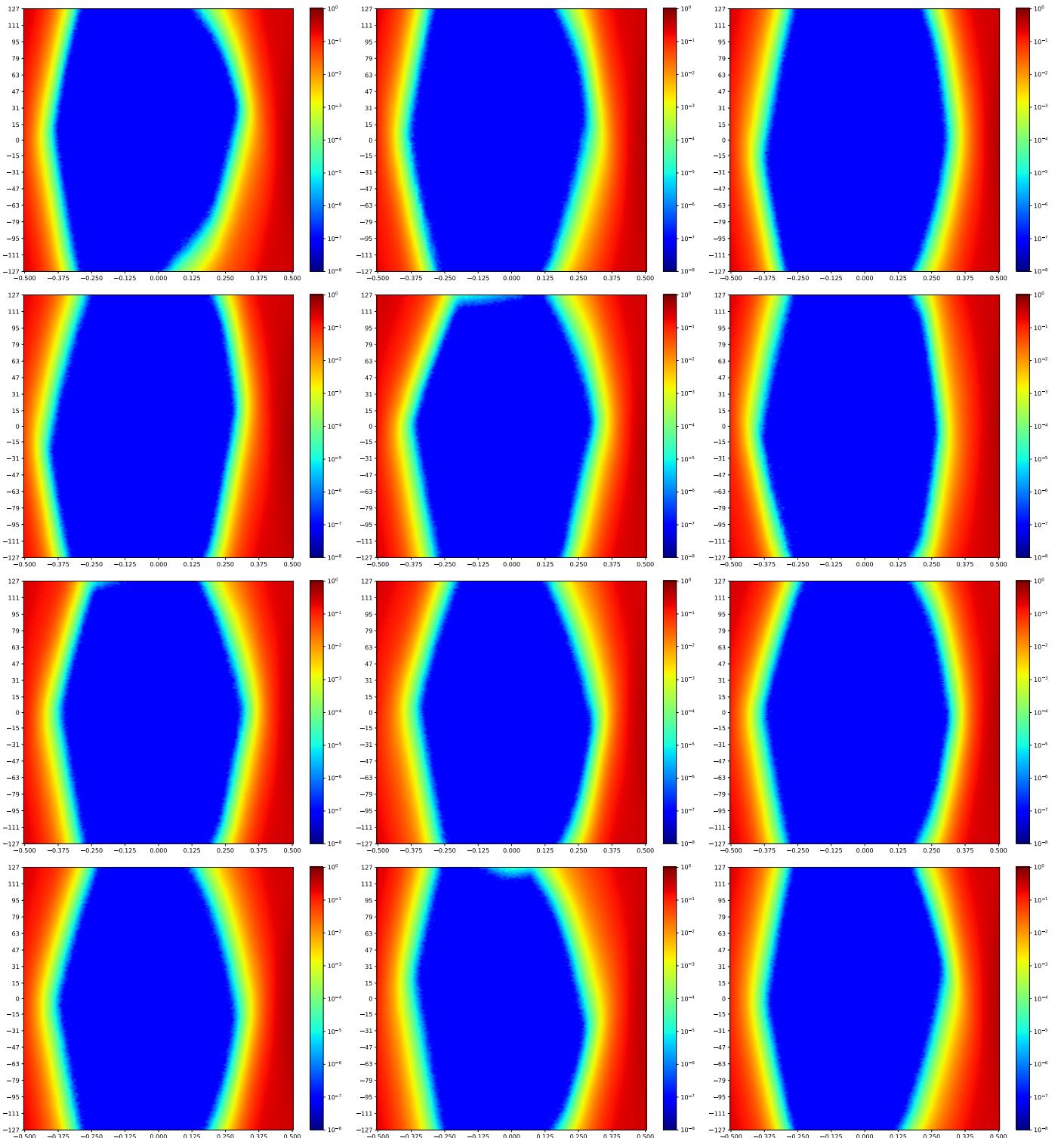


Figure 3.240: MSP\_A TX1 MSP\_C RX13 Minipod Loopback

A cross-reference to Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.253.

### 3.19.1 MSP\_A\_FPGA-TX1-00-RX13-00-MSP\_C\_FPGA

Table 3.222: MSP\_A\_FPGA-TX1-00-RX13-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:39:55		2018-Jan-24 01:40:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17182	81	62.79%	252	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

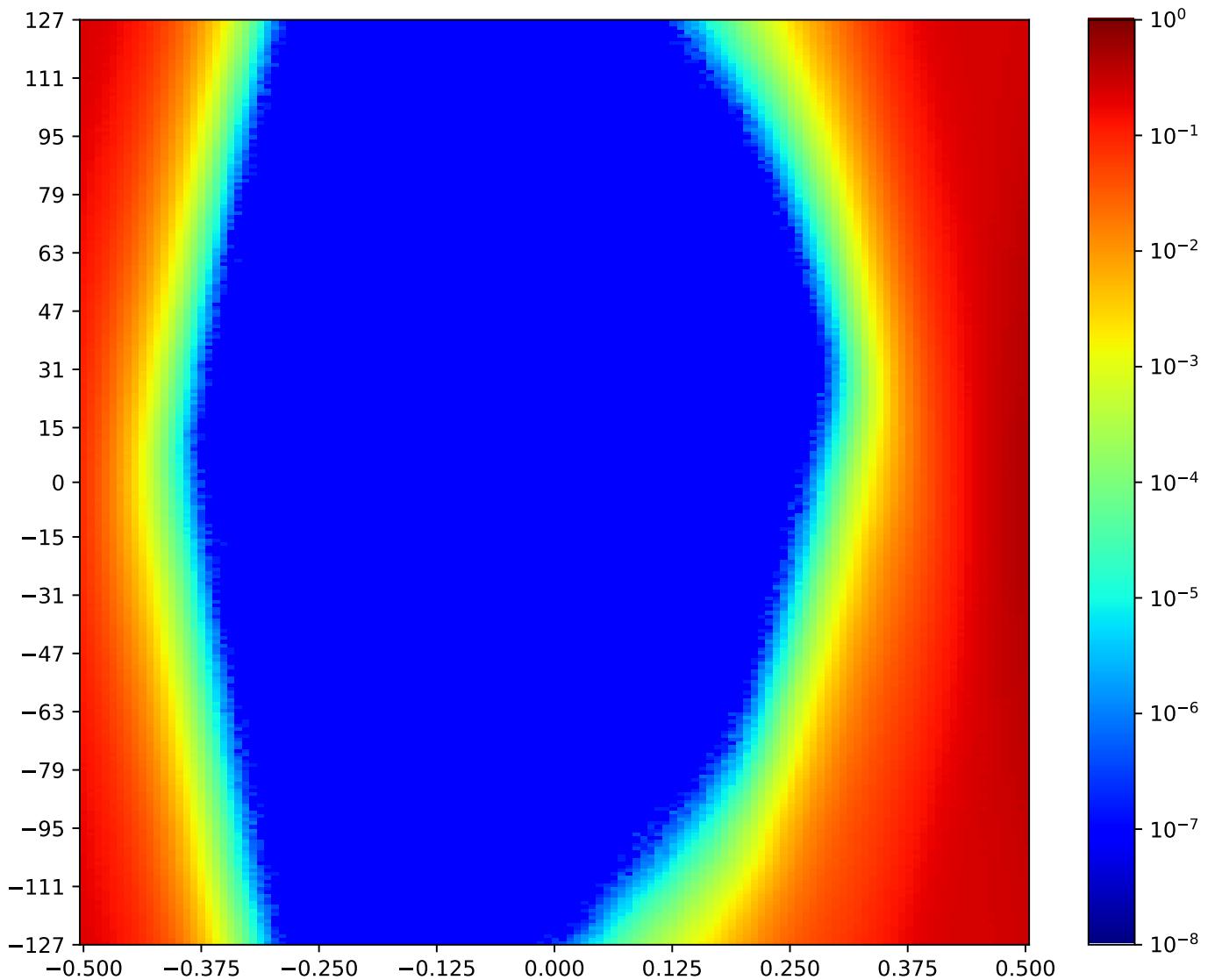


Figure 3.241: MSP\_A\_FPGA-TX1-00-RX13-00-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.2 MSP\_A\_FPGA-TX1-01-RX13-01-MSP\_C\_FPGA

Table 3.223: MSP\_A\_FPGA-TX1-01-RX13-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:41:19		2018-Jan-24 01:42:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16992	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

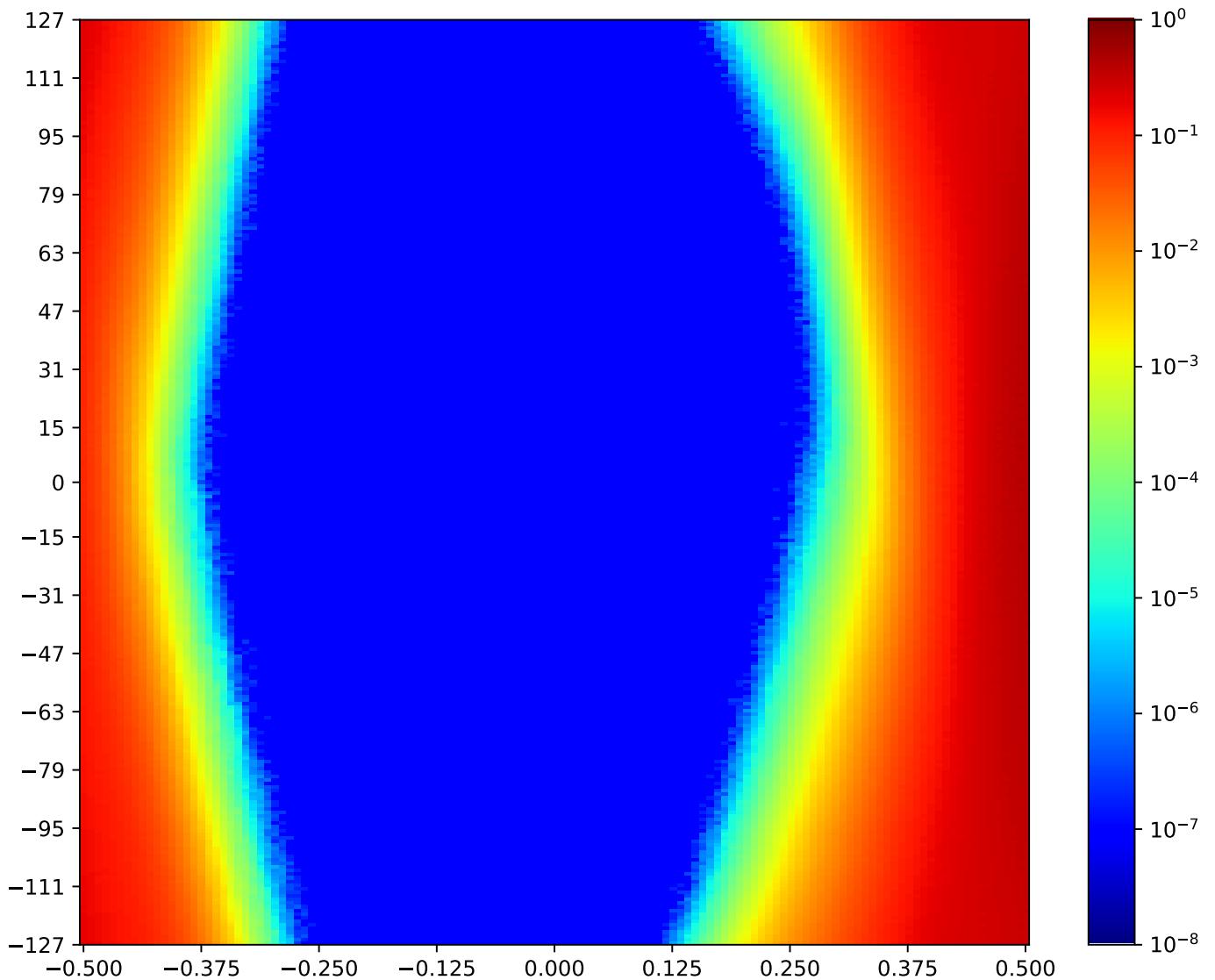


Figure 3.242: MSP\_A\_FPGA-TX1-01-RX13-01-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.3 MSP\_A\_FPGA-TX1-02-RX13-02-MSP\_C\_FPGA

Table 3.224: MSP\_A\_FPGA-TX1-02-RX13-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:42:00		2018-Jan-24 01:42:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18291	84	65.12%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

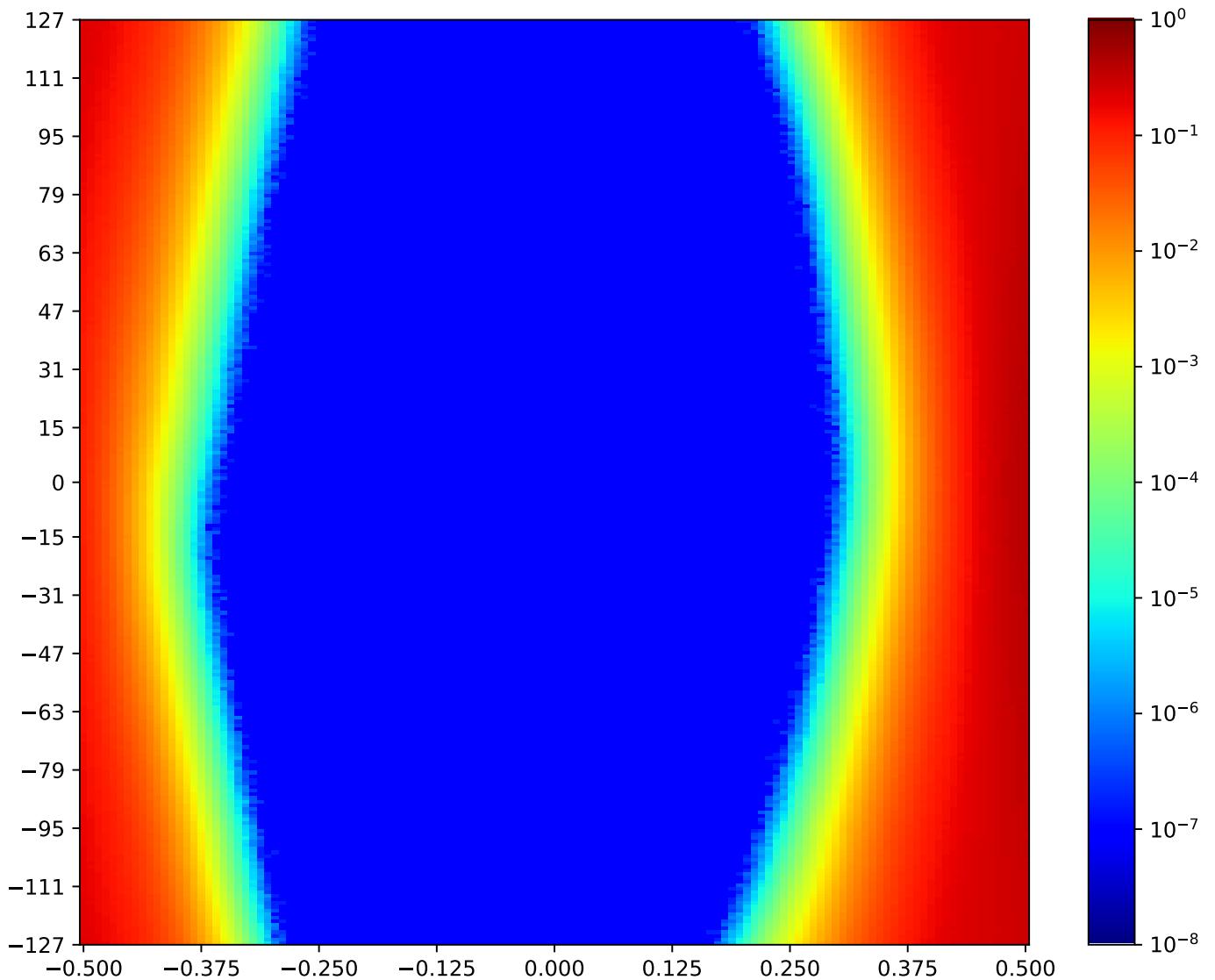


Figure 3.243: MSP\_A\_FPGA-TX1-02-RX13-02-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.4 MSP\_A\_FPGA-TX1-03-RX13-03-MSP\_C\_FPGA

Table 3.225: MSP\_A\_FPGA-TX1-03-RX13-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:38:32		2018-Jan-24 01:39:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18521	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

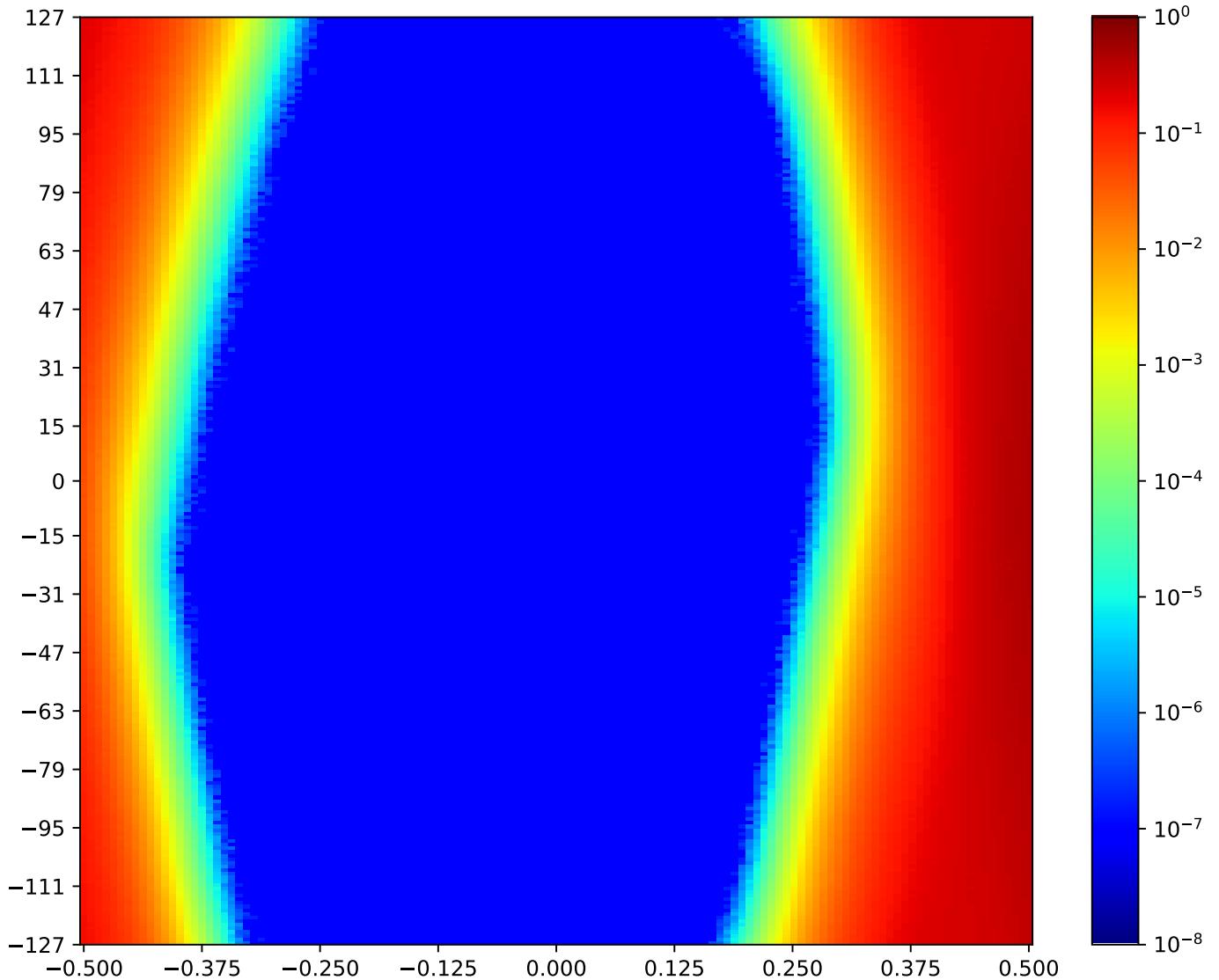


Figure 3.244: MSP\_A\_FPGA-TX1-03-RX13-03-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.5 MSP\_A\_FPGA-TX1-04-RX13-04-MSP\_C\_FPGA

Table 3.226: MSP\_A\_FPGA-TX1-04-RX13-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:44:05		2018-Jan-24 01:44:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16172	80	62.02%	249	96.86%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

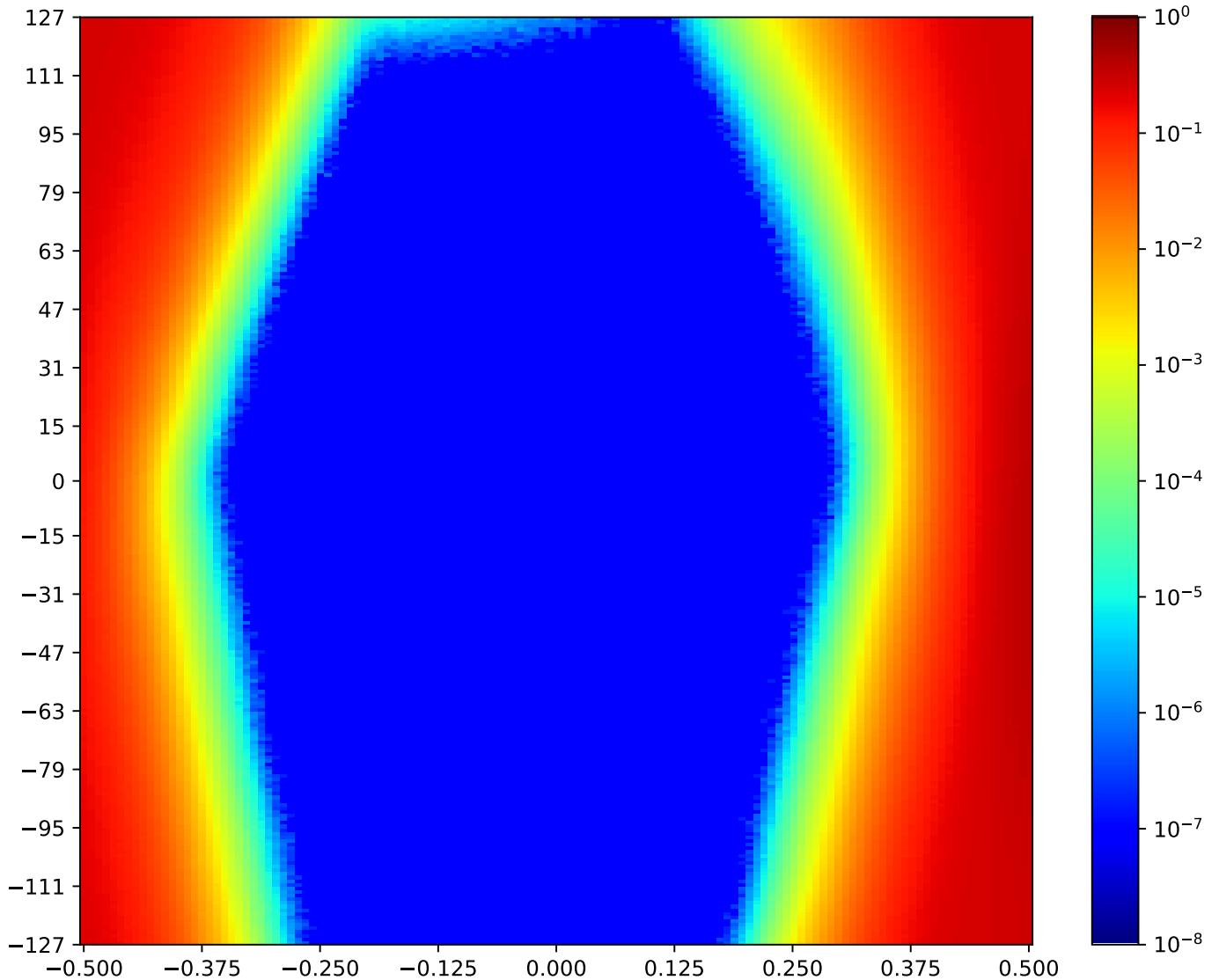


Figure 3.245: MSP\_A\_FPGA-TX1-04-RX13-04-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.6 MSP\_A\_FPGA-TX1-05-RX13-05-MSP\_C\_FPGA

Table 3.227: MSP\_A\_FPGA-TX1-05-RX13-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:37:50		2018-Jan-24 01:38:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17474	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

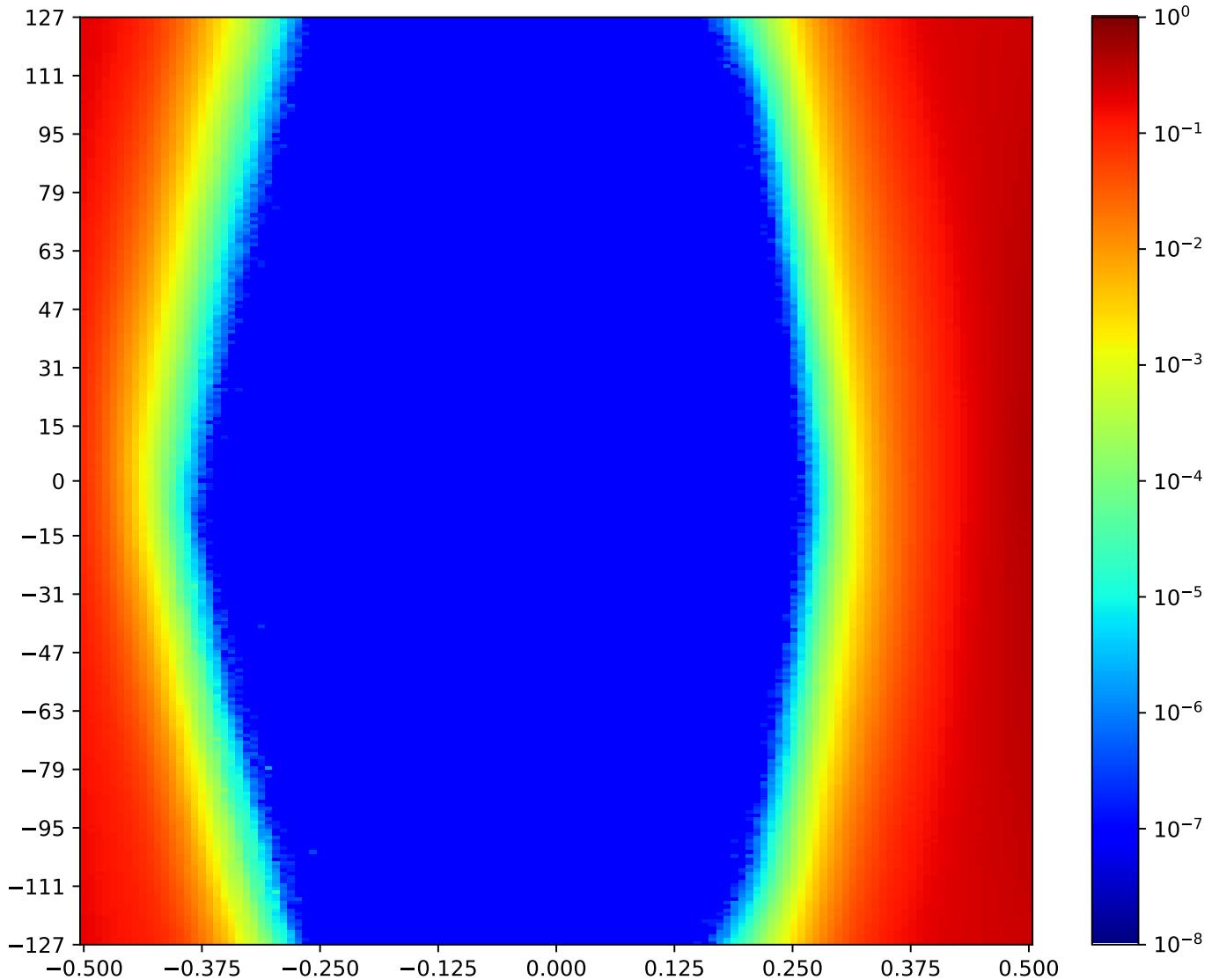


Figure 3.246: MSP\_A\_FPGA-TX1-05-RX13-05-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.7 MSP\_A\_FPGA-TX1-06-RX13-06-MSP\_C\_FPGA

Table 3.228: MSP\_A\_FPGA-TX1-06-RX13-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:45:28		2018-Jan-24 01:46:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17401	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

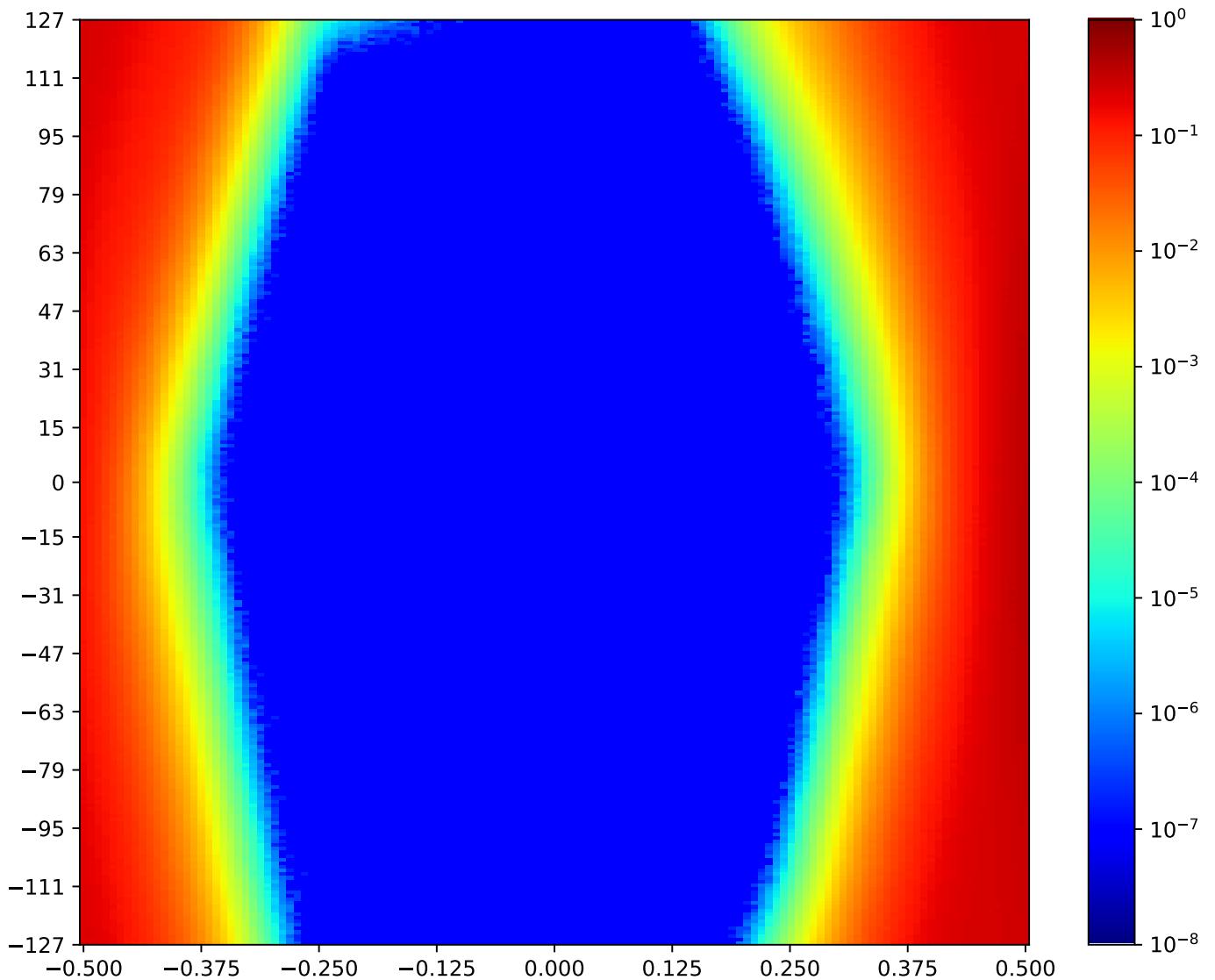


Figure 3.247: MSP\_A\_FPGA-TX1-06-RX13-06-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.8 MSP\_A\_FPGA-TX1-07-RX13-07-MSP\_C\_FPGA

Table 3.229: MSP\_A\_FPGA-TX1-07-RX13-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:39:14		2018-Jan-24 01:39:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16071	78	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

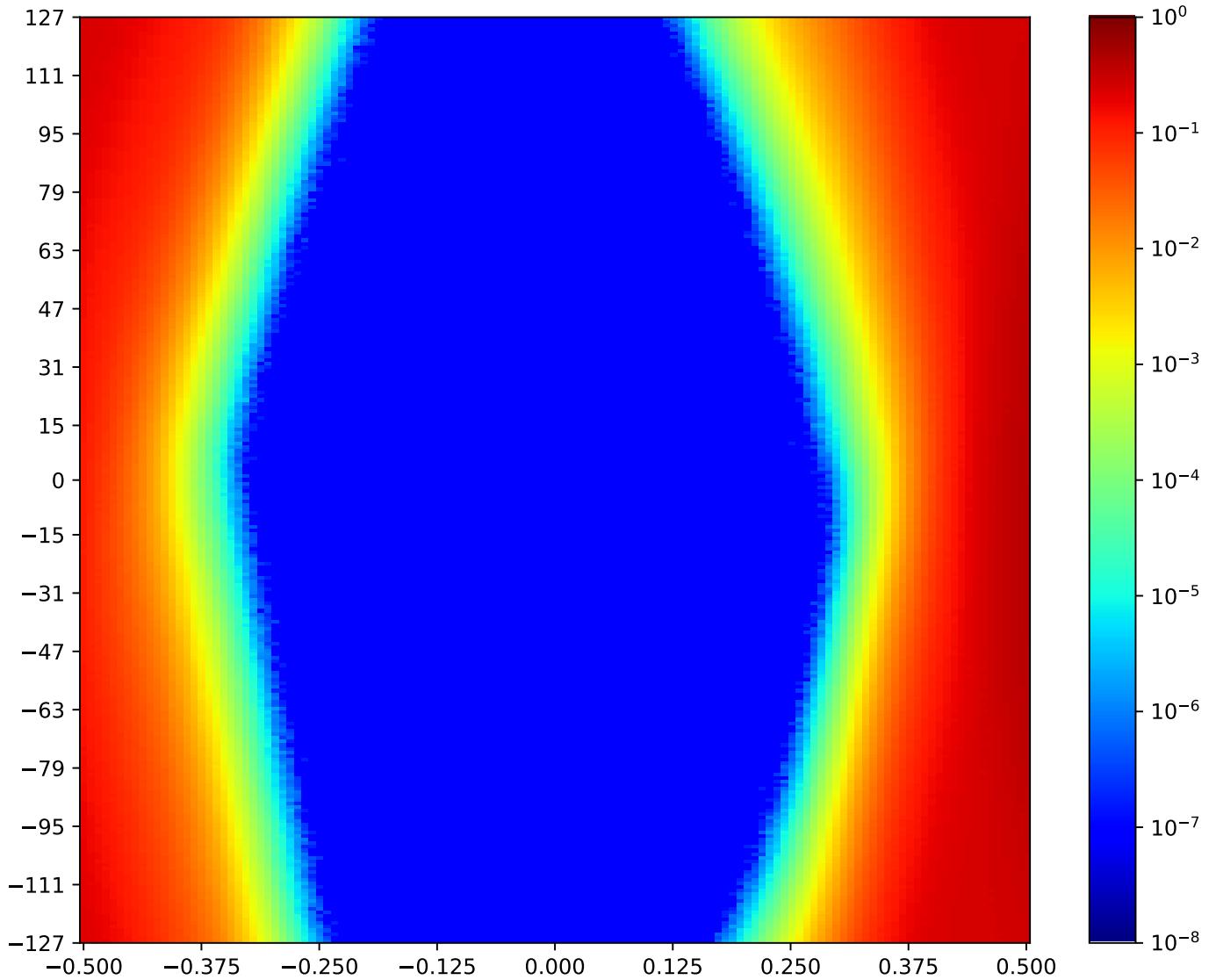


Figure 3.248: MSP\_A\_FPGA-TX1-07-RX13-07-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.9 MSP\_A\_FPGA-TX1-08-RX13-08-MSP\_C\_FPGA

Table 3.230: MSP\_A\_FPGA-TX1-08-RX13-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:44:46		2018-Jan-24 01:45:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17977	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

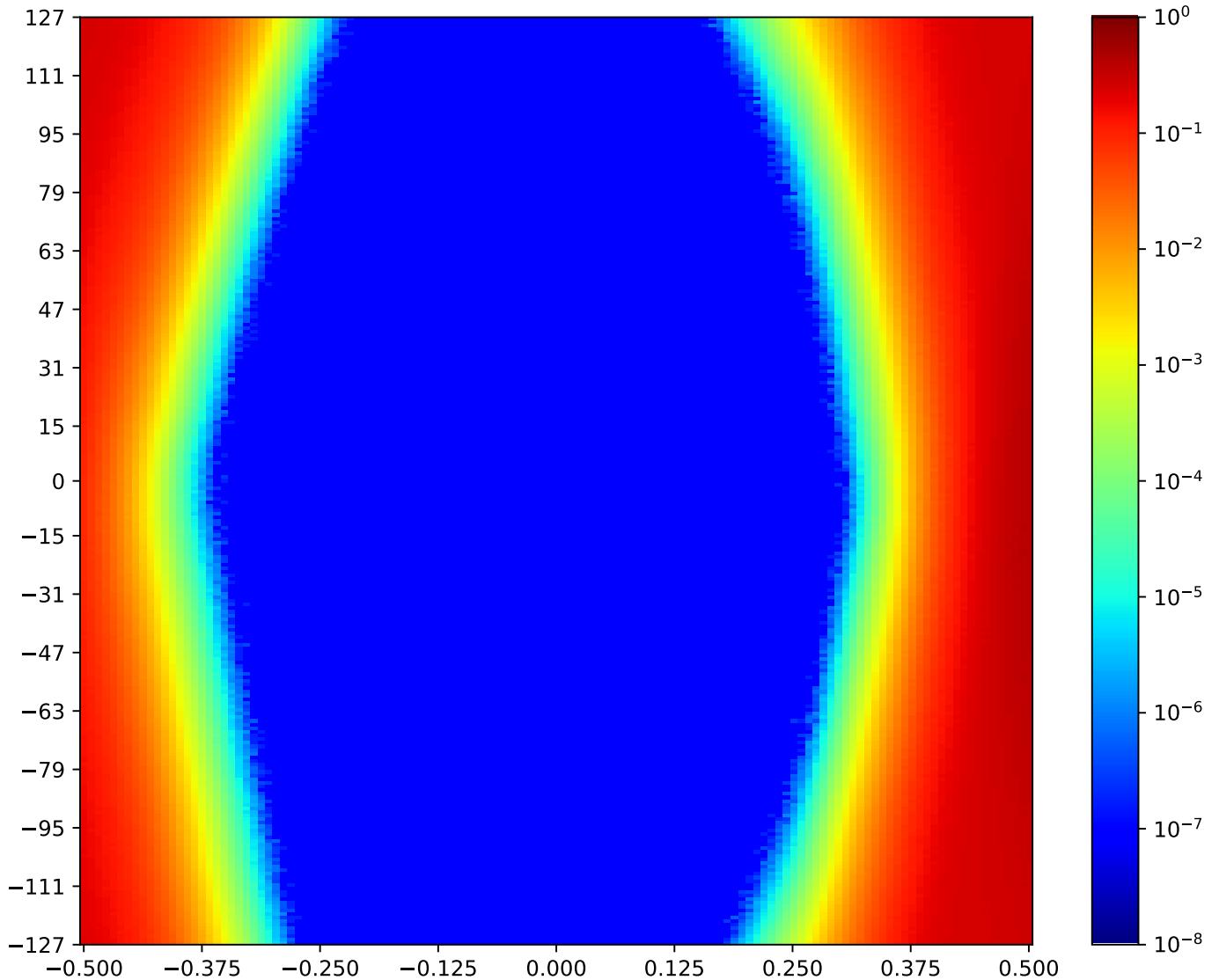


Figure 3.249: MSP\_A\_FPGA-TX1-08-RX13-08-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.10 MSP\_A\_FPGA-TX1-09-RX13-09-MSP\_C\_FPGA

Table 3.231: MSP\_A\_FPGA-TX1-09-RX13-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:40:37		2018-Jan-24 01:41:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16842	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

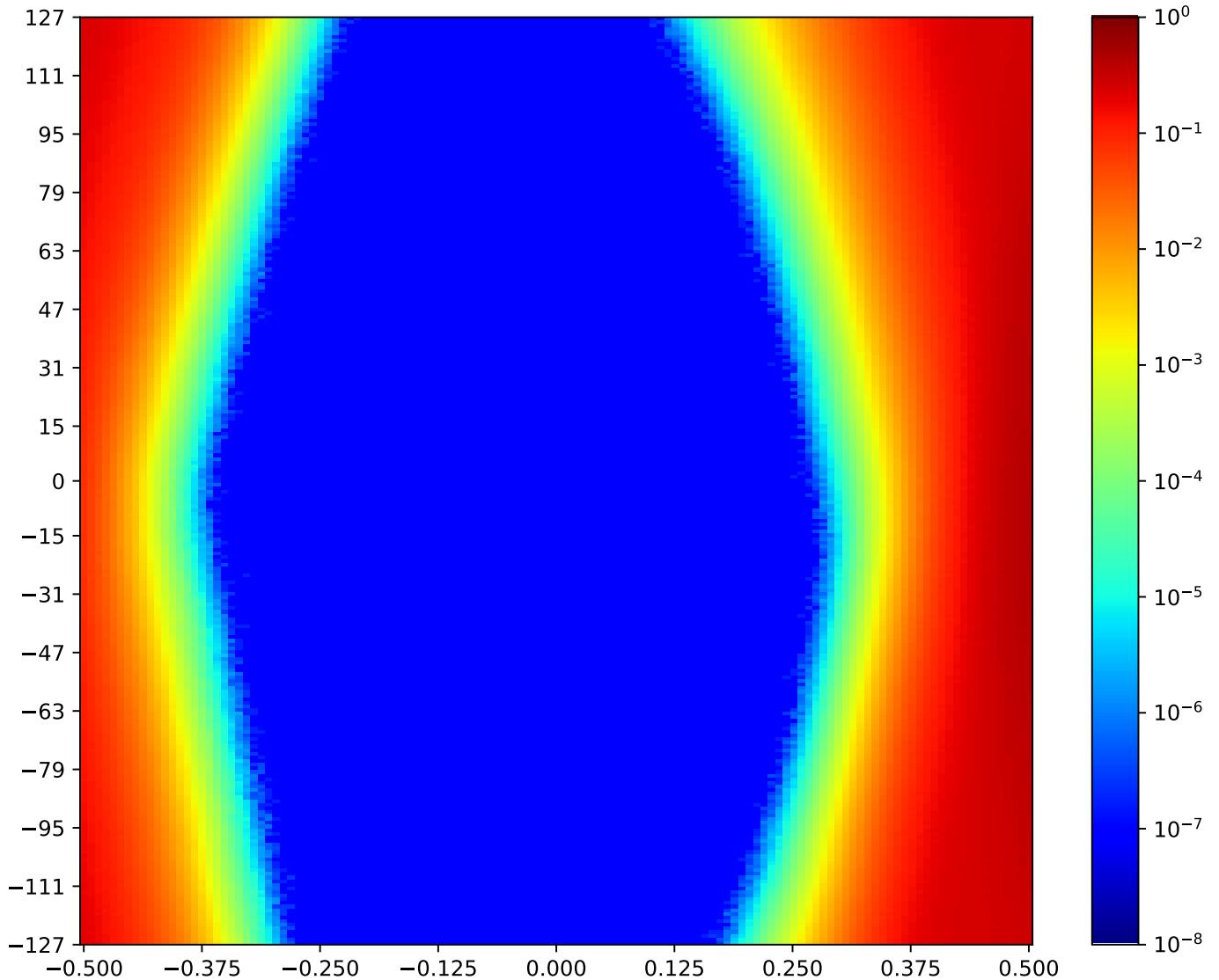


Figure 3.250: MSP\_A\_FPGA-TX1-09-RX13-09-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.11 MSP\_A\_FPGA-TX1-10-RX13-10-MSP\_C\_FPGA

Table 3.232: MSP\_A\_FPGA-TX1-10-RX13-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:43:23		2018-Jan-24 01:44:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15461	73	56.59%	242	94.51%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

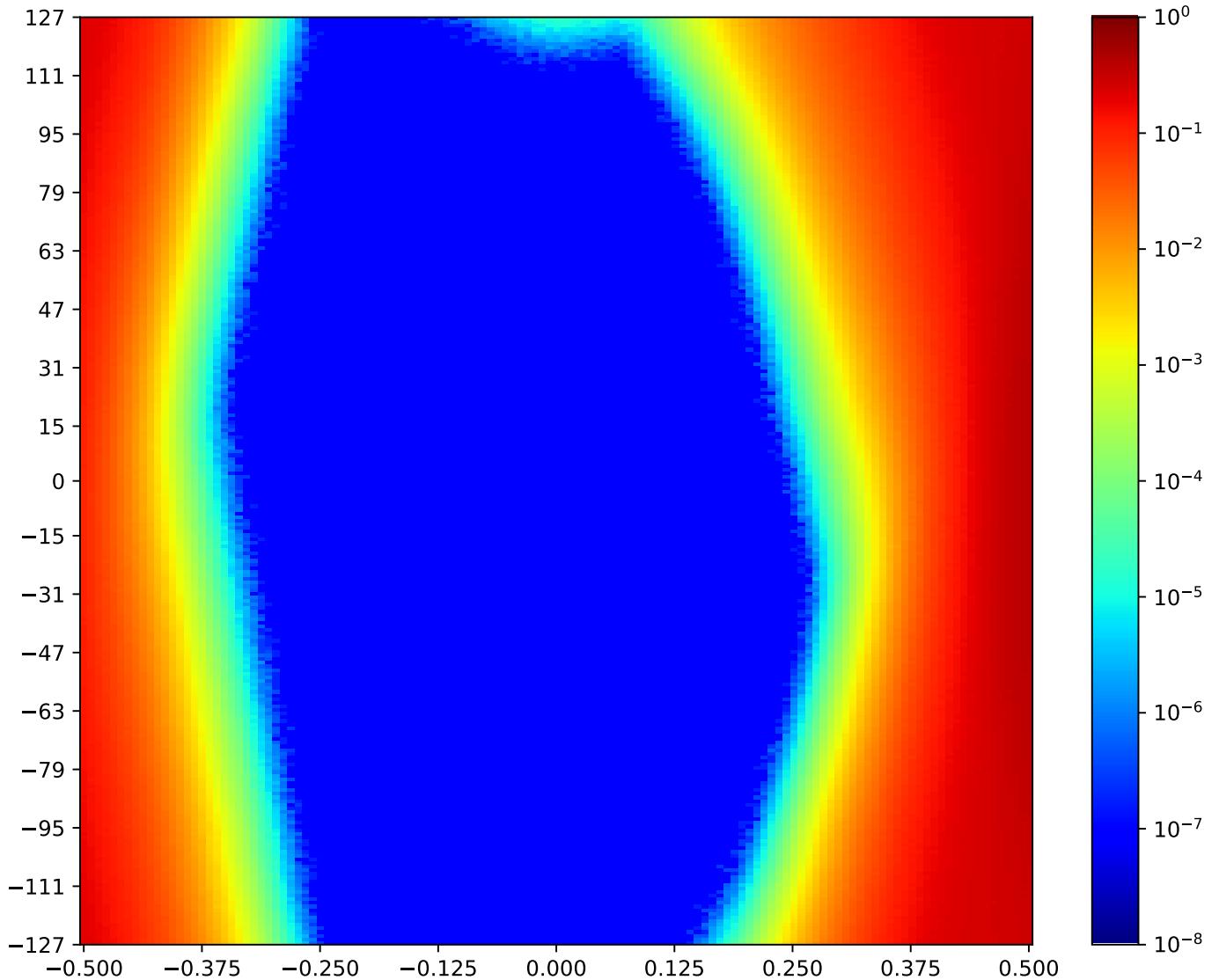


Figure 3.251: MSP\_A\_FPGA-TX1-10-RX13-10-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.19.12 MSP\_A\_FPGA-TX1-11-RX13-11-MSP\_C\_FPGA

Table 3.233: MSP\_A\_FPGA-TX1-11-RX13-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:42:42		2018-Jan-24 01:43:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16938	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

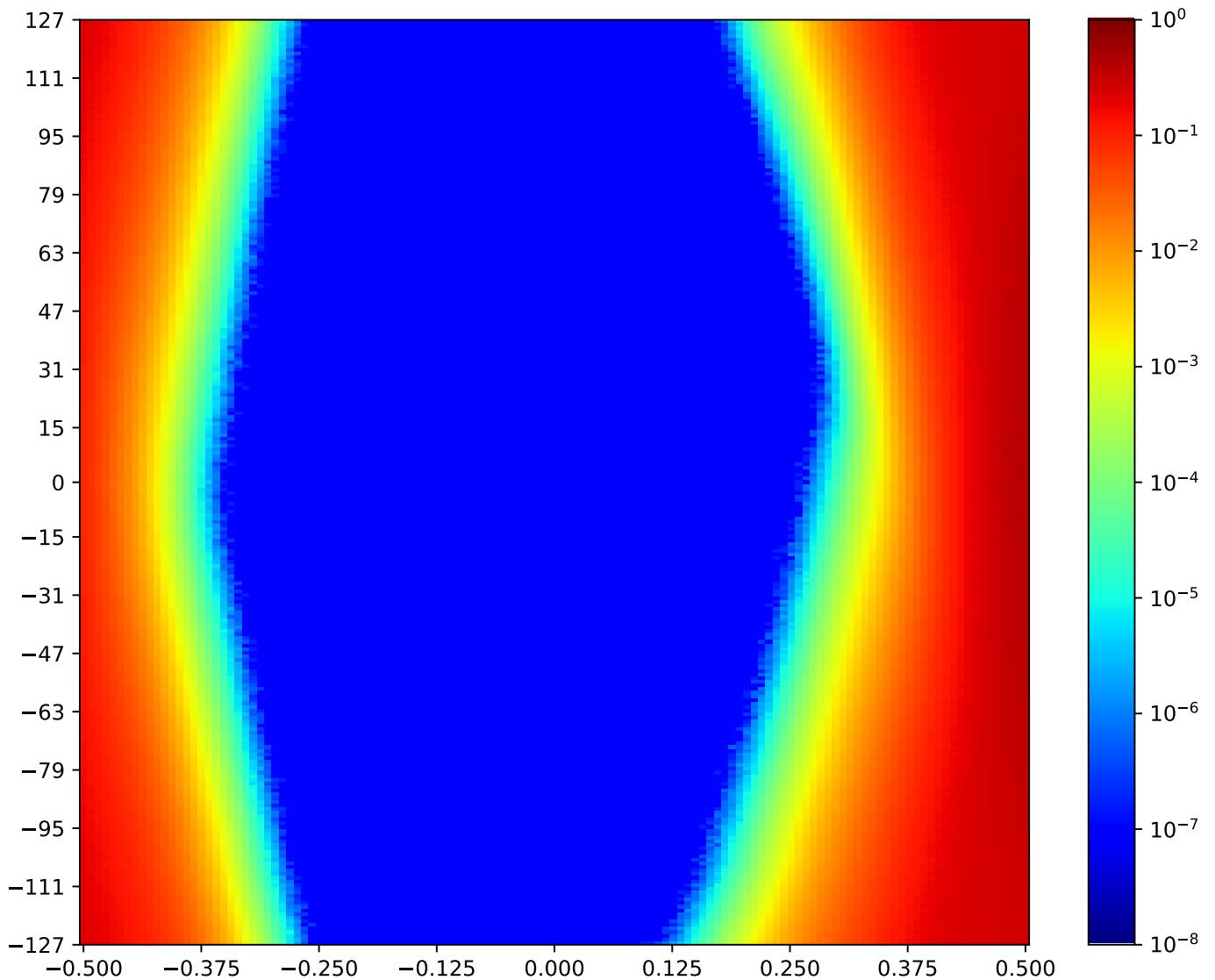


Figure 3.252: MSP\_A\_FPGA-TX1-11-RX13-11-MSP\_C\_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20 MSP\_A TX2 MSP\_C RX12 Minipod Loopback

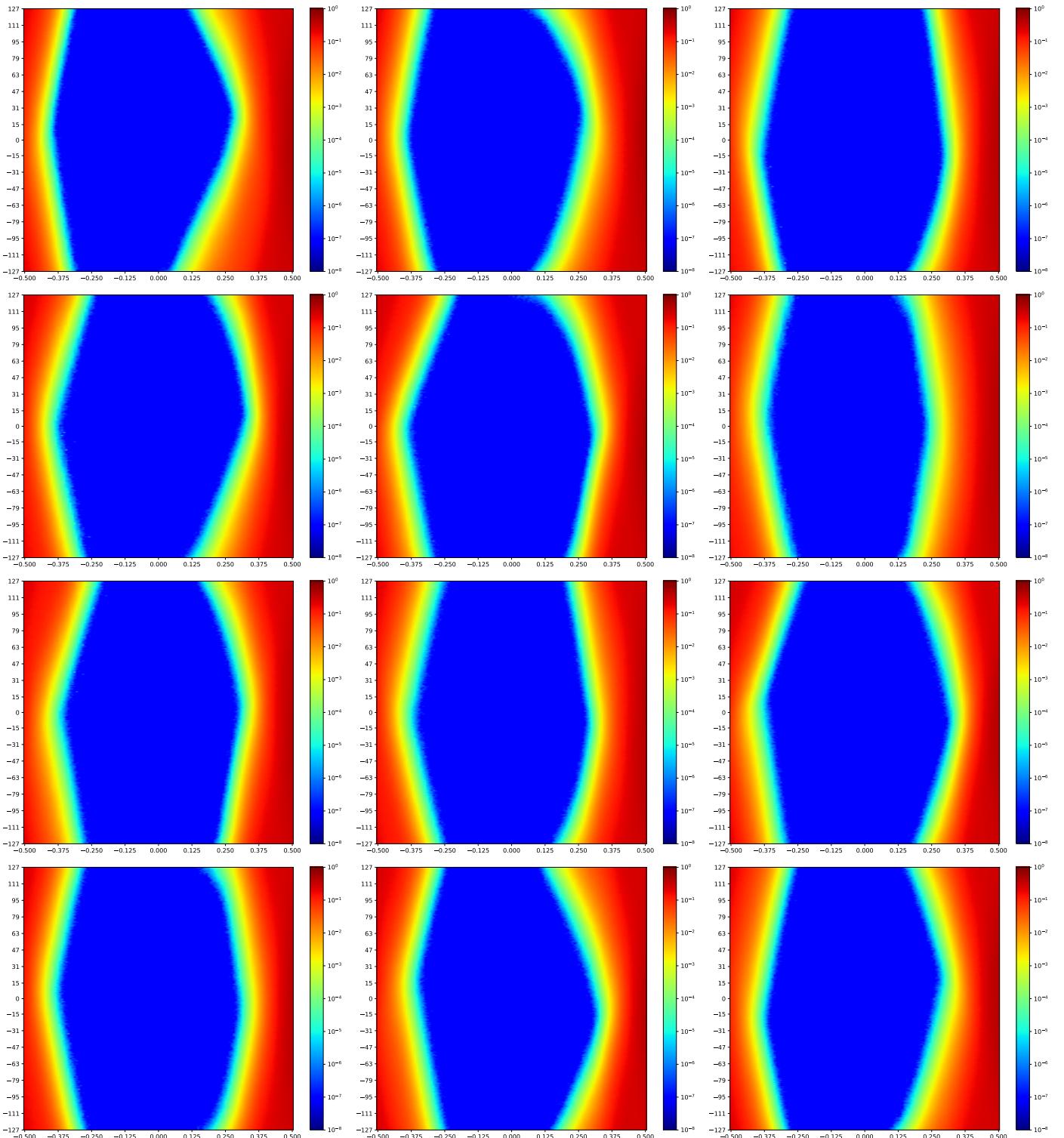


Figure 3.253: MSP\_A TX2 MSP\_C RX12 Minipod Loopback

A cross-reference to Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.266.

### 3.20.1 MSP\_A\_FPGA-TX2-00-RX12-00-MSP\_C\_FPGA

Table 3.234: MSP\_A\_FPGA-TX2-00-RX12-00-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:48:15		2018-Jan-24 01:48:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16566	79	61.24%	254	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

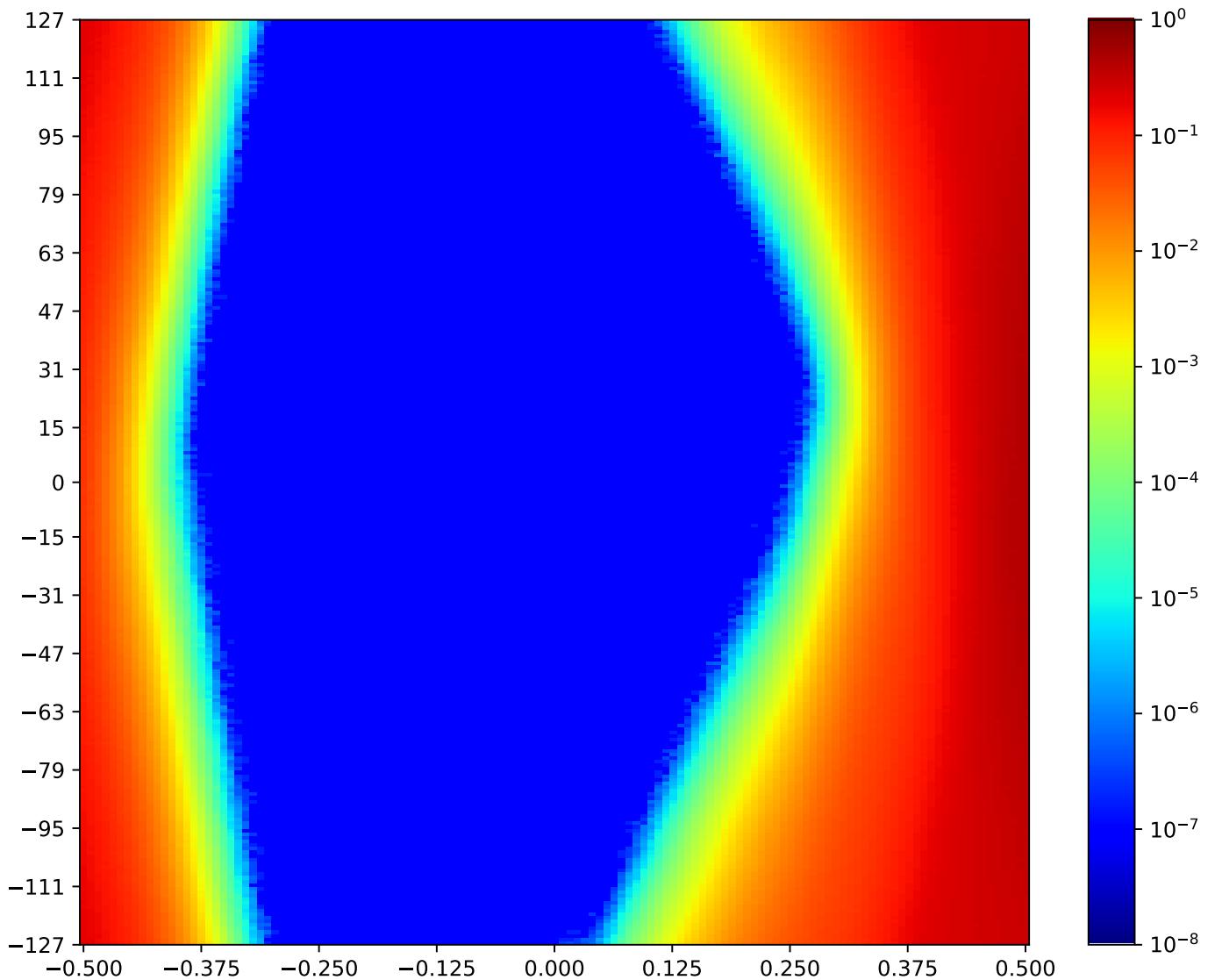


Figure 3.254: MSP\_A\_FPGA-TX2-00-RX12-00-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.2 MSP\_A\_FPGA-TX2-01-RX12-01-MSP\_C\_FPGA

Table 3.235: MSP\_A\_FPGA-TX2-01-RX12-01-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:46:51		2018-Jan-24 01:47:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16221	78	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

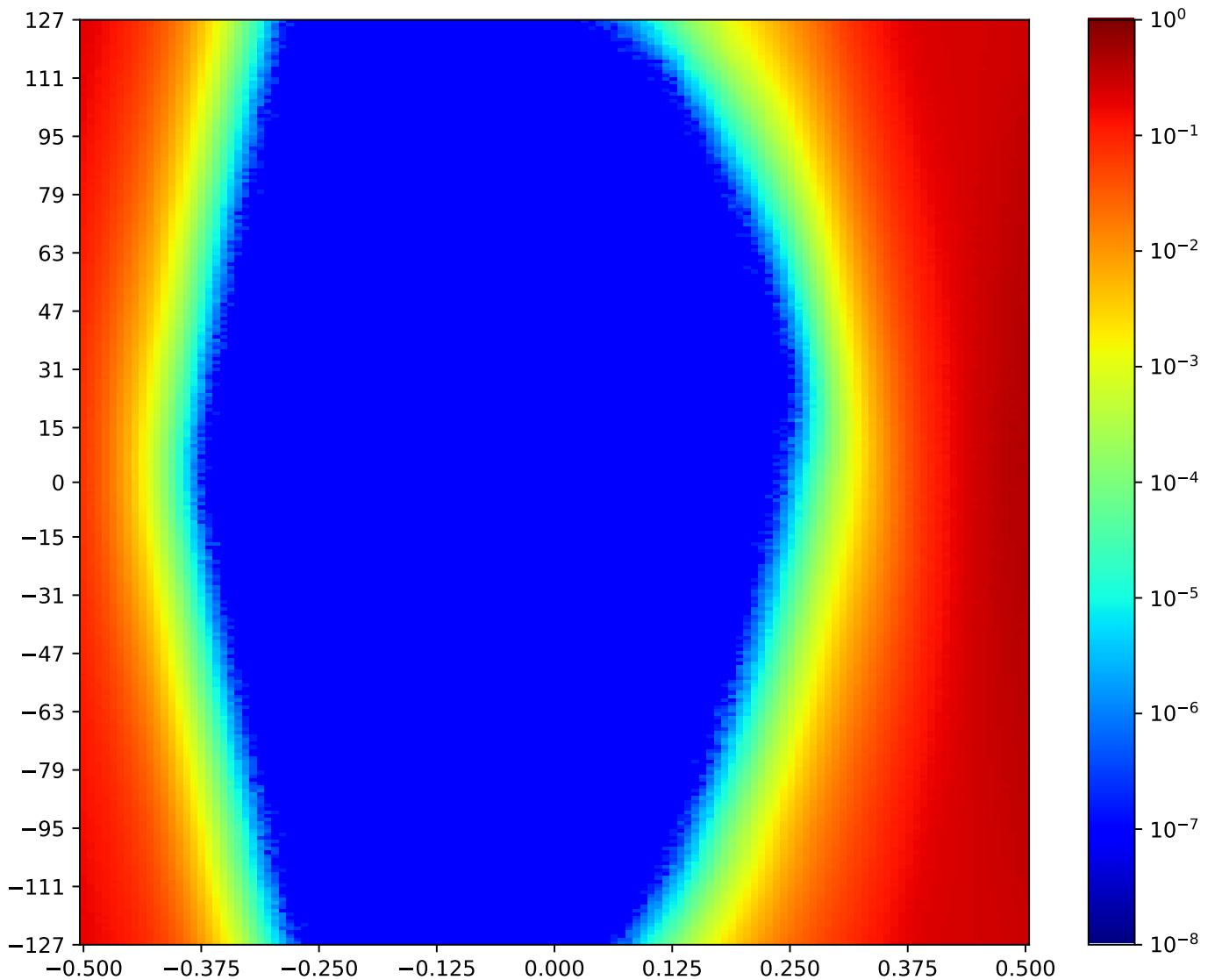


Figure 3.255: MSP\_A\_FPGA-TX2-01-RX12-01-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.3 MSP\_A\_FPGA-TX2-02-RX12-02-MSP\_C\_FPGA

Table 3.236: MSP\_A\_FPGA-TX2-02-RX12-02-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:50:22		2018-Jan-24 01:51:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18133	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

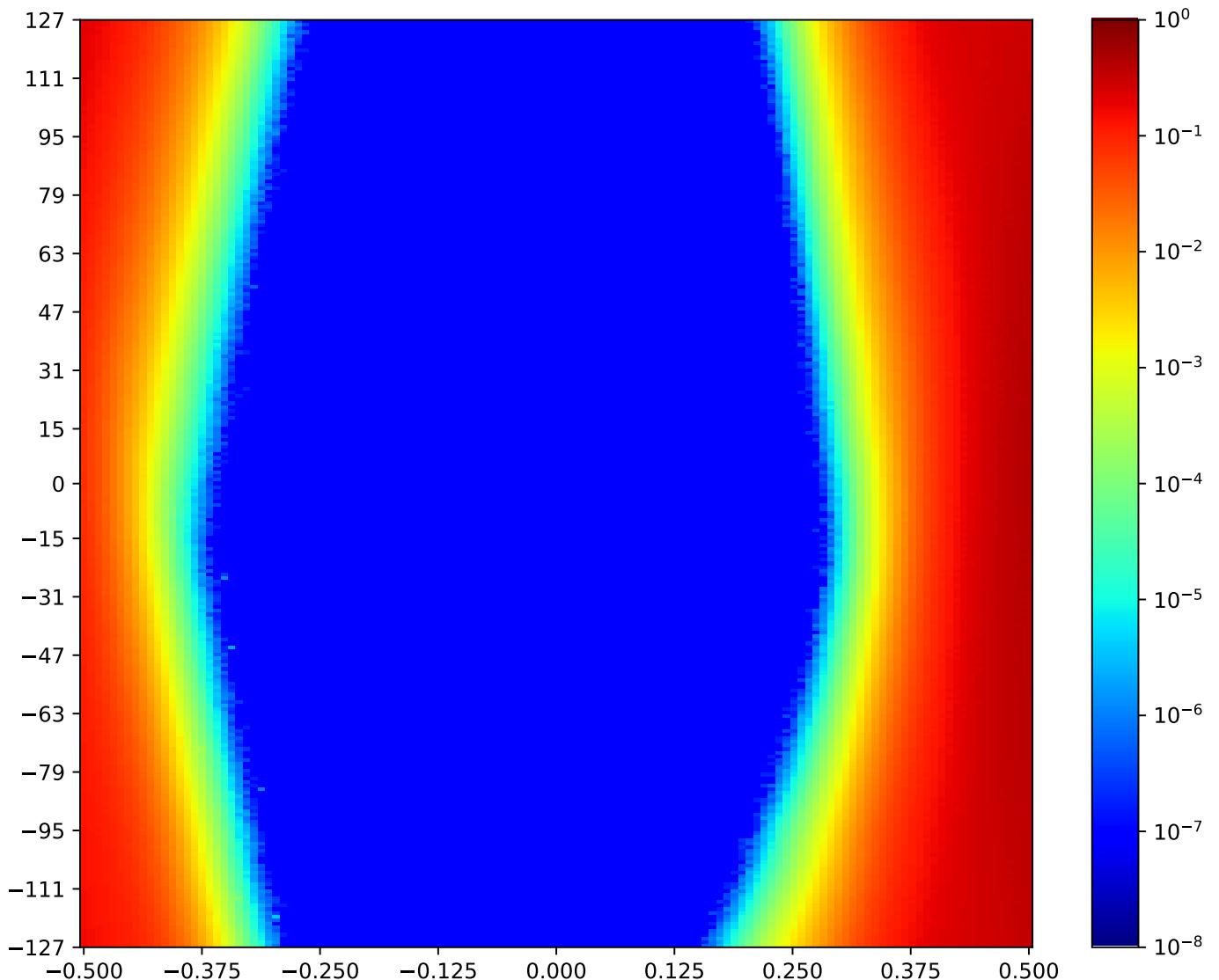


Figure 3.256: MSP\_A\_FPGA-TX2-02-RX12-02-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.4 MSP\_A\_FPGA-TX2-03-RX12-03-MSP\_C\_FPGA

Table 3.237: MSP\_A\_FPGA-TX2-03-RX12-03-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:46:09		2018-Jan-24 01:46:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17192	84	65.12%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

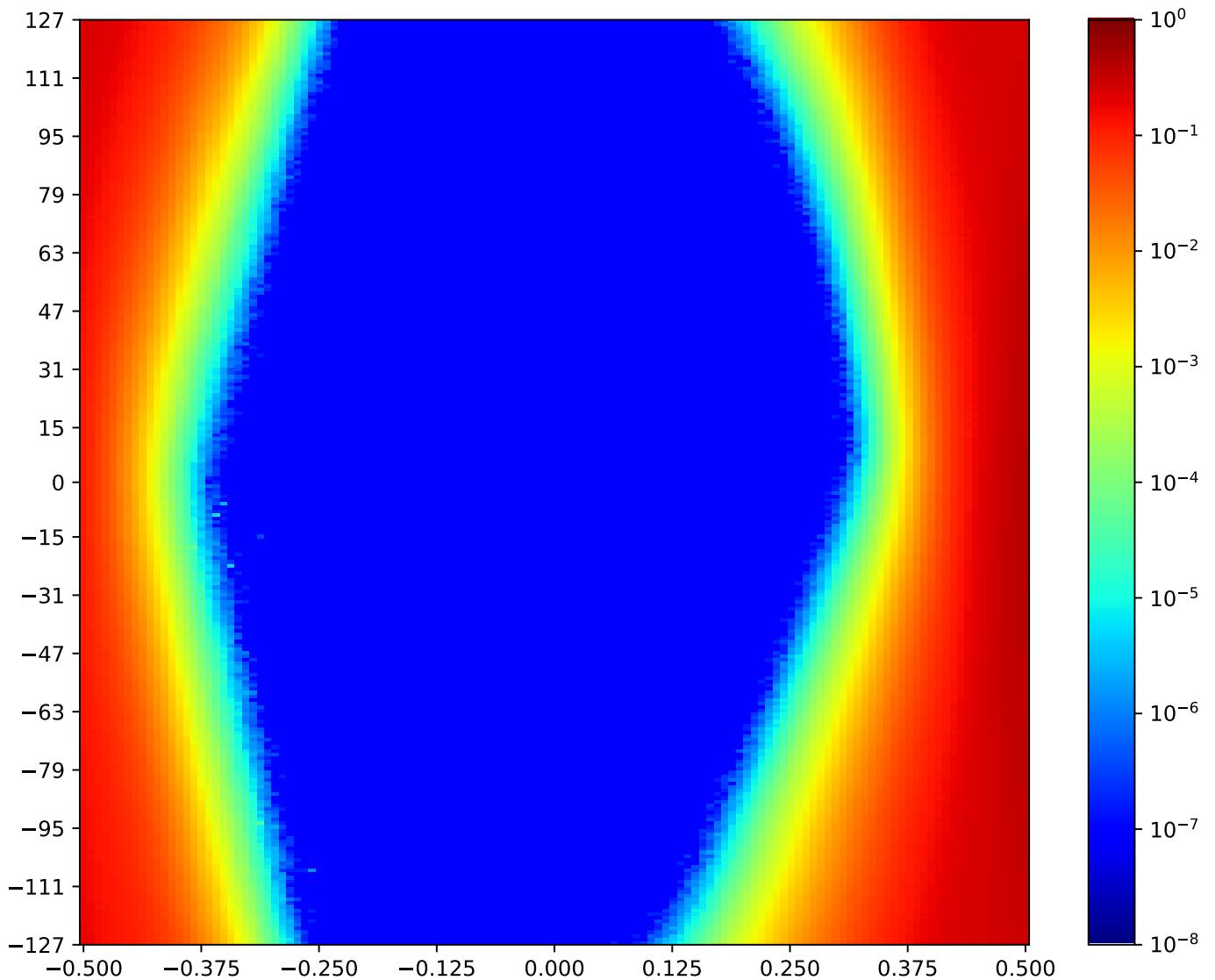


Figure 3.257: MSP\_A\_FPGA-TX2-03-RX12-03-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.5 MSP\_A\_FPGA-TX2-04-RX12-04-MSP\_C\_FPGA

Table 3.238: MSP\_A\_FPGA-TX2-04-RX12-04-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:52:30		2018-Jan-24 01:53:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16962	83	64.34%	254	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

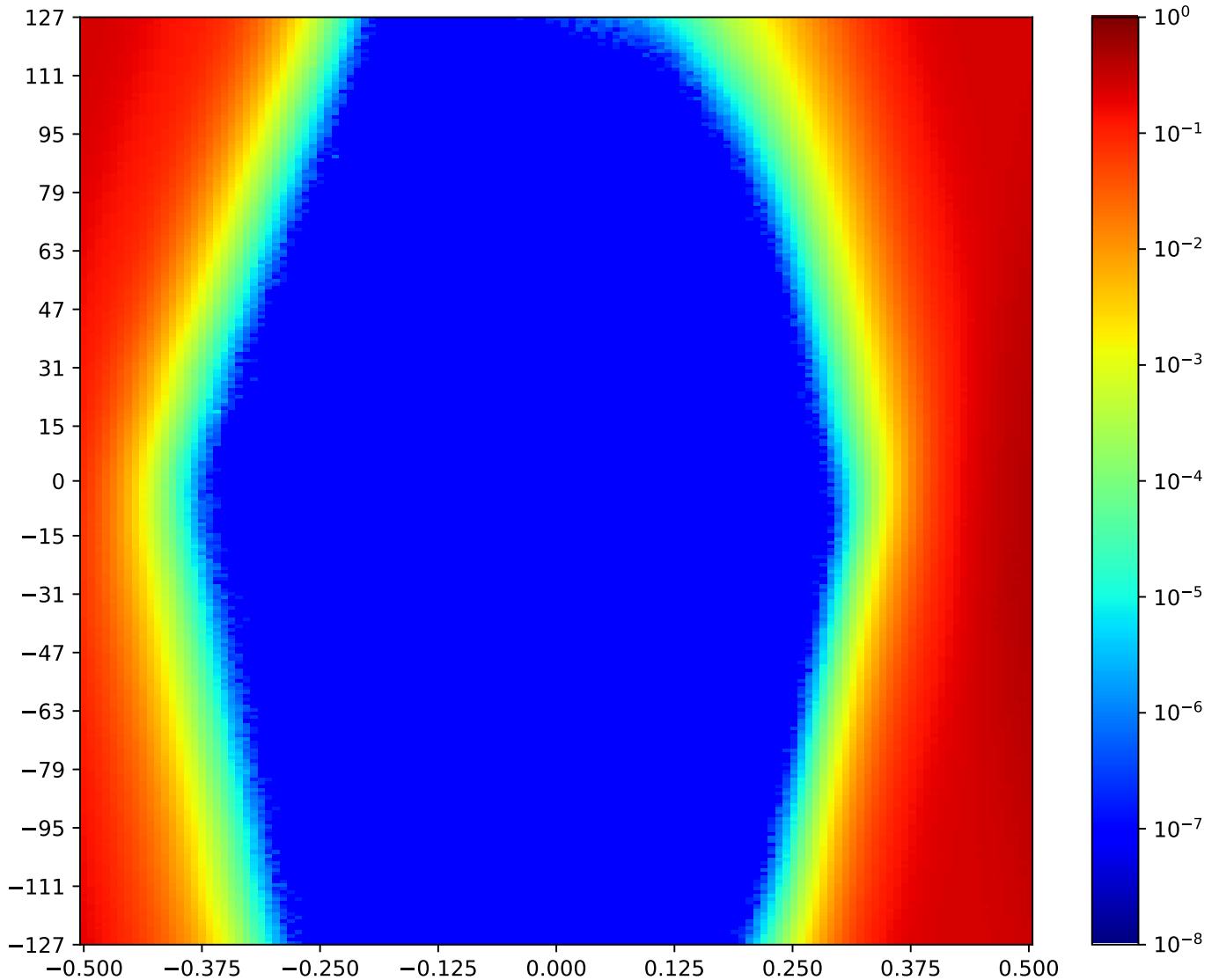


Figure 3.258: MSP\_A\_FPGA-TX2-04-RX12-04-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.6 MSP\_A\_FPGA-TX2-05-RX12-05-MSP\_C\_FPGA

Table 3.239: MSP\_A\_FPGA-TX2-05-RX12-05-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:47:33		2018-Jan-24 01:48:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15140	70	53.49%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

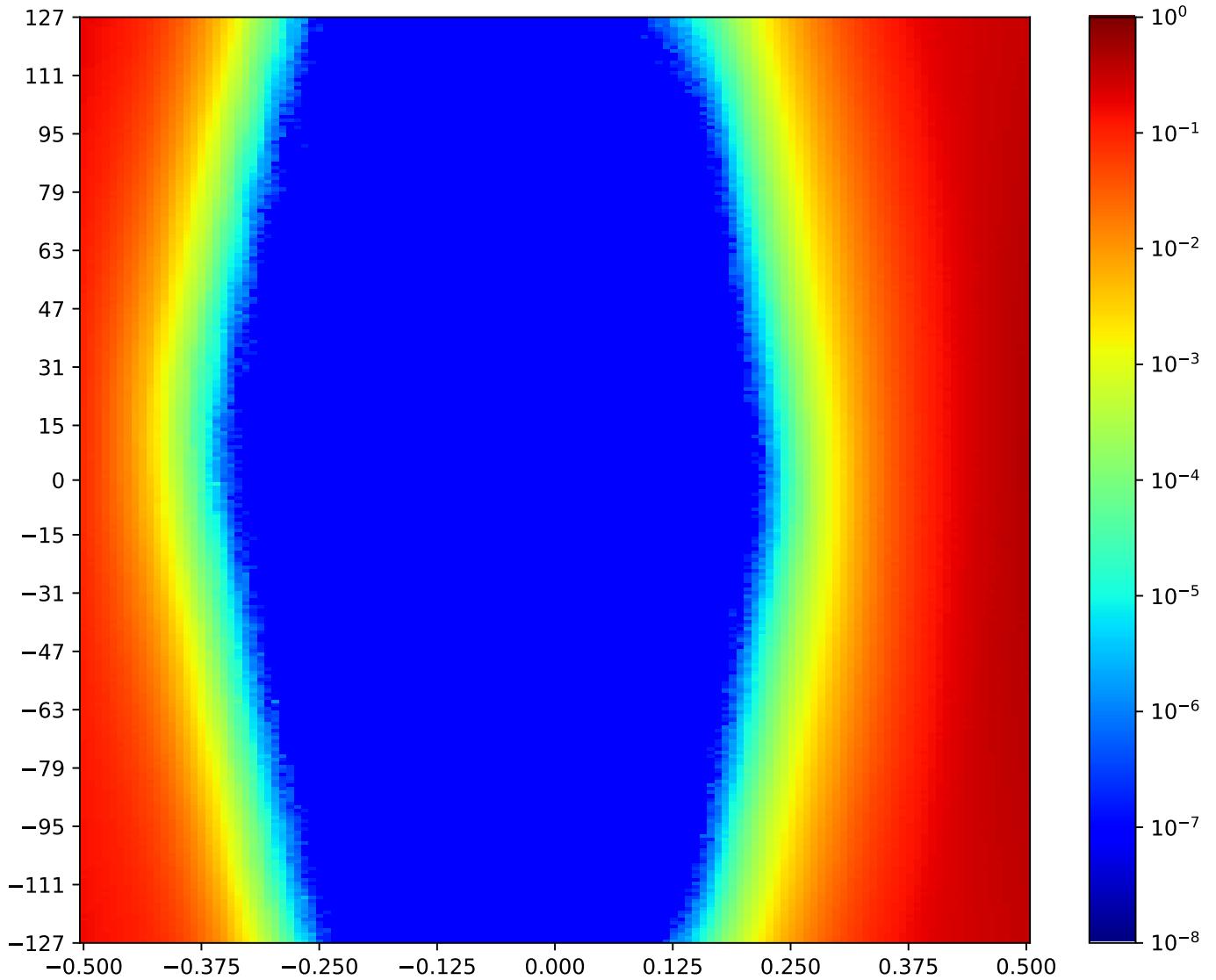


Figure 3.259: MSP\_A\_FPGA-TX2-05-RX12-05-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.7 MSP\_A\_FPGA-TX2-06-RX12-06-MSP\_C\_FPGA

Table 3.240: MSP\_A\_FPGA-TX2-06-RX12-06-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:53:55		2018-Jan-24 01:54:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16925	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

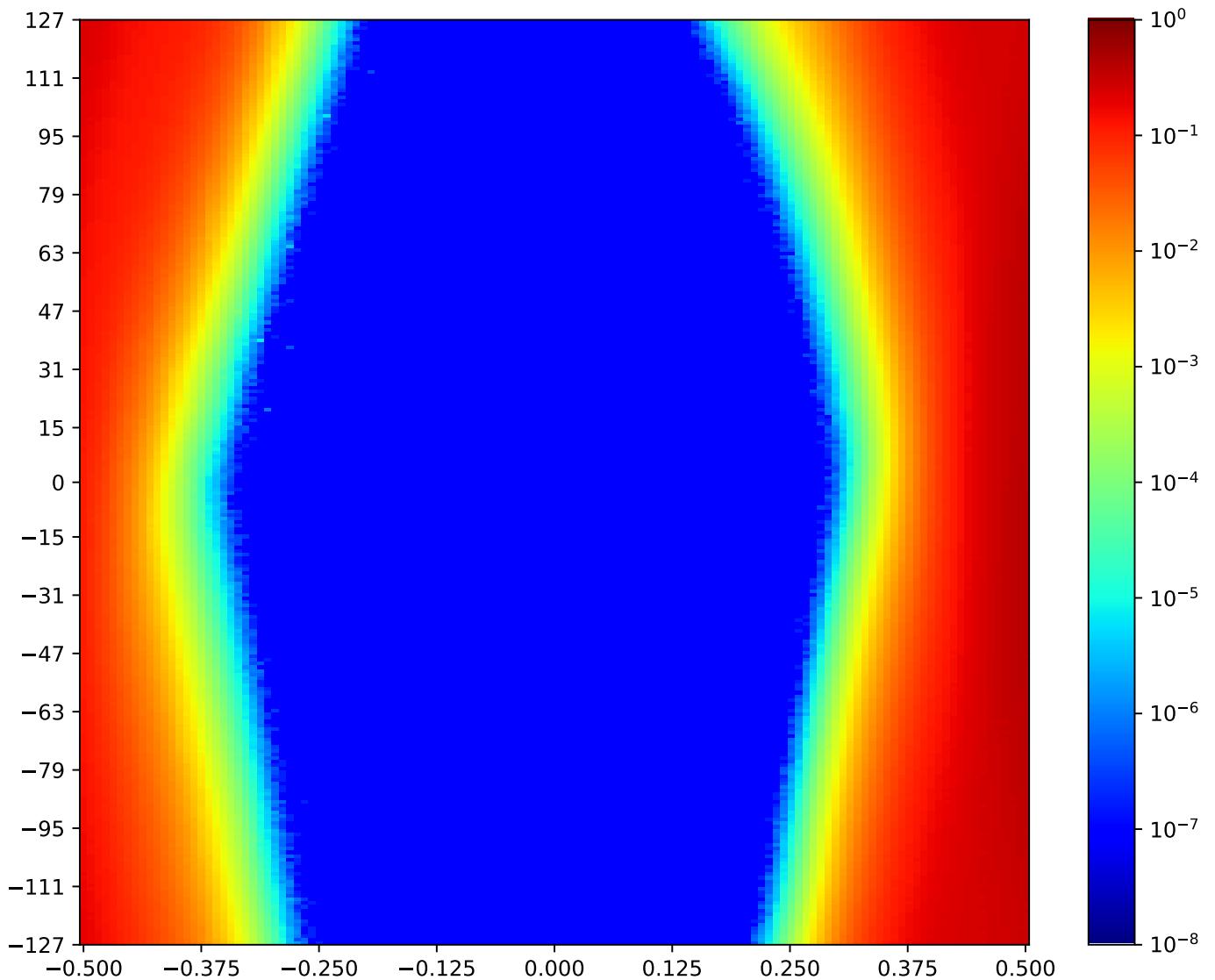


Figure 3.260: MSP\_A\_FPGA-TX2-06-RX12-06-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.8 MSP\_A\_FPGA-TX2-07-RX12-07-MSP\_C\_FPGA

Table 3.241: MSP\_A\_FPGA-TX2-07-RX12-07-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:48:57		2018-Jan-24 01:49:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16707	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

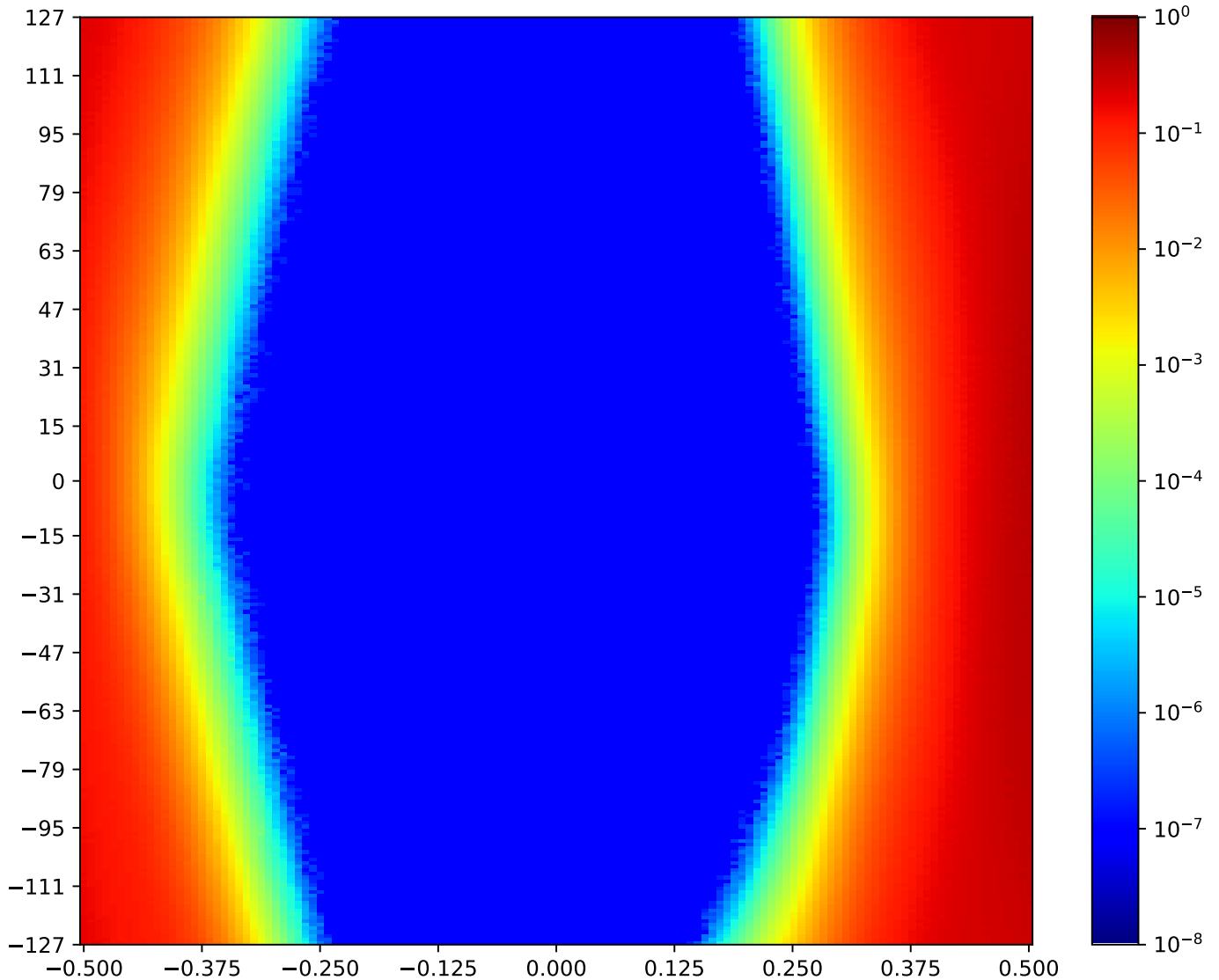


Figure 3.261: MSP\_A\_FPGA-TX2-07-RX12-07-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.9 MSP\_A\_FPGA-TX2-08-RX12-08-MSP\_C\_FPGA

Table 3.242: MSP\_A\_FPGA-TX2-08-RX12-08-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:53:13		2018-Jan-24 01:53:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17393	82	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

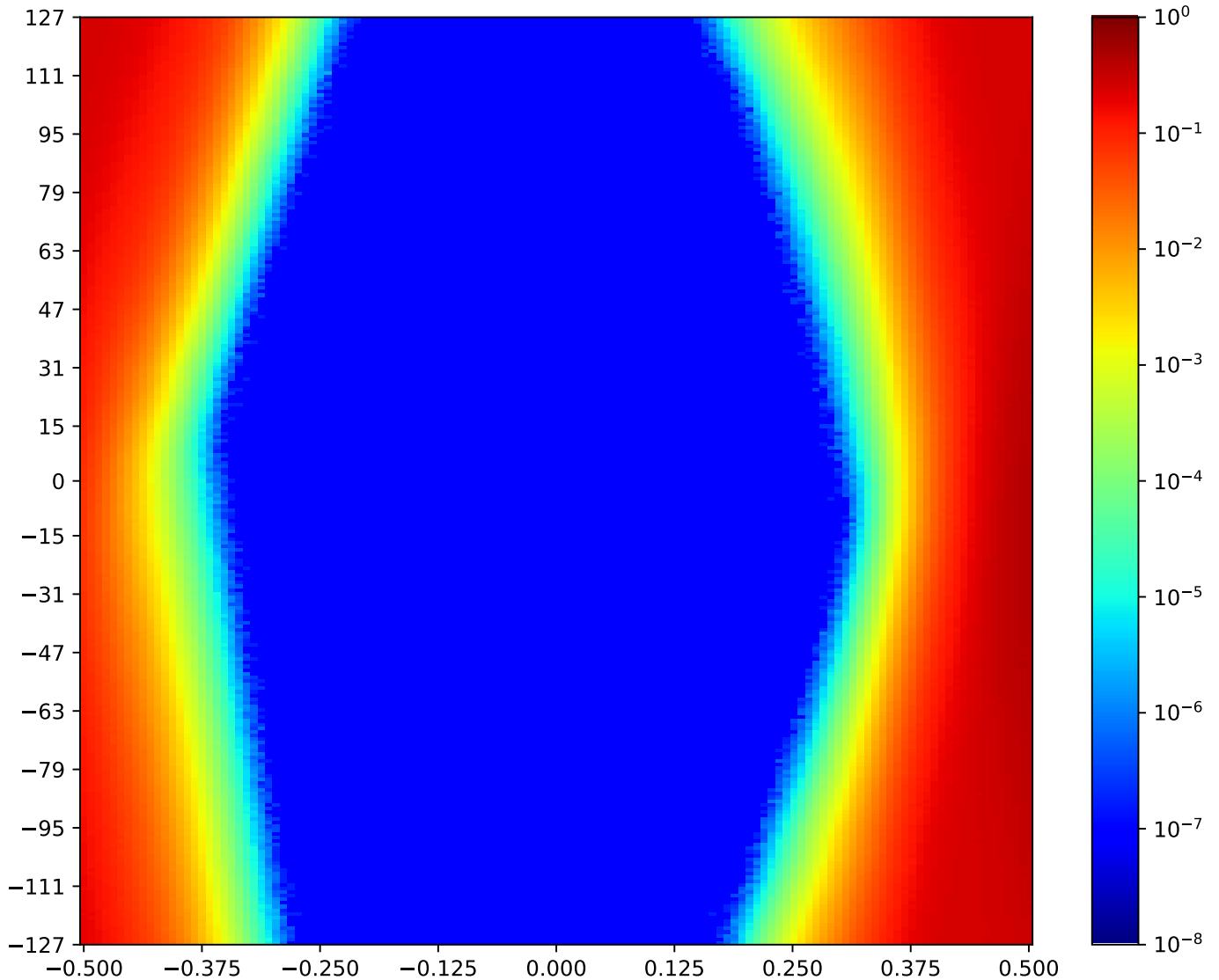


Figure 3.262: MSP\_A\_FPGA-TX2-08-RX12-08-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.10 MSP\_A\_FPGA-TX2-09-RX12-09-MSP\_C\_FPGA

Table 3.243: MSP\_A\_FPGA-TX2-09-RX12-09-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:49:40		2018-Jan-24 01:50:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17948	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

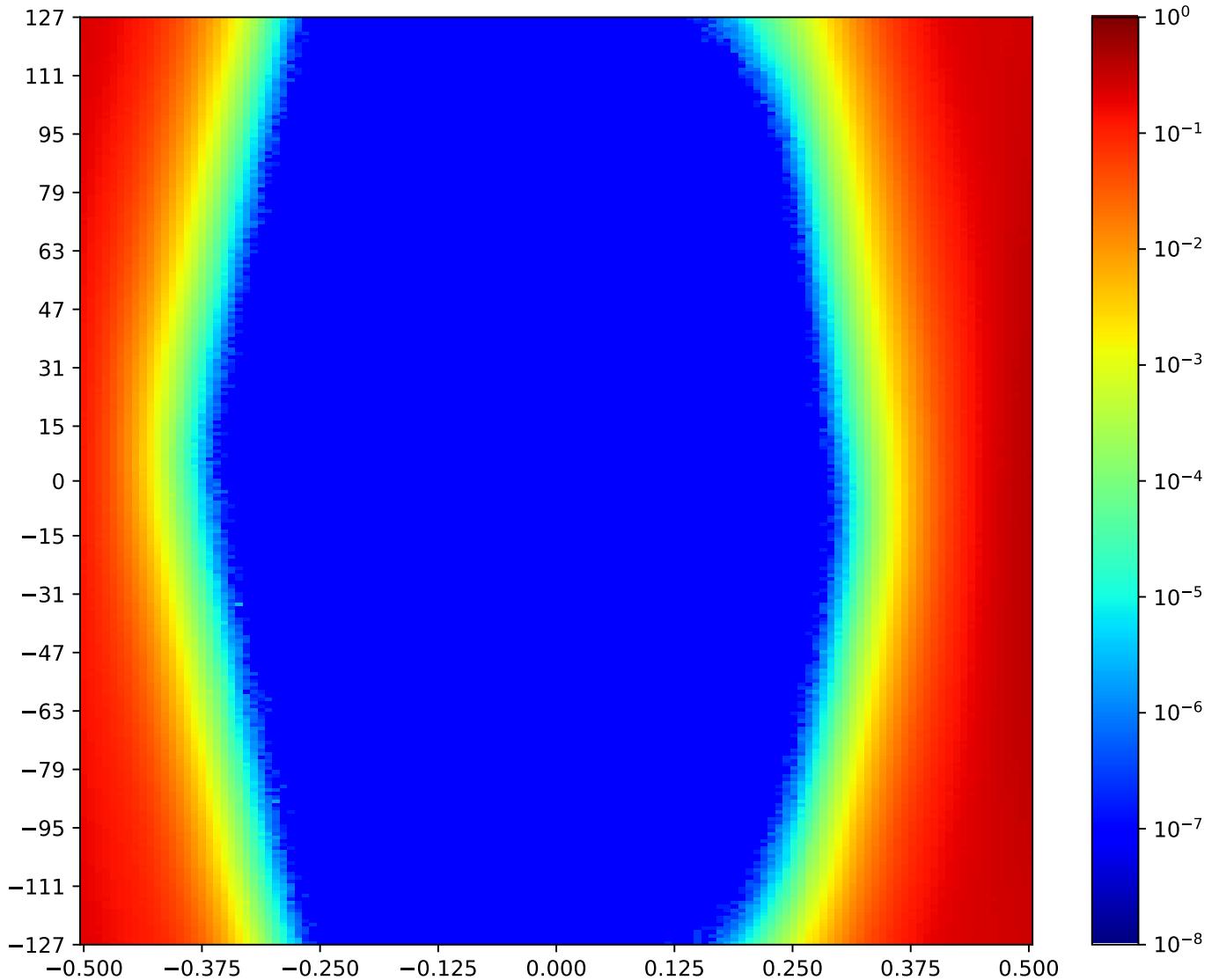


Figure 3.263: MSP\_A\_FPGA-TX2-09-RX12-09-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.11 MSP\_A\_FPGA-TX2-10-RX12-10-MSP\_C\_FPGA

Table 3.244: MSP\_A\_FPGA-TX2-10-RX12-10-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:51:48		2018-Jan-24 01:52:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16336	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

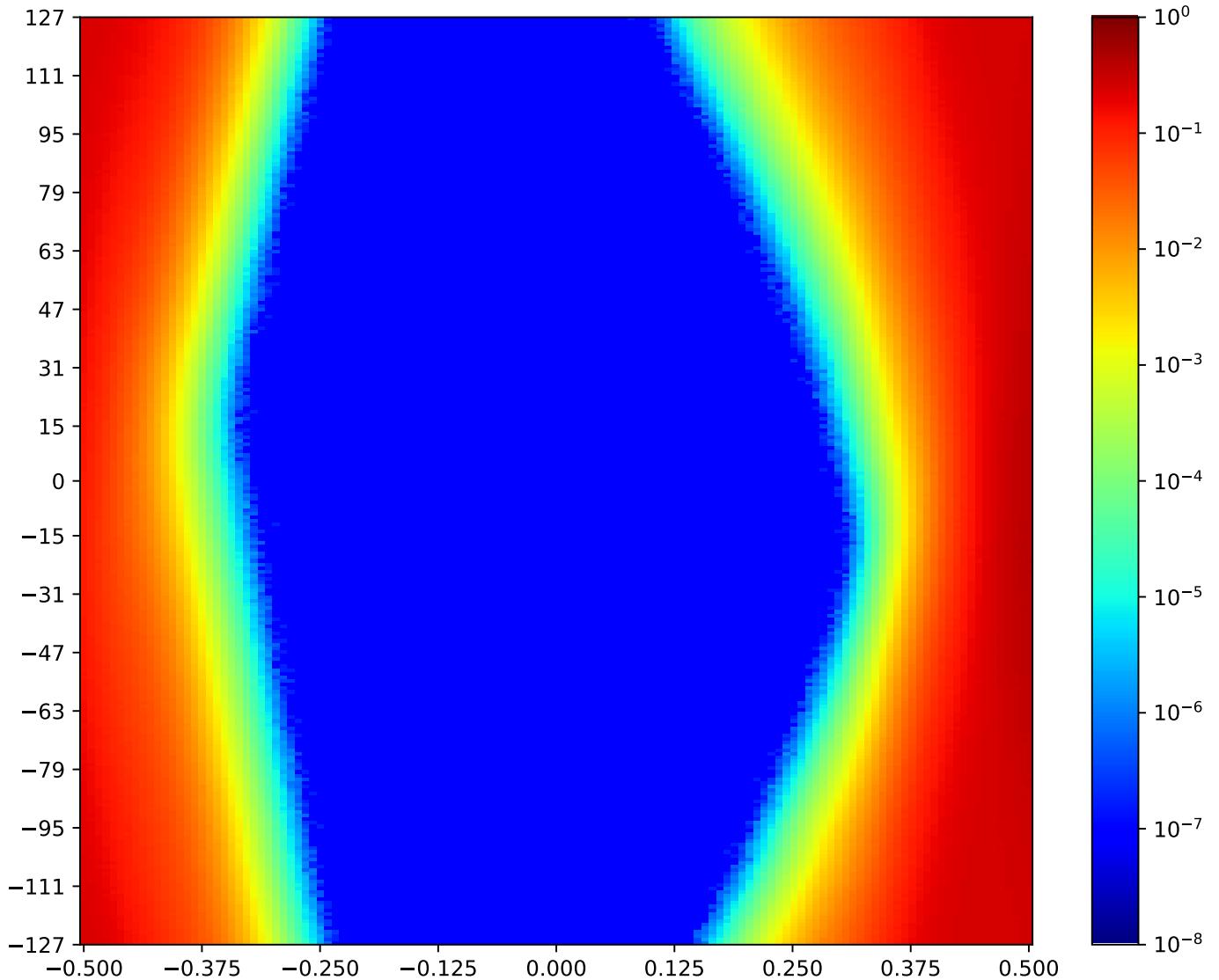


Figure 3.264: MSP\_A\_FPGA-TX2-10-RX12-10-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.20.12 MSP\_A\_FPGA-TX2-11-RX12-11-MSP\_C\_FPGA

Table 3.245: MSP\_A\_FPGA-TX2-11-RX12-11-MSP\_C\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:51:05		2018-Jan-24 01:51:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16455	74	57.36%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

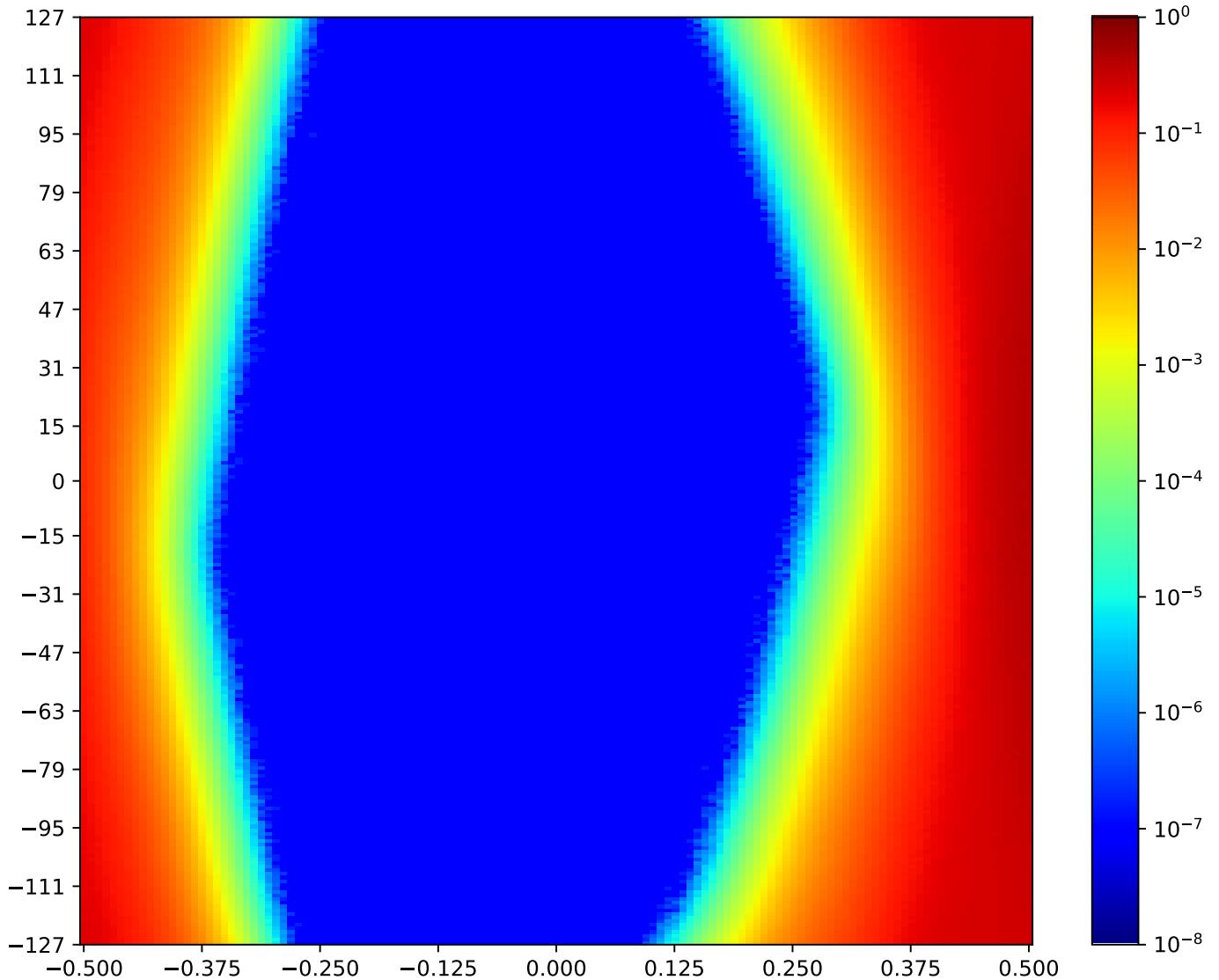


Figure 3.265: MSP\_A\_FPGA-TX2-11-RX12-11-MSP\_C\_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21 MSP\_C TX3 MSP\_A RX4 Minipod Loopback

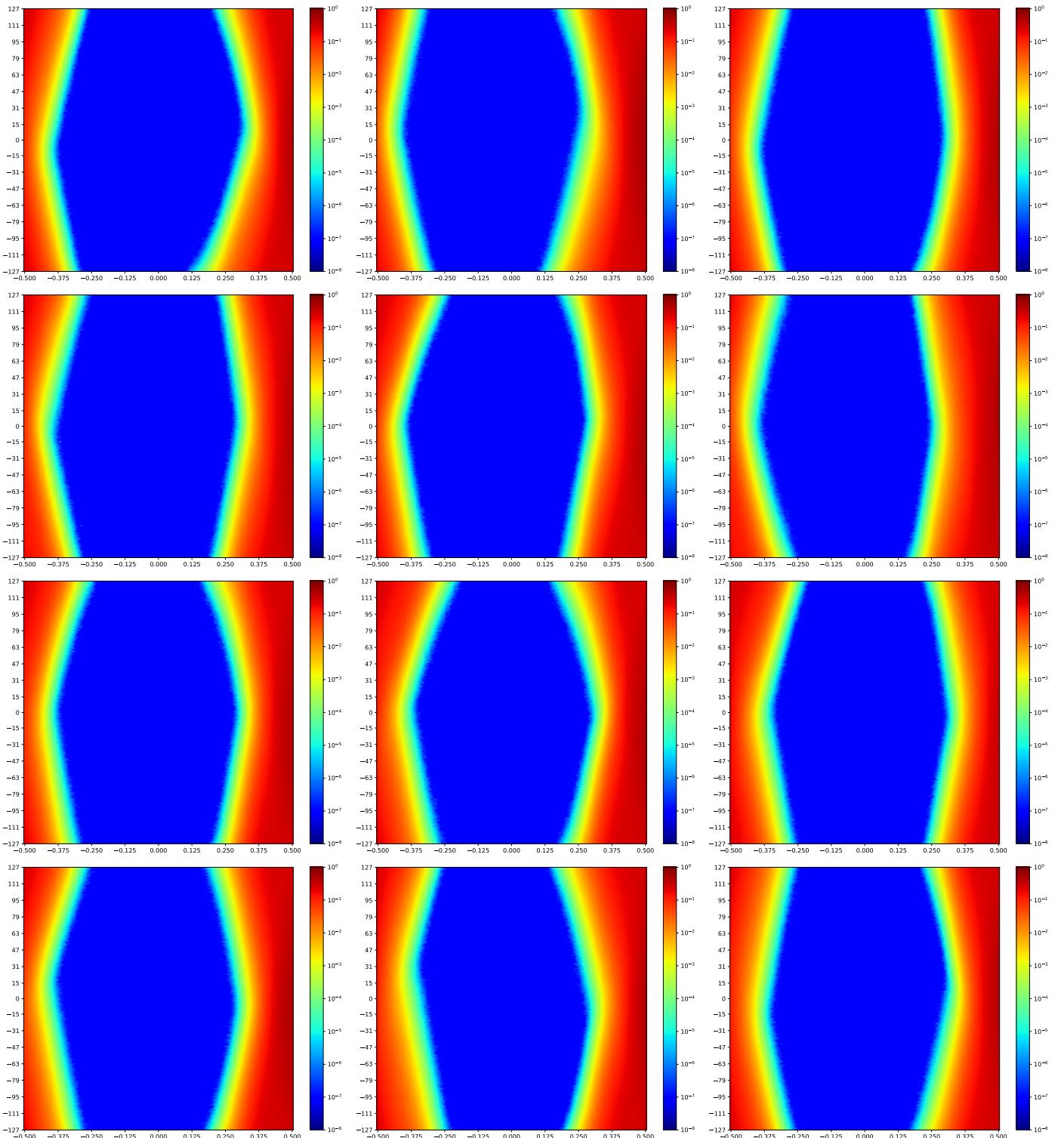


Figure 3.266: MSP\_C TX3 MSP\_A RX4 Minipod Loopback

A cross-reference to Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.279.

### 3.21.1 MSP\_C\_FPGA-TX3-00-RX4-00-MSP\_A\_FPGA

Table 3.246: MSP\_C\_FPGA-TX3-00-RX4-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:56:47		2018-Jan-24 01:57:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18014	83	64.34%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

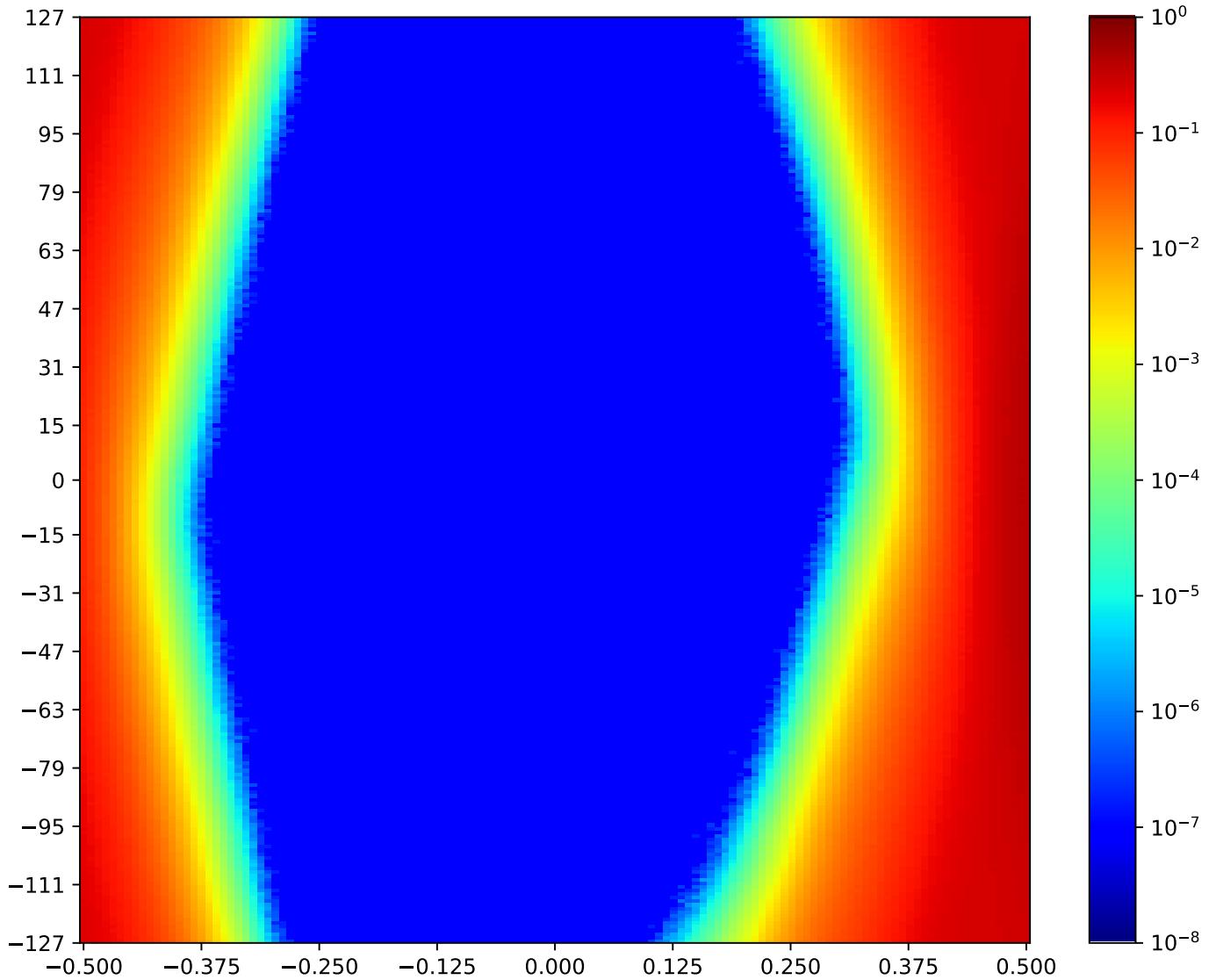


Figure 3.267: MSP\_C\_FPGA-TX3-00-RX4-00-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.2 MSP\_C\_FPGA-TX3-01-RX4-01-MSP\_A\_FPGA

Table 3.247: MSP\_C\_FPGA-TX3-01-RX4-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:58:12		2018-Jan-24 01:58:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16973	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

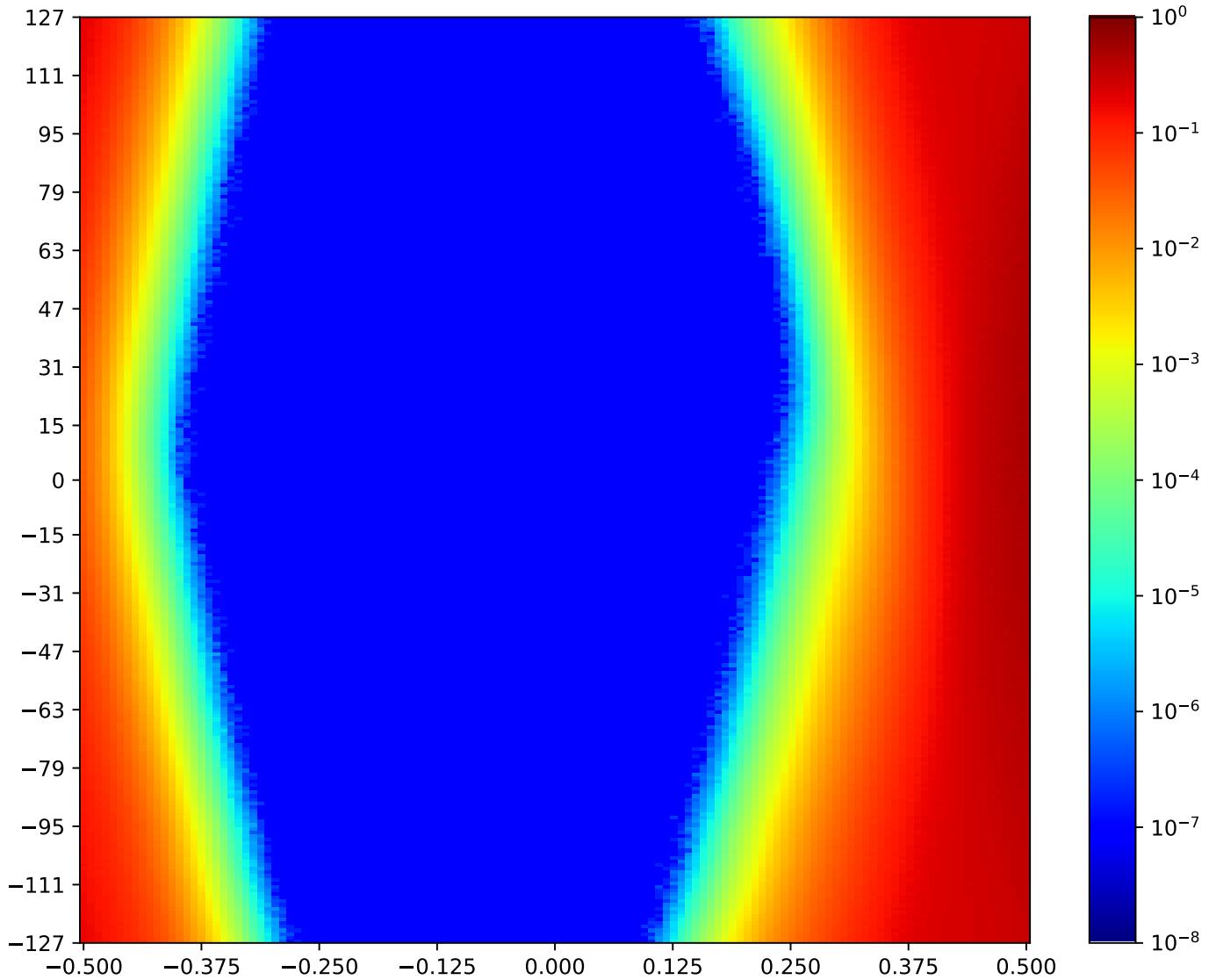


Figure 3.268: MSP\_C\_FPGA-TX3-01-RX4-01-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.3 MSP\_C\_FPGA-TX3-02-RX4-02-MSP\_A\_FPGA

Table 3.248: MSP\_C\_FPGA-TX3-02-RX4-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:58:55		2018-Jan-24 01:59:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18448	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

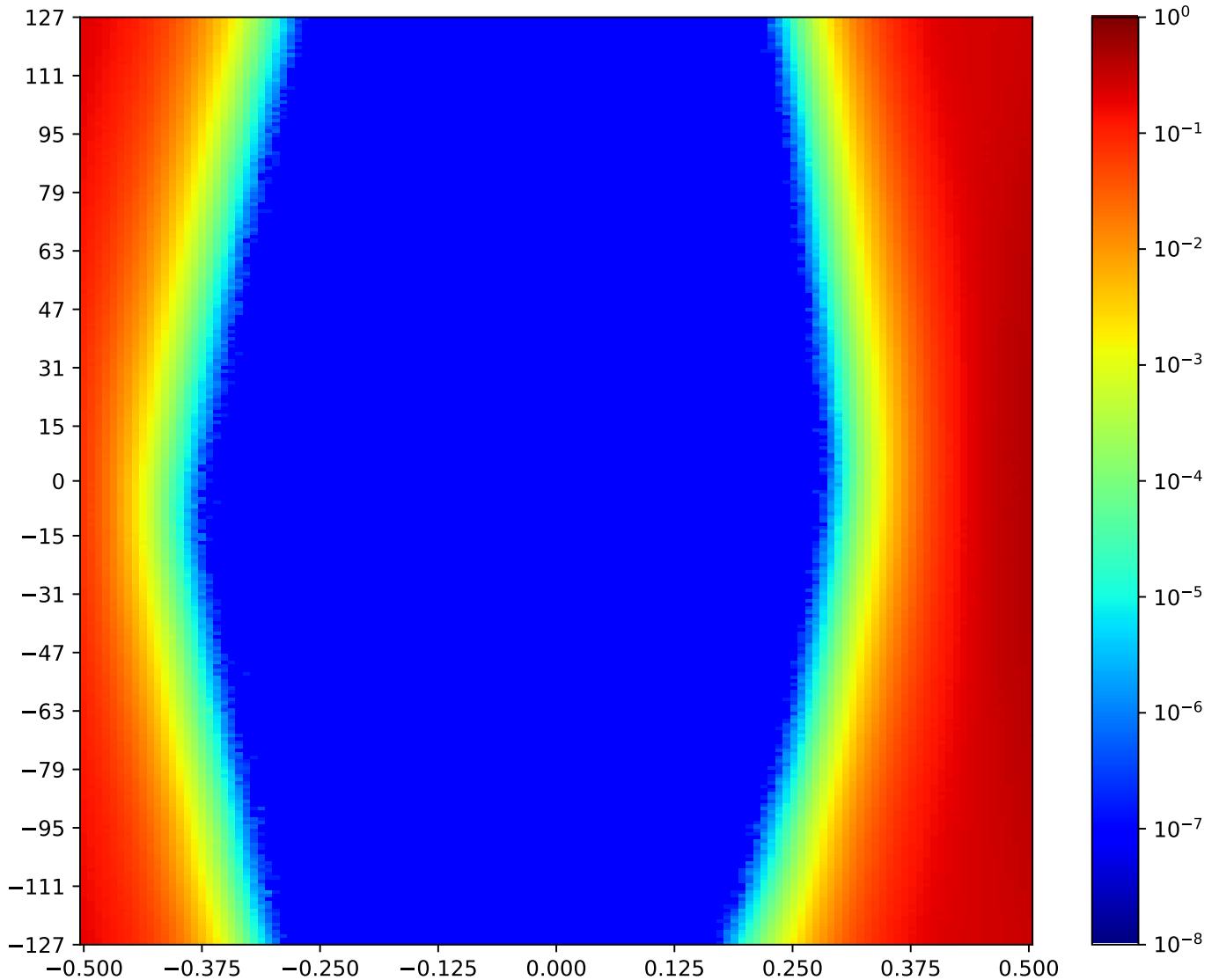


Figure 3.269: MSP\_C\_FPGA-TX3-02-RX4-02-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.4 MSP\_C\_FPGA-TX3-03-RX4-03-MSP\_A\_FPGA

Table 3.249: MSP\_C\_FPGA-TX3-03-RX4-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:55:21		2018-Jan-24 01:56:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17991	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

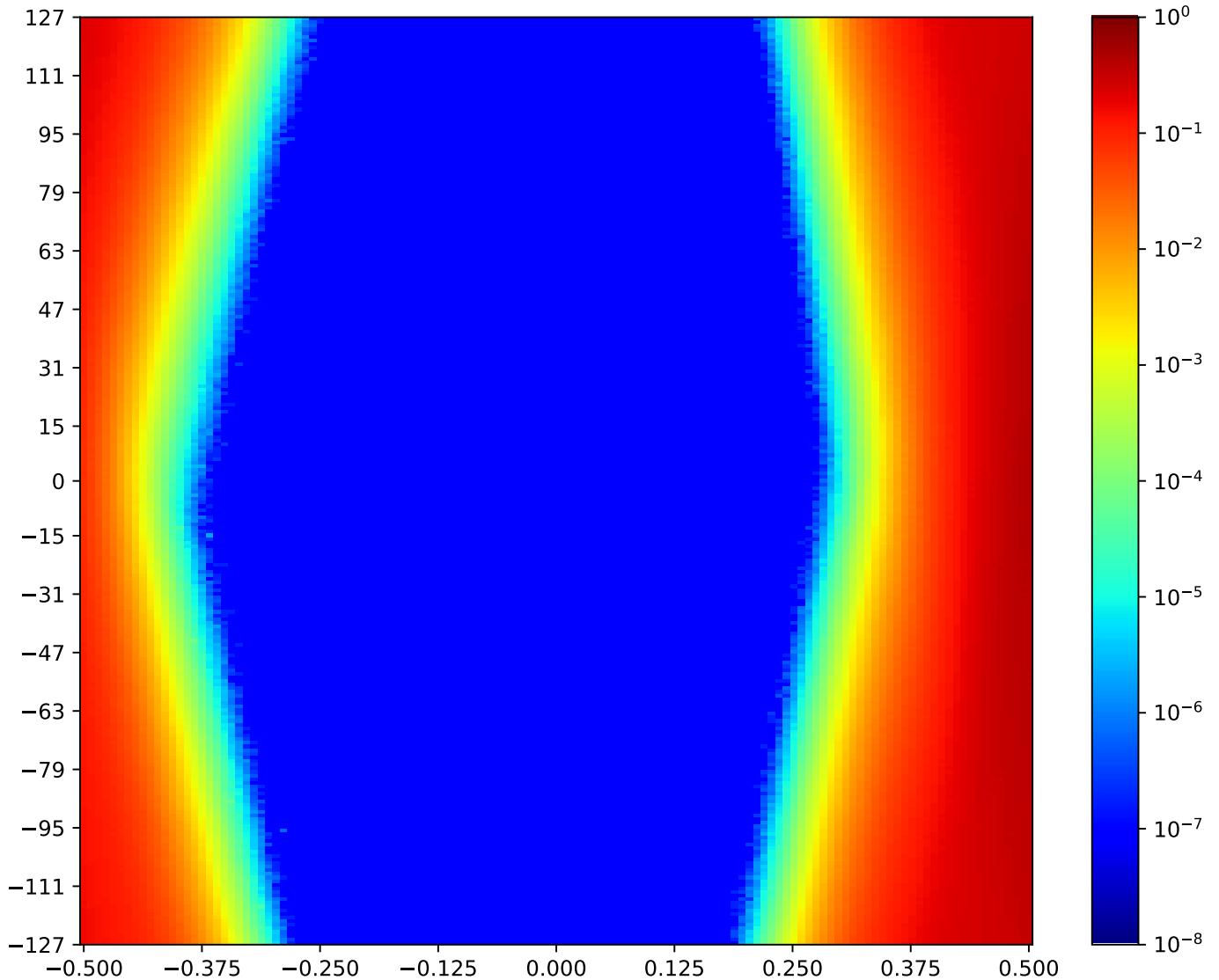


Figure 3.270: MSP\_C\_FPGA-TX3-03-RX4-03-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.5 MSP\_C\_FPGA-TX3-04-RX4-04-MSP\_A\_FPGA

Table 3.250: MSP\_C\_FPGA-TX3-04-RX4-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:01:03		2018-Jan-24 02:01:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17509	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

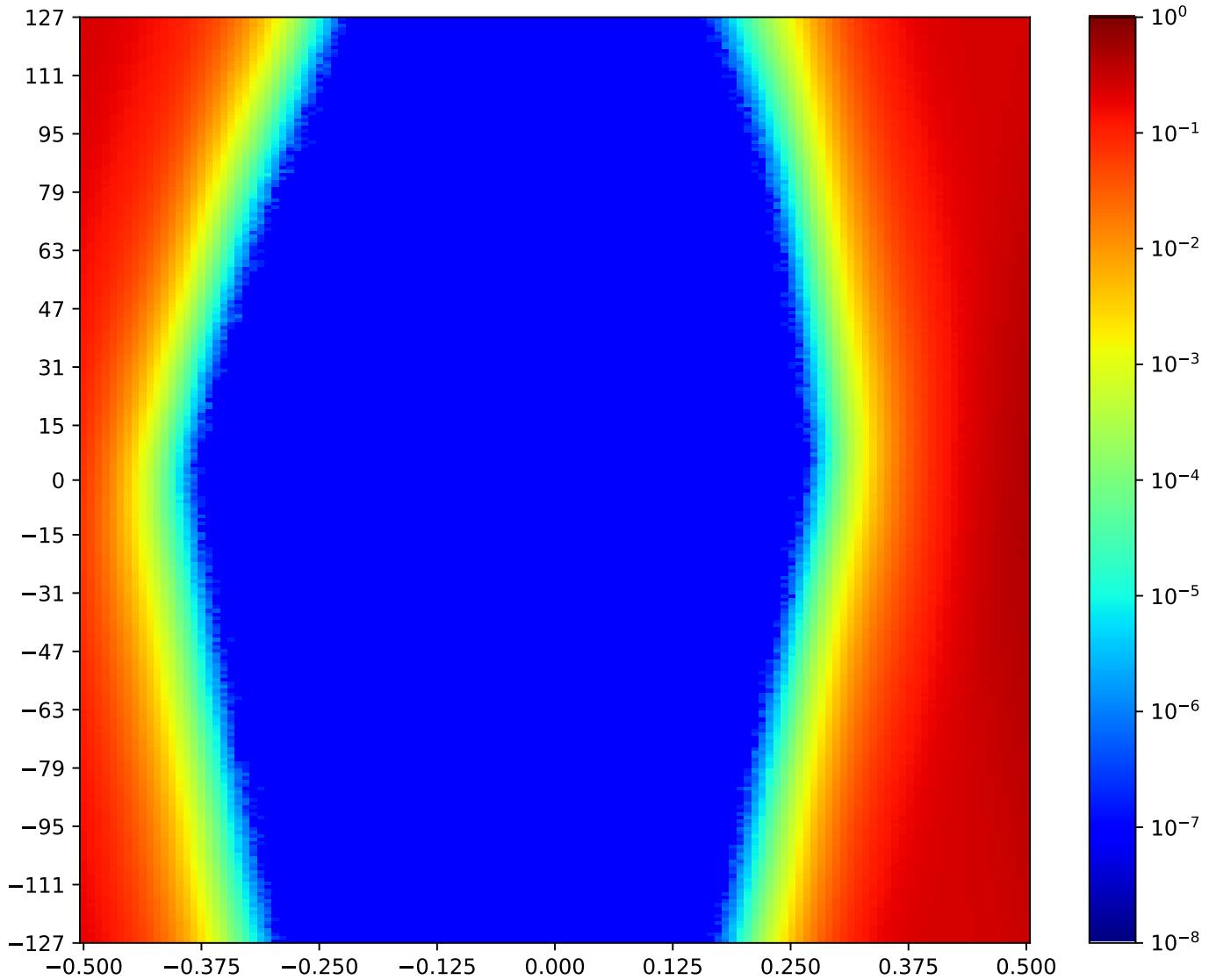


Figure 3.271: MSP\_C\_FPGA-TX3-04-RX4-04-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.6 MSP\_C\_FPGA-TX3-05-RX4-05-MSP\_A\_FPGA

Table 3.251: MSP\_C\_FPGA-TX3-05-RX4-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:54:38		2018-Jan-24 01:55:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16706	79	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

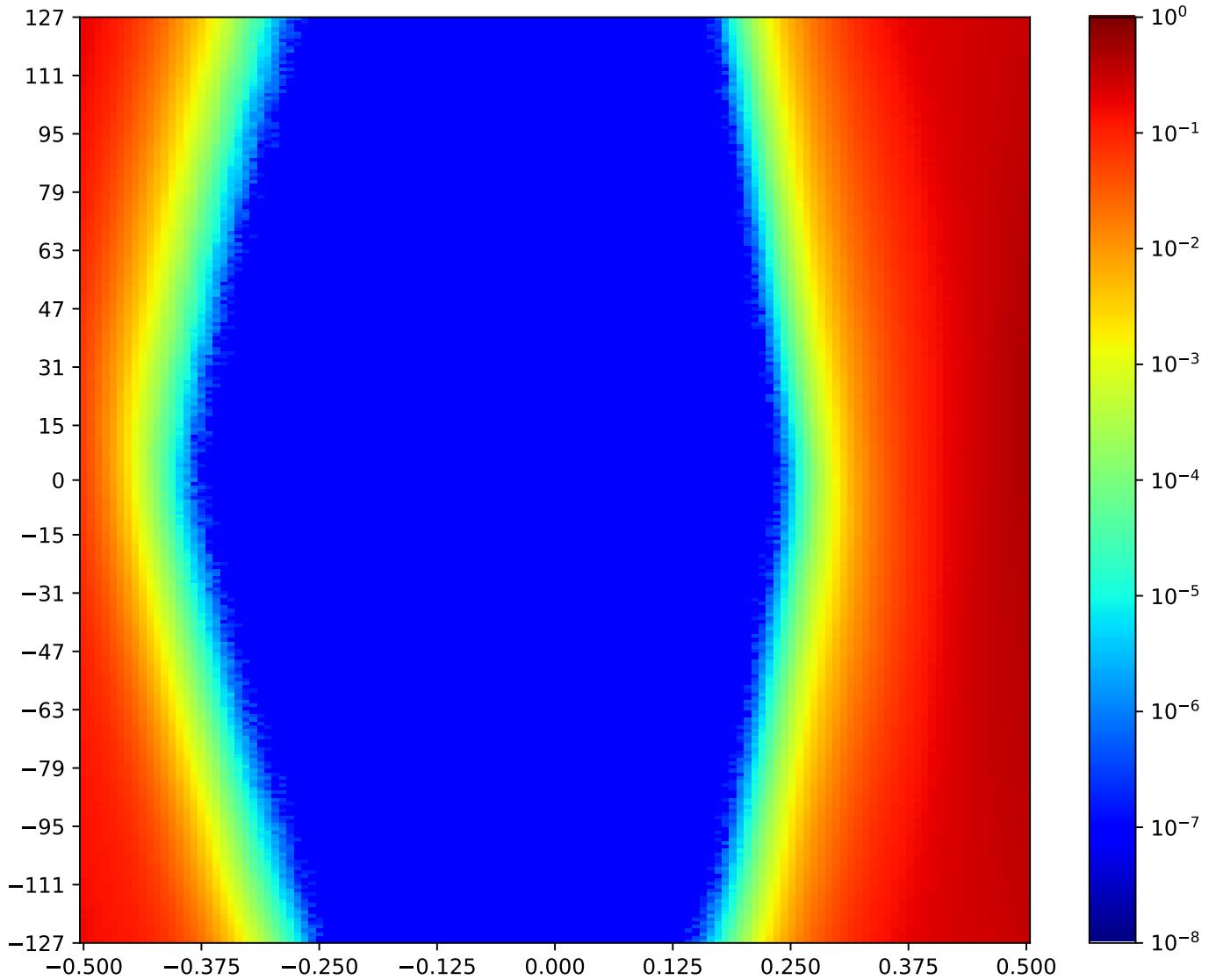


Figure 3.272: MSP\_C\_FPGA-TX3-05-RX4-05-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.7 MSP\_C\_FPGA-TX3-06-RX4-06-MSP\_A\_FPGA

Table 3.252: MSP\_C\_FPGA-TX3-06-RX4-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:02:28		2018-Jan-24 02:03:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17653	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

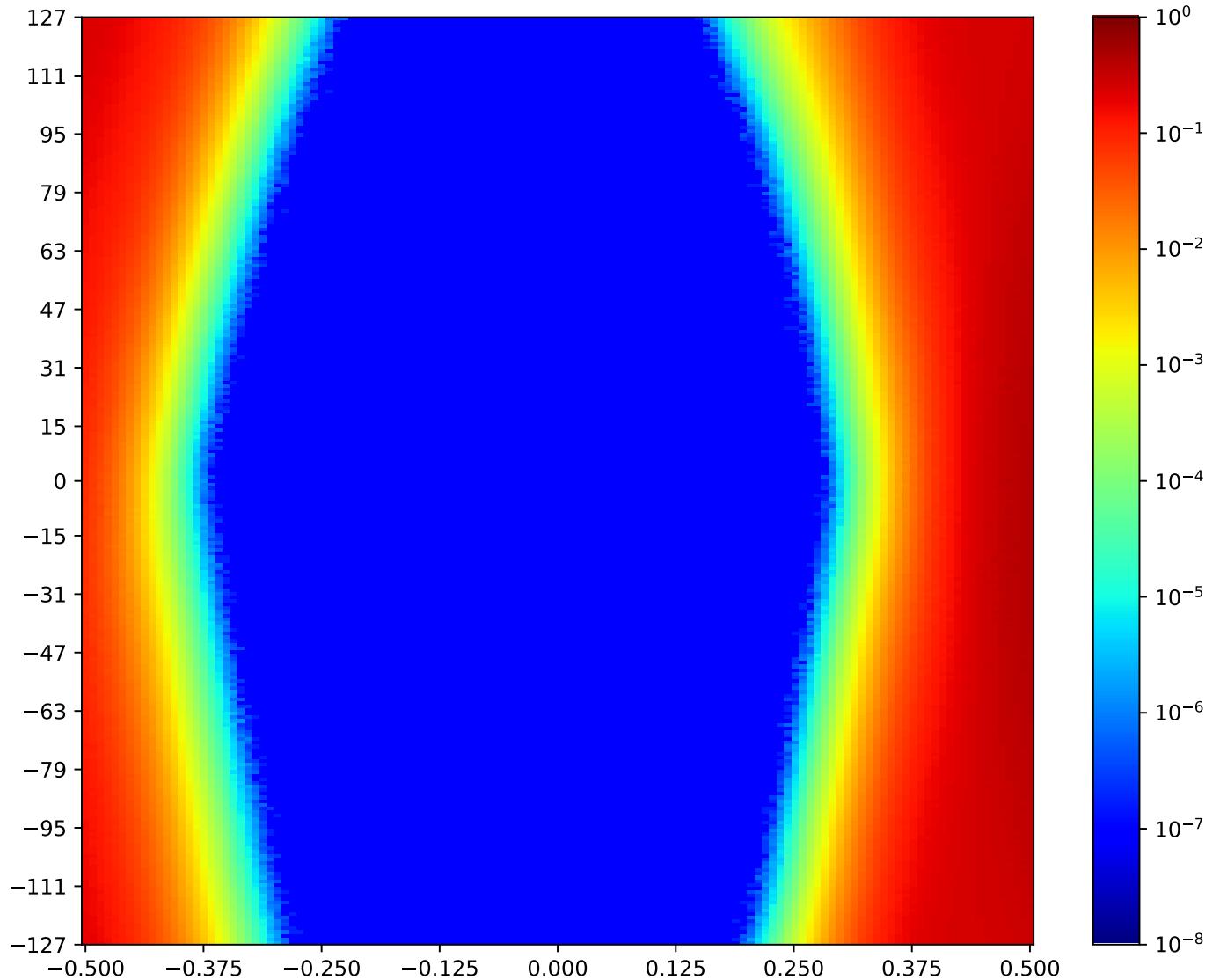


Figure 3.273: MSP\_C\_FPGA-TX3-06-RX4-06-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.8 MSP\_C\_FPGA-TX3-07-RX4-07-MSP\_A\_FPGA

Table 3.253: MSP\_C\_FPGA-TX3-07-RX4-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:56:04		2018-Jan-24 01:56:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16549	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

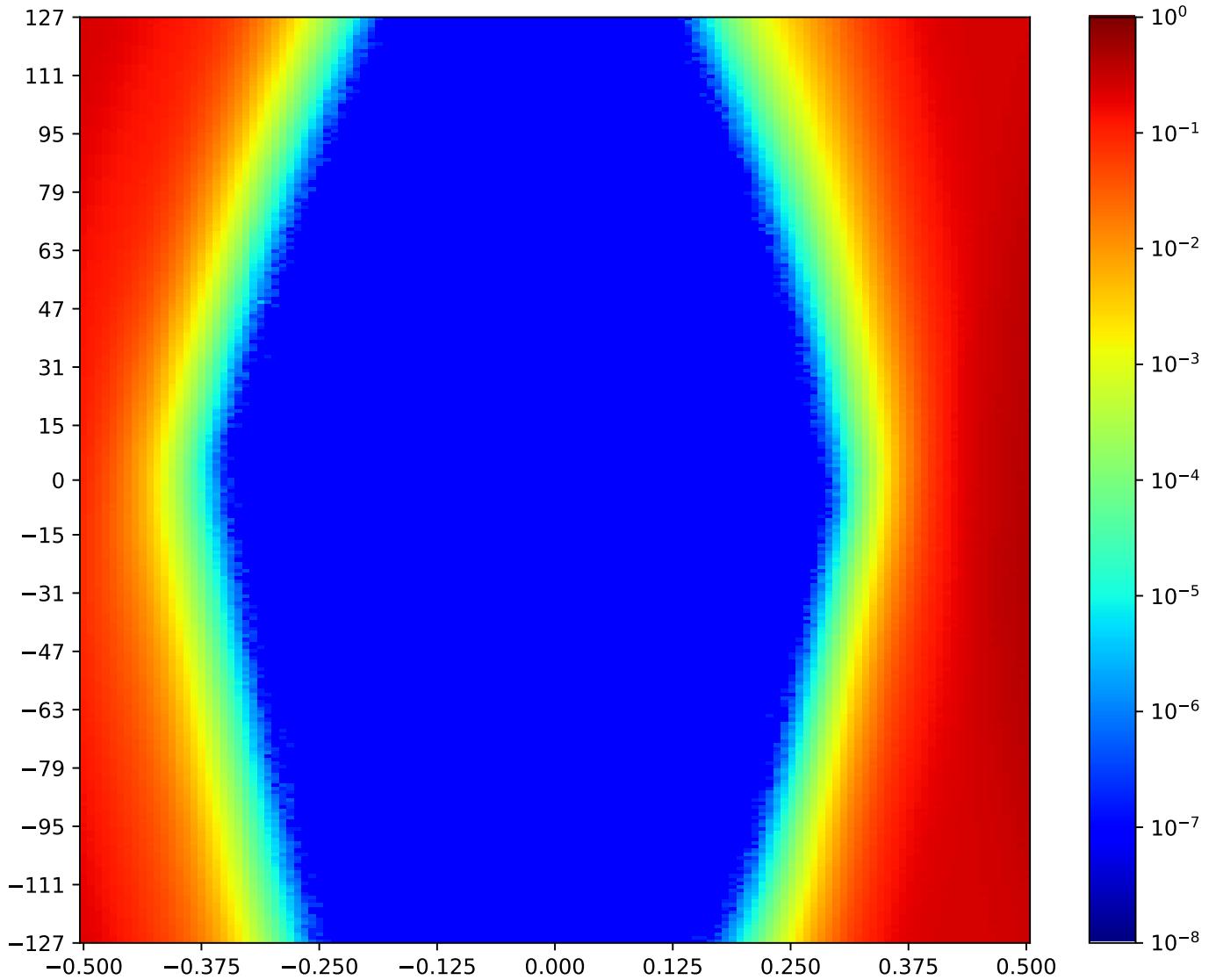


Figure 3.274: MSP\_C\_FPGA-TX3-07-RX4-07-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.9 MSP\_C\_FPGA-TX3-08-RX4-08-MSP\_A\_FPGA

Table 3.254: MSP\_C\_FPGA-TX3-08-RX4-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:01:45		2018-Jan-24 02:02:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17330	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

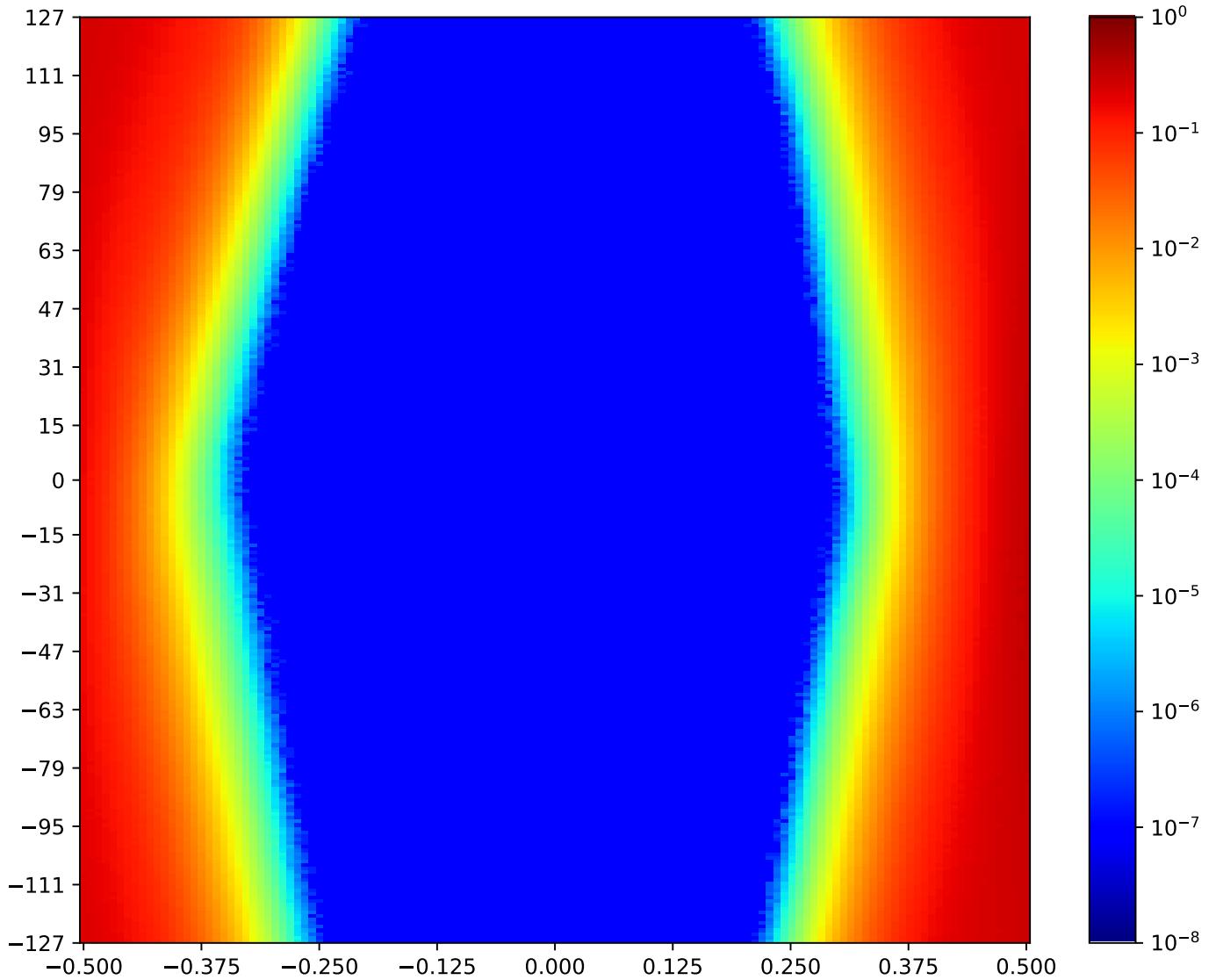


Figure 3.275: MSP\_C\_FPGA-TX3-08-RX4-08-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.10 MSP\_C\_FPGA-TX3-09-RX4-09-MSP\_A\_FPGA

Table 3.255: MSP\_C\_FPGA-TX3-09-RX4-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:57:30		2018-Jan-24 01:58:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17489	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

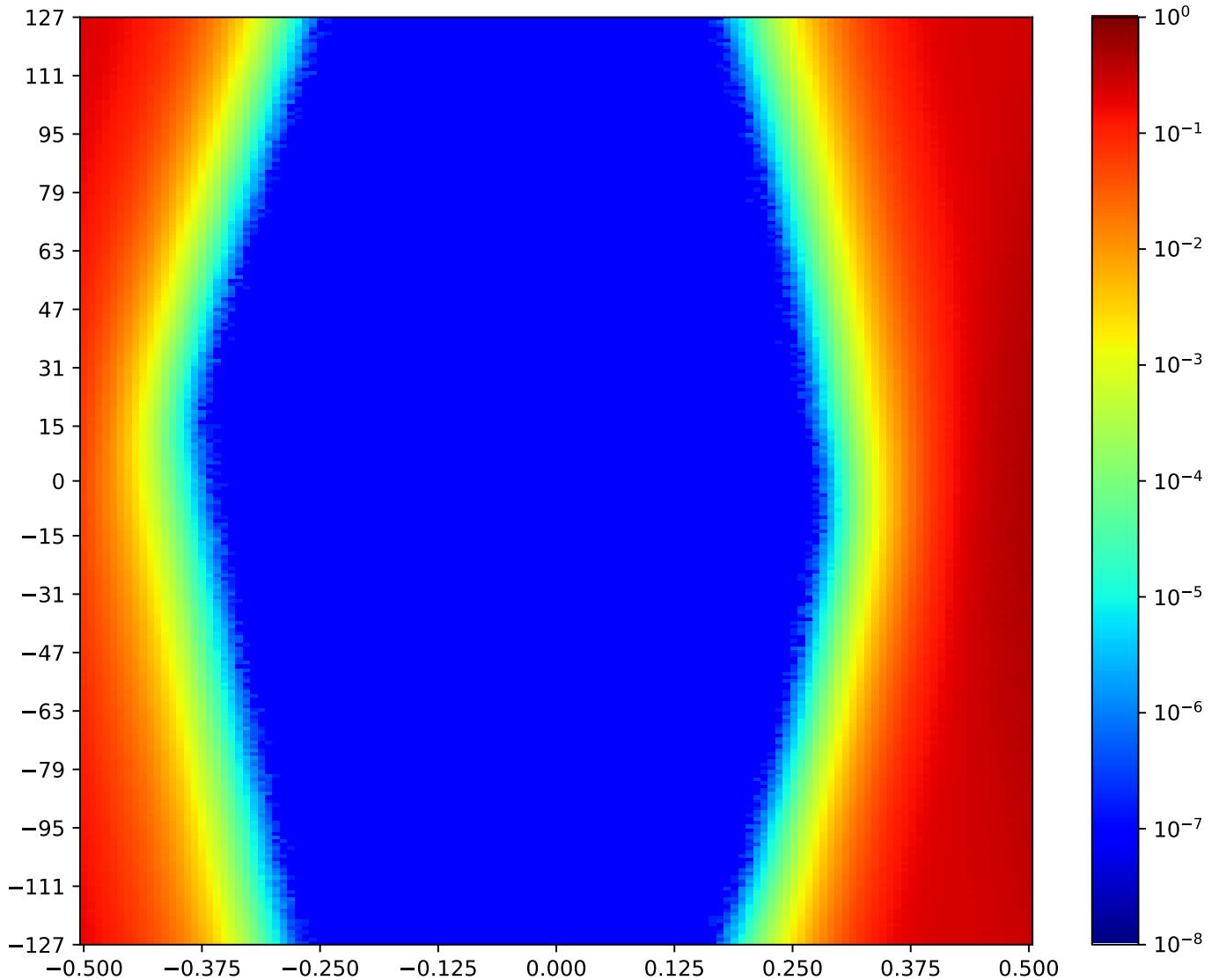


Figure 3.276: MSP\_C\_FPGA-TX3-09-RX4-09-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.11 MSP\_C\_FPGA-TX3-10-RX4-10-MSP\_A\_FPGA

Table 3.256: MSP\_C\_FPGA-TX3-10-RX4-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:00:20		2018-Jan-24 02:01:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16258	75	57.36%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

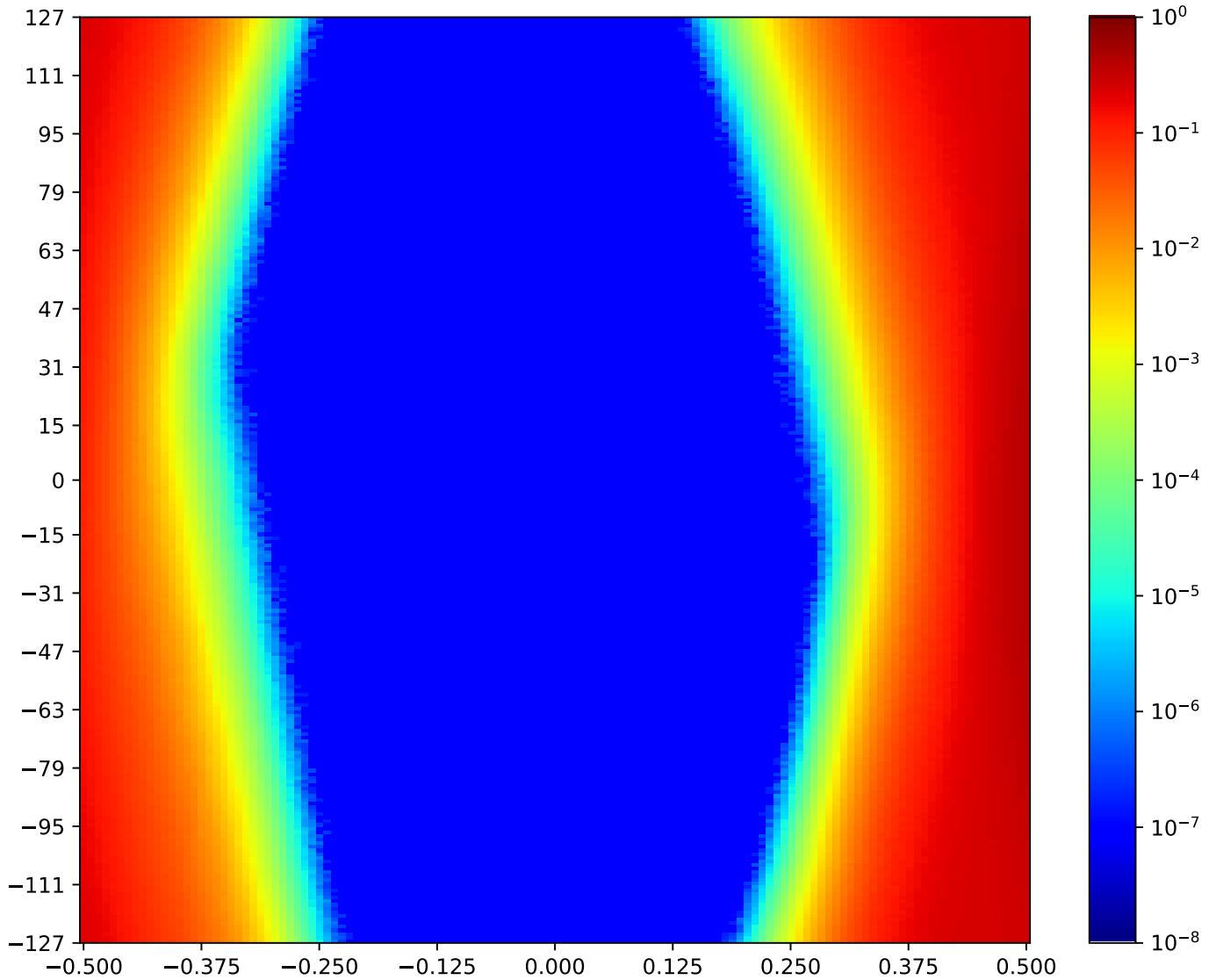


Figure 3.277: MSP\_C\_FPGA-TX3-10-RX4-10-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.21.12 MSP\_C\_FPGA-TX3-11-RX4-11-MSP\_A\_FPGA

Table 3.257: MSP\_C\_FPGA-TX3-11-RX4-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:59:37		2018-Jan-24 02:00:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17379	78	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

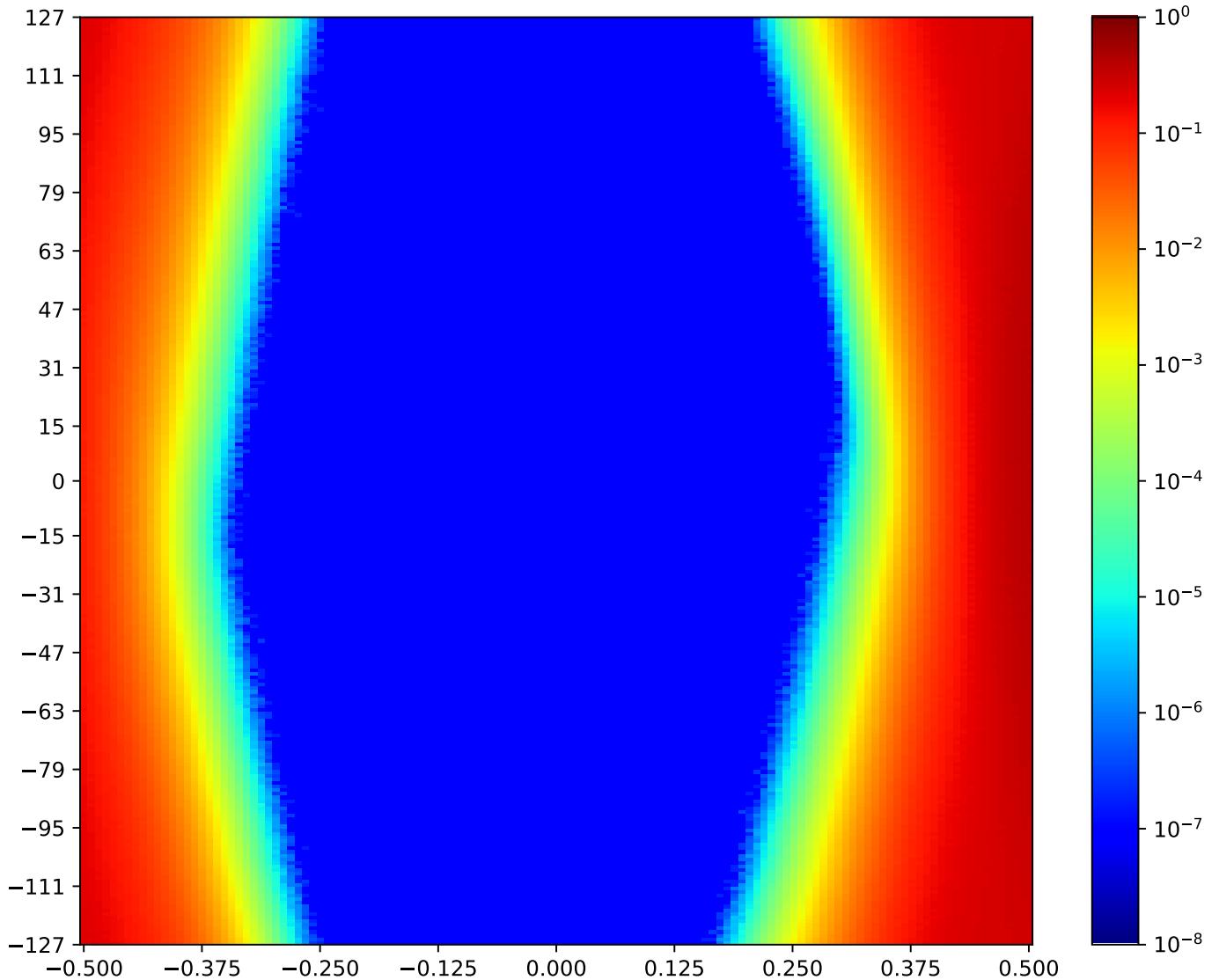


Figure 3.278: MSP\_C\_FPGA-TX3-11-RX4-11-MSP\_A\_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22 MSP\_C TX4 MSP\_A RX3 Minipod Loopback

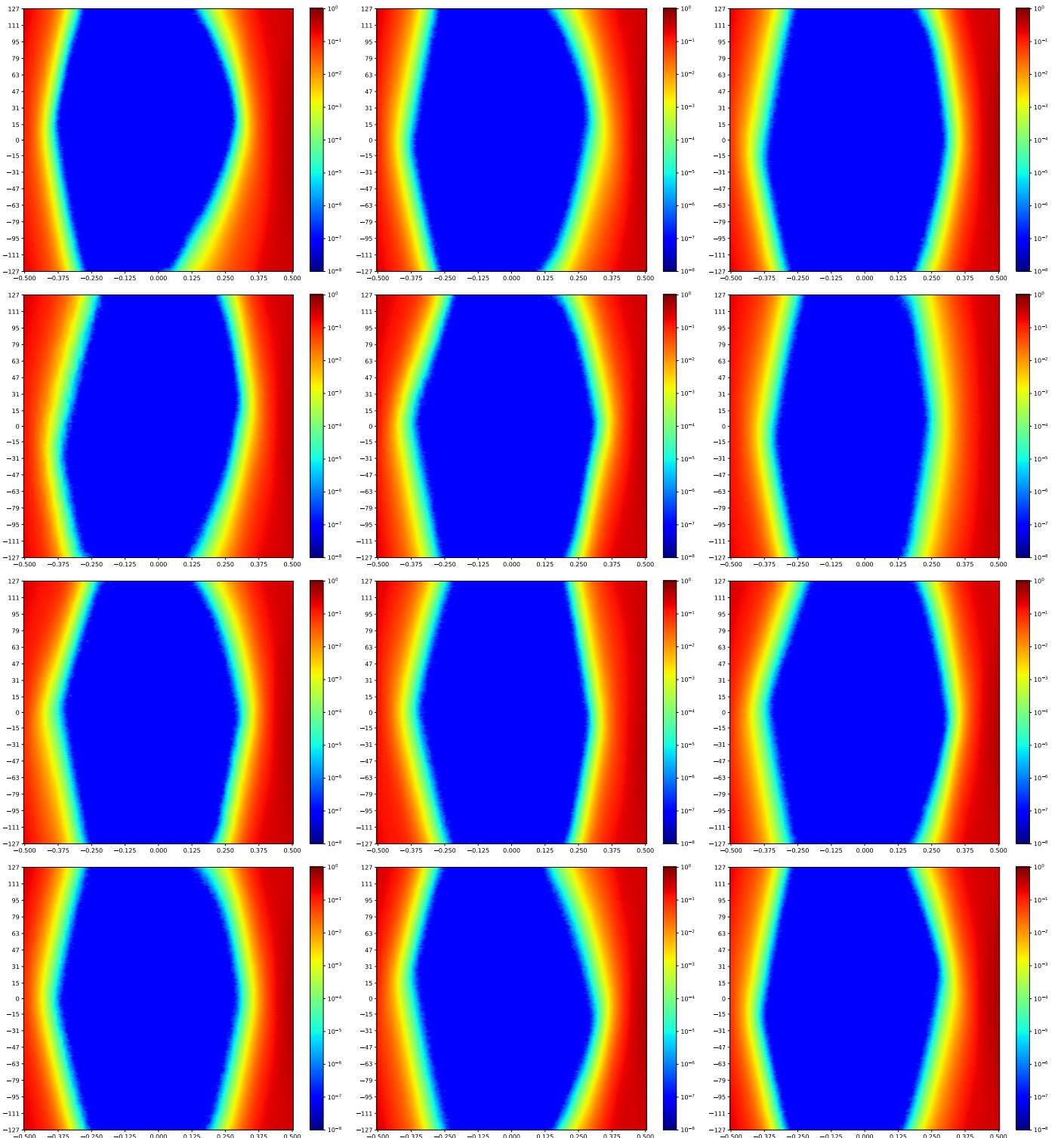


Figure 3.279: MSP\_C TX4 MSP\_A RX3 Minipod Loopback

A cross-reference to Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.  
Next summary Figure 3.279.

### 3.22.1 MSP\_C\_FPGA-TX4-00-RX3-00-MSP\_A\_FPGA

Table 3.258: MSP\_C\_FPGA-TX4-00-RX3-00-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:05:18		2018-Jan-24 02:06:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16722	80	62.02%	254	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

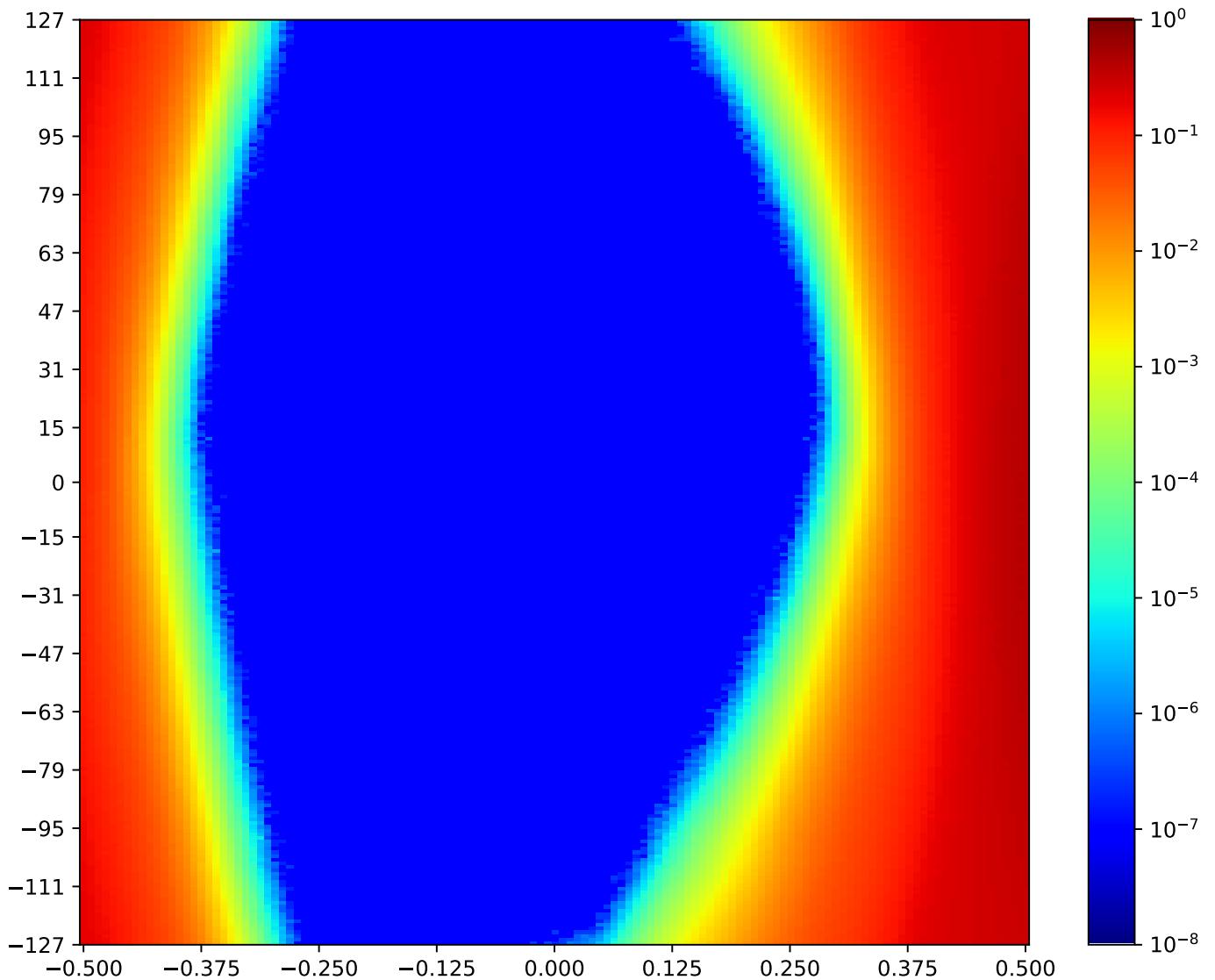


Figure 3.280: MSP\_C\_FPGA-TX4-00-RX3-00-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.2 MSP\_C\_FPGA-TX4-01-RX3-01-MSP\_A\_FPGA

Table 3.259: MSP\_C\_FPGA-TX4-01-RX3-01-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:03:53		2018-Jan-24 02:04:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16727	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

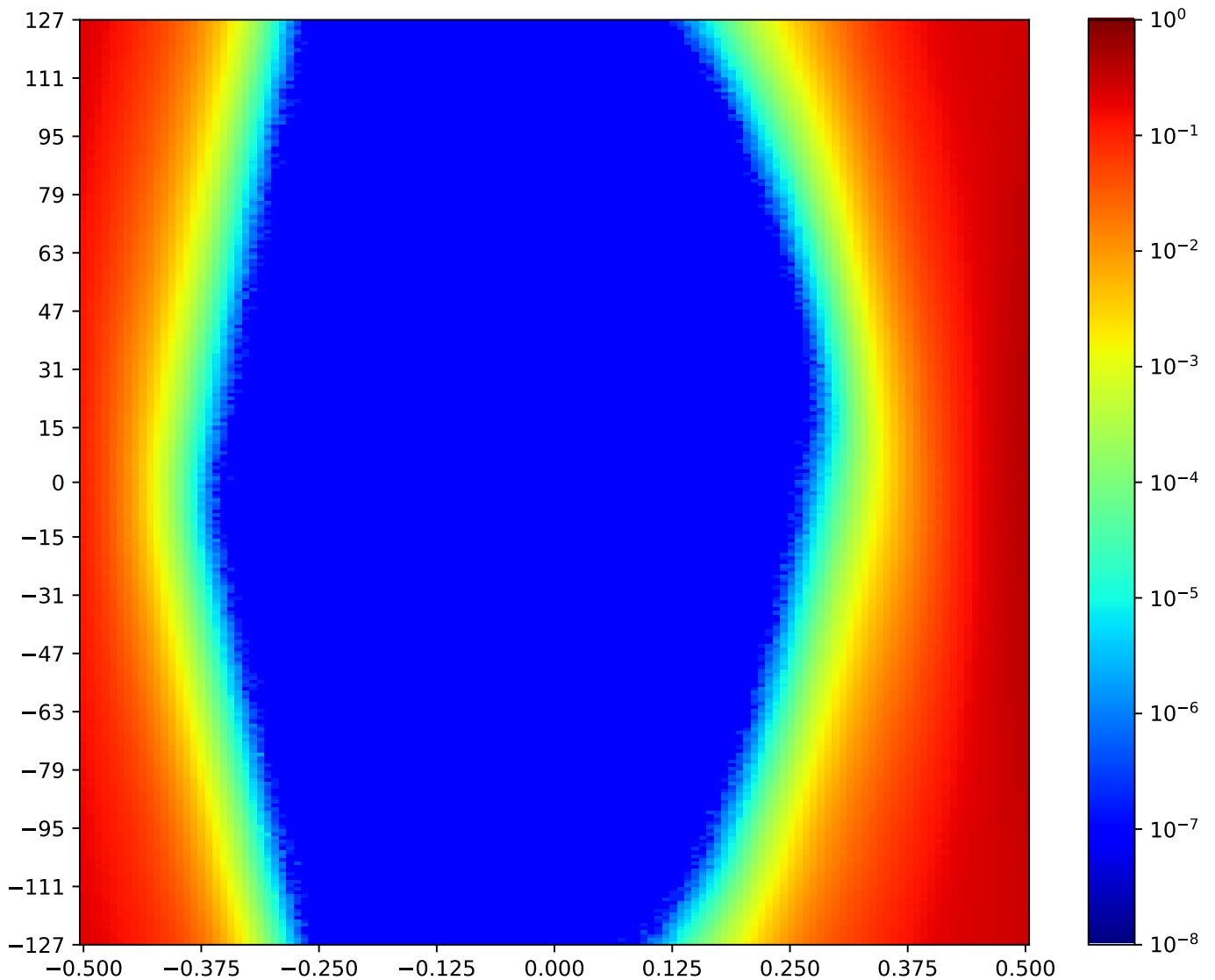


Figure 3.281: MSP\_C\_FPGA-TX4-01-RX3-01-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.3 MSP\_C\_FPGA-TX4-02-RX3-02-MSP\_A\_FPGA

Table 3.260: MSP\_C\_FPGA-TX4-02-RX3-02-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:07:29		2018-Jan-24 02:08:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17942	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

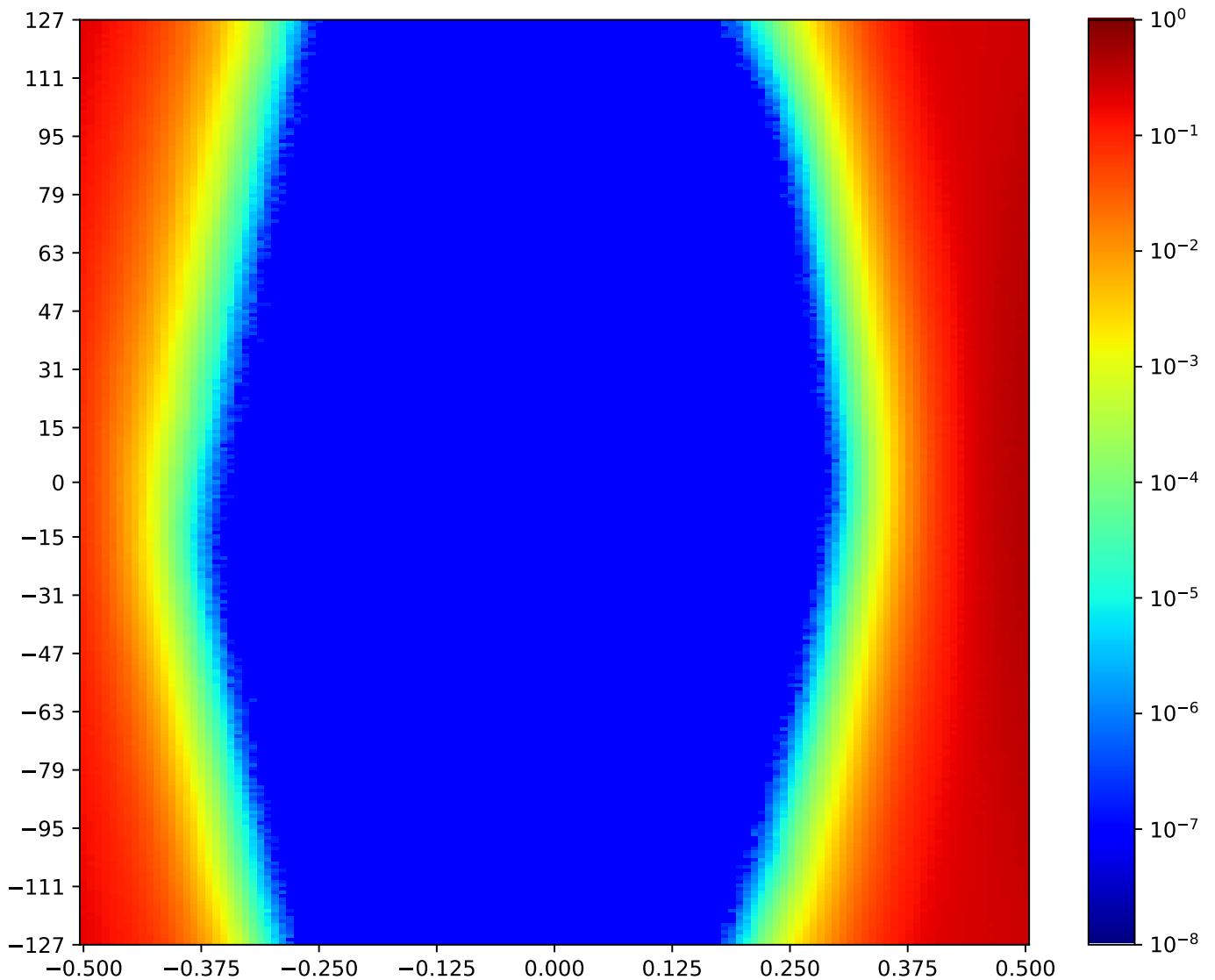


Figure 3.282: MSP\_C\_FPGA-TX4-02-RX3-02-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.4 MSP\_C\_FPGA-TX4-03-RX3-03-MSP\_A\_FPGA

Table 3.261: MSP\_C\_FPGA-TX4-03-RX3-03-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:03:10		2018-Jan-24 02:03:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16756	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

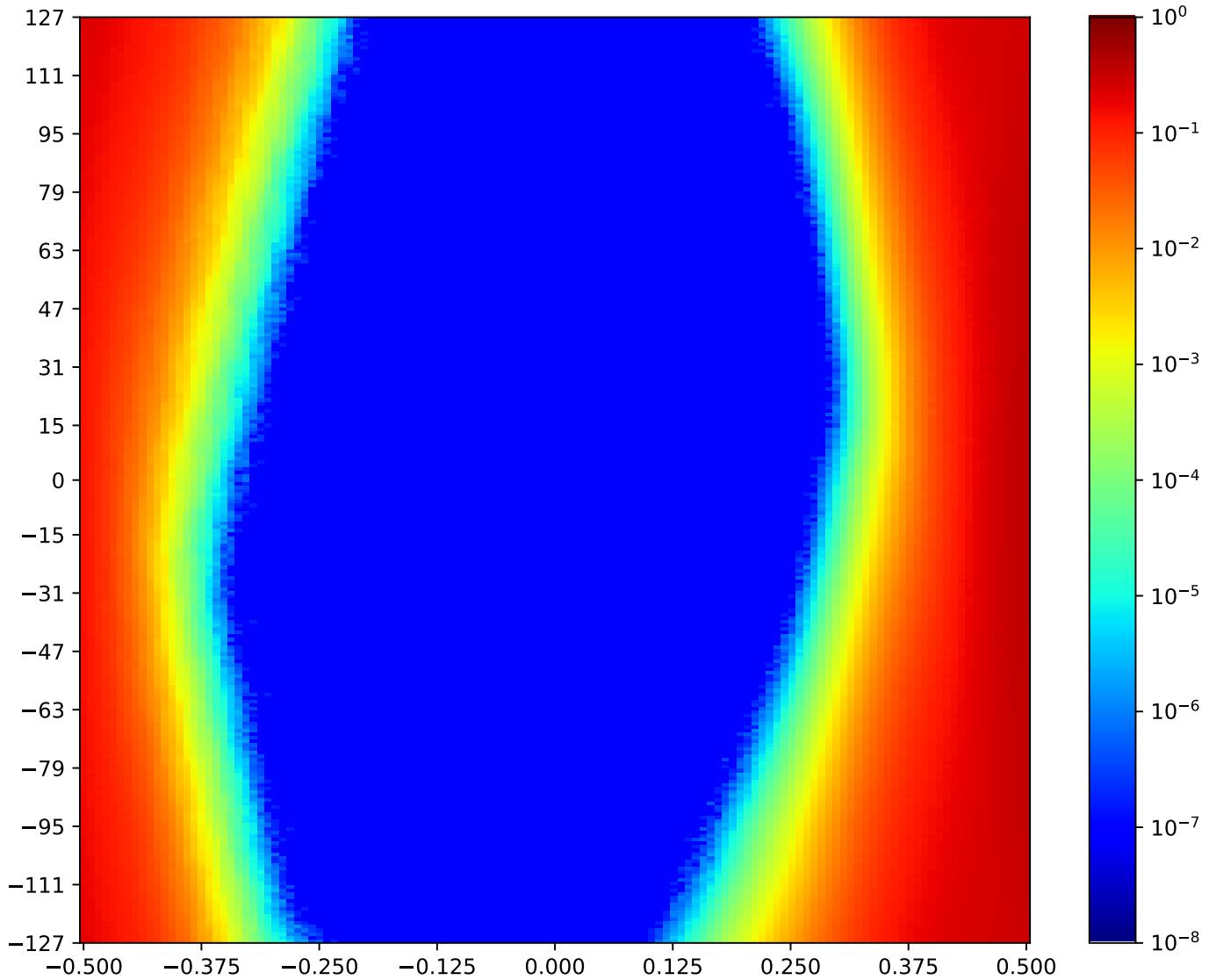


Figure 3.283: MSP\_C\_FPGA-TX4-03-RX3-03-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.5 MSP\_C\_FPGA-TX4-04-RX3-04-MSP\_A\_FPGA

Table 3.262: MSP\_C\_FPGA-TX4-04-RX3-04-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:09:36		2018-Jan-24 02:10:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17150	82	63.57%	254	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

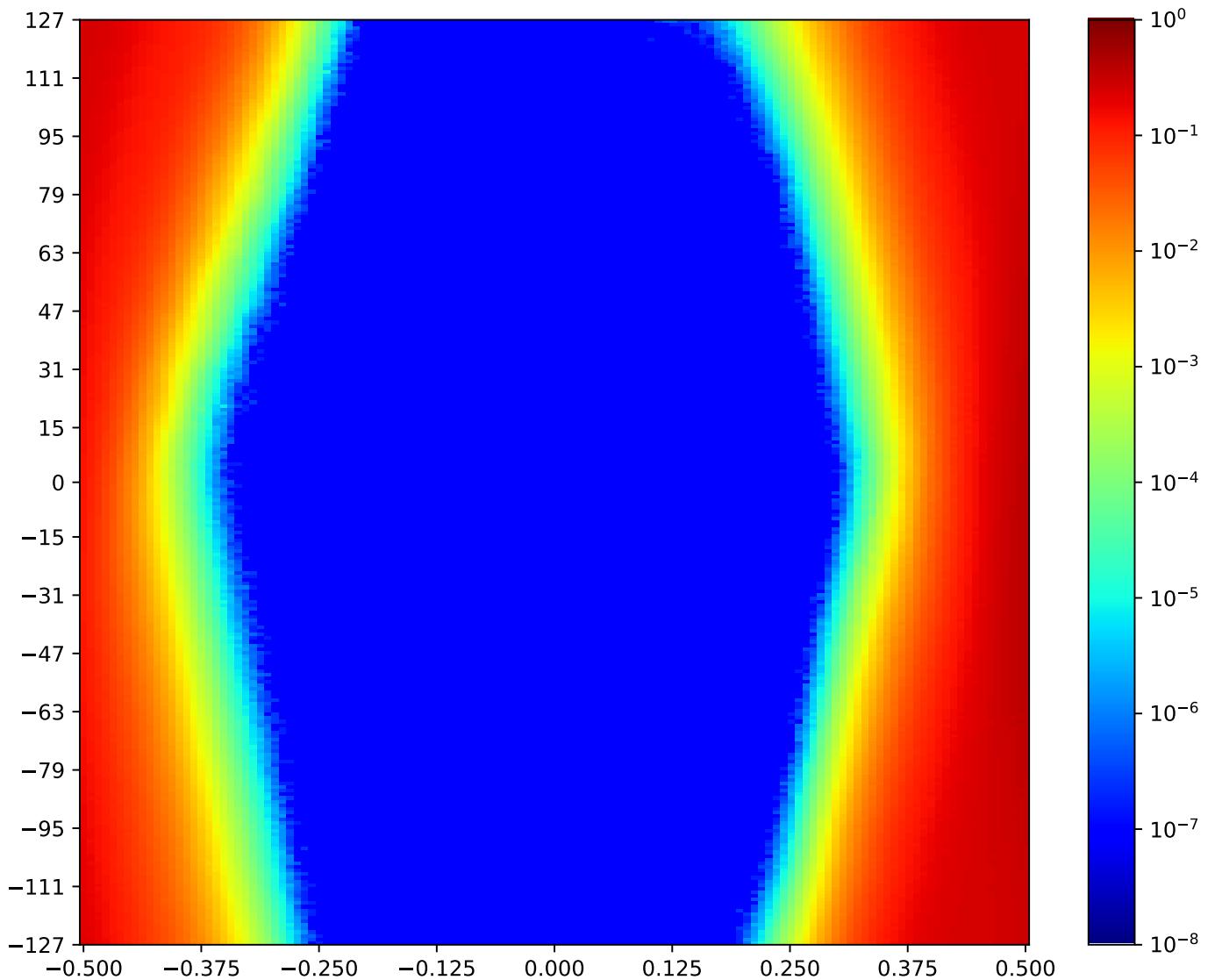


Figure 3.284: MSP\_C\_FPGA-TX4-04-RX3-04-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.6 MSP\_C\_FPGA-TX4-05-RX3-05-MSP\_A\_FPGA

Table 3.263: MSP\_C\_FPGA-TX4-05-RX3-05-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:04:36		2018-Jan-24 02:05:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	14794	68	52.71%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

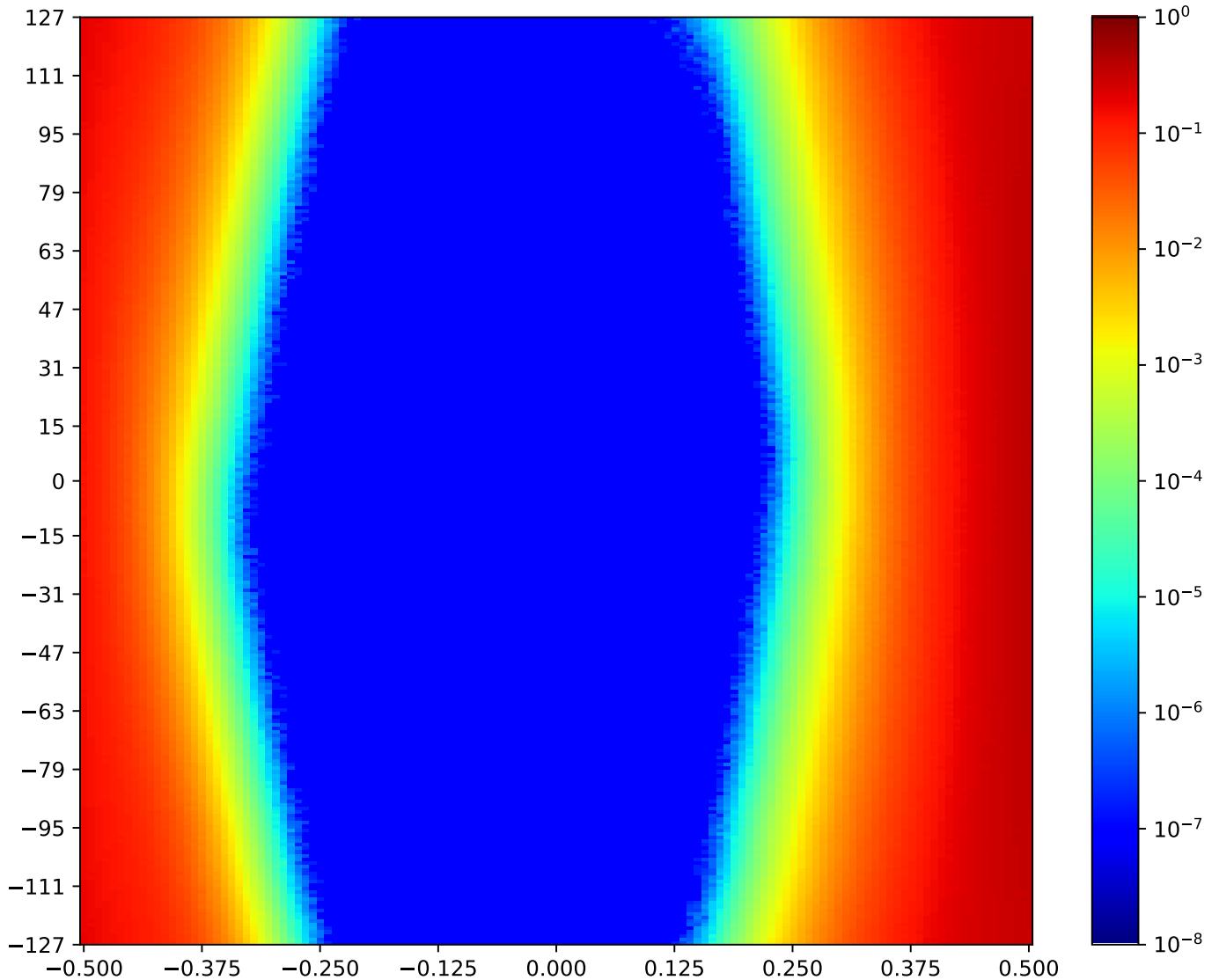


Figure 3.285: MSP\_C\_FPGA-TX4-05-RX3-05-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.7 MSP\_C\_FPGA-TX4-06-RX3-06-MSP\_A\_FPGA

Table 3.264: MSP\_C\_FPGA-TX4-06-RX3-06-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:11:01		2018-Jan-24 02:11:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16823	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

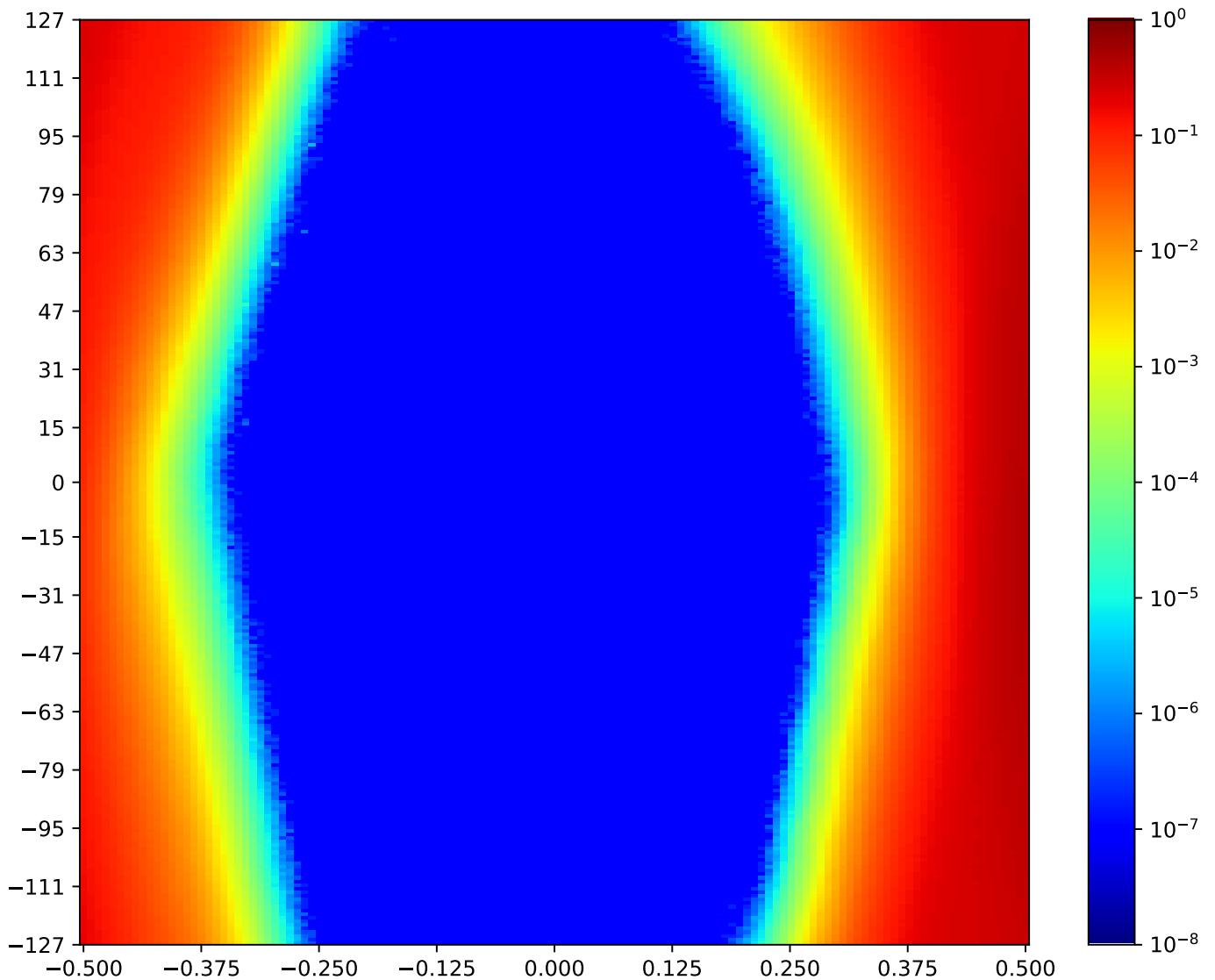


Figure 3.286: MSP\_C\_FPGA-TX4-06-RX3-06-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.8 MSP\_C\_FPGA-TX4-07-RX3-07-MSP\_A\_FPGA

Table 3.265: MSP\_C\_FPGA-TX4-07-RX3-07-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:06:01		2018-Jan-24 02:06:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16527	75	58.14%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

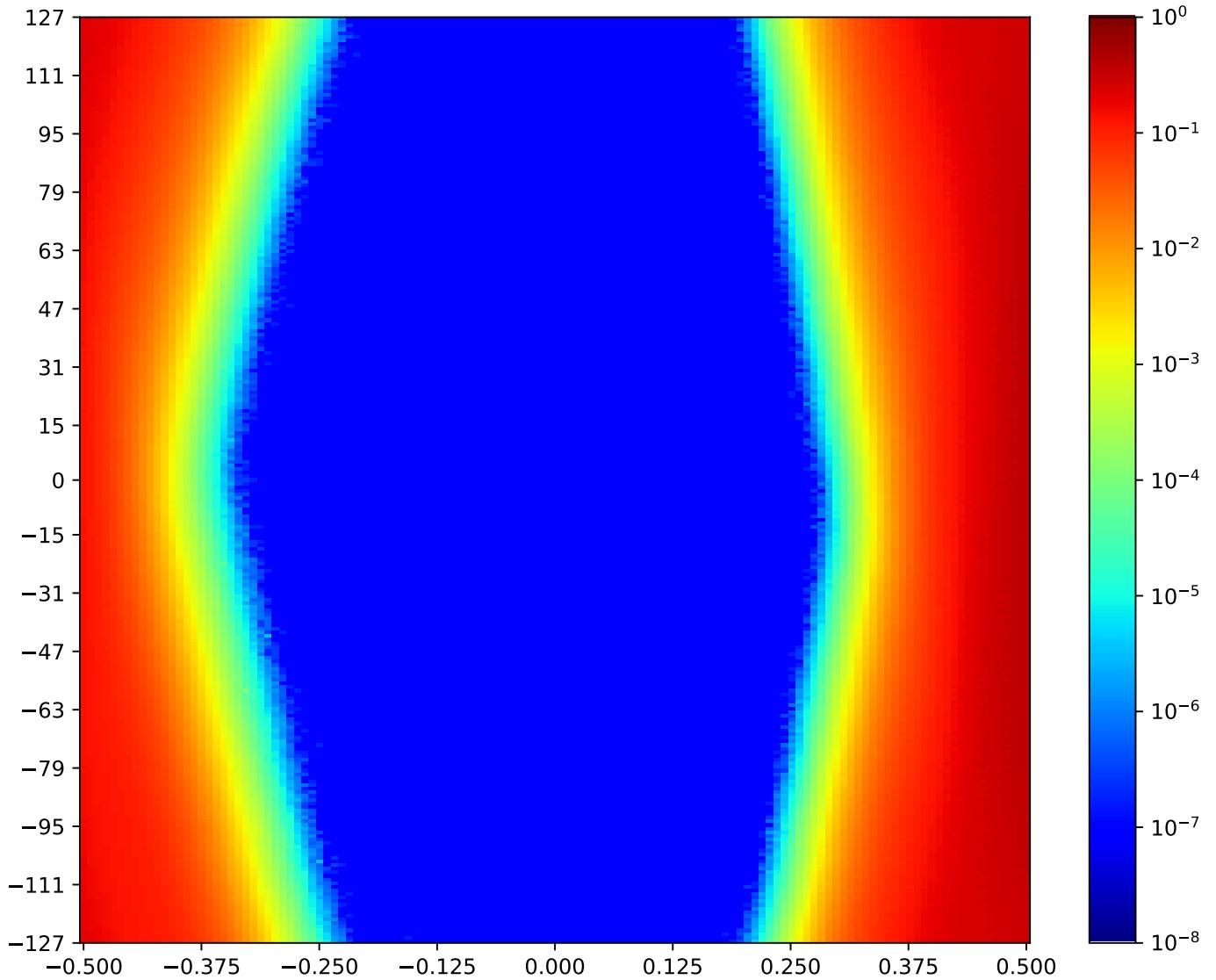


Figure 3.287: MSP\_C\_FPGA-TX4-07-RX3-07-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.9 MSP\_C\_FPGA-TX4-08-RX3-08-MSP\_A\_FPGA

Table 3.266: MSP\_C\_FPGA-TX4-08-RX3-08-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:10:19		2018-Jan-24 02:11:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17015	81	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

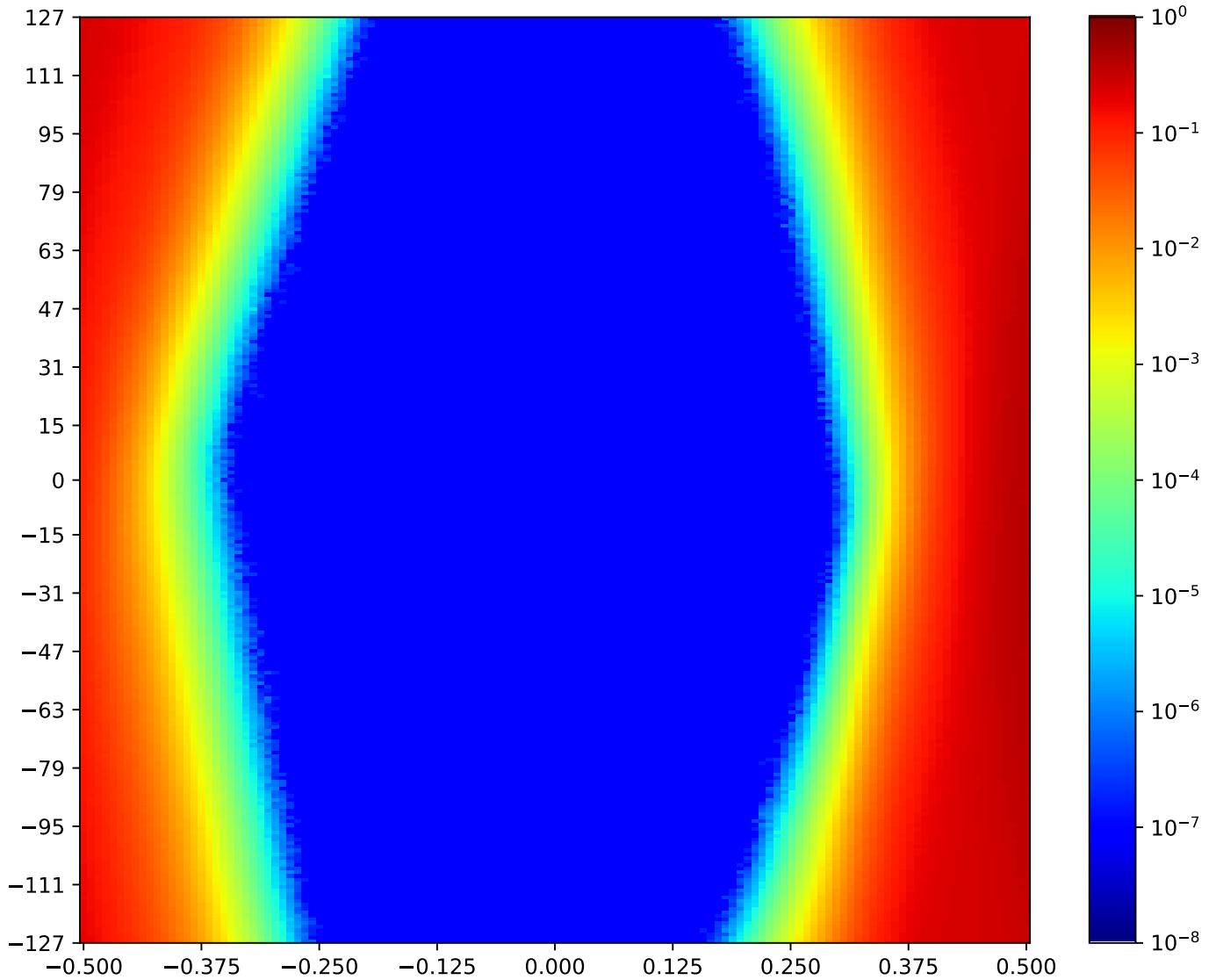


Figure 3.288: MSP\_C\_FPGA-TX4-08-RX3-08-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.10 MSP\_C\_FPGA-TX4-09-RX3-09-MSP\_A\_FPGA

Table 3.267: MSP\_C\_FPGA-TX4-09-RX3-09-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:06:45		2018-Jan-24 02:07:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17443	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

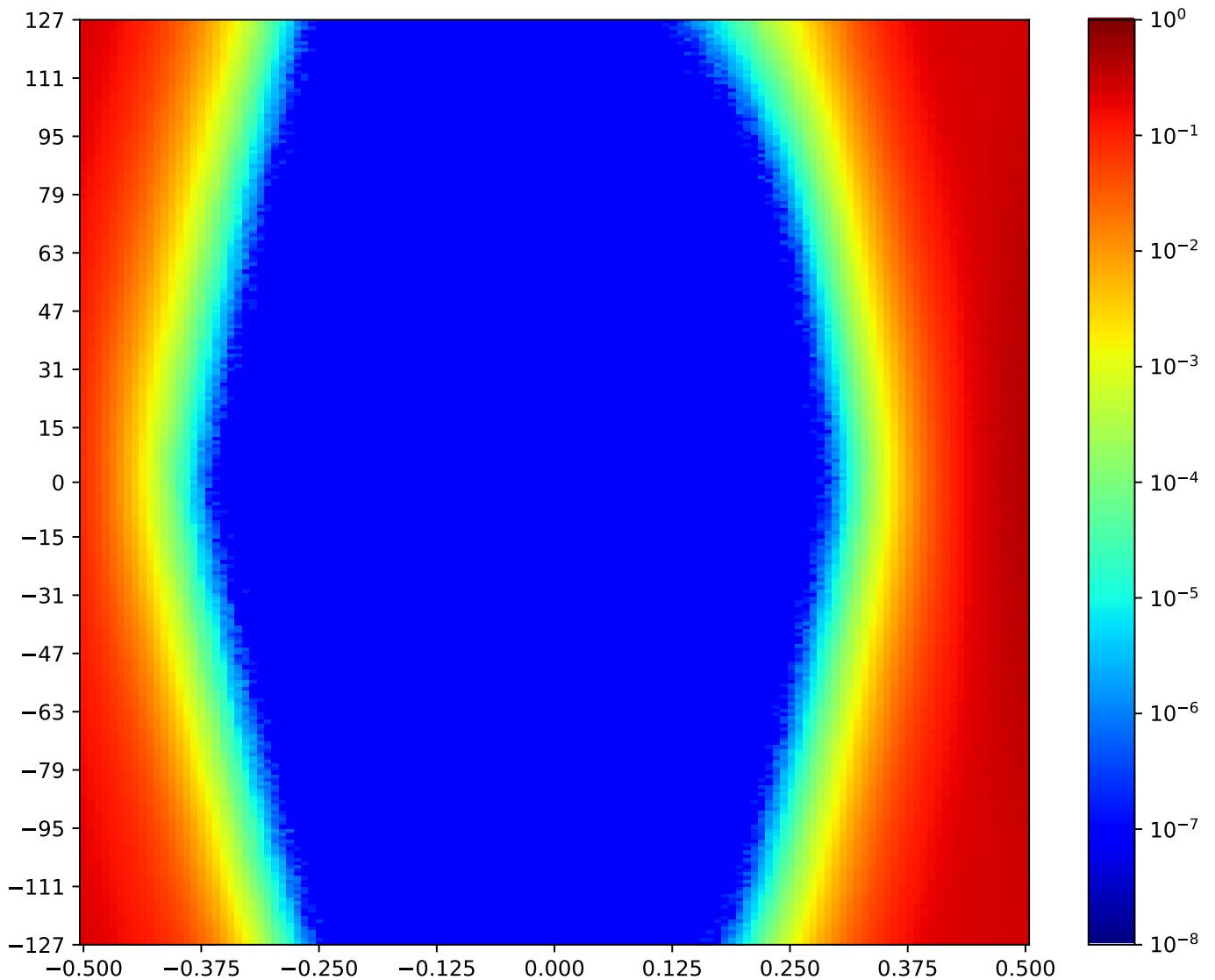


Figure 3.289: MSP\_C\_FPGA-TX4-09-RX3-09-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.11 MSP\_C\_FPGA-TX4-10-RX3-10-MSP\_A\_FPGA

Table 3.268: MSP\_C\_FPGA-TX4-10-RX3-10-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:08:54		2018-Jan-24 02:09:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16654	79	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

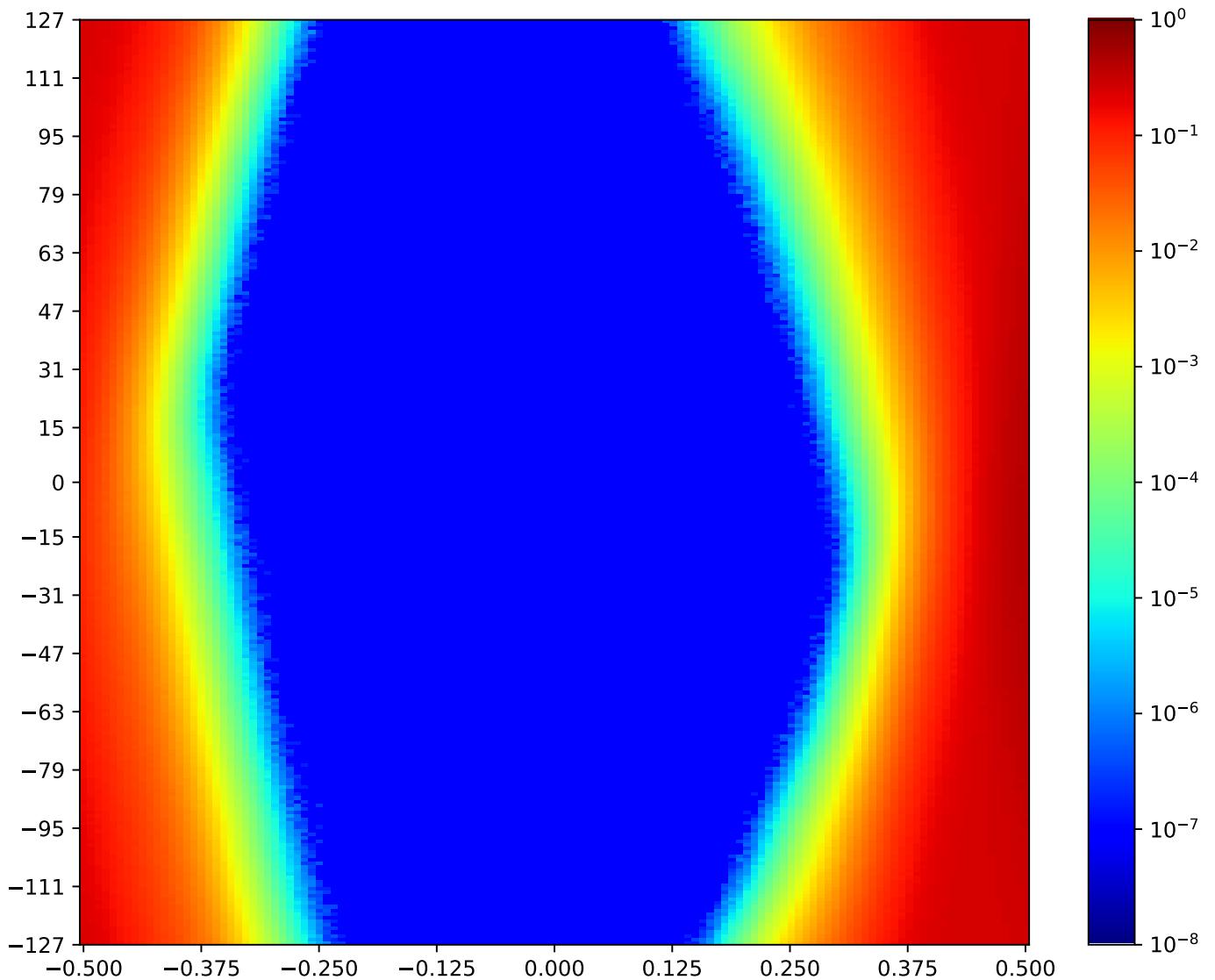


Figure 3.290: MSP\_C\_FPGA-TX4-10-RX3-10-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.

### 3.22.12 MSP\_C\_FPGA-TX4-11-RX3-11-MSP\_A\_FPGA

Table 3.269: MSP\_C\_FPGA-TX4-11-RX3-11-MSP\_A\_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:08:11		2018-Jan-24 02:08:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17251	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

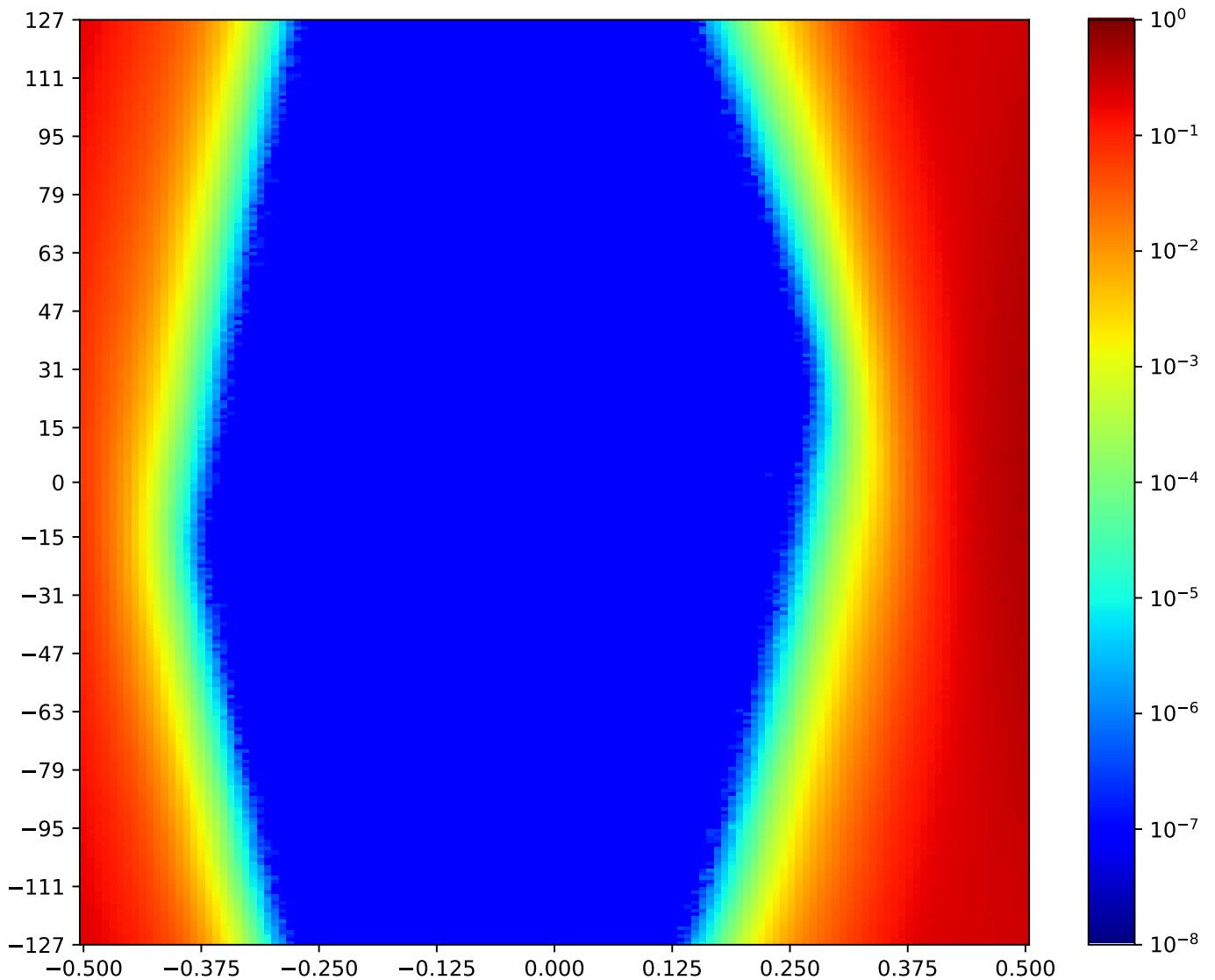


Figure 3.291: MSP\_C\_FPGA-TX4-11-RX3-11-MSP\_A\_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: 6.4-optimized, 9.6-optimized.