

ATLAS MUCTPI
Serial Link Test Report
October 15, 2018

M.V. Silva Oliveira
CERN
EP-ESE-BE
marcos.oliveira@cern.ch

Contents

1	Initial Considerations	20
1.1	Eye diagram mask	20
2	MUCTPI V1 6.4 Gbps	21
2.1	MSP_A TX1 MSP_C RX16 Minipod Loopback	22
2.1.1	MSP_A_FPGA-TX1-00-RX16-00-MSP_C_FPGA	23
2.1.2	MSP_A_FPGA-TX1-01-RX16-01-MSP_C_FPGA	24
2.1.3	MSP_A_FPGA-TX1-02-RX16-02-MSP_C_FPGA	25
2.1.4	MSP_A_FPGA-TX1-03-RX16-03-MSP_C_FPGA	26
2.1.5	MSP_A_FPGA-TX1-04-RX16-04-MSP_C_FPGA	27
2.1.6	MSP_A_FPGA-TX1-05-RX16-05-MSP_C_FPGA	28
2.1.7	MSP_A_FPGA-TX1-06-RX16-06-MSP_C_FPGA	29
2.1.8	MSP_A_FPGA-TX1-07-RX16-07-MSP_C_FPGA	30
2.1.9	MSP_A_FPGA-TX1-08-RX16-08-MSP_C_FPGA	31
2.1.10	MSP_A_FPGA-TX1-09-RX16-09-MSP_C_FPGA	32
2.1.11	MSP_A_FPGA-TX1-10-RX16-10-MSP_C_FPGA	33
2.1.12	MSP_A_FPGA-TX1-11-RX16-11-MSP_C_FPGA	34
2.2	MSP_A TX2 MSP_C RX15 Minipod Loopback	35
2.2.1	MSP_A_FPGA-TX2-00-RX15-00-MSP_C_FPGA	36
2.2.2	MSP_A_FPGA-TX2-01-RX15-01-MSP_C_FPGA	37
2.2.3	MSP_A_FPGA-TX2-02-RX15-02-MSP_C_FPGA	38
2.2.4	MSP_A_FPGA-TX2-03-RX15-03-MSP_C_FPGA	39
2.2.5	MSP_A_FPGA-TX2-04-RX15-04-MSP_C_FPGA	40
2.2.6	MSP_A_FPGA-TX2-05-RX15-05-MSP_C_FPGA	41
2.2.7	MSP_A_FPGA-TX2-06-RX15-06-MSP_C_FPGA	42
2.2.8	MSP_A_FPGA-TX2-07-RX15-07-MSP_C_FPGA	43
2.2.9	MSP_A_FPGA-TX2-08-RX15-08-MSP_C_FPGA	44
2.2.10	MSP_A_FPGA-TX2-09-RX15-09-MSP_C_FPGA	45
2.2.11	MSP_A_FPGA-TX2-10-RX15-10-MSP_C_FPGA	46
2.2.12	MSP_A_FPGA-TX2-11-RX15-11-MSP_C_FPGA	47
2.3	MSP_C TX3 MSP_A RX7 Minipod Loopback	48
2.3.1	MSP_C_FPGA-TX3-00-RX7-00-MSP_A_FPGA	49
2.3.2	MSP_C_FPGA-TX3-01-RX7-01-MSP_A_FPGA	50
2.3.3	MSP_C_FPGA-TX3-02-RX7-02-MSP_A_FPGA	51
2.3.4	MSP_C_FPGA-TX3-03-RX7-03-MSP_A_FPGA	52
2.3.5	MSP_C_FPGA-TX3-04-RX7-04-MSP_A_FPGA	53
2.3.6	MSP_C_FPGA-TX3-05-RX7-05-MSP_A_FPGA	54
2.3.7	MSP_C_FPGA-TX3-06-RX7-06-MSP_A_FPGA	55
2.3.8	MSP_C_FPGA-TX3-07-RX7-07-MSP_A_FPGA	56
2.3.9	MSP_C_FPGA-TX3-08-RX7-08-MSP_A_FPGA	57
2.3.10	MSP_C_FPGA-TX3-09-RX7-09-MSP_A_FPGA	58
2.3.11	MSP_C_FPGA-TX3-10-RX7-10-MSP_A_FPGA	59
2.3.12	MSP_C_FPGA-TX3-11-RX7-11-MSP_A_FPGA	60
2.4	MSP_C TX4 MSP_A RX6 Minipod Loopback	61
2.4.1	MSP_C_FPGA-TX4-00-RX6-00-MSP_A_FPGA	62
2.4.2	MSP_C_FPGA-TX4-01-RX6-01-MSP_A_FPGA	63
2.4.3	MSP_C_FPGA-TX4-02-RX6-02-MSP_A_FPGA	64
2.4.4	MSP_C_FPGA-TX4-03-RX6-03-MSP_A_FPGA	65
2.4.5	MSP_C_FPGA-TX4-04-RX6-04-MSP_A_FPGA	66
2.4.6	MSP_C_FPGA-TX4-05-RX6-05-MSP_A_FPGA	67
2.4.7	MSP_C_FPGA-TX4-06-RX6-06-MSP_A_FPGA	68
2.4.8	MSP_C_FPGA-TX4-07-RX6-07-MSP_A_FPGA	69

2.4.9	MSP_C_FPGA-TX4-08-RX6-08-MSP_A_FPGA	70
2.4.10	MSP_C_FPGA-TX4-09-RX6-09-MSP_A_FPGA	71
2.4.11	MSP_C_FPGA-TX4-10-RX6-10-MSP_A_FPGA	72
2.4.12	MSP_C_FPGA-TX4-11-RX6-11-MSP_A_FPGA	73
2.5	Partial TRP TX5 MSP_A RX5 Minipod Loopback	74
2.5.1	TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA	76
2.5.2	TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA	77
2.5.3	TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA	78
2.5.4	TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA	79
2.5.5	TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA	80
2.5.6	TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA	81
2.5.7	TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA	82
2.5.8	TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA	83
2.6	TRP J1 QSFP Loopback	84
2.6.1	TRP_FPGA-J1-00-J1-00-TRP_FPGA	85
2.6.2	TRP_FPGA-J1-01-J1-01-TRP_FPGA	86
2.6.3	TRP_FPGA-J1-02-J1-02-TRP_FPGA	87
2.6.4	TRP_FPGA-J1-03-J1-03-TRP_FPGA	88
2.7	TRP J3 SFP Loopback	89
2.7.1	TRP_FPGA-J3-00-J3-00-TRP_FPGA	90
2.8	MSP_A TRP On board links	91
2.8.1	MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA	93
2.8.2	MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA	94
2.8.3	MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA	95
2.8.4	MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA	96
2.8.5	MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA	97
2.8.6	MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA	98
2.8.7	MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA	99
2.8.8	MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA	100
2.8.9	MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA	101
2.8.10	MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA	102
2.8.11	MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA	103
2.8.12	MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA	104
2.8.13	MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA	105
2.8.14	MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA	106
2.8.15	MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA	107
2.8.16	MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA	108
2.8.17	MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA	109
2.8.18	MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA	110
2.8.19	MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA	111
2.8.20	MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA	112
2.8.21	MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA	113
2.8.22	MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA	114
2.8.23	MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA	115
2.8.24	MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA	116
2.8.25	MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA	117
2.8.26	MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA	118
2.8.27	MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA	119
2.8.28	MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA	120
2.9	MSP_C TRP On board links	121
2.9.1	MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA	123
2.9.2	MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA	124
2.9.3	MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA	125
2.9.4	MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA	126
2.9.5	MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA	127
2.9.6	MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA	128
2.9.7	MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA	129
2.9.8	MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA	130
2.9.9	MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA	131
2.9.10	MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA	132
2.9.11	MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA	133
2.9.12	MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA	134
2.9.13	MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA	135
2.9.14	MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA	136

2.9.15	MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA	137
2.9.16	MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA	138
2.9.17	MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA	139
2.9.18	MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA	140
2.9.19	MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA	141
2.9.20	MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA	142
2.9.21	MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA	143
2.9.22	MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA	144
2.9.23	MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA	145
2.9.24	MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA	146
2.9.25	MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA	147
2.9.26	MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA	148
2.9.27	MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA	149
2.9.28	MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA	150
2.10	MSP_A_TX1 MSP_C_RX18 Minipod Loopback	151
2.10.1	MSP_A_FPGA-TX1-00-RX18-00-MSP_C_FPGA	152
2.10.2	MSP_A_FPGA-TX1-01-RX18-01-MSP_C_FPGA	153
2.10.3	MSP_A_FPGA-TX1-02-RX18-02-MSP_C_FPGA	154
2.10.4	MSP_A_FPGA-TX1-03-RX18-03-MSP_C_FPGA	155
2.10.5	MSP_A_FPGA-TX1-04-RX18-04-MSP_C_FPGA	156
2.10.6	MSP_A_FPGA-TX1-05-RX18-05-MSP_C_FPGA	157
2.10.7	MSP_A_FPGA-TX1-06-RX18-06-MSP_C_FPGA	158
2.10.8	MSP_A_FPGA-TX1-07-RX18-07-MSP_C_FPGA	159
2.10.9	MSP_A_FPGA-TX1-08-RX18-08-MSP_C_FPGA	160
2.10.10	MSP_A_FPGA-TX1-09-RX18-09-MSP_C_FPGA	161
2.10.11	MSP_A_FPGA-TX1-10-RX18-10-MSP_C_FPGA	162
2.10.12	MSP_A_FPGA-TX1-11-RX18-11-MSP_C_FPGA	163
2.11	MSP_A_TX2 MSP_C_RX17 Minipod Loopback	164
2.11.1	MSP_A_FPGA-TX2-00-RX17-00-MSP_C_FPGA	165
2.11.2	MSP_A_FPGA-TX2-01-RX17-01-MSP_C_FPGA	166
2.11.3	MSP_A_FPGA-TX2-02-RX17-02-MSP_C_FPGA	167
2.11.4	MSP_A_FPGA-TX2-03-RX17-03-MSP_C_FPGA	168
2.11.5	MSP_A_FPGA-TX2-04-RX17-04-MSP_C_FPGA	169
2.11.6	MSP_A_FPGA-TX2-05-RX17-05-MSP_C_FPGA	170
2.11.7	MSP_A_FPGA-TX2-06-RX17-06-MSP_C_FPGA	171
2.11.8	MSP_A_FPGA-TX2-07-RX17-07-MSP_C_FPGA	172
2.11.9	MSP_A_FPGA-TX2-08-RX17-08-MSP_C_FPGA	173
2.11.10	MSP_A_FPGA-TX2-09-RX17-09-MSP_C_FPGA	174
2.11.11	MSP_A_FPGA-TX2-10-RX17-10-MSP_C_FPGA	175
2.11.12	MSP_A_FPGA-TX2-11-RX17-11-MSP_C_FPGA	176
2.12	MSP_C_TX3 MSP_A_RX9 Minipod Loopback	177
2.12.1	MSP_C_FPGA-TX3-00-RX9-00-MSP_A_FPGA	178
2.12.2	MSP_C_FPGA-TX3-01-RX9-01-MSP_A_FPGA	179
2.12.3	MSP_C_FPGA-TX3-02-RX9-02-MSP_A_FPGA	180
2.12.4	MSP_C_FPGA-TX3-03-RX9-03-MSP_A_FPGA	181
2.12.5	MSP_C_FPGA-TX3-04-RX9-04-MSP_A_FPGA	182
2.12.6	MSP_C_FPGA-TX3-05-RX9-05-MSP_A_FPGA	183
2.12.7	MSP_C_FPGA-TX3-06-RX9-06-MSP_A_FPGA	184
2.12.8	MSP_C_FPGA-TX3-07-RX9-07-MSP_A_FPGA	185
2.12.9	MSP_C_FPGA-TX3-08-RX9-08-MSP_A_FPGA	186
2.12.10	MSP_C_FPGA-TX3-09-RX9-09-MSP_A_FPGA	187
2.12.11	MSP_C_FPGA-TX3-10-RX9-10-MSP_A_FPGA	188
2.12.12	MSP_C_FPGA-TX3-11-RX9-11-MSP_A_FPGA	189
2.13	MSP_C_TX4 MSP_A_RX8 Minipod Loopback	190
2.13.1	MSP_C_FPGA-TX4-00-RX8-00-MSP_A_FPGA	191
2.13.2	MSP_C_FPGA-TX4-01-RX8-01-MSP_A_FPGA	192
2.13.3	MSP_C_FPGA-TX4-02-RX8-02-MSP_A_FPGA	193
2.13.4	MSP_C_FPGA-TX4-03-RX8-03-MSP_A_FPGA	194
2.13.5	MSP_C_FPGA-TX4-04-RX8-04-MSP_A_FPGA	195
2.13.6	MSP_C_FPGA-TX4-05-RX8-05-MSP_A_FPGA	196
2.13.7	MSP_C_FPGA-TX4-06-RX8-06-MSP_A_FPGA	197
2.13.8	MSP_C_FPGA-TX4-07-RX8-07-MSP_A_FPGA	198
2.13.9	MSP_C_FPGA-TX4-08-RX8-08-MSP_A_FPGA	199
2.13.10	MSP_C_FPGA-TX4-09-RX8-09-MSP_A_FPGA	200

2.13.11	MSP_C_FPGA-TX4-10-RX8-10-MSP_A_FPGA	201
2.13.12	MSP_C_FPGA-TX4-11-RX8-11-MSP_A_FPGA	202
2.14	Partial TRP TX5 MSP_C RX14 Minipod Loopback	203
2.14.1	TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA	205
2.14.2	TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA	206
2.14.3	TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA	207
2.14.4	TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA	208
2.14.5	TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA	209
2.14.6	TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA	210
2.14.7	TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA	211
2.14.8	TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA	212
2.15	MSP_A TX1 MSP_C RX11 Minipod Loopback	213
2.15.1	MSP_A_FPGA-TX1-00-RX11-00-MSP_C_FPGA	214
2.15.2	MSP_A_FPGA-TX1-01-RX11-01-MSP_C_FPGA	215
2.15.3	MSP_A_FPGA-TX1-02-RX11-02-MSP_C_FPGA	216
2.15.4	MSP_A_FPGA-TX1-03-RX11-03-MSP_C_FPGA	217
2.15.5	MSP_A_FPGA-TX1-04-RX11-04-MSP_C_FPGA	218
2.15.6	MSP_A_FPGA-TX1-05-RX11-05-MSP_C_FPGA	219
2.15.7	MSP_A_FPGA-TX1-06-RX11-06-MSP_C_FPGA	220
2.15.8	MSP_A_FPGA-TX1-07-RX11-07-MSP_C_FPGA	221
2.15.9	MSP_A_FPGA-TX1-08-RX11-08-MSP_C_FPGA	222
2.15.10	MSP_A_FPGA-TX1-09-RX11-09-MSP_C_FPGA	223
2.15.11	MSP_A_FPGA-TX1-10-RX11-10-MSP_C_FPGA	224
2.15.12	MSP_A_FPGA-TX1-11-RX11-11-MSP_C_FPGA	225
2.16	MSP_A TX2 MSP_C RX10 Minipod Loopback	226
2.16.1	MSP_A_FPGA-TX2-00-RX10-00-MSP_C_FPGA	227
2.16.2	MSP_A_FPGA-TX2-01-RX10-01-MSP_C_FPGA	228
2.16.3	MSP_A_FPGA-TX2-02-RX10-02-MSP_C_FPGA	229
2.16.4	MSP_A_FPGA-TX2-03-RX10-03-MSP_C_FPGA	230
2.16.5	MSP_A_FPGA-TX2-04-RX10-04-MSP_C_FPGA	231
2.16.6	MSP_A_FPGA-TX2-05-RX10-05-MSP_C_FPGA	232
2.16.7	MSP_A_FPGA-TX2-06-RX10-06-MSP_C_FPGA	233
2.16.8	MSP_A_FPGA-TX2-07-RX10-07-MSP_C_FPGA	234
2.16.9	MSP_A_FPGA-TX2-08-RX10-08-MSP_C_FPGA	235
2.16.10	MSP_A_FPGA-TX2-09-RX10-09-MSP_C_FPGA	236
2.16.11	MSP_A_FPGA-TX2-10-RX10-10-MSP_C_FPGA	237
2.16.12	MSP_A_FPGA-TX2-11-RX10-11-MSP_C_FPGA	238
2.17	MSP_C TX3 MSP_A RX2 Minipod Loopback	239
2.17.1	MSP_C_FPGA-TX3-00-RX2-00-MSP_A_FPGA	240
2.17.2	MSP_C_FPGA-TX3-01-RX2-01-MSP_A_FPGA	241
2.17.3	MSP_C_FPGA-TX3-02-RX2-02-MSP_A_FPGA	242
2.17.4	MSP_C_FPGA-TX3-03-RX2-03-MSP_A_FPGA	243
2.17.5	MSP_C_FPGA-TX3-04-RX2-04-MSP_A_FPGA	244
2.17.6	MSP_C_FPGA-TX3-05-RX2-05-MSP_A_FPGA	245
2.17.7	MSP_C_FPGA-TX3-06-RX2-06-MSP_A_FPGA	246
2.17.8	MSP_C_FPGA-TX3-07-RX2-07-MSP_A_FPGA	247
2.17.9	MSP_C_FPGA-TX3-08-RX2-08-MSP_A_FPGA	248
2.17.10	MSP_C_FPGA-TX3-09-RX2-09-MSP_A_FPGA	249
2.17.11	MSP_C_FPGA-TX3-10-RX2-10-MSP_A_FPGA	250
2.17.12	MSP_C_FPGA-TX3-11-RX2-11-MSP_A_FPGA	251
2.18	MSP_C TX4 MSP_A RX1 Minipod Loopback	252
2.18.1	MSP_C_FPGA-TX4-00-RX1-00-MSP_A_FPGA	253
2.18.2	MSP_C_FPGA-TX4-01-RX1-01-MSP_A_FPGA	254
2.18.3	MSP_C_FPGA-TX4-02-RX1-02-MSP_A_FPGA	255
2.18.4	MSP_C_FPGA-TX4-03-RX1-03-MSP_A_FPGA	256
2.18.5	MSP_C_FPGA-TX4-04-RX1-04-MSP_A_FPGA	257
2.18.6	MSP_C_FPGA-TX4-05-RX1-05-MSP_A_FPGA	258
2.18.7	MSP_C_FPGA-TX4-06-RX1-06-MSP_A_FPGA	259
2.18.8	MSP_C_FPGA-TX4-07-RX1-07-MSP_A_FPGA	260
2.18.9	MSP_C_FPGA-TX4-08-RX1-08-MSP_A_FPGA	261
2.18.10	MSP_C_FPGA-TX4-09-RX1-09-MSP_A_FPGA	262
2.18.11	MSP_C_FPGA-TX4-10-RX1-10-MSP_A_FPGA	263
2.18.12	MSP_C_FPGA-TX4-11-RX1-11-MSP_A_FPGA	264
2.19	MSP_A TX1 MSP_C RX13 Minipod Loopback	265

2.19.1	MSP_A_FPGA-TX1-00-RX13-00-MSP_C_FPGA	266
2.19.2	MSP_A_FPGA-TX1-01-RX13-01-MSP_C_FPGA	267
2.19.3	MSP_A_FPGA-TX1-02-RX13-02-MSP_C_FPGA	268
2.19.4	MSP_A_FPGA-TX1-03-RX13-03-MSP_C_FPGA	269
2.19.5	MSP_A_FPGA-TX1-04-RX13-04-MSP_C_FPGA	270
2.19.6	MSP_A_FPGA-TX1-05-RX13-05-MSP_C_FPGA	271
2.19.7	MSP_A_FPGA-TX1-06-RX13-06-MSP_C_FPGA	272
2.19.8	MSP_A_FPGA-TX1-07-RX13-07-MSP_C_FPGA	273
2.19.9	MSP_A_FPGA-TX1-08-RX13-08-MSP_C_FPGA	274
2.19.10	MSP_A_FPGA-TX1-09-RX13-09-MSP_C_FPGA	275
2.19.11	MSP_A_FPGA-TX1-10-RX13-10-MSP_C_FPGA	276
2.19.12	MSP_A_FPGA-TX1-11-RX13-11-MSP_C_FPGA	277
2.20	MSP_A_TX2 MSP_C_RX12 Minipod Loopback	278
2.20.1	MSP_A_FPGA-TX2-00-RX12-00-MSP_C_FPGA	279
2.20.2	MSP_A_FPGA-TX2-01-RX12-01-MSP_C_FPGA	280
2.20.3	MSP_A_FPGA-TX2-02-RX12-02-MSP_C_FPGA	281
2.20.4	MSP_A_FPGA-TX2-03-RX12-03-MSP_C_FPGA	282
2.20.5	MSP_A_FPGA-TX2-04-RX12-04-MSP_C_FPGA	283
2.20.6	MSP_A_FPGA-TX2-05-RX12-05-MSP_C_FPGA	284
2.20.7	MSP_A_FPGA-TX2-06-RX12-06-MSP_C_FPGA	285
2.20.8	MSP_A_FPGA-TX2-07-RX12-07-MSP_C_FPGA	286
2.20.9	MSP_A_FPGA-TX2-08-RX12-08-MSP_C_FPGA	287
2.20.10	MSP_A_FPGA-TX2-09-RX12-09-MSP_C_FPGA	288
2.20.11	MSP_A_FPGA-TX2-10-RX12-10-MSP_C_FPGA	289
2.20.12	MSP_A_FPGA-TX2-11-RX12-11-MSP_C_FPGA	290
2.21	MSP_C_TX3 MSP_A_RX4 Minipod Loopback	291
2.21.1	MSP_C_FPGA-TX3-00-RX4-00-MSP_A_FPGA	292
2.21.2	MSP_C_FPGA-TX3-01-RX4-01-MSP_A_FPGA	293
2.21.3	MSP_C_FPGA-TX3-02-RX4-02-MSP_A_FPGA	294
2.21.4	MSP_C_FPGA-TX3-03-RX4-03-MSP_A_FPGA	295
2.21.5	MSP_C_FPGA-TX3-04-RX4-04-MSP_A_FPGA	296
2.21.6	MSP_C_FPGA-TX3-05-RX4-05-MSP_A_FPGA	297
2.21.7	MSP_C_FPGA-TX3-06-RX4-06-MSP_A_FPGA	298
2.21.8	MSP_C_FPGA-TX3-07-RX4-07-MSP_A_FPGA	299
2.21.9	MSP_C_FPGA-TX3-08-RX4-08-MSP_A_FPGA	300
2.21.10	MSP_C_FPGA-TX3-09-RX4-09-MSP_A_FPGA	301
2.21.11	MSP_C_FPGA-TX3-10-RX4-10-MSP_A_FPGA	302
2.21.12	MSP_C_FPGA-TX3-11-RX4-11-MSP_A_FPGA	303
2.22	MSP_C_TX4 MSP_A_RX3 Minipod Loopback	304
2.22.1	MSP_C_FPGA-TX4-00-RX3-00-MSP_A_FPGA	305
2.22.2	MSP_C_FPGA-TX4-01-RX3-01-MSP_A_FPGA	306
2.22.3	MSP_C_FPGA-TX4-02-RX3-02-MSP_A_FPGA	307
2.22.4	MSP_C_FPGA-TX4-03-RX3-03-MSP_A_FPGA	308
2.22.5	MSP_C_FPGA-TX4-04-RX3-04-MSP_A_FPGA	309
2.22.6	MSP_C_FPGA-TX4-05-RX3-05-MSP_A_FPGA	310
2.22.7	MSP_C_FPGA-TX4-06-RX3-06-MSP_A_FPGA	311
2.22.8	MSP_C_FPGA-TX4-07-RX3-07-MSP_A_FPGA	312
2.22.9	MSP_C_FPGA-TX4-08-RX3-08-MSP_A_FPGA	313
2.22.10	MSP_C_FPGA-TX4-09-RX3-09-MSP_A_FPGA	314
2.22.11	MSP_C_FPGA-TX4-10-RX3-10-MSP_A_FPGA	315
2.22.12	MSP_C_FPGA-TX4-11-RX3-11-MSP_A_FPGA	316

3	MUCTPI V1 12.8 Gbps	317
3.1	MSP_A_TX1 MSP_C_RX16 Minipod Loopback	318
3.1.1	MSP_A_FPGA-TX1-00-RX16-00-MSP_C_FPGA	319
3.1.2	MSP_A_FPGA-TX1-01-RX16-01-MSP_C_FPGA	320
3.1.3	MSP_A_FPGA-TX1-02-RX16-02-MSP_C_FPGA	321
3.1.4	MSP_A_FPGA-TX1-03-RX16-03-MSP_C_FPGA	322
3.1.5	MSP_A_FPGA-TX1-04-RX16-04-MSP_C_FPGA	323
3.1.6	MSP_A_FPGA-TX1-05-RX16-05-MSP_C_FPGA	324
3.1.7	MSP_A_FPGA-TX1-06-RX16-06-MSP_C_FPGA	325
3.1.8	MSP_A_FPGA-TX1-07-RX16-07-MSP_C_FPGA	326
3.1.9	MSP_A_FPGA-TX1-08-RX16-08-MSP_C_FPGA	327
3.1.10	MSP_A_FPGA-TX1-09-RX16-09-MSP_C_FPGA	328

3.1.11	MSP_A_FPGA-TX1-10-RX16-10-MSP_C_FPGA	329
3.1.12	MSP_A_FPGA-TX1-11-RX16-11-MSP_C_FPGA	330
3.2	MSP_A TX2 MSP_C RX15 Minipod Loopback	331
3.2.1	MSP_A_FPGA-TX2-00-RX15-00-MSP_C_FPGA	332
3.2.2	MSP_A_FPGA-TX2-01-RX15-01-MSP_C_FPGA	333
3.2.3	MSP_A_FPGA-TX2-02-RX15-02-MSP_C_FPGA	334
3.2.4	MSP_A_FPGA-TX2-03-RX15-03-MSP_C_FPGA	335
3.2.5	MSP_A_FPGA-TX2-04-RX15-04-MSP_C_FPGA	336
3.2.6	MSP_A_FPGA-TX2-05-RX15-05-MSP_C_FPGA	337
3.2.7	MSP_A_FPGA-TX2-06-RX15-06-MSP_C_FPGA	338
3.2.8	MSP_A_FPGA-TX2-07-RX15-07-MSP_C_FPGA	339
3.2.9	MSP_A_FPGA-TX2-08-RX15-08-MSP_C_FPGA	340
3.2.10	MSP_A_FPGA-TX2-09-RX15-09-MSP_C_FPGA	341
3.2.11	MSP_A_FPGA-TX2-10-RX15-10-MSP_C_FPGA	342
3.2.12	MSP_A_FPGA-TX2-11-RX15-11-MSP_C_FPGA	343
3.3	MSP_C TX3 MSP_A RX7 Minipod Loopback	344
3.3.1	MSP_C_FPGA-TX3-00-RX7-00-MSP_A_FPGA	345
3.3.2	MSP_C_FPGA-TX3-01-RX7-01-MSP_A_FPGA	346
3.3.3	MSP_C_FPGA-TX3-02-RX7-02-MSP_A_FPGA	347
3.3.4	MSP_C_FPGA-TX3-03-RX7-03-MSP_A_FPGA	348
3.3.5	MSP_C_FPGA-TX3-04-RX7-04-MSP_A_FPGA	349
3.3.6	MSP_C_FPGA-TX3-05-RX7-05-MSP_A_FPGA	350
3.3.7	MSP_C_FPGA-TX3-06-RX7-06-MSP_A_FPGA	351
3.3.8	MSP_C_FPGA-TX3-07-RX7-07-MSP_A_FPGA	352
3.3.9	MSP_C_FPGA-TX3-08-RX7-08-MSP_A_FPGA	353
3.3.10	MSP_C_FPGA-TX3-09-RX7-09-MSP_A_FPGA	354
3.3.11	MSP_C_FPGA-TX3-10-RX7-10-MSP_A_FPGA	355
3.3.12	MSP_C_FPGA-TX3-11-RX7-11-MSP_A_FPGA	356
3.4	MSP_C TX4 MSP_A RX6 Minipod Loopback	357
3.4.1	MSP_C_FPGA-TX4-00-RX6-00-MSP_A_FPGA	358
3.4.2	MSP_C_FPGA-TX4-01-RX6-01-MSP_A_FPGA	359
3.4.3	MSP_C_FPGA-TX4-02-RX6-02-MSP_A_FPGA	360
3.4.4	MSP_C_FPGA-TX4-03-RX6-03-MSP_A_FPGA	361
3.4.5	MSP_C_FPGA-TX4-04-RX6-04-MSP_A_FPGA	362
3.4.6	MSP_C_FPGA-TX4-05-RX6-05-MSP_A_FPGA	363
3.4.7	MSP_C_FPGA-TX4-06-RX6-06-MSP_A_FPGA	364
3.4.8	MSP_C_FPGA-TX4-07-RX6-07-MSP_A_FPGA	365
3.4.9	MSP_C_FPGA-TX4-08-RX6-08-MSP_A_FPGA	366
3.4.10	MSP_C_FPGA-TX4-09-RX6-09-MSP_A_FPGA	367
3.4.11	MSP_C_FPGA-TX4-10-RX6-10-MSP_A_FPGA	368
3.4.12	MSP_C_FPGA-TX4-11-RX6-11-MSP_A_FPGA	369
3.5	Partial TRP TX5 MSP_A RX5 Minipod Loopback	370
3.5.1	TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA	372
3.5.2	TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA	373
3.5.3	TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA	374
3.5.4	TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA	375
3.5.5	TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA	376
3.5.6	TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA	377
3.5.7	TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA	378
3.5.8	TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA	379
3.6	TRP J1 QSFP Loopback	380
3.6.1	TRP_FPGA-J1-00-J1-00-TRP_FPGA	381
3.6.2	TRP_FPGA-J1-01-J1-01-TRP_FPGA	382
3.6.3	TRP_FPGA-J1-02-J1-02-TRP_FPGA	383
3.6.4	TRP_FPGA-J1-03-J1-03-TRP_FPGA	384
3.7	TRP J3 SFP Loopback	385
3.7.1	TRP_FPGA-J3-00-J3-00-TRP_FPGA	386
3.8	MSP_A TRP On board links	387
3.8.1	MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA	389
3.8.2	MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA	390
3.8.3	MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA	391
3.8.4	MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA	392
3.8.5	MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA	393
3.8.6	MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA	394

3.8.7	MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA	395
3.8.8	MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA	396
3.8.9	MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA	397
3.8.10	MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA	398
3.8.11	MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA	399
3.8.12	MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA	400
3.8.13	MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA	401
3.8.14	MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA	402
3.8.15	MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA	403
3.8.16	MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA	404
3.8.17	MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA	405
3.8.18	MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA	406
3.8.19	MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA	407
3.8.20	MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA	408
3.8.21	MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA	409
3.8.22	MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA	410
3.8.23	MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA	411
3.8.24	MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA	412
3.8.25	MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA	413
3.8.26	MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA	414
3.8.27	MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA	415
3.8.28	MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA	416
3.9	MSP_C TRP On board links	417
3.9.1	MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA	419
3.9.2	MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA	420
3.9.3	MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA	421
3.9.4	MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA	422
3.9.5	MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA	423
3.9.6	MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA	424
3.9.7	MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA	425
3.9.8	MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA	426
3.9.9	MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA	427
3.9.10	MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA	428
3.9.11	MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA	429
3.9.12	MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA	430
3.9.13	MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA	431
3.9.14	MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA	432
3.9.15	MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA	433
3.9.16	MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA	434
3.9.17	MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA	435
3.9.18	MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA	436
3.9.19	MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA	437
3.9.20	MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA	438
3.9.21	MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA	439
3.9.22	MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA	440
3.9.23	MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA	441
3.9.24	MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA	442
3.9.25	MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA	443
3.9.26	MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA	444
3.9.27	MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA	445
3.9.28	MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA	446
3.10	MSP_A TX1 MSP_C RX18 Minipod Loopback	447
3.10.1	MSP_A_FPGA-TX1-00-RX18-00-MSP_C_FPGA	448
3.10.2	MSP_A_FPGA-TX1-01-RX18-01-MSP_C_FPGA	449
3.10.3	MSP_A_FPGA-TX1-02-RX18-02-MSP_C_FPGA	450
3.10.4	MSP_A_FPGA-TX1-03-RX18-03-MSP_C_FPGA	451
3.10.5	MSP_A_FPGA-TX1-04-RX18-04-MSP_C_FPGA	452
3.10.6	MSP_A_FPGA-TX1-05-RX18-05-MSP_C_FPGA	453
3.10.7	MSP_A_FPGA-TX1-06-RX18-06-MSP_C_FPGA	454
3.10.8	MSP_A_FPGA-TX1-07-RX18-07-MSP_C_FPGA	455
3.10.9	MSP_A_FPGA-TX1-08-RX18-08-MSP_C_FPGA	456
3.10.10	MSP_A_FPGA-TX1-09-RX18-09-MSP_C_FPGA	457
3.10.11	MSP_A_FPGA-TX1-10-RX18-10-MSP_C_FPGA	458
3.10.12	MSP_A_FPGA-TX1-11-RX18-11-MSP_C_FPGA	459

3.11	MSP_A TX2 MSP_C RX17 Minipod Loopback	460
3.11.1	MSP_A_FPGA-TX2-00-RX17-00-MSP_C_FPGA	461
3.11.2	MSP_A_FPGA-TX2-01-RX17-01-MSP_C_FPGA	462
3.11.3	MSP_A_FPGA-TX2-02-RX17-02-MSP_C_FPGA	463
3.11.4	MSP_A_FPGA-TX2-03-RX17-03-MSP_C_FPGA	464
3.11.5	MSP_A_FPGA-TX2-04-RX17-04-MSP_C_FPGA	465
3.11.6	MSP_A_FPGA-TX2-05-RX17-05-MSP_C_FPGA	466
3.11.7	MSP_A_FPGA-TX2-06-RX17-06-MSP_C_FPGA	467
3.11.8	MSP_A_FPGA-TX2-07-RX17-07-MSP_C_FPGA	468
3.11.9	MSP_A_FPGA-TX2-08-RX17-08-MSP_C_FPGA	469
3.11.10	MSP_A_FPGA-TX2-09-RX17-09-MSP_C_FPGA	470
3.11.11	MSP_A_FPGA-TX2-10-RX17-10-MSP_C_FPGA	471
3.11.12	MSP_A_FPGA-TX2-11-RX17-11-MSP_C_FPGA	472
3.12	MSP_C TX3 MSP_A RX9 Minipod Loopback	473
3.12.1	MSP_C_FPGA-TX3-00-RX9-00-MSP_A_FPGA	474
3.12.2	MSP_C_FPGA-TX3-01-RX9-01-MSP_A_FPGA	475
3.12.3	MSP_C_FPGA-TX3-02-RX9-02-MSP_A_FPGA	476
3.12.4	MSP_C_FPGA-TX3-03-RX9-03-MSP_A_FPGA	477
3.12.5	MSP_C_FPGA-TX3-04-RX9-04-MSP_A_FPGA	478
3.12.6	MSP_C_FPGA-TX3-05-RX9-05-MSP_A_FPGA	479
3.12.7	MSP_C_FPGA-TX3-06-RX9-06-MSP_A_FPGA	480
3.12.8	MSP_C_FPGA-TX3-07-RX9-07-MSP_A_FPGA	481
3.12.9	MSP_C_FPGA-TX3-08-RX9-08-MSP_A_FPGA	482
3.12.10	MSP_C_FPGA-TX3-09-RX9-09-MSP_A_FPGA	483
3.12.11	MSP_C_FPGA-TX3-10-RX9-10-MSP_A_FPGA	484
3.12.12	MSP_C_FPGA-TX3-11-RX9-11-MSP_A_FPGA	485
3.13	MSP_C TX4 MSP_A RX8 Minipod Loopback	486
3.13.1	MSP_C_FPGA-TX4-00-RX8-00-MSP_A_FPGA	487
3.13.2	MSP_C_FPGA-TX4-01-RX8-01-MSP_A_FPGA	488
3.13.3	MSP_C_FPGA-TX4-02-RX8-02-MSP_A_FPGA	489
3.13.4	MSP_C_FPGA-TX4-03-RX8-03-MSP_A_FPGA	490
3.13.5	MSP_C_FPGA-TX4-04-RX8-04-MSP_A_FPGA	491
3.13.6	MSP_C_FPGA-TX4-05-RX8-05-MSP_A_FPGA	492
3.13.7	MSP_C_FPGA-TX4-06-RX8-06-MSP_A_FPGA	493
3.13.8	MSP_C_FPGA-TX4-07-RX8-07-MSP_A_FPGA	494
3.13.9	MSP_C_FPGA-TX4-08-RX8-08-MSP_A_FPGA	495
3.13.10	MSP_C_FPGA-TX4-09-RX8-09-MSP_A_FPGA	496
3.13.11	MSP_C_FPGA-TX4-10-RX8-10-MSP_A_FPGA	497
3.13.12	MSP_C_FPGA-TX4-11-RX8-11-MSP_A_FPGA	498
3.14	Partial TRP TX5 MSP_C RX14 Minipod Loopback	499
3.14.1	TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA	501
3.14.2	TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA	502
3.14.3	TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA	503
3.14.4	TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA	504
3.14.5	TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA	505
3.14.6	TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA	506
3.14.7	TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA	507
3.14.8	TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA	508
3.15	MSP_A TX1 MSP_C RX11 Minipod Loopback	509
3.15.1	MSP_A_FPGA-TX1-00-RX11-00-MSP_C_FPGA	510
3.15.2	MSP_A_FPGA-TX1-01-RX11-01-MSP_C_FPGA	511
3.15.3	MSP_A_FPGA-TX1-02-RX11-02-MSP_C_FPGA	512
3.15.4	MSP_A_FPGA-TX1-03-RX11-03-MSP_C_FPGA	513
3.15.5	MSP_A_FPGA-TX1-04-RX11-04-MSP_C_FPGA	514
3.15.6	MSP_A_FPGA-TX1-05-RX11-05-MSP_C_FPGA	515
3.15.7	MSP_A_FPGA-TX1-06-RX11-06-MSP_C_FPGA	516
3.15.8	MSP_A_FPGA-TX1-07-RX11-07-MSP_C_FPGA	517
3.15.9	MSP_A_FPGA-TX1-08-RX11-08-MSP_C_FPGA	518
3.15.10	MSP_A_FPGA-TX1-09-RX11-09-MSP_C_FPGA	519
3.15.11	MSP_A_FPGA-TX1-10-RX11-10-MSP_C_FPGA	520
3.15.12	MSP_A_FPGA-TX1-11-RX11-11-MSP_C_FPGA	521
3.16	MSP_A TX2 MSP_C RX10 Minipod Loopback	522
3.16.1	MSP_A_FPGA-TX2-00-RX10-00-MSP_C_FPGA	523
3.16.2	MSP_A_FPGA-TX2-01-RX10-01-MSP_C_FPGA	524

3.16.3	MSP_A_FPGA-TX2-02-RX10-02-MSP_C_FPGA	525
3.16.4	MSP_A_FPGA-TX2-03-RX10-03-MSP_C_FPGA	526
3.16.5	MSP_A_FPGA-TX2-04-RX10-04-MSP_C_FPGA	527
3.16.6	MSP_A_FPGA-TX2-05-RX10-05-MSP_C_FPGA	528
3.16.7	MSP_A_FPGA-TX2-06-RX10-06-MSP_C_FPGA	529
3.16.8	MSP_A_FPGA-TX2-07-RX10-07-MSP_C_FPGA	530
3.16.9	MSP_A_FPGA-TX2-08-RX10-08-MSP_C_FPGA	531
3.16.10	MSP_A_FPGA-TX2-09-RX10-09-MSP_C_FPGA	532
3.16.11	MSP_A_FPGA-TX2-10-RX10-10-MSP_C_FPGA	533
3.16.12	MSP_A_FPGA-TX2-11-RX10-11-MSP_C_FPGA	534
3.17	MSP_C TX3 MSP_A RX2 Minipod Loopback	535
3.17.1	MSP_C_FPGA-TX3-00-RX2-00-MSP_A_FPGA	536
3.17.2	MSP_C_FPGA-TX3-01-RX2-01-MSP_A_FPGA	537
3.17.3	MSP_C_FPGA-TX3-02-RX2-02-MSP_A_FPGA	538
3.17.4	MSP_C_FPGA-TX3-03-RX2-03-MSP_A_FPGA	539
3.17.5	MSP_C_FPGA-TX3-04-RX2-04-MSP_A_FPGA	540
3.17.6	MSP_C_FPGA-TX3-05-RX2-05-MSP_A_FPGA	541
3.17.7	MSP_C_FPGA-TX3-06-RX2-06-MSP_A_FPGA	542
3.17.8	MSP_C_FPGA-TX3-07-RX2-07-MSP_A_FPGA	543
3.17.9	MSP_C_FPGA-TX3-08-RX2-08-MSP_A_FPGA	544
3.17.10	MSP_C_FPGA-TX3-09-RX2-09-MSP_A_FPGA	545
3.17.11	MSP_C_FPGA-TX3-10-RX2-10-MSP_A_FPGA	546
3.17.12	MSP_C_FPGA-TX3-11-RX2-11-MSP_A_FPGA	547
3.18	MSP_C TX4 MSP_A RX1 Minipod Loopback	548
3.18.1	MSP_C_FPGA-TX4-00-RX1-00-MSP_A_FPGA	549
3.18.2	MSP_C_FPGA-TX4-01-RX1-01-MSP_A_FPGA	550
3.18.3	MSP_C_FPGA-TX4-02-RX1-02-MSP_A_FPGA	551
3.18.4	MSP_C_FPGA-TX4-03-RX1-03-MSP_A_FPGA	552
3.18.5	MSP_C_FPGA-TX4-04-RX1-04-MSP_A_FPGA	553
3.18.6	MSP_C_FPGA-TX4-05-RX1-05-MSP_A_FPGA	554
3.18.7	MSP_C_FPGA-TX4-06-RX1-06-MSP_A_FPGA	555
3.18.8	MSP_C_FPGA-TX4-07-RX1-07-MSP_A_FPGA	556
3.18.9	MSP_C_FPGA-TX4-08-RX1-08-MSP_A_FPGA	557
3.18.10	MSP_C_FPGA-TX4-09-RX1-09-MSP_A_FPGA	558
3.18.11	MSP_C_FPGA-TX4-10-RX1-10-MSP_A_FPGA	559
3.18.12	MSP_C_FPGA-TX4-11-RX1-11-MSP_A_FPGA	560
3.19	MSP_A TX1 MSP_C RX13 Minipod Loopback	561
3.19.1	MSP_A_FPGA-TX1-00-RX13-00-MSP_C_FPGA	562
3.19.2	MSP_A_FPGA-TX1-01-RX13-01-MSP_C_FPGA	563
3.19.3	MSP_A_FPGA-TX1-02-RX13-02-MSP_C_FPGA	564
3.19.4	MSP_A_FPGA-TX1-03-RX13-03-MSP_C_FPGA	565
3.19.5	MSP_A_FPGA-TX1-04-RX13-04-MSP_C_FPGA	566
3.19.6	MSP_A_FPGA-TX1-05-RX13-05-MSP_C_FPGA	567
3.19.7	MSP_A_FPGA-TX1-06-RX13-06-MSP_C_FPGA	568
3.19.8	MSP_A_FPGA-TX1-07-RX13-07-MSP_C_FPGA	569
3.19.9	MSP_A_FPGA-TX1-08-RX13-08-MSP_C_FPGA	570
3.19.10	MSP_A_FPGA-TX1-09-RX13-09-MSP_C_FPGA	571
3.19.11	MSP_A_FPGA-TX1-10-RX13-10-MSP_C_FPGA	572
3.19.12	MSP_A_FPGA-TX1-11-RX13-11-MSP_C_FPGA	573
3.20	MSP_A TX2 MSP_C RX12 Minipod Loopback	574
3.20.1	MSP_A_FPGA-TX2-00-RX12-00-MSP_C_FPGA	575
3.20.2	MSP_A_FPGA-TX2-01-RX12-01-MSP_C_FPGA	576
3.20.3	MSP_A_FPGA-TX2-02-RX12-02-MSP_C_FPGA	577
3.20.4	MSP_A_FPGA-TX2-03-RX12-03-MSP_C_FPGA	578
3.20.5	MSP_A_FPGA-TX2-04-RX12-04-MSP_C_FPGA	579
3.20.6	MSP_A_FPGA-TX2-05-RX12-05-MSP_C_FPGA	580
3.20.7	MSP_A_FPGA-TX2-06-RX12-06-MSP_C_FPGA	581
3.20.8	MSP_A_FPGA-TX2-07-RX12-07-MSP_C_FPGA	582
3.20.9	MSP_A_FPGA-TX2-08-RX12-08-MSP_C_FPGA	583
3.20.10	MSP_A_FPGA-TX2-09-RX12-09-MSP_C_FPGA	584
3.20.11	MSP_A_FPGA-TX2-10-RX12-10-MSP_C_FPGA	585
3.20.12	MSP_A_FPGA-TX2-11-RX12-11-MSP_C_FPGA	586
3.21	MSP_C TX3 MSP_A RX4 Minipod Loopback	587
3.21.1	MSP_C_FPGA-TX3-00-RX4-00-MSP_A_FPGA	588

3.21.2	MSP_C_FPGA-TX3-01-RX4-01-MSP_A_FPGA	589
3.21.3	MSP_C_FPGA-TX3-02-RX4-02-MSP_A_FPGA	590
3.21.4	MSP_C_FPGA-TX3-03-RX4-03-MSP_A_FPGA	591
3.21.5	MSP_C_FPGA-TX3-04-RX4-04-MSP_A_FPGA	592
3.21.6	MSP_C_FPGA-TX3-05-RX4-05-MSP_A_FPGA	593
3.21.7	MSP_C_FPGA-TX3-06-RX4-06-MSP_A_FPGA	594
3.21.8	MSP_C_FPGA-TX3-07-RX4-07-MSP_A_FPGA	595
3.21.9	MSP_C_FPGA-TX3-08-RX4-08-MSP_A_FPGA	596
3.21.10	MSP_C_FPGA-TX3-09-RX4-09-MSP_A_FPGA	597
3.21.11	MSP_C_FPGA-TX3-10-RX4-10-MSP_A_FPGA	598
3.21.12	MSP_C_FPGA-TX3-11-RX4-11-MSP_A_FPGA	599
3.22	MSP_C_TX4 MSP_A_RX3 Minipod Loopback	600
3.22.1	MSP_C_FPGA-TX4-00-RX3-00-MSP_A_FPGA	601
3.22.2	MSP_C_FPGA-TX4-01-RX3-01-MSP_A_FPGA	602
3.22.3	MSP_C_FPGA-TX4-02-RX3-02-MSP_A_FPGA	603
3.22.4	MSP_C_FPGA-TX4-03-RX3-03-MSP_A_FPGA	604
3.22.5	MSP_C_FPGA-TX4-04-RX3-04-MSP_A_FPGA	605
3.22.6	MSP_C_FPGA-TX4-05-RX3-05-MSP_A_FPGA	606
3.22.7	MSP_C_FPGA-TX4-06-RX3-06-MSP_A_FPGA	607
3.22.8	MSP_C_FPGA-TX4-07-RX3-07-MSP_A_FPGA	608
3.22.9	MSP_C_FPGA-TX4-08-RX3-08-MSP_A_FPGA	609
3.22.10	MSP_C_FPGA-TX4-09-RX3-09-MSP_A_FPGA	610
3.22.11	MSP_C_FPGA-TX4-10-RX3-10-MSP_A_FPGA	611
3.22.12	MSP_C_FPGA-TX4-11-RX3-11-MSP_A_FPGA	612

4 MUCTPI V2 6.4 Gbps 613

4.1	MSP_A_TX1 MSP_C_RX15 Minipod Loopback	614
4.1.1	MSP_A_FPGA-TX1-00-RX15-00-MSP_C_FPGA	615
4.1.2	MSP_A_FPGA-TX1-01-RX15-01-MSP_C_FPGA	616
4.1.3	MSP_A_FPGA-TX1-02-RX15-02-MSP_C_FPGA	617
4.1.4	MSP_A_FPGA-TX1-03-RX15-03-MSP_C_FPGA	618
4.1.5	MSP_A_FPGA-TX1-04-RX15-04-MSP_C_FPGA	619
4.1.6	MSP_A_FPGA-TX1-05-RX15-05-MSP_C_FPGA	620
4.1.7	MSP_A_FPGA-TX1-06-RX15-06-MSP_C_FPGA	621
4.1.8	MSP_A_FPGA-TX1-07-RX15-07-MSP_C_FPGA	622
4.1.9	MSP_A_FPGA-TX1-08-RX15-08-MSP_C_FPGA	623
4.1.10	MSP_A_FPGA-TX1-09-RX15-09-MSP_C_FPGA	624
4.1.11	MSP_A_FPGA-TX1-10-RX15-10-MSP_C_FPGA	625
4.1.12	MSP_A_FPGA-TX1-11-RX15-11-MSP_C_FPGA	626
4.2	MSP_A_TX2 MSP_C_RX16 Minipod Loopback	627
4.2.1	MSP_A_FPGA-TX2-00-RX16-00-MSP_C_FPGA	628
4.2.2	MSP_A_FPGA-TX2-01-RX16-01-MSP_C_FPGA	629
4.2.3	MSP_A_FPGA-TX2-02-RX16-02-MSP_C_FPGA	630
4.2.4	MSP_A_FPGA-TX2-03-RX16-03-MSP_C_FPGA	631
4.2.5	MSP_A_FPGA-TX2-04-RX16-04-MSP_C_FPGA	632
4.2.6	MSP_A_FPGA-TX2-05-RX16-05-MSP_C_FPGA	633
4.2.7	MSP_A_FPGA-TX2-06-RX16-06-MSP_C_FPGA	634
4.2.8	MSP_A_FPGA-TX2-07-RX16-07-MSP_C_FPGA	635
4.2.9	MSP_A_FPGA-TX2-08-RX16-08-MSP_C_FPGA	636
4.2.10	MSP_A_FPGA-TX2-09-RX16-09-MSP_C_FPGA	637
4.2.11	MSP_A_FPGA-TX2-10-RX16-10-MSP_C_FPGA	638
4.2.12	MSP_A_FPGA-TX2-11-RX16-11-MSP_C_FPGA	639
4.3	MSP_C_TX3 MSP_A_RX6 Minipod Loopback	640
4.3.1	MSP_C_FPGA-TX3-00-RX6-00-MSP_A_FPGA	641
4.3.2	MSP_C_FPGA-TX3-01-RX6-01-MSP_A_FPGA	642
4.3.3	MSP_C_FPGA-TX3-02-RX6-02-MSP_A_FPGA	643
4.3.4	MSP_C_FPGA-TX3-03-RX6-03-MSP_A_FPGA	644
4.3.5	MSP_C_FPGA-TX3-04-RX6-04-MSP_A_FPGA	645
4.3.6	MSP_C_FPGA-TX3-05-RX6-05-MSP_A_FPGA	646
4.3.7	MSP_C_FPGA-TX3-06-RX6-06-MSP_A_FPGA	647
4.3.8	MSP_C_FPGA-TX3-07-RX6-07-MSP_A_FPGA	648
4.3.9	MSP_C_FPGA-TX3-08-RX6-08-MSP_A_FPGA	649
4.3.10	MSP_C_FPGA-TX3-09-RX6-09-MSP_A_FPGA	650
4.3.11	MSP_C_FPGA-TX3-10-RX6-10-MSP_A_FPGA	651

4.3.12	MSP_C_FPGA-TX3-11-RX6-11-MSP_A_FPGA	652
4.4	MSP_C TX4 MSP_A RX7 Minipod Loopback	653
4.4.1	MSP_C_FPGA-TX4-00-RX7-00-MSP_A_FPGA	654
4.4.2	MSP_C_FPGA-TX4-01-RX7-01-MSP_A_FPGA	655
4.4.3	MSP_C_FPGA-TX4-02-RX7-02-MSP_A_FPGA	656
4.4.4	MSP_C_FPGA-TX4-03-RX7-03-MSP_A_FPGA	657
4.4.5	MSP_C_FPGA-TX4-04-RX7-04-MSP_A_FPGA	658
4.4.6	MSP_C_FPGA-TX4-05-RX7-05-MSP_A_FPGA	659
4.4.7	MSP_C_FPGA-TX4-06-RX7-06-MSP_A_FPGA	660
4.4.8	MSP_C_FPGA-TX4-07-RX7-07-MSP_A_FPGA	661
4.4.9	MSP_C_FPGA-TX4-08-RX7-08-MSP_A_FPGA	662
4.4.10	MSP_C_FPGA-TX4-09-RX7-09-MSP_A_FPGA	663
4.4.11	MSP_C_FPGA-TX4-10-RX7-10-MSP_A_FPGA	664
4.4.12	MSP_C_FPGA-TX4-11-RX7-11-MSP_A_FPGA	665
4.5	Partial TRP TX5 MSP_A RX5 Minipod Loopback	666
4.5.1	TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA	668
4.5.2	TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA	669
4.5.3	TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA	670
4.5.4	TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA	671
4.5.5	TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA	672
4.5.6	TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA	673
4.5.7	TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA	674
4.5.8	TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA	675
4.6	TRP J1 QSFP Loopback	676
4.6.1	TRP_FPGA-J1-00-J1-00-TRP_FPGA	677
4.6.2	TRP_FPGA-J1-01-J1-01-TRP_FPGA	678
4.6.3	TRP_FPGA-J1-02-J1-02-TRP_FPGA	679
4.6.4	TRP_FPGA-J1-03-J1-03-TRP_FPGA	680
4.7	TRP J3 SFP Loopback	681
4.7.1	TRP_FPGA-J3-00-J3-00-TRP_FPGA	682
4.8	MSP_A TRP On board links	683
4.8.1	MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA	685
4.8.2	MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA	686
4.8.3	MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA	687
4.8.4	MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA	688
4.8.5	MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA	689
4.8.6	MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA	690
4.8.7	MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA	691
4.8.8	MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA	692
4.8.9	MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA	693
4.8.10	MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA	694
4.8.11	MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA	695
4.8.12	MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA	696
4.8.13	MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA	697
4.8.14	MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA	698
4.8.15	MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA	699
4.8.16	MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA	700
4.8.17	MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA	701
4.8.18	MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA	702
4.8.19	MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA	703
4.8.20	MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA	704
4.8.21	MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA	705
4.8.22	MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA	706
4.8.23	MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA	707
4.8.24	MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA	708
4.8.25	MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA	709
4.8.26	MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA	710
4.8.27	MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA	711
4.8.28	MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA	712
4.9	MSP_C TRP On board links	713
4.9.1	MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA	715
4.9.2	MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA	716
4.9.3	MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA	717
4.9.4	MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA	718

4.9.5	MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA	719
4.9.6	MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA	720
4.9.7	MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA	721
4.9.8	MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA	722
4.9.9	MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA	723
4.9.10	MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA	724
4.9.11	MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA	725
4.9.12	MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA	726
4.9.13	MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA	727
4.9.14	MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA	728
4.9.15	MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA	729
4.9.16	MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA	730
4.9.17	MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA	731
4.9.18	MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA	732
4.9.19	MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA	733
4.9.20	MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA	734
4.9.21	MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA	735
4.9.22	MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA	736
4.9.23	MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA	737
4.9.24	MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA	738
4.9.25	MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA	739
4.9.26	MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA	740
4.9.27	MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA	741
4.9.28	MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA	742
4.10	MSP_A_TX1 MSP_C_RX17 Minipod Loopback	743
4.10.1	MSP_A_FPGA-TX1-00-RX17-00-MSP_C_FPGA	744
4.10.2	MSP_A_FPGA-TX1-01-RX17-01-MSP_C_FPGA	745
4.10.3	MSP_A_FPGA-TX1-02-RX17-02-MSP_C_FPGA	746
4.10.4	MSP_A_FPGA-TX1-03-RX17-03-MSP_C_FPGA	747
4.10.5	MSP_A_FPGA-TX1-04-RX17-04-MSP_C_FPGA	748
4.10.6	MSP_A_FPGA-TX1-05-RX17-05-MSP_C_FPGA	749
4.10.7	MSP_A_FPGA-TX1-06-RX17-06-MSP_C_FPGA	750
4.10.8	MSP_A_FPGA-TX1-07-RX17-07-MSP_C_FPGA	751
4.10.9	MSP_A_FPGA-TX1-08-RX17-08-MSP_C_FPGA	752
4.10.10	MSP_A_FPGA-TX1-09-RX17-09-MSP_C_FPGA	753
4.10.11	MSP_A_FPGA-TX1-10-RX17-10-MSP_C_FPGA	754
4.10.12	MSP_A_FPGA-TX1-11-RX17-11-MSP_C_FPGA	755
4.11	MSP_A_TX2 MSP_C_RX18 Minipod Loopback	756
4.11.1	MSP_A_FPGA-TX2-00-RX18-00-MSP_C_FPGA	757
4.11.2	MSP_A_FPGA-TX2-01-RX18-01-MSP_C_FPGA	758
4.11.3	MSP_A_FPGA-TX2-02-RX18-02-MSP_C_FPGA	759
4.11.4	MSP_A_FPGA-TX2-03-RX18-03-MSP_C_FPGA	760
4.11.5	MSP_A_FPGA-TX2-04-RX18-04-MSP_C_FPGA	761
4.11.6	MSP_A_FPGA-TX2-05-RX18-05-MSP_C_FPGA	762
4.11.7	MSP_A_FPGA-TX2-06-RX18-06-MSP_C_FPGA	763
4.11.8	MSP_A_FPGA-TX2-07-RX18-07-MSP_C_FPGA	764
4.11.9	MSP_A_FPGA-TX2-08-RX18-08-MSP_C_FPGA	765
4.11.10	MSP_A_FPGA-TX2-09-RX18-09-MSP_C_FPGA	766
4.11.11	MSP_A_FPGA-TX2-10-RX18-10-MSP_C_FPGA	767
4.11.12	MSP_A_FPGA-TX2-11-RX18-11-MSP_C_FPGA	768
4.12	MSP_C_TX3 MSP_A_RX8 Minipod Loopback	769
4.12.1	MSP_C_FPGA-TX3-00-RX8-00-MSP_A_FPGA	770
4.12.2	MSP_C_FPGA-TX3-01-RX8-01-MSP_A_FPGA	771
4.12.3	MSP_C_FPGA-TX3-02-RX8-02-MSP_A_FPGA	772
4.12.4	MSP_C_FPGA-TX3-03-RX8-03-MSP_A_FPGA	773
4.12.5	MSP_C_FPGA-TX3-04-RX8-04-MSP_A_FPGA	774
4.12.6	MSP_C_FPGA-TX3-05-RX8-05-MSP_A_FPGA	775
4.12.7	MSP_C_FPGA-TX3-06-RX8-06-MSP_A_FPGA	776
4.12.8	MSP_C_FPGA-TX3-07-RX8-07-MSP_A_FPGA	777
4.12.9	MSP_C_FPGA-TX3-08-RX8-08-MSP_A_FPGA	778
4.12.10	MSP_C_FPGA-TX3-09-RX8-09-MSP_A_FPGA	779
4.12.11	MSP_C_FPGA-TX3-10-RX8-10-MSP_A_FPGA	780
4.12.12	MSP_C_FPGA-TX3-11-RX8-11-MSP_A_FPGA	781
4.13	MSP_C_TX4 MSP_A_RX9 Minipod Loopback	782

4.13.1	MSP_C_FPGA-TX4-00-RX9-00-MSP_A_FPGA	783
4.13.2	MSP_C_FPGA-TX4-01-RX9-01-MSP_A_FPGA	784
4.13.3	MSP_C_FPGA-TX4-02-RX9-02-MSP_A_FPGA	785
4.13.4	MSP_C_FPGA-TX4-03-RX9-03-MSP_A_FPGA	786
4.13.5	MSP_C_FPGA-TX4-04-RX9-04-MSP_A_FPGA	787
4.13.6	MSP_C_FPGA-TX4-05-RX9-05-MSP_A_FPGA	788
4.13.7	MSP_C_FPGA-TX4-06-RX9-06-MSP_A_FPGA	789
4.13.8	MSP_C_FPGA-TX4-07-RX9-07-MSP_A_FPGA	790
4.13.9	MSP_C_FPGA-TX4-08-RX9-08-MSP_A_FPGA	791
4.13.10	MSP_C_FPGA-TX4-09-RX9-09-MSP_A_FPGA	792
4.13.11	MSP_C_FPGA-TX4-10-RX9-10-MSP_A_FPGA	793
4.13.12	MSP_C_FPGA-TX4-11-RX9-11-MSP_A_FPGA	794
4.14	Partial TRP TX5 MSP_C RX14 Minipod Loopback	795
4.14.1	TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA	797
4.14.2	TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA	798
4.14.3	TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA	799
4.14.4	TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA	800
4.14.5	TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA	801
4.14.6	TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA	802
4.14.7	TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA	803
4.14.8	TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA	804
4.15	MSP_A TX1 MSP_C RX10 Minipod Loopback	805
4.15.1	MSP_A_FPGA-TX1-00-RX10-00-MSP_C_FPGA	806
4.15.2	MSP_A_FPGA-TX1-01-RX10-01-MSP_C_FPGA	807
4.15.3	MSP_A_FPGA-TX1-02-RX10-02-MSP_C_FPGA	808
4.15.4	MSP_A_FPGA-TX1-03-RX10-03-MSP_C_FPGA	809
4.15.5	MSP_A_FPGA-TX1-04-RX10-04-MSP_C_FPGA	810
4.15.6	MSP_A_FPGA-TX1-05-RX10-05-MSP_C_FPGA	811
4.15.7	MSP_A_FPGA-TX1-06-RX10-06-MSP_C_FPGA	812
4.15.8	MSP_A_FPGA-TX1-07-RX10-07-MSP_C_FPGA	813
4.15.9	MSP_A_FPGA-TX1-08-RX10-08-MSP_C_FPGA	814
4.15.10	MSP_A_FPGA-TX1-09-RX10-09-MSP_C_FPGA	815
4.15.11	MSP_A_FPGA-TX1-10-RX10-10-MSP_C_FPGA	816
4.15.12	MSP_A_FPGA-TX1-11-RX10-11-MSP_C_FPGA	817
4.16	MSP_A TX2 MSP_C RX11 Minipod Loopback	818
4.16.1	MSP_A_FPGA-TX2-00-RX11-00-MSP_C_FPGA	819
4.16.2	MSP_A_FPGA-TX2-01-RX11-01-MSP_C_FPGA	820
4.16.3	MSP_A_FPGA-TX2-02-RX11-02-MSP_C_FPGA	821
4.16.4	MSP_A_FPGA-TX2-03-RX11-03-MSP_C_FPGA	822
4.16.5	MSP_A_FPGA-TX2-04-RX11-04-MSP_C_FPGA	823
4.16.6	MSP_A_FPGA-TX2-05-RX11-05-MSP_C_FPGA	824
4.16.7	MSP_A_FPGA-TX2-06-RX11-06-MSP_C_FPGA	825
4.16.8	MSP_A_FPGA-TX2-07-RX11-07-MSP_C_FPGA	826
4.16.9	MSP_A_FPGA-TX2-08-RX11-08-MSP_C_FPGA	827
4.16.10	MSP_A_FPGA-TX2-09-RX11-09-MSP_C_FPGA	828
4.16.11	MSP_A_FPGA-TX2-10-RX11-10-MSP_C_FPGA	829
4.16.12	MSP_A_FPGA-TX2-11-RX11-11-MSP_C_FPGA	830
4.17	MSP_C TX3 MSP_A RX1 Minipod Loopback	831
4.17.1	MSP_C_FPGA-TX3-00-RX1-00-MSP_A_FPGA	832
4.17.2	MSP_C_FPGA-TX3-01-RX1-01-MSP_A_FPGA	833
4.17.3	MSP_C_FPGA-TX3-02-RX1-02-MSP_A_FPGA	834
4.17.4	MSP_C_FPGA-TX3-03-RX1-03-MSP_A_FPGA	835
4.17.5	MSP_C_FPGA-TX3-04-RX1-04-MSP_A_FPGA	836
4.17.6	MSP_C_FPGA-TX3-05-RX1-05-MSP_A_FPGA	837
4.17.7	MSP_C_FPGA-TX3-06-RX1-06-MSP_A_FPGA	838
4.17.8	MSP_C_FPGA-TX3-07-RX1-07-MSP_A_FPGA	839
4.17.9	MSP_C_FPGA-TX3-08-RX1-08-MSP_A_FPGA	840
4.17.10	MSP_C_FPGA-TX3-09-RX1-09-MSP_A_FPGA	841
4.17.11	MSP_C_FPGA-TX3-10-RX1-10-MSP_A_FPGA	842
4.17.12	MSP_C_FPGA-TX3-11-RX1-11-MSP_A_FPGA	843
4.18	MSP_C TX4 MSP_A RX2 Minipod Loopback	844
4.18.1	MSP_C_FPGA-TX4-00-RX2-00-MSP_A_FPGA	845
4.18.2	MSP_C_FPGA-TX4-01-RX2-01-MSP_A_FPGA	846
4.18.3	MSP_C_FPGA-TX4-02-RX2-02-MSP_A_FPGA	847

4.18.4	MSP_C_FPGA-TX4-03-RX2-03-MSP_A_FPGA	848
4.18.5	MSP_C_FPGA-TX4-04-RX2-04-MSP_A_FPGA	849
4.18.6	MSP_C_FPGA-TX4-05-RX2-05-MSP_A_FPGA	850
4.18.7	MSP_C_FPGA-TX4-06-RX2-06-MSP_A_FPGA	851
4.18.8	MSP_C_FPGA-TX4-07-RX2-07-MSP_A_FPGA	852
4.18.9	MSP_C_FPGA-TX4-08-RX2-08-MSP_A_FPGA	853
4.18.10	MSP_C_FPGA-TX4-09-RX2-09-MSP_A_FPGA	854
4.18.11	MSP_C_FPGA-TX4-10-RX2-10-MSP_A_FPGA	855
4.18.12	MSP_C_FPGA-TX4-11-RX2-11-MSP_A_FPGA	856
4.19	MSP_A TX1 MSP_C RX12 Minipod Loopback	857
4.19.1	MSP_A_FPGA-TX1-00-RX12-00-MSP_C_FPGA	858
4.19.2	MSP_A_FPGA-TX1-01-RX12-01-MSP_C_FPGA	859
4.19.3	MSP_A_FPGA-TX1-02-RX12-02-MSP_C_FPGA	860
4.19.4	MSP_A_FPGA-TX1-03-RX12-03-MSP_C_FPGA	861
4.19.5	MSP_A_FPGA-TX1-04-RX12-04-MSP_C_FPGA	862
4.19.6	MSP_A_FPGA-TX1-05-RX12-05-MSP_C_FPGA	863
4.19.7	MSP_A_FPGA-TX1-06-RX12-06-MSP_C_FPGA	864
4.19.8	MSP_A_FPGA-TX1-07-RX12-07-MSP_C_FPGA	865
4.19.9	MSP_A_FPGA-TX1-08-RX12-08-MSP_C_FPGA	866
4.19.10	MSP_A_FPGA-TX1-09-RX12-09-MSP_C_FPGA	867
4.19.11	MSP_A_FPGA-TX1-10-RX12-10-MSP_C_FPGA	868
4.19.12	MSP_A_FPGA-TX1-11-RX12-11-MSP_C_FPGA	869
4.20	MSP_A TX2 MSP_C RX13 Minipod Loopback	870
4.20.1	MSP_A_FPGA-TX2-00-RX13-00-MSP_C_FPGA	871
4.20.2	MSP_A_FPGA-TX2-01-RX13-01-MSP_C_FPGA	872
4.20.3	MSP_A_FPGA-TX2-02-RX13-02-MSP_C_FPGA	873
4.20.4	MSP_A_FPGA-TX2-03-RX13-03-MSP_C_FPGA	874
4.20.5	MSP_A_FPGA-TX2-04-RX13-04-MSP_C_FPGA	875
4.20.6	MSP_A_FPGA-TX2-05-RX13-05-MSP_C_FPGA	876
4.20.7	MSP_A_FPGA-TX2-06-RX13-06-MSP_C_FPGA	877
4.20.8	MSP_A_FPGA-TX2-07-RX13-07-MSP_C_FPGA	878
4.20.9	MSP_A_FPGA-TX2-08-RX13-08-MSP_C_FPGA	879
4.20.10	MSP_A_FPGA-TX2-09-RX13-09-MSP_C_FPGA	880
4.20.11	MSP_A_FPGA-TX2-10-RX13-10-MSP_C_FPGA	881
4.20.12	MSP_A_FPGA-TX2-11-RX13-11-MSP_C_FPGA	882
4.21	MSP_C TX3 MSP_A RX3 Minipod Loopback	883
4.21.1	MSP_C_FPGA-TX3-00-RX3-00-MSP_A_FPGA	884
4.21.2	MSP_C_FPGA-TX3-01-RX3-01-MSP_A_FPGA	885
4.21.3	MSP_C_FPGA-TX3-02-RX3-02-MSP_A_FPGA	886
4.21.4	MSP_C_FPGA-TX3-03-RX3-03-MSP_A_FPGA	887
4.21.5	MSP_C_FPGA-TX3-04-RX3-04-MSP_A_FPGA	888
4.21.6	MSP_C_FPGA-TX3-05-RX3-05-MSP_A_FPGA	889
4.21.7	MSP_C_FPGA-TX3-06-RX3-06-MSP_A_FPGA	890
4.21.8	MSP_C_FPGA-TX3-07-RX3-07-MSP_A_FPGA	891
4.21.9	MSP_C_FPGA-TX3-08-RX3-08-MSP_A_FPGA	892
4.21.10	MSP_C_FPGA-TX3-09-RX3-09-MSP_A_FPGA	893
4.21.11	MSP_C_FPGA-TX3-10-RX3-10-MSP_A_FPGA	894
4.21.12	MSP_C_FPGA-TX3-11-RX3-11-MSP_A_FPGA	895
4.22	MSP_C TX4 MSP_A RX4 Minipod Loopback	896
4.22.1	MSP_C_FPGA-TX4-00-RX4-00-MSP_A_FPGA	897
4.22.2	MSP_C_FPGA-TX4-01-RX4-01-MSP_A_FPGA	898
4.22.3	MSP_C_FPGA-TX4-02-RX4-02-MSP_A_FPGA	899
4.22.4	MSP_C_FPGA-TX4-03-RX4-03-MSP_A_FPGA	900
4.22.5	MSP_C_FPGA-TX4-04-RX4-04-MSP_A_FPGA	901
4.22.6	MSP_C_FPGA-TX4-05-RX4-05-MSP_A_FPGA	902
4.22.7	MSP_C_FPGA-TX4-06-RX4-06-MSP_A_FPGA	903
4.22.8	MSP_C_FPGA-TX4-07-RX4-07-MSP_A_FPGA	904
4.22.9	MSP_C_FPGA-TX4-08-RX4-08-MSP_A_FPGA	905
4.22.10	MSP_C_FPGA-TX4-09-RX4-09-MSP_A_FPGA	906
4.22.11	MSP_C_FPGA-TX4-10-RX4-10-MSP_A_FPGA	907
4.22.12	MSP_C_FPGA-TX4-11-RX4-11-MSP_A_FPGA	908

5 MUCTPI V2 12.8 Gbps	909
5.1 MSP_A TX1 MSP_C RX15 Minipod Loopback	910
5.1.1 MSP_A_FPGA-TX1-00-RX15-00-MSP_C_FPGA	911
5.1.2 MSP_A_FPGA-TX1-01-RX15-01-MSP_C_FPGA	912
5.1.3 MSP_A_FPGA-TX1-02-RX15-02-MSP_C_FPGA	913
5.1.4 MSP_A_FPGA-TX1-03-RX15-03-MSP_C_FPGA	914
5.1.5 MSP_A_FPGA-TX1-04-RX15-04-MSP_C_FPGA	915
5.1.6 MSP_A_FPGA-TX1-05-RX15-05-MSP_C_FPGA	916
5.1.7 MSP_A_FPGA-TX1-06-RX15-06-MSP_C_FPGA	917
5.1.8 MSP_A_FPGA-TX1-07-RX15-07-MSP_C_FPGA	918
5.1.9 MSP_A_FPGA-TX1-08-RX15-08-MSP_C_FPGA	919
5.1.10 MSP_A_FPGA-TX1-09-RX15-09-MSP_C_FPGA	920
5.1.11 MSP_A_FPGA-TX1-10-RX15-10-MSP_C_FPGA	921
5.1.12 MSP_A_FPGA-TX1-11-RX15-11-MSP_C_FPGA	922
5.2 MSP_A TX2 MSP_C RX16 Minipod Loopback	923
5.2.1 MSP_A_FPGA-TX2-00-RX16-00-MSP_C_FPGA	924
5.2.2 MSP_A_FPGA-TX2-01-RX16-01-MSP_C_FPGA	925
5.2.3 MSP_A_FPGA-TX2-02-RX16-02-MSP_C_FPGA	926
5.2.4 MSP_A_FPGA-TX2-03-RX16-03-MSP_C_FPGA	927
5.2.5 MSP_A_FPGA-TX2-04-RX16-04-MSP_C_FPGA	928
5.2.6 MSP_A_FPGA-TX2-05-RX16-05-MSP_C_FPGA	929
5.2.7 MSP_A_FPGA-TX2-06-RX16-06-MSP_C_FPGA	930
5.2.8 MSP_A_FPGA-TX2-07-RX16-07-MSP_C_FPGA	931
5.2.9 MSP_A_FPGA-TX2-08-RX16-08-MSP_C_FPGA	932
5.2.10 MSP_A_FPGA-TX2-09-RX16-09-MSP_C_FPGA	933
5.2.11 MSP_A_FPGA-TX2-10-RX16-10-MSP_C_FPGA	934
5.2.12 MSP_A_FPGA-TX2-11-RX16-11-MSP_C_FPGA	935
5.3 MSP_C TX3 MSP_A RX6 Minipod Loopback	936
5.3.1 MSP_C_FPGA-TX3-00-RX6-00-MSP_A_FPGA	937
5.3.2 MSP_C_FPGA-TX3-01-RX6-01-MSP_A_FPGA	938
5.3.3 MSP_C_FPGA-TX3-02-RX6-02-MSP_A_FPGA	939
5.3.4 MSP_C_FPGA-TX3-03-RX6-03-MSP_A_FPGA	940
5.3.5 MSP_C_FPGA-TX3-04-RX6-04-MSP_A_FPGA	941
5.3.6 MSP_C_FPGA-TX3-05-RX6-05-MSP_A_FPGA	942
5.3.7 MSP_C_FPGA-TX3-06-RX6-06-MSP_A_FPGA	943
5.3.8 MSP_C_FPGA-TX3-07-RX6-07-MSP_A_FPGA	944
5.3.9 MSP_C_FPGA-TX3-08-RX6-08-MSP_A_FPGA	945
5.3.10 MSP_C_FPGA-TX3-09-RX6-09-MSP_A_FPGA	946
5.3.11 MSP_C_FPGA-TX3-10-RX6-10-MSP_A_FPGA	947
5.3.12 MSP_C_FPGA-TX3-11-RX6-11-MSP_A_FPGA	948
5.4 MSP_C TX4 MSP_A RX7 Minipod Loopback	949
5.4.1 MSP_C_FPGA-TX4-00-RX7-00-MSP_A_FPGA	950
5.4.2 MSP_C_FPGA-TX4-01-RX7-01-MSP_A_FPGA	951
5.4.3 MSP_C_FPGA-TX4-02-RX7-02-MSP_A_FPGA	952
5.4.4 MSP_C_FPGA-TX4-03-RX7-03-MSP_A_FPGA	953
5.4.5 MSP_C_FPGA-TX4-04-RX7-04-MSP_A_FPGA	954
5.4.6 MSP_C_FPGA-TX4-05-RX7-05-MSP_A_FPGA	955
5.4.7 MSP_C_FPGA-TX4-06-RX7-06-MSP_A_FPGA	956
5.4.8 MSP_C_FPGA-TX4-07-RX7-07-MSP_A_FPGA	957
5.4.9 MSP_C_FPGA-TX4-08-RX7-08-MSP_A_FPGA	958
5.4.10 MSP_C_FPGA-TX4-09-RX7-09-MSP_A_FPGA	959
5.4.11 MSP_C_FPGA-TX4-10-RX7-10-MSP_A_FPGA	960
5.4.12 MSP_C_FPGA-TX4-11-RX7-11-MSP_A_FPGA	961
5.5 Partial TRP TX5 MSP_A RX5 Minipod Loopback	962
5.5.1 TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA	964
5.5.2 TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA	965
5.5.3 TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA	966
5.5.4 TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA	967
5.5.5 TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA	968
5.5.6 TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA	969
5.5.7 TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA	970
5.5.8 TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA	971
5.6 TRP J1 QSFP Loopback	972
5.6.1 TRP_FPGA-J1-00-J1-00-TRP_FPGA	973

5.6.2	TRP_FPGA-J1-01-J1-01-TRP_FPGA	974
5.6.3	TRP_FPGA-J1-02-J1-02-TRP_FPGA	975
5.6.4	TRP_FPGA-J1-03-J1-03-TRP_FPGA	976
5.7	TRP J3 SFP Loopback	977
5.7.1	TRP_FPGA-J3-00-J3-00-TRP_FPGA	978
5.8	MSP_A TRP On board links	979
5.8.1	MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA	981
5.8.2	MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA	982
5.8.3	MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA	983
5.8.4	MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA	984
5.8.5	MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA	985
5.8.6	MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA	986
5.8.7	MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA	987
5.8.8	MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA	988
5.8.9	MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA	989
5.8.10	MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA	990
5.8.11	MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA	991
5.8.12	MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA	992
5.8.13	MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA	993
5.8.14	MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA	994
5.8.15	MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA	995
5.8.16	MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA	996
5.8.17	MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA	997
5.8.18	MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA	998
5.8.19	MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA	999
5.8.20	MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA	1000
5.8.21	MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA	1001
5.8.22	MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA	1002
5.8.23	MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA	1003
5.8.24	MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA	1004
5.8.25	MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA	1005
5.8.26	MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA	1006
5.8.27	MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA	1007
5.8.28	MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA	1008
5.9	MSP_C TRP On board links	1009
5.9.1	MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA	1011
5.9.2	MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA	1012
5.9.3	MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA	1013
5.9.4	MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA	1014
5.9.5	MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA	1015
5.9.6	MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA	1016
5.9.7	MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA	1017
5.9.8	MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA	1018
5.9.9	MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA	1019
5.9.10	MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA	1020
5.9.11	MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA	1021
5.9.12	MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA	1022
5.9.13	MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA	1023
5.9.14	MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA	1024
5.9.15	MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA	1025
5.9.16	MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA	1026
5.9.17	MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA	1027
5.9.18	MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA	1028
5.9.19	MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA	1029
5.9.20	MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA	1030
5.9.21	MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA	1031
5.9.22	MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA	1032
5.9.23	MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA	1033
5.9.24	MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA	1034
5.9.25	MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA	1035
5.9.26	MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA	1036
5.9.27	MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA	1037
5.9.28	MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA	1038
5.10	MSP_A TX1 MSP_C RX17 Minipod Loopback	1039

5.10.1	MSP_A_FPGA-TX1-00-RX17-00-MSP_C_FPGA	1040
5.10.2	MSP_A_FPGA-TX1-01-RX17-01-MSP_C_FPGA	1041
5.10.3	MSP_A_FPGA-TX1-02-RX17-02-MSP_C_FPGA	1042
5.10.4	MSP_A_FPGA-TX1-03-RX17-03-MSP_C_FPGA	1043
5.10.5	MSP_A_FPGA-TX1-04-RX17-04-MSP_C_FPGA	1044
5.10.6	MSP_A_FPGA-TX1-05-RX17-05-MSP_C_FPGA	1045
5.10.7	MSP_A_FPGA-TX1-06-RX17-06-MSP_C_FPGA	1046
5.10.8	MSP_A_FPGA-TX1-07-RX17-07-MSP_C_FPGA	1047
5.10.9	MSP_A_FPGA-TX1-08-RX17-08-MSP_C_FPGA	1048
5.10.10	MSP_A_FPGA-TX1-09-RX17-09-MSP_C_FPGA	1049
5.10.11	MSP_A_FPGA-TX1-10-RX17-10-MSP_C_FPGA	1050
5.10.12	MSP_A_FPGA-TX1-11-RX17-11-MSP_C_FPGA	1051
5.11	MSP_A TX2 MSP_C RX18 Minipod Loopback	1052
5.11.1	MSP_A_FPGA-TX2-00-RX18-00-MSP_C_FPGA	1053
5.11.2	MSP_A_FPGA-TX2-01-RX18-01-MSP_C_FPGA	1054
5.11.3	MSP_A_FPGA-TX2-02-RX18-02-MSP_C_FPGA	1055
5.11.4	MSP_A_FPGA-TX2-03-RX18-03-MSP_C_FPGA	1056
5.11.5	MSP_A_FPGA-TX2-04-RX18-04-MSP_C_FPGA	1057
5.11.6	MSP_A_FPGA-TX2-05-RX18-05-MSP_C_FPGA	1058
5.11.7	MSP_A_FPGA-TX2-06-RX18-06-MSP_C_FPGA	1059
5.11.8	MSP_A_FPGA-TX2-07-RX18-07-MSP_C_FPGA	1060
5.11.9	MSP_A_FPGA-TX2-08-RX18-08-MSP_C_FPGA	1061
5.11.10	MSP_A_FPGA-TX2-09-RX18-09-MSP_C_FPGA	1062
5.11.11	MSP_A_FPGA-TX2-10-RX18-10-MSP_C_FPGA	1063
5.11.12	MSP_A_FPGA-TX2-11-RX18-11-MSP_C_FPGA	1064
5.12	MSP_C TX3 MSP_A RX8 Minipod Loopback	1065
5.12.1	MSP_C_FPGA-TX3-00-RX8-00-MSP_A_FPGA	1066
5.12.2	MSP_C_FPGA-TX3-01-RX8-01-MSP_A_FPGA	1067
5.12.3	MSP_C_FPGA-TX3-02-RX8-02-MSP_A_FPGA	1068
5.12.4	MSP_C_FPGA-TX3-03-RX8-03-MSP_A_FPGA	1069
5.12.5	MSP_C_FPGA-TX3-04-RX8-04-MSP_A_FPGA	1070
5.12.6	MSP_C_FPGA-TX3-05-RX8-05-MSP_A_FPGA	1071
5.12.7	MSP_C_FPGA-TX3-06-RX8-06-MSP_A_FPGA	1072
5.12.8	MSP_C_FPGA-TX3-07-RX8-07-MSP_A_FPGA	1073
5.12.9	MSP_C_FPGA-TX3-08-RX8-08-MSP_A_FPGA	1074
5.12.10	MSP_C_FPGA-TX3-09-RX8-09-MSP_A_FPGA	1075
5.12.11	MSP_C_FPGA-TX3-10-RX8-10-MSP_A_FPGA	1076
5.12.12	MSP_C_FPGA-TX3-11-RX8-11-MSP_A_FPGA	1077
5.13	MSP_C TX4 MSP_A RX9 Minipod Loopback	1078
5.13.1	MSP_C_FPGA-TX4-00-RX9-00-MSP_A_FPGA	1079
5.13.2	MSP_C_FPGA-TX4-01-RX9-01-MSP_A_FPGA	1080
5.13.3	MSP_C_FPGA-TX4-02-RX9-02-MSP_A_FPGA	1081
5.13.4	MSP_C_FPGA-TX4-03-RX9-03-MSP_A_FPGA	1082
5.13.5	MSP_C_FPGA-TX4-04-RX9-04-MSP_A_FPGA	1083
5.13.6	MSP_C_FPGA-TX4-05-RX9-05-MSP_A_FPGA	1084
5.13.7	MSP_C_FPGA-TX4-06-RX9-06-MSP_A_FPGA	1085
5.13.8	MSP_C_FPGA-TX4-07-RX9-07-MSP_A_FPGA	1086
5.13.9	MSP_C_FPGA-TX4-08-RX9-08-MSP_A_FPGA	1087
5.13.10	MSP_C_FPGA-TX4-09-RX9-09-MSP_A_FPGA	1088
5.13.11	MSP_C_FPGA-TX4-10-RX9-10-MSP_A_FPGA	1089
5.13.12	MSP_C_FPGA-TX4-11-RX9-11-MSP_A_FPGA	1090
5.14	Partial TRP TX5 MSP_C RX14 Minipod Loopback	1091
5.14.1	TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA	1093
5.14.2	TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA	1094
5.14.3	TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA	1095
5.14.4	TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA	1096
5.14.5	TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA	1097
5.14.6	TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA	1098
5.14.7	TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA	1099
5.14.8	TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA	1100
5.15	MSP_A TX1 MSP_C RX10 Minipod Loopback	1101
5.15.1	MSP_A_FPGA-TX1-00-RX10-00-MSP_C_FPGA	1102
5.15.2	MSP_A_FPGA-TX1-01-RX10-01-MSP_C_FPGA	1103
5.15.3	MSP_A_FPGA-TX1-02-RX10-02-MSP_C_FPGA	1104

5.15.4	MSP_A_FPGA-TX1-03-RX10-03-MSP_C_FPGA	1105
5.15.5	MSP_A_FPGA-TX1-04-RX10-04-MSP_C_FPGA	1106
5.15.6	MSP_A_FPGA-TX1-05-RX10-05-MSP_C_FPGA	1107
5.15.7	MSP_A_FPGA-TX1-06-RX10-06-MSP_C_FPGA	1108
5.15.8	MSP_A_FPGA-TX1-07-RX10-07-MSP_C_FPGA	1109
5.15.9	MSP_A_FPGA-TX1-08-RX10-08-MSP_C_FPGA	1110
5.15.10	MSP_A_FPGA-TX1-09-RX10-09-MSP_C_FPGA	1111
5.15.11	MSP_A_FPGA-TX1-10-RX10-10-MSP_C_FPGA	1112
5.15.12	MSP_A_FPGA-TX1-11-RX10-11-MSP_C_FPGA	1113
5.16	MSP_A_TX2 MSP_C_RX11 Minipod Loopback	1114
5.16.1	MSP_A_FPGA-TX2-00-RX11-00-MSP_C_FPGA	1115
5.16.2	MSP_A_FPGA-TX2-01-RX11-01-MSP_C_FPGA	1116
5.16.3	MSP_A_FPGA-TX2-02-RX11-02-MSP_C_FPGA	1117
5.16.4	MSP_A_FPGA-TX2-03-RX11-03-MSP_C_FPGA	1118
5.16.5	MSP_A_FPGA-TX2-04-RX11-04-MSP_C_FPGA	1119
5.16.6	MSP_A_FPGA-TX2-05-RX11-05-MSP_C_FPGA	1120
5.16.7	MSP_A_FPGA-TX2-06-RX11-06-MSP_C_FPGA	1121
5.16.8	MSP_A_FPGA-TX2-07-RX11-07-MSP_C_FPGA	1122
5.16.9	MSP_A_FPGA-TX2-08-RX11-08-MSP_C_FPGA	1123
5.16.10	MSP_A_FPGA-TX2-09-RX11-09-MSP_C_FPGA	1124
5.16.11	MSP_A_FPGA-TX2-10-RX11-10-MSP_C_FPGA	1125
5.16.12	MSP_A_FPGA-TX2-11-RX11-11-MSP_C_FPGA	1126
5.17	MSP_C_TX3 MSP_A_RX1 Minipod Loopback	1127
5.17.1	MSP_C_FPGA-TX3-00-RX1-00-MSP_A_FPGA	1128
5.17.2	MSP_C_FPGA-TX3-01-RX1-01-MSP_A_FPGA	1129
5.17.3	MSP_C_FPGA-TX3-02-RX1-02-MSP_A_FPGA	1130
5.17.4	MSP_C_FPGA-TX3-03-RX1-03-MSP_A_FPGA	1131
5.17.5	MSP_C_FPGA-TX3-04-RX1-04-MSP_A_FPGA	1132
5.17.6	MSP_C_FPGA-TX3-05-RX1-05-MSP_A_FPGA	1133
5.17.7	MSP_C_FPGA-TX3-06-RX1-06-MSP_A_FPGA	1134
5.17.8	MSP_C_FPGA-TX3-07-RX1-07-MSP_A_FPGA	1135
5.17.9	MSP_C_FPGA-TX3-08-RX1-08-MSP_A_FPGA	1136
5.17.10	MSP_C_FPGA-TX3-09-RX1-09-MSP_A_FPGA	1137
5.17.11	MSP_C_FPGA-TX3-10-RX1-10-MSP_A_FPGA	1138
5.17.12	MSP_C_FPGA-TX3-11-RX1-11-MSP_A_FPGA	1139
5.18	MSP_C_TX4 MSP_A_RX2 Minipod Loopback	1140
5.18.1	MSP_C_FPGA-TX4-00-RX2-00-MSP_A_FPGA	1141
5.18.2	MSP_C_FPGA-TX4-01-RX2-01-MSP_A_FPGA	1142
5.18.3	MSP_C_FPGA-TX4-02-RX2-02-MSP_A_FPGA	1143
5.18.4	MSP_C_FPGA-TX4-03-RX2-03-MSP_A_FPGA	1144
5.18.5	MSP_C_FPGA-TX4-04-RX2-04-MSP_A_FPGA	1145
5.18.6	MSP_C_FPGA-TX4-05-RX2-05-MSP_A_FPGA	1146
5.18.7	MSP_C_FPGA-TX4-06-RX2-06-MSP_A_FPGA	1147
5.18.8	MSP_C_FPGA-TX4-07-RX2-07-MSP_A_FPGA	1148
5.18.9	MSP_C_FPGA-TX4-08-RX2-08-MSP_A_FPGA	1149
5.18.10	MSP_C_FPGA-TX4-09-RX2-09-MSP_A_FPGA	1150
5.18.11	MSP_C_FPGA-TX4-10-RX2-10-MSP_A_FPGA	1151
5.18.12	MSP_C_FPGA-TX4-11-RX2-11-MSP_A_FPGA	1152
5.19	MSP_A_TX1 MSP_C_RX12 Minipod Loopback	1153
5.19.1	MSP_A_FPGA-TX1-00-RX12-00-MSP_C_FPGA	1154
5.19.2	MSP_A_FPGA-TX1-01-RX12-01-MSP_C_FPGA	1155
5.19.3	MSP_A_FPGA-TX1-02-RX12-02-MSP_C_FPGA	1156
5.19.4	MSP_A_FPGA-TX1-03-RX12-03-MSP_C_FPGA	1157
5.19.5	MSP_A_FPGA-TX1-04-RX12-04-MSP_C_FPGA	1158
5.19.6	MSP_A_FPGA-TX1-05-RX12-05-MSP_C_FPGA	1159
5.19.7	MSP_A_FPGA-TX1-06-RX12-06-MSP_C_FPGA	1160
5.19.8	MSP_A_FPGA-TX1-07-RX12-07-MSP_C_FPGA	1161
5.19.9	MSP_A_FPGA-TX1-08-RX12-08-MSP_C_FPGA	1162
5.19.10	MSP_A_FPGA-TX1-09-RX12-09-MSP_C_FPGA	1163
5.19.11	MSP_A_FPGA-TX1-10-RX12-10-MSP_C_FPGA	1164
5.19.12	MSP_A_FPGA-TX1-11-RX12-11-MSP_C_FPGA	1165
5.20	MSP_A_TX2 MSP_C_RX13 Minipod Loopback	1166
5.20.1	MSP_A_FPGA-TX2-00-RX13-00-MSP_C_FPGA	1167
5.20.2	MSP_A_FPGA-TX2-01-RX13-01-MSP_C_FPGA	1168

5.20.3	MSP_A_FPGA-TX2-02-RX13-02-MSP_C_FPGA	1169
5.20.4	MSP_A_FPGA-TX2-03-RX13-03-MSP_C_FPGA	1170
5.20.5	MSP_A_FPGA-TX2-04-RX13-04-MSP_C_FPGA	1171
5.20.6	MSP_A_FPGA-TX2-05-RX13-05-MSP_C_FPGA	1172
5.20.7	MSP_A_FPGA-TX2-06-RX13-06-MSP_C_FPGA	1173
5.20.8	MSP_A_FPGA-TX2-07-RX13-07-MSP_C_FPGA	1174
5.20.9	MSP_A_FPGA-TX2-08-RX13-08-MSP_C_FPGA	1175
5.20.10	MSP_A_FPGA-TX2-09-RX13-09-MSP_C_FPGA	1176
5.20.11	MSP_A_FPGA-TX2-10-RX13-10-MSP_C_FPGA	1177
5.20.12	MSP_A_FPGA-TX2-11-RX13-11-MSP_C_FPGA	1178
5.21	MSP_C TX3 MSP_A RX3 Minipod Loopback	1179
5.21.1	MSP_C_FPGA-TX3-00-RX3-00-MSP_A_FPGA	1180
5.21.2	MSP_C_FPGA-TX3-01-RX3-01-MSP_A_FPGA	1181
5.21.3	MSP_C_FPGA-TX3-02-RX3-02-MSP_A_FPGA	1182
5.21.4	MSP_C_FPGA-TX3-03-RX3-03-MSP_A_FPGA	1183
5.21.5	MSP_C_FPGA-TX3-04-RX3-04-MSP_A_FPGA	1184
5.21.6	MSP_C_FPGA-TX3-05-RX3-05-MSP_A_FPGA	1185
5.21.7	MSP_C_FPGA-TX3-06-RX3-06-MSP_A_FPGA	1186
5.21.8	MSP_C_FPGA-TX3-07-RX3-07-MSP_A_FPGA	1187
5.21.9	MSP_C_FPGA-TX3-08-RX3-08-MSP_A_FPGA	1188
5.21.10	MSP_C_FPGA-TX3-09-RX3-09-MSP_A_FPGA	1189
5.21.11	MSP_C_FPGA-TX3-10-RX3-10-MSP_A_FPGA	1190
5.21.12	MSP_C_FPGA-TX3-11-RX3-11-MSP_A_FPGA	1191
5.22	MSP_C TX4 MSP_A RX4 Minipod Loopback	1192
5.22.1	MSP_C_FPGA-TX4-00-RX4-00-MSP_A_FPGA	1193
5.22.2	MSP_C_FPGA-TX4-01-RX4-01-MSP_A_FPGA	1194
5.22.3	MSP_C_FPGA-TX4-02-RX4-02-MSP_A_FPGA	1195
5.22.4	MSP_C_FPGA-TX4-03-RX4-03-MSP_A_FPGA	1196
5.22.5	MSP_C_FPGA-TX4-04-RX4-04-MSP_A_FPGA	1197
5.22.6	MSP_C_FPGA-TX4-05-RX4-05-MSP_A_FPGA	1198
5.22.7	MSP_C_FPGA-TX4-06-RX4-06-MSP_A_FPGA	1199
5.22.8	MSP_C_FPGA-TX4-07-RX4-07-MSP_A_FPGA	1200
5.22.9	MSP_C_FPGA-TX4-08-RX4-08-MSP_A_FPGA	1201
5.22.10	MSP_C_FPGA-TX4-09-RX4-09-MSP_A_FPGA	1202
5.22.11	MSP_C_FPGA-TX4-10-RX4-10-MSP_A_FPGA	1203
5.22.12	MSP_C_FPGA-TX4-11-RX4-11-MSP_A_FPGA	1204

Chapter 1

Initial Considerations

1.1 Eye diagram mask

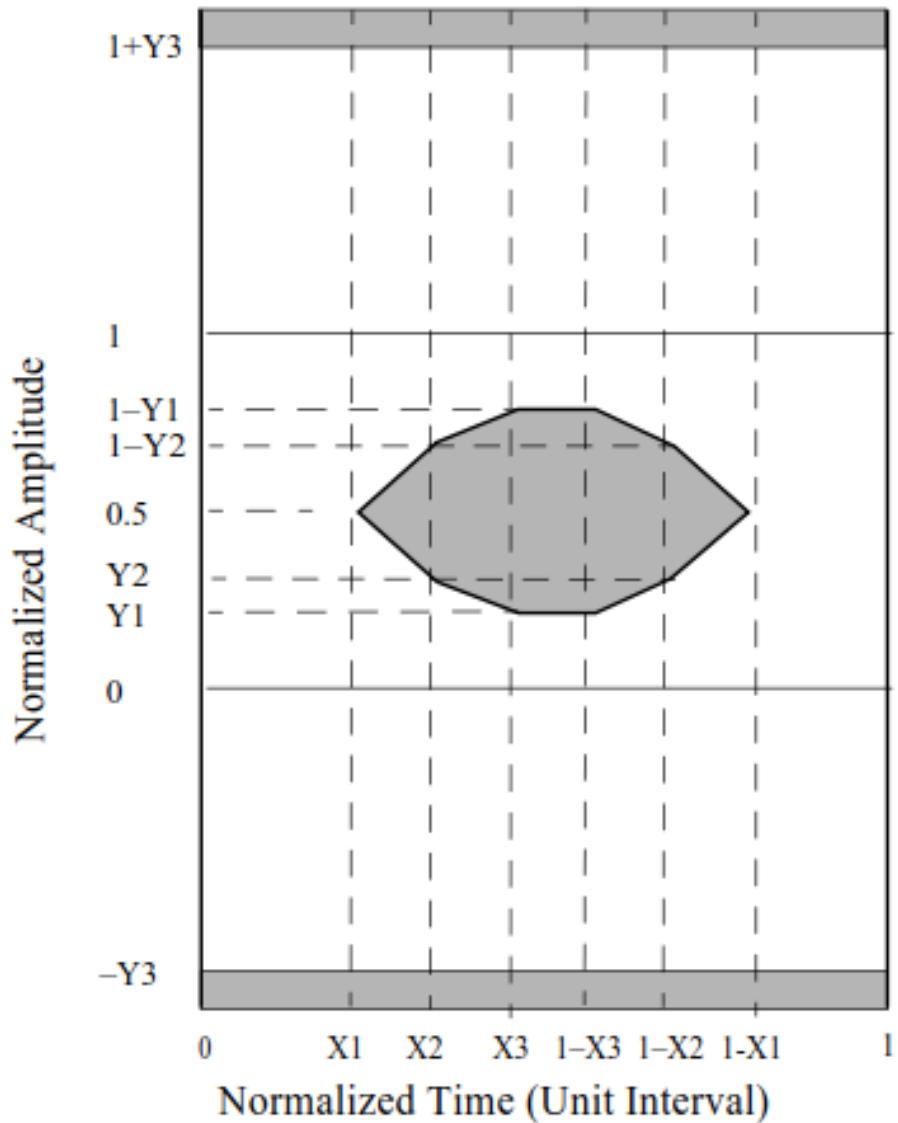


Figure 1.1: Transmitter eye mask definition

Figure 1.1 shows the eye mask parameters $X_1 = 0.25$, $X_2 = 0.40$, $X_3 = 0.45$, $Y_1 = 0.25$, $Y_2 = 0.40$, $Y_3 = 0.45$, $1-Y_1 = 0.28$, $1-Y_2 = 0.25$, $1+Y_3 = 0.80$ extracted from the Table 68-3—10GBASE-LRM transmit characteristics part of the IEEE Std 802.3-2015 SECTION 5.

Chapter 2

MUCTPI V1 6.4 Gbps

2.1 MSP_A TX1 MSP_C RX16 Minipod Loopback

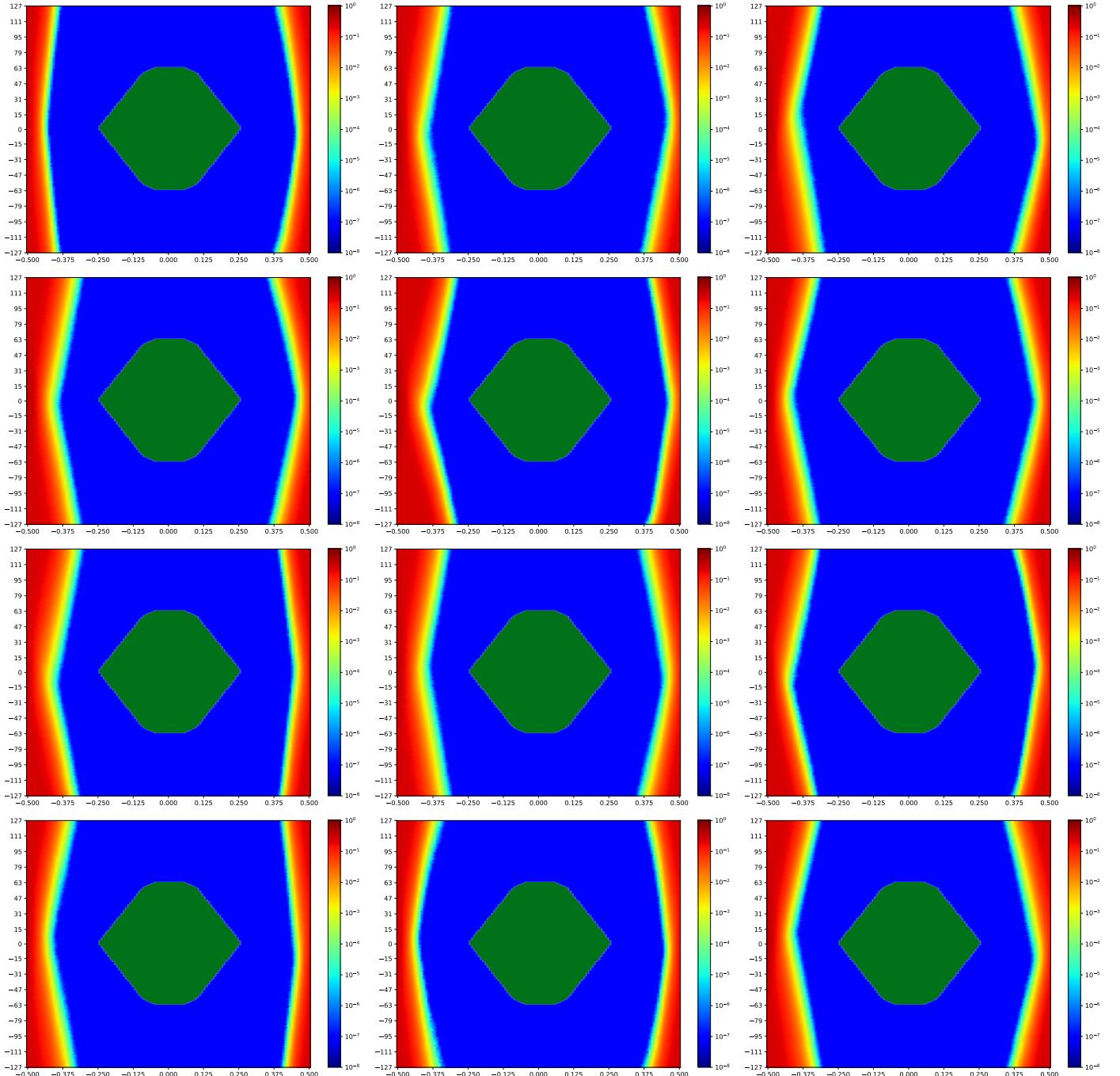


Figure 2.1: MSP_A TX1 MSP_C RX16 Minipod Loopback

A cross-reference to Figure 2.1. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.14.

2.1.1 MSP_A_FPGA-TX1-00-RX16-00-MSP_C_FPGA

Table 2.1: MSP_A_FPGA-TX1-00-RX16-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:01:44		2018-Jan-24 03:02:56	
Reset RX	OA	HO		HO (%)	
true	26480	110		85.27%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

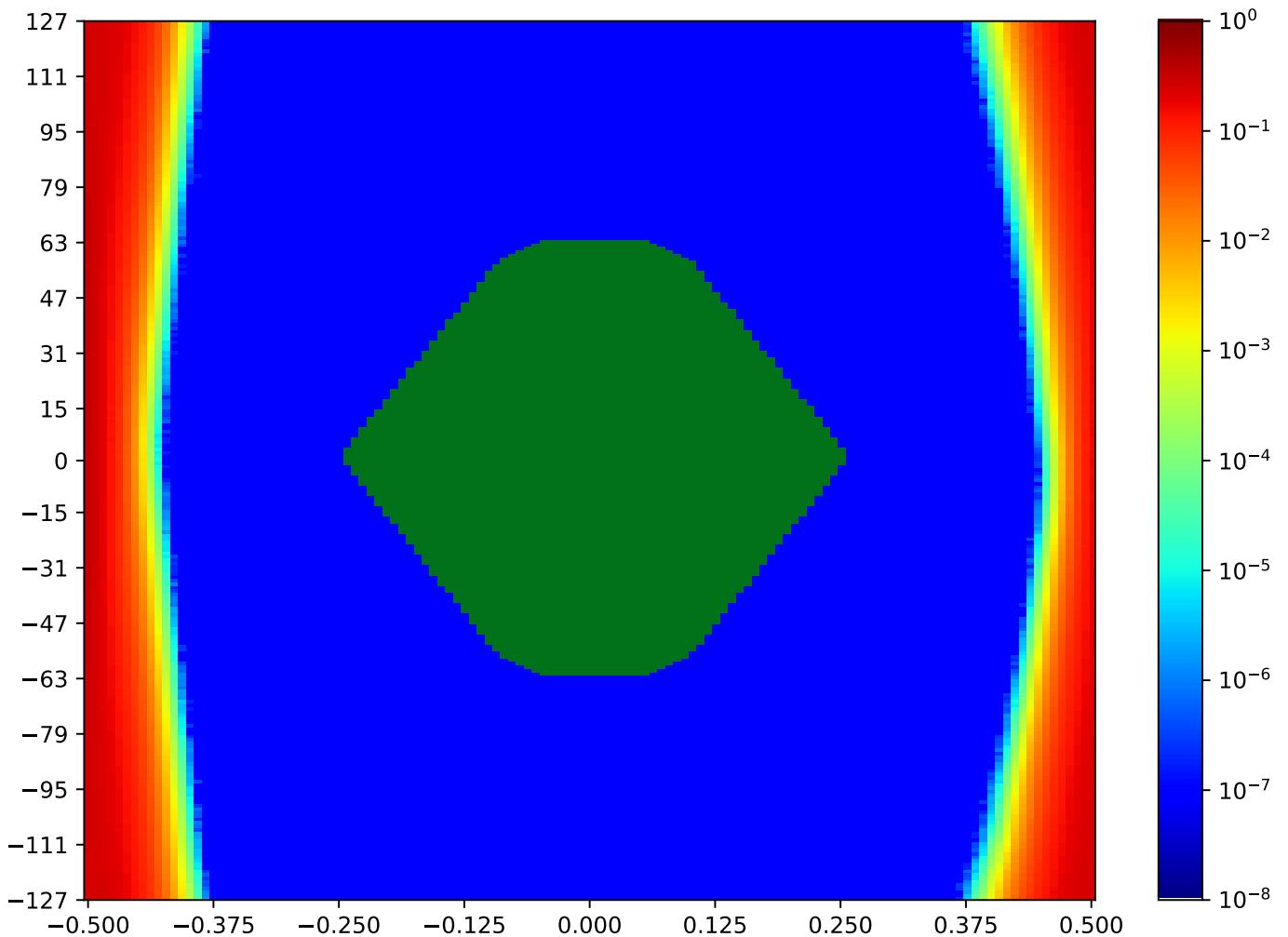


Figure 2.2: MSP_A_FPGA-TX1-00-RX16-00-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.2 MSP_A_FPGA-TX1-01-RX16-01-MSP_C_FPGA

Table 2.2: MSP_A_FPGA-TX1-01-RX16-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:04:07		2018-Jan-24 03:05:16	
Reset RX	OA	HO		HO (%)	
true	24136	105		81.40%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

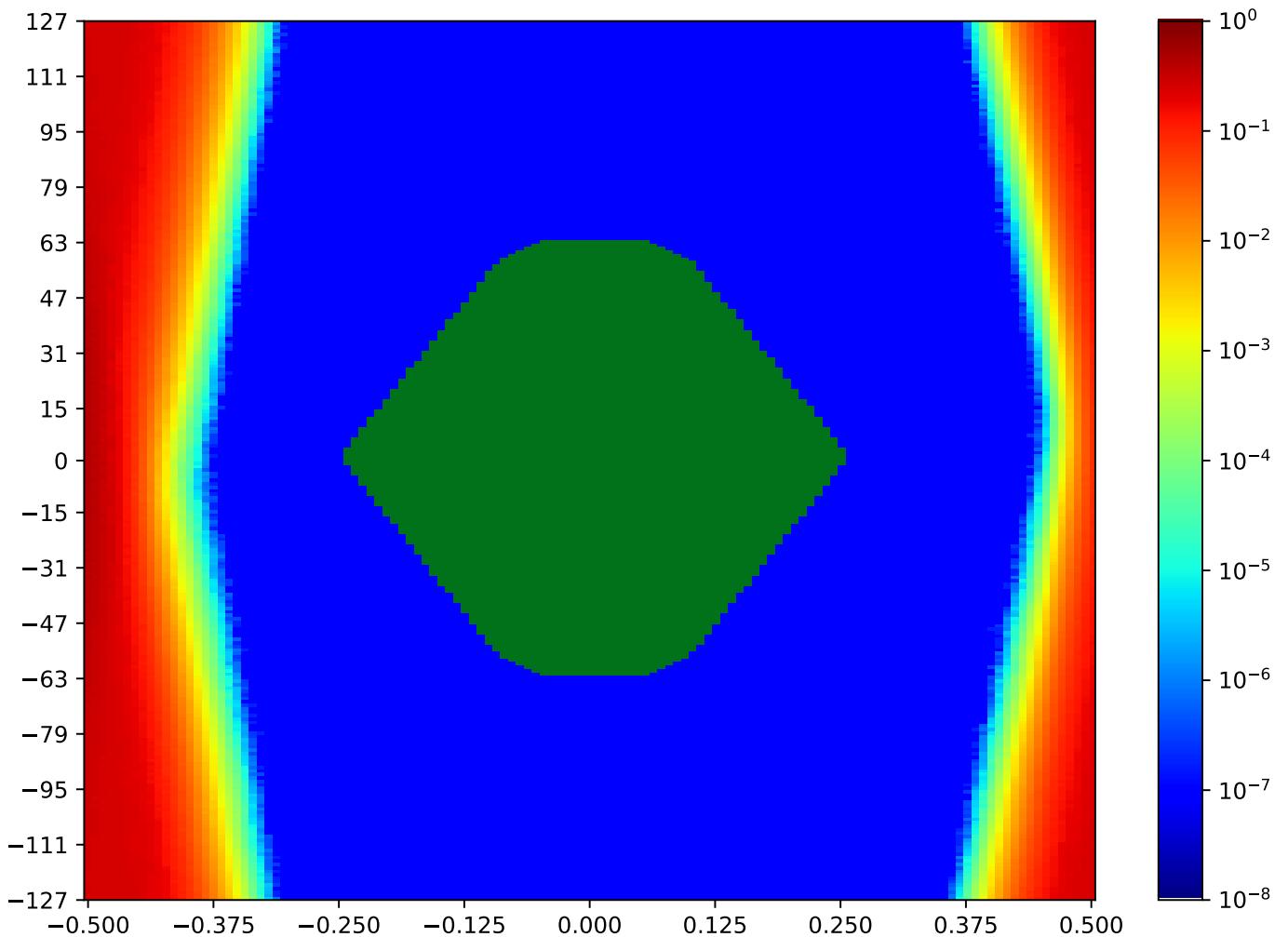


Figure 2.3: MSP_A_FPGA-TX1-01-RX16-01-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.3 MSP_A_FPGA-TX1-02-RX16-02-MSP_C_FPGA

Table 2.3: MSP_A_FPGA-TX1-02-RX16-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:05:16		2018-Jan-24 03:06:25	
Reset RX	OA	HO		HO (%)	
true	23799	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

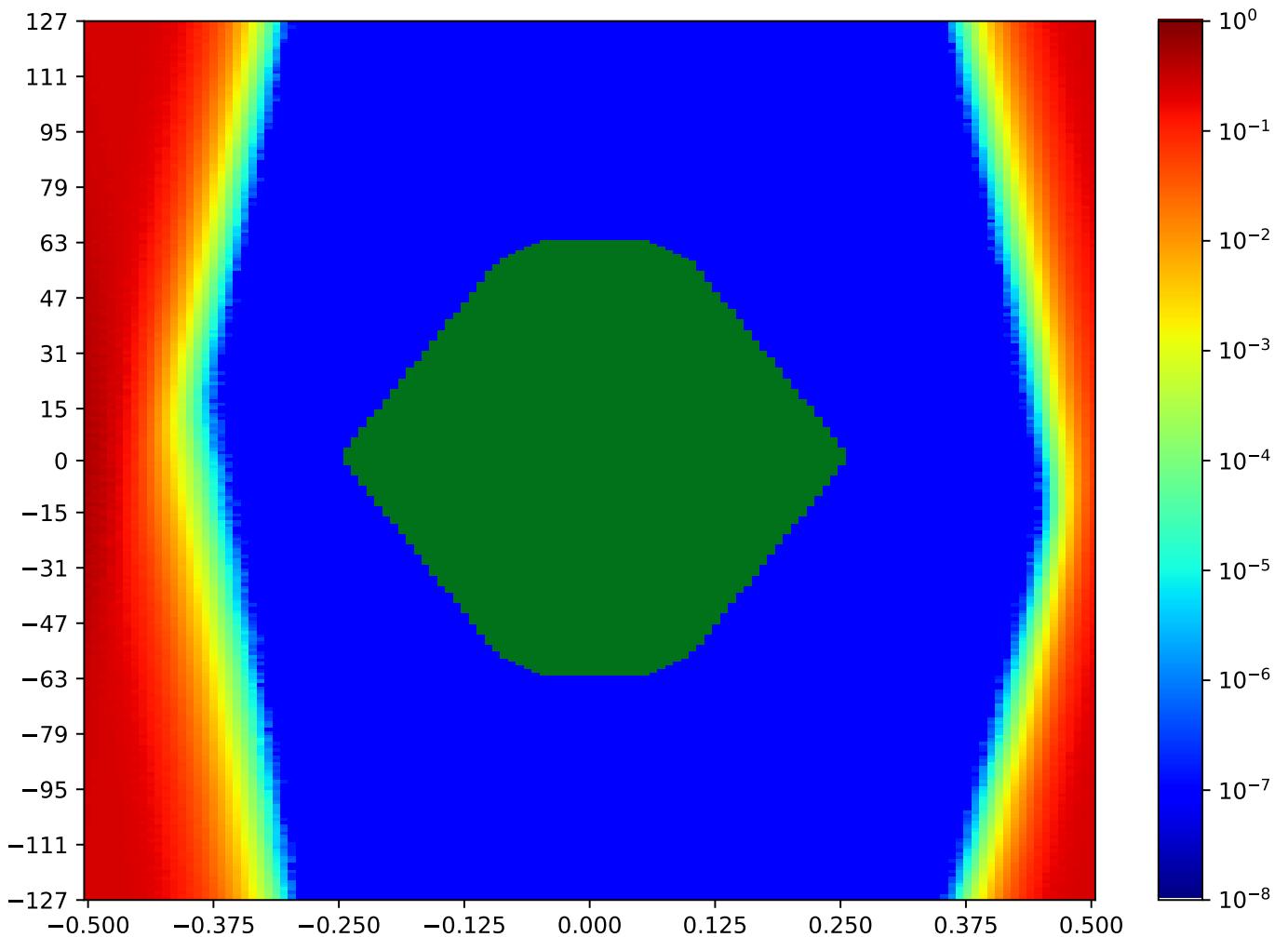


Figure 2.4: MSP_A_FPGA-TX1-02-RX16-02-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.4 MSP_A_FPGA-TX1-03-RX16-03-MSP_C_FPGA

Table 2.4: MSP_A_FPGA-TX1-03-RX16-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 02:59:26		2018-Jan-24 03:00:35	
Reset RX	OA	HO		HO (%)	
true	23900	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

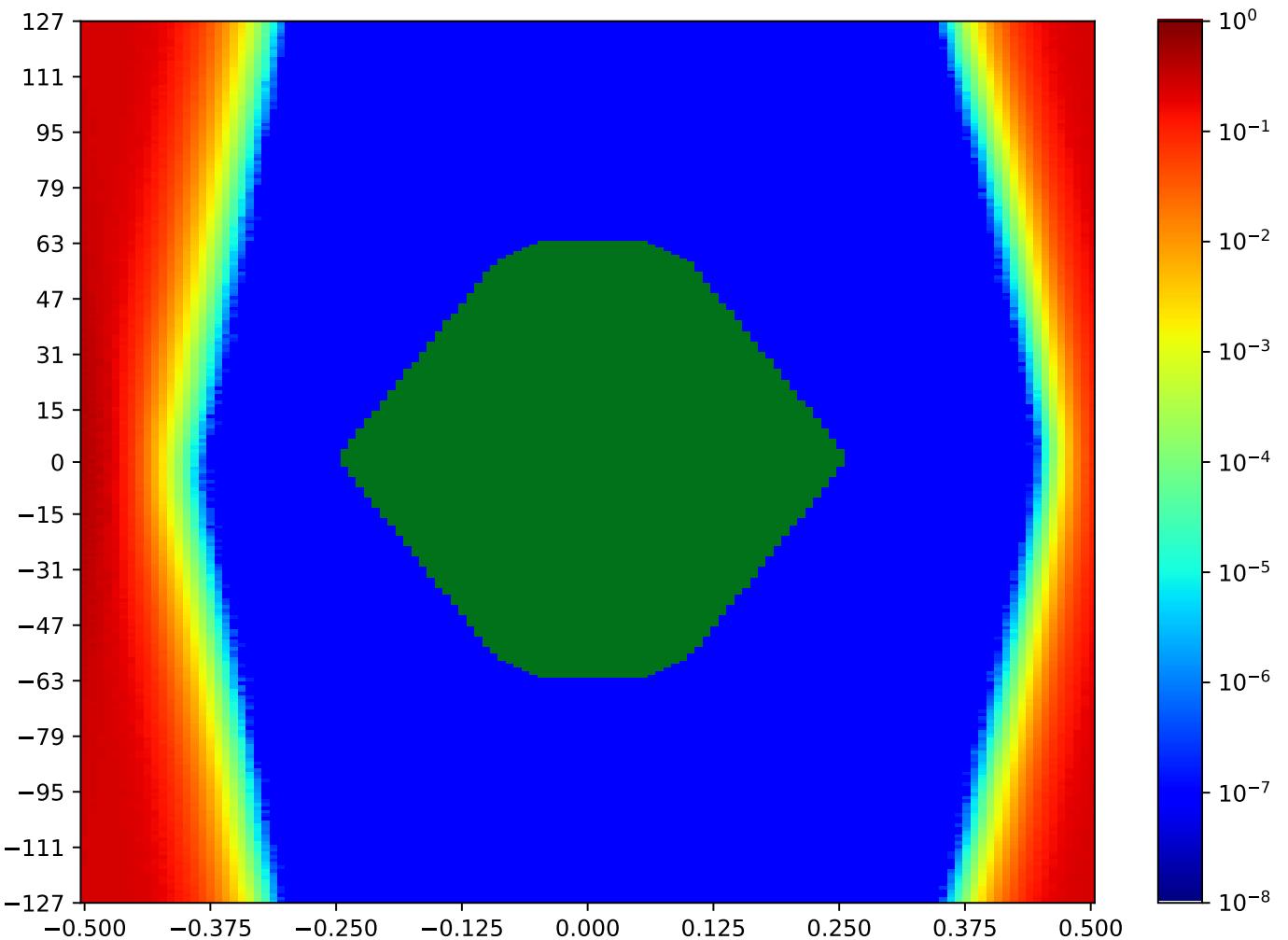


Figure 2.5: MSP_A_FPGA-TX1-03-RX16-03-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.5 MSP_A_FPGA-TX1-04-RX16-04-MSP_C_FPGA

Table 2.5: MSP_A_FPGA-TX1-04-RX16-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:08:45		2018-Jan-24 03:09:54	
Reset RX	OA	HO		HO (%)	
true	24095	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

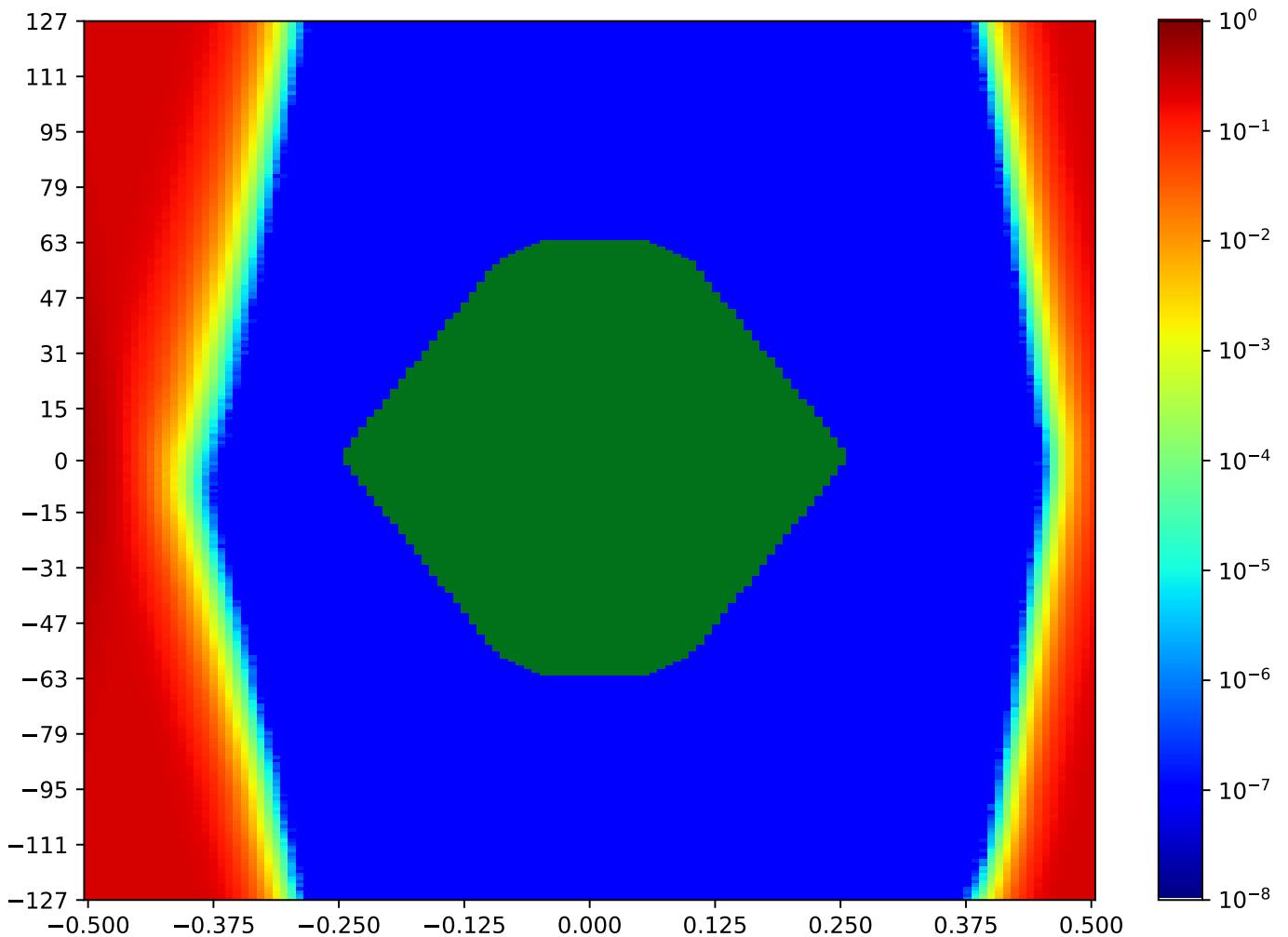


Figure 2.6: MSP_A_FPGA-TX1-04-RX16-04-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.6 MSP_A_FPGA-TX1-05-RX16-05-MSP_C_FPGA

Table 2.6: MSP_A_FPGA-TX1-05-RX16-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 02:58:17		2018-Jan-24 02:59:26	
Reset RX	OA	HO		HO (%)	
true	24014	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

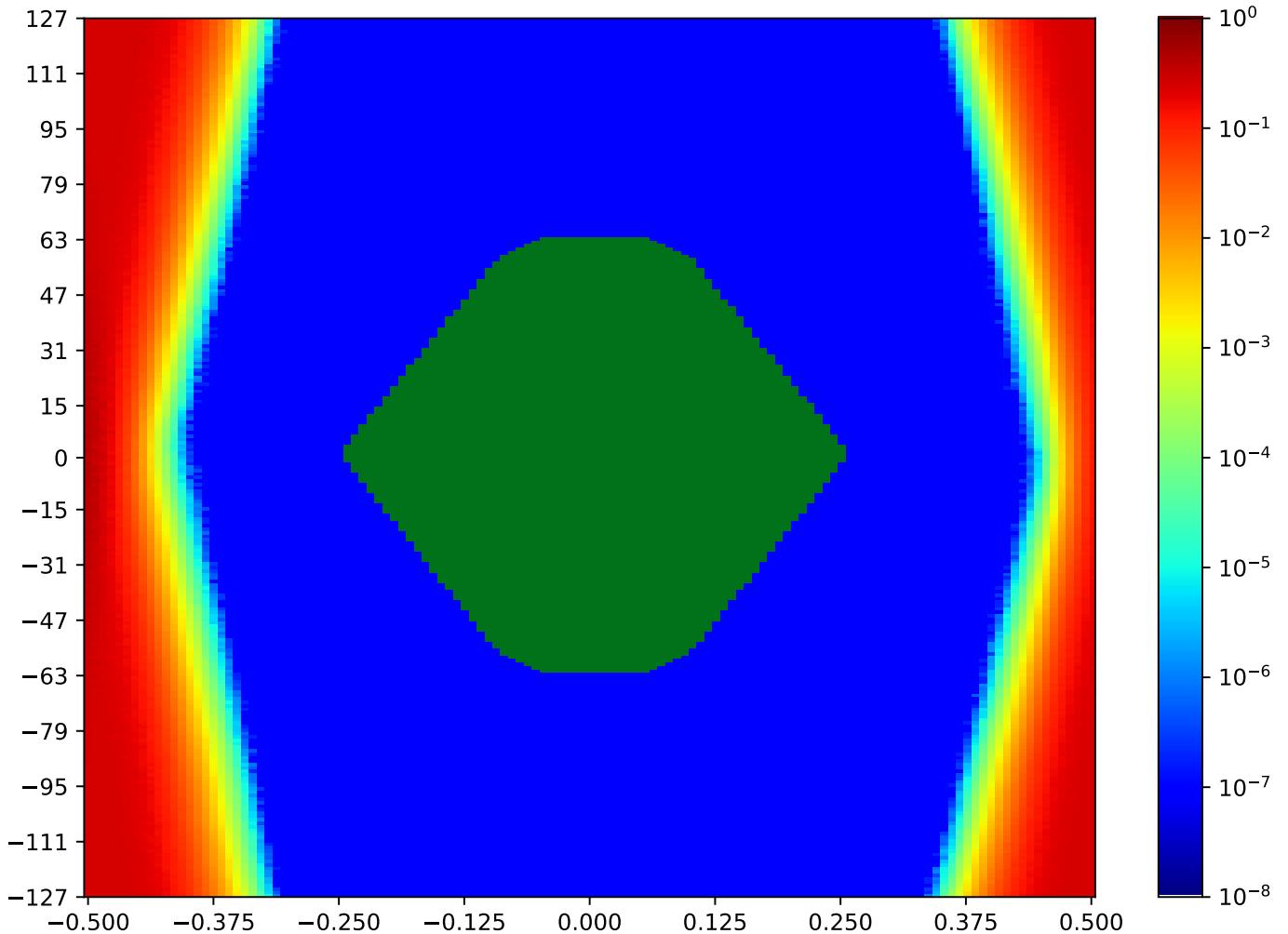


Figure 2.7: MSP_A_FPGA-TX1-05-RX16-05-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.7 MSP_A_FPGA-TX1-06-RX16-06-MSP_C_FPGA

Table 2.7: MSP_A_FPGA-TX1-06-RX16-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:11:04		2018-Jan-24 03:12:14	
Reset RX	OA	HO		HO (%)	
true	24471	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

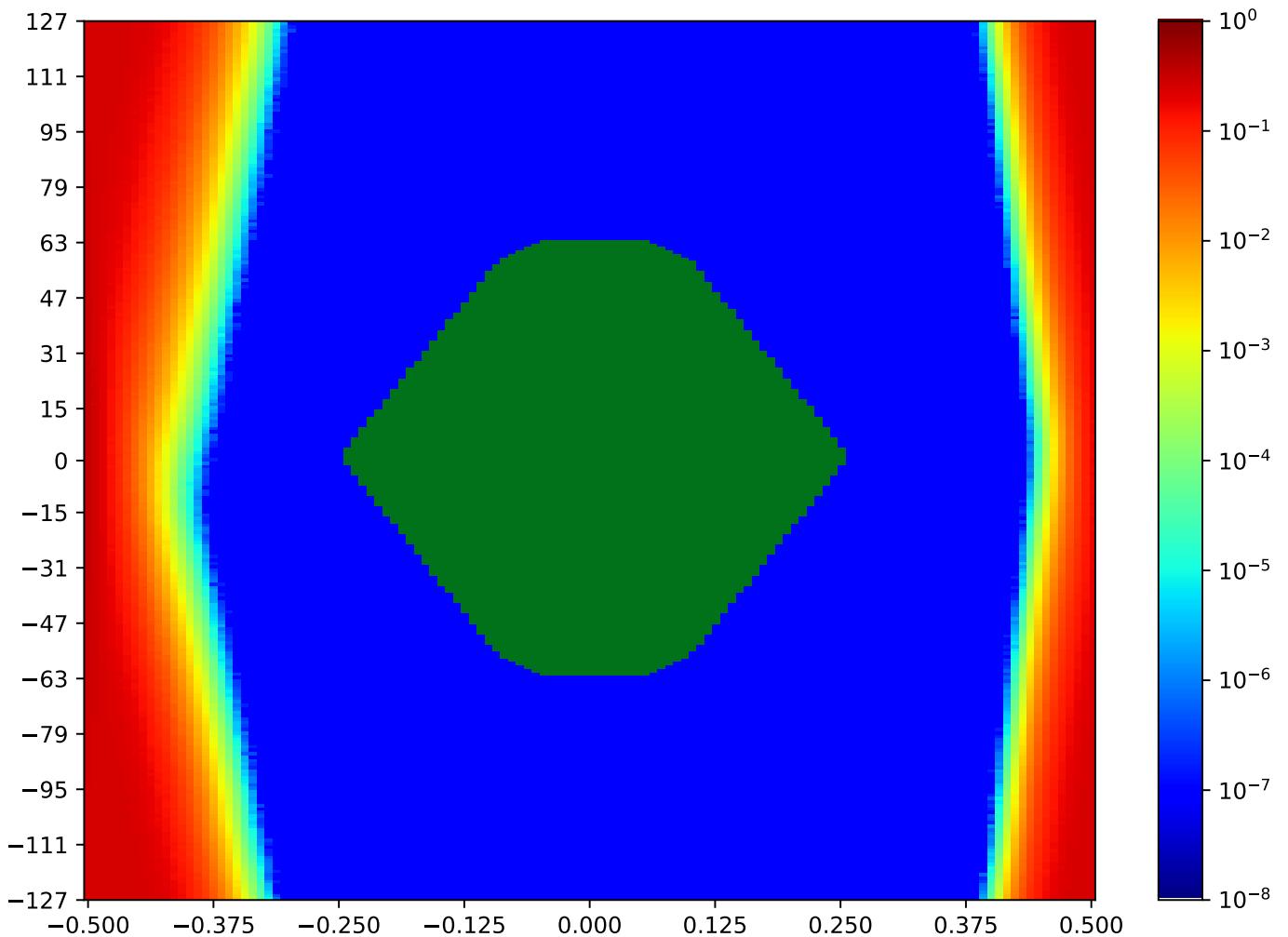


Figure 2.8: MSP_A_FPGA-TX1-06-RX16-06-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.8 MSP_A_FPGA-TX1-07-RX16-07-MSP_C_FPGA

Table 2.8: MSP_A_FPGA-TX1-07-RX16-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:00:35		2018-Jan-24 03:01:44	
Reset RX	OA	HO		HO (%)	
true	23737	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

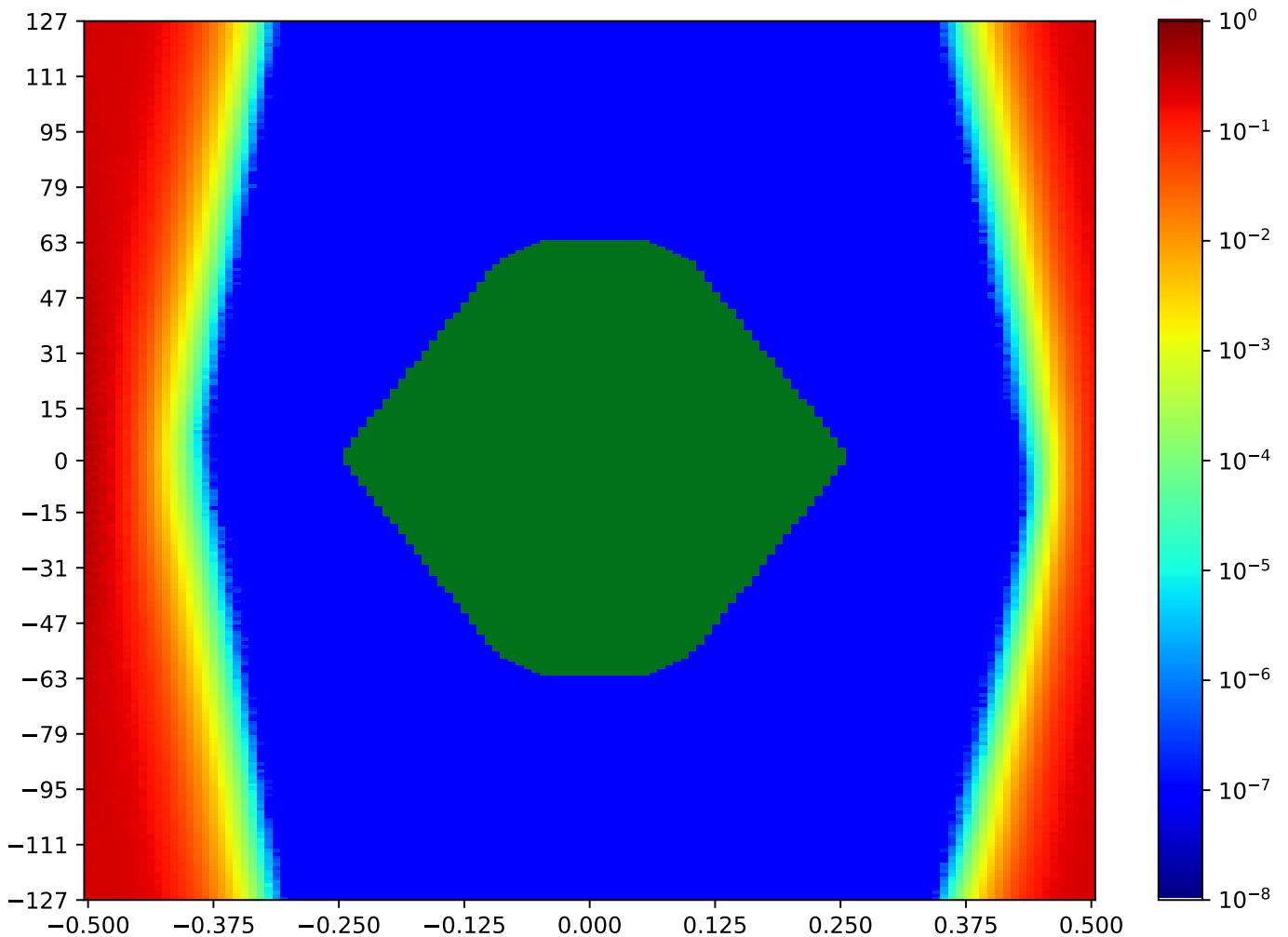


Figure 2.9: MSP_A_FPGA-TX1-07-RX16-07-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.9 MSP_A_FPGA-TX1-08-RX16-08-MSP_C_FPGA

Table 2.9: MSP_A_FPGA-TX1-08-RX16-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:09:54		2018-Jan-24 03:11:04	
Reset RX	OA	HO		HO (%)	
true	24784	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

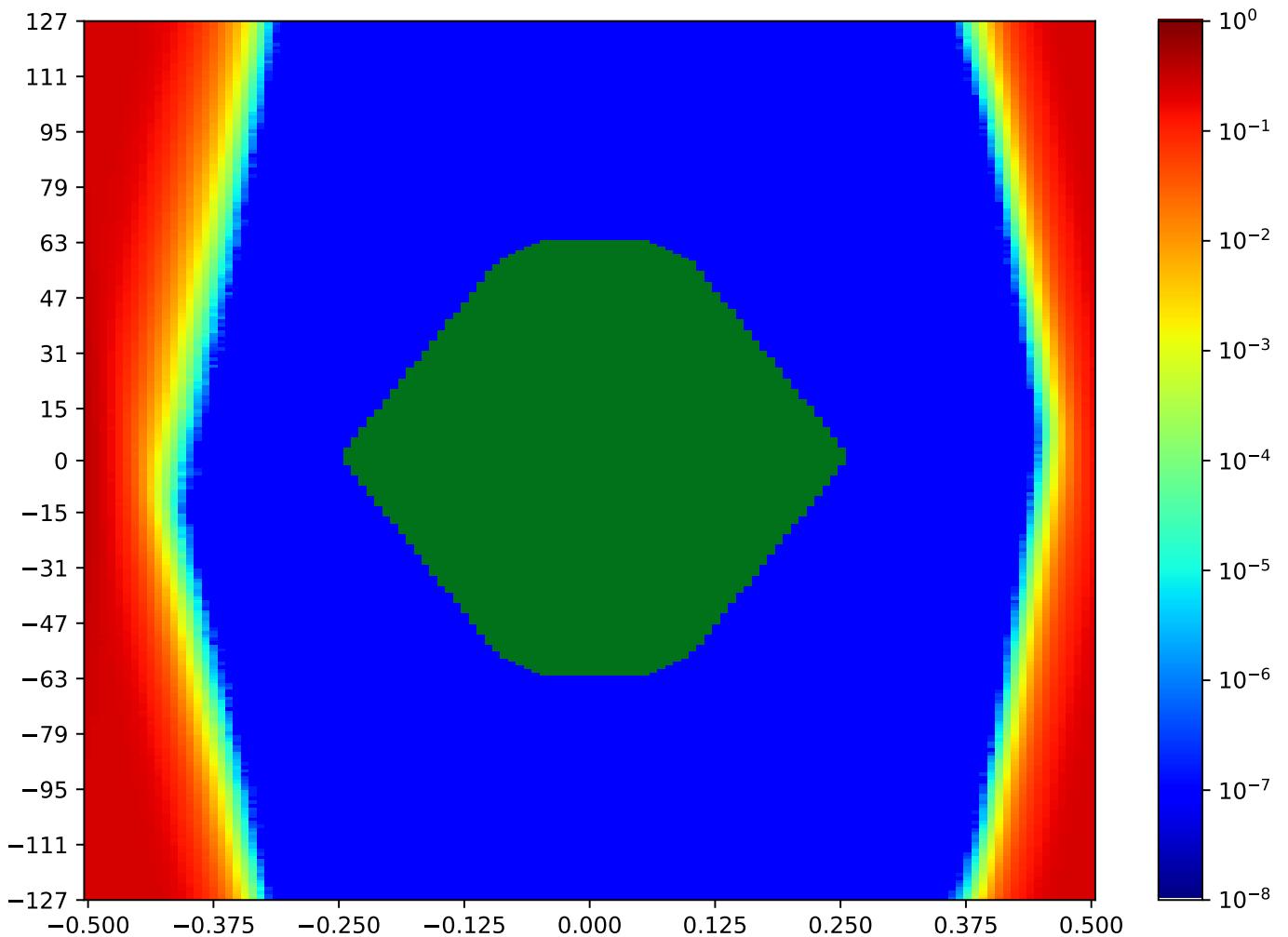


Figure 2.10: MSP_A_FPGA-TX1-08-RX16-08-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.10 MSP_A_FPGA-TX1-09-RX16-09-MSP_C_FPGA

Table 2.10: MSP_A_FPGA-TX1-09-RX16-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:02:56		2018-Jan-24 03:04:07	
Reset RX	OA	HO		HO (%)	
true	25174	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

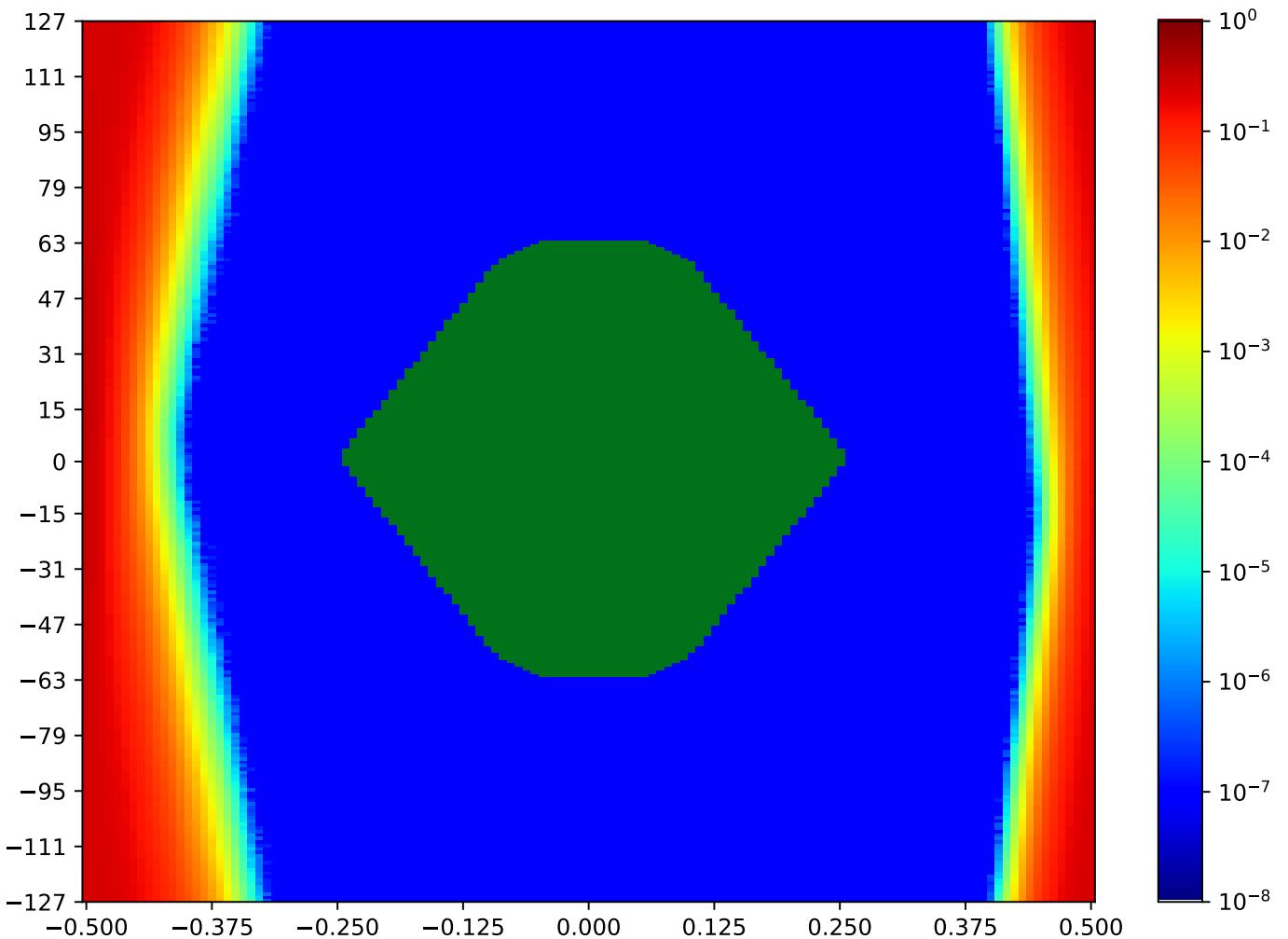


Figure 2.11: MSP_A_FPGA-TX1-09-RX16-09-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.11 MSP_A_FPGA-TX1-10-RX16-10-MSP_C_FPGA

Table 2.11: MSP_A_FPGA-TX1-10-RX16-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:07:34		2018-Jan-24 03:08:45	
Reset RX	OA	HO		HO (%)	
true	25665	110		84.50%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

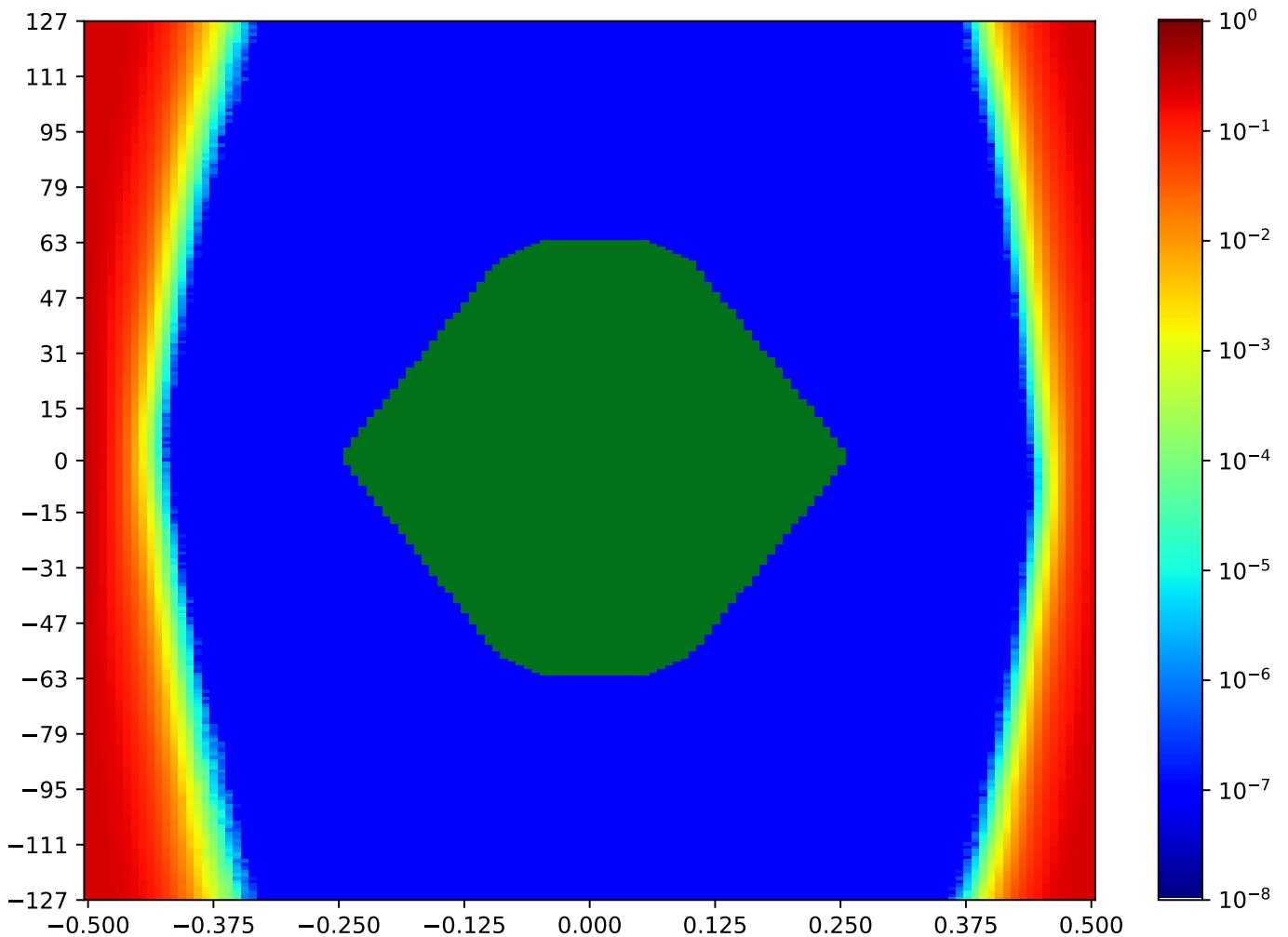


Figure 2.12: MSP_A_FPGA-TX1-10-RX16-10-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.1.12 MSP_A_FPGA-TX1-11-RX16-11-MSP_C_FPGA

Table 2.12: MSP_A_FPGA-TX1-11-RX16-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:06:25		2018-Jan-24 03:07:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23816	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

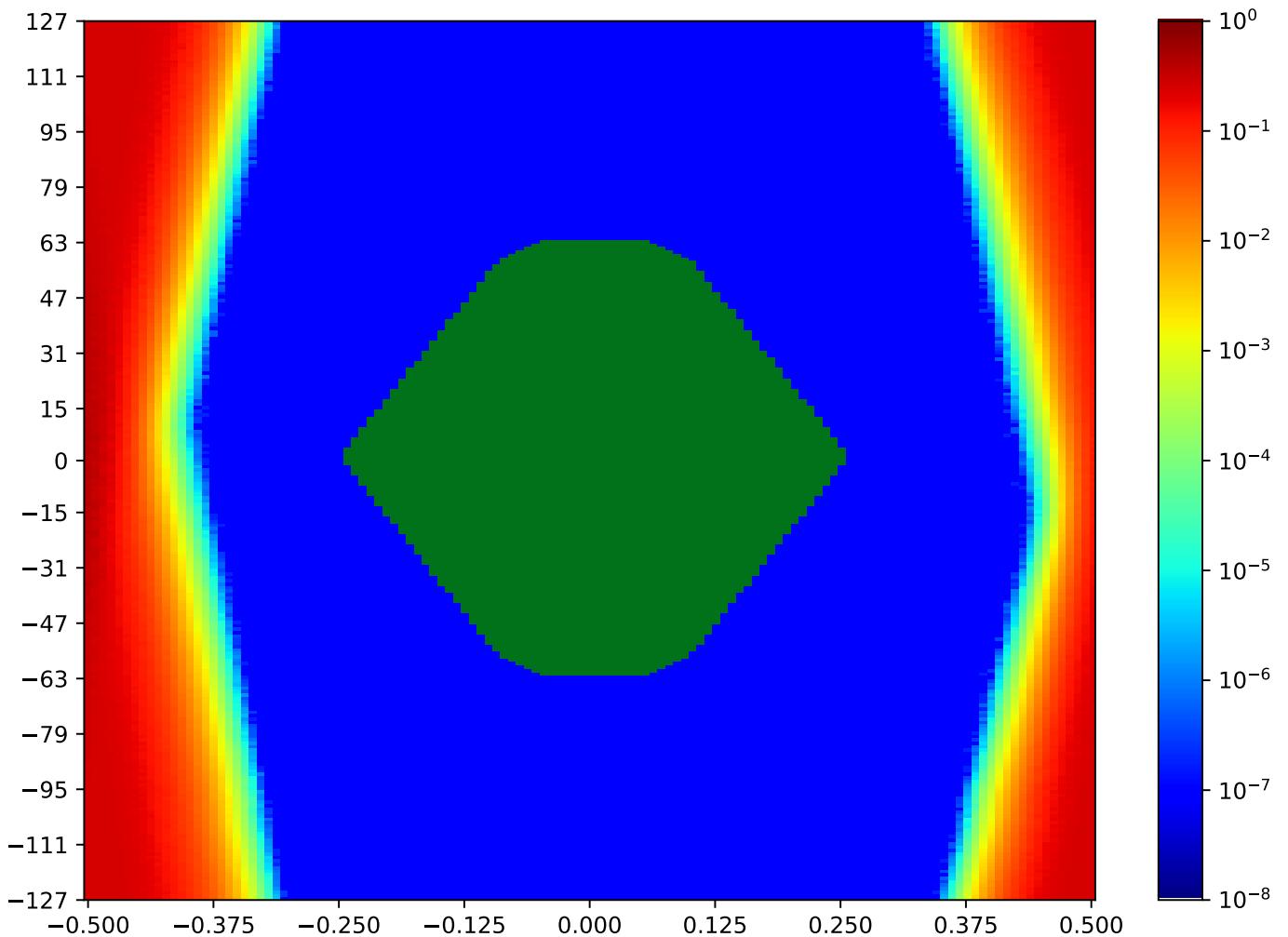


Figure 2.13: MSP_A_FPGA-TX1-11-RX16-11-MSP_C_FPGA

Call back to summary Figure 2.1. Sibling eye diagrams: V1-12.8.

2.2 MSP_A TX2 MSP_C RX15 Minipod Loopback

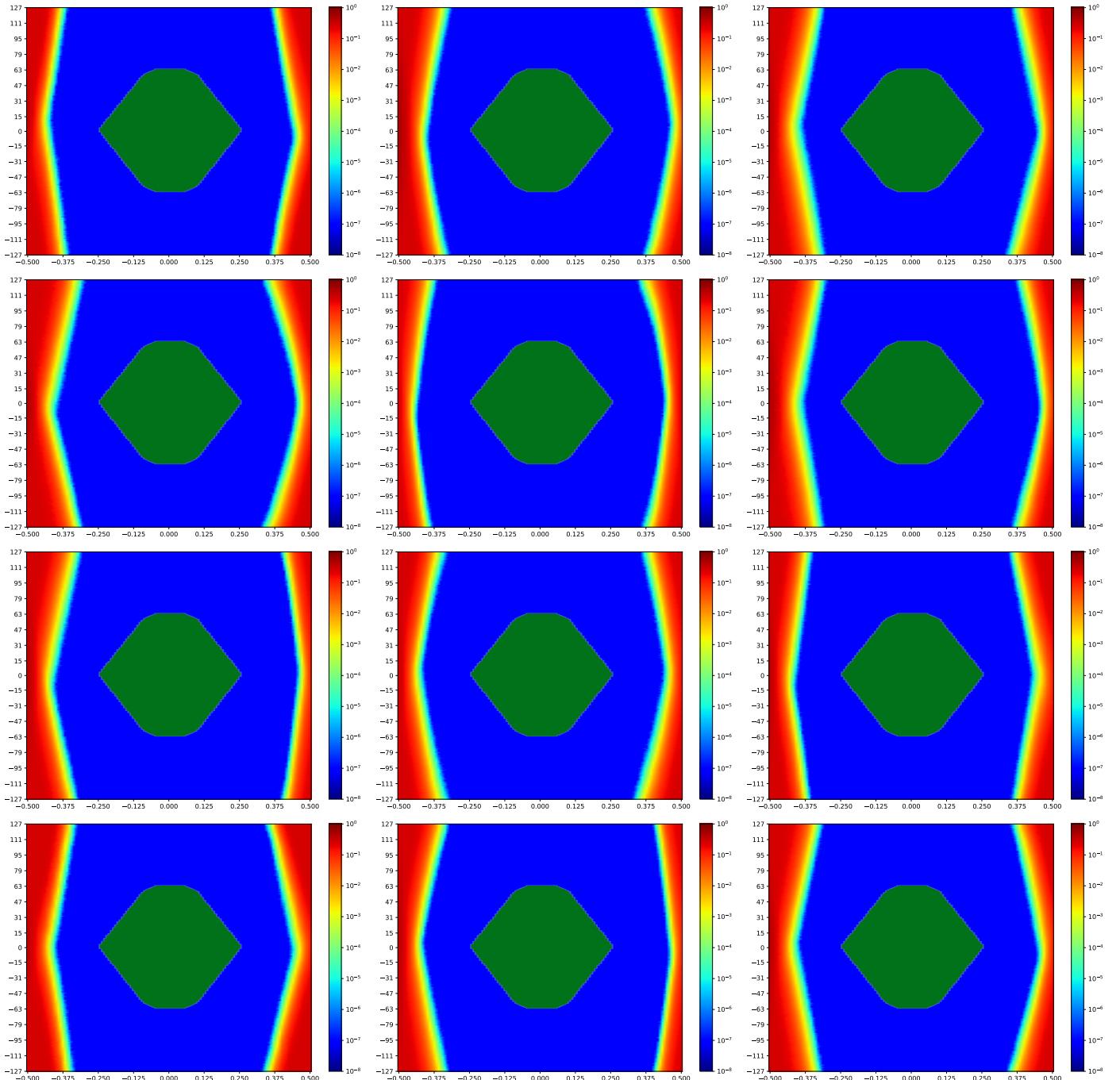


Figure 2.14: MSP_A TX2 MSP_C RX15 Minipod Loopback

A cross-reference to Figure 2.14. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.27.

2.2.1 MSP_A_FPGA-TX2-00-RX15-00-MSP_C_FPGA

Table 2.13: MSP_A_FPGA-TX2-00-RX15-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:15:44		2018-Jan-24 03:16:54	
Reset RX	OA	HO		HO (%)	
true	25122	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

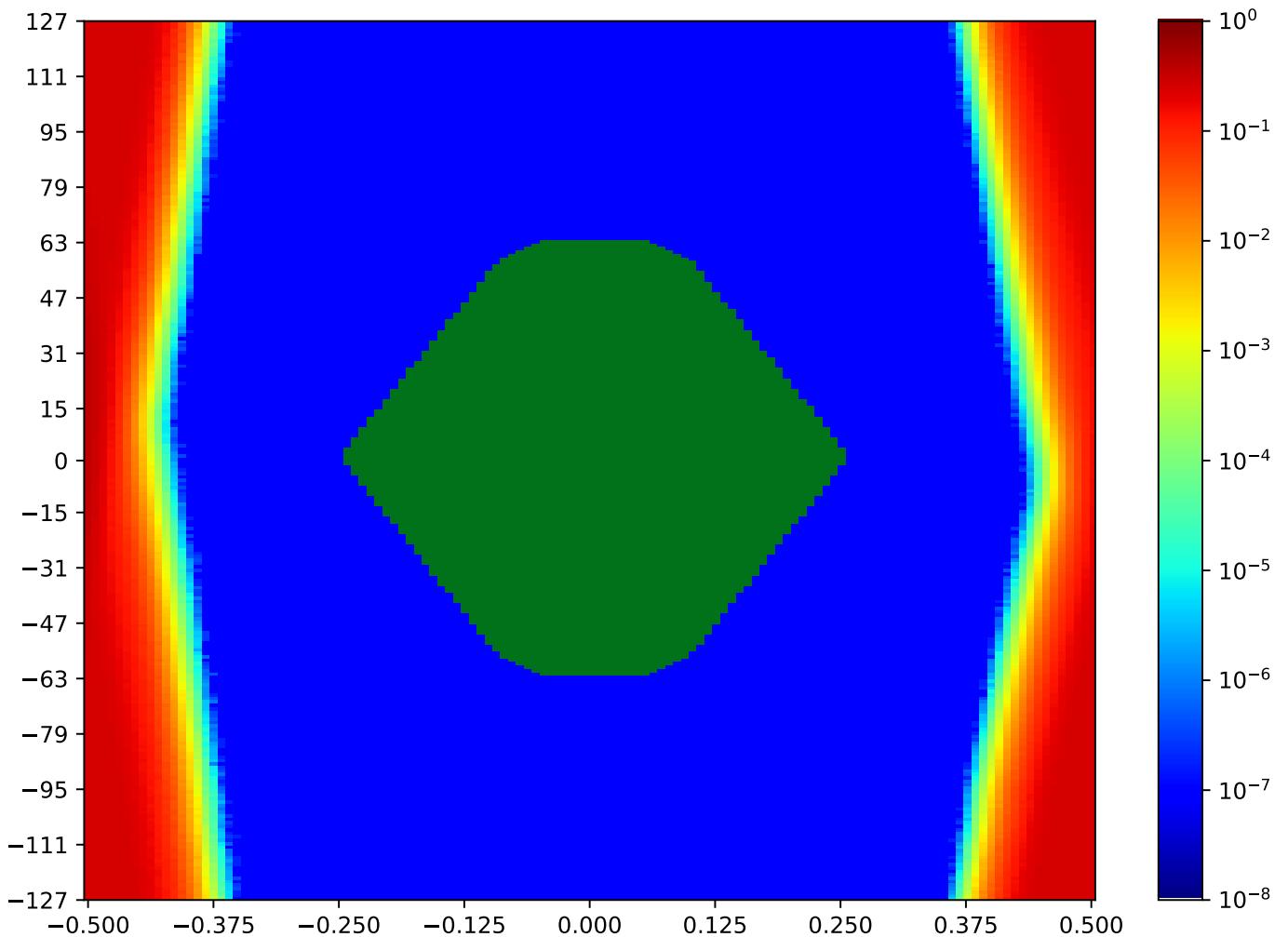


Figure 2.15: MSP_A_FPGA-TX2-00-RX15-00-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.2 MSP_A_FPGA-TX2-01-RX15-01-MSP_C_FPGA

Table 2.14: MSP_A_FPGA-TX2-01-RX15-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:13:24		2018-Jan-24 03:14:34	
Reset RX	OA	HO		HO (%)	
true	24923	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

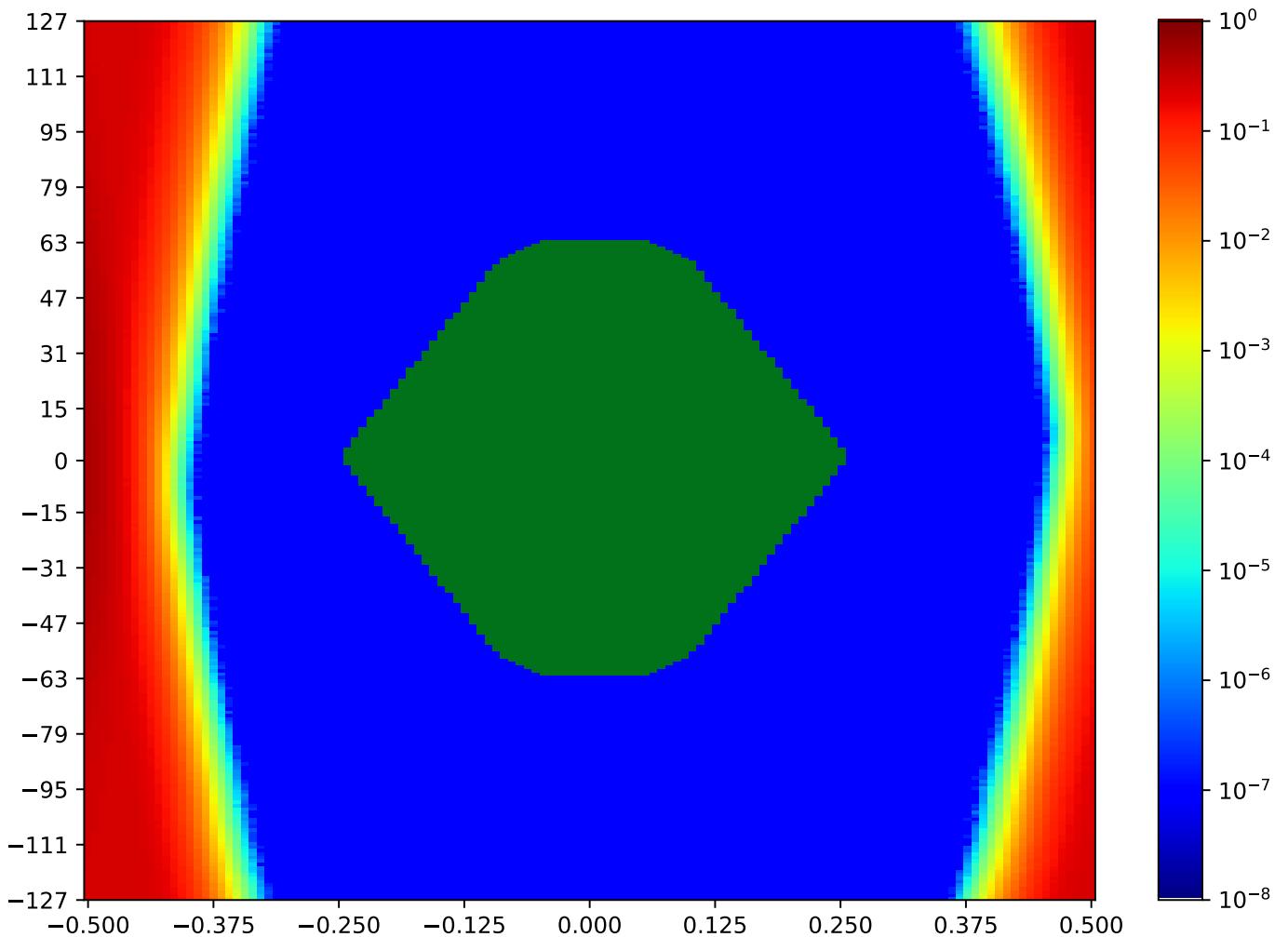


Figure 2.16: MSP_A_FPGA-TX2-01-RX15-01-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.3 MSP_A_FPGA-TX2-02-RX15-02-MSP_C_FPGA

Table 2.15: MSP_A_FPGA-TX2-02-RX15-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:19:16		2018-Jan-24 03:20:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23533	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

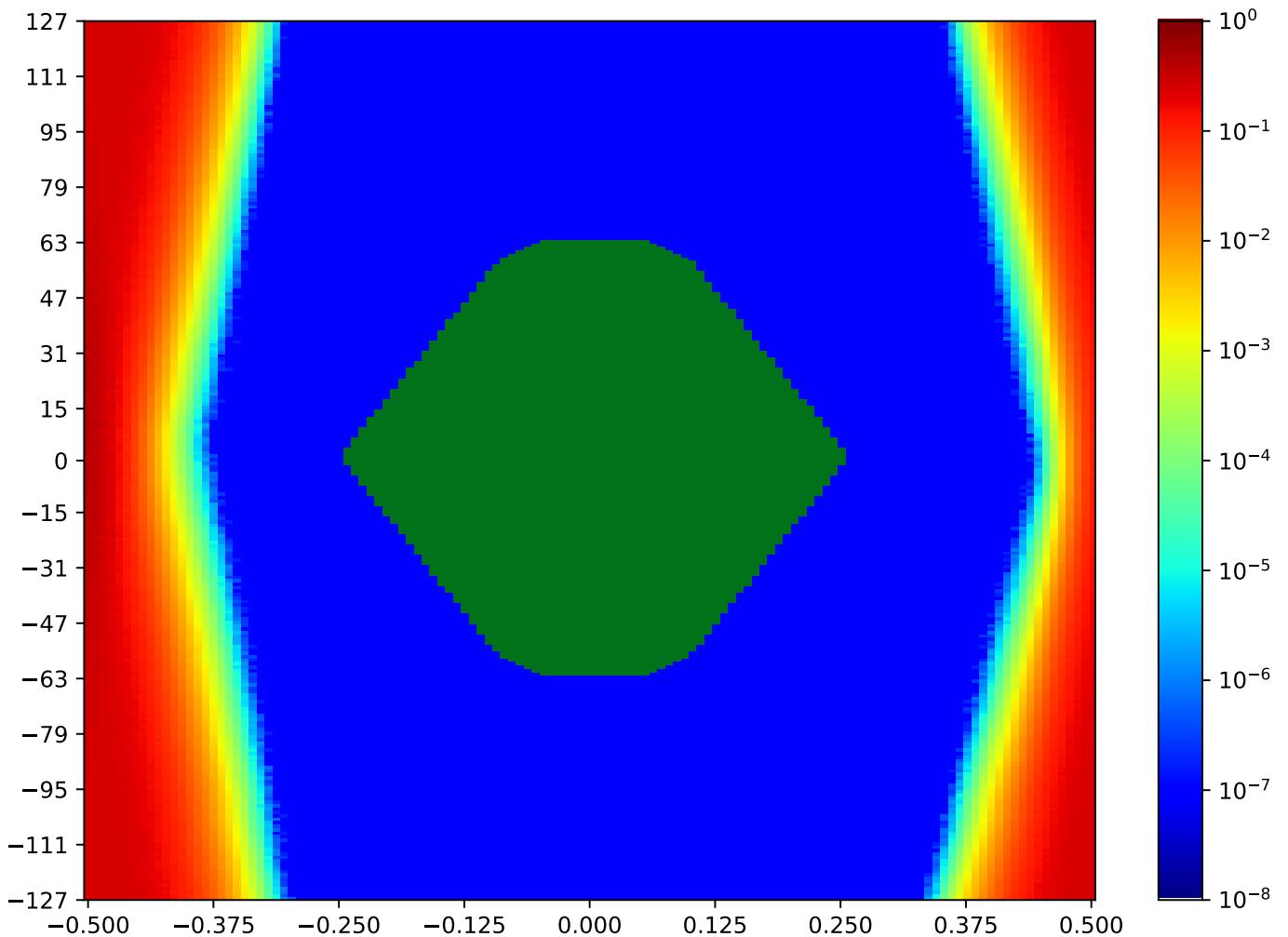


Figure 2.17: MSP_A_FPGA-TX2-02-RX15-02-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.4 MSP_A_FPGA-TX2-03-RX15-03-MSP_C_FPGA

Table 2.16: MSP_A_FPGA-TX2-03-RX15-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:12:14		2018-Jan-24 03:13:24	
Reset RX	OA	HO		HO (%)	
true	23818	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

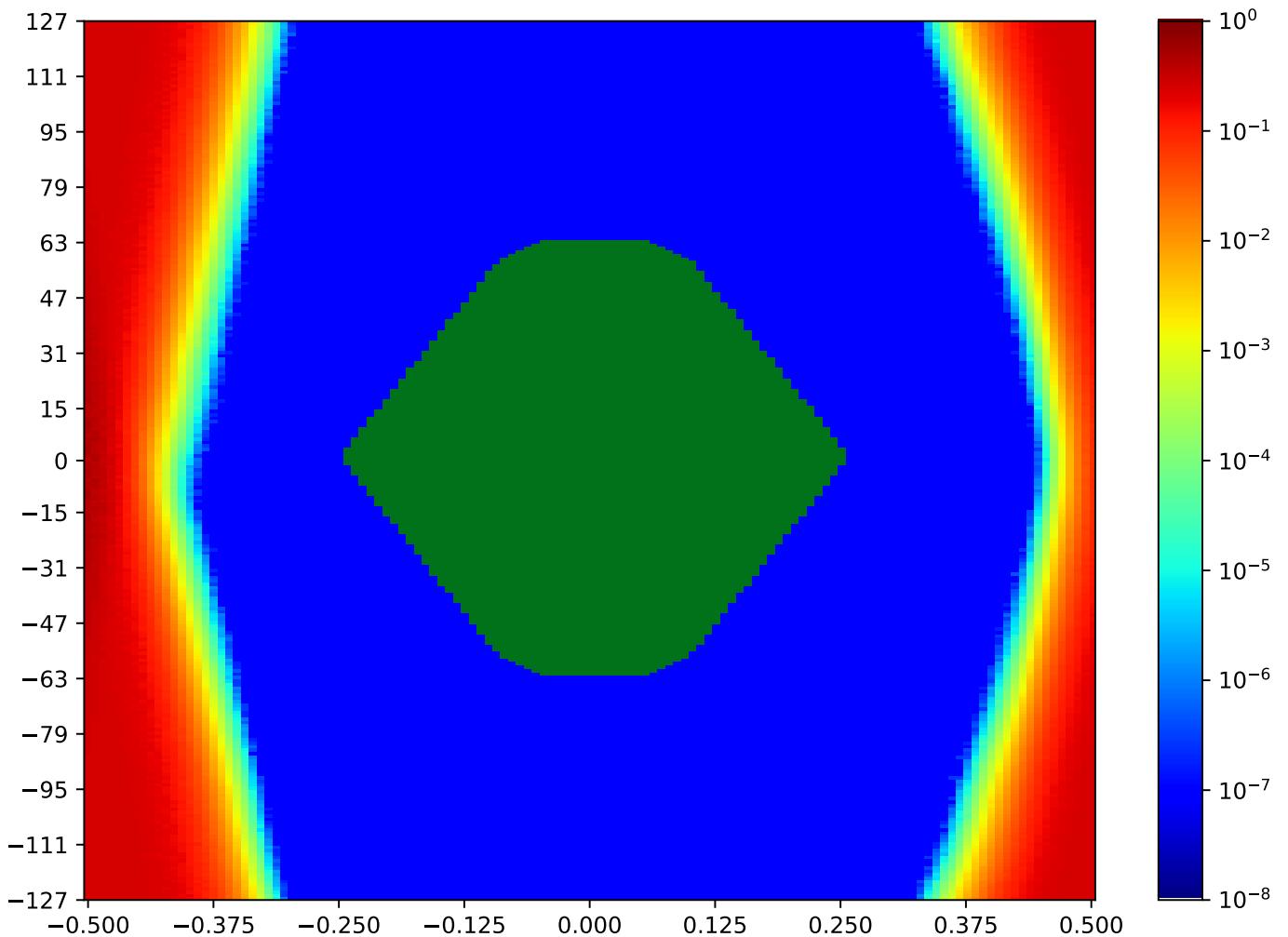


Figure 2.18: MSP_A_FPGA-TX2-03-RX15-03-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.5 MSP_A_FPGA-TX2-04-RX15-04-MSP_C_FPGA

Table 2.17: MSP_A_FPGA-TX2-04-RX15-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:22:48		2018-Jan-24 03:24:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26054	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

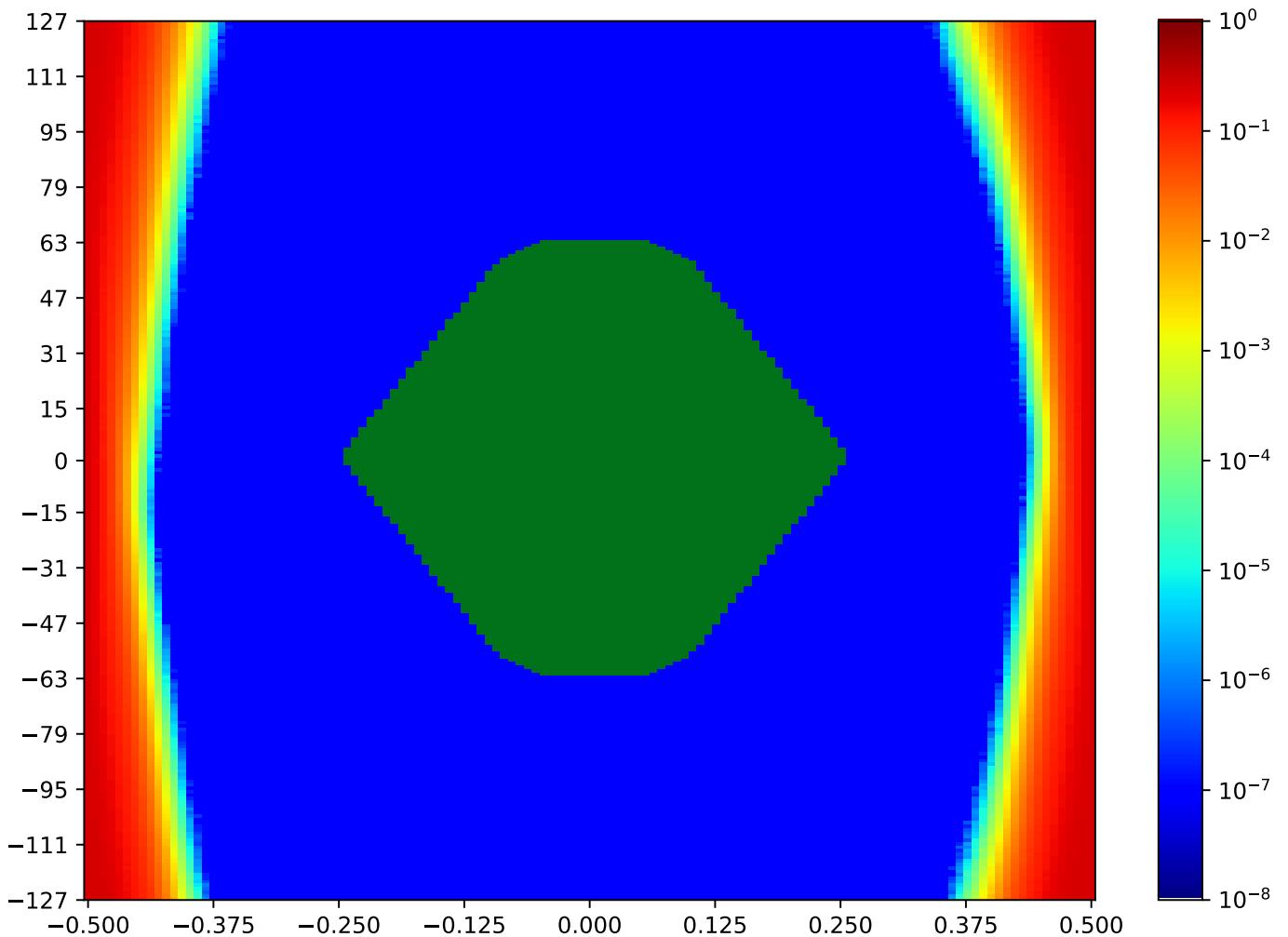


Figure 2.19: MSP_A_FPGA-TX2-04-RX15-04-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.6 MSP_A_FPGA-TX2-05-RX15-05-MSP_C_FPGA

Table 2.18: MSP_A_FPGA-TX2-05-RX15-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:14:34		2018-Jan-24 03:15:44	
Reset RX	OA	HO		HO (%)	
true	24033	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

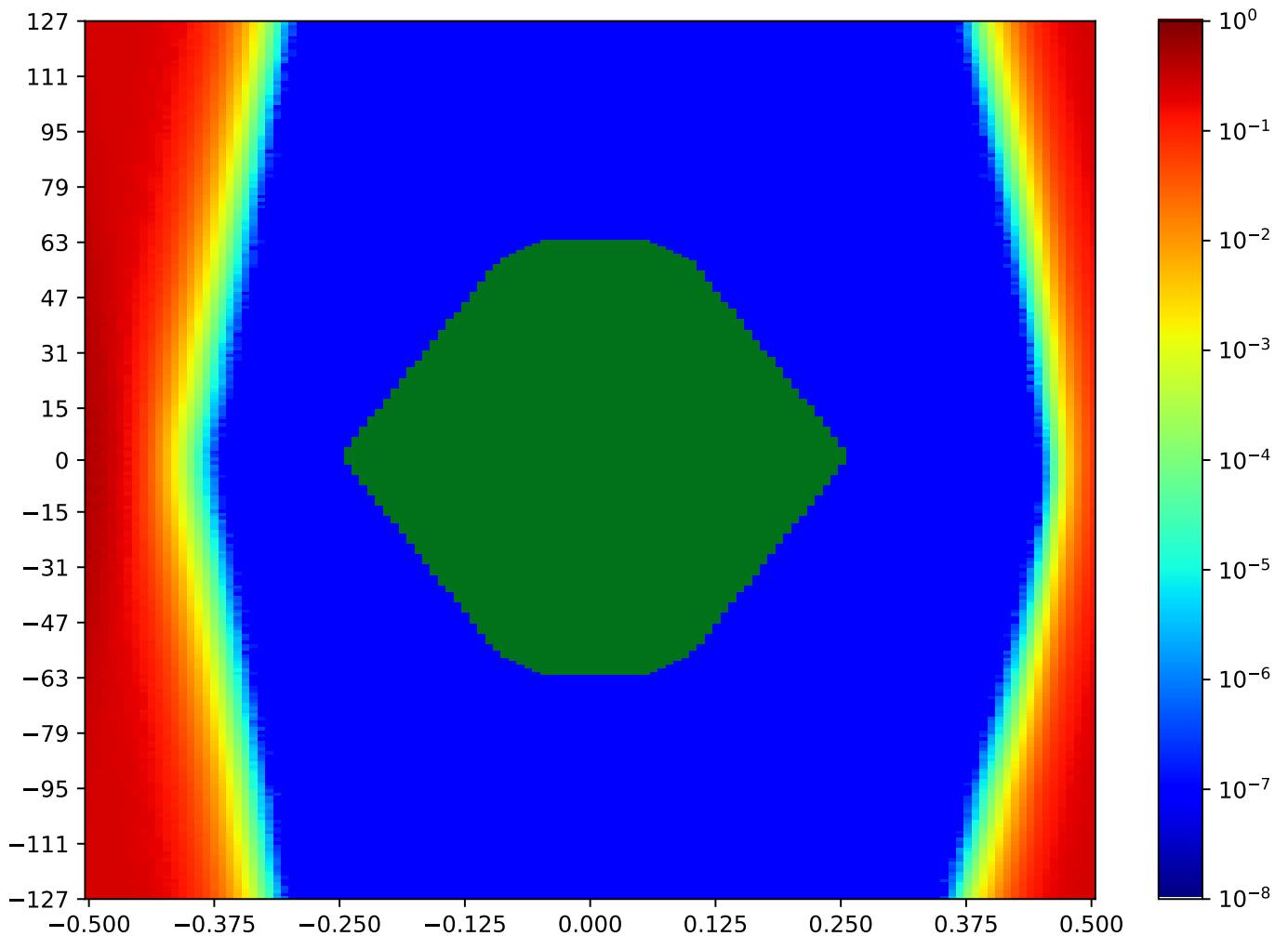


Figure 2.20: MSP_A_FPGA-TX2-05-RX15-05-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.7 MSP_A_FPGA-TX2-06-RX15-06-MSP_C_FPGA

Table 2.19: MSP_A_FPGA-TX2-06-RX15-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:25:11		2018-Jan-24 03:26:23	
Reset RX	OA	HO		HO (%)	
true	25298	107		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

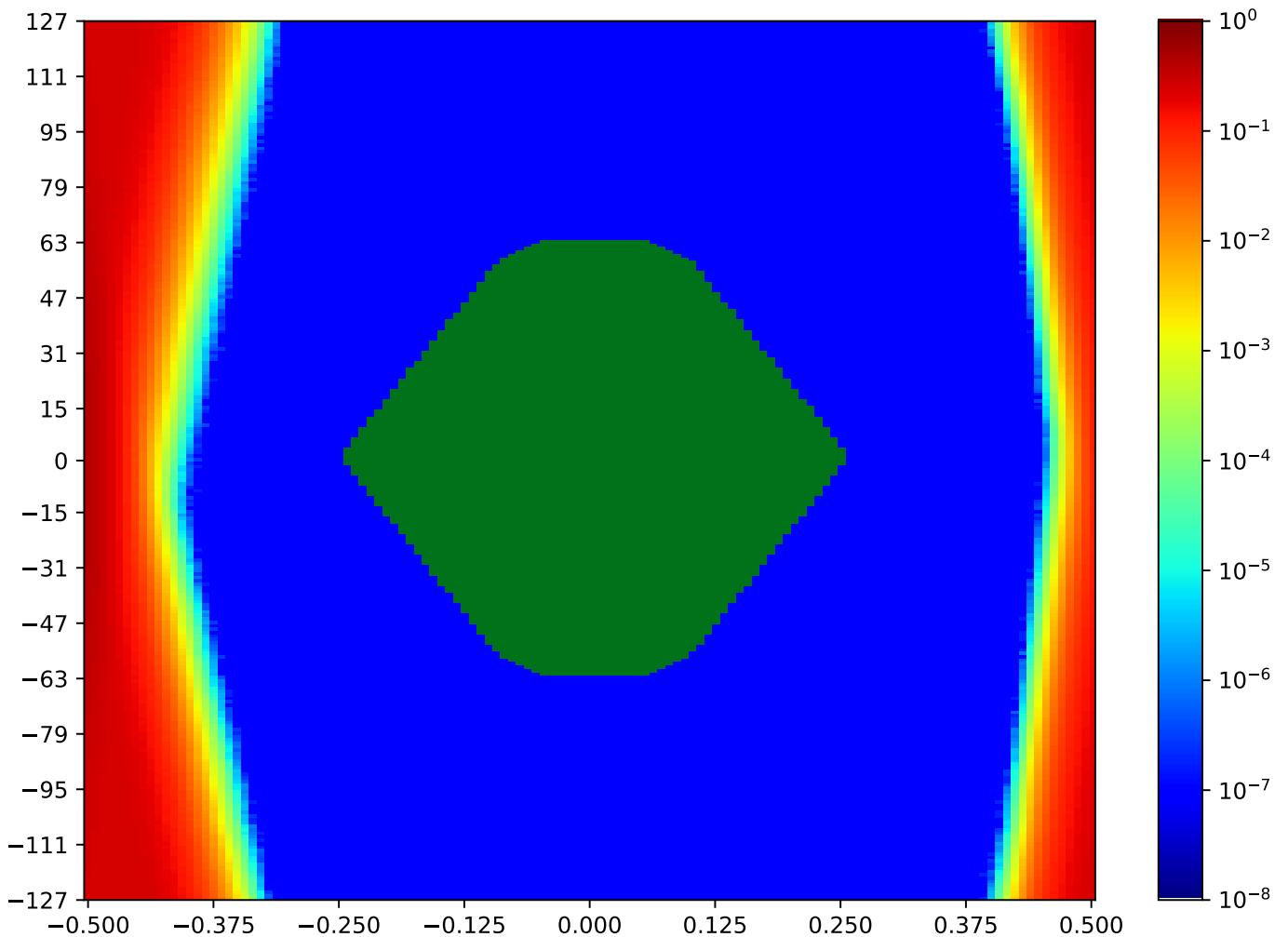


Figure 2.21: MSP_A_FPGA-TX2-06-RX15-06-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.8 MSP_A_FPGA-TX2-07-RX15-07-MSP_C_FPGA

Table 2.20: MSP_A_FPGA-TX2-07-RX15-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:16:54		2018-Jan-24 03:18:06	
Reset RX	OA	HO		HO (%)	
true	24574	107		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

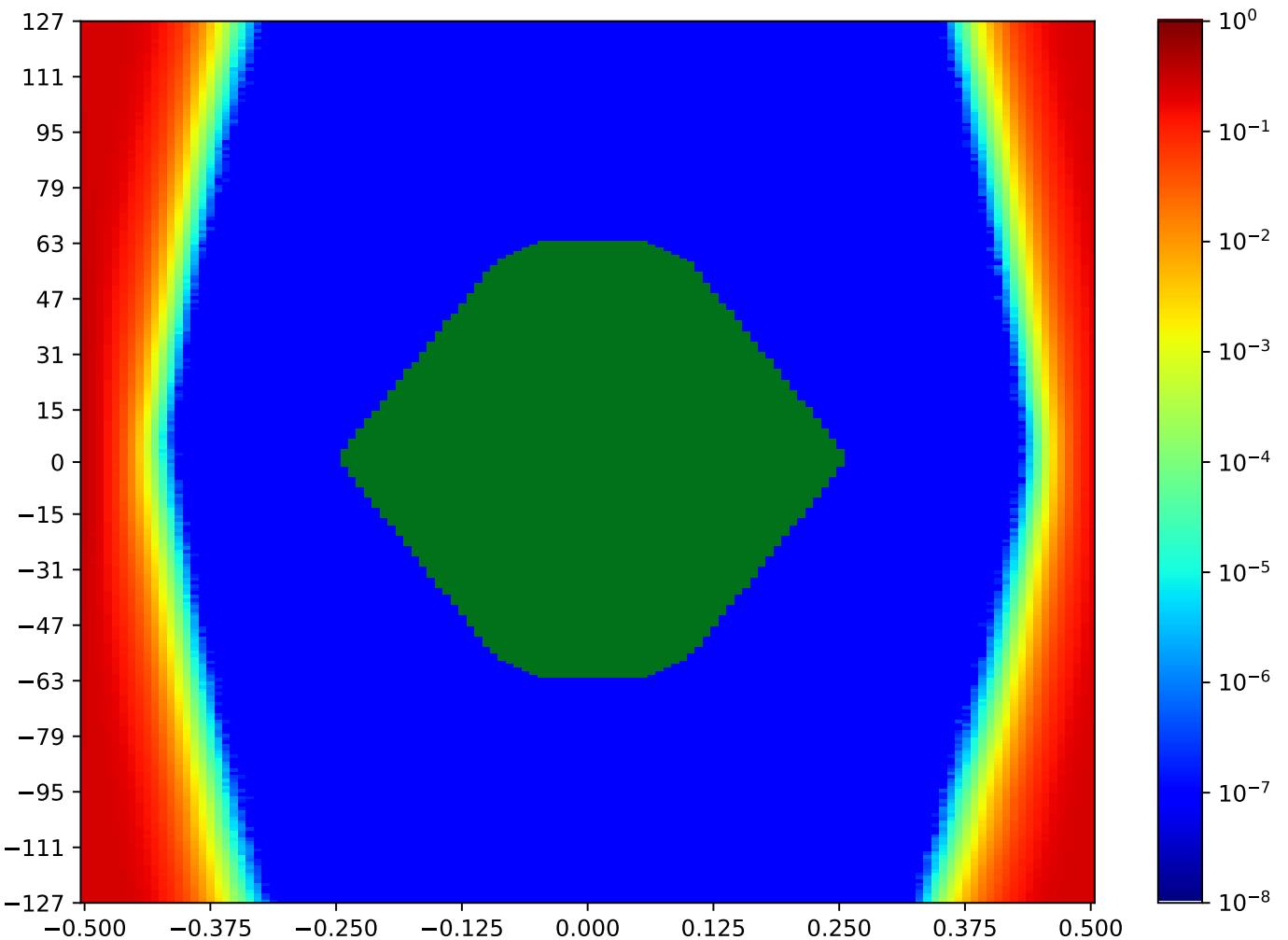


Figure 2.22: MSP_A_FPGA-TX2-07-RX15-07-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.9 MSP_A_FPGA-TX2-08-RX15-08-MSP_C_FPGA

Table 2.21: MSP_A_FPGA-TX2-08-RX15-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:24:00		2018-Jan-24 03:25:11	
Reset RX	OA	HO		VO VO (%)	
true	24627	104		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

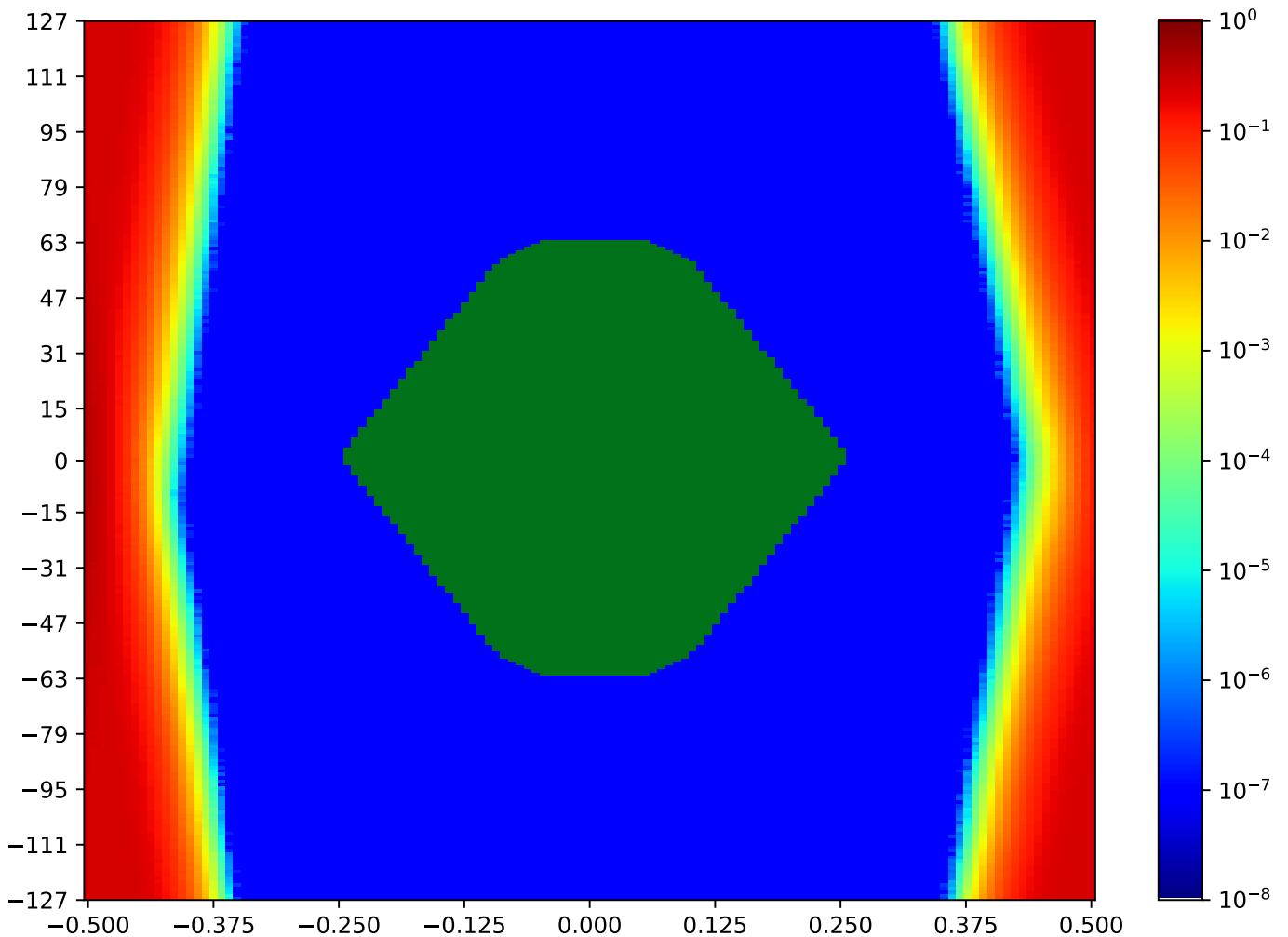


Figure 2.23: MSP_A_FPGA-TX2-08-RX15-08-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.10 MSP_A_FPGA-TX2-09-RX15-09-MSP_C_FPGA

Table 2.22: MSP_A_FPGA-TX2-09-RX15-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:18:06		2018-Jan-24 03:19:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23995	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

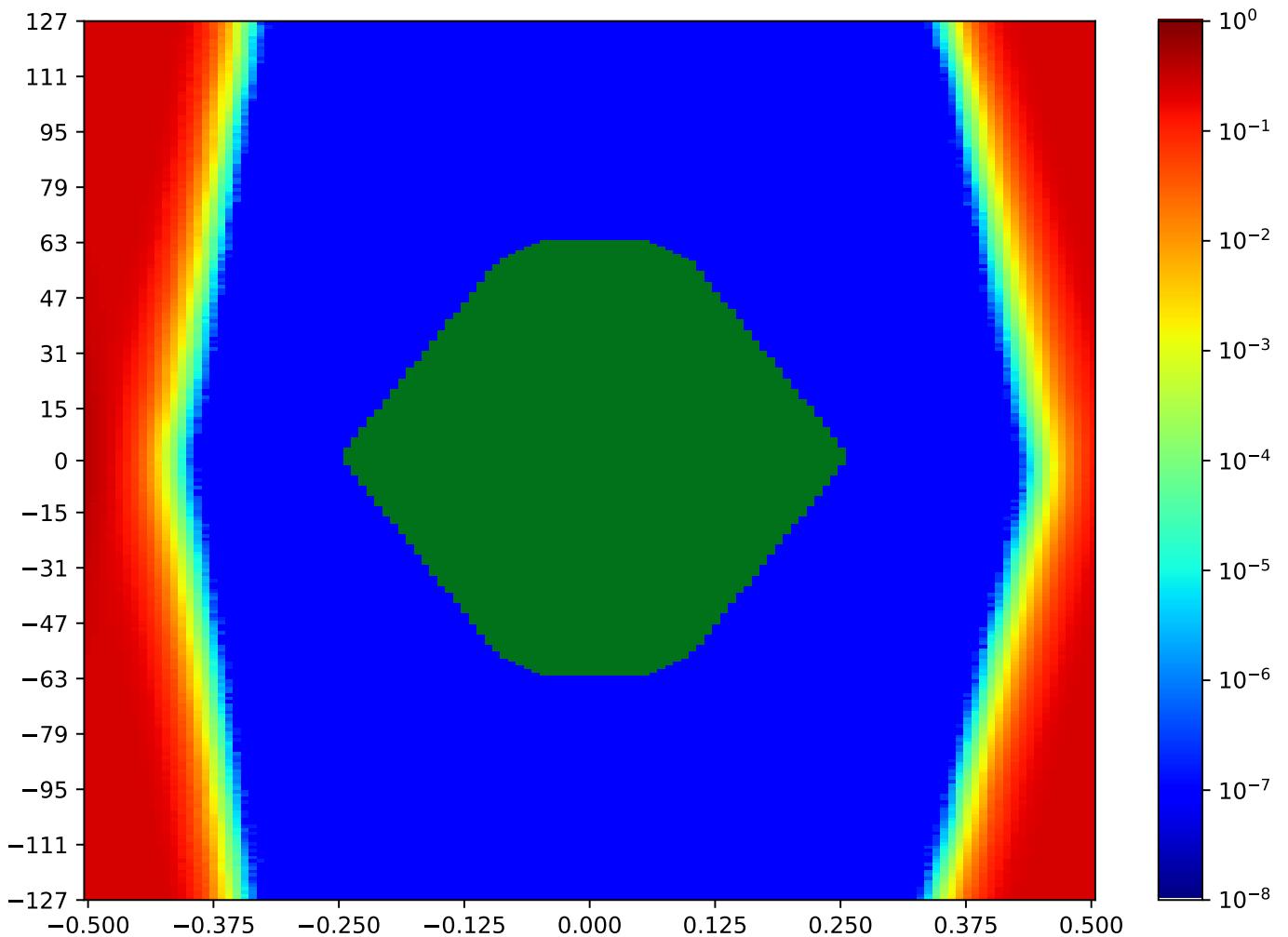


Figure 2.24: MSP_A_FPGA-TX2-09-RX15-09-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.11 MSP_A_FPGA-TX2-10-RX15-10-MSP_C_FPGA

Table 2.23: MSP_A_FPGA-TX2-10-RX15-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:21:36		2018-Jan-24 03:22:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25713	108	83.72%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

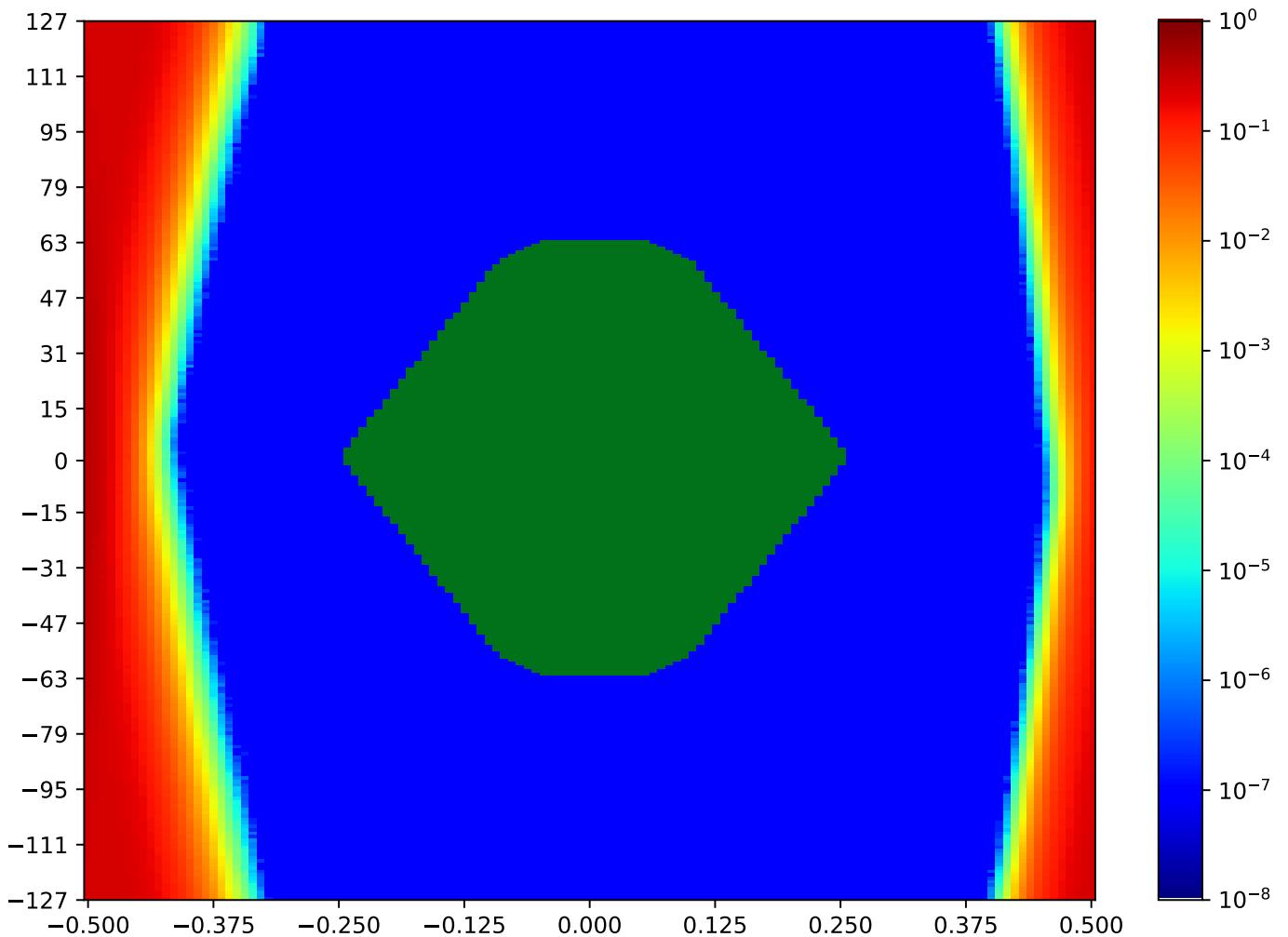


Figure 2.25: MSP_A_FPGA-TX2-10-RX15-10-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.2.12 MSP_A_FPGA-TX2-11-RX15-11-MSP_C_FPGA

Table 2.24: MSP_A_FPGA-TX2-11-RX15-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:20:26		2018-Jan-24 03:21:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24162	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

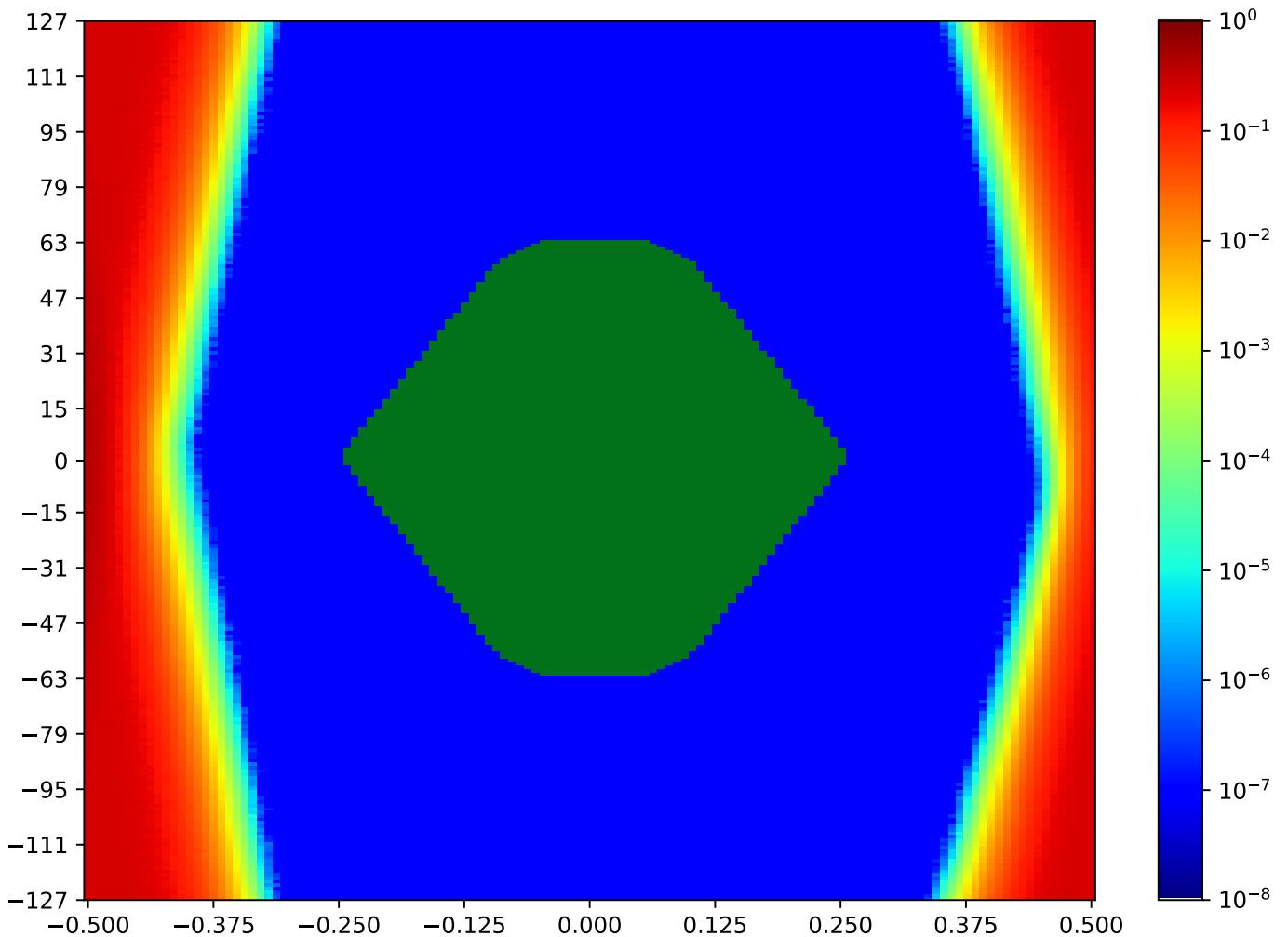


Figure 2.26: MSP_A_FPGA-TX2-11-RX15-11-MSP_C_FPGA

Call back to summary Figure 2.14. Sibling eye diagrams: V1-12.8.

2.3 MSP_C TX3 MSP_A RX7 Minipod Loopback

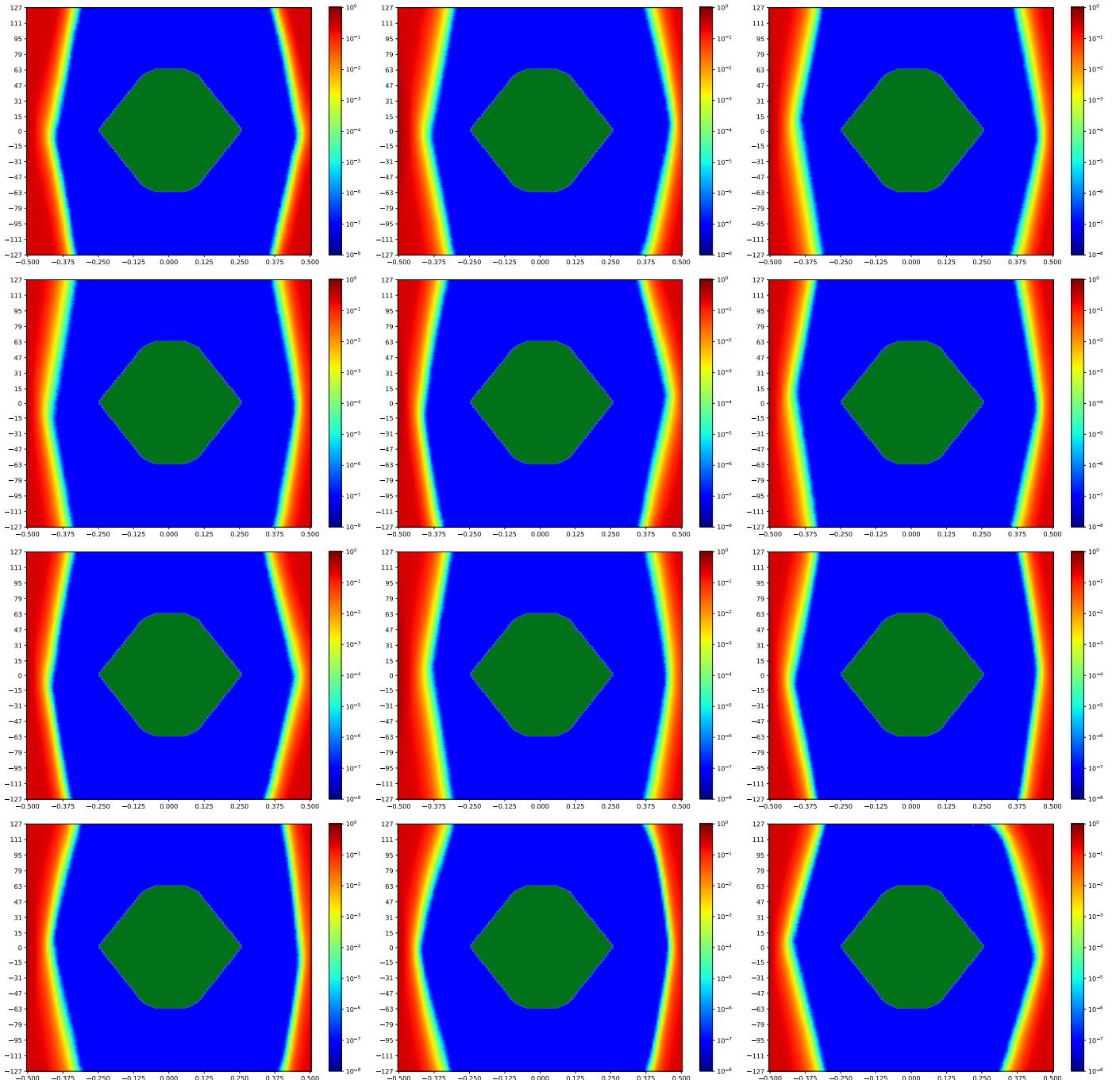


Figure 2.27: MSP_C TX3 MSP_A RX7 Minipod Loopback

A cross-reference to Figure 2.27. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.40.

2.3.1 MSP_C_FPGA-TX3-00-RX7-00-MSP_A_FPGA

Table 2.25: MSP_C_FPGA-TX3-00-RX7-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:29:54		2018-Jan-24 03:31:04	
Reset RX	OA	HO		HO (%)	
true	24473	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

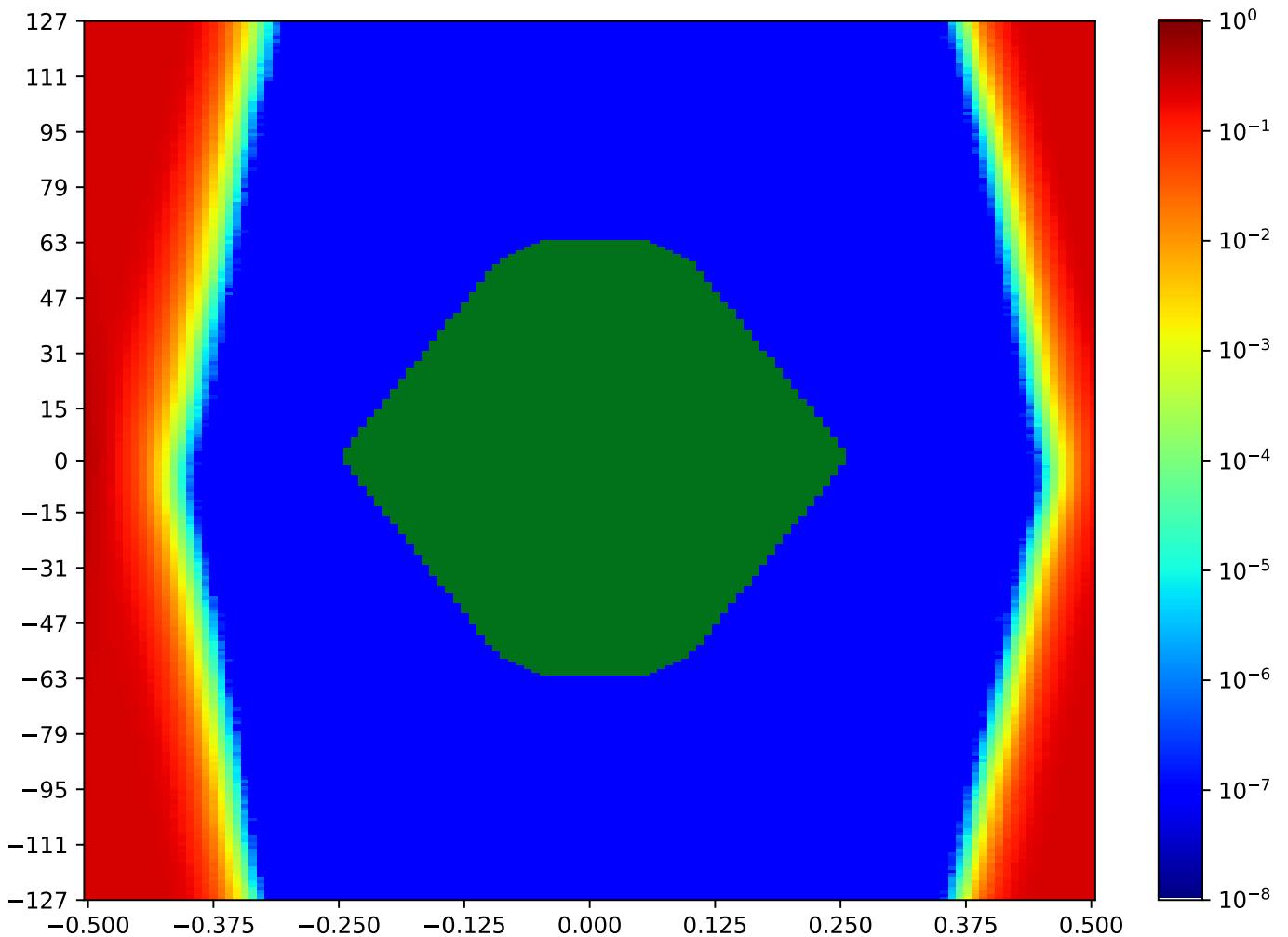


Figure 2.28: MSP_C_FPGA-TX3-00-RX7-00-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.2 MSP_C_FPGA-TX3-01-RX7-01-MSP_A_FPGA

Table 2.26: MSP_C_FPGA-TX3-01-RX7-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:32:15		2018-Jan-24 03:33:25	
Reset RX	OA	HO		HO (%)	
true	24117	105		81.40%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

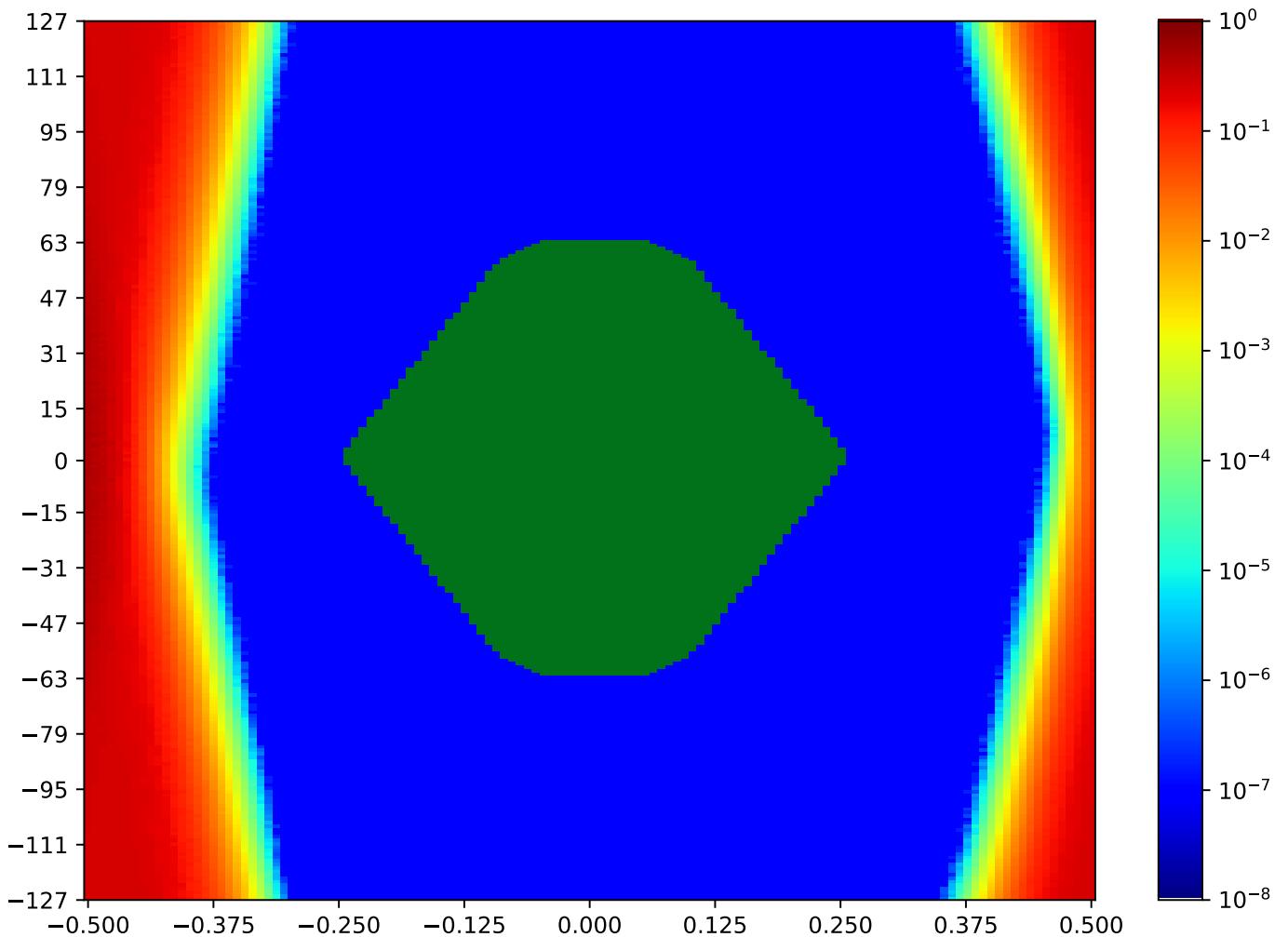


Figure 2.29: MSP_C_FPGA-TX3-01-RX7-01-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.3 MSP_C_FPGA-TX3-02-RX7-02-MSP_A_FPGA

Table 2.27: MSP_C_FPGA-TX3-02-RX7-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:33:25		2018-Jan-24 03:34:35	
Reset RX	OA	HO		HO (%)	
true	24045	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

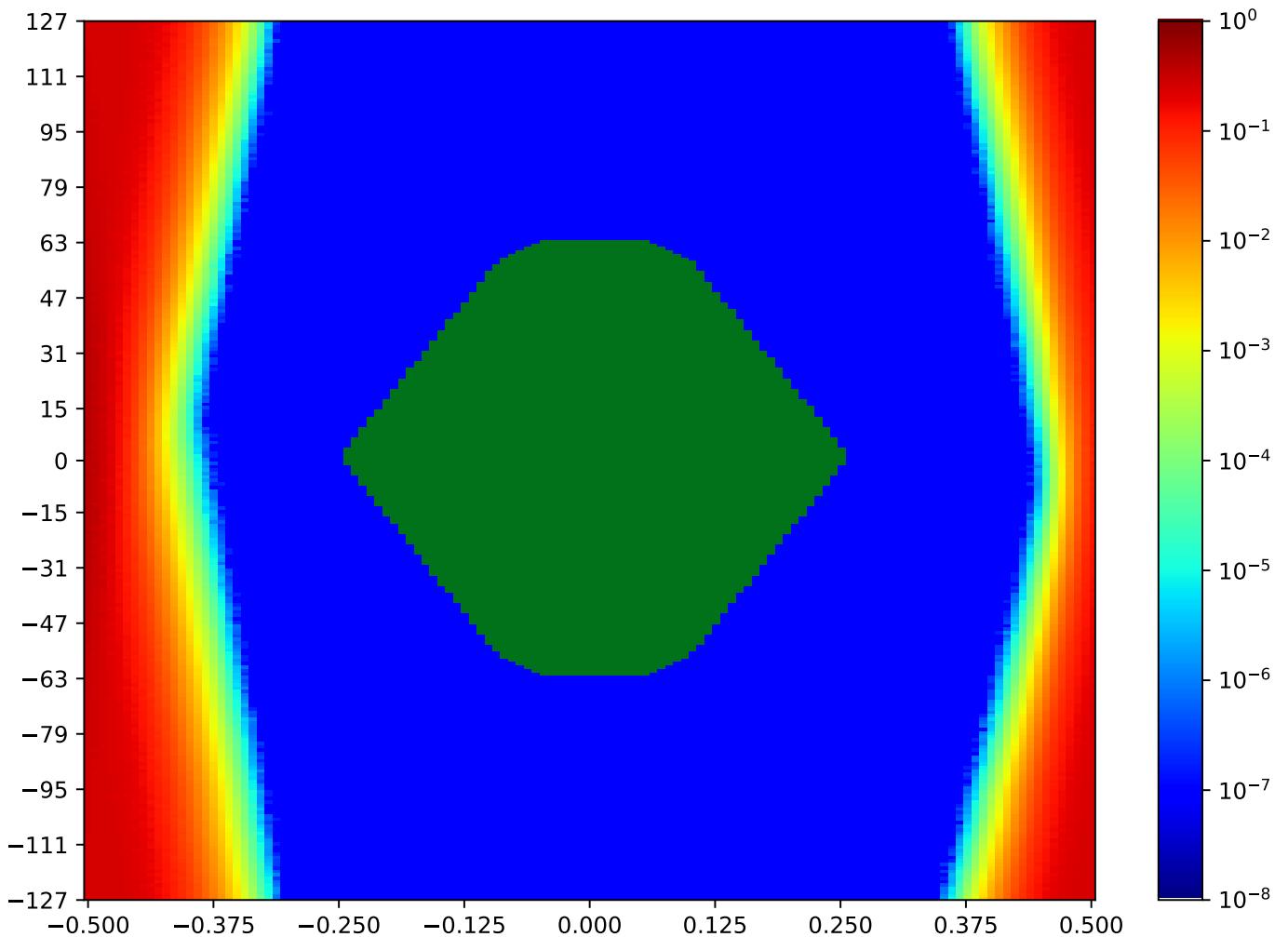


Figure 2.30: MSP_C_FPGA-TX3-02-RX7-02-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.4 MSP_C_FPGA-TX3-03-RX7-03-MSP_A_FPGA

Table 2.28: MSP_C_FPGA-TX3-03-RX7-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:27:34		2018-Jan-24 03:28:45	
Reset RX	OA	HO		HO (%)	
true	24759	105		81.40%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

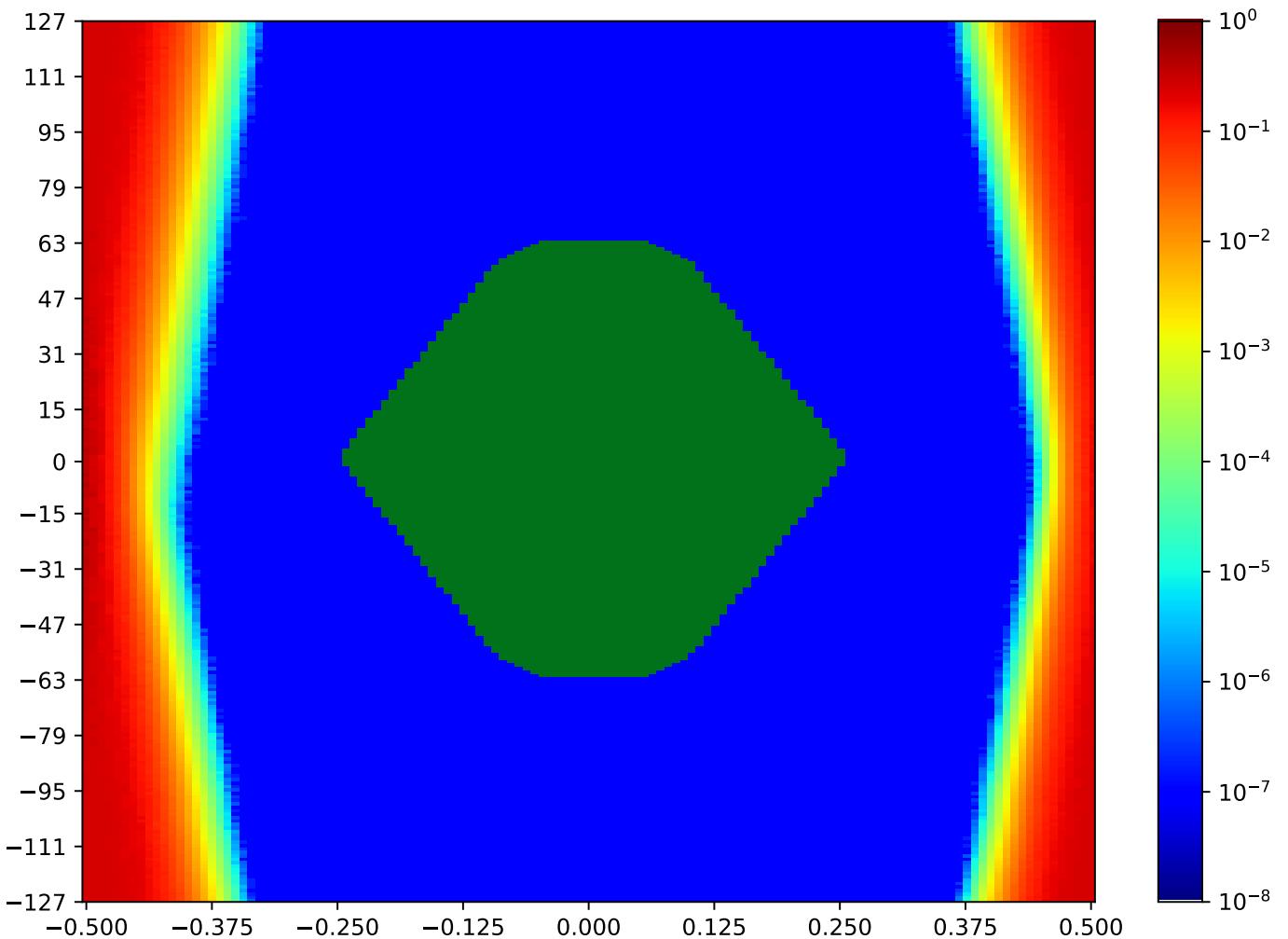


Figure 2.31: MSP_C_FPGA-TX3-03-RX7-03-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.5 MSP_C_FPGA-TX3-04-RX7-04-MSP_A_FPGA

Table 2.29: MSP_C_FPGA-TX3-04-RX7-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:36:56		2018-Jan-24 03:38:07	
Reset RX	OA	HO		HO (%)	
true	24517	105		81.40%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

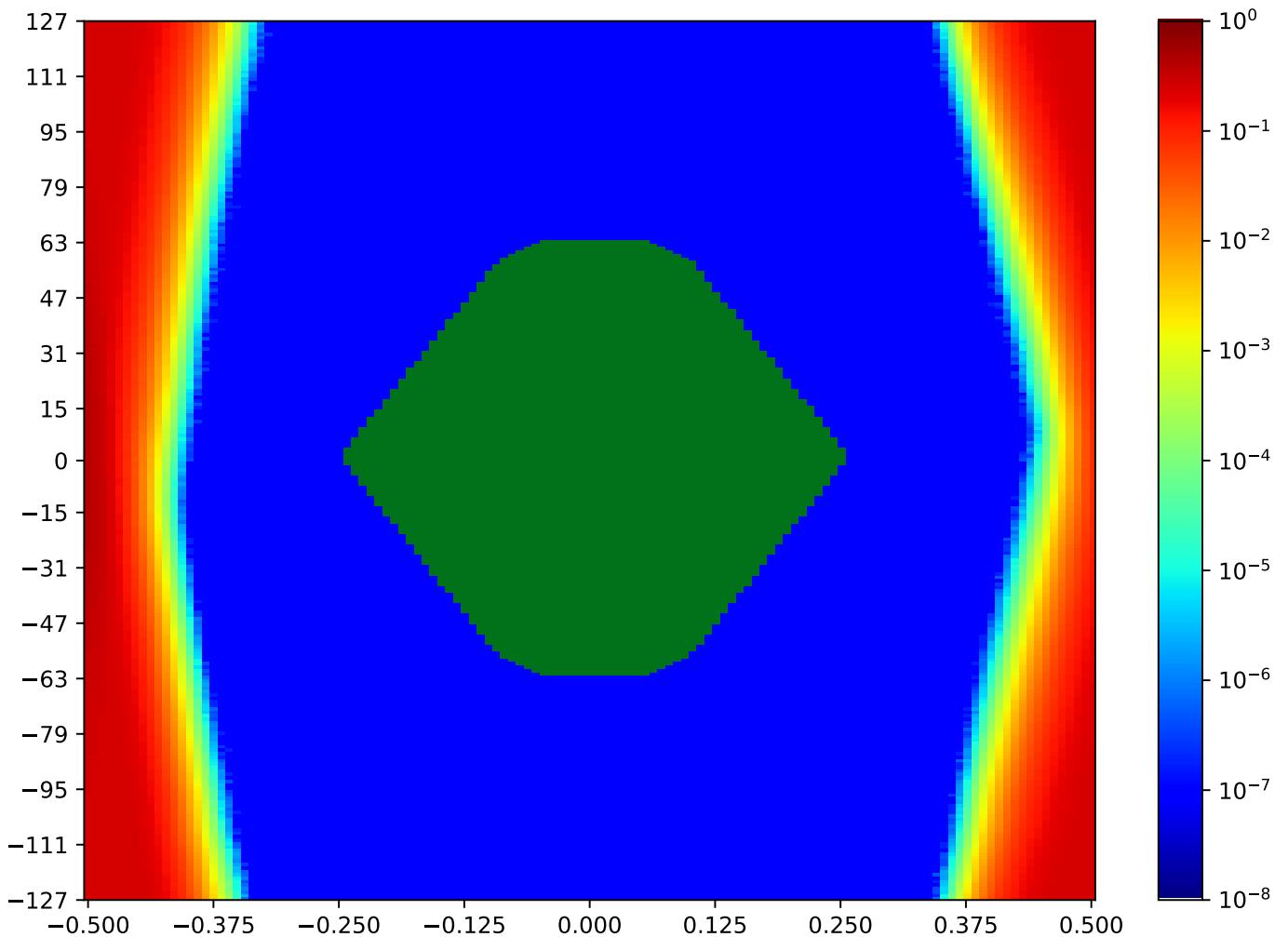


Figure 2.32: MSP_C_FPGA-TX3-04-RX7-04-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.6 MSP_C_FPGA-TX3-05-RX7-05-MSP_A_FPGA

Table 2.30: MSP_C_FPGA-TX3-05-RX7-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:26:23		2018-Jan-24 03:27:34	
Reset RX	OA	HO		HO (%)	
true	24534	105		81.40%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

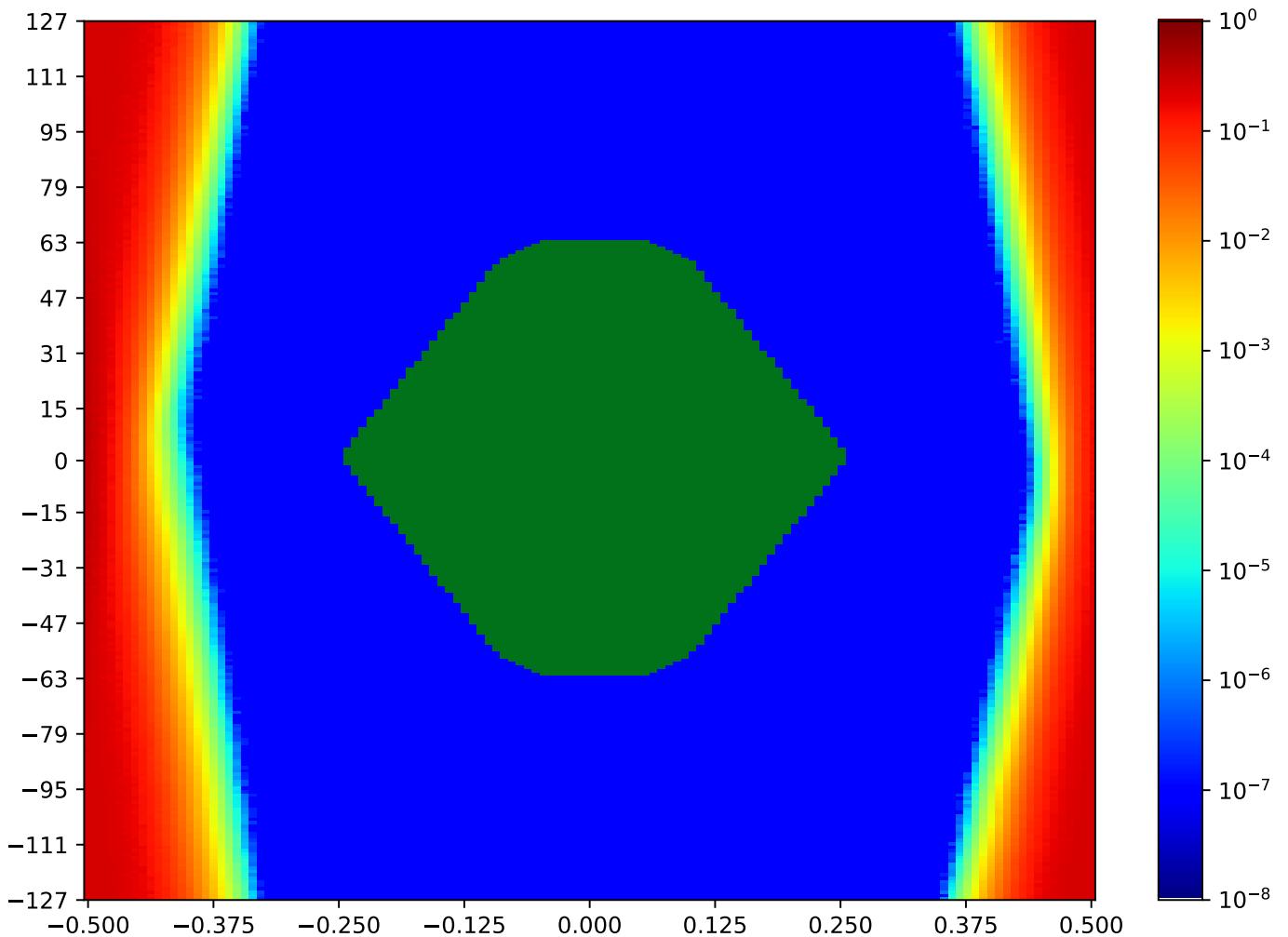


Figure 2.33: MSP_C_FPGA-TX3-05-RX7-05-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.7 MSP_C_FPGA-TX3-06-RX7-06-MSP_A_FPGA

Table 2.31: MSP_C_FPGA-TX3-06-RX7-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:39:19		2018-Jan-24 03:40:29	
Reset RX	OA	HO		HO (%)	
true	24508	107		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

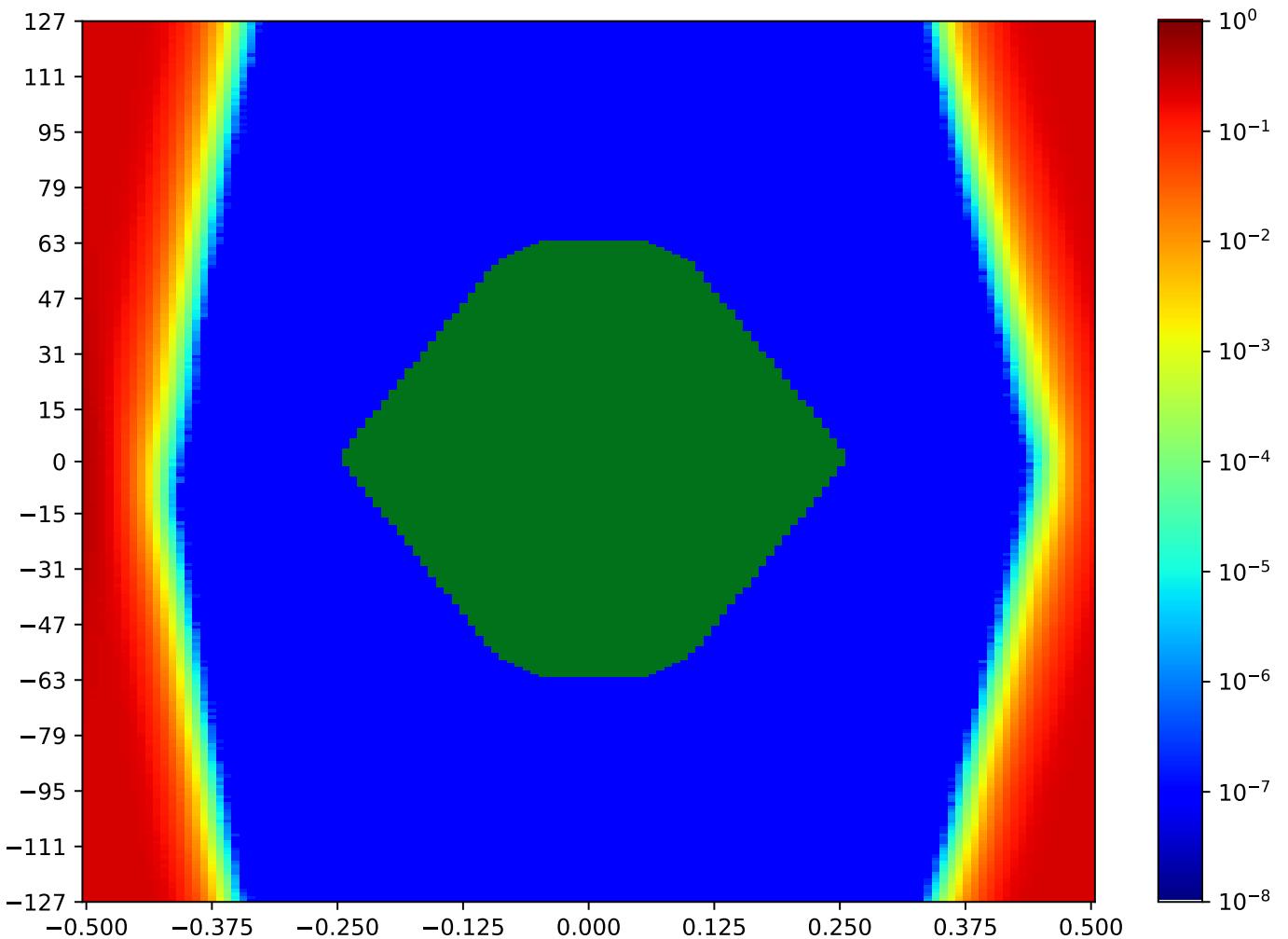


Figure 2.34: MSP_C_FPGA-TX3-06-RX7-06-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.8 MSP_C_FPGA-TX3-07-RX7-07-MSP_A_FPGA

Table 2.32: MSP_C_FPGA-TX3-07-RX7-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:28:45		2018-Jan-24 03:29:54	
Reset RX	OA	HO		HO (%)	
true	24044	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

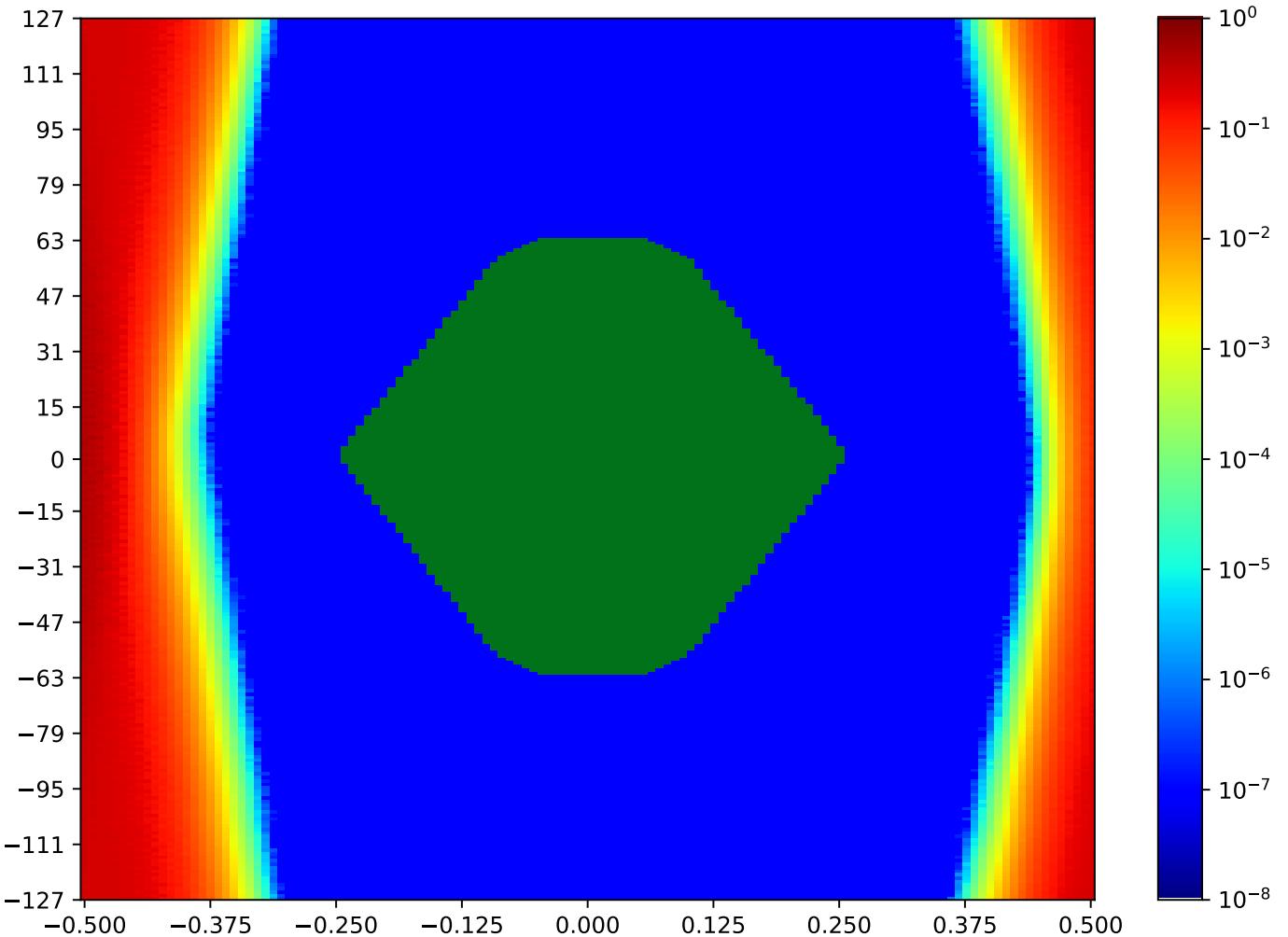


Figure 2.35: MSP_C_FPGA-TX3-07-RX7-07-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.9 MSP_C_FPGA-TX3-08-RX7-08-MSP_A_FPGA

Table 2.33: MSP_C_FPGA-TX3-08-RX7-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:38:07		2018-Jan-24 03:39:19	
Reset RX	OA	HO		HO (%)	
true	24952	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

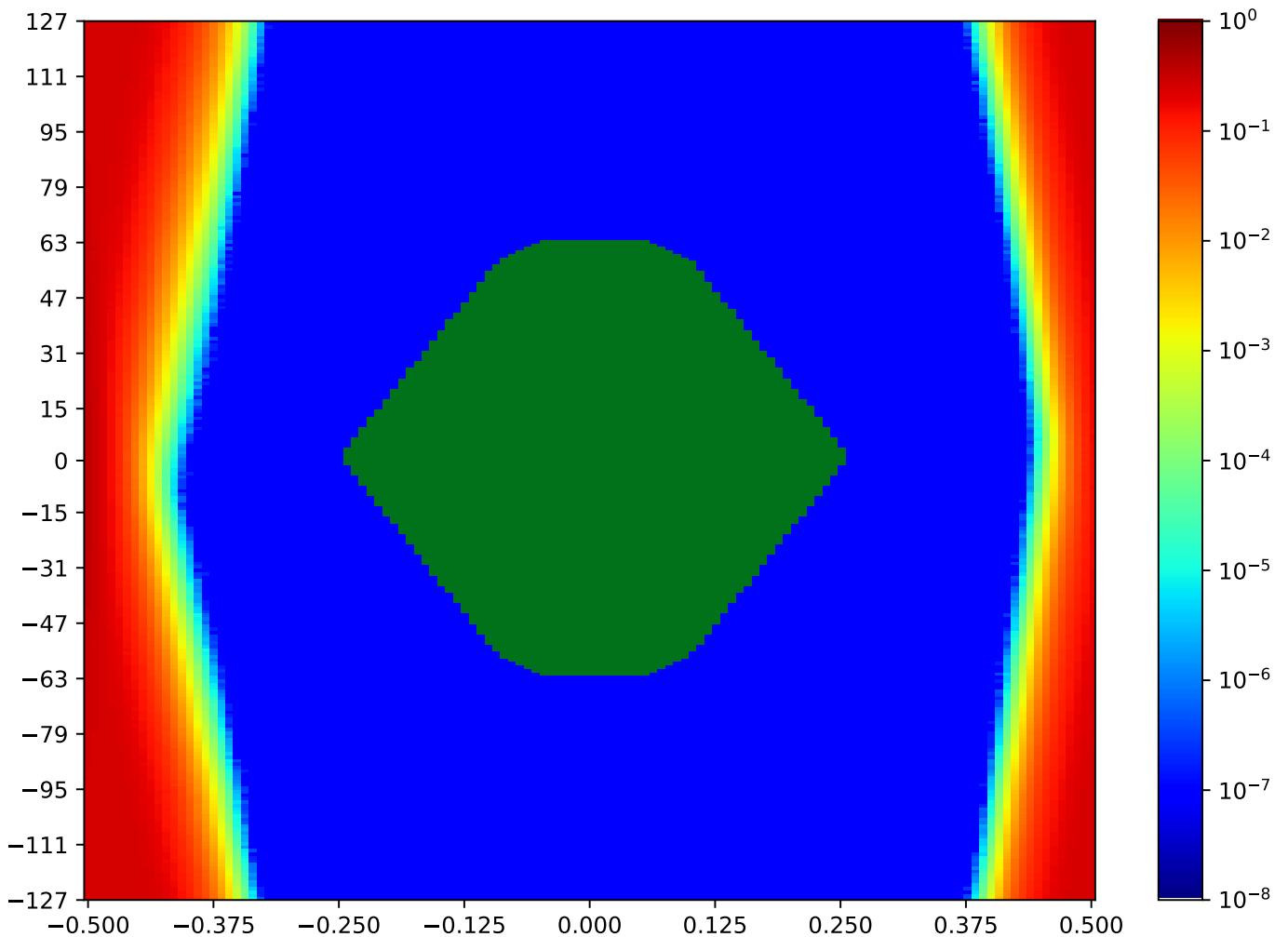


Figure 2.36: MSP_C_FPGA-TX3-08-RX7-08-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.10 MSP_C_FPGA-TX3-09-RX7-09-MSP_A_FPGA

Table 2.34: MSP_C_FPGA-TX3-09-RX7-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:31:04		2018-Jan-24 03:32:15	
Reset RX	OA	HO		HO (%)	
true	25299	108		83.72%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

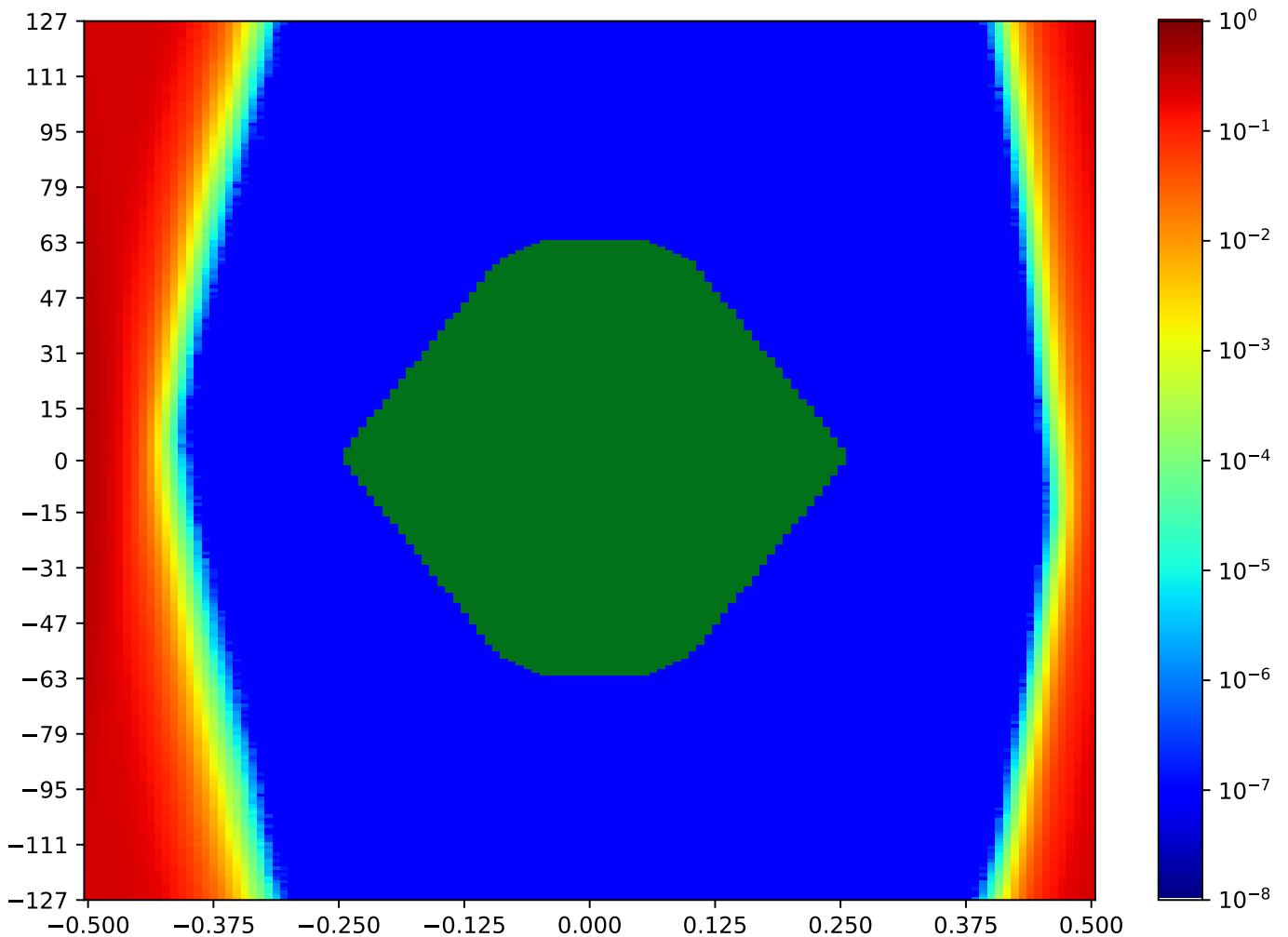


Figure 2.37: MSP_C_FPGA-TX3-09-RX7-09-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.11 MSP_C_FPGA-TX3-10-RX7-10-MSP_A_FPGA

Table 2.35: MSP_C_FPGA-TX3-10-RX7-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:35:45		2018-Jan-24 03:36:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25247	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

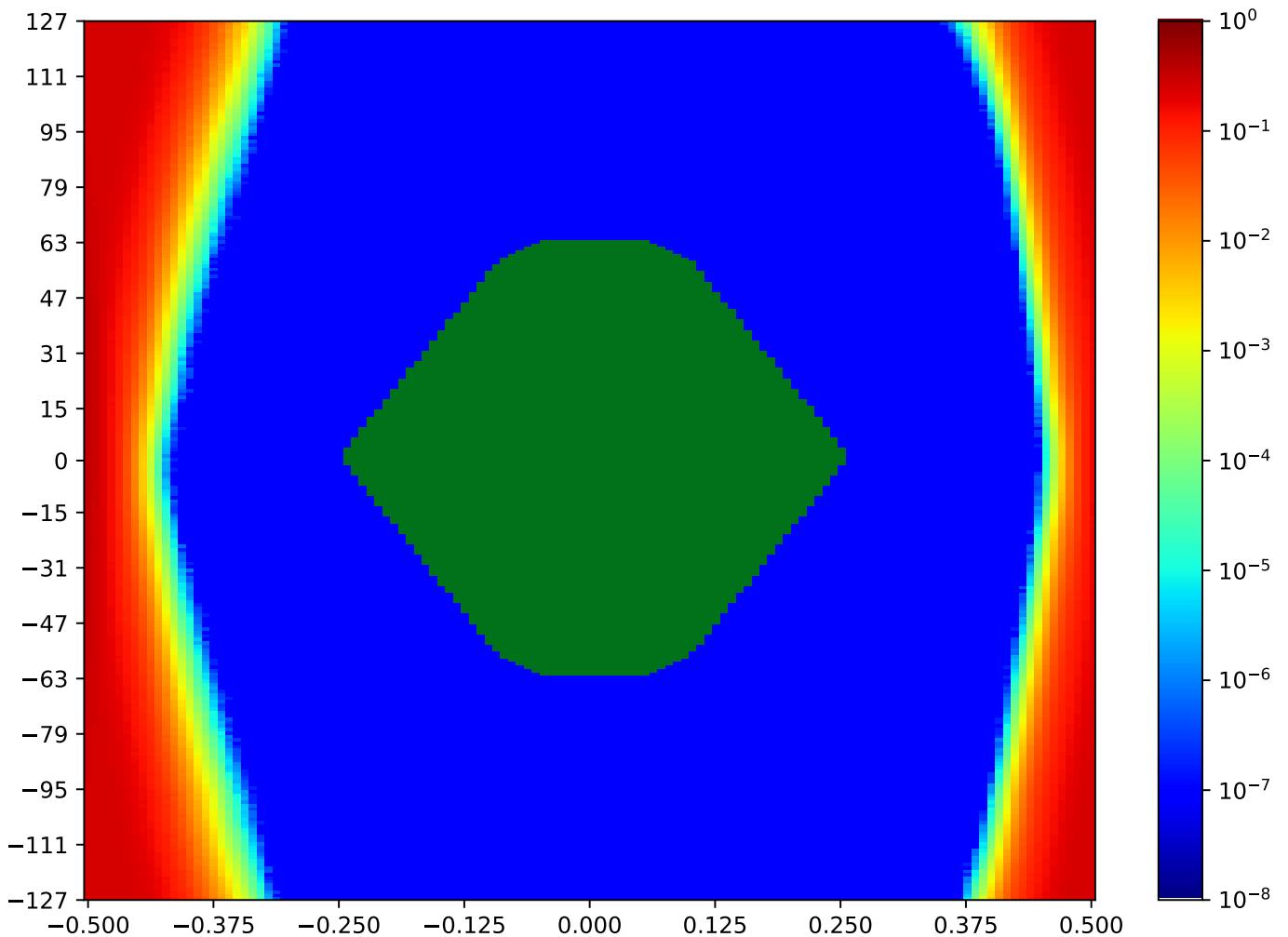


Figure 2.38: MSP_C_FPGA-TX3-10-RX7-10-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.3.12 MSP_C_FPGA-TX3-11-RX7-11-MSP_A_FPGA

Table 2.36: MSP_C_FPGA-TX3-11-RX7-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:34:35		2018-Jan-24 03:35:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23369	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

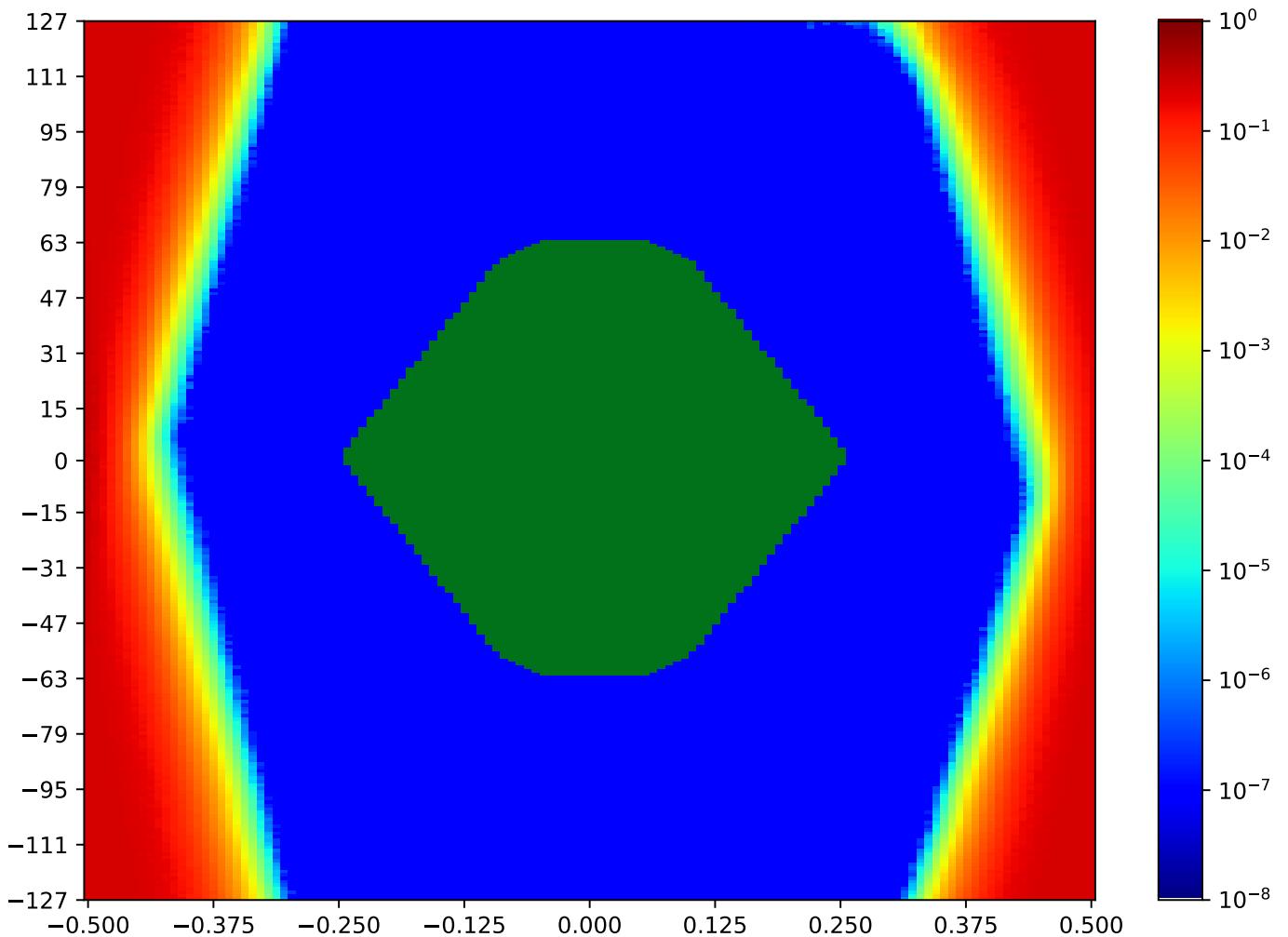


Figure 2.39: MSP_C_FPGA-TX3-11-RX7-11-MSP_A_FPGA

Call back to summary Figure 2.27. Sibling eye diagrams: V1-12.8.

2.4 MSP_C TX4 MSP_A RX6 Minipod Loopback

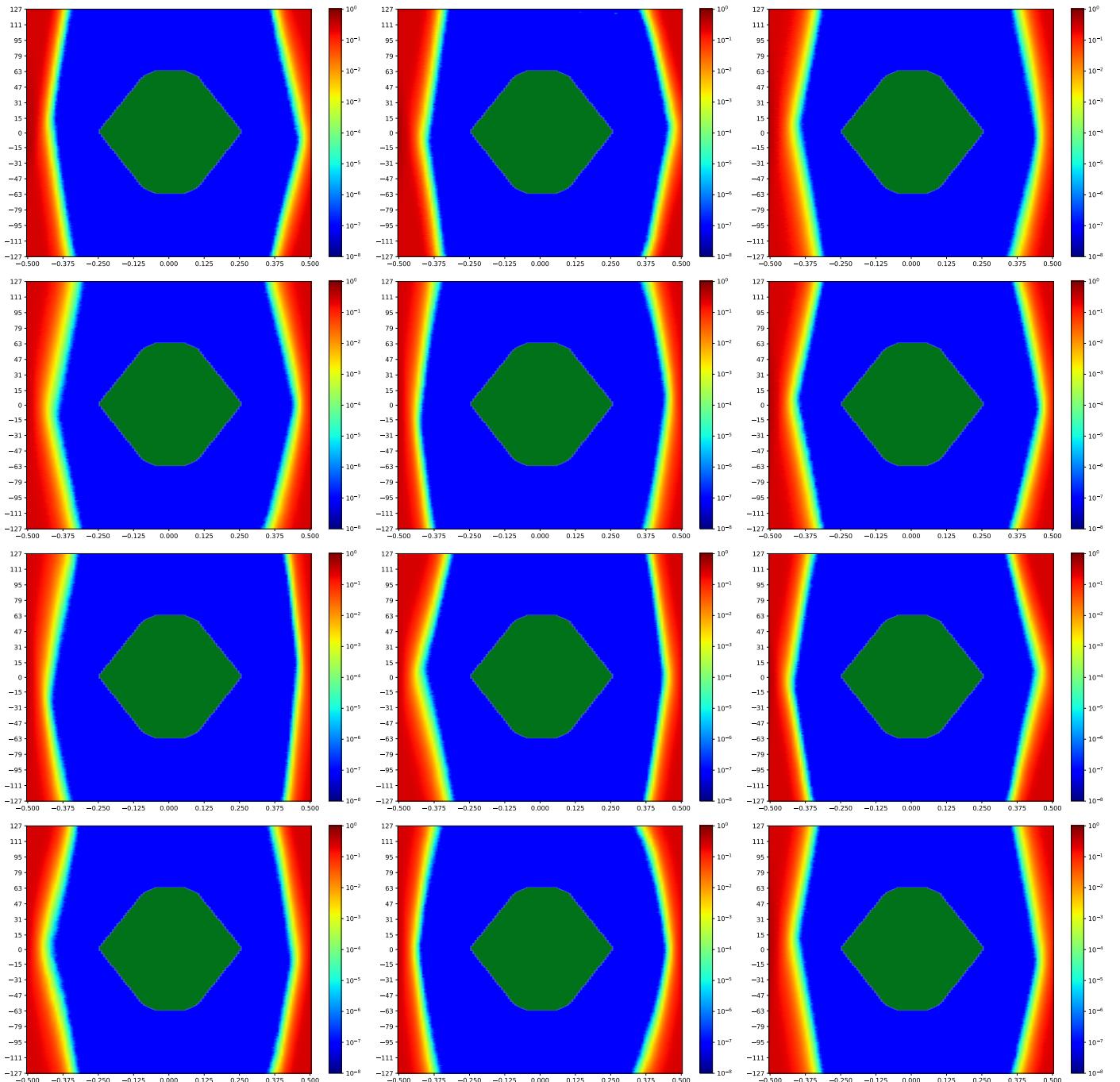


Figure 2.40: MSP_C TX4 MSP_A RX6 Minipod Loopback

A cross-reference to Figure 2.40. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.53.

2.4.1 MSP_C_FPGA-TX4-00-RX6-00-MSP_A_FPGA

Table 2.37: MSP_C_FPGA-TX4-00-RX6-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:44:00		2018-Jan-24 03:45:11	
Reset RX	OA	HO		HO (%)	
true	24953	107		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

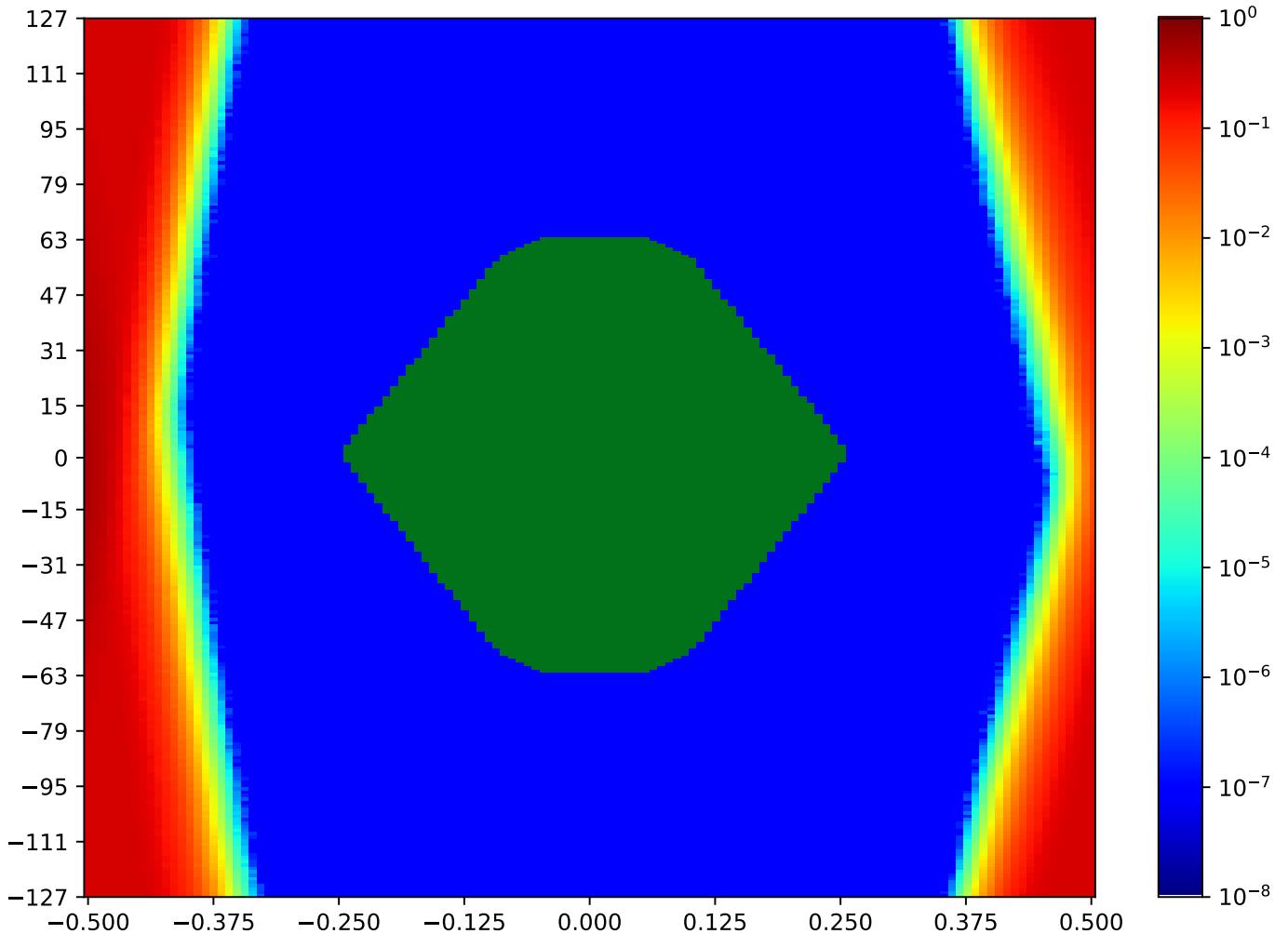


Figure 2.41: MSP_C_FPGA-TX4-00-RX6-00-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.2 MSP_C_FPGA-TX4-01-RX6-01-MSP_A_FPGA

Table 2.38: MSP_C_FPGA-TX4-01-RX6-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:41:39		2018-Jan-24 03:42:49	
Reset RX	OA	HO		HO (%)	
true	24589	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

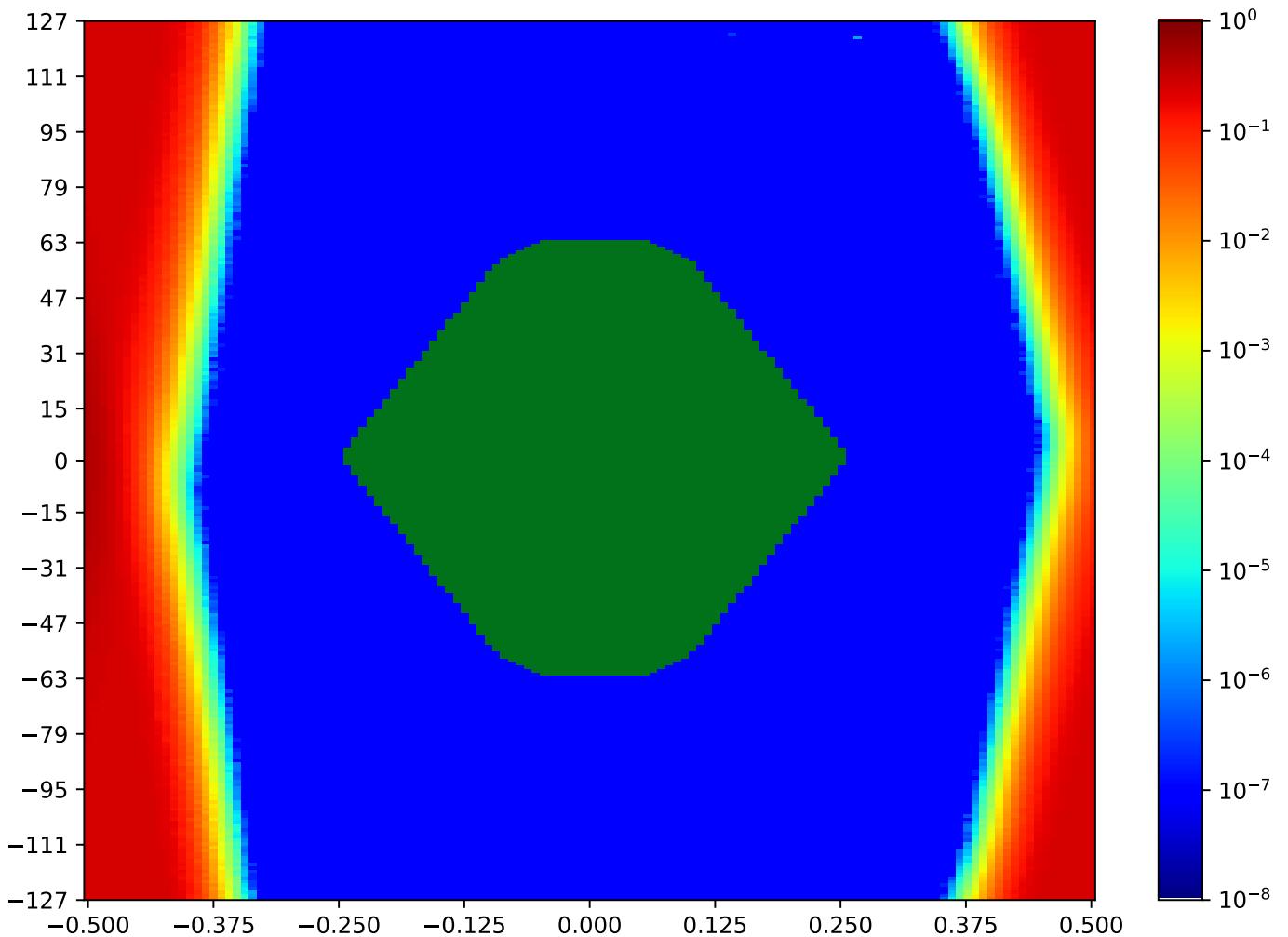


Figure 2.42: MSP_C_FPGA-TX4-01-RX6-01-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.3 MSP_C_FPGA-TX4-02-RX6-02-MSP_A_FPGA

Table 2.39: MSP_C_FPGA-TX4-02-RX6-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:47:33		2018-Jan-24 03:48:43	
Reset RX	OA	HO		HO (%)	
true	23831	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

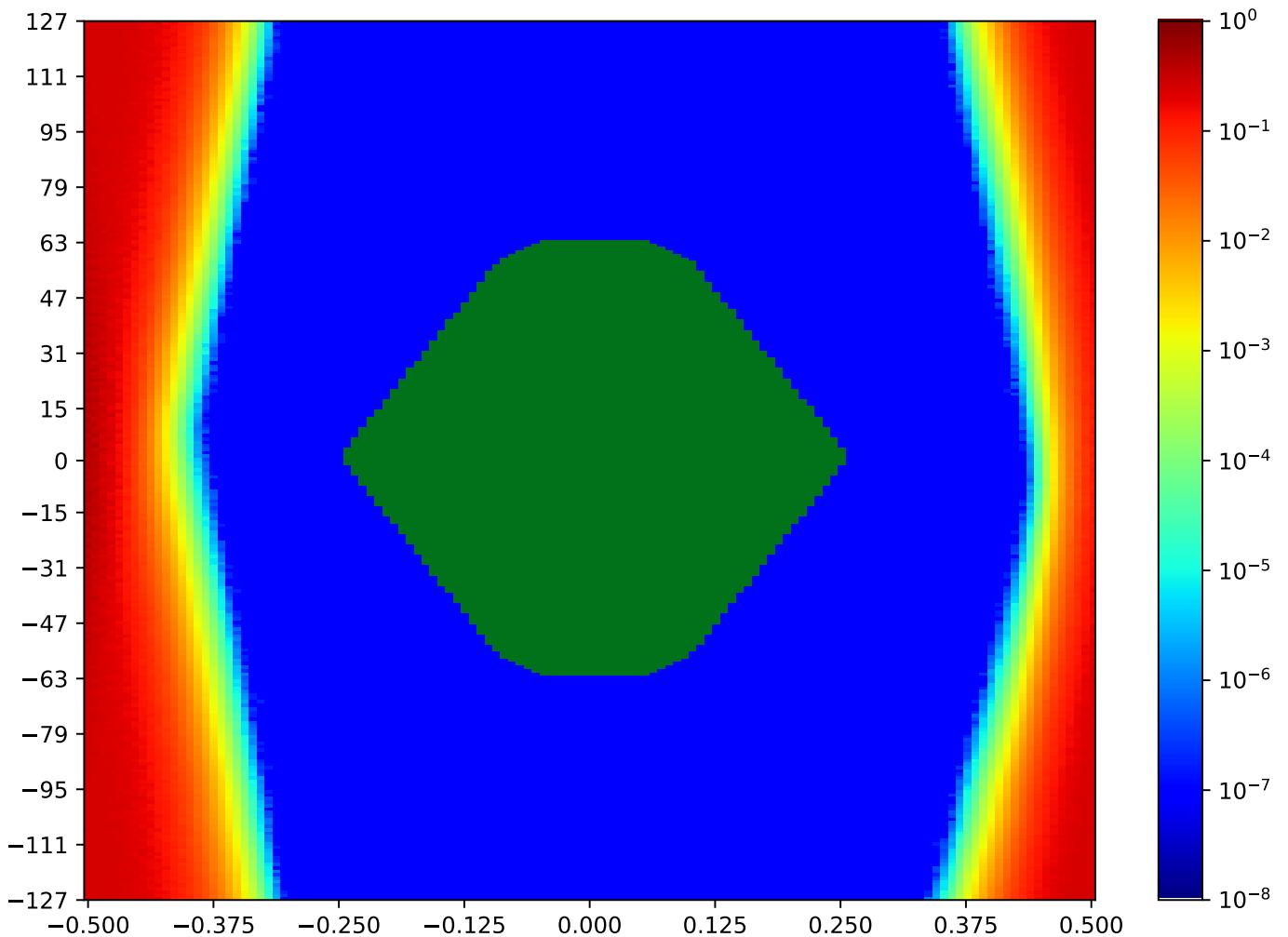


Figure 2.43: MSP_C_FPGA-TX4-02-RX6-02-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.4 MSP_C_FPGA-TX4-03-RX6-03-MSP_A_FPGA

Table 2.40: MSP_C_FPGA-TX4-03-RX6-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:40:29		2018-Jan-24 03:41:39	
Reset RX	OA	HO		HO (%)	
true	23501	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

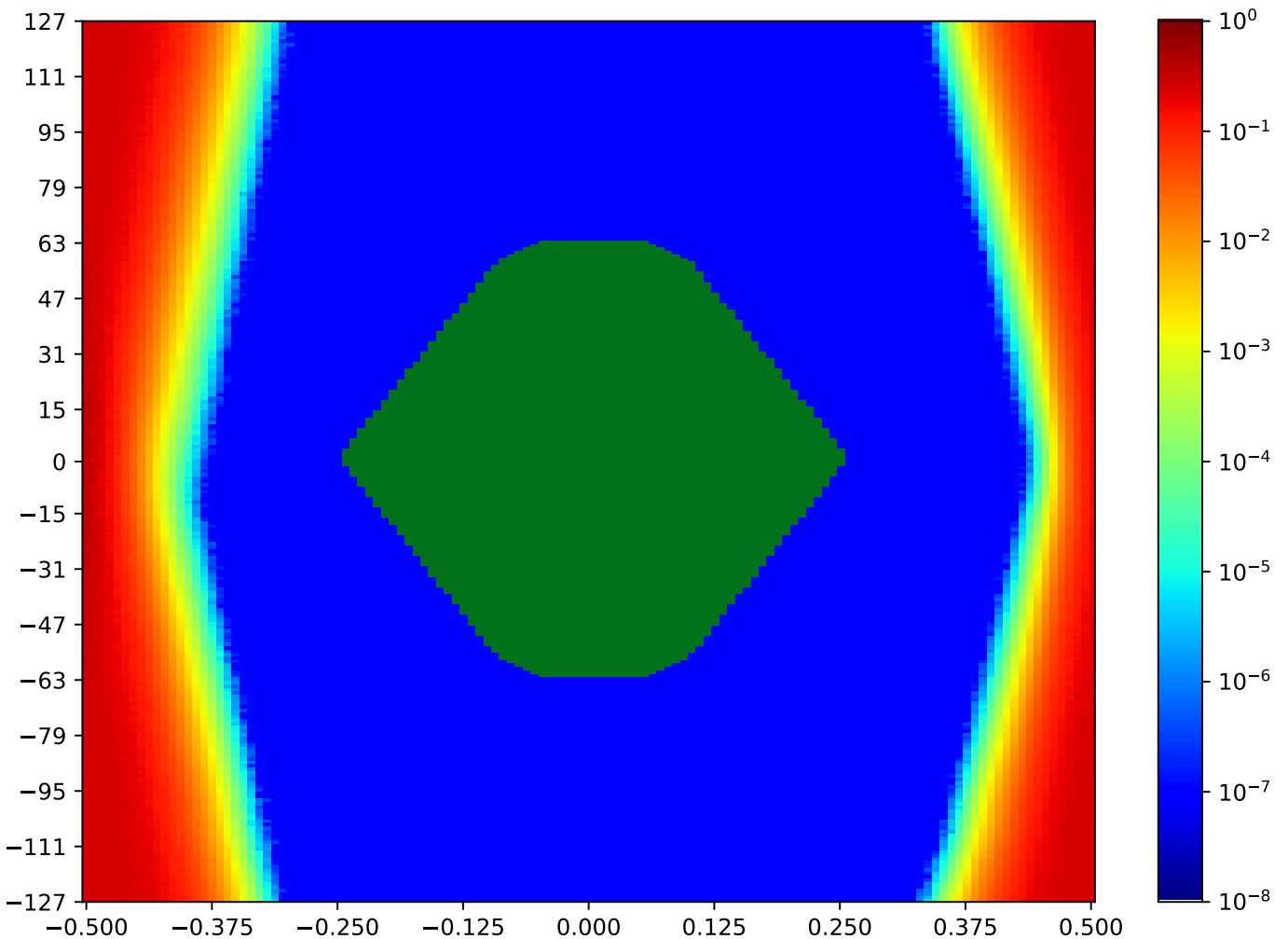


Figure 2.44: MSP_C_FPGA-TX4-03-RX6-03-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.5 MSP_C_FPGA-TX4-04-RX6-04-MSP_A_FPGA

Table 2.41: MSP_C_FPGA-TX4-04-RX6-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:51:04		2018-Jan-24 03:52:15	
Reset RX	OA	HO		HO (%)	
true	25545	107		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

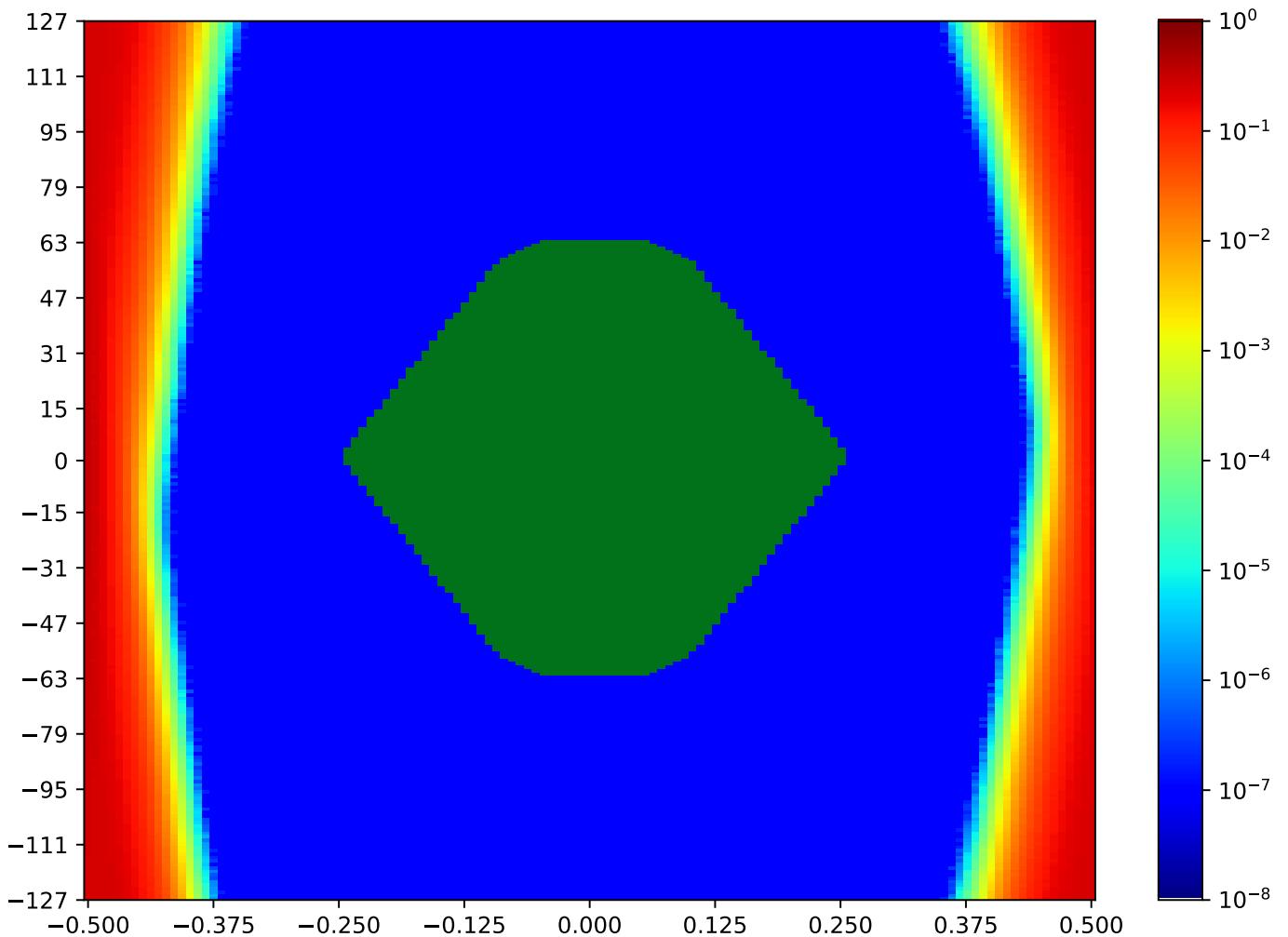


Figure 2.45: MSP_C_FPGA-TX4-04-RX6-04-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.6 MSP_C_FPGA-TX4-05-RX6-05-MSP_A_FPGA

Table 2.42: MSP_C_FPGA-TX4-05-RX6-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:42:49		2018-Jan-24 03:44:00	
Reset RX	OA	HO		HO (%)	
true	24175	105		81.40%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

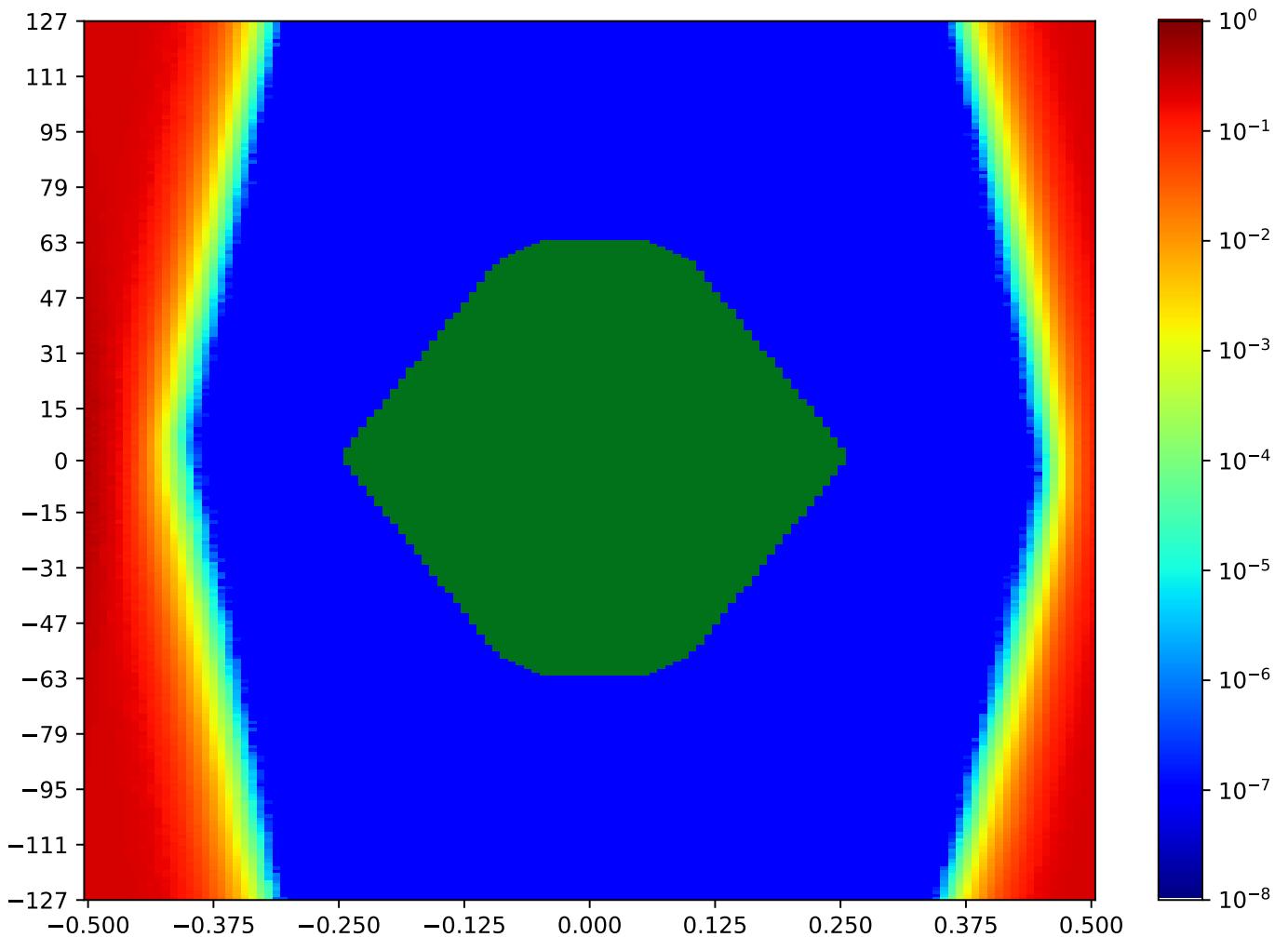


Figure 2.46: MSP_C_FPGA-TX4-05-RX6-05-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.7 MSP_C_FPGA-TX4-06-RX6-06-MSP_A_FPGA

Table 2.43: MSP_C_FPGA-TX4-06-RX6-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:53:26		2018-Jan-24 03:54:38	
Reset RX	OA	HO		HO (%)	
true	25715	107		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

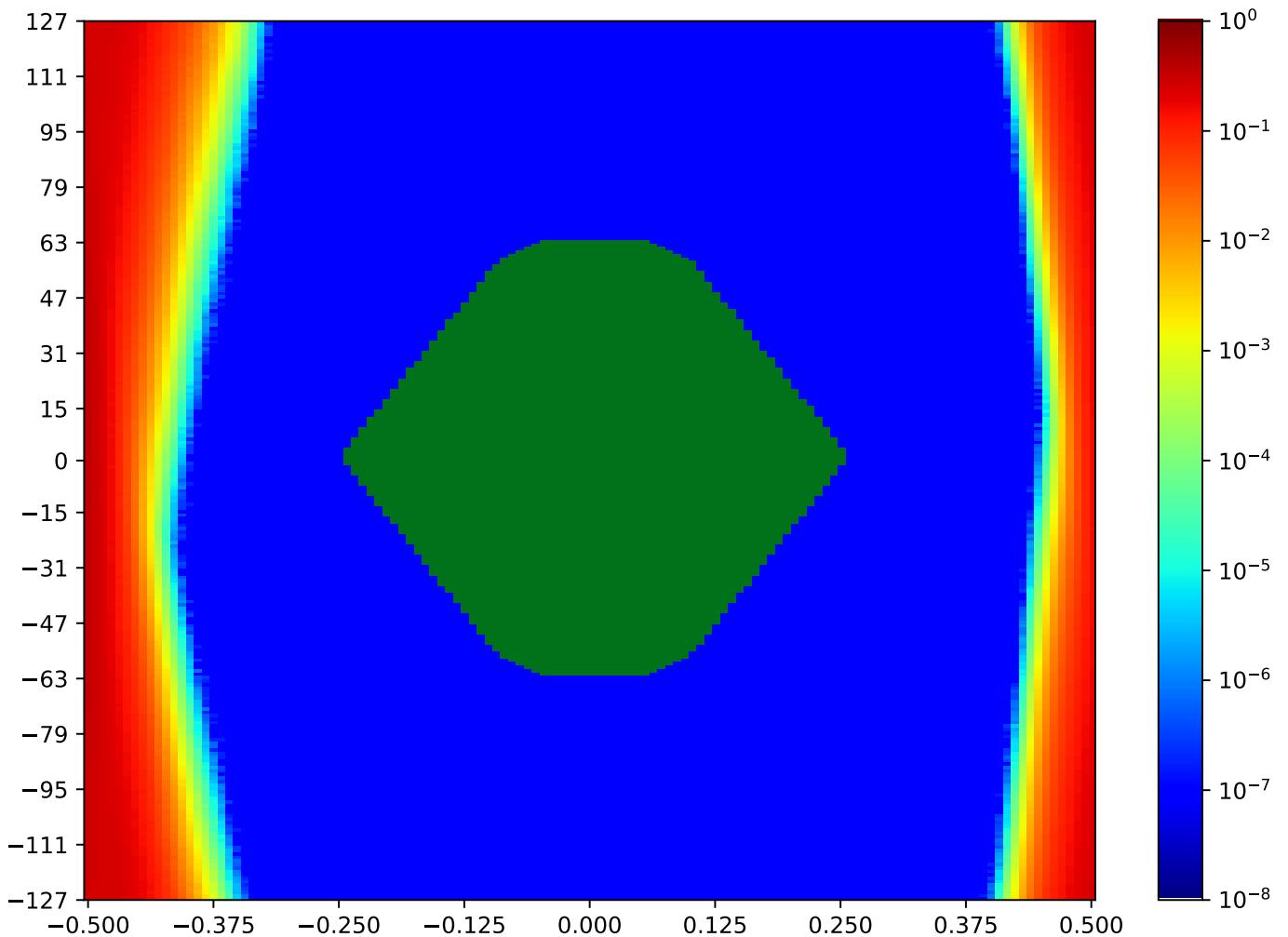


Figure 2.47: MSP_C_FPGA-TX4-06-RX6-06-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.8 MSP_C_FPGA-TX4-07-RX6-07-MSP_A_FPGA

Table 2.44: MSP_C_FPGA-TX4-07-RX6-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:45:11		2018-Jan-24 03:46:22	
Reset RX	OA	HO		HO (%)	
true	24237	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

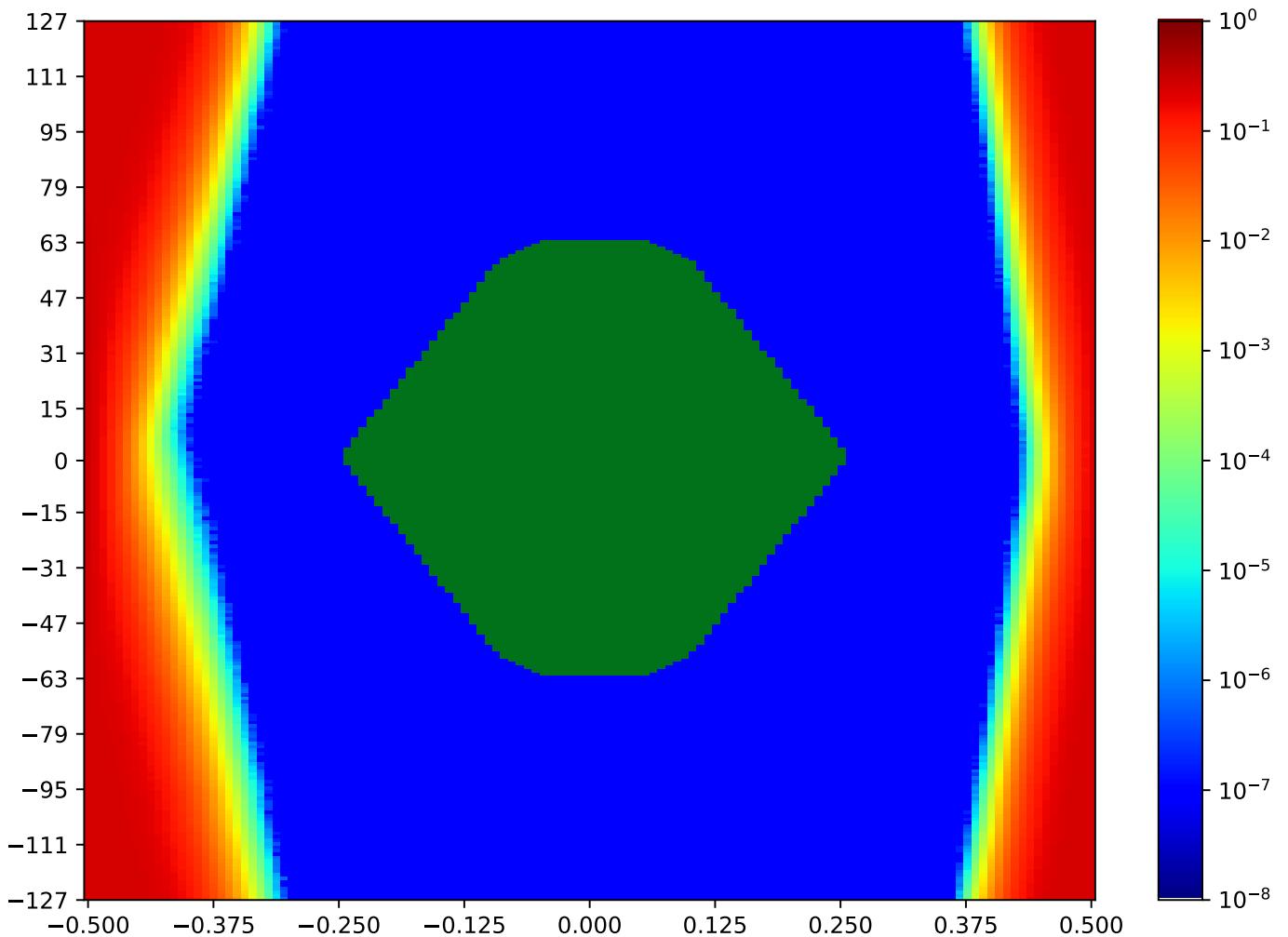


Figure 2.48: MSP_C_FPGA-TX4-07-RX6-07-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.9 MSP_C_FPGA-TX4-08-RX6-08-MSP_A_FPGA

Table 2.45: MSP_C_FPGA-TX4-08-RX6-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:52:15		2018-Jan-24 03:53:25	
Reset RX	OA	HO		HO (%)	
true	24361	105		81.40%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

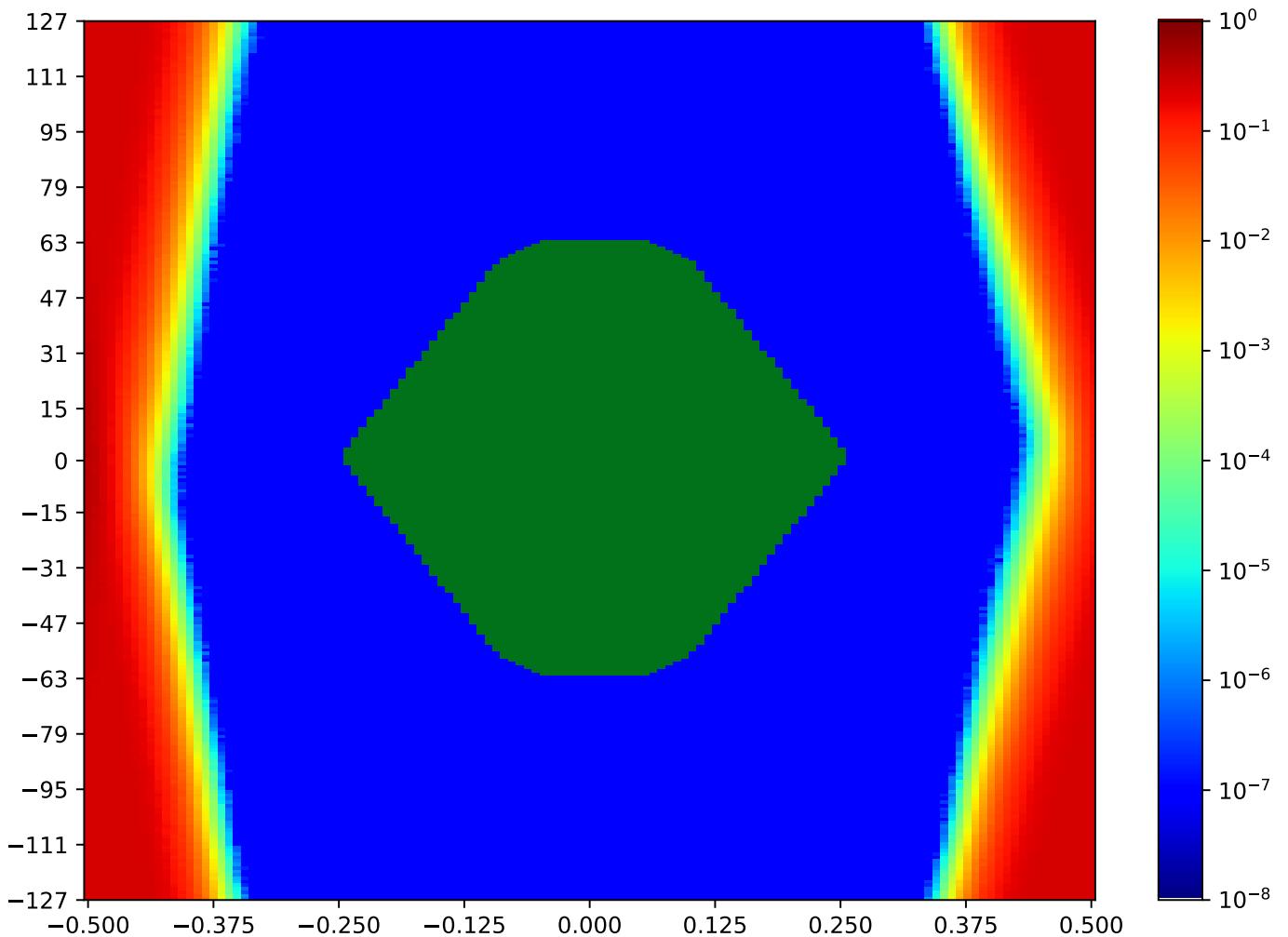


Figure 2.49: MSP_C_FPGA-TX4-08-RX6-08-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.10 MSP_C_FPGA-TX4-09-RX6-09-MSP_A_FPGA

Table 2.46: MSP_C_FPGA-TX4-09-RX6-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:46:22		2018-Jan-24 03:47:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24115	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

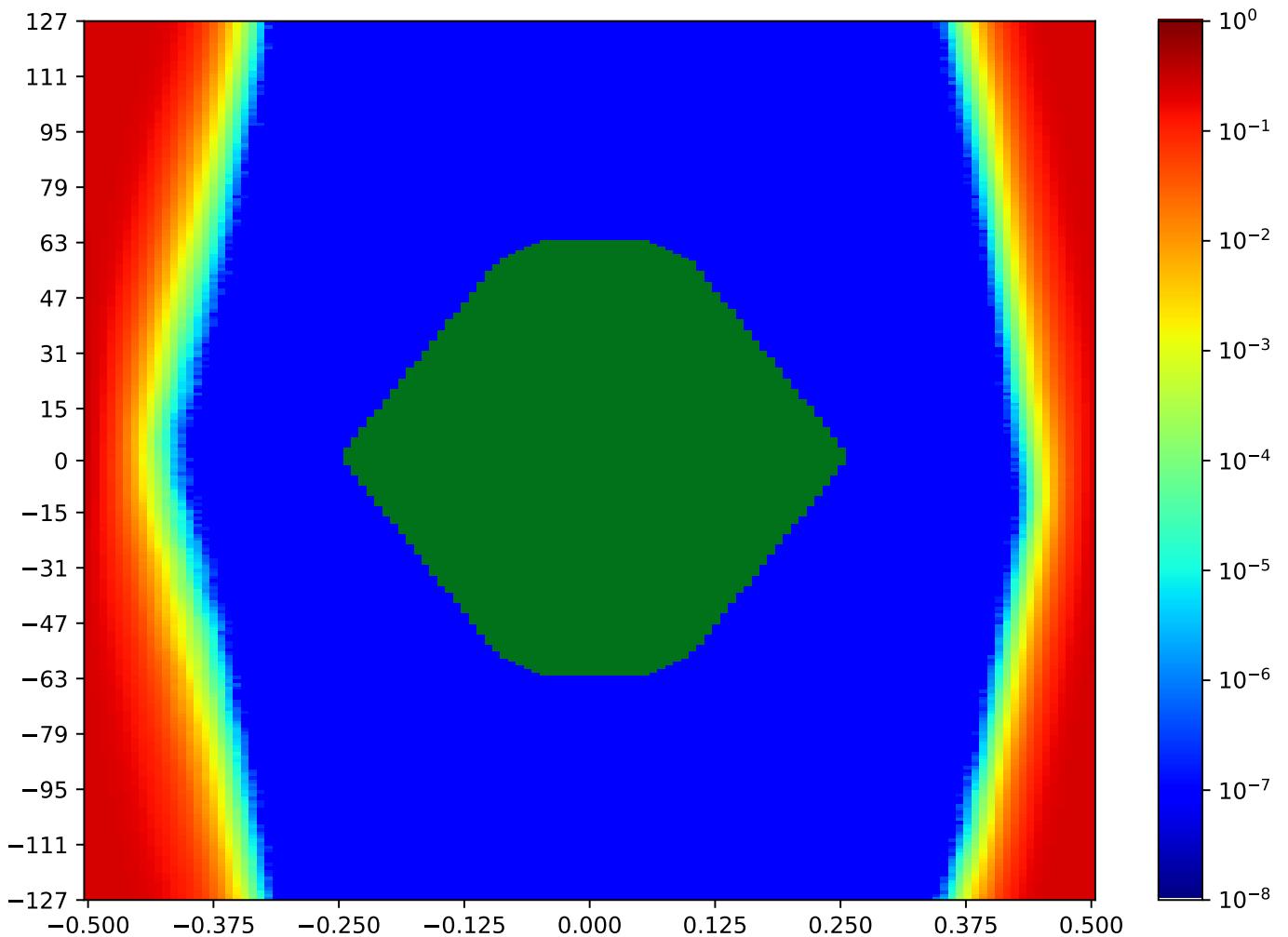


Figure 2.50: MSP_C_FPGA-TX4-09-RX6-09-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.11 MSP_C_FPGA-TX4-10-RX6-10-MSP_A_FPGA

Table 2.47: MSP_C_FPGA-TX4-10-RX6-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:49:53		2018-Jan-24 03:51:04	
Reset RX	OA	HO		HO (%)	
true	25295	110		85.27%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

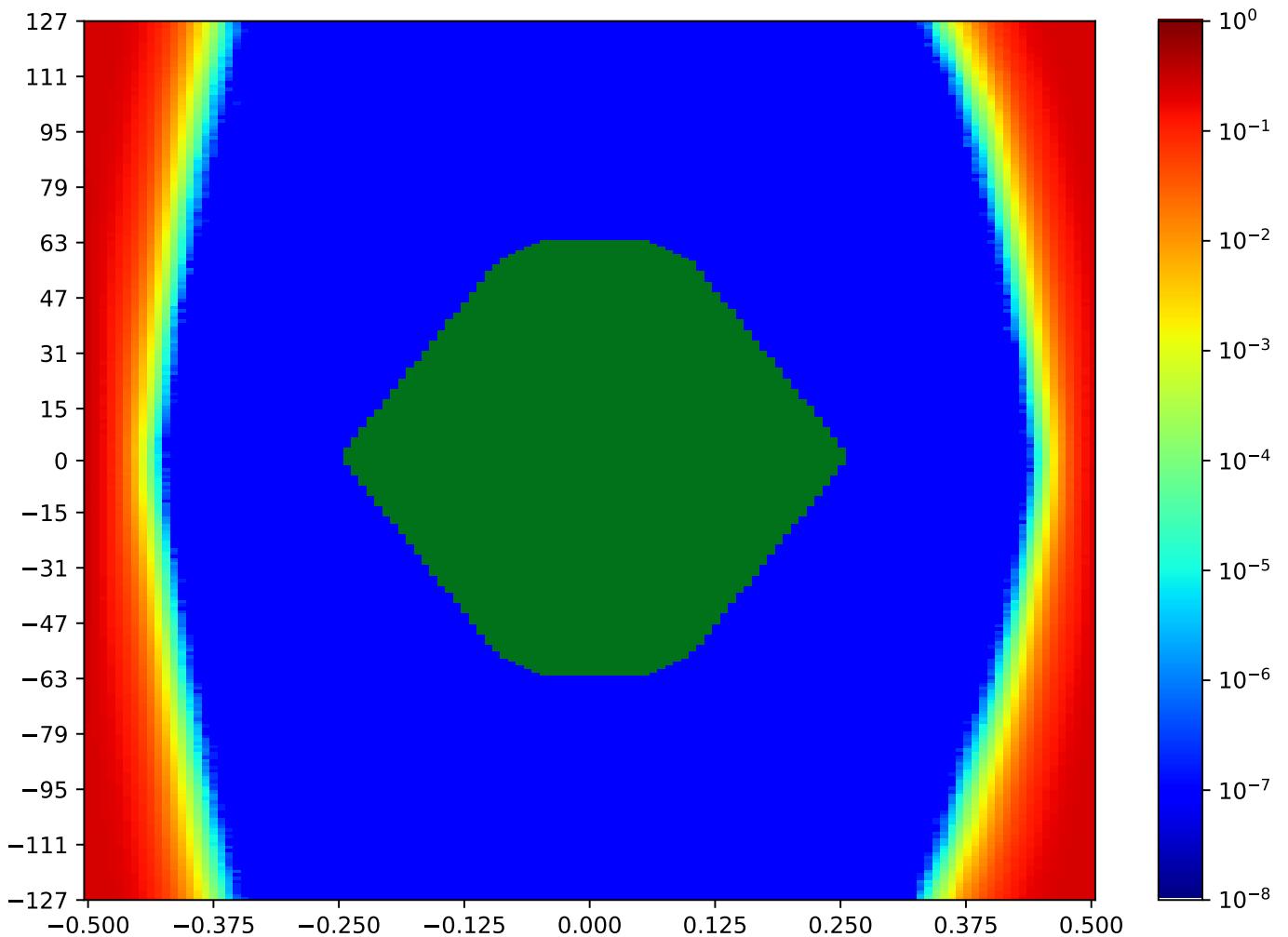


Figure 2.51: MSP_C_FPGA-TX4-10-RX6-10-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.4.12 MSP_C_FPGA-TX4-11-RX6-11-MSP_A_FPGA

Table 2.48: MSP_C_FPGA-TX4-11-RX6-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:48:43		2018-Jan-24 03:49:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24154	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

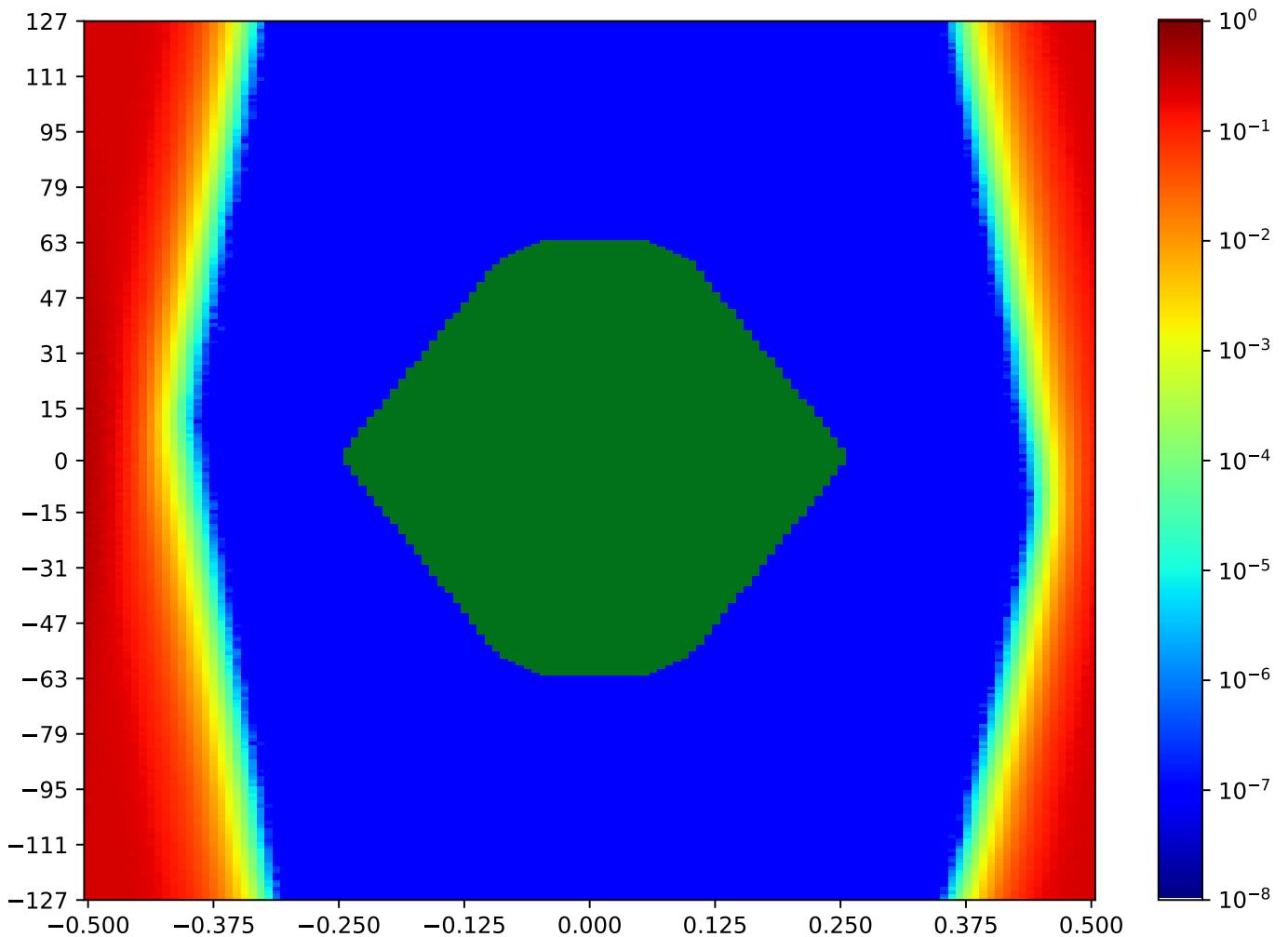


Figure 2.52: MSP_C_FPGA-TX4-11-RX6-11-MSP_A_FPGA

Call back to summary Figure 2.40. Sibling eye diagrams: V1-12.8.

2.5 Partial TRP TX5 MSP_A RX5 Minipod Loopback

A cross-reference to Figure 2.53. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.
Next summary Figure 2.62.

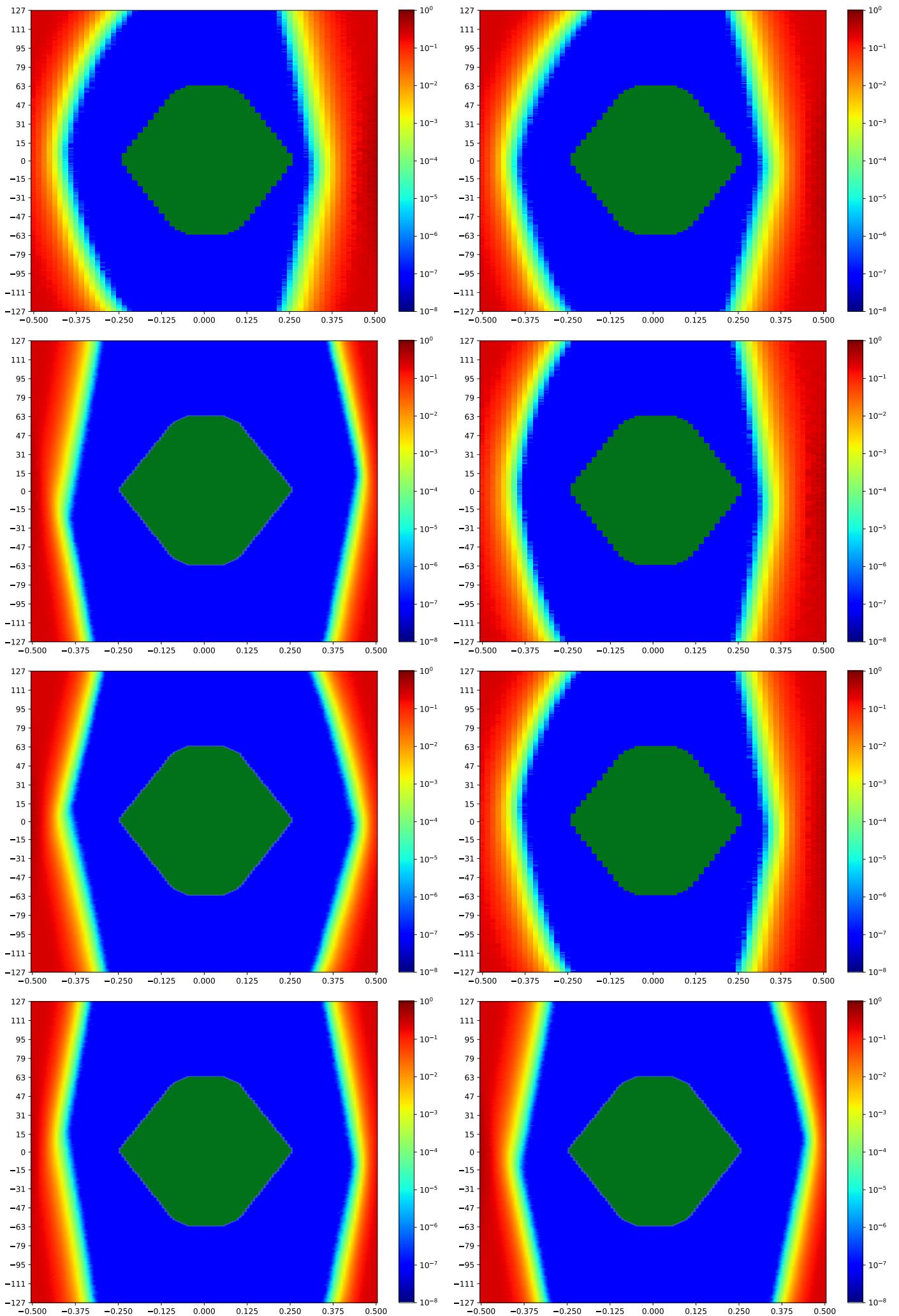


Figure 2.53: Partial TRP TX5 MSP_A RX5 Minipod Loopback

2.5.1 TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

Table 2.49: TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 03:56:27		2018-Jan-24 03:57:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9300	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

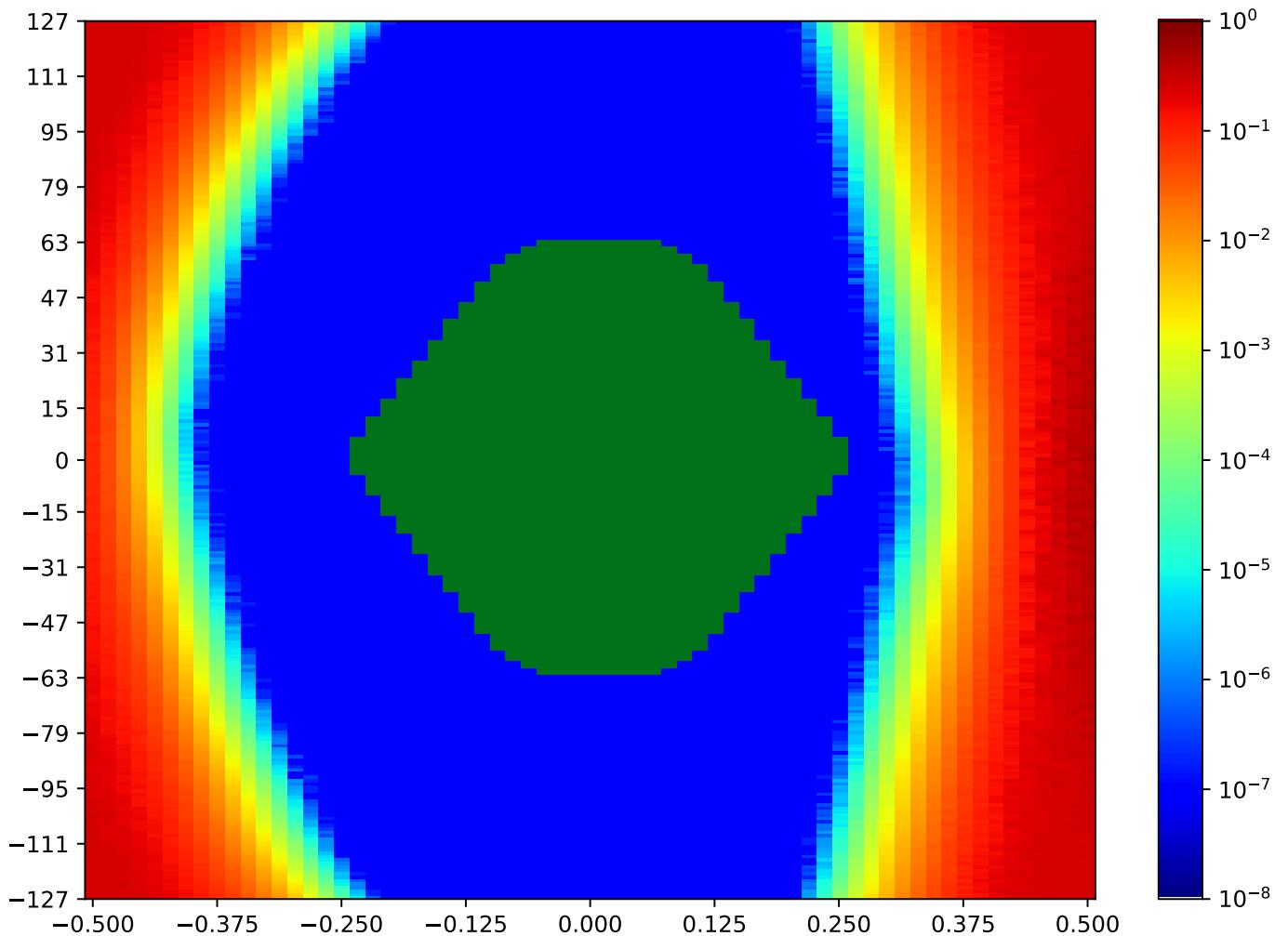


Figure 2.54: TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.5.2 TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

Table 2.50: TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 03:55:14		2018-Jan-24 03:55:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9161	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

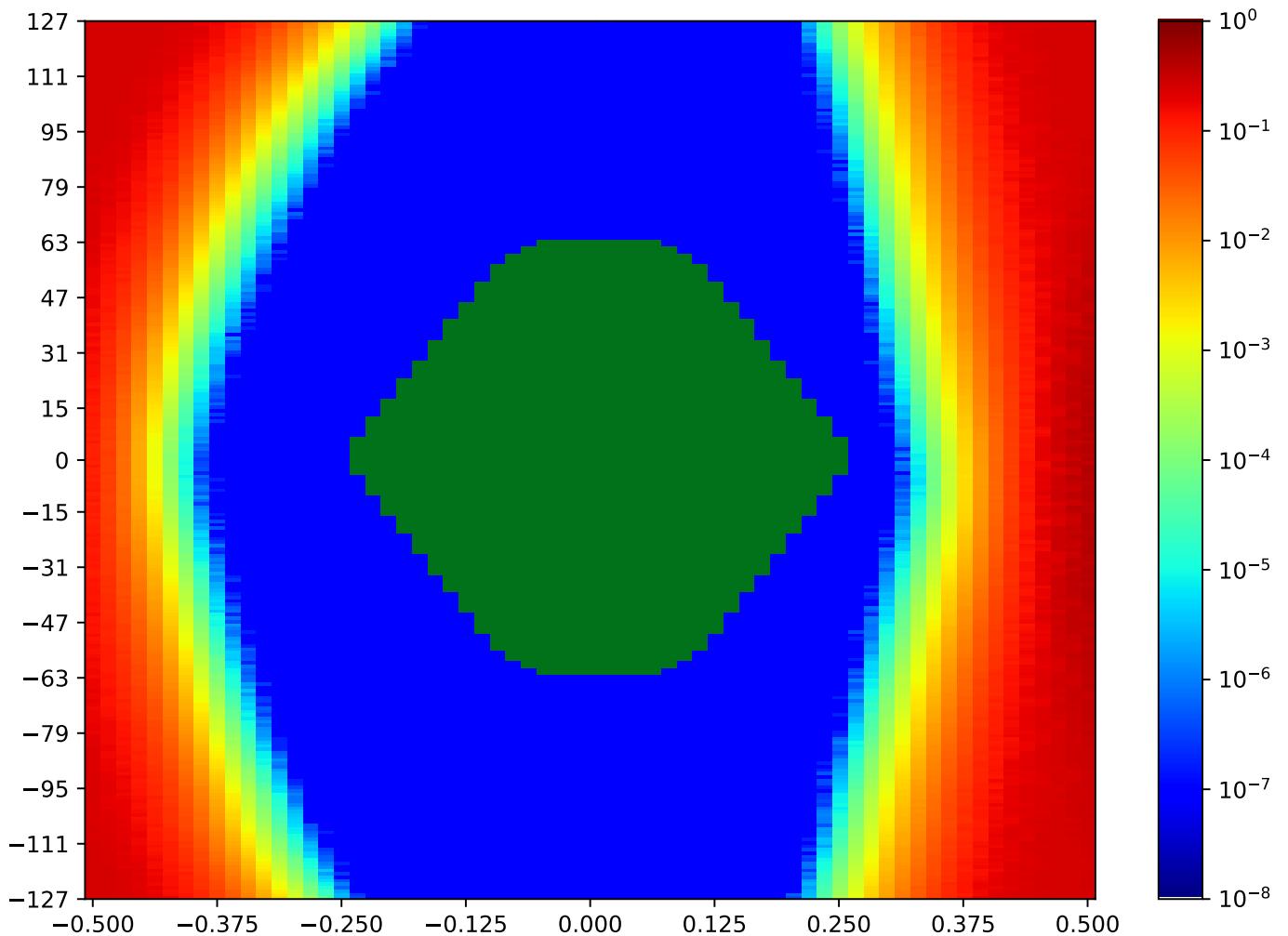


Figure 2.55: TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.5.3 TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

Table 2.51: TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:58:15		2018-Jan-24 03:59:25	
Reset RX	OA	HO		HO (%)	
true	23781	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

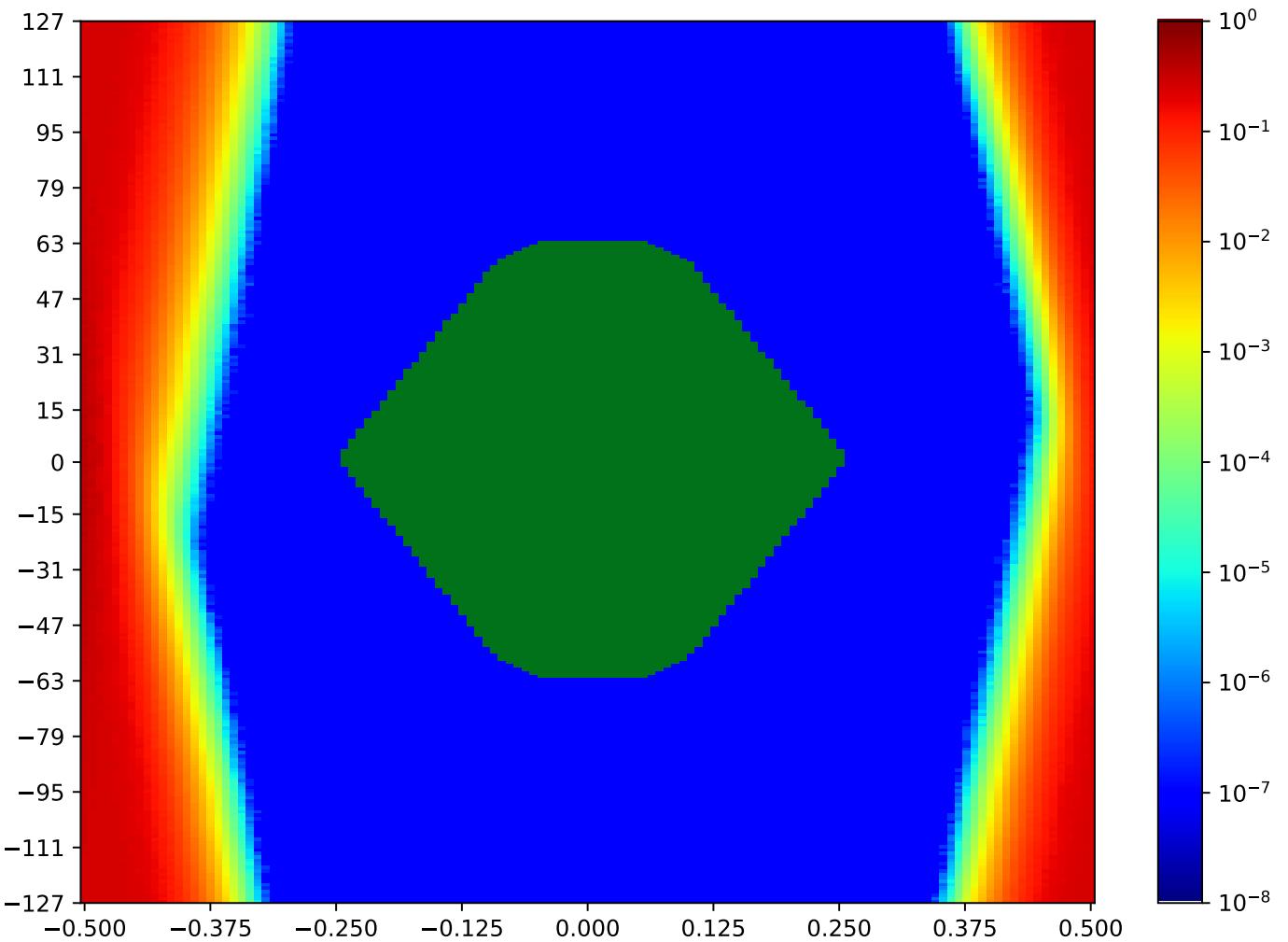


Figure 2.56: TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.5.4 TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

Table 2.52: TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 03:55:50		2018-Jan-24 03:56:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9700	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

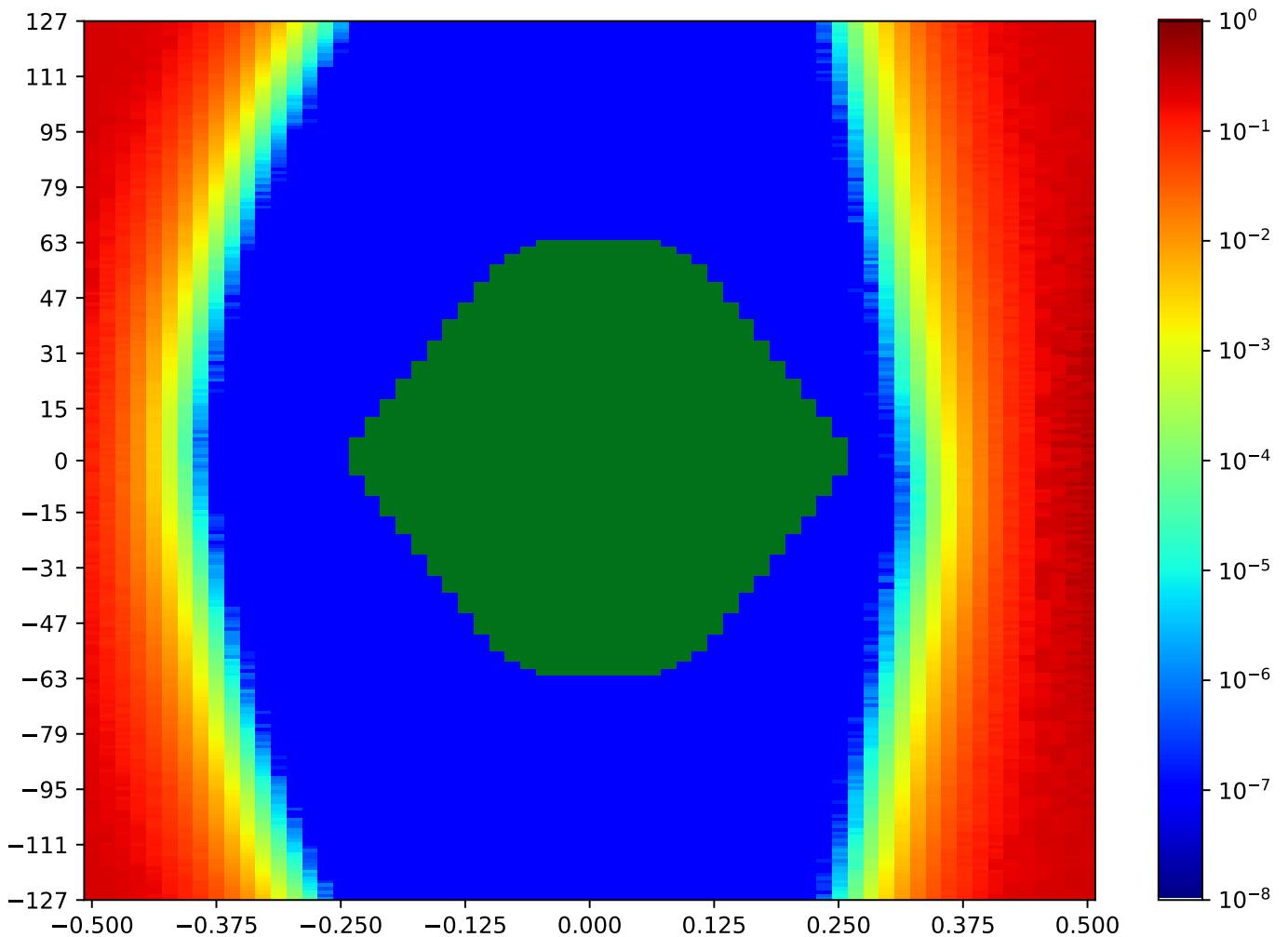


Figure 2.57: TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.5.5 TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

Table 2.53: TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:00:34		2018-Jan-24 04:01:43	
Reset RX	OA	HO		HO (%)	
true	22608	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

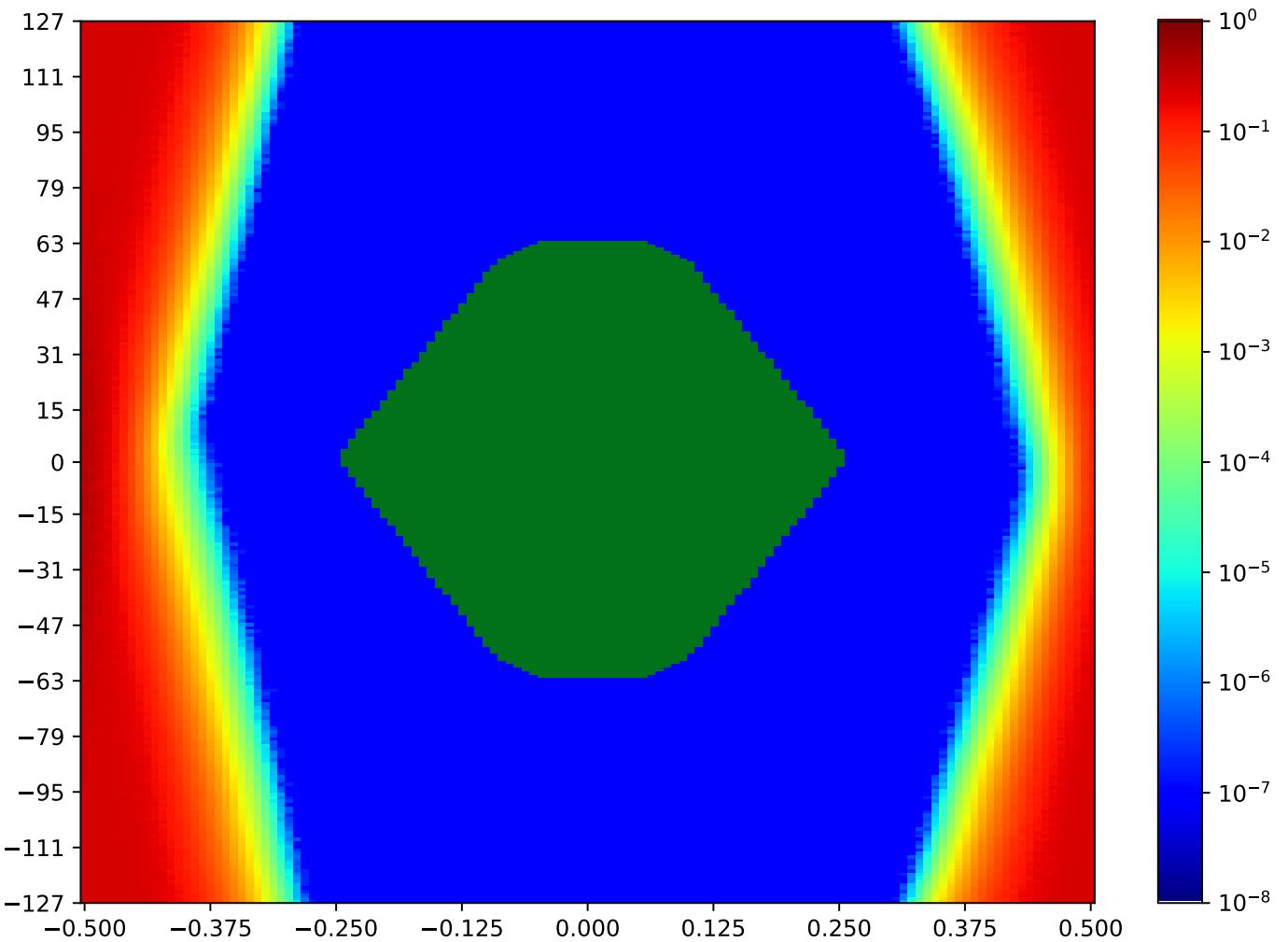


Figure 2.58: TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.5.6 TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

Table 2.54: TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 03:54:38		2018-Jan-24 03:55:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9645	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

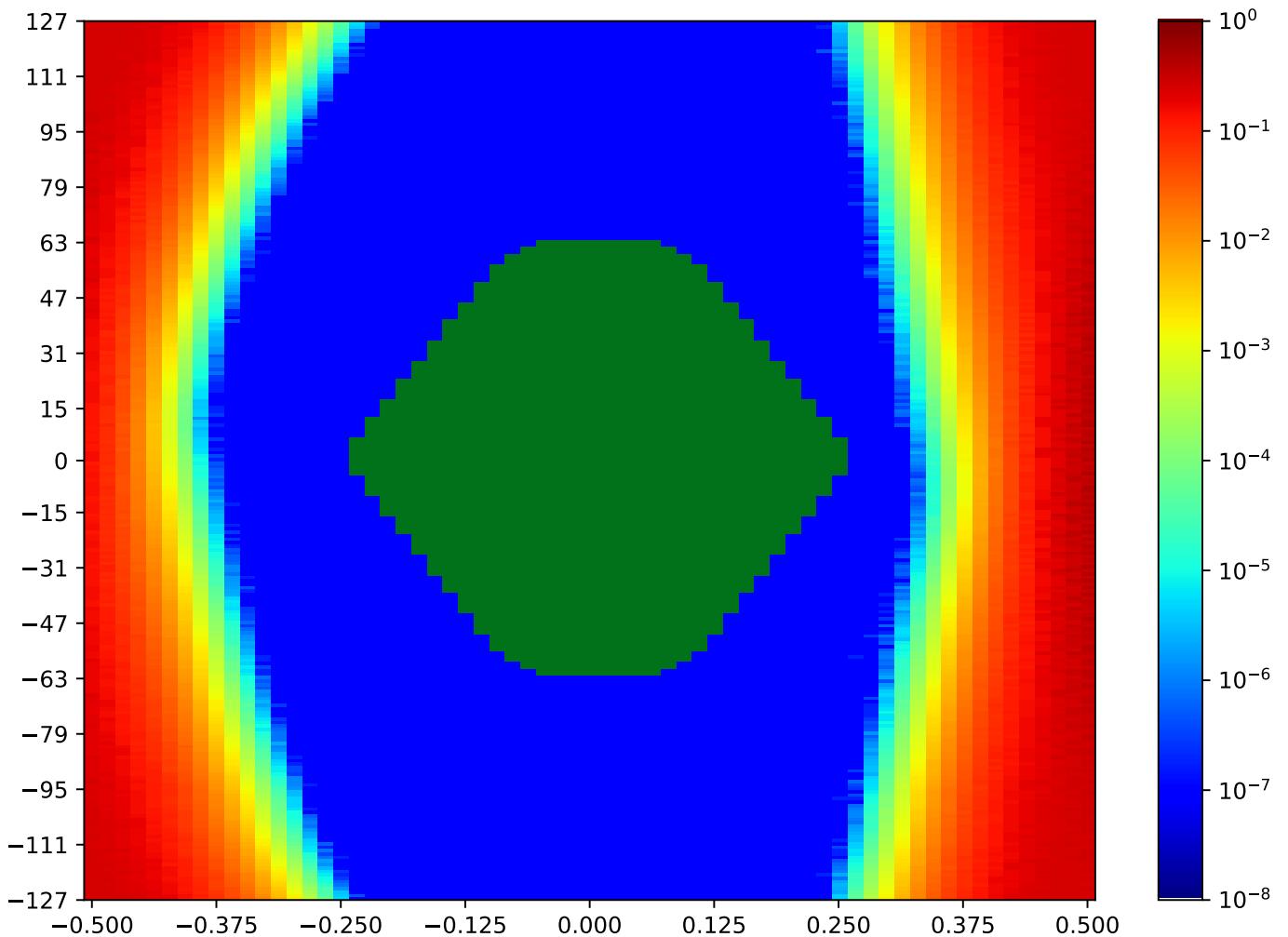


Figure 2.59: TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.5.7 TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

Table 2.55: TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:57:04		2018-Jan-24 03:58:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23835	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

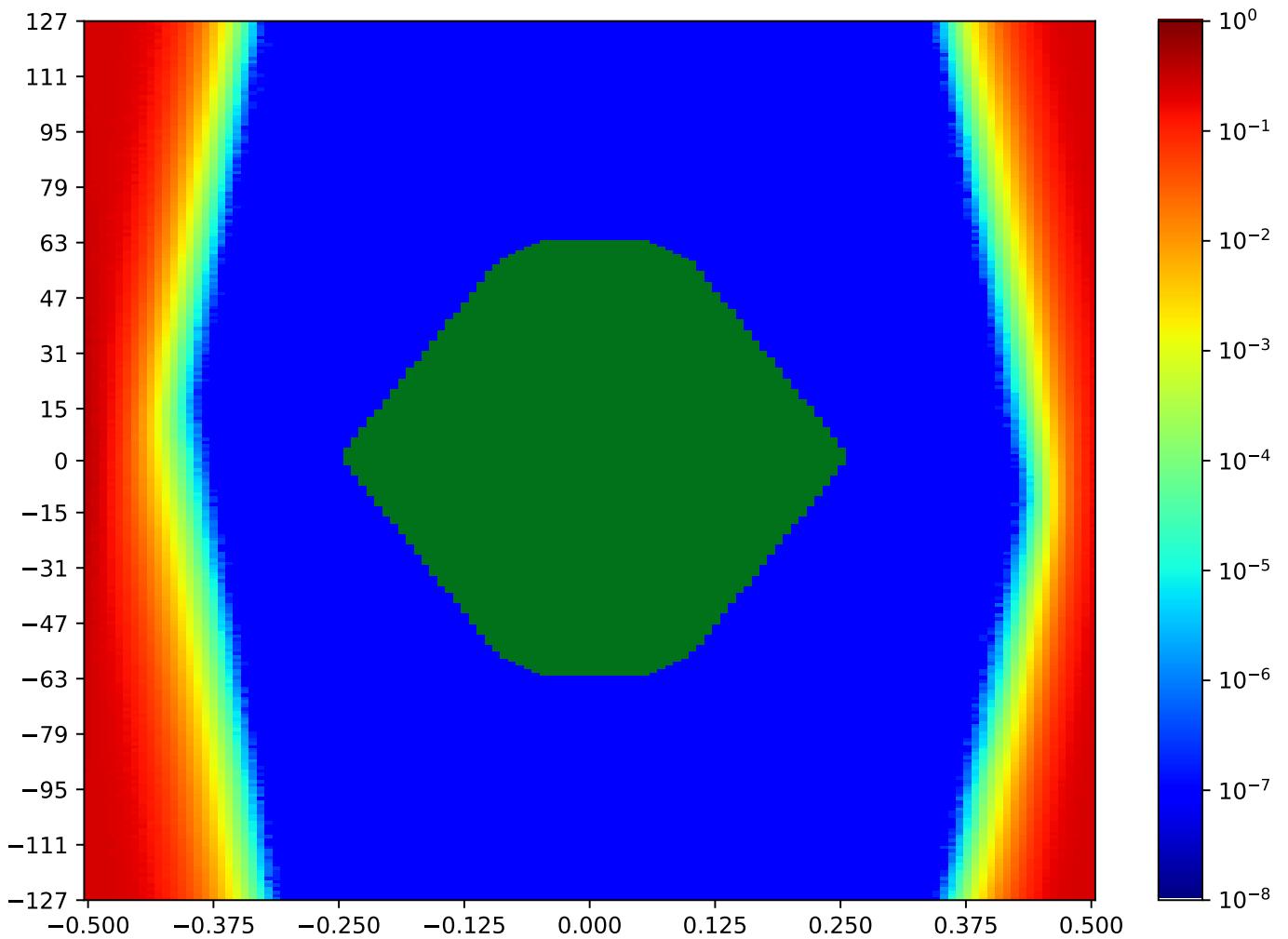


Figure 2.60: TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.5.8 TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

Table 2.56: TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 03:59:25		2018-Jan-24 04:00:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23218	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

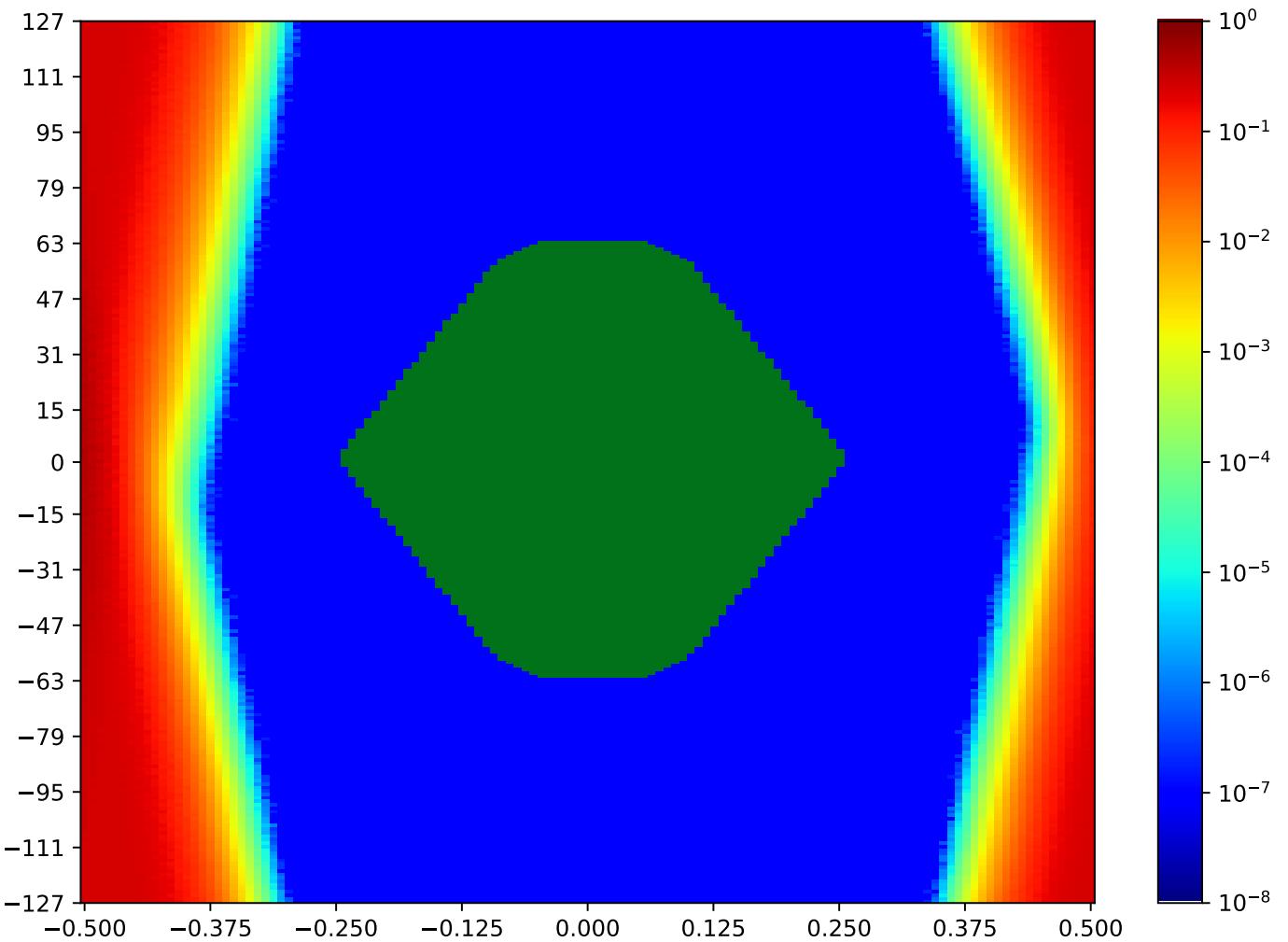


Figure 2.61: TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

Call back to summary Figure 2.53. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.6 TRP J1 QSFP Loopback

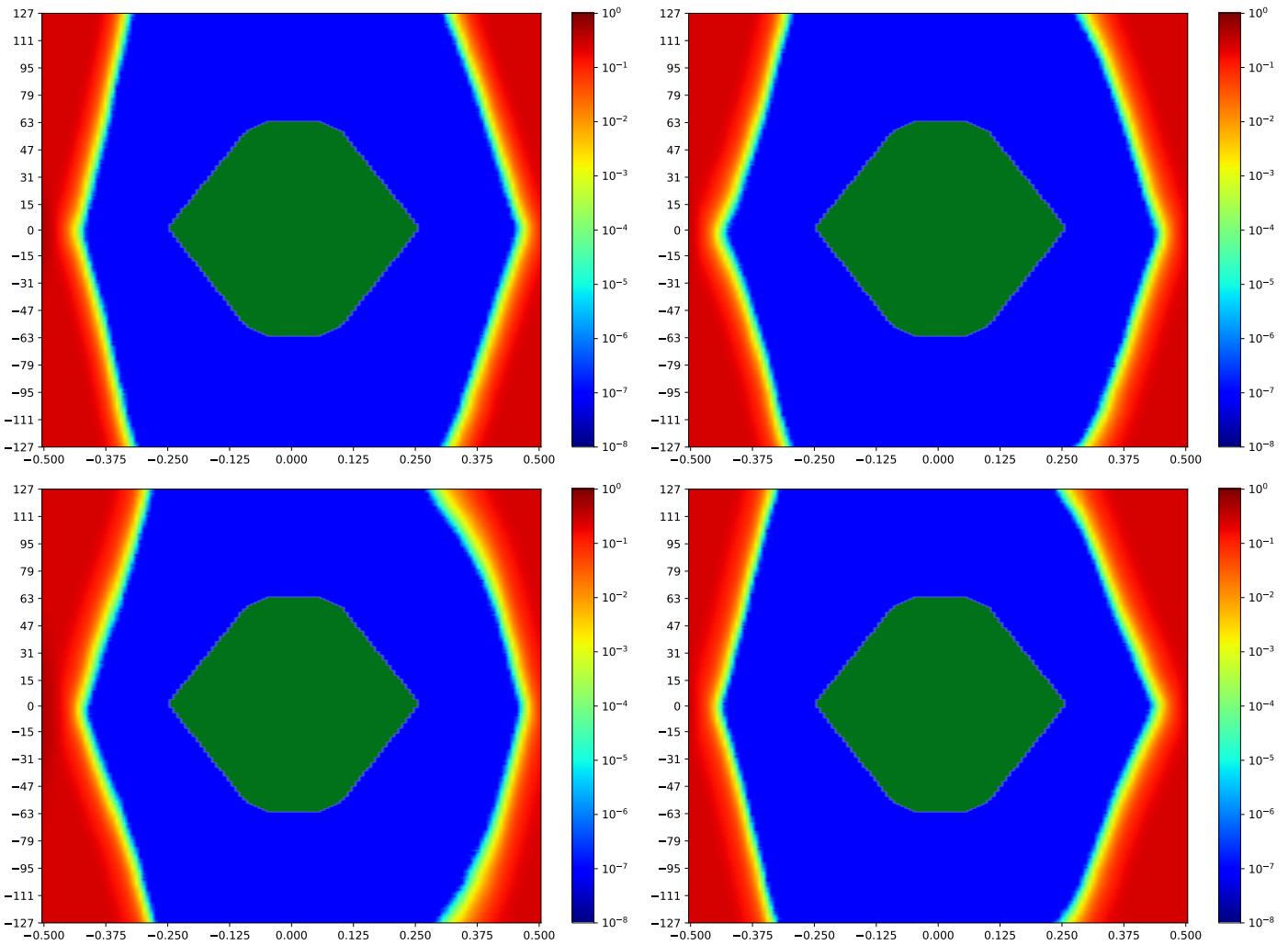


Figure 2.62: TRP J1 QSFP Loopback

A cross-reference to Figure 2.62. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.
Next summary Figure 2.67.

2.6.1 TRP_FPGA-J1-00–J1-00-TRP_FPGA

Table 2.57: TRP_FPGA-J1-00–J1-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:01:43		2018-Jan-24 04:02:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24091	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

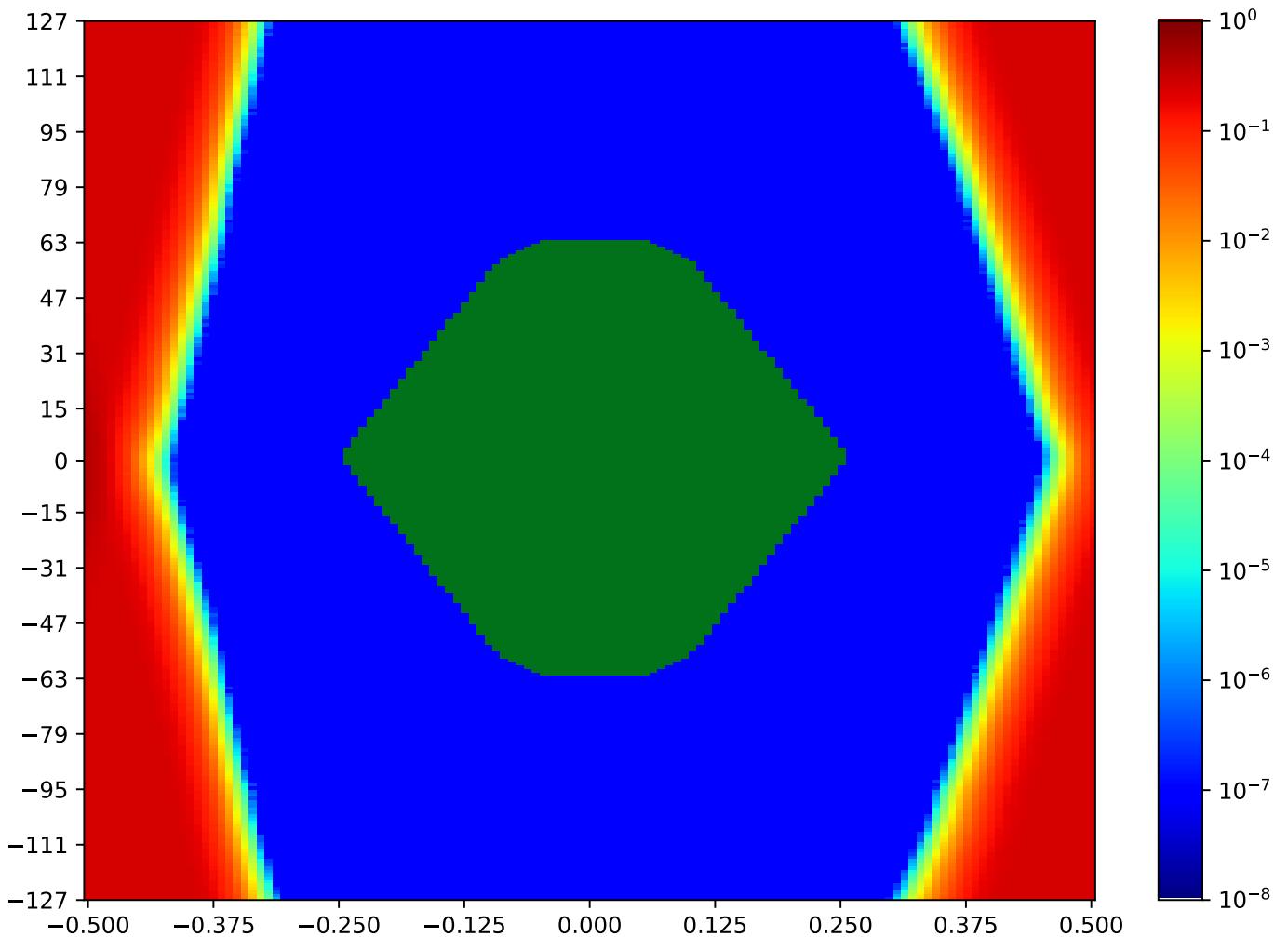


Figure 2.63: TRP_FPGA-J1-00–J1-00-TRP_FPGA

Call back to summary Figure 2.62. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.6.2 TRP_FPGA-J1-01–J1-01-TRP_FPGA

Table 2.58: TRP_FPGA-J1-01–J1-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:02:52		2018-Jan-24 04:04:00	
Reset RX	OA	HO		HO (%)	
true	23169	108		83.72%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

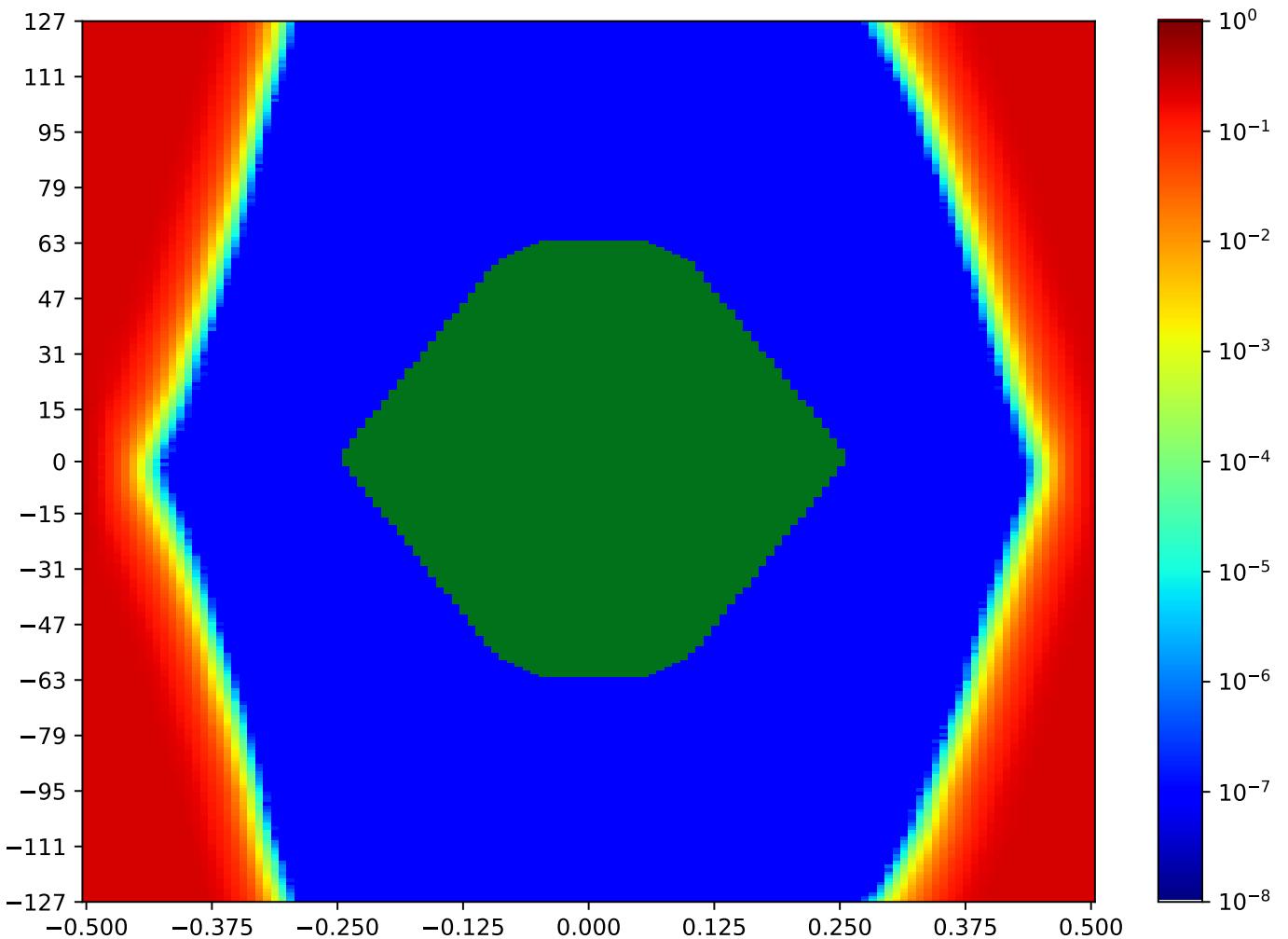


Figure 2.64: TRP_FPGA-J1-01–J1-01-TRP_FPGA

Call back to summary Figure 2.62. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.6.3 TRP_FPGA-J1-02–J1-02-TRP_FPGA

Table 2.59: TRP_FPGA-J1-02–J1-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:04:00		2018-Jan-24 04:05:09	
Reset RX	OA	HO		HO (%)	
true	23460	109		84.50%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

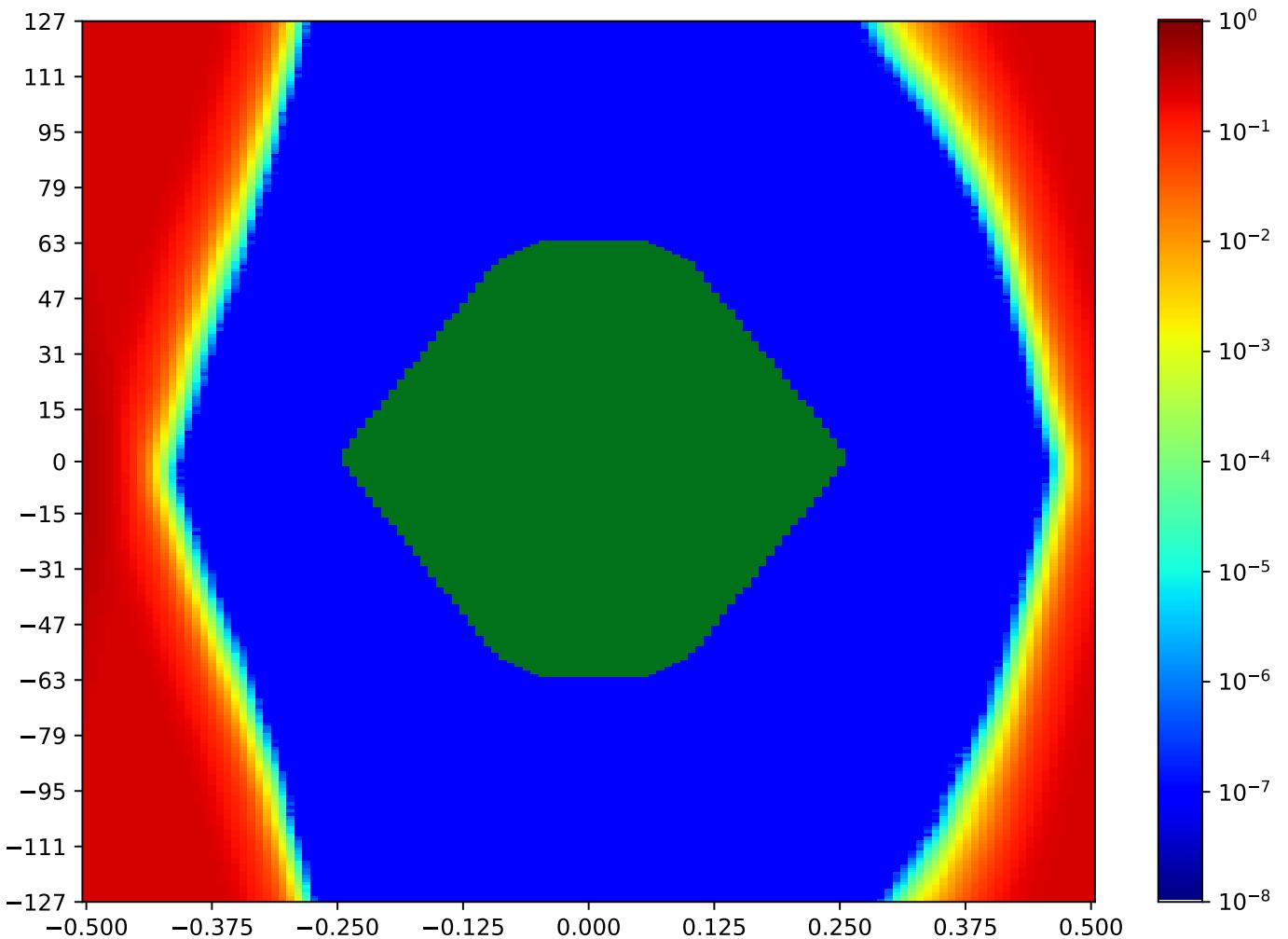


Figure 2.65: TRP_FPGA-J1-02–J1-02-TRP_FPGA

Call back to summary Figure 2.62. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.6.4 TRP_FPGA-J1-03–J1-03-TRP_FPGA

Table 2.60: TRP_FPGA-J1-03–J1-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:05:09		2018-Jan-24 04:06:18	
Reset RX	OA	HO		HO (%)	
true	23051	108		83.72%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

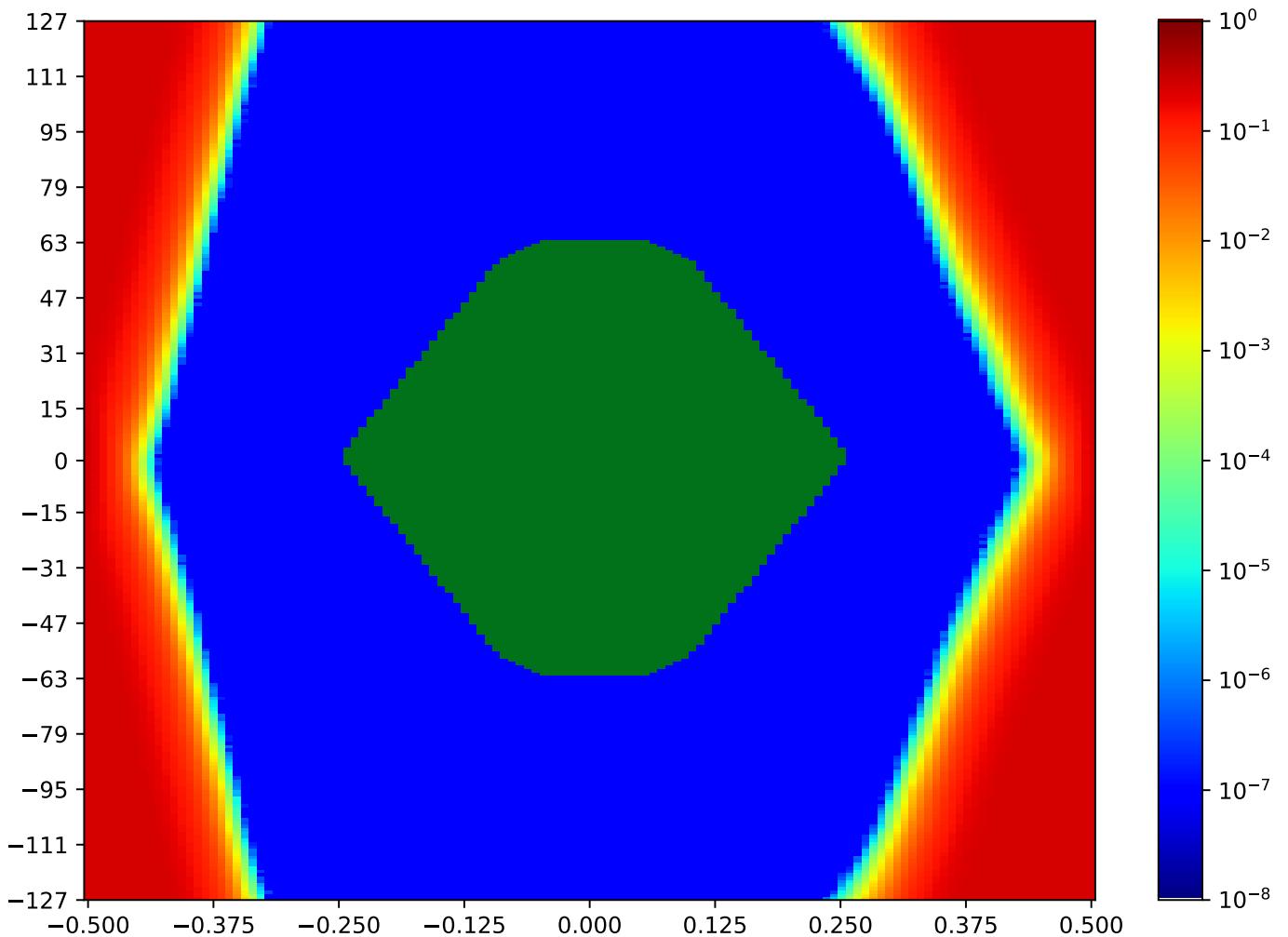


Figure 2.66: TRP_FPGA-J1-03–J1-03-TRP_FPGA

Call back to summary Figure 2.62. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.7 TRP J3 SFP Loopback

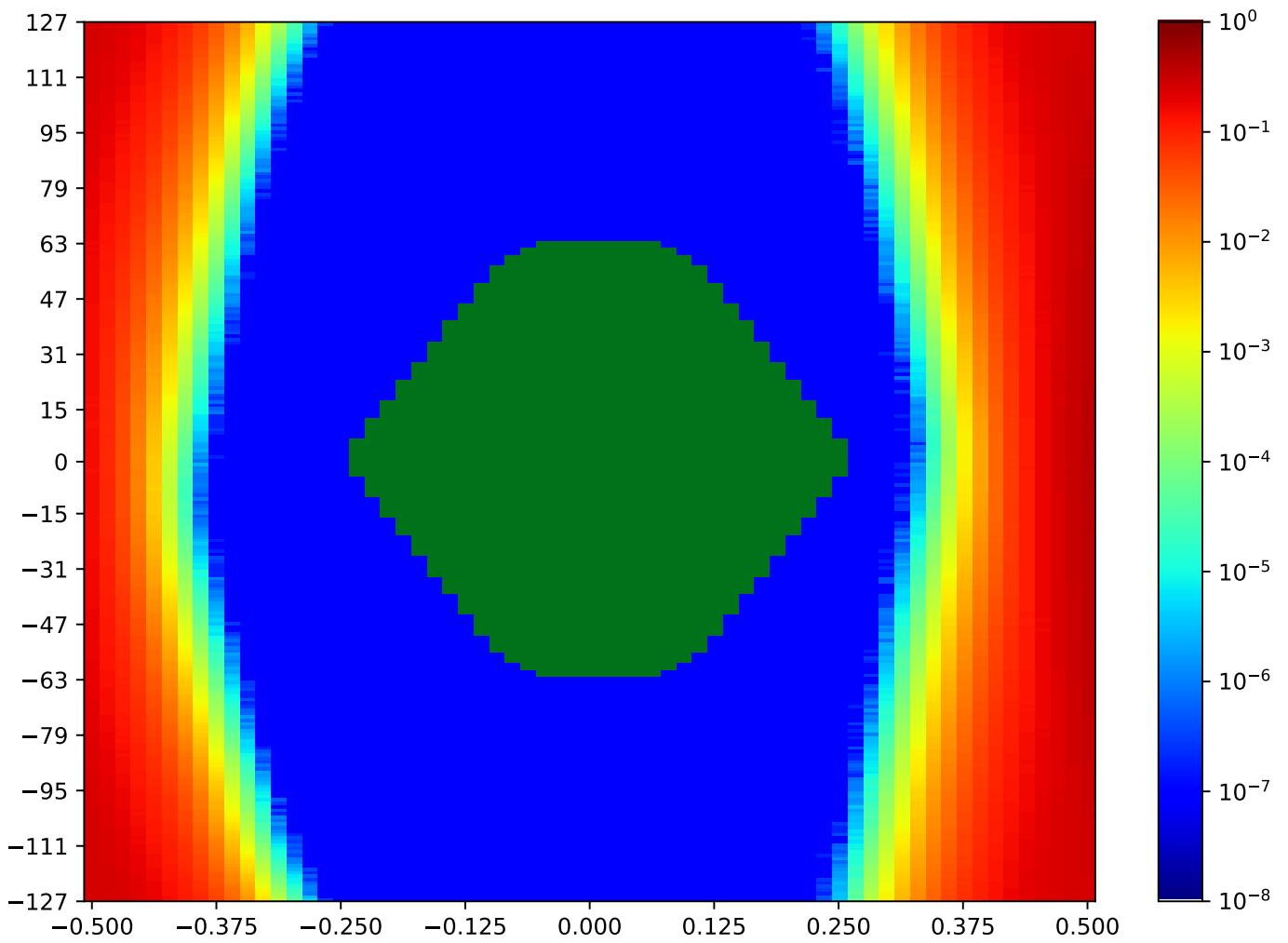


Figure 2.67: TRP J3 SFP Loopback

A cross-reference to Figure 2.67. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.
Next summary Figure 2.69.

2.7.1 TRP_FPGA-J3-00–J3-00-TRP_FPGA

Table 2.61: TRP_FPGA-J3-00–J3-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:06:19		2018-Jan-24 04:06:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9895	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

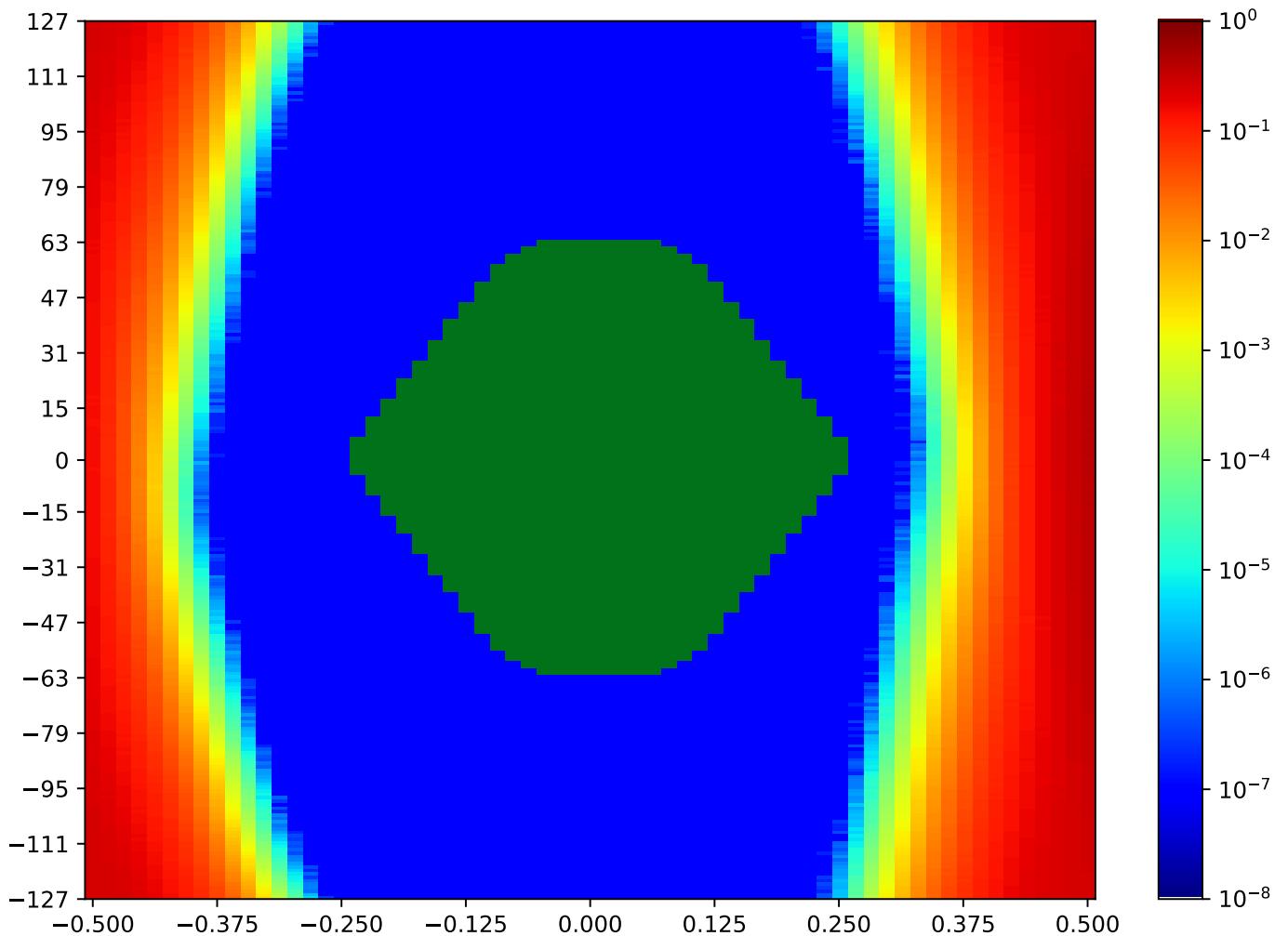


Figure 2.68: TRP_FPGA-J3-00–J3-00-TRP_FPGA

Call back to summary Figure 2.67. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8 MSP_A TRP On board links

A cross-reference to Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.
Next summary Figure 2.98.

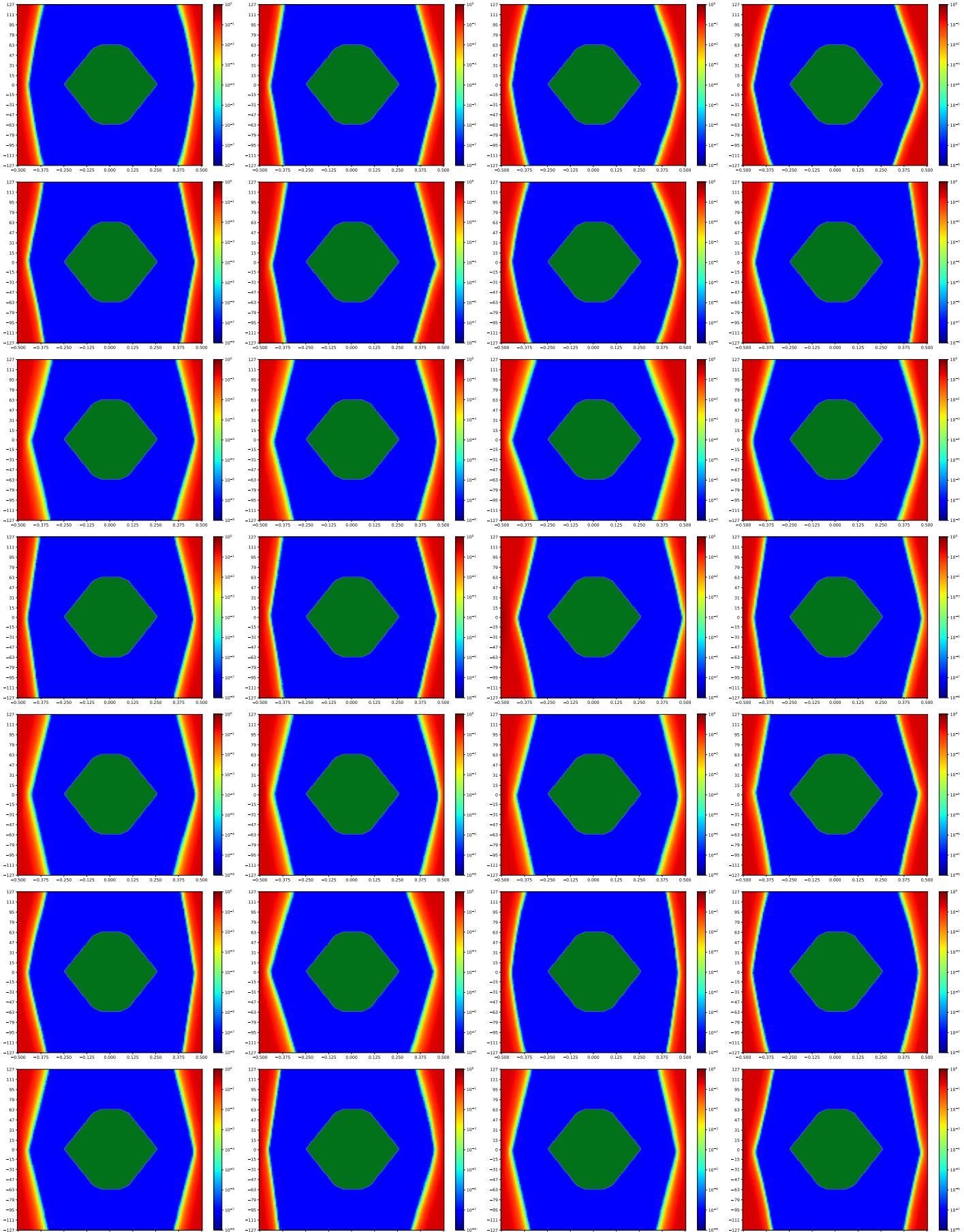


Figure 2.69: MSP_A TRP On board links

2.8.1 MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

Table 2.62: MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:06:55		2018-Jan-24 04:08:07	
Reset RX	OA	HO		HO (%)	
true	26390	113		87.60%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

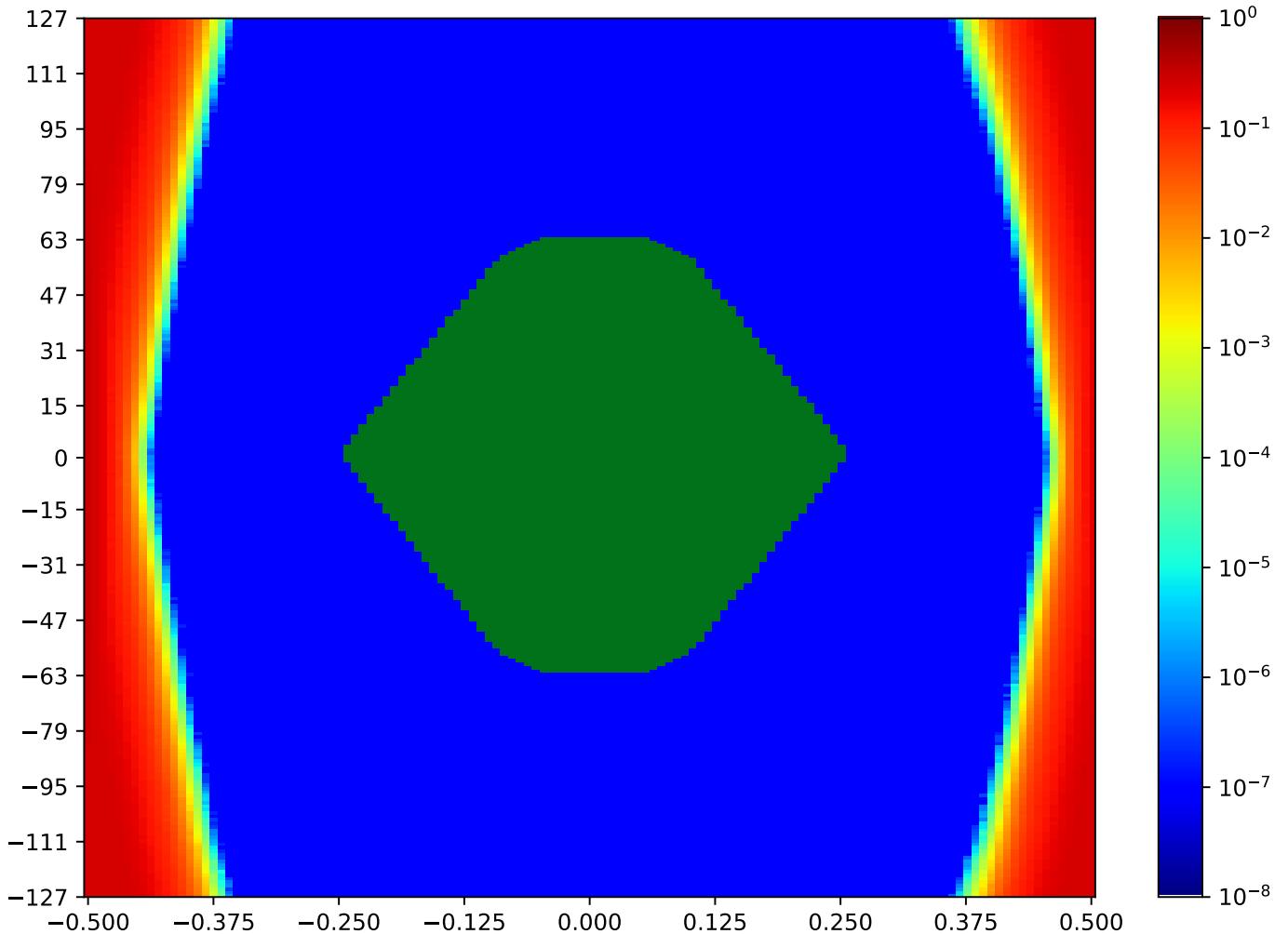


Figure 2.70: MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.2 MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

Table 2.63: MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:08:07		2018-Jan-24 04:09:17	
Reset RX	OA	HO		HO (%)	
true	25962	113		87.60%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

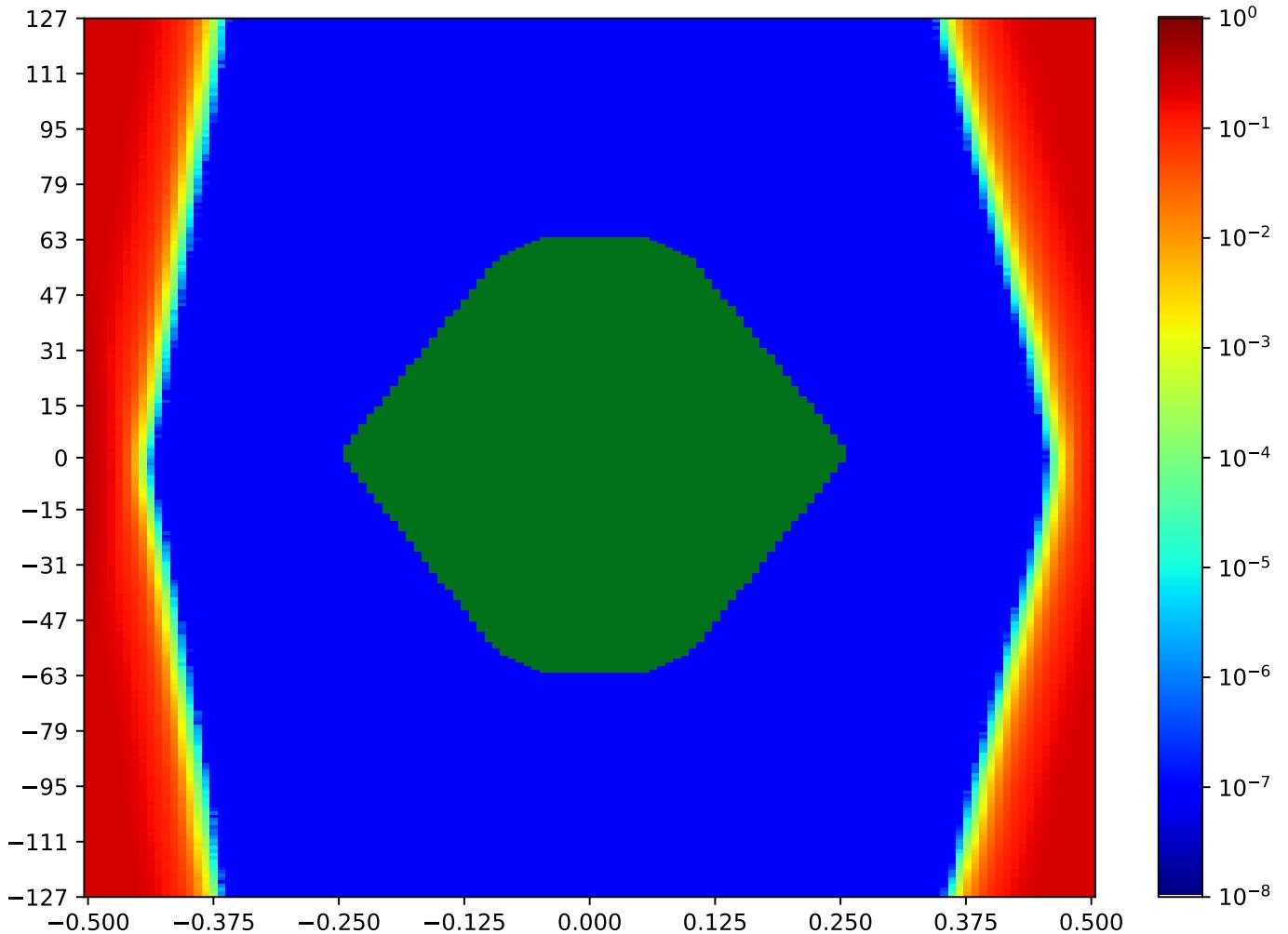


Figure 2.71: MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.3 MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

Table 2.64: MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:09:17		2018-Jan-24 04:10:28	
Reset RX	OA	HO		HO (%)	
true	25694	113		87.60%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

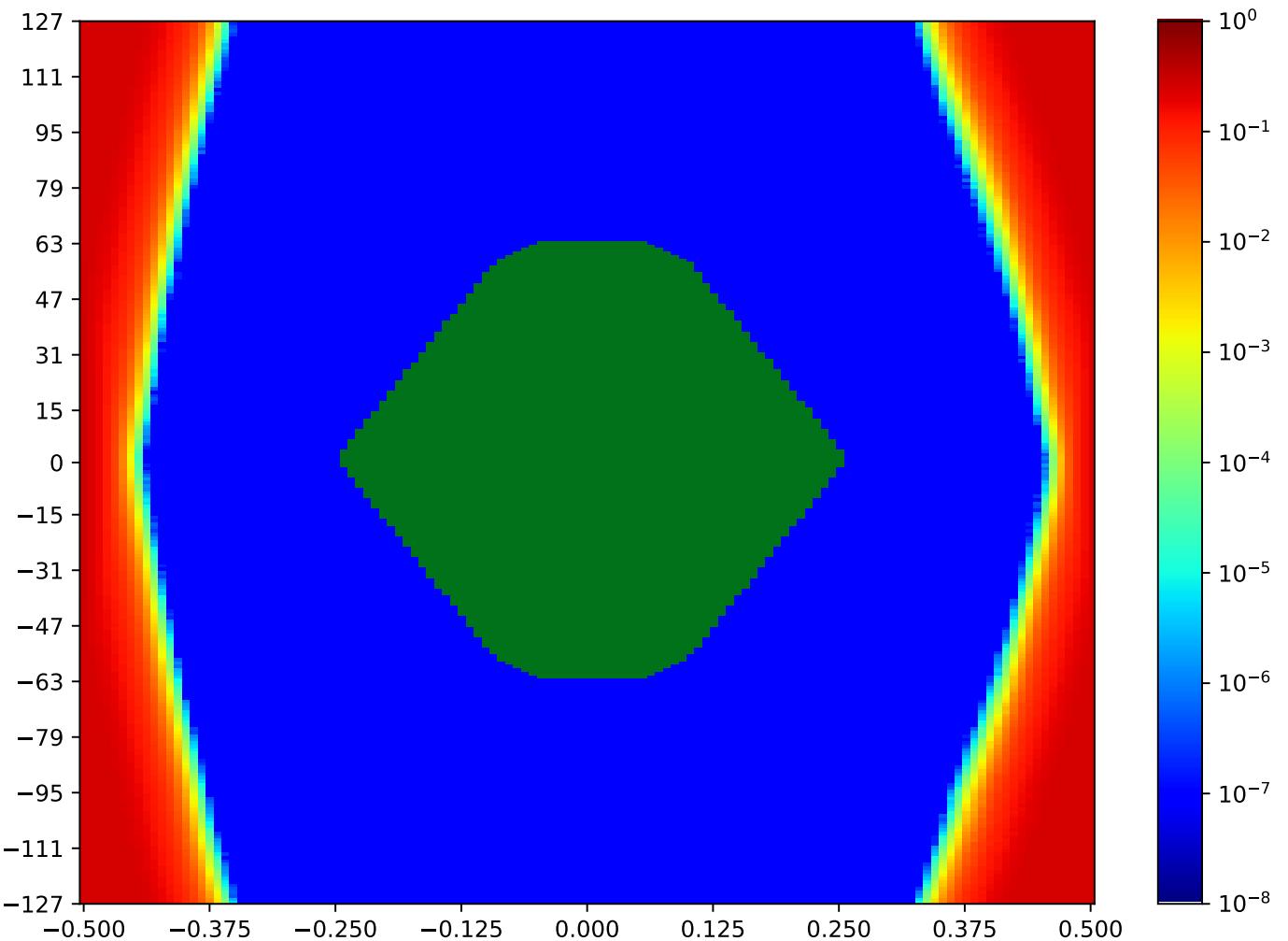


Figure 2.72: MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.4 MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

Table 2.65: MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:10:28		2018-Jan-24 04:11:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25246	115	89.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

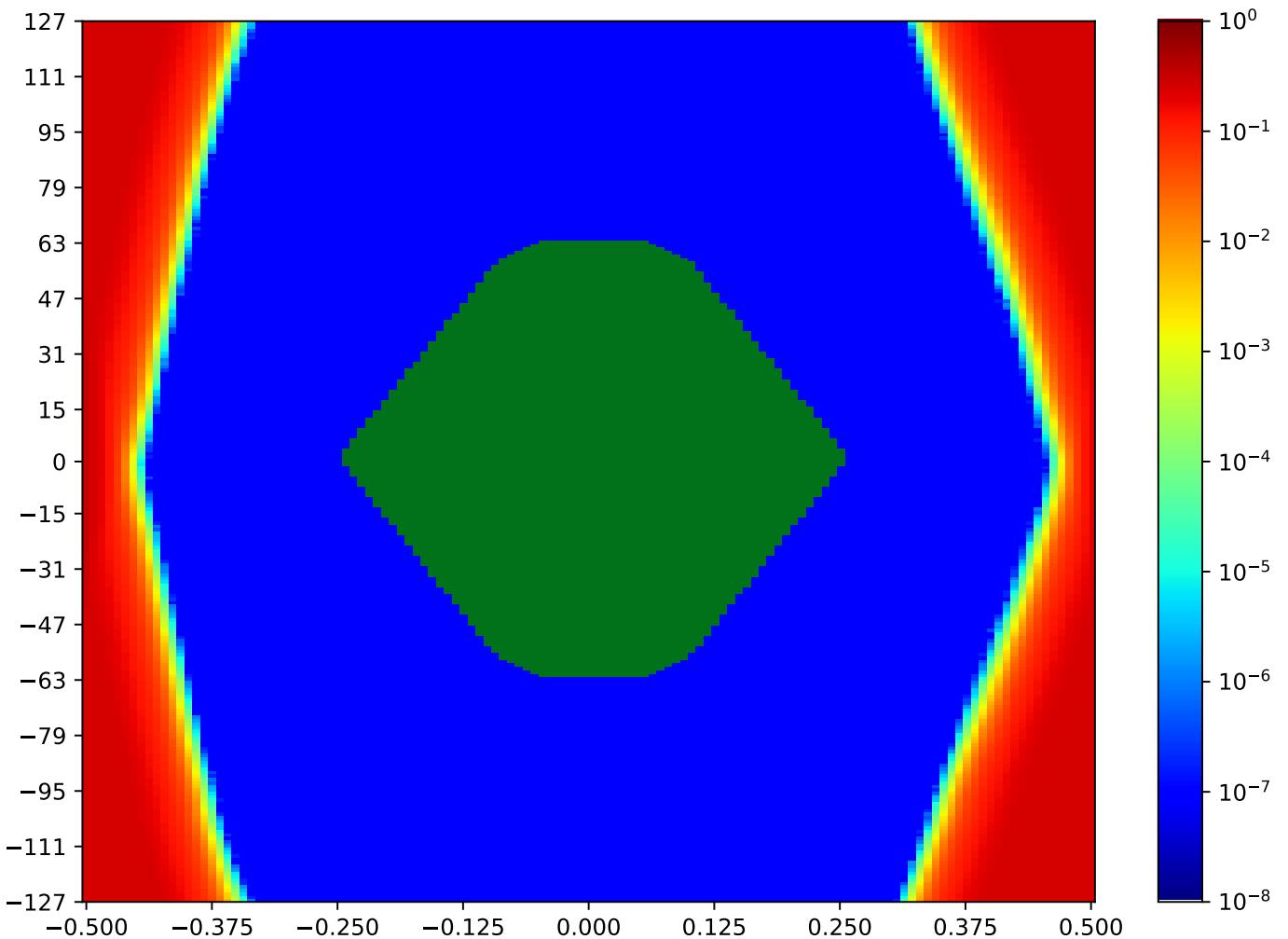


Figure 2.73: MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.5 MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

Table 2.66: MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:11:39		2018-Jan-24 04:12:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26162	114	88.37%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

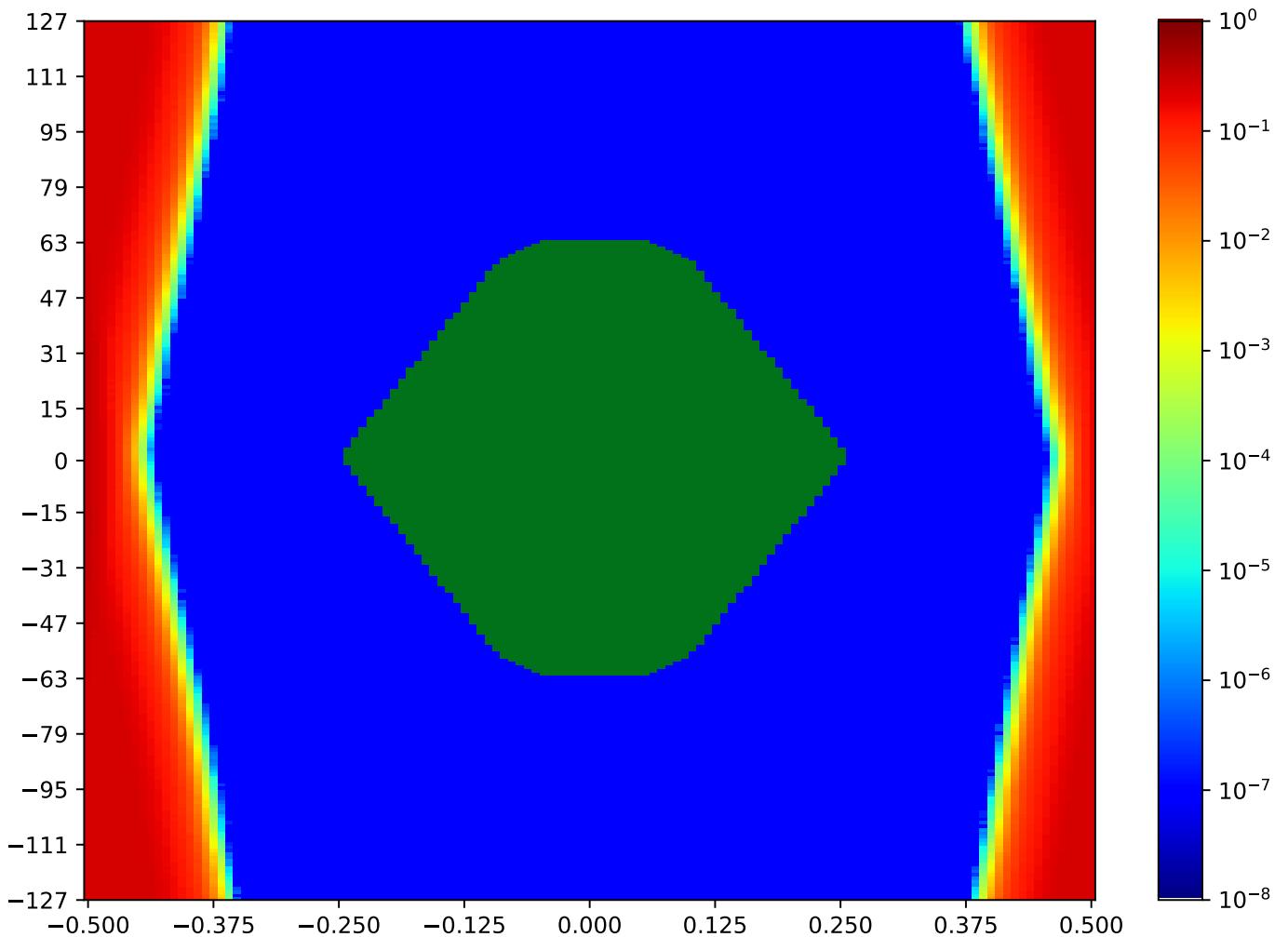


Figure 2.74: MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.6 MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

Table 2.67: MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:12:50		2018-Jan-24 04:14:00	
Reset RX	OA	HO		VO VO (%)	
true	25140	111		86.05%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

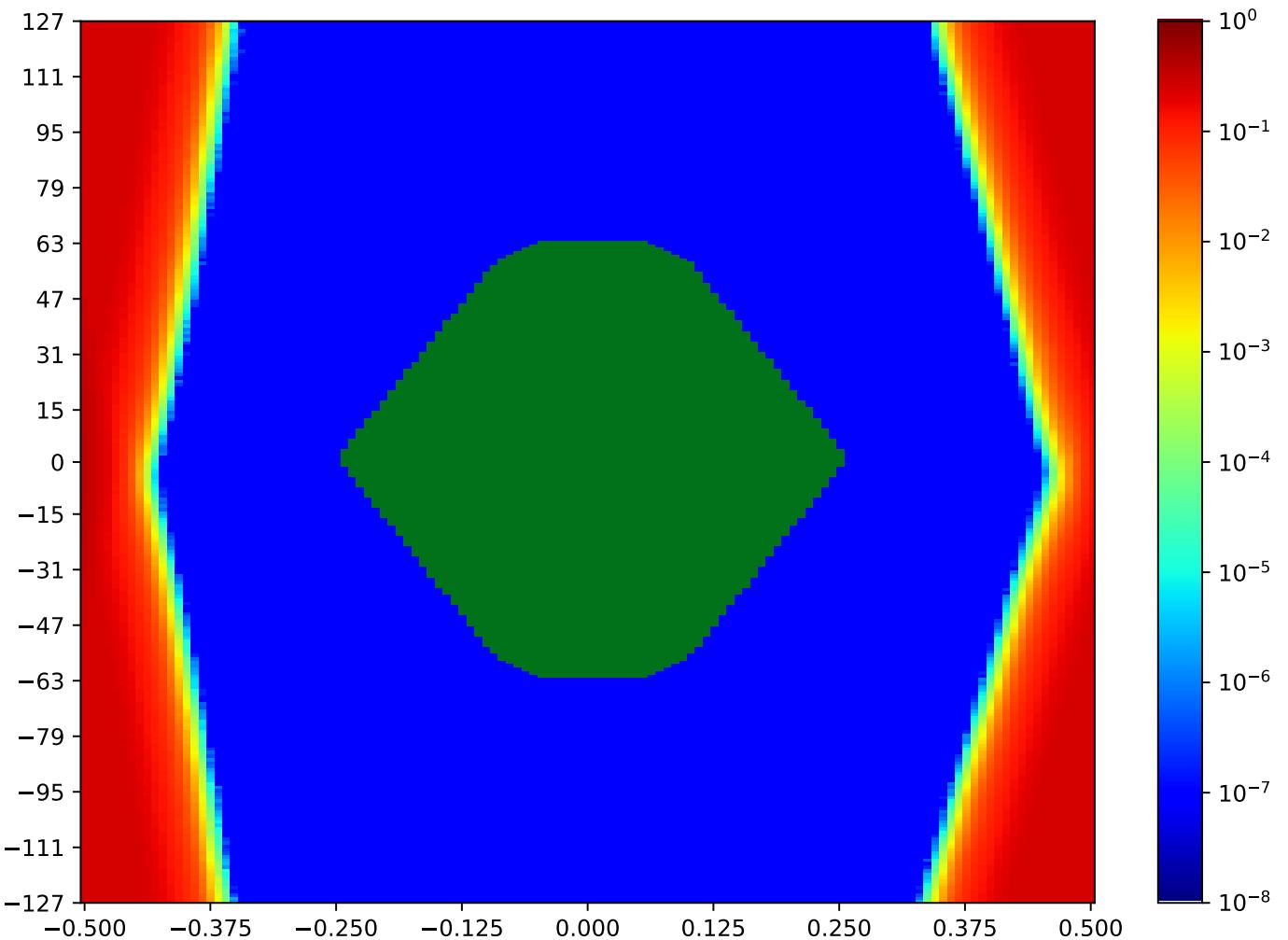


Figure 2.75: MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.7 MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

Table 2.68: MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:14:00		2018-Jan-24 04:15:11	
Reset RX	OA	HO		VO VO (%)	
true	25577	114		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

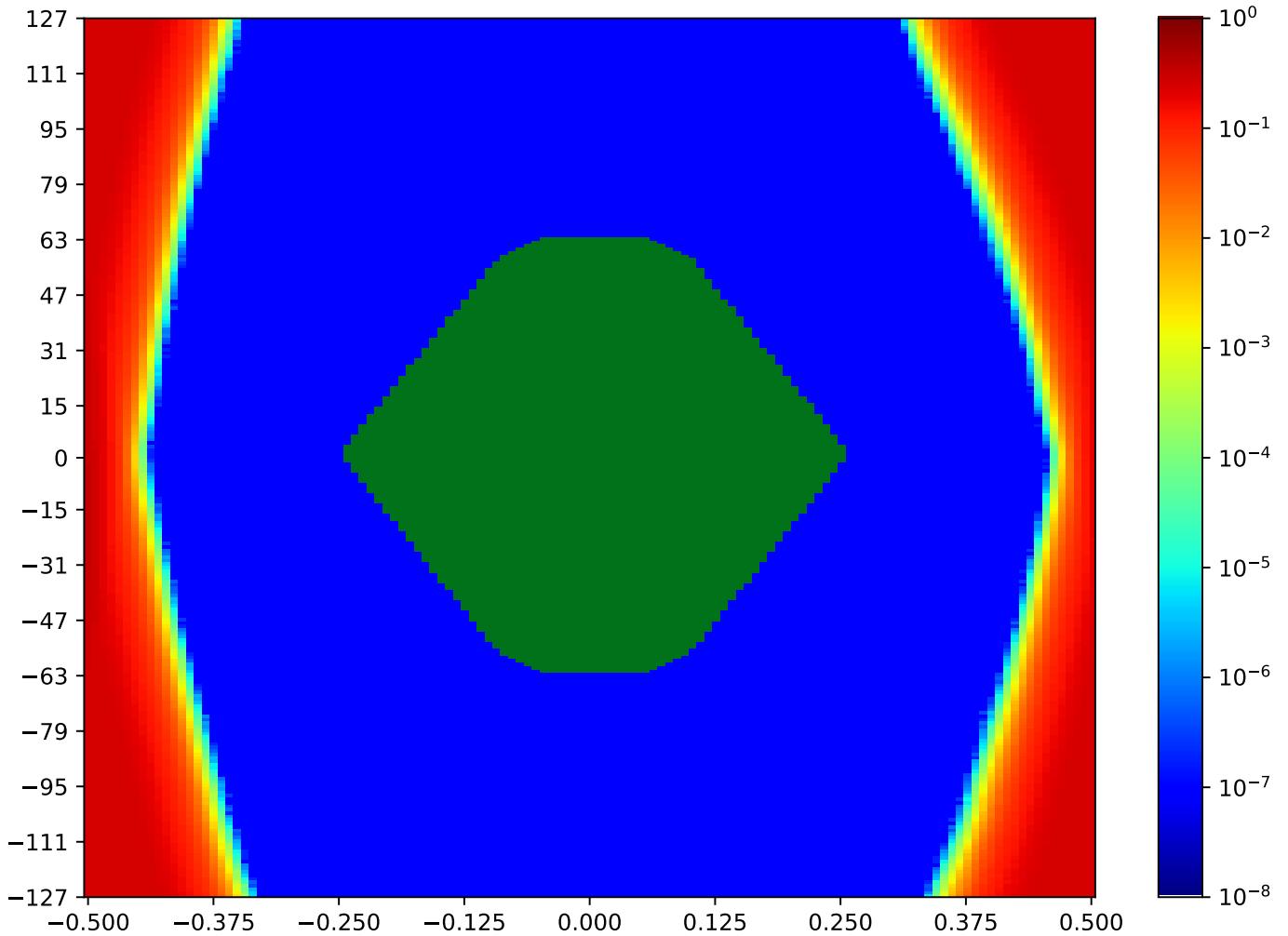


Figure 2.76: MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.8 MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

Table 2.69: MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:15:11		2018-Jan-24 04:16:23	
Reset RX	OA	HO		HO (%)	
true	26077	112		86.82%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

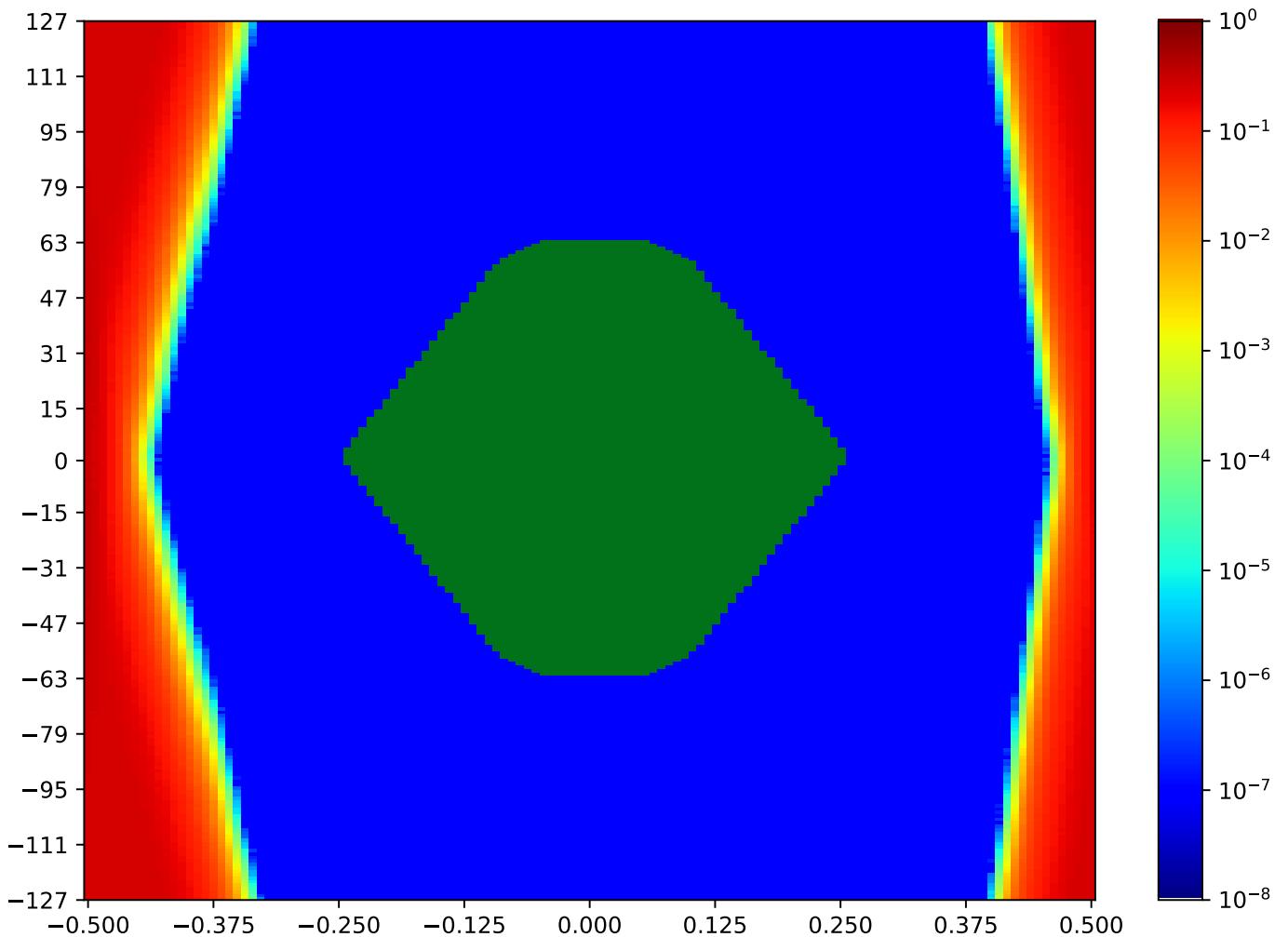


Figure 2.77: MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.9 MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

Table 2.70: MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:16:23		2018-Jan-24 04:17:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24814	111	86.05%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

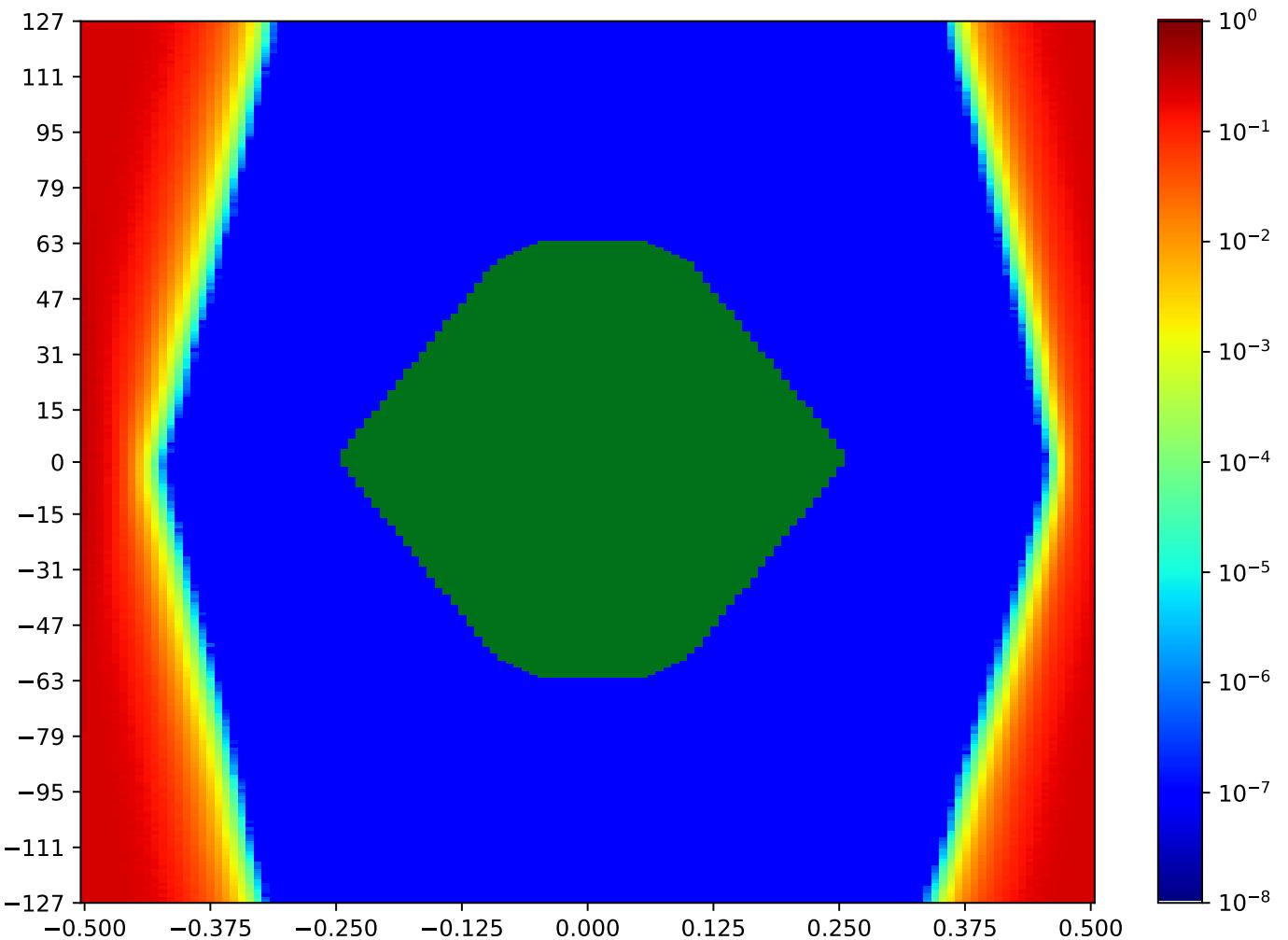


Figure 2.78: MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.10 MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

Table 2.71: MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:17:33		2018-Jan-24 04:18:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24850	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

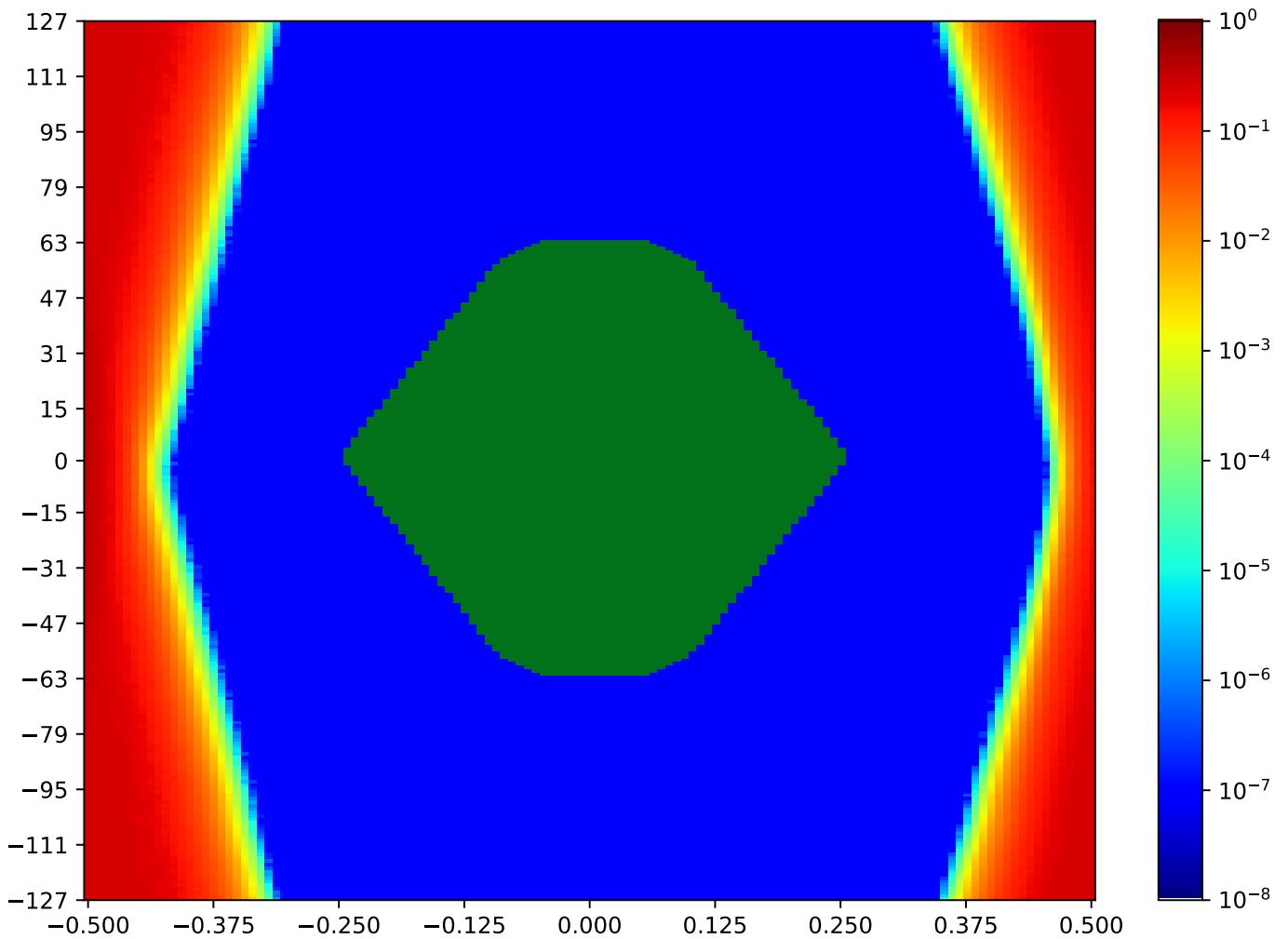


Figure 2.79: MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.11 MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

Table 2.72: MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:18:43		2018-Jan-24 04:19:52	
Reset RX	OA	HO		HO (%)	
true	23569	111		86.05%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

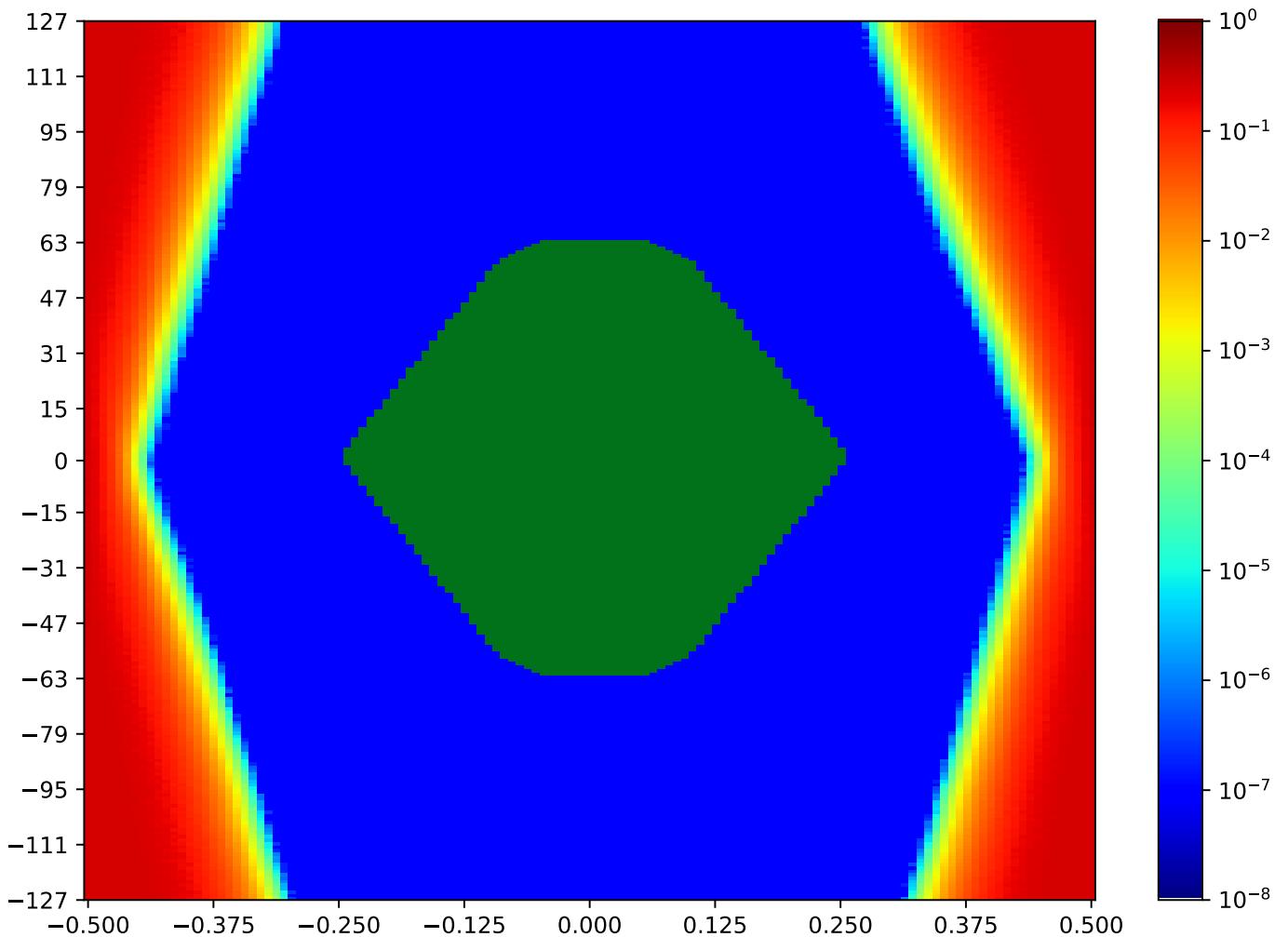


Figure 2.80: MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.12 MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

Table 2.73: MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:19:52		2018-Jan-24 04:21:03	
Reset RX	OA	HO		HO (%)	
true	25462	114		88.37%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

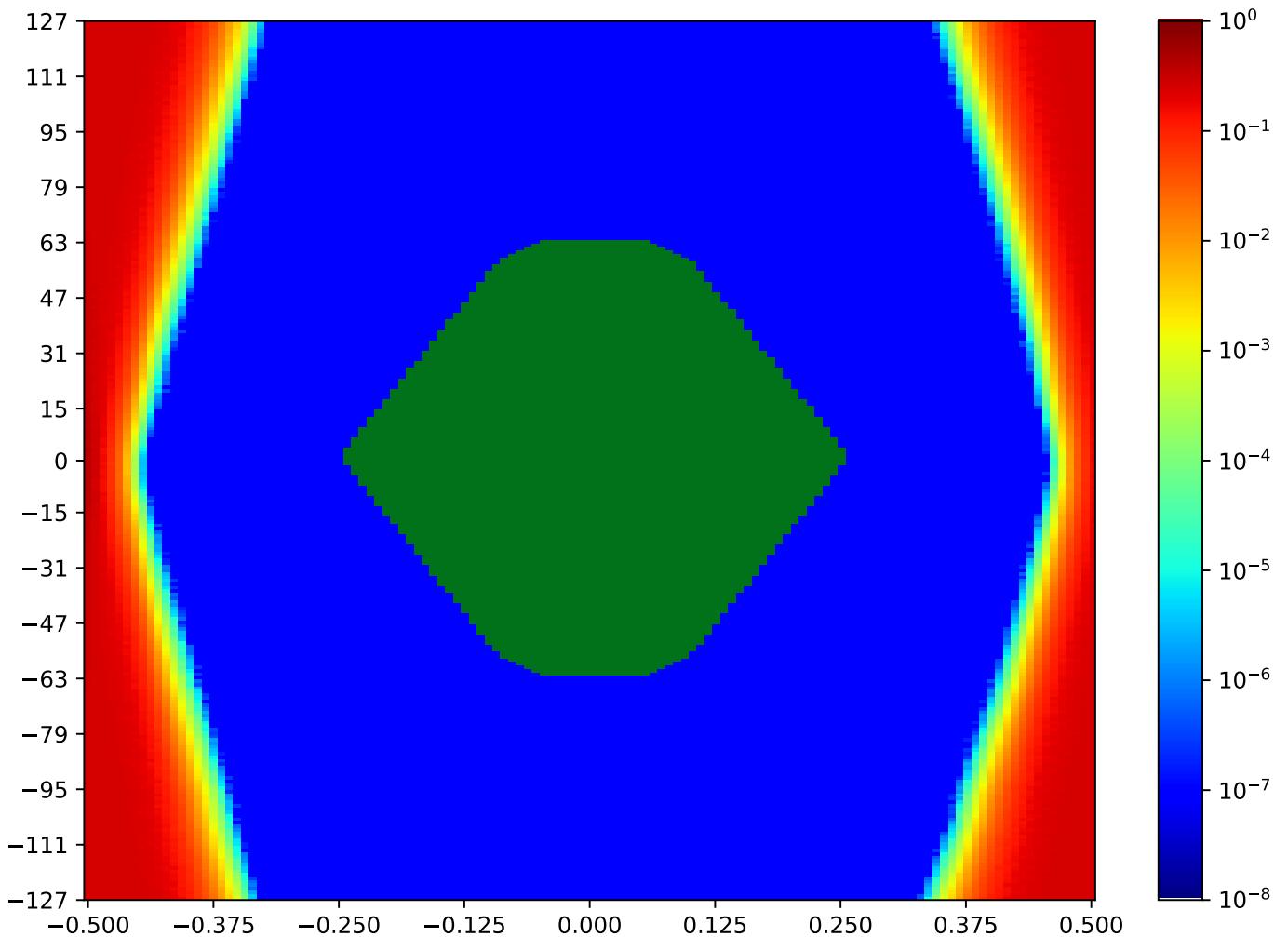


Figure 2.81: MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.13 MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

Table 2.74: MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:21:03		2018-Jan-24 04:22:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26216	114	88.37%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

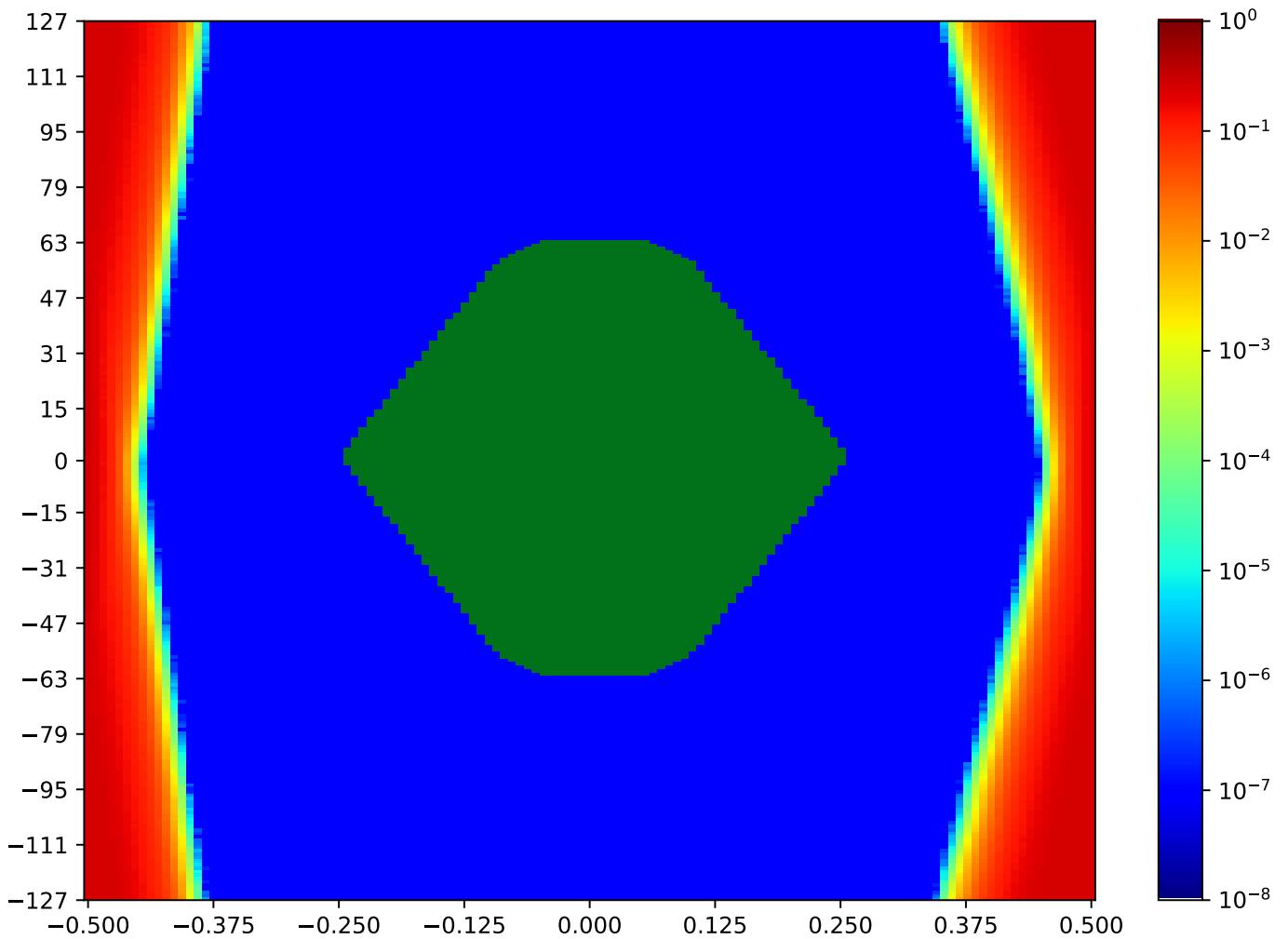


Figure 2.82: MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.14 MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

Table 2.75: MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:22:14		2018-Jan-24 04:23:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26043	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

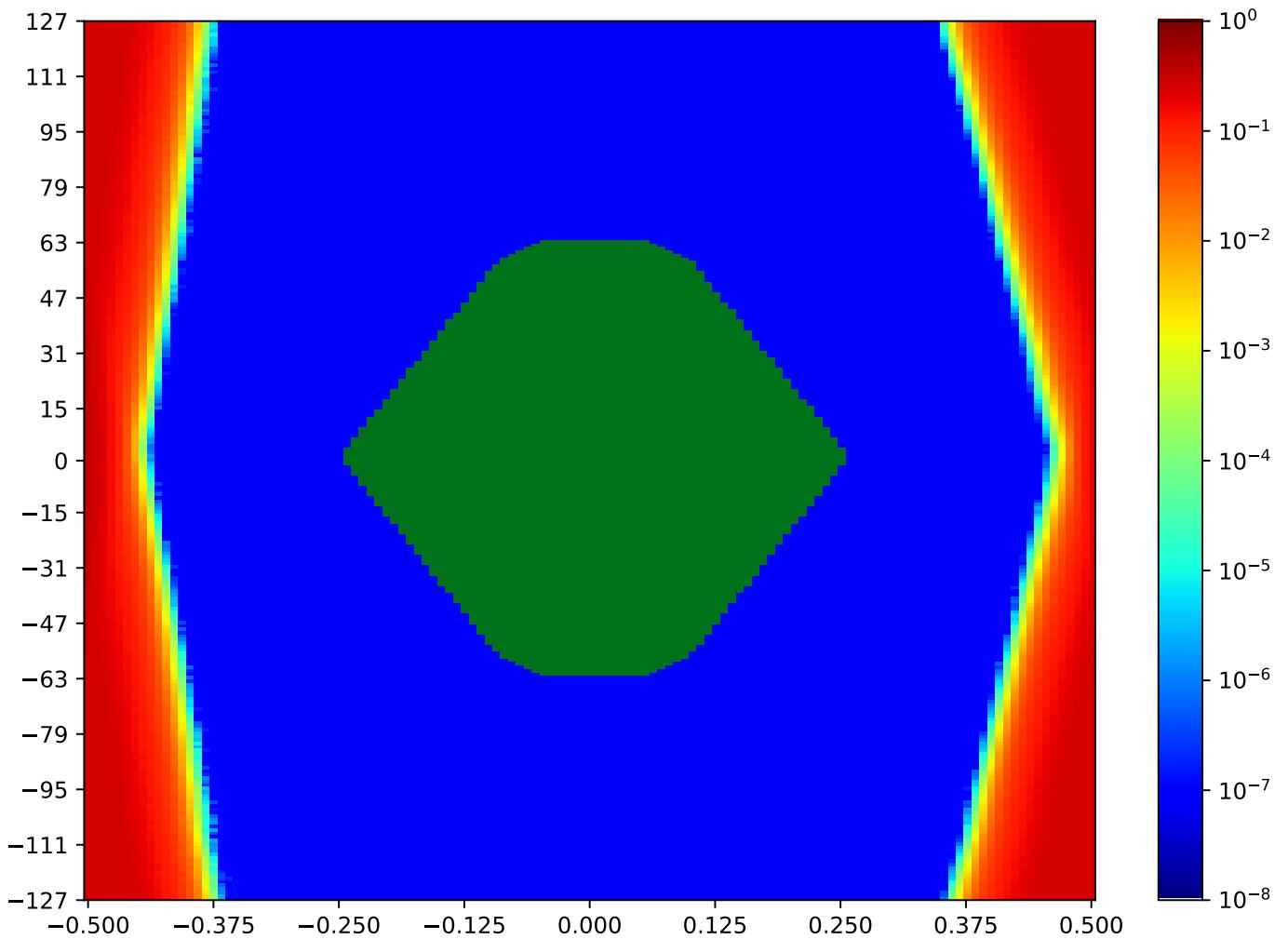


Figure 2.83: MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.15 MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

Table 2.76: MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:23:25		2018-Jan-24 04:24:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25265	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

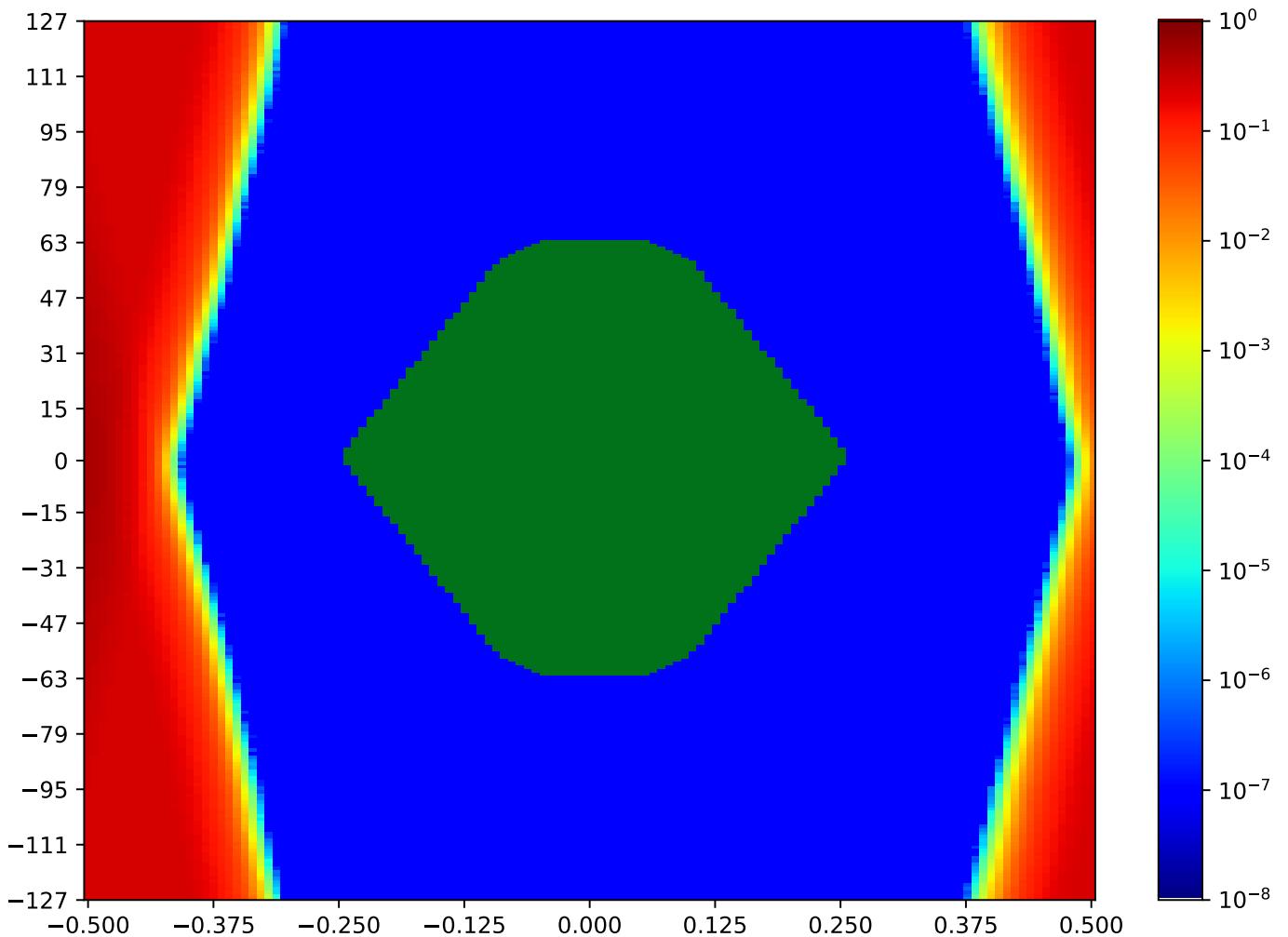


Figure 2.84: MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.16 MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

Table 2.77: MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:24:35		2018-Jan-24 04:25:46	
Reset RX	OA	HO		HO (%)	
true	26431	114		88.37%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

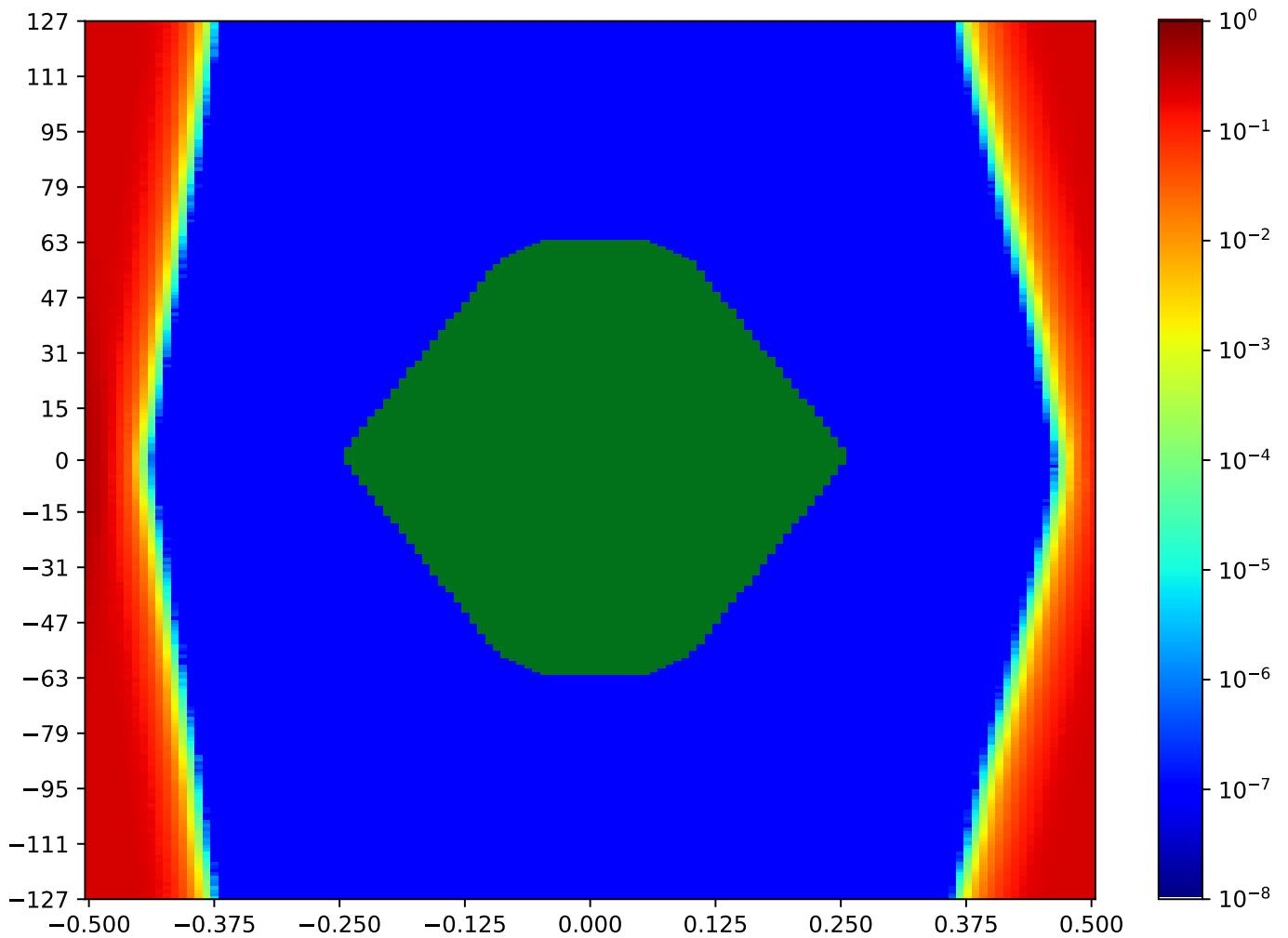


Figure 2.85: MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.17 MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

Table 2.78: MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:25:46		2018-Jan-24 04:26:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25058	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

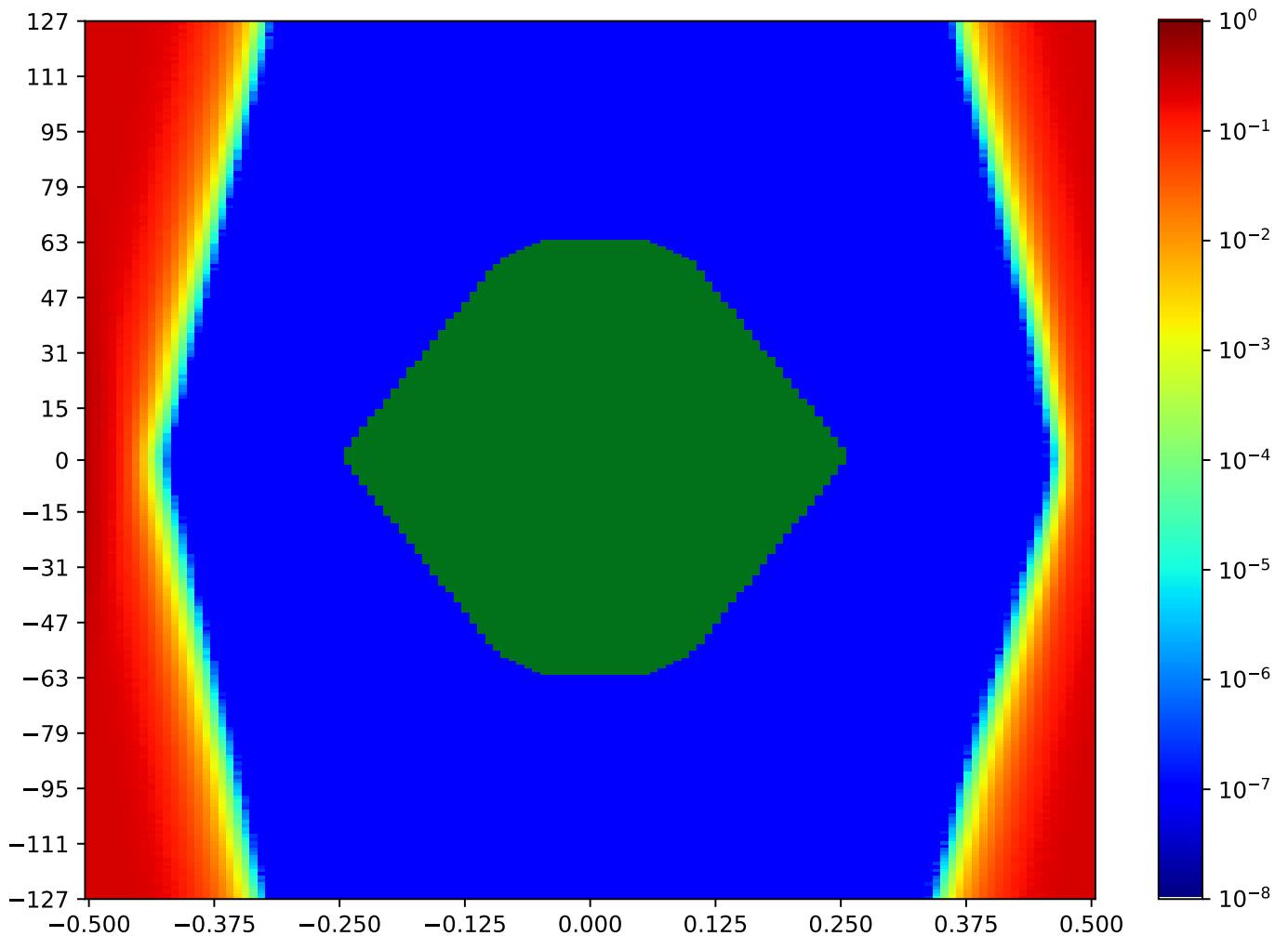


Figure 2.86: MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.18 MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

Table 2.79: MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:26:57		2018-Jan-24 04:28:09	
Reset RX	OA	HO		HO (%)	
true	25220	113		87.60%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

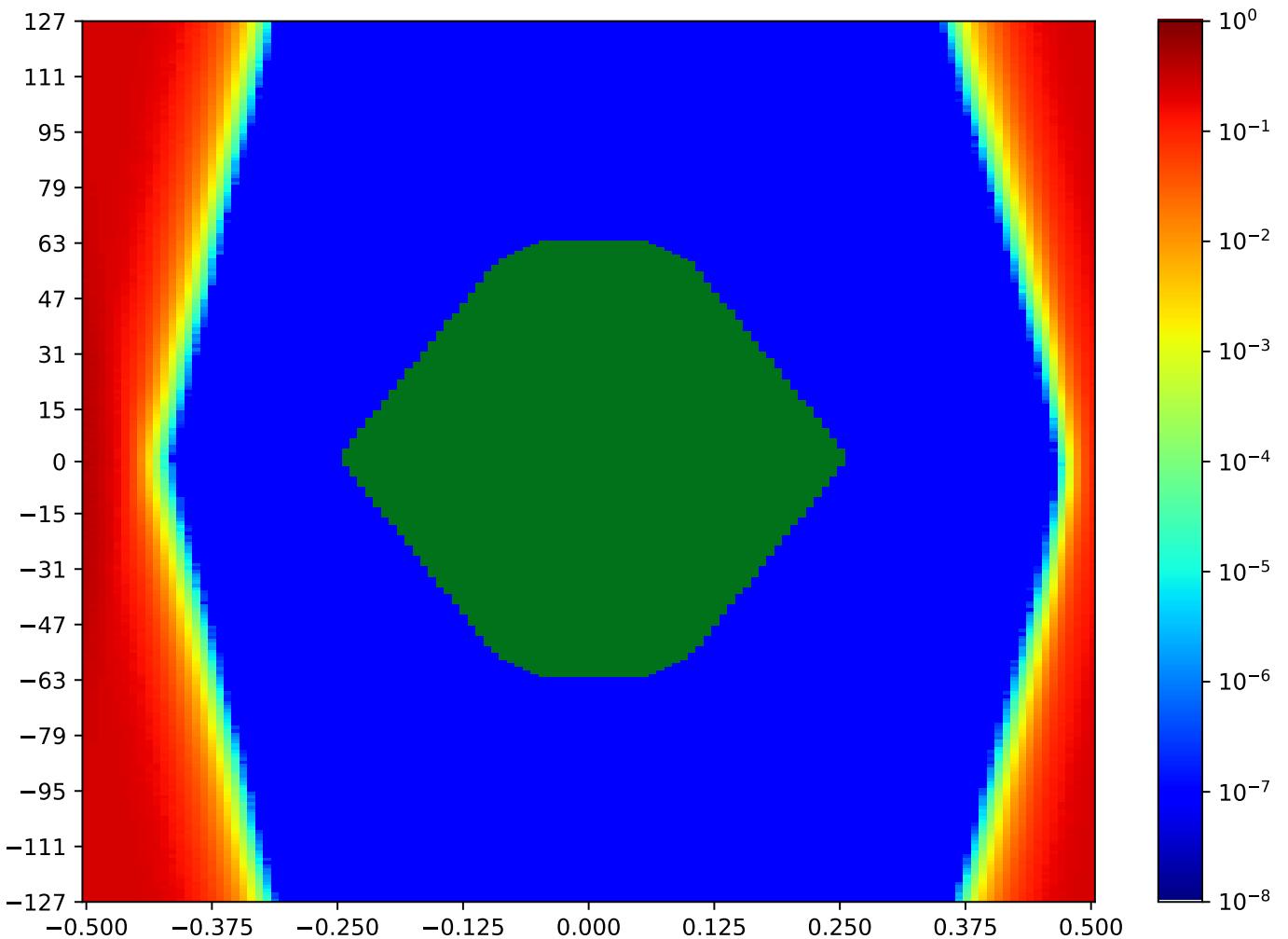


Figure 2.87: MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.19 MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

Table 2.80: MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:28:09		2018-Jan-24 04:29:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24698	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

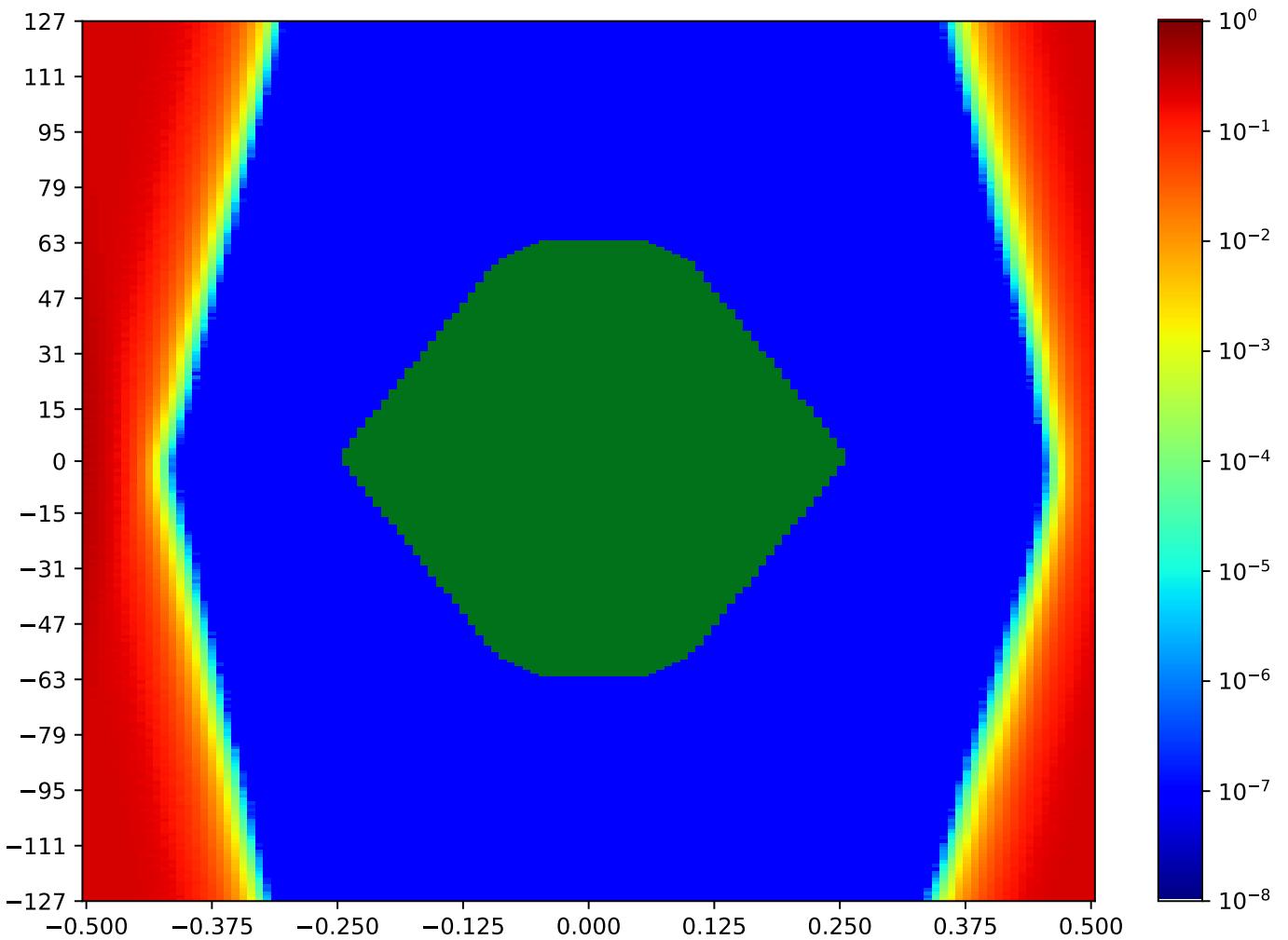


Figure 2.88: MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.20 MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

Table 2.81: MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:29:18		2018-Jan-24 04:30:28	
Reset RX	OA	HO		HO (%)	
true	24985	110		85.27%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

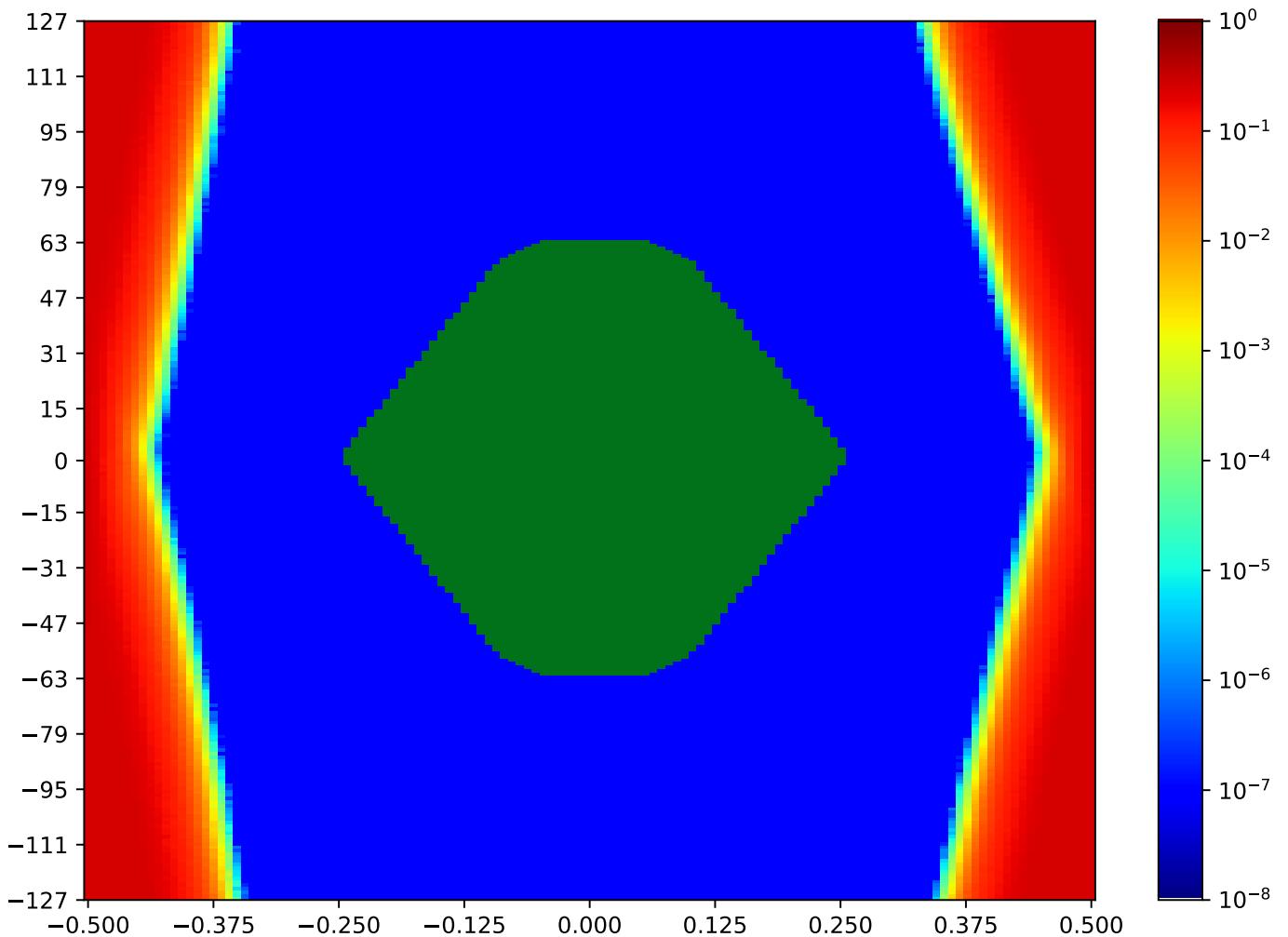


Figure 2.89: MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.21 MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

Table 2.82: MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:30:28		2018-Jan-24 04:31:39	
Reset RX	OA	HO		HO (%)	
true	26272	113		87.60%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

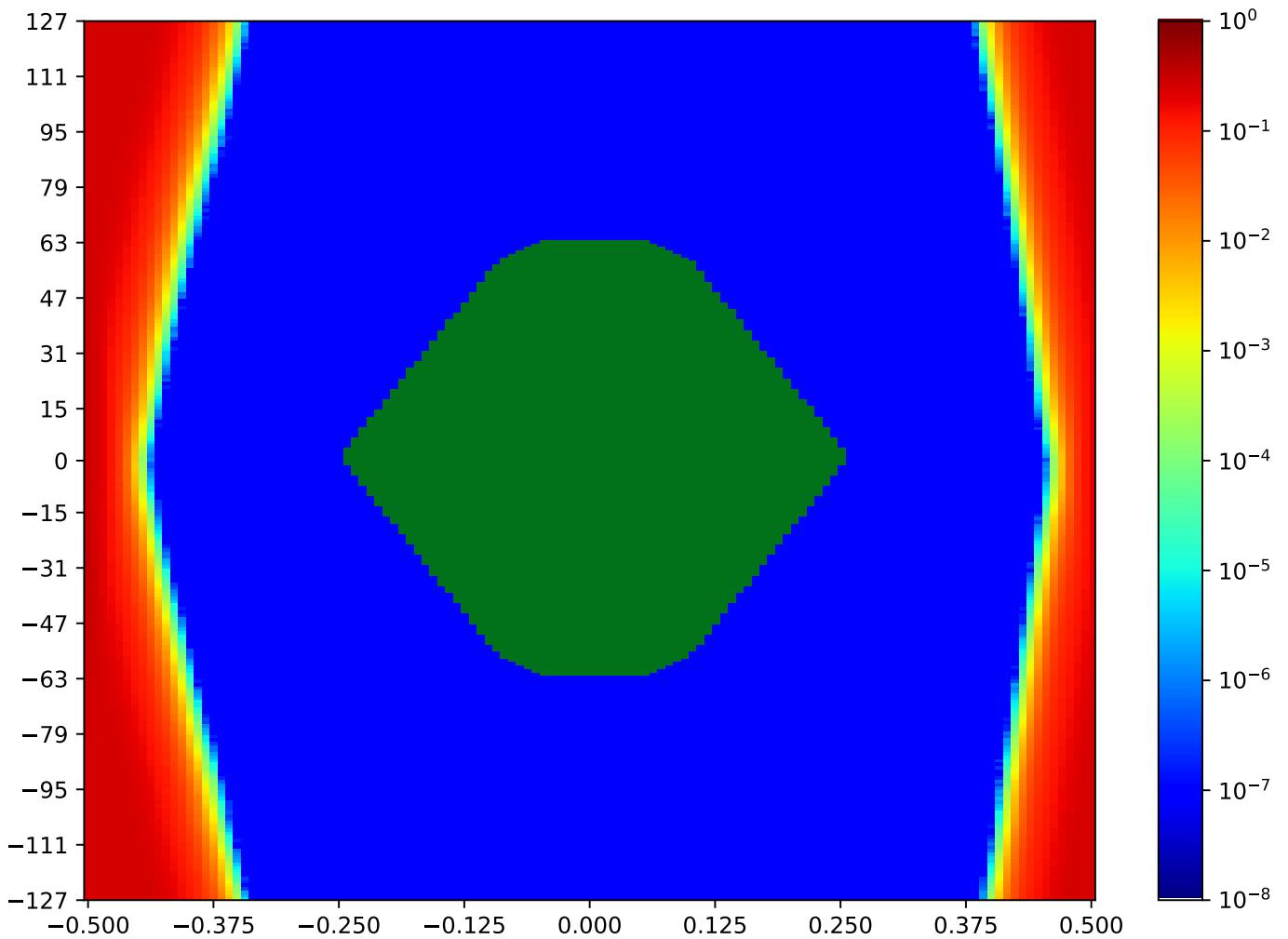


Figure 2.90: MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.22 MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

Table 2.83: MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:31:39		2018-Jan-24 04:32:49	
Reset RX	OA	HO		HO (%)	
true	24021	111		86.05%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

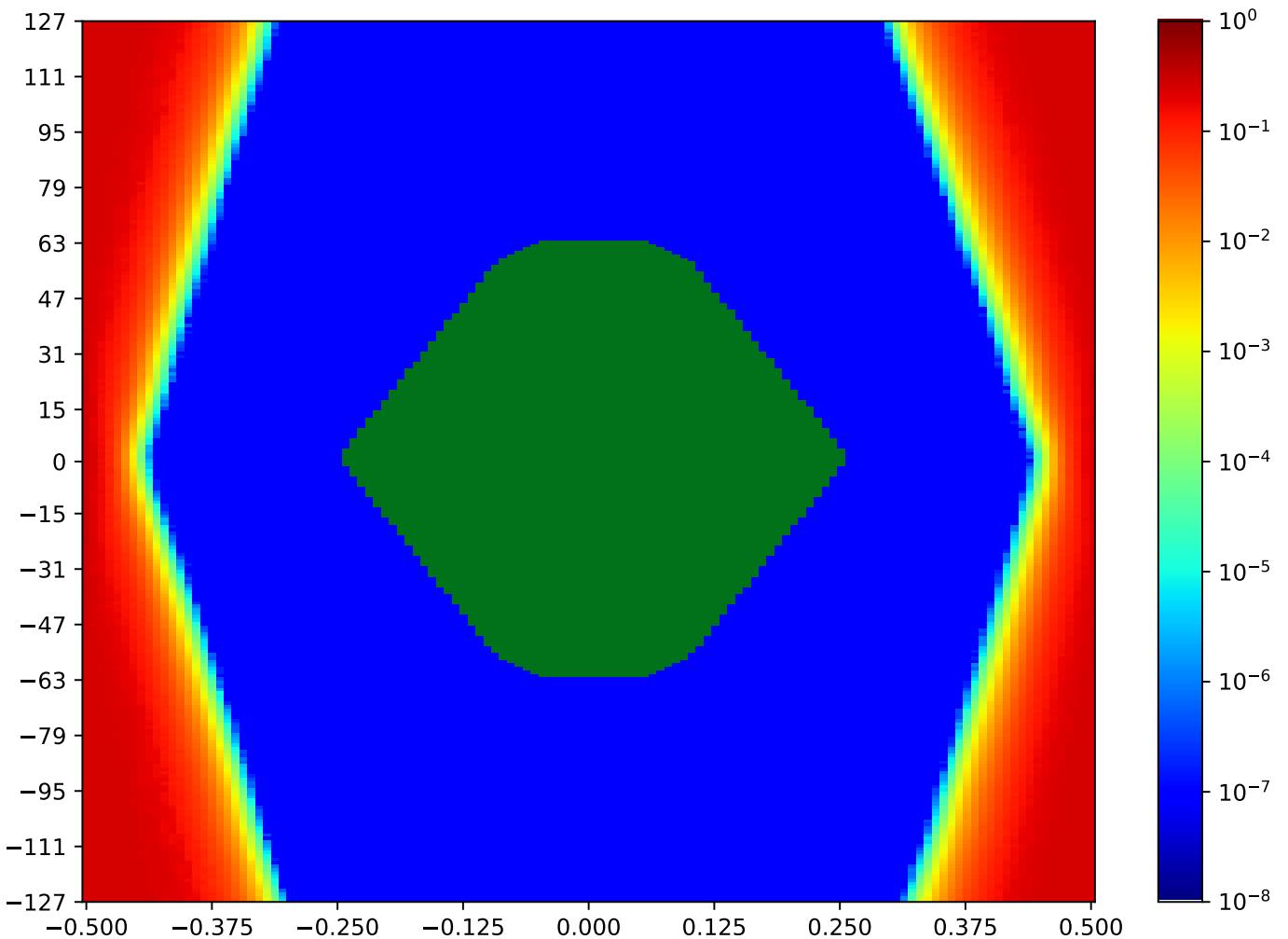


Figure 2.91: MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.23 MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

Table 2.84: MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:32:50		2018-Jan-24 04:34:02	
Reset RX	OA	HO		HO (%)	
true	27017	114		88.37%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

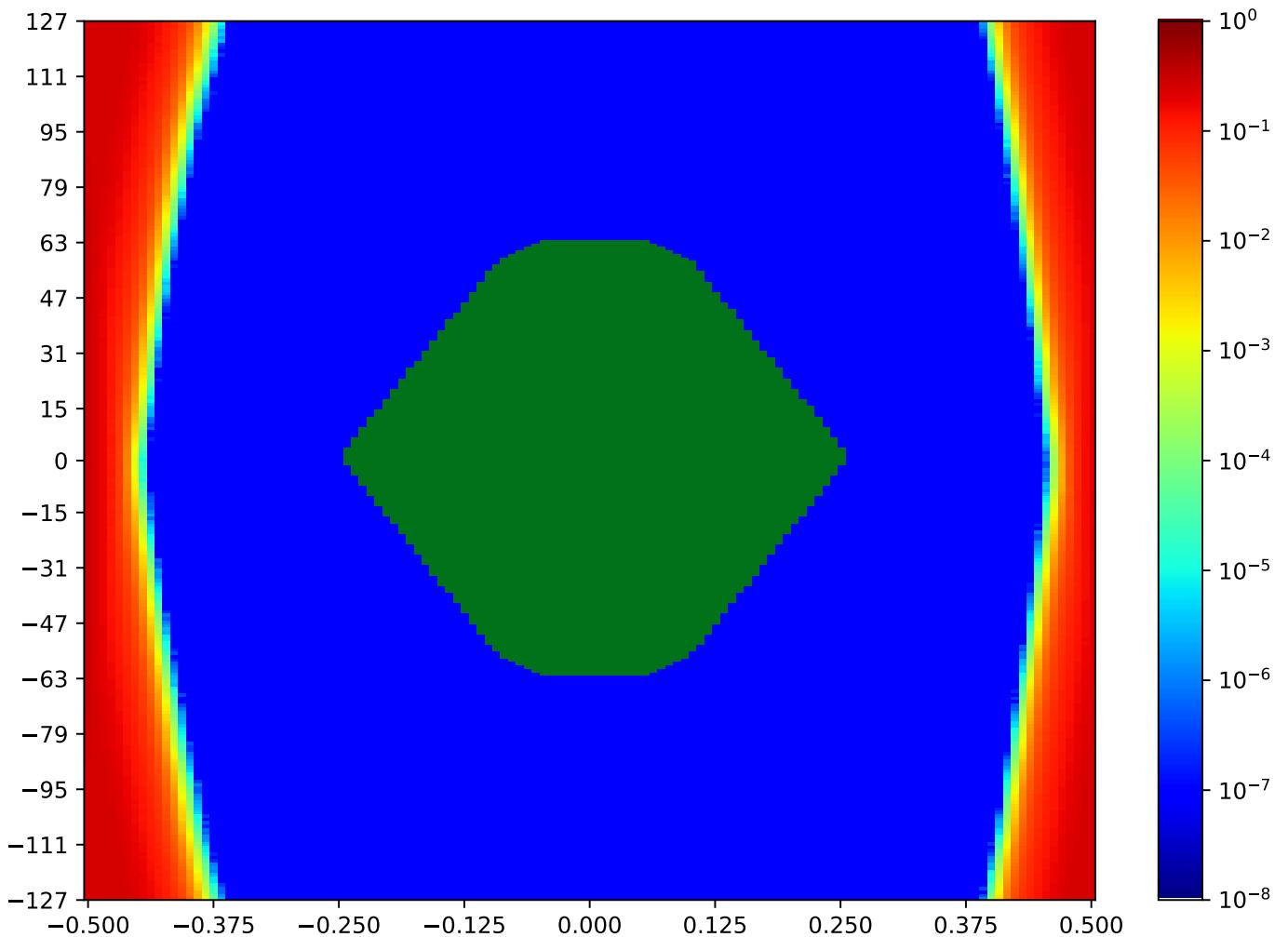


Figure 2.92: MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.24 MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

Table 2.85: MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:34:02		2018-Jan-24 04:35:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26158	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

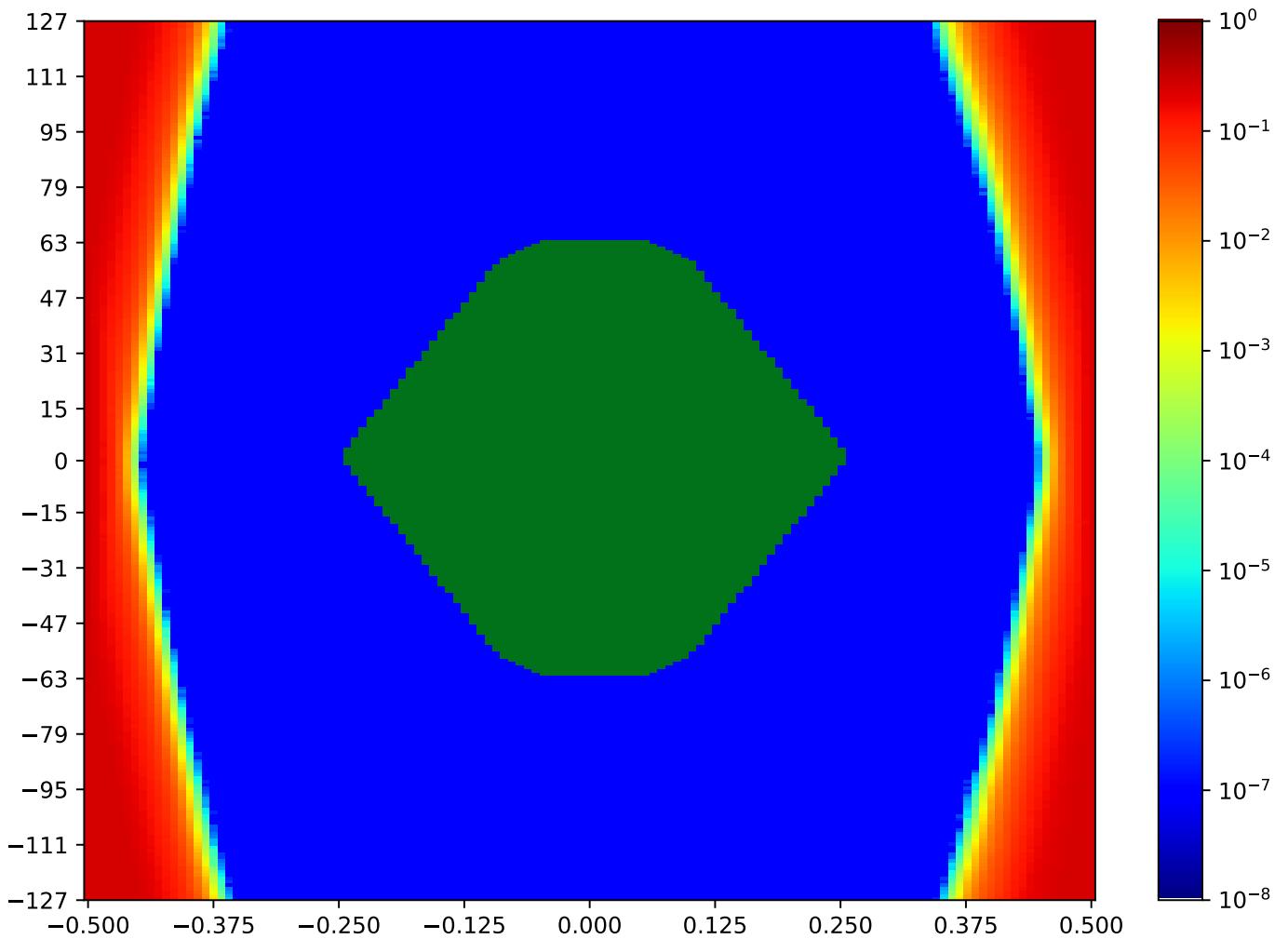


Figure 2.93: MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.25 MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

Table 2.86: MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:35:14		2018-Jan-24 04:36:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25233	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

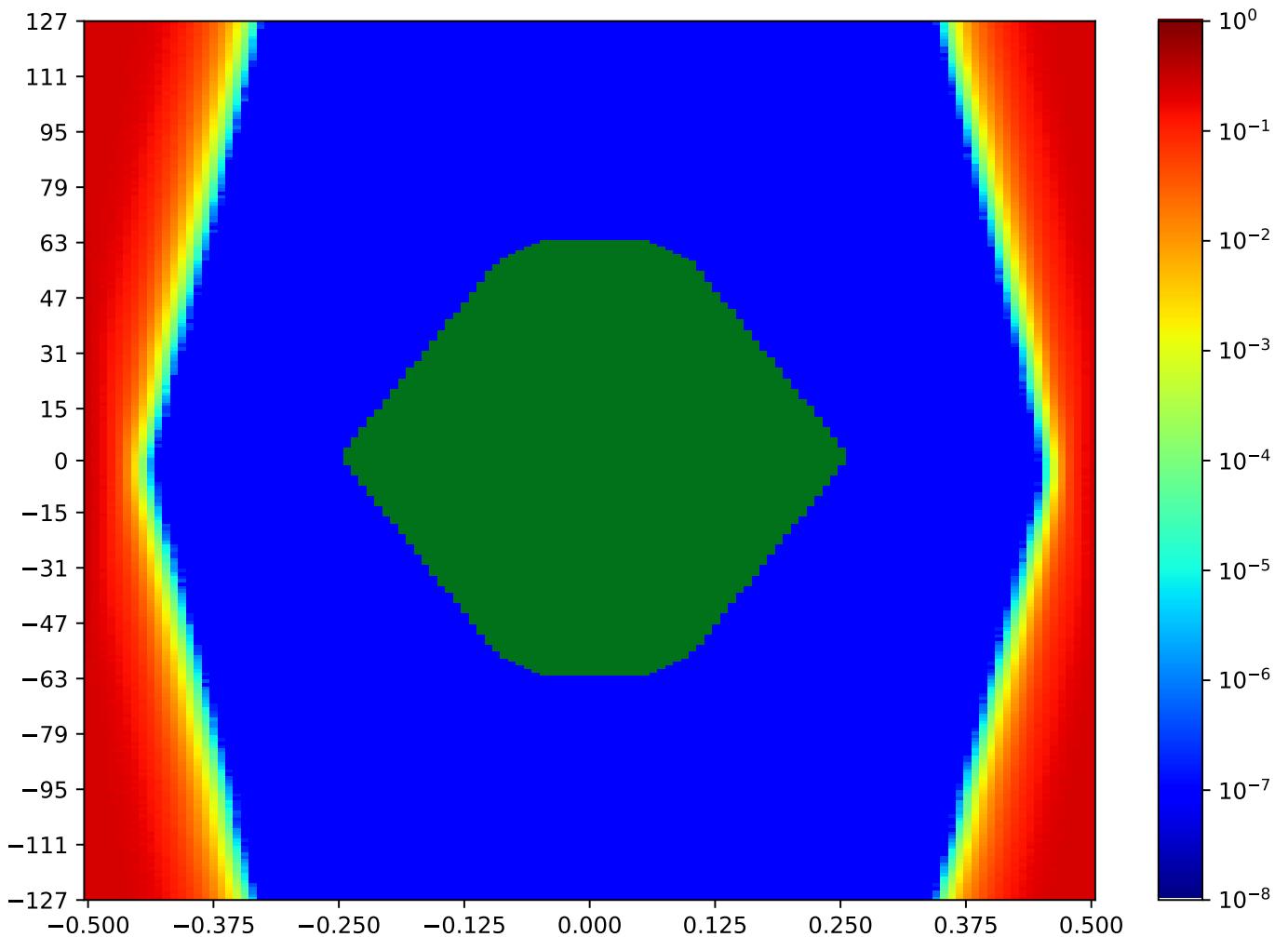


Figure 2.94: MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.26 MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

Table 2.87: MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:36:24		2018-Jan-24 04:37:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26102	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

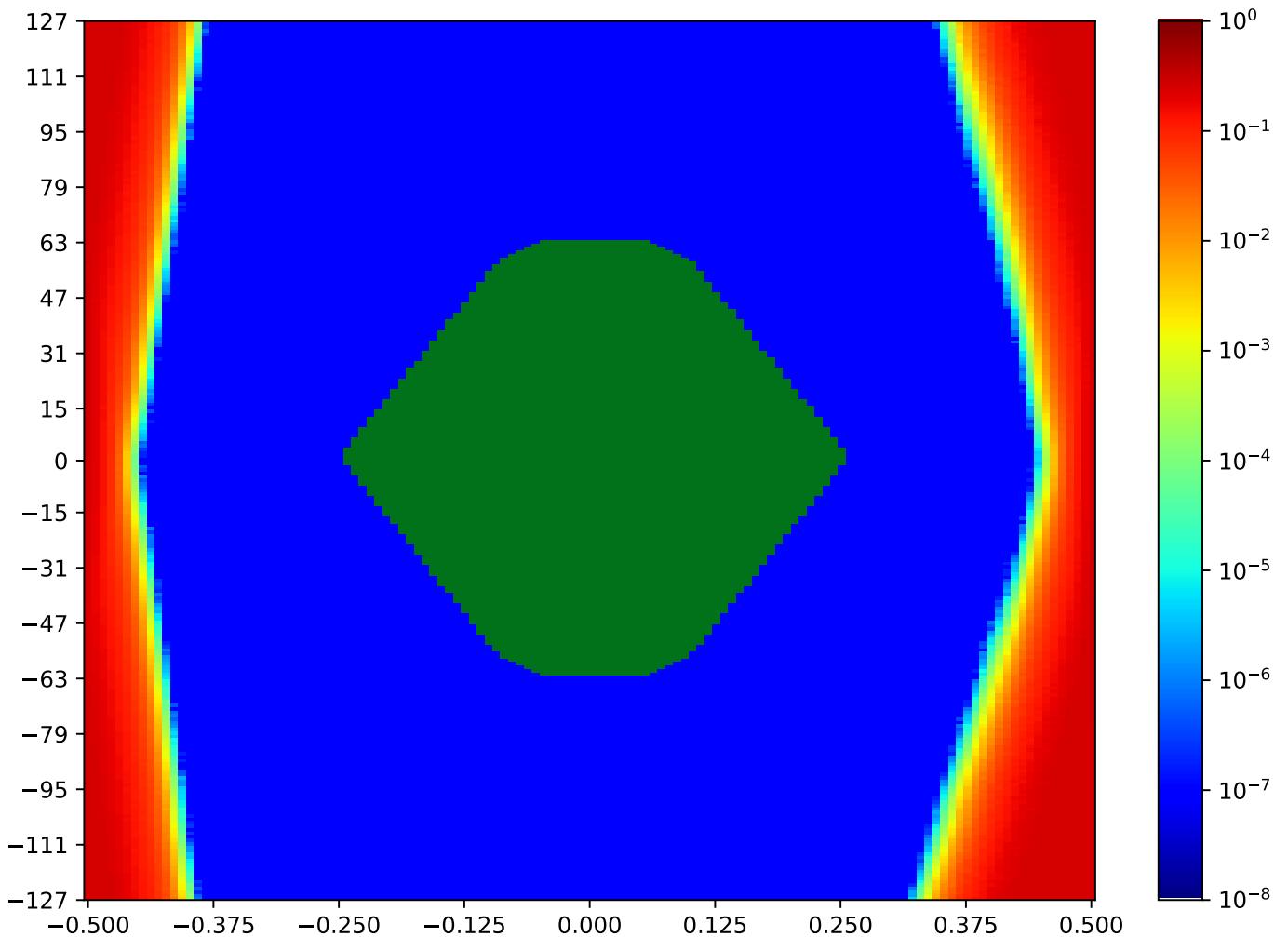


Figure 2.95: MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.27 MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

Table 2.88: MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:37:36		2018-Jan-24 04:38:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25203	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

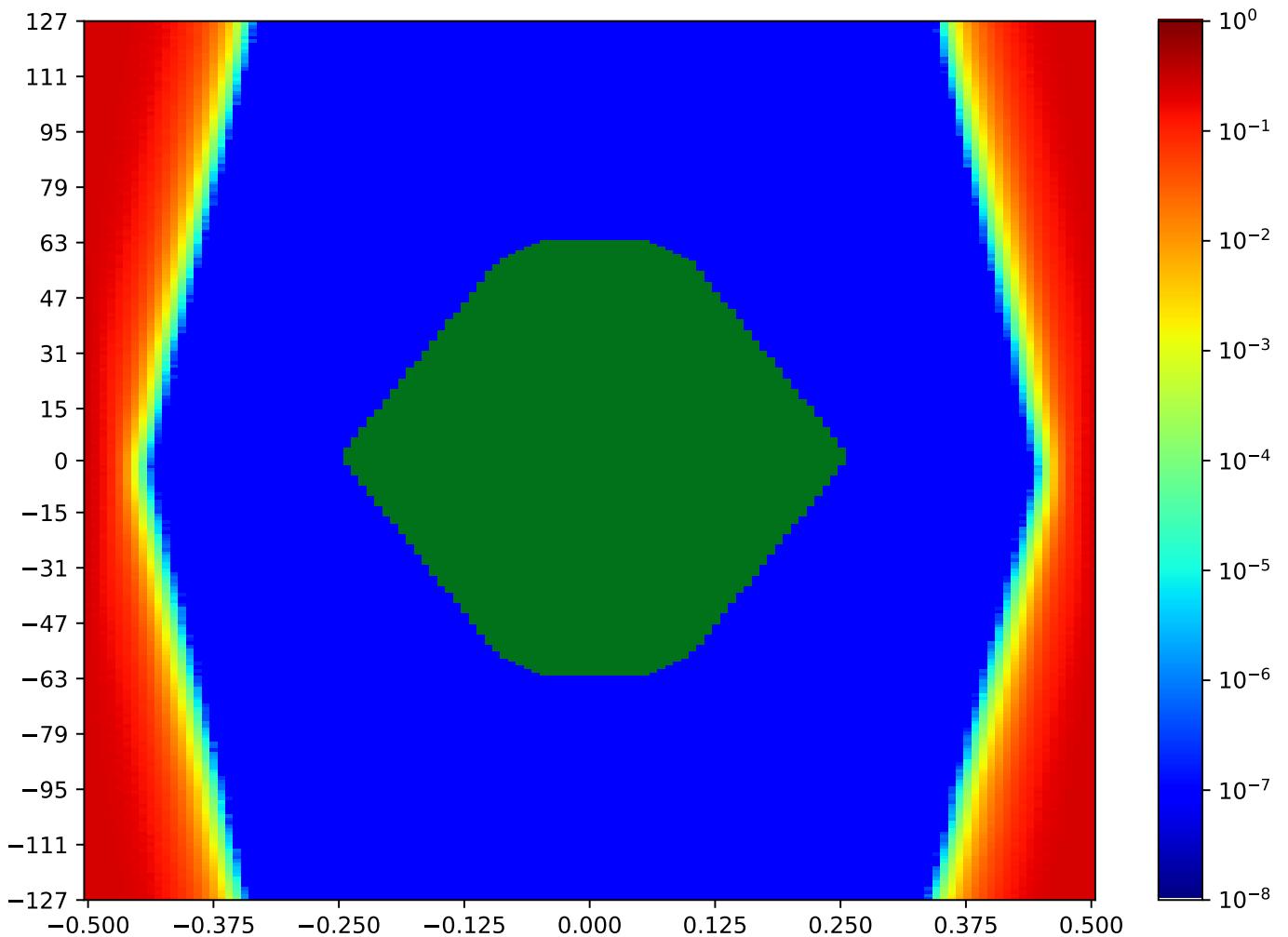


Figure 2.96: MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.8.28 MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

Table 2.89: MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 04:38:47		2018-Jan-24 04:39:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25578	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

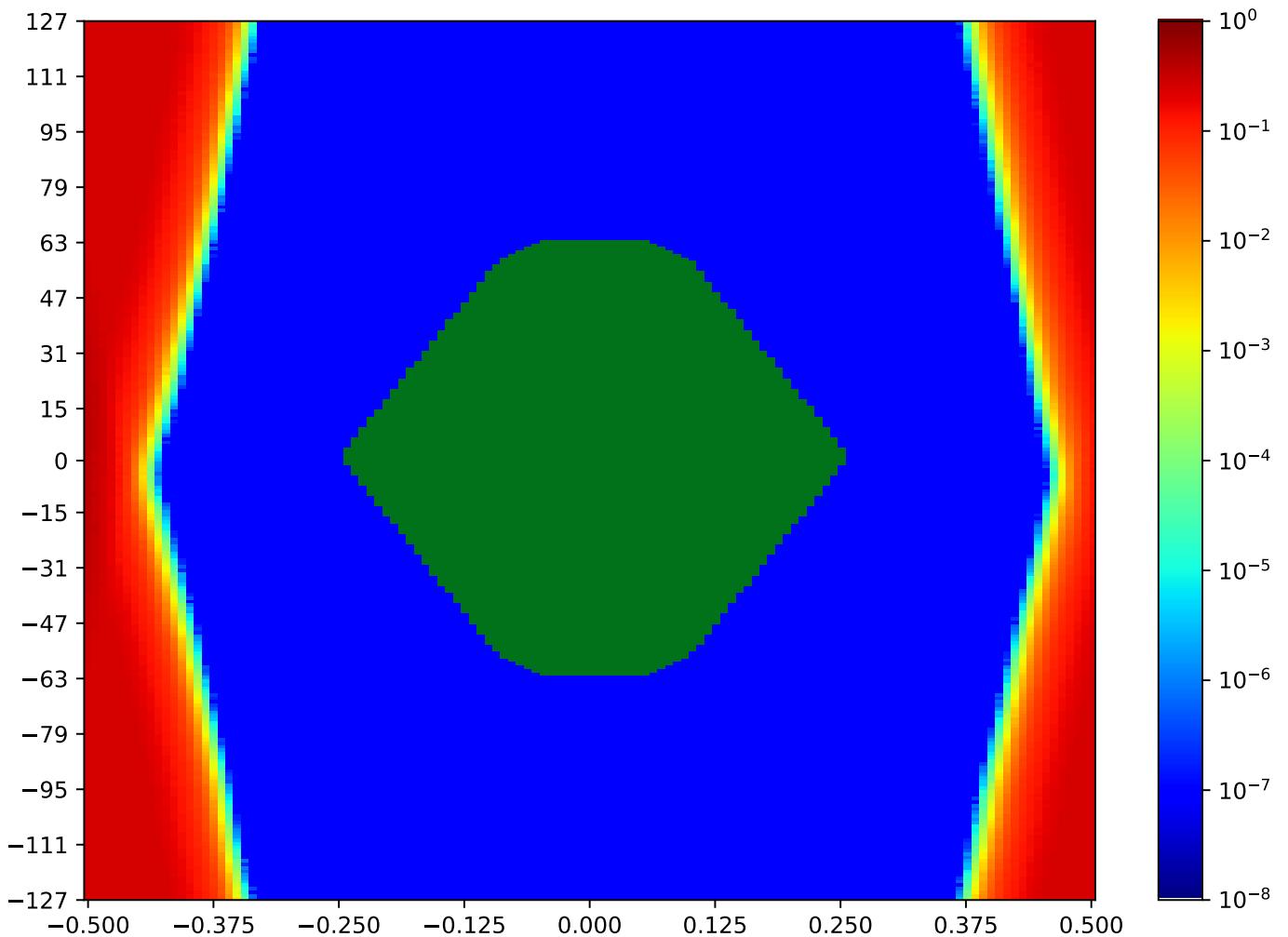


Figure 2.97: MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

Call back to summary Figure 2.69. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9 MSP_C TRP On board links

A cross-reference to Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.
Next summary Figure ??.

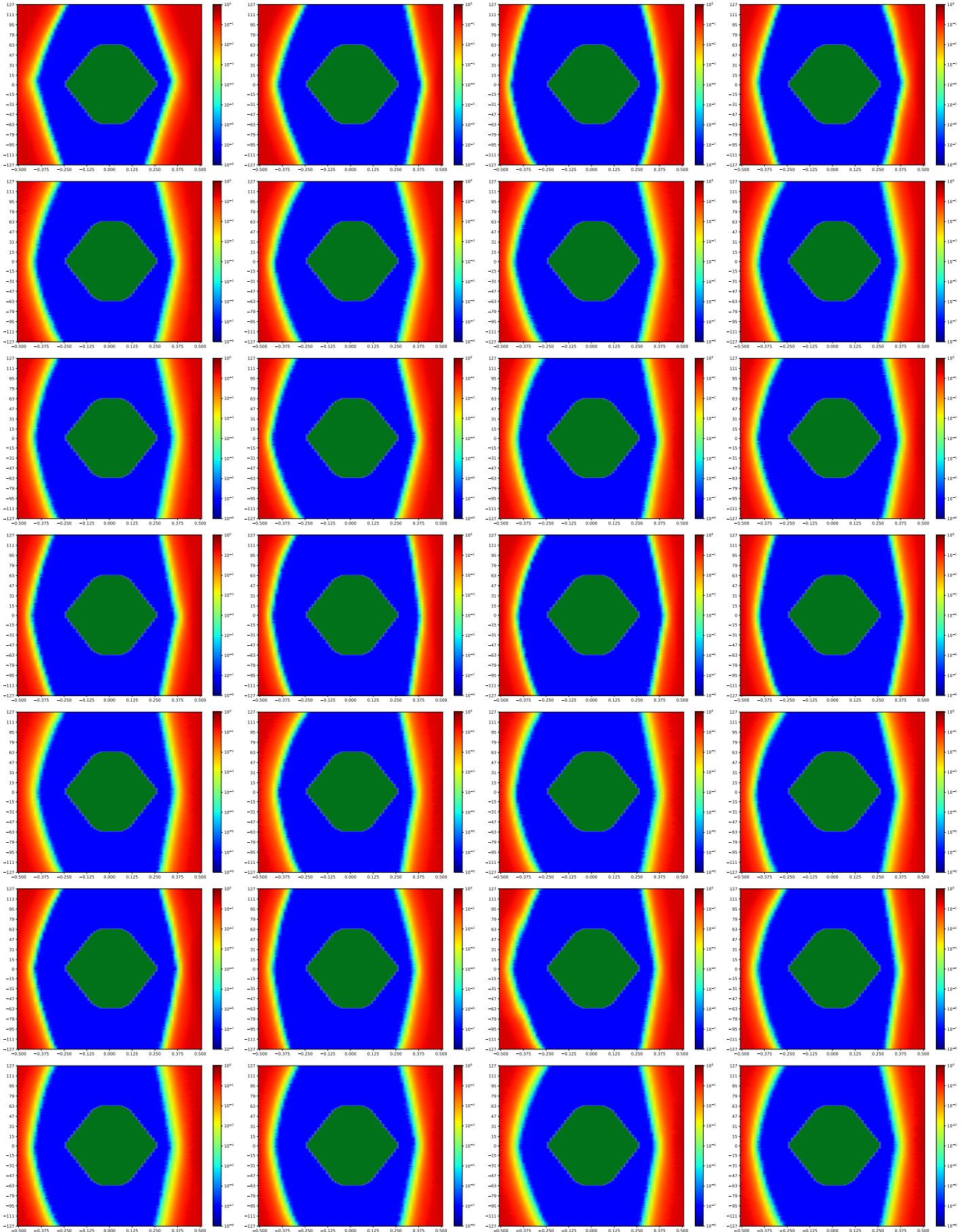


Figure 2.98: MSP_C TRP On board links

2.9.1 MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

Table 2.90: MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:39:58		2018-Jan-24 04:40:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9329	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

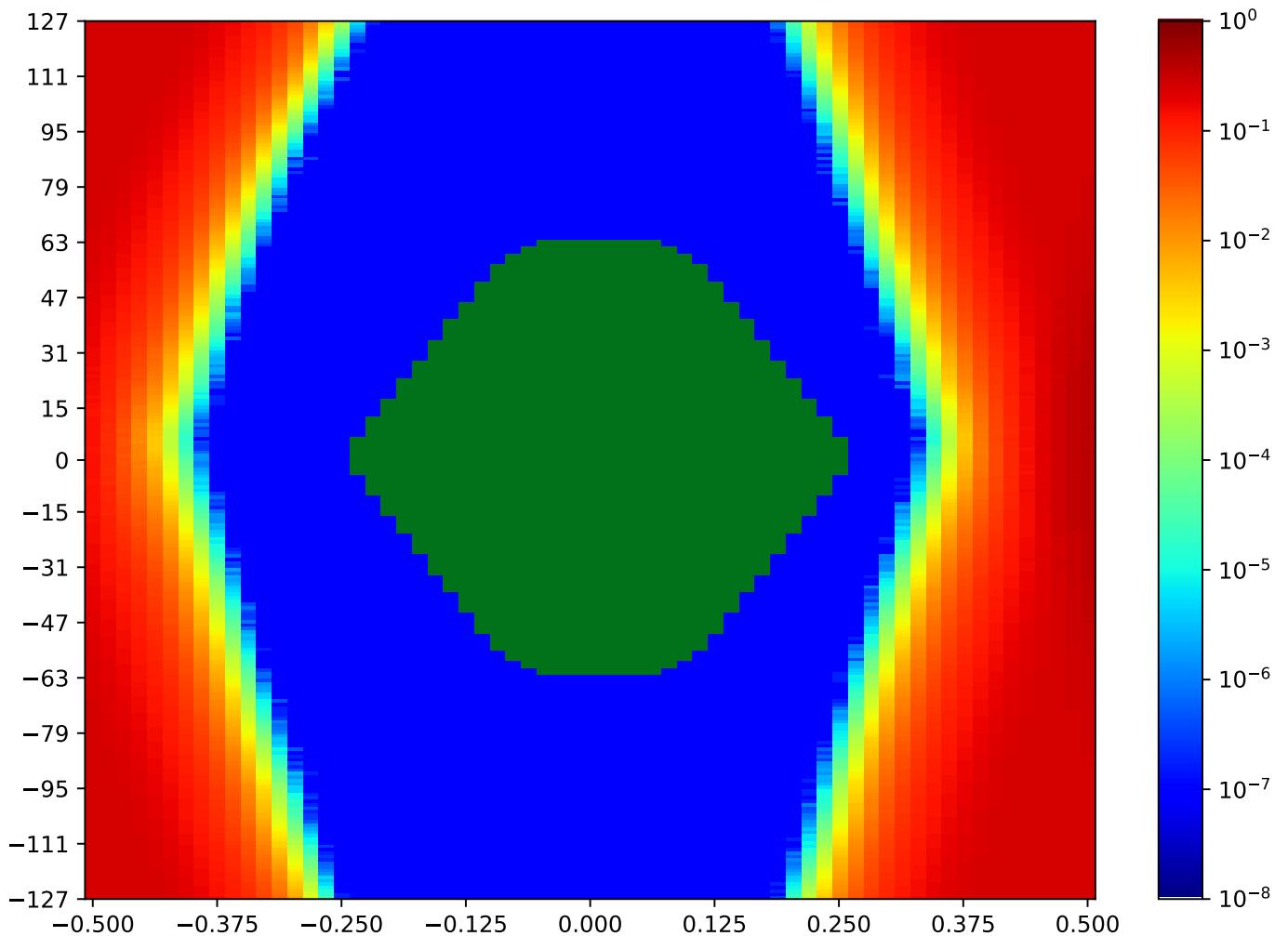


Figure 2.99: MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.2 MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

Table 2.91: MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:40:32		2018-Jan-24 04:41:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10647	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

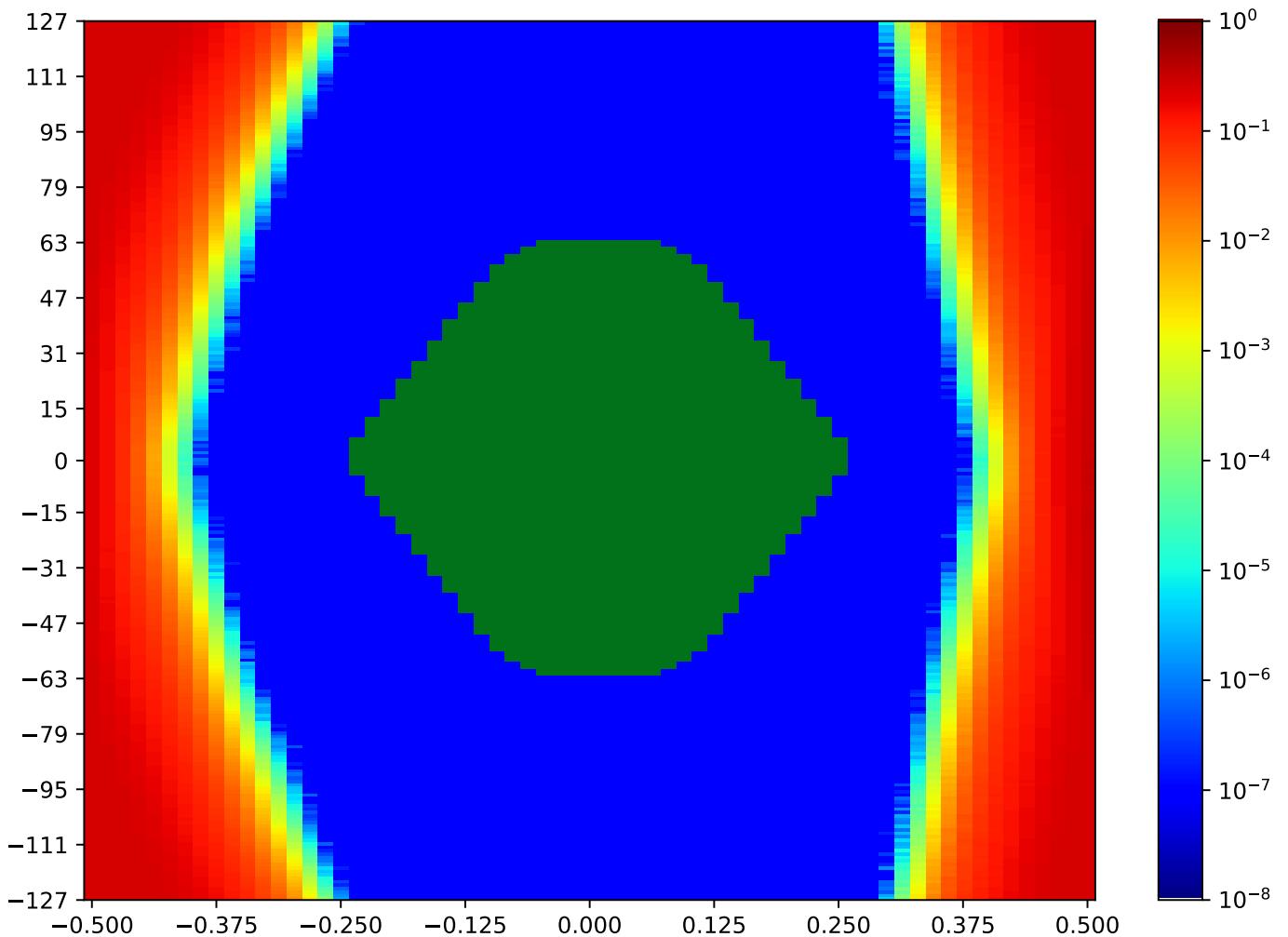


Figure 2.100: MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.3 MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

Table 2.92: MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:41:09		2018-Jan-24 04:41:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11284	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

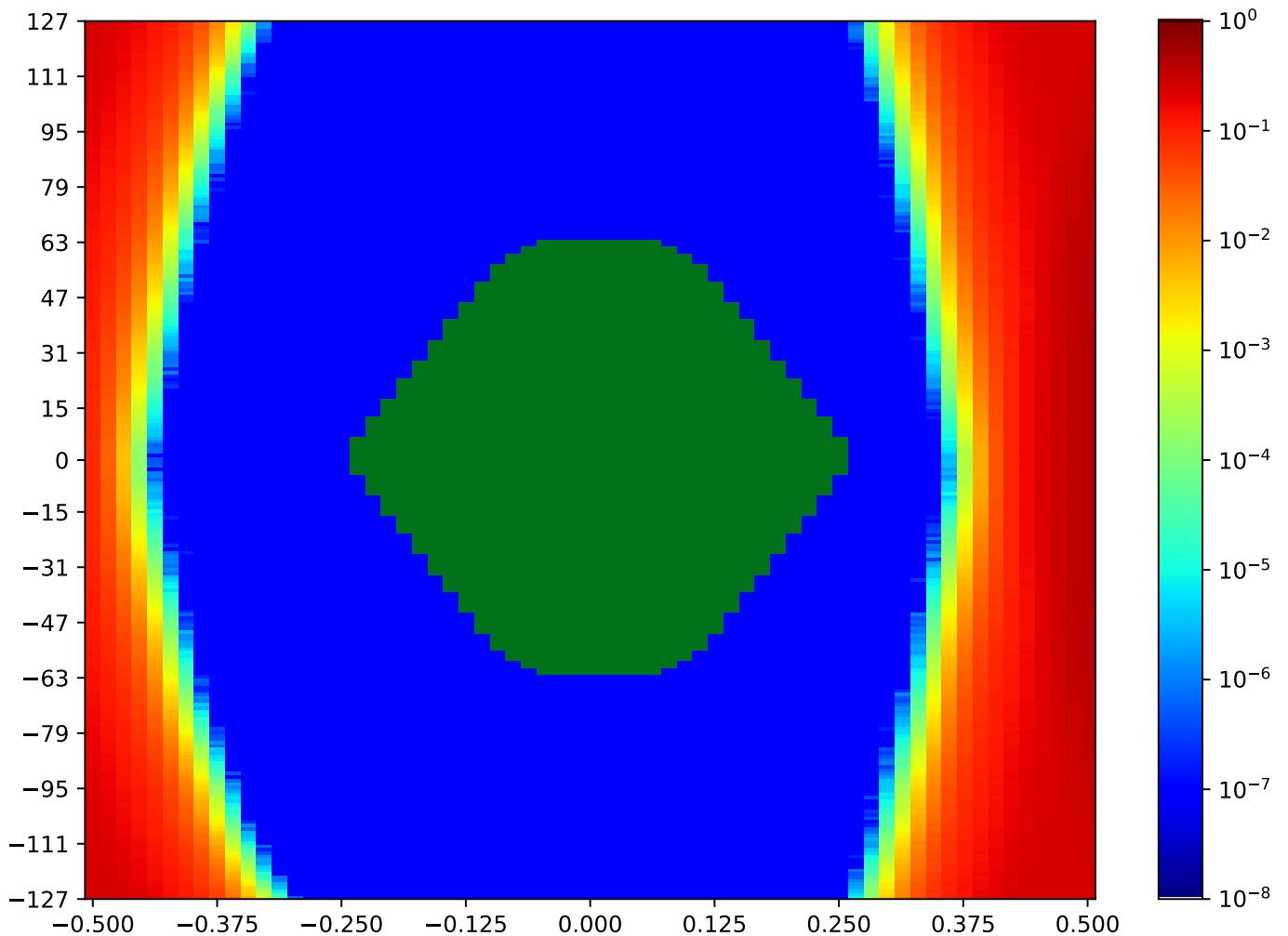


Figure 2.101: MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.4 MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

Table 2.93: MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:41:45		2018-Jan-24 04:42:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10814	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

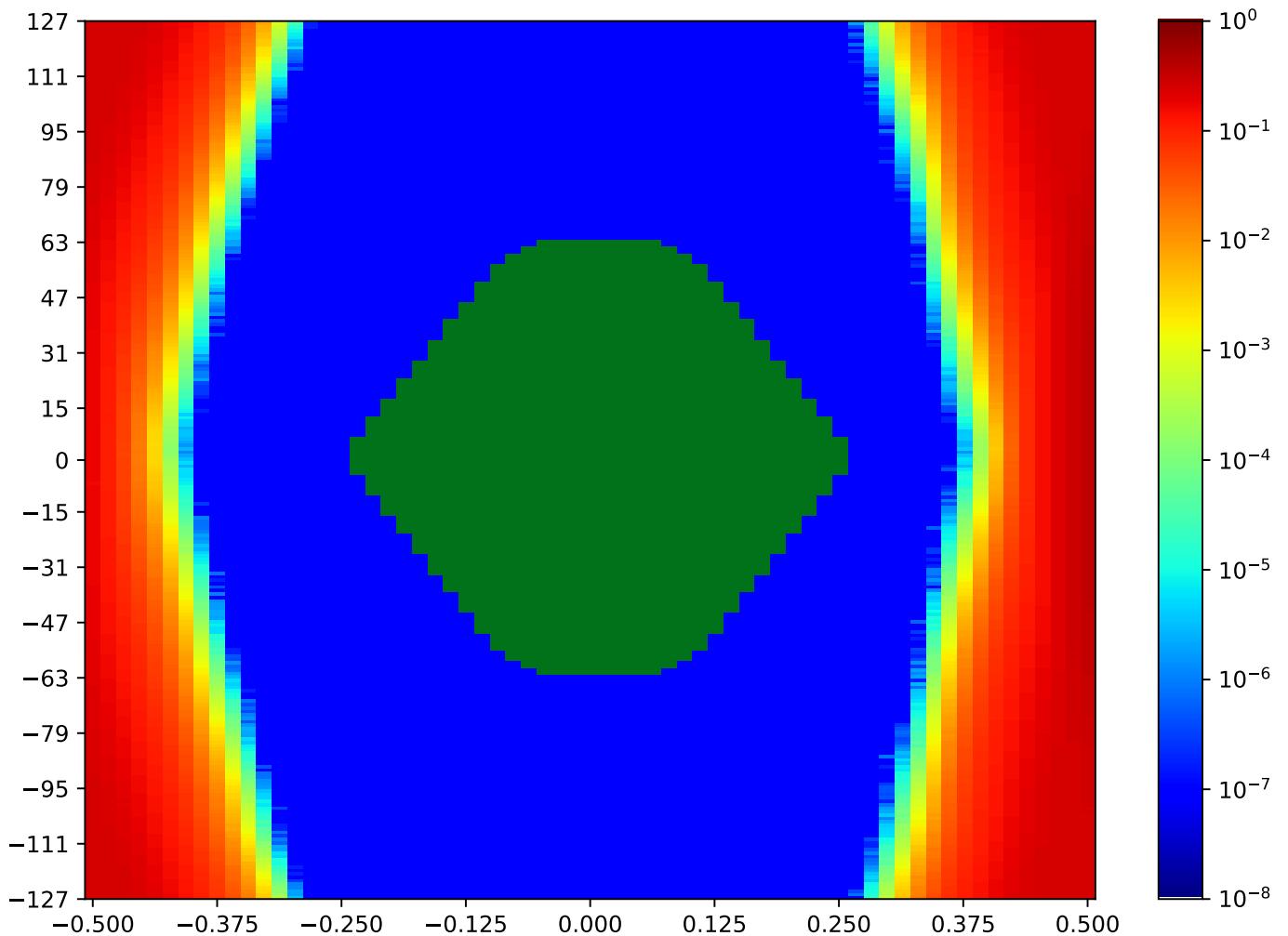


Figure 2.102: MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.5 MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

Table 2.94: MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:42:22		2018-Jan-24 04:42:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10218	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

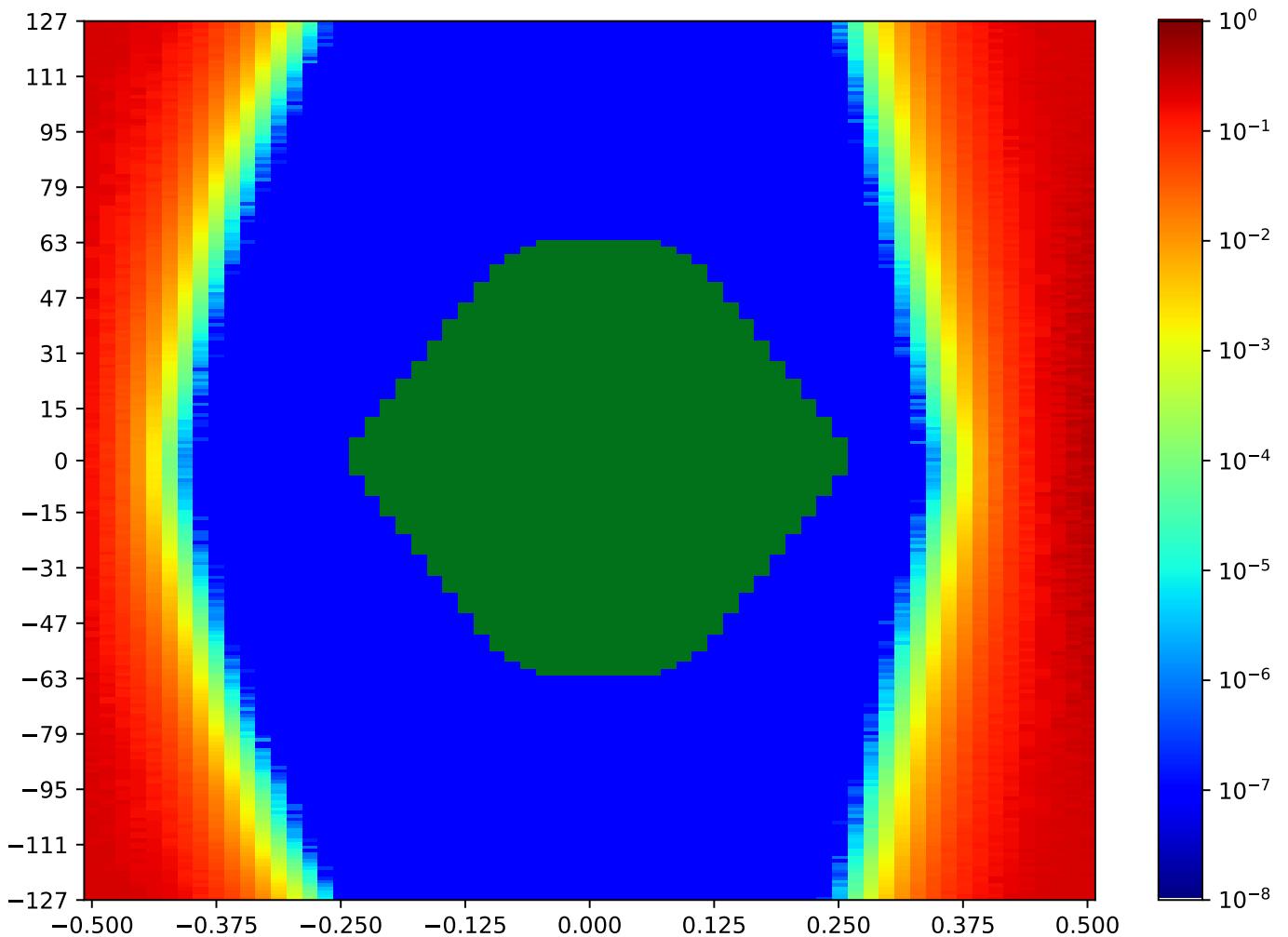


Figure 2.103: MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.6 MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

Table 2.95: MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:42:59		2018-Jan-24 04:43:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10324	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

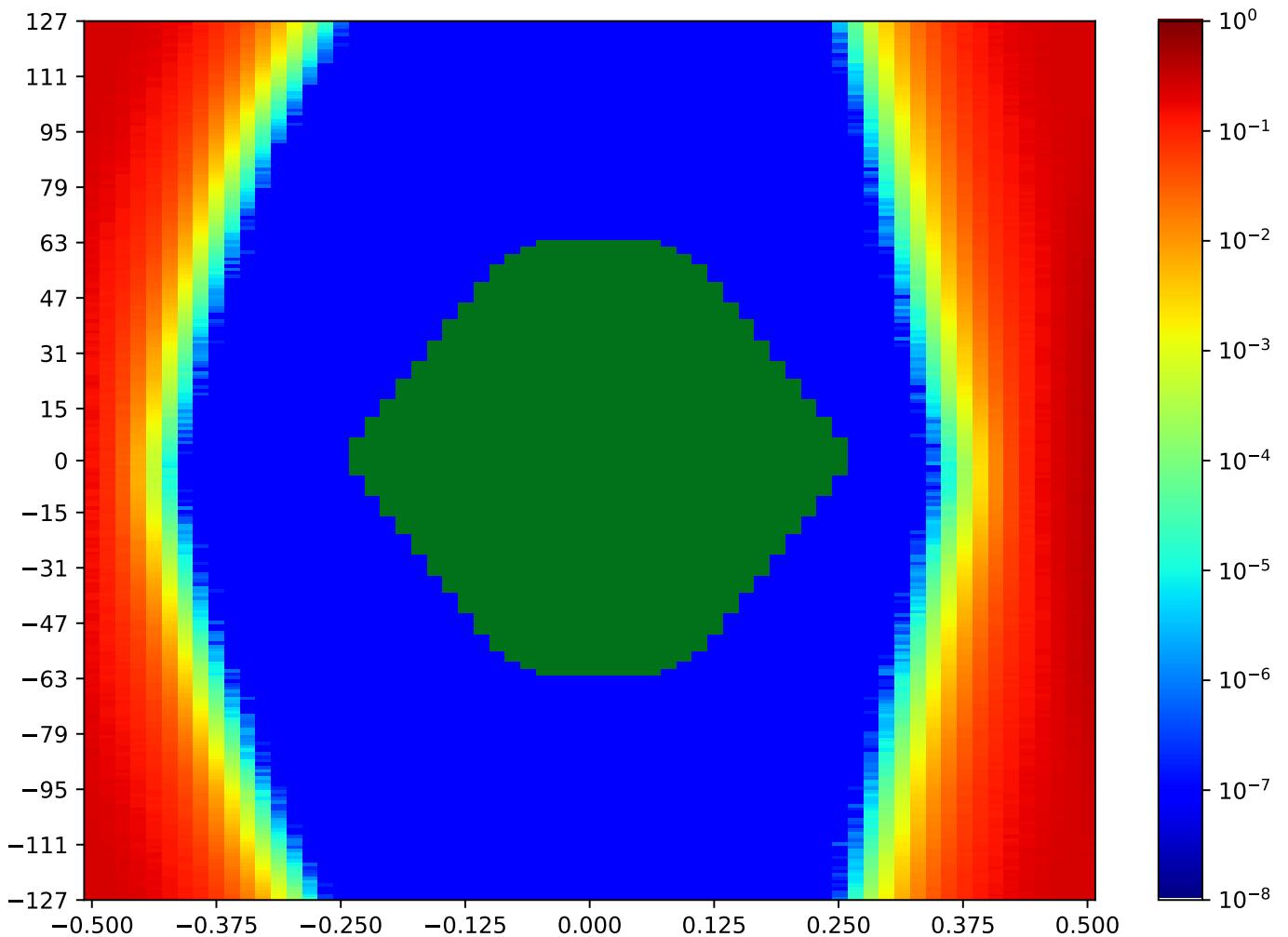


Figure 2.104: MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.7 MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

Table 2.96: MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:43:35		2018-Jan-24 04:44:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10407	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

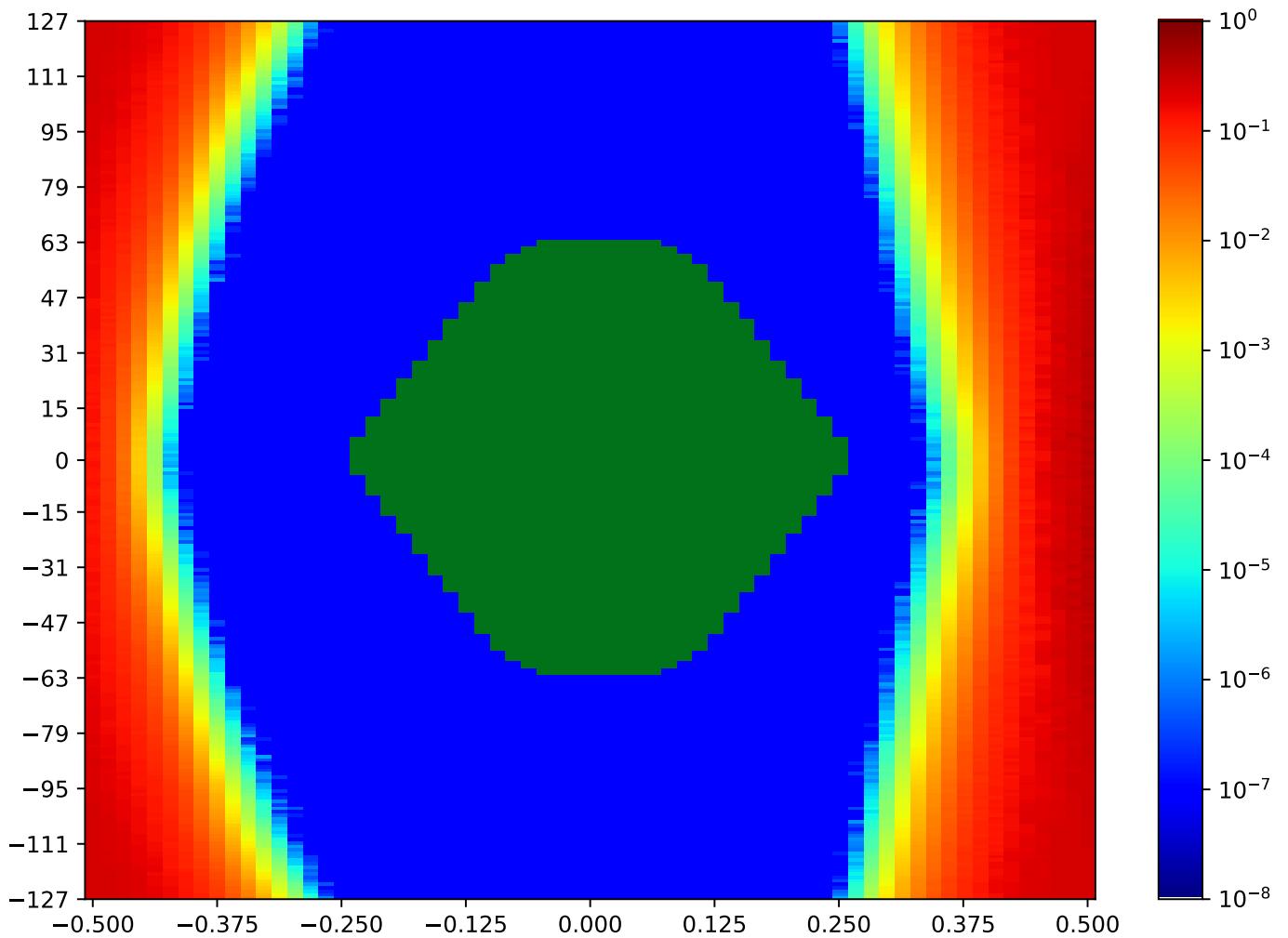


Figure 2.105: MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.8 MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

Table 2.97: MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:44:12		2018-Jan-24 04:44:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10368	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

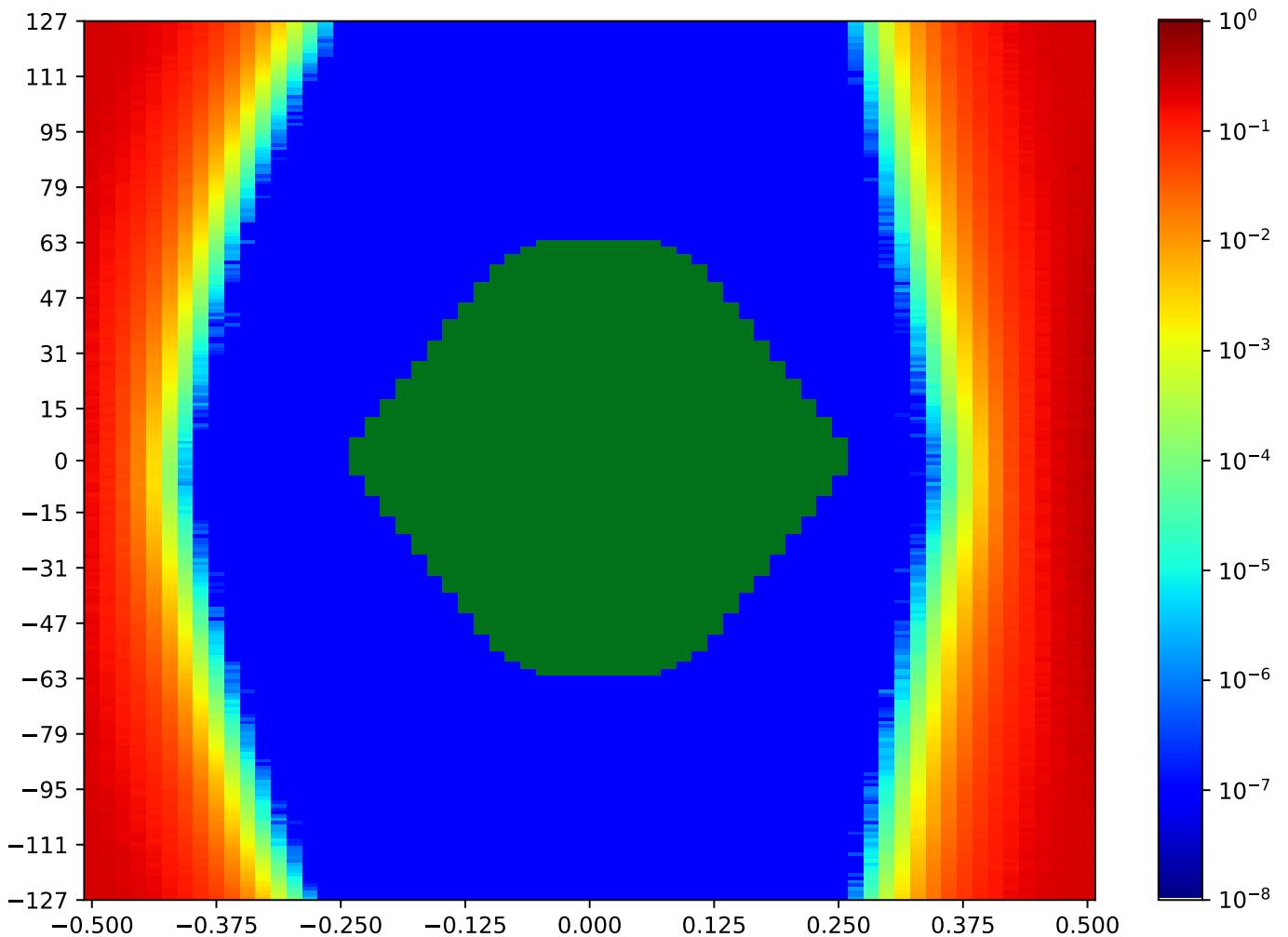


Figure 2.106: MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.9 MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

Table 2.98: MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:44:49		2018-Jan-24 04:45:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10358	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

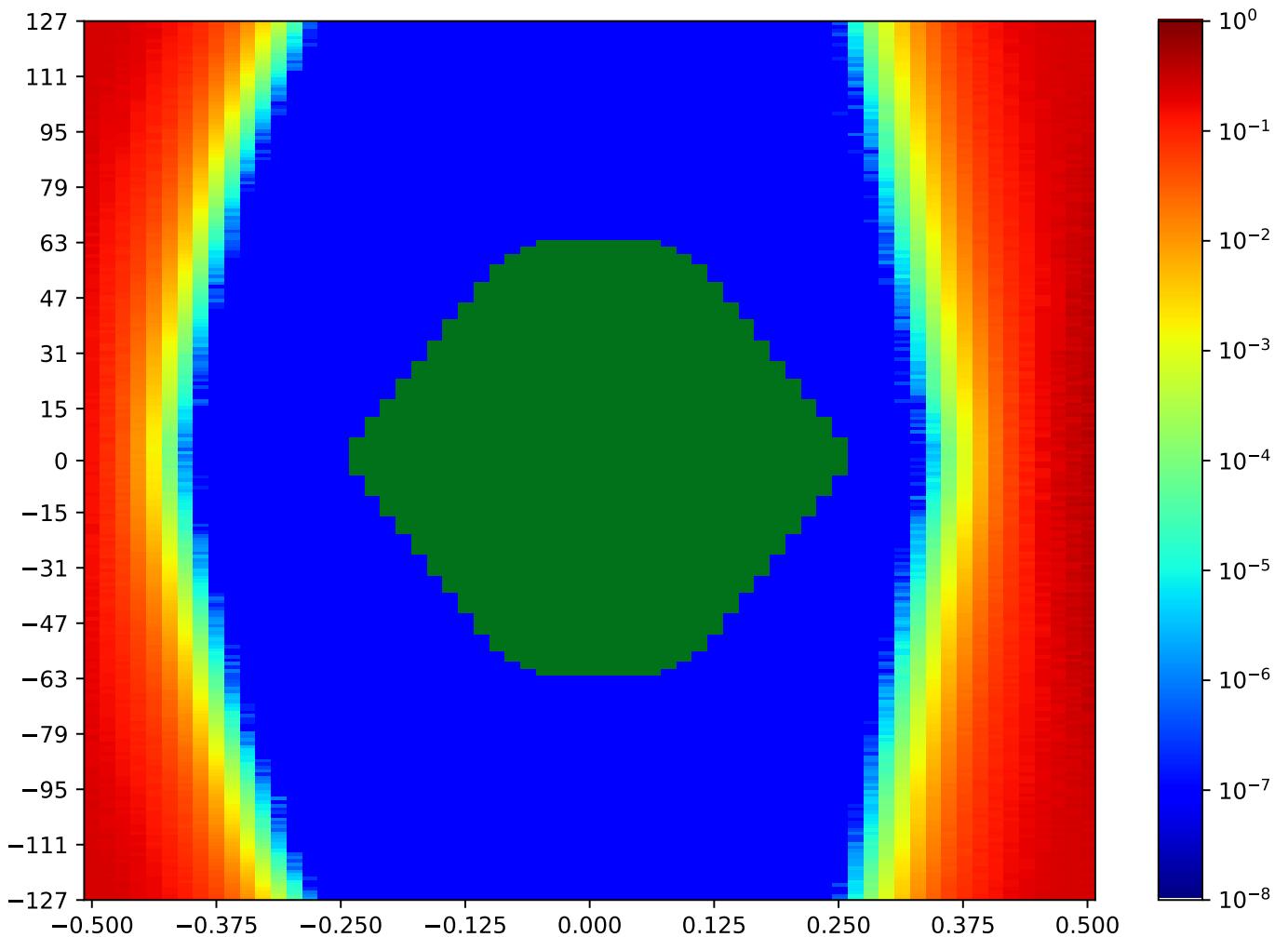


Figure 2.107: MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.10 MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

Table 2.99: MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:45:26		2018-Jan-24 04:46:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10570	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

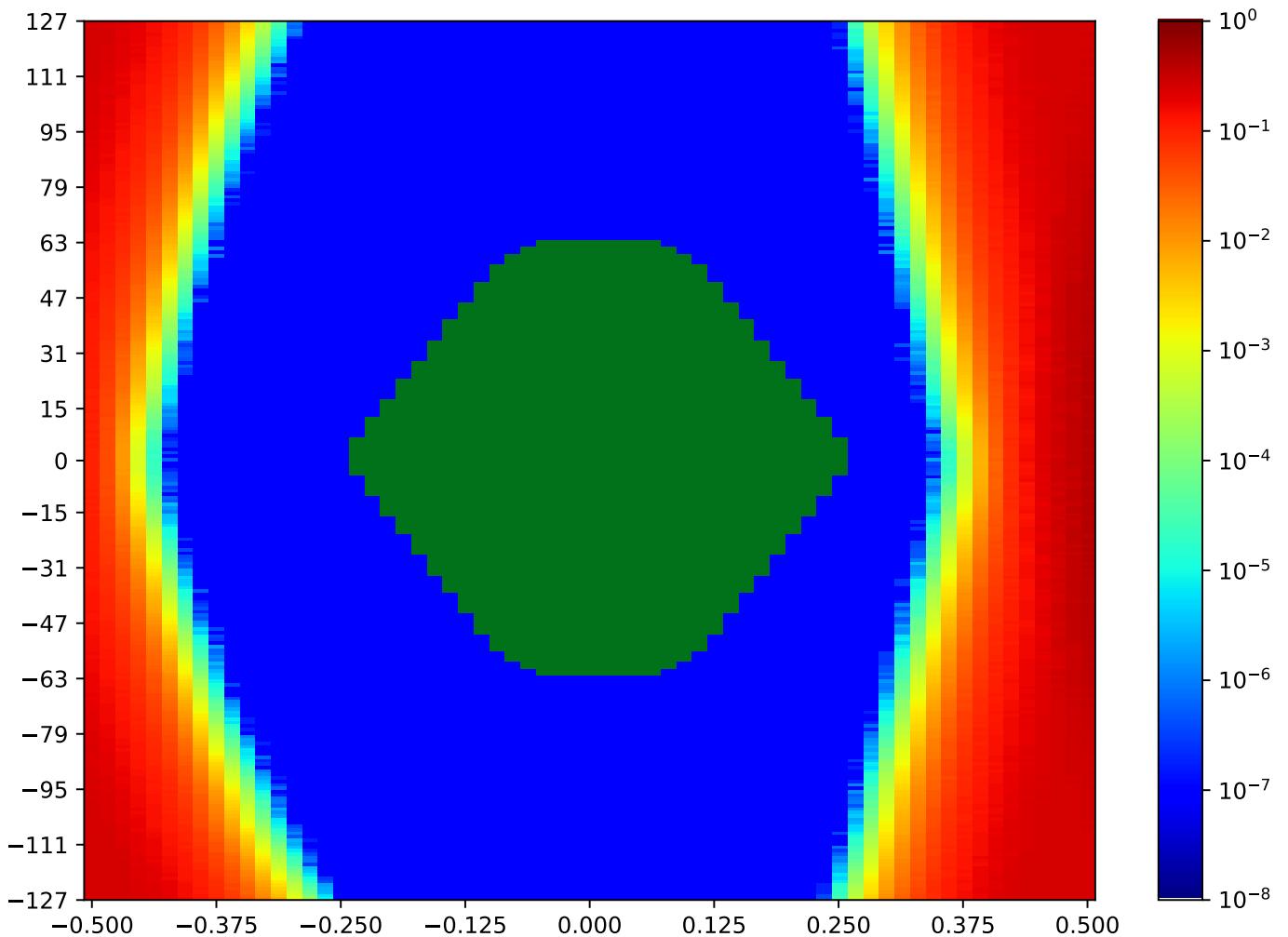


Figure 2.108: MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.11 MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

Table 2.100: MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:46:02		2018-Jan-24 04:46:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10483	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

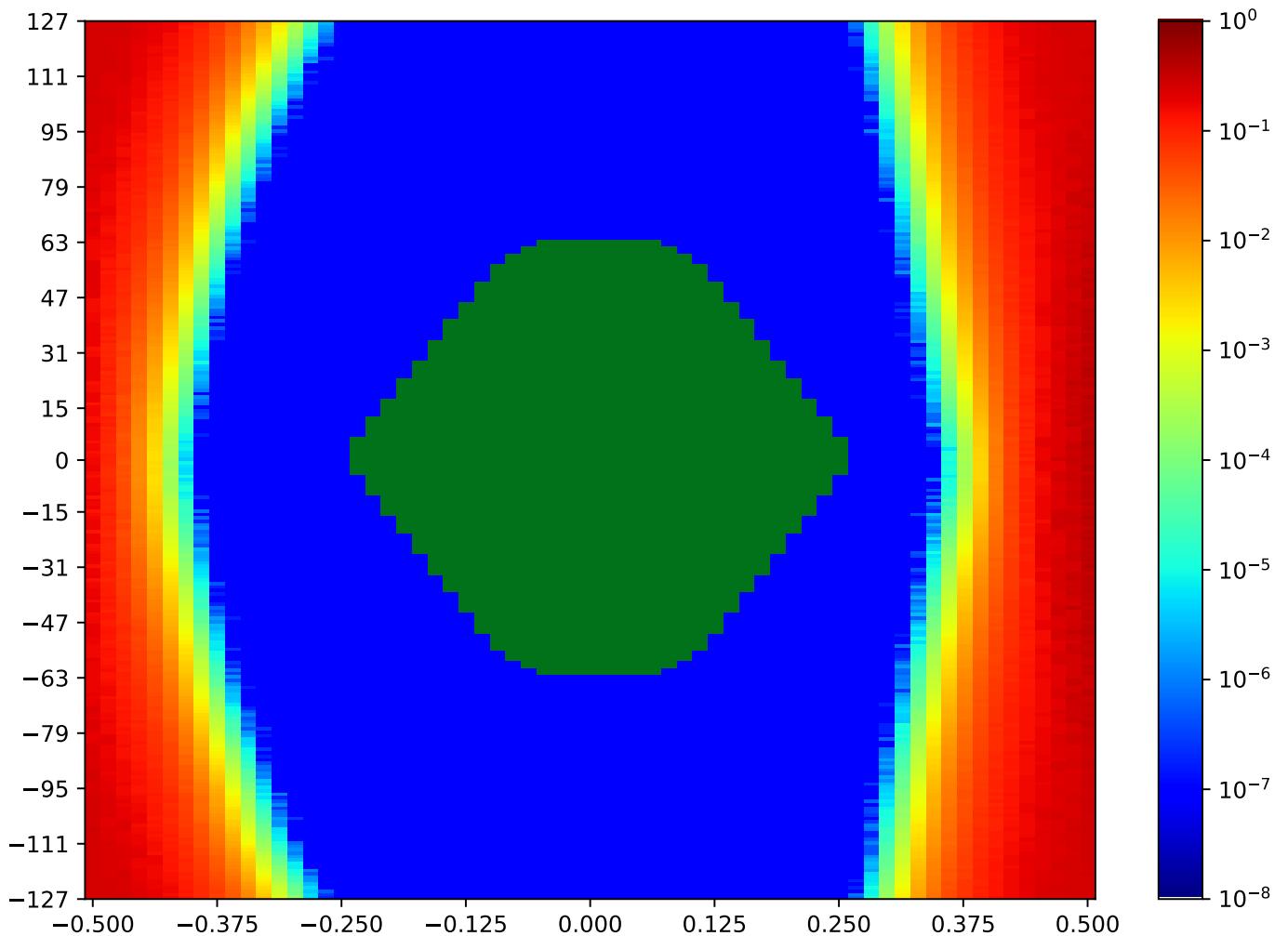


Figure 2.109: MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.12 MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

Table 2.101: MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:46:39		2018-Jan-24 04:47:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10606	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

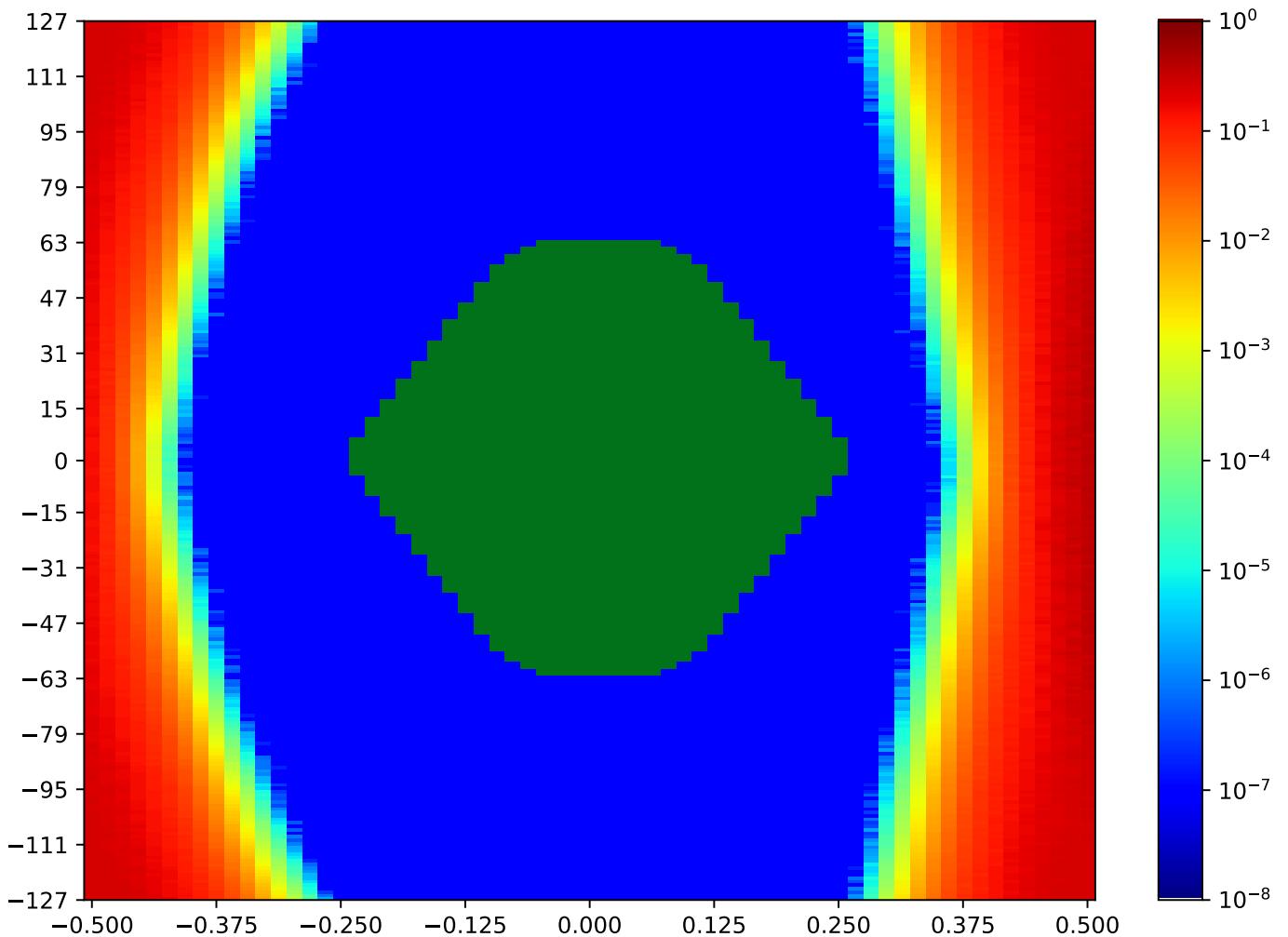


Figure 2.110: MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.13 MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

Table 2.102: MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:47:15		2018-Jan-24 04:47:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10889	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

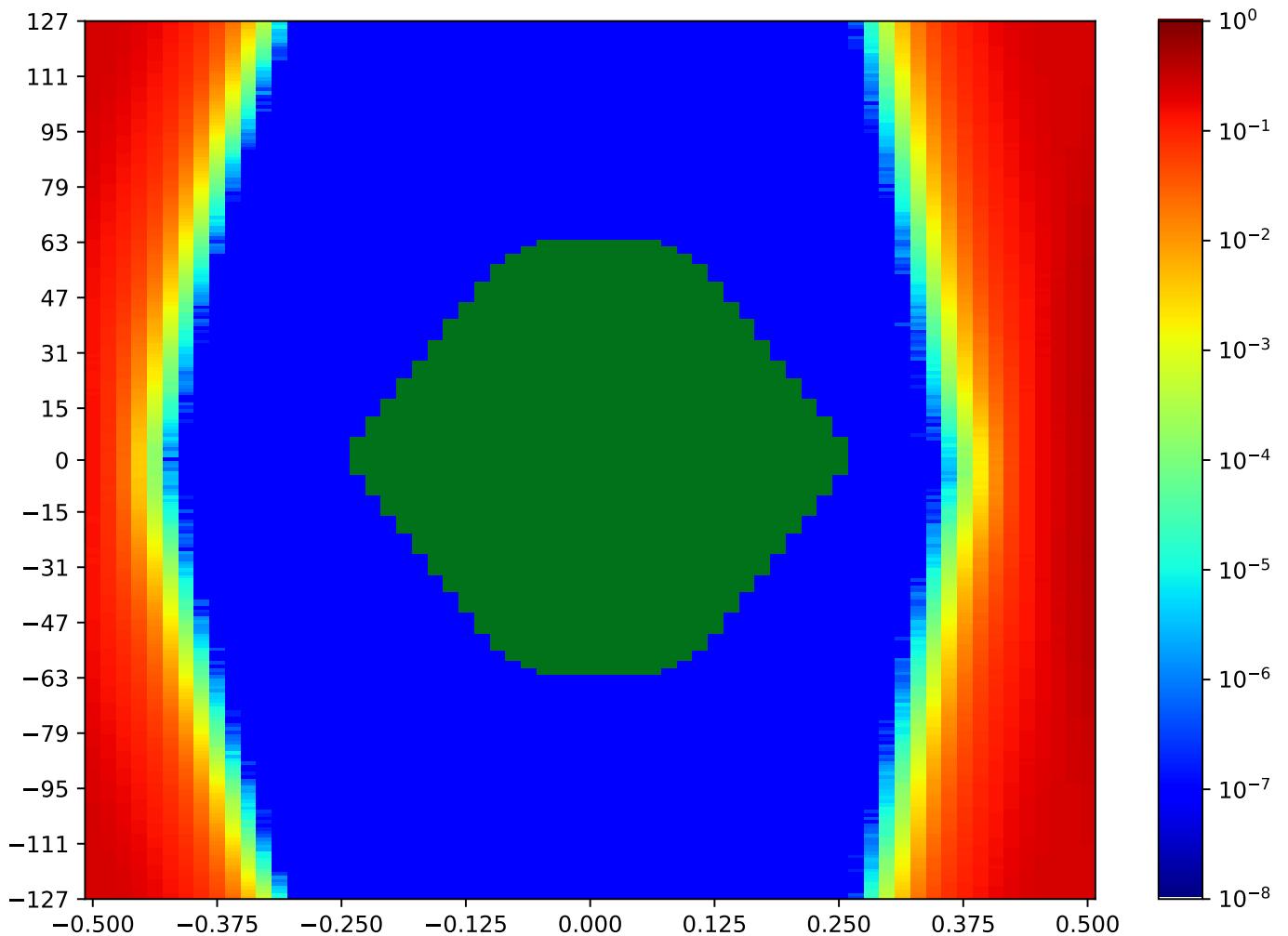


Figure 2.111: MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.14 MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

Table 2.103: MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:47:52		2018-Jan-24 04:48:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11580	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

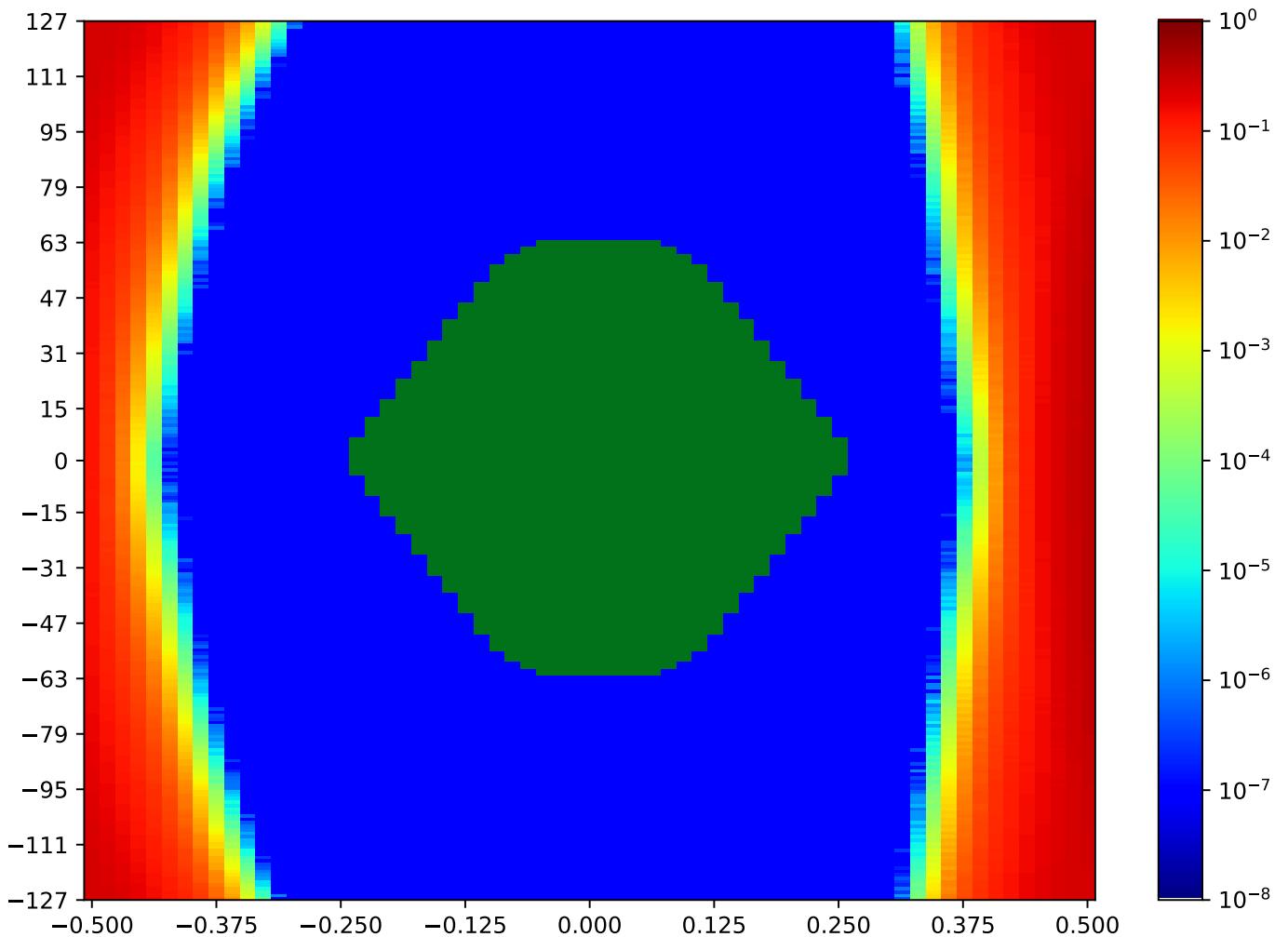


Figure 2.112: MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.15 MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

Table 2.104: MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:48:28		2018-Jan-24 04:49:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11183	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

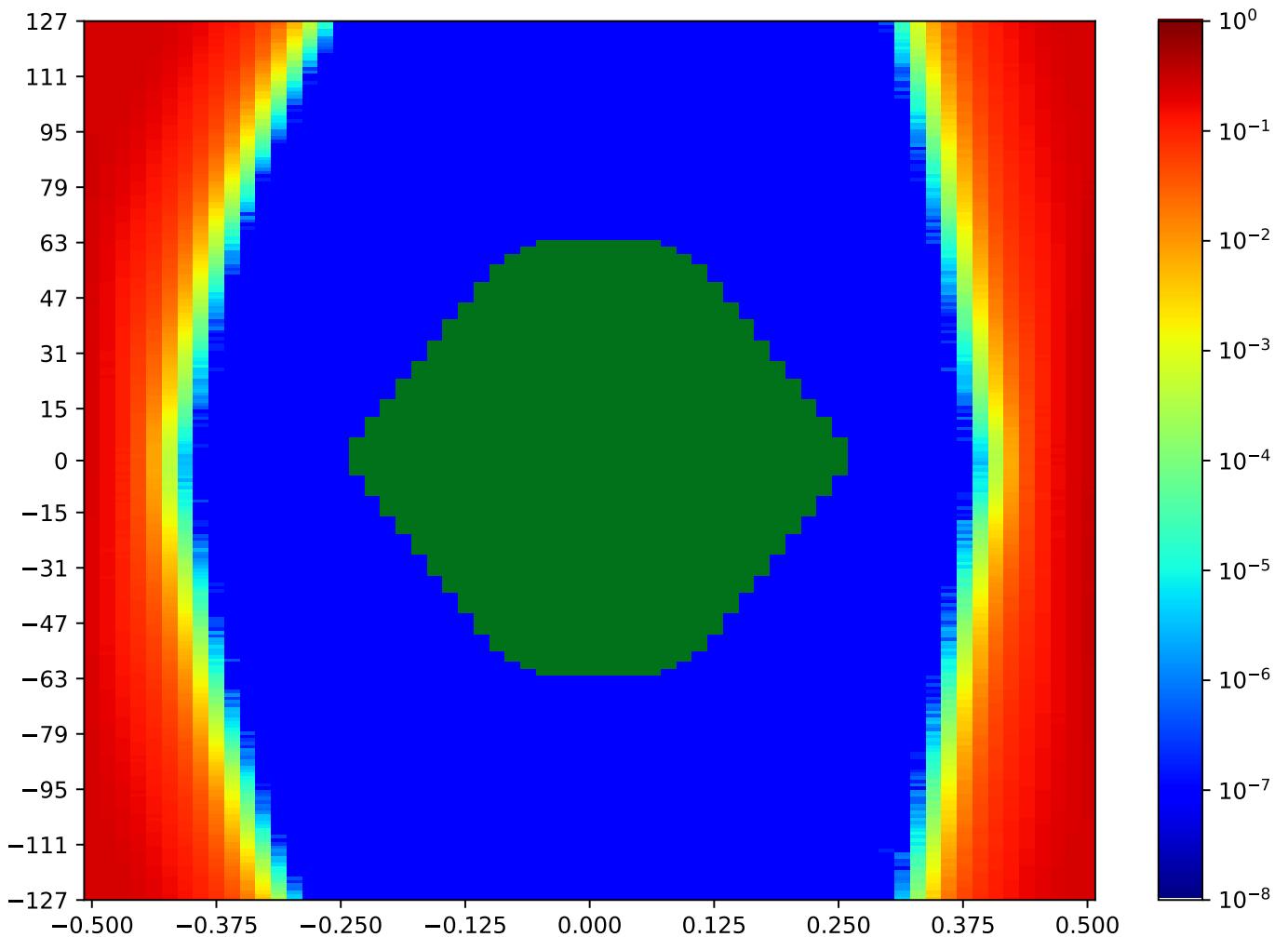


Figure 2.113: MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.16 MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

Table 2.105: MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:49:04		2018-Jan-24 04:49:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11184	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

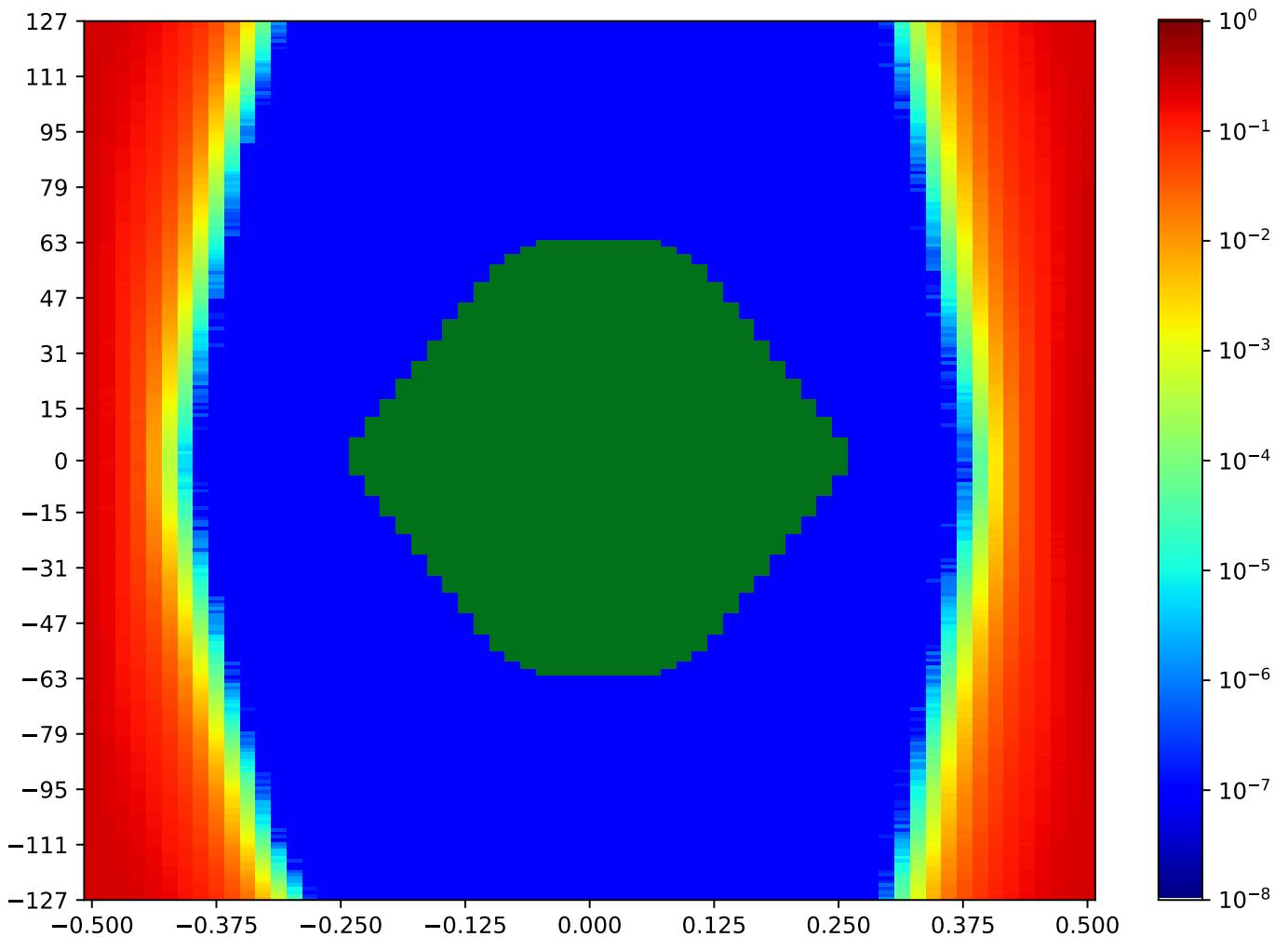


Figure 2.114: MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.17 MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

Table 2.106: MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:49:41		2018-Jan-24 04:50:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10134	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

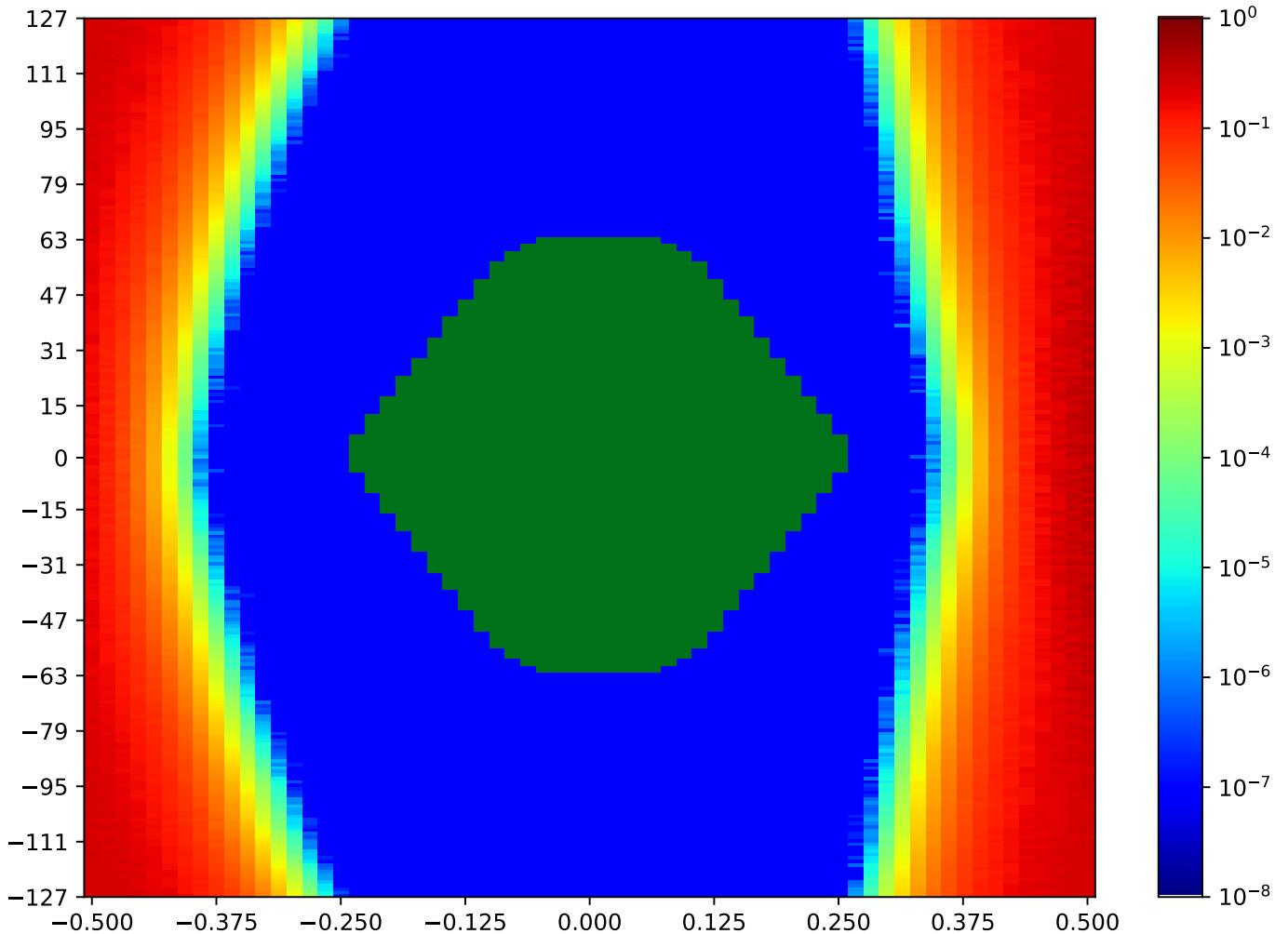


Figure 2.115: MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.18 MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

Table 2.107: MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:50:17		2018-Jan-24 04:50:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10236	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

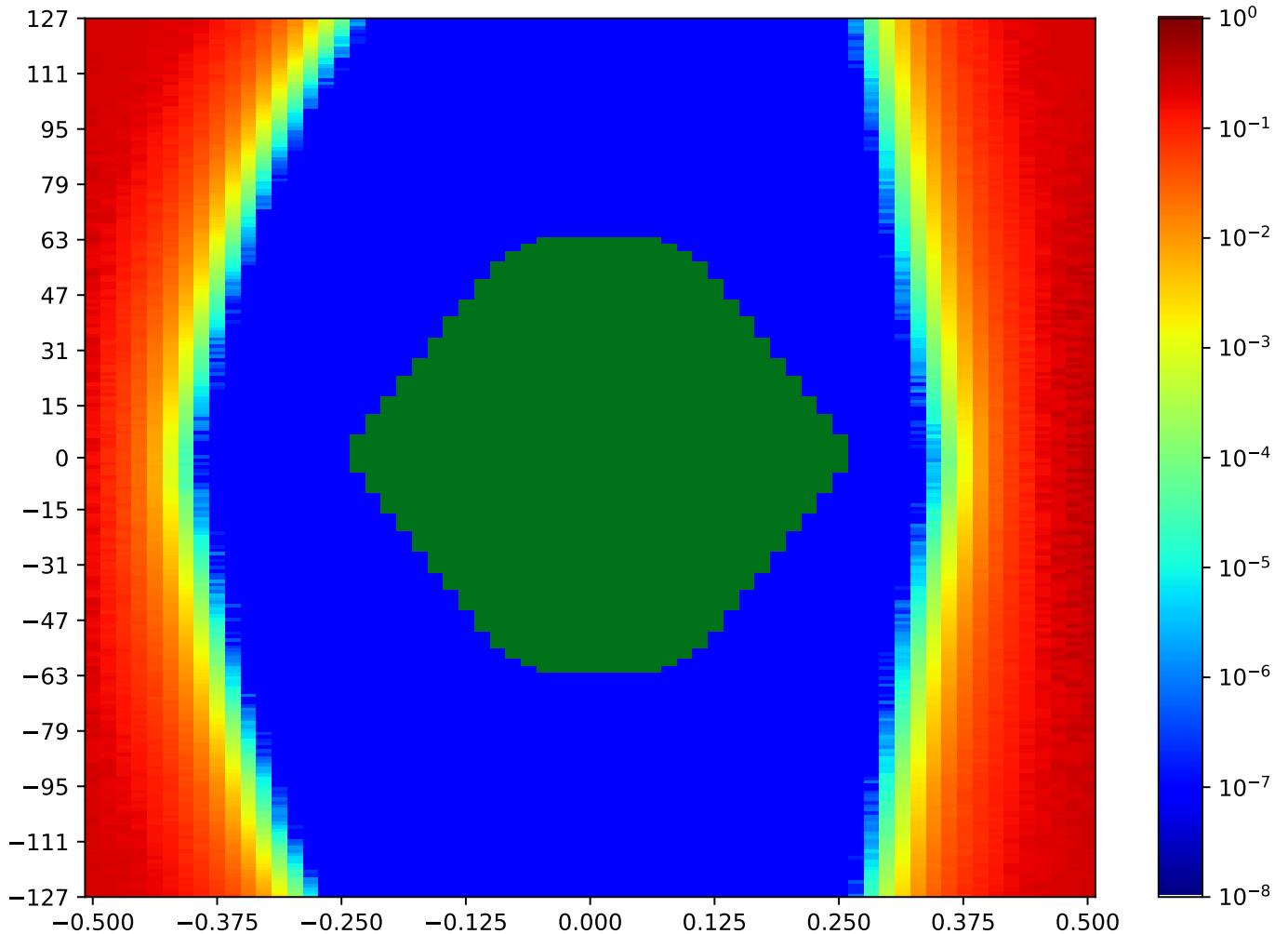


Figure 2.116: MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.19 MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

Table 2.108: MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:50:53		2018-Jan-24 04:51:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10543	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

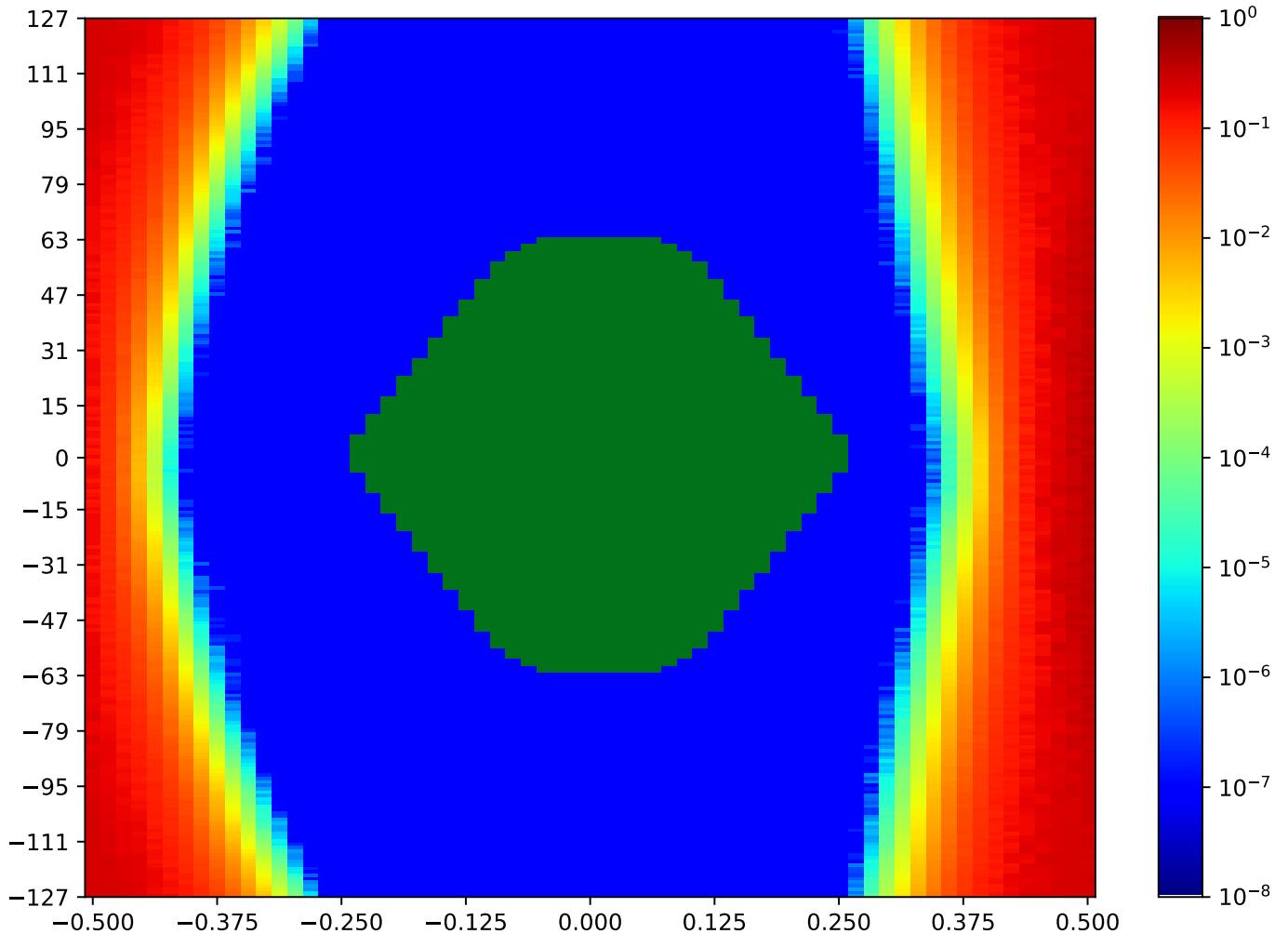


Figure 2.117: MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.20 MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

Table 2.109: MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:51:29		2018-Jan-24 04:52:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10508	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

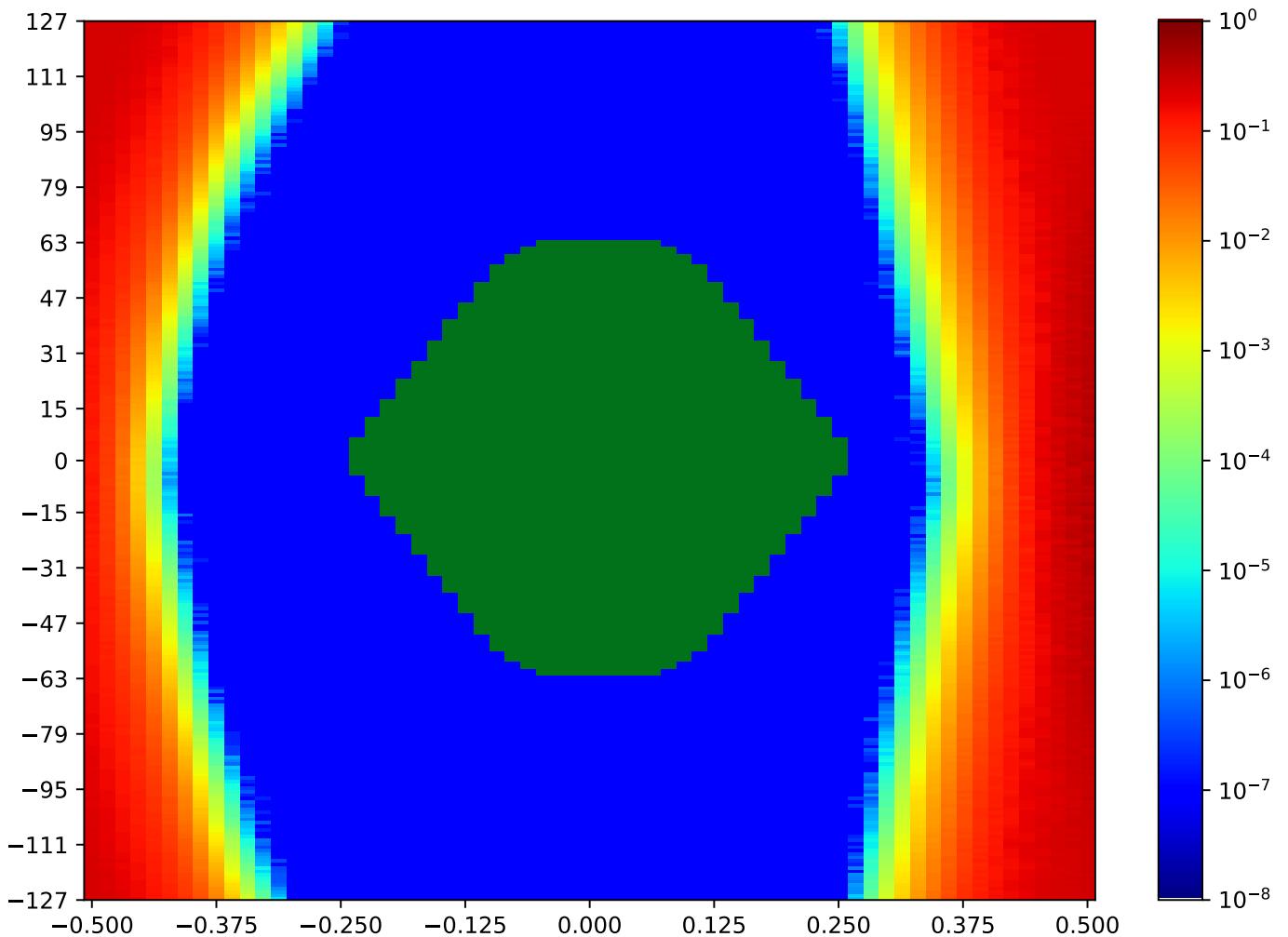


Figure 2.118: MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.21 MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

Table 2.110: MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:52:06		2018-Jan-24 04:52:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10753	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

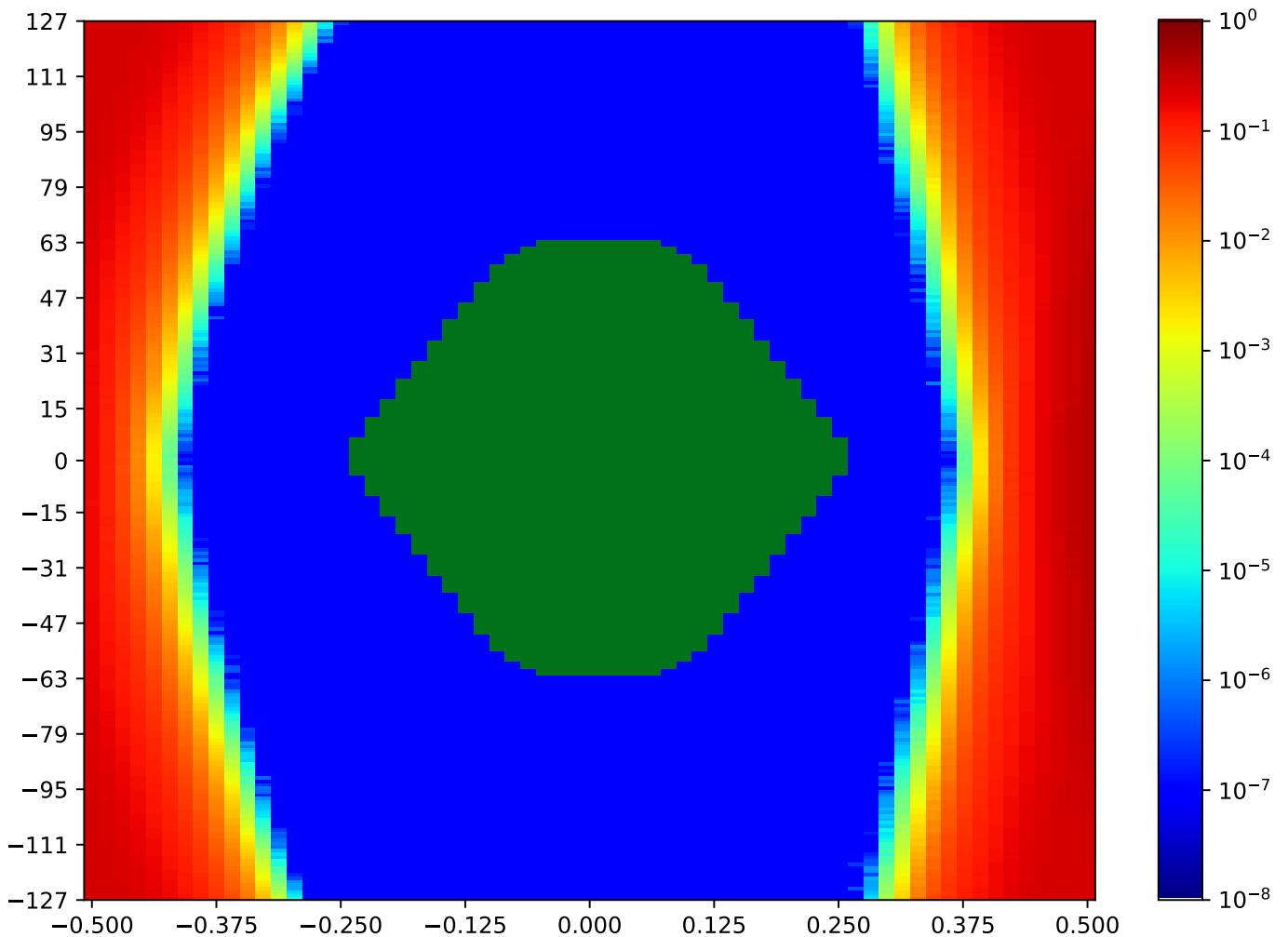


Figure 2.119: MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.22 MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

Table 2.111: MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:52:42		2018-Jan-24 04:53:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10797	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

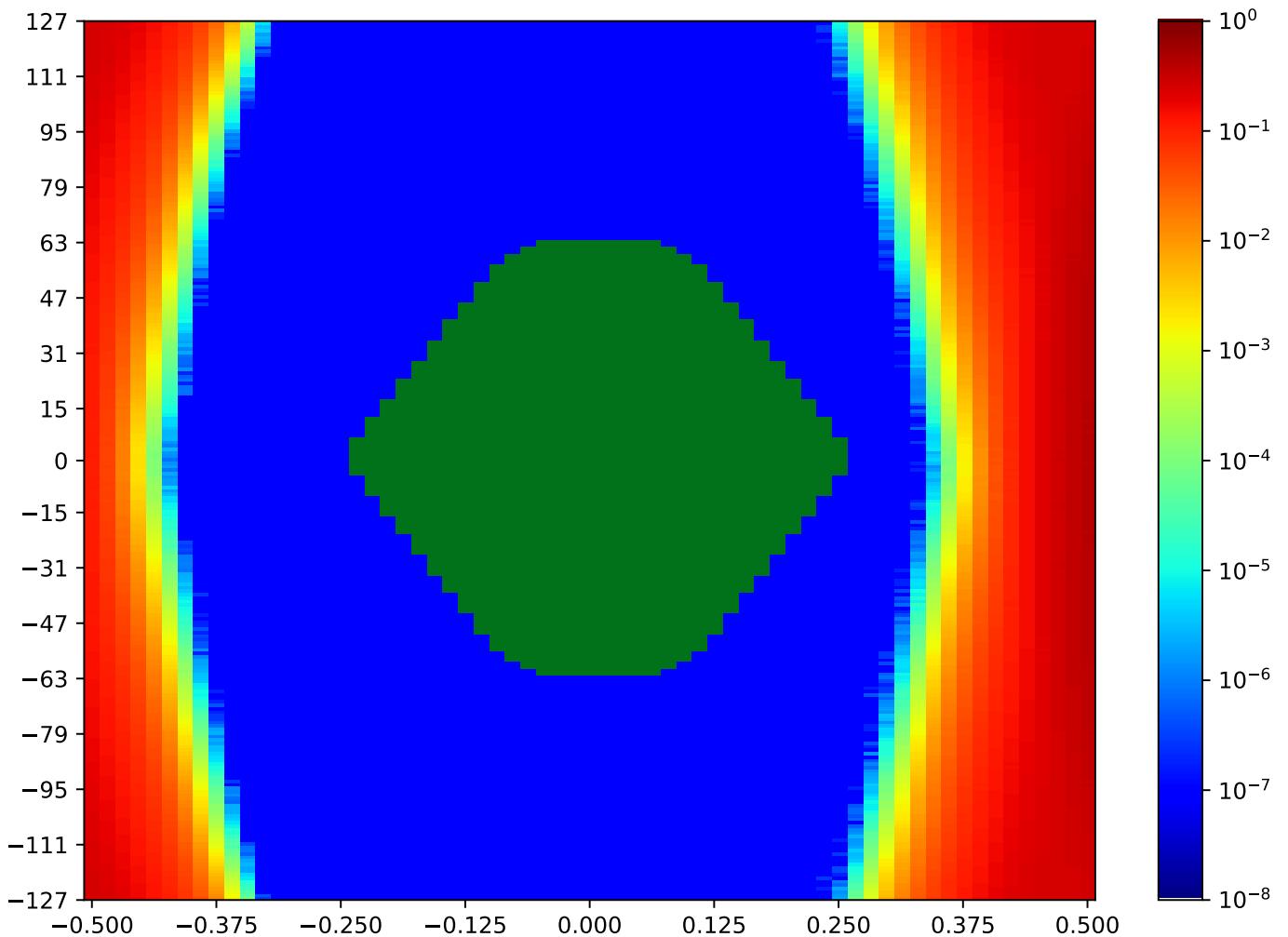


Figure 2.120: MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.23 MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

Table 2.112: MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:53:19		2018-Jan-24 04:53:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10526	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

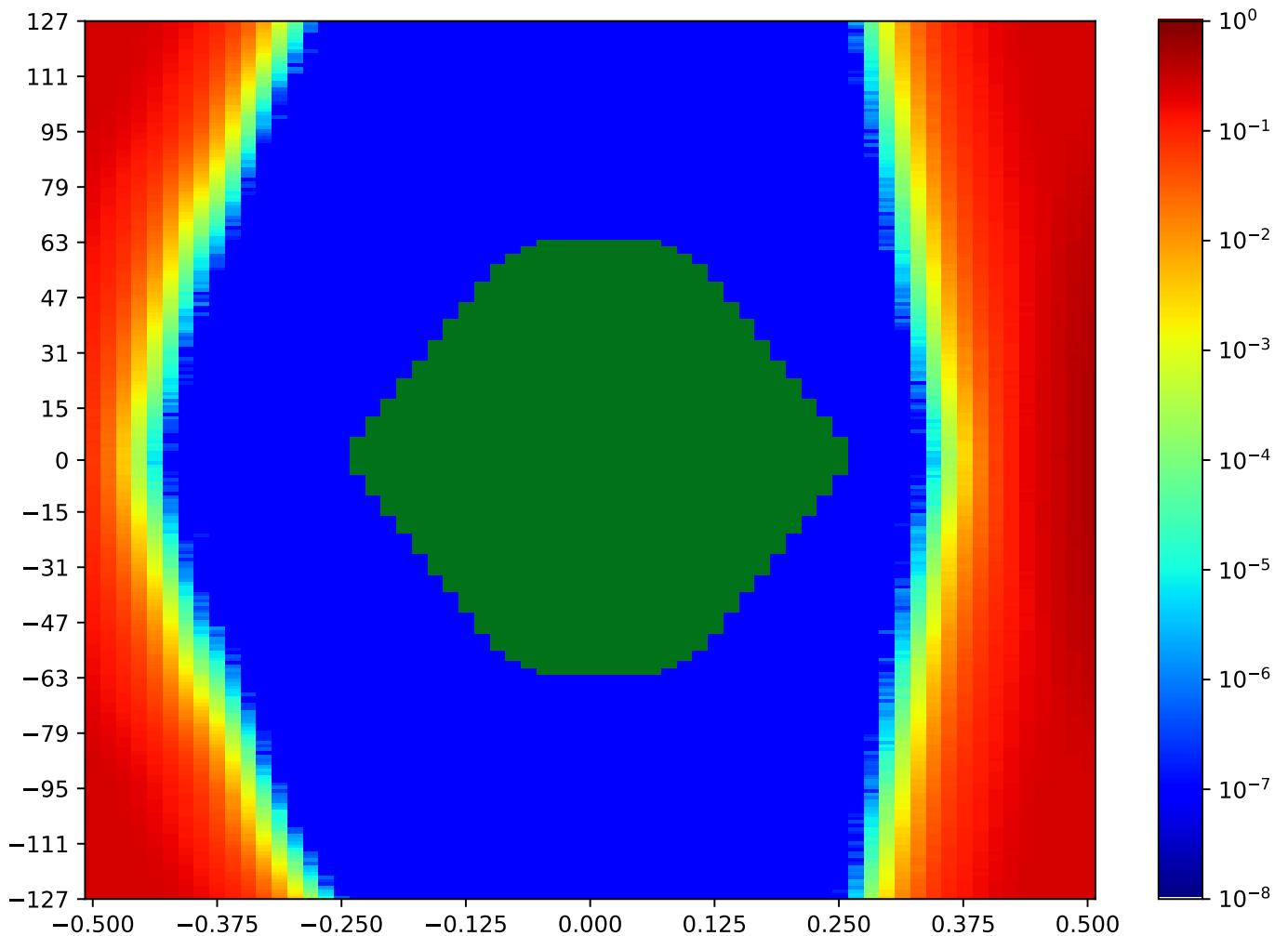


Figure 2.121: MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.24 MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

Table 2.113: MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:53:54		2018-Jan-24 04:54:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10510	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

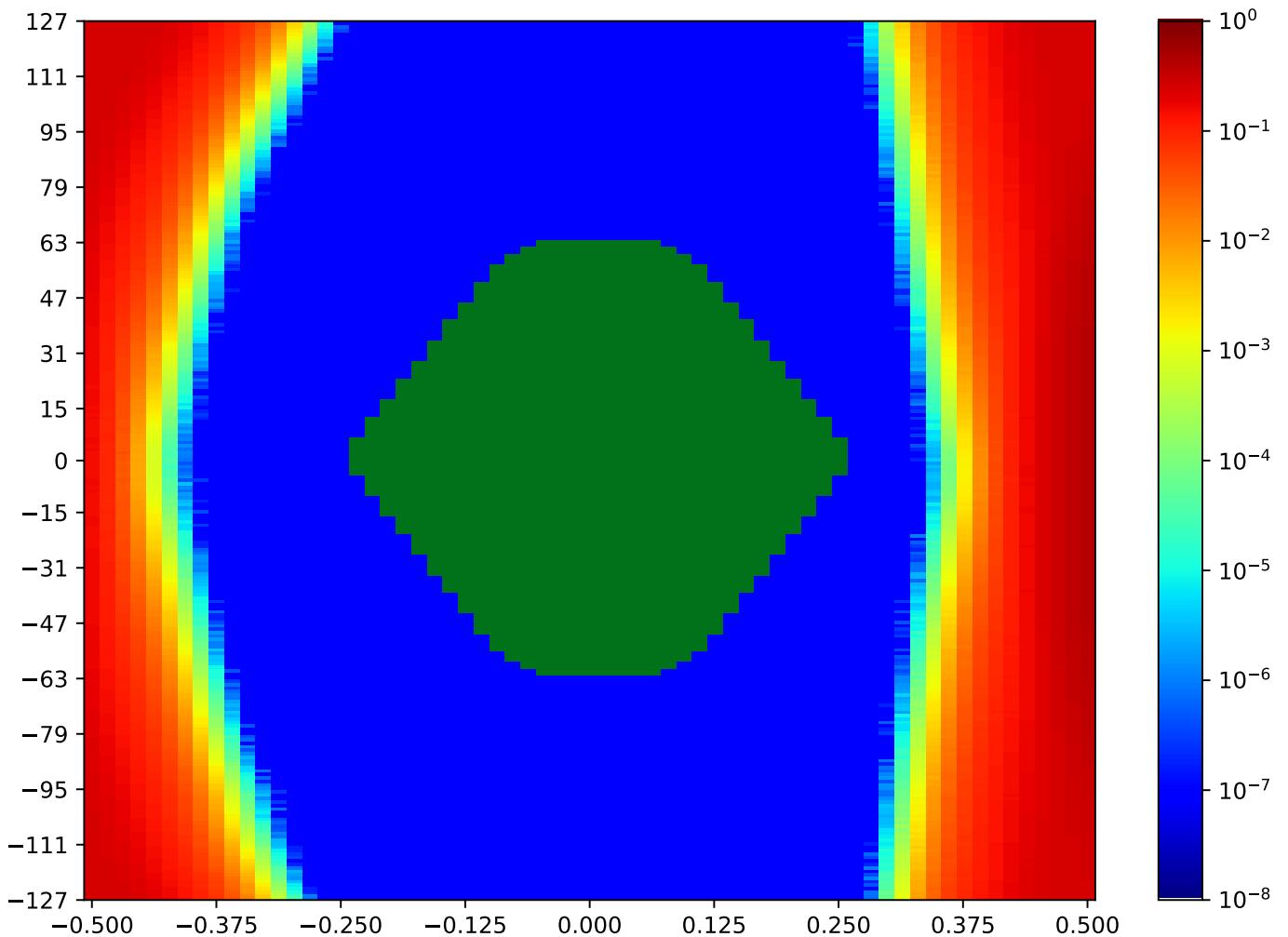


Figure 2.122: MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.25 MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

Table 2.114: MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:54:30		2018-Jan-24 04:55:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10410	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

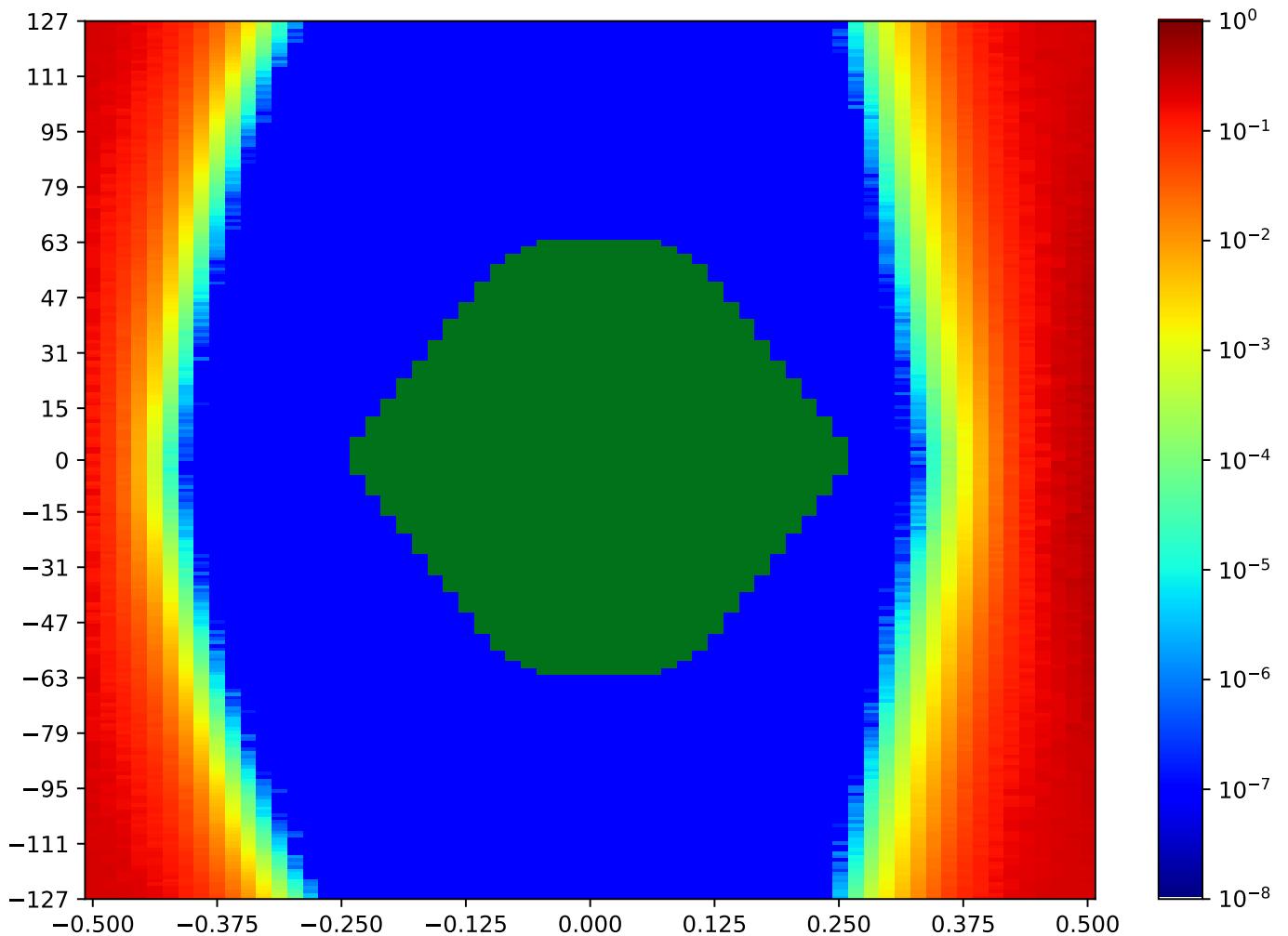


Figure 2.123: MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.26 MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

Table 2.115: MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:55:07		2018-Jan-24 04:55:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10608	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

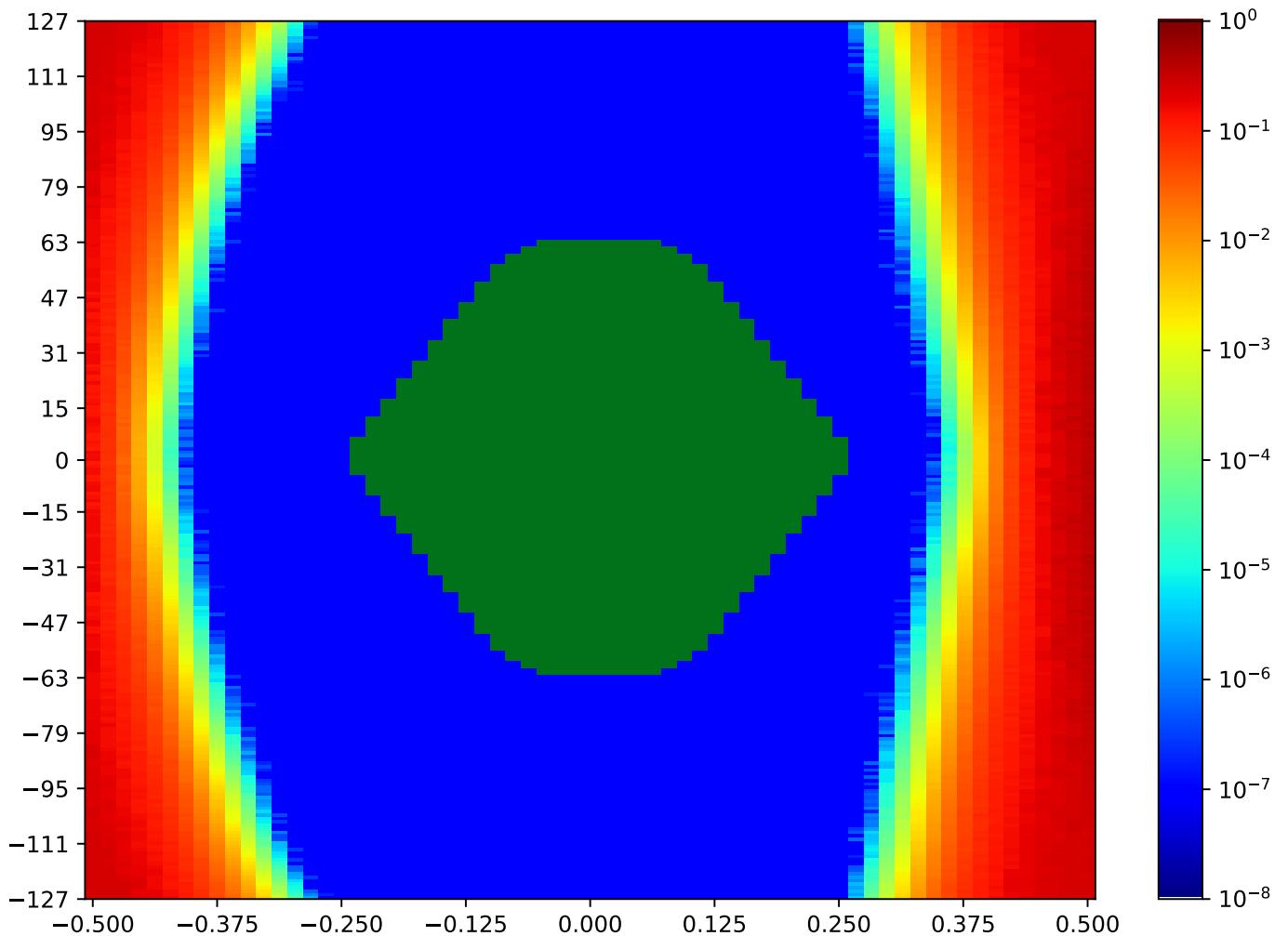


Figure 2.124: MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.27 MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

Table 2.116: MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:55:44		2018-Jan-24 04:56:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10023	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

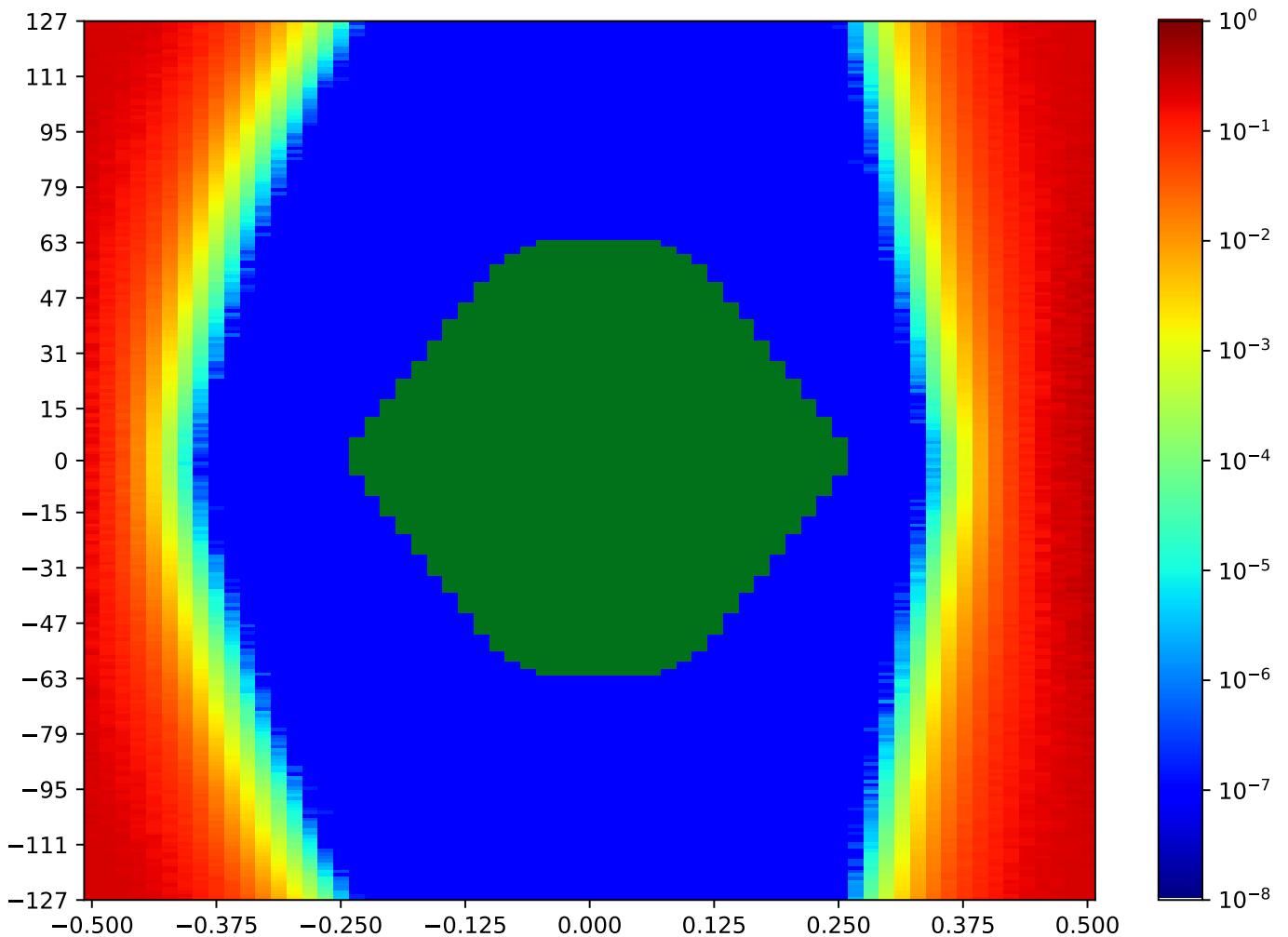


Figure 2.125: MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.9.28 MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

Table 2.117: MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 04:56:20		2018-Jan-24 04:56:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10306	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

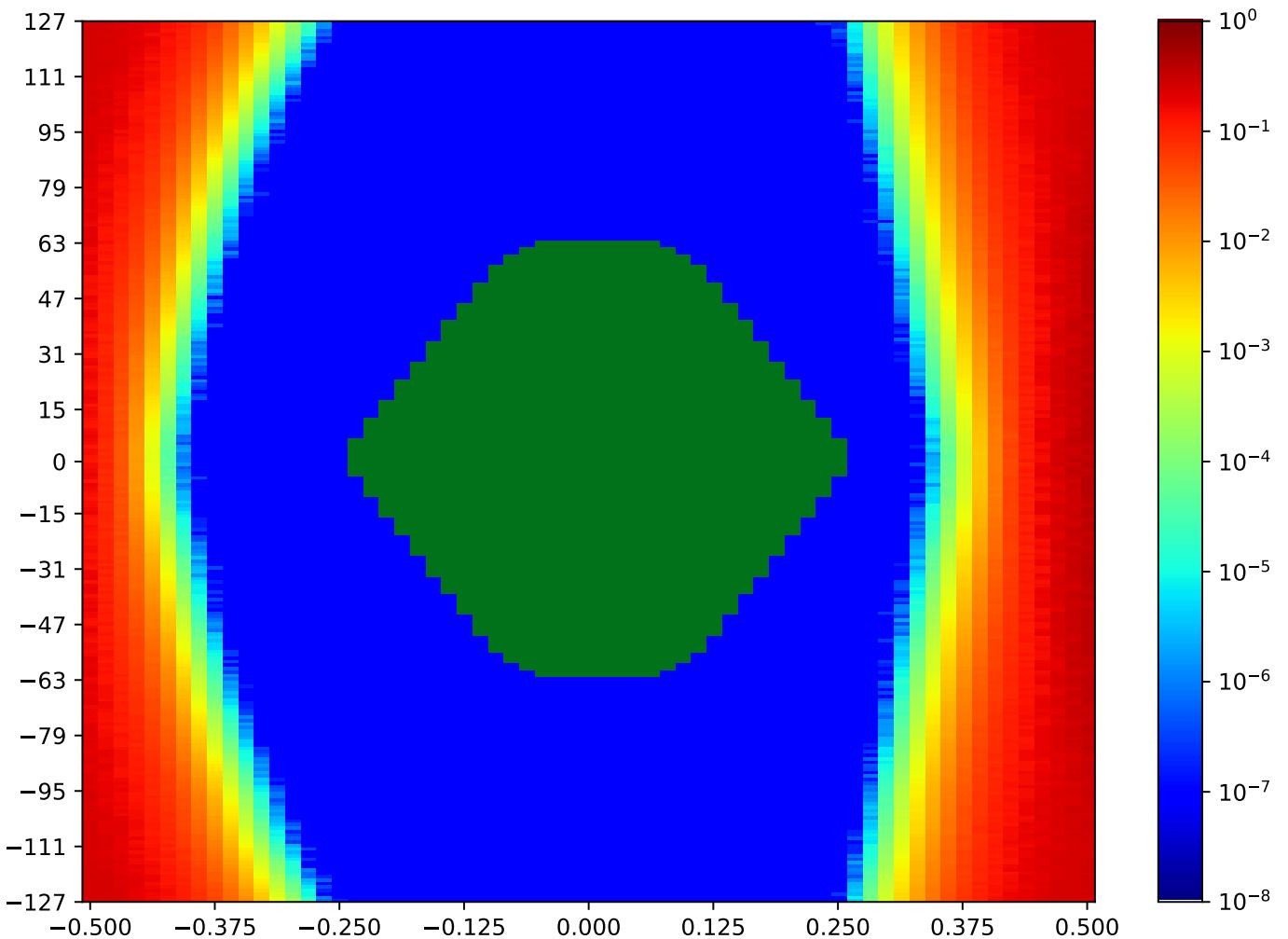


Figure 2.126: MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

Call back to summary Figure 2.98. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.10 MSP_A TX1 MSP_C RX18 Minipod Loopback

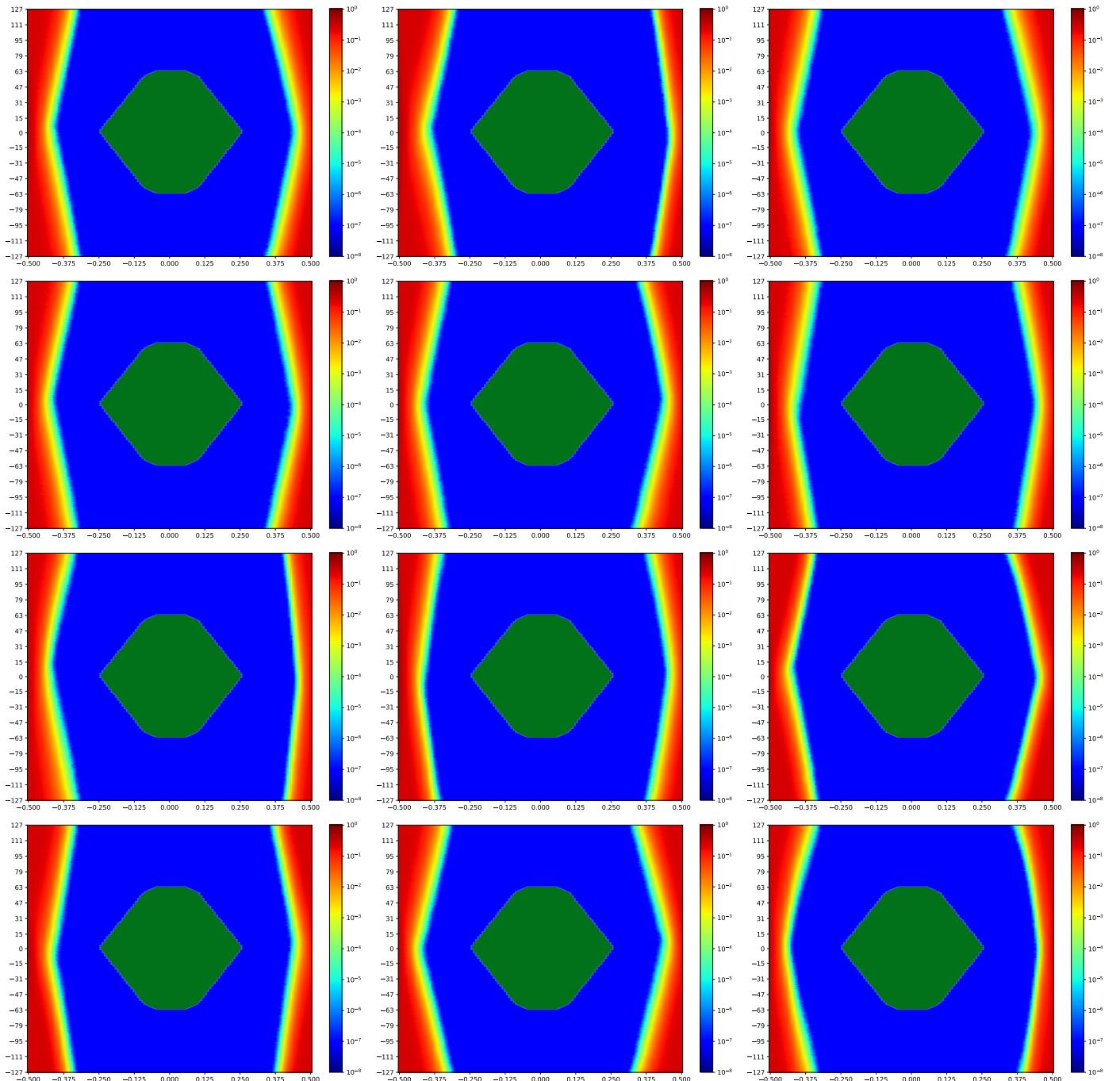


Figure 2.127: MSP_A TX1 MSP_C RX18 Minipod Loopback

A cross-reference to Figure 2.127. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.140.

2.10.1 MSP_A_FPGA-TX1-00-RX18-00-MSP_C_FPGA

Table 2.118: MSP_A_FPGA-TX1-00-RX18-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:31:48		2018-Jan-24 15:32:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23780	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

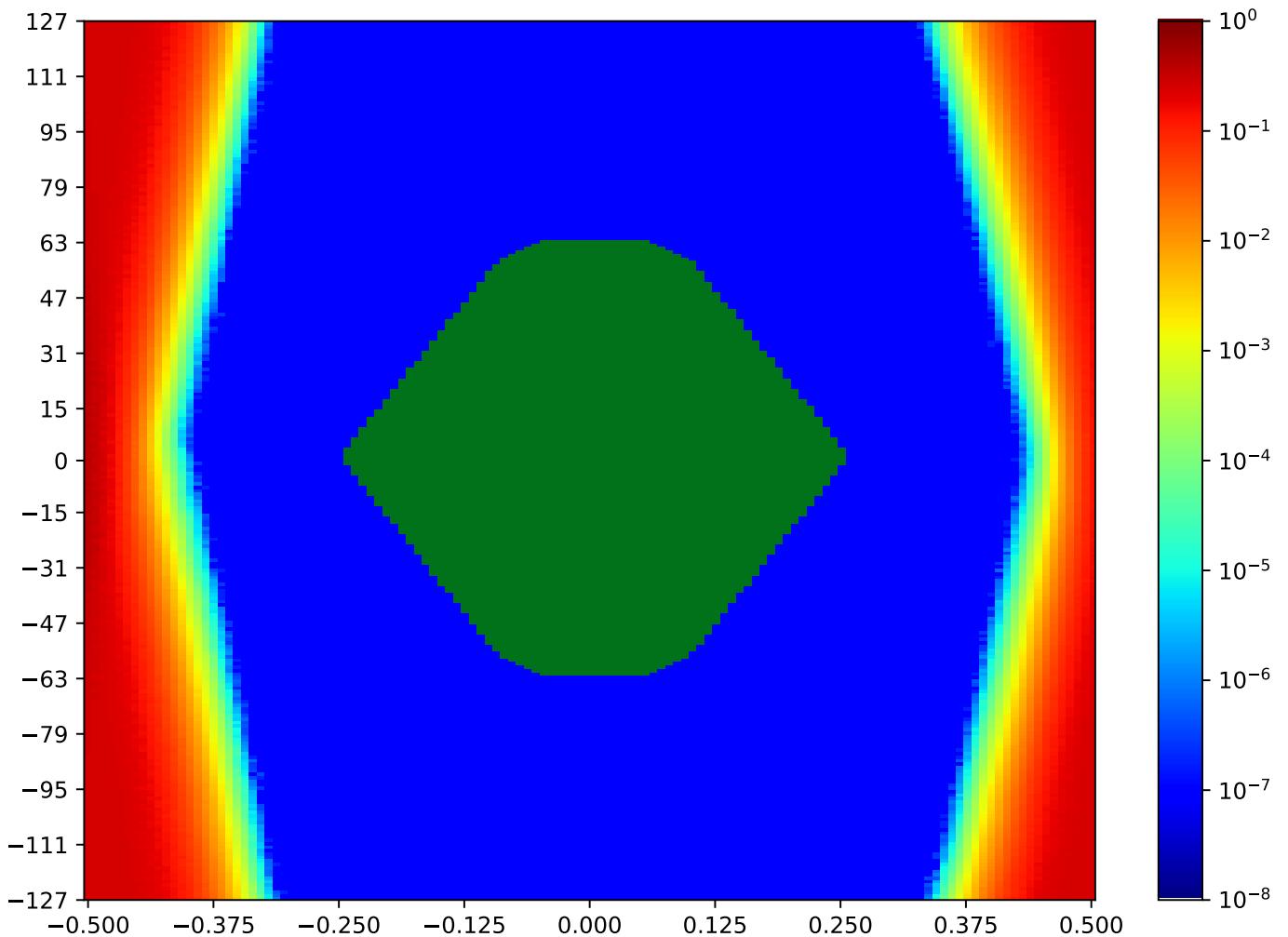


Figure 2.128: MSP_A_FPGA-TX1-00-RX18-00-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.2 MSP_A_FPGA-TX1-01-RX18-01-MSP_C_FPGA

Table 2.119: MSP_A_FPGA-TX1-01-RX18-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:34:06		2018-Jan-24 15:35:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24279	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

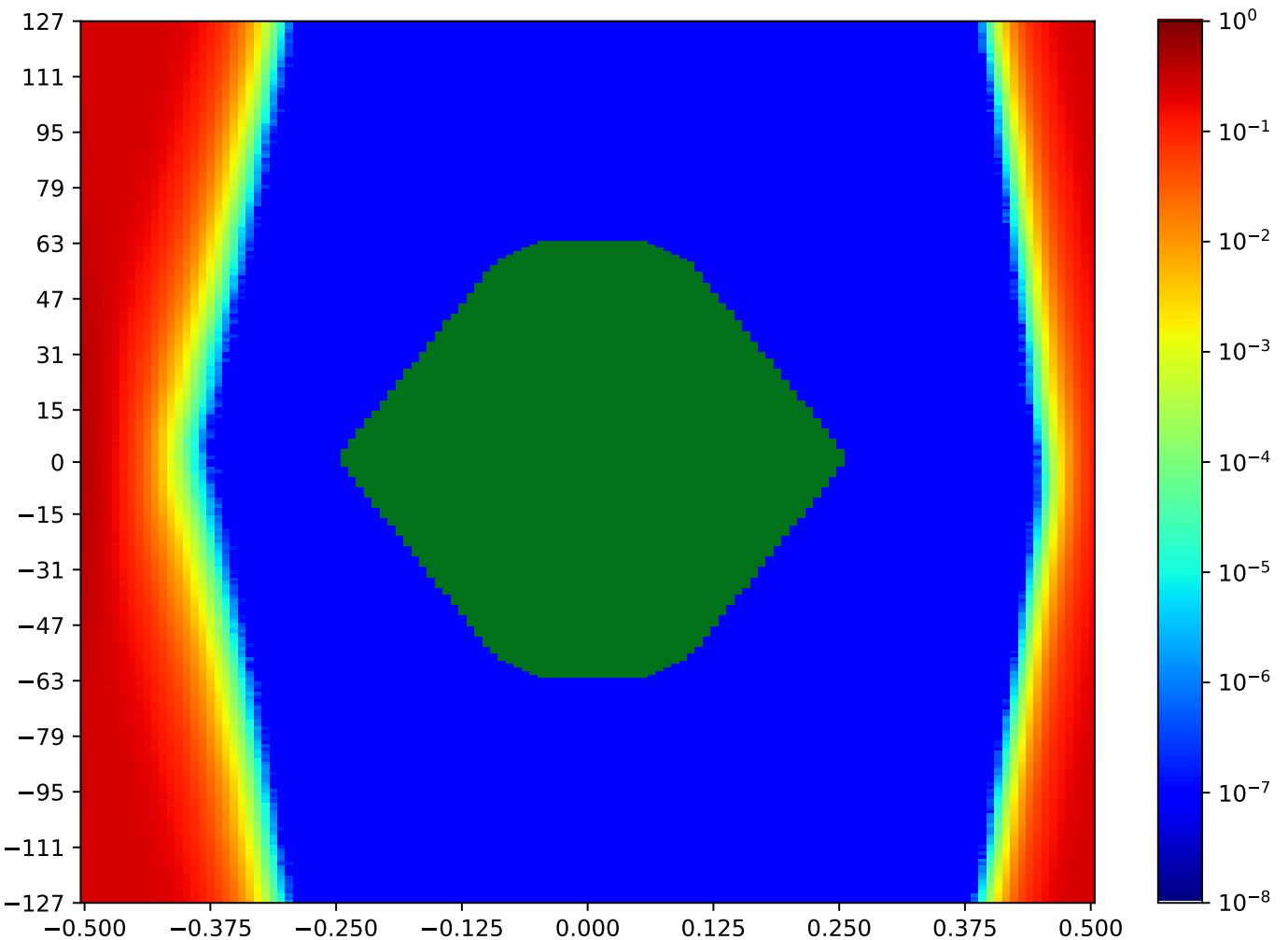


Figure 2.129: MSP_A_FPGA-TX1-01-RX18-01-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.3 MSP_A_FPGA-TX1-02-RX18-02-MSP_C_FPGA

Table 2.120: MSP_A_FPGA-TX1-02-RX18-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:35:16		2018-Jan-24 15:36:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23426	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

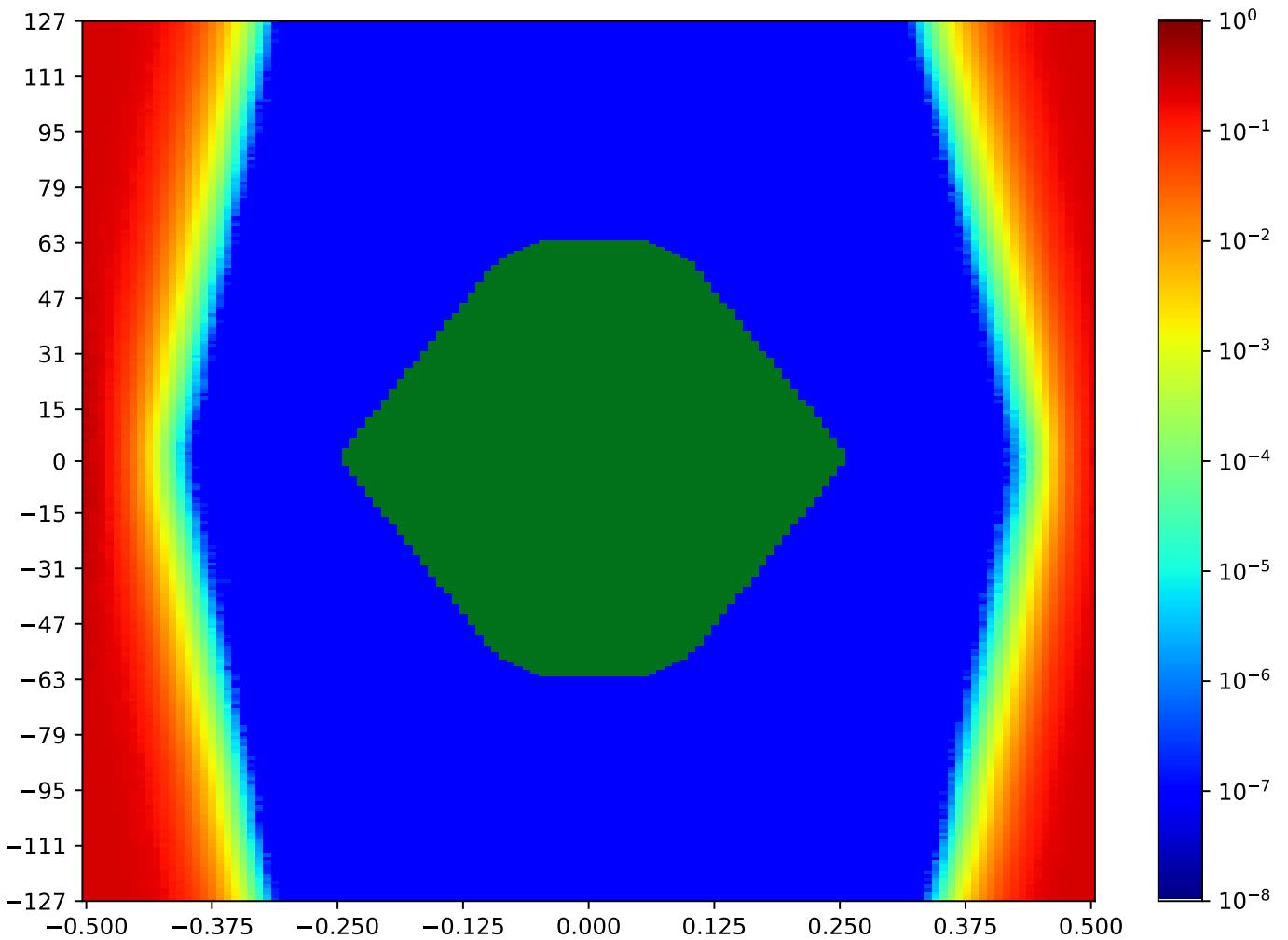


Figure 2.130: MSP_A_FPGA-TX1-02-RX18-02-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.4 MSP_A_FPGA-TX1-03-RX18-03-MSP_C_FPGA

Table 2.121: MSP_A_FPGA-TX1-03-RX18-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:29:30		2018-Jan-24 15:30:39	
Reset RX	OA	HO		HO (%)	
true	23913	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

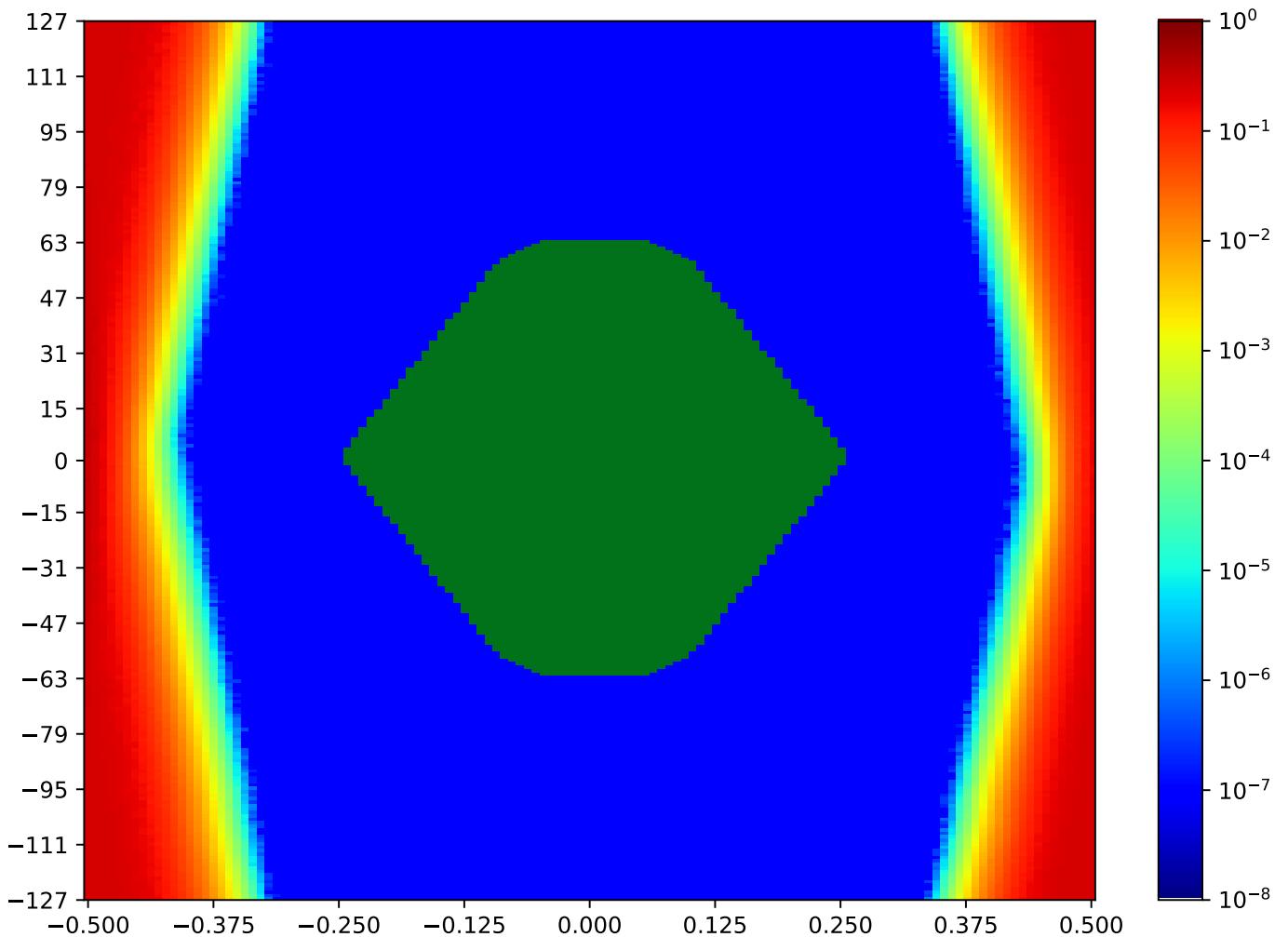


Figure 2.131: MSP_A_FPGA-TX1-03-RX18-03-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.5 MSP_A_FPGA-TX1-04-RX18-04-MSP_C_FPGA

Table 2.122: MSP_A_FPGA-TX1-04-RX18-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:38:45		2018-Jan-24 15:39:54	
Reset RX	OA	HO		HO (%)	
true	23720	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

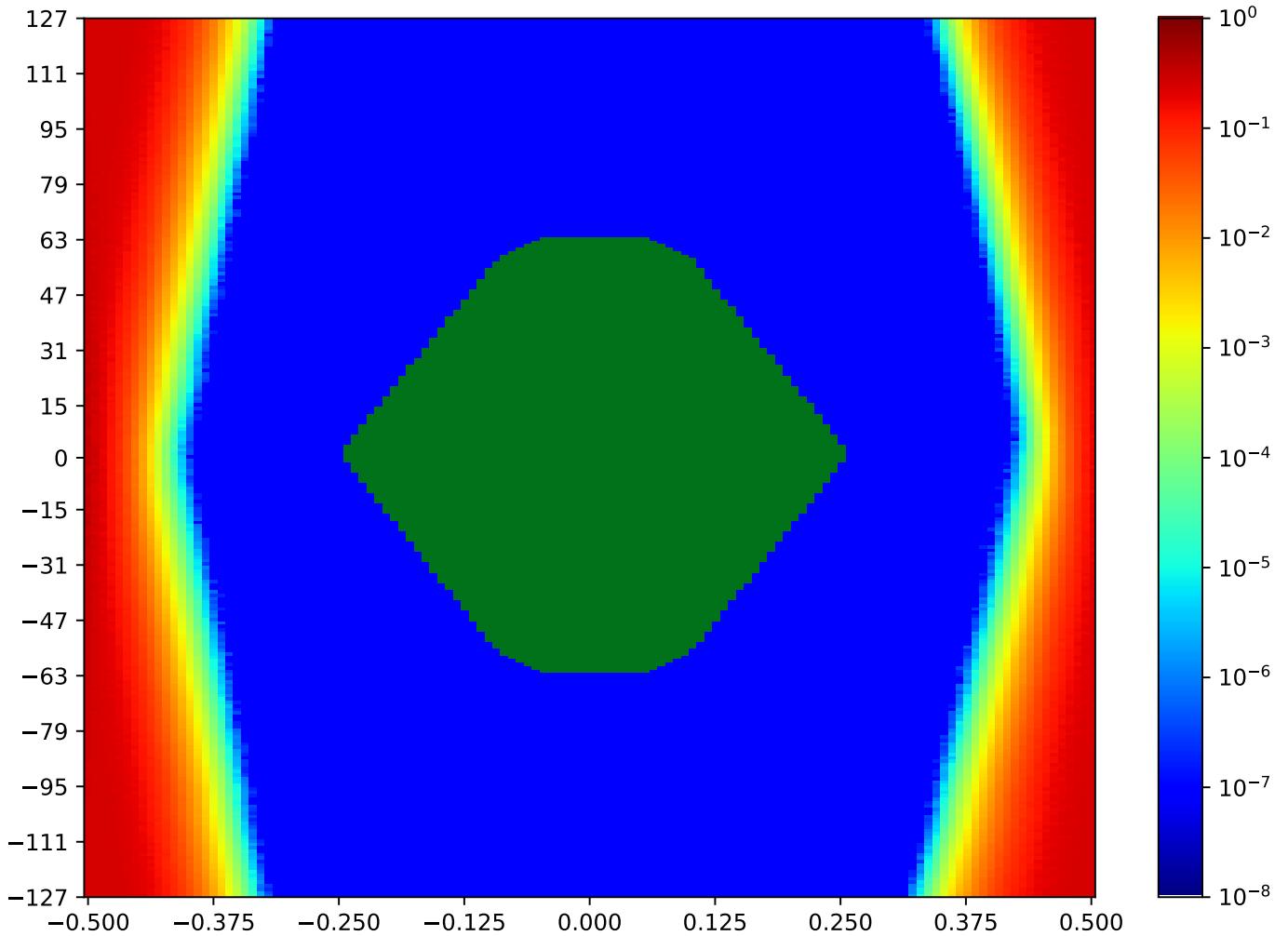


Figure 2.132: MSP_A_FPGA-TX1-04-RX18-04-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.6 MSP_A_FPGA-TX1-05-RX18-05-MSP_C_FPGA

Table 2.123: MSP_A_FPGA-TX1-05-RX18-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:28:21		2018-Jan-24 15:29:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24172	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

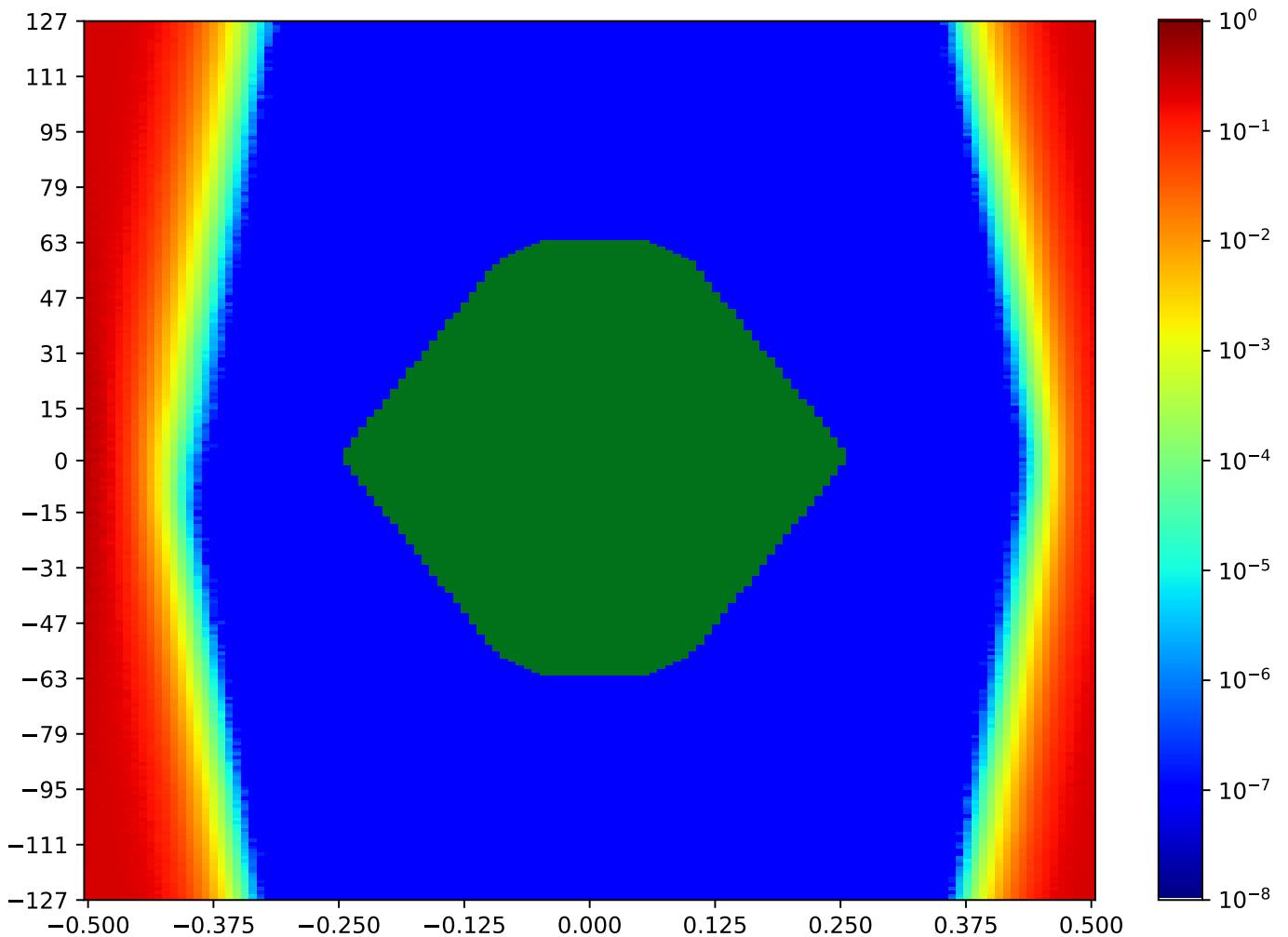


Figure 2.133: MSP_A_FPGA-TX1-05-RX18-05-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.7 MSP_A_FPGA-TX1-06-RX18-06-MSP_C_FPGA

Table 2.124: MSP_A_FPGA-TX1-06-RX18-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:41:05		2018-Jan-24 15:42:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25351	107	82.95%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

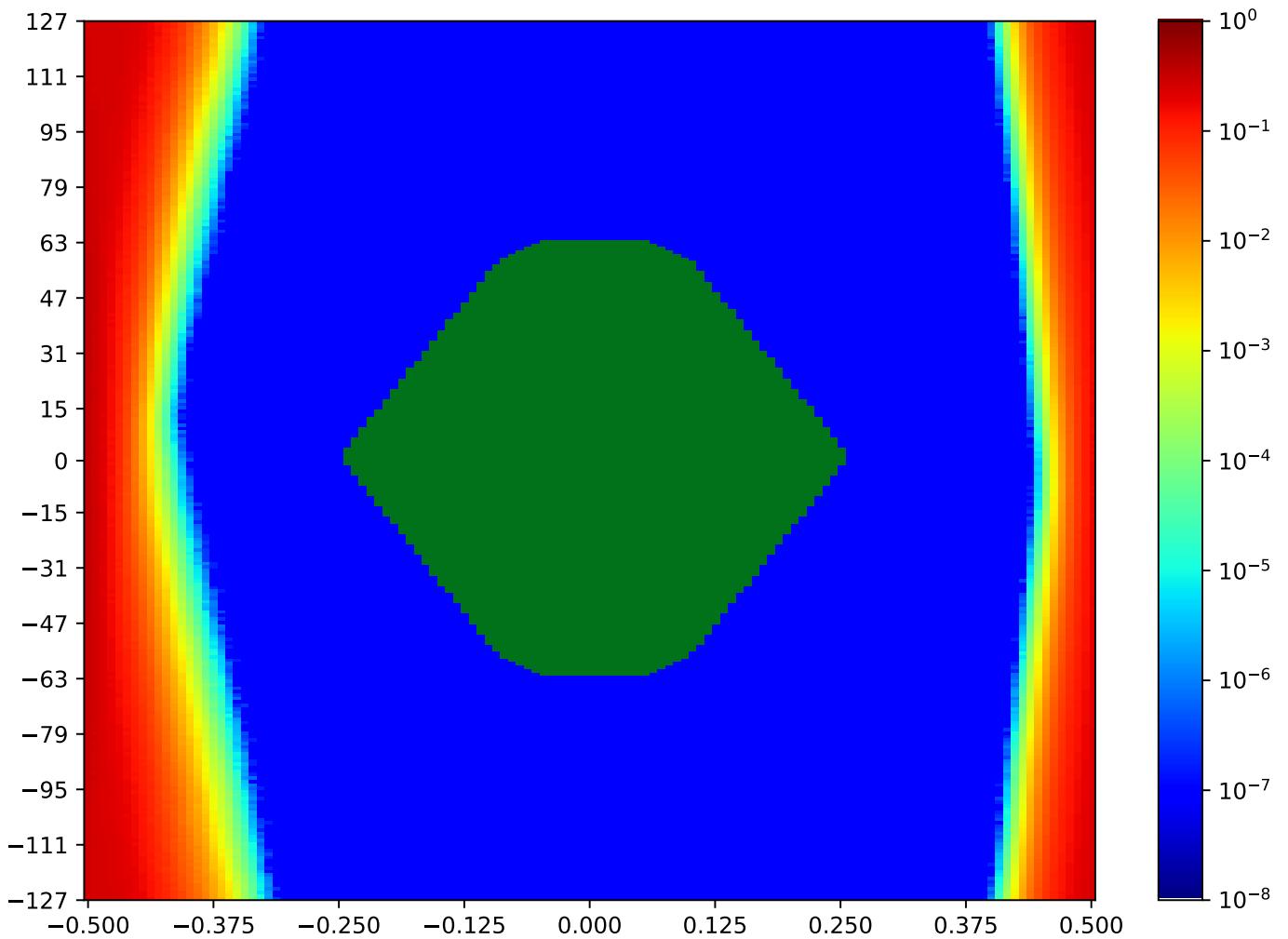


Figure 2.134: MSP_A_FPGA-TX1-06-RX18-06-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.8 MSP_A_FPGA-TX1-07-RX18-07-MSP_C_FPGA

Table 2.125: MSP_A_FPGA-TX1-07-RX18-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:30:39		2018-Jan-24 15:31:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25212	107	82.95%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

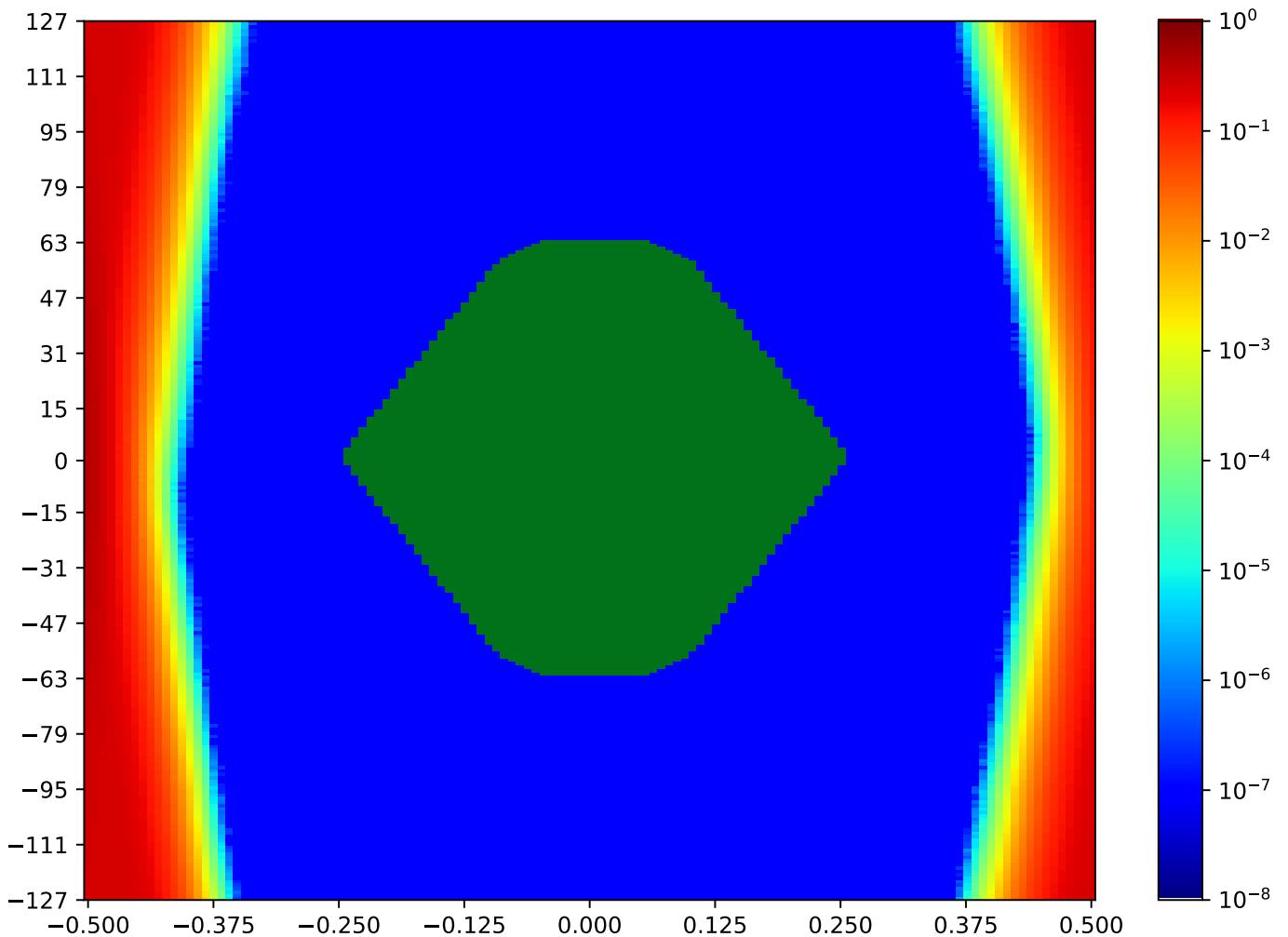


Figure 2.135: MSP_A_FPGA-TX1-07-RX18-07-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.9 MSP_A_FPGA-TX1-08-RX18-08-MSP_C_FPGA

Table 2.126: MSP_A_FPGA-TX1-08-RX18-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:39:55		2018-Jan-24 15:41:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24400	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

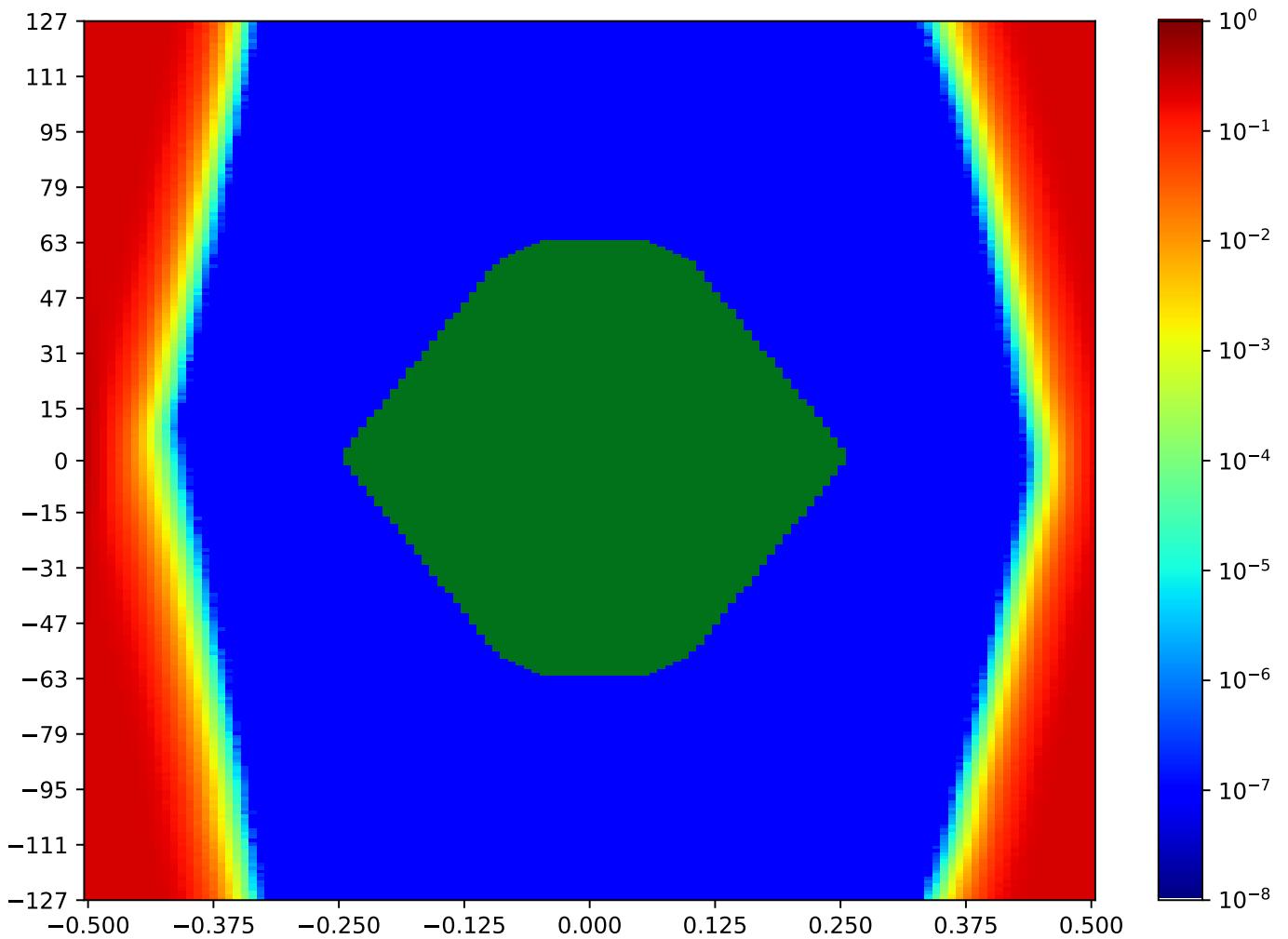


Figure 2.136: MSP_A_FPGA-TX1-08-RX18-08-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.10 MSP_A_FPGA-TX1-09-RX18-09-MSP_C_FPGA

Table 2.127: MSP_A_FPGA-TX1-09-RX18-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:32:58		2018-Jan-24 15:34:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24246	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

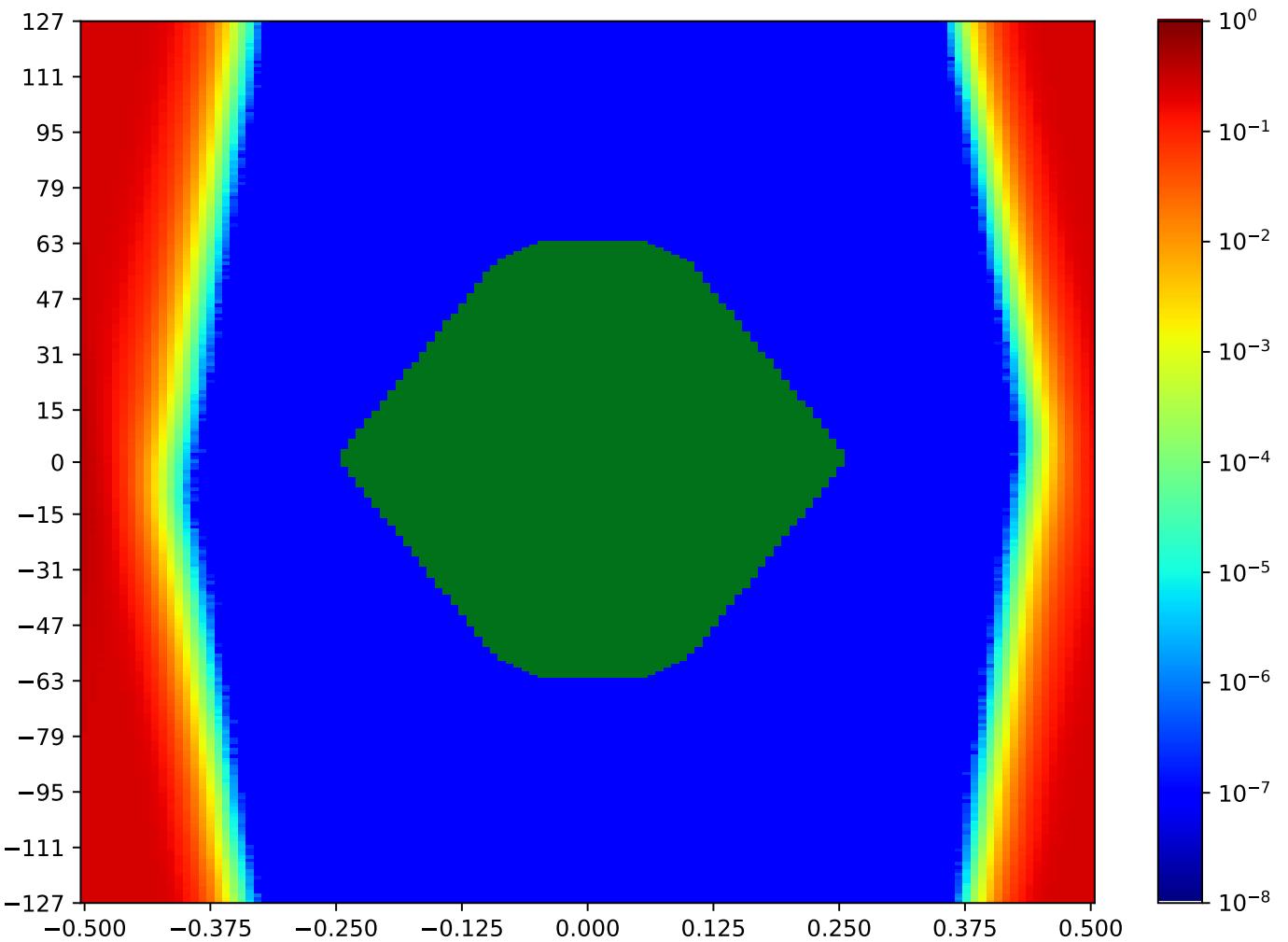


Figure 2.137: MSP_A_FPGA-TX1-09-RX18-09-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.11 MSP_A_FPGA-TX1-10-RX18-10-MSP_C_FPGA

Table 2.128: MSP_A_FPGA-TX1-10-RX18-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:37:36		2018-Jan-24 15:38:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23357	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

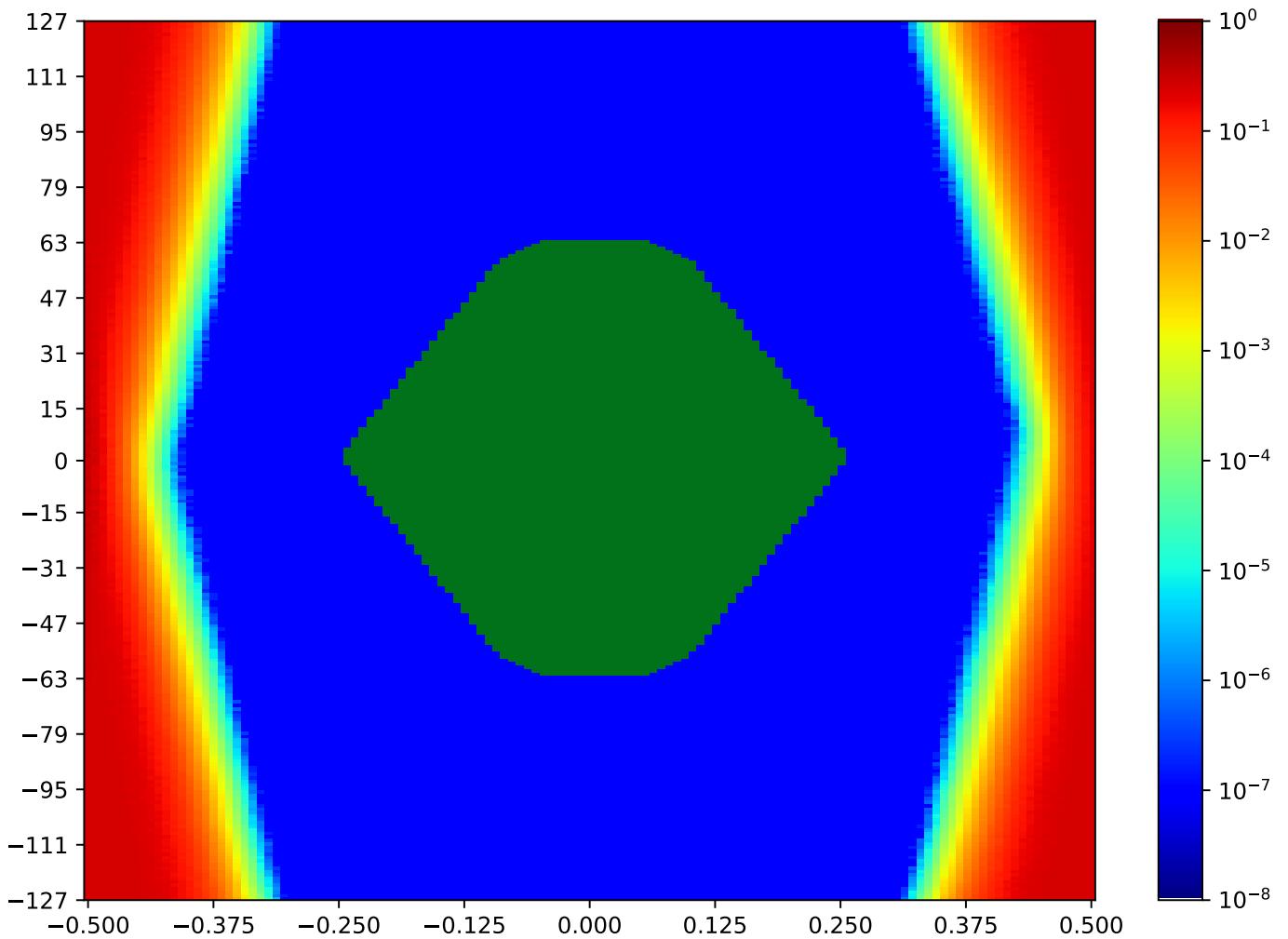


Figure 2.138: MSP_A_FPGA-TX1-10-RX18-10-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.10.12 MSP_A_FPGA-TX1-11-RX18-11-MSP_C_FPGA

Table 2.129: MSP_A_FPGA-TX1-11-RX18-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:36:25		2018-Jan-24 15:37:35	
Reset RX	OA	HO		HO (%)	
true	25337	109		84.50%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

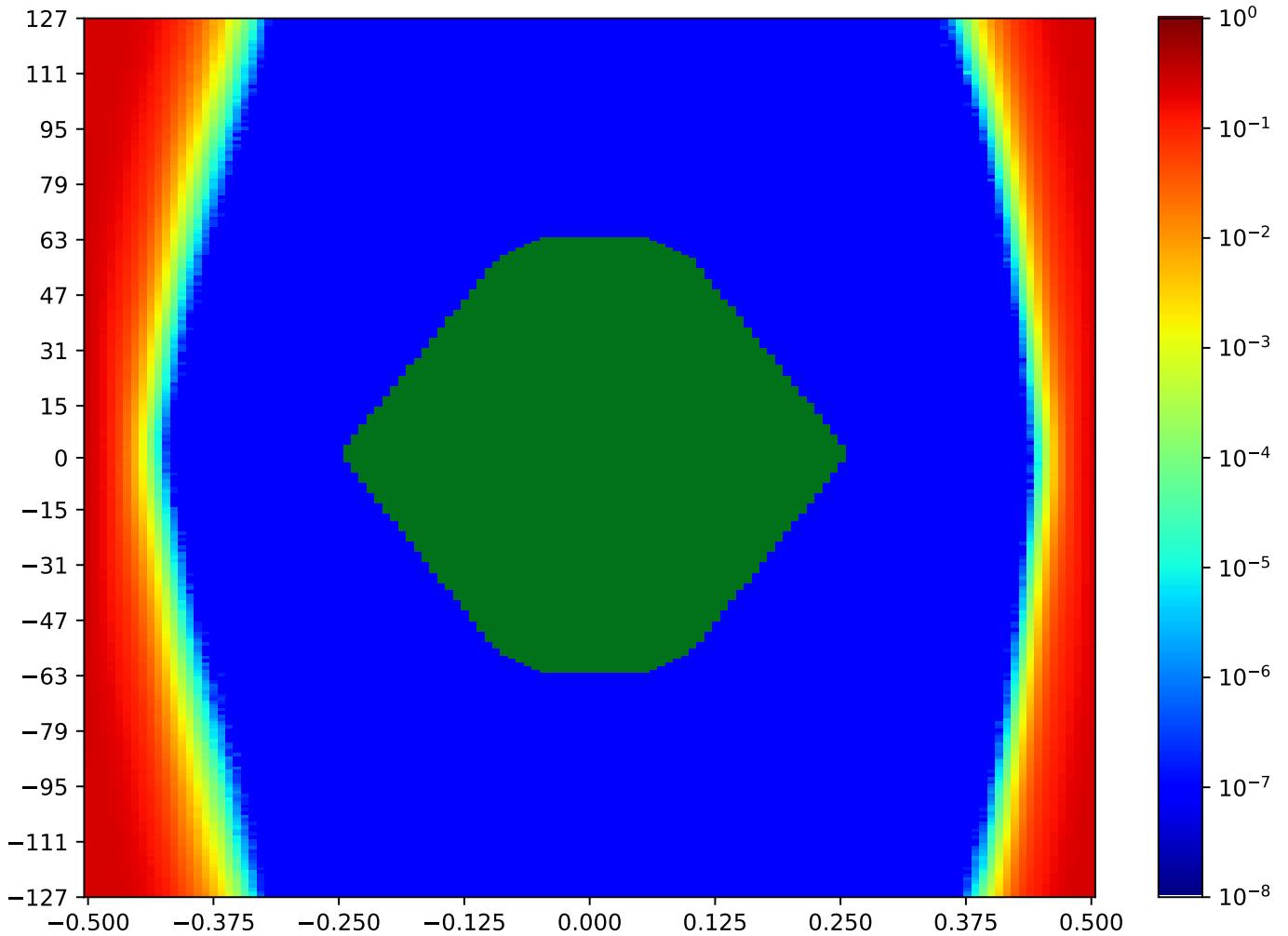


Figure 2.139: MSP_A_FPGA-TX1-11-RX18-11-MSP_C_FPGA

Call back to summary Figure 2.127. Sibling eye diagrams: V1-12.8.

2.11 MSP_A TX2 MSP_C RX17 Minipod Loopback

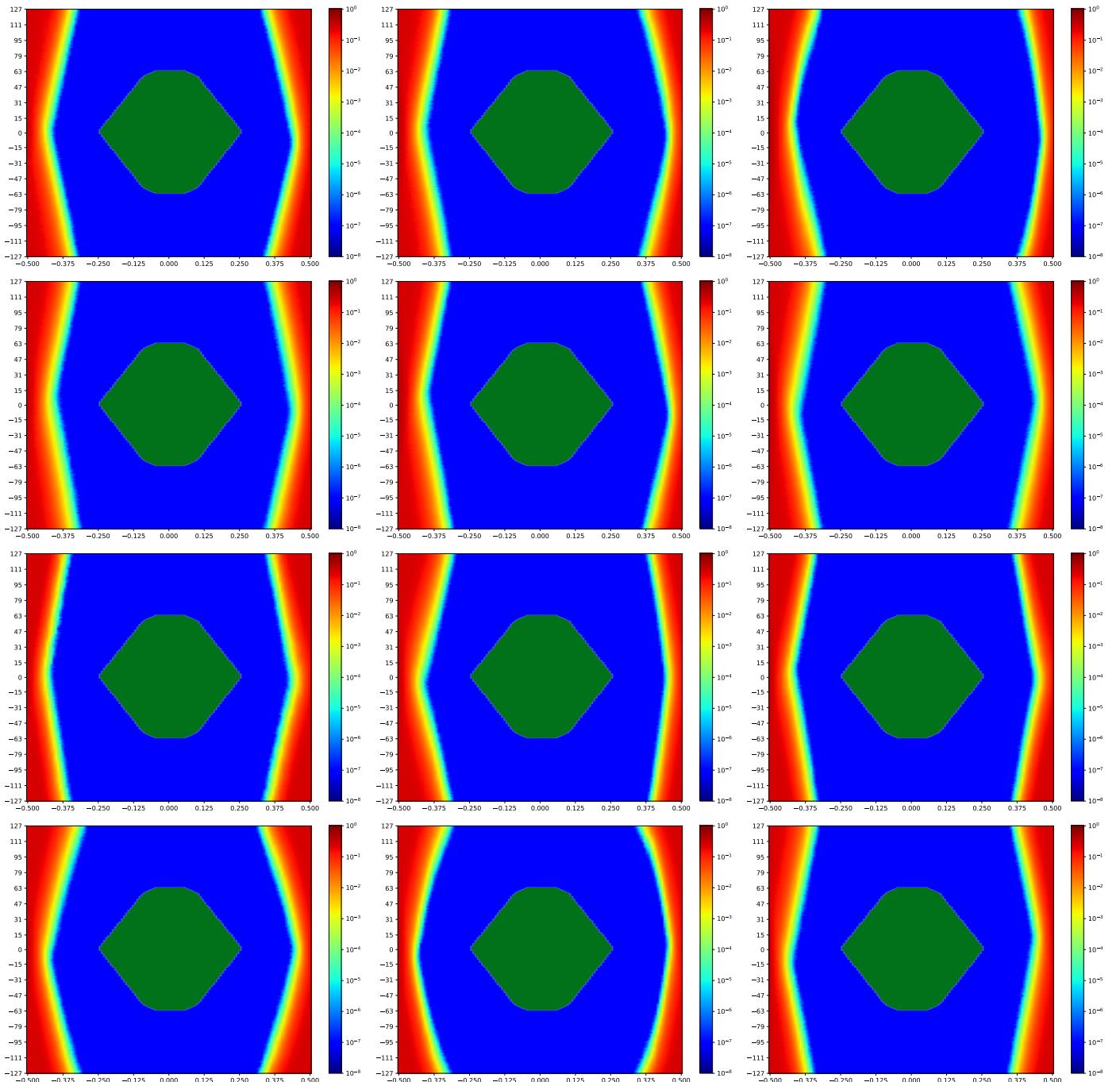


Figure 2.140: MSP_A TX2 MSP_C RX17 Minipod Loopback

A cross-reference to Figure 2.140. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.153.

2.11.1 MSP_A_FPGA-TX2-00-RX17-00-MSP_C_FPGA

Table 2.130: MSP_A_FPGA-TX2-00-RX17-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:45:47		2018-Jan-24 15:46:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23920	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

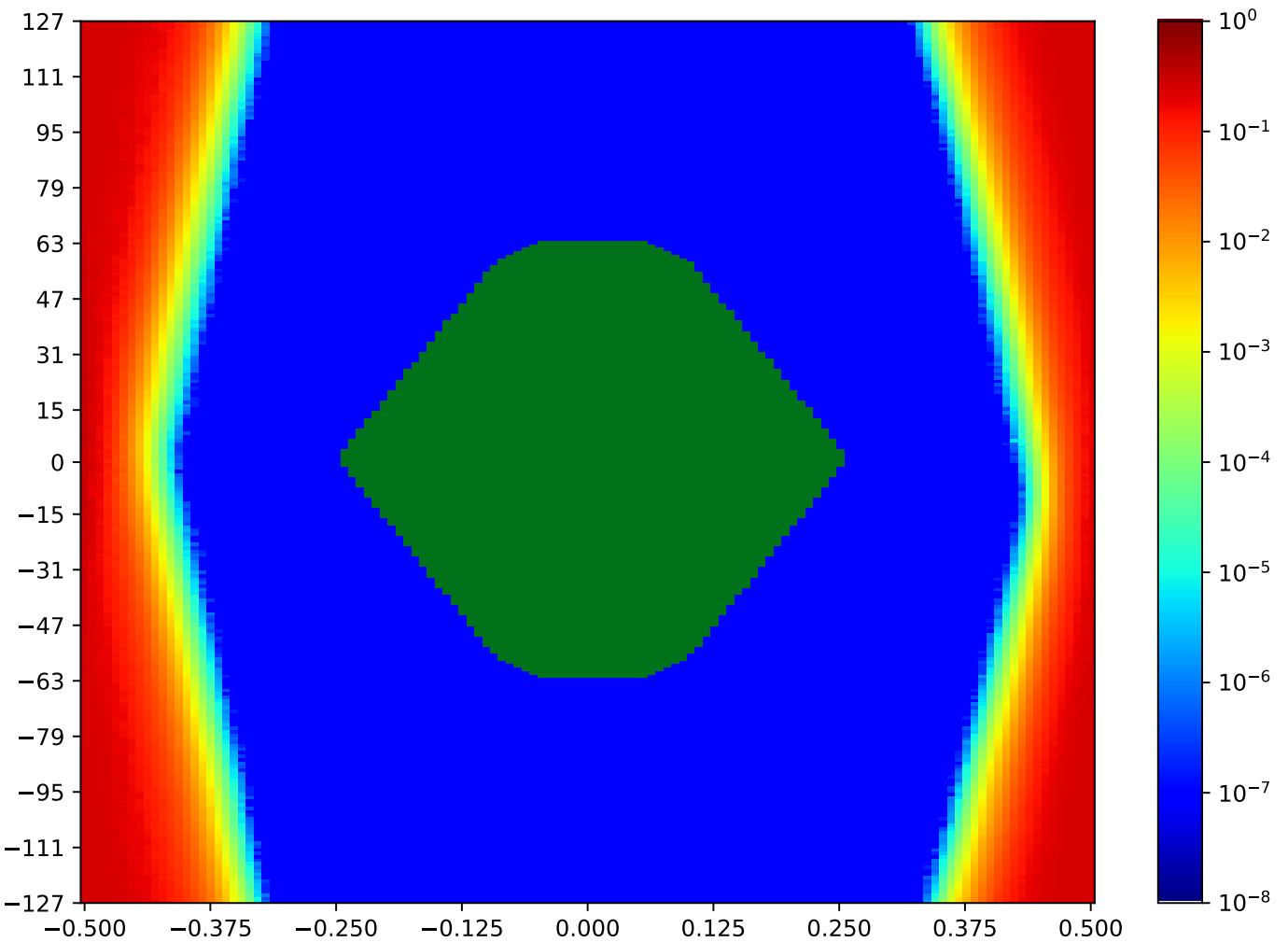


Figure 2.141: MSP_A_FPGA-TX2-00-RX17-00-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.2 MSP_A_FPGA-TX2-01-RX17-01-MSP_C_FPGA

Table 2.131: MSP_A_FPGA-TX2-01-RX17-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:43:26		2018-Jan-24 15:44:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24122	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

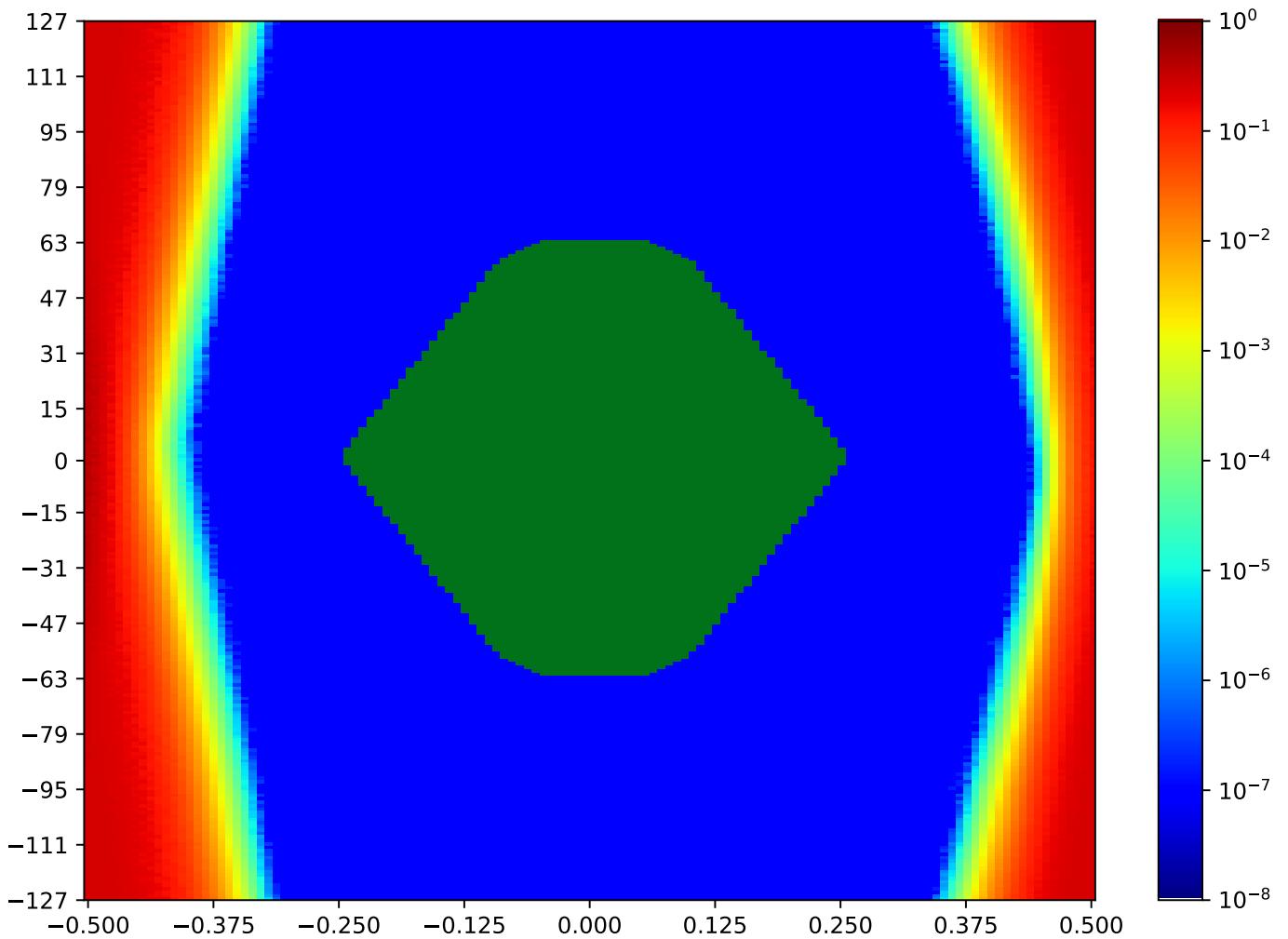


Figure 2.142: MSP_A_FPGA-TX2-01-RX17-01-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.3 MSP_A_FPGA-TX2-02-RX17-02-MSP_C_FPGA

Table 2.132: MSP_A_FPGA-TX2-02-RX17-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:49:16		2018-Jan-24 15:50:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24995	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

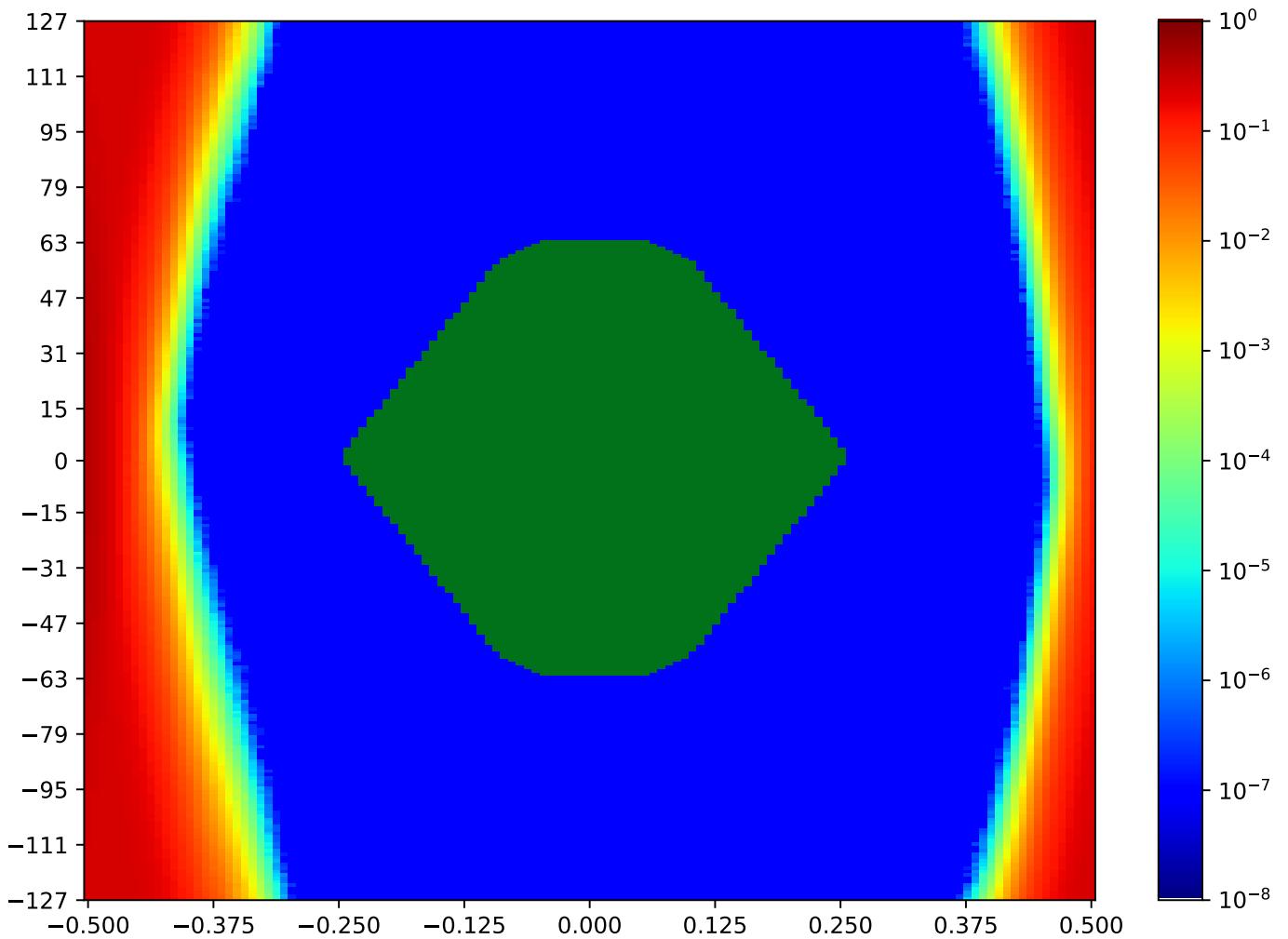


Figure 2.143: MSP_A_FPGA-TX2-02-RX17-02-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.4 MSP_A_FPGA-TX2-03-RX17-03-MSP_C_FPGA

Table 2.133: MSP_A_FPGA-TX2-03-RX17-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:42:15		2018-Jan-24 15:43:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23435	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

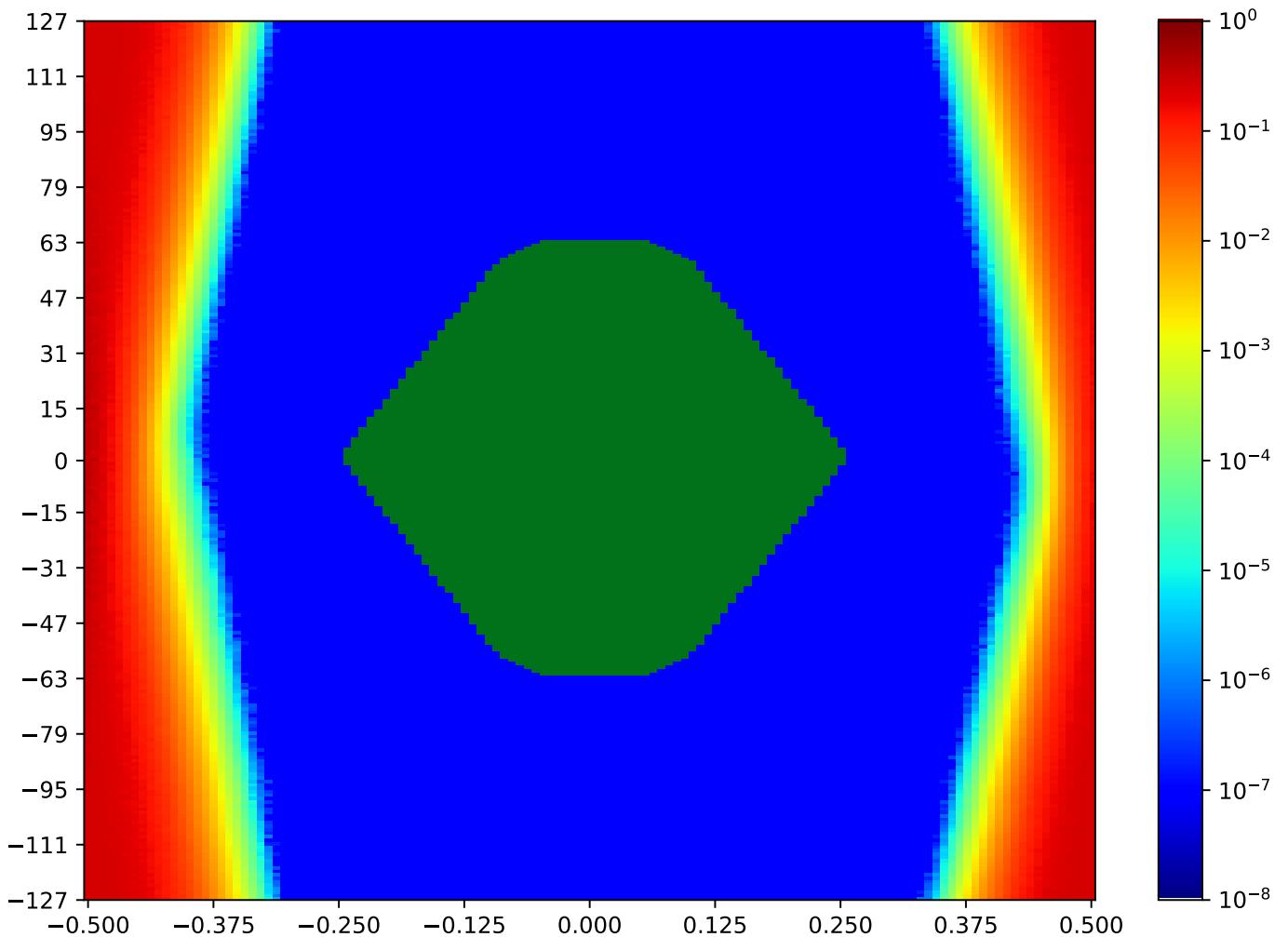


Figure 2.144: MSP_A_FPGA-TX2-03-RX17-03-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.5 MSP_A_FPGA-TX2-04-RX17-04-MSP_C_FPGA

Table 2.134: MSP_A_FPGA-TX2-04-RX17-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:52:51		2018-Jan-24 15:54:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24225	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

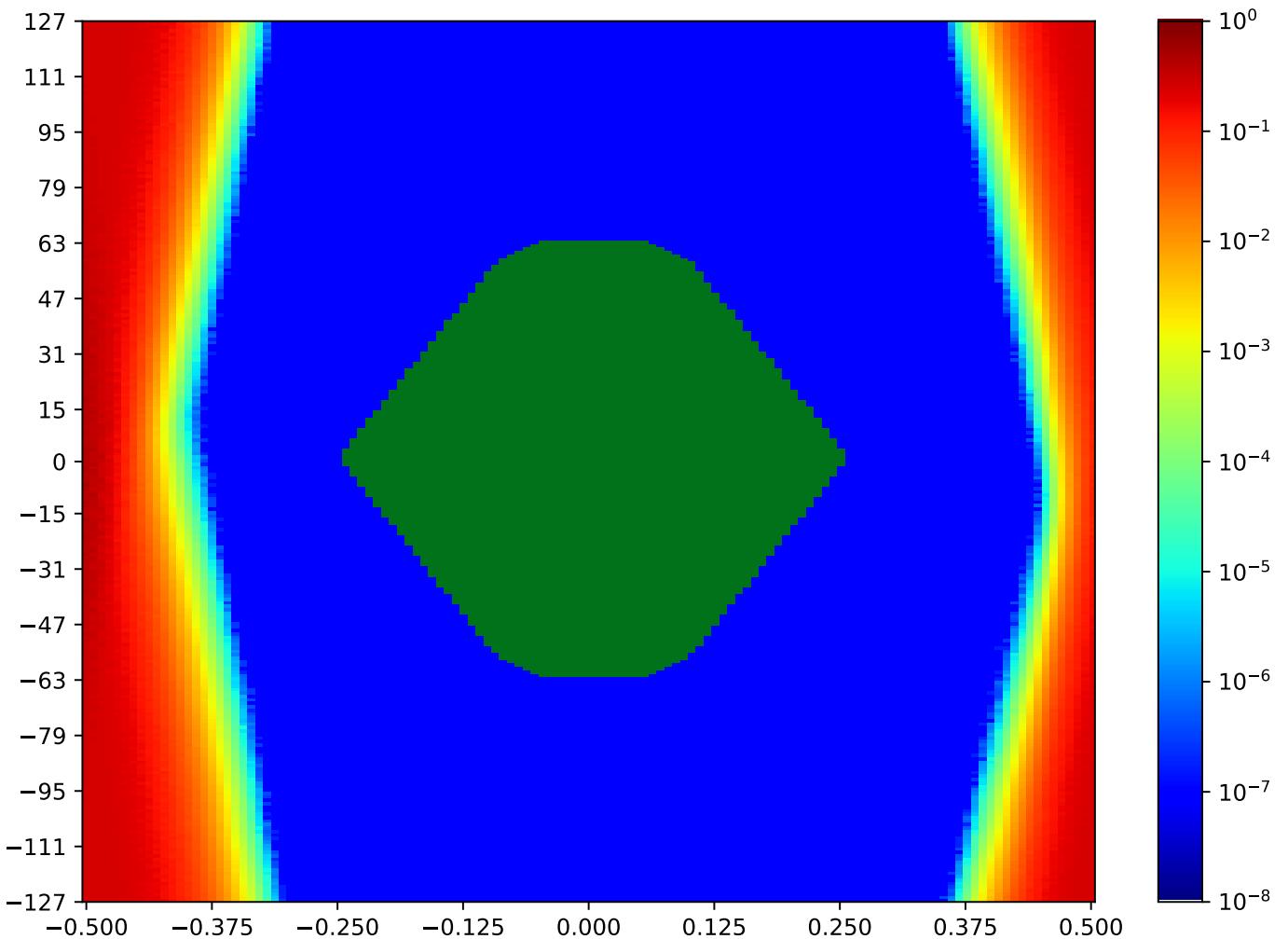


Figure 2.145: MSP_A_FPGA-TX2-04-RX17-04-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.6 MSP_A_FPGA-TX2-05-RX17-05-MSP_C_FPGA

Table 2.135: MSP_A_FPGA-TX2-05-RX17-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:44:36		2018-Jan-24 15:45:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23474	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

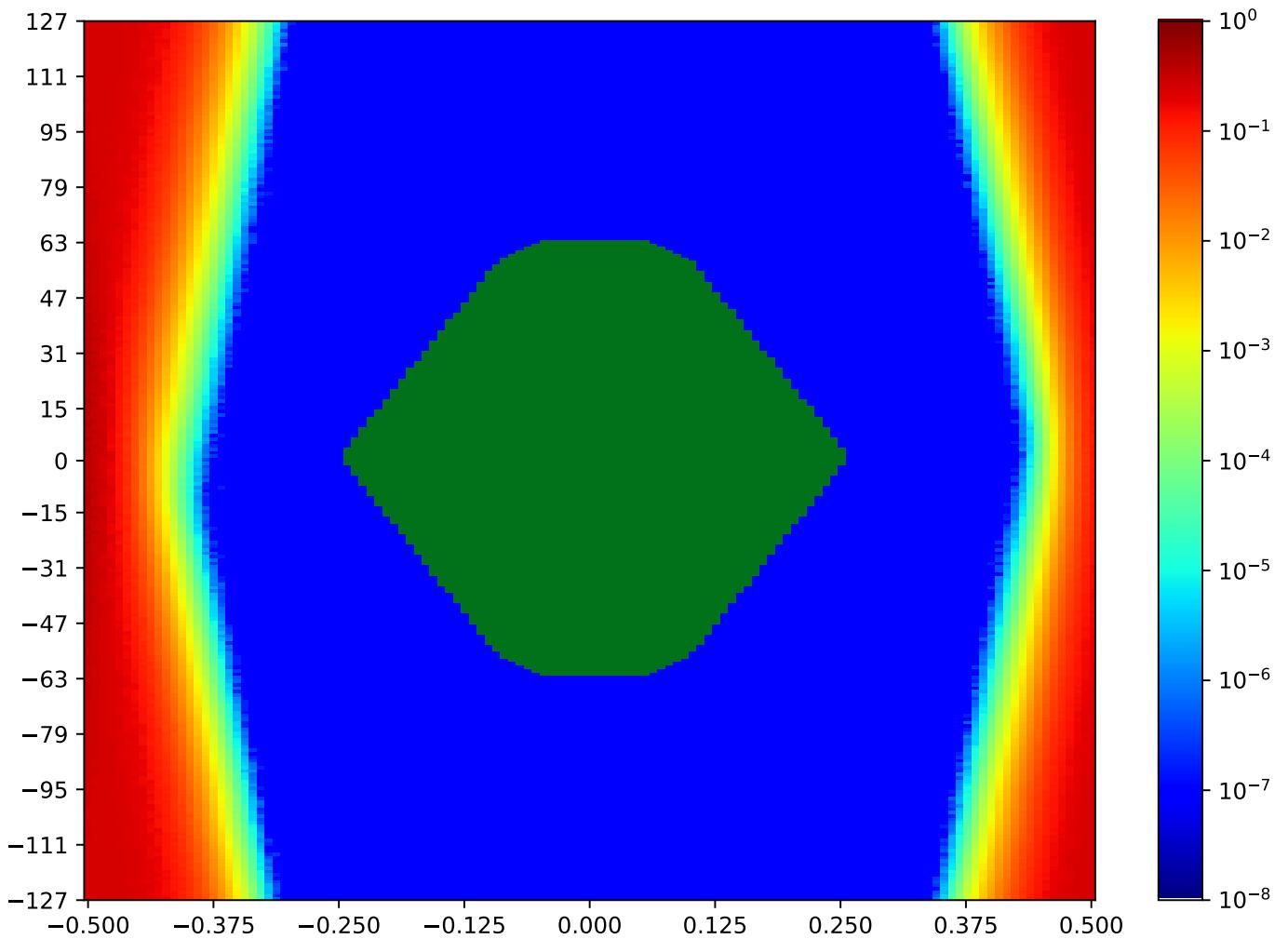


Figure 2.146: MSP_A_FPGA-TX2-05-RX17-05-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.7 MSP_A_FPGA-TX2-06-RX17-06-MSP_C_FPGA

Table 2.136: MSP_A_FPGA-TX2-06-RX17-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:55:11		2018-Jan-24 15:56:23	
Reset RX	OA	HO		HO (%)	
true	24264	105		81.40%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

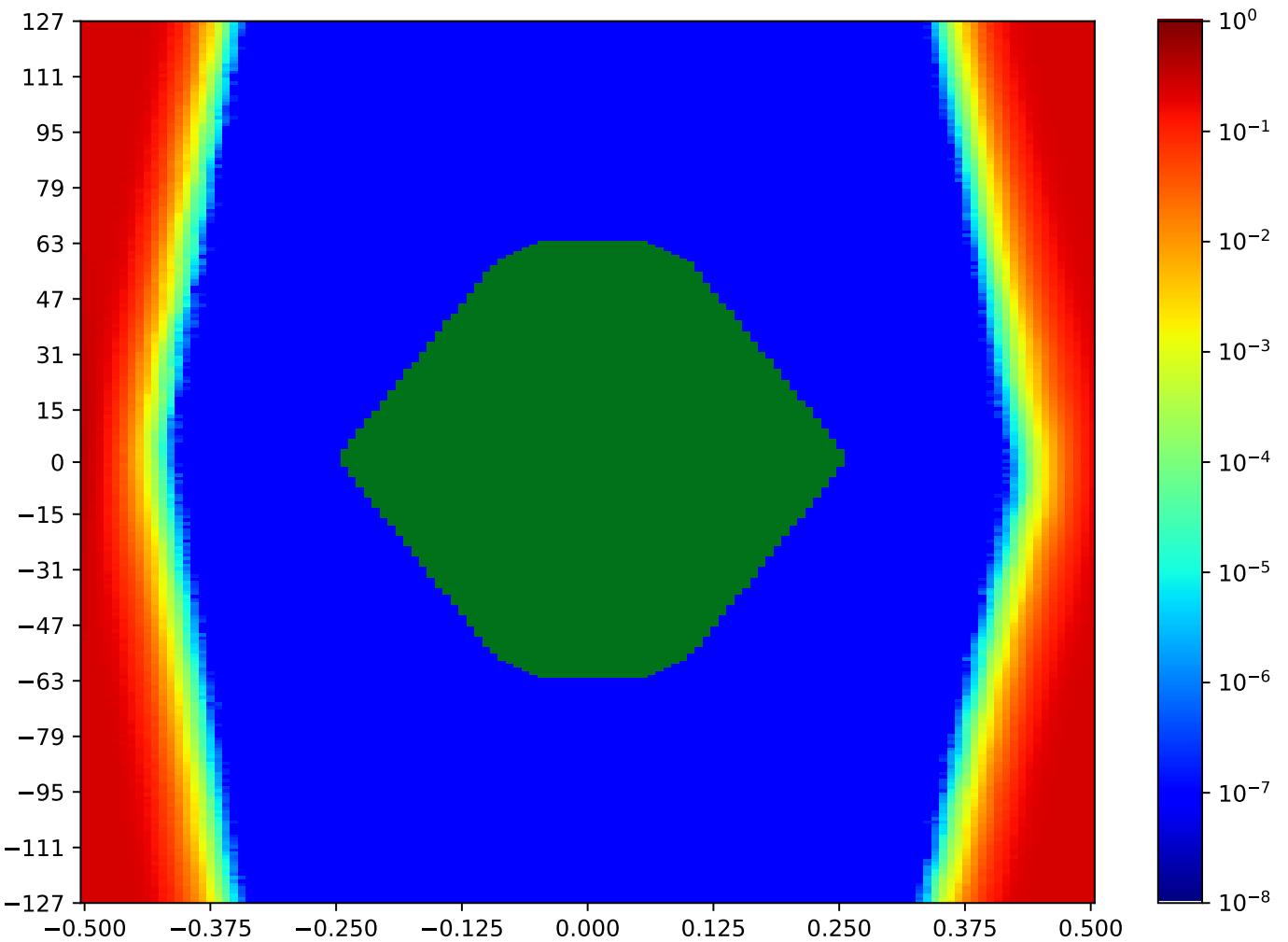


Figure 2.147: MSP_A_FPGA-TX2-06-RX17-06-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.8 MSP_A_FPGA-TX2-07-RX17-07-MSP_C_FPGA

Table 2.137: MSP_A_FPGA-TX2-07-RX17-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:46:57		2018-Jan-24 15:48:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24407	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

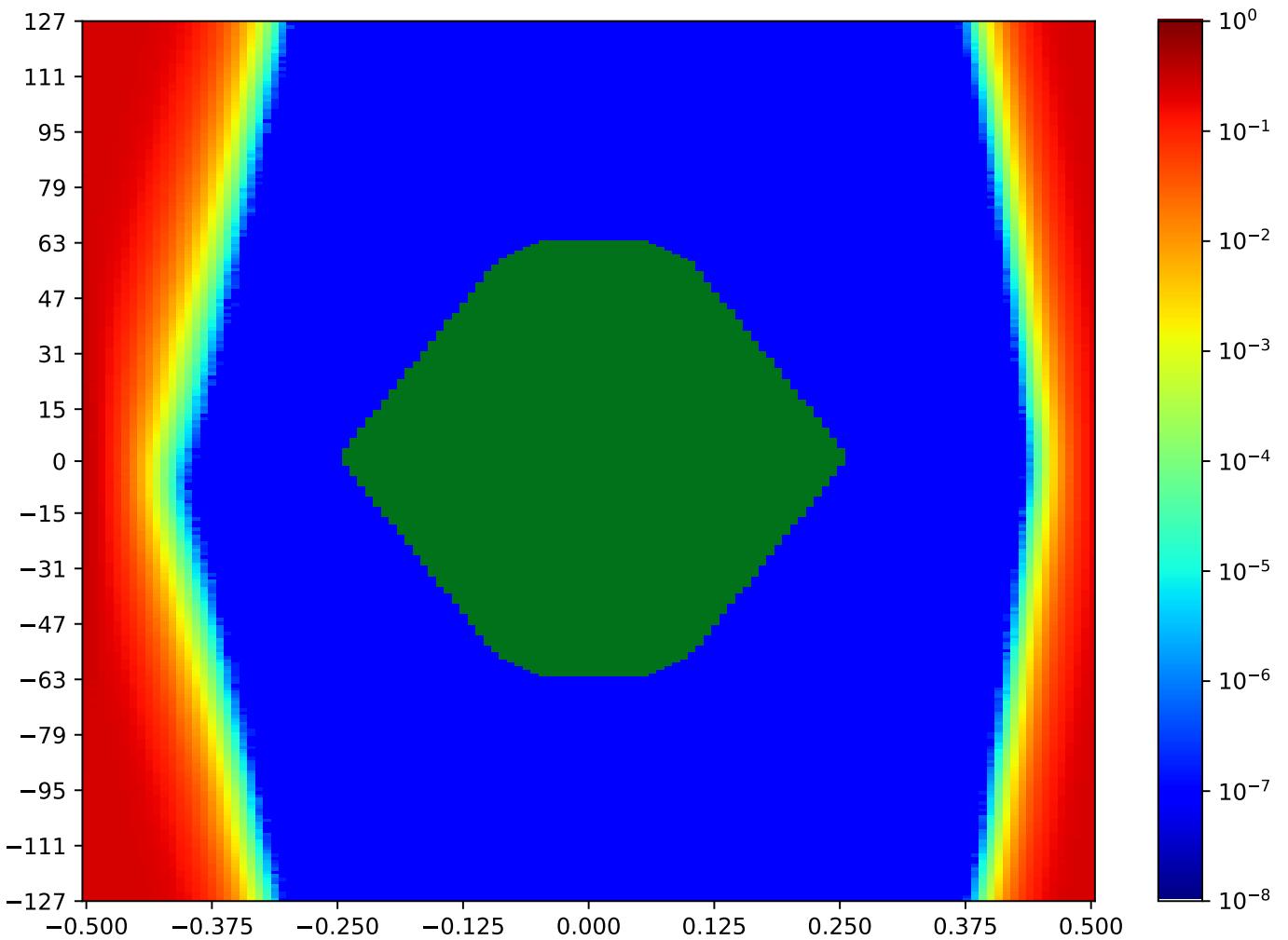


Figure 2.148: MSP_A_FPGA-TX2-07-RX17-07-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.9 MSP_A_FPGA-TX2-08-RX17-08-MSP_C_FPGA

Table 2.138: MSP_A_FPGA-TX2-08-RX17-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:54:01		2018-Jan-24 15:55:11	
Reset RX	OA	HO		HO (%)	
true	24308	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

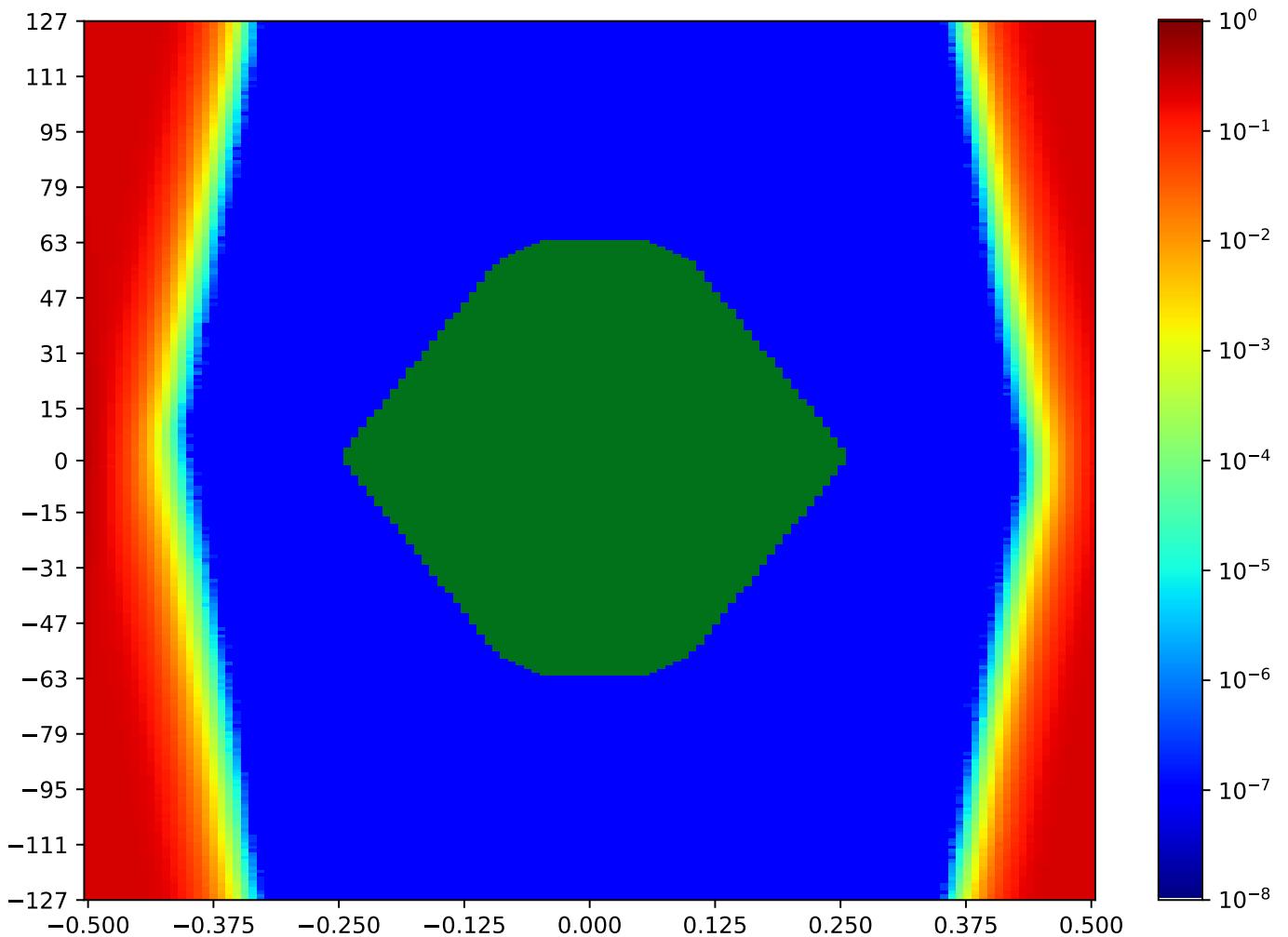


Figure 2.149: MSP_A_FPGA-TX2-08-RX17-08-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.10 MSP_A_FPGA-TX2-09-RX17-09-MSP_C_FPGA

Table 2.139: MSP_A_FPGA-TX2-09-RX17-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:48:07		2018-Jan-24 15:49:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23551	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

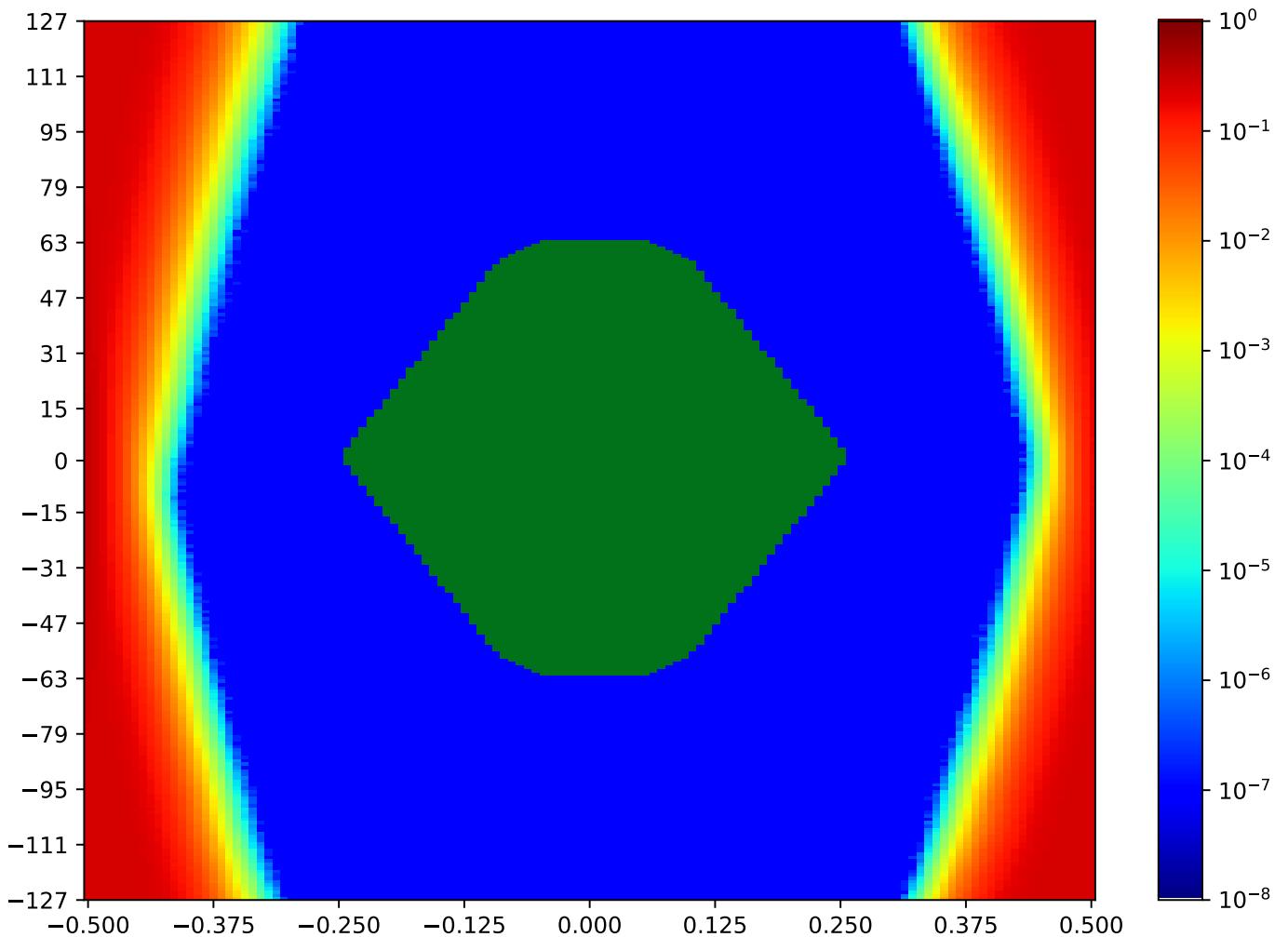


Figure 2.150: MSP_A_FPGA-TX2-09-RX17-09-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.11 MSP_A_FPGA-TX2-10-RX17-10-MSP_C_FPGA

Table 2.140: MSP_A_FPGA-TX2-10-RX17-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:51:38		2018-Jan-24 15:52:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25126	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

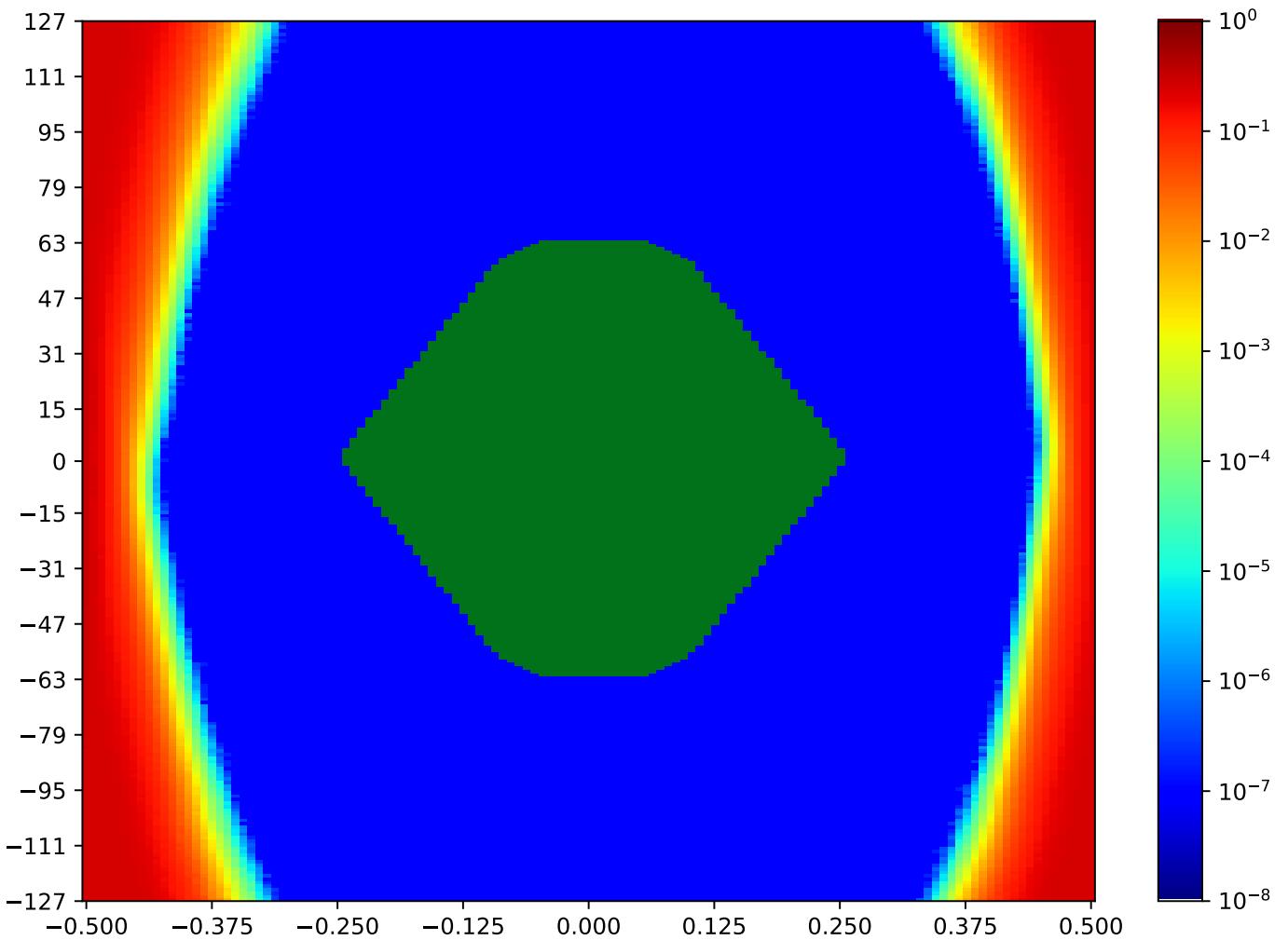


Figure 2.151: MSP_A_FPGA-TX2-10-RX17-10-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.11.12 MSP_A_FPGA-TX2-11-RX17-11-MSP_C_FPGA

Table 2.141: MSP_A_FPGA-TX2-11-RX17-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:50:27		2018-Jan-24 15:51:38	
Reset RX	OA	HO		HO (%)	
true	24326	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

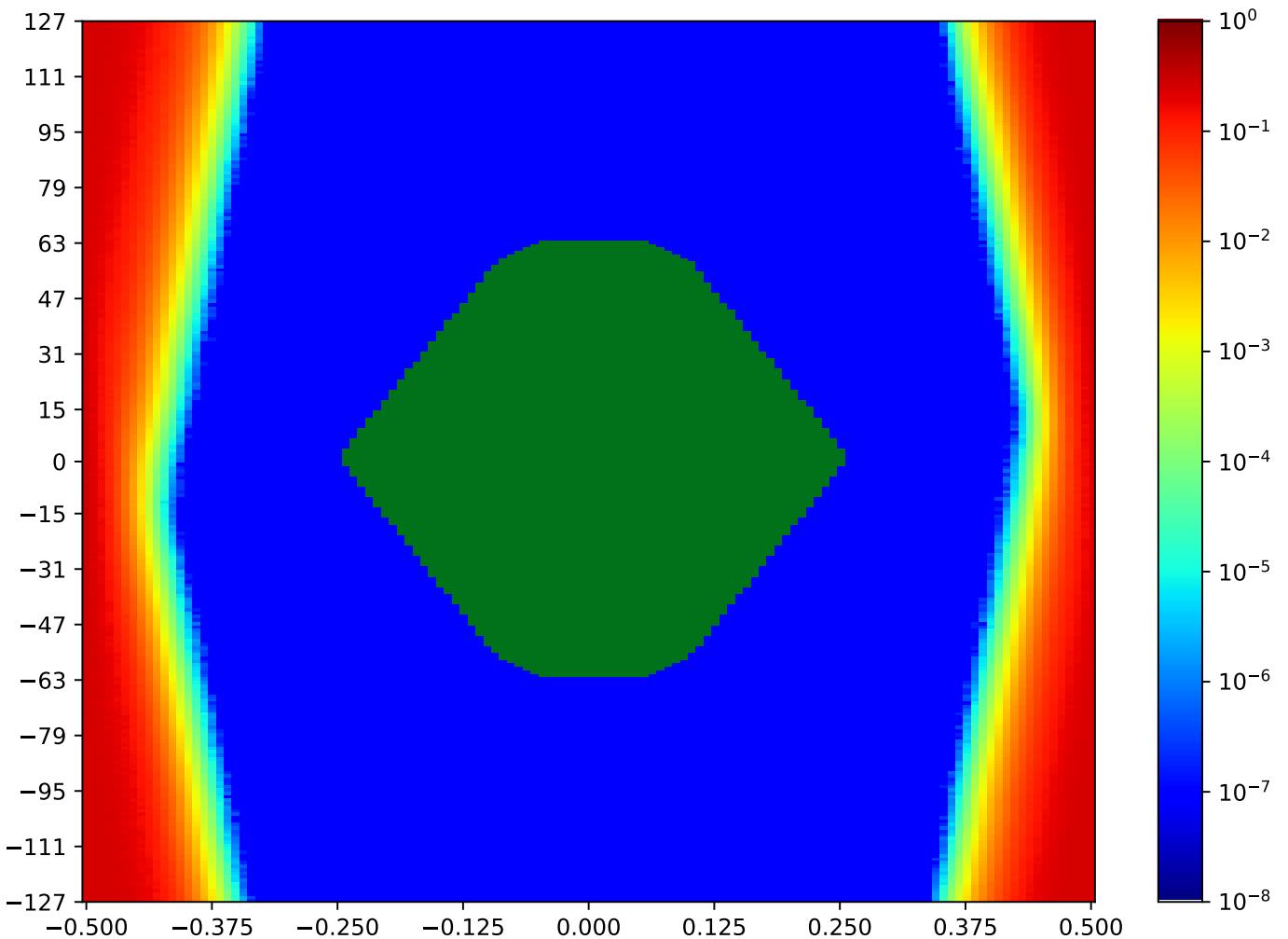


Figure 2.152: MSP_A_FPGA-TX2-11-RX17-11-MSP_C_FPGA

Call back to summary Figure 2.140. Sibling eye diagrams: V1-12.8.

2.12 MSP_C TX3 MSP_A RX9 Minipod Loopback

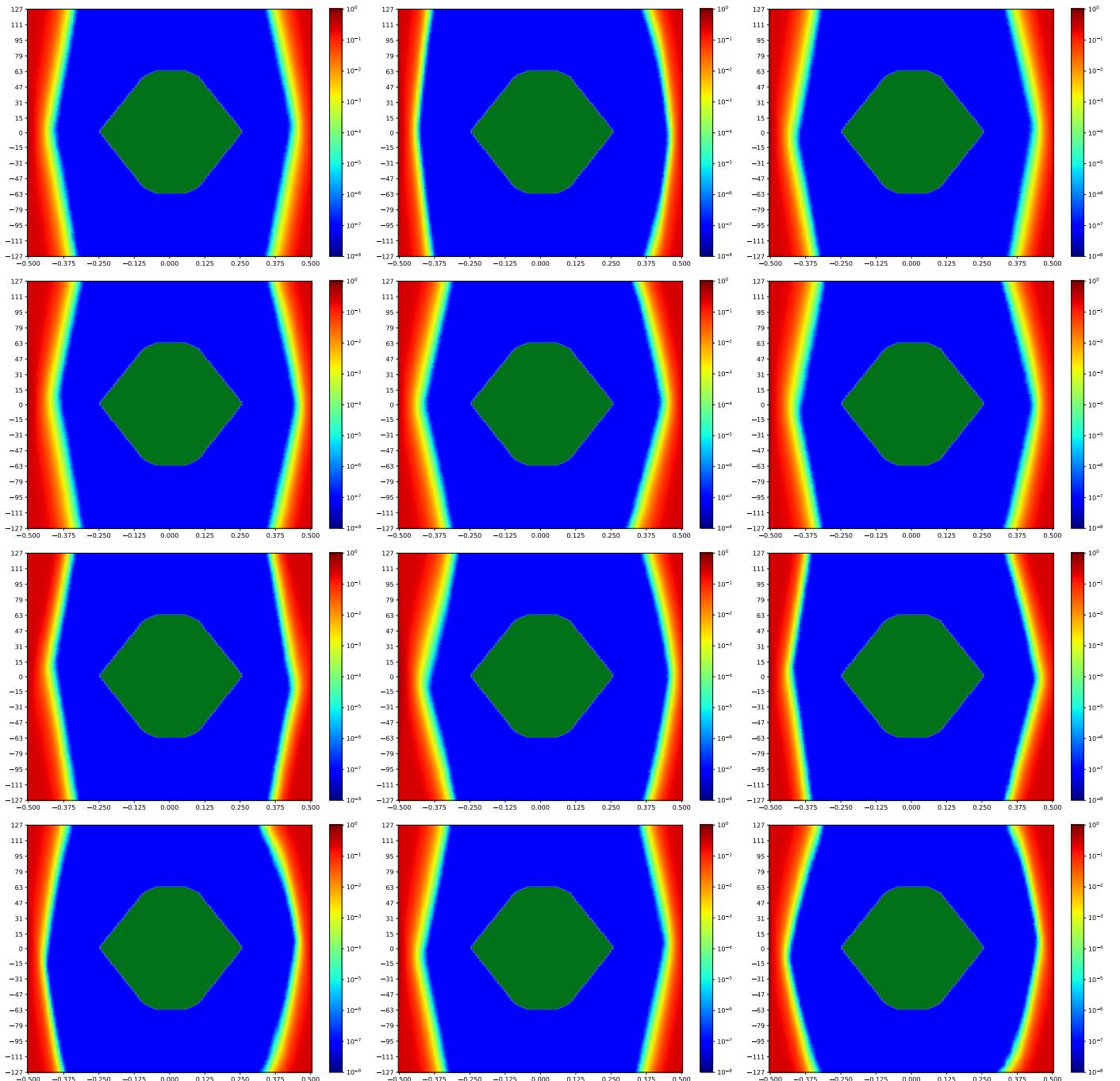


Figure 2.153: MSP_C TX3 MSP_A RX9 Minipod Loopback

A cross-reference to Figure 2.153. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.166.

2.12.1 MSP_C_FPGA-TX3-00-RX9-00-MSP_A_FPGA

Table 2.142: MSP_C_FPGA-TX3-00-RX9-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:59:53		2018-Jan-24 16:01:04	
Reset RX	OA	HO		HO (%)	
true	23958	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

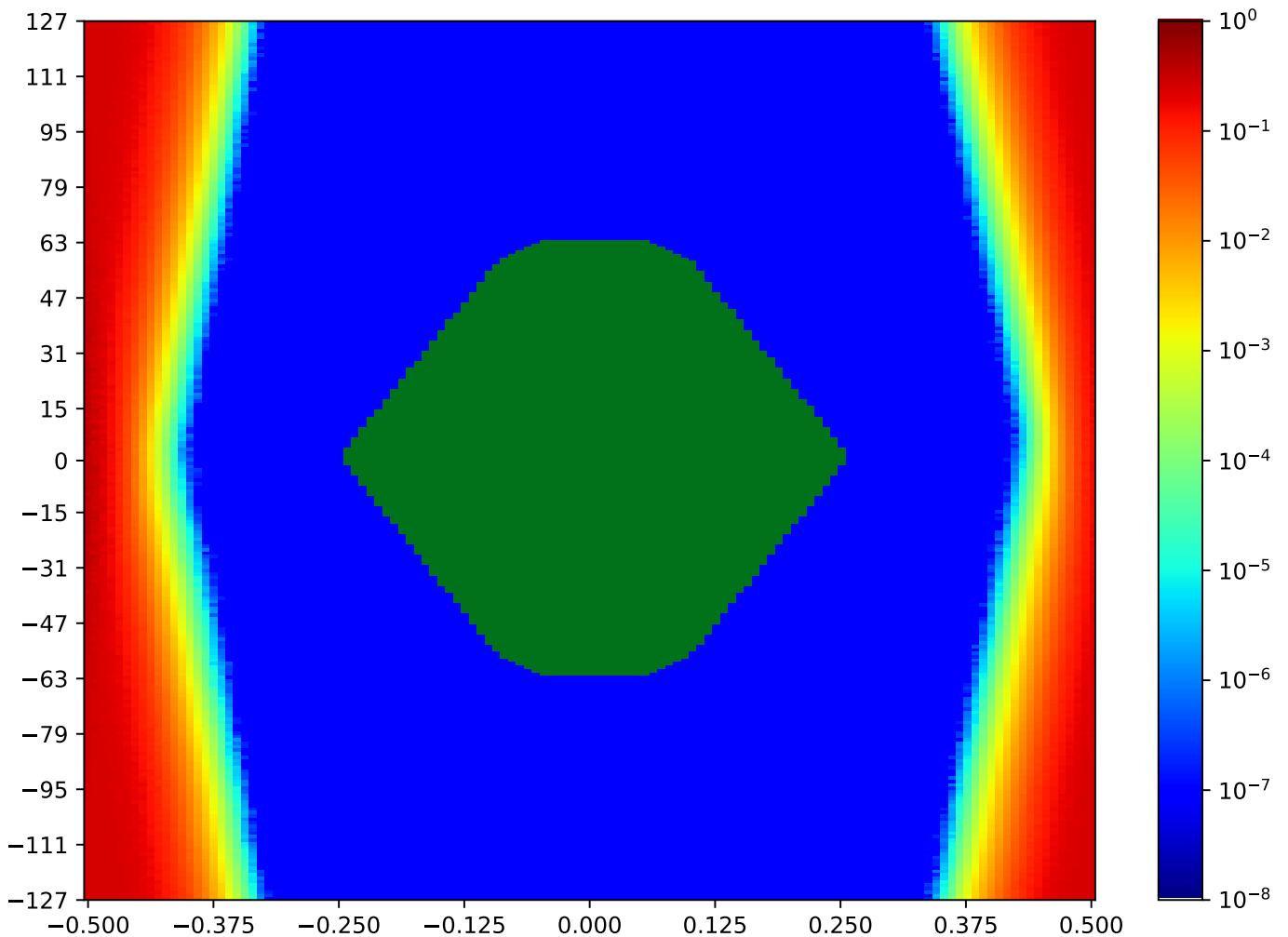


Figure 2.154: MSP_C_FPGA-TX3-00-RX9-00-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.2 MSP_C_FPGA-TX3-01-RX9-01-MSP_A_FPGA

Table 2.143: MSP_C_FPGA-TX3-01-RX9-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:02:15		2018-Jan-24 16:03:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26307	111	86.05%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

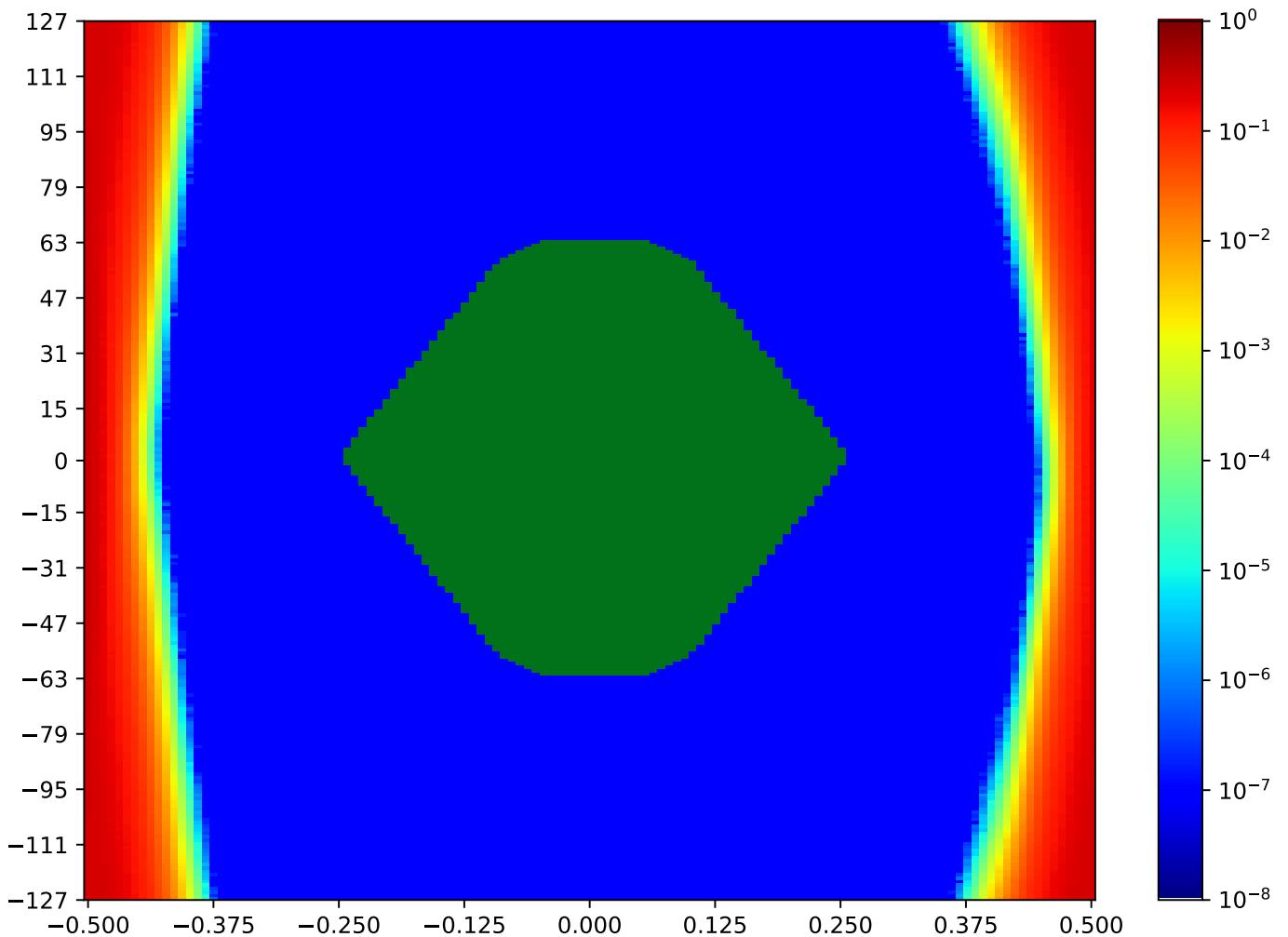


Figure 2.155: MSP_C_FPGA-TX3-01-RX9-01-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.3 MSP_C_FPGA-TX3-02-RX9-02-MSP_A_FPGA

Table 2.144: MSP_C_FPGA-TX3-02-RX9-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:03:27		2018-Jan-24 16:04:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23633	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

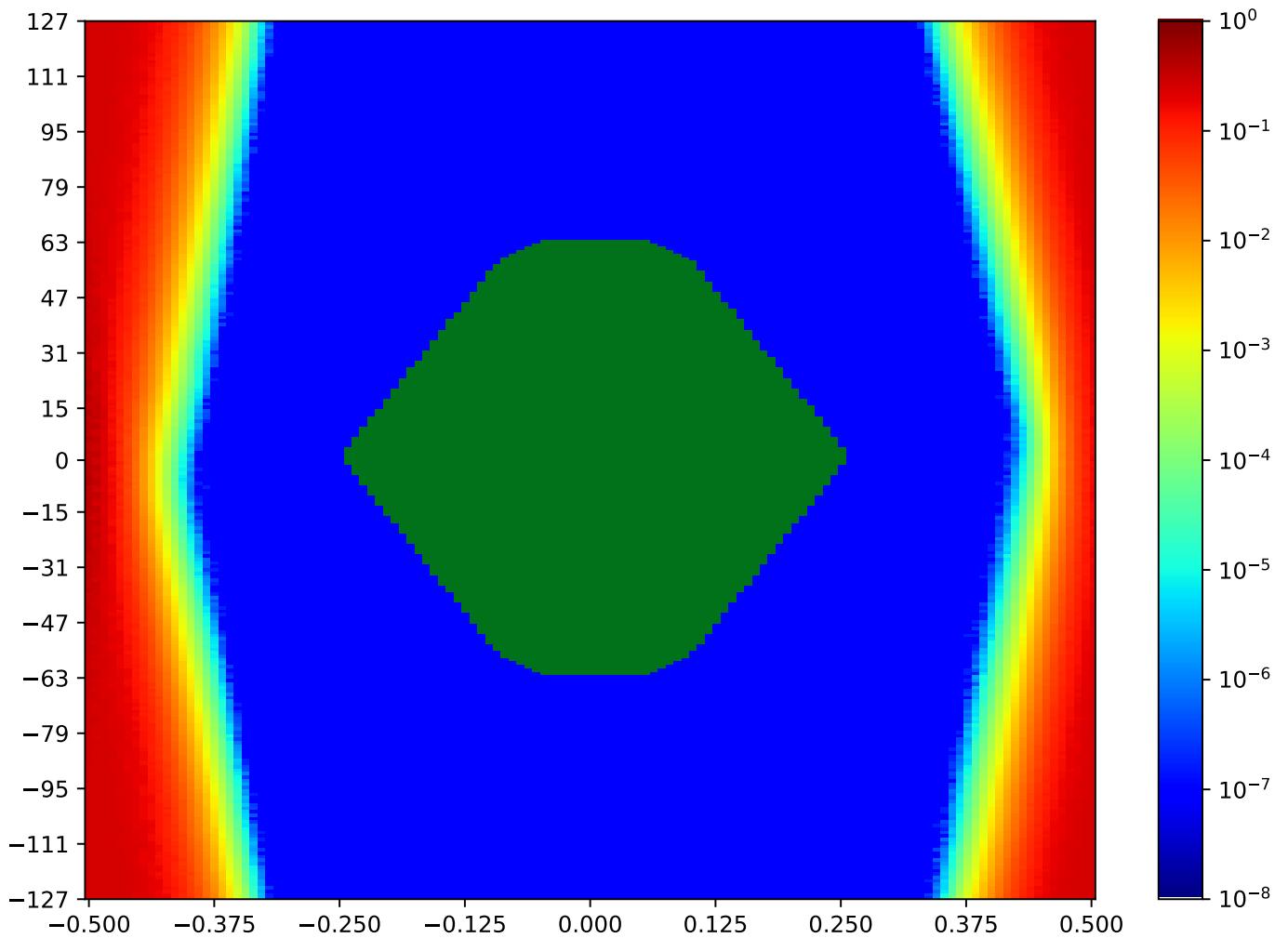


Figure 2.156: MSP_C_FPGA-TX3-02-RX9-02-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.4 MSP_C_FPGA-TX3-03-RX9-03-MSP_A_FPGA

Table 2.145: MSP_C_FPGA-TX3-03-RX9-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:57:33		2018-Jan-24 15:58:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23780	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

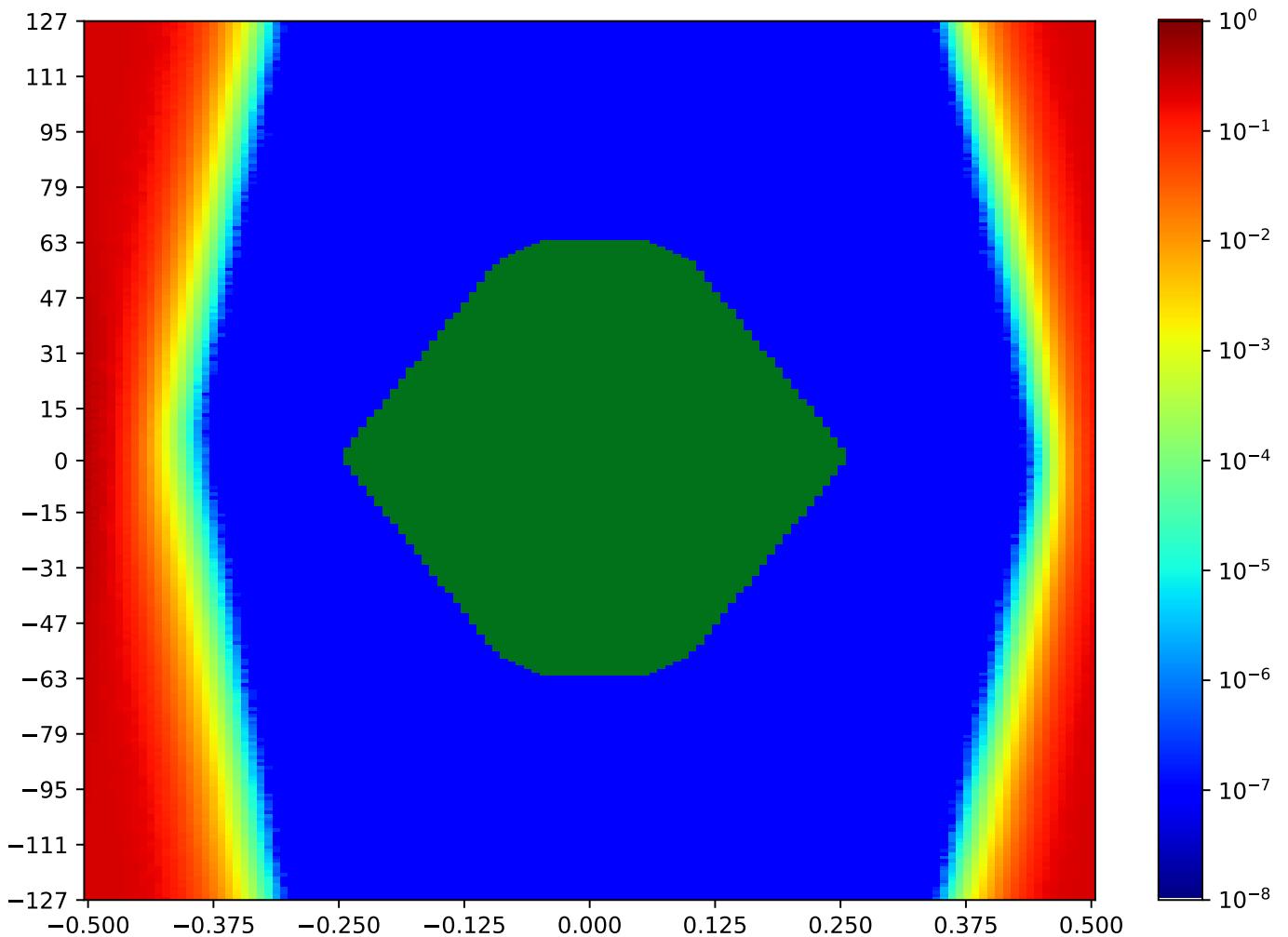


Figure 2.157: MSP_C_FPGA-TX3-03-RX9-03-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.5 MSP_C_FPGA-TX3-04-RX9-04-MSP_A_FPGA

Table 2.146: MSP_C_FPGA-TX3-04-RX9-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:06:57		2018-Jan-24 16:08:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23296	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

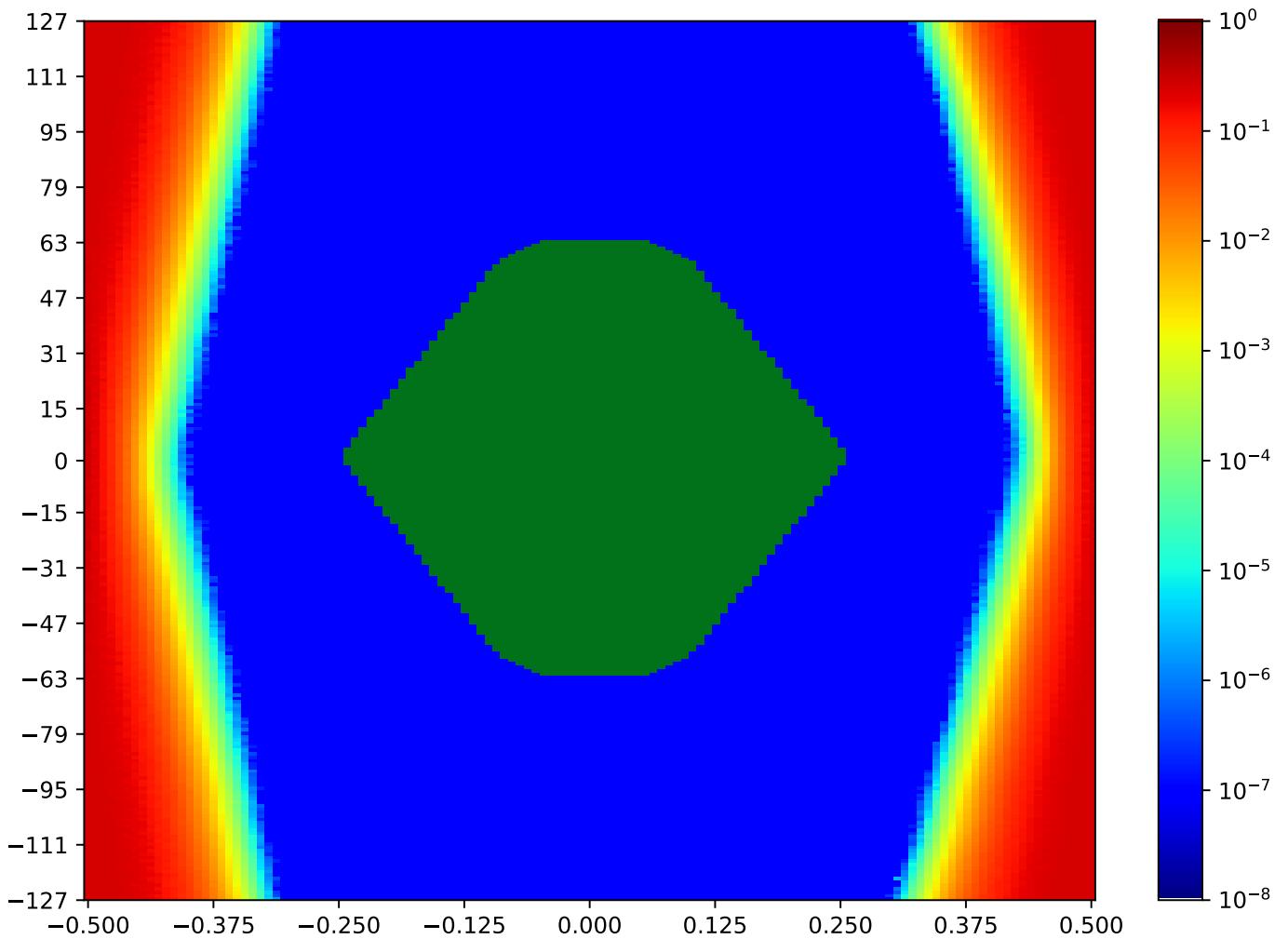


Figure 2.158: MSP_C_FPGA-TX3-04-RX9-04-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.6 MSP_C_FPGA-TX3-05-RX9-05-MSP_A_FPGA

Table 2.147: MSP_C_FPGA-TX3-05-RX9-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:56:23		2018-Jan-24 15:57:33	
Reset RX	OA	HO		HO (%)	
true	23205	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

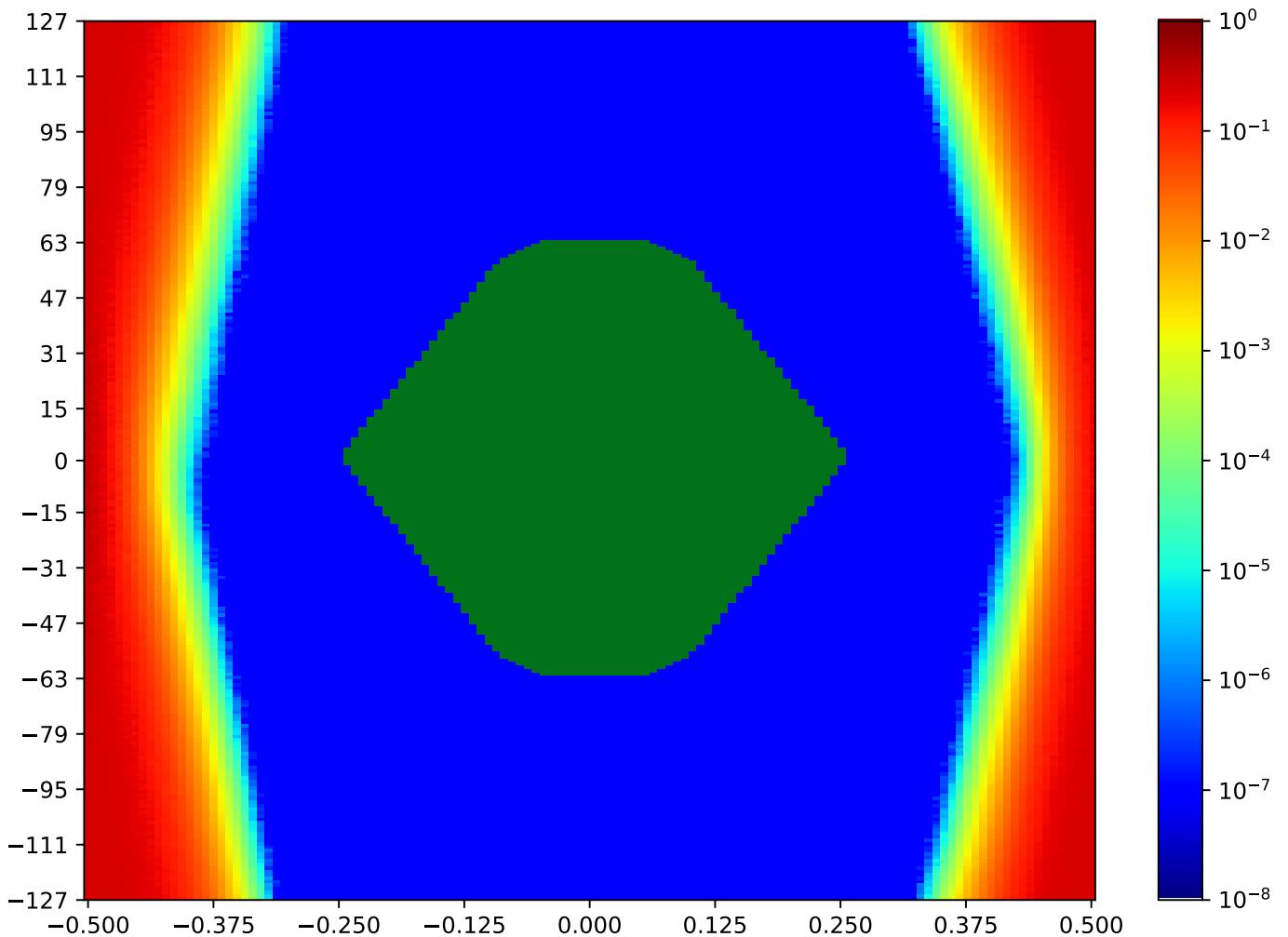


Figure 2.159: MSP_C_FPGA-TX3-05-RX9-05-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.7 MSP_C_FPGA-TX3-06-RX9-06-MSP_A_FPGA

Table 2.148: MSP_C_FPGA-TX3-06-RX9-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:09:17		2018-Jan-24 16:10:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24025	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

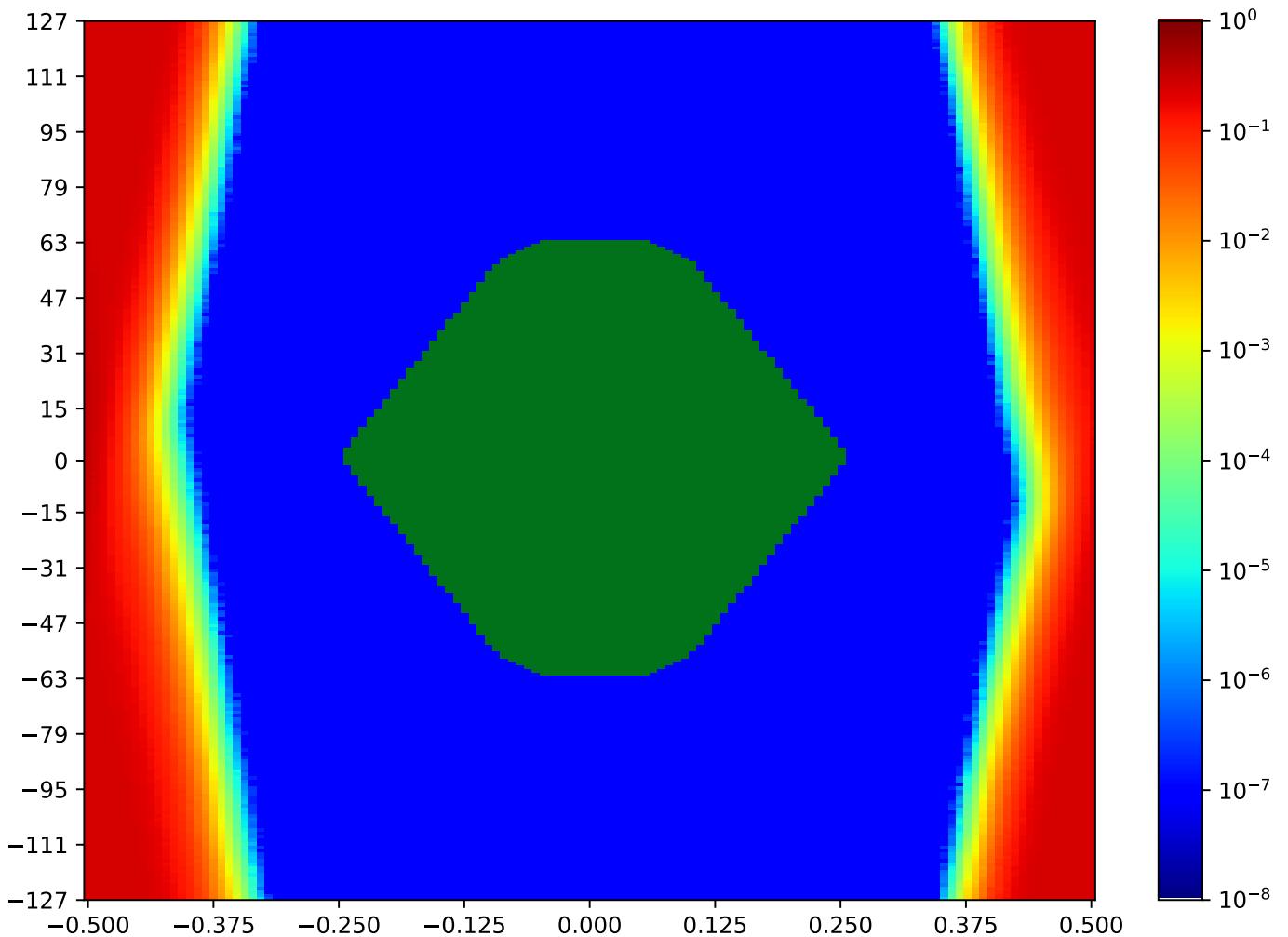


Figure 2.160: MSP_C_FPGA-TX3-06-RX9-06-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.8 MSP_C_FPGA-TX3-07-RX9-07-MSP_A_FPGA

Table 2.149: MSP_C_FPGA-TX3-07-RX9-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 15:58:43		2018-Jan-24 15:59:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24012	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

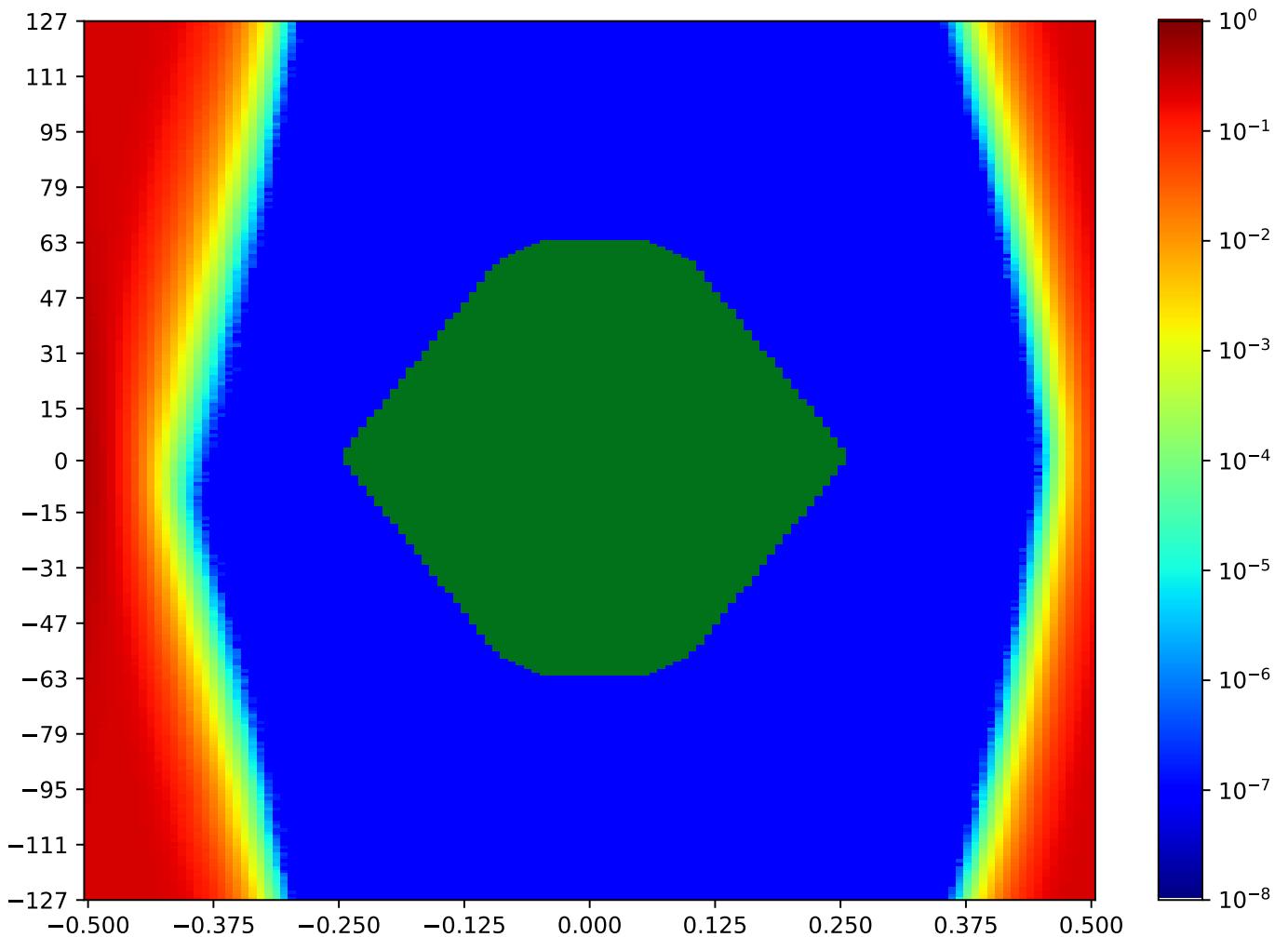


Figure 2.161: MSP_C_FPGA-TX3-07-RX9-07-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.9 MSP_C_FPGA-TX3-08-RX9-08-MSP_A_FPGA

Table 2.150: MSP_C_FPGA-TX3-08-RX9-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:08:08		2018-Jan-24 16:09:17	
Reset RX	OA	HO		VO VO (%)	
true	24620	106		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

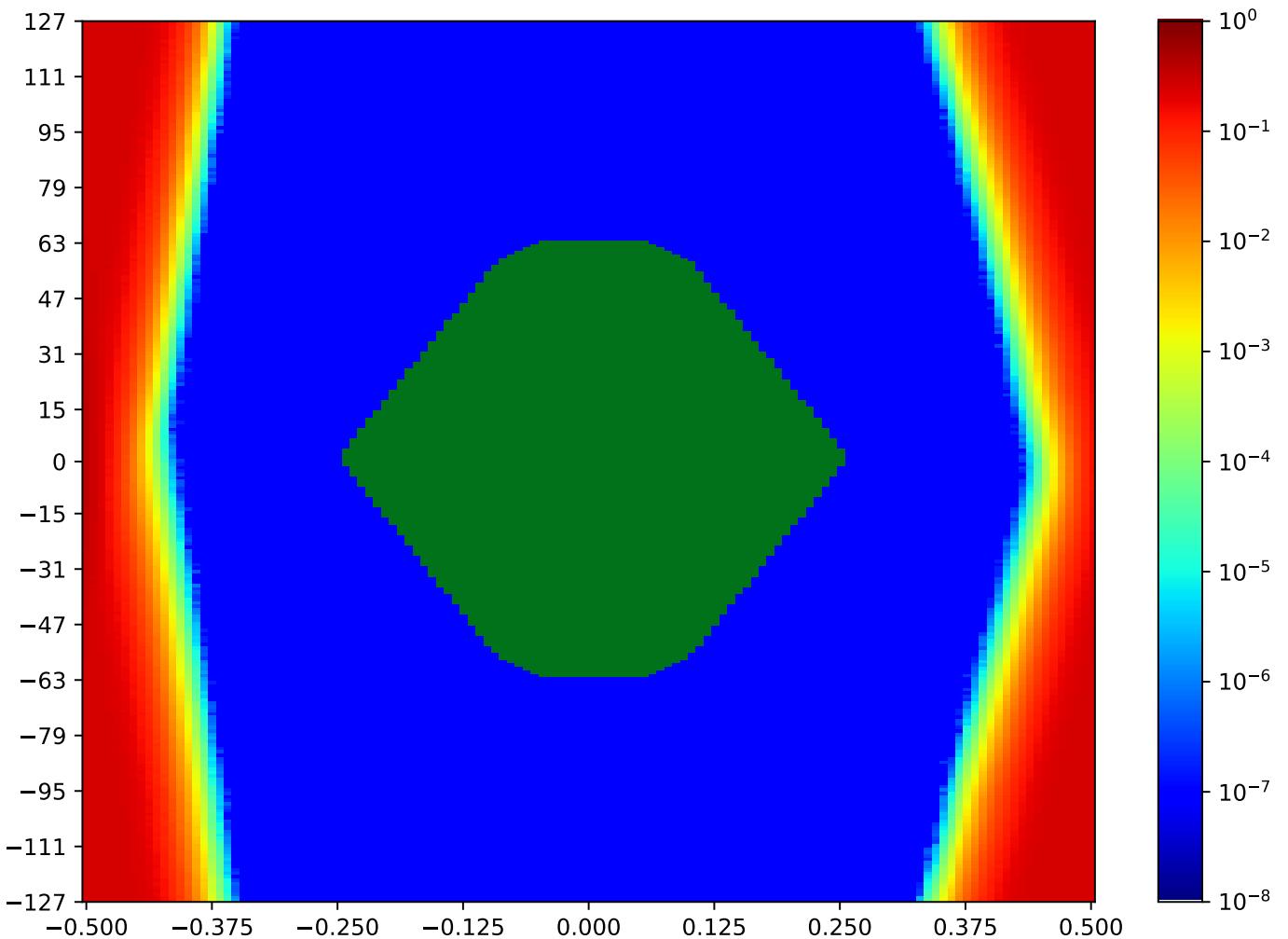


Figure 2.162: MSP_C_FPGA-TX3-08-RX9-08-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.10 MSP_C_FPGA-TX3-09-RX9-09-MSP_A_FPGA

Table 2.151: MSP_C_FPGA-TX3-09-RX9-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:01:04		2018-Jan-24 16:02:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25363	110	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

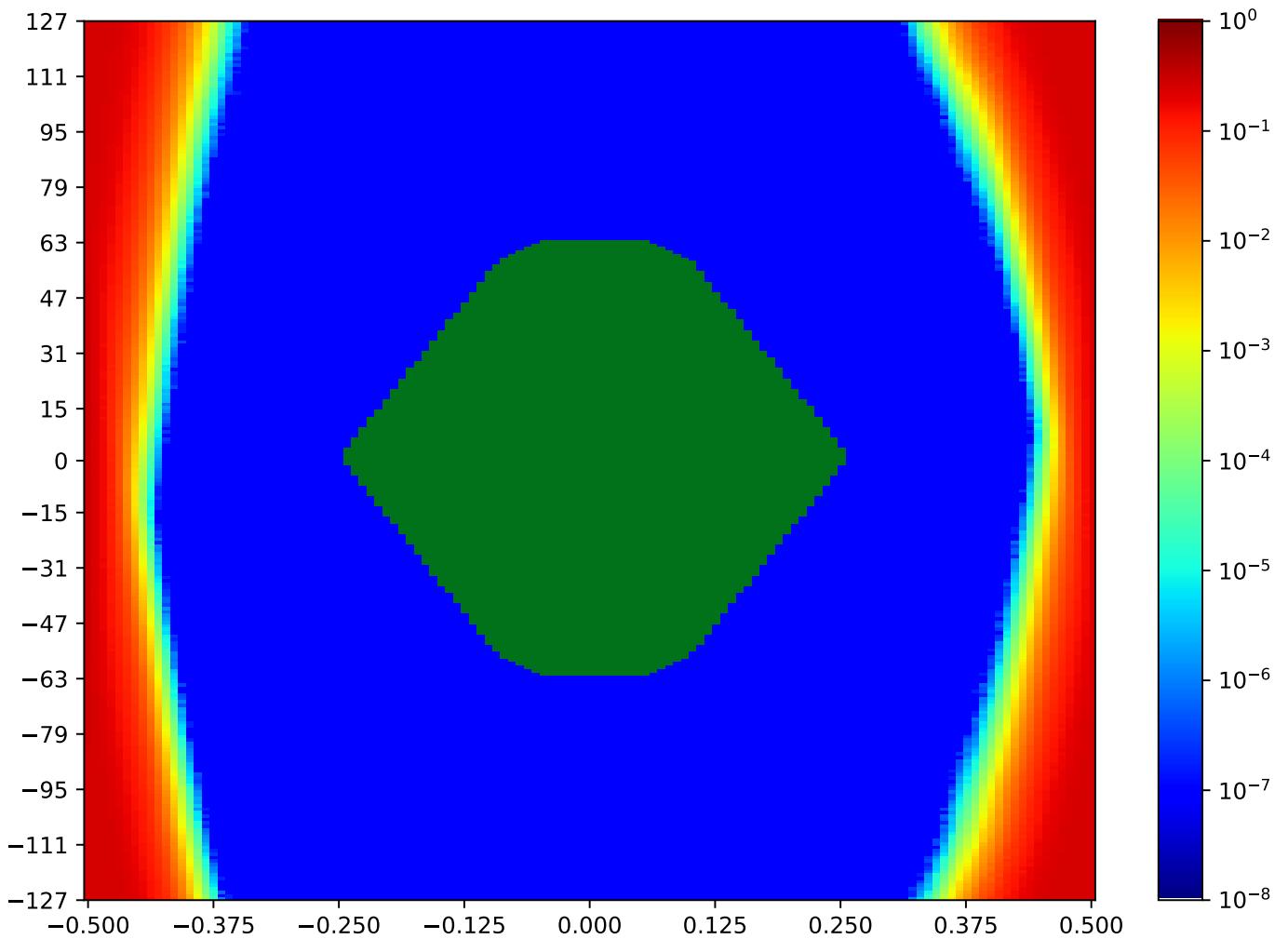


Figure 2.163: MSP_C_FPGA-TX3-09-RX9-09-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.11 MSP_C_FPGA-TX3-10-RX9-10-MSP_A_FPGA

Table 2.152: MSP_C_FPGA-TX3-10-RX9-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:05:47		2018-Jan-24 16:06:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24122	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

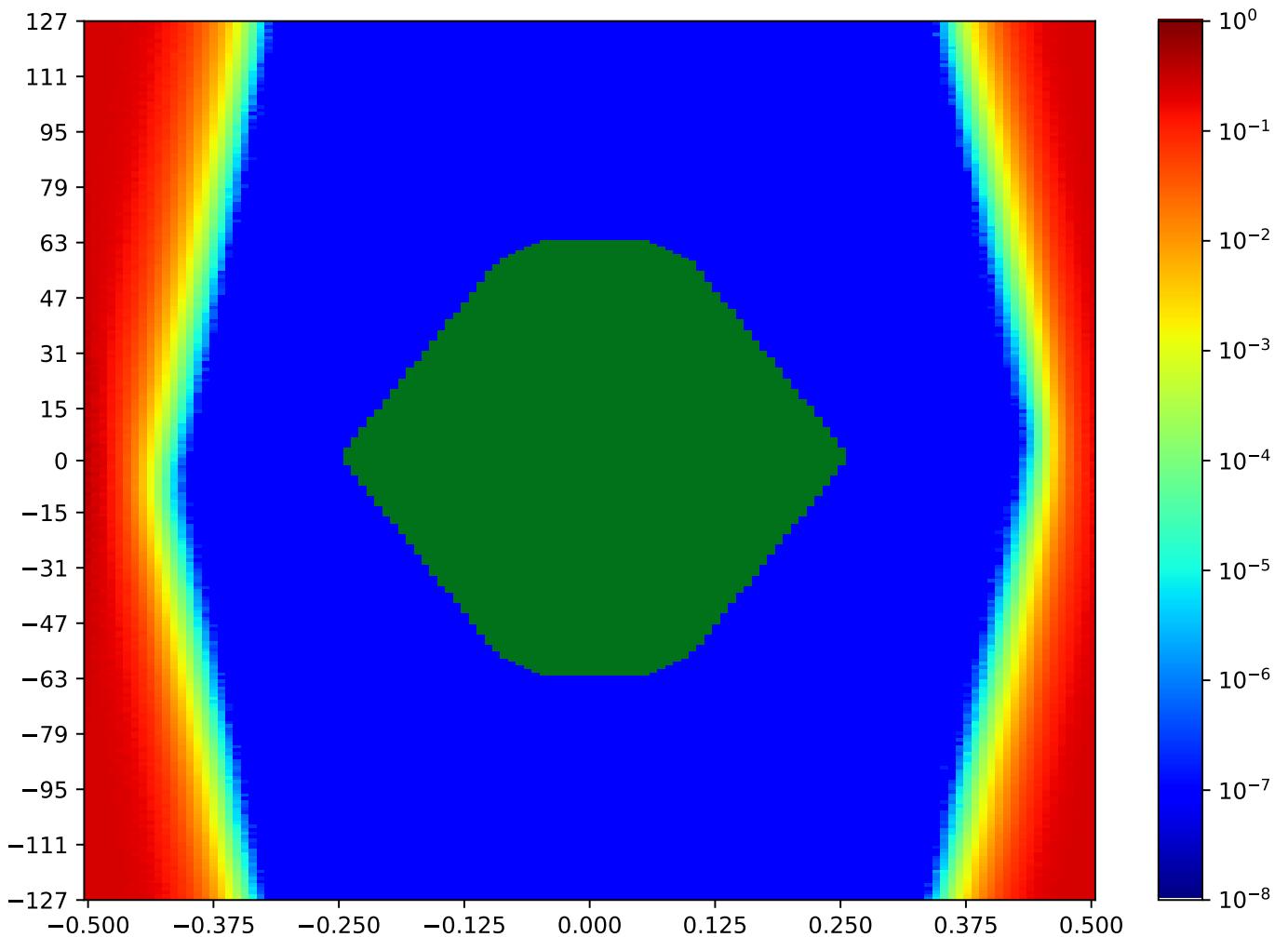


Figure 2.164: MSP_C_FPGA-TX3-10-RX9-10-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.12.12 MSP_C_FPGA-TX3-11-RX9-11-MSP_A_FPGA

Table 2.153: MSP_C_FPGA-TX3-11-RX9-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:04:36		2018-Jan-24 16:05:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24800	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

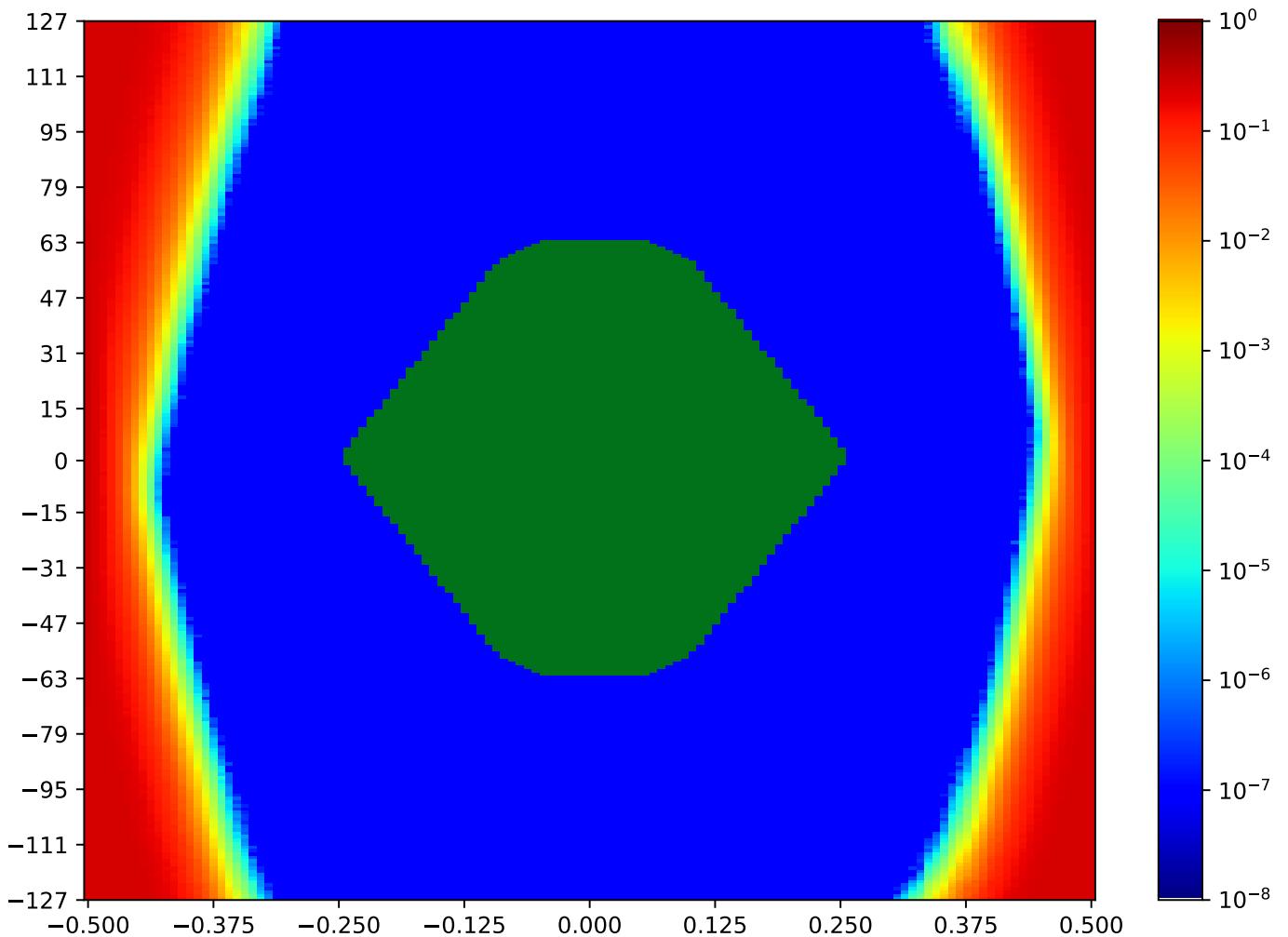


Figure 2.165: MSP_C_FPGA-TX3-11-RX9-11-MSP_A_FPGA

Call back to summary Figure 2.153. Sibling eye diagrams: V1-12.8.

2.13 MSP_C TX4 MSP_A RX8 Minipod Loopback

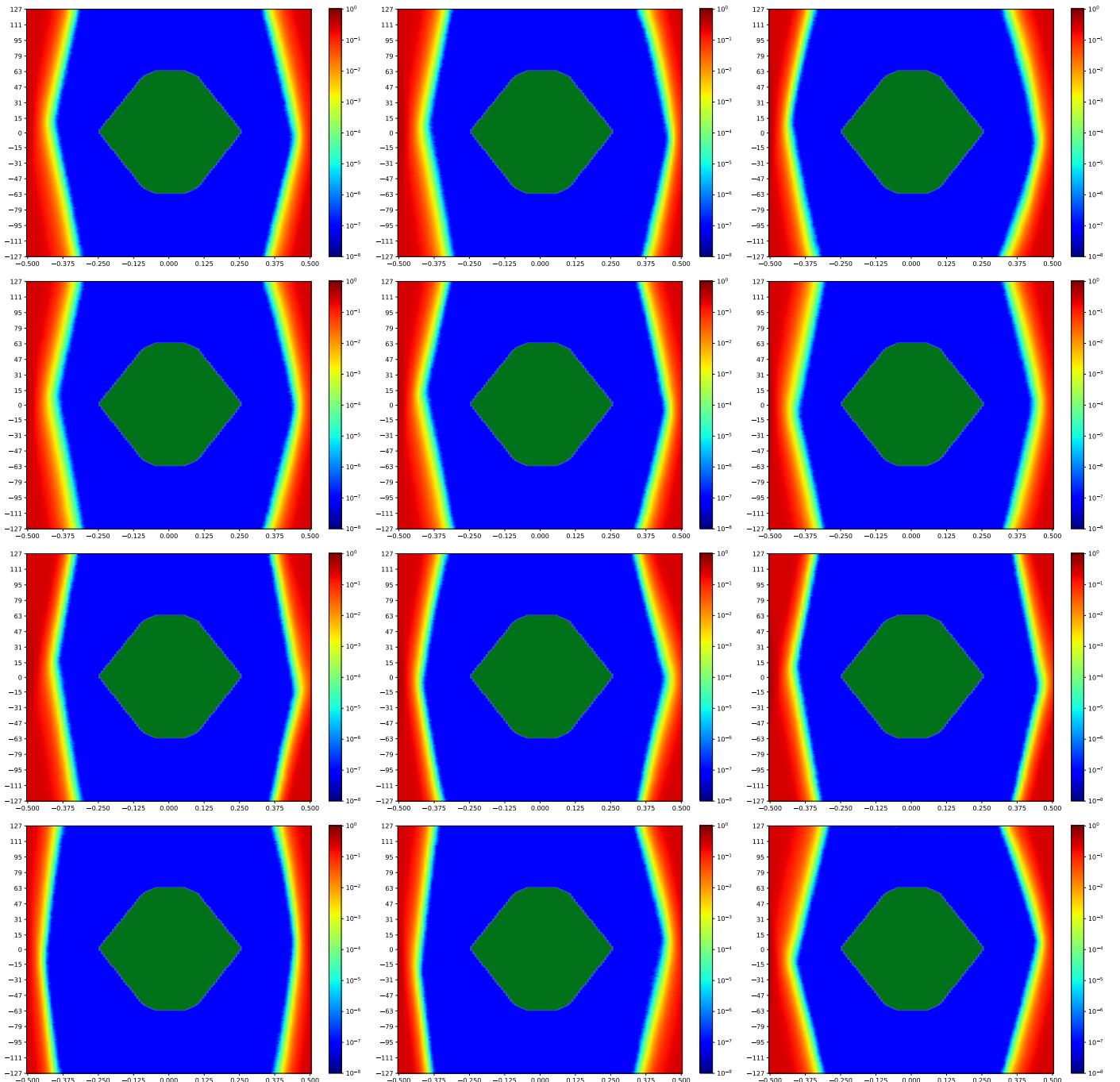


Figure 2.166: MSP_C TX4 MSP_A RX8 Minipod Loopback

A cross-reference to Figure 2.166. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.179.

2.13.1 MSP_C_FPGA-TX4-00-RX8-00-MSP_A_FPGA

Table 2.154: MSP_C_FPGA-TX4-00-RX8-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:13:55		2018-Jan-24 16:15:04	
Reset RX	OA	HO		HO (%)	
true	23614	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

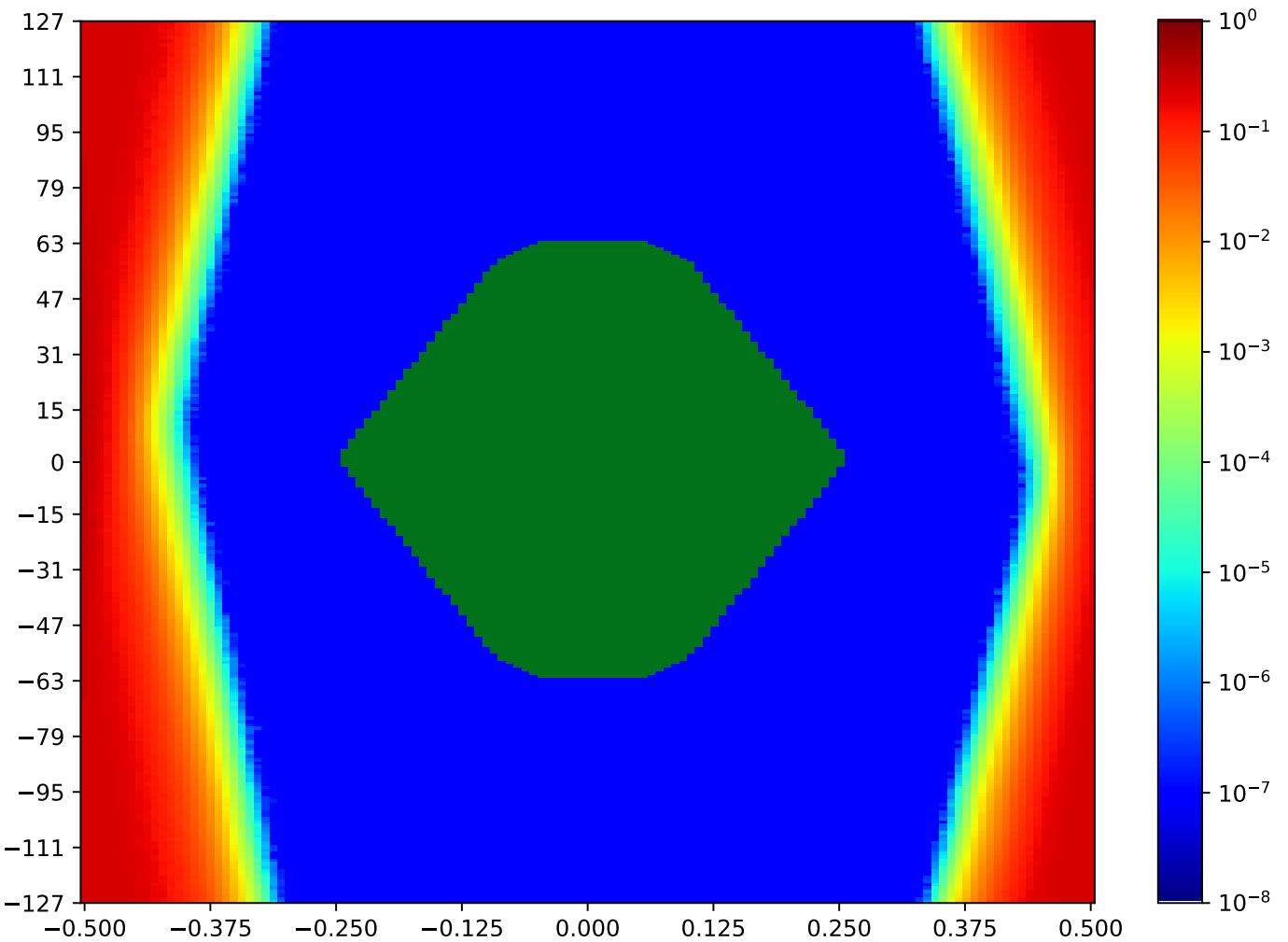


Figure 2.167: MSP_C_FPGA-TX4-00-RX8-00-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.2 MSP_C_FPGA-TX4-01-RX8-01-MSP_A_FPGA

Table 2.155: MSP_C_FPGA-TX4-01-RX8-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:11:36		2018-Jan-24 16:12:46	
Reset RX	OA	HO		HO (%)	
true	23971	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

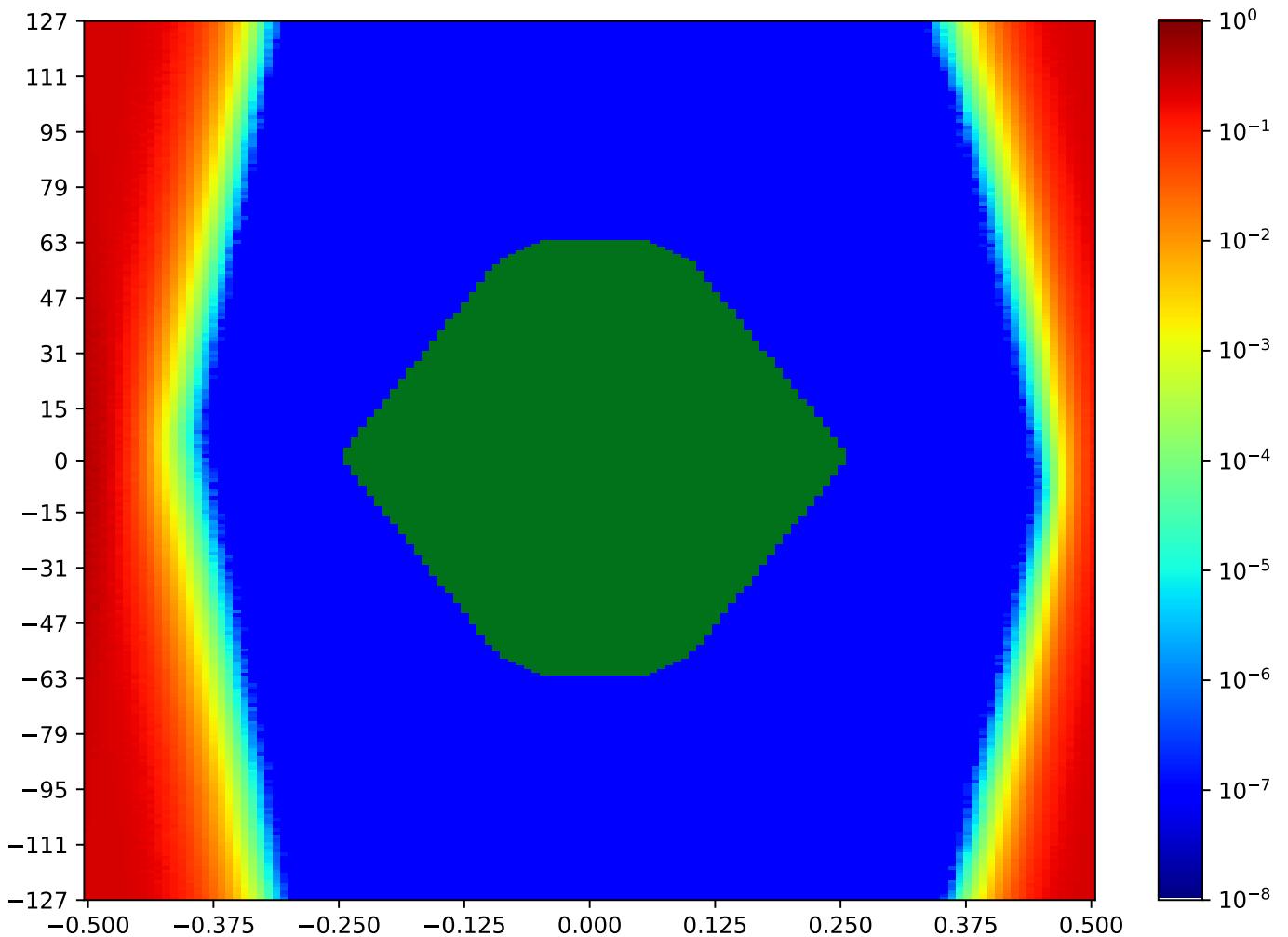


Figure 2.168: MSP_C_FPGA-TX4-01-RX8-01-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.3 MSP_C_FPGA-TX4-02-RX8-02-MSP_A_FPGA

Table 2.156: MSP_C_FPGA-TX4-02-RX8-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:17:28		2018-Jan-24 16:18:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24149	106	82.17%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

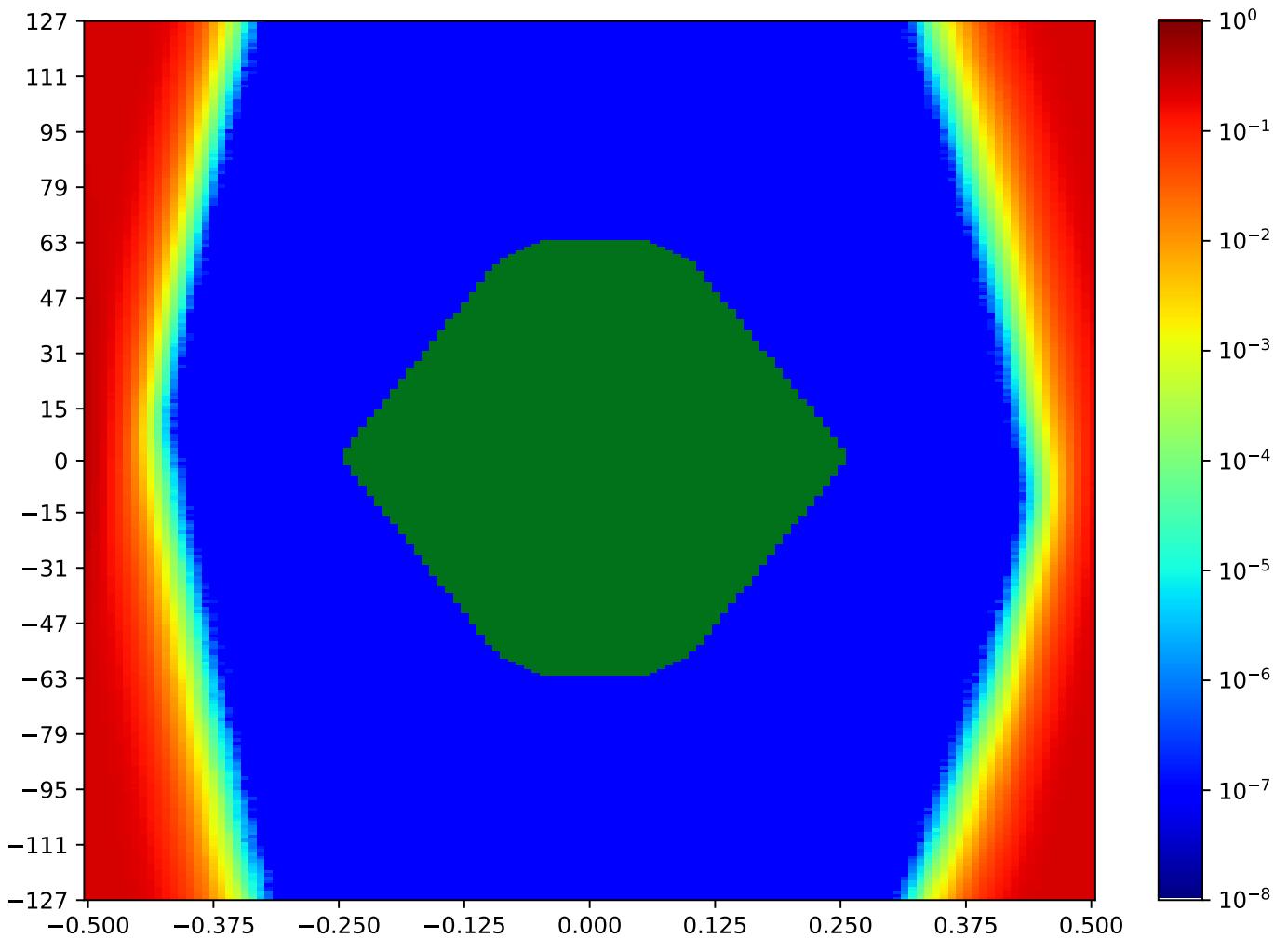


Figure 2.169: MSP_C_FPGA-TX4-02-RX8-02-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.4 MSP_C_FPGA-TX4-03-RX8-03-MSP_A_FPGA

Table 2.157: MSP_C_FPGA-TX4-03-RX8-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:10:27		2018-Jan-24 16:11:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23407	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

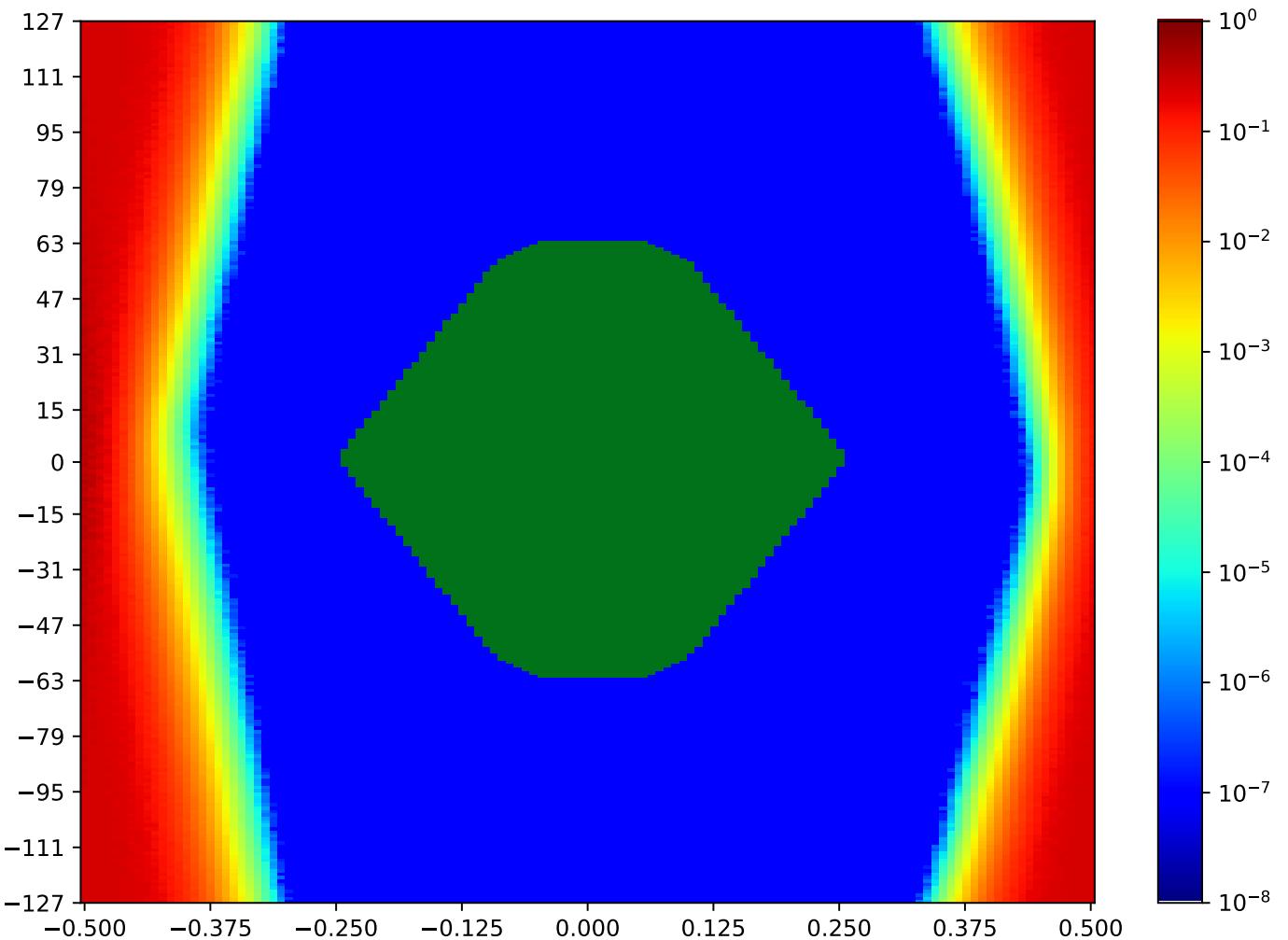


Figure 2.170: MSP_C_FPGA-TX4-03-RX8-03-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.5 MSP_C_FPGA-TX4-04-RX8-04-MSP_A_FPGA

Table 2.158: MSP_C_FPGA-TX4-04-RX8-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:20:59		2018-Jan-24 16:22:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23756	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

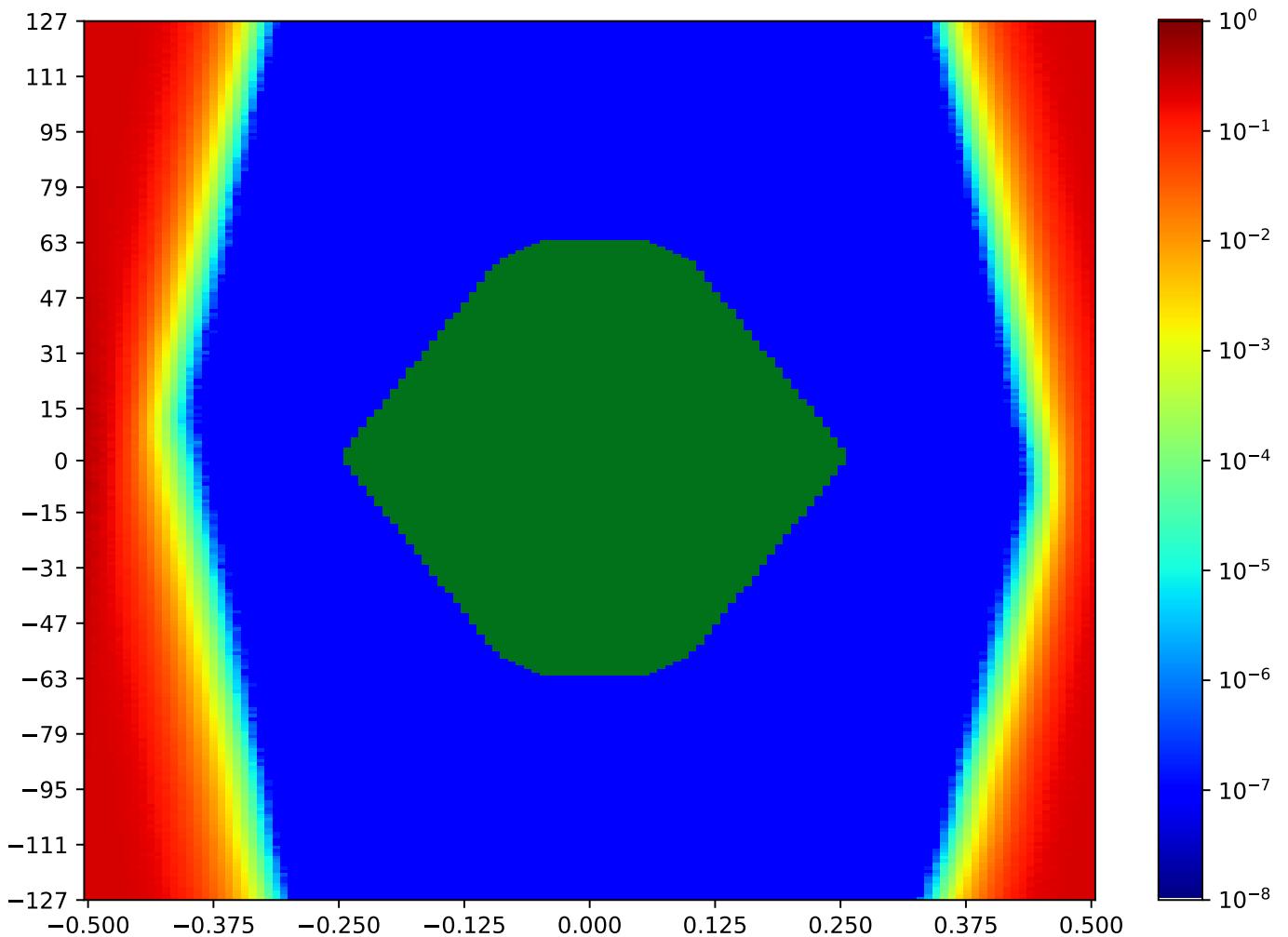


Figure 2.171: MSP_C_FPGA-TX4-04-RX8-04-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.6 MSP_C_FPGA-TX4-05-RX8-05-MSP_A_FPGA

Table 2.159: MSP_C_FPGA-TX4-05-RX8-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:12:46		2018-Jan-24 16:13:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23153	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

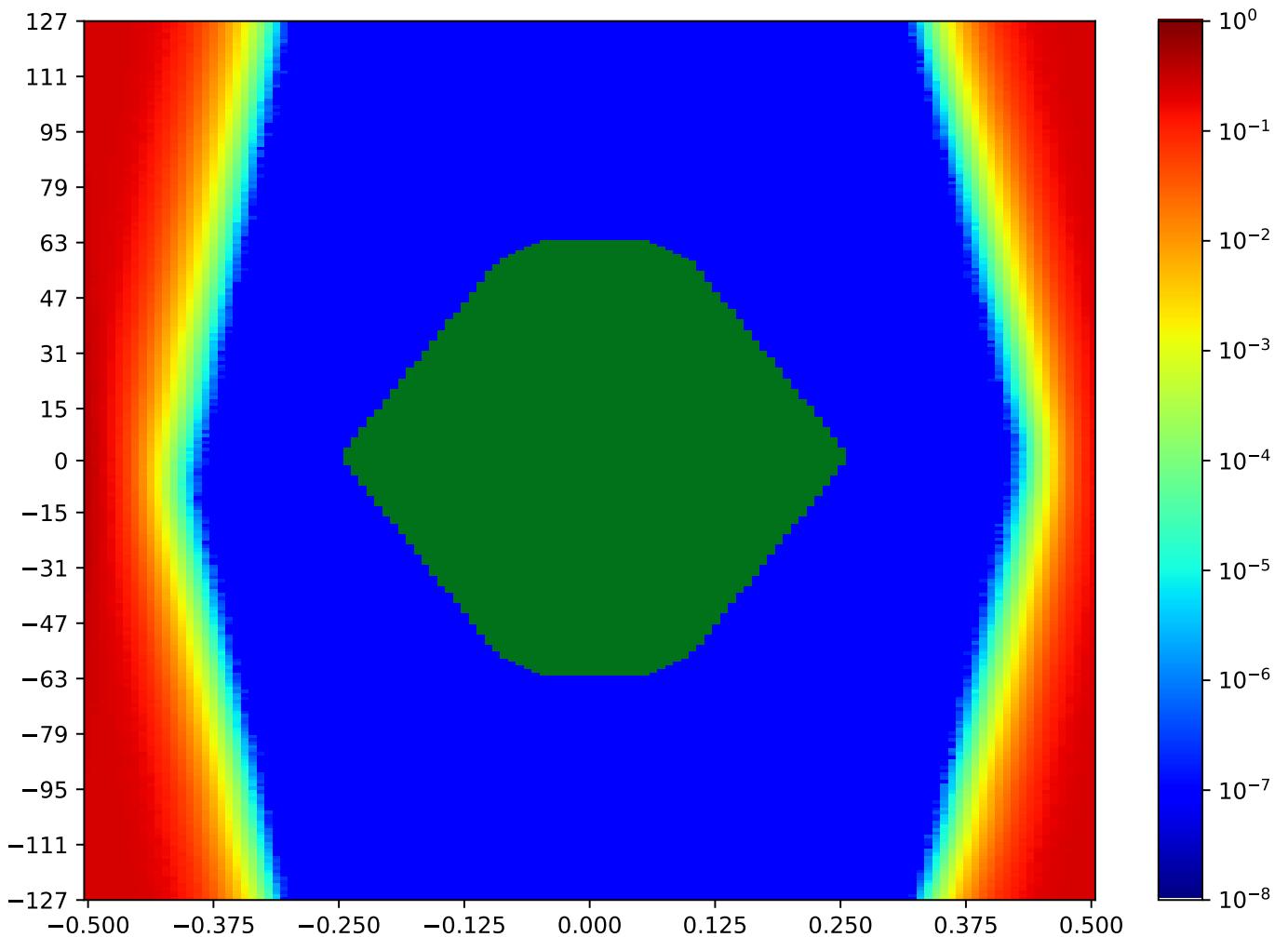


Figure 2.172: MSP_C_FPGA-TX4-05-RX8-05-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.7 MSP_C_FPGA-TX4-06-RX8-06-MSP_A_FPGA

Table 2.160: MSP_C_FPGA-TX4-06-RX8-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:23:20		2018-Jan-24 16:24:29	
Reset RX	OA	HO		HO (%)	
true	23919	102		79.07%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

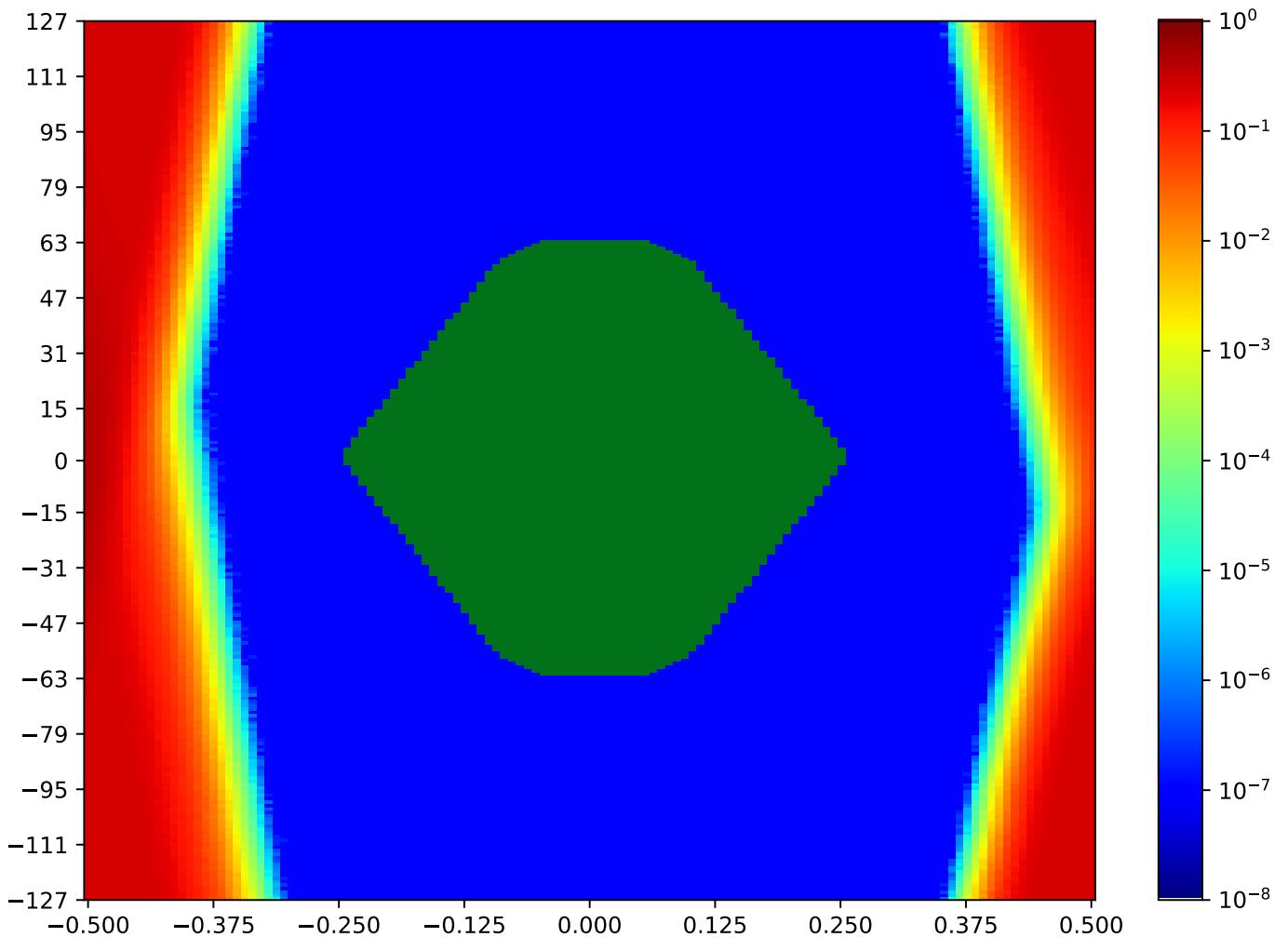


Figure 2.173: MSP_C_FPGA-TX4-06-RX8-06-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.8 MSP_C_FPGA-TX4-07-RX8-07-MSP_A_FPGA

Table 2.161: MSP_C_FPGA-TX4-07-RX8-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:15:05		2018-Jan-24 16:16:15	
Reset RX	OA	HO		HO (%)	
true	24251	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

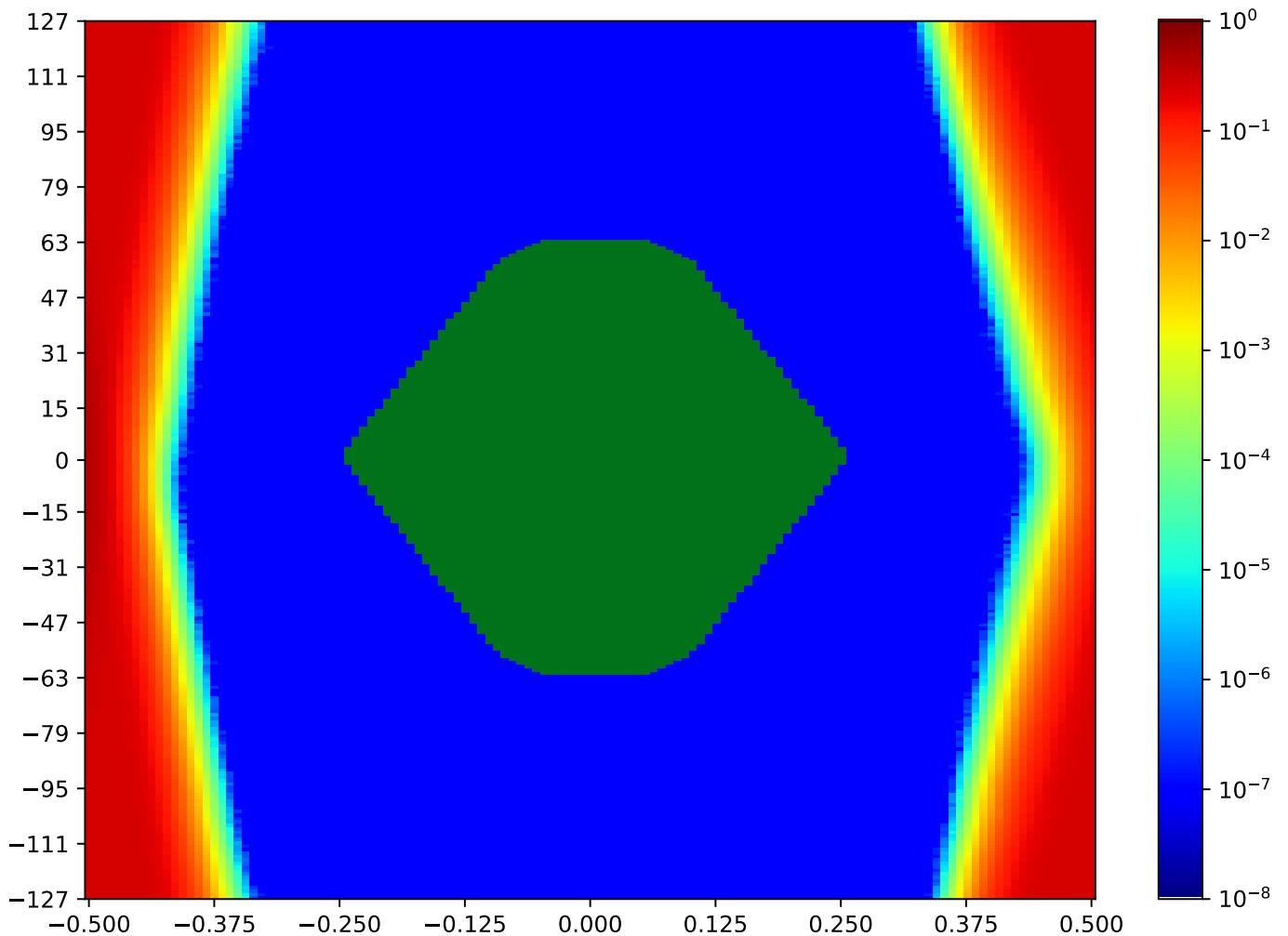


Figure 2.174: MSP_C_FPGA-TX4-07-RX8-07-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.9 MSP_C_FPGA-TX4-08-RX8-08-MSP_A_FPGA

Table 2.162: MSP_C_FPGA-TX4-08-RX8-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:22:10		2018-Jan-24 16:23:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24374	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

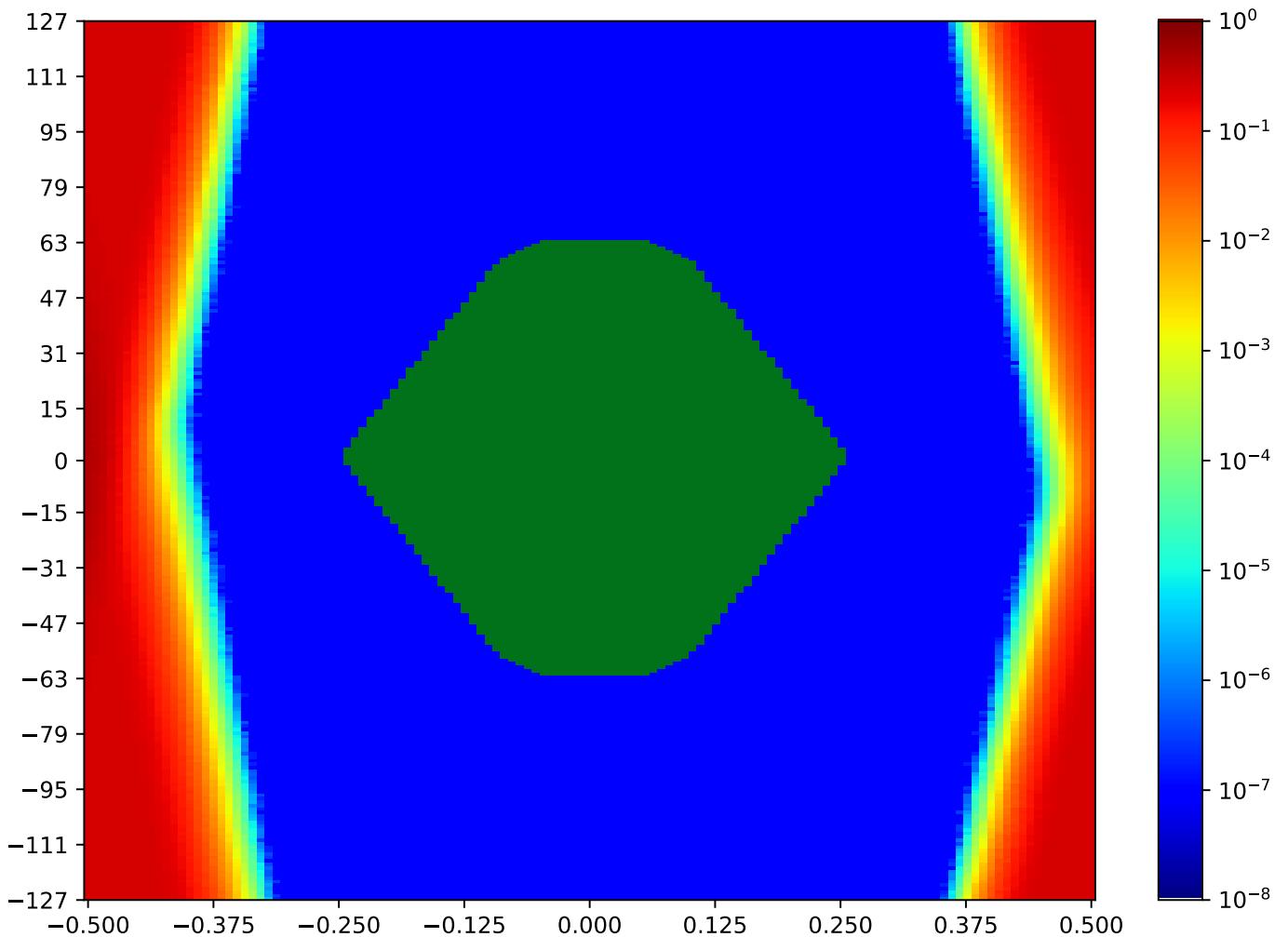


Figure 2.175: MSP_C_FPGA-TX4-08-RX8-08-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.10 MSP_C_FPGA-TX4-09-RX8-09-MSP_A_FPGA

Table 2.163: MSP_C_FPGA-TX4-09-RX8-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:16:15		2018-Jan-24 16:17:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26067	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

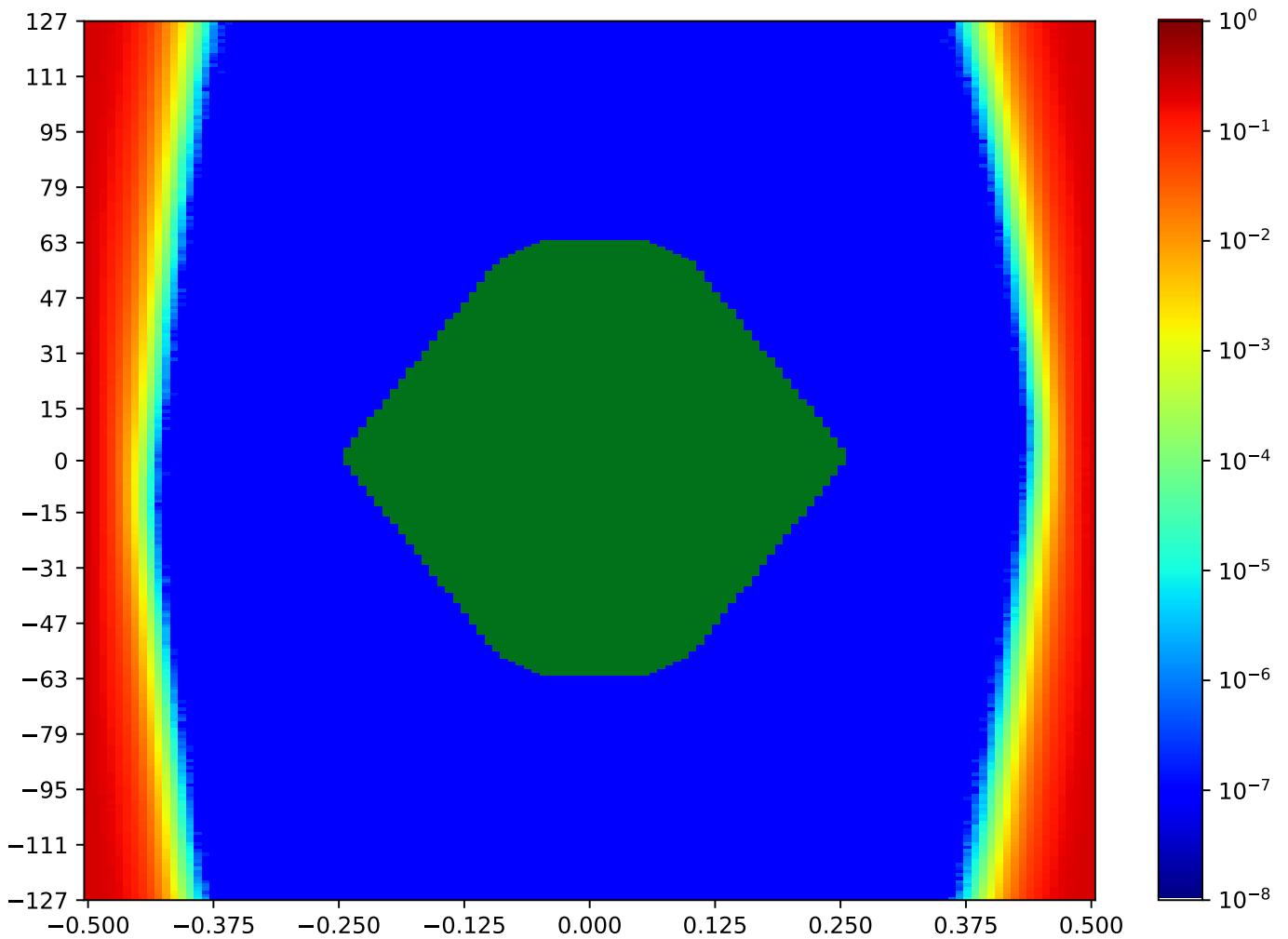


Figure 2.176: MSP_C_FPGA-TX4-09-RX8-09-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.11 MSP_C_FPGA-TX4-10-RX8-10-MSP_A_FPGA

Table 2.164: MSP_C_FPGA-TX4-10-RX8-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:19:47		2018-Jan-24 16:20:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24853	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

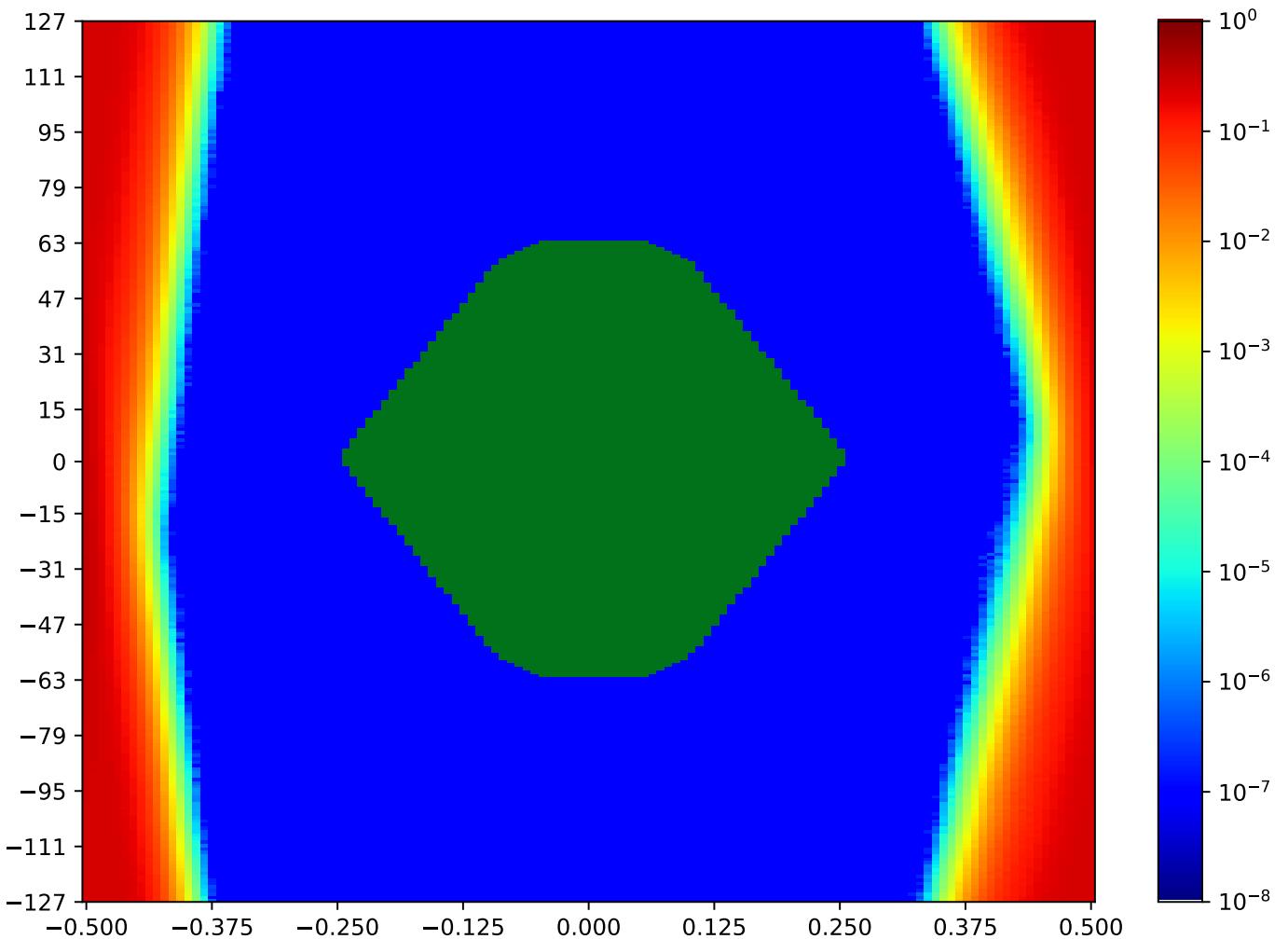


Figure 2.177: MSP_C_FPGA-TX4-10-RX8-10-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.13.12 MSP_C_FPGA-TX4-11-RX8-11-MSP_A_FPGA

Table 2.165: MSP_C_FPGA-TX4-11-RX8-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:18:39		2018-Jan-24 16:19:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23351	104	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

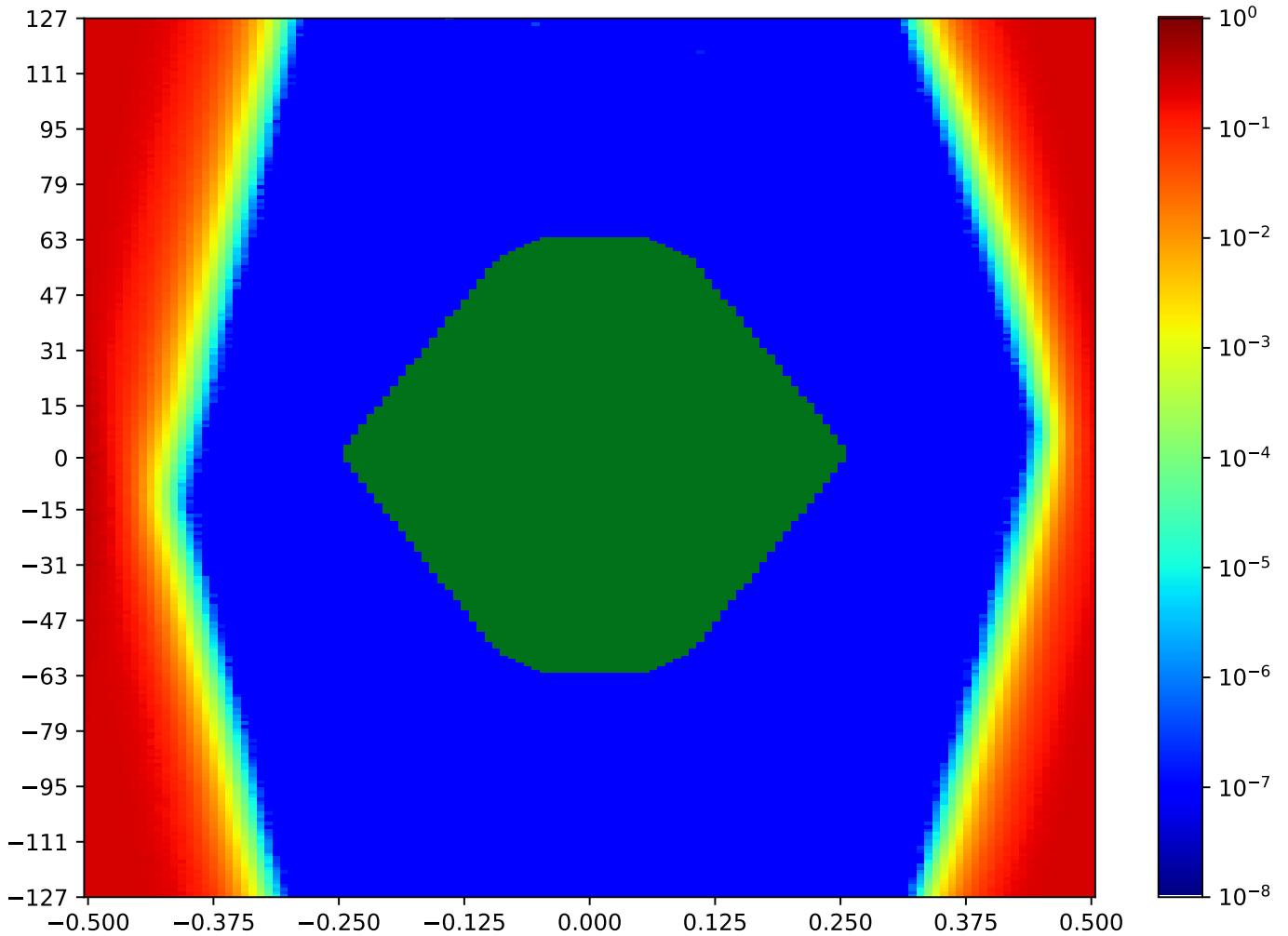


Figure 2.178: MSP_C_FPGA-TX4-11-RX8-11-MSP_A_FPGA

Call back to summary Figure 2.166. Sibling eye diagrams: V1-12.8.

2.14 Partial TRP TX5 MSP_C RX14 Minipod Loopback

A cross-reference to Figure 2.179. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

Next summary Figure ??.

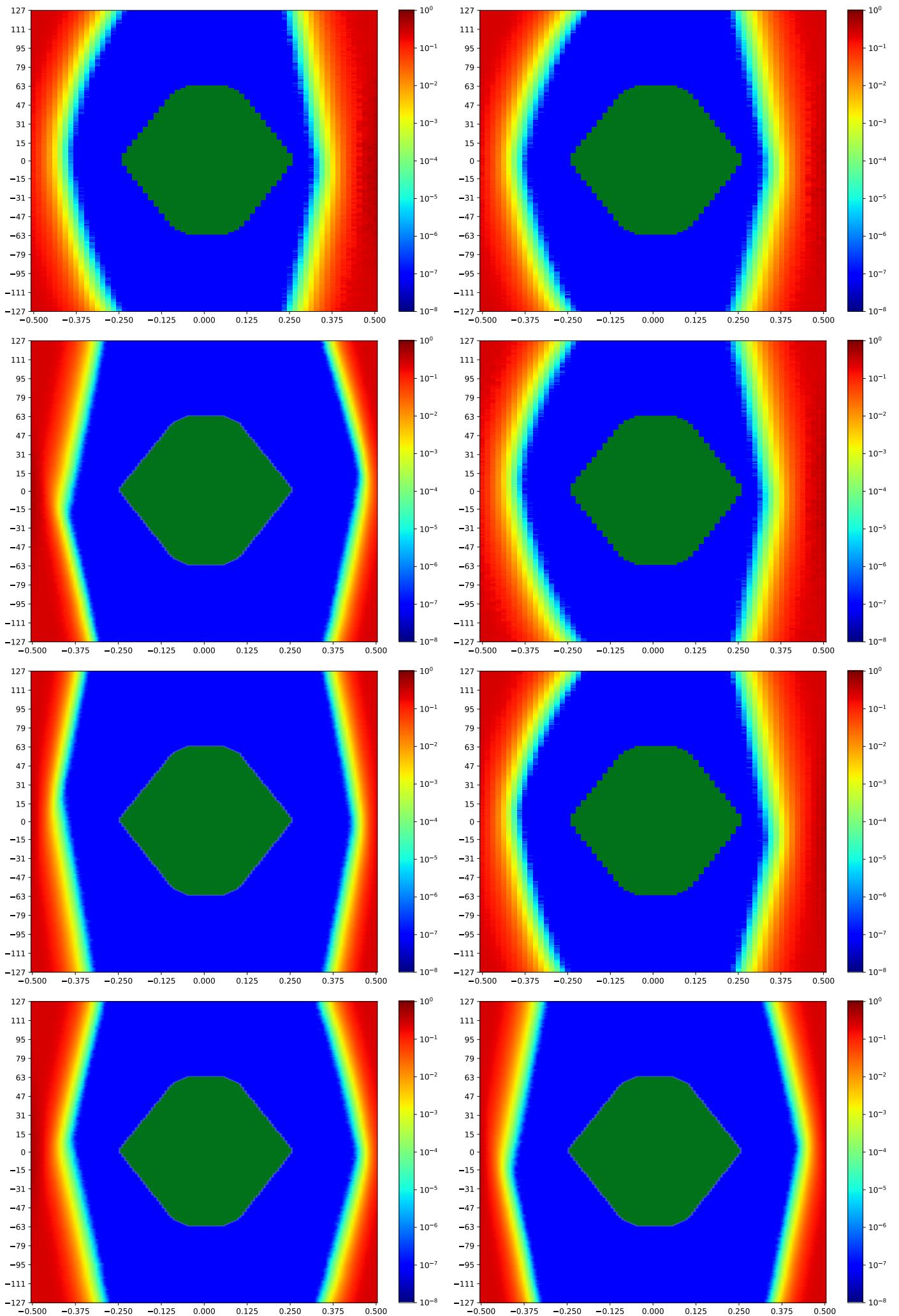


Figure 2.179: Partial TRP TX5 MSP_C RX14 Minipod Loopback

2.14.1 TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

Table 2.166: TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:26:20		2018-Jan-24 16:26:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9606	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

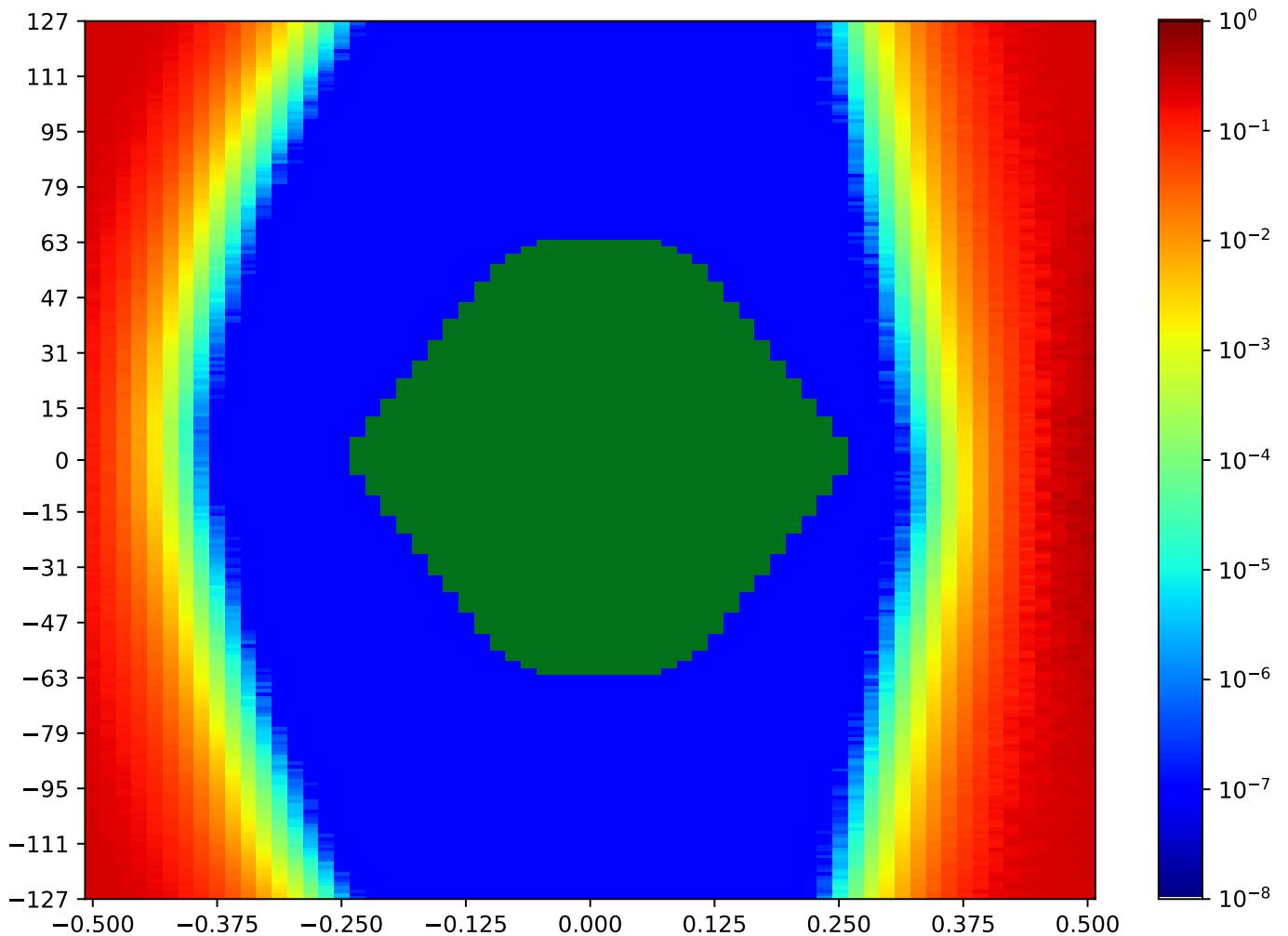


Figure 2.180: TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.14.2 TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

Table 2.167: TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:25:06		2018-Jan-24 16:25:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9161	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

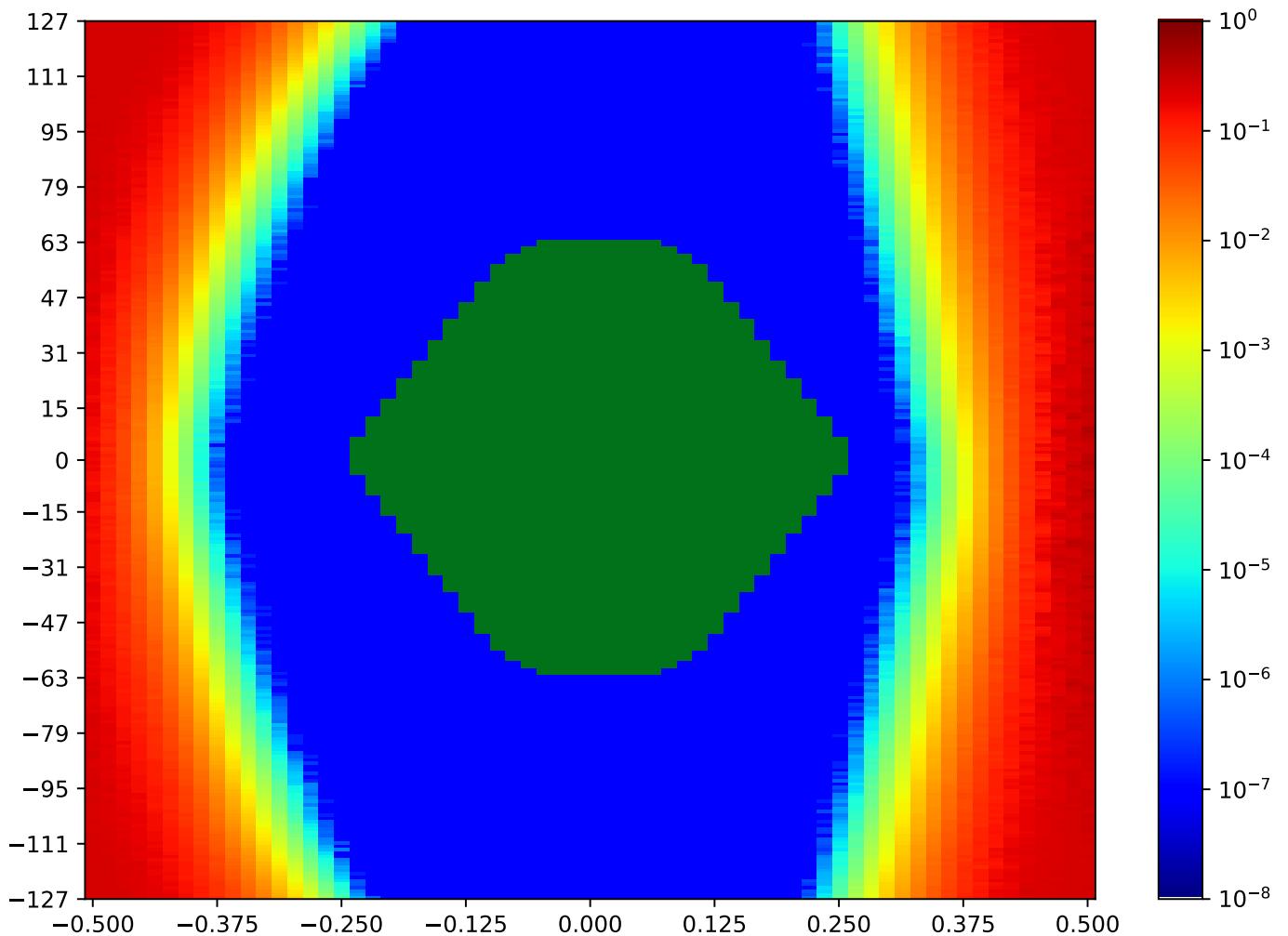


Figure 2.181: TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.14.3 TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

Table 2.168: TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:28:05		2018-Jan-24 16:29:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23674	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

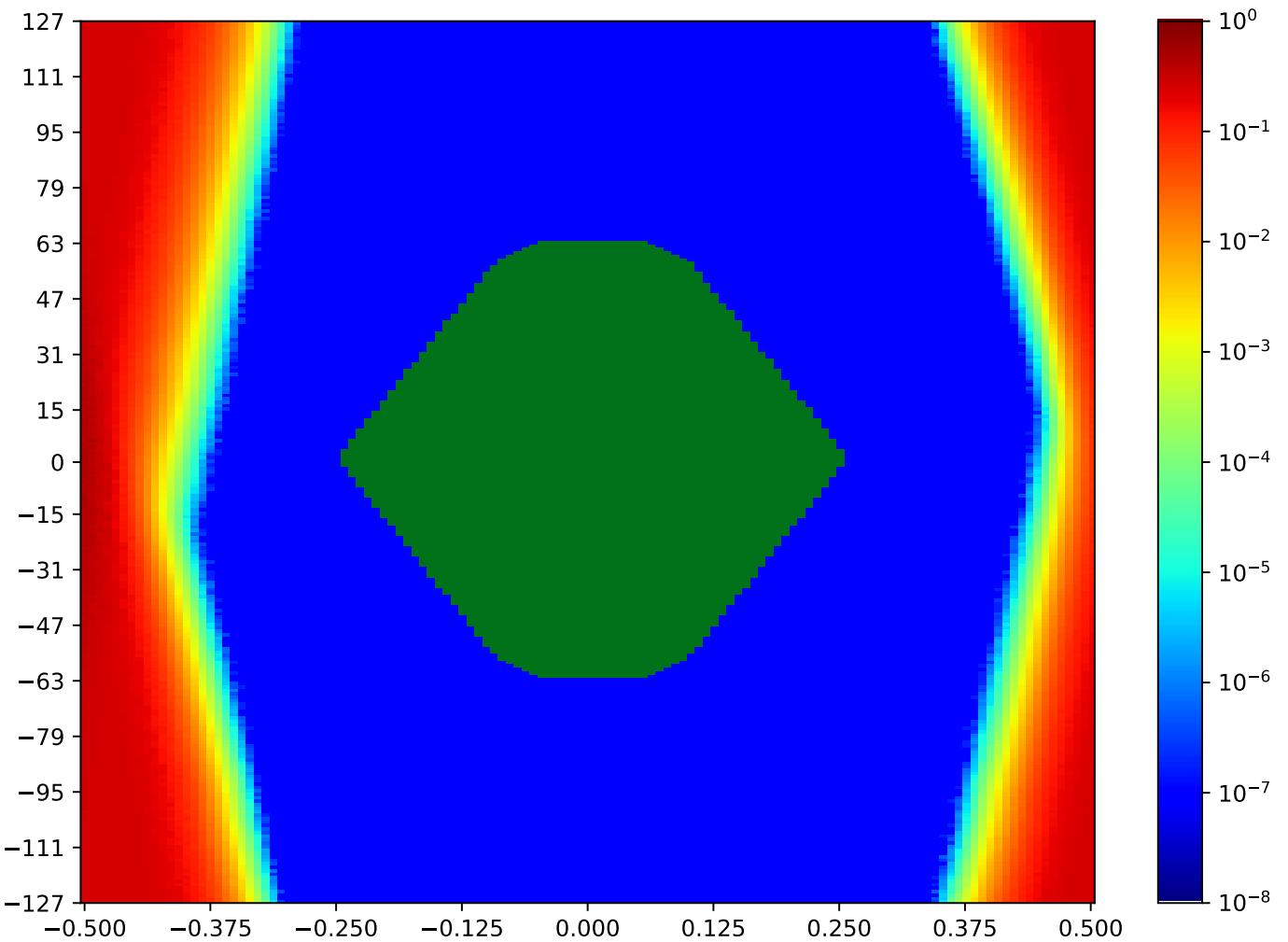


Figure 2.182: TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.14.4 TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

Table 2.169: TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:25:43		2018-Jan-24 16:26:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9248	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

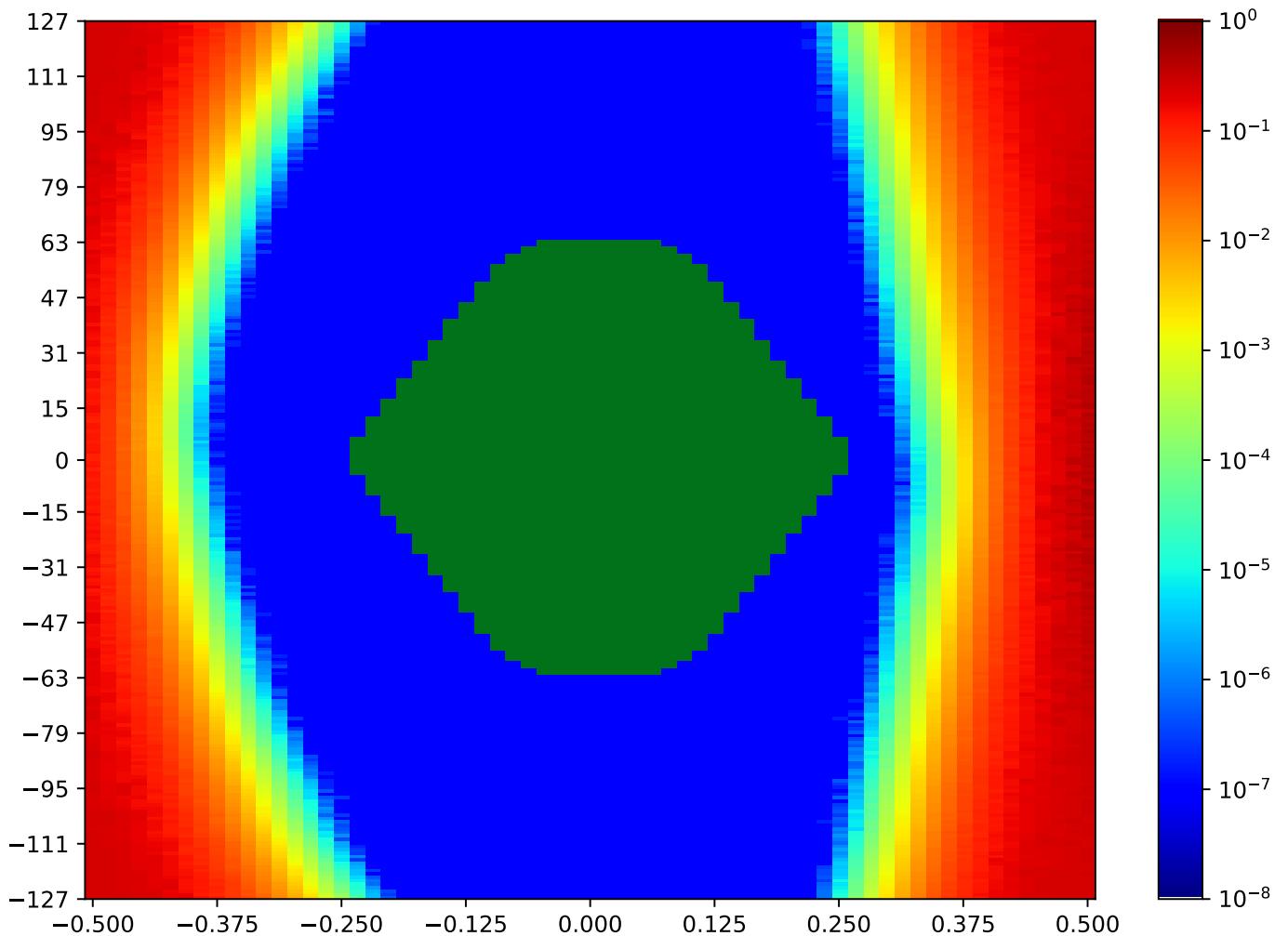


Figure 2.183: TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.14.5 TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

Table 2.170: TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:30:24		2018-Jan-24 16:31:35	
Reset RX	OA	HO		HO (%)	
true	24092	103		79.84%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

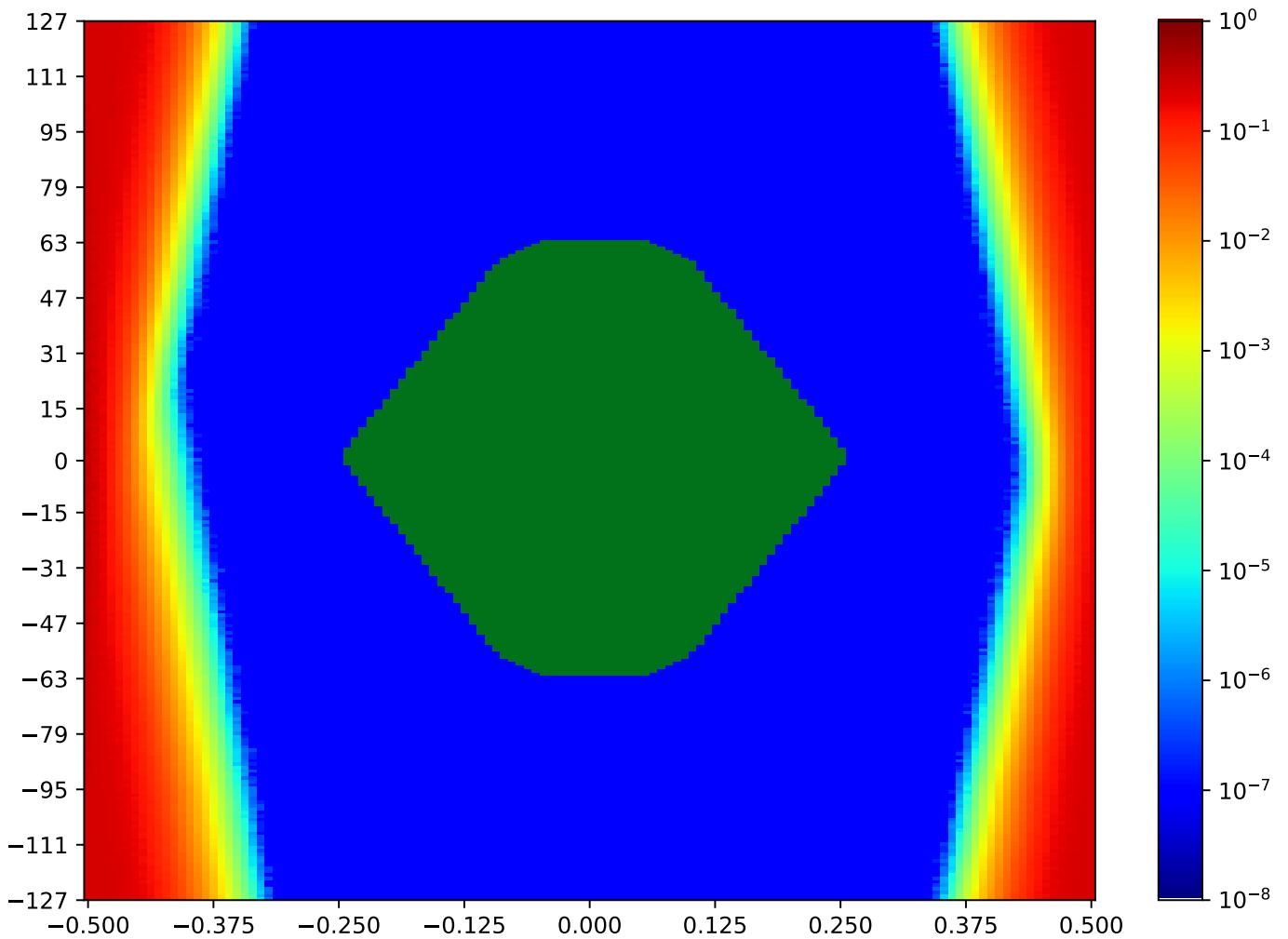


Figure 2.184: TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.14.6 TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

Table 2.171: TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:24:30		2018-Jan-24 16:25:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9530	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

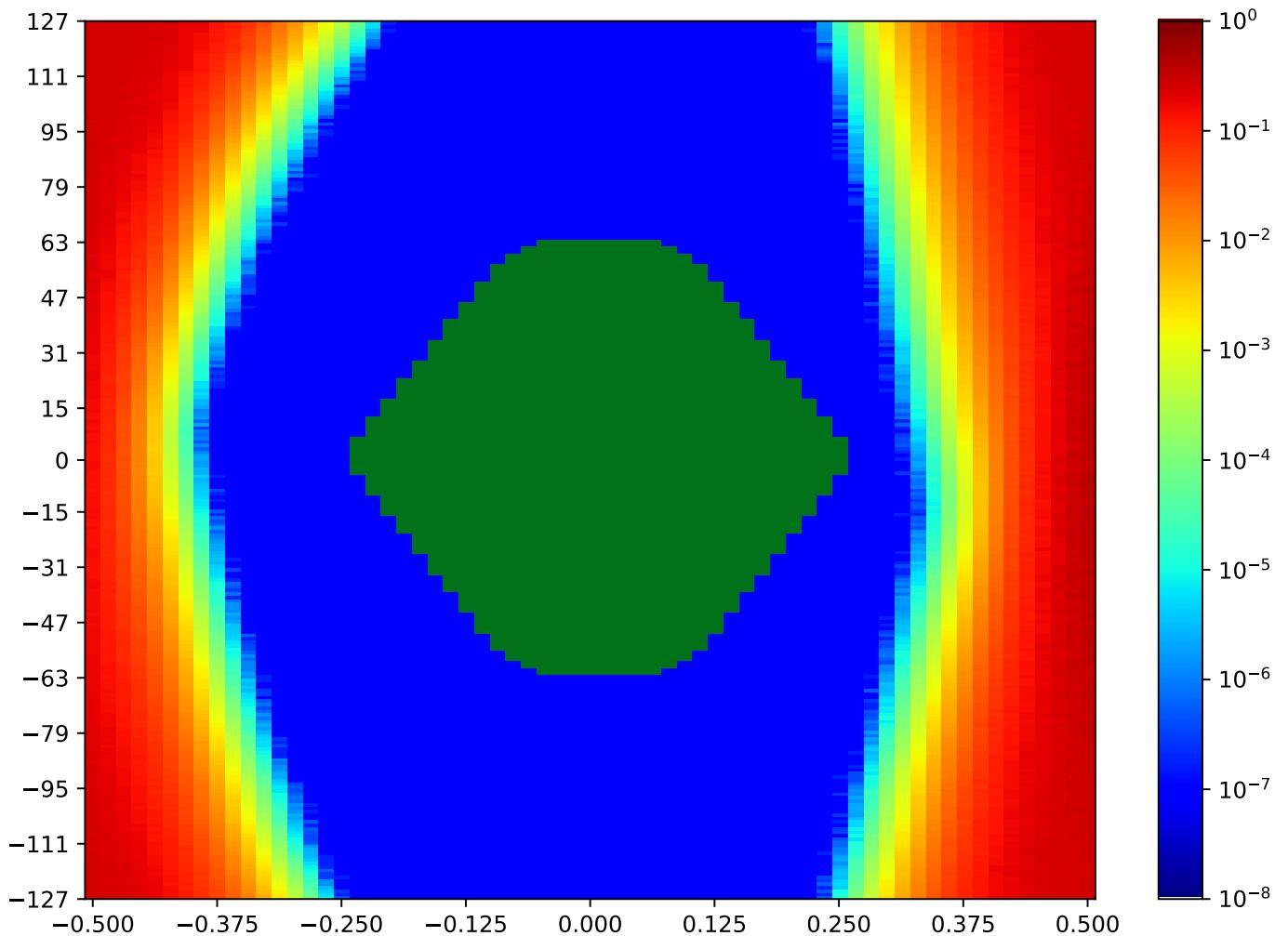


Figure 2.185: TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.14.7 TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

Table 2.172: TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:26:57		2018-Jan-24 16:28:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	22893	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

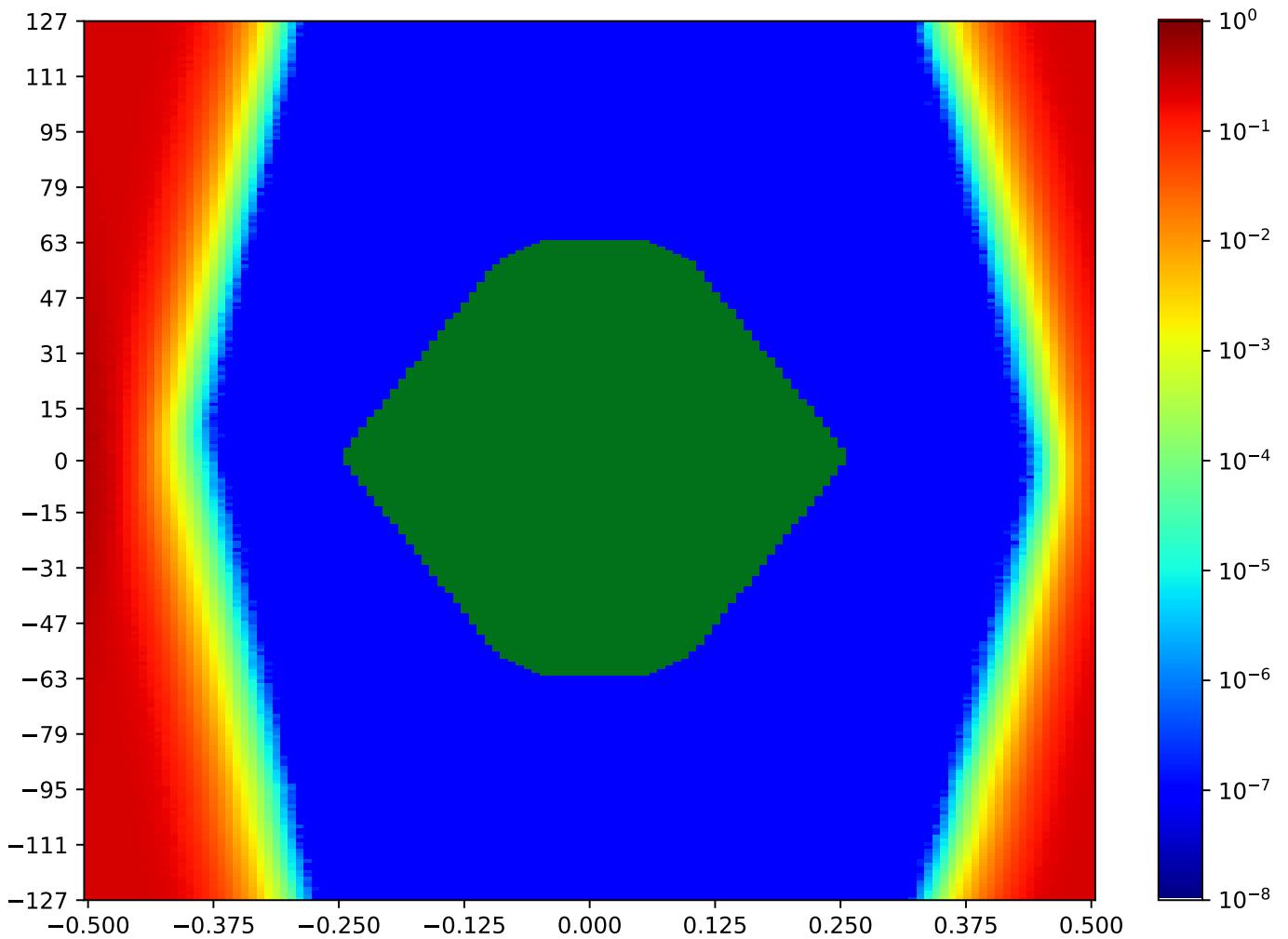


Figure 2.186: TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.14.8 TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

Table 2.173: TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 16:29:14		2018-Jan-24 16:30:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23417	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

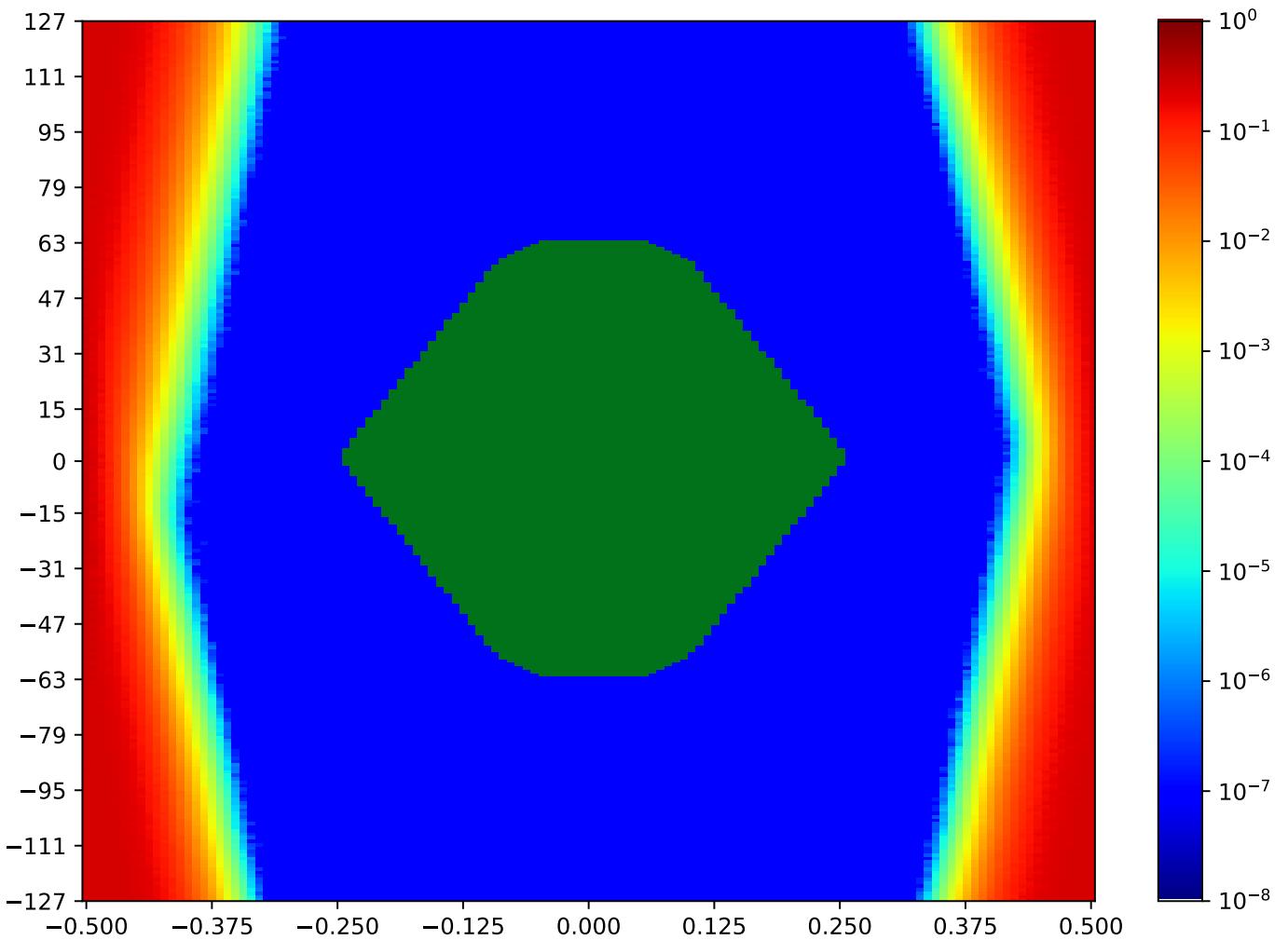


Figure 2.187: TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

Call back to summary Figure 2.179. Sibling eye diagrams: V1-12.8, V2-6.4, V2-12.8.

2.15 MSP_A TX1 MSP_C RX11 Minipod Loopback

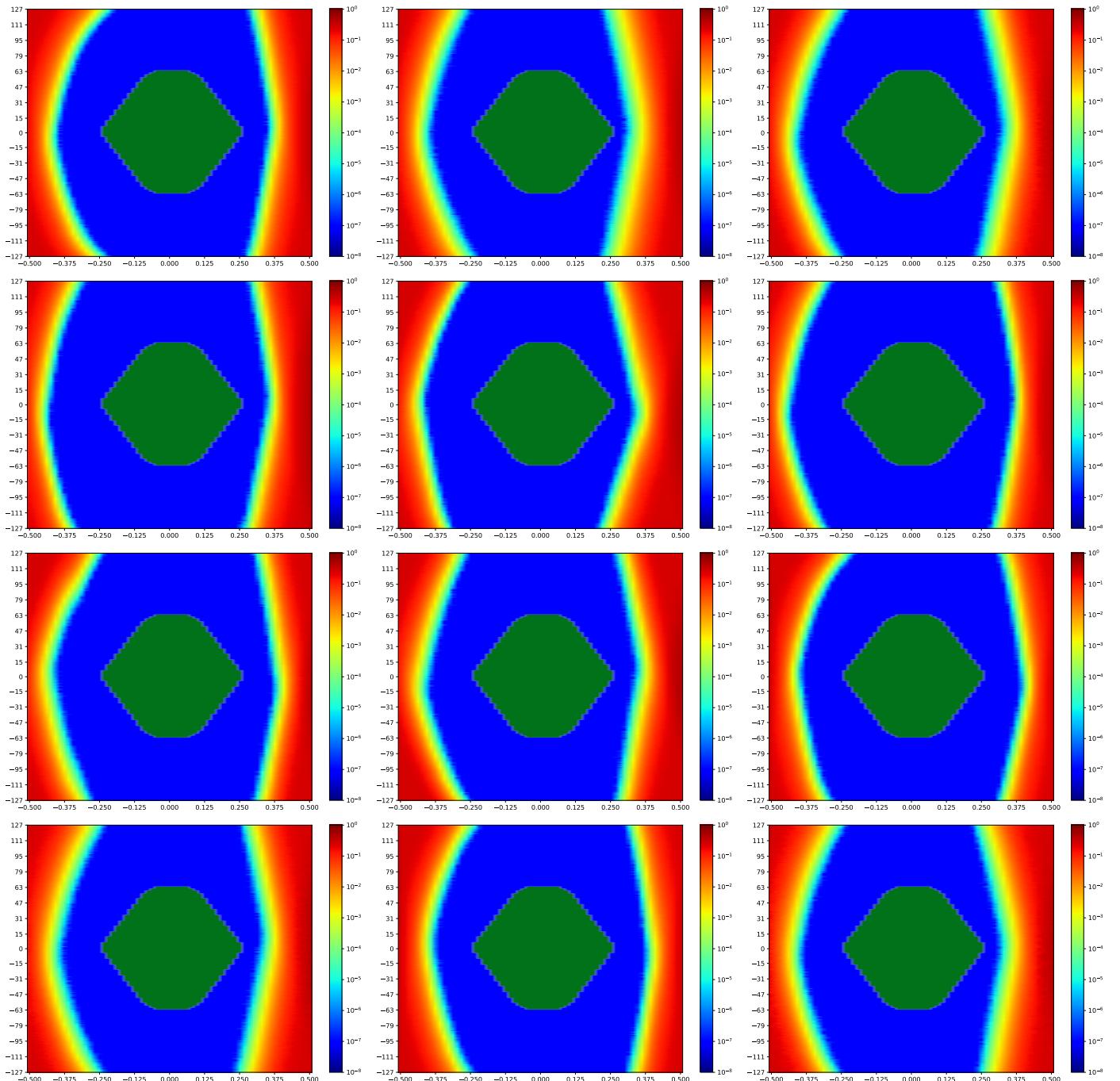


Figure 2.188: MSP_A TX1 MSP_C RX11 Minipod Loopback

A cross-reference to Figure 2.188. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.201.

2.15.1 MSP_A_FPGA-TX1-00-RX11-00-MSP_C_FPGA

Table 2.174: MSP_A_FPGA-TX1-00-RX11-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:50:09		2018-Jan-24 16:50:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10284	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

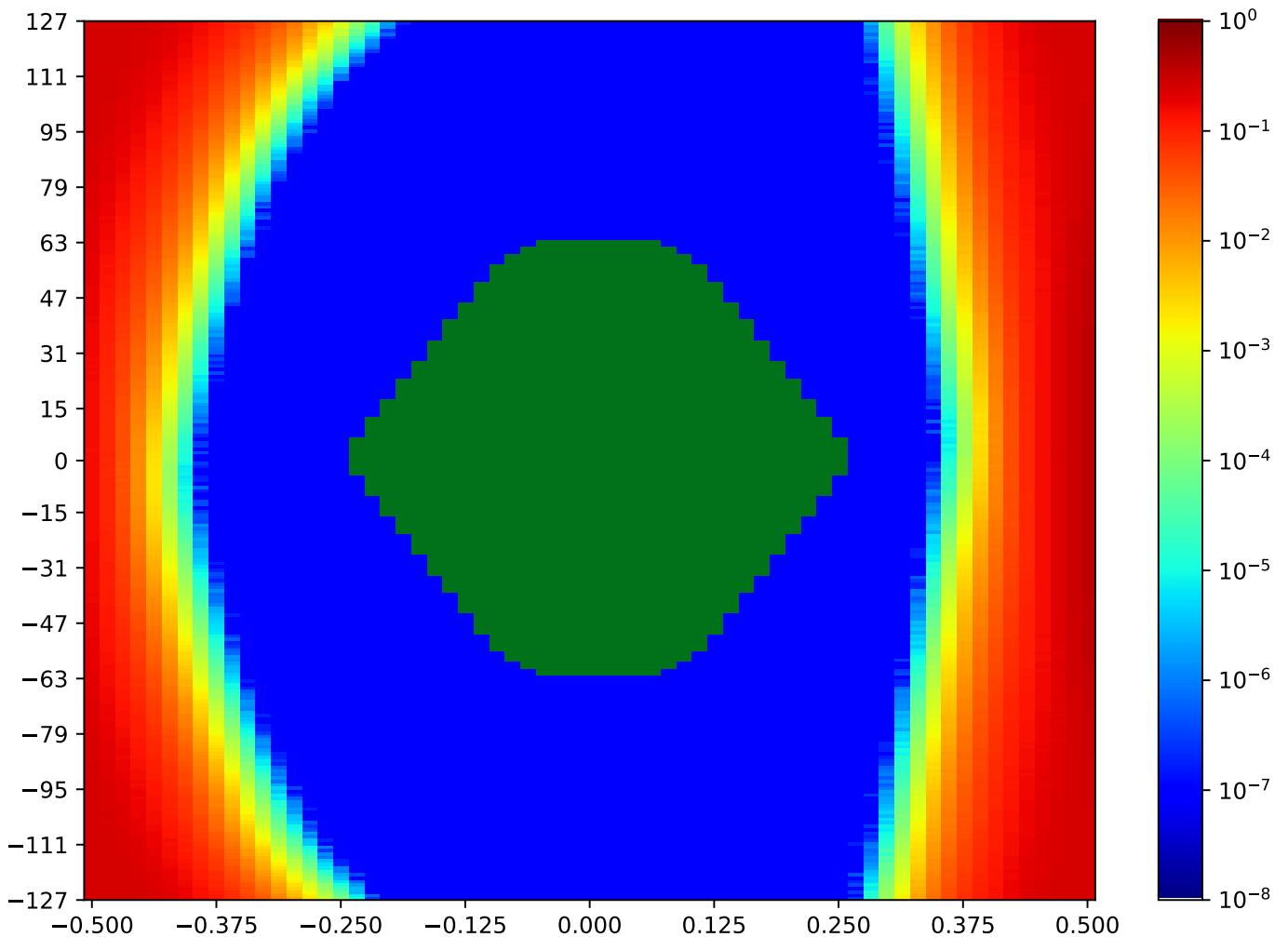


Figure 2.189: MSP_A_FPGA-TX1-00-RX11-00-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.2 MSP_A_FPGA-TX1-01-RX11-01-MSP_C_FPGA

Table 2.175: MSP_A_FPGA-TX1-01-RX11-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:51:17		2018-Jan-24 16:51:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9215	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

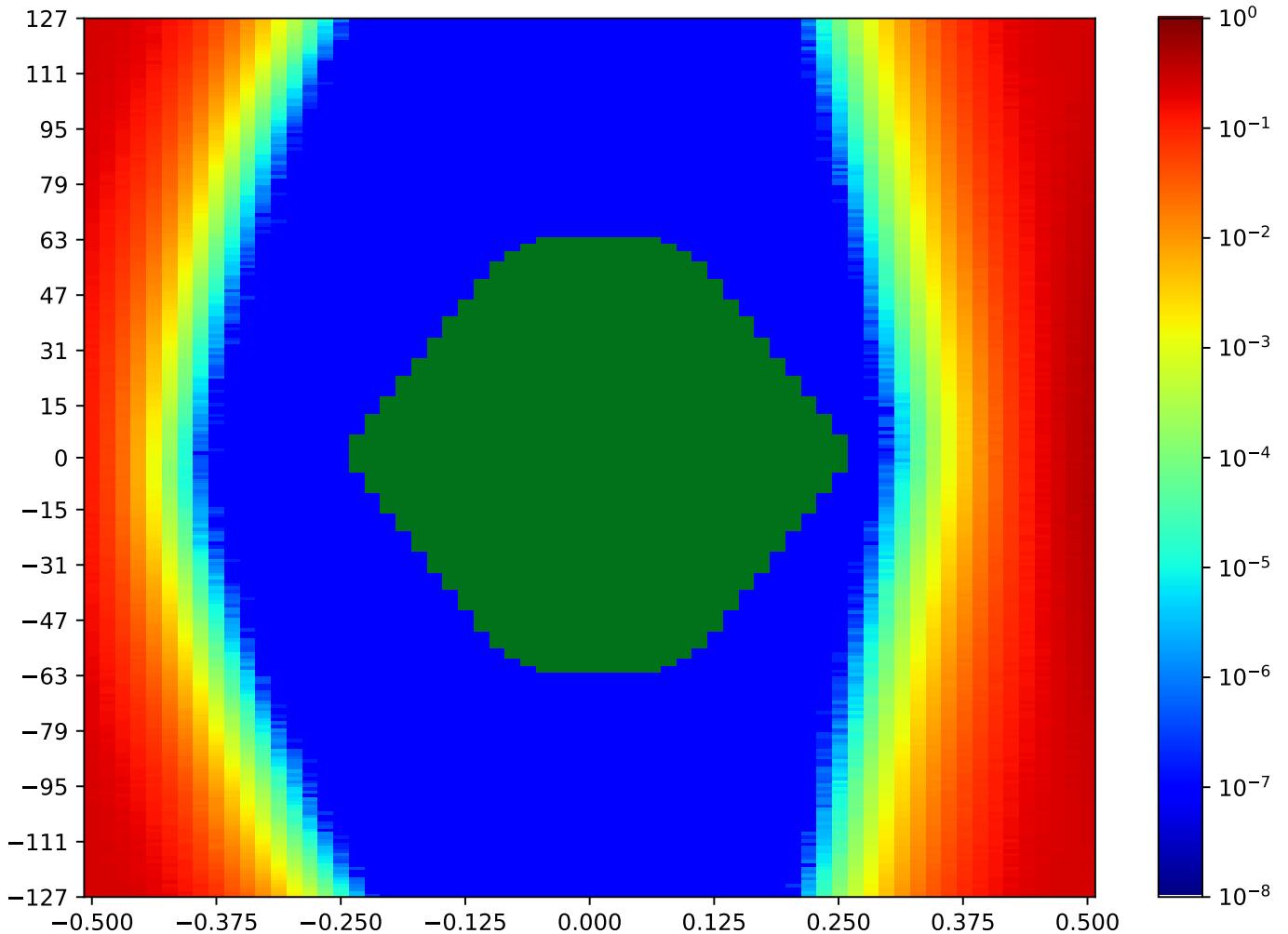


Figure 2.190: MSP_A_FPGA-TX1-01-RX11-01-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.3 MSP_A_FPGA-TX1-02-RX11-02-MSP_C_FPGA

Table 2.176: MSP_A_FPGA-TX1-02-RX11-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:51:51		2018-Jan-24 16:52:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9521	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

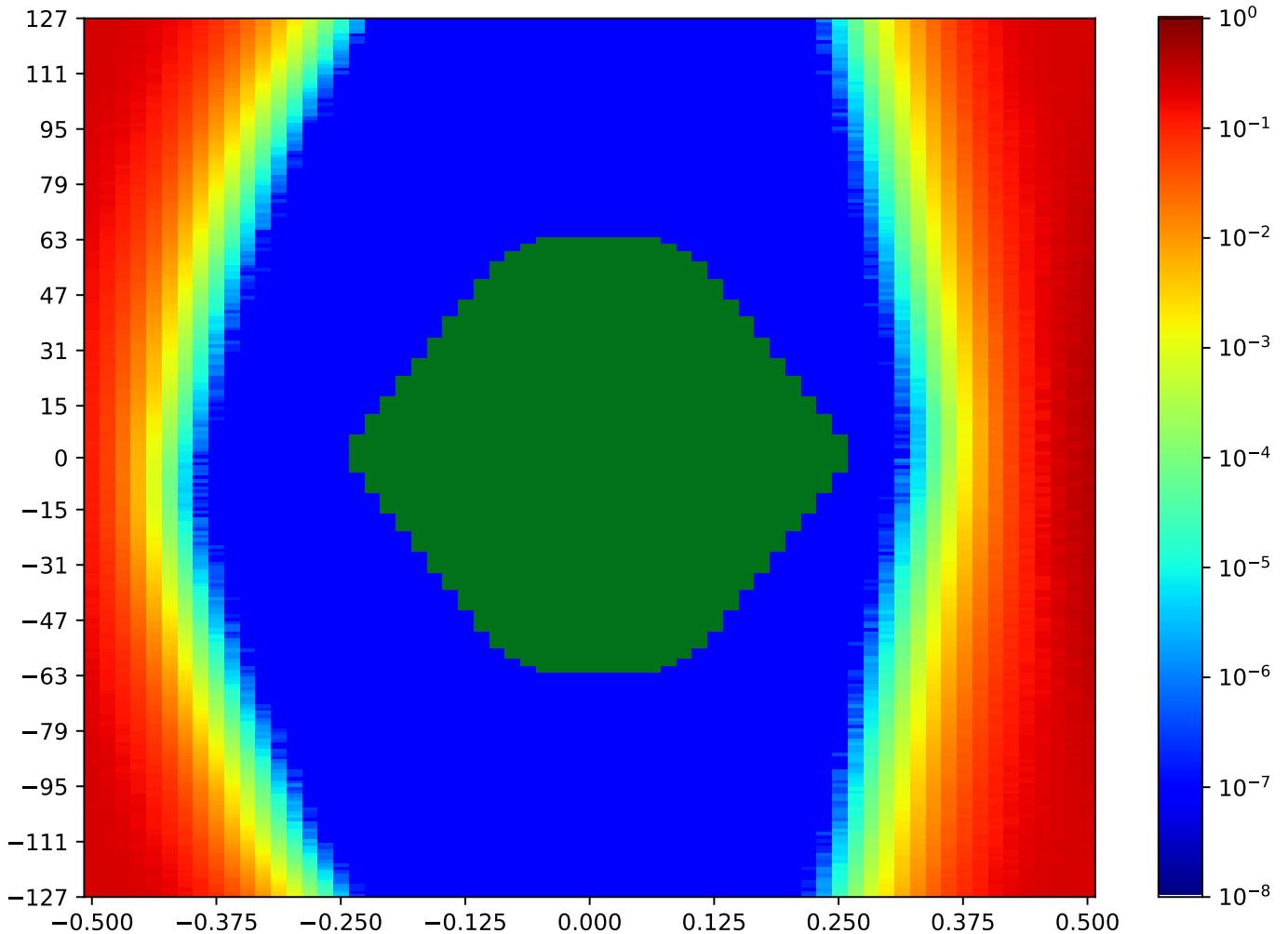


Figure 2.191: MSP_A_FPGA-TX1-02-RX11-02-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.4 MSP_A_FPGA-TX1-03-RX11-03-MSP_C_FPGA

Table 2.177: MSP_A_FPGA-TX1-03-RX11-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:48:59		2018-Jan-24 16:49:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11027	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

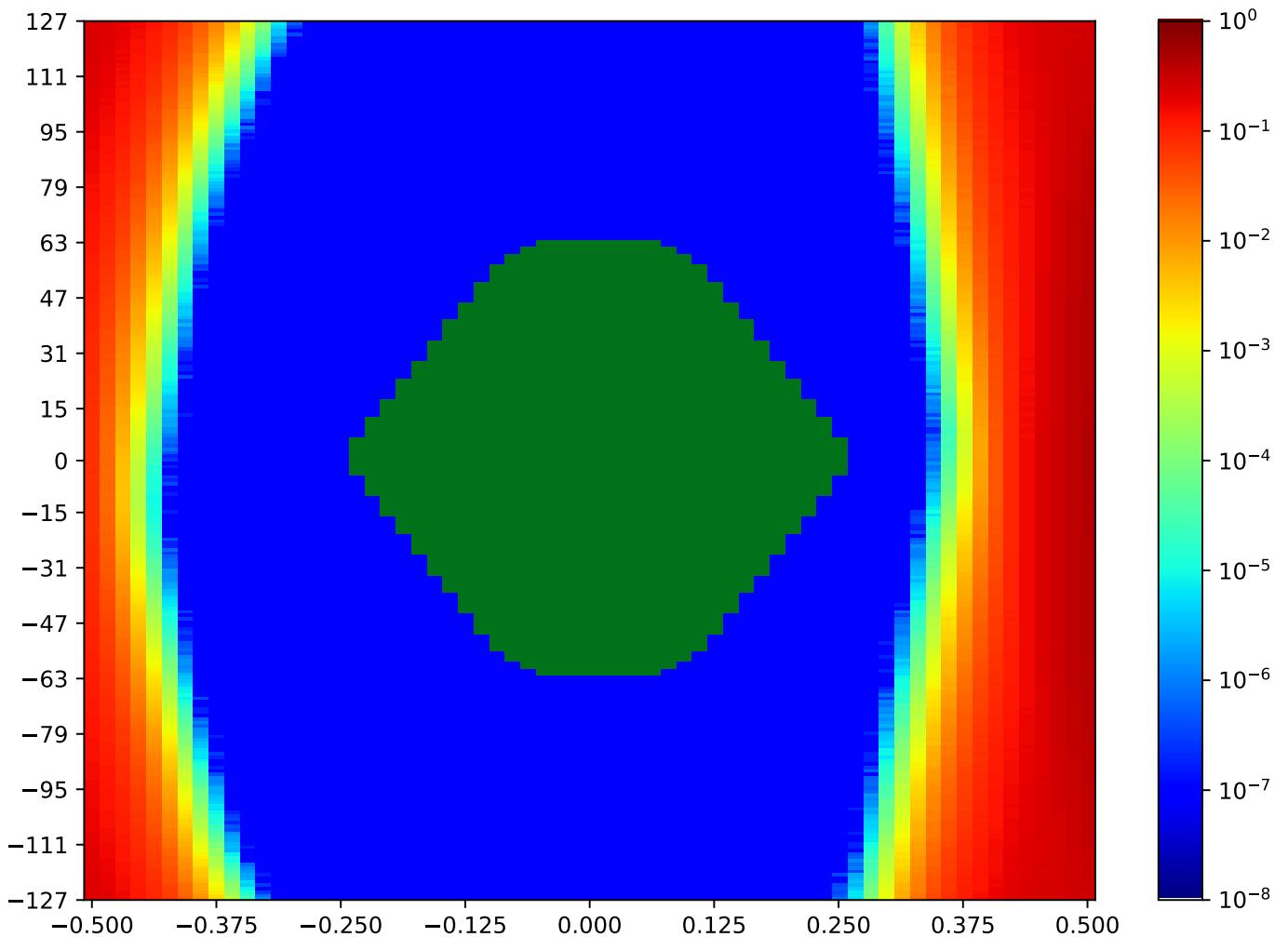


Figure 2.192: MSP_A_FPGA-TX1-03-RX11-03-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.5 MSP_A_FPGA-TX1-04-RX11-04-MSP_C_FPGA

Table 2.178: MSP_A_FPGA-TX1-04-RX11-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:53:38		2018-Jan-24 16:54:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10031	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

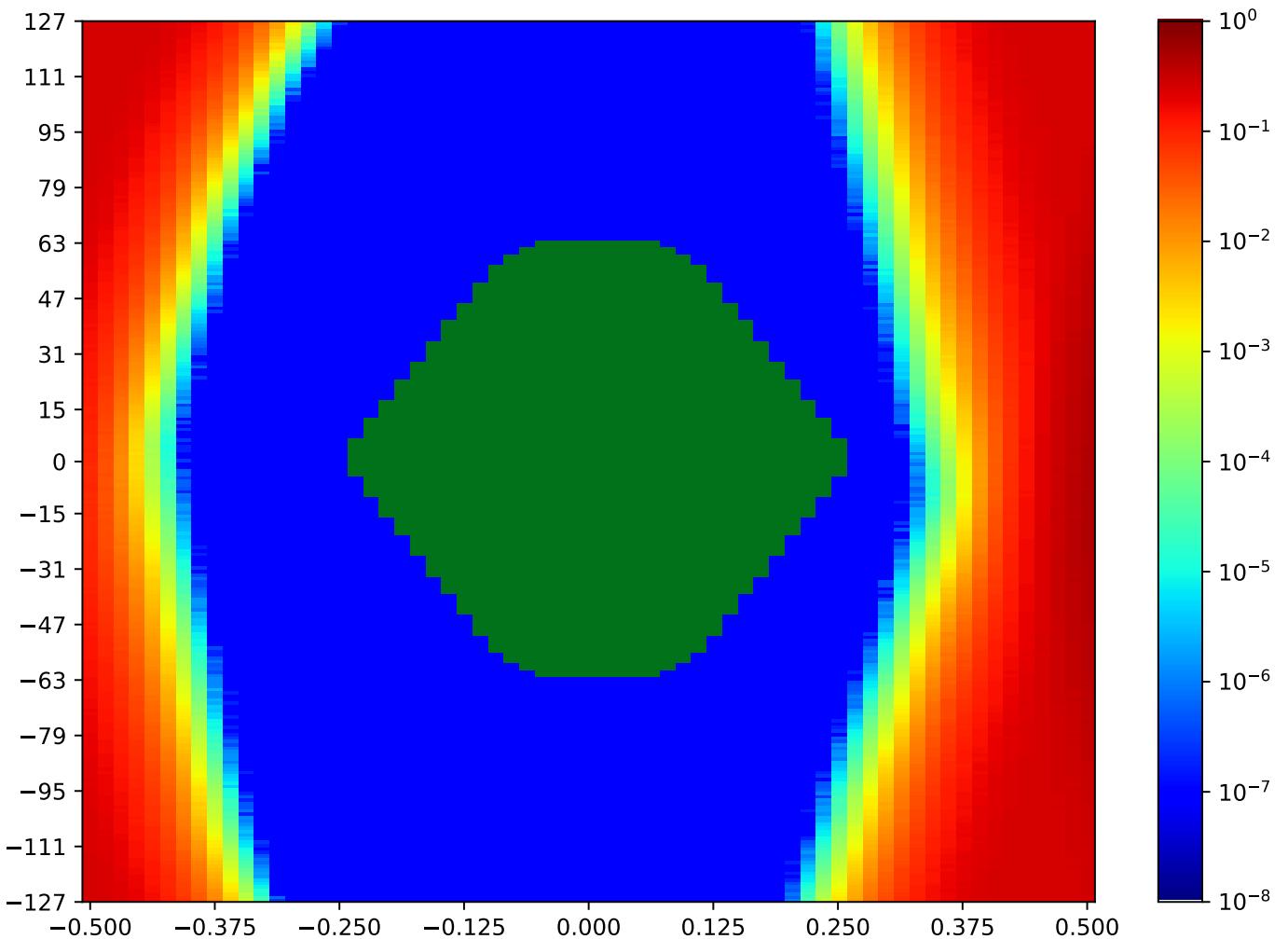


Figure 2.193: MSP_A_FPGA-TX1-04-RX11-04-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.6 MSP_A_FPGA-TX1-05-RX11-05-MSP_C_FPGA

Table 2.179: MSP_A_FPGA-TX1-05-RX11-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:48:24		2018-Jan-24 16:48:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11151	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

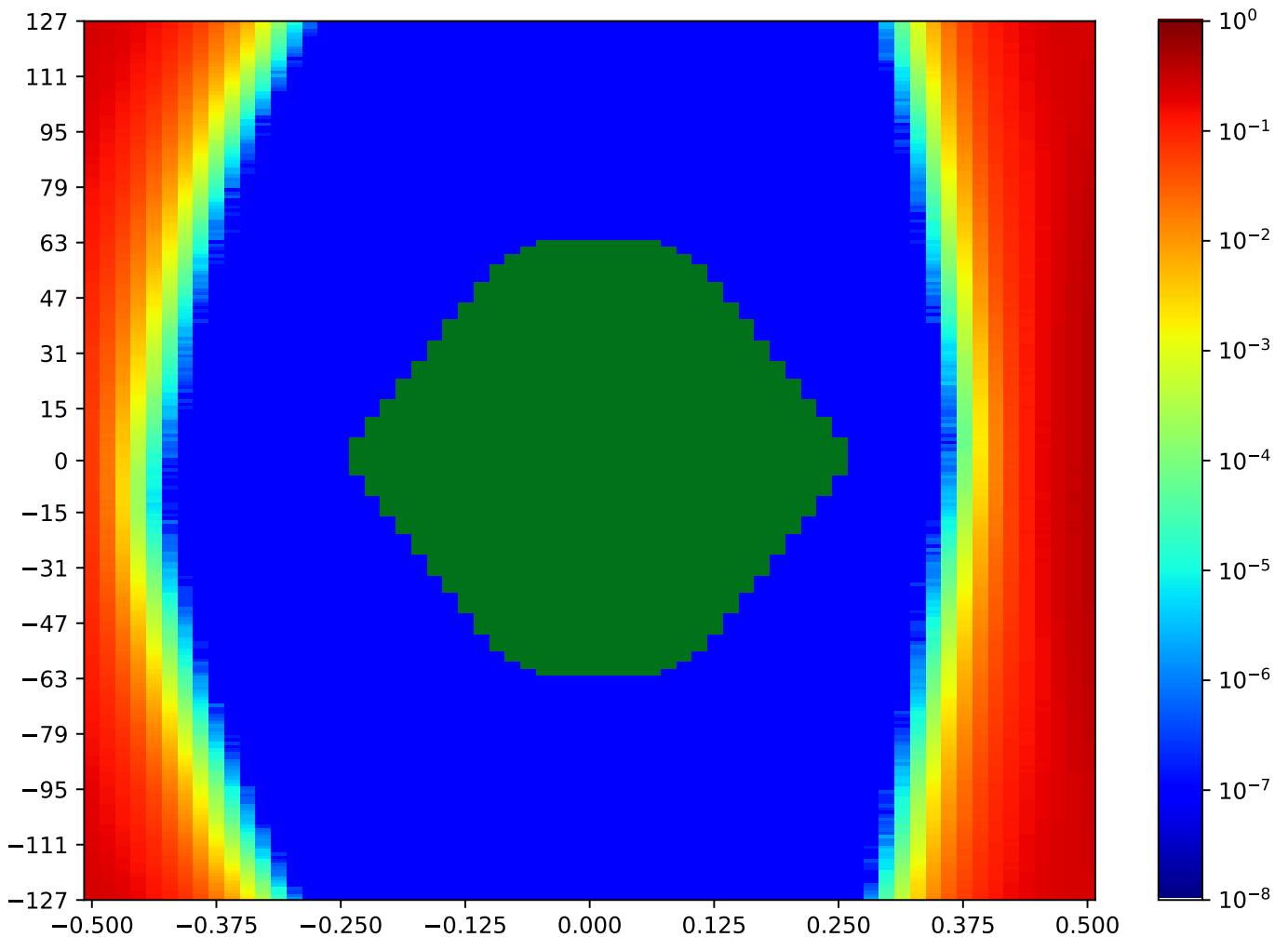


Figure 2.194: MSP_A_FPGA-TX1-05-RX11-05-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.7 MSP_A_FPGA-TX1-06-RX11-06-MSP_C_FPGA

Table 2.180: MSP_A_FPGA-TX1-06-RX11-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:54:48		2018-Jan-24 16:55:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10738	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

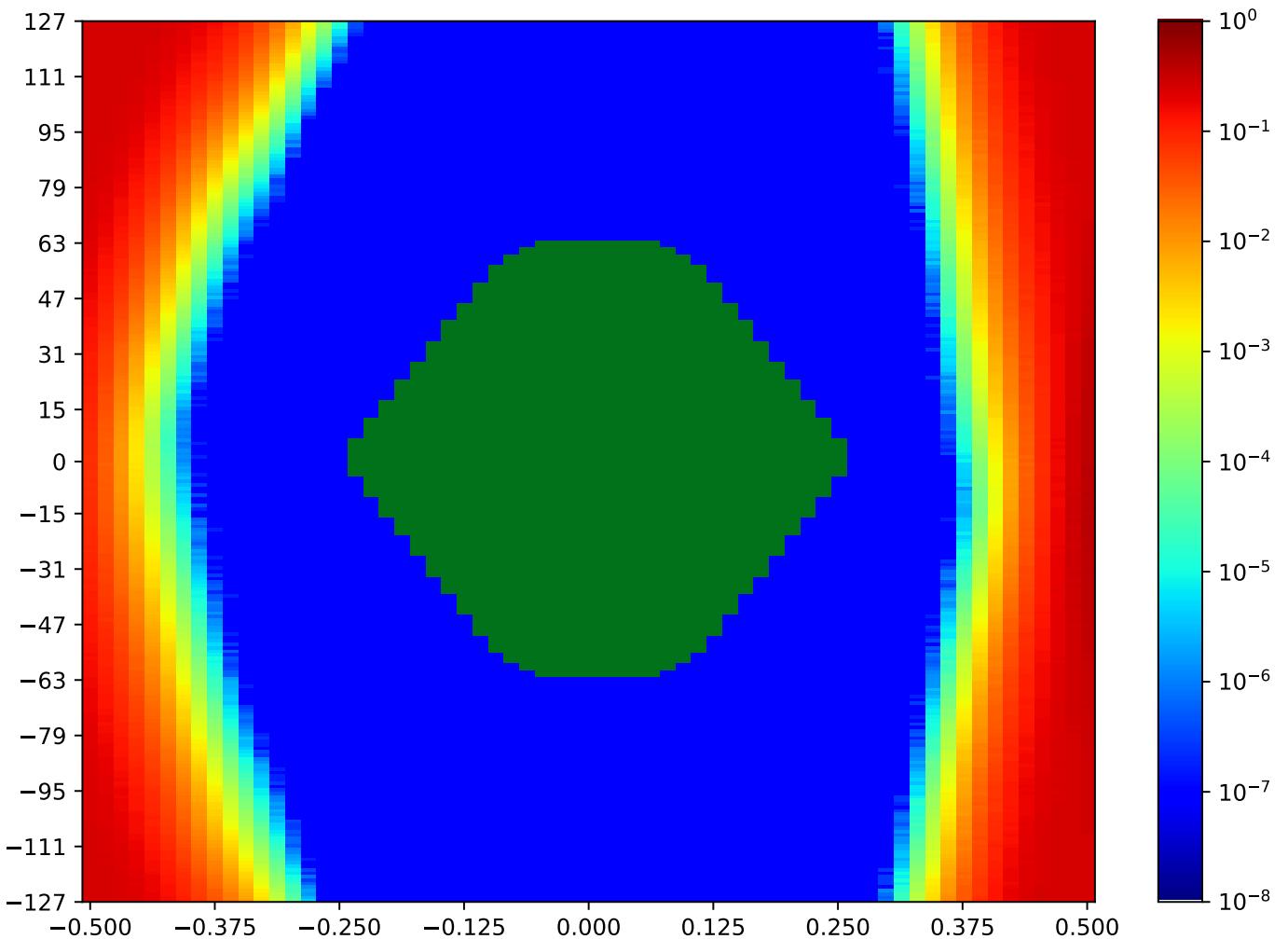


Figure 2.195: MSP_A_FPGA-TX1-06-RX11-06-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.8 MSP_A_FPGA-TX1-07-RX11-07-MSP_C_FPGA

Table 2.181: MSP_A_FPGA-TX1-07-RX11-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:49:34		2018-Jan-24 16:50:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10090	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

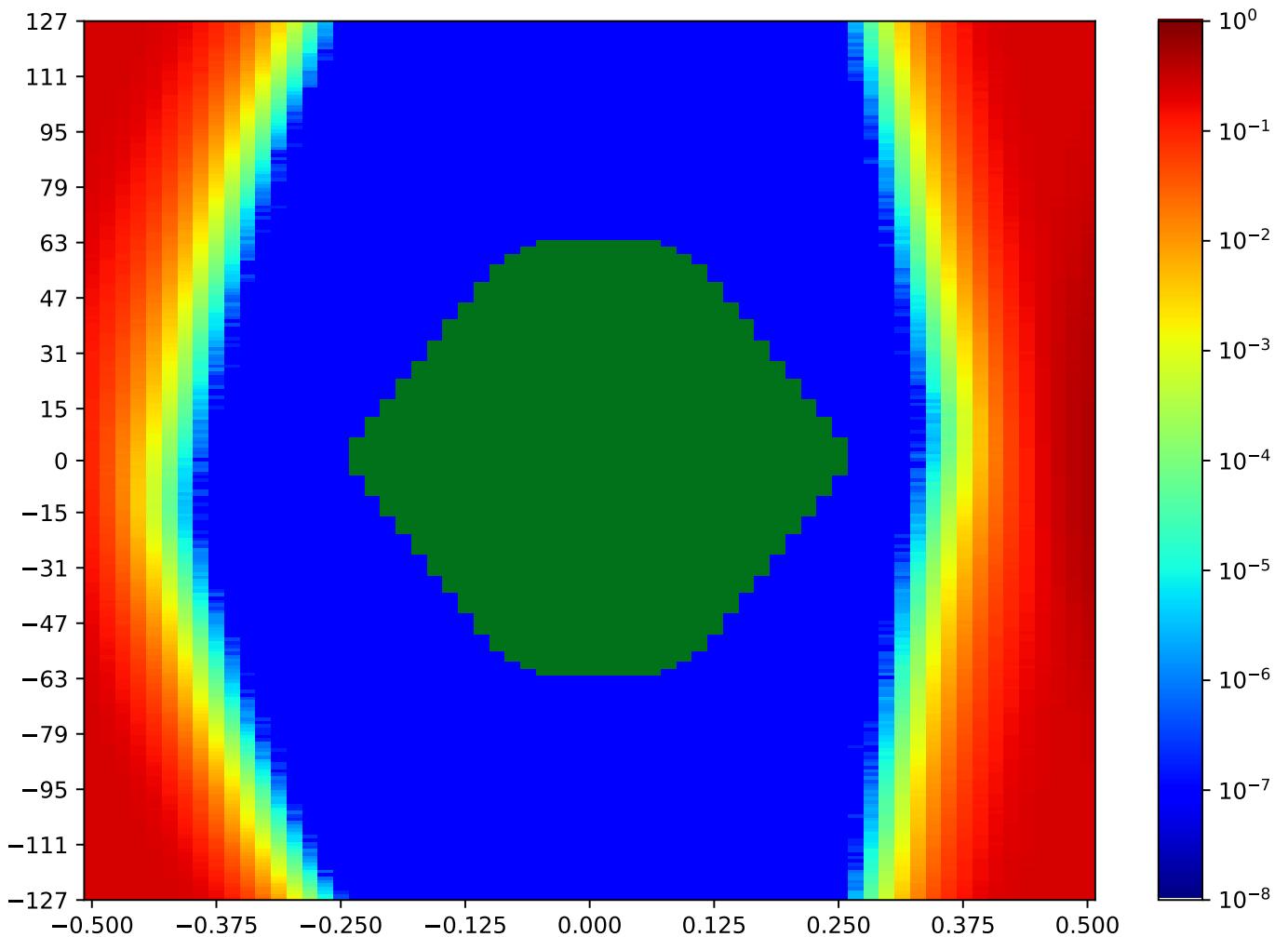


Figure 2.196: MSP_A_FPGA-TX1-07-RX11-07-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.9 MSP_A_FPGA-TX1-08-RX11-08-MSP_C_FPGA

Table 2.182: MSP_A_FPGA-TX1-08-RX11-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:54:13		2018-Jan-24 16:54:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10946	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

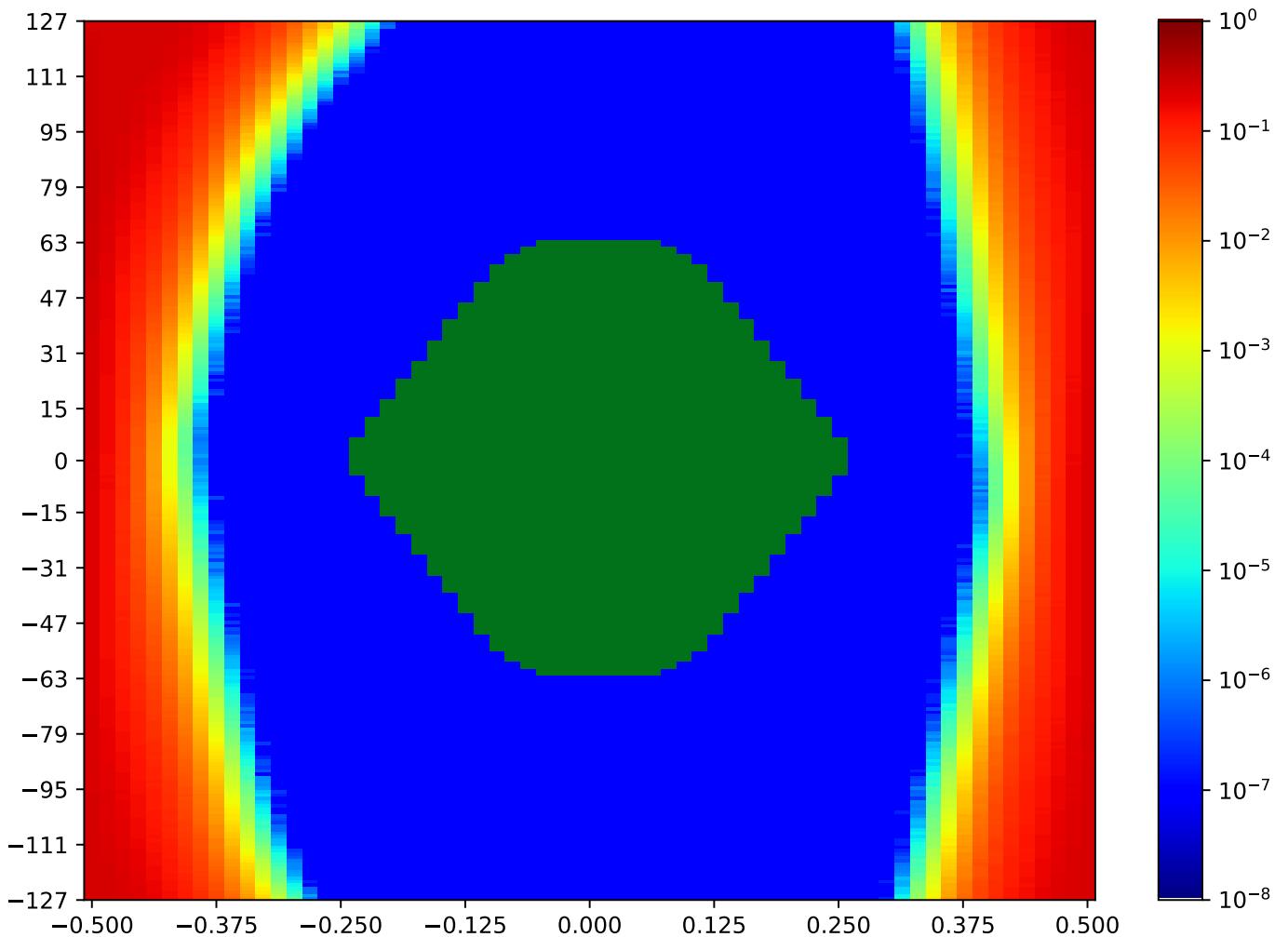


Figure 2.197: MSP_A_FPGA-TX1-08-RX11-08-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.10 MSP_A_FPGA-TX1-09-RX11-09-MSP_C_FPGA

Table 2.183: MSP_A_FPGA-TX1-09-RX11-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:50:42		2018-Jan-24 16:51:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9517	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

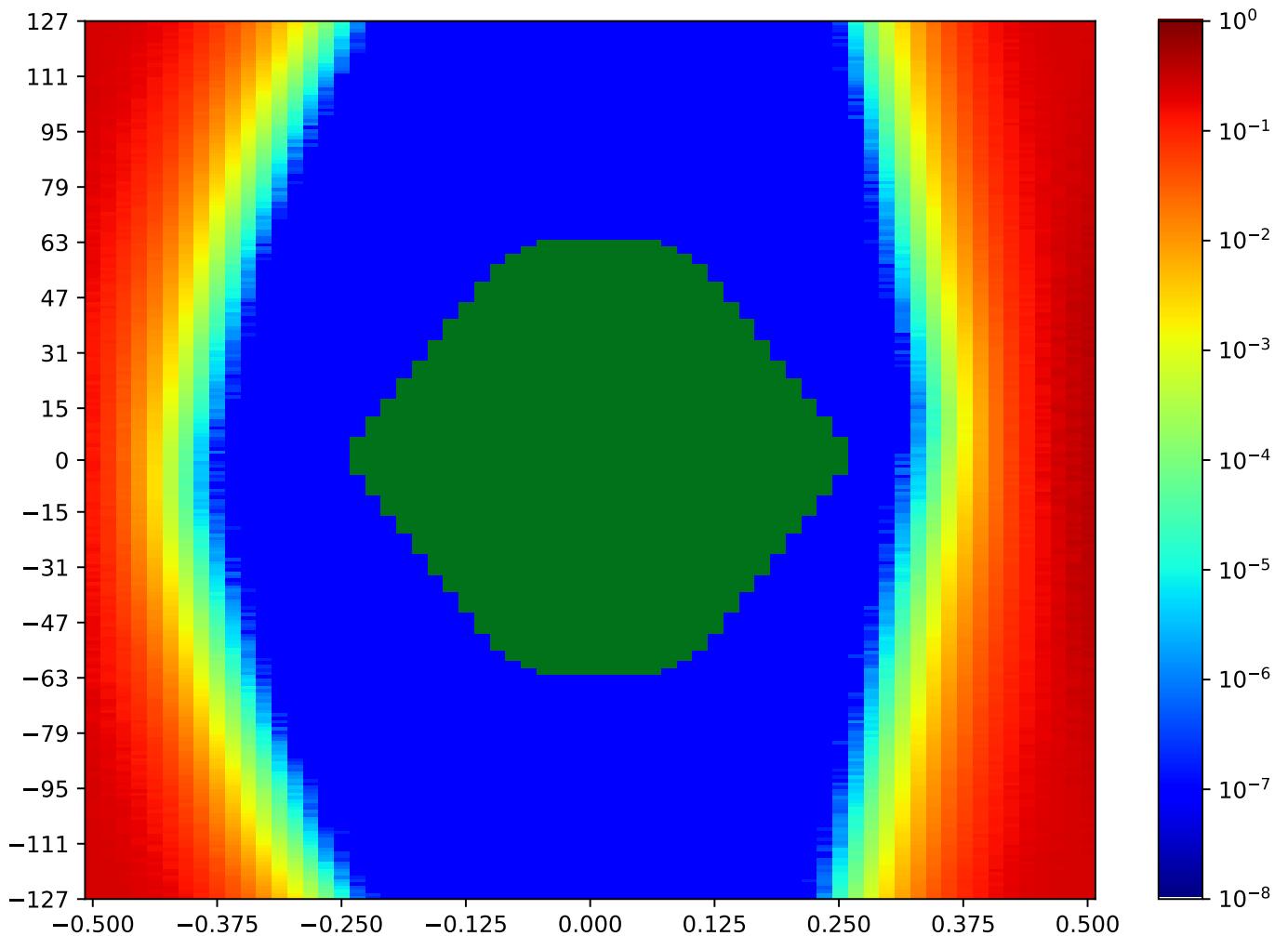


Figure 2.198: MSP_A_FPGA-TX1-09-RX11-09-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.11 MSP_A_FPGA-TX1-10-RX11-10-MSP_C_FPGA

Table 2.184: MSP_A_FPGA-TX1-10-RX11-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:53:02		2018-Jan-24 16:53:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10481	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

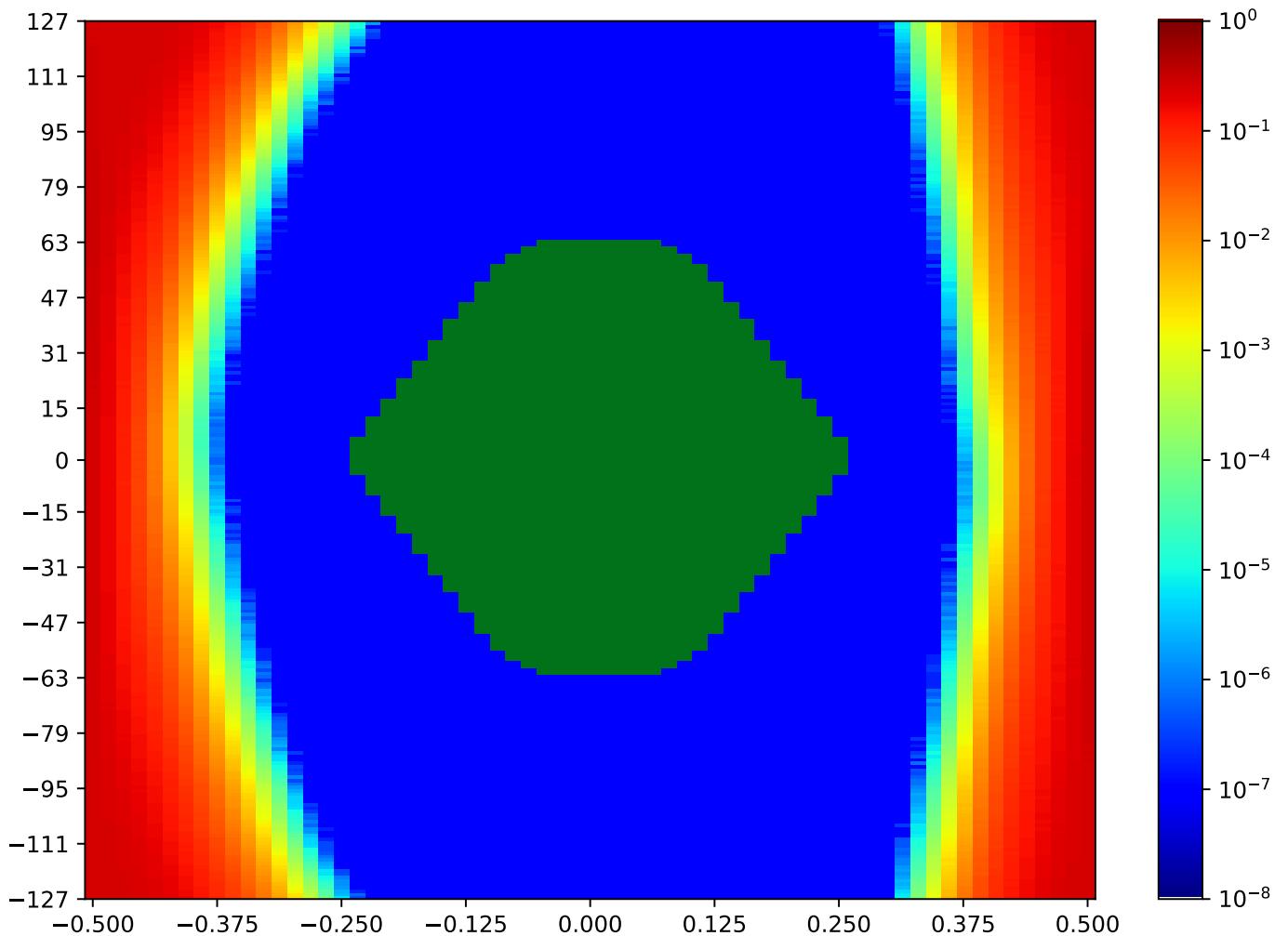


Figure 2.199: MSP_A_FPGA-TX1-10-RX11-10-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.15.12 MSP_A_FPGA-TX1-11-RX11-11-MSP_C_FPGA

Table 2.185: MSP_A_FPGA-TX1-11-RX11-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:52:27		2018-Jan-24 16:53:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9481	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

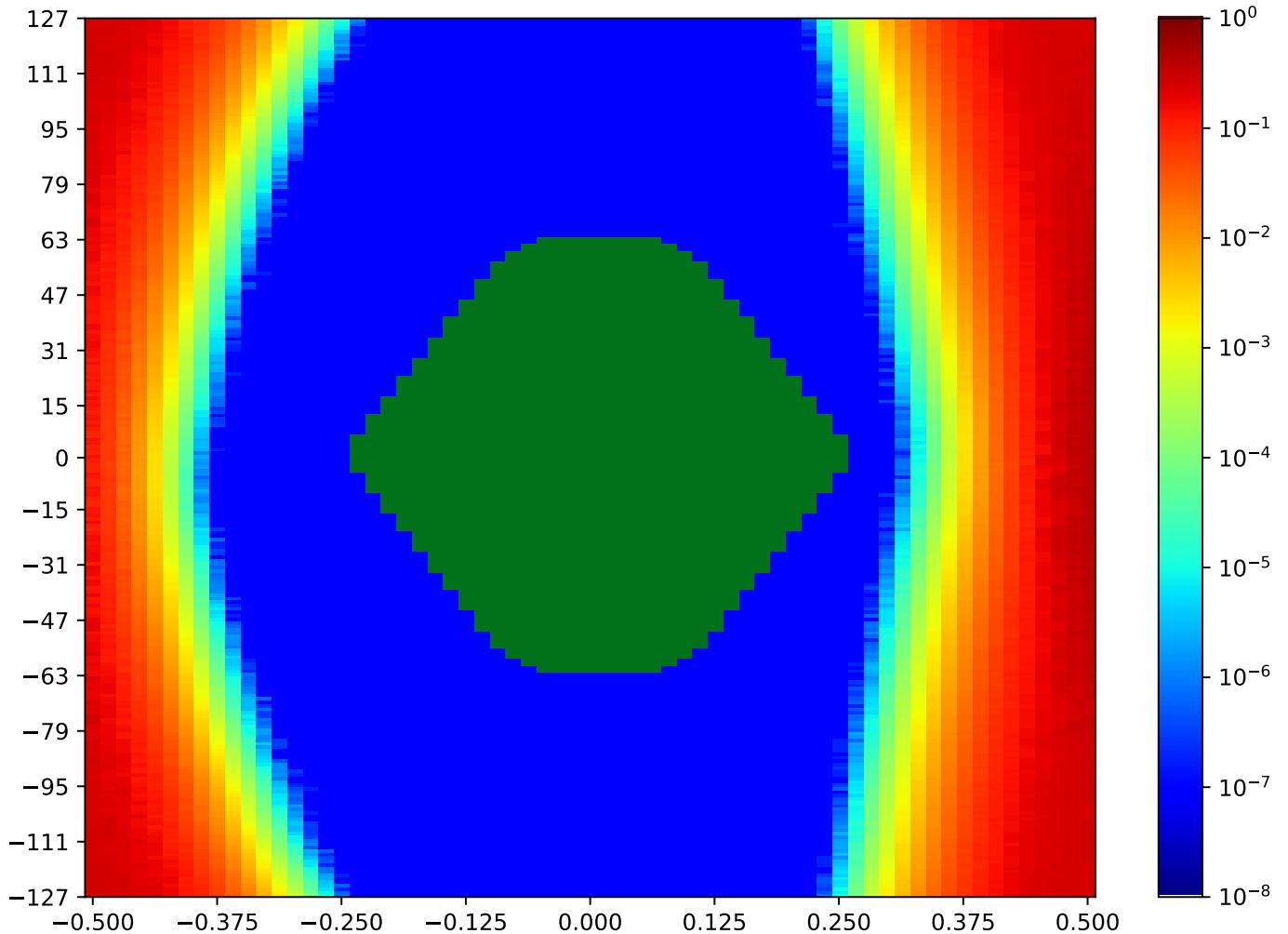


Figure 2.200: MSP_A_FPGA-TX1-11-RX11-11-MSP_C_FPGA

Call back to summary Figure 2.188. Sibling eye diagrams: V1-12.8.

2.16 MSP_A TX2 MSP_C RX10 Minipod Loopback

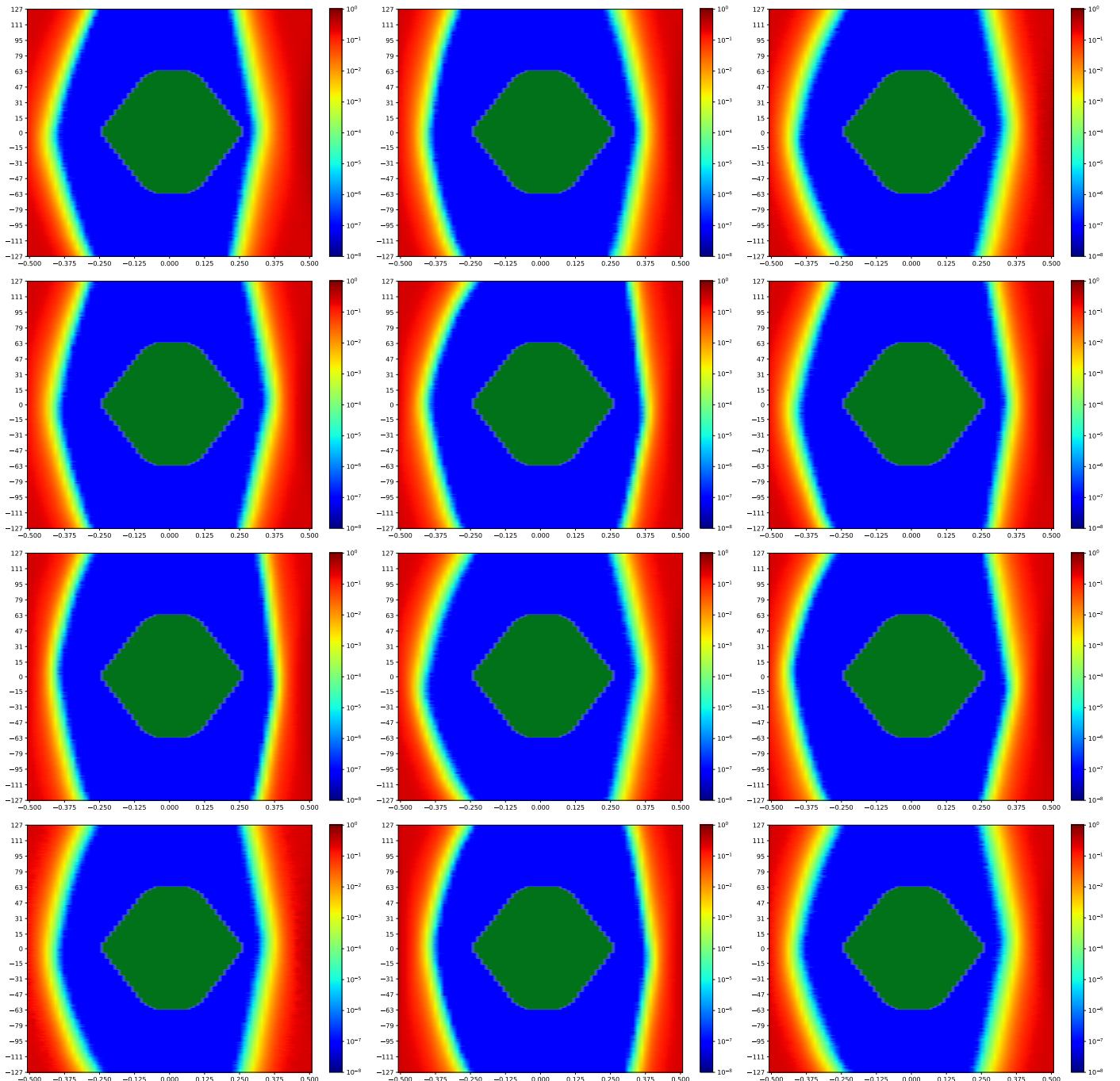


Figure 2.201: MSP_A TX2 MSP_C RX10 Minipod Loopback

A cross-reference to Figure 2.201. Sibling eye diagrams: V1-12.8.
Next summary Figure 2.214.

2.16.1 MSP_A_FPGA-TX2-00-RX10-00-MSP_C_FPGA

Table 2.186: MSP_A_FPGA-TX2-00-RX10-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:57:12		2018-Jan-24 16:57:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9347	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

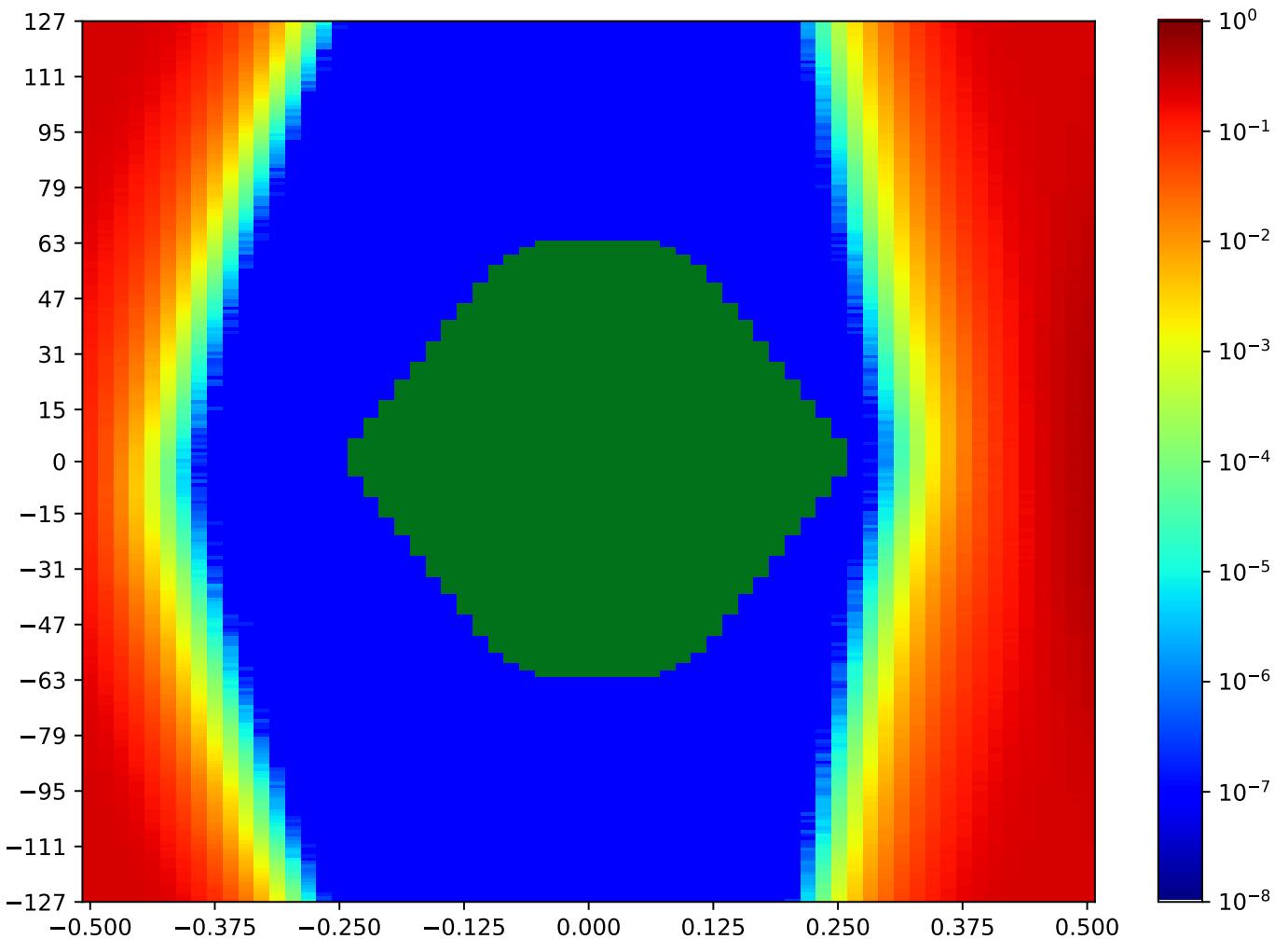


Figure 2.202: MSP_A_FPGA-TX2-00-RX10-00-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.2 MSP_A_FPGA-TX2-01-RX10-01-MSP_C_FPGA

Table 2.187: MSP_A_FPGA-TX2-01-RX10-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:56:01		2018-Jan-24 16:56:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10109	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

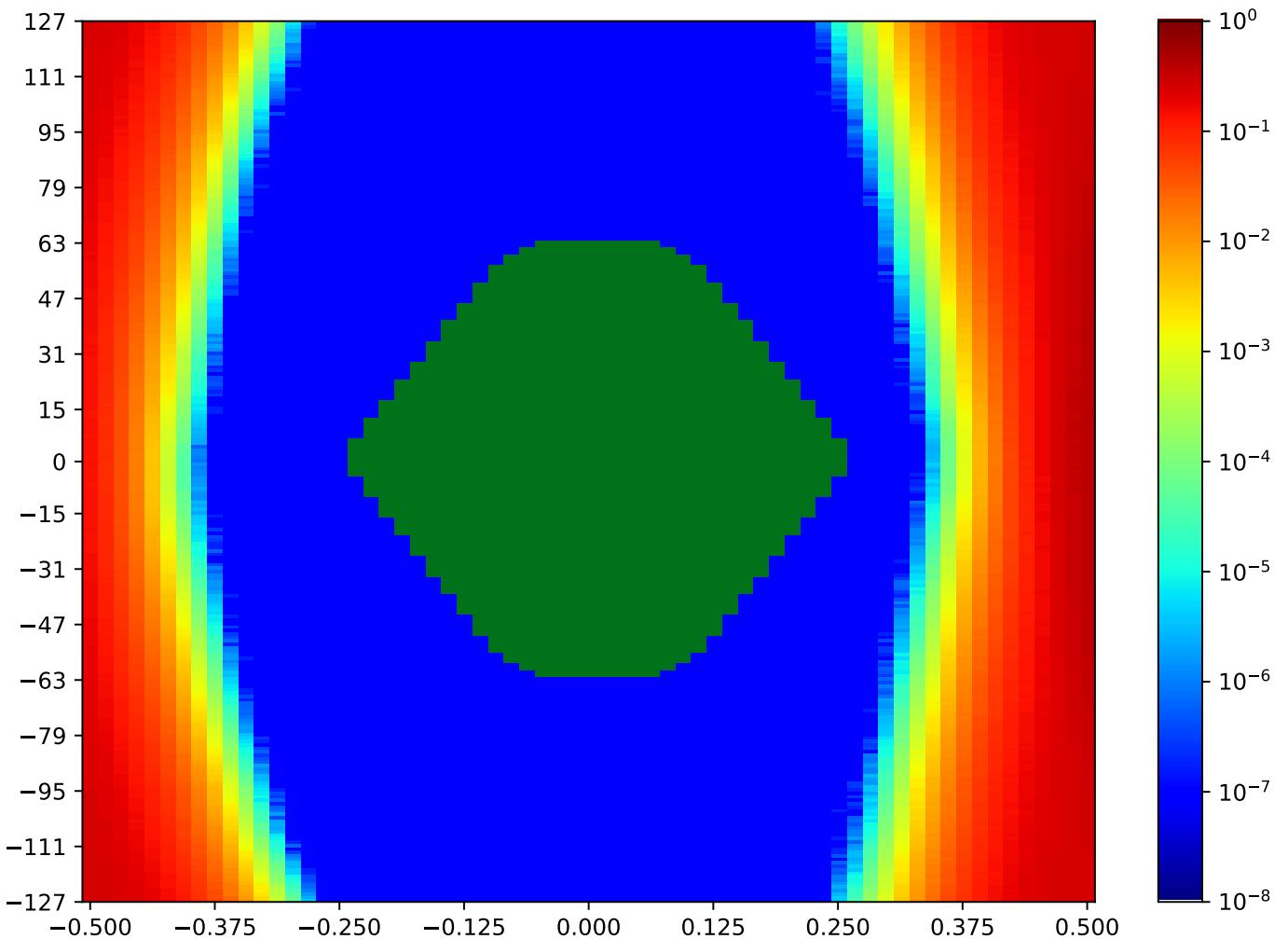


Figure 2.203: MSP_A_FPGA-TX2-01-RX10-01-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.3 MSP_A_FPGA-TX2-02-RX10-02-MSP_C_FPGA

Table 2.188: MSP_A_FPGA-TX2-02-RX10-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:59:00		2018-Jan-24 16:59:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9467	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

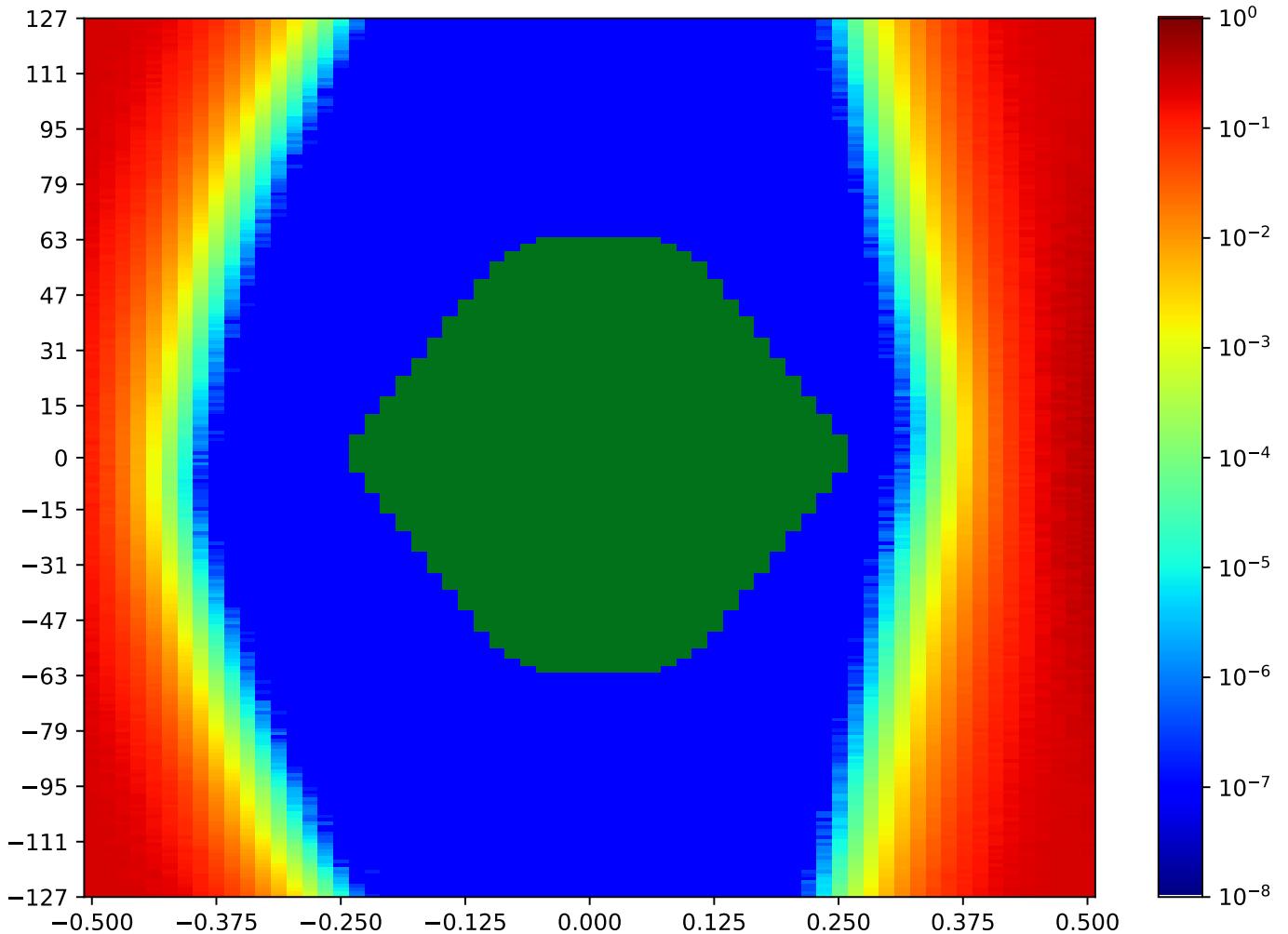


Figure 2.204: MSP_A_FPGA-TX2-02-RX10-02-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.4 MSP_A_FPGA-TX2-03-RX10-03-MSP_C_FPGA

Table 2.189: MSP_A_FPGA-TX2-03-RX10-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:55:25		2018-Jan-24 16:56:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10061	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

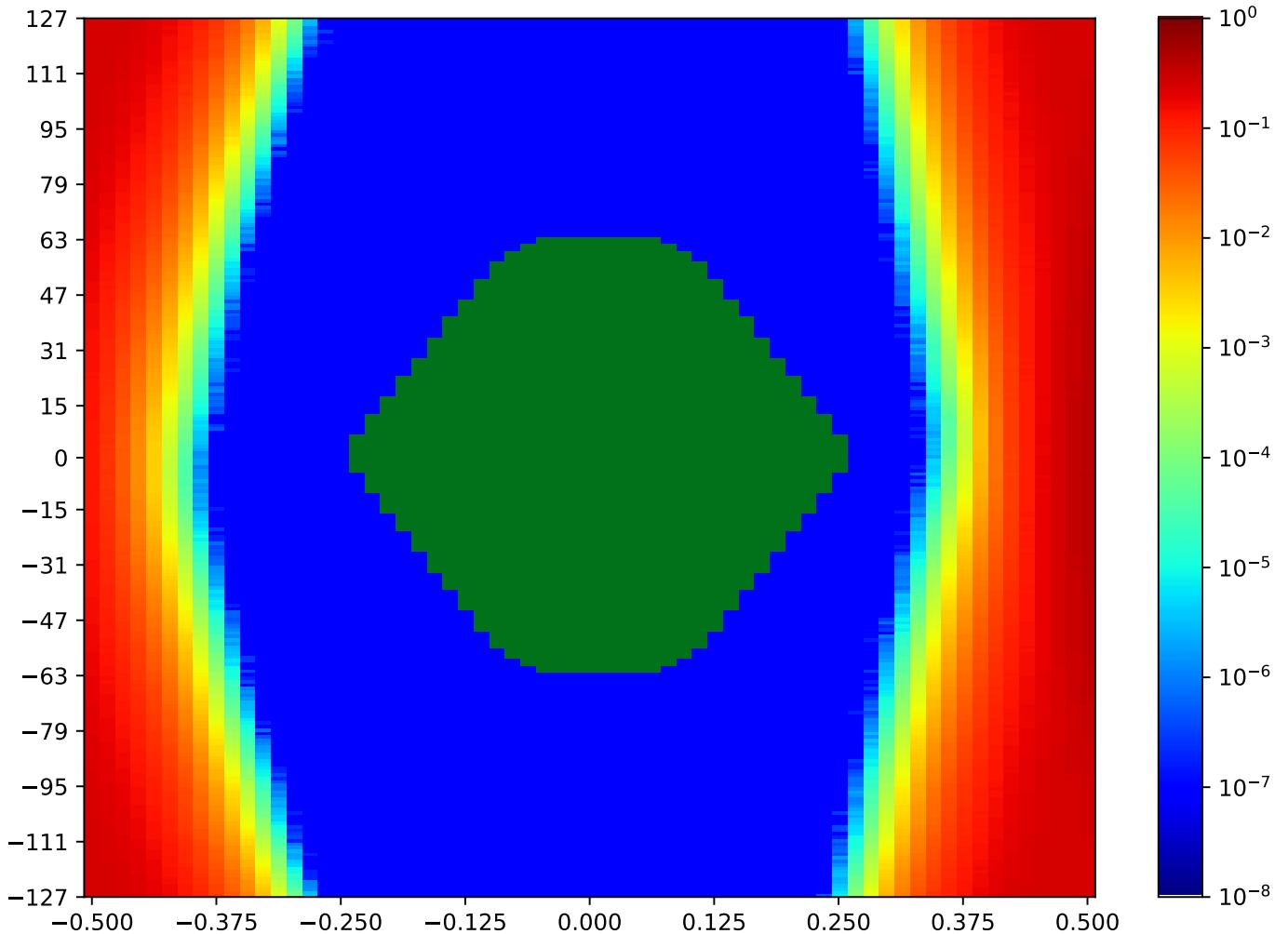


Figure 2.205: MSP_A_FPGA-TX2-03-RX10-03-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.5 MSP_A_FPGA-TX2-04-RX10-04-MSP_C_FPGA

Table 2.190: MSP_A_FPGA-TX2-04-RX10-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:00:49		2018-Jan-24 17:01:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10520	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

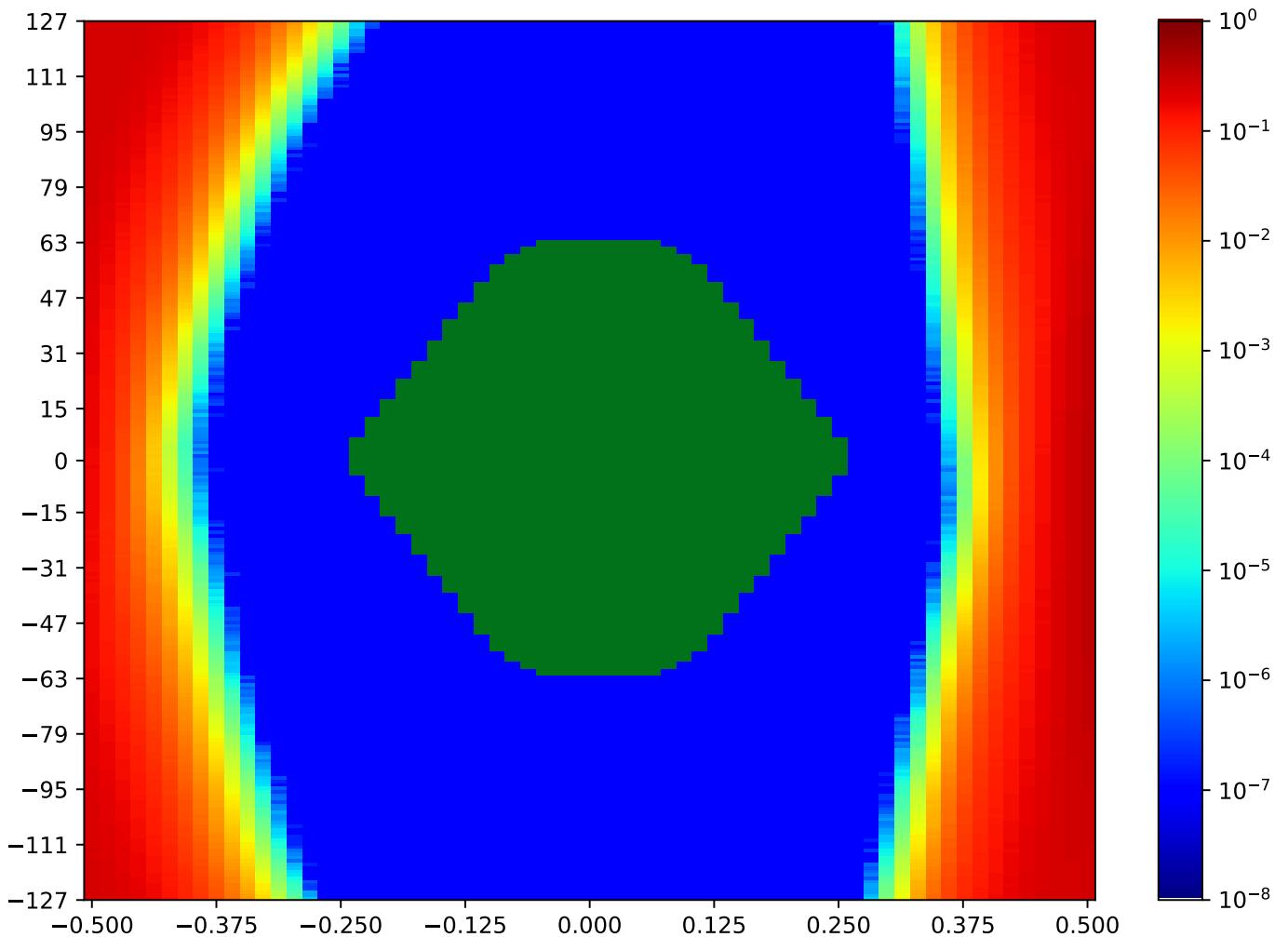


Figure 2.206: MSP_A_FPGA-TX2-04-RX10-04-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.6 MSP_A_FPGA-TX2-05-RX10-05-MSP_C_FPGA

Table 2.191: MSP_A_FPGA-TX2-05-RX10-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:56:37		2018-Jan-24 16:57:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10066	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

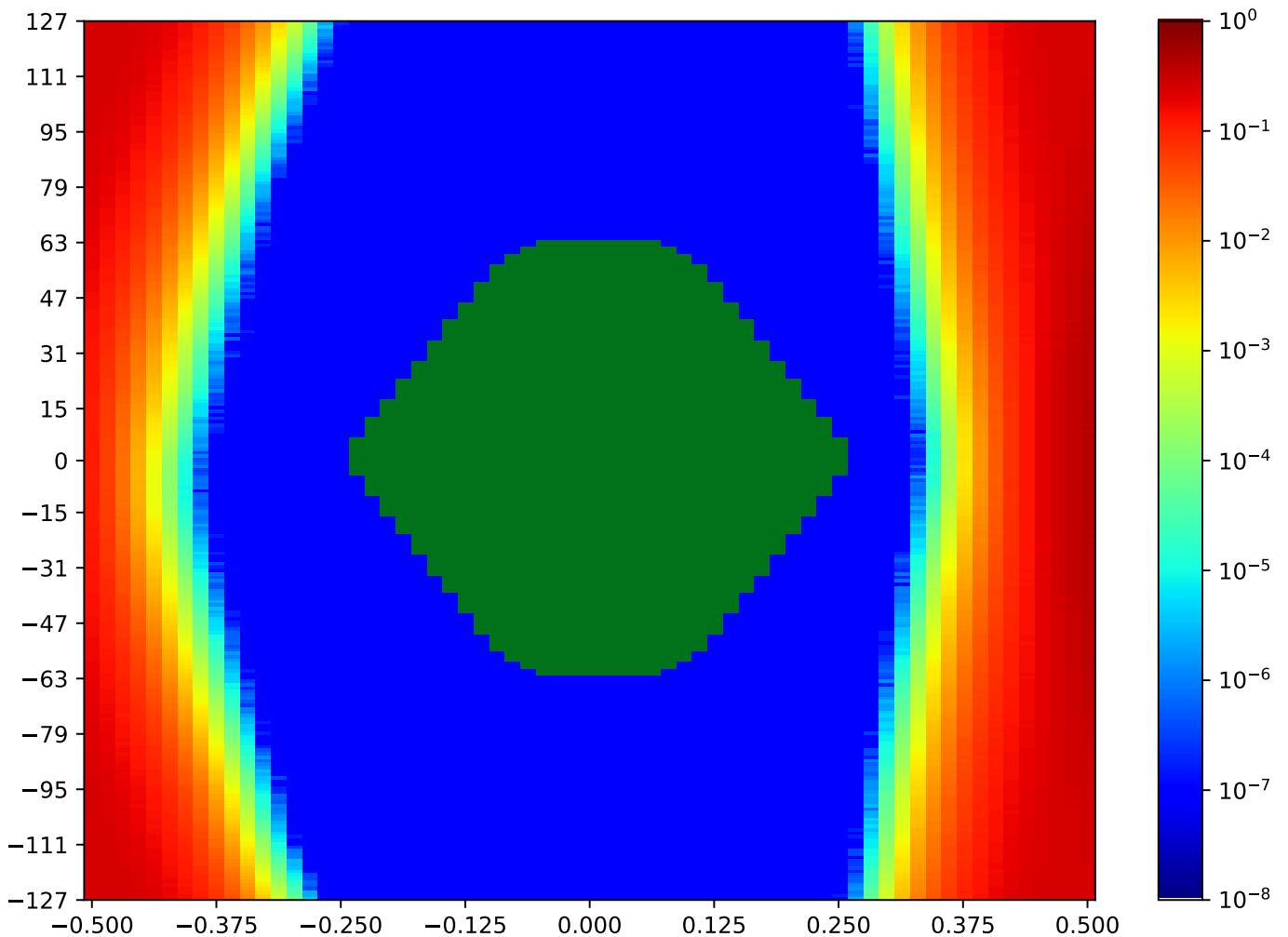


Figure 2.207: MSP_A_FPGA-TX2-05-RX10-05-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.7 MSP_A_FPGA-TX2-06-RX10-06-MSP_C_FPGA

Table 2.192: MSP_A_FPGA-TX2-06-RX10-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:02:03		2018-Jan-24 17:02:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10811	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

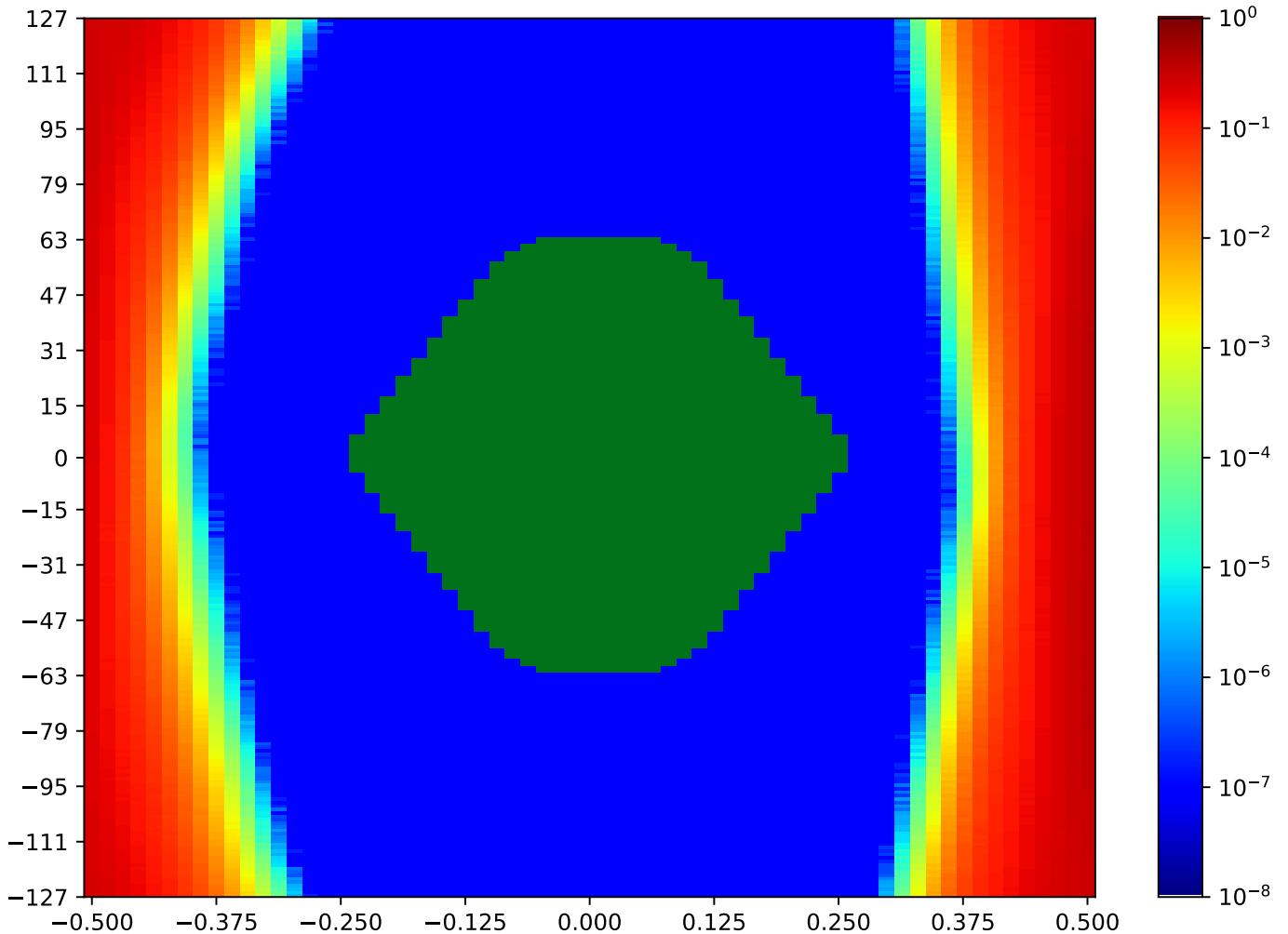


Figure 2.208: MSP_A_FPGA-TX2-06-RX10-06-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.8 MSP_A_FPGA-TX2-07-RX10-07-MSP_C_FPGA

Table 2.193: MSP_A_FPGA-TX2-07-RX10-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:57:47		2018-Jan-24 16:58:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9804	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

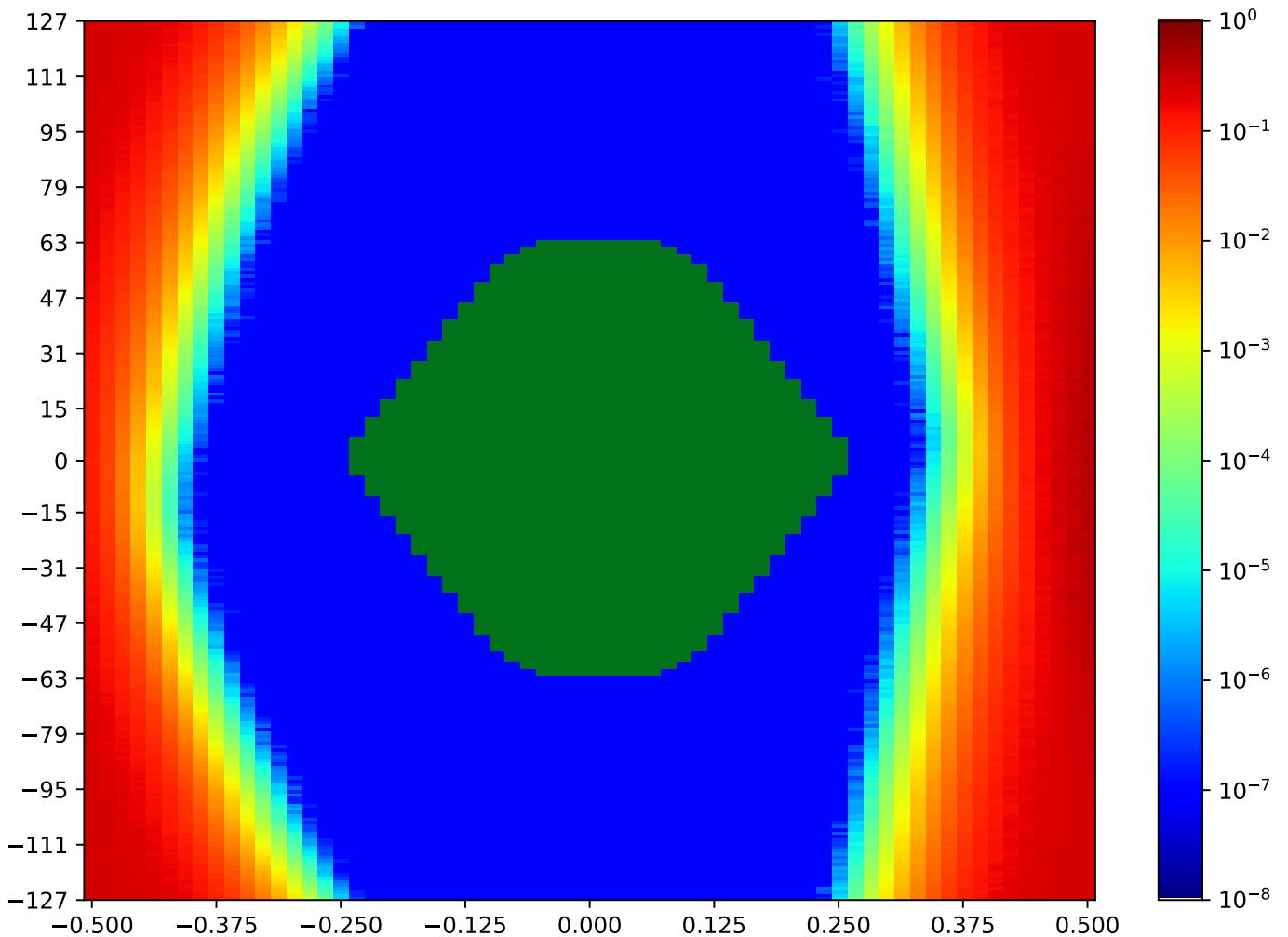


Figure 2.209: MSP_A_FPGA-TX2-07-RX10-07-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.9 MSP_A_FPGA-TX2-08-RX10-08-MSP_C_FPGA

Table 2.194: MSP_A_FPGA-TX2-08-RX10-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:01:26		2018-Jan-24 17:02:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10399	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

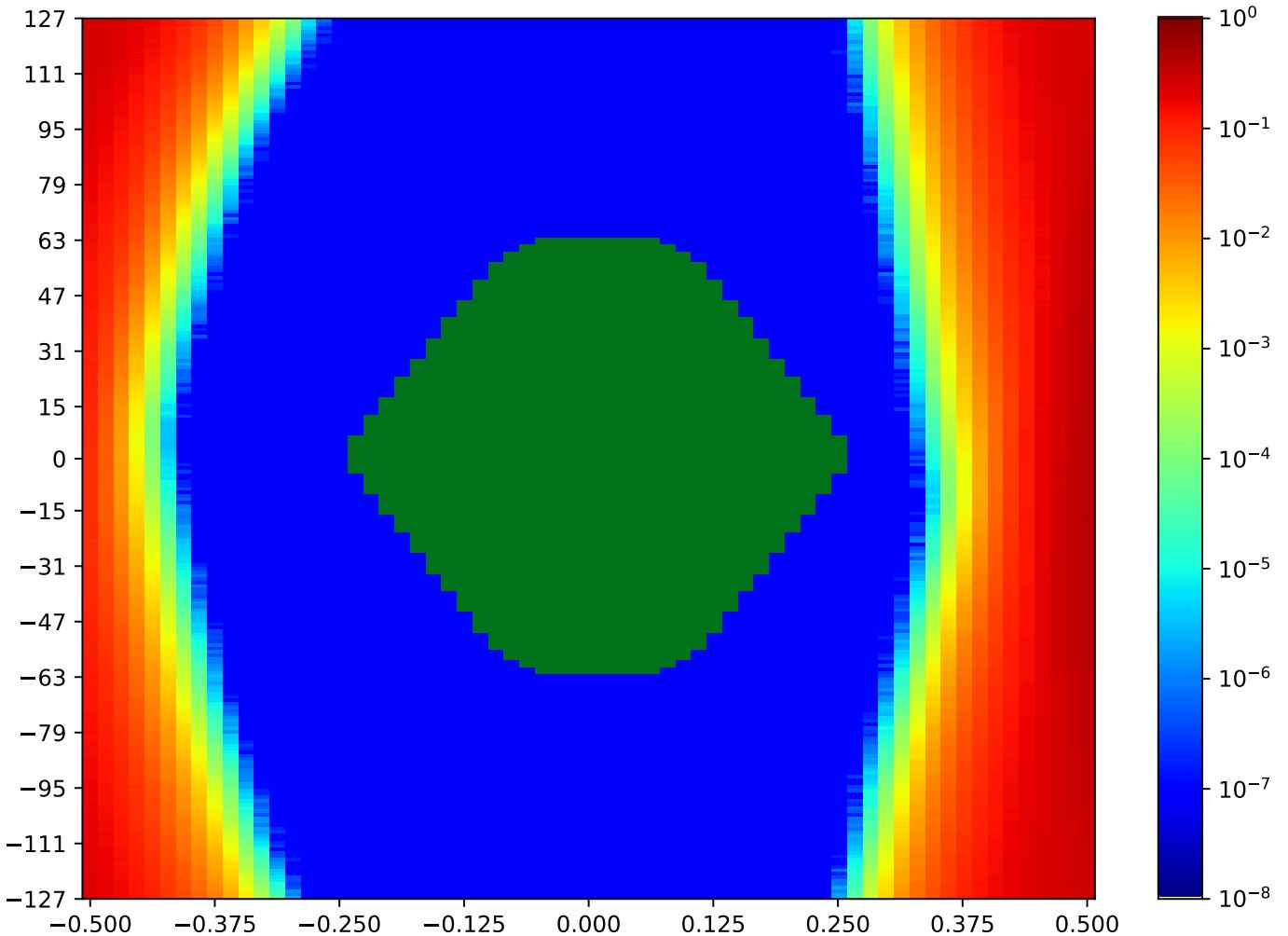


Figure 2.210: MSP_A_FPGA-TX2-08-RX10-08-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.10 MSP_A_FPGA-TX2-09-RX10-09-MSP_C_FPGA

Table 2.195: MSP_A_FPGA-TX2-09-RX10-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:58:23		2018-Jan-24 16:59:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9677	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

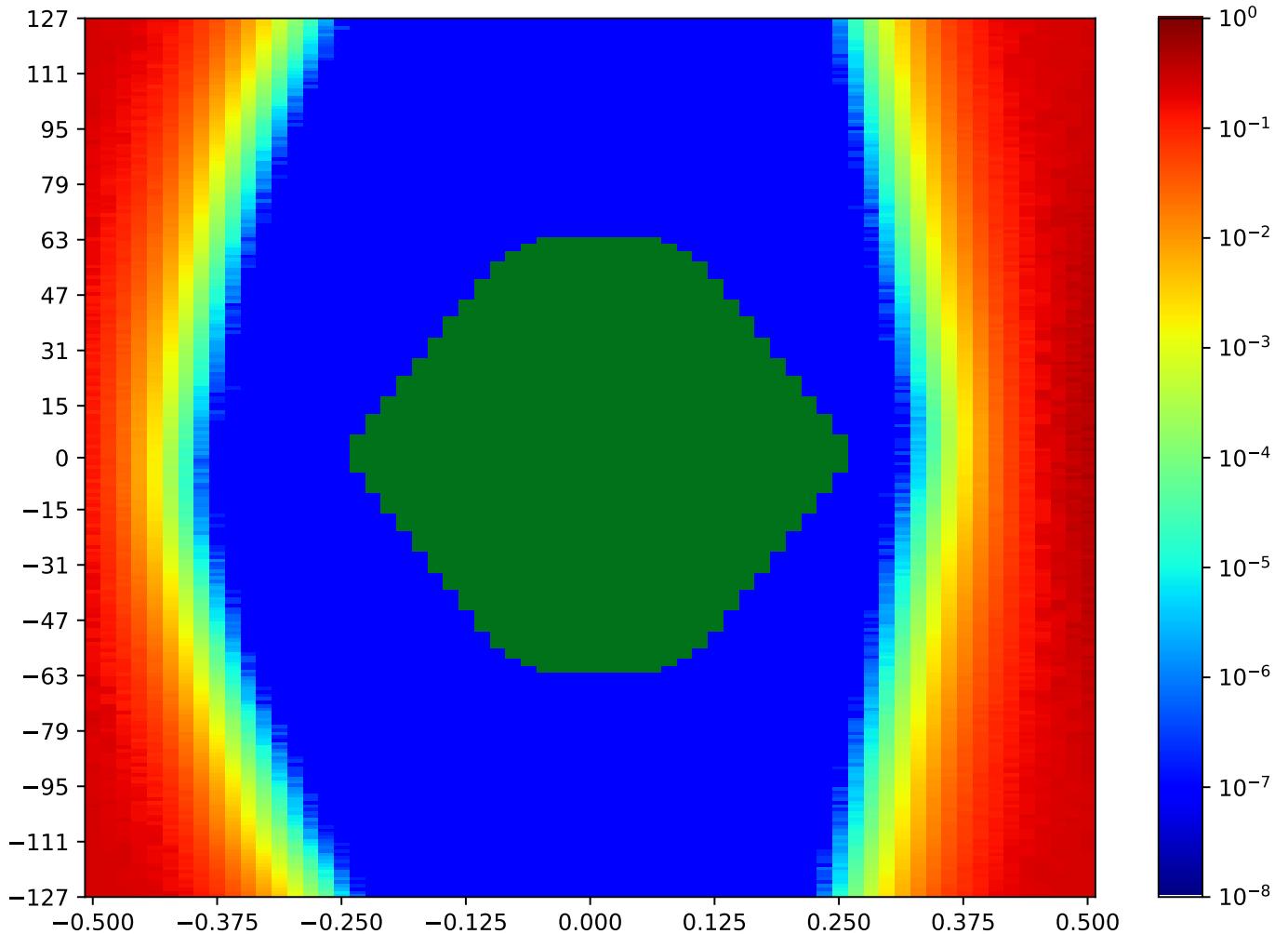


Figure 2.211: MSP_A_FPGA-TX2-09-RX10-09-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.11 MSP_A_FPGA-TX2-10-RX10-10-MSP_C_FPGA

Table 2.196: MSP_A_FPGA-TX2-10-RX10-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:00:13		2018-Jan-24 17:00:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10521	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

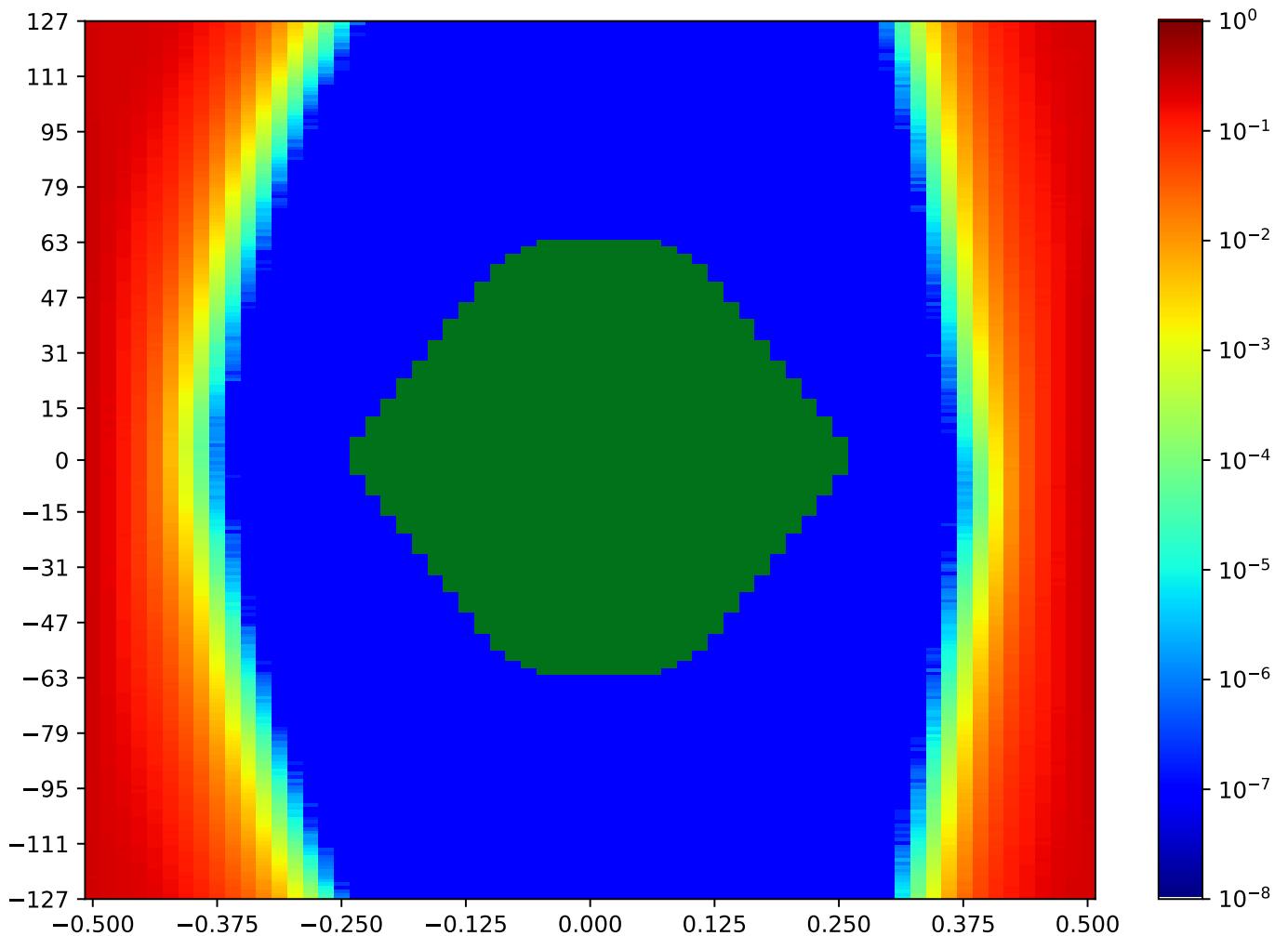


Figure 2.212: MSP_A_FPGA-TX2-10-RX10-10-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.16.12 MSP_A_FPGA-TX2-11-RX10-11-MSP_C_FPGA

Table 2.197: MSP_A_FPGA-TX2-11-RX10-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 16:59:36		2018-Jan-24 17:00:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9373	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

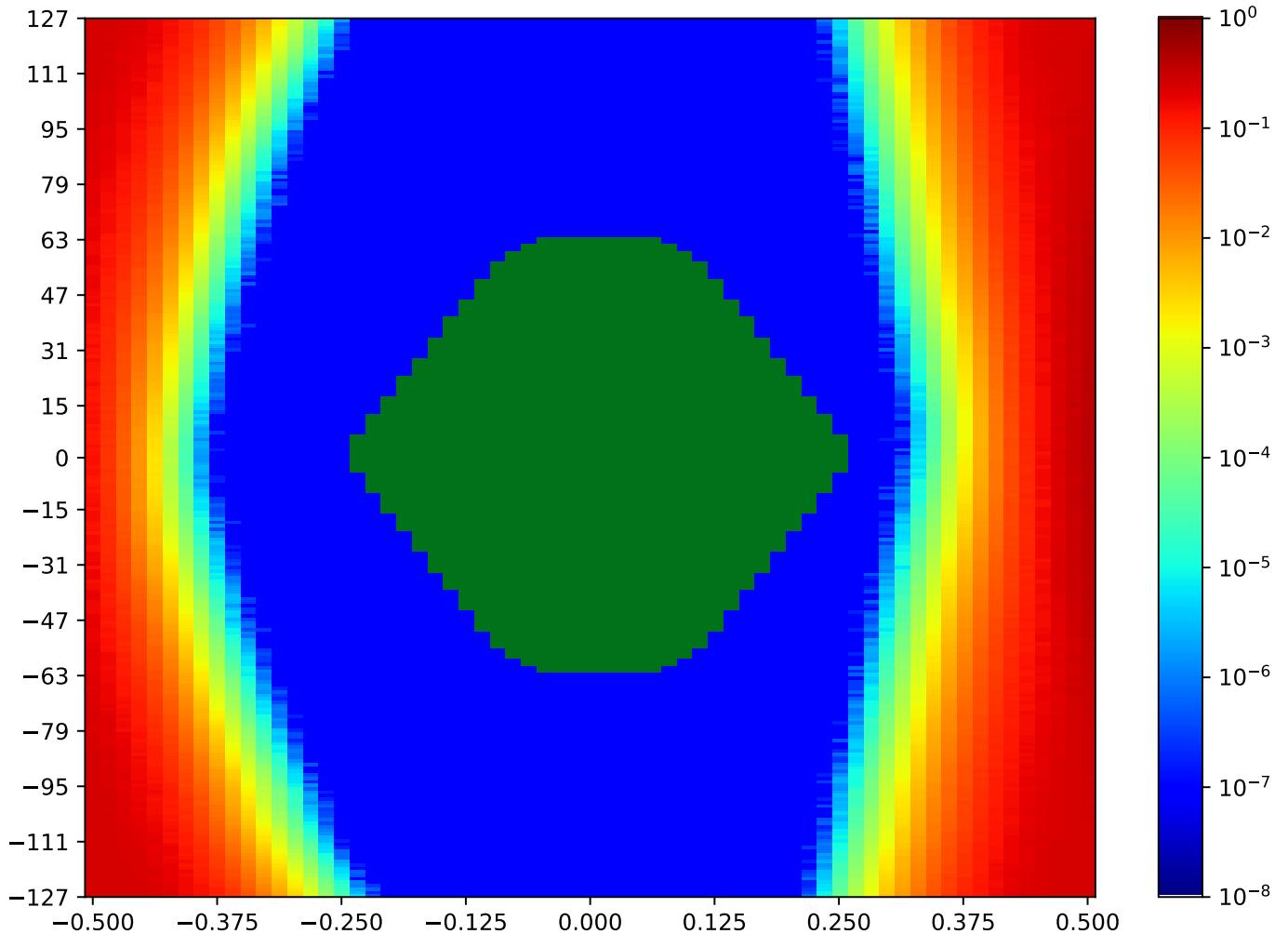


Figure 2.213: MSP_A_FPGA-TX2-11-RX10-11-MSP_C_FPGA

Call back to summary Figure 2.201. Sibling eye diagrams: V1-12.8.

2.17 MSP_C TX3 MSP_A RX2 Minipod Loopback

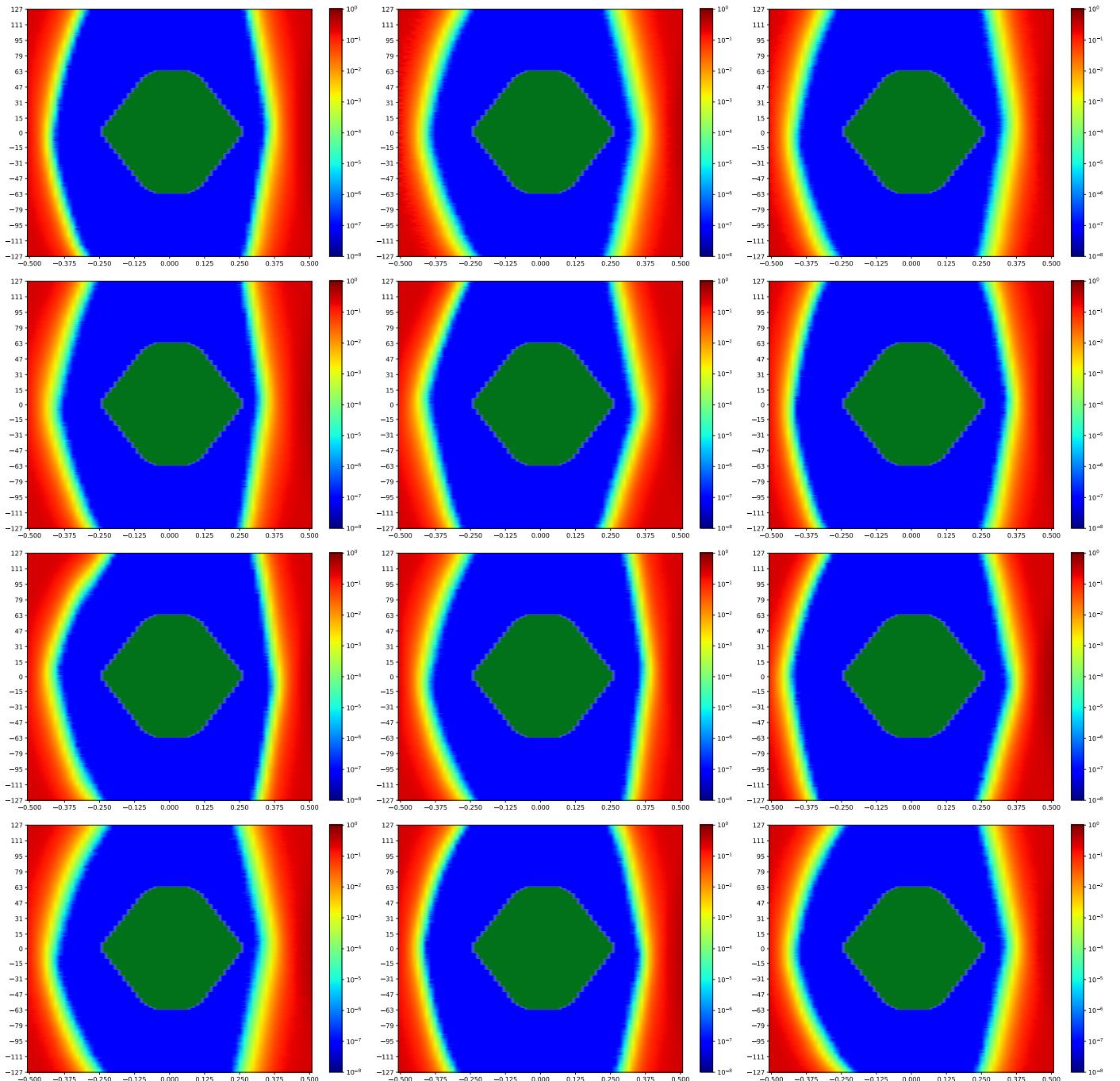


Figure 2.214: MSP_C TX3 MSP_A RX2 Minipod Loopback

A cross-reference to Figure 2.214. Sibling eye diagrams: V1-12.8.
Next summary Figure 2.227.

2.17.1 MSP_C_FPGA-TX3-00-RX2-00-MSP_A_FPGA

Table 2.198: MSP_C_FPGA-TX3-00-RX2-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:04:29		2018-Jan-24 17:05:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10572	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

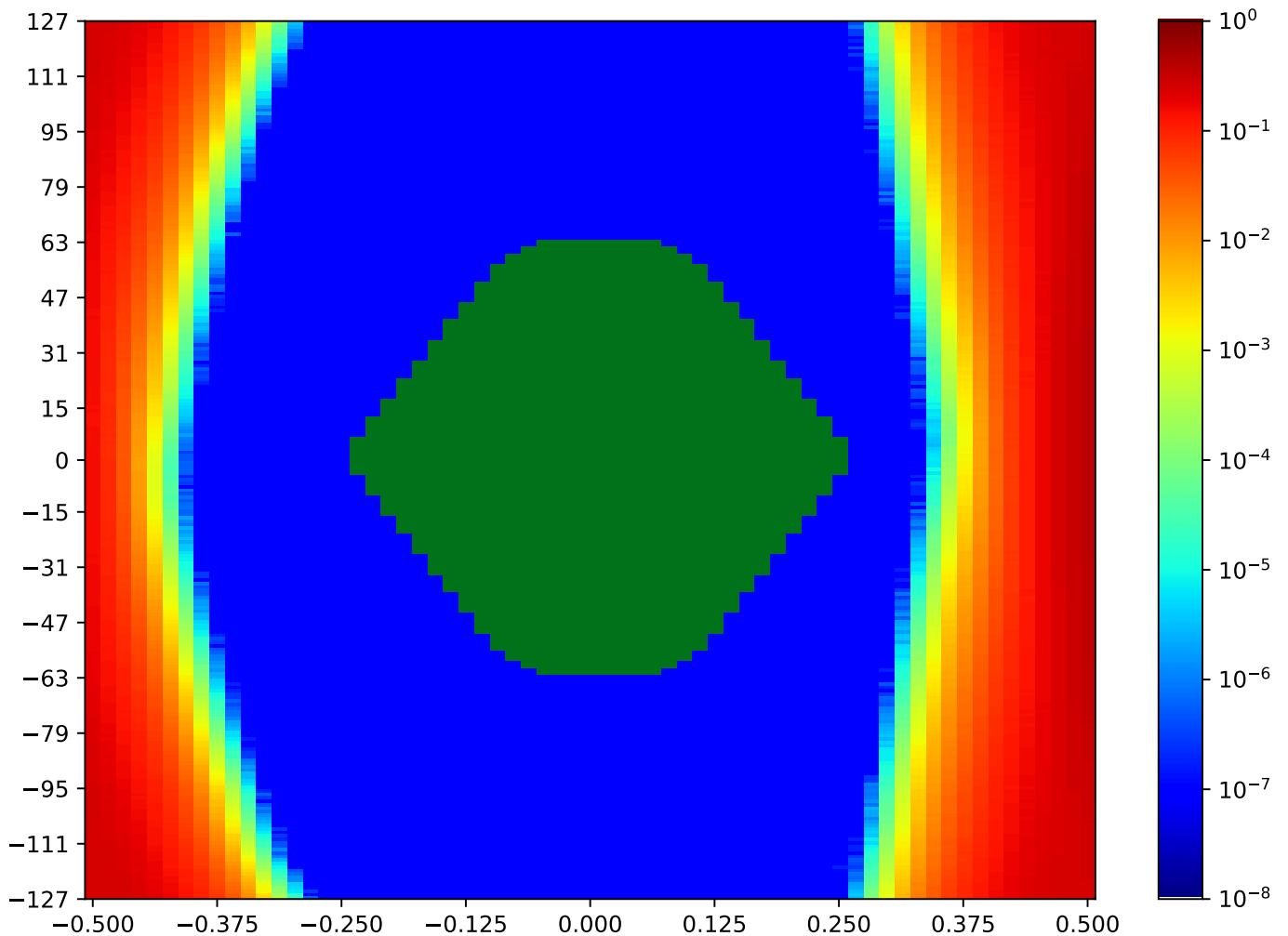


Figure 2.215: MSP_C_FPGA-TX3-00-RX2-00-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.2 MSP_C_FPGA-TX3-01-RX2-01-MSP_A_FPGA

Table 2.199: MSP_C_FPGA-TX3-01-RX2-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:05:42		2018-Jan-24 17:06:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9499	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

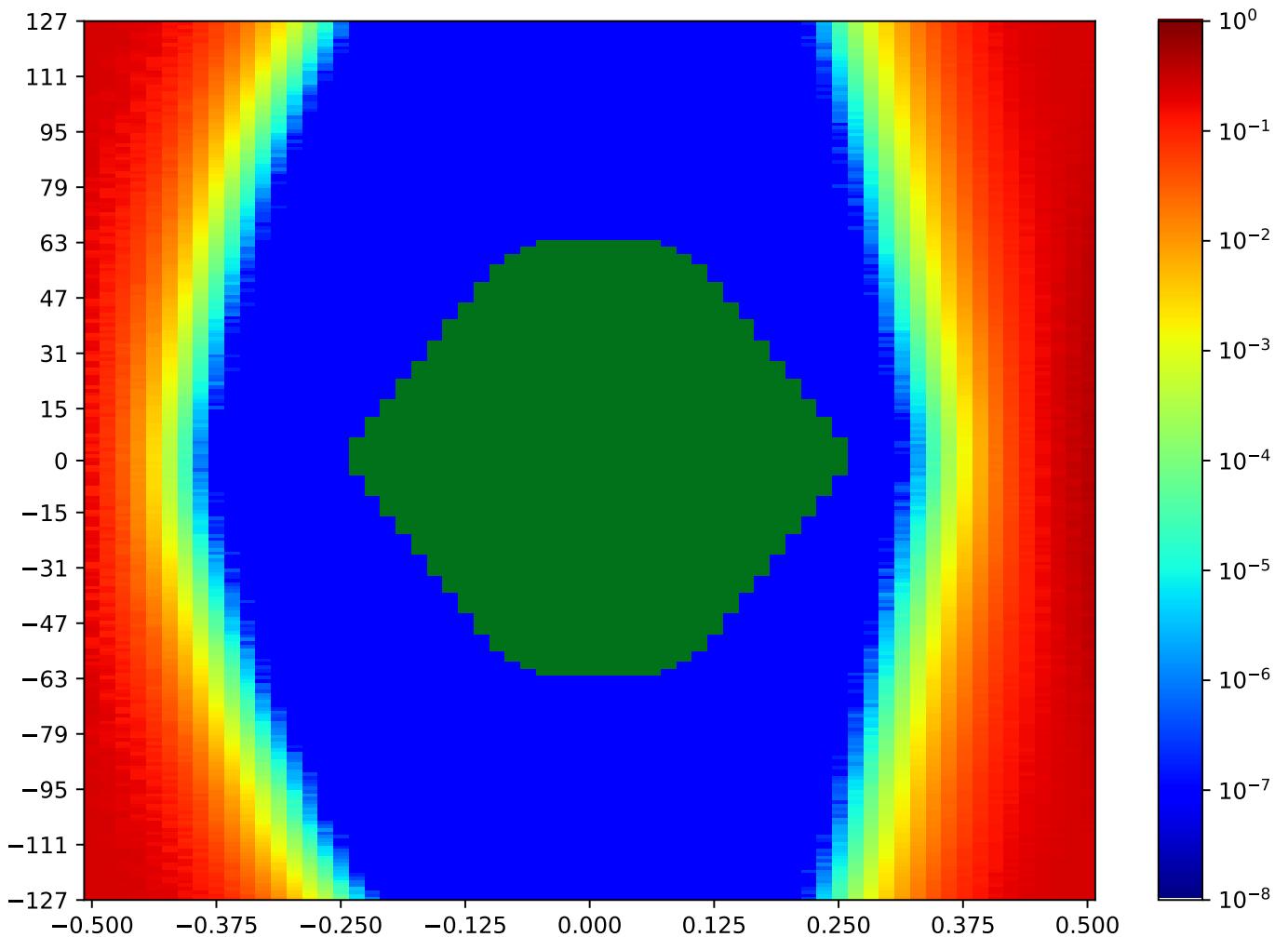


Figure 2.216: MSP_C_FPGA-TX3-01-RX2-01-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.3 MSP_C_FPGA-TX3-02-RX2-02-MSP_A_FPGA

Table 2.200: MSP_C_FPGA-TX3-02-RX2-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:06:20		2018-Jan-24 17:06:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9884	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

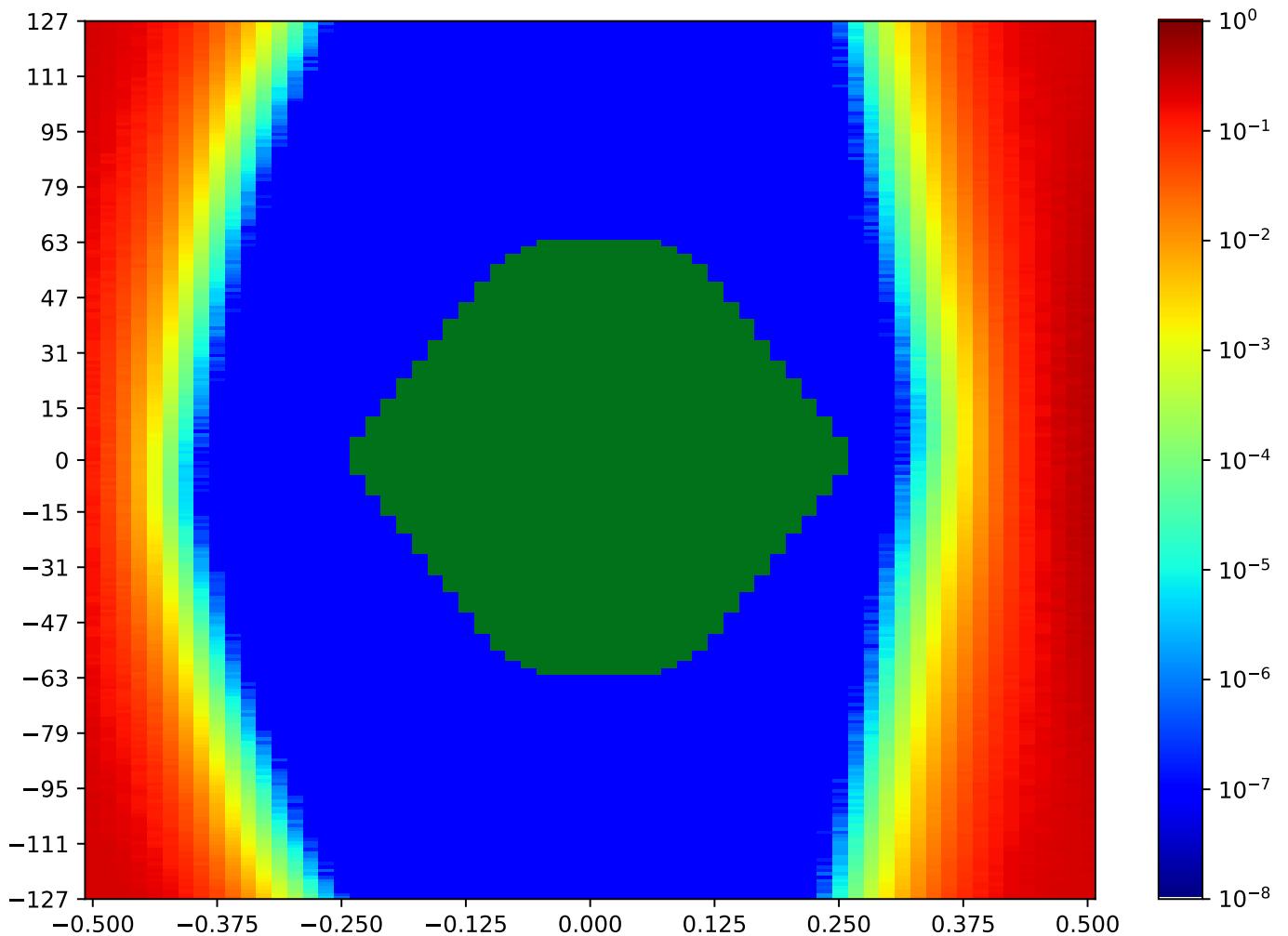


Figure 2.217: MSP_C_FPGA-TX3-02-RX2-02-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.4 MSP_C_FPGA-TX3-03-RX2-03-MSP_A_FPGA

Table 2.201: MSP_C_FPGA-TX3-03-RX2-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:03:16		2018-Jan-24 17:03:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9661	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

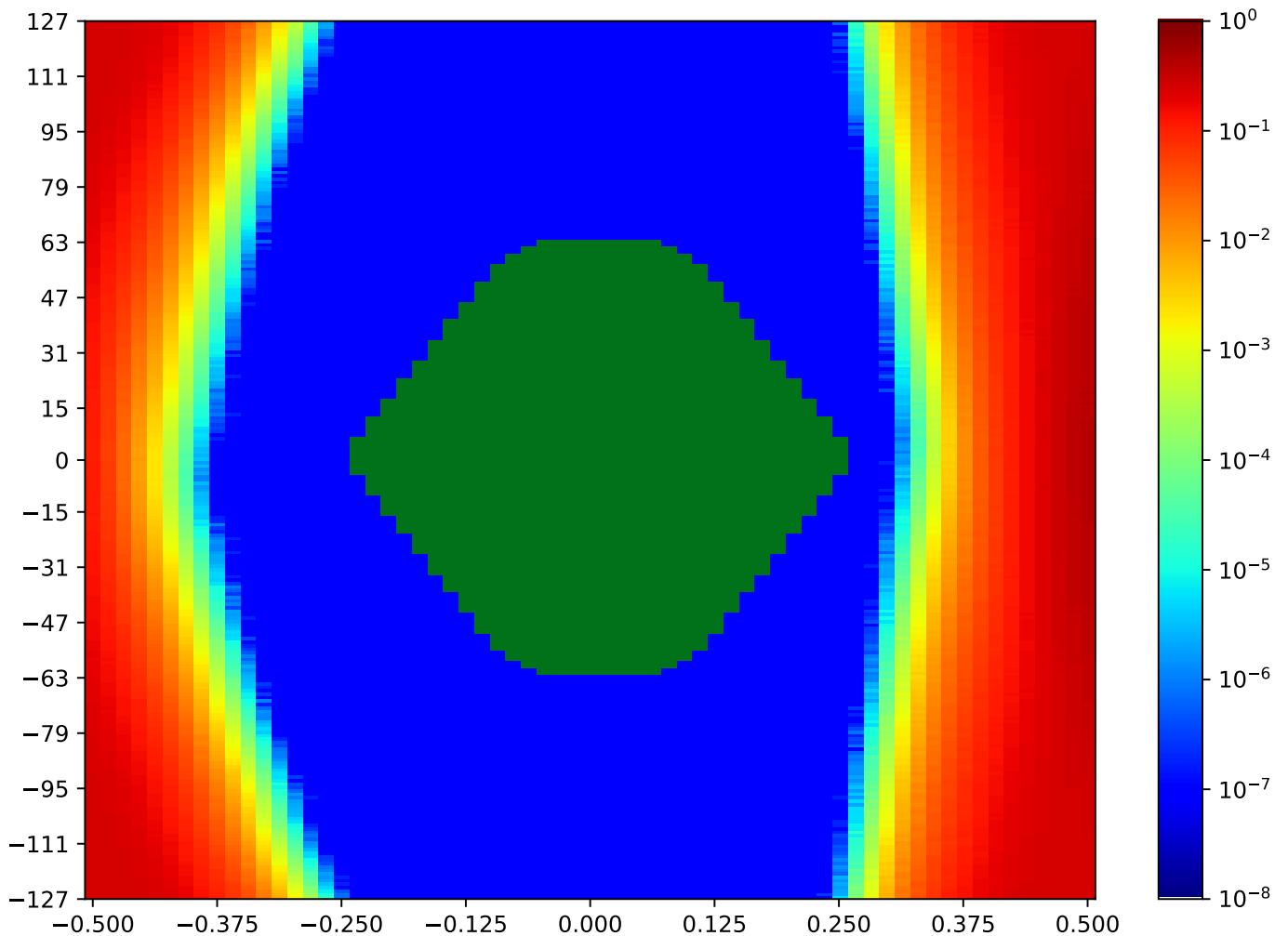


Figure 2.218: MSP_C_FPGA-TX3-03-RX2-03-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.5 MSP_C_FPGA-TX3-04-RX2-04-MSP_A_FPGA

Table 2.202: MSP_C_FPGA-TX3-04-RX2-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:08:11		2018-Jan-24 17:08:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9647	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

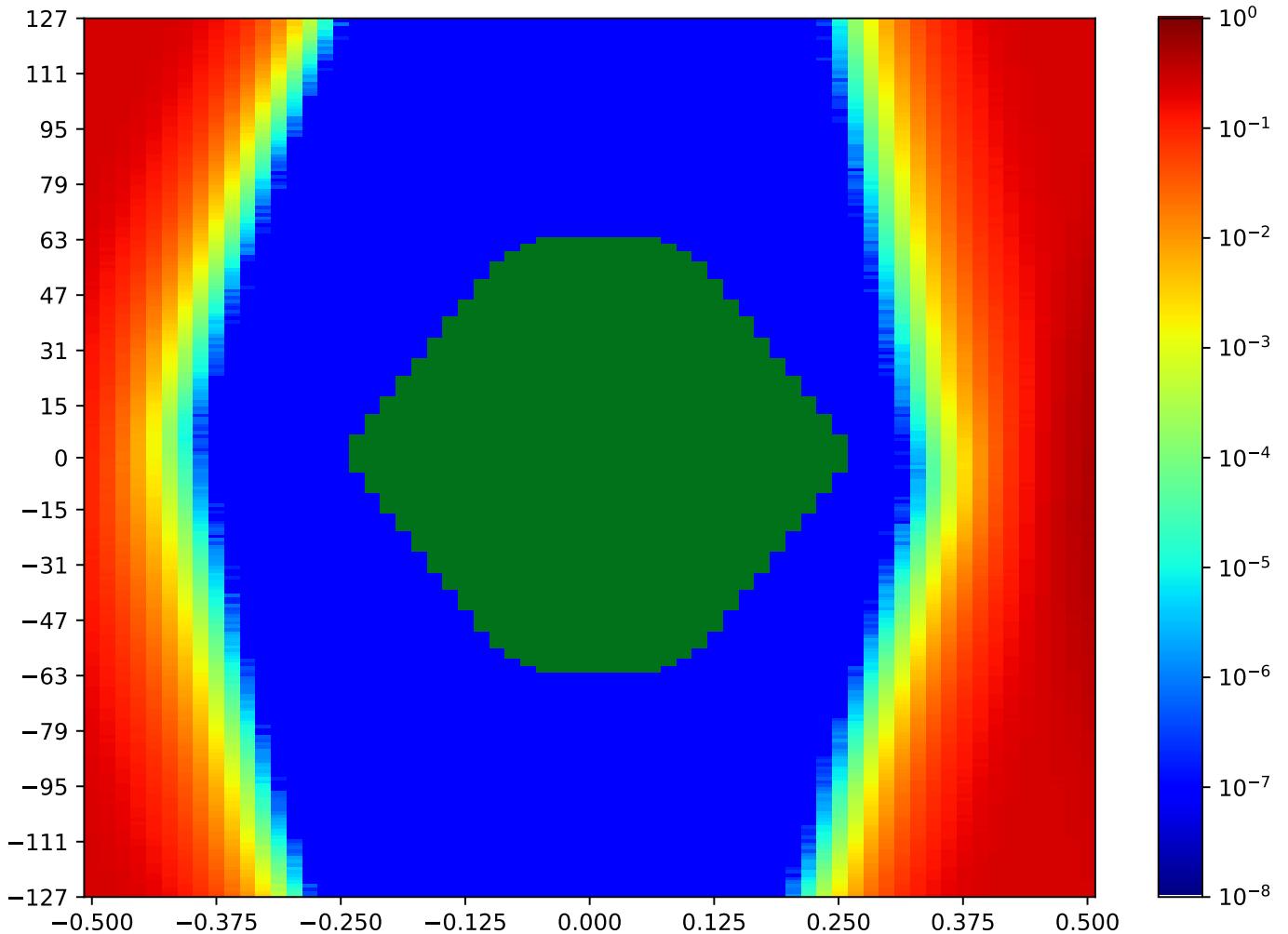


Figure 2.219: MSP_C_FPGA-TX3-04-RX2-04-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.6 MSP_C_FPGA-TX3-05-RX2-05-MSP_A_FPGA

Table 2.203: MSP_C_FPGA-TX3-05-RX2-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:02:40		2018-Jan-24 17:03:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10571	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

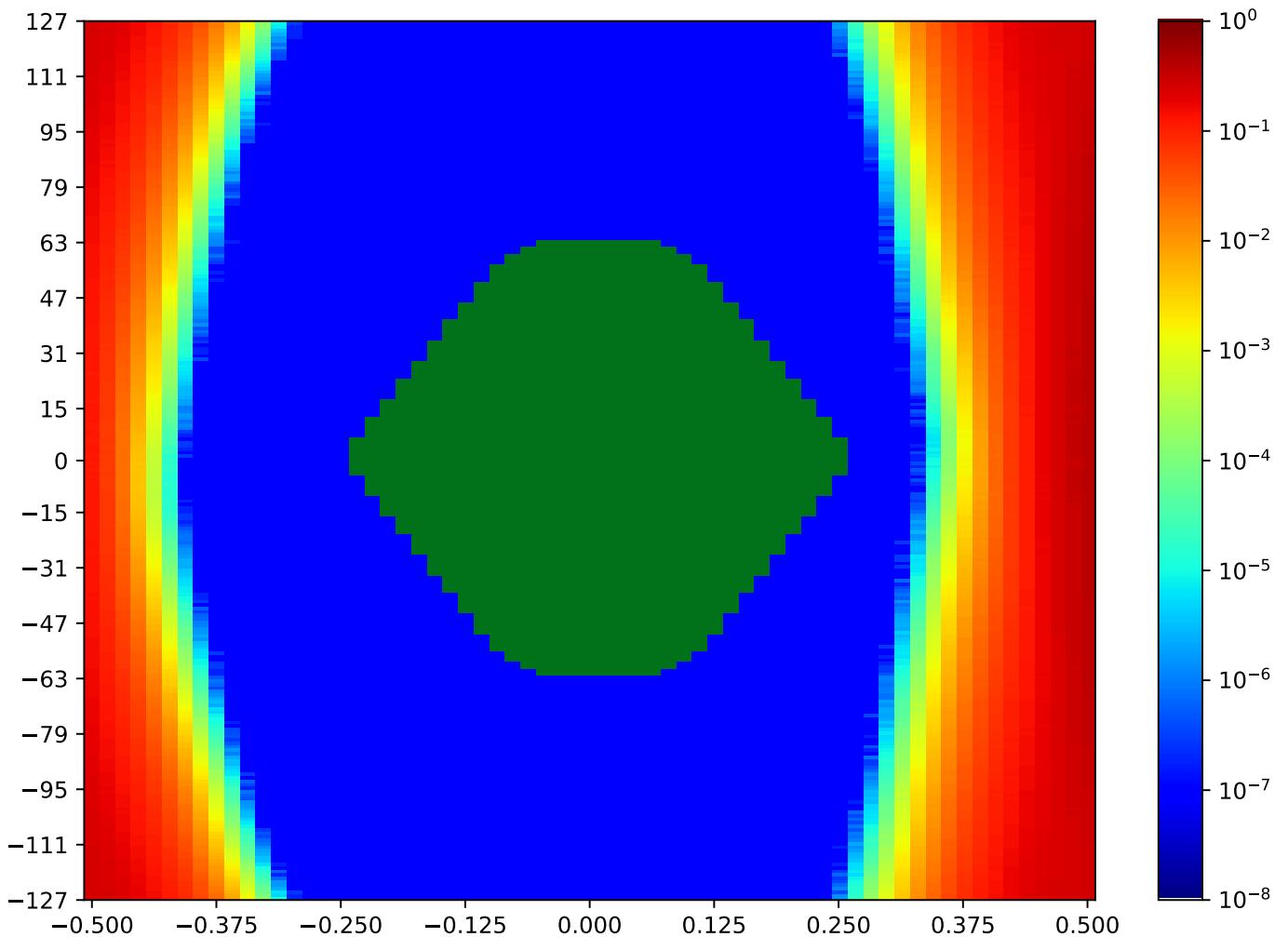


Figure 2.220: MSP_C_FPGA-TX3-05-RX2-05-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.7 MSP_C_FPGA-TX3-06-RX2-06-MSP_A_FPGA

Table 2.204: MSP_C_FPGA-TX3-06-RX2-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:09:24		2018-Jan-24 17:10:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10302	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

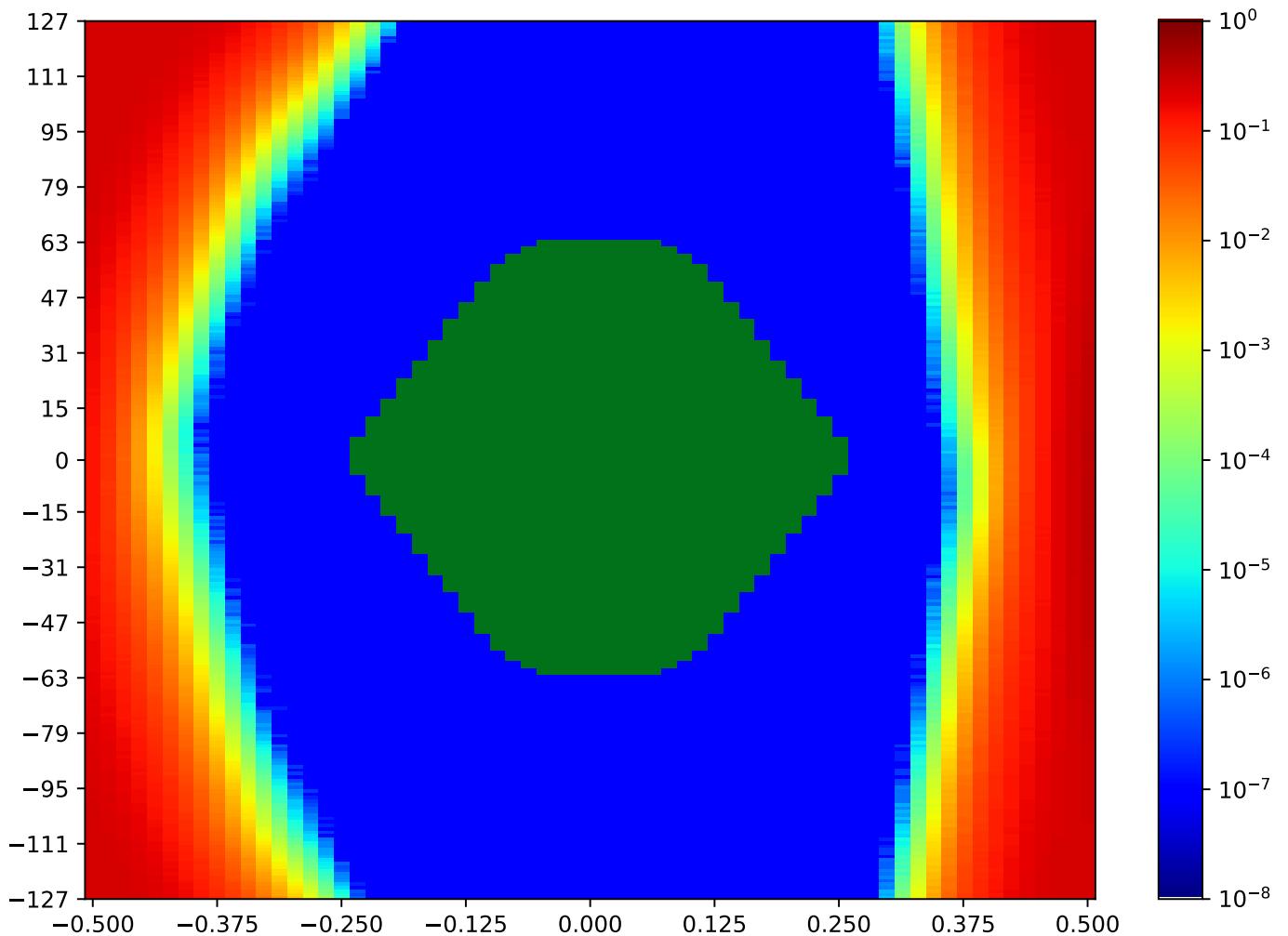


Figure 2.221: MSP_C_FPGA-TX3-06-RX2-06-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.8 MSP_C_FPGA-TX3-07-RX2-07-MSP_A_FPGA

Table 2.205: MSP_C_FPGA-TX3-07-RX2-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:03:51		2018-Jan-24 17:04:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10336	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

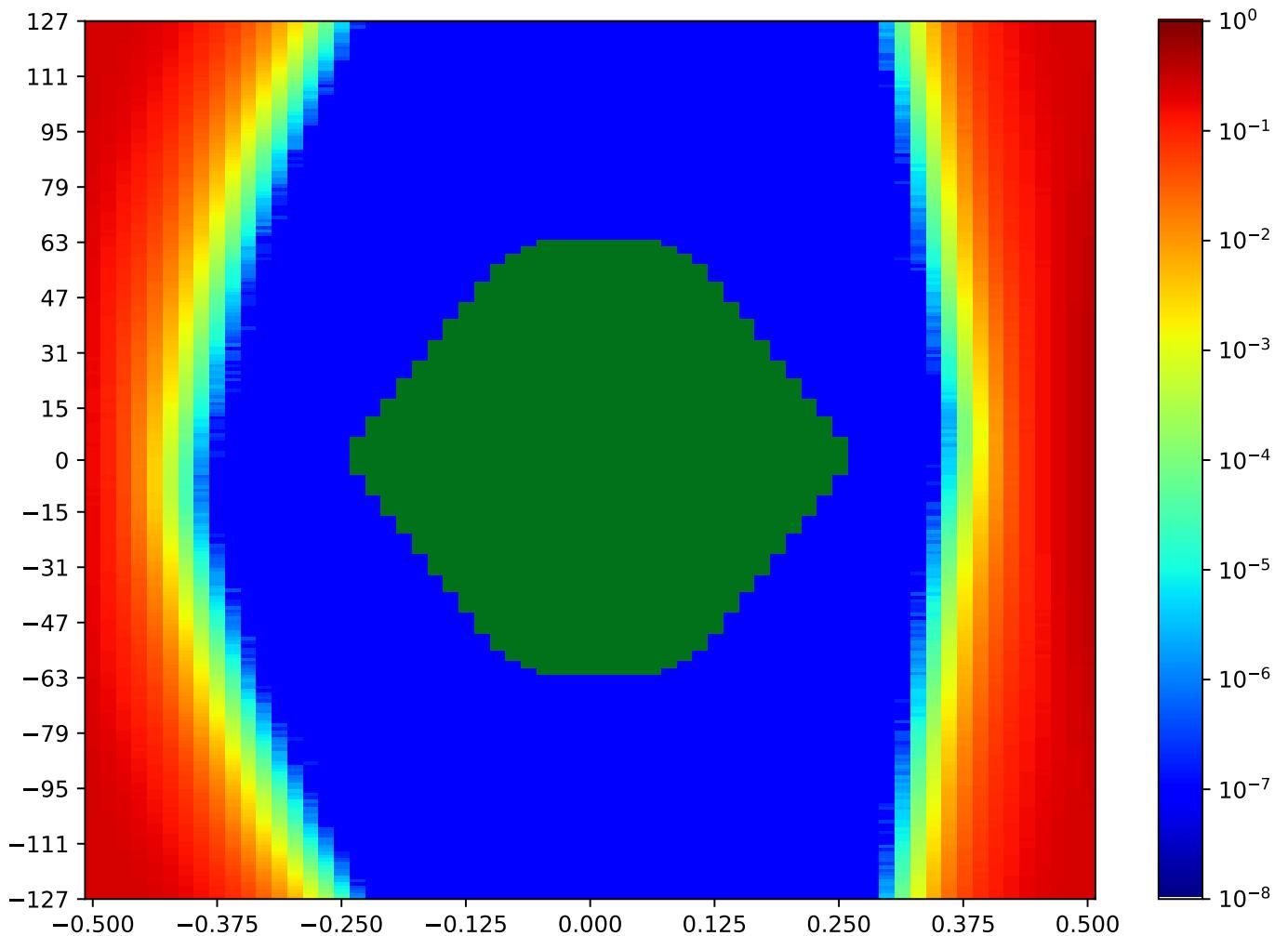


Figure 2.222: MSP_C_FPGA-TX3-07-RX2-07-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.9 MSP_C_FPGA-TX3-08-RX2-08-MSP_A_FPGA

Table 2.206: MSP_C_FPGA-TX3-08-RX2-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:08:47		2018-Jan-24 17:09:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10515	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

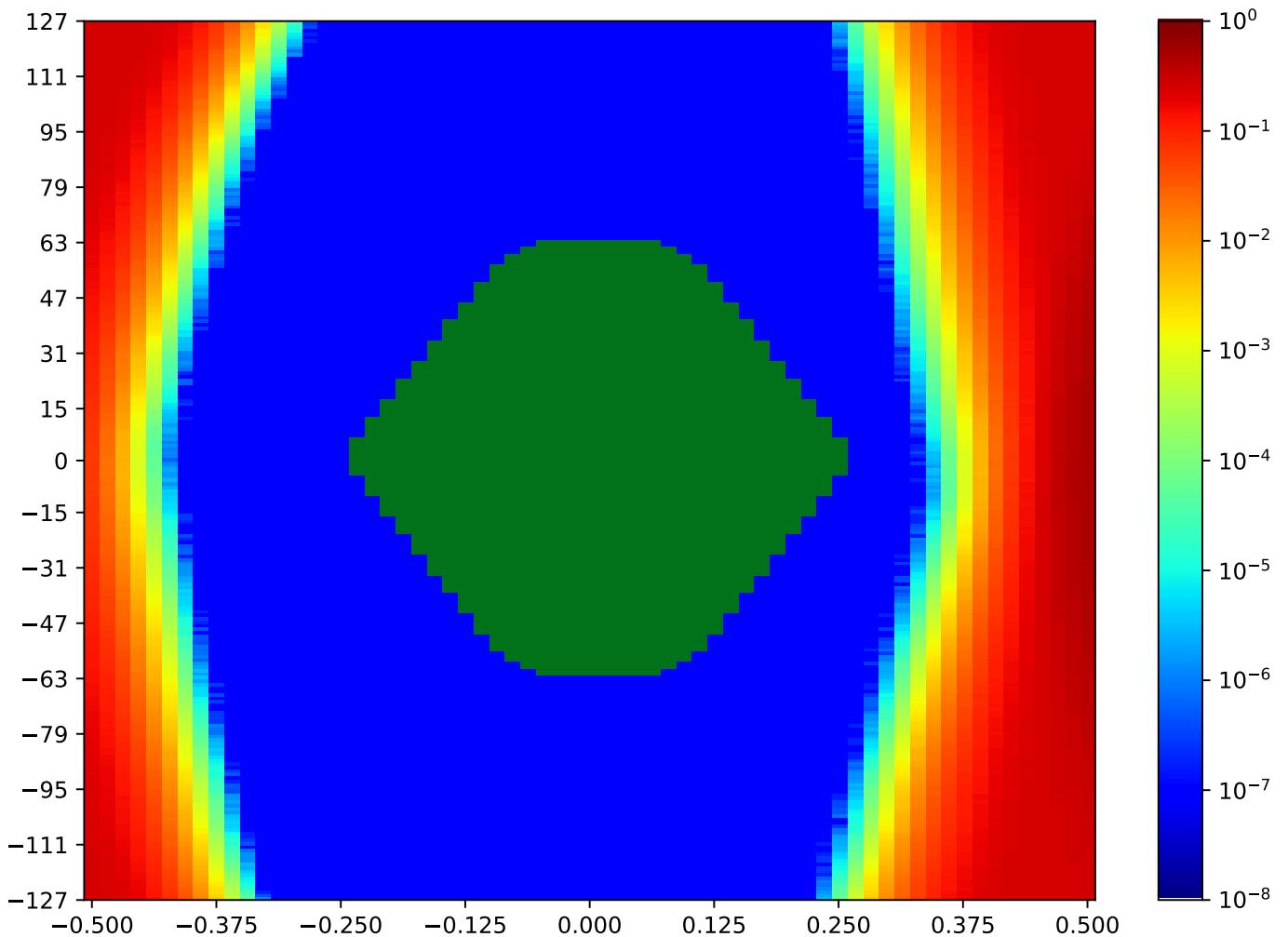


Figure 2.223: MSP_C_FPGA-TX3-08-RX2-08-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.10 MSP_C_FPGA-TX3-09-RX2-09-MSP_A_FPGA

Table 2.207: MSP_C_FPGA-TX3-09-RX2-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:05:06		2018-Jan-24 17:05:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9389	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

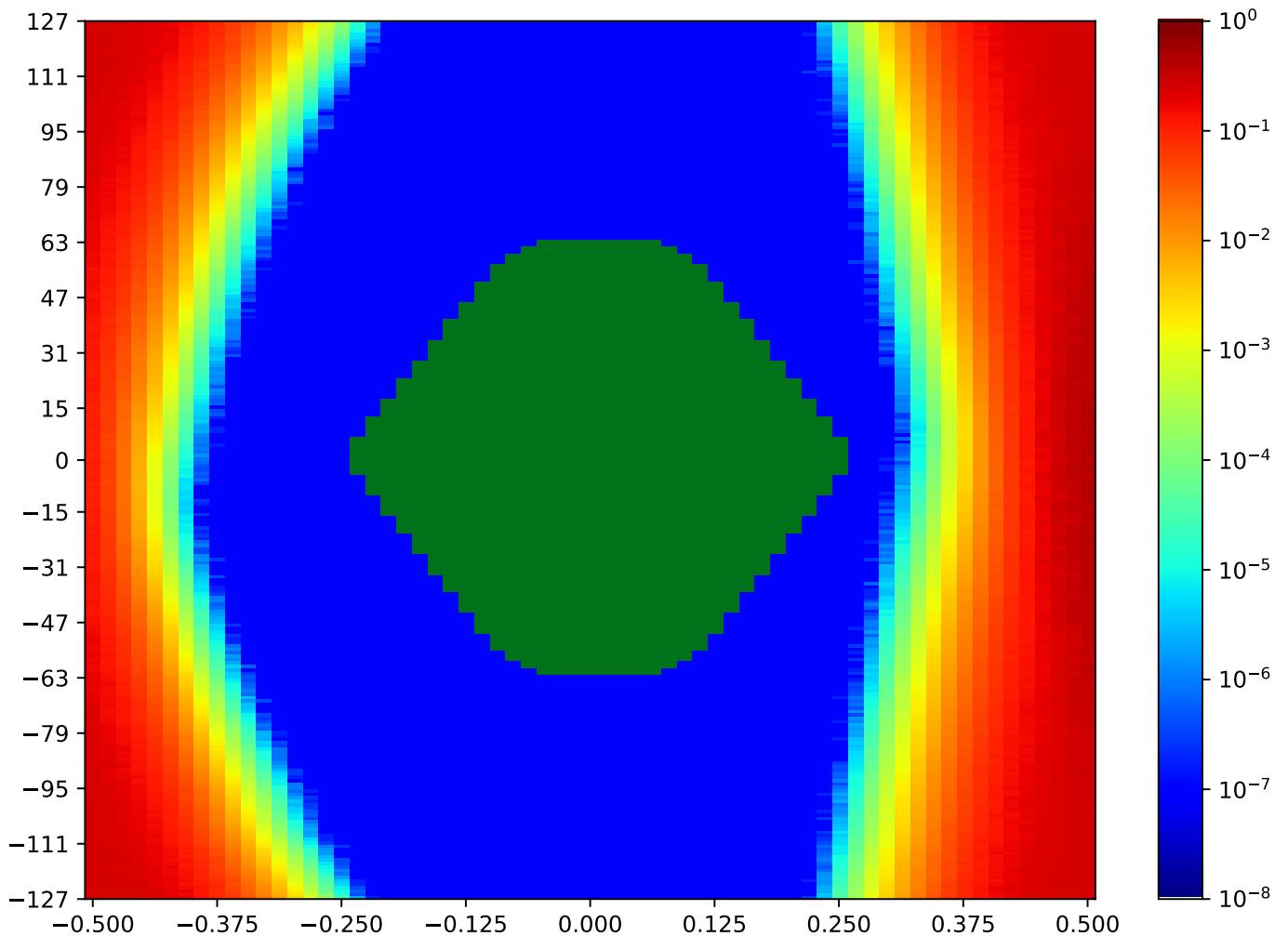


Figure 2.224: MSP_C_FPGA-TX3-09-RX2-09-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.11 MSP_C_FPGA-TX3-10-RX2-10-MSP_A_FPGA

Table 2.208: MSP_C_FPGA-TX3-10-RX2-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:07:34		2018-Jan-24 17:08:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10517	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

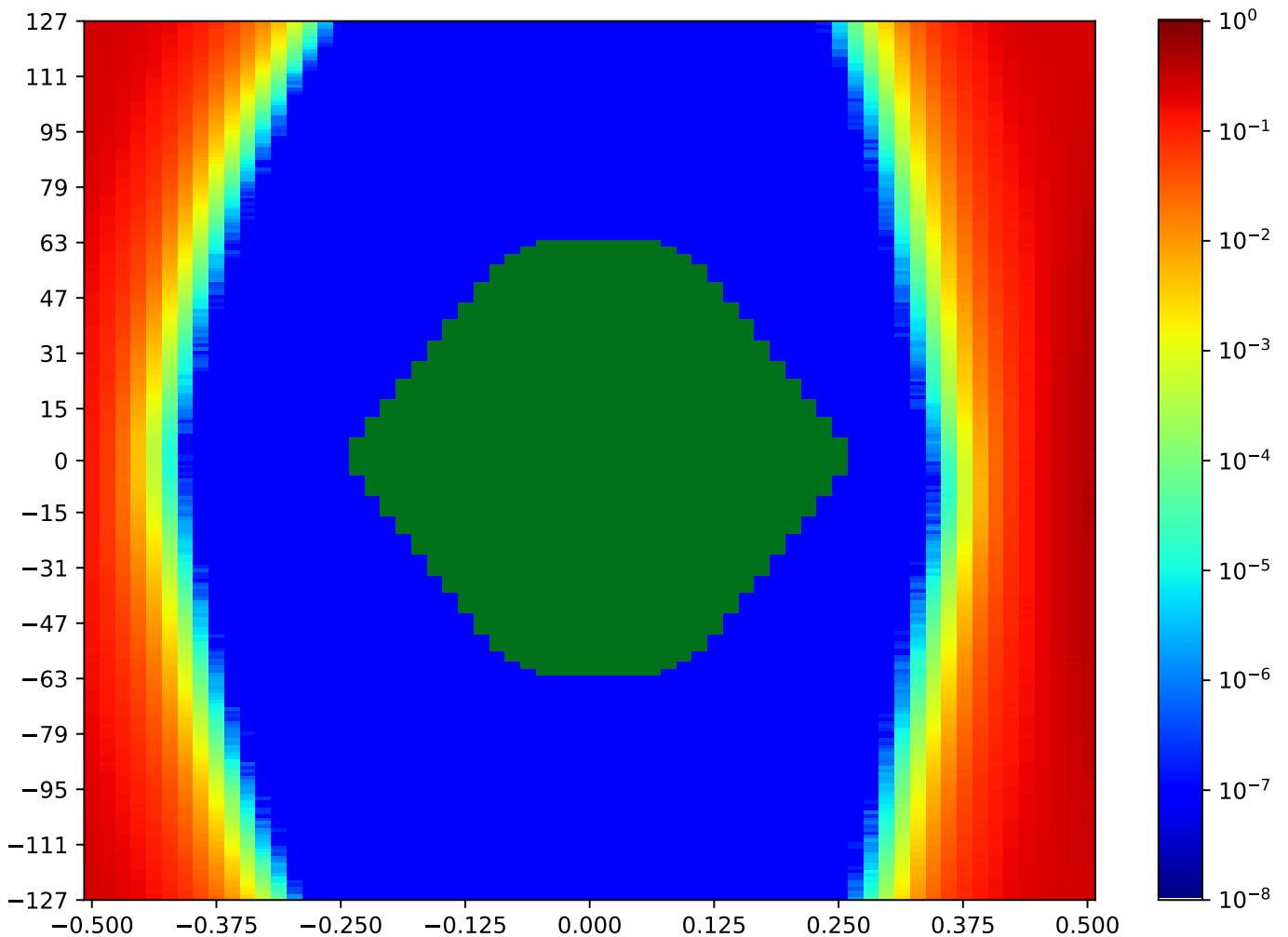


Figure 2.225: MSP_C_FPGA-TX3-10-RX2-10-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.17.12 MSP_C_FPGA-TX3-11-RX2-11-MSP_A_FPGA

Table 2.209: MSP_C_FPGA-TX3-11-RX2-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:06:57		2018-Jan-24 17:07:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9717	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

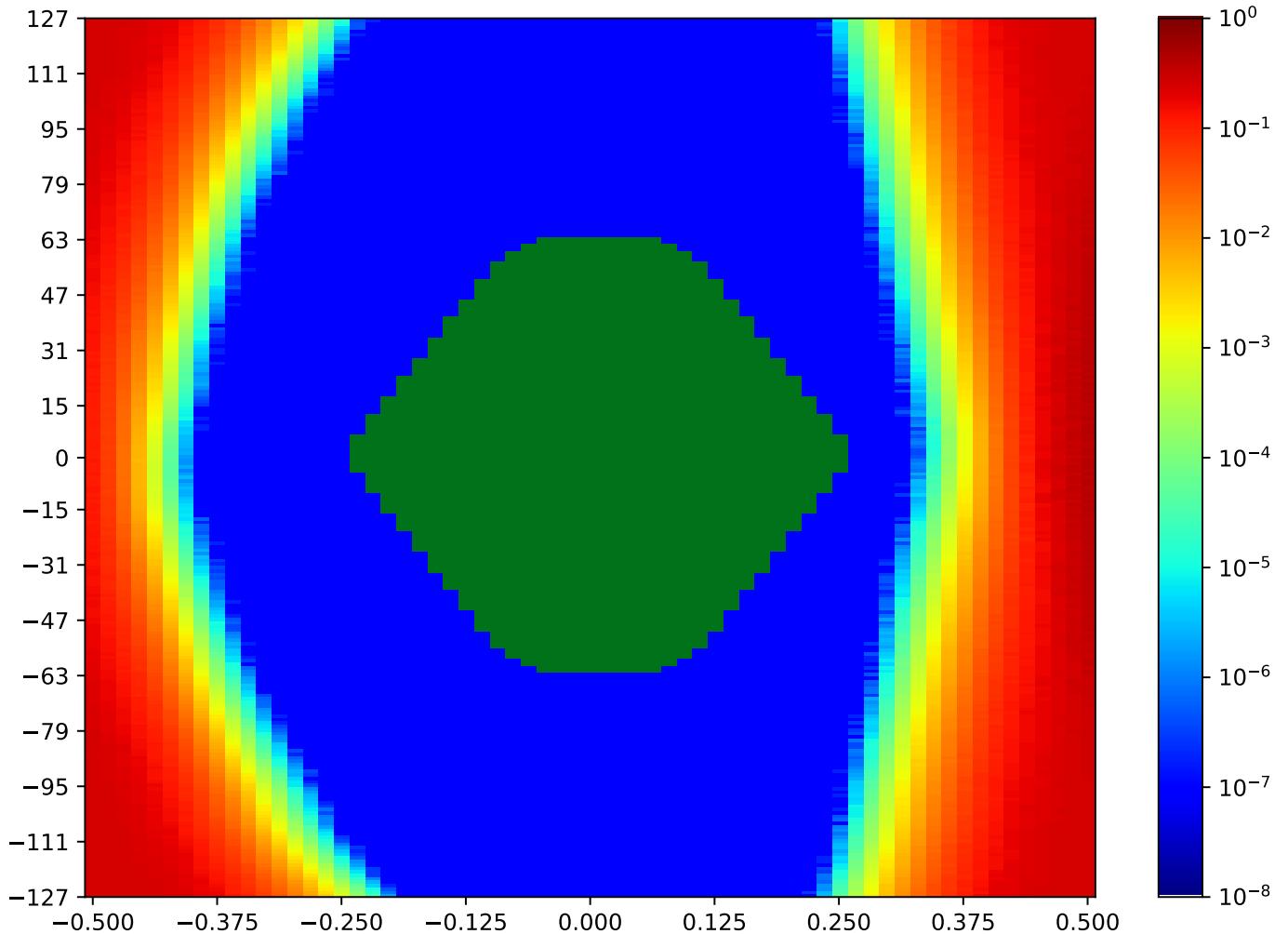


Figure 2.226: MSP_C_FPGA-TX3-11-RX2-11-MSP_A_FPGA

Call back to summary Figure 2.214. Sibling eye diagrams: V1-12.8.

2.18 MSP_C TX4 MSP_A RX1 Minipod Loopback

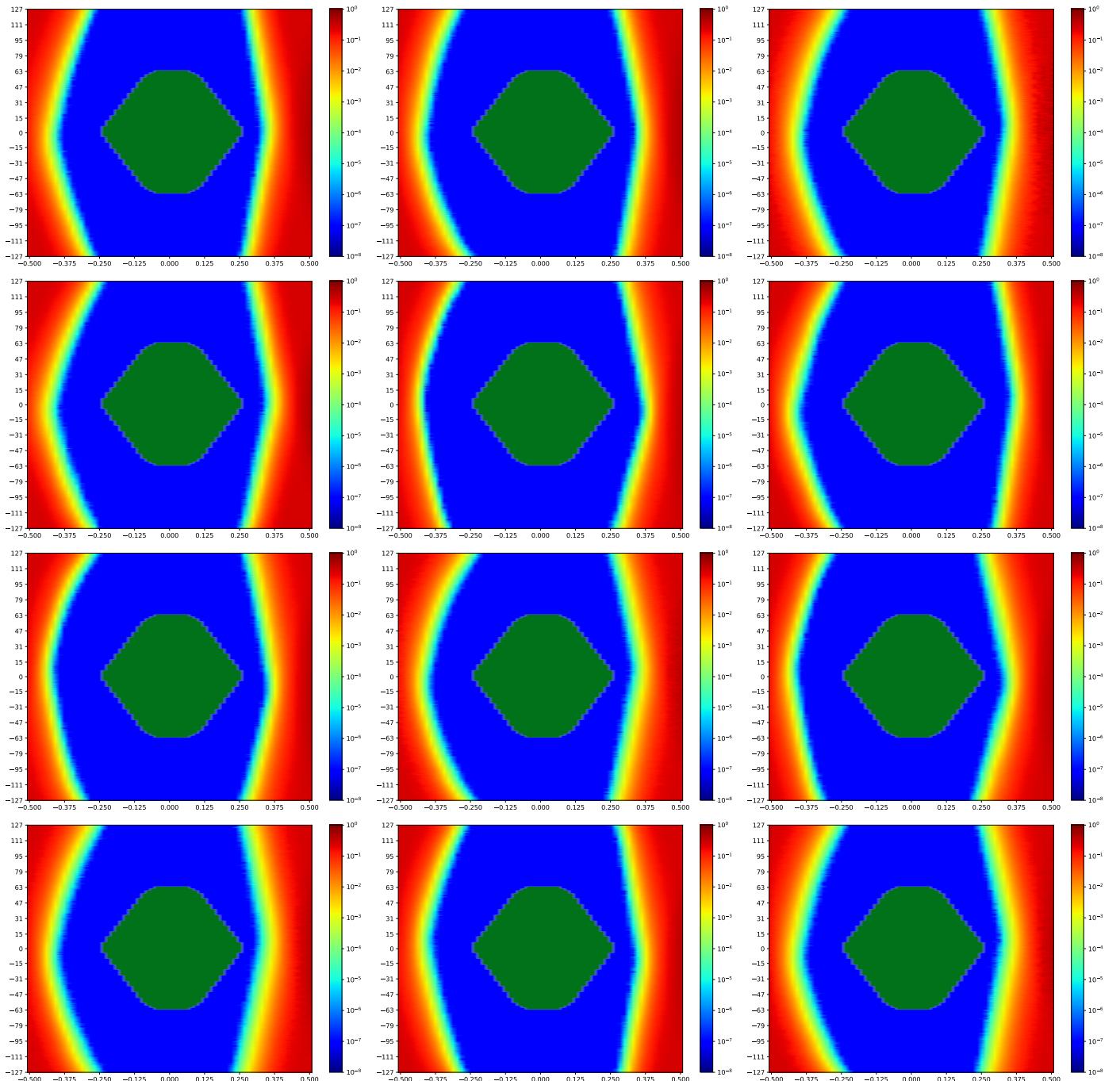


Figure 2.227: MSP_C TX4 MSP_A RX1 Minipod Loopback

A cross-reference to Figure 2.227. Sibling eye diagrams: V1-12.8.
Next summary Figure 2.240.

2.18.1 MSP_C_FPGA-TX4-00-RX1-00-MSP_A_FPGA

Table 2.210: MSP_C_FPGA-TX4-00-RX1-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:11:51		2018-Jan-24 17:12:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9864	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

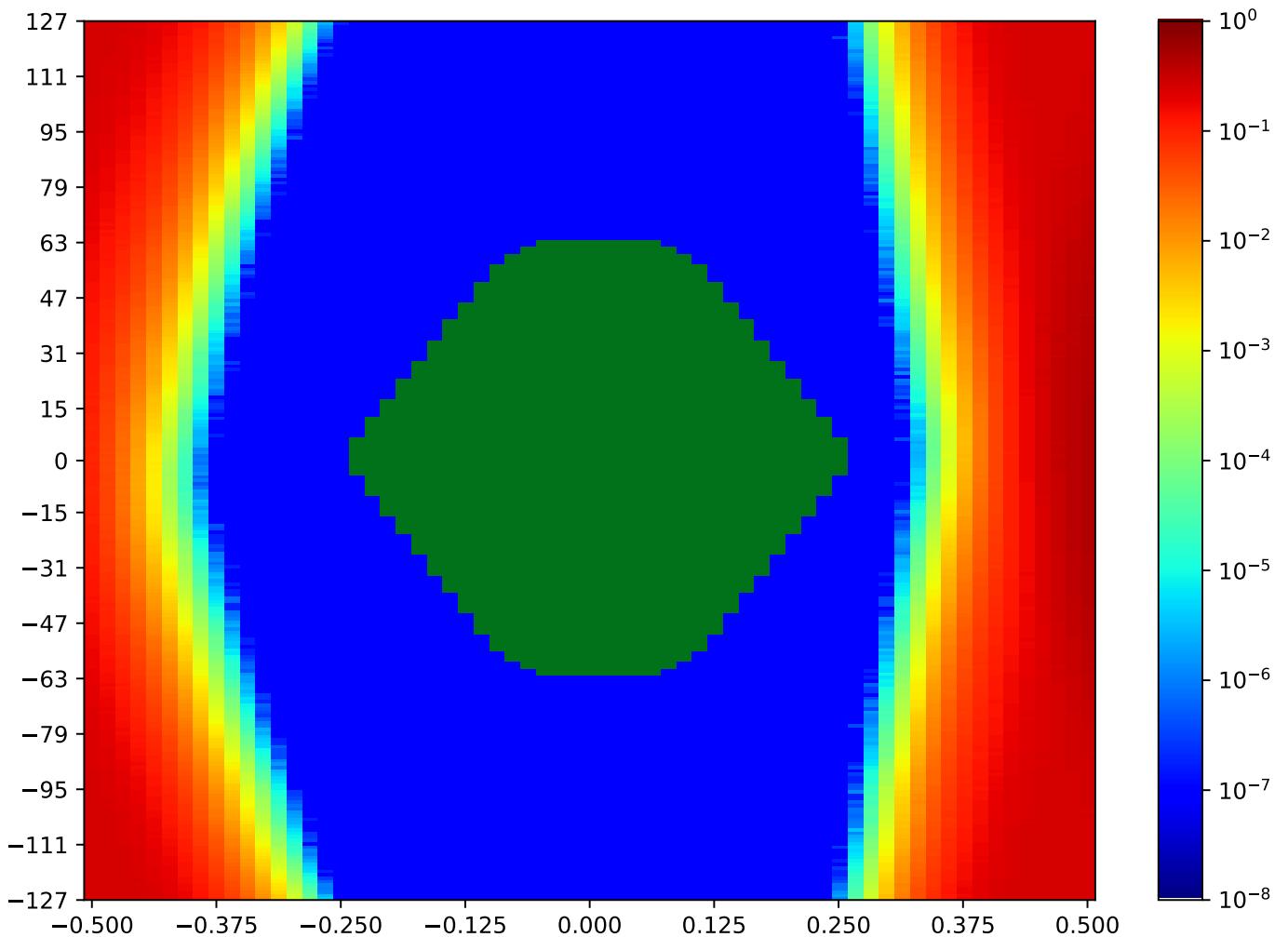


Figure 2.228: MSP_C_FPGA-TX4-00-RX1-00-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.2 MSP_C_FPGA-TX4-01-RX1-01-MSP_A_FPGA

Table 2.211: MSP_C_FPGA-TX4-01-RX1-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:10:38		2018-Jan-24 17:11:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10164	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

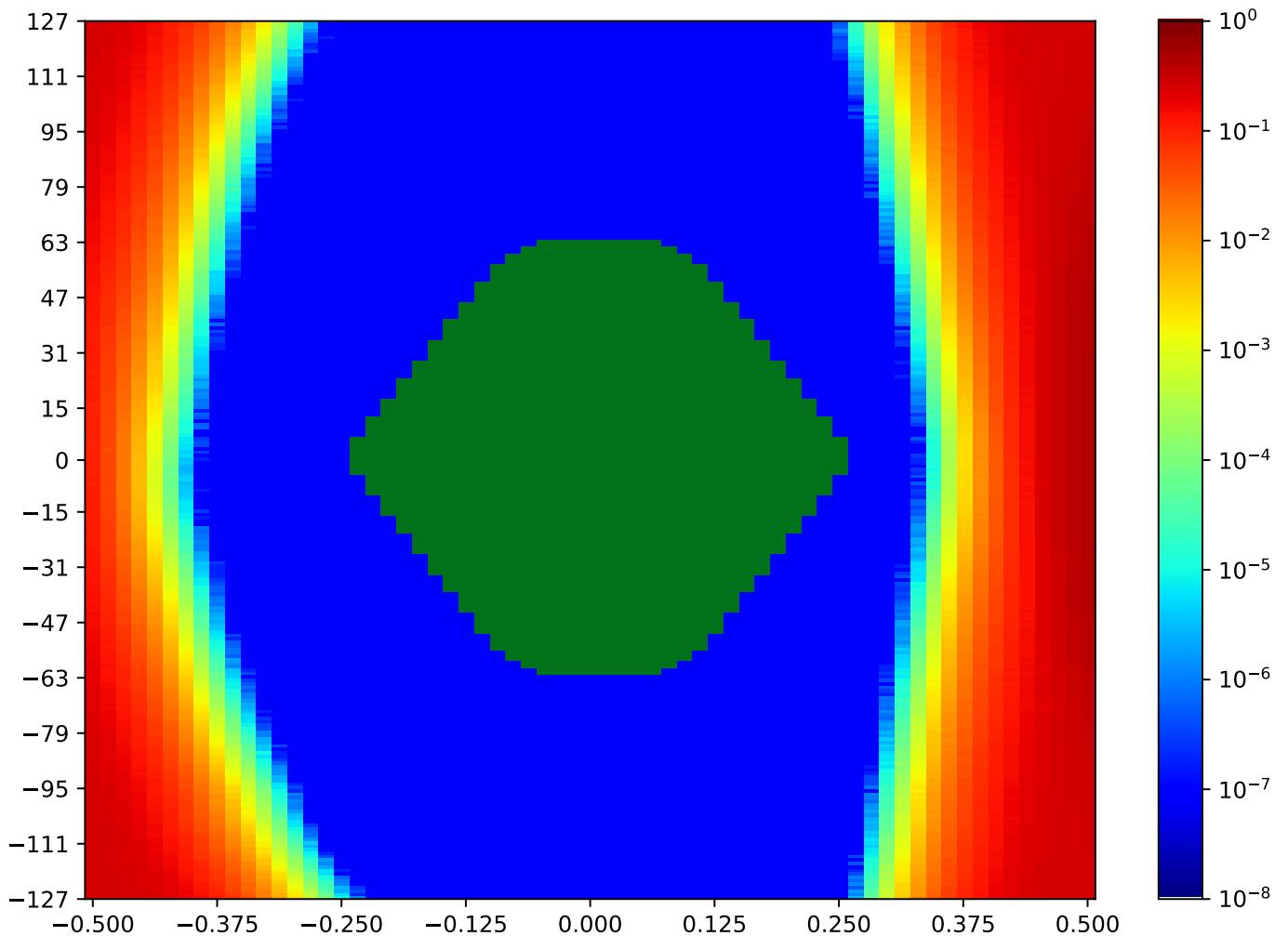


Figure 2.229: MSP_C_FPGA-TX4-01-RX1-01-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.3 MSP_C_FPGA-TX4-02-RX1-02-MSP_A_FPGA

Table 2.212: MSP_C_FPGA-TX4-02-RX1-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:13:40		2018-Jan-24 17:14:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9515	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

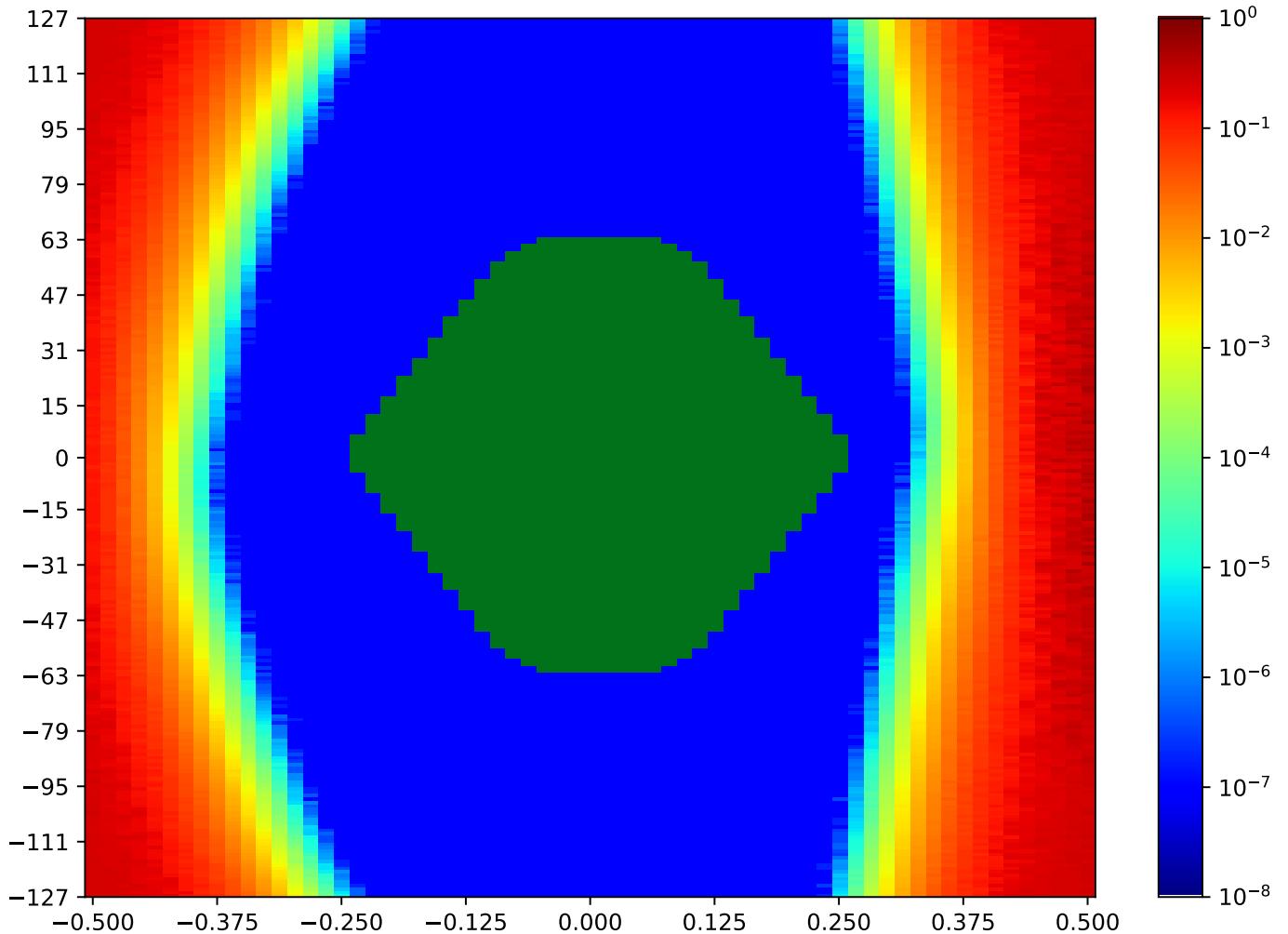


Figure 2.230: MSP_C_FPGA-TX4-02-RX1-02-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.4 MSP_C_FPGA-TX4-03-RX1-03-MSP_A_FPGA

Table 2.213: MSP_C_FPGA-TX4-03-RX1-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:10:01		2018-Jan-24 17:10:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9848	45	69.23%	255	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

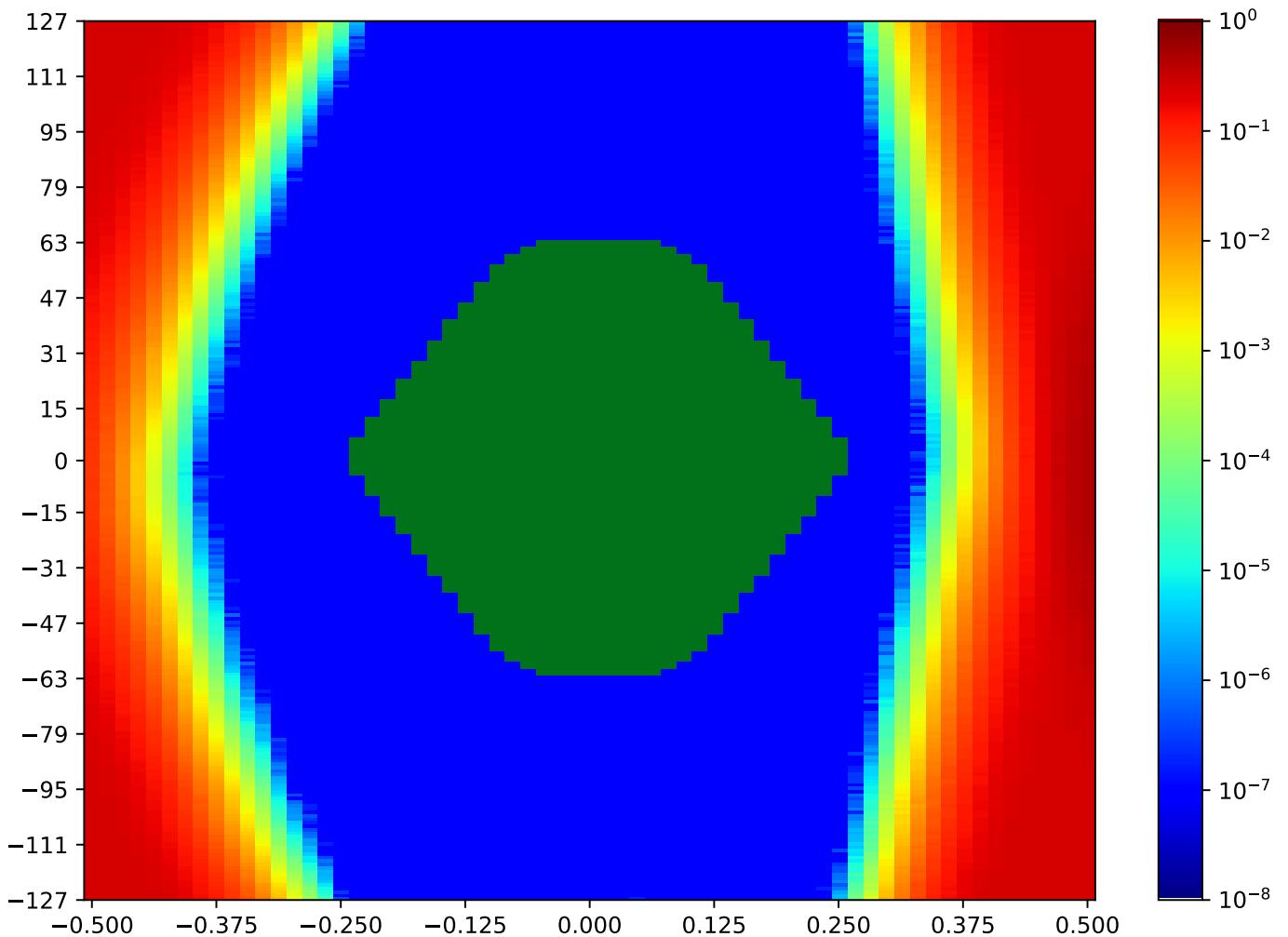


Figure 2.231: MSP_C_FPGA-TX4-03-RX1-03-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.5 MSP_C_FPGA-TX4-04-RX1-04-MSP_A_FPGA

Table 2.214: MSP_C_FPGA-TX4-04-RX1-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:15:29		2018-Jan-24 17:16:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10751	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

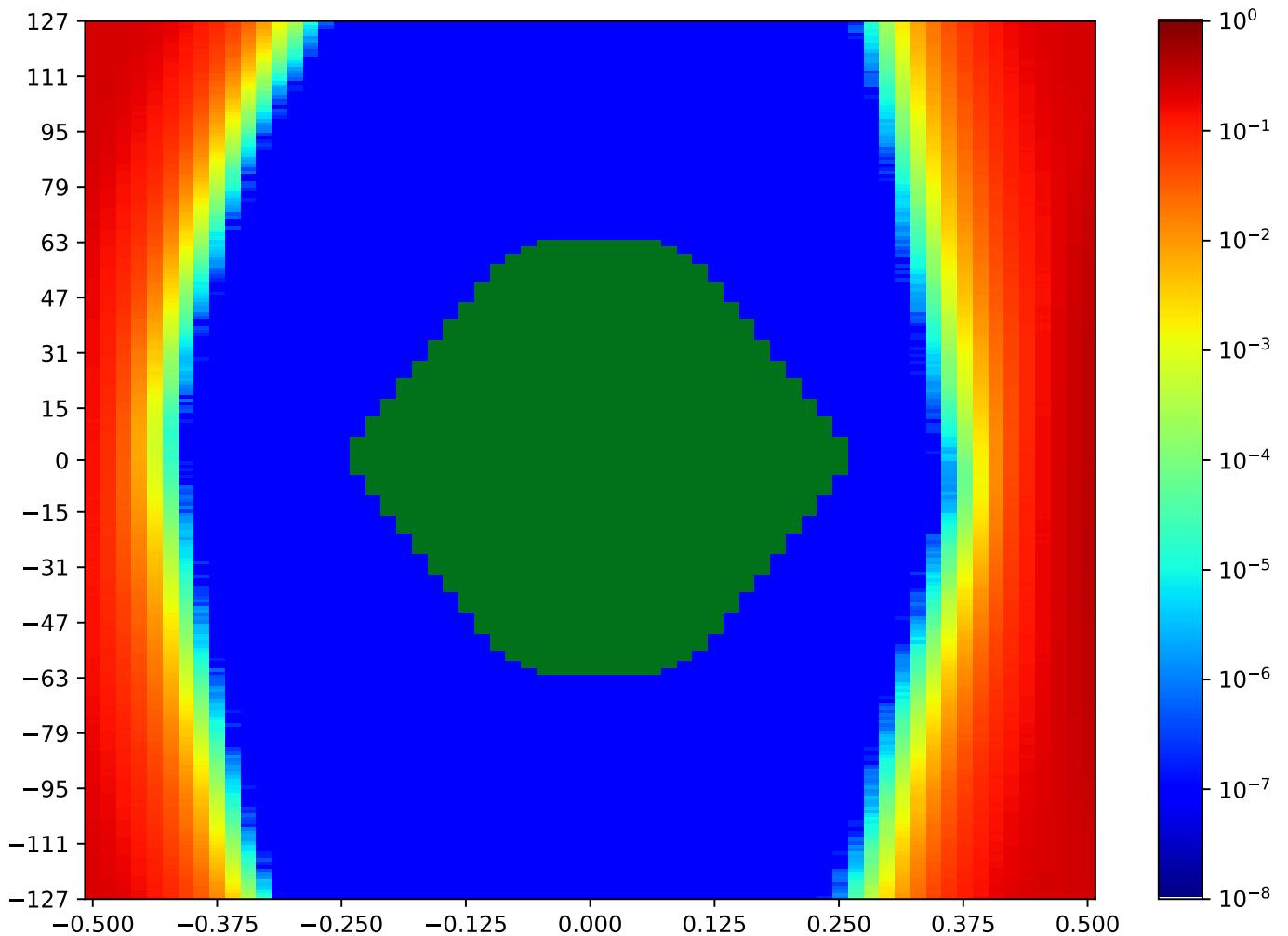


Figure 2.232: MSP_C_FPGA-TX4-04-RX1-04-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.6 MSP_C_FPGA-TX4-05-RX1-05-MSP_A_FPGA

Table 2.215: MSP_C_FPGA-TX4-05-RX1-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:11:15		2018-Jan-24 17:11:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10213	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

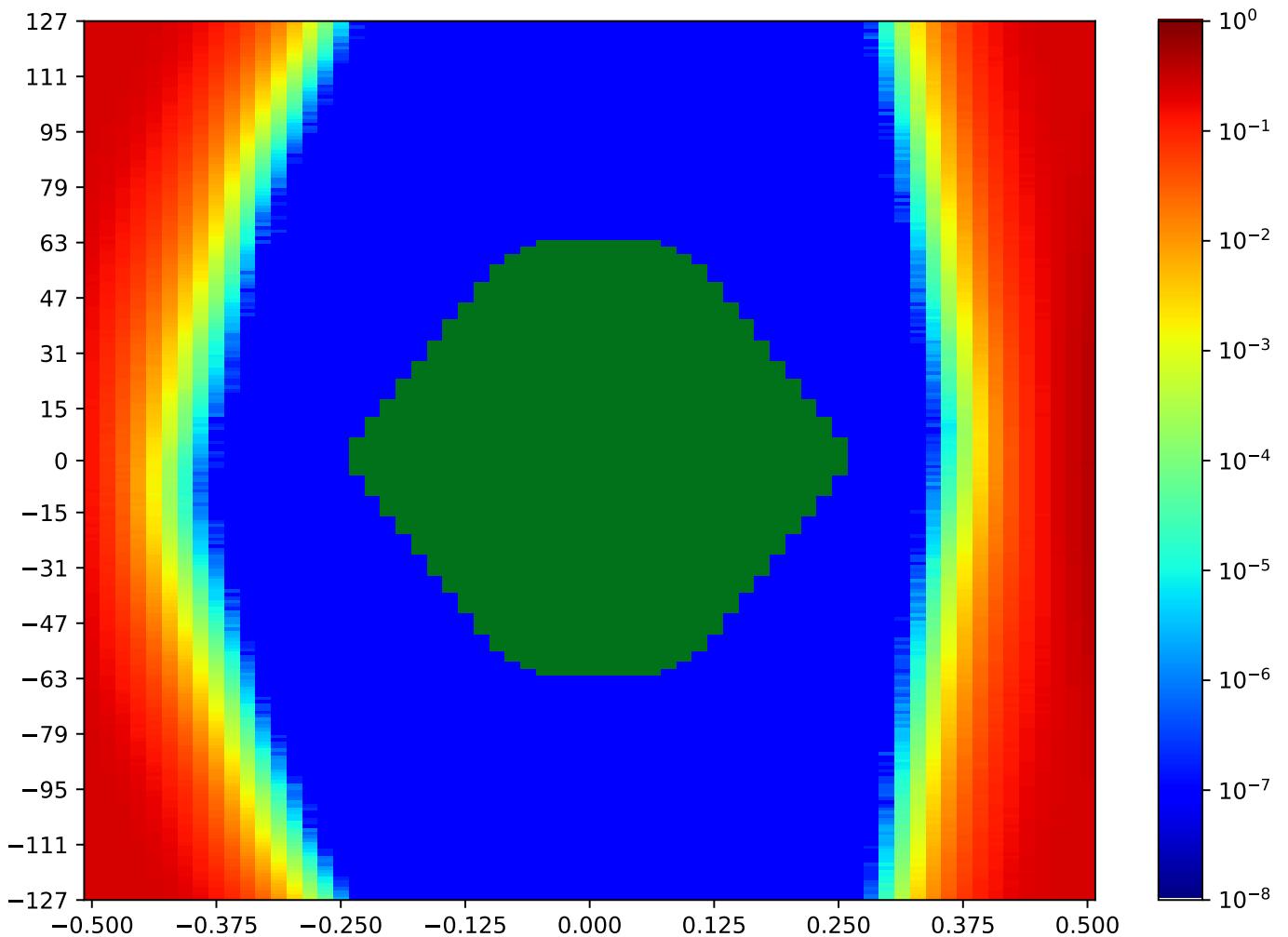


Figure 2.233: MSP_C_FPGA-TX4-05-RX1-05-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.7 MSP_C_FPGA-TX4-06-RX1-06-MSP_A_FPGA

Table 2.216: MSP_C_FPGA-TX4-06-RX1-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:16:43		2018-Jan-24 17:17:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10381	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

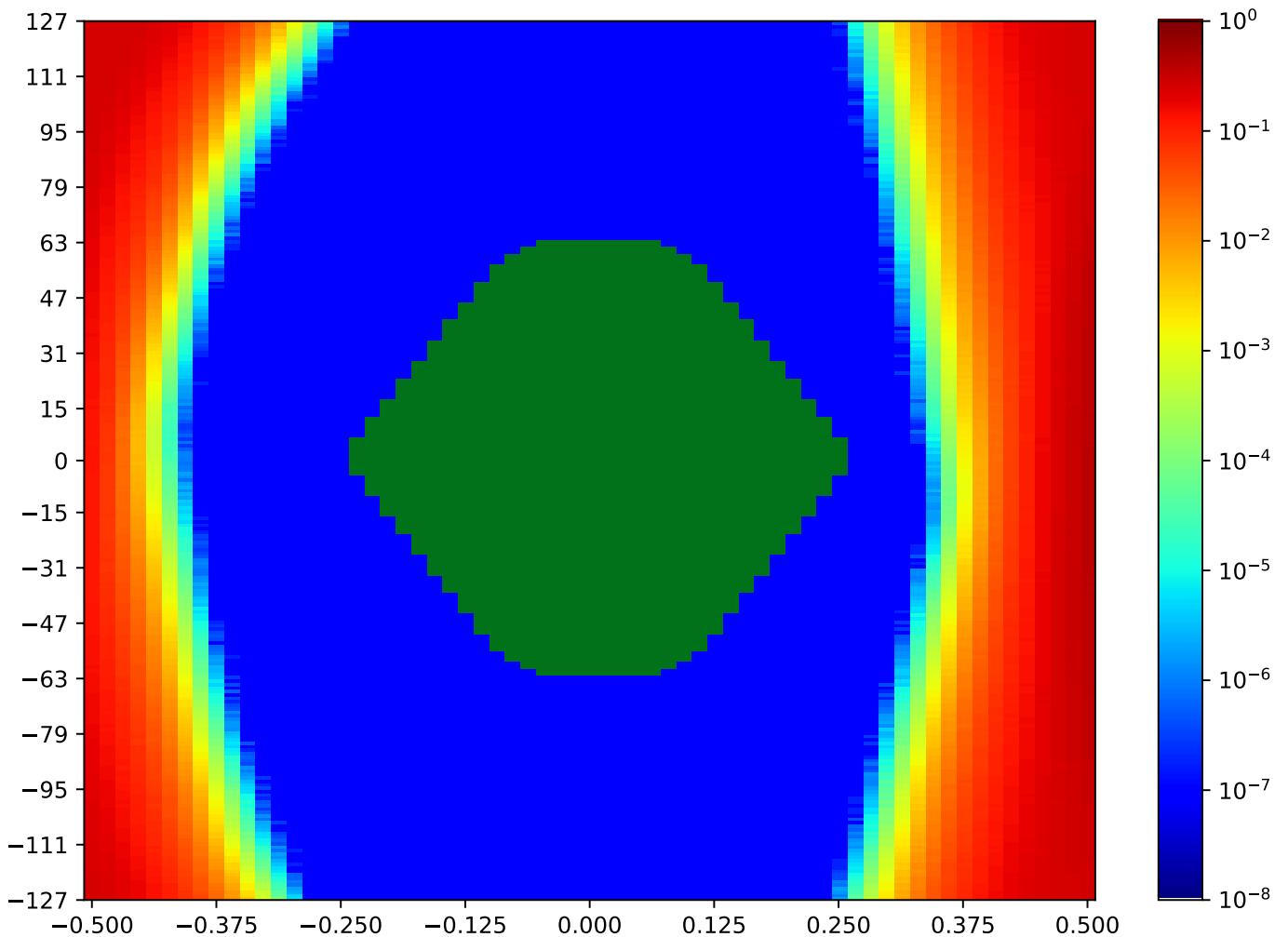


Figure 2.234: MSP_C_FPGA-TX4-06-RX1-06-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.8 MSP_C_FPGA-TX4-07-RX1-07-MSP_A_FPGA

Table 2.217: MSP_C_FPGA-TX4-07-RX1-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:12:27		2018-Jan-24 17:13:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9532	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

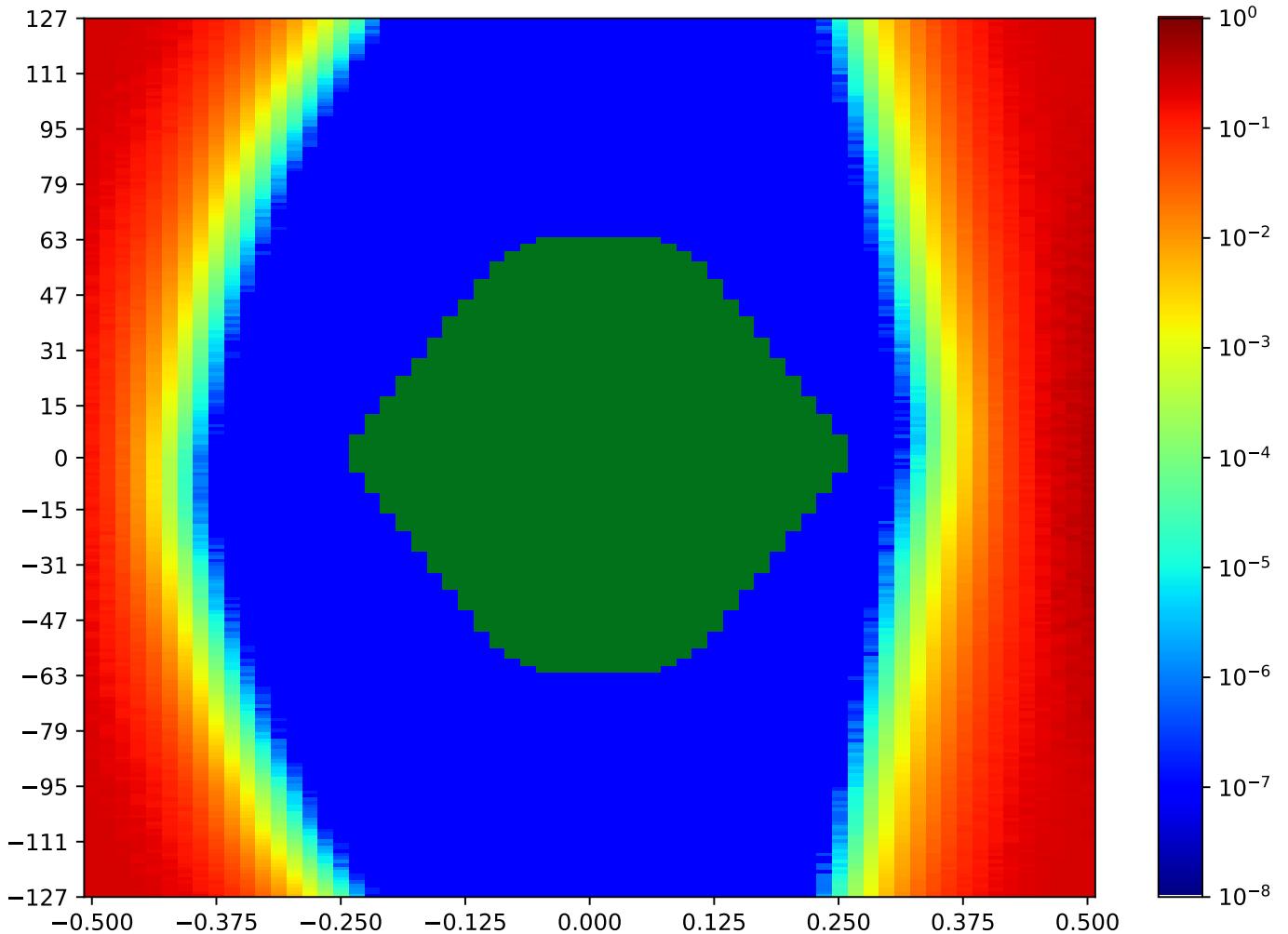


Figure 2.235: MSP_C_FPGA-TX4-07-RX1-07-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.9 MSP_C_FPGA-TX4-08-RX1-08-MSP_A_FPGA

Table 2.218: MSP_C_FPGA-TX4-08-RX1-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:16:06		2018-Jan-24 17:16:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9922	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

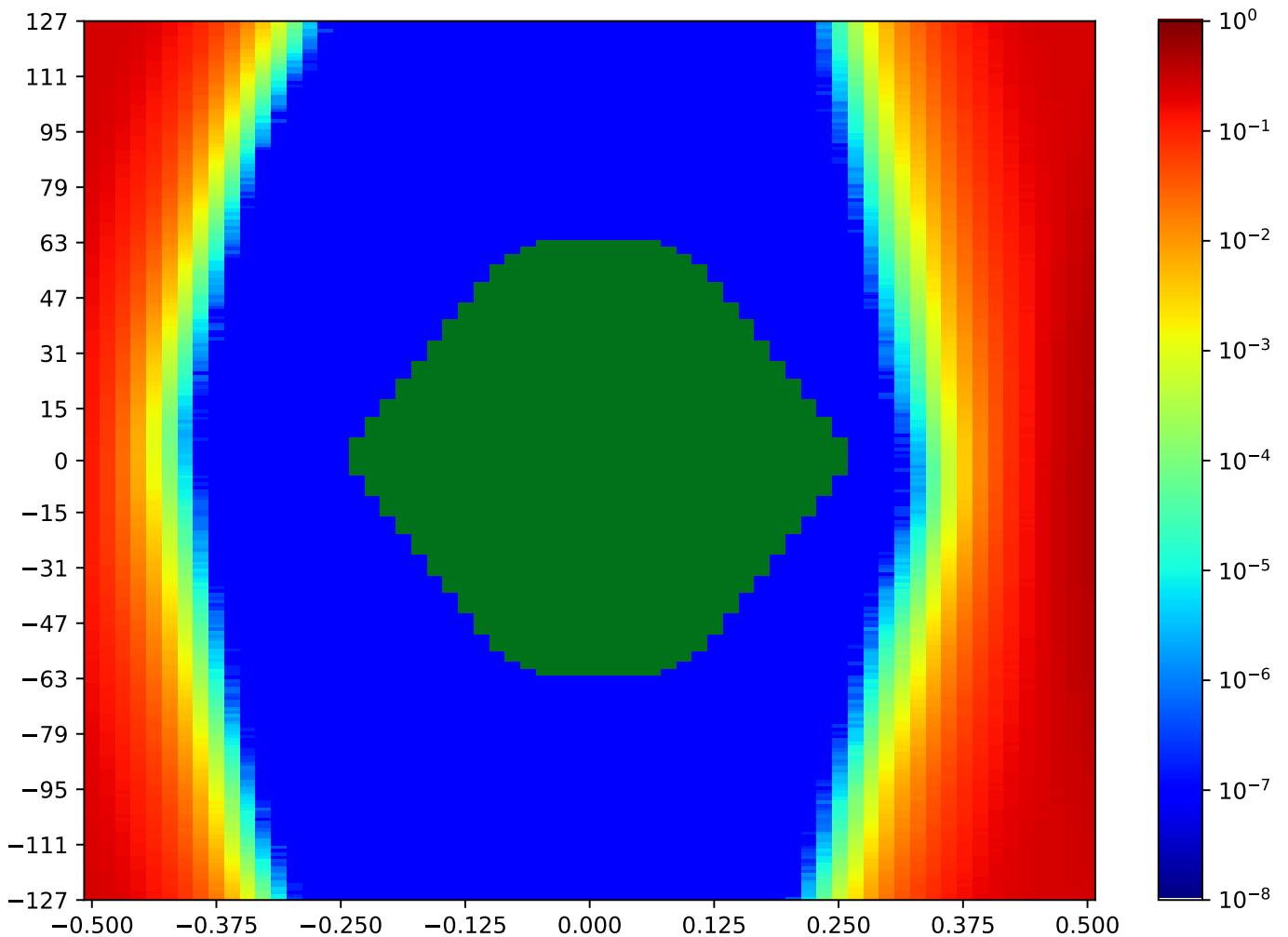


Figure 2.236: MSP_C_FPGA-TX4-08-RX1-08-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.10 MSP_C_FPGA-TX4-09-RX1-09-MSP_A_FPGA

Table 2.219: MSP_C_FPGA-TX4-09-RX1-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:13:03		2018-Jan-24 17:13:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9374	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

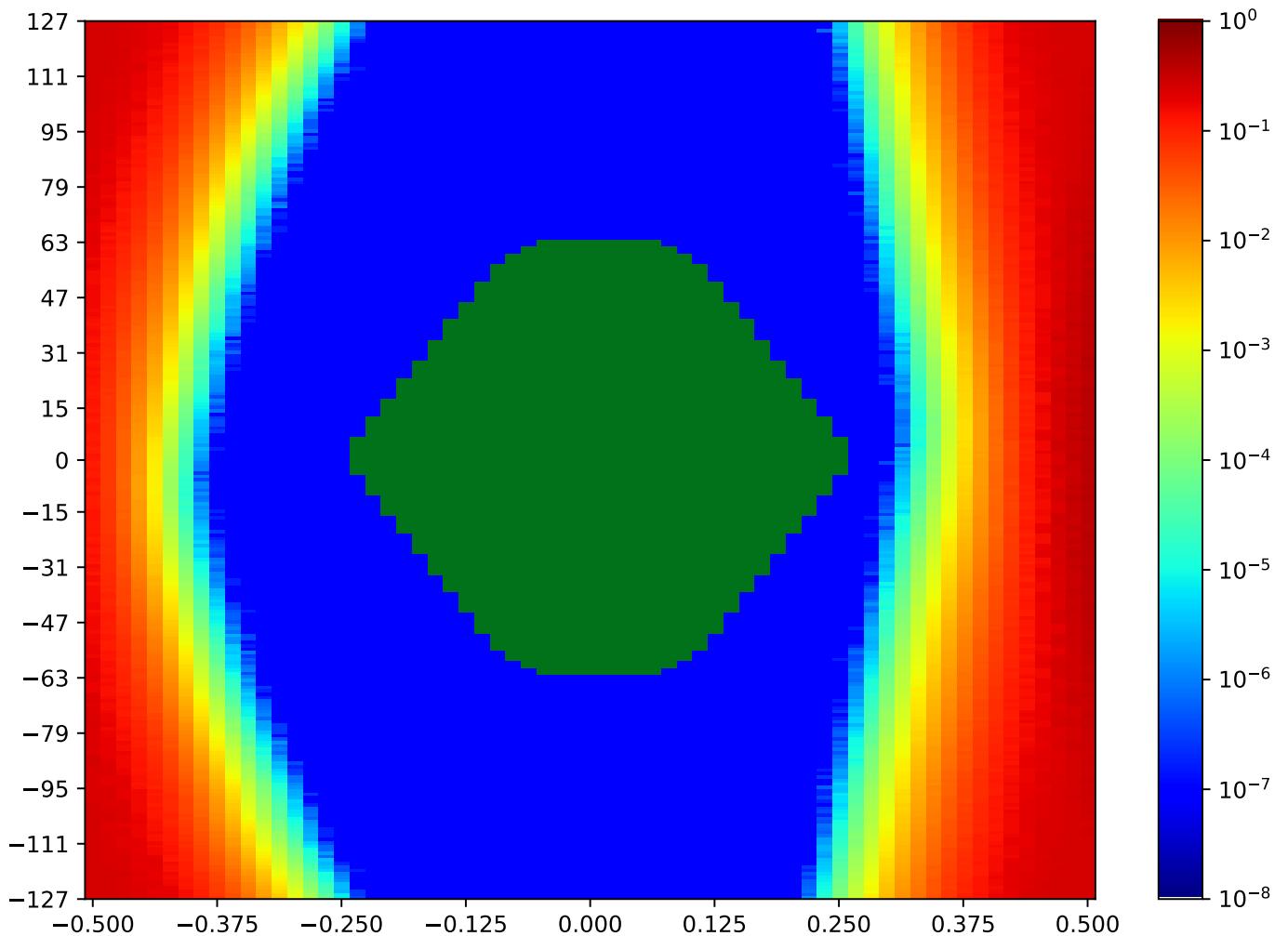


Figure 2.237: MSP_C_FPGA-TX4-09-RX1-09-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.11 MSP_C_FPGA-TX4-10-RX1-10-MSP_A_FPGA

Table 2.220: MSP_C_FPGA-TX4-10-RX1-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:14:53		2018-Jan-24 17:15:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9938	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

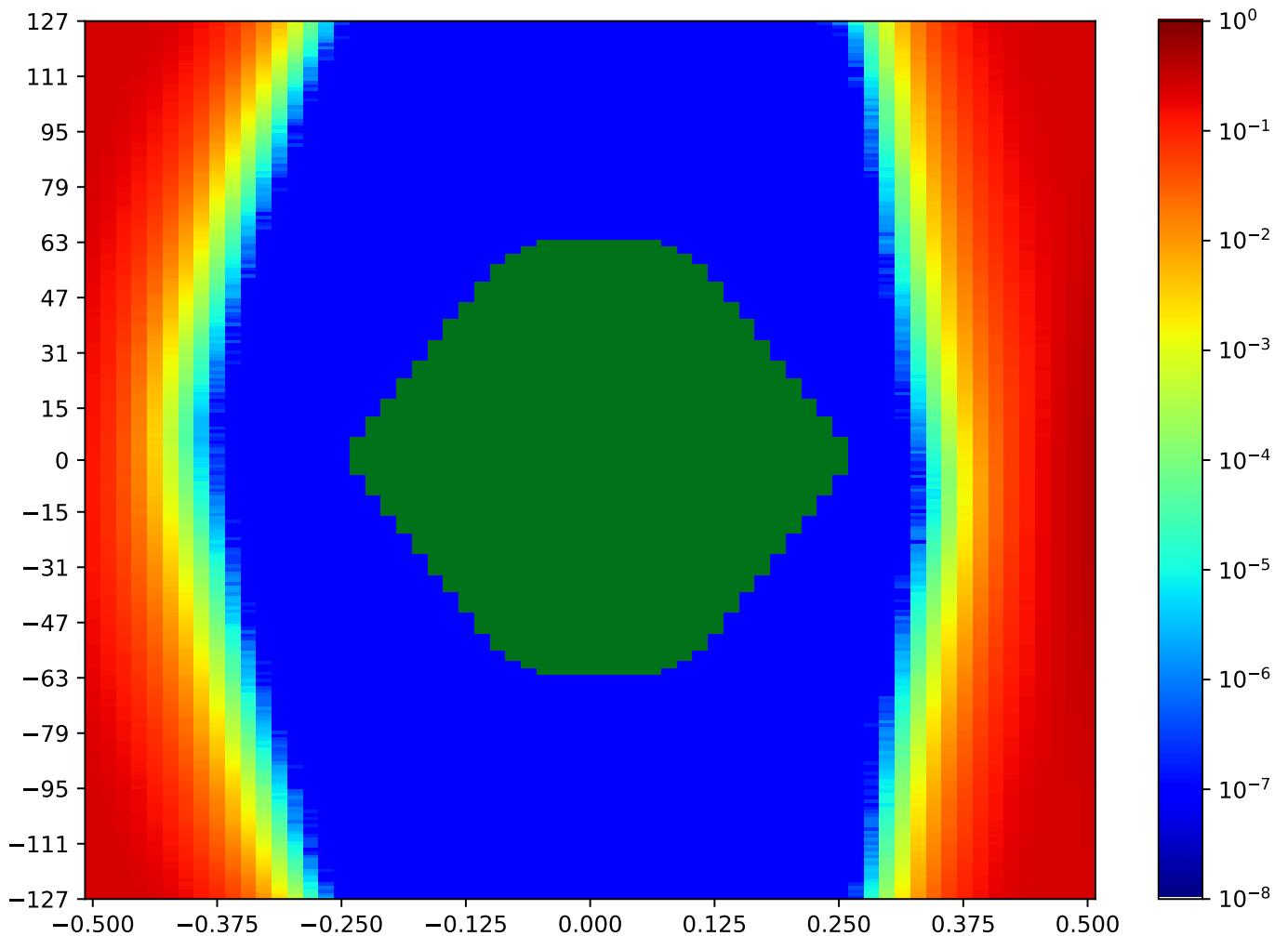


Figure 2.238: MSP_C_FPGA-TX4-10-RX1-10-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.18.12 MSP_C_FPGA-TX4-11-RX1-11-MSP_A_FPGA

Table 2.221: MSP_C_FPGA-TX4-11-RX1-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:14:16		2018-Jan-24 17:14:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9223	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

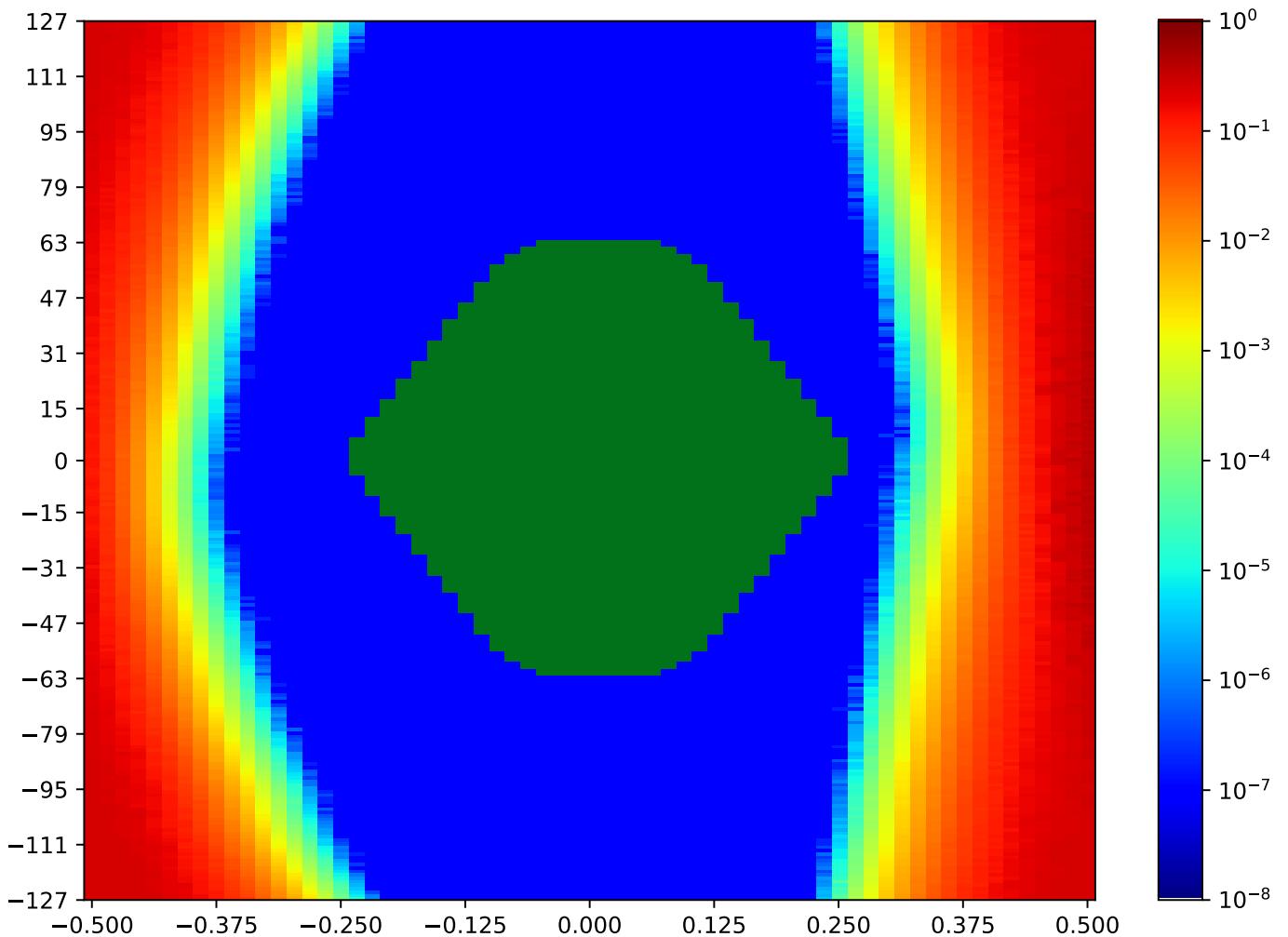


Figure 2.239: MSP_C_FPGA-TX4-11-RX1-11-MSP_A_FPGA

Call back to summary Figure 2.227. Sibling eye diagrams: V1-12.8.

2.19 MSP_A TX1 MSP_C RX13 Minipod Loopback

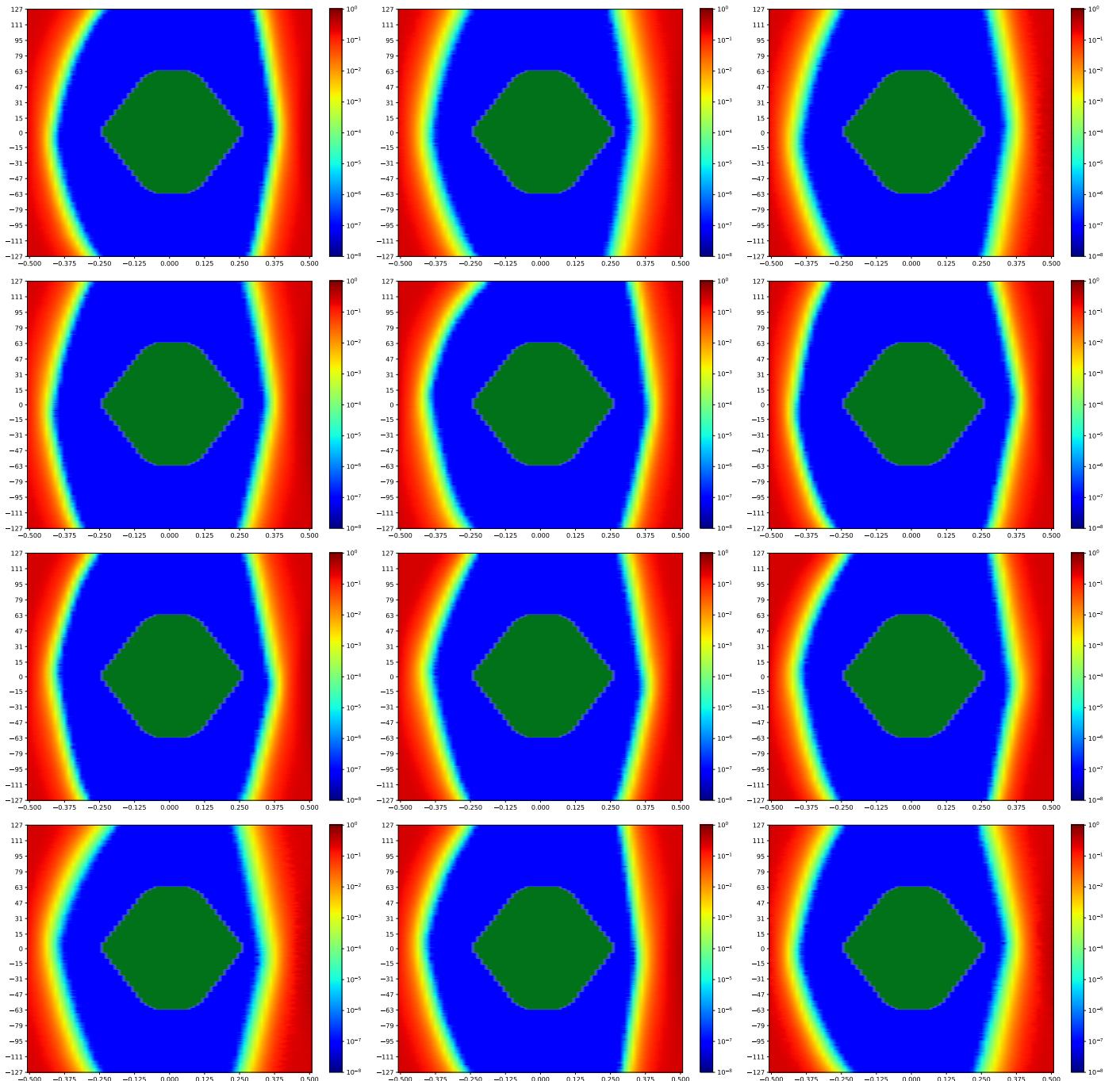


Figure 2.240: MSP_A TX1 MSP_C RX13 Minipod Loopback

A cross-reference to Figure 2.240. Sibling eye diagrams: V1-12.8.
Next summary Figure 2.253.

2.19.1 MSP_A_FPGA-TX1-00-RX13-00-MSP_C_FPGA

Table 2.222: MSP_A_FPGA-TX1-00-RX13-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:33:20		2018-Jan-24 17:33:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10586	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

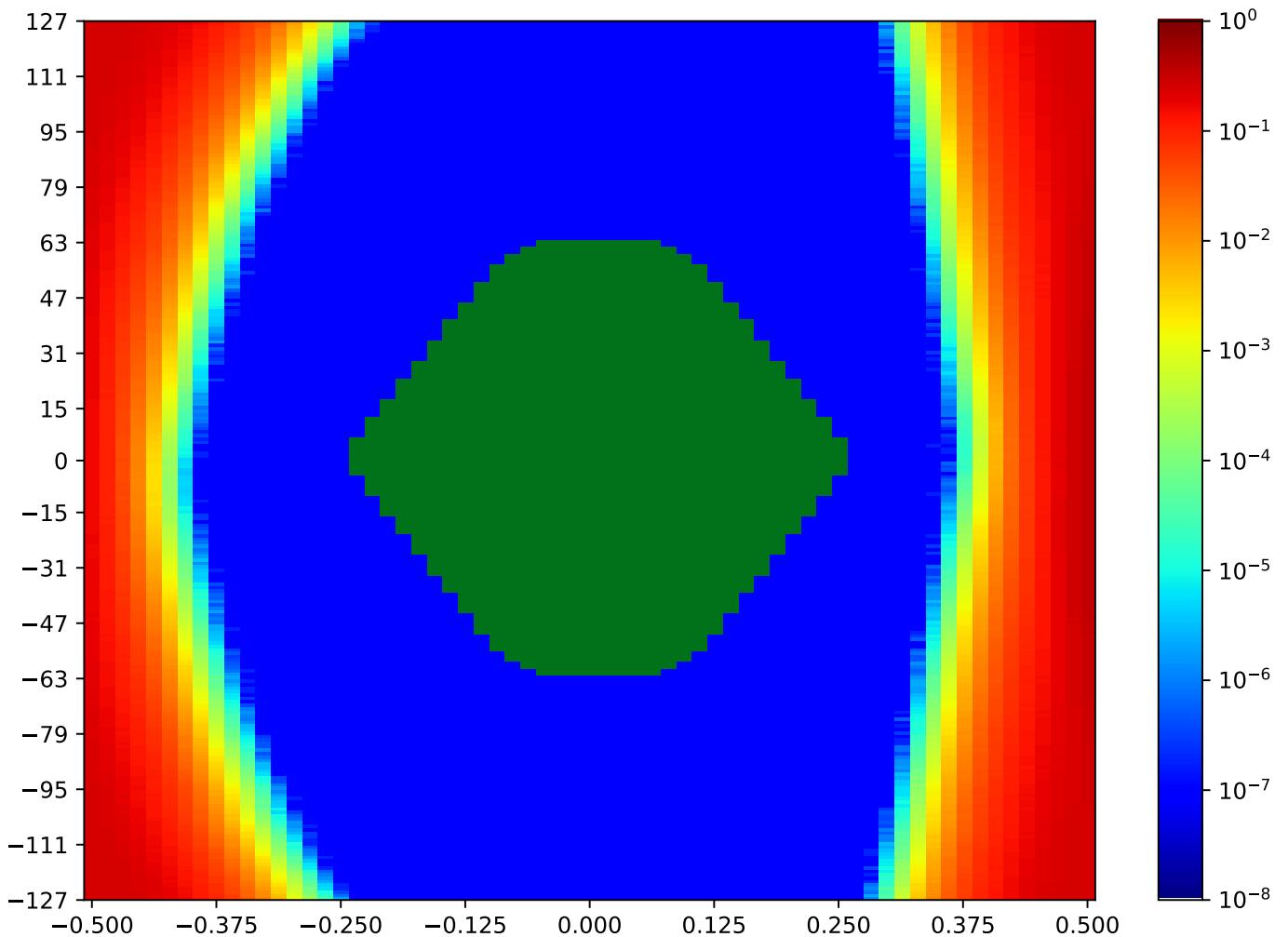


Figure 2.241: MSP_A_FPGA-TX1-00-RX13-00-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.2 MSP_A_FPGA-TX1-01-RX13-01-MSP_C_FPGA

Table 2.223: MSP_A_FPGA-TX1-01-RX13-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:34:31		2018-Jan-24 17:35:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9453	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

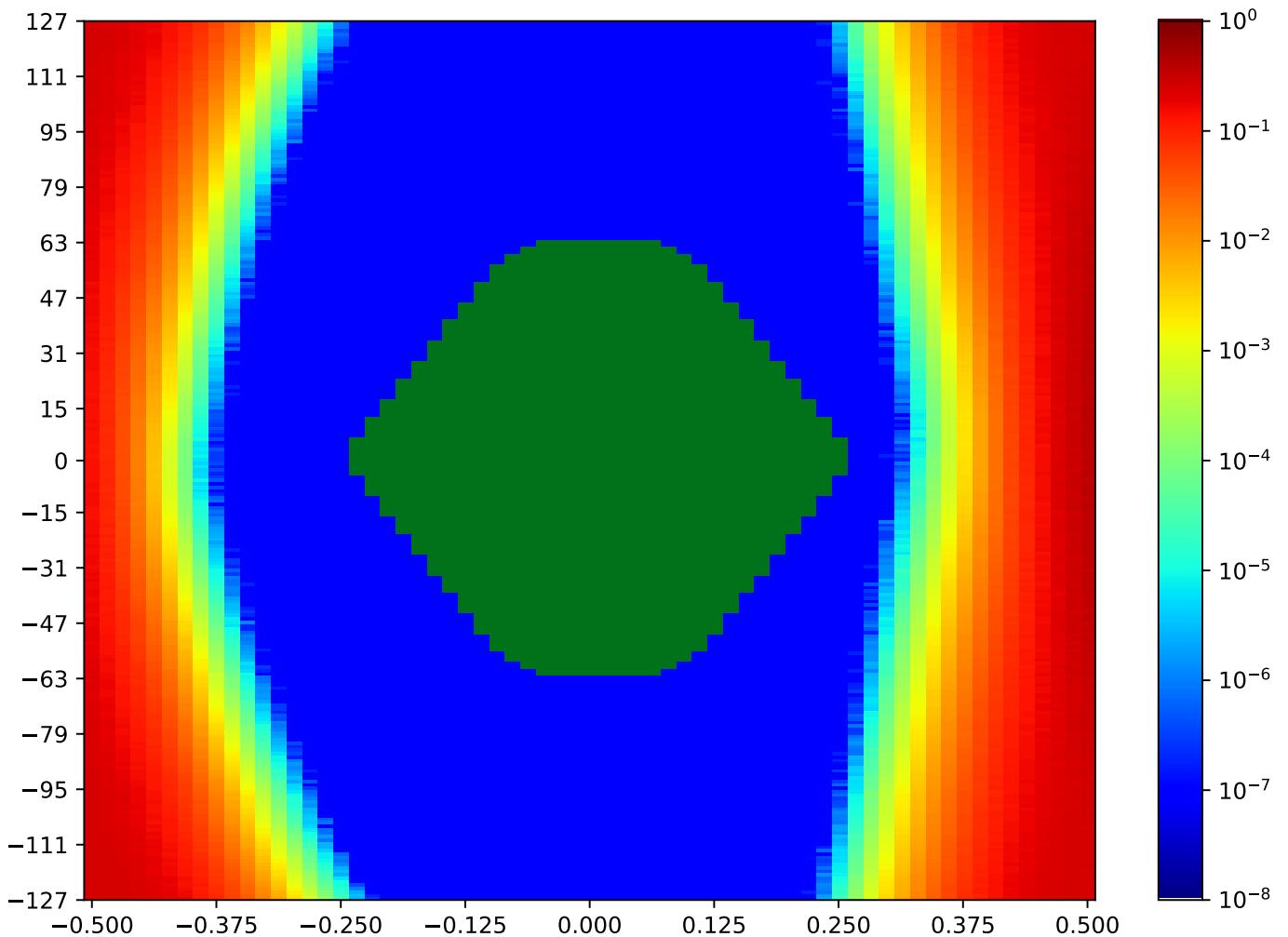


Figure 2.242: MSP_A_FPGA-TX1-01-RX13-01-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.3 MSP_A_FPGA-TX1-02-RX13-02-MSP_C_FPGA

Table 2.224: MSP_A_FPGA-TX1-02-RX13-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:35:06		2018-Jan-24 17:35:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9799	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

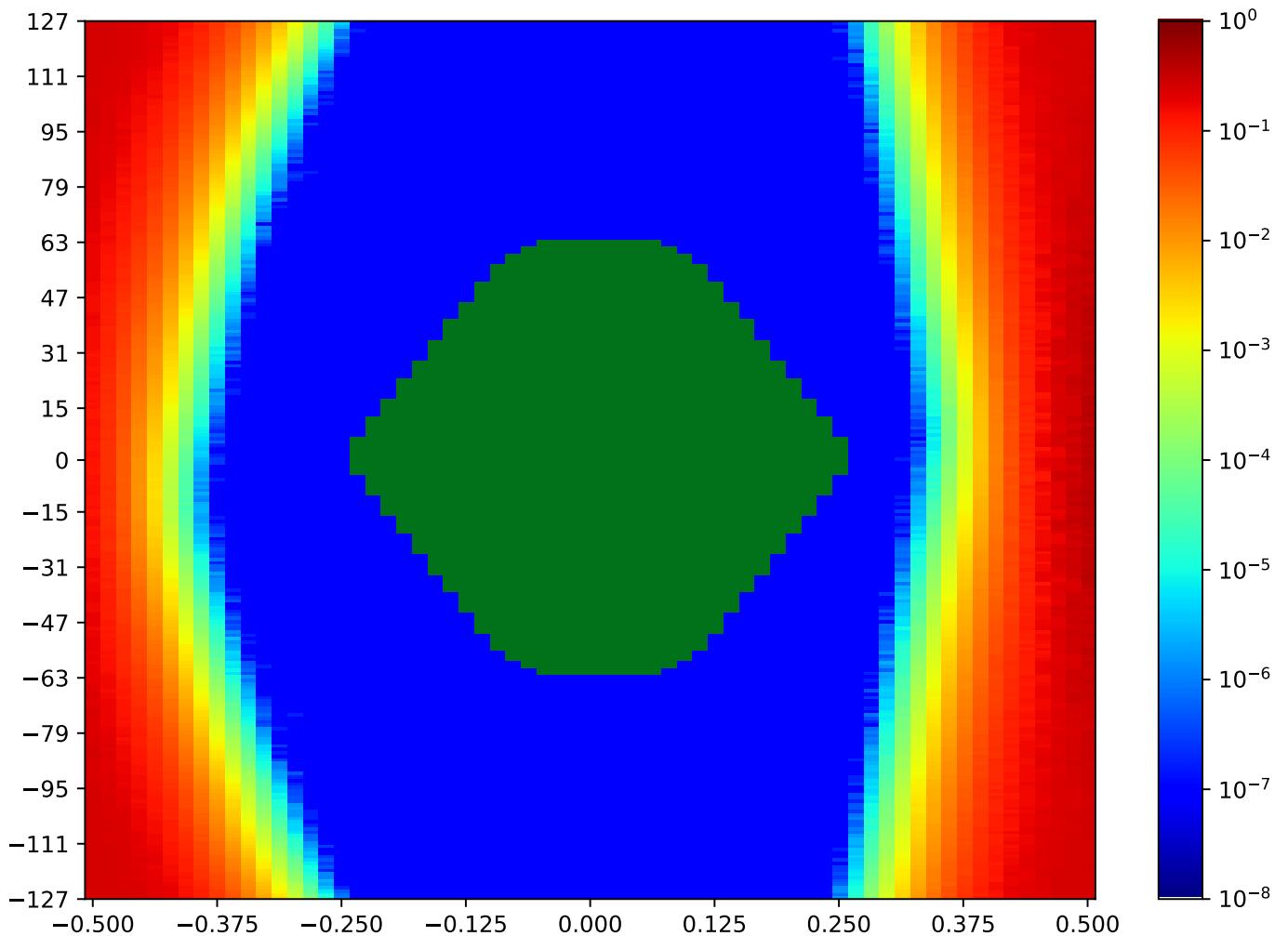


Figure 2.243: MSP_A_FPGA-TX1-02-RX13-02-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.4 MSP_A_FPGA-TX1-03-RX13-03-MSP_C_FPGA

Table 2.225: MSP_A_FPGA-TX1-03-RX13-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:32:10		2018-Jan-24 17:32:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10448	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

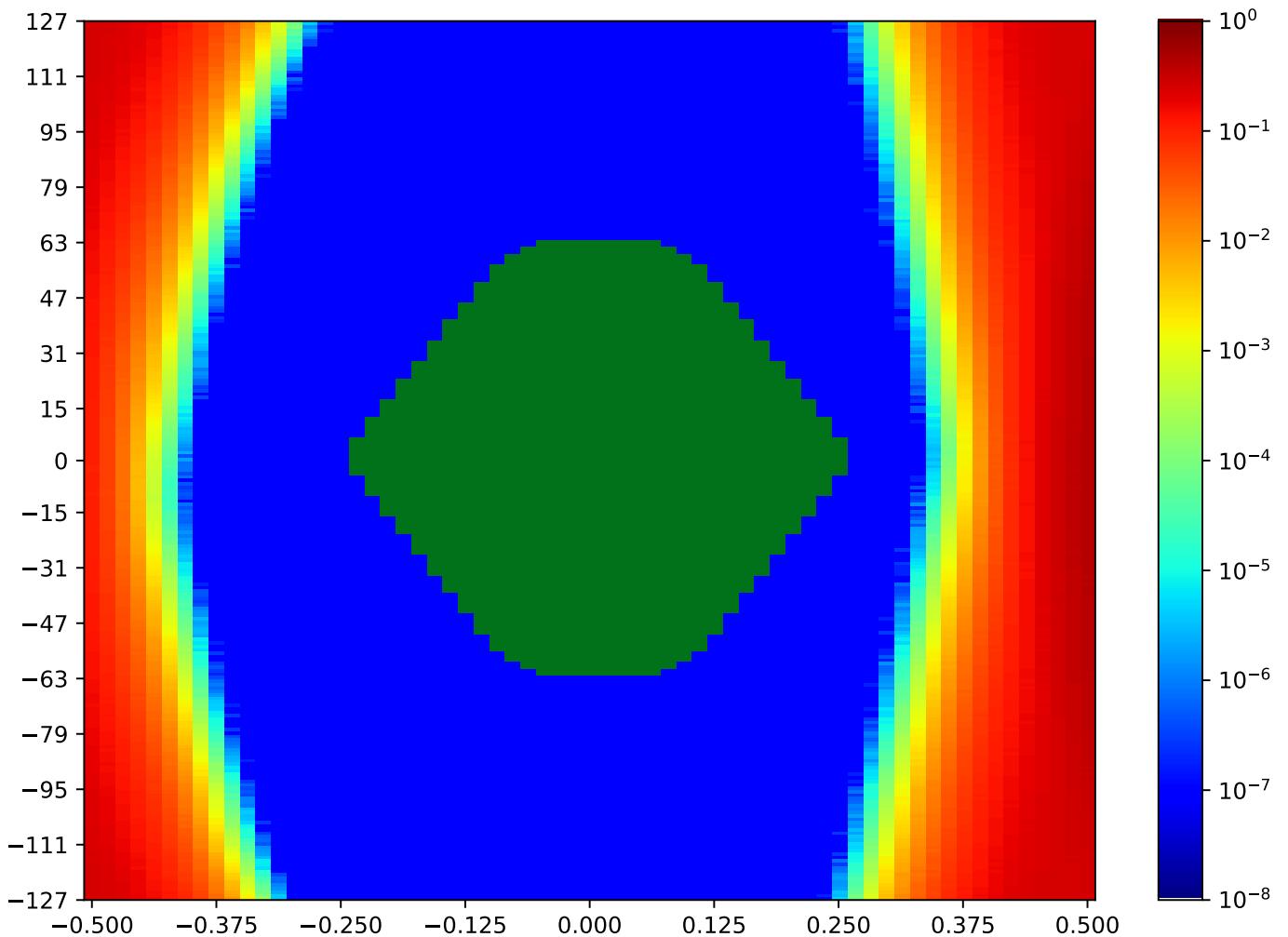


Figure 2.244: MSP_A_FPGA-TX1-03-RX13-03-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.5 MSP_A_FPGA-TX1-04-RX13-04-MSP_C_FPGA

Table 2.226: MSP_A_FPGA-TX1-04-RX13-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:36:51		2018-Jan-24 17:37:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10450	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

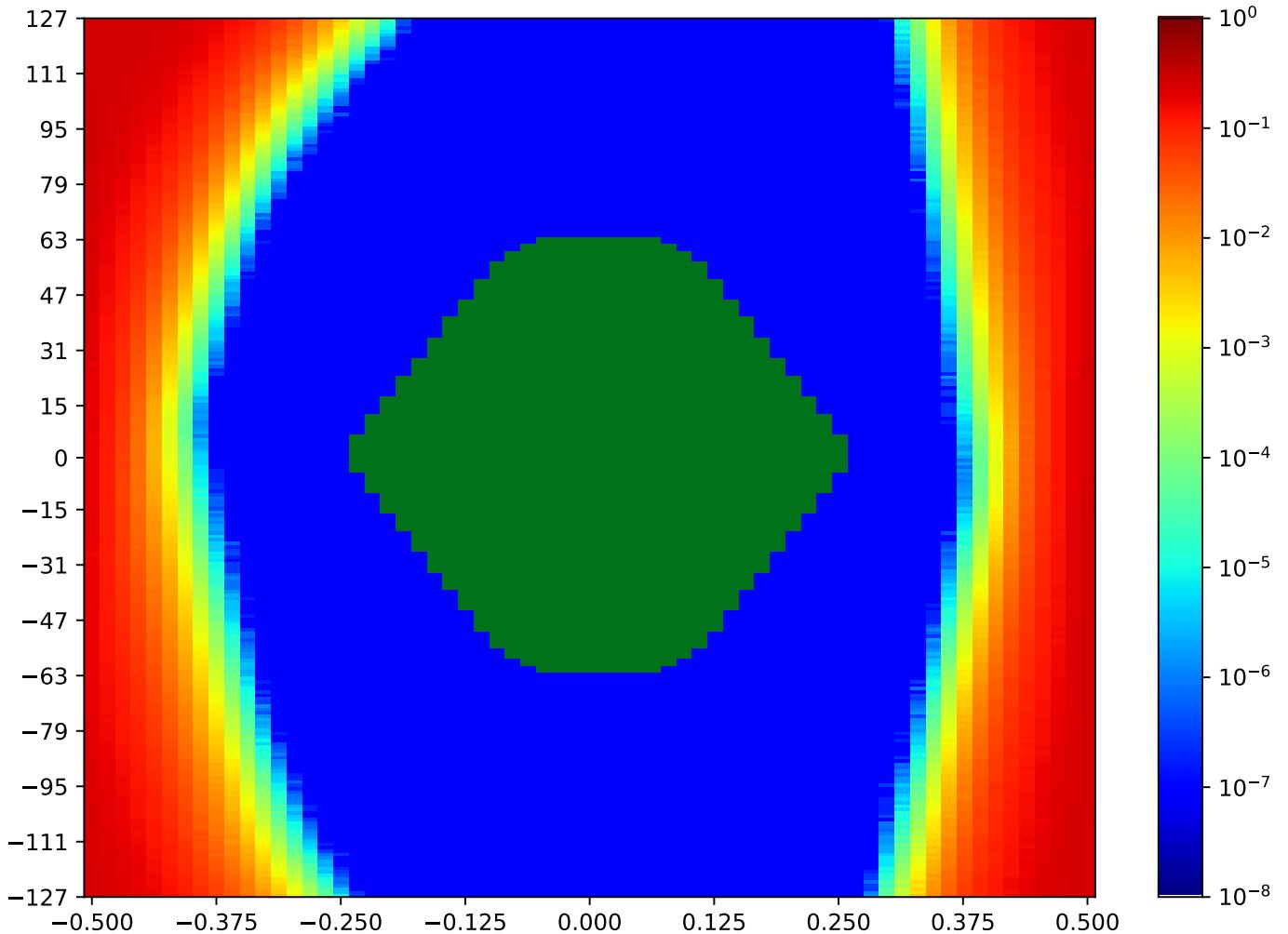


Figure 2.245: MSP_A_FPGA-TX1-04-RX13-04-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.6 MSP_A_FPGA-TX1-05-RX13-05-MSP_C_FPGA

Table 2.227: MSP_A_FPGA-TX1-05-RX13-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:31:34		2018-Jan-24 17:32:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10642	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

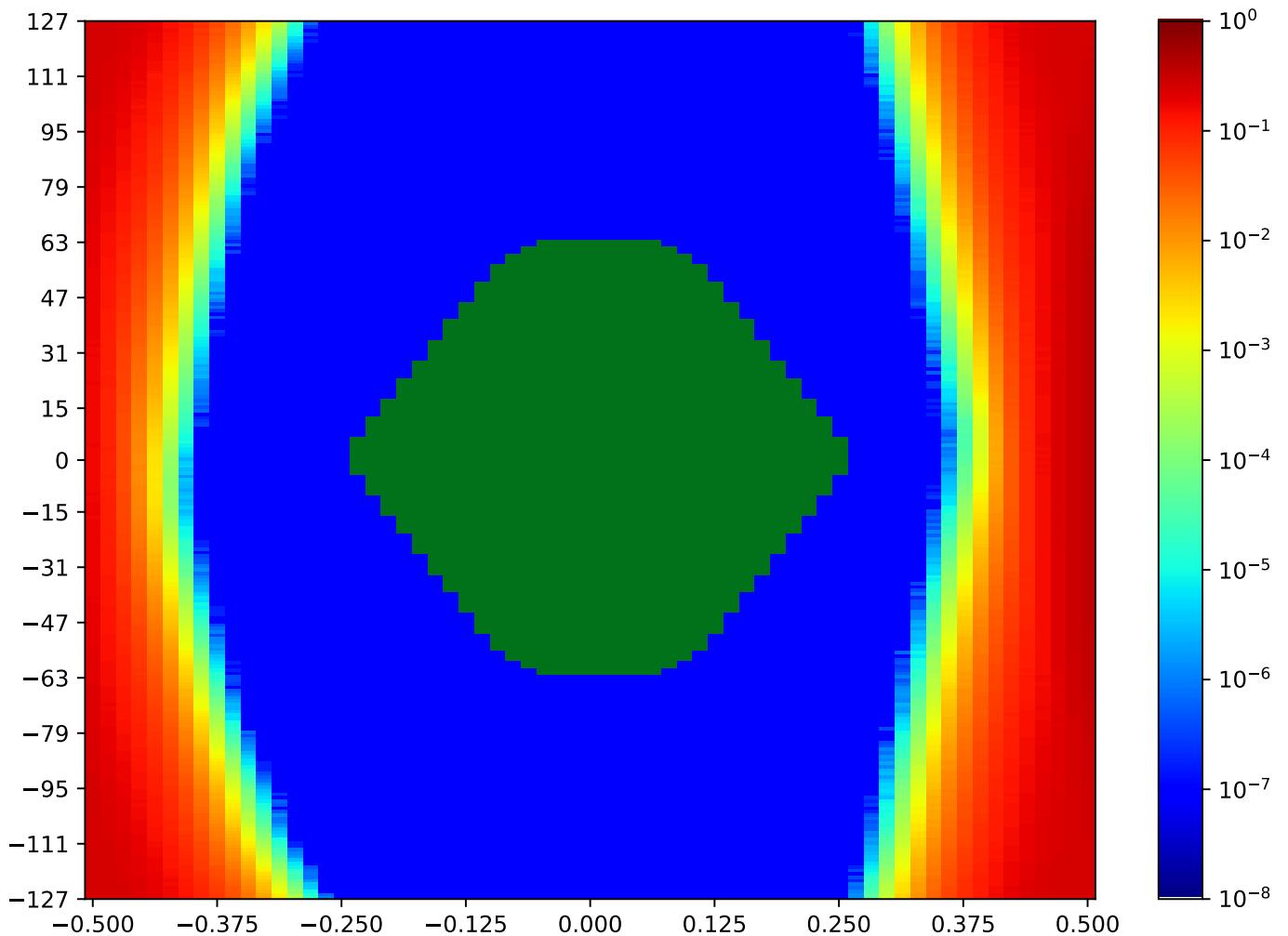


Figure 2.246: MSP_A_FPGA-TX1-05-RX13-05-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.7 MSP_A_FPGA-TX1-06-RX13-06-MSP_C_FPGA

Table 2.228: MSP_A_FPGA-TX1-06-RX13-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:38:02		2018-Jan-24 17:38:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10339	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

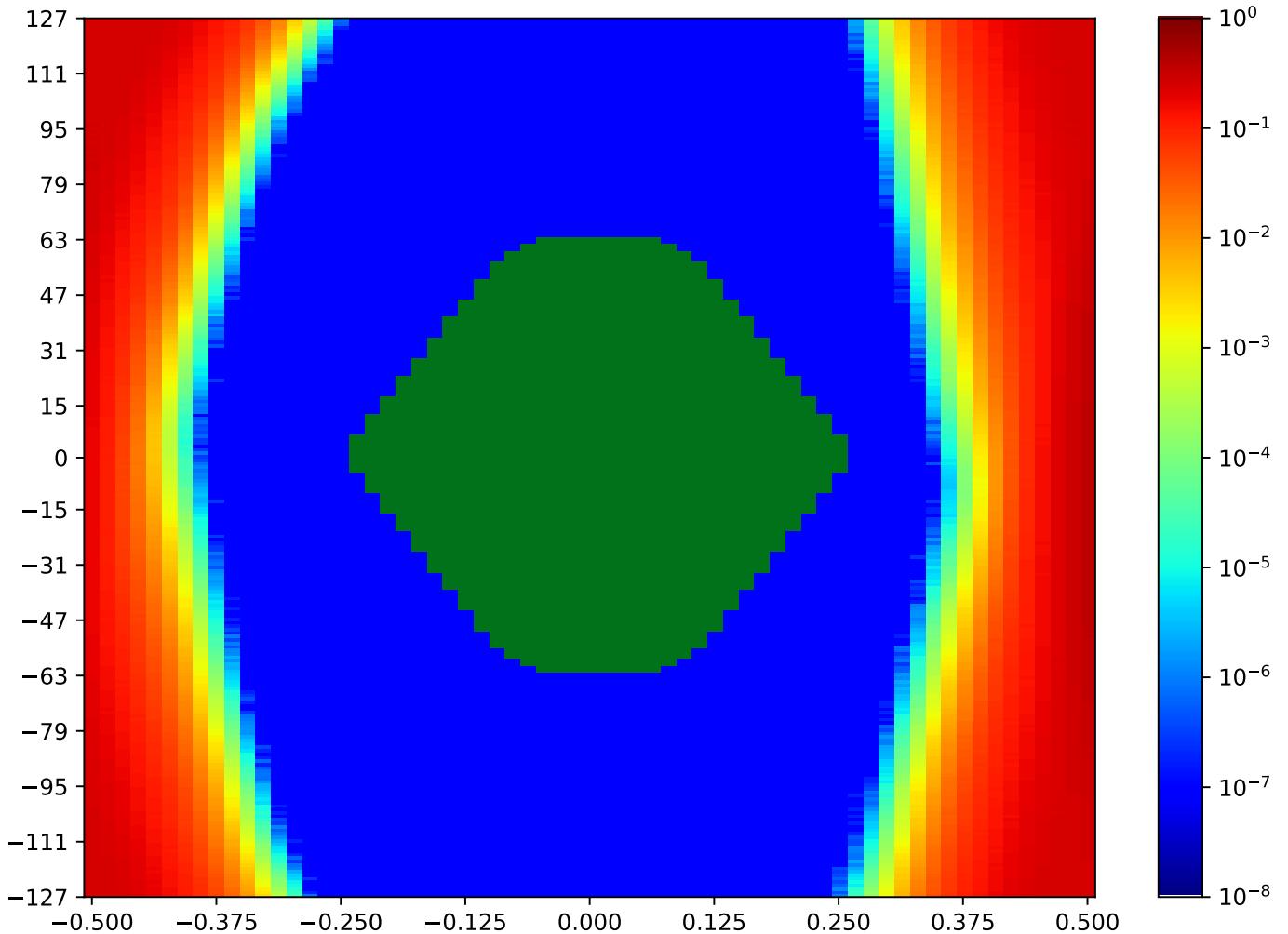


Figure 2.247: MSP_A_FPGA-TX1-06-RX13-06-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.8 MSP_A_FPGA-TX1-07-RX13-07-MSP_C_FPGA

Table 2.229: MSP_A_FPGA-TX1-07-RX13-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:32:45		2018-Jan-24 17:33:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10064	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

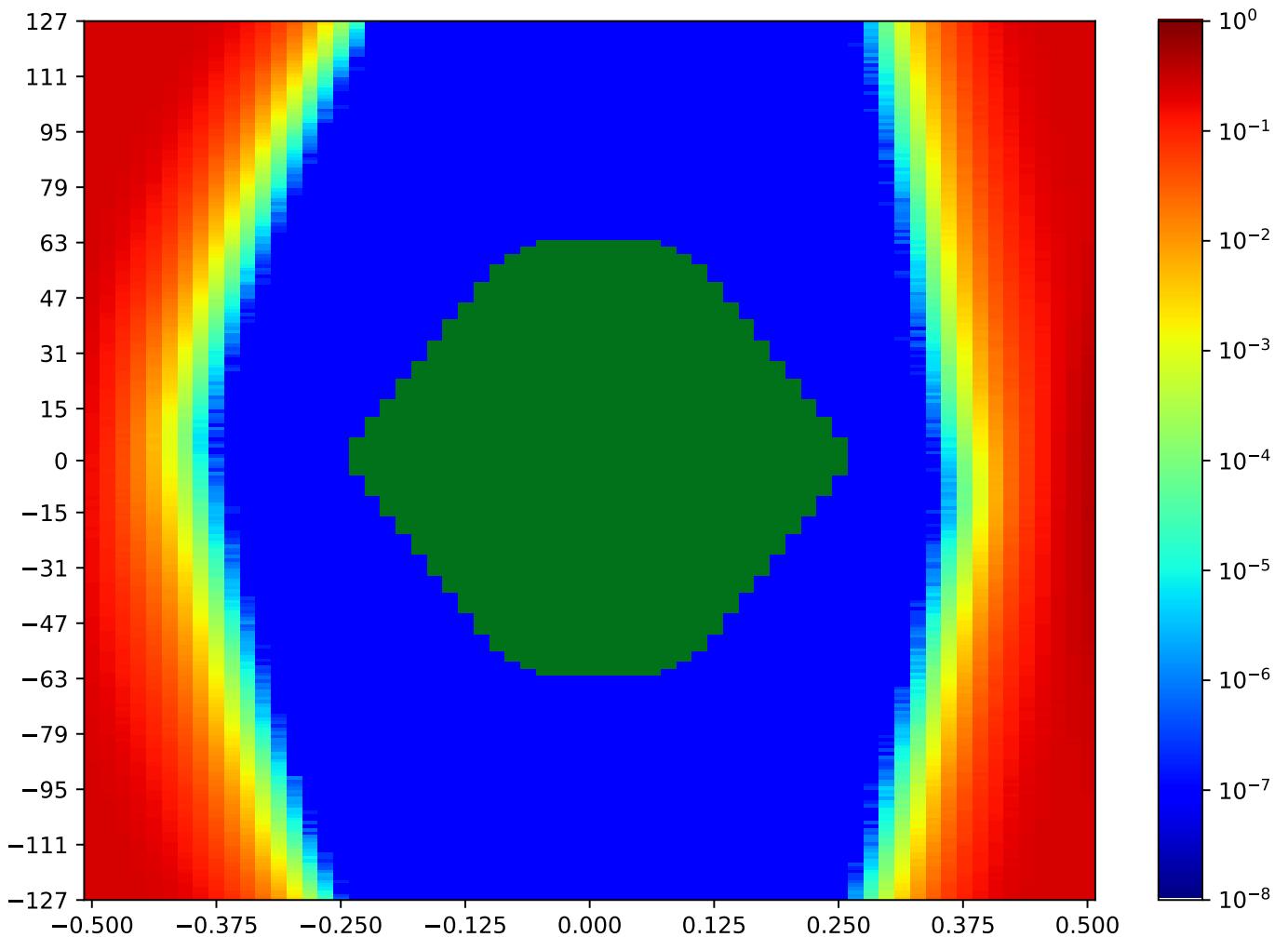


Figure 2.248: MSP_A_FPGA-TX1-07-RX13-07-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.9 MSP_A_FPGA-TX1-08-RX13-08-MSP_C_FPGA

Table 2.230: MSP_A_FPGA-TX1-08-RX13-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:37:27		2018-Jan-24 17:38:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10003	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

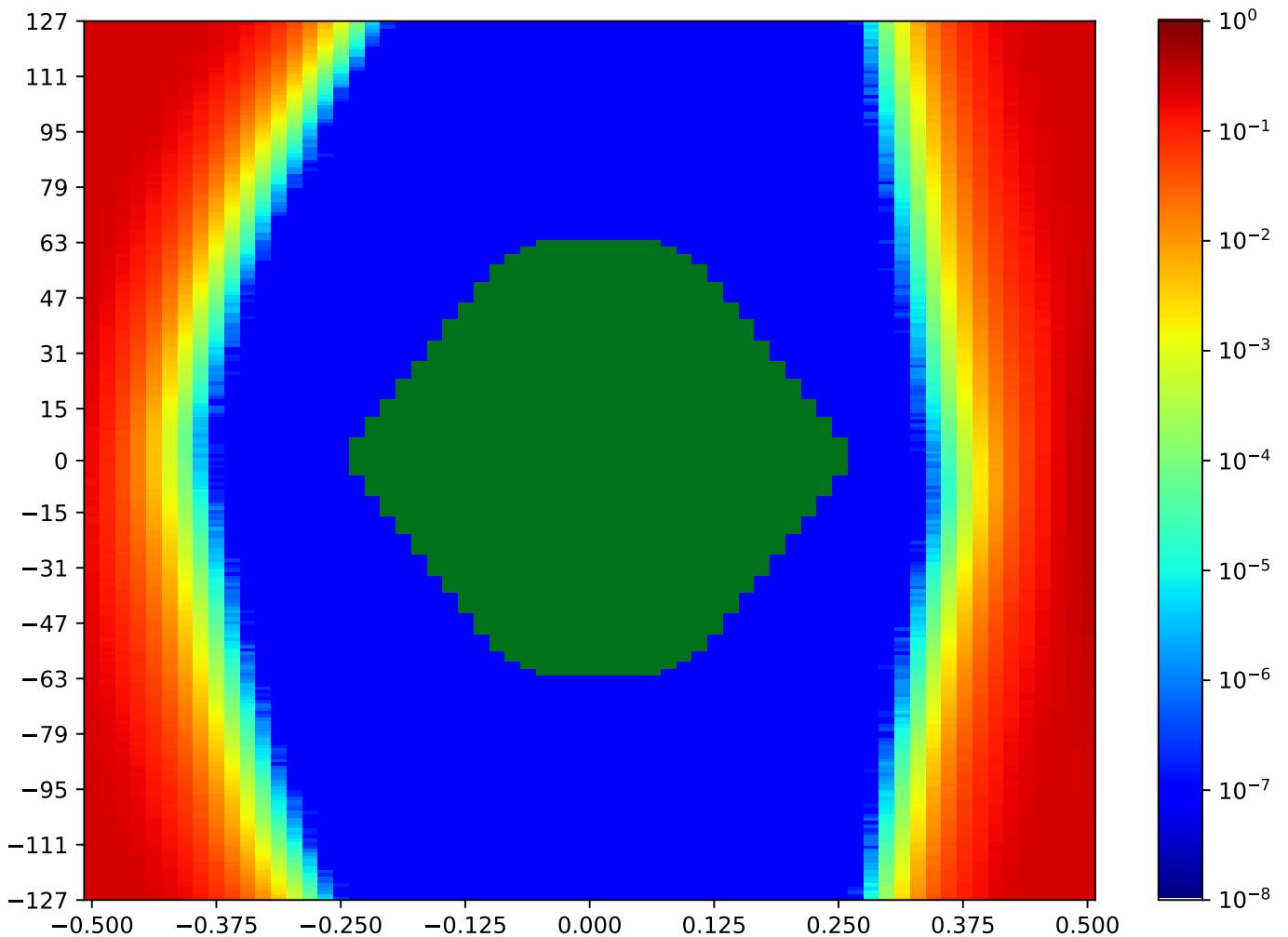


Figure 2.249: MSP_A_FPGA-TX1-08-RX13-08-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.10 MSP_A_FPGA-TX1-09-RX13-09-MSP_C_FPGA

Table 2.231: MSP_A_FPGA-TX1-09-RX13-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:33:57		2018-Jan-24 17:34:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9246	44	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

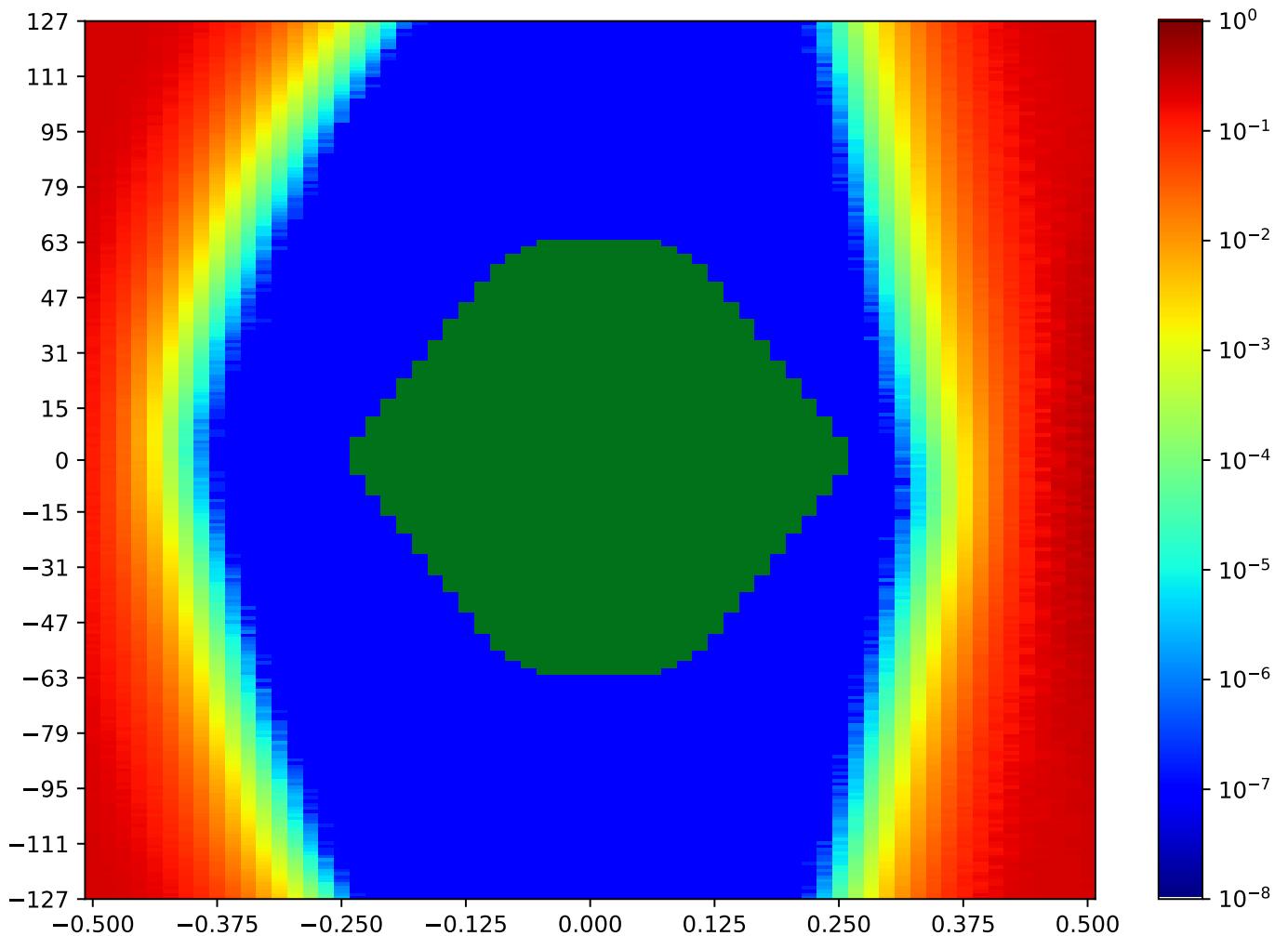


Figure 2.250: MSP_A_FPGA-TX1-09-RX13-09-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.11 MSP_A_FPGA-TX1-10-RX13-10-MSP_C_FPGA

Table 2.232: MSP_A_FPGA-TX1-10-RX13-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:36:16		2018-Jan-24 17:36:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10194	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

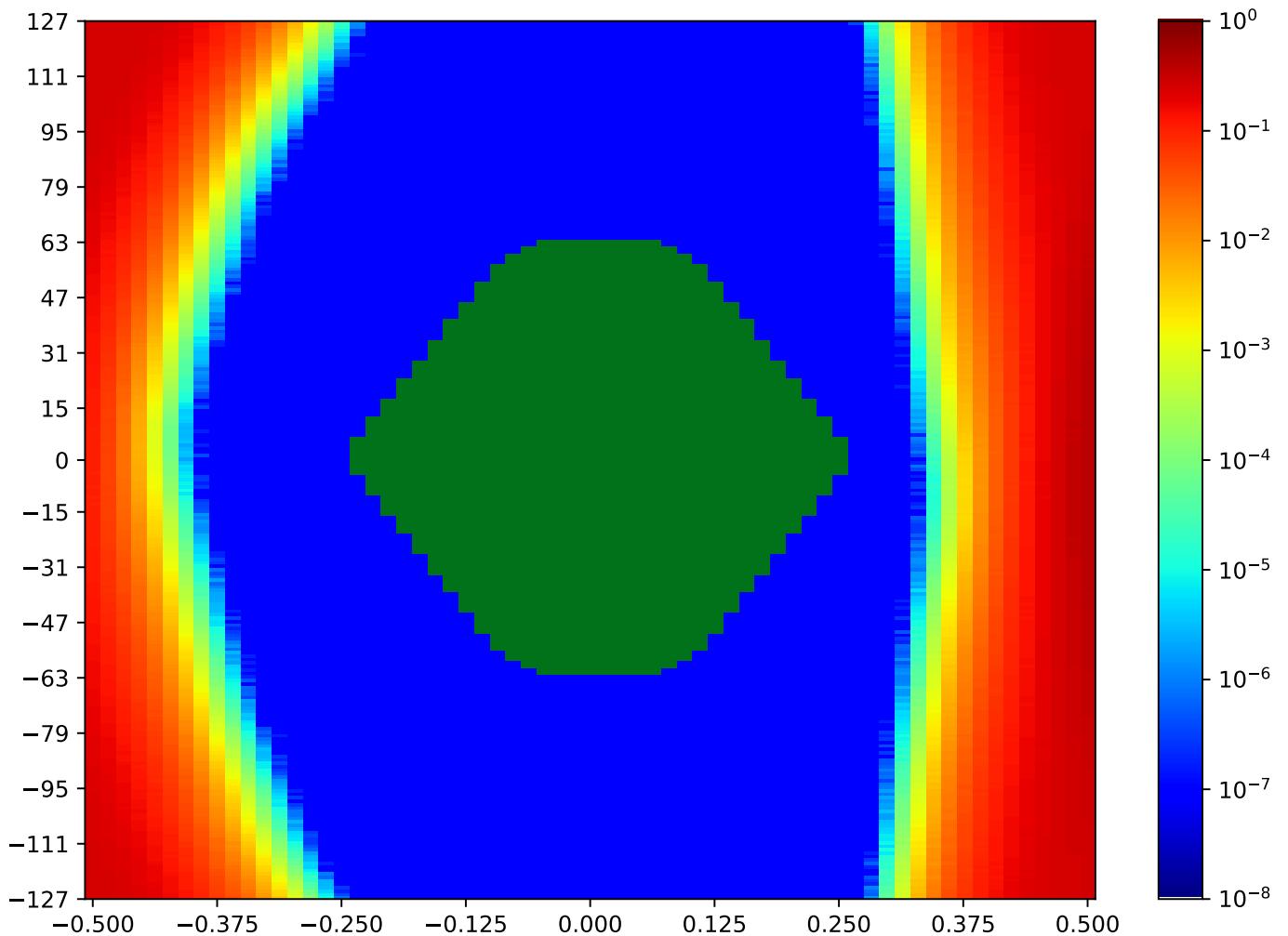


Figure 2.251: MSP_A_FPGA-TX1-10-RX13-10-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.19.12 MSP_A_FPGA-TX1-11-RX13-11-MSP_C_FPGA

Table 2.233: MSP_A_FPGA-TX1-11-RX13-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:35:41		2018-Jan-24 17:36:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9570	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

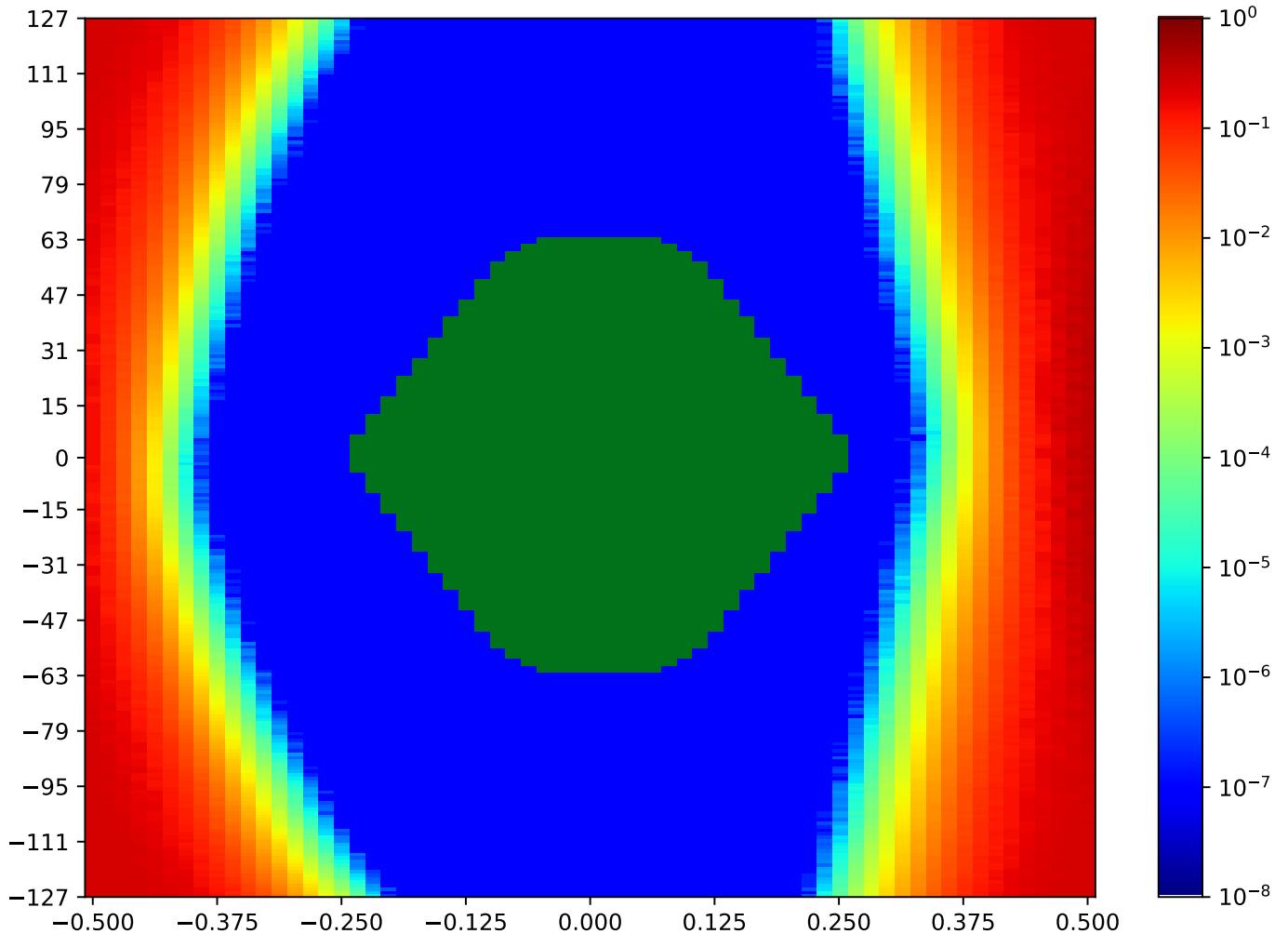


Figure 2.252: MSP_A_FPGA-TX1-11-RX13-11-MSP_C_FPGA

Call back to summary Figure 2.240. Sibling eye diagrams: V1-12.8.

2.20 MSP_A TX2 MSP_C RX12 Minipod Loopback

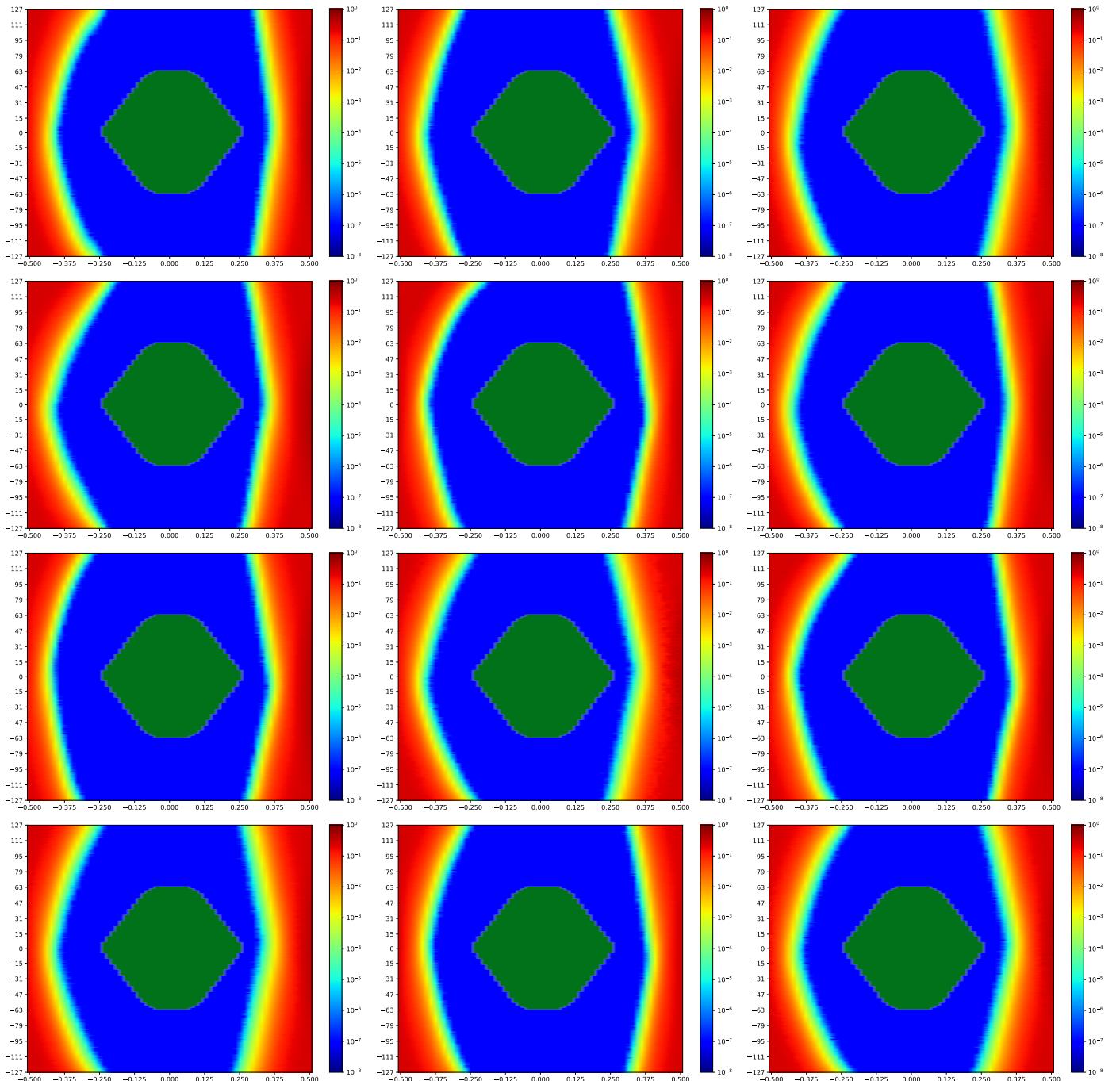


Figure 2.253: MSP_A TX2 MSP_C RX12 Minipod Loopback

A cross-reference to Figure 2.253. Sibling eye diagrams: V1-12.8.

Next summary Figure 2.266.

2.20.1 MSP_A_FPGA-TX2-00-RX12-00-MSP_C_FPGA

Table 2.234: MSP_A_FPGA-TX2-00-RX12-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:40:25		2018-Jan-24 17:41:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10309	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

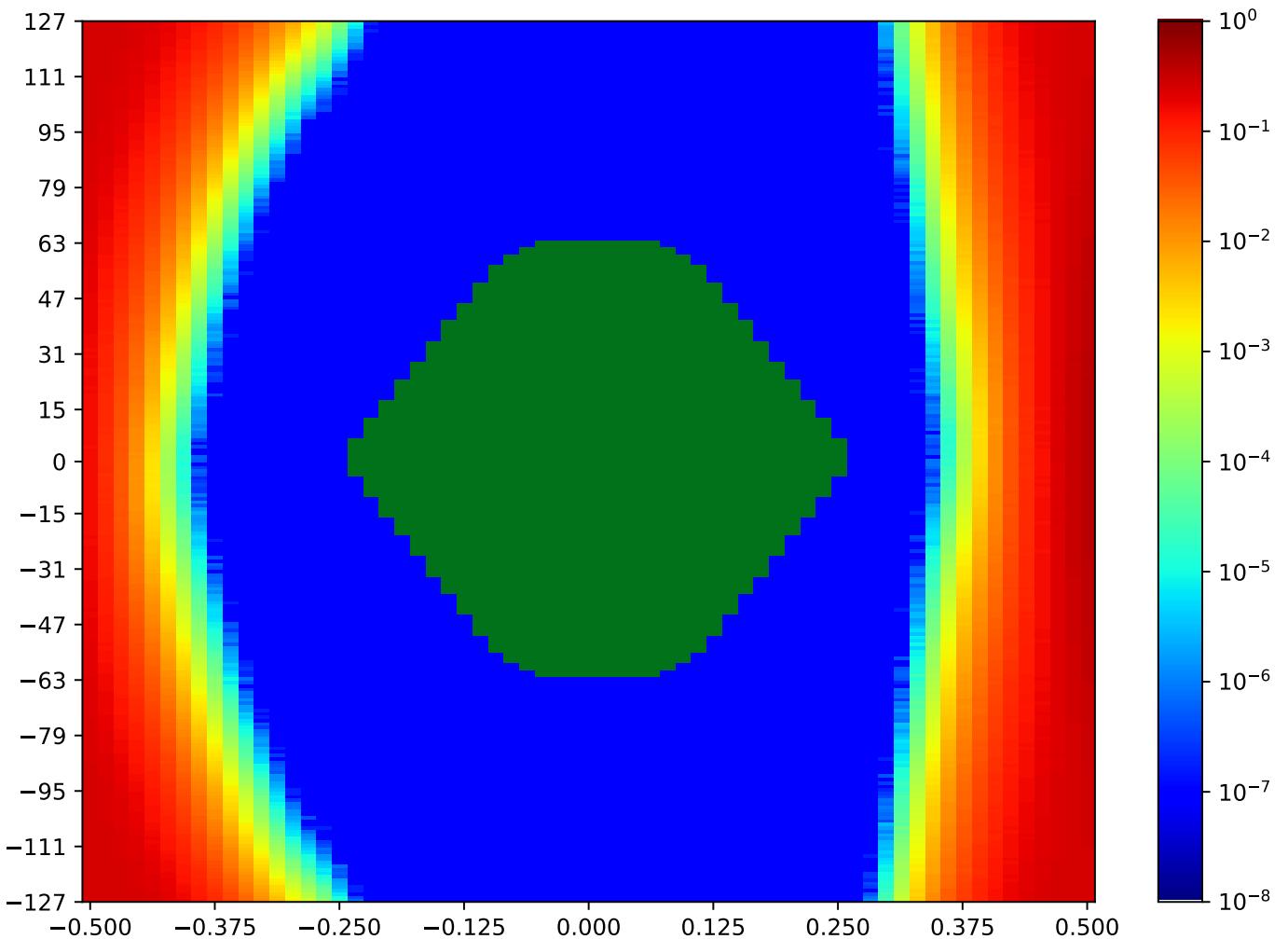


Figure 2.254: MSP_A_FPGA-TX2-00-RX12-00-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.2 MSP_A_FPGA-TX2-01-RX12-01-MSP_C_FPGA

Table 2.235: MSP_A_FPGA-TX2-01-RX12-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:39:14		2018-Jan-24 17:39:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9844	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

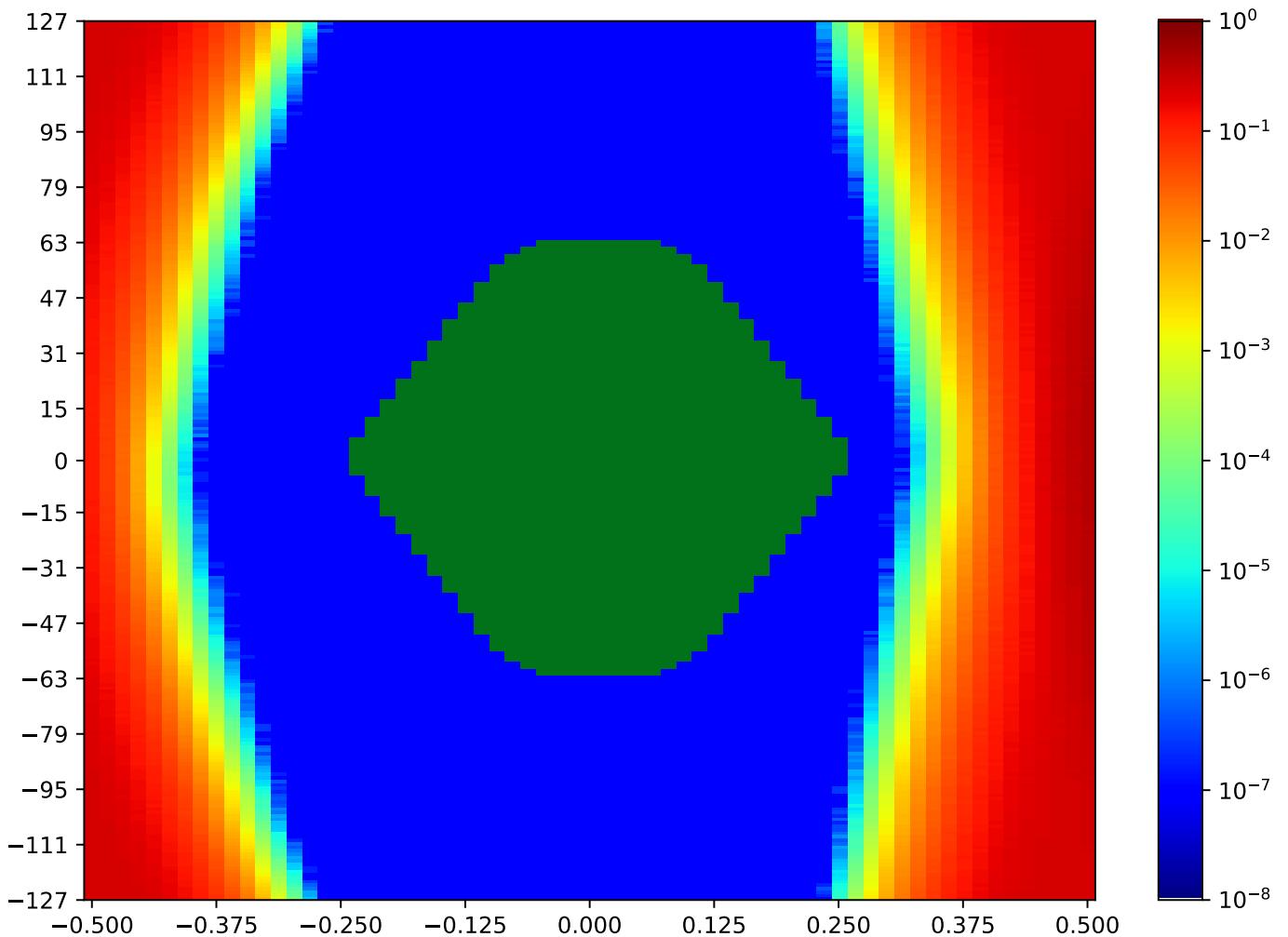


Figure 2.255: MSP_A_FPGA-TX2-01-RX12-01-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.3 MSP_A_FPGA-TX2-02-RX12-02-MSP_C_FPGA

Table 2.236: MSP_A_FPGA-TX2-02-RX12-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:42:12		2018-Jan-24 17:42:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9925	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

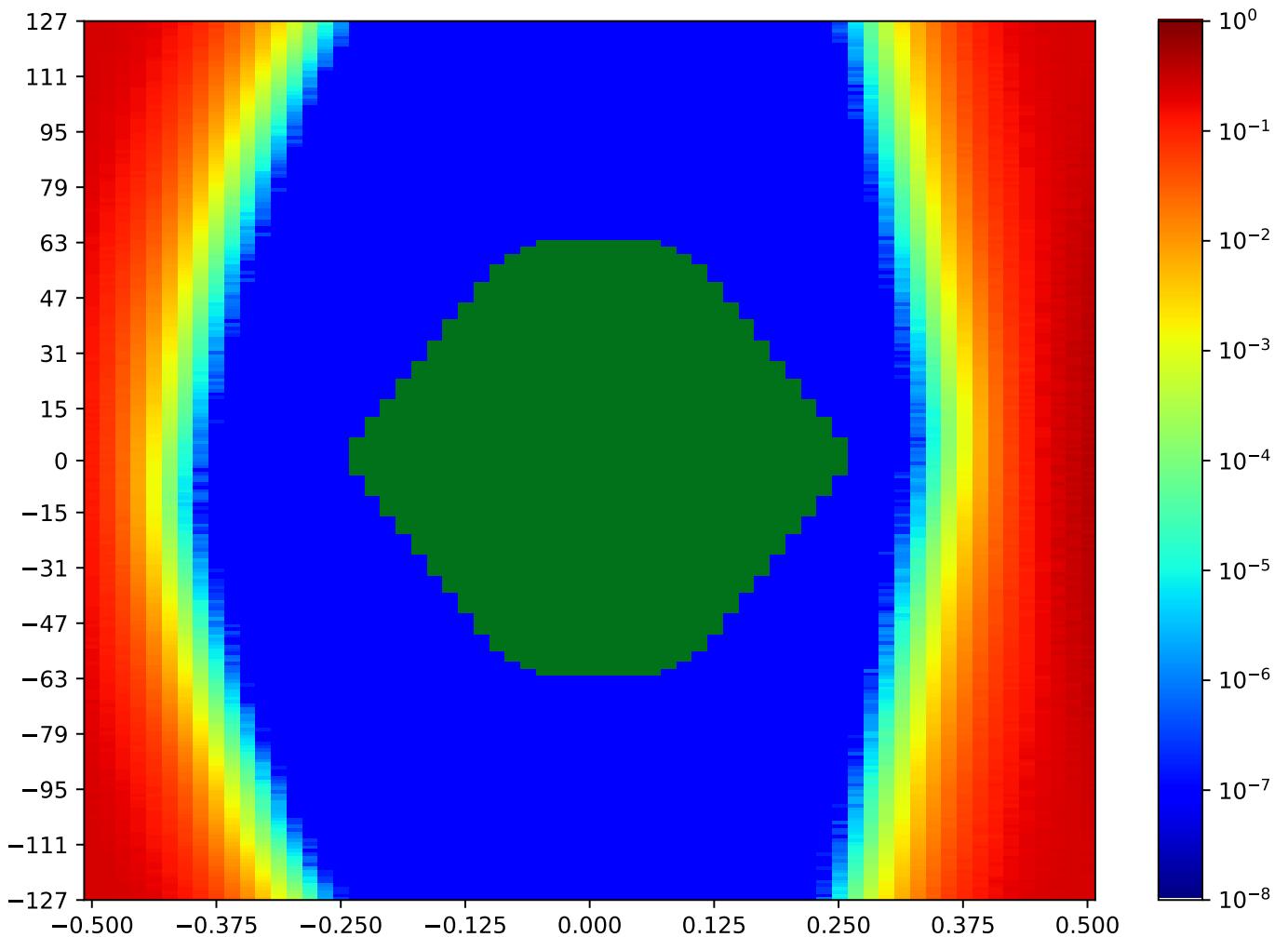


Figure 2.256: MSP_A_FPGA-TX2-02-RX12-02-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.4 MSP_A_FPGA-TX2-03-RX12-03-MSP_C_FPGA

Table 2.237: MSP_A_FPGA-TX2-03-RX12-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:38:39		2018-Jan-24 17:39:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9632	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

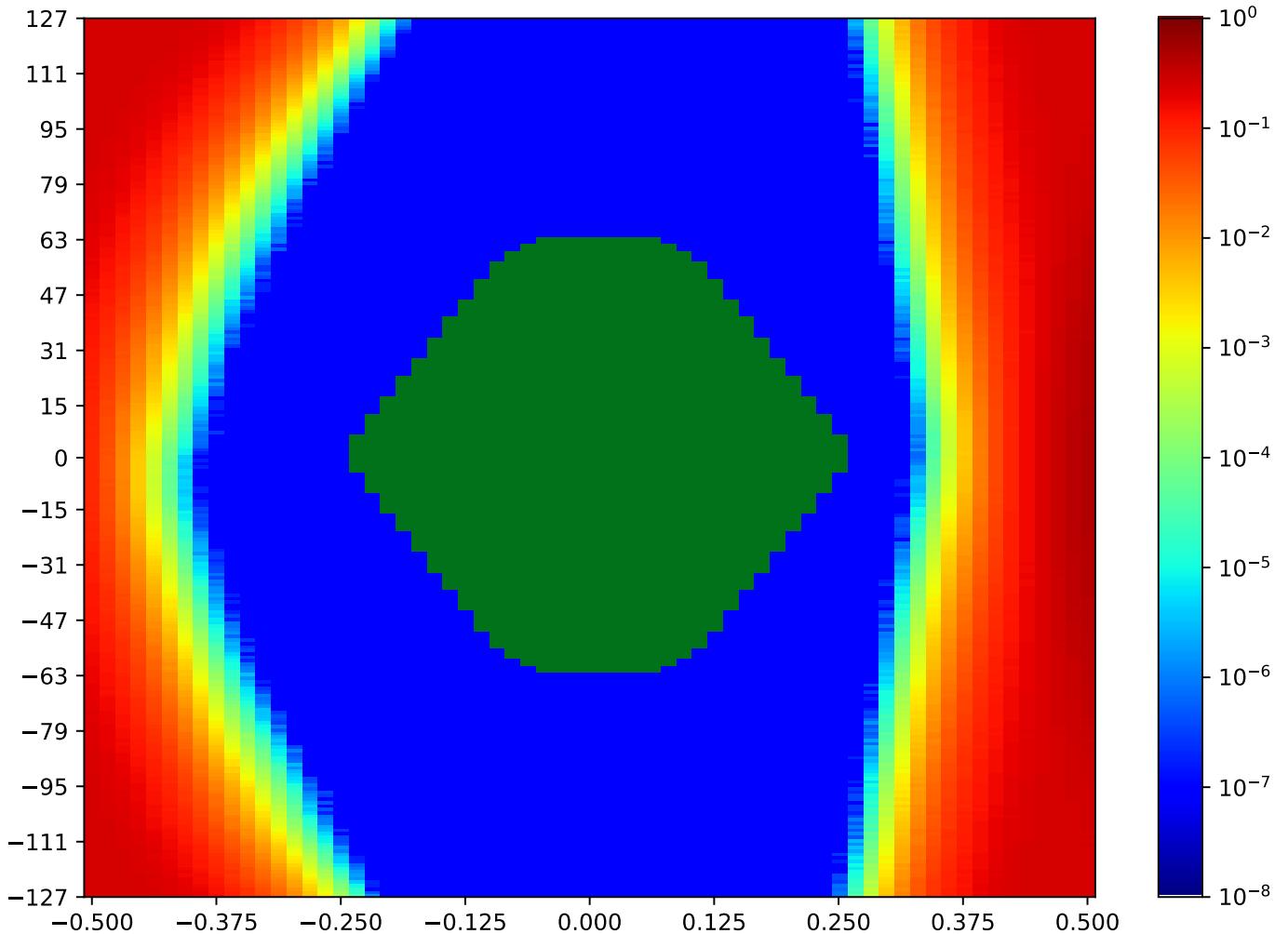


Figure 2.257: MSP_A_FPGA-TX2-03-RX12-03-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.5 MSP_A_FPGA-TX2-04-RX12-04-MSP_C_FPGA

Table 2.238: MSP_A_FPGA-TX2-04-RX12-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:44:01		2018-Jan-24 17:44:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10527	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

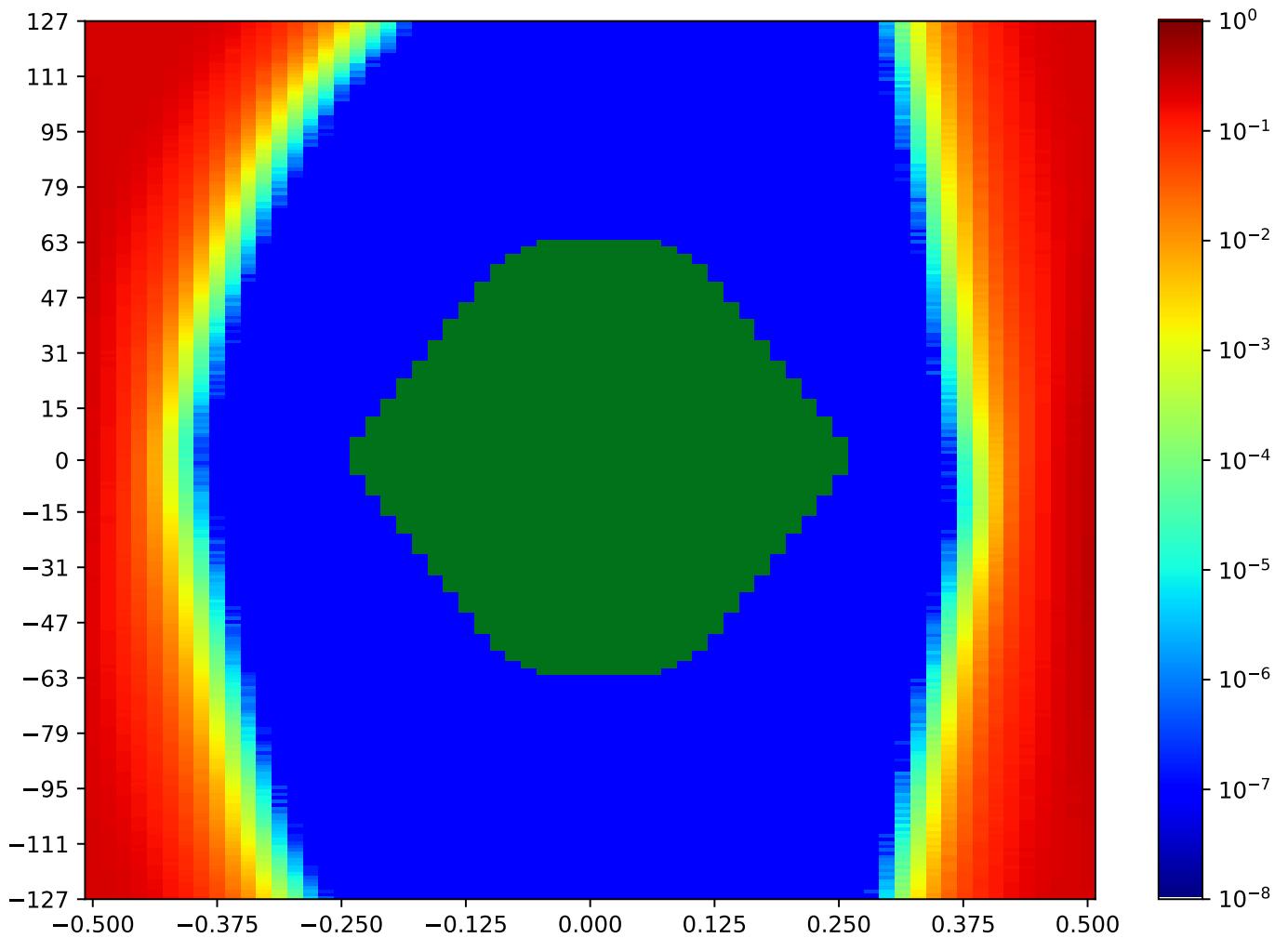


Figure 2.258: MSP_A_FPGA-TX2-04-RX12-04-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.6 MSP_A_FPGA-TX2-05-RX12-05-MSP_C_FPGA

Table 2.239: MSP_A_FPGA-TX2-05-RX12-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:39:49		2018-Jan-24 17:40:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10060	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

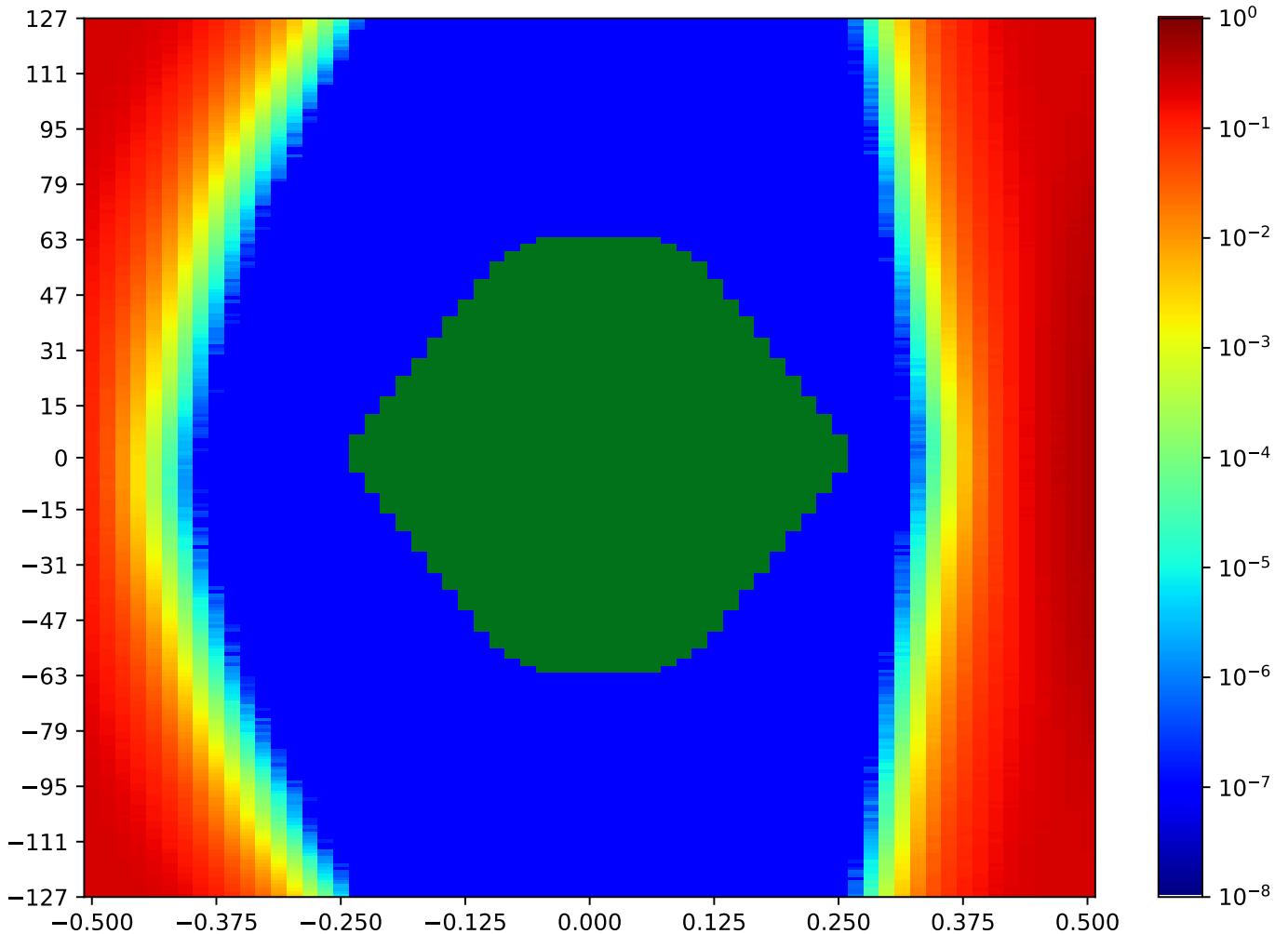


Figure 2.259: MSP_A_FPGA-TX2-05-RX12-05-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.7 MSP_A_FPGA-TX2-06-RX12-06-MSP_C_FPGA

Table 2.240: MSP_A_FPGA-TX2-06-RX12-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:45:14		2018-Jan-24 17:45:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10641	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

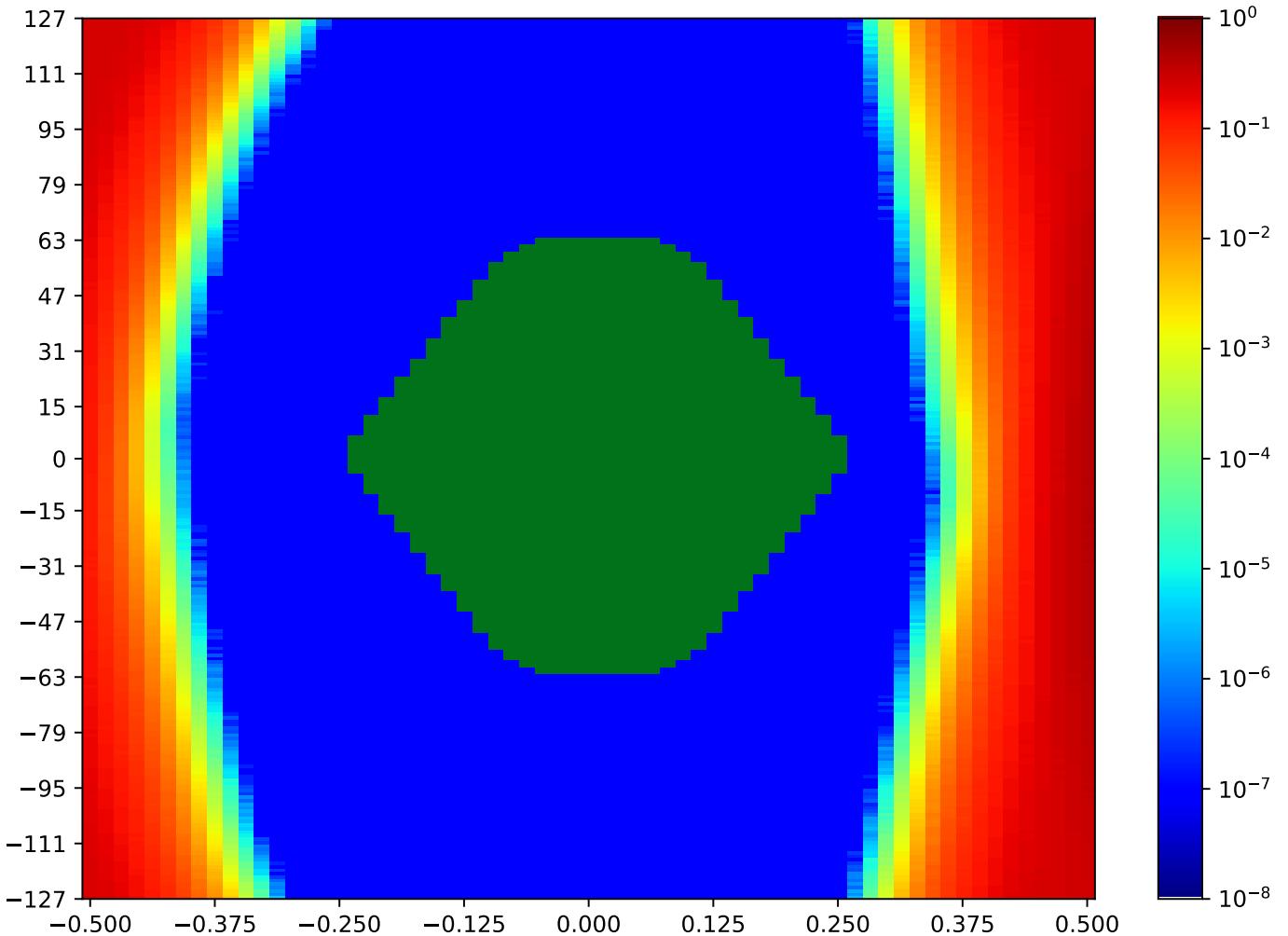


Figure 2.260: MSP_A_FPGA-TX2-06-RX12-06-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.8 MSP_A_FPGA-TX2-07-RX12-07-MSP_C_FPGA

Table 2.241: MSP_A_FPGA-TX2-07-RX12-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:41:01		2018-Jan-24 17:41:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9436	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

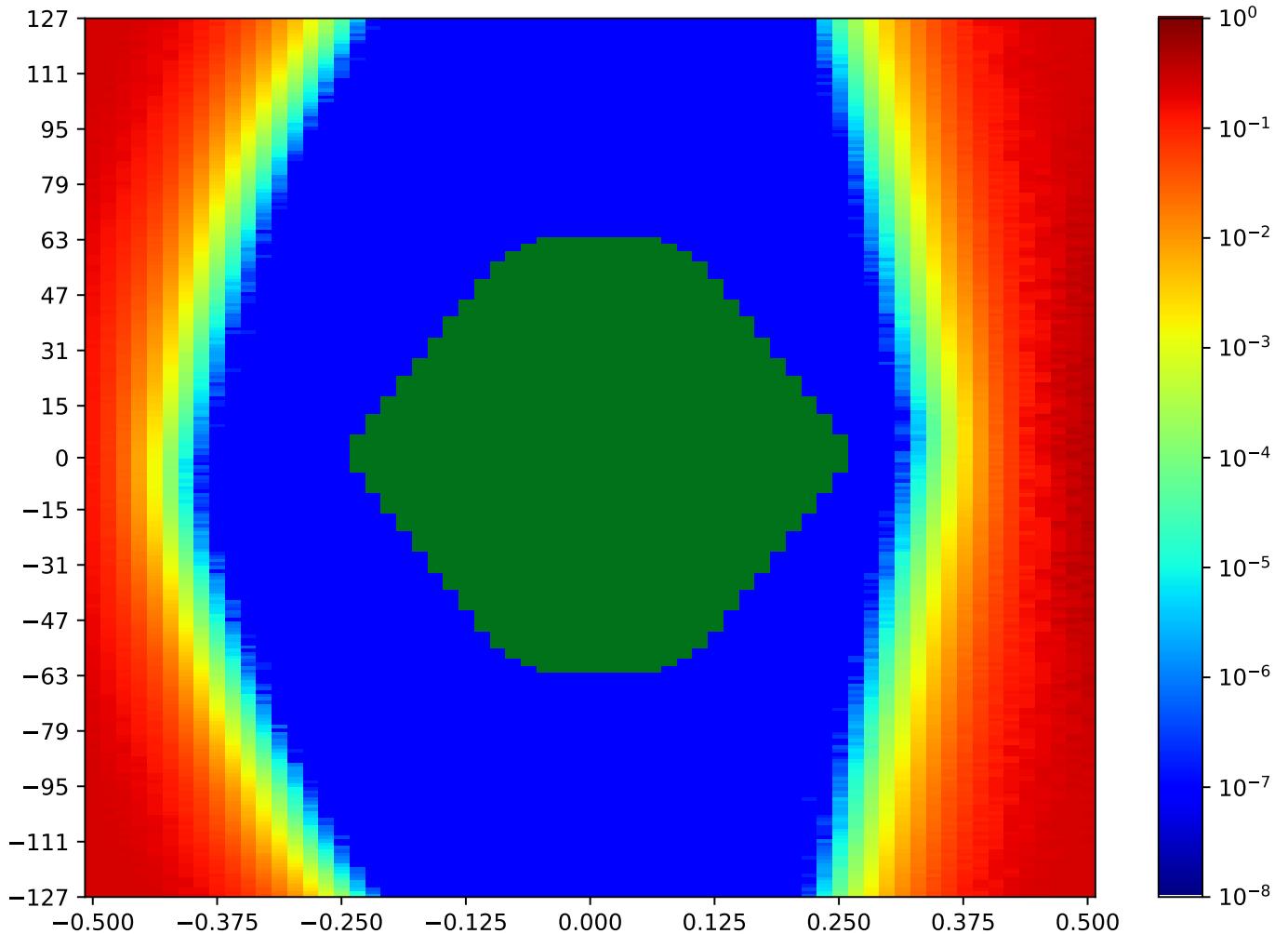


Figure 2.261: MSP_A_FPGA-TX2-07-RX12-07-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.9 MSP_A_FPGA-TX2-08-RX12-08-MSP_C_FPGA

Table 2.242: MSP_A_FPGA-TX2-08-RX12-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:44:37		2018-Jan-24 17:45:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10209	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

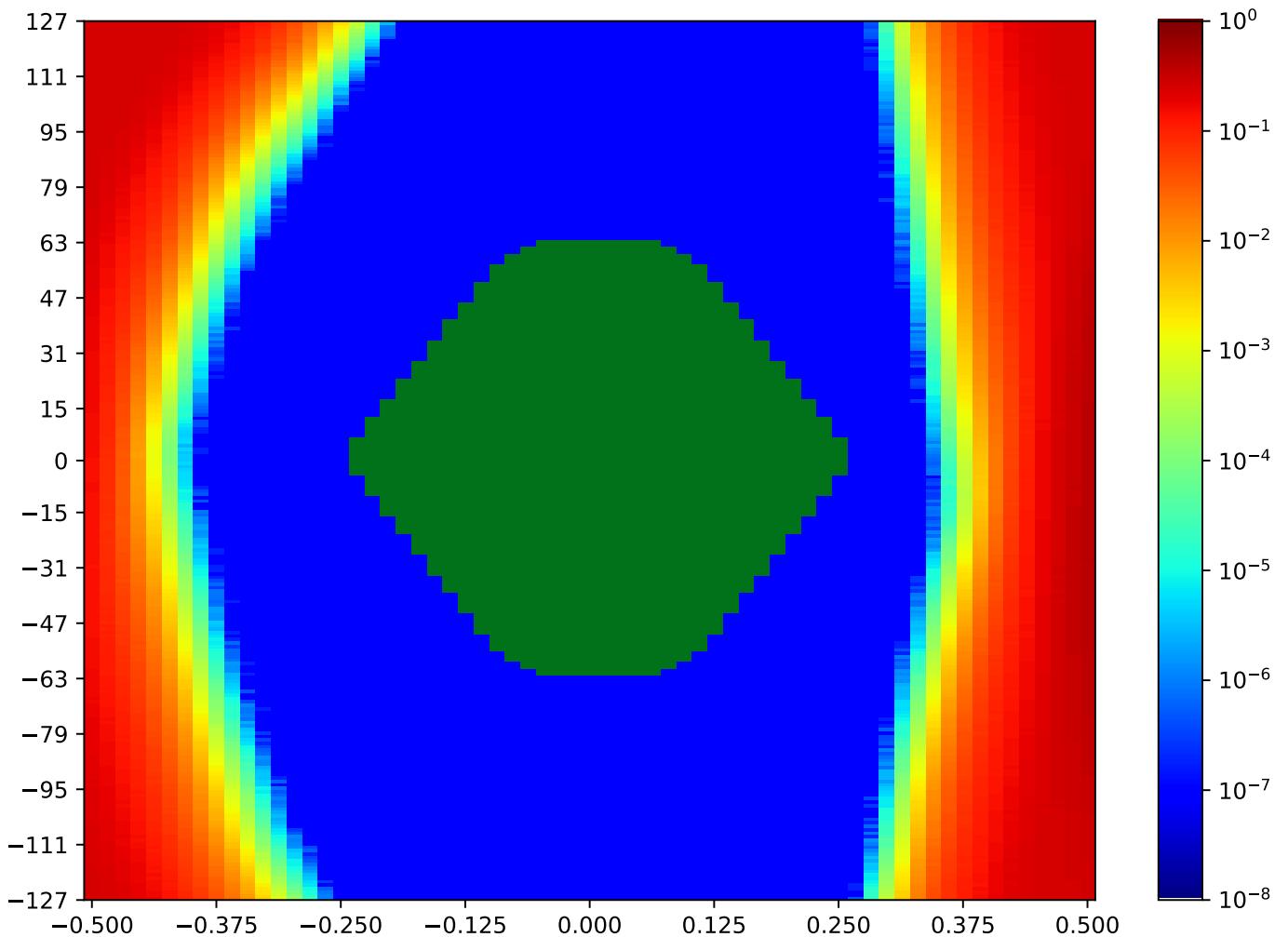


Figure 2.262: MSP_A_FPGA-TX2-08-RX12-08-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.10 MSP_A_FPGA-TX2-09-RX12-09-MSP_C_FPGA

Table 2.243: MSP_A_FPGA-TX2-09-RX12-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:41:37		2018-Jan-24 17:42:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9434	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

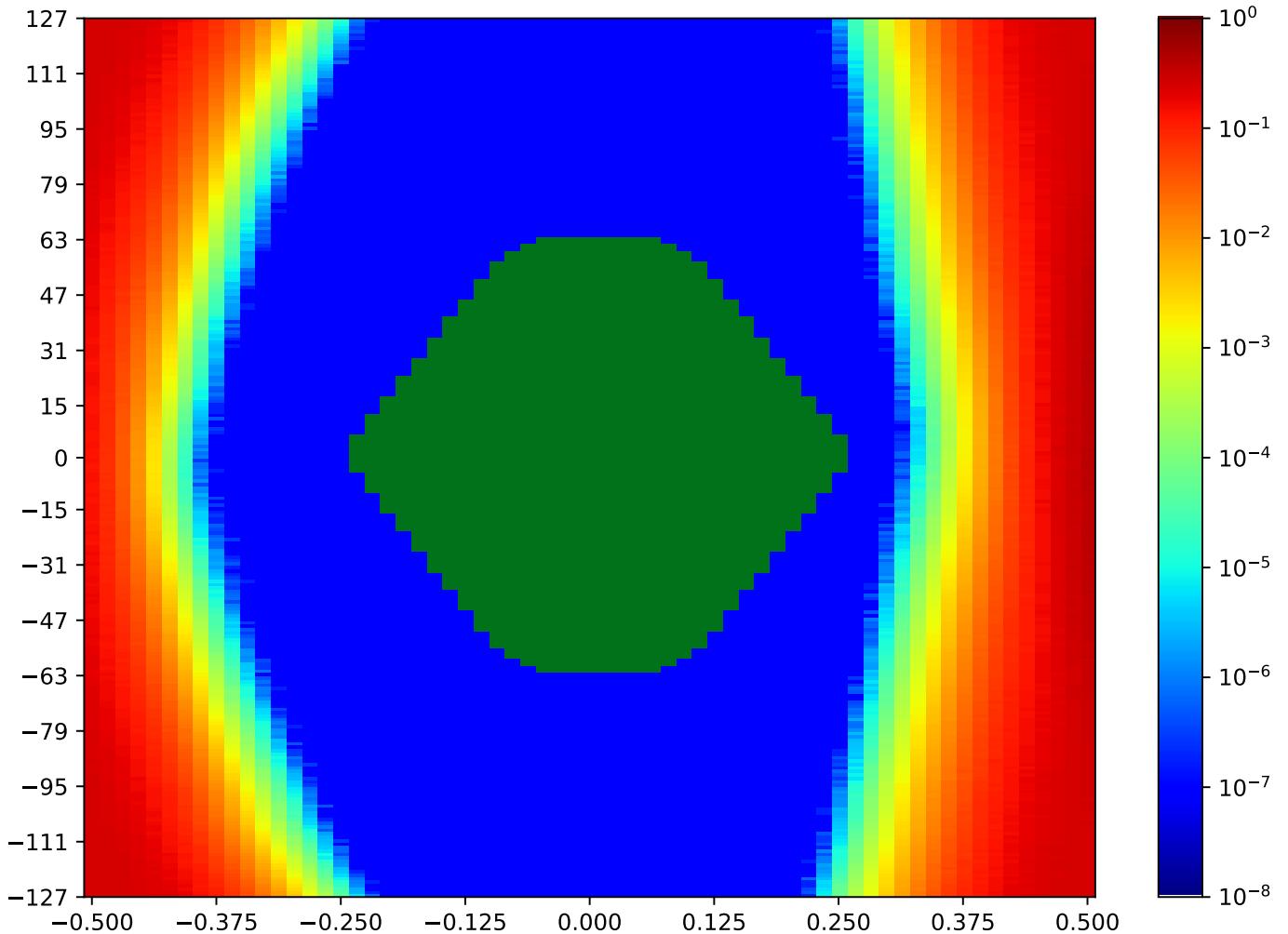


Figure 2.263: MSP_A_FPGA-TX2-09-RX12-09-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.11 MSP_A_FPGA-TX2-10-RX12-10-MSP_C_FPGA

Table 2.244: MSP_A_FPGA-TX2-10-RX12-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:43:24		2018-Jan-24 17:44:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10612	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

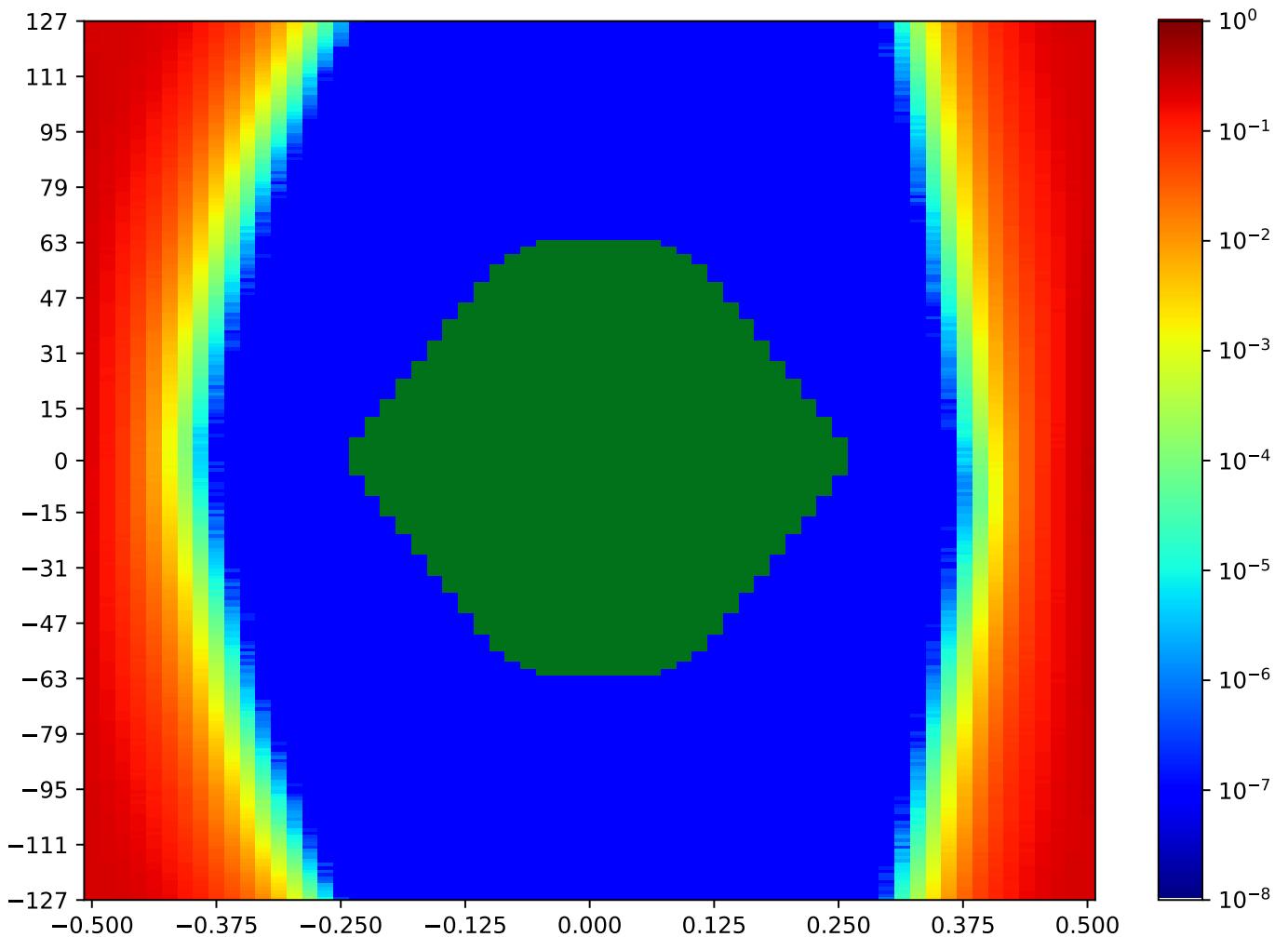


Figure 2.264: MSP_A_FPGA-TX2-10-RX12-10-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.20.12 MSP_A_FPGA-TX2-11-RX12-11-MSP_C_FPGA

Table 2.245: MSP_A_FPGA-TX2-11-RX12-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:42:48		2018-Jan-24 17:43:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9389	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

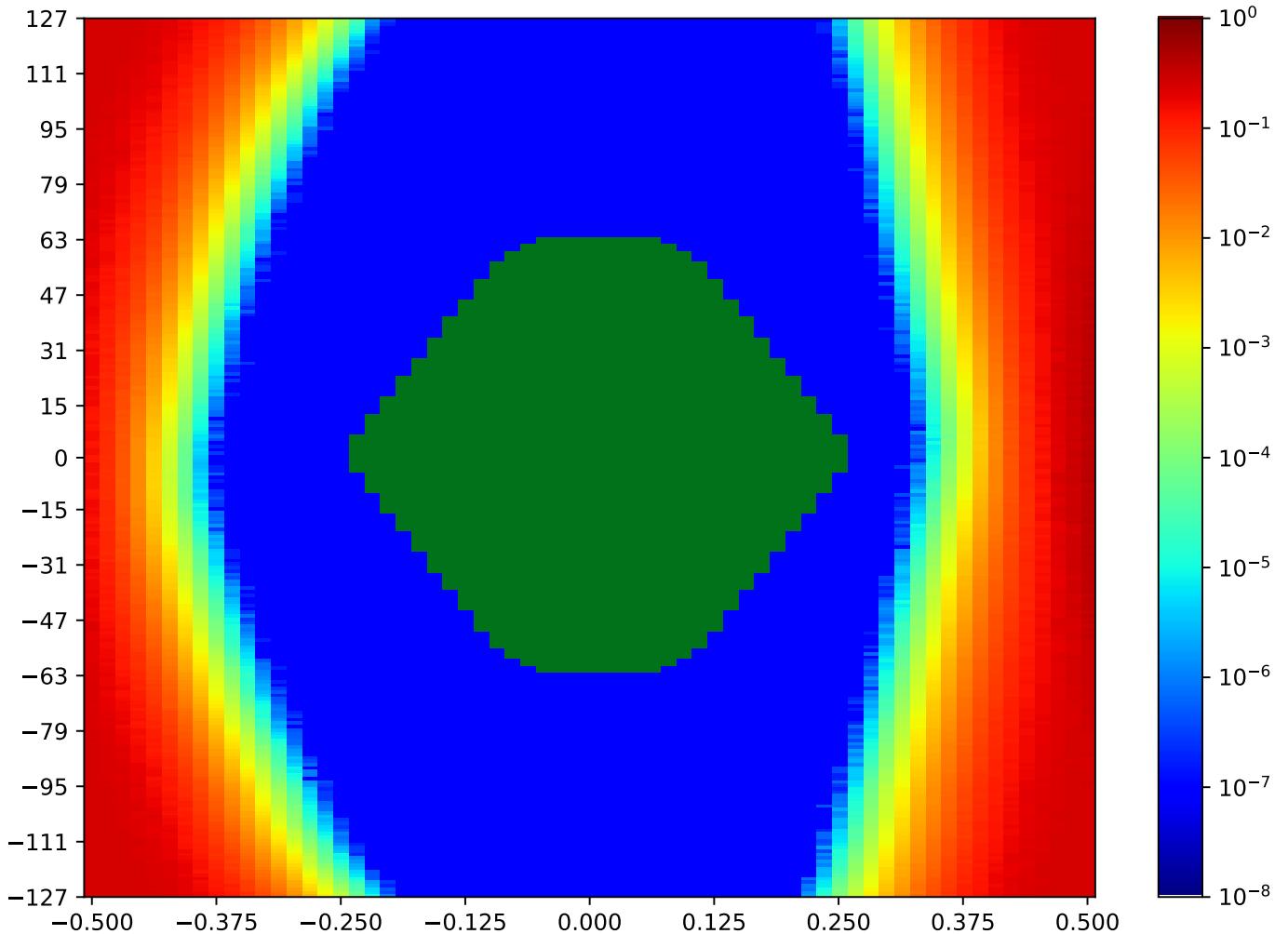


Figure 2.265: MSP_A_FPGA-TX2-11-RX12-11-MSP_C_FPGA

Call back to summary Figure 2.253. Sibling eye diagrams: V1-12.8.

2.21 MSP_C TX3 MSP_A RX4 Minipod Loopback

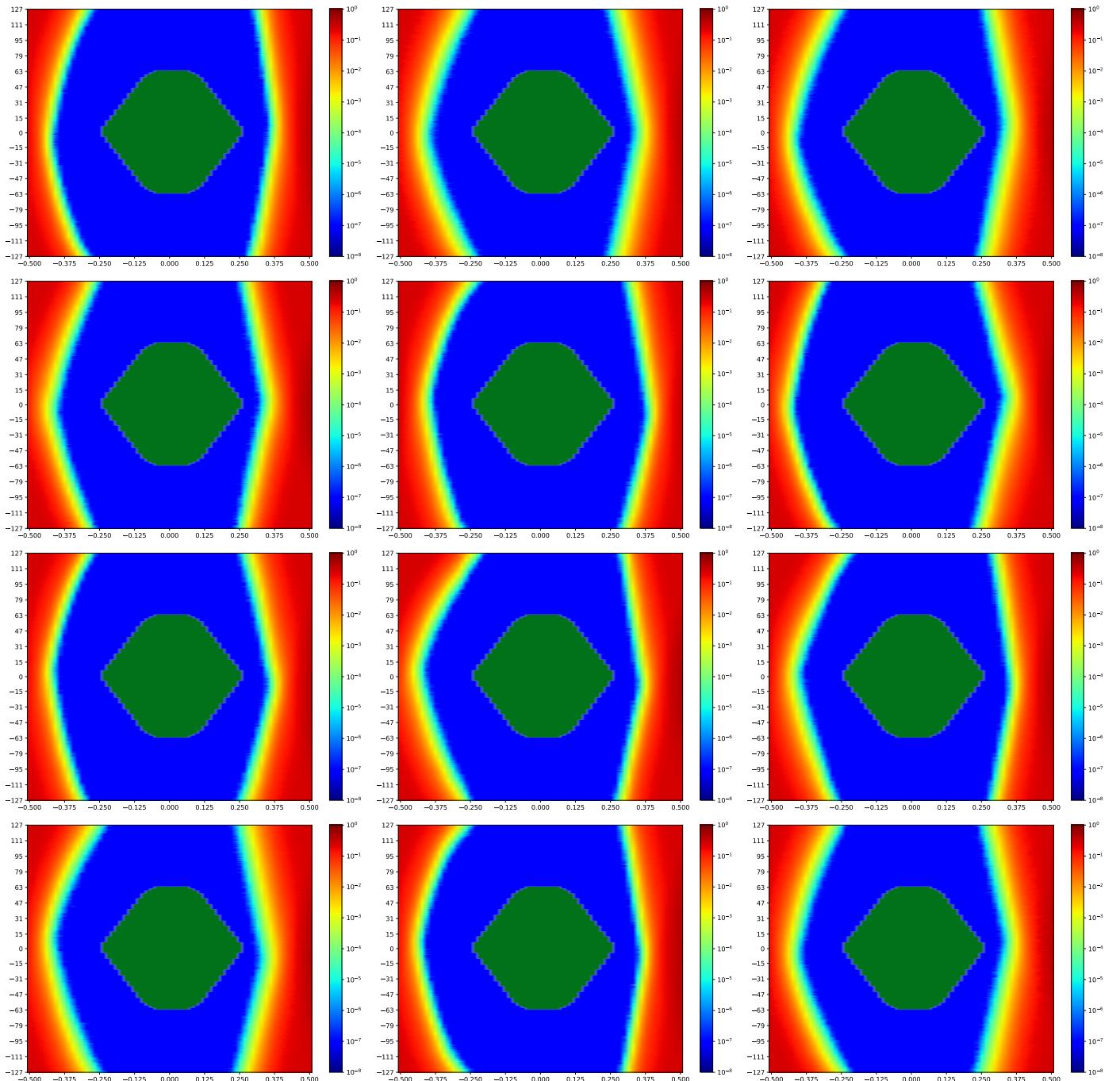


Figure 2.266: MSP_C TX3 MSP_A RX4 Minipod Loopback

A cross-reference to Figure 2.266. Sibling eye diagrams: V1-12.8.
Next summary Figure 2.279.

2.21.1 MSP_C_FPGA-TX3-00-RX4-00-MSP_A_FPGA

Table 2.246: MSP_C_FPGA-TX3-00-RX4-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:47:37		2018-Jan-24 17:48:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10745	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

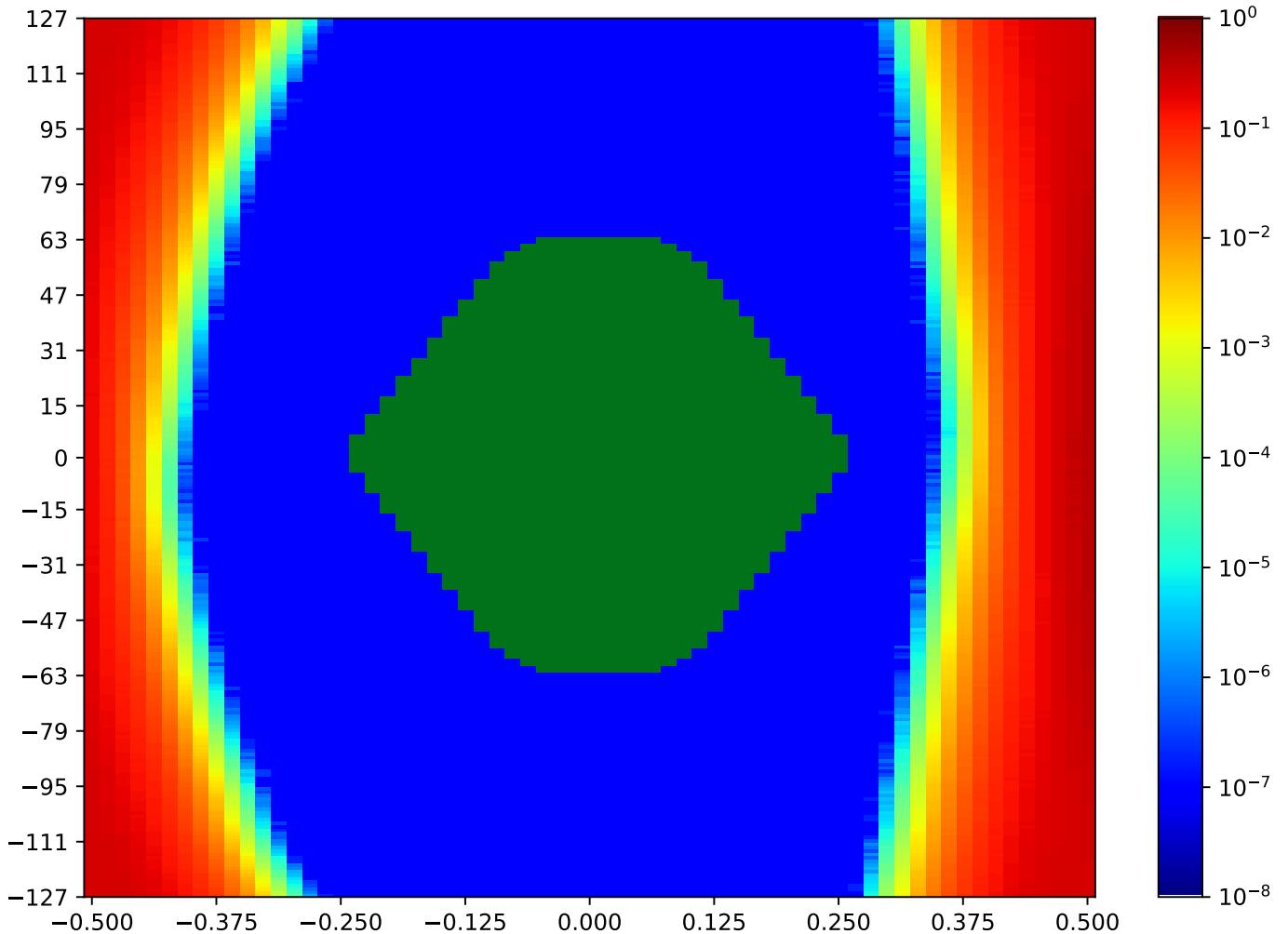


Figure 2.267: MSP_C_FPGA-TX3-00-RX4-00-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.2 MSP_C_FPGA-TX3-01-RX4-01-MSP_A_FPGA

Table 2.247: MSP_C_FPGA-TX3-01-RX4-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:48:49		2018-Jan-24 17:49:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9327	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

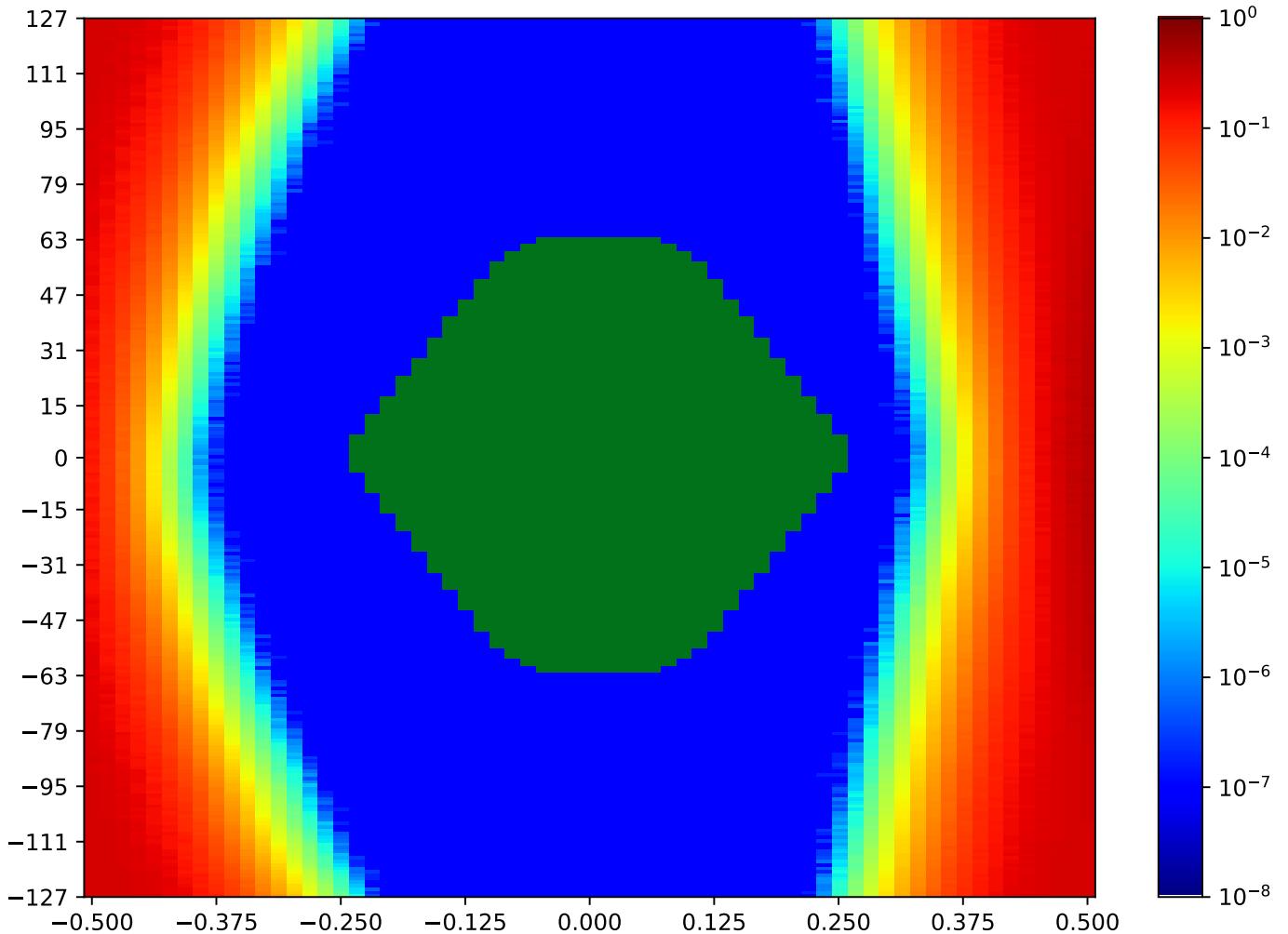


Figure 2.268: MSP_C_FPGA-TX3-01-RX4-01-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.3 MSP_C_FPGA-TX3-02-RX4-02-MSP_A_FPGA

Table 2.248: MSP_C_FPGA-TX3-02-RX4-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:49:25		2018-Jan-24 17:50:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9474	44	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

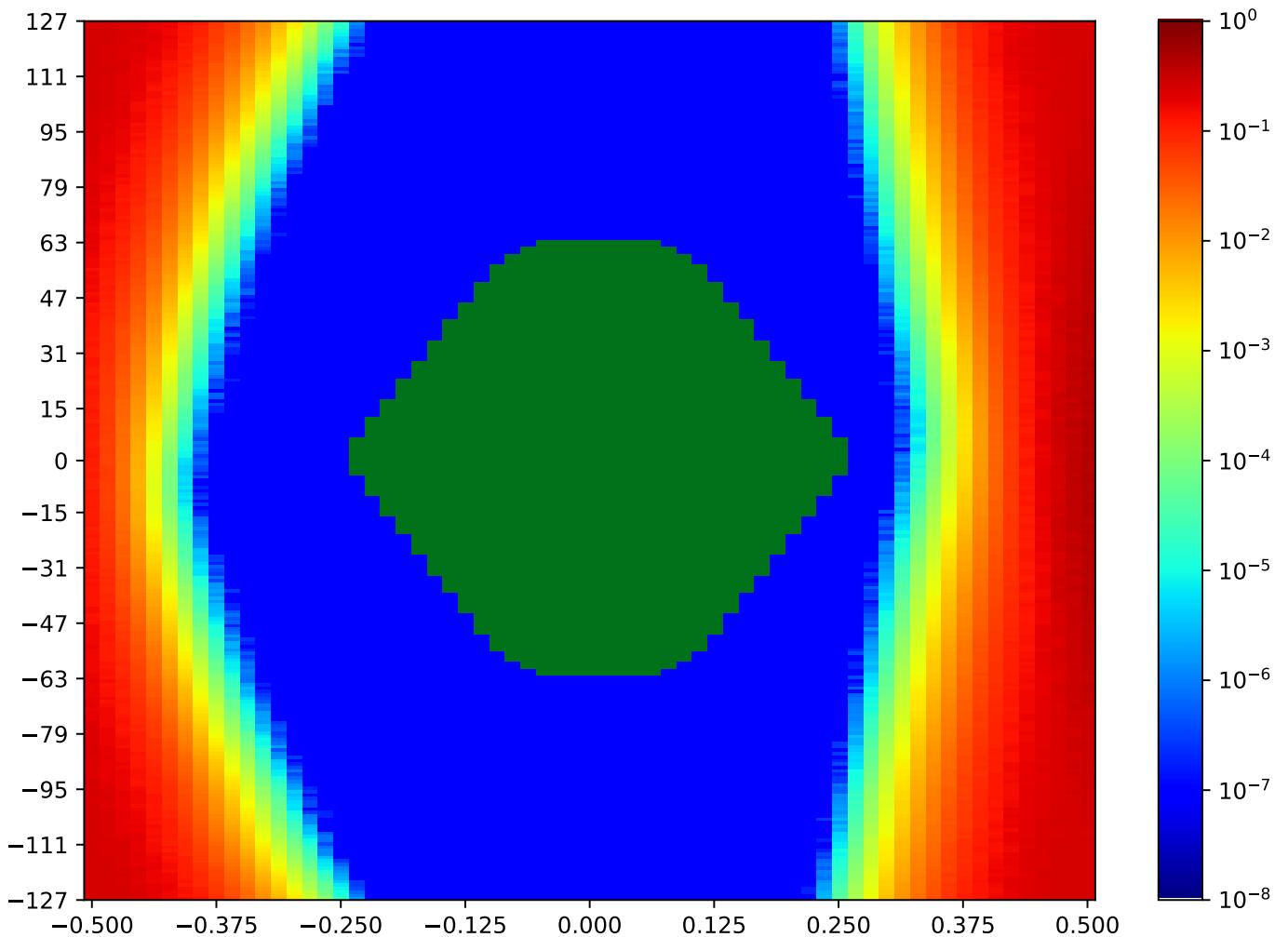


Figure 2.269: MSP_C_FPGA-TX3-02-RX4-02-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.4 MSP_C_FPGA-TX3-03-RX4-03-MSP_A_FPGA

Table 2.249: MSP_C_FPGA-TX3-03-RX4-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:46:26		2018-Jan-24 17:47:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9584	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

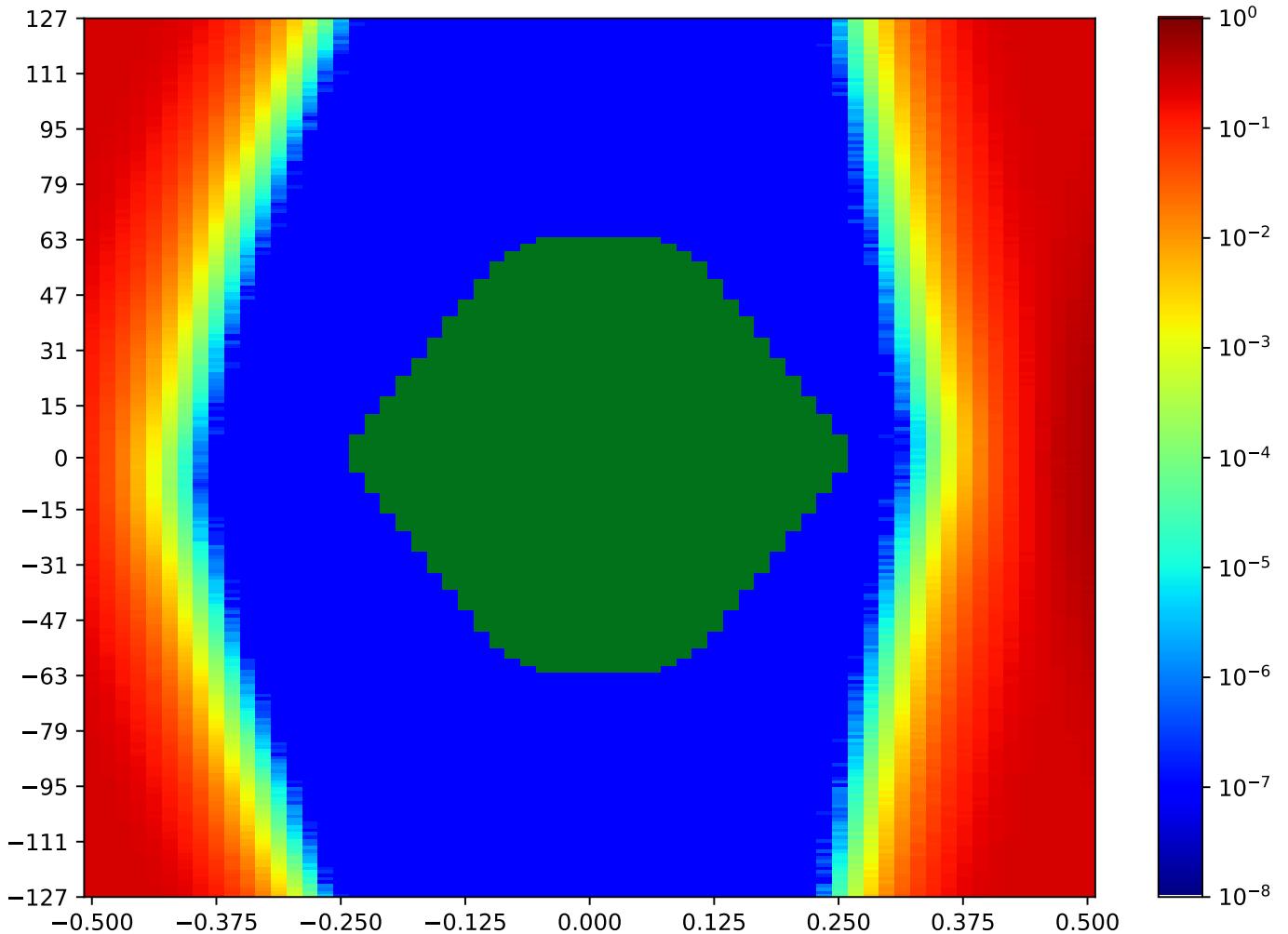


Figure 2.270: MSP_C_FPGA-TX3-03-RX4-03-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.5 MSP_C_FPGA-TX3-04-RX4-04-MSP_A_FPGA

Table 2.250: MSP_C_FPGA-TX3-04-RX4-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:51:13		2018-Jan-24 17:51:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10410	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

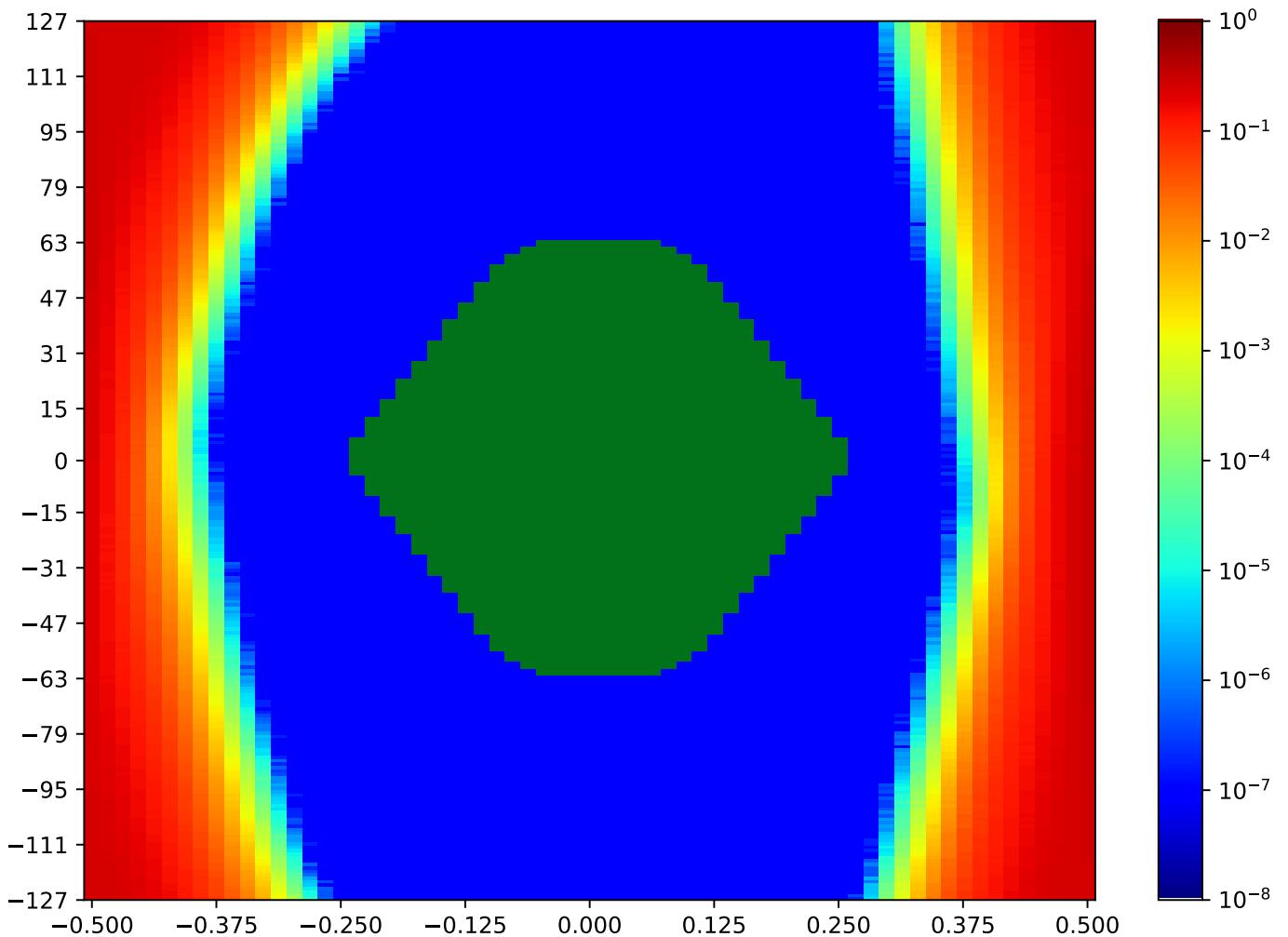


Figure 2.271: MSP_C_FPGA-TX3-04-RX4-04-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.6 MSP_C_FPGA-TX3-05-RX4-05-MSP_A_FPGA

Table 2.251: MSP_C_FPGA-TX3-05-RX4-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:45:50		2018-Jan-24 17:46:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9895	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

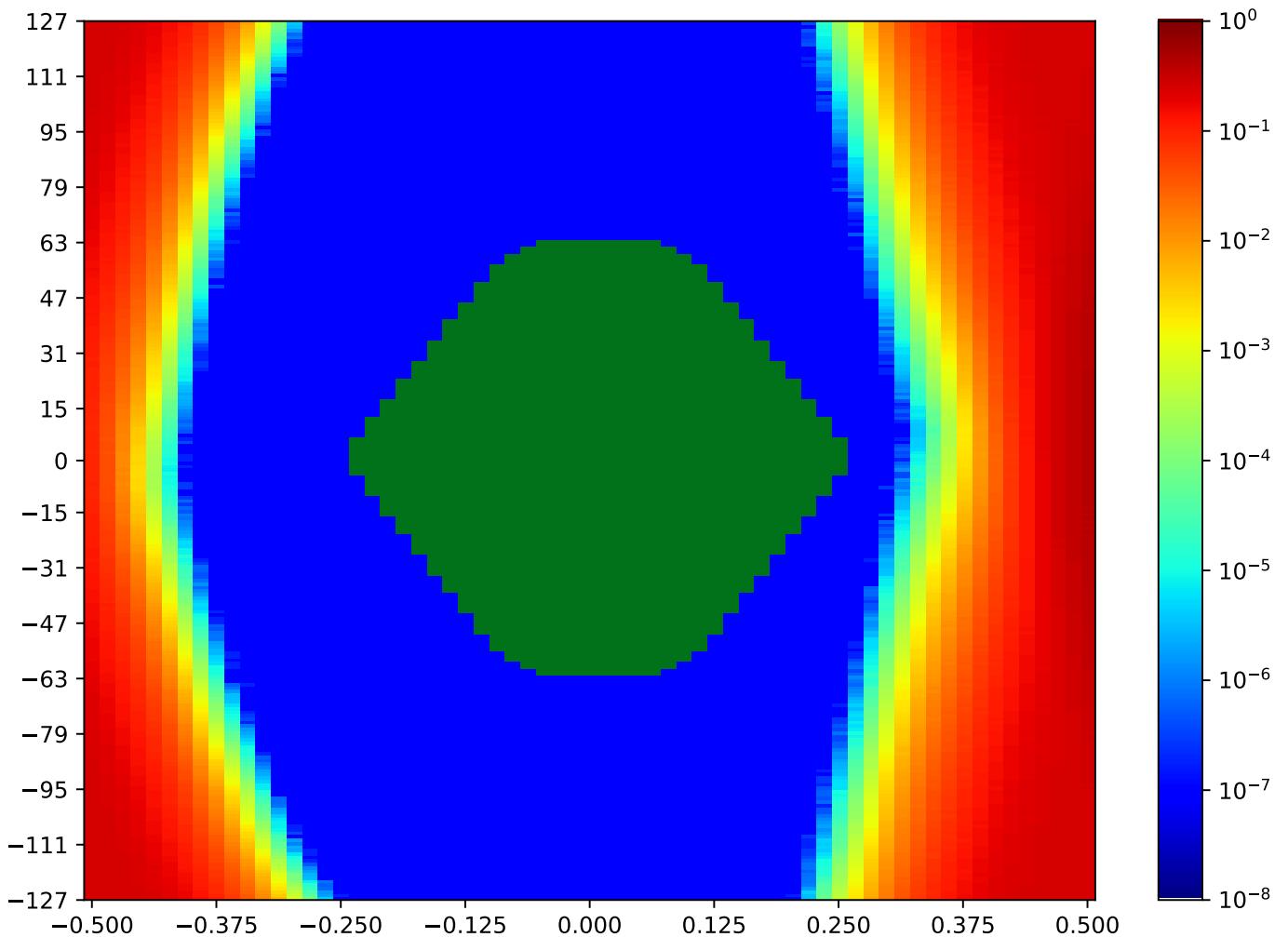


Figure 2.272: MSP_C_FPGA-TX3-05-RX4-05-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.7 MSP_C_FPGA-TX3-06-RX4-06-MSP_A_FPGA

Table 2.252: MSP_C_FPGA-TX3-06-RX4-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:52:24		2018-Jan-24 17:53:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10308	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

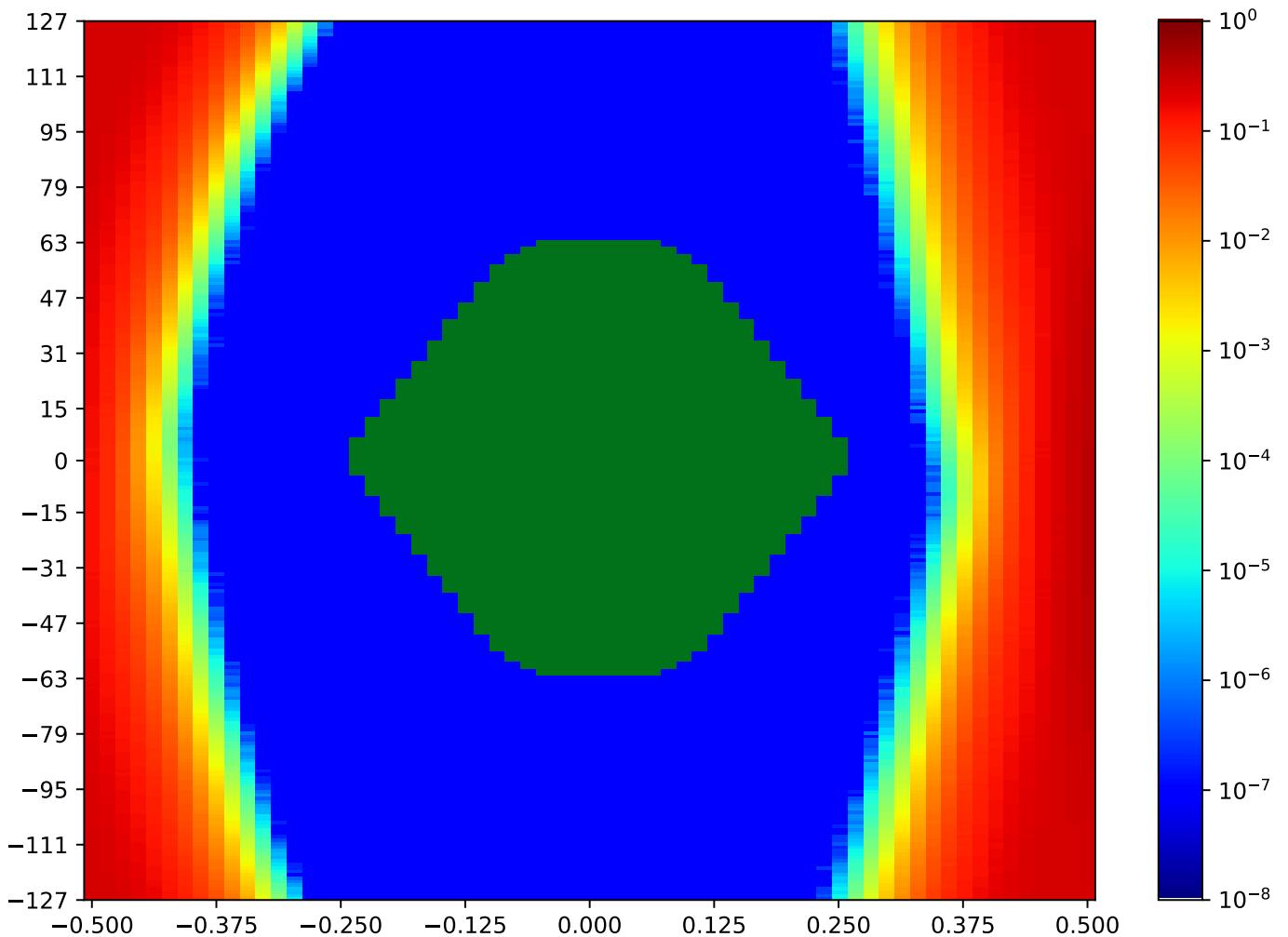


Figure 2.273: MSP_C_FPGA-TX3-06-RX4-06-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.8 MSP_C_FPGA-TX3-07-RX4-07-MSP_A_FPGA

Table 2.253: MSP_C_FPGA-TX3-07-RX4-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:47:02		2018-Jan-24 17:47:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10057	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

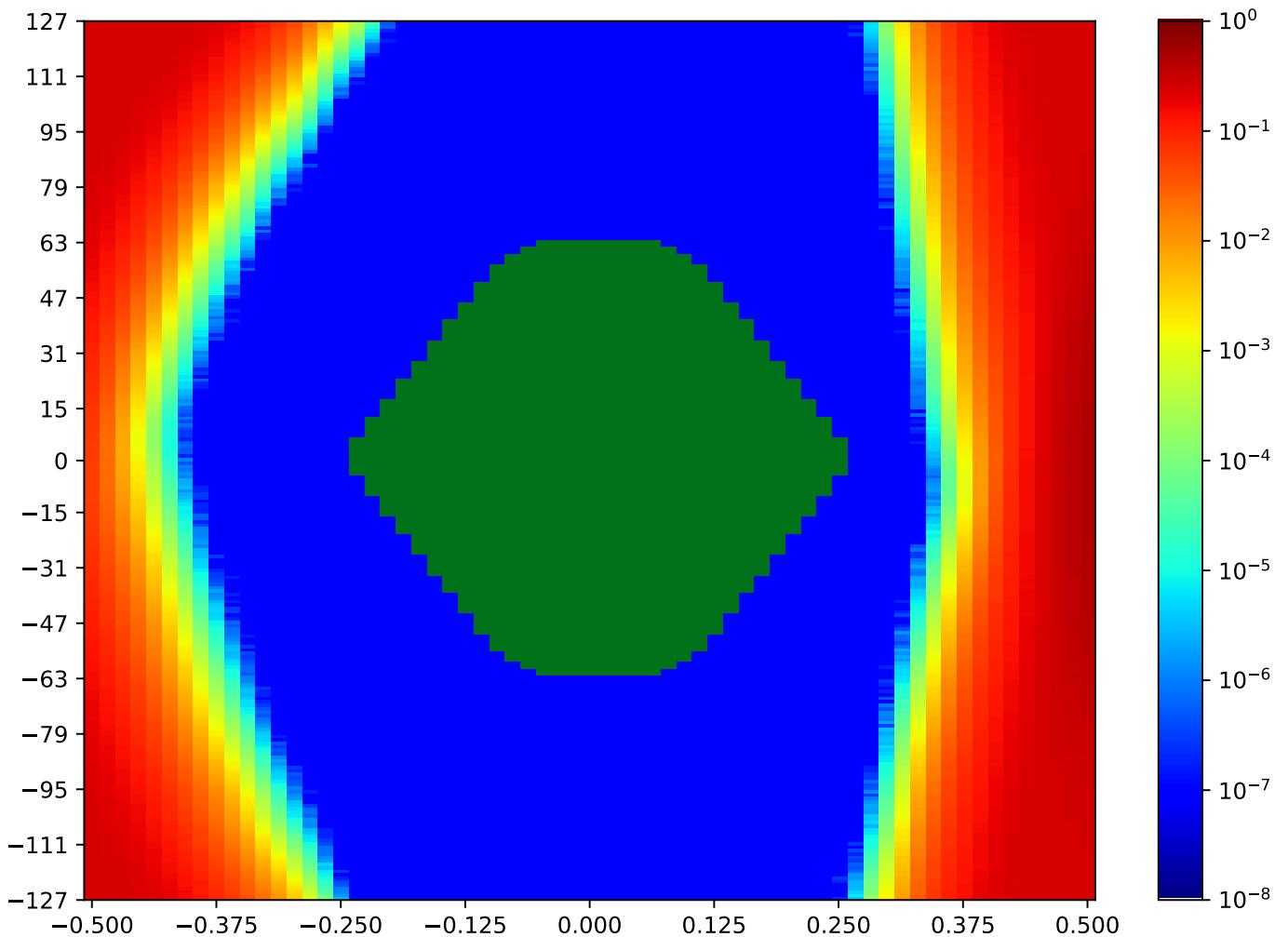


Figure 2.274: MSP_C_FPGA-TX3-07-RX4-07-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.9 MSP_C_FPGA-TX3-08-RX4-08-MSP_A_FPGA

Table 2.254: MSP_C_FPGA-TX3-08-RX4-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:51:49		2018-Jan-24 17:52:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9879	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

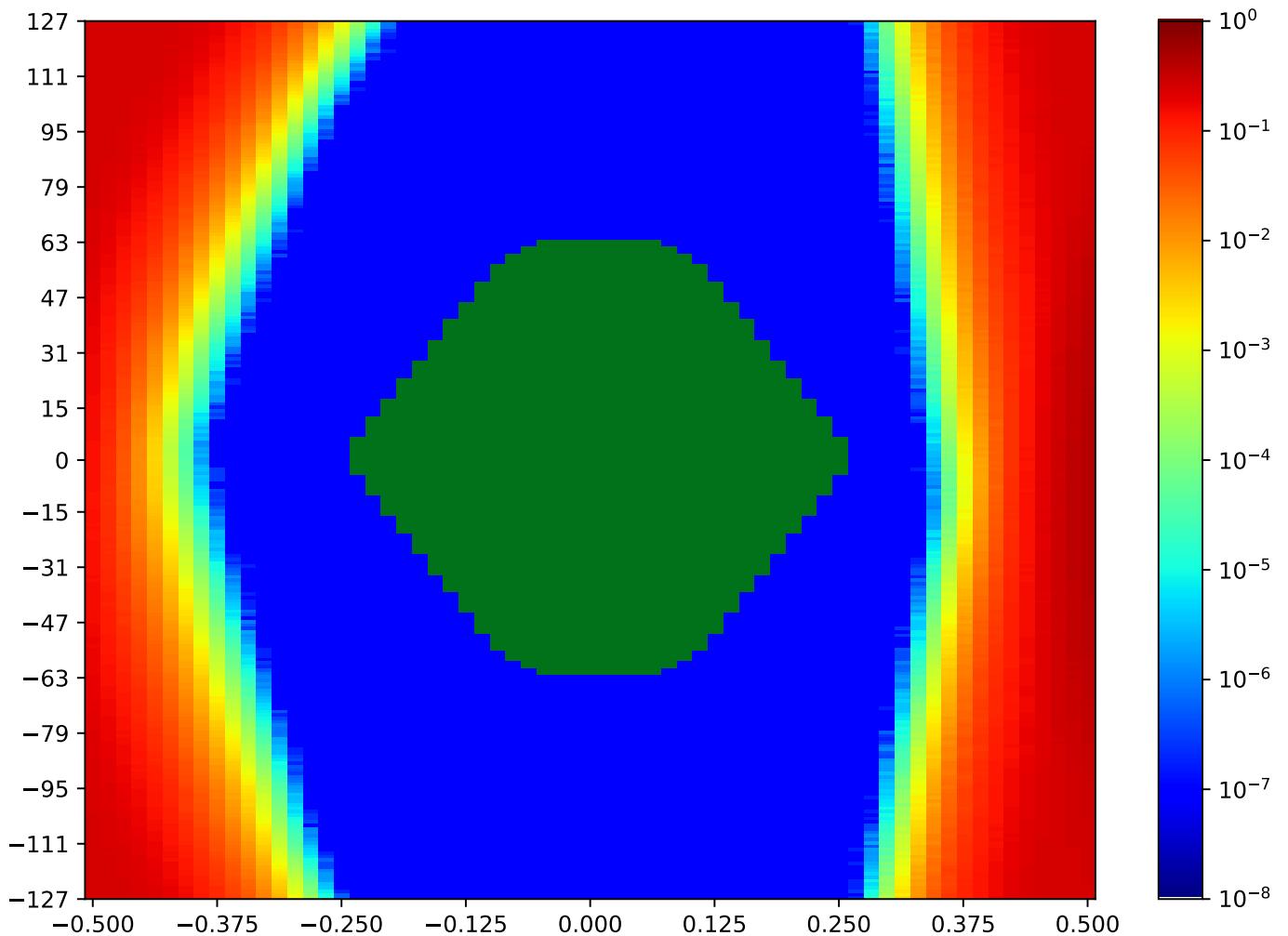


Figure 2.275: MSP_C_FPGA-TX3-08-RX4-08-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.10 MSP_C_FPGA-TX3-09-RX4-09-MSP_A_FPGA

Table 2.255: MSP_C_FPGA-TX3-09-RX4-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:48:13		2018-Jan-24 17:48:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9384	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

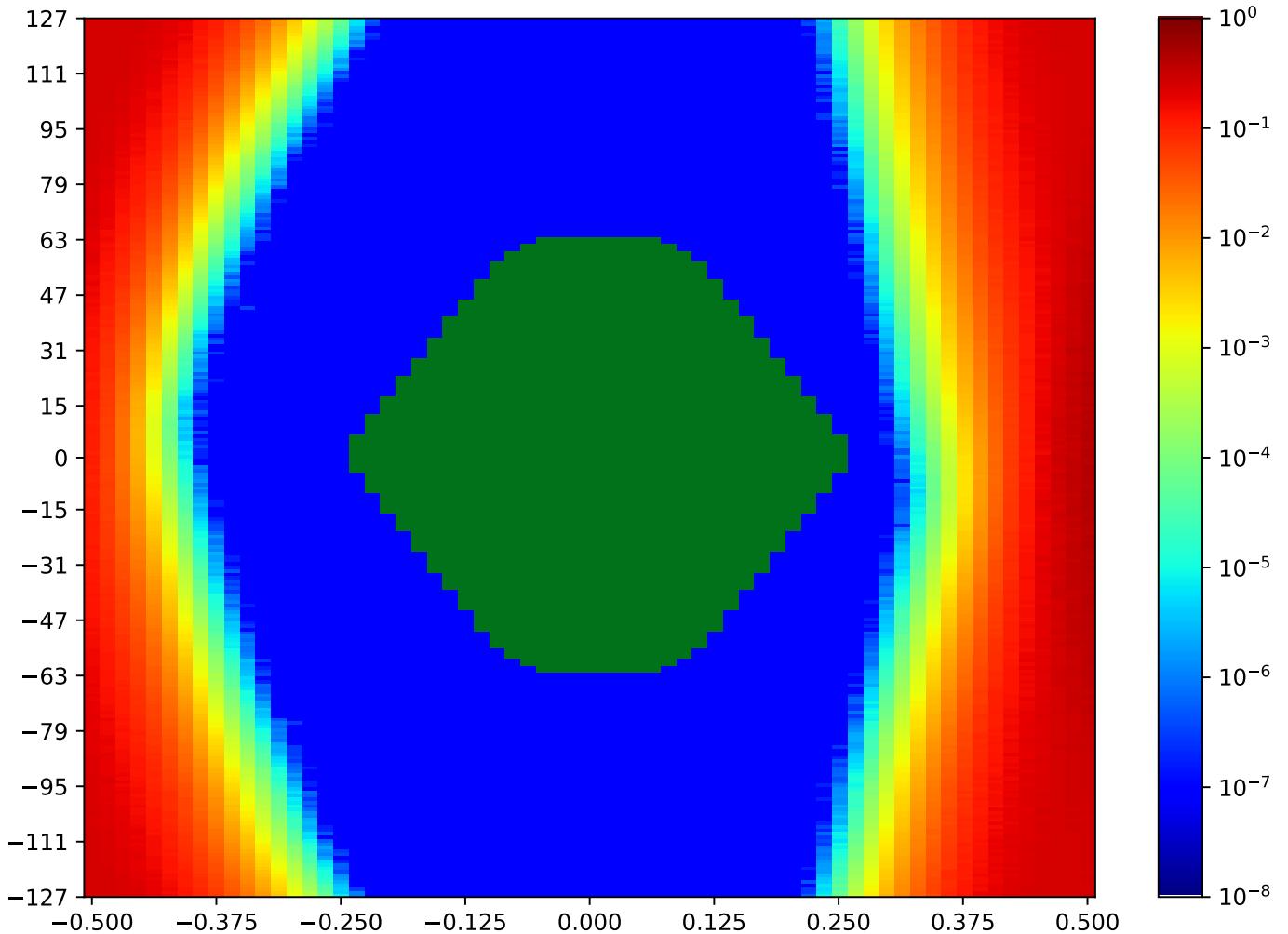


Figure 2.276: MSP_C_FPGA-TX3-09-RX4-09-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.11 MSP_C_FPGA-TX3-10-RX4-10-MSP_A_FPGA

Table 2.256: MSP_C_FPGA-TX3-10-RX4-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:50:37		2018-Jan-24 17:51:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10617	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

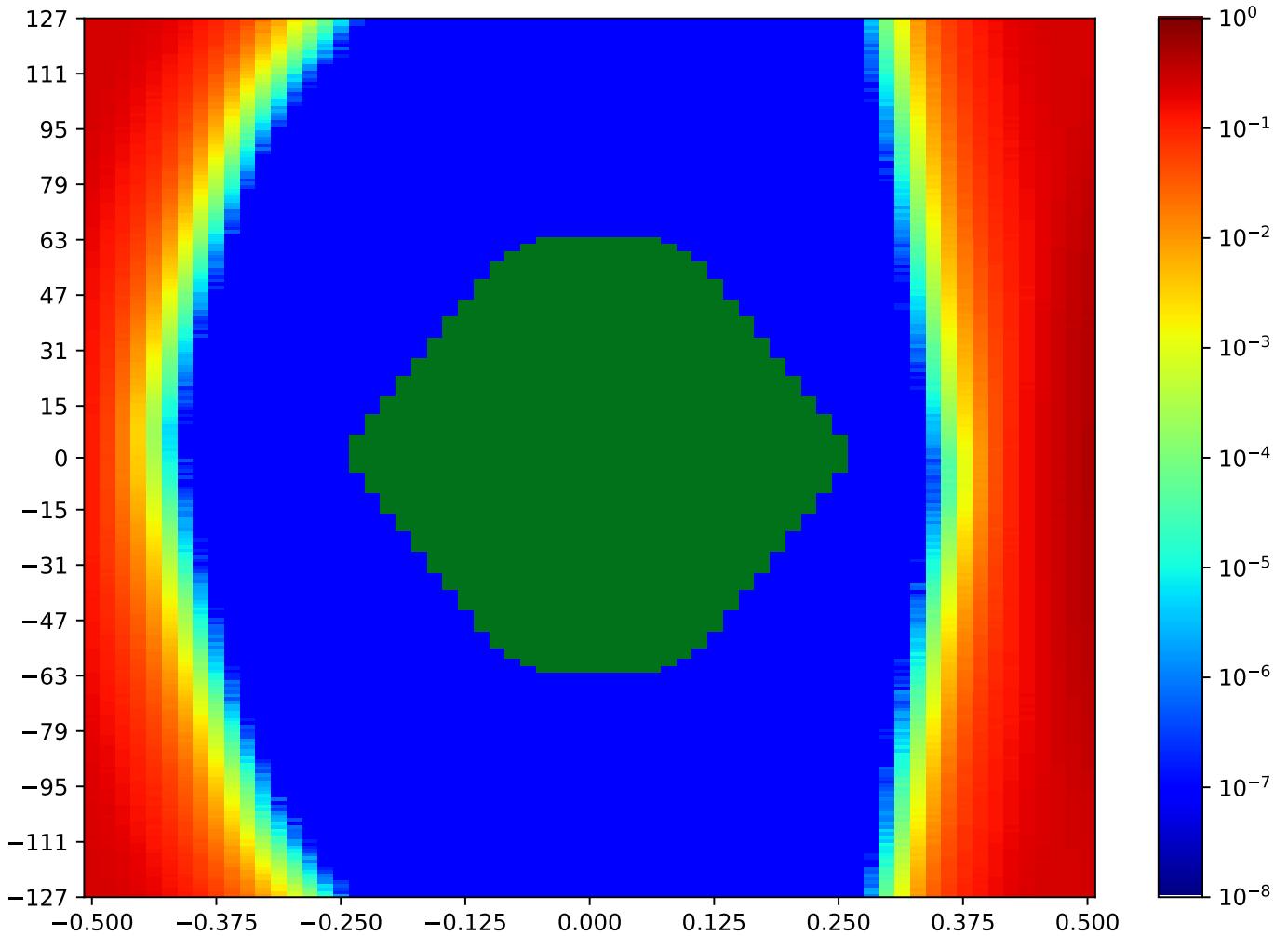


Figure 2.277: MSP_C_FPGA-TX3-10-RX4-10-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.21.12 MSP_C_FPGA-TX3-11-RX4-11-MSP_A_FPGA

Table 2.257: MSP_C_FPGA-TX3-11-RX4-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:50:01		2018-Jan-24 17:50:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9338	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

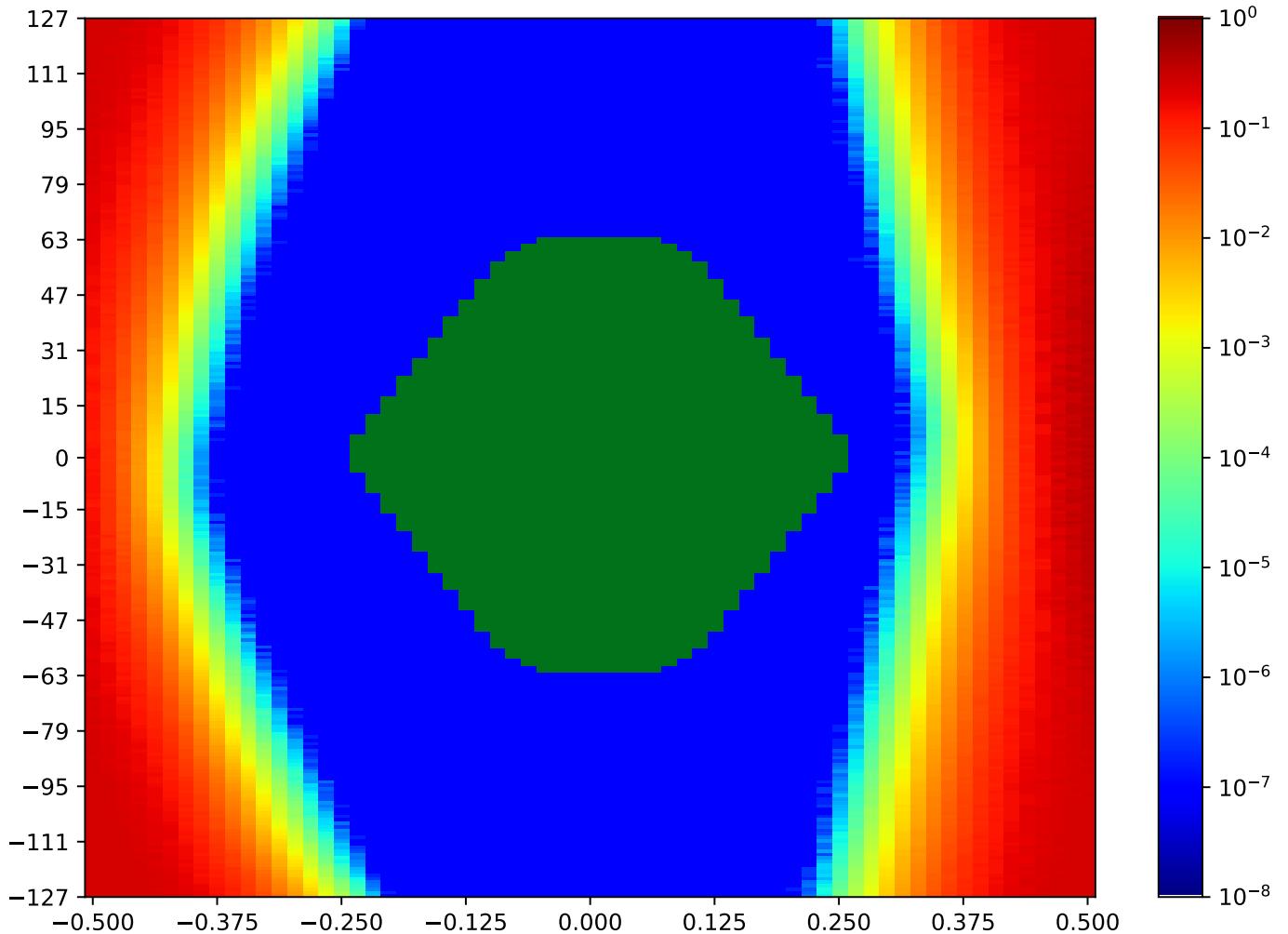


Figure 2.278: MSP_C_FPGA-TX3-11-RX4-11-MSP_A_FPGA

Call back to summary Figure 2.266. Sibling eye diagrams: V1-12.8.

2.22 MSP_C TX4 MSP_A RX3 Minipod Loopback

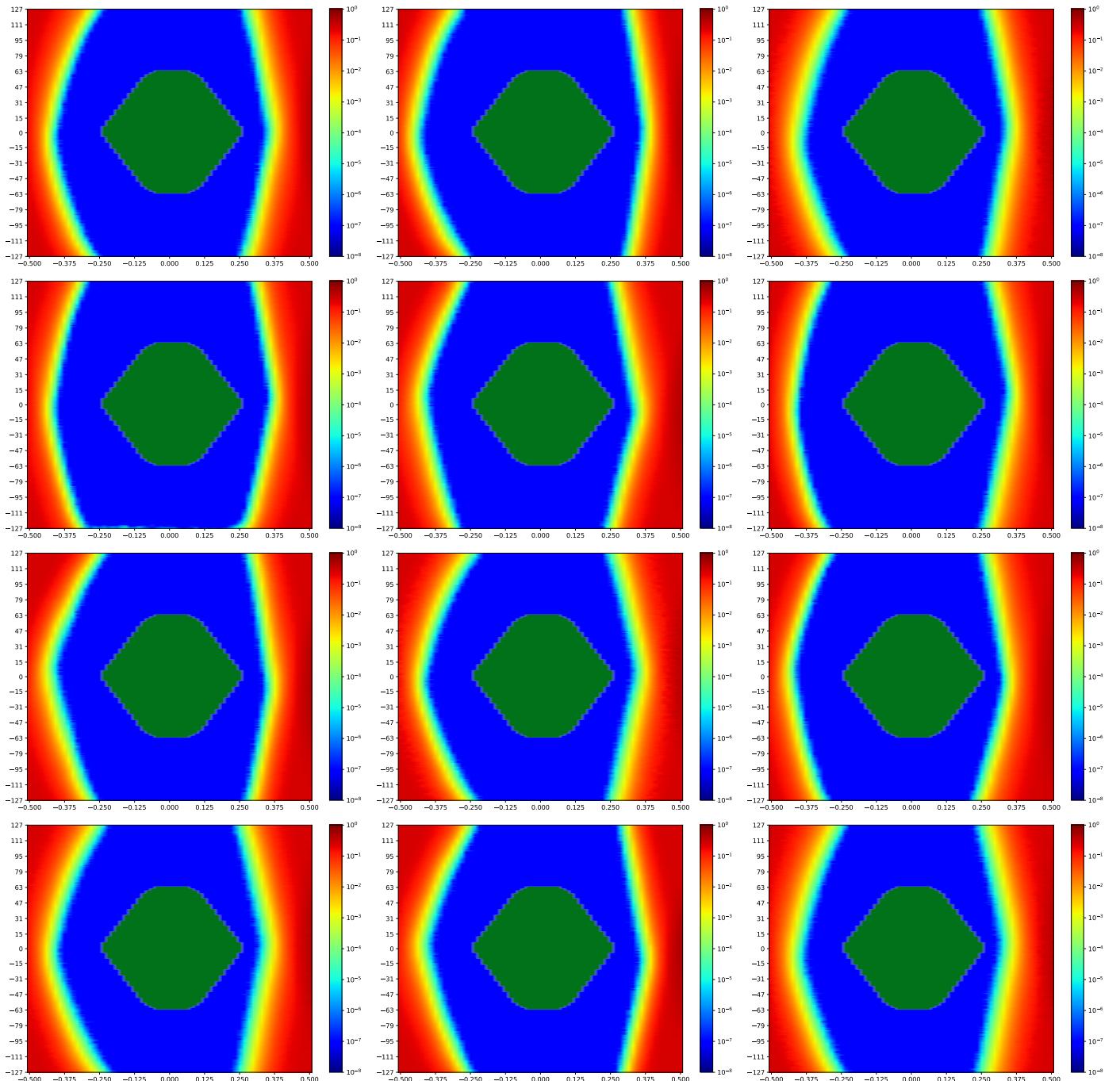


Figure 2.279: MSP_C TX4 MSP_A RX3 Minipod Loopback

A cross-reference to Figure 2.279. Sibling eye diagrams: V1-12.8.

Next summary Figure 3.1.

2.22.1 MSP_C_FPGA-TX4-00-RX3-00-MSP_A_FPGA

Table 2.258: MSP_C_FPGA-TX4-00-RX3-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:54:49		2018-Jan-24 17:55:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10077	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

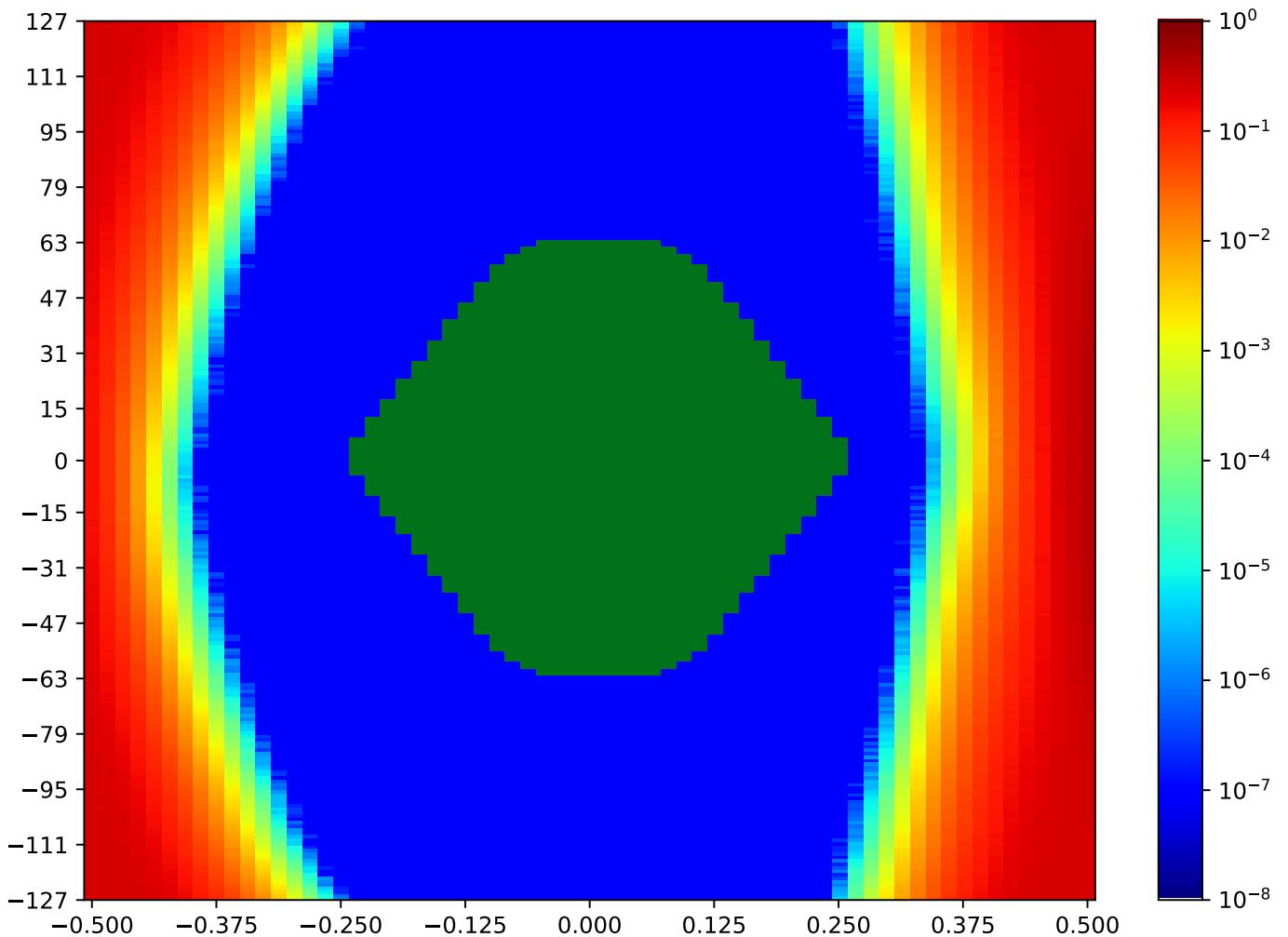


Figure 2.280: MSP_C_FPGA-TX4-00-RX3-00-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.2 MSP_C_FPGA-TX4-01-RX3-01-MSP_A_FPGA

Table 2.259: MSP_C_FPGA-TX4-01-RX3-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:53:37		2018-Jan-24 17:54:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10755	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

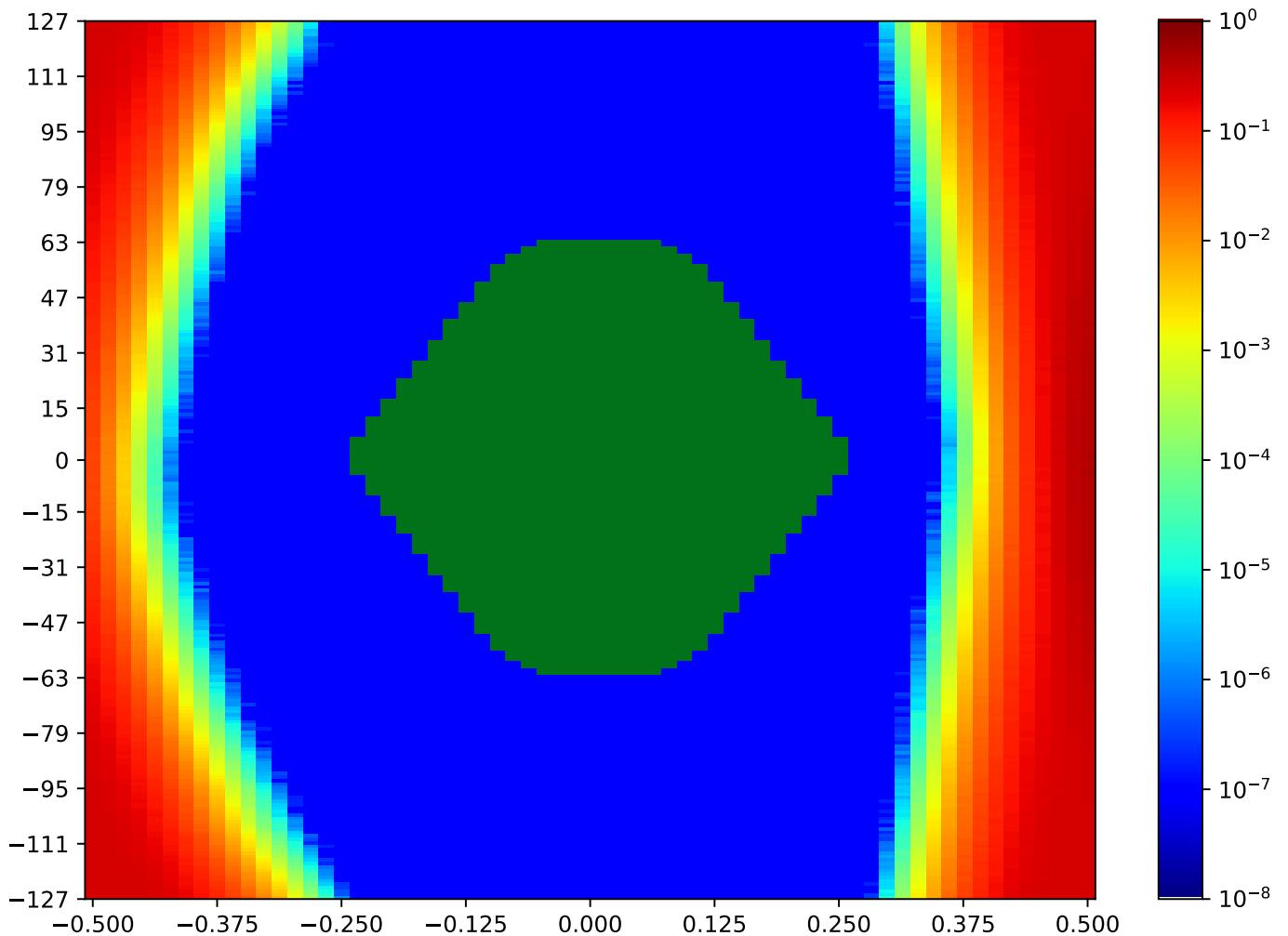


Figure 2.281: MSP_C_FPGA-TX4-01-RX3-01-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.3 MSP_C_FPGA-TX4-02-RX3-02-MSP_A_FPGA

Table 2.260: MSP_C_FPGA-TX4-02-RX3-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:56:39		2018-Jan-24 17:57:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9436	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

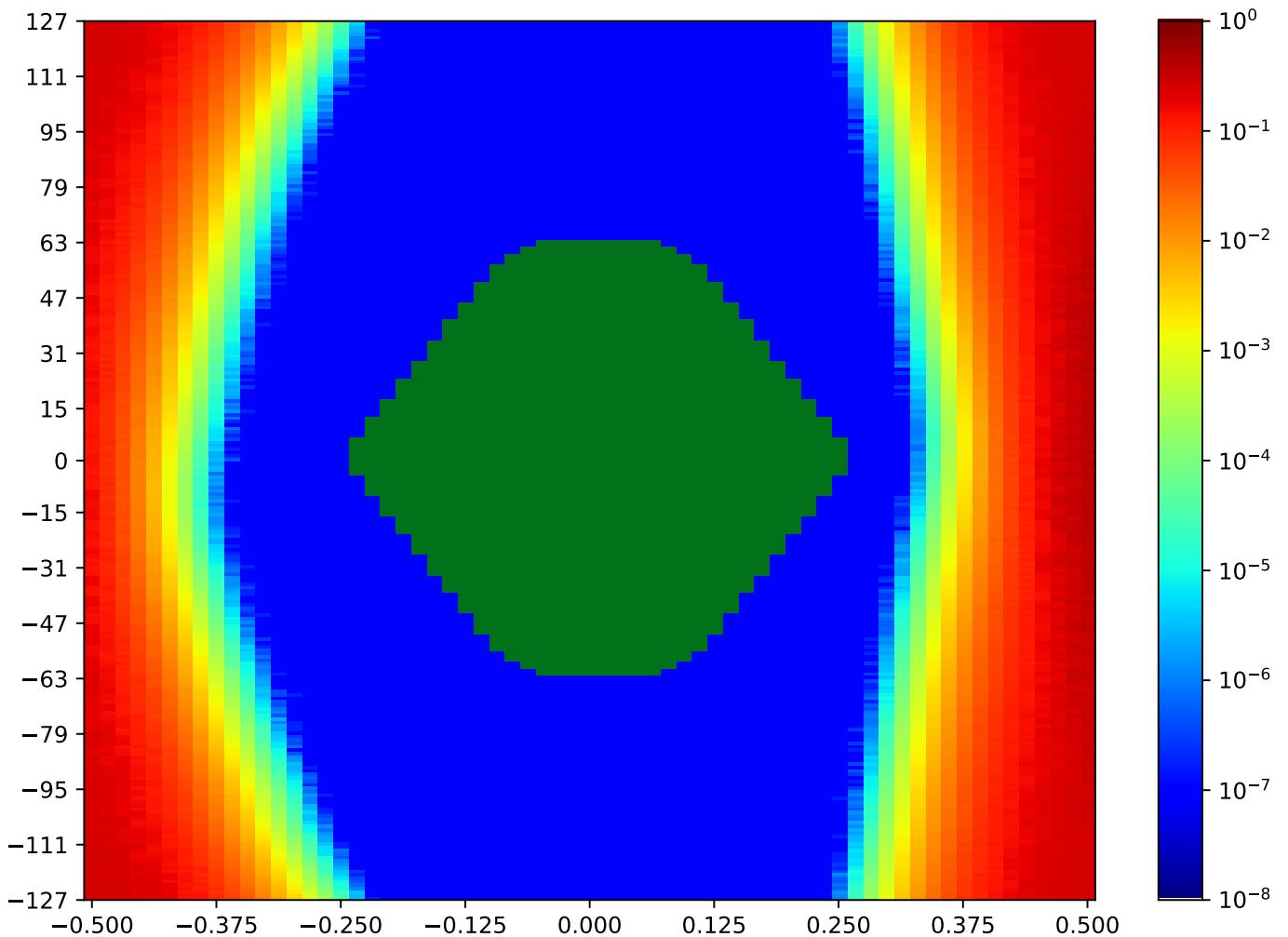


Figure 2.282: MSP_C_FPGA-TX4-02-RX3-02-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.4 MSP_C_FPGA-TX4-03-RX3-03-MSP_A_FPGA

Table 2.261: MSP_C_FPGA-TX4-03-RX3-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:53:00		2018-Jan-24 17:53:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10510	47	72.31%	253	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

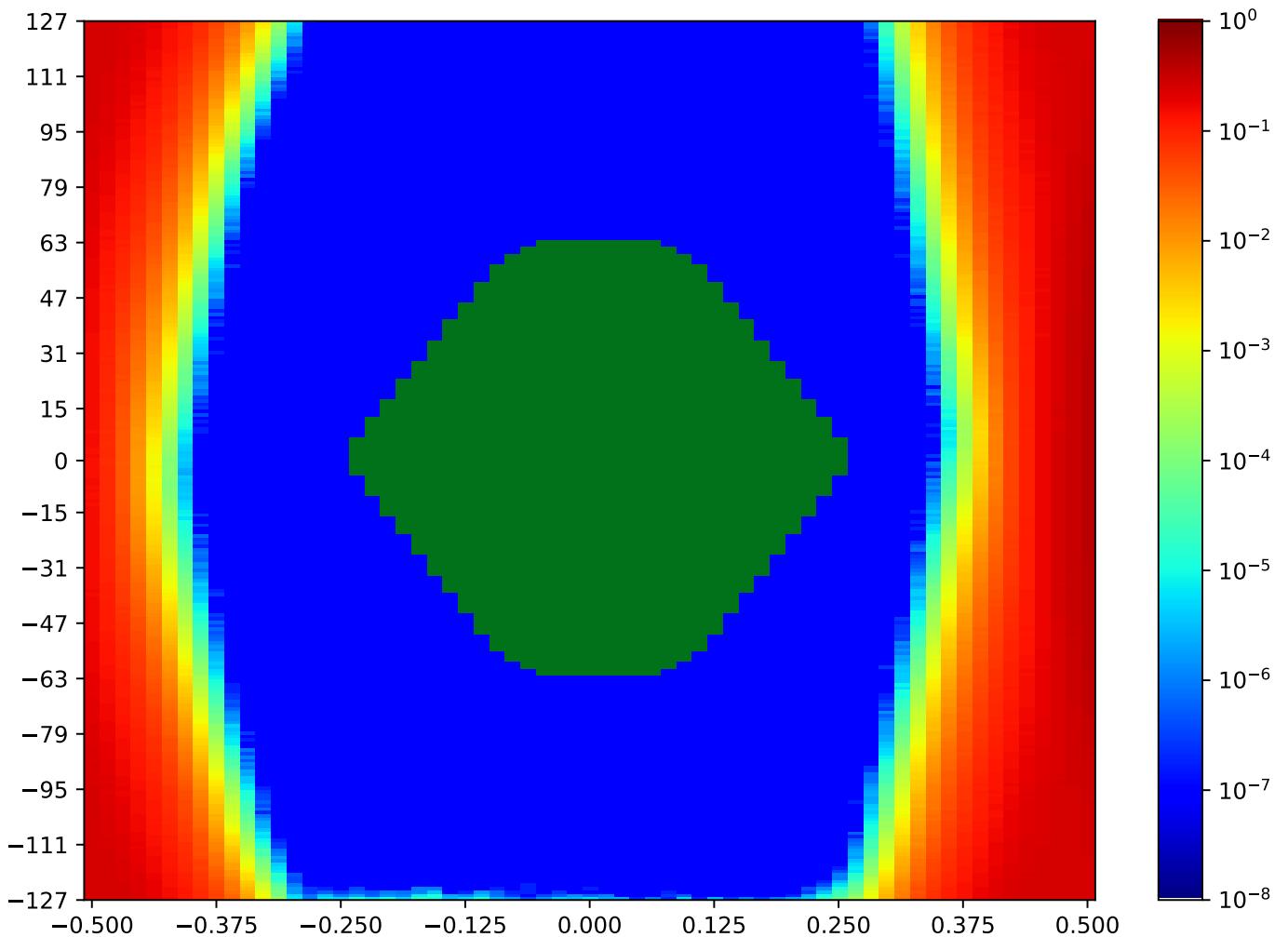


Figure 2.283: MSP_C_FPGA-TX4-03-RX3-03-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.5 MSP_C_FPGA-TX4-04-RX3-04-MSP_A_FPGA

Table 2.262: MSP_C_FPGA-TX4-04-RX3-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:58:28		2018-Jan-24 17:59:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9723	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

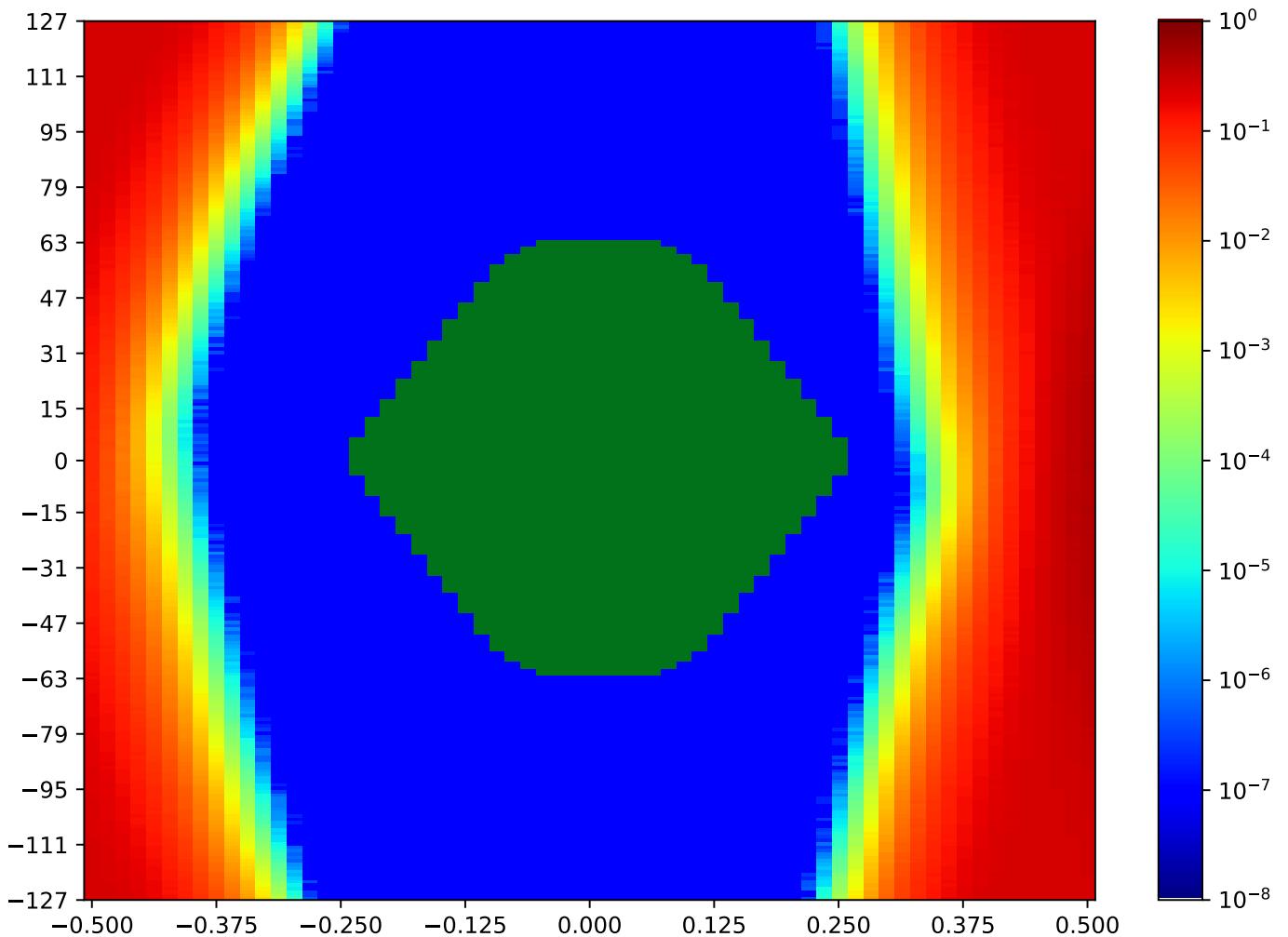


Figure 2.284: MSP_C_FPGA-TX4-04-RX3-04-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.6 MSP_C_FPGA-TX4-05-RX3-05-MSP_A_FPGA

Table 2.263: MSP_C_FPGA-TX4-05-RX3-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:54:13		2018-Jan-24 17:54:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10308	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

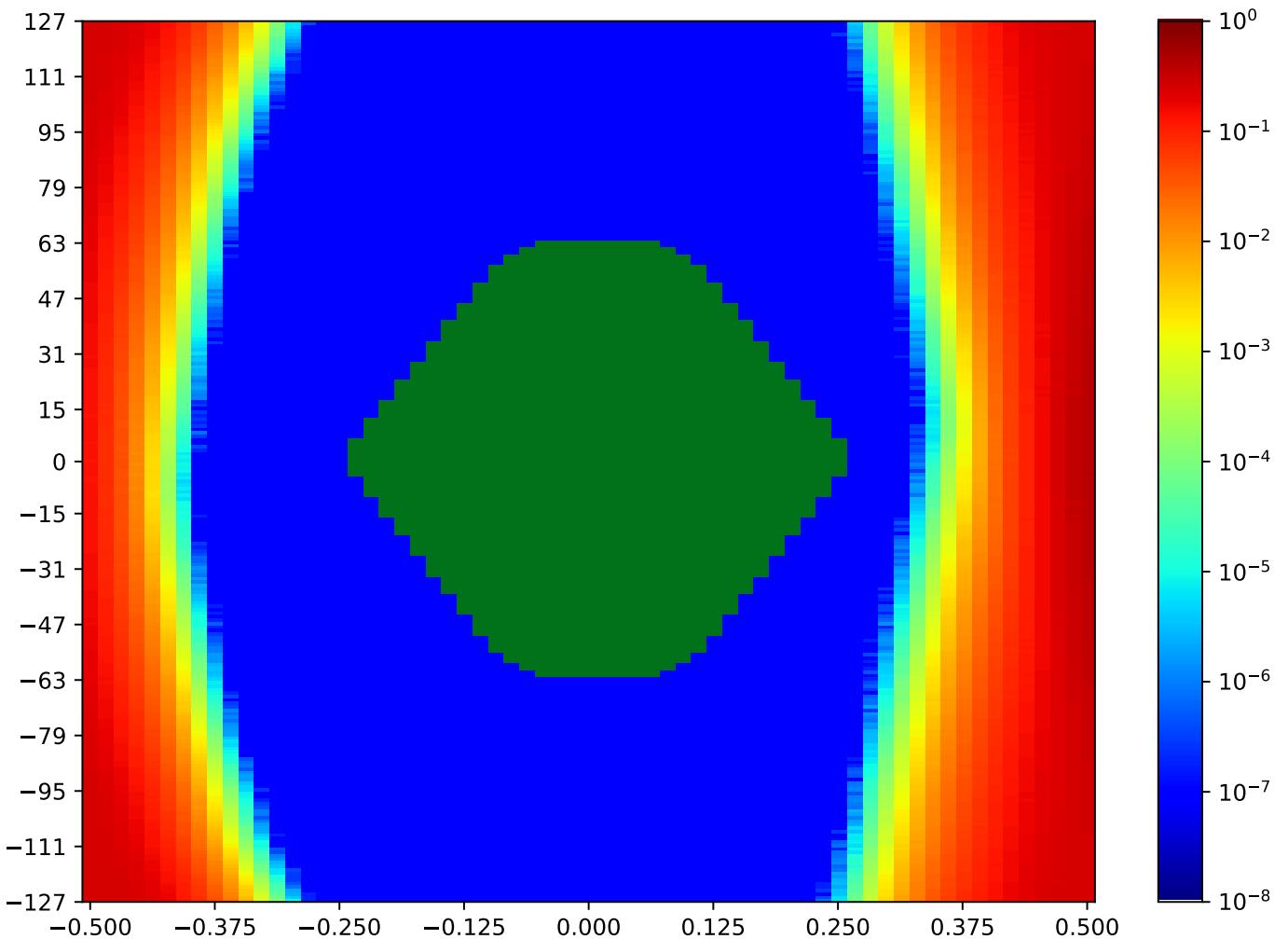


Figure 2.285: MSP_C_FPGA-TX4-05-RX3-05-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.7 MSP_C_FPGA-TX4-06-RX3-06-MSP_A_FPGA

Table 2.264: MSP_C_FPGA-TX4-06-RX3-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:59:37		2018-Jan-24 18:00:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9958	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

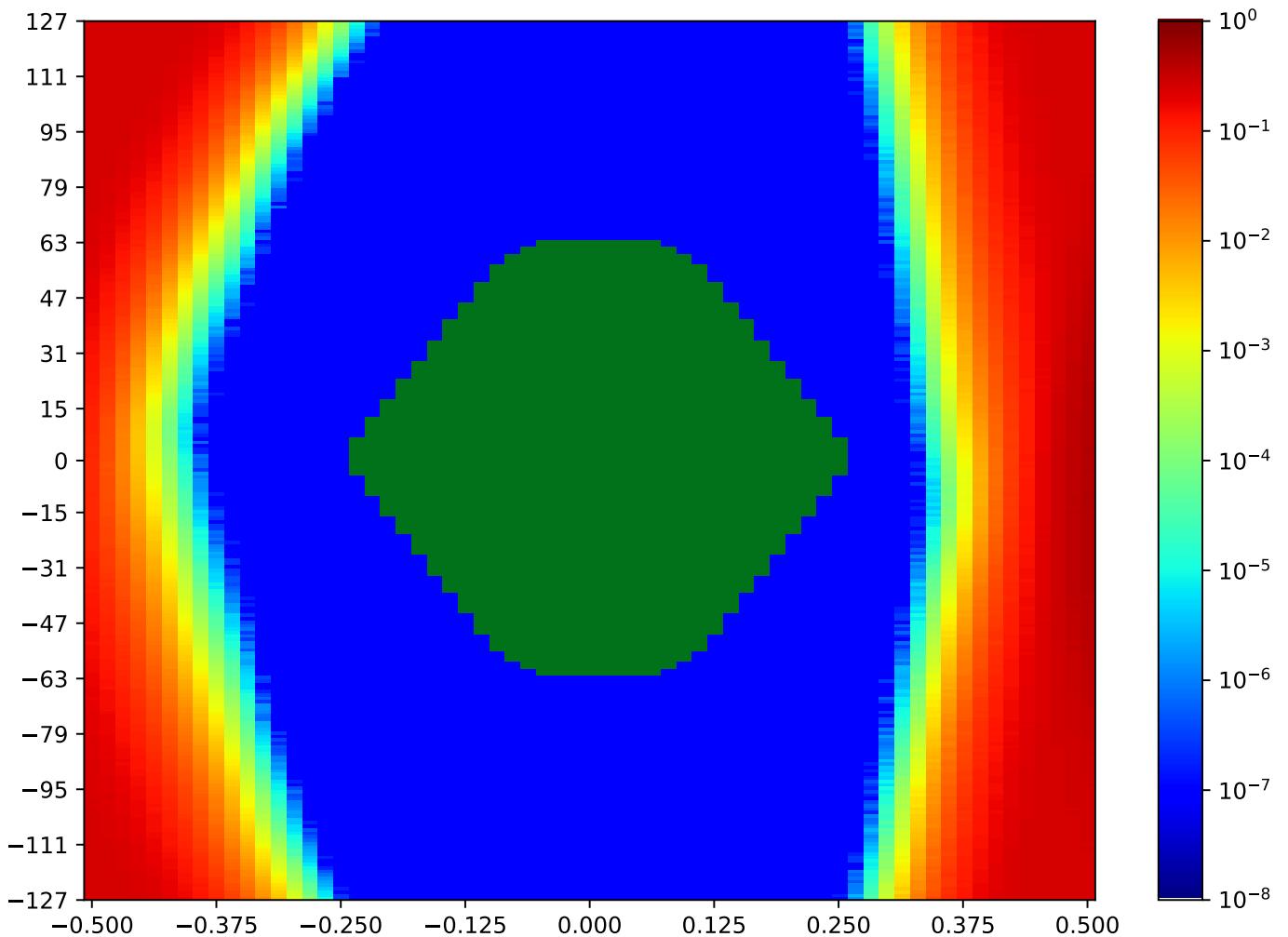


Figure 2.286: MSP_C_FPGA-TX4-06-RX3-06-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.8 MSP_C_FPGA-TX4-07-RX3-07-MSP_A_FPGA

Table 2.265: MSP_C_FPGA-TX4-07-RX3-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:55:26		2018-Jan-24 17:56:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9504	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

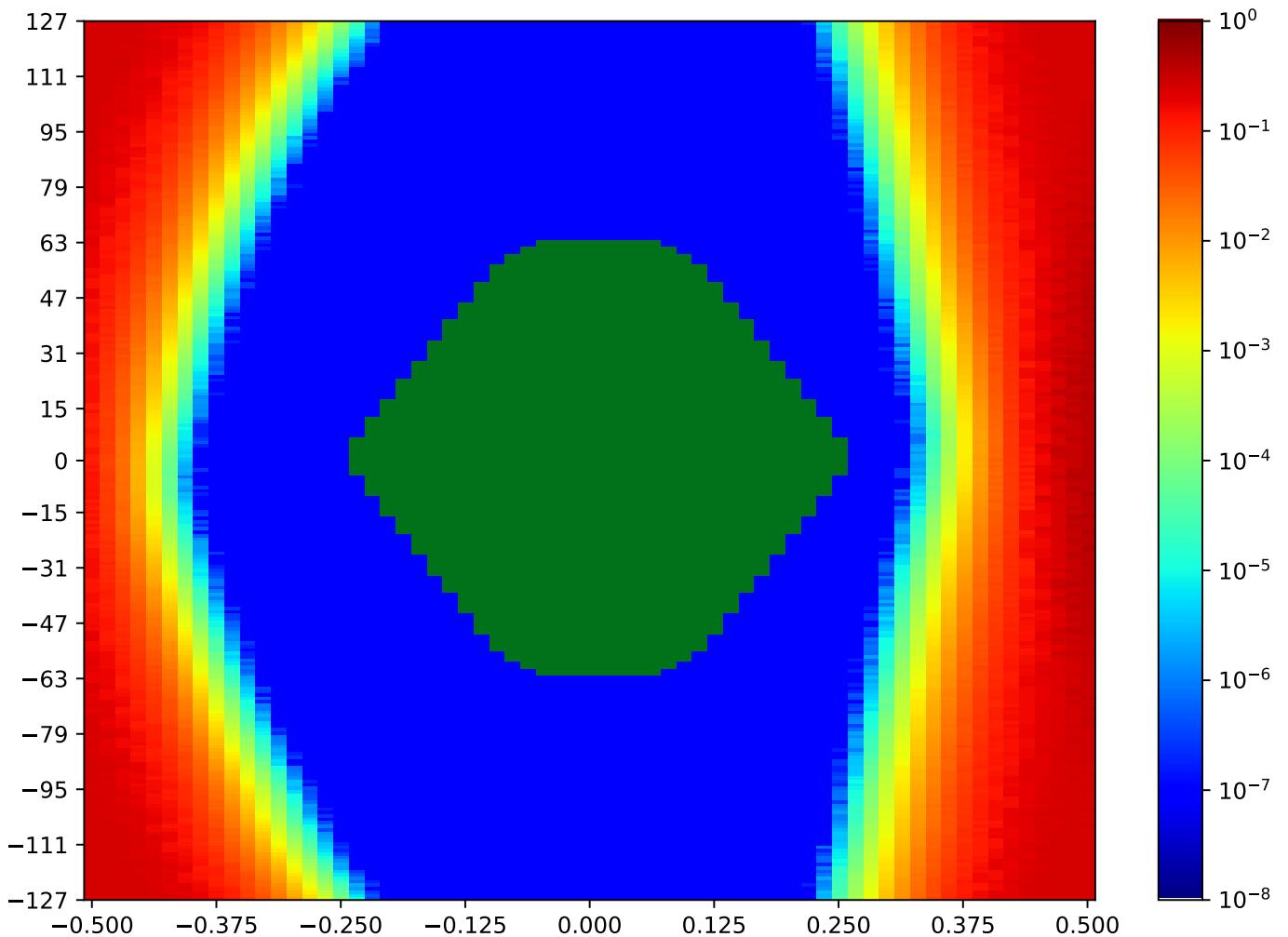


Figure 2.287: MSP_C_FPGA-TX4-07-RX3-07-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.9 MSP_C_FPGA-TX4-08-RX3-08-MSP_A_FPGA

Table 2.266: MSP_C_FPGA-TX4-08-RX3-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:59:02		2018-Jan-24 17:59:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9976	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

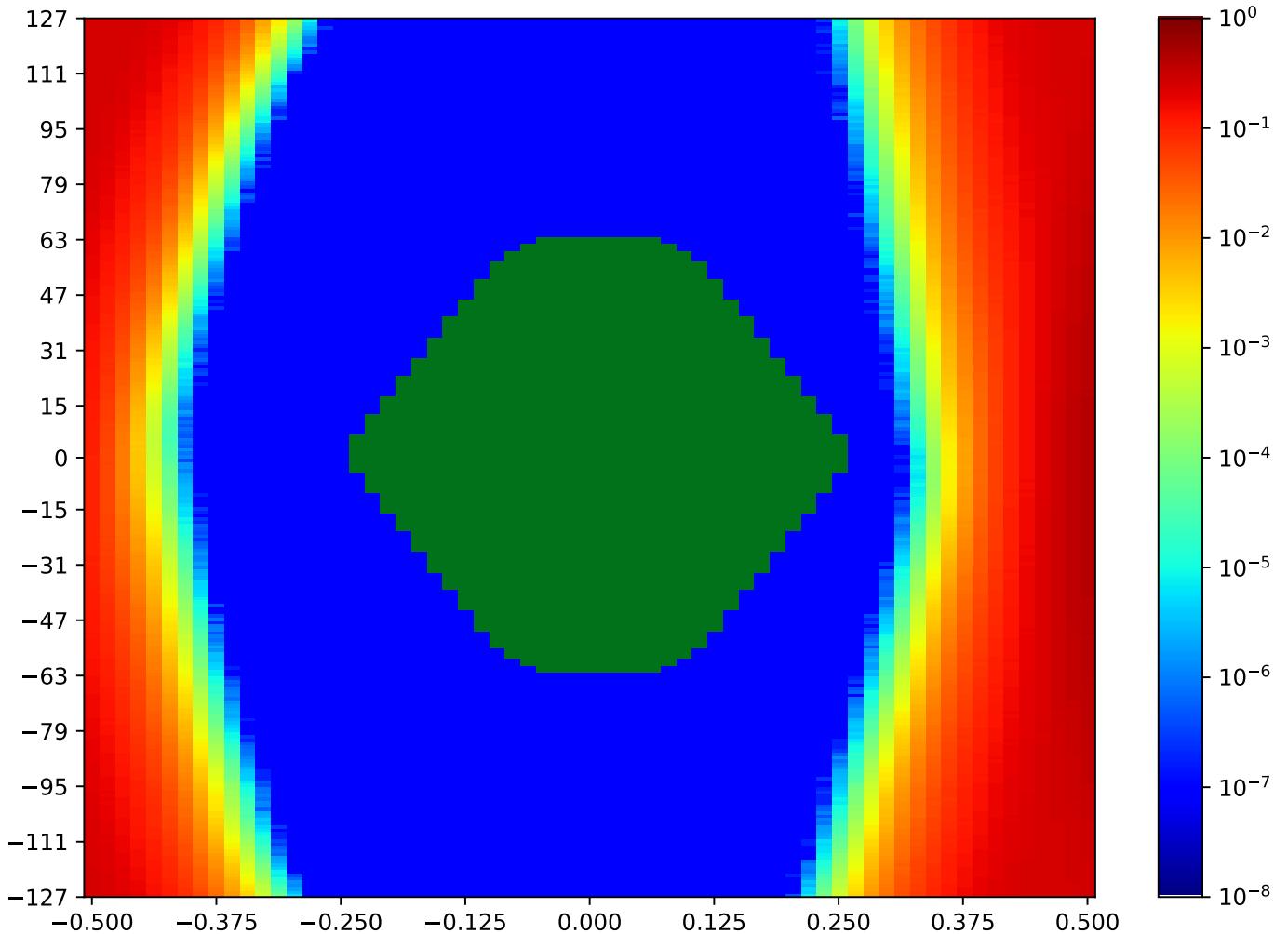


Figure 2.288: MSP_C_FPGA-TX4-08-RX3-08-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.10 MSP_C_FPGA-TX4-09-RX3-09-MSP_A_FPGA

Table 2.267: MSP_C_FPGA-TX4-09-RX3-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:56:03		2018-Jan-24 17:56:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9280	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

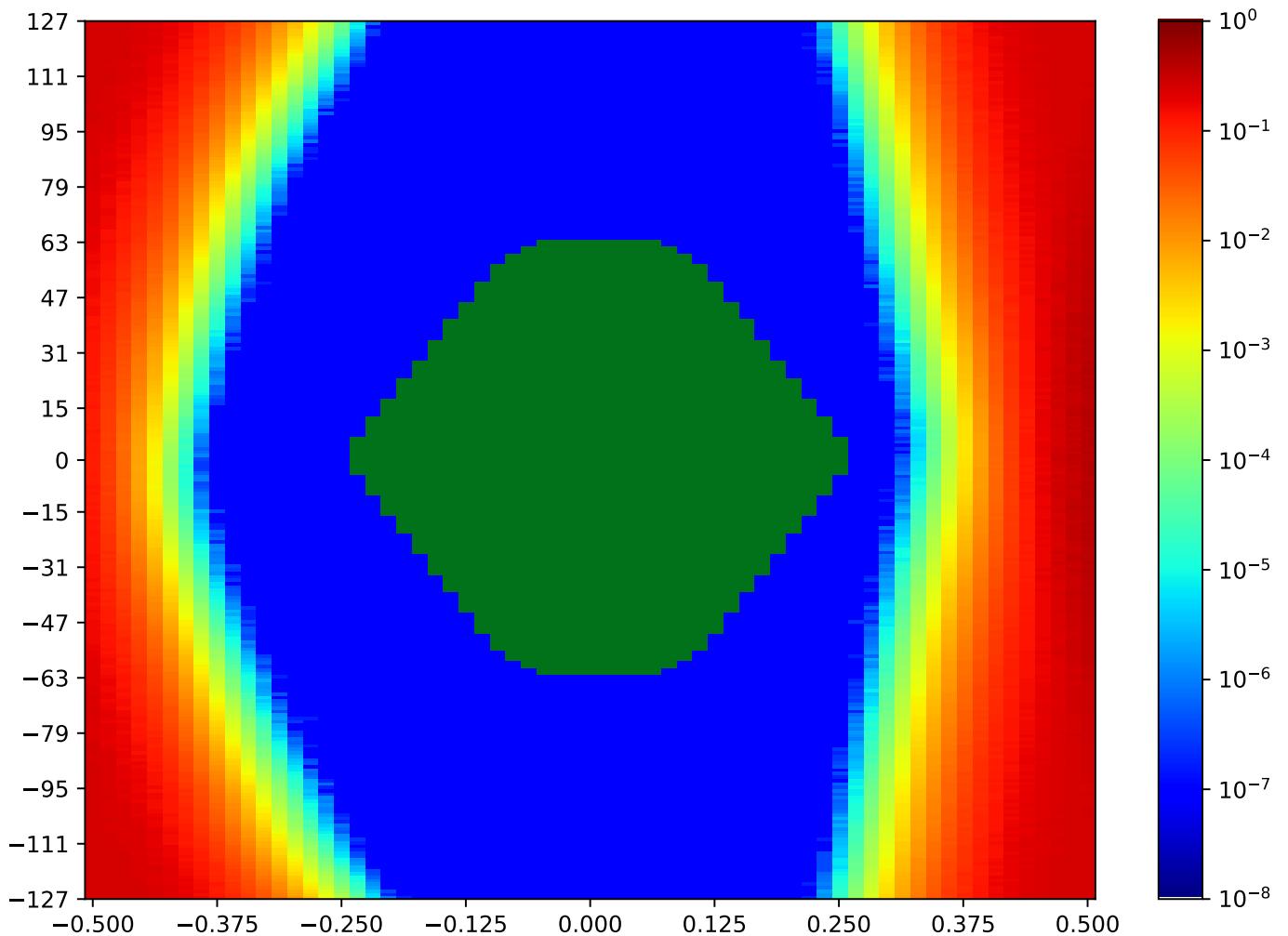


Figure 2.289: MSP_C_FPGA-TX4-09-RX3-09-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.11 MSP_C_FPGA-TX4-10-RX3-10-MSP_A_FPGA

Table 2.268: MSP_C_FPGA-TX4-10-RX3-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:57:51		2018-Jan-24 17:58:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9915	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

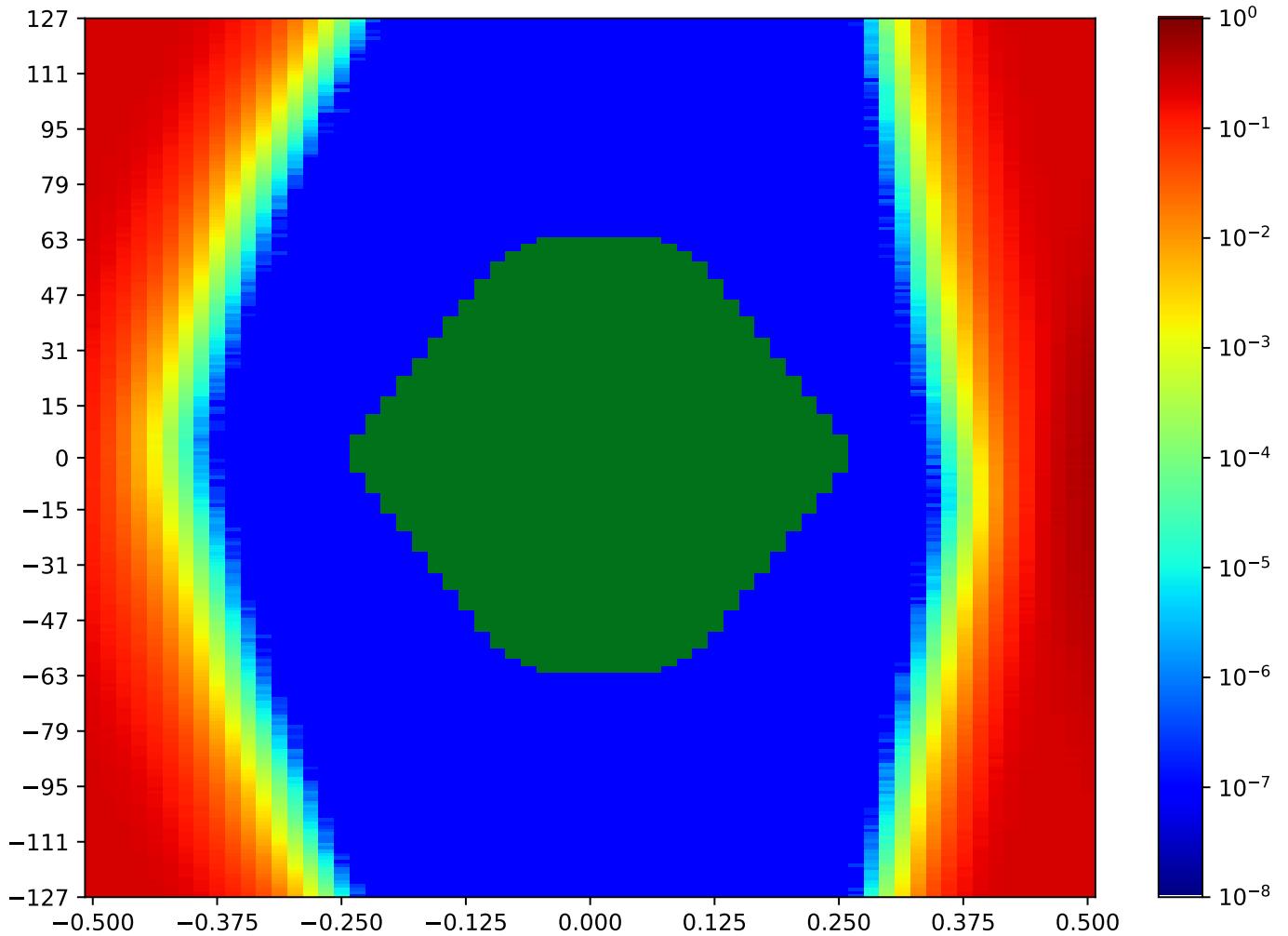


Figure 2.290: MSP_C_FPGA-TX4-10-RX3-10-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

2.22.12 MSP_C_FPGA-TX4-11-RX3-11-MSP_A_FPGA

Table 2.269: MSP_C_FPGA-TX4-11-RX3-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 17:57:15		2018-Jan-24 17:57:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9166	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

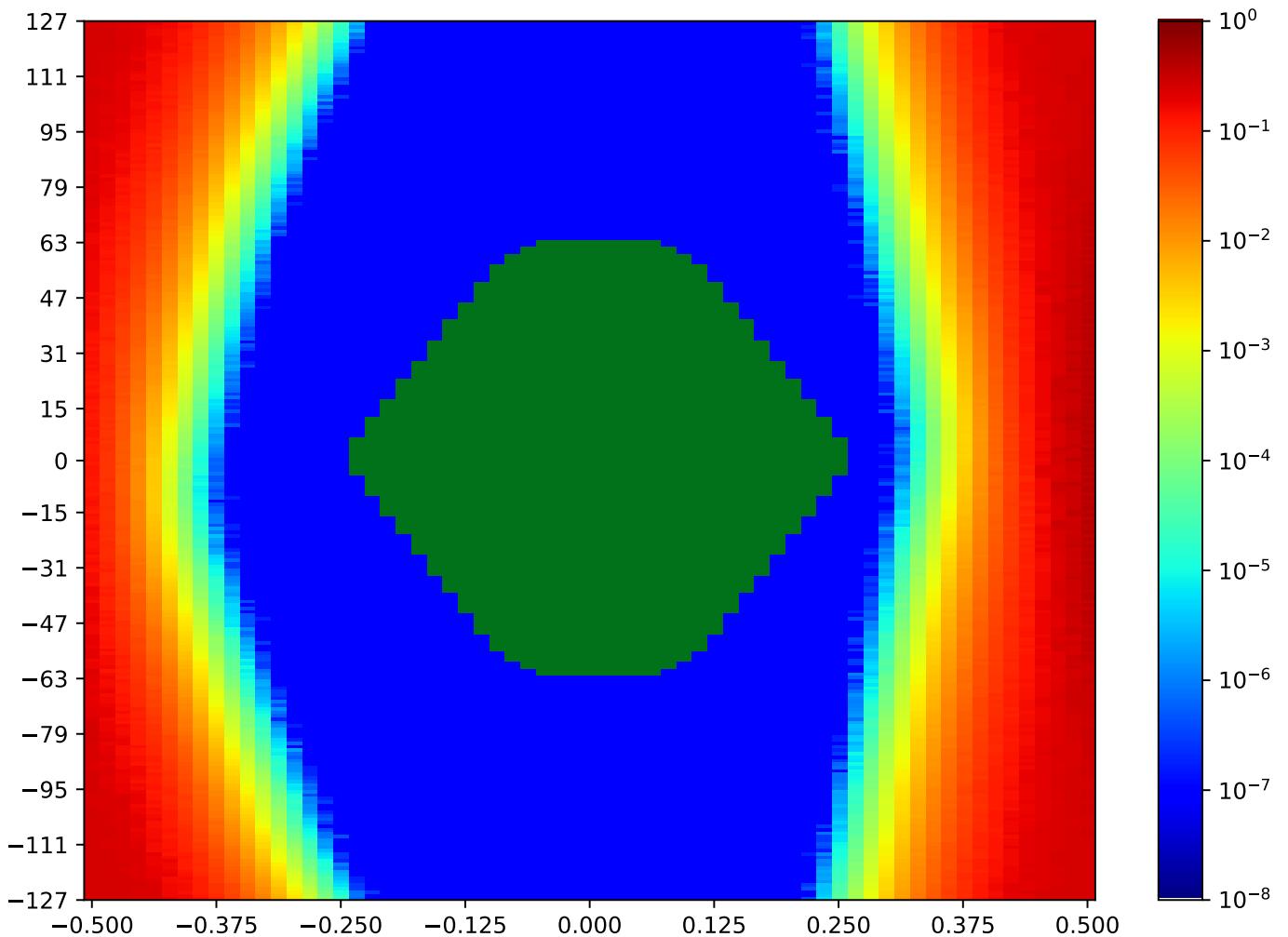


Figure 2.291: MSP_C_FPGA-TX4-11-RX3-11-MSP_A_FPGA

Call back to summary Figure 2.279. Sibling eye diagrams: V1-12.8.

Chapter 3

MUCTPI V1 12.8 Gbps

3.1 MSP_A TX1 MSP_C RX16 Minipod Loopback

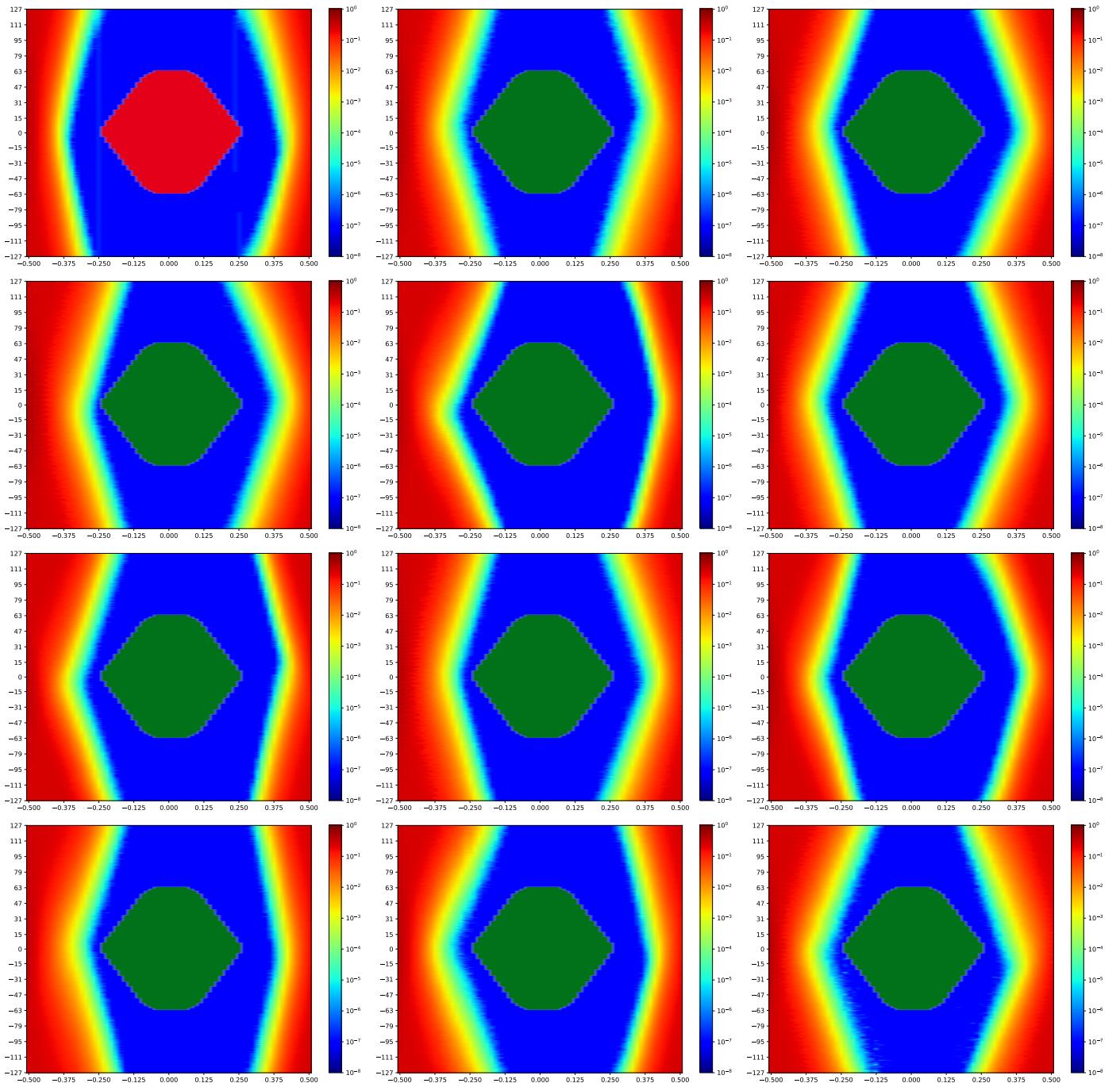


Figure 3.1: MSP_A TX1 MSP_C RX16 Minipod Loopback

A cross-reference to Figure 3.1. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.14.

3.1.1 MSP_A_FPGA-TX1-00-RX16-00-MSP_C_FPGA

Table 3.1: MSP_A_FPGA-TX1-00-RX16-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:29:15		2018-Jan-23 23:29:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9912	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

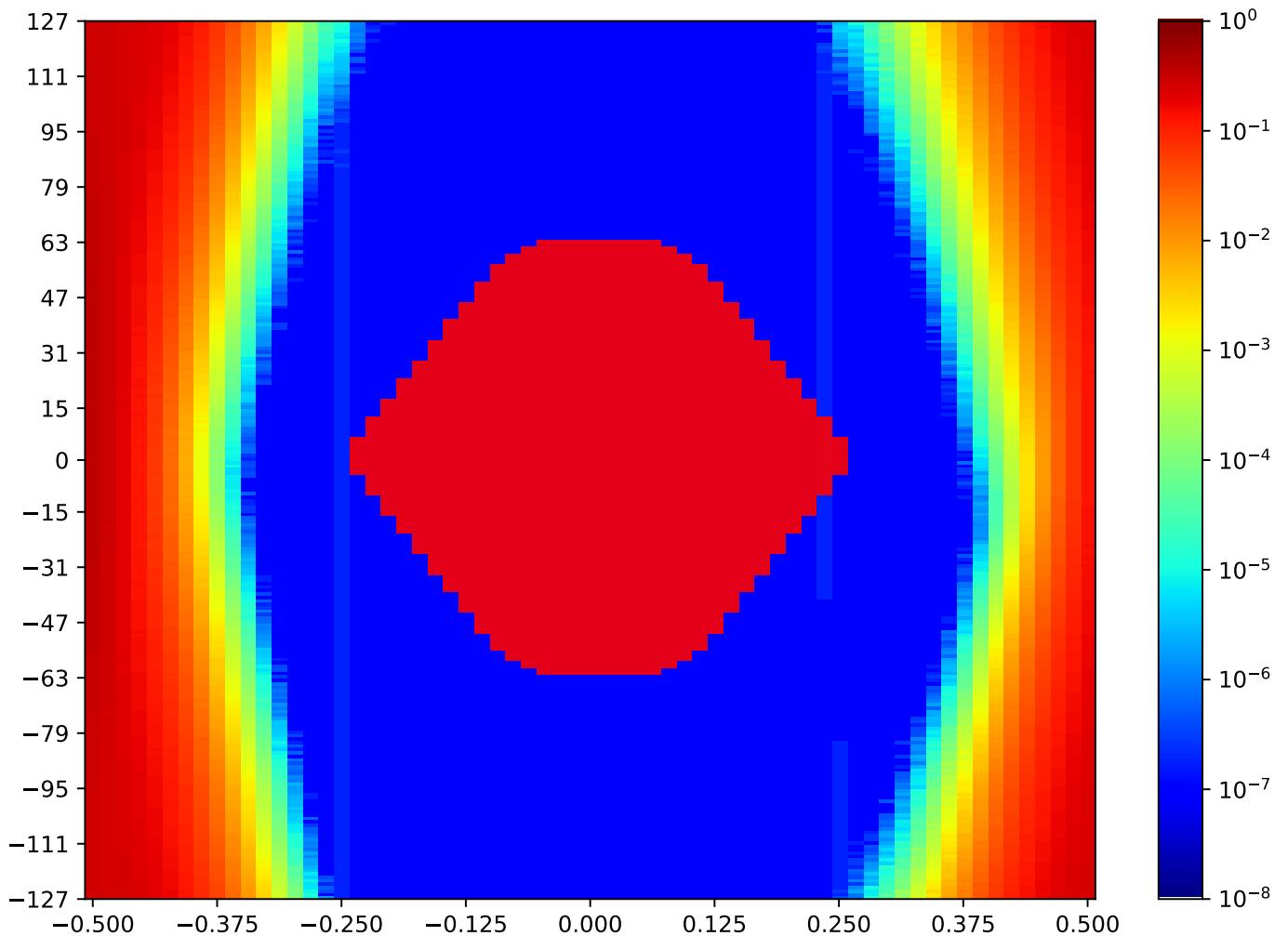


Figure 3.2: MSP_A_FPGA-TX1-00-RX16-00-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.2 MSP_A_FPGA-TX1-01-RX16-01-MSP_C_FPGA

Table 3.2: MSP_A_FPGA-TX1-01-RX16-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:29:57		2018-Jan-23 23:30:17	
Reset RX	OA	HO		HO (%)	
true	7286	34		52.31%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

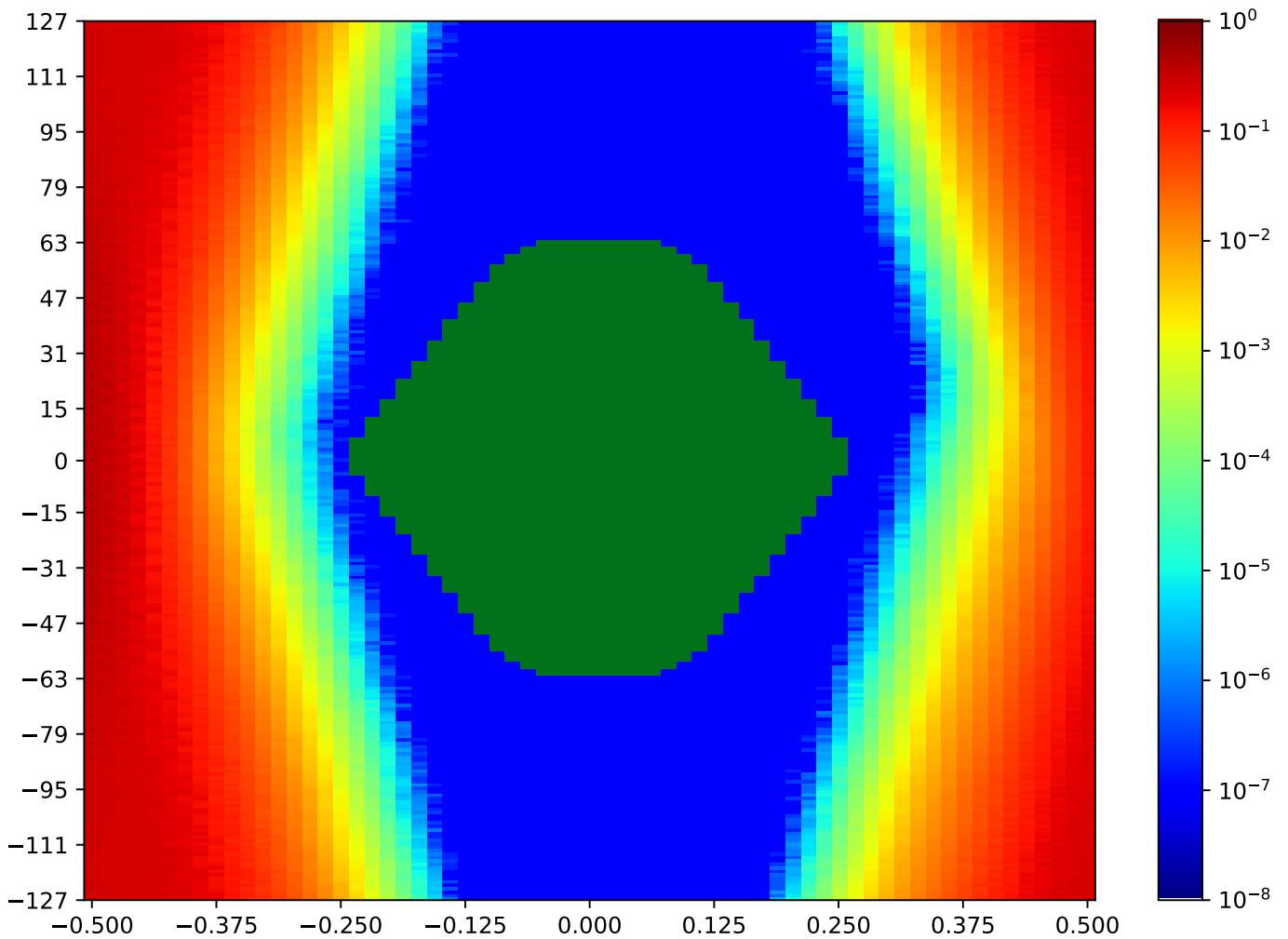


Figure 3.3: MSP_A_FPGA-TX1-01-RX16-01-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.3 MSP_A_FPGA-TX1-02-RX16-02-MSP_C_FPGA

Table 3.3: MSP_A_FPGA-TX1-02-RX16-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:30:17		2018-Jan-23 23:30:38	
Reset RX	OA	HO		HO (%)	
true	7392	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

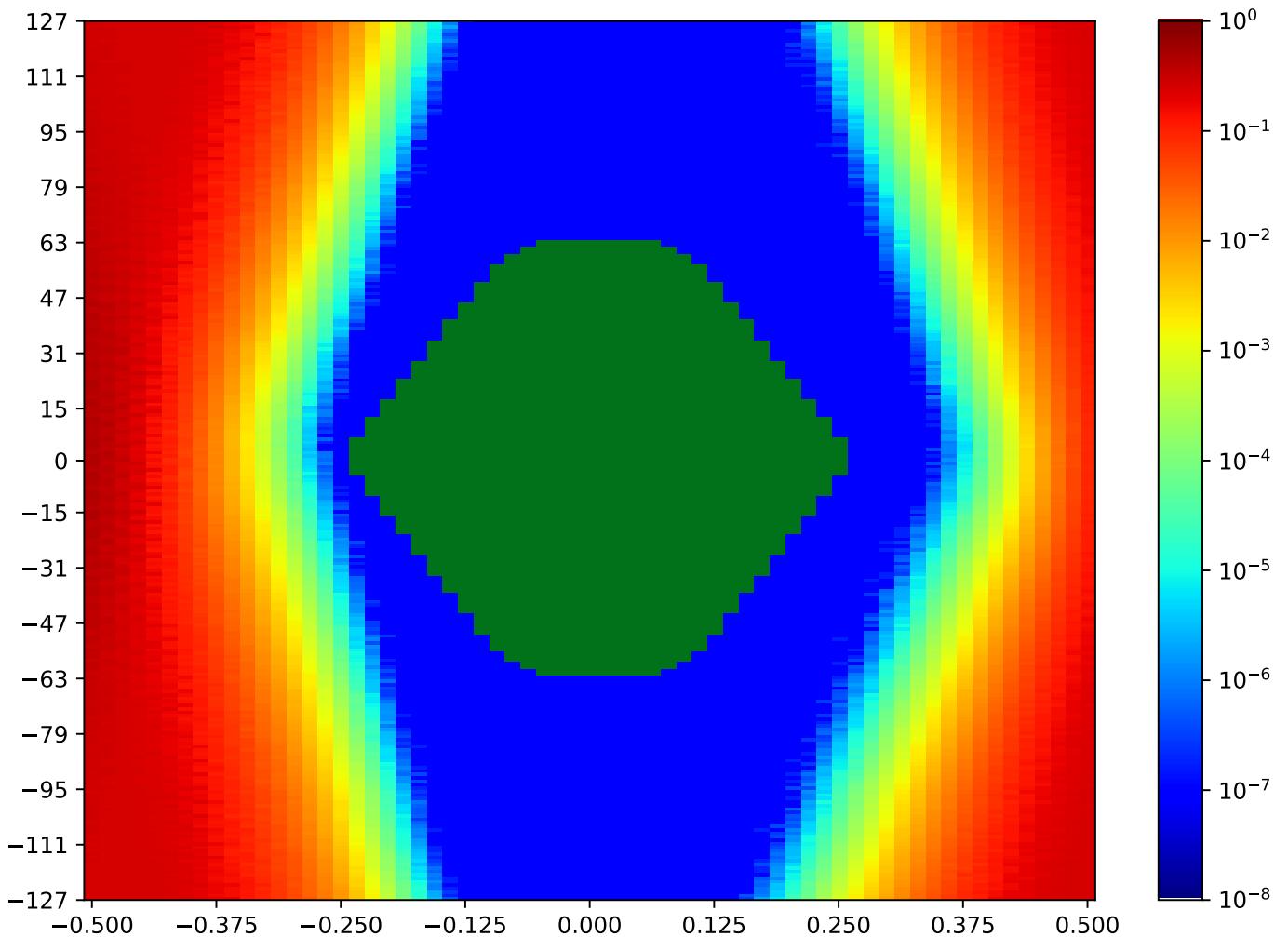


Figure 3.4: MSP_A_FPGA-TX1-02-RX16-02-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.4 MSP_A_FPGA-TX1-03-RX16-03-MSP_C_FPGA

Table 3.4: MSP_A_FPGA-TX1-03-RX16-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:28:33		2018-Jan-23 23:28:54	
Reset RX	OA	HO		HO (%)	
true	7363	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

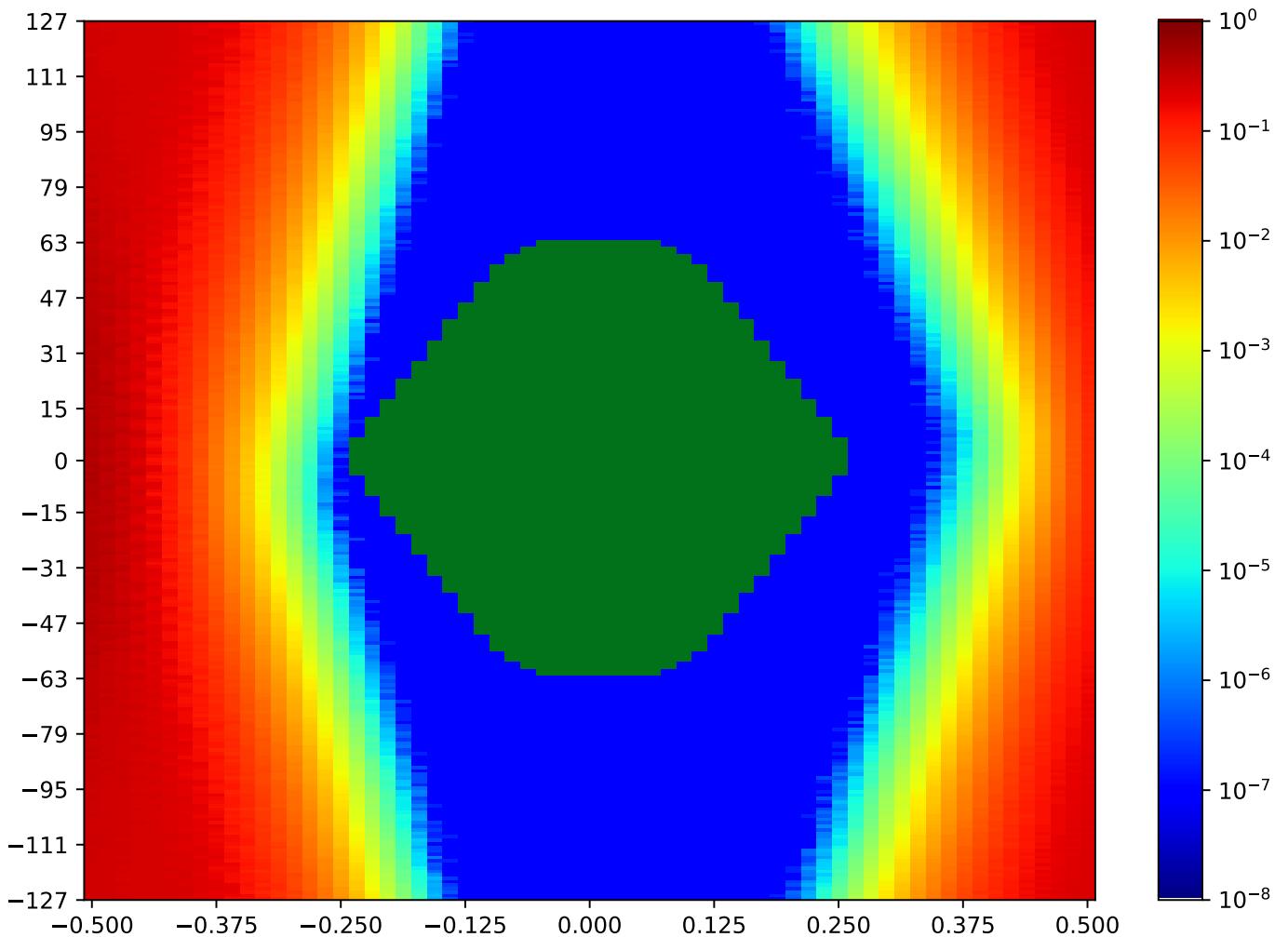


Figure 3.5: MSP_A_FPGA-TX1-03-RX16-03-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.5 MSP_A_FPGA-TX1-04-RX16-04-MSP_C_FPGA

Table 3.5: MSP_A_FPGA-TX1-04-RX16-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:31:18		2018-Jan-23 23:31:39	
Reset RX	OA	HO		HO (%)	
true	8744	41		63.08%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

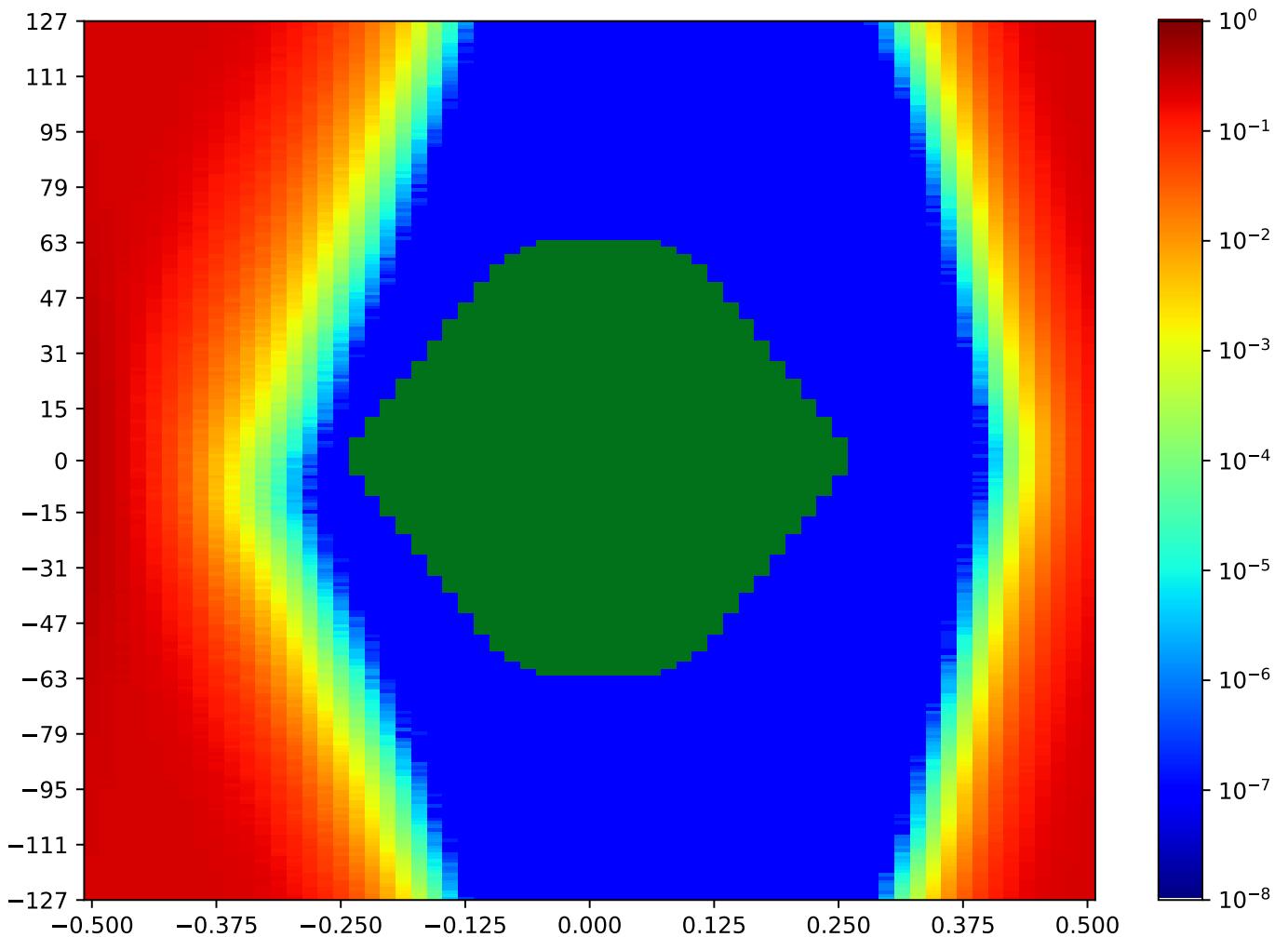


Figure 3.6: MSP_A_FPGA-TX1-04-RX16-04-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.6 MSP_A_FPGA-TX1-05-RX16-05-MSP_C_FPGA

Table 3.6: MSP_A_FPGA-TX1-05-RX16-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:28:13		2018-Jan-23 23:28:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7387	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

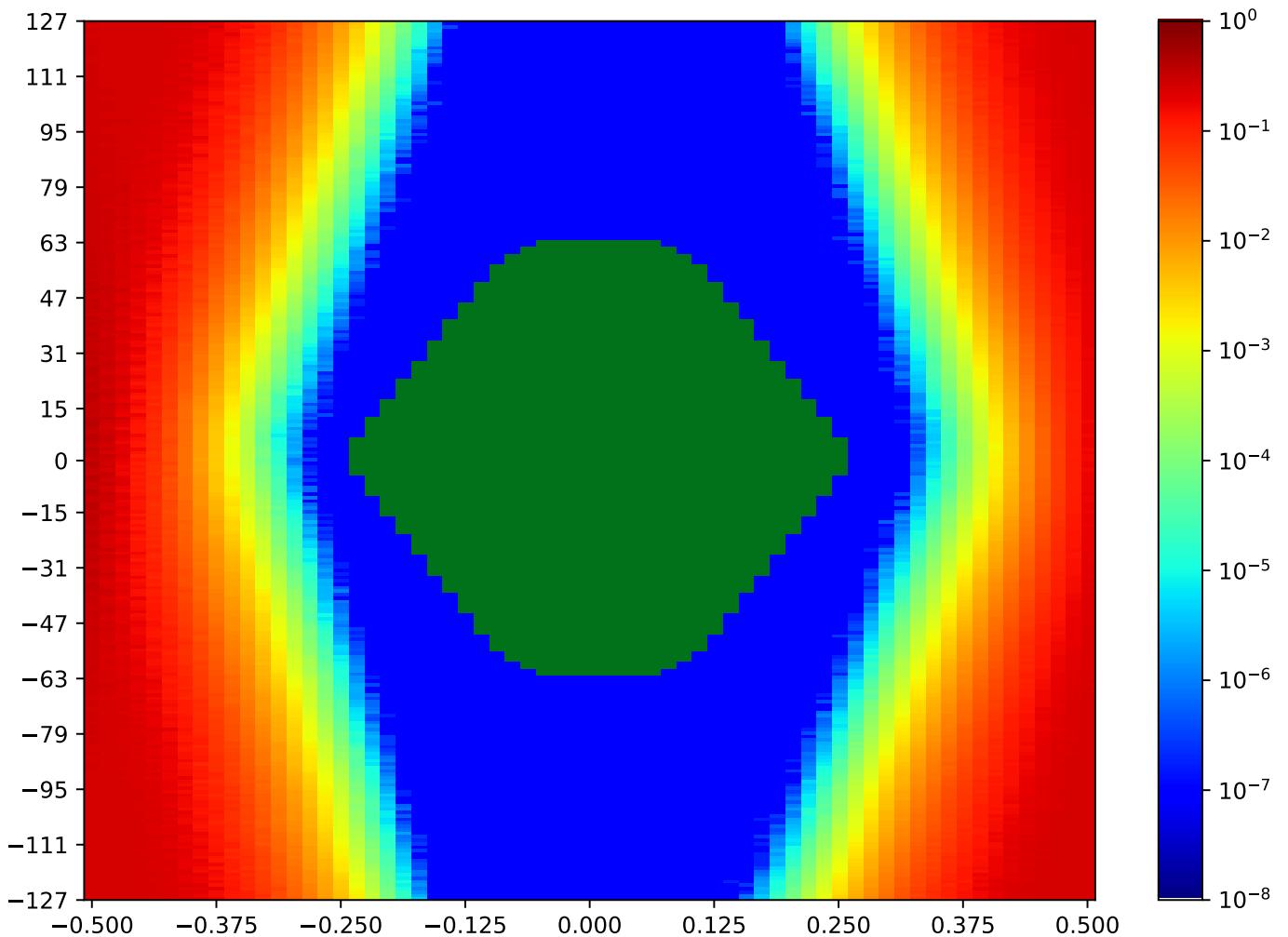


Figure 3.7: MSP_A_FPGA-TX1-05-RX16-05-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.7 MSP_A_FPGA-TX1-06-RX16-06-MSP_C_FPGA

Table 3.7: MSP_A_FPGA-TX1-06-RX16-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:31:59		2018-Jan-23 23:32:19	
Reset RX	OA	HO		HO (%)	
true	8842	41		63.08%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

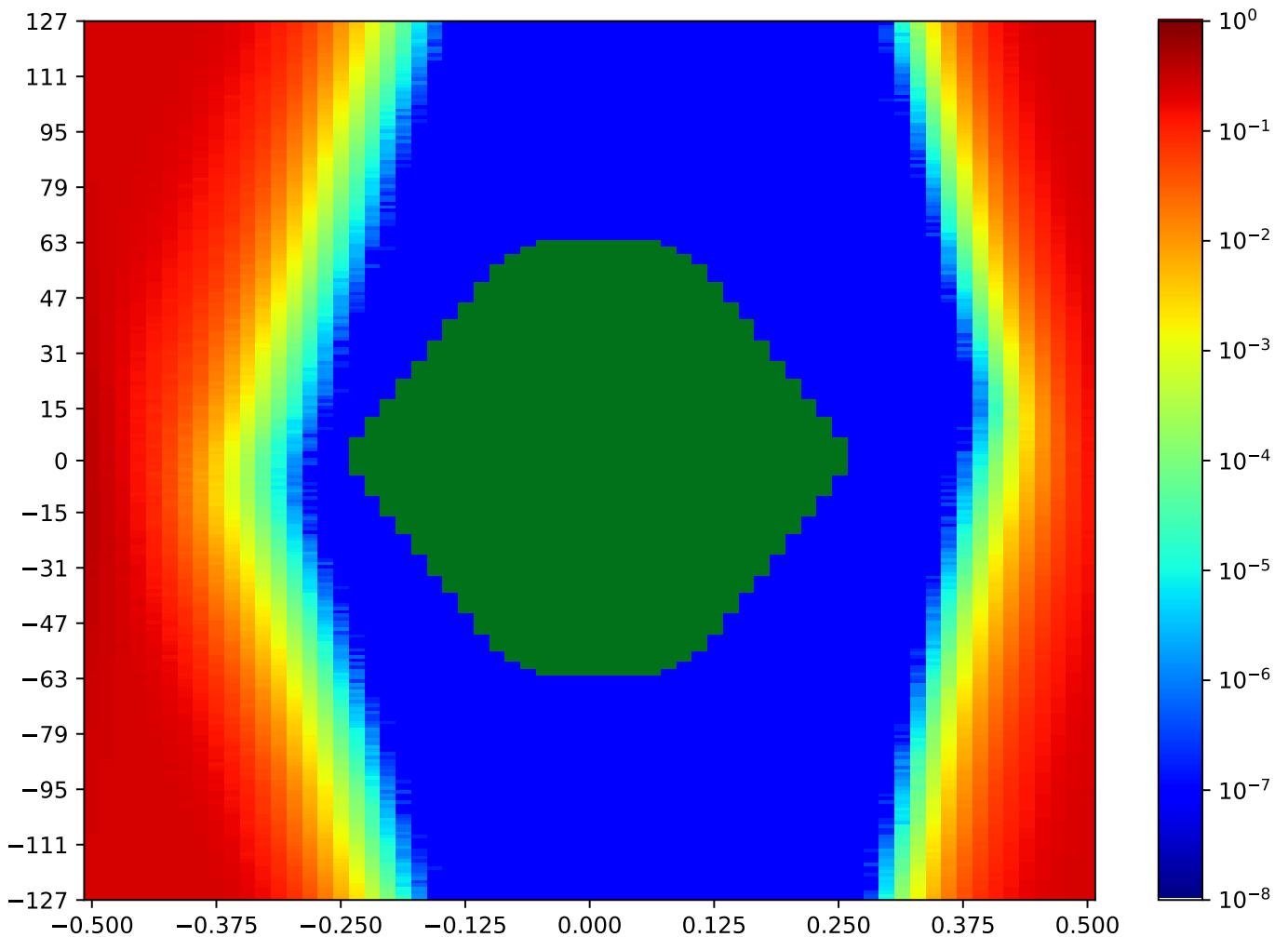


Figure 3.8: MSP_A_FPGA-TX1-06-RX16-06-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.8 MSP_A_FPGA-TX1-07-RX16-07-MSP_C_FPGA

Table 3.8: MSP_A_FPGA-TX1-07-RX16-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:28:54		2018-Jan-23 23:29:15	
Reset RX	OA	HO		HO (%)	
true	7642	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

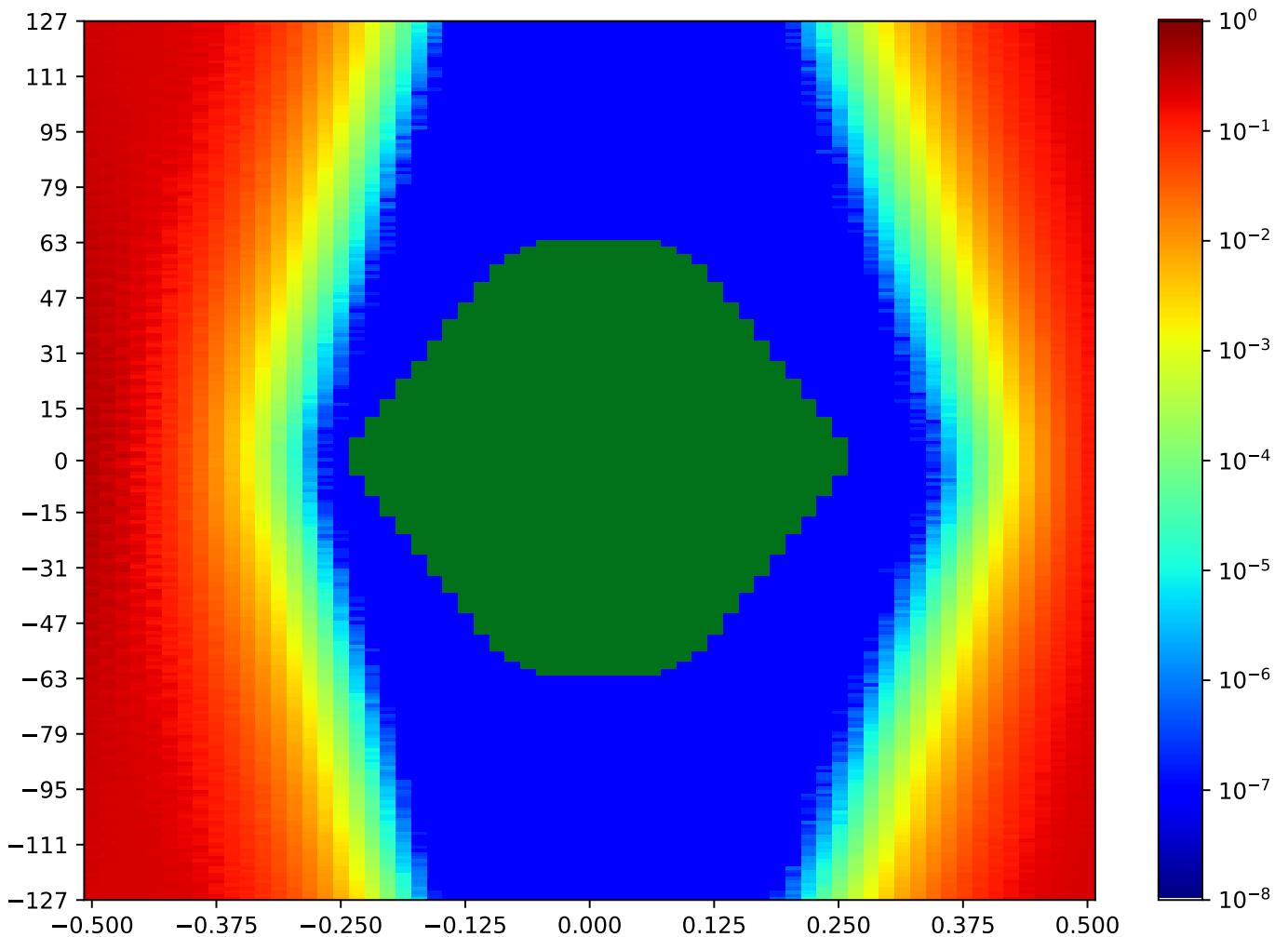


Figure 3.9: MSP_A_FPGA-TX1-07-RX16-07-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.9 MSP_A_FPGA-TX1-08-RX16-08-MSP_C_FPGA

Table 3.9: MSP_A_FPGA-TX1-08-RX16-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:31:39		2018-Jan-23 23:31:59	
Reset RX	OA	HO		HO (%)	
true	8316	41		63.08%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

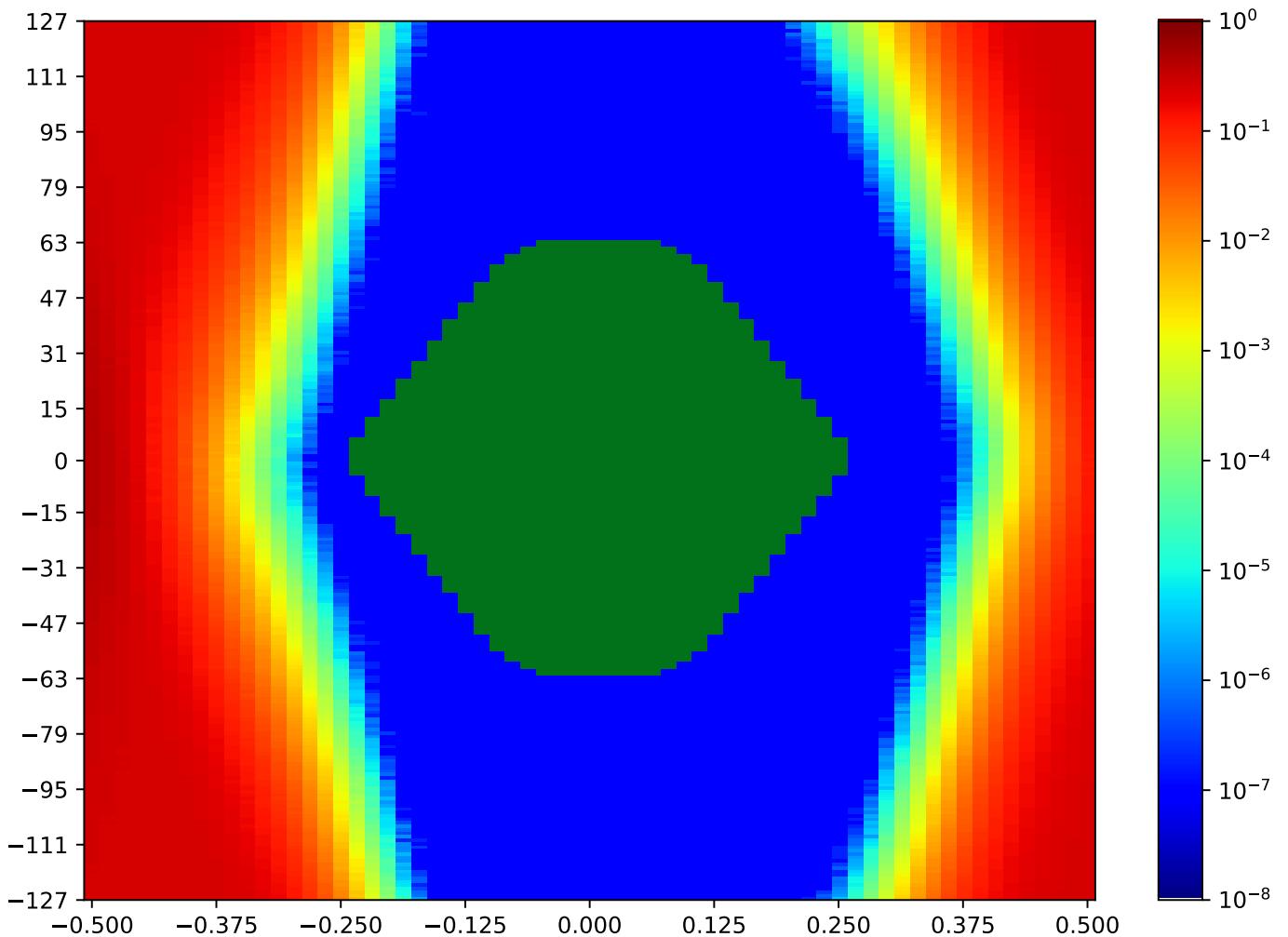


Figure 3.10: MSP_A_FPGA-TX1-08-RX16-08-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.10 MSP_A_FPGA-TX1-09-RX16-09-MSP_C_FPGA

Table 3.10: MSP_A_FPGA-TX1-09-RX16-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:29:36		2018-Jan-23 23:29:57	
Reset RX	OA	HO		HO (%)	
true	8464	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

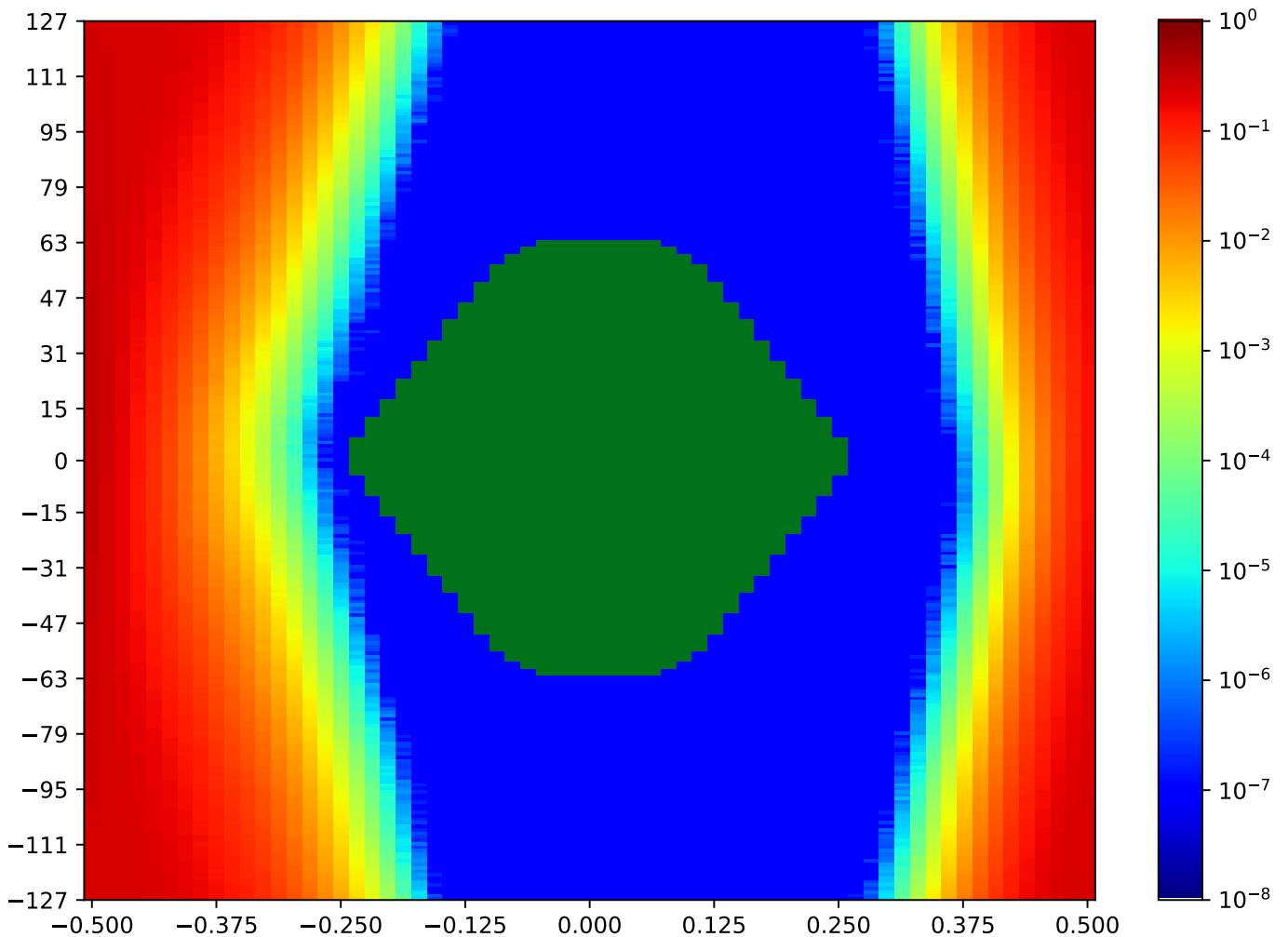


Figure 3.11: MSP_A_FPGA-TX1-09-RX16-09-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.11 MSP_A_FPGA-TX1-10-RX16-10-MSP_C_FPGA

Table 3.11: MSP_A_FPGA-TX1-10-RX16-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:30:58		2018-Jan-23 23:31:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8137	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

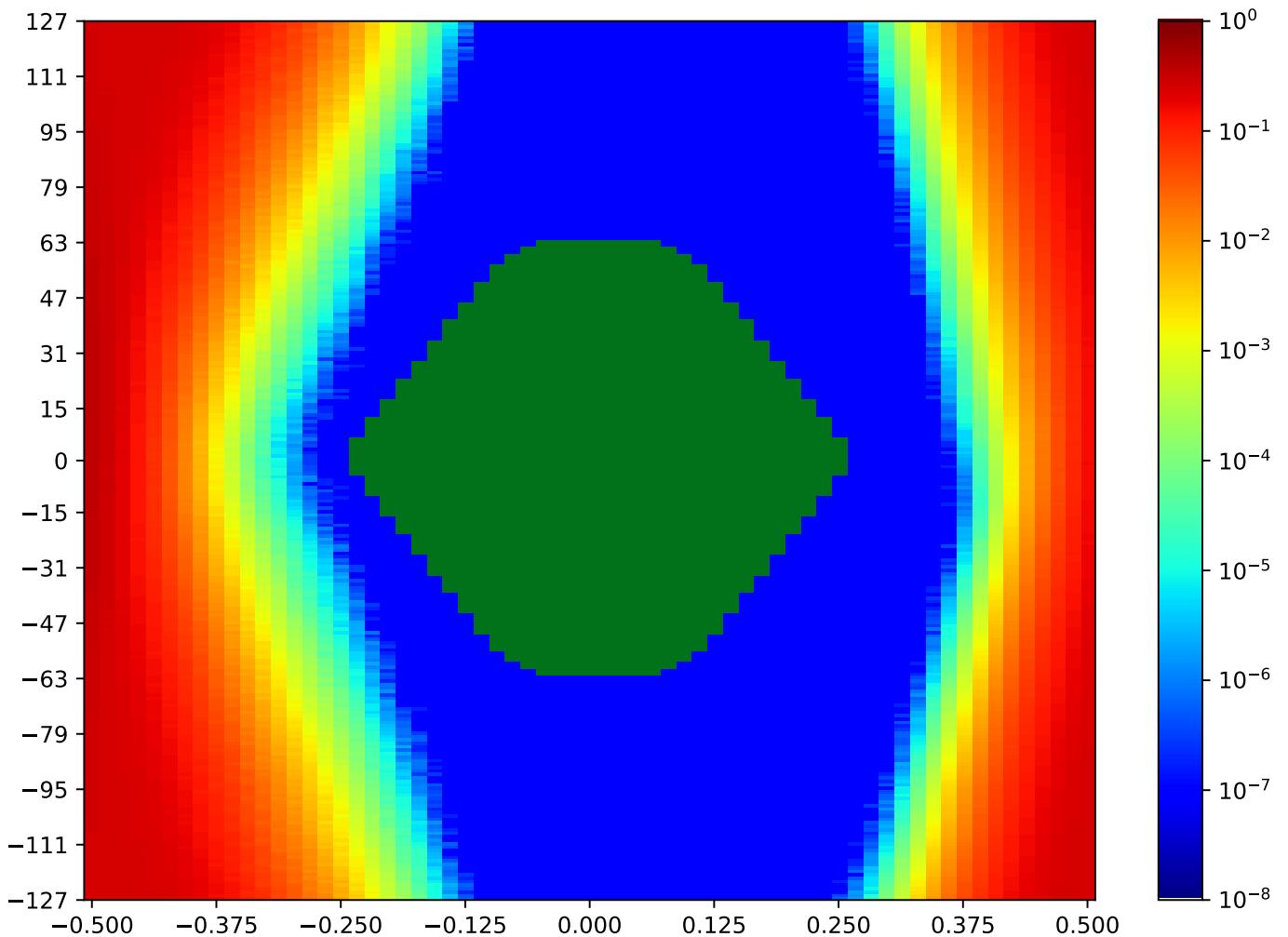


Figure 3.12: MSP_A_FPGA-TX1-10-RX16-10-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.1.12 MSP_A_FPGA-TX1-11-RX16-11-MSP_C_FPGA

Table 3.12: MSP_A_FPGA-TX1-11-RX16-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:30:38		2018-Jan-23 23:30:58	
Reset RX	OA	HO		HO (%)	
true	6656	34		52.31%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

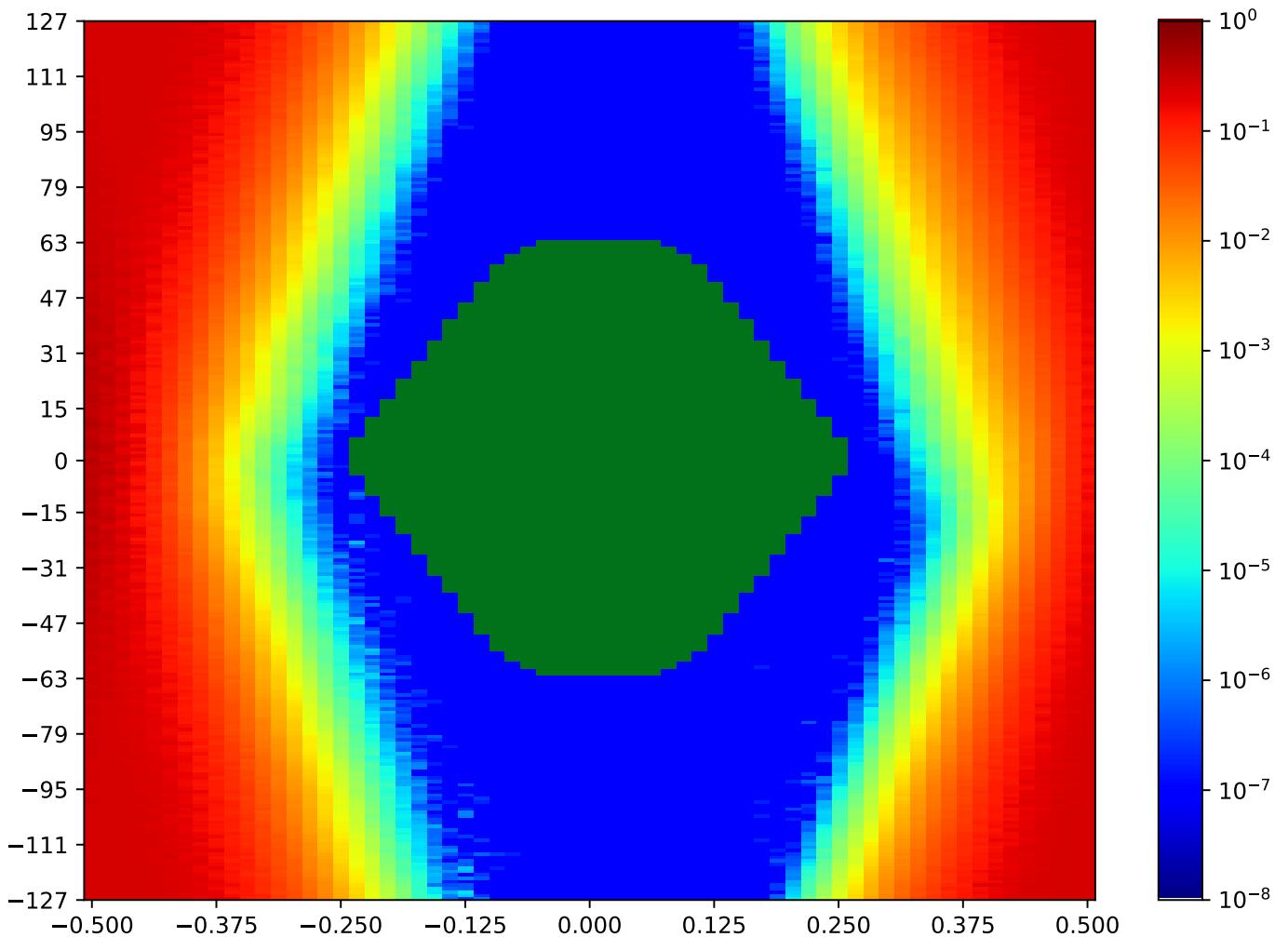


Figure 3.13: MSP_A_FPGA-TX1-11-RX16-11-MSP_C_FPGA

Call back to summary Figure 3.1. Sibling eye diagrams: V1-6.4.

3.2 MSP_A TX2 MSP_C RX15 Minipod Loopback

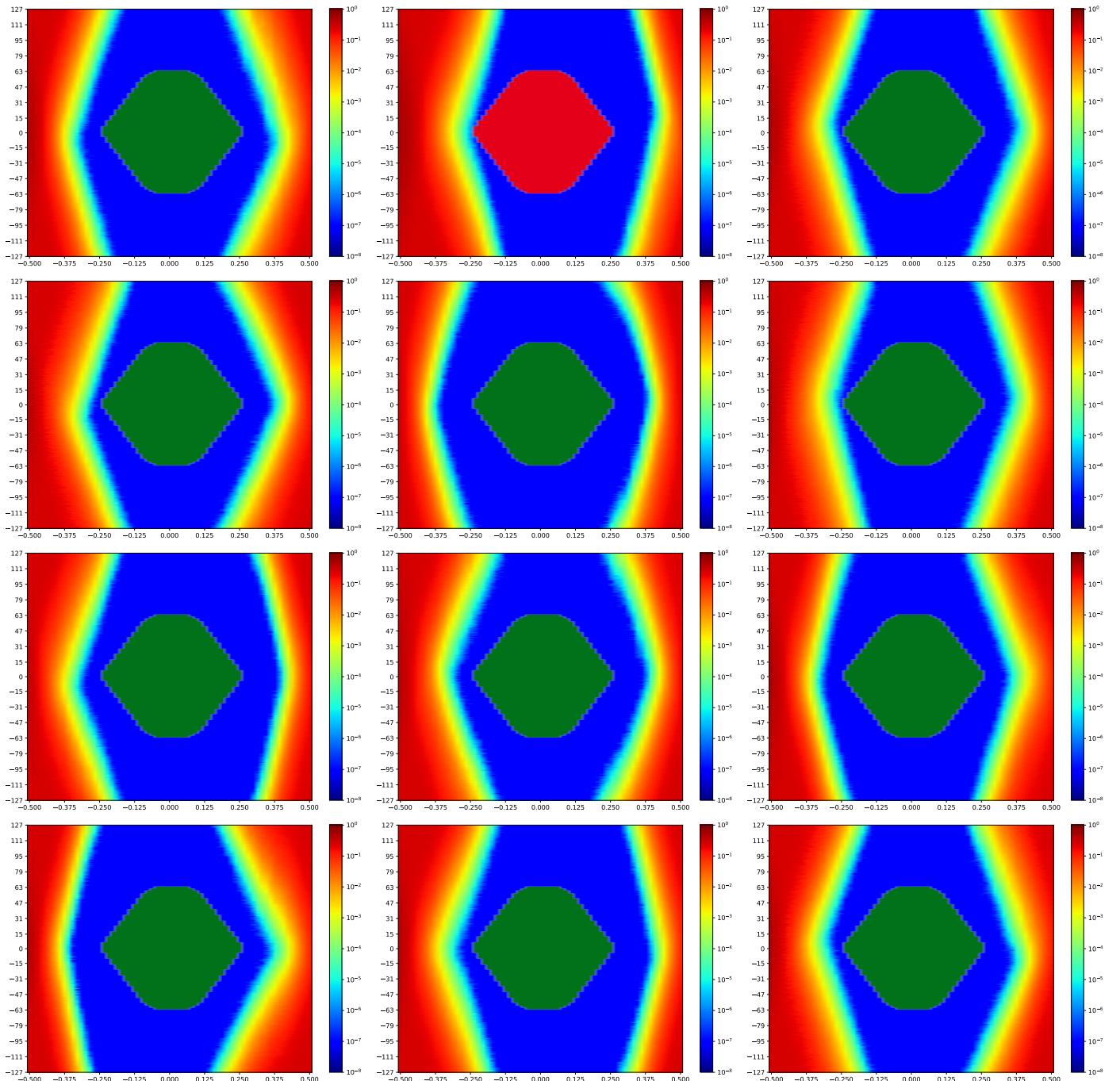


Figure 3.14: MSP_A TX2 MSP_C RX15 Minipod Loopback

A cross-reference to Figure 3.14. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.27.

3.2.1 MSP_A_FPGA-TX2-00-RX15-00-MSP_C_FPGA

Table 3.13: MSP_A_FPGA-TX2-00-RX15-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:33:20		2018-Jan-23 23:33:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8099	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

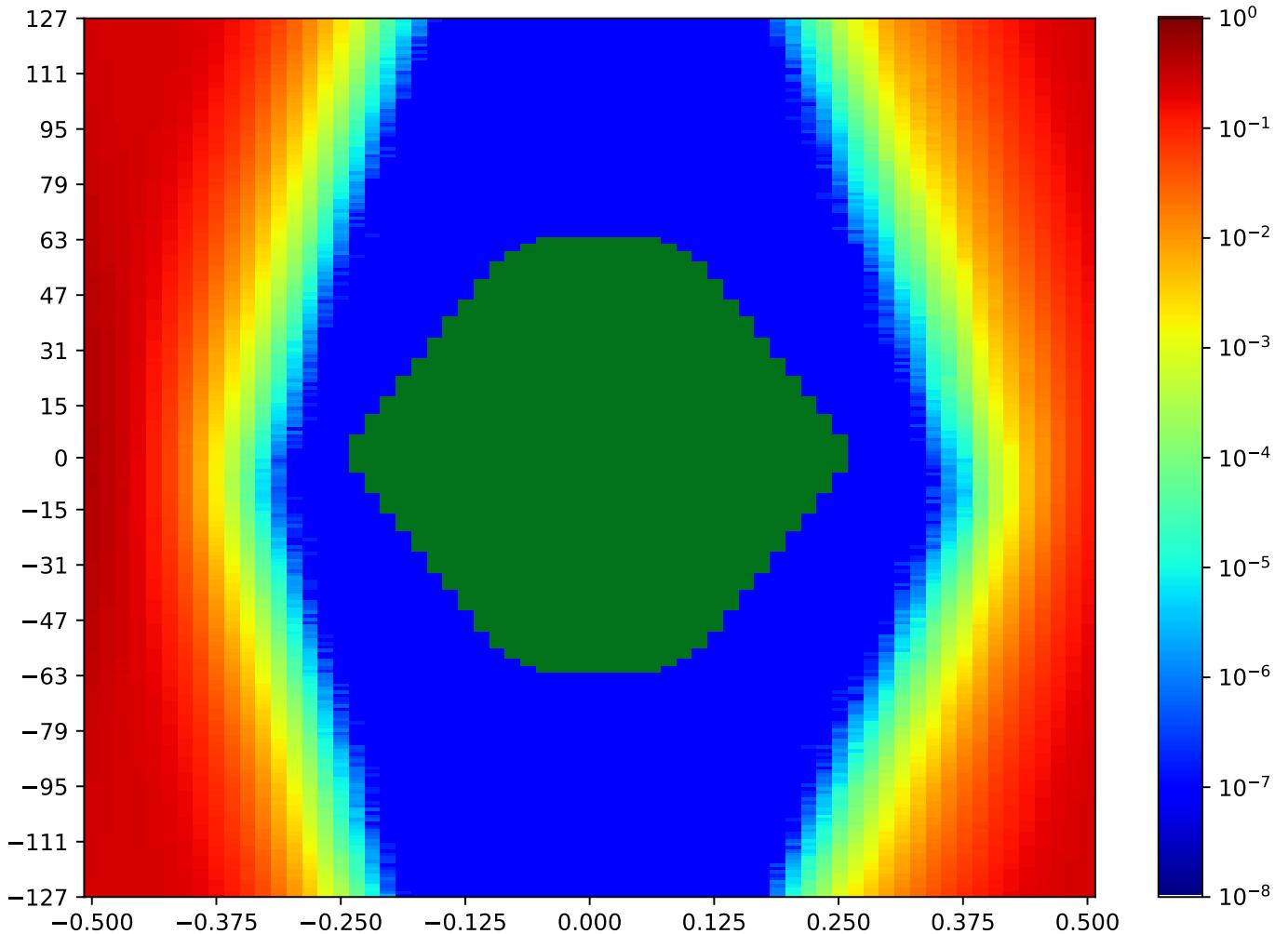


Figure 3.15: MSP_A_FPGA-TX2-00-RX15-00-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.2 MSP_A_FPGA-TX2-01-RX15-01-MSP_C_FPGA

Table 3.14: MSP_A_FPGA-TX2-01-RX15-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:32:39		2018-Jan-23 23:33:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8220	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

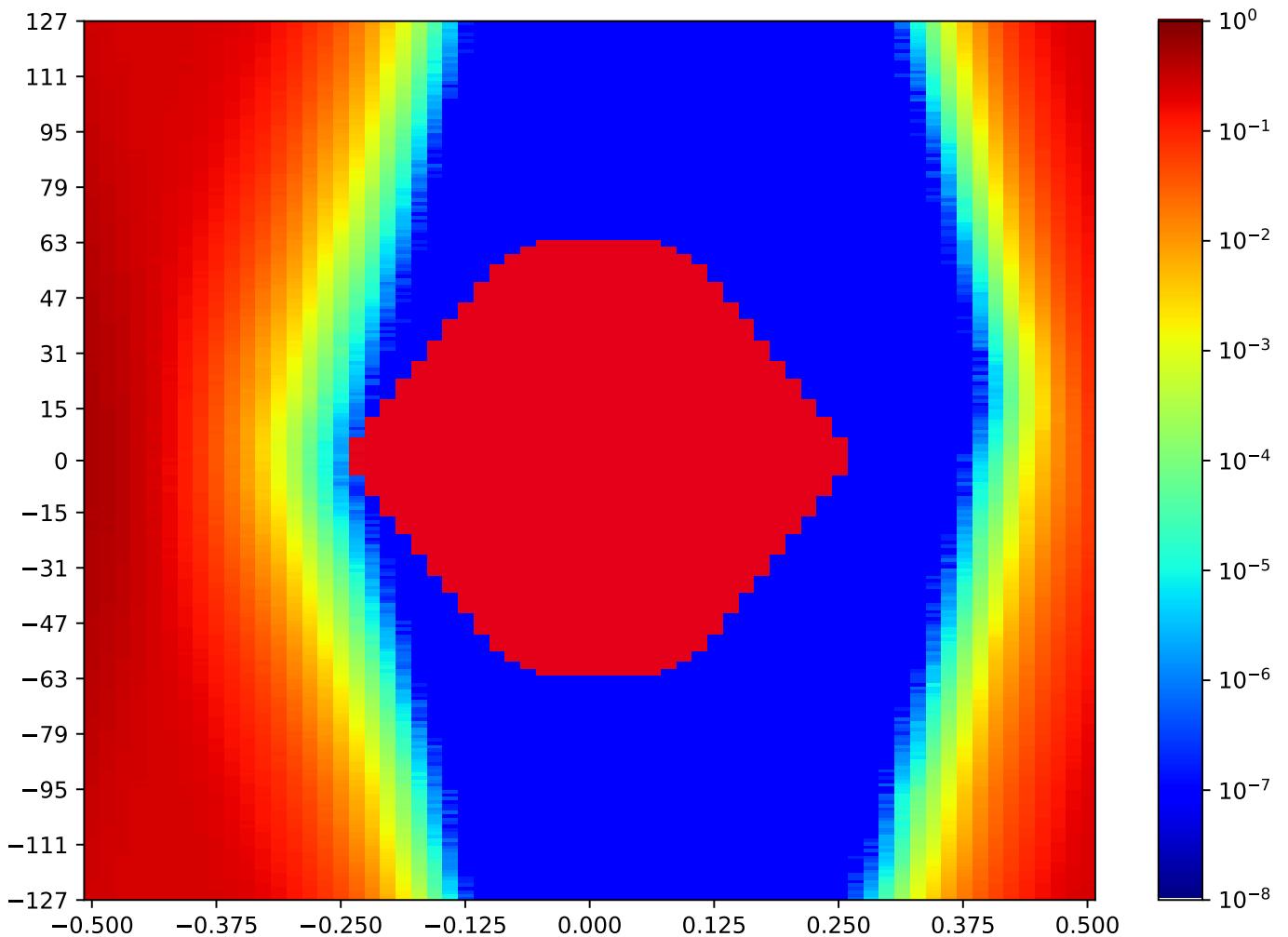


Figure 3.16: MSP_A_FPGA-TX2-01-RX15-01-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.3 MSP_A_FPGA-TX2-02-RX15-02-MSP_C_FPGA

Table 3.15: MSP_A_FPGA-TX2-02-RX15-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:34:20		2018-Jan-23 23:34:40	
Reset RX	OA	HO		HO (%)	
true	7526	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

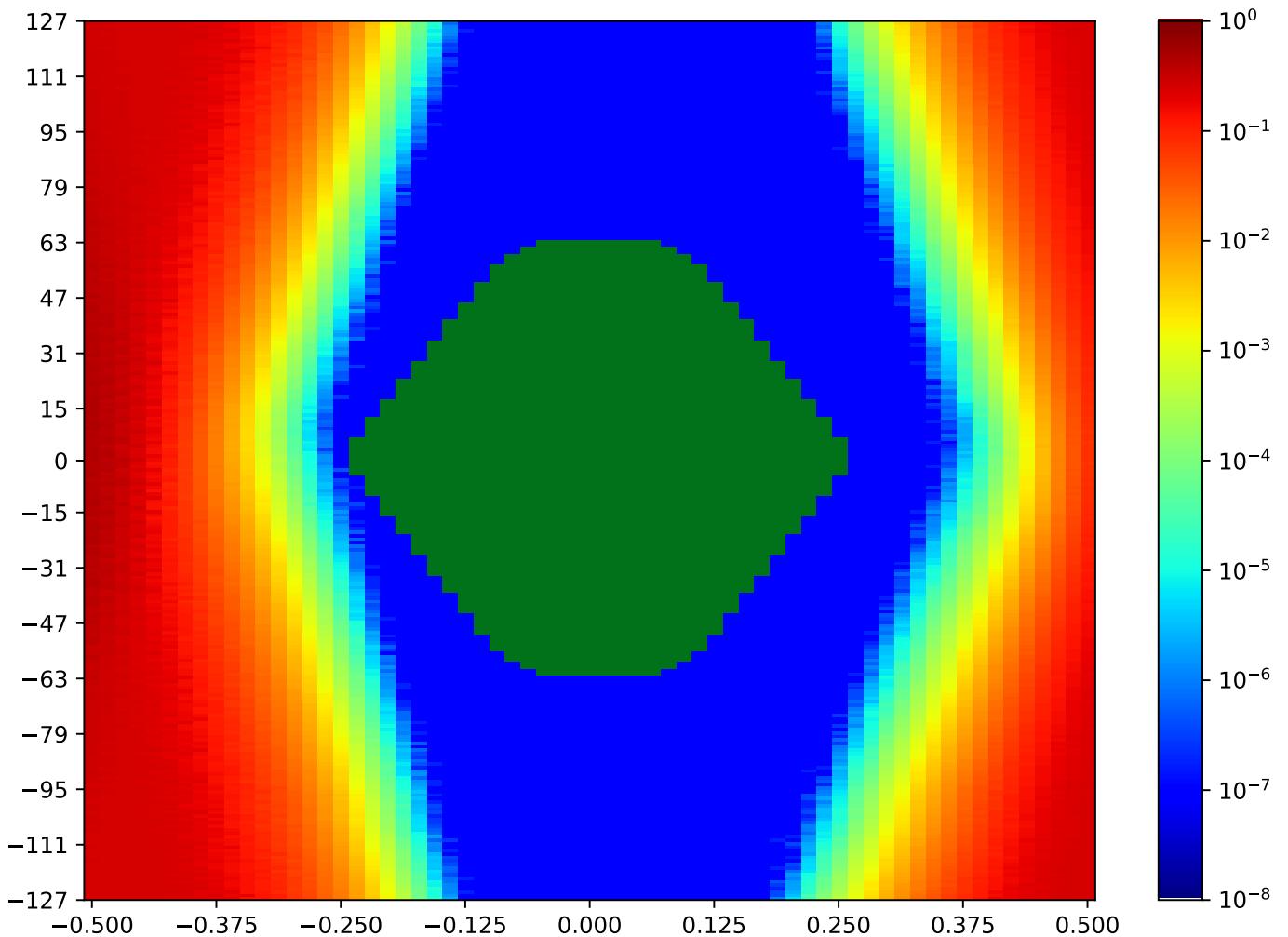


Figure 3.17: MSP_A_FPGA-TX2-02-RX15-02-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.4 MSP_A_FPGA-TX2-03-RX15-03-MSP_C_FPGA

Table 3.16: MSP_A_FPGA-TX2-03-RX15-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:32:19		2018-Jan-23 23:32:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7300	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

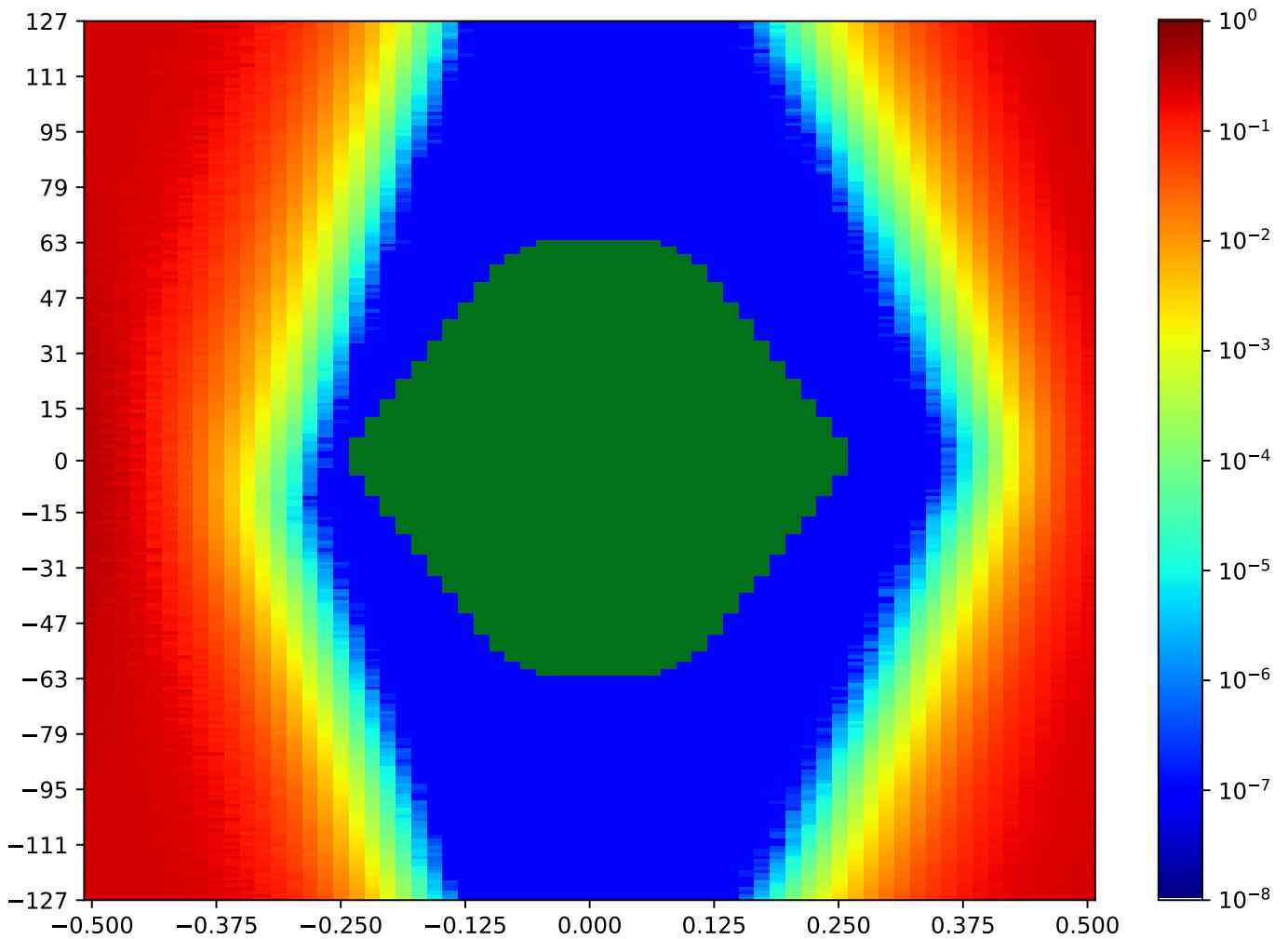


Figure 3.18: MSP_A_FPGA-TX2-03-RX15-03-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.5 MSP_A_FPGA-TX2-04-RX15-04-MSP_C_FPGA

Table 3.17: MSP_A_FPGA-TX2-04-RX15-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:35:22		2018-Jan-23 23:35:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9666	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

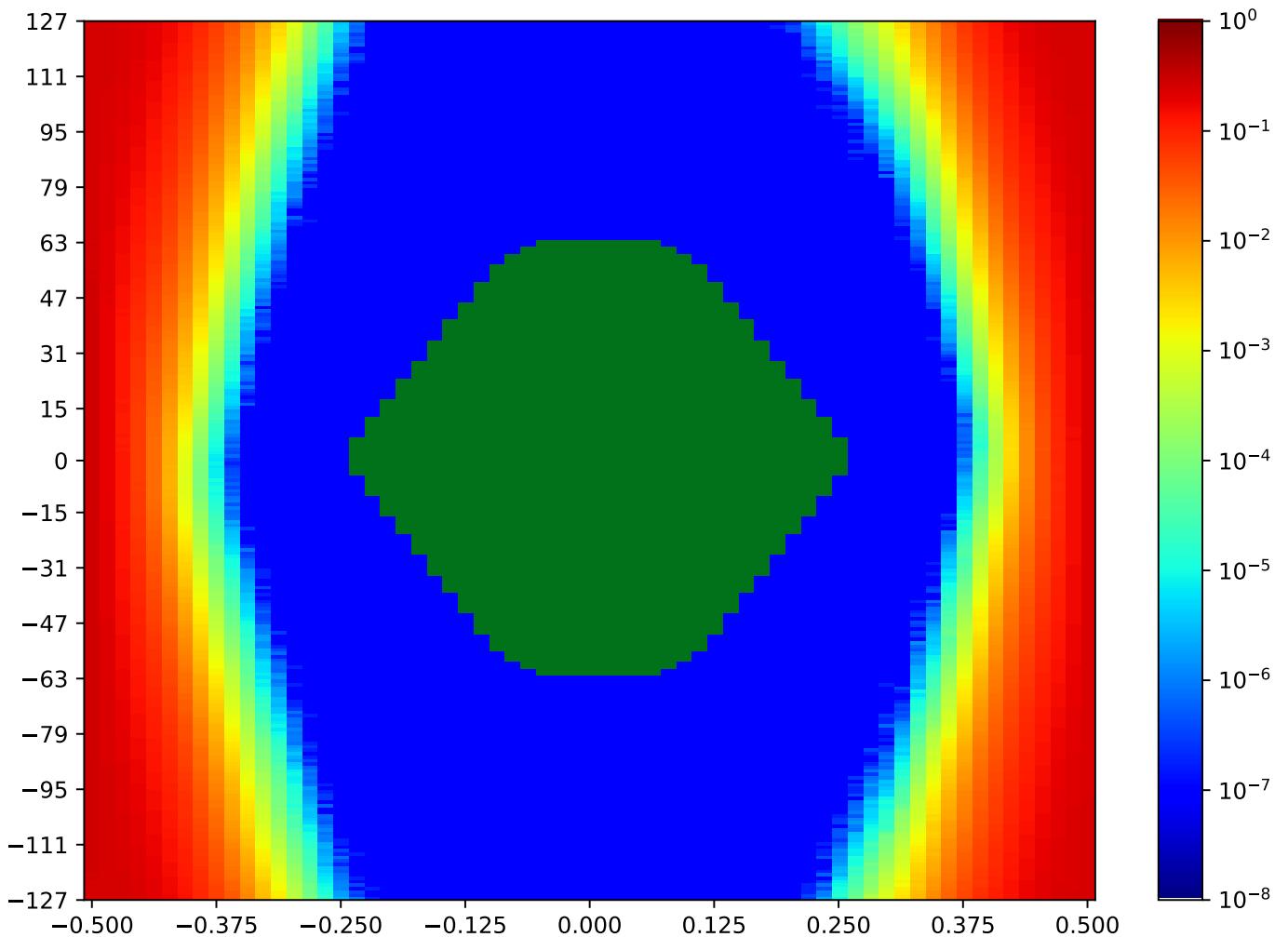


Figure 3.19: MSP_A_FPGA-TX2-04-RX15-04-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.6 MSP_A_FPGA-TX2-05-RX15-05-MSP_C_FPGA

Table 3.18: MSP_A_FPGA-TX2-05-RX15-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:33:00		2018-Jan-23 23:33:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7204	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

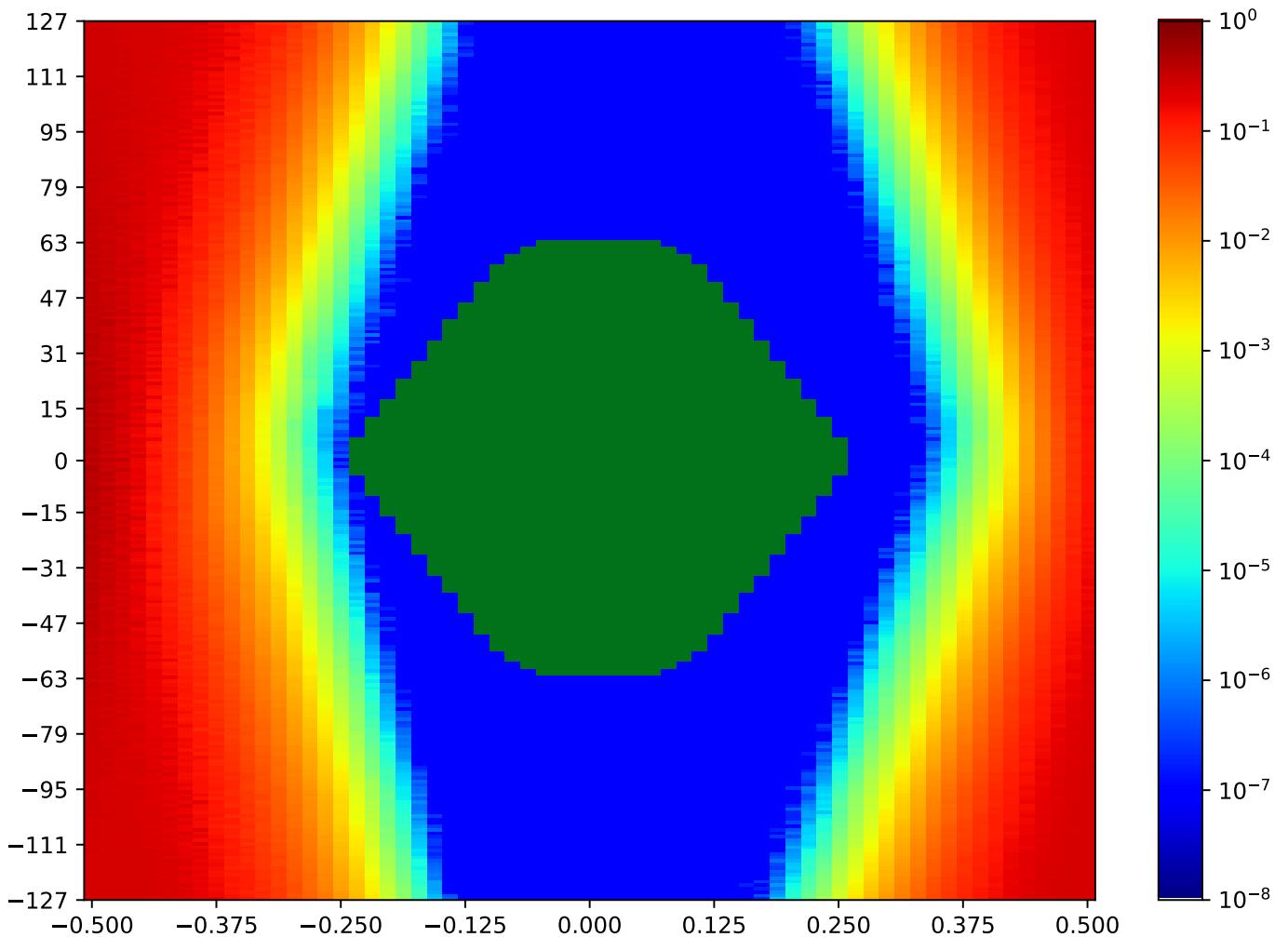


Figure 3.20: MSP_A_FPGA-TX2-05-RX15-05-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.7 MSP_A_FPGA-TX2-06-RX15-06-MSP_C_FPGA

Table 3.19: MSP_A_FPGA-TX2-06-RX15-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:36:03		2018-Jan-23 23:36:24	
Reset RX	OA	HO		HO (%)	
true	9151	44		66.15%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

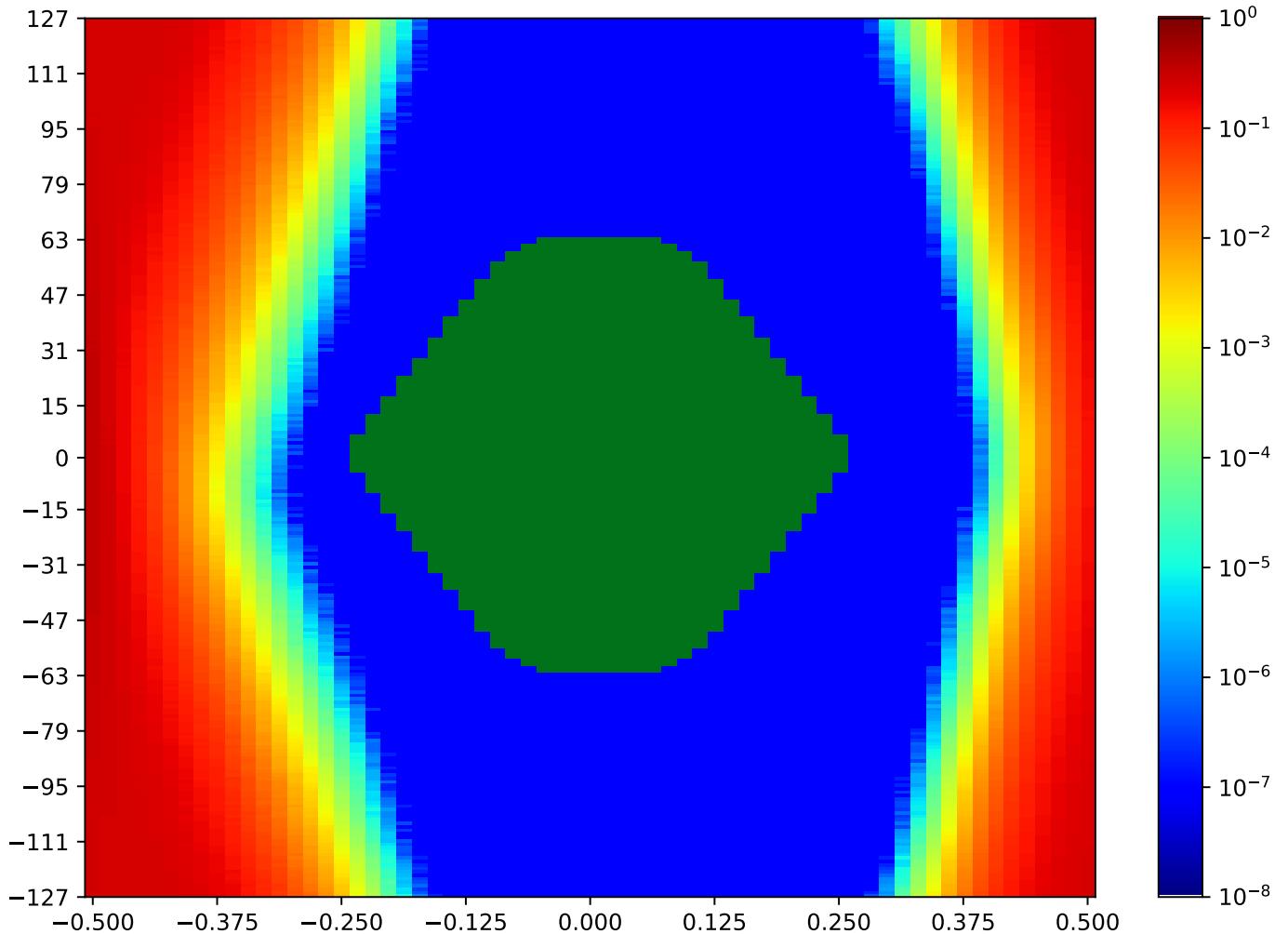


Figure 3.21: MSP_A_FPGA-TX2-06-RX15-06-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.8 MSP_A_FPGA-TX2-07-RX15-07-MSP_C_FPGA

Table 3.20: MSP_A_FPGA-TX2-07-RX15-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:33:40		2018-Jan-23 23:34:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7917	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

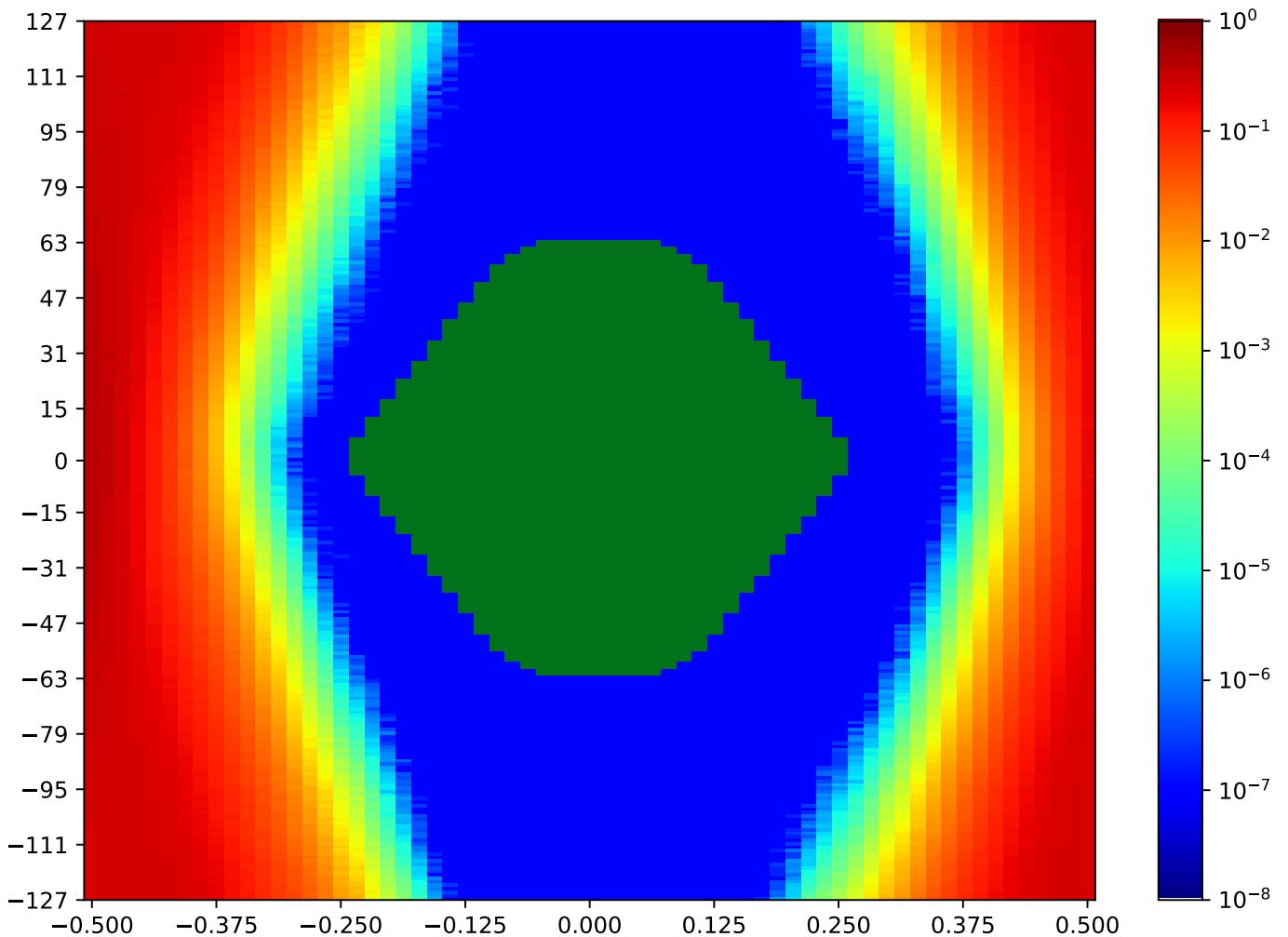


Figure 3.22: MSP_A_FPGA-TX2-07-RX15-07-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.9 MSP_A_FPGA-TX2-08-RX15-08-MSP_C_FPGA

Table 3.21: MSP_A_FPGA-TX2-08-RX15-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:35:42			2018-Jan-23 23:36:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	8277	41	63.08%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

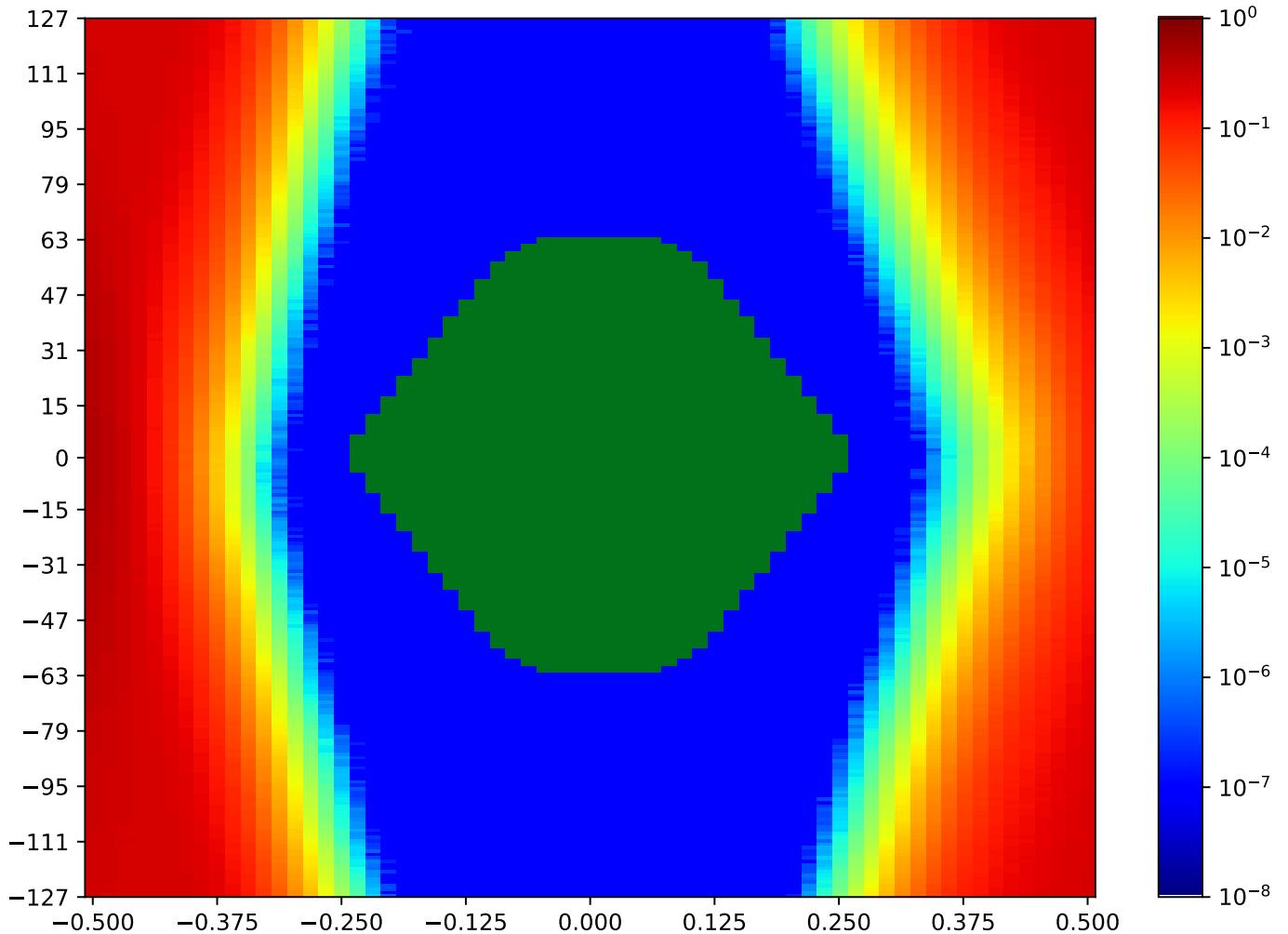


Figure 3.23: MSP_A_FPGA-TX2-08-RX15-08-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.10 MSP_A_FPGA-TX2-09-RX15-09-MSP_C_FPGA

Table 3.22: MSP_A_FPGA-TX2-09-RX15-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:34:00		2018-Jan-23 23:34:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8683	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

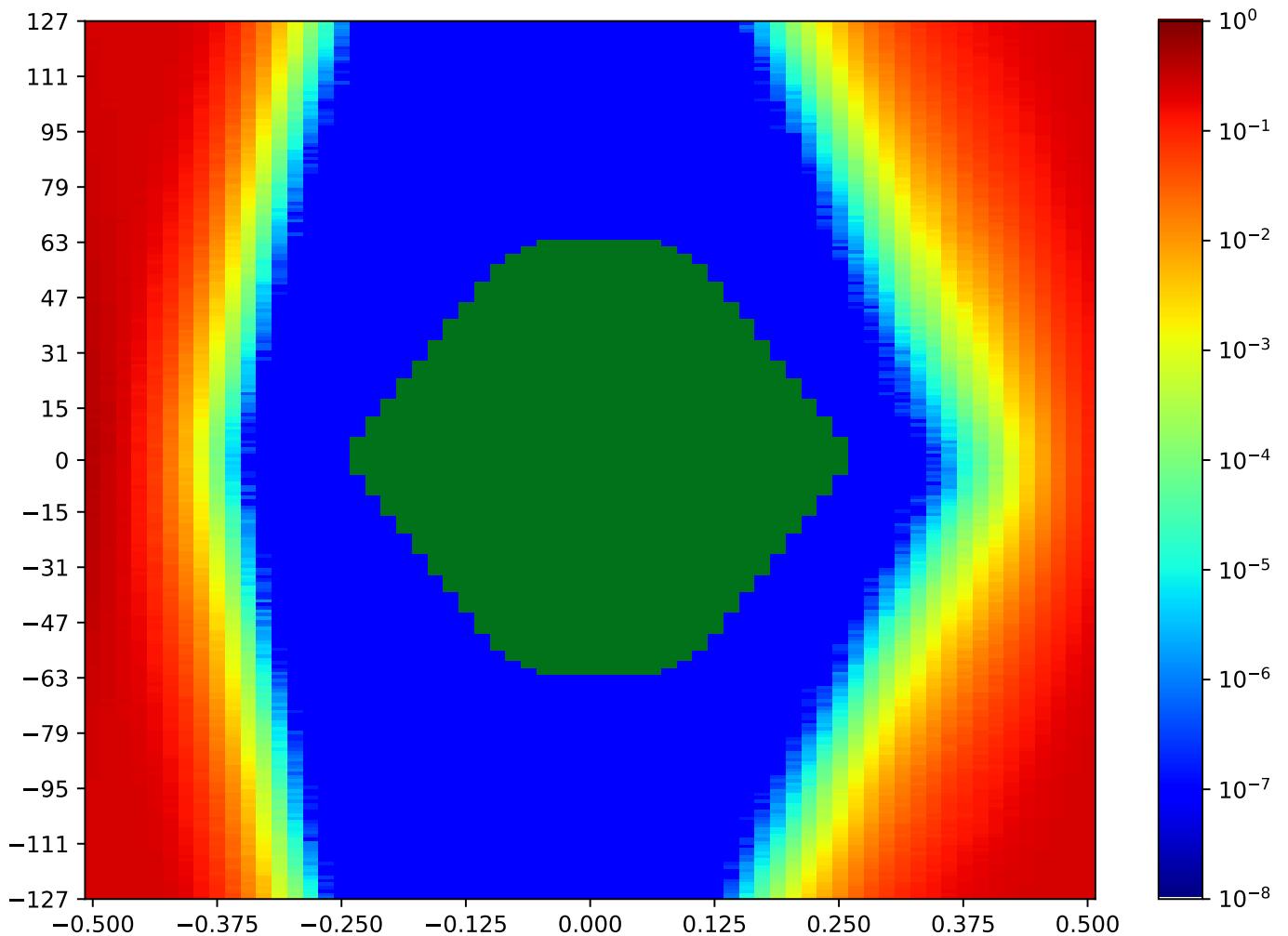


Figure 3.24: MSP_A_FPGA-TX2-09-RX15-09-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.11 MSP_A_FPGA-TX2-10-RX15-10-MSP_C_FPGA

Table 3.23: MSP_A_FPGA-TX2-10-RX15-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:35:01		2018-Jan-23 23:35:22	
Reset RX	OA	HO		HO (%)	
true	8711	42		64.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

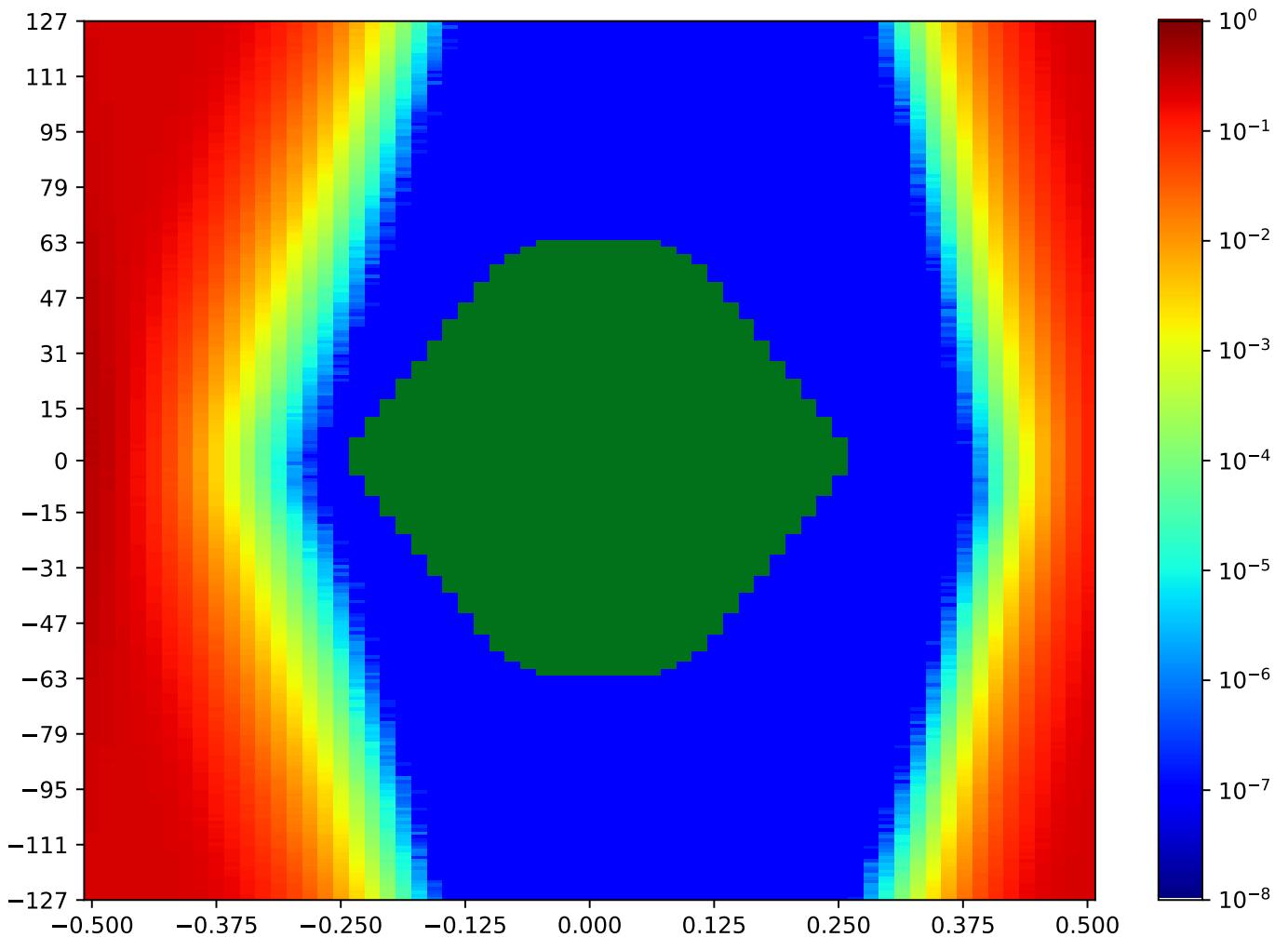


Figure 3.25: MSP_A_FPGA-TX2-10-RX15-10-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.2.12 MSP_A_FPGA-TX2-11-RX15-11-MSP_C_FPGA

Table 3.24: MSP_A_FPGA-TX2-11-RX15-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:34:41		2018-Jan-23 23:35:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7588	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

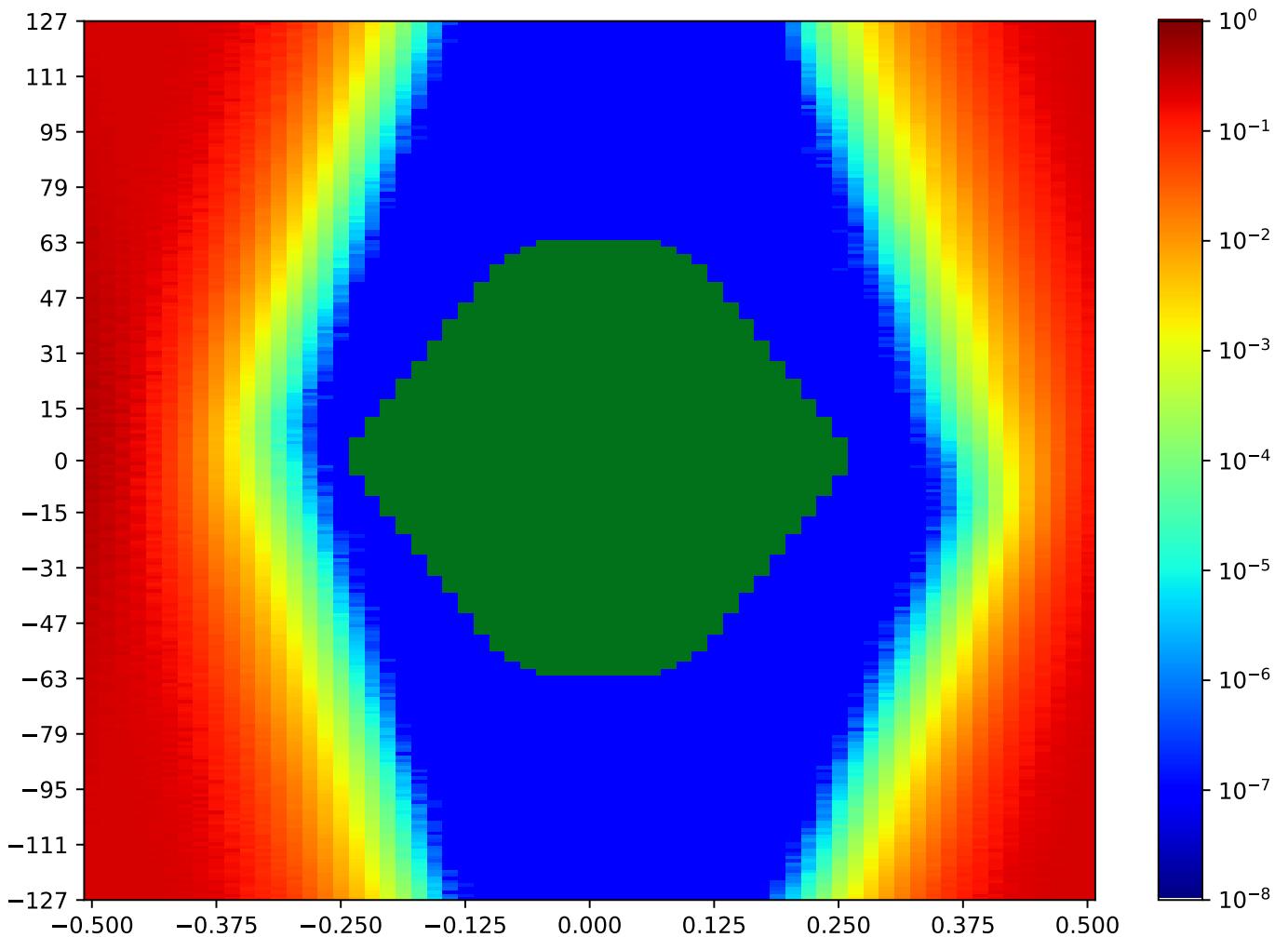


Figure 3.26: MSP_A_FPGA-TX2-11-RX15-11-MSP_C_FPGA

Call back to summary Figure 3.14. Sibling eye diagrams: V1-6.4.

3.3 MSP_C TX3 MSP_A RX7 Minipod Loopback

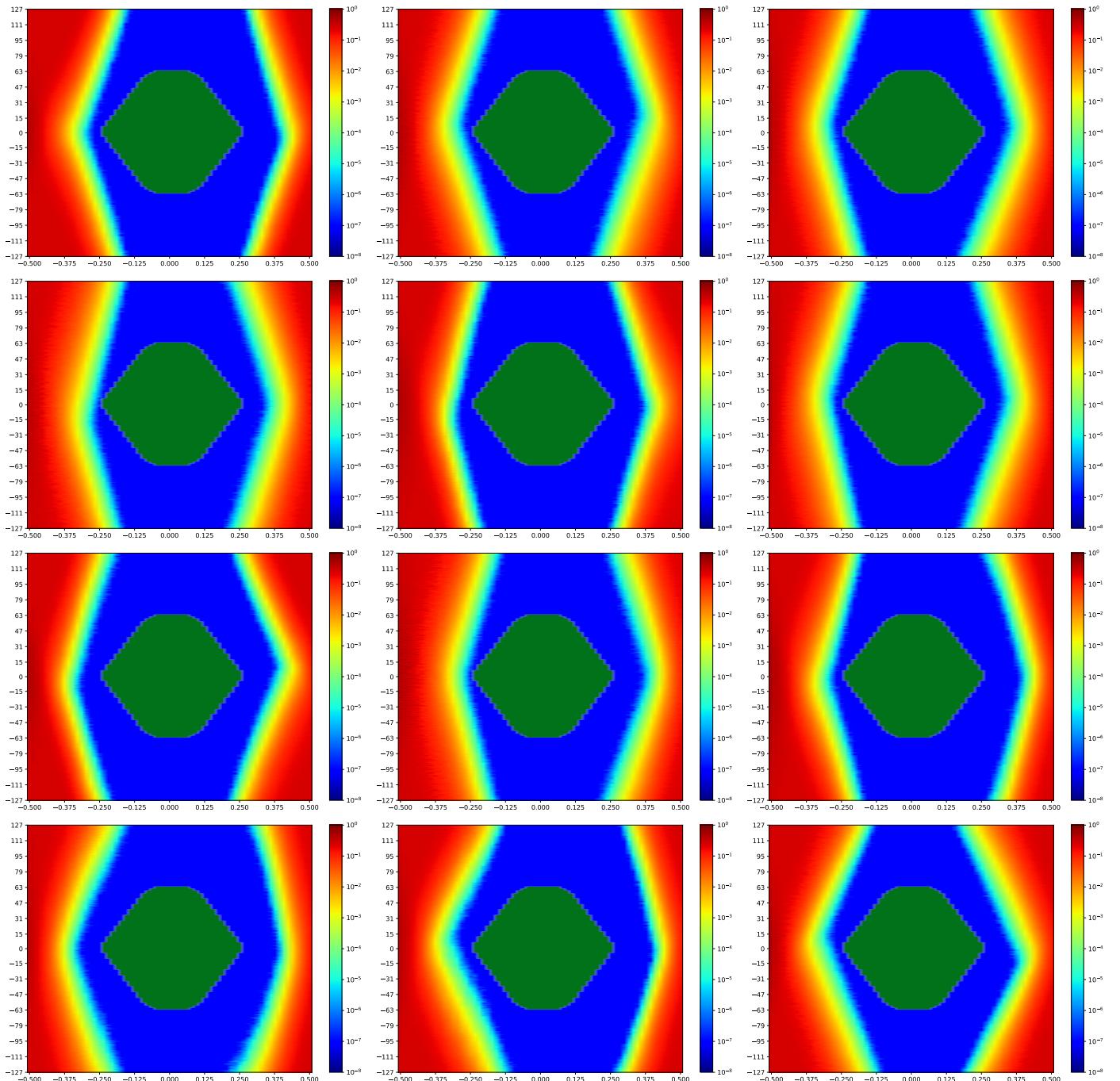


Figure 3.27: MSP_C TX3 MSP_A RX7 Minipod Loopback

A cross-reference to Figure 3.27. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.40.

3.3.1 MSP_C_FPGA-TX3-00-RX7-00-MSP_A_FPGA

Table 3.25: MSP_C_FPGA-TX3-00-RX7-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:37:26		2018-Jan-23 23:37:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8461	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

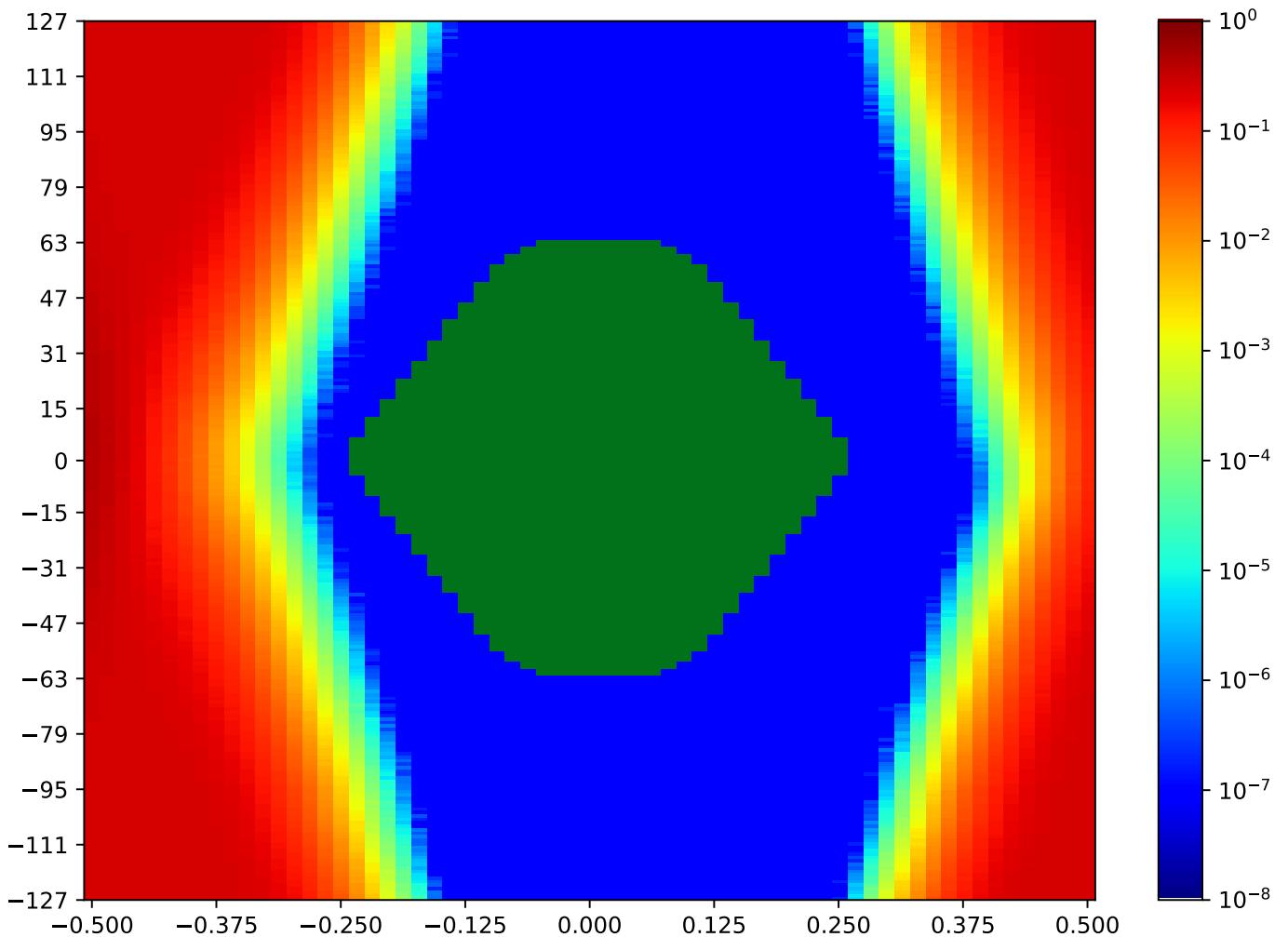


Figure 3.28: MSP_C_FPGA-TX3-00-RX7-00-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.2 MSP_C_FPGA-TX3-01-RX7-01-MSP_A_FPGA

Table 3.26: MSP_C_FPGA-TX3-01-RX7-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:38:07		2018-Jan-23 23:38:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7348	36	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

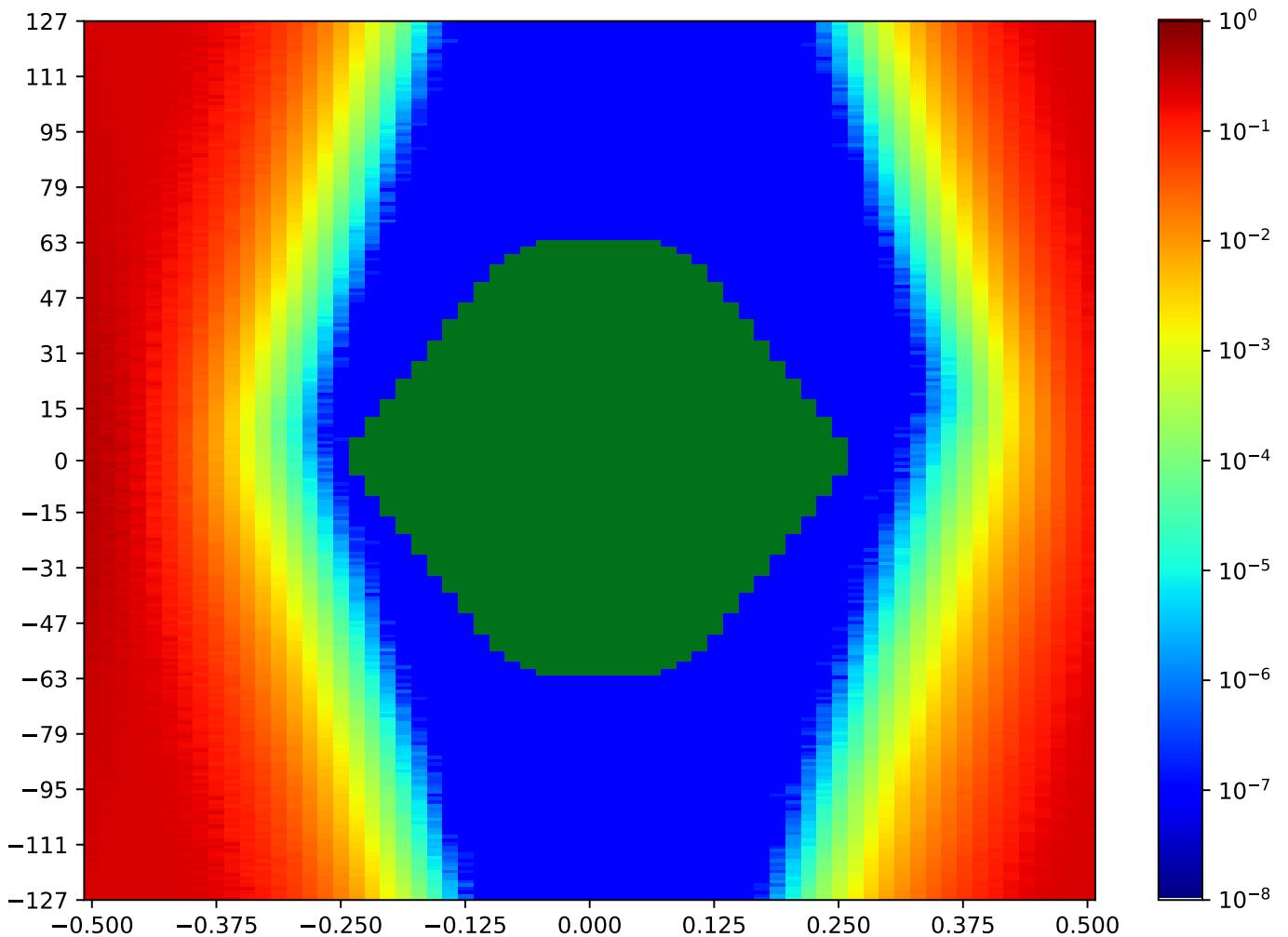


Figure 3.29: MSP_C_FPGA-TX3-01-RX7-01-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.3 MSP_C_FPGA-TX3-02-RX7-02-MSP_A_FPGA

Table 3.27: MSP_C_FPGA-TX3-02-RX7-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:38:27		2018-Jan-23 23:38:47	
Reset RX	OA	HO		HO (%)	
true	7455	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

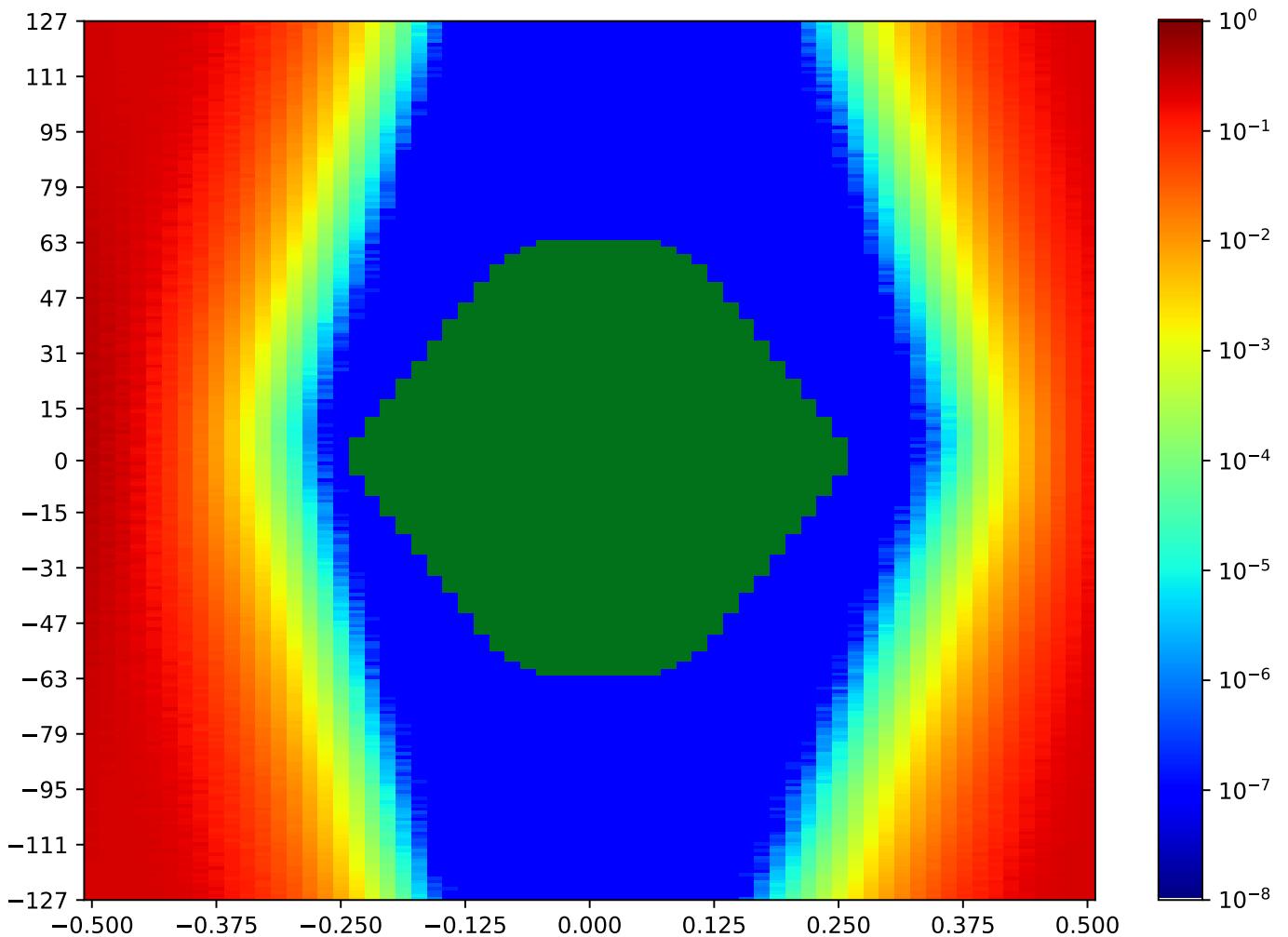


Figure 3.30: MSP_C_FPGA-TX3-02-RX7-02-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.4 MSP_C_FPGA-TX3-03-RX7-03-MSP_A_FPGA

Table 3.28: MSP_C_FPGA-TX3-03-RX7-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:36:45		2018-Jan-23 23:37:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7479	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

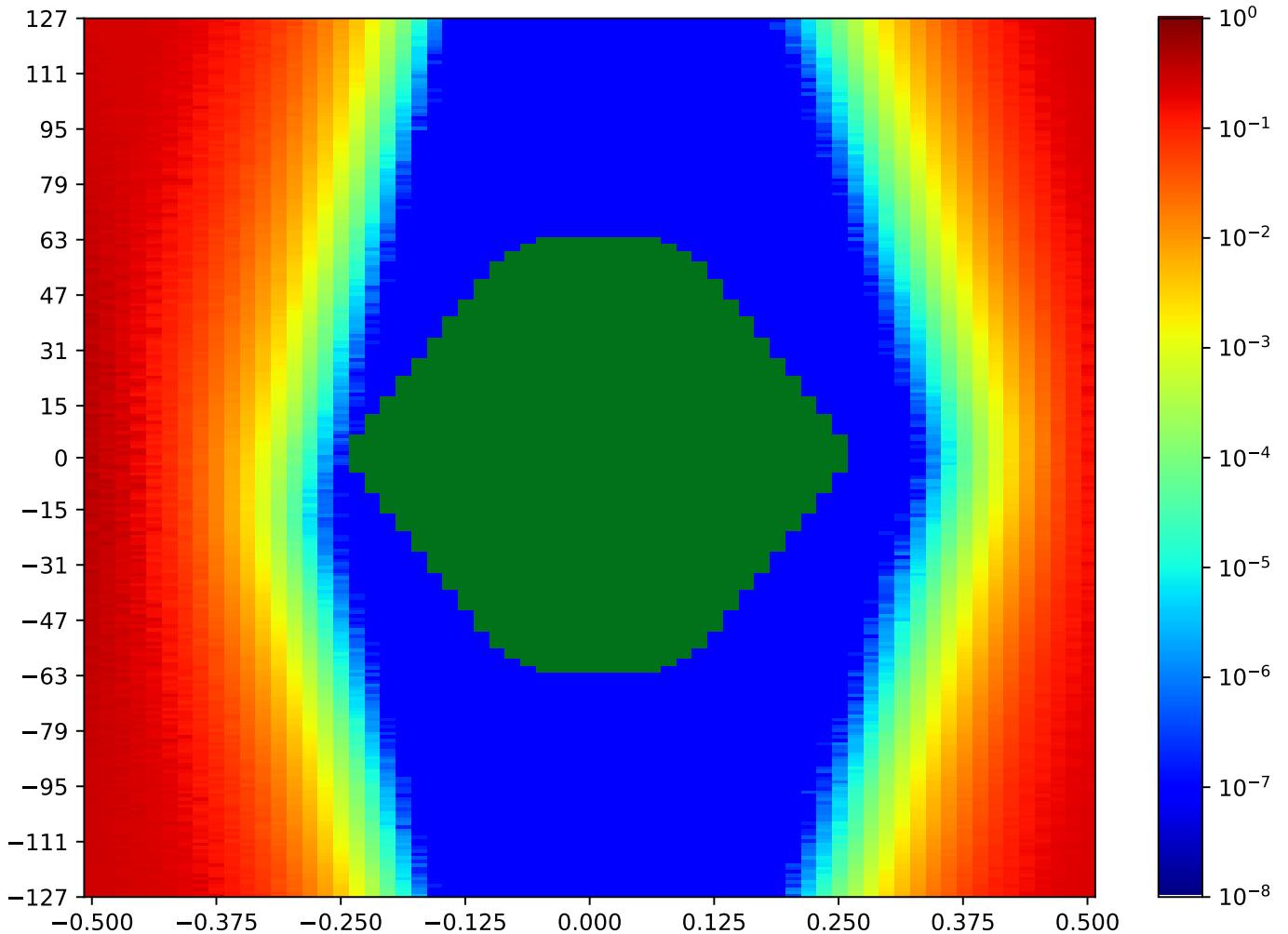


Figure 3.31: MSP_C_FPGA-TX3-03-RX7-03-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.5 MSP_C_FPGA-TX3-04-RX7-04-MSP_A_FPGA

Table 3.29: MSP_C_FPGA-TX3-04-RX7-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:39:28		2018-Jan-23 23:39:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8625	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

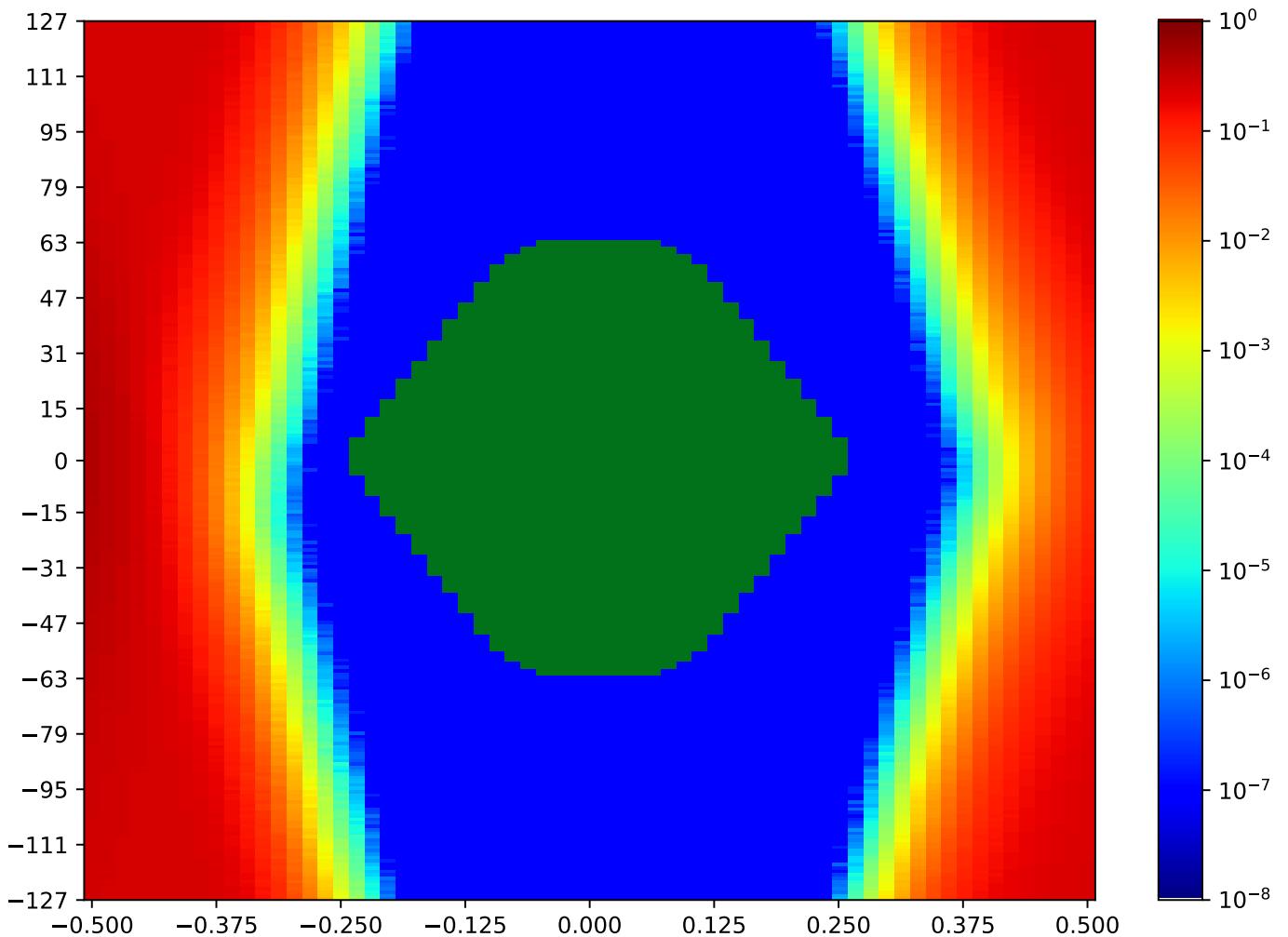


Figure 3.32: MSP_C_FPGA-TX3-04-RX7-04-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.6 MSP_C_FPGA-TX3-05-RX7-05-MSP_A_FPGA

Table 3.30: MSP_C_FPGA-TX3-05-RX7-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:36:24		2018-Jan-23 23:36:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7365	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

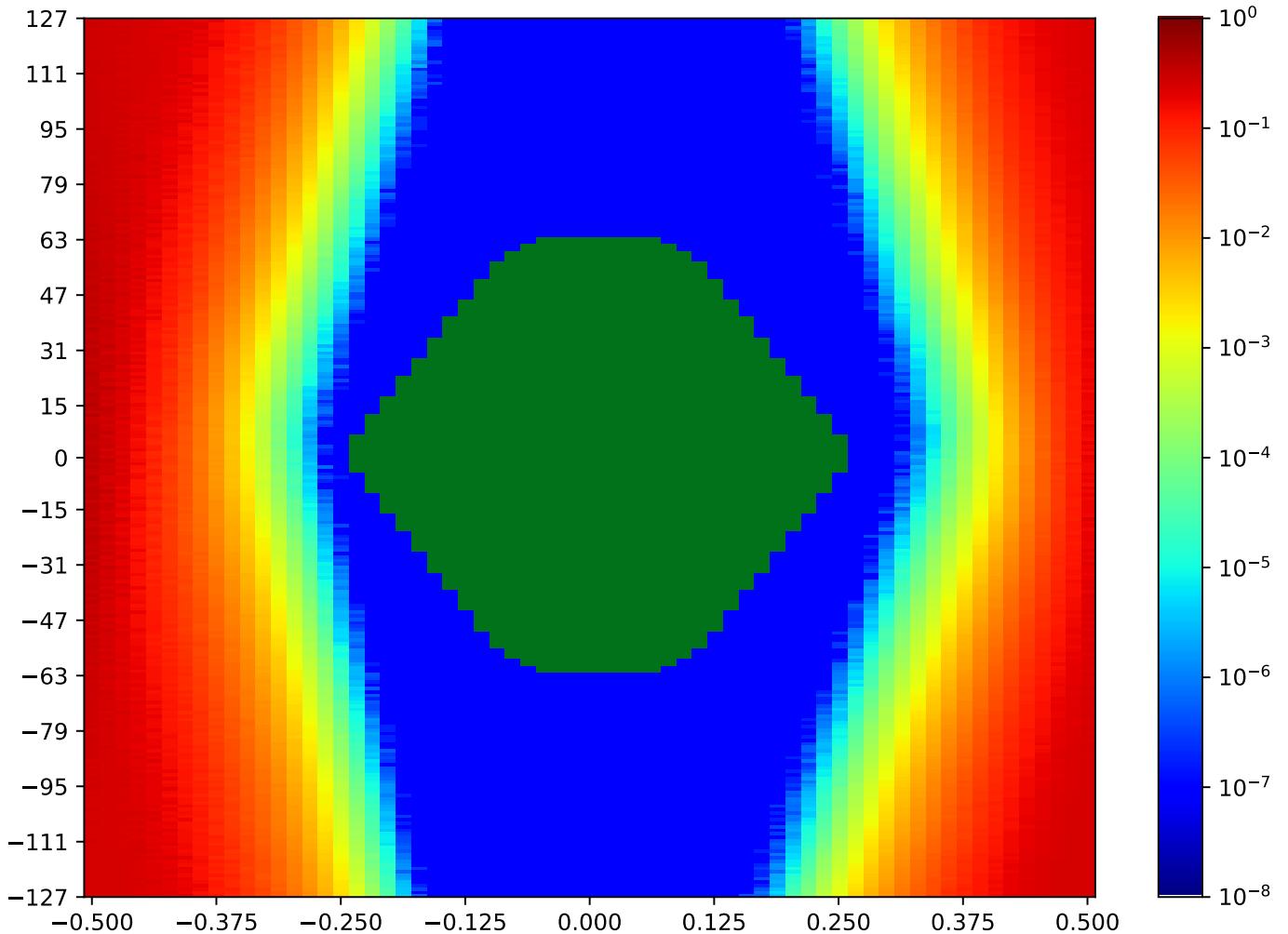


Figure 3.33: MSP_C_FPGA-TX3-05-RX7-05-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.7 MSP_C_FPGA-TX3-06-RX7-06-MSP_A_FPGA

Table 3.31: MSP_C_FPGA-TX3-06-RX7-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:40:08		2018-Jan-23 23:40:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8644	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

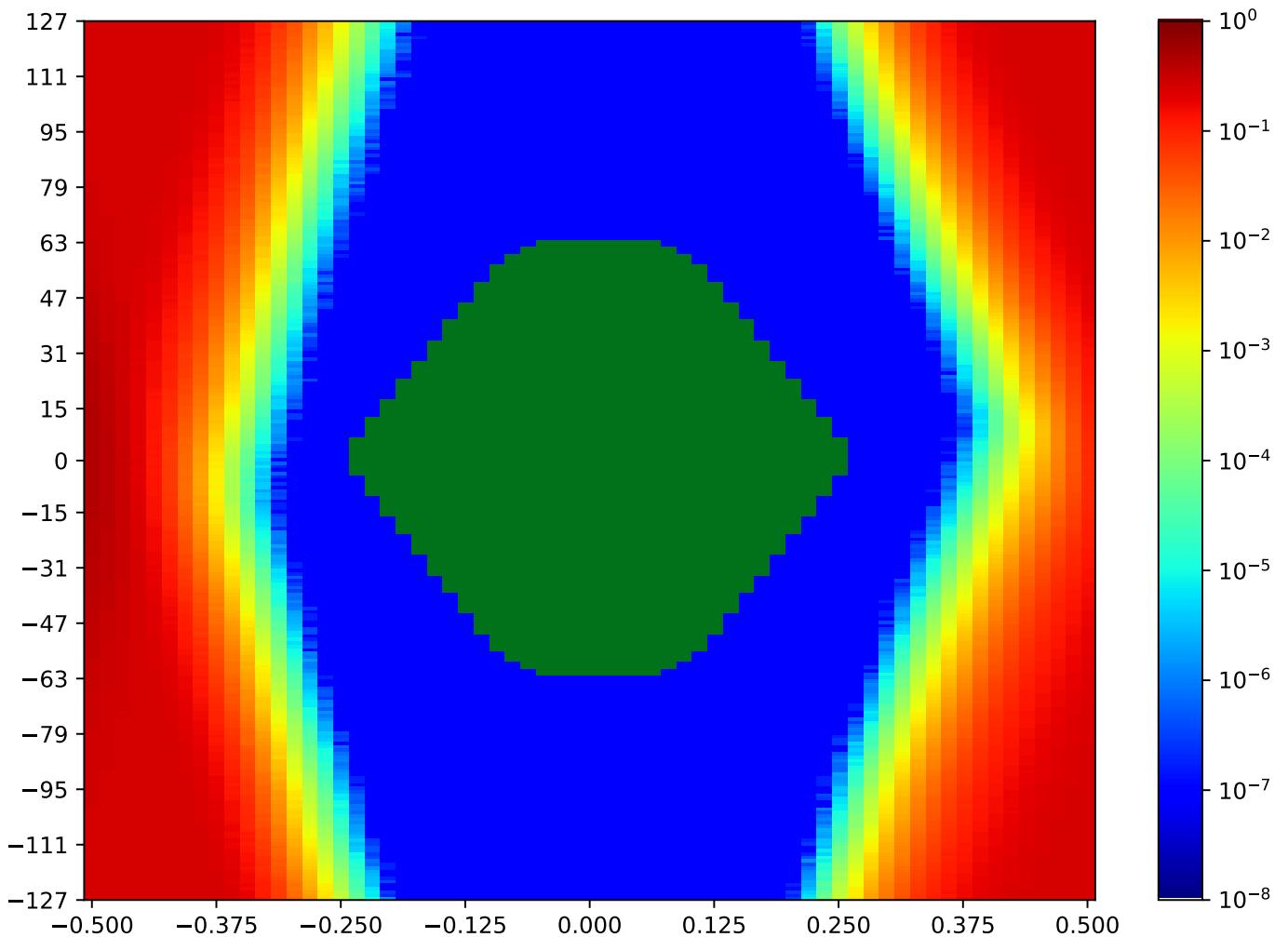


Figure 3.34: MSP_C_FPGA-TX3-06-RX7-06-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.8 MSP_C_FPGA-TX3-07-RX7-07-MSP_A_FPGA

Table 3.32: MSP_C_FPGA-TX3-07-RX7-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:37:06		2018-Jan-23 23:37:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7651	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

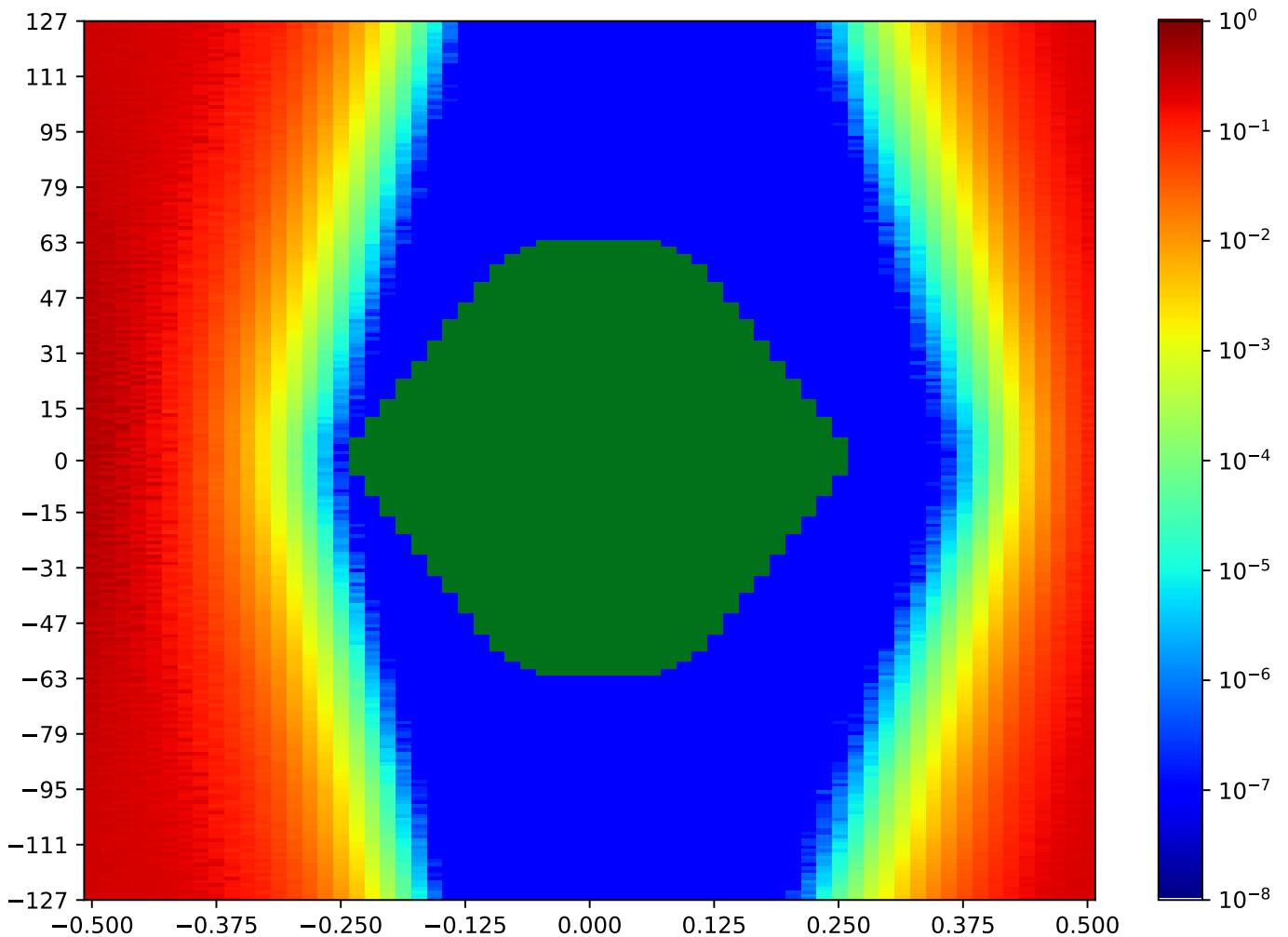


Figure 3.35: MSP_C_FPGA-TX3-07-RX7-07-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.9 MSP_C_FPGA-TX3-08-RX7-08-MSP_A_FPGA

Table 3.33: MSP_C_FPGA-TX3-08-RX7-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:39:48		2018-Jan-23 23:40:08	
Reset RX	OA	HO		HO (%)	
true	8655	42		64.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

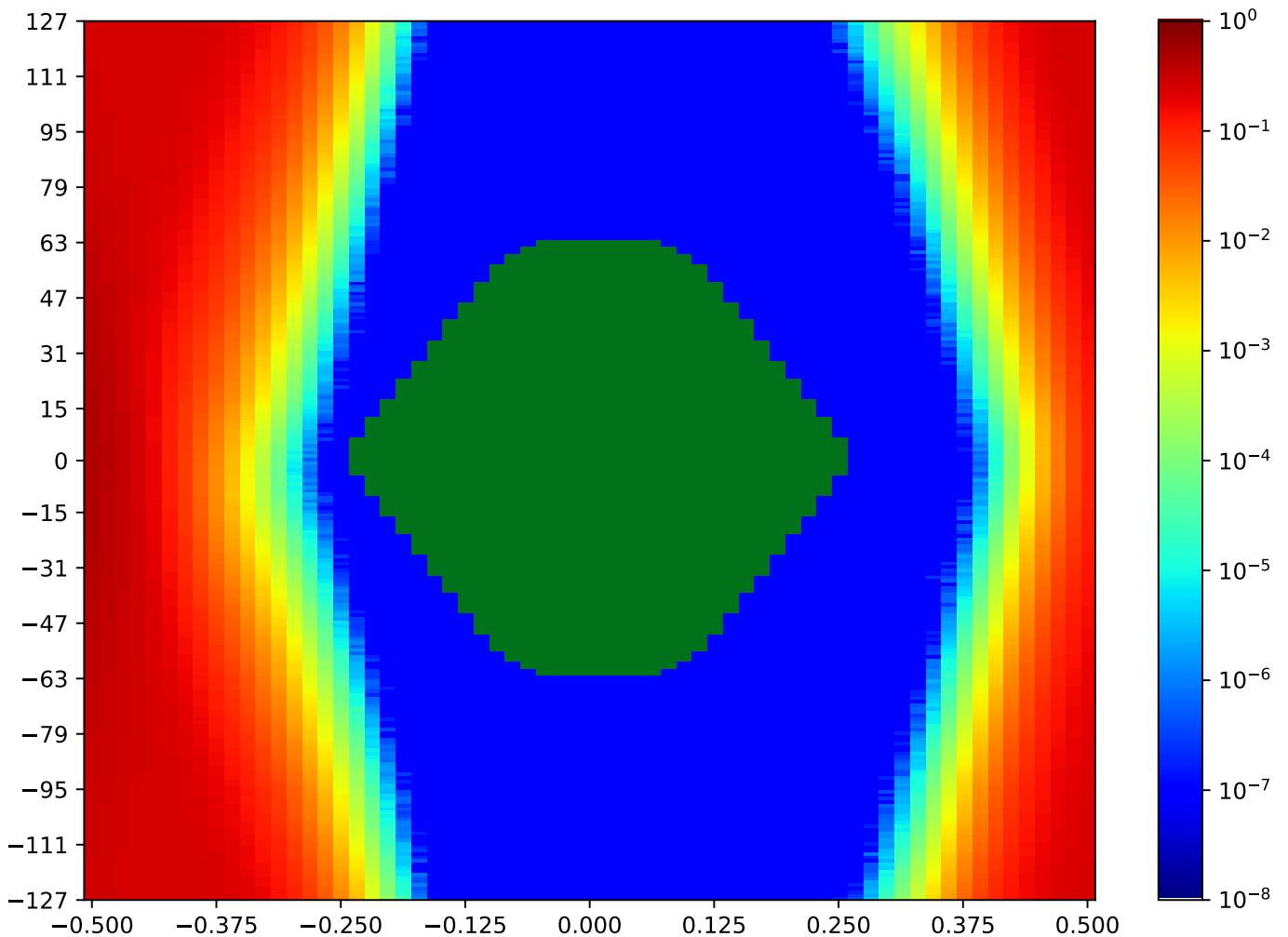


Figure 3.36: MSP_C_FPGA-TX3-08-RX7-08-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.10 MSP_C_FPGA-TX3-09-RX7-09-MSP_A_FPGA

Table 3.34: MSP_C_FPGA-TX3-09-RX7-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:37:46		2018-Jan-23 23:38:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8835	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

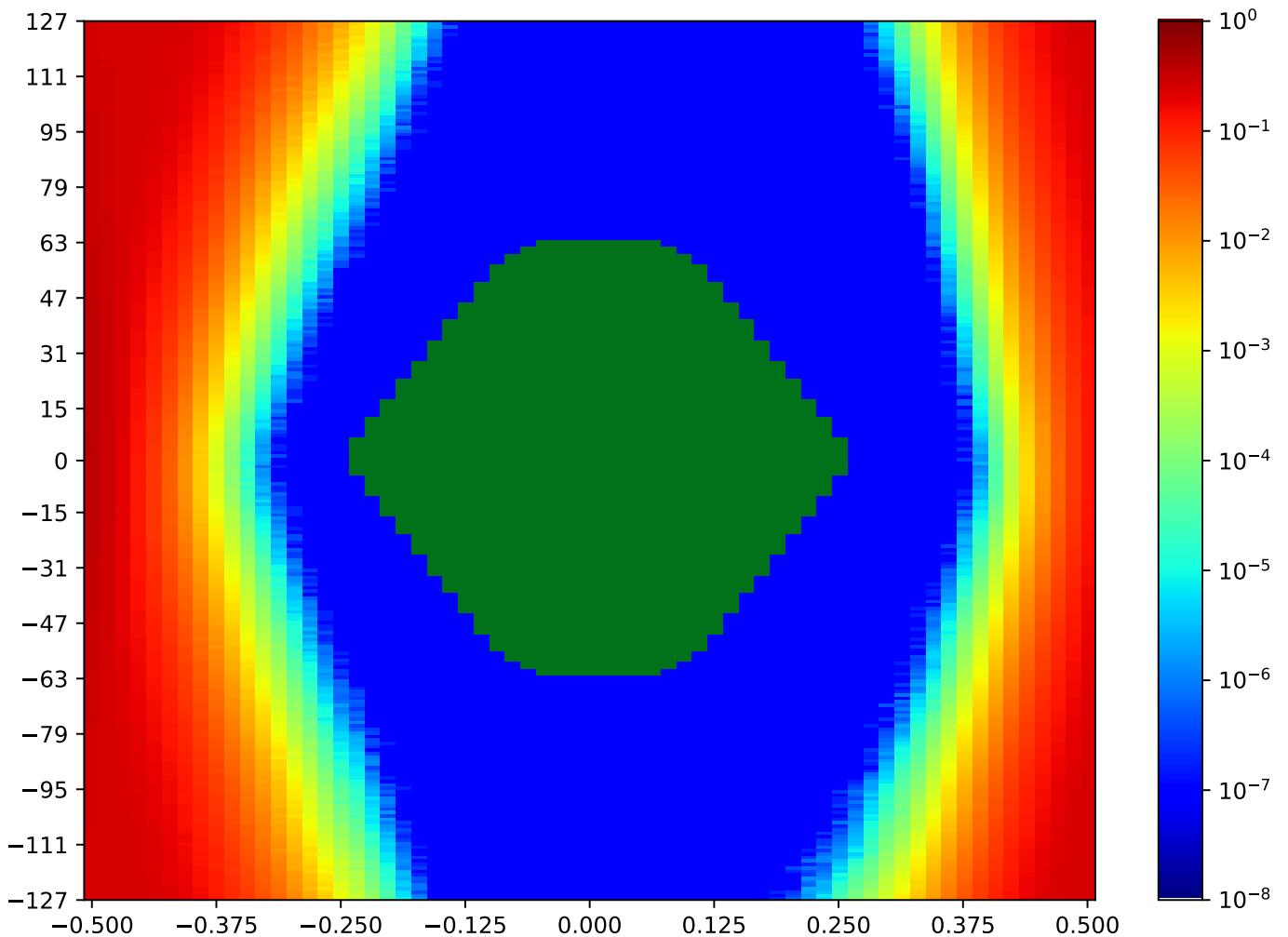


Figure 3.37: MSP_C_FPGA-TX3-09-RX7-09-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.11 MSP_C_FPGA-TX3-10-RX7-10-MSP_A_FPGA

Table 3.35: MSP_C_FPGA-TX3-10-RX7-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:39:07		2018-Jan-23 23:39:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8522	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

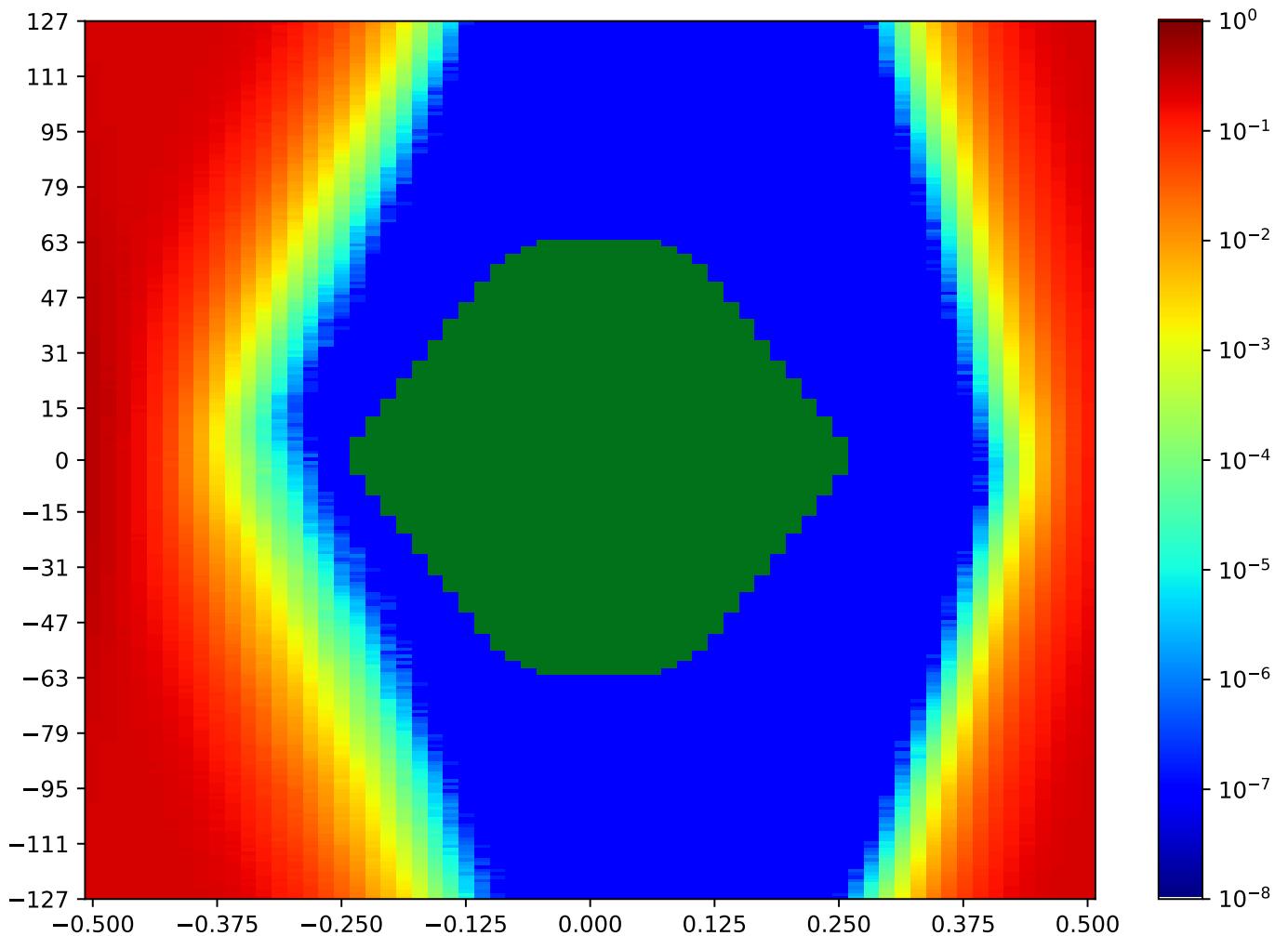


Figure 3.38: MSP_C_FPGA-TX3-10-RX7-10-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.3.12 MSP_C_FPGA-TX3-11-RX7-11-MSP_A_FPGA

Table 3.36: MSP_C_FPGA-TX3-11-RX7-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:38:47		2018-Jan-23 23:39:07	
Reset RX	OA	HO		HO (%)	
true	7328	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

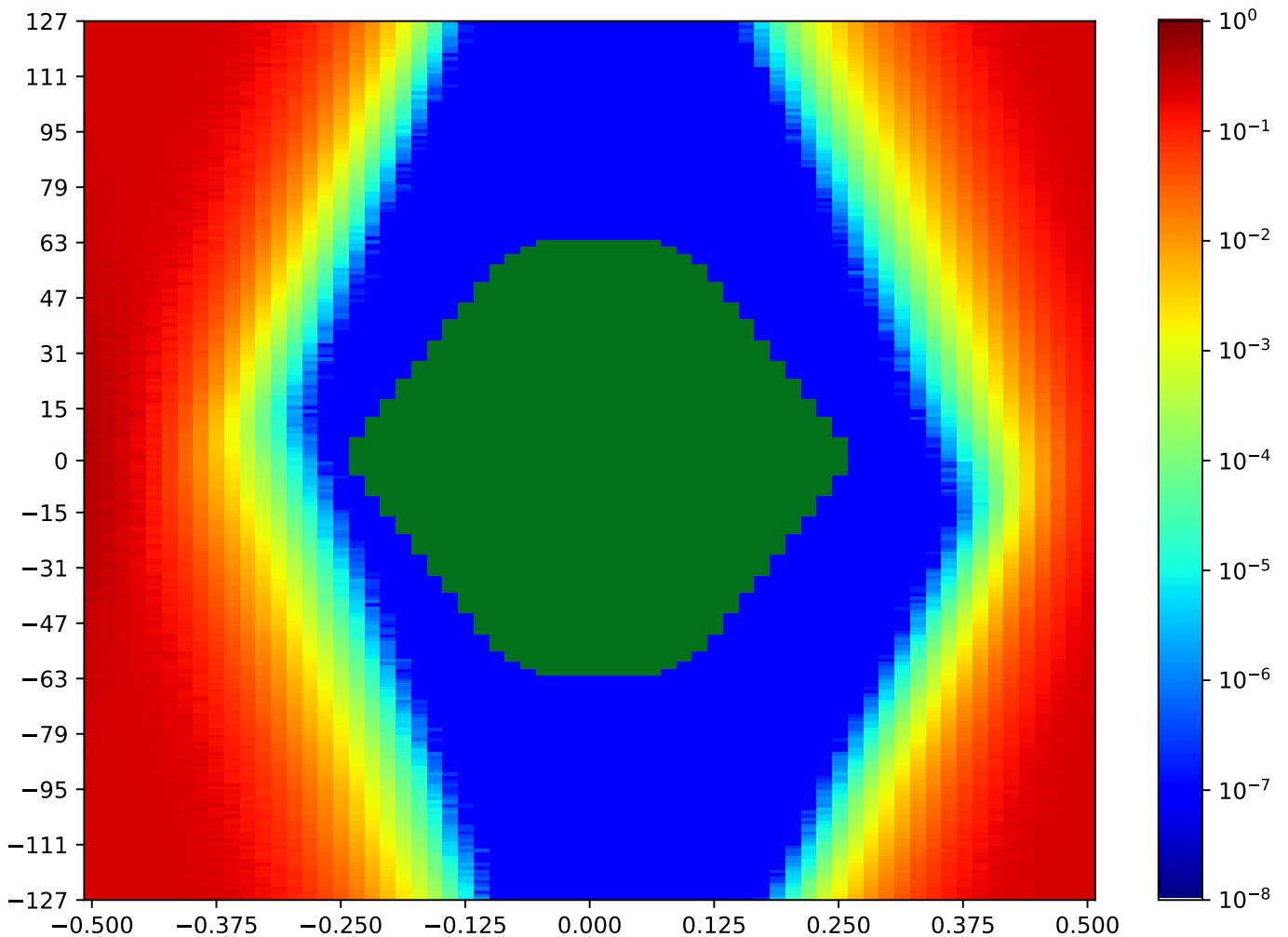


Figure 3.39: MSP_C_FPGA-TX3-11-RX7-11-MSP_A_FPGA

Call back to summary Figure 3.27. Sibling eye diagrams: V1-6.4.

3.4 MSP_C TX4 MSP_A RX6 Minipod Loopback

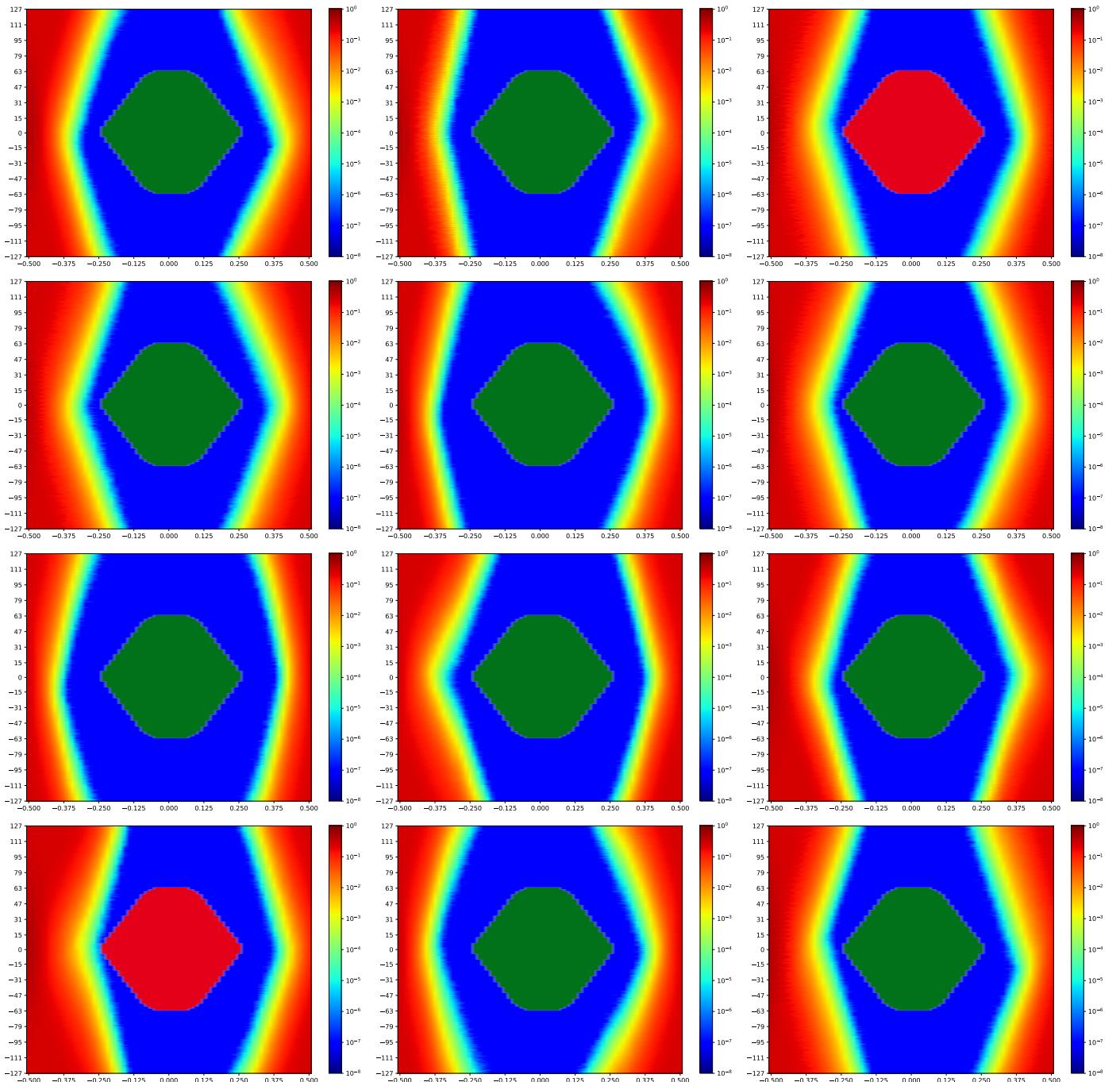


Figure 3.40: MSP_C TX4 MSP_A RX6 Minipod Loopback

A cross-reference to Figure 3.40. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.53.

3.4.1 MSP_C_FPGA-TX4-00-RX6-00-MSP_A_FPGA

Table 3.37: MSP_C_FPGA-TX4-00-RX6-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:41:29		2018-Jan-23 23:41:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8049	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

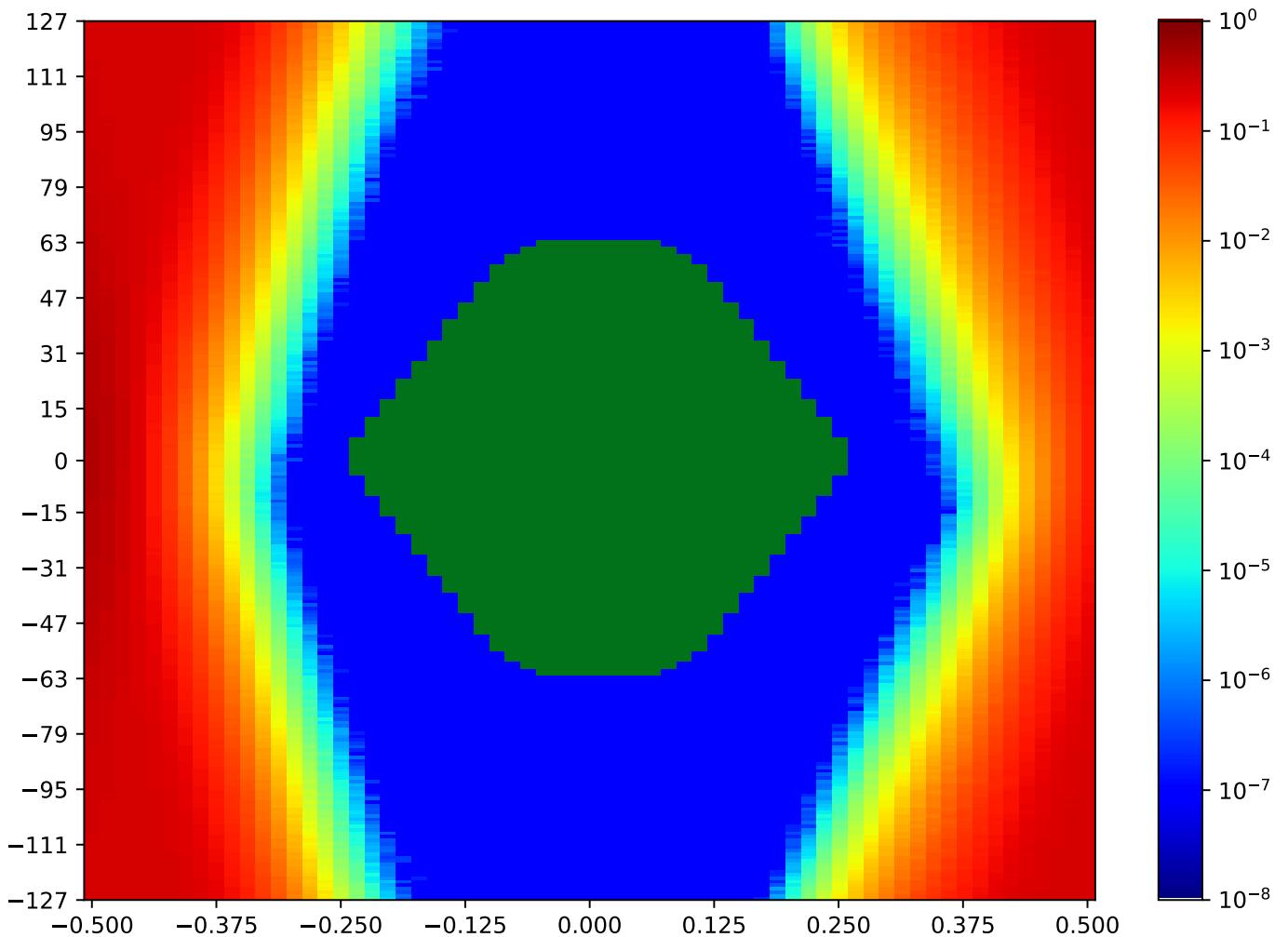


Figure 3.41: MSP_C_FPGA-TX4-00-RX6-00-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.2 MSP_C_FPGA-TX4-01-RX6-01-MSP_A_FPGA

Table 3.38: MSP_C_FPGA-TX4-01-RX6-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:40:49		2018-Jan-23 23:41:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8514	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

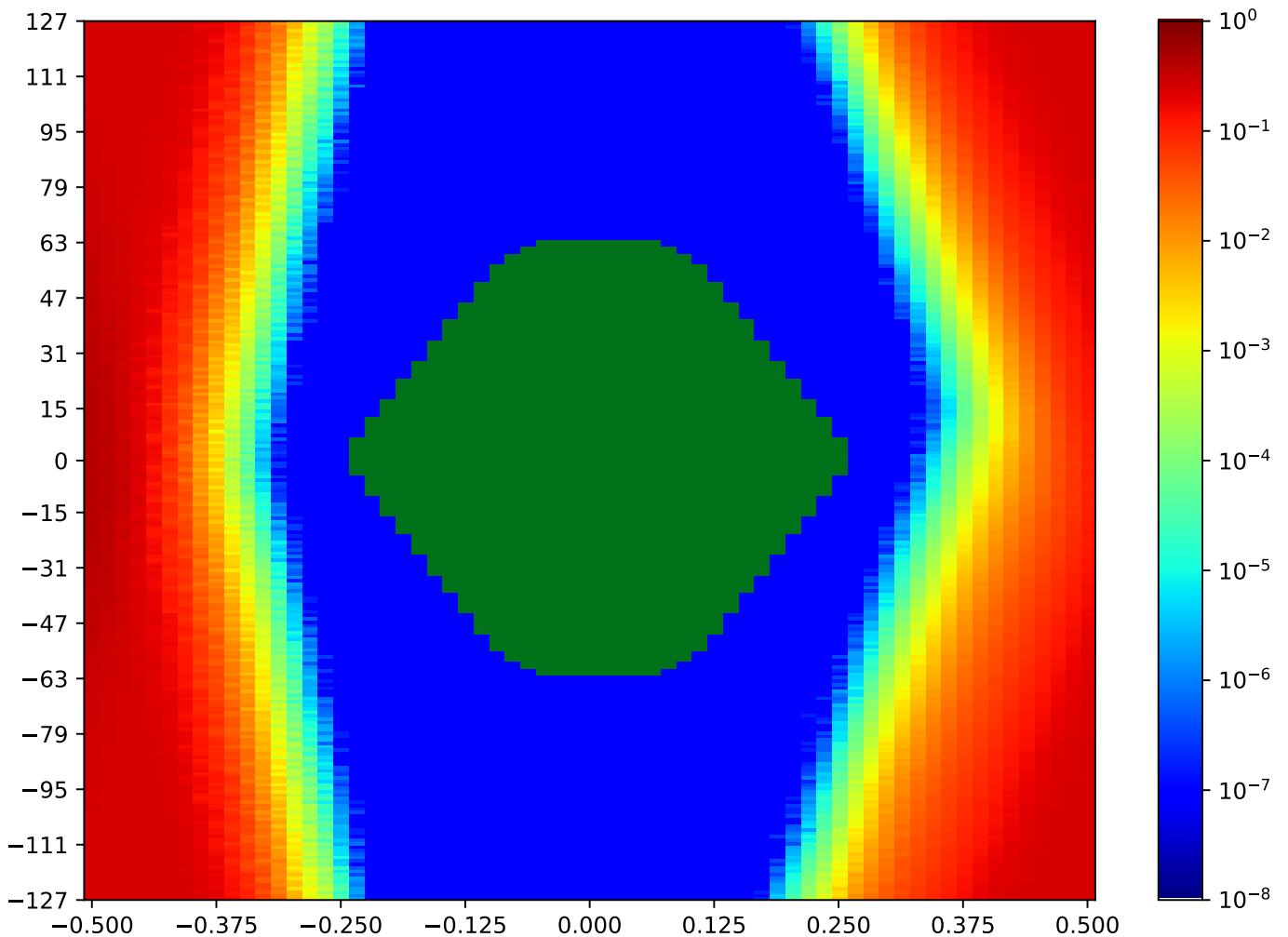


Figure 3.42: MSP_C_FPGA-TX4-01-RX6-01-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.3 MSP_C_FPGA-TX4-02-RX6-02-MSP_A_FPGA

Table 3.39: MSP_C_FPGA-TX4-02-RX6-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:42:30		2018-Jan-23 23:42:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7417	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

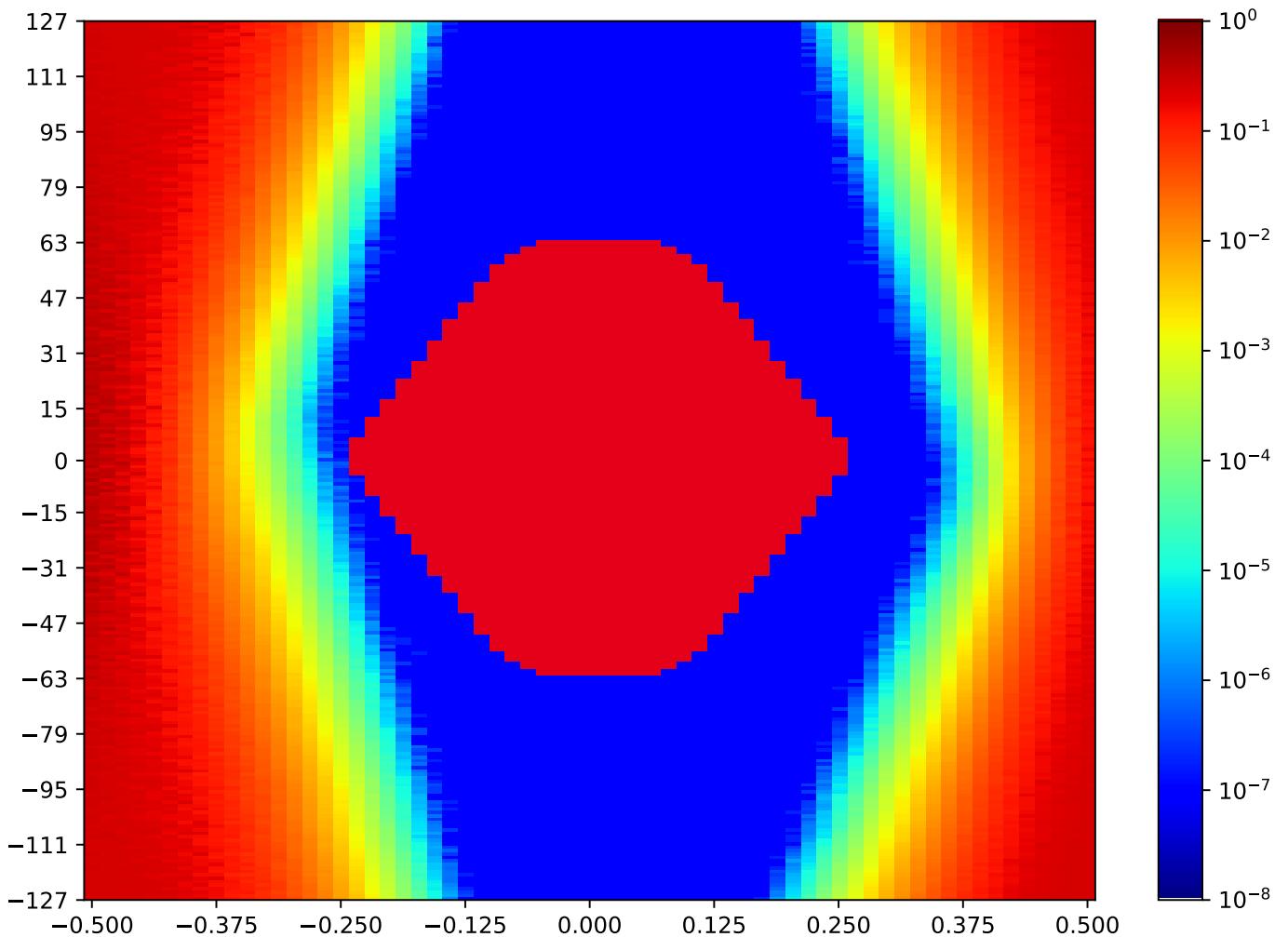


Figure 3.43: MSP_C_FPGA-TX4-02-RX6-02-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.4 MSP_C_FPGA-TX4-03-RX6-03-MSP_A_FPGA

Table 3.40: MSP_C_FPGA-TX4-03-RX6-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:40:29		2018-Jan-23 23:40:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7328	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

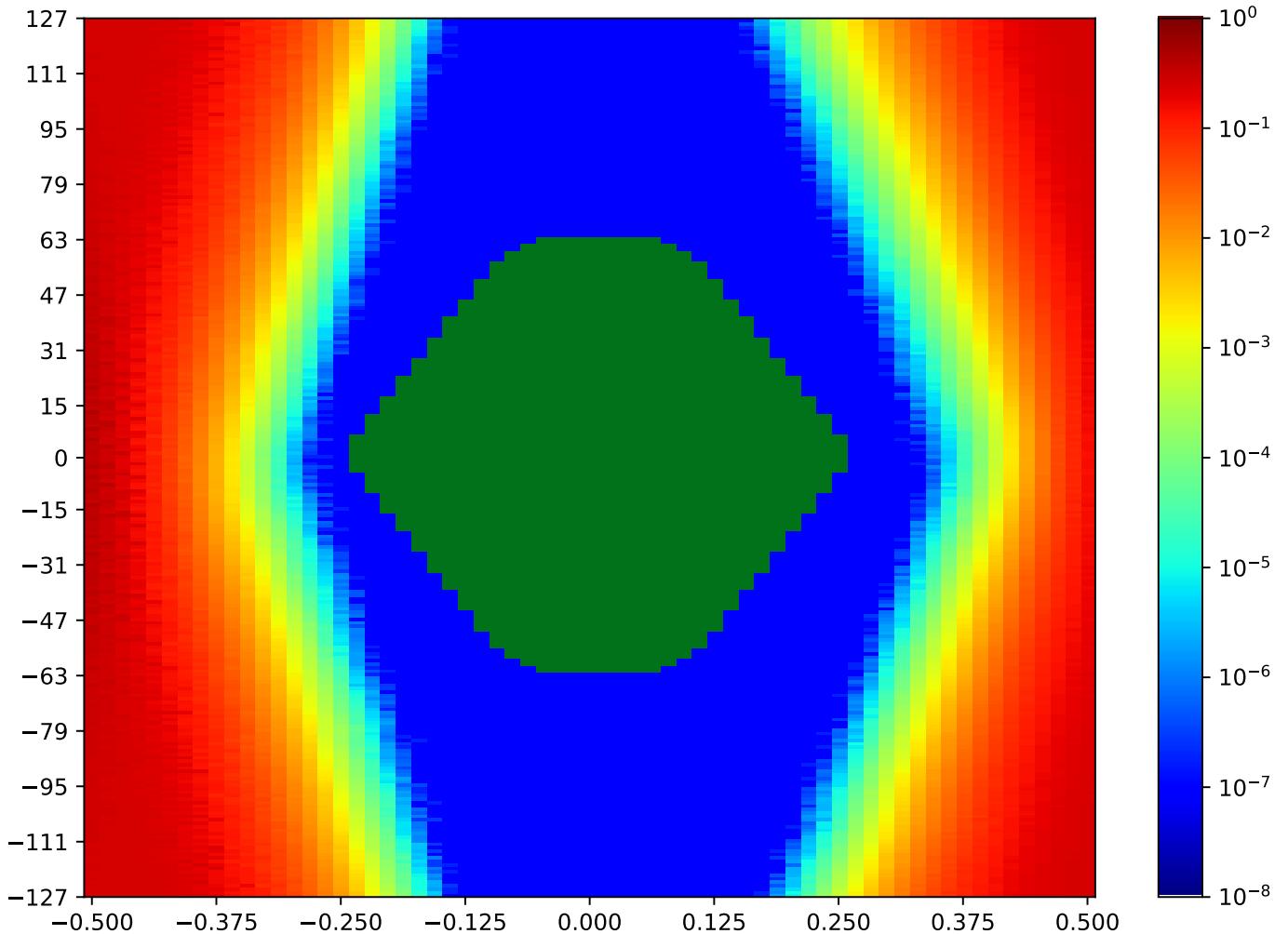


Figure 3.44: MSP_C_FPGA-TX4-03-RX6-03-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.5 MSP_C_FPGA-TX4-04-RX6-04-MSP_A_FPGA

Table 3.41: MSP_C_FPGA-TX4-04-RX6-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:43:31		2018-Jan-23 23:43:51	
Reset RX	OA	HO		HO (%)	
true	9465	46		70.77%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

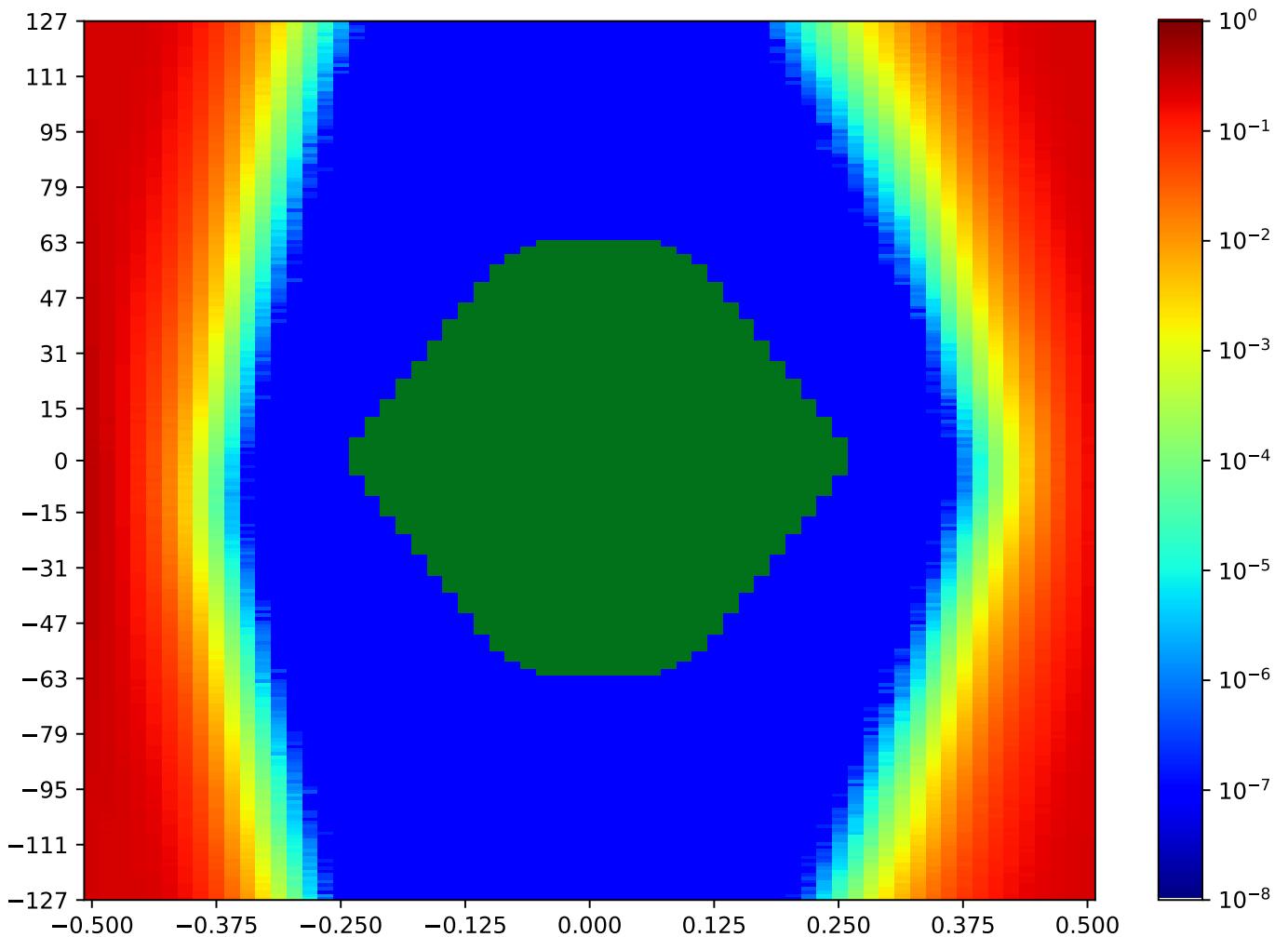


Figure 3.45: MSP_C_FPGA-TX4-04-RX6-04-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.6 MSP_C_FPGA-TX4-05-RX6-05-MSP_A_FPGA

Table 3.42: MSP_C_FPGA-TX4-05-RX6-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:41:09		2018-Jan-23 23:41:29	
Reset RX	OA	HO		HO (%)	
true	7266	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

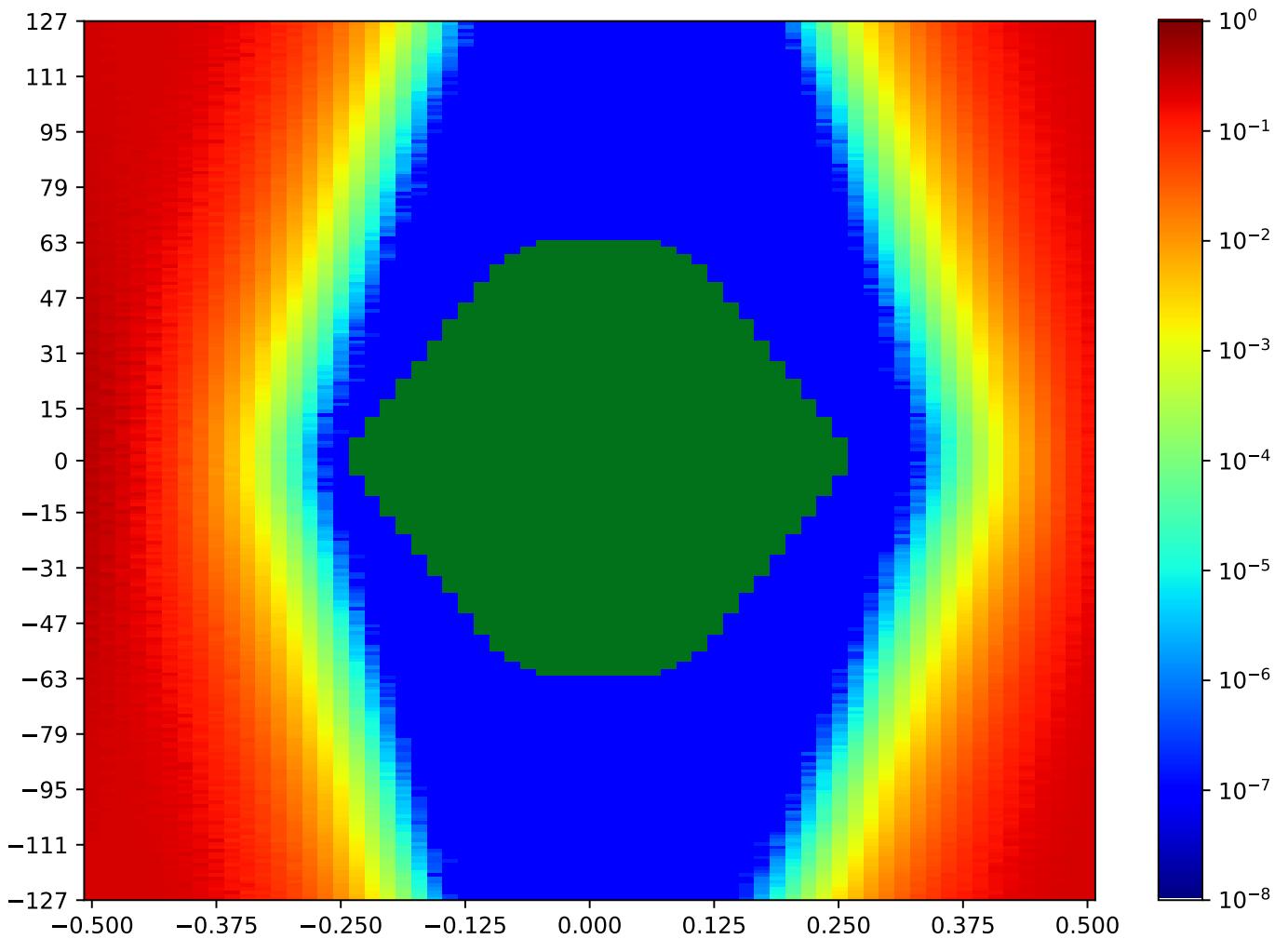


Figure 3.46: MSP_C_FPGA-TX4-05-RX6-05-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.7 MSP_C_FPGA-TX4-06-RX6-06-MSP_A_FPGA

Table 3.43: MSP_C_FPGA-TX4-06-RX6-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:44:12		2018-Jan-23 23:44:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10205	47	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

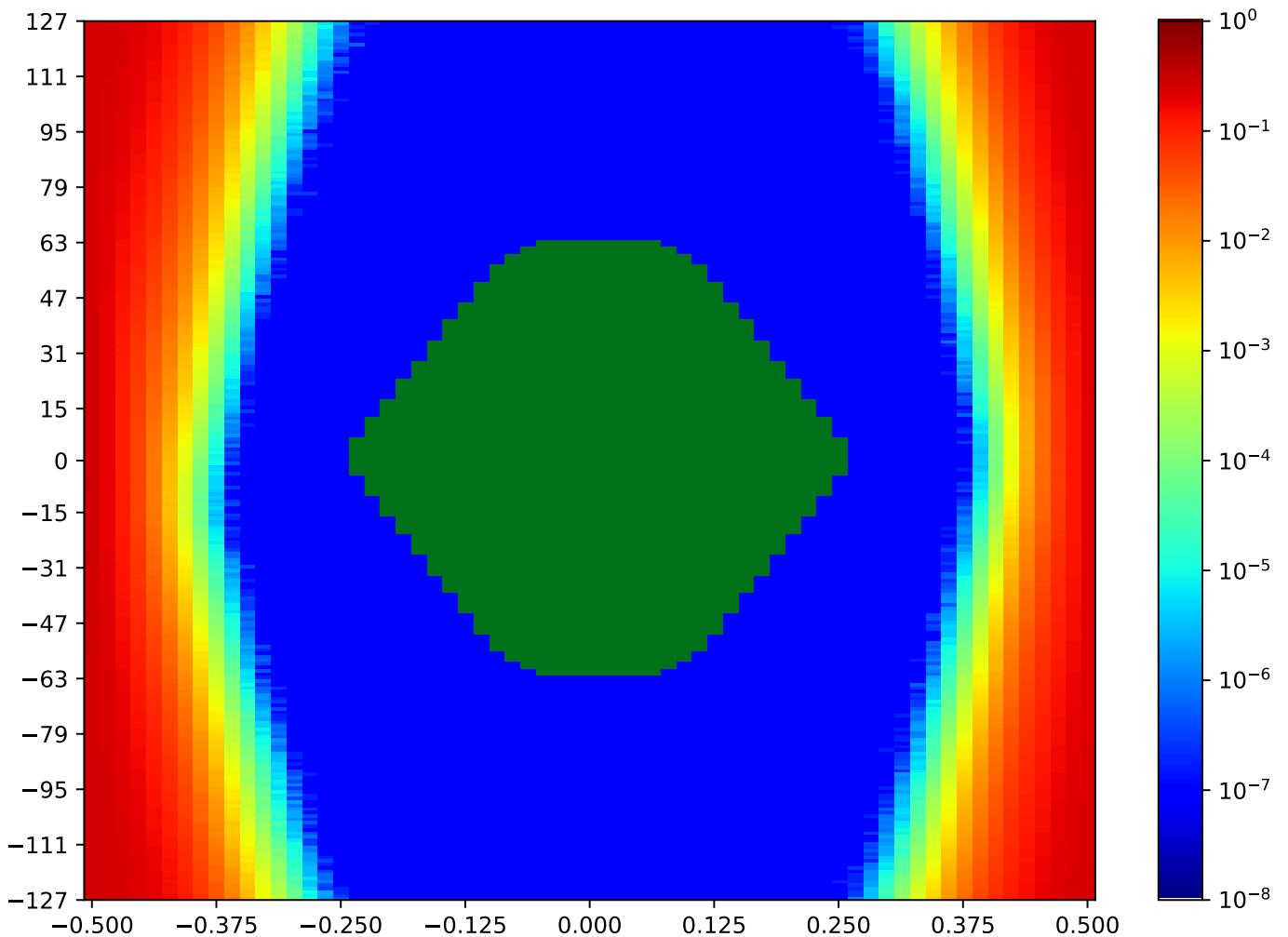


Figure 3.47: MSP_C_FPGA-TX4-06-RX6-06-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.8 MSP_C_FPGA-TX4-07-RX6-07-MSP_A_FPGA

Table 3.44: MSP_C_FPGA-TX4-07-RX6-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:41:49		2018-Jan-23 23:42:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8571	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

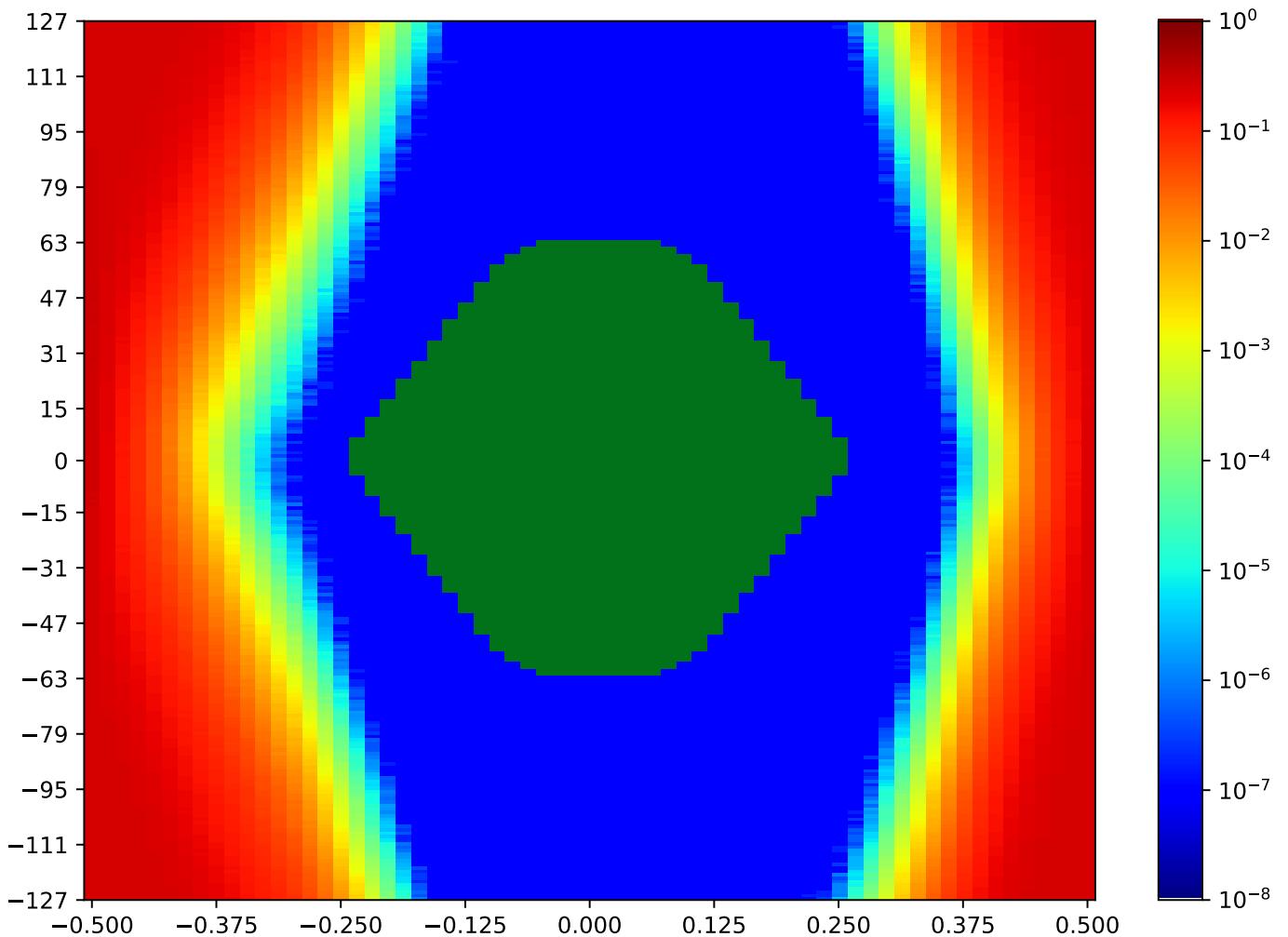


Figure 3.48: MSP_C_FPGA-TX4-07-RX6-07-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.9 MSP_C_FPGA-TX4-08-RX6-08-MSP_A_FPGA

Table 3.45: MSP_C_FPGA-TX4-08-RX6-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:43:52		2018-Jan-23 23:44:12	
Reset RX	OA	HO		HO (%)	
true	7631	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0xC002 SVN: 0	

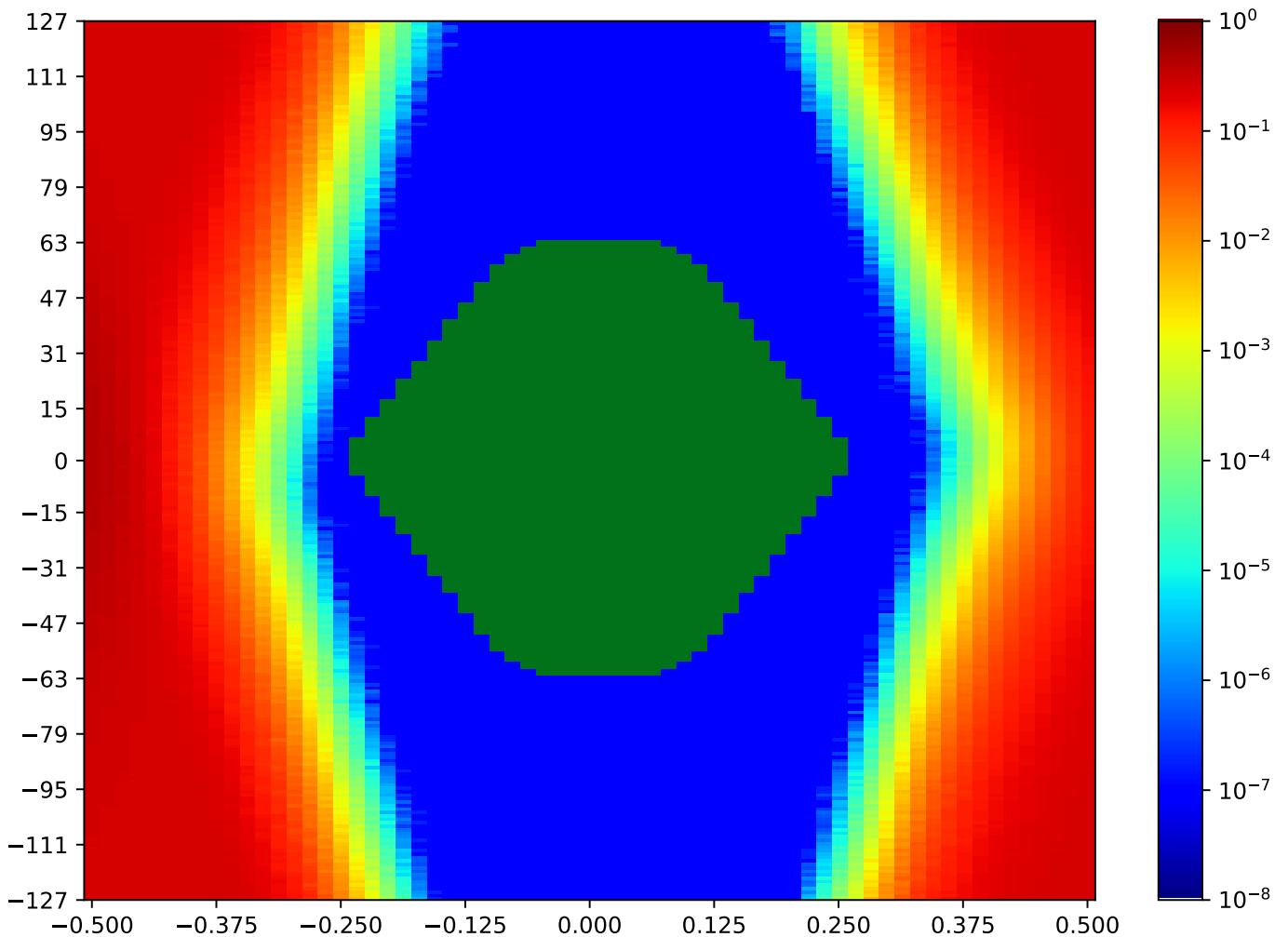


Figure 3.49: MSP_C_FPGA-TX4-08-RX6-08-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.10 MSP_C_FPGA-TX4-09-RX6-09-MSP_A_FPGA

Table 3.46: MSP_C_FPGA-TX4-09-RX6-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:42:10		2018-Jan-23 23:42:30	
Reset RX	OA	HO		HO (%)	
true	7727	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

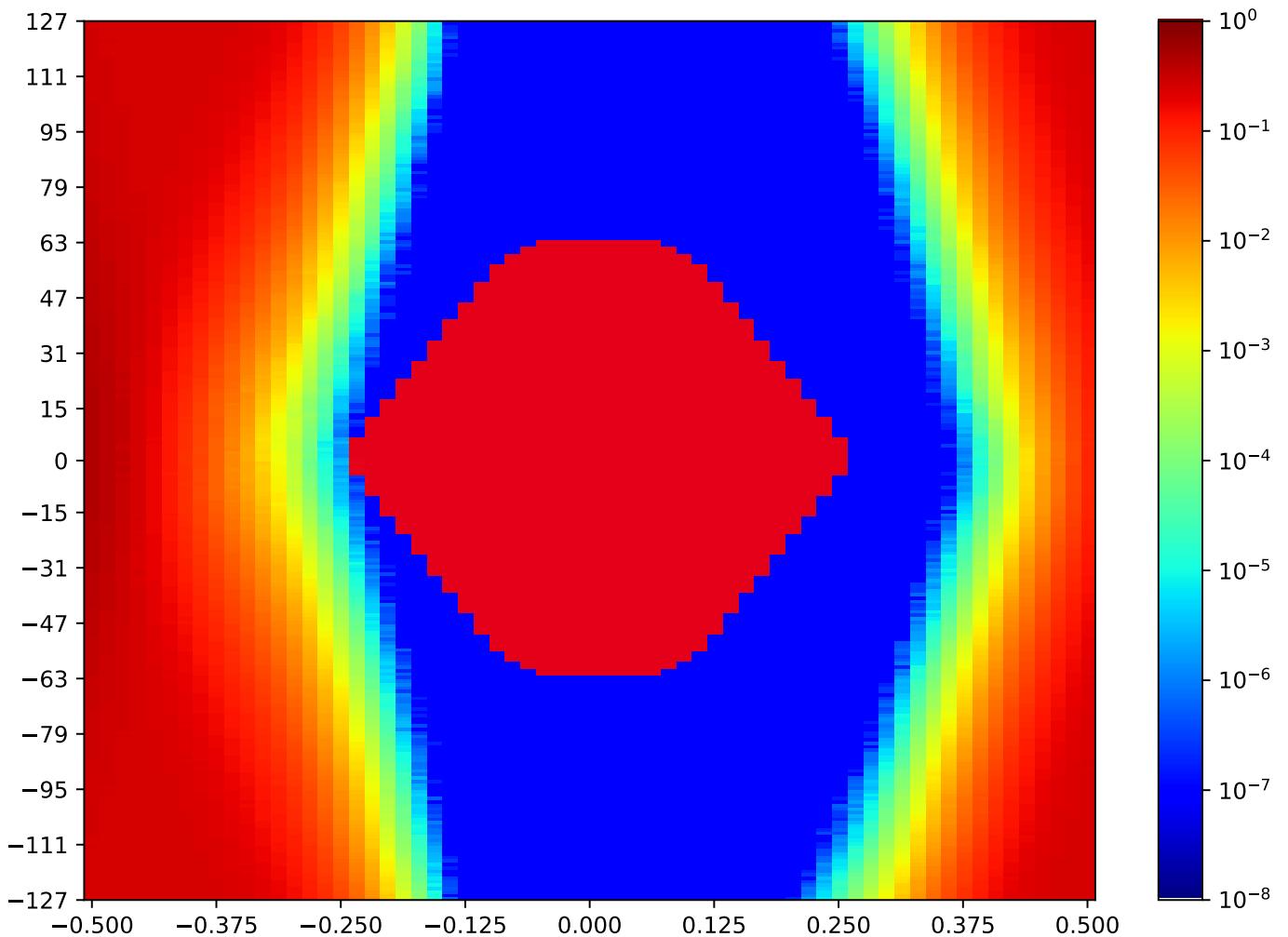


Figure 3.50: MSP_C_FPGA-TX4-09-RX6-09-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.11 MSP_C_FPGA-TX4-10-RX6-10-MSP_A_FPGA

Table 3.47: MSP_C_FPGA-TX4-10-RX6-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:43:11		2018-Jan-23 23:43:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8491	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

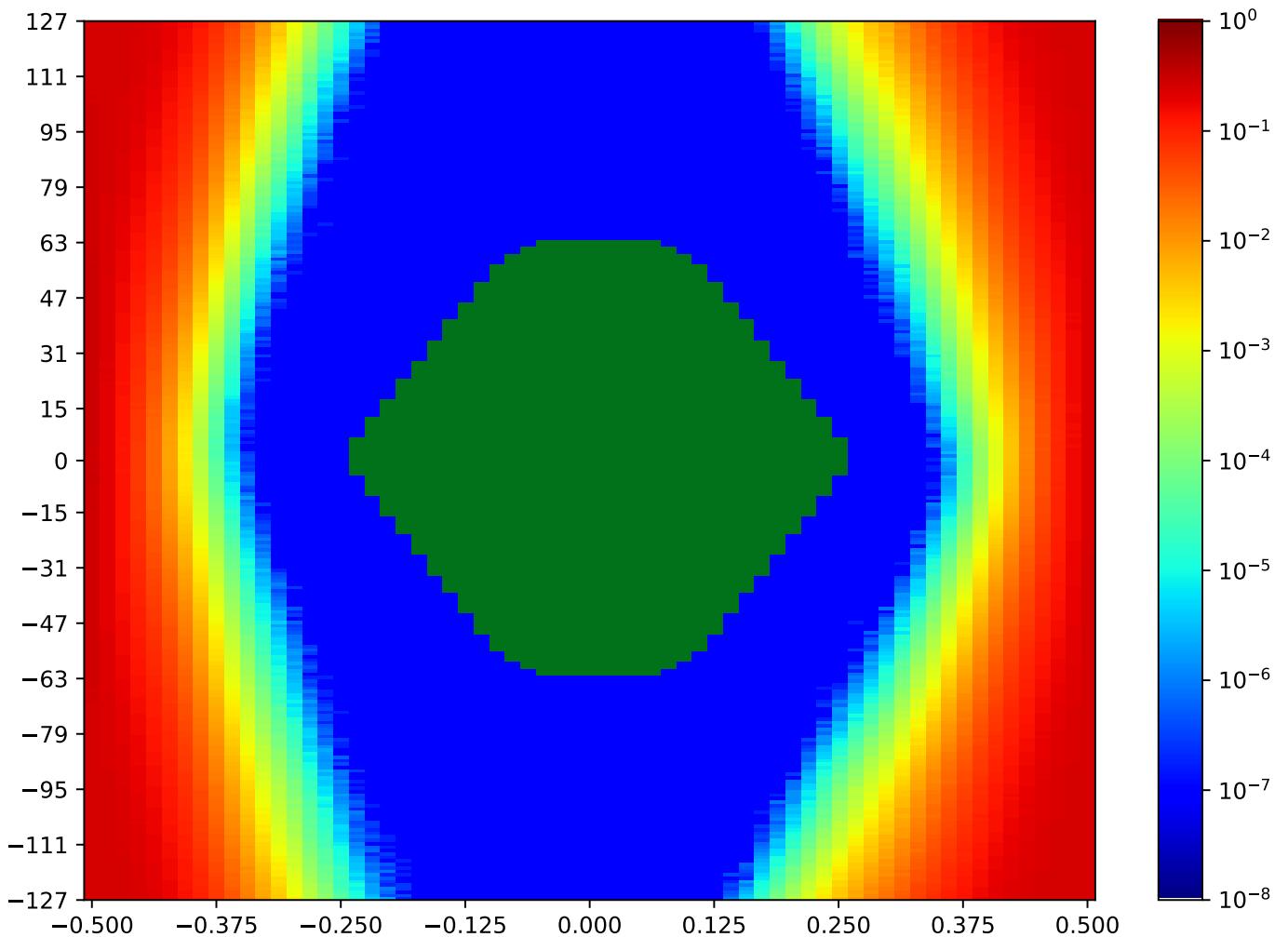


Figure 3.51: MSP_C_FPGA-TX4-10-RX6-10-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.4.12 MSP_C_FPGA-TX4-11-RX6-11-MSP_A_FPGA

Table 3.48: MSP_C_FPGA-TX4-11-RX6-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:42:50		2018-Jan-23 23:43:11	
Reset RX	OA	HO		HO (%)	
true	7853	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

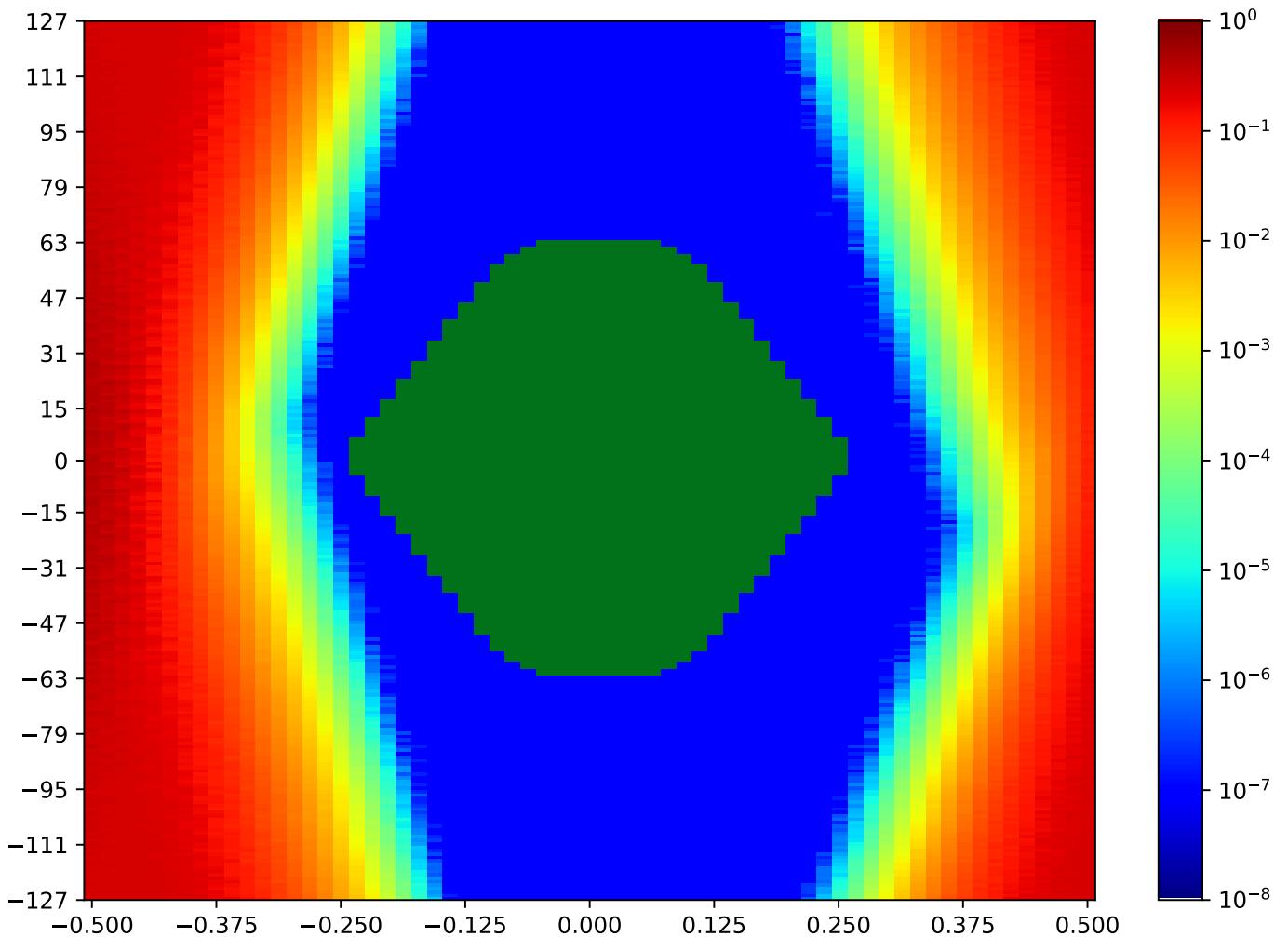


Figure 3.52: MSP_C_FPGA-TX4-11-RX6-11-MSP_A_FPGA

Call back to summary Figure 3.40. Sibling eye diagrams: V1-6.4.

3.5 Partial TRP TX5 MSP_A RX5 Minipod Loopback

A cross-reference to Figure 3.53. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

Next summary Figure 3.62.

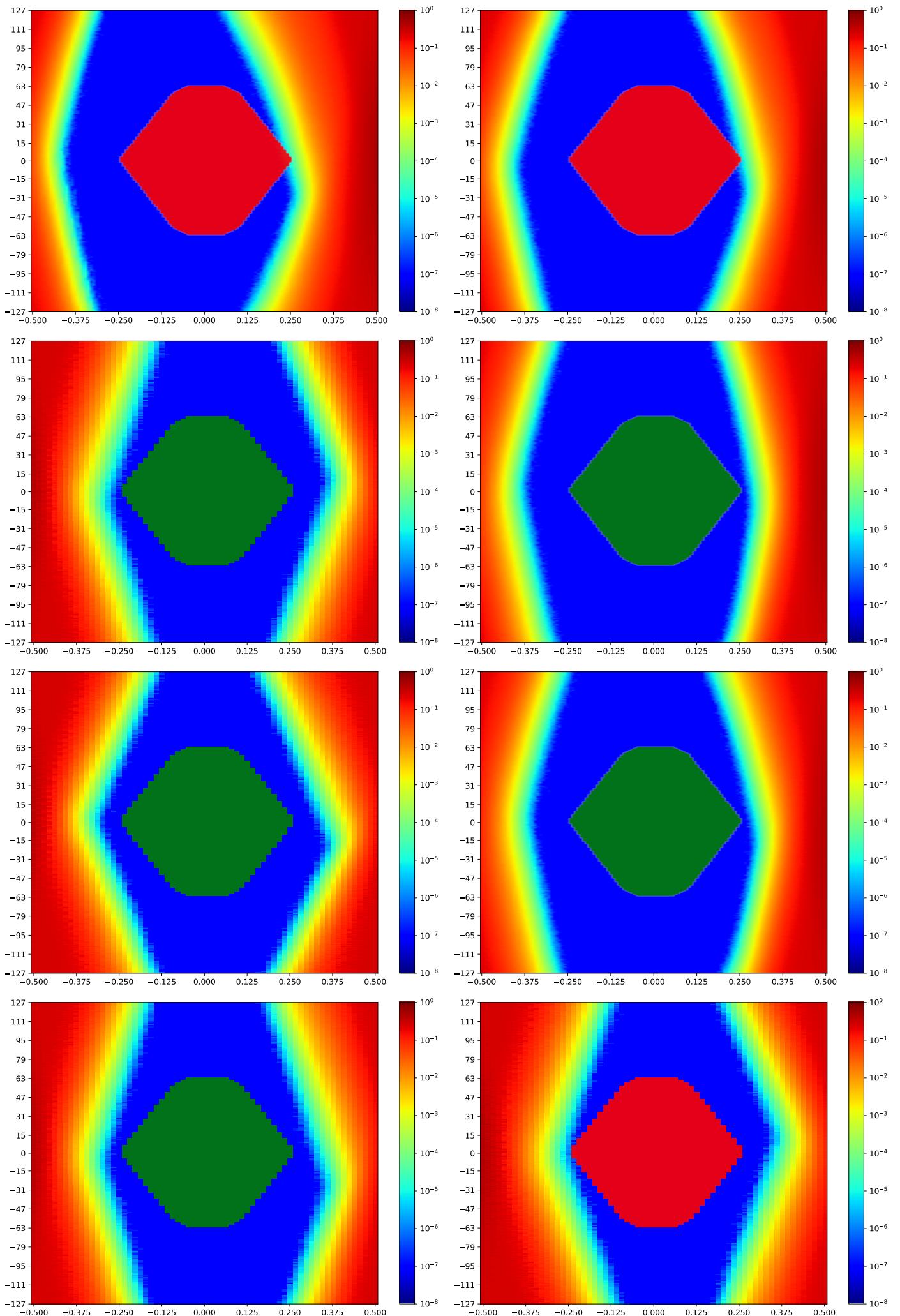


Figure 3.53: Partial TRP TX5 MSP_A RX5 Minipod Loopback

3.5.1 TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

Table 3.49: TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:46:35		2018-Jan-23 23:47:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16281	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

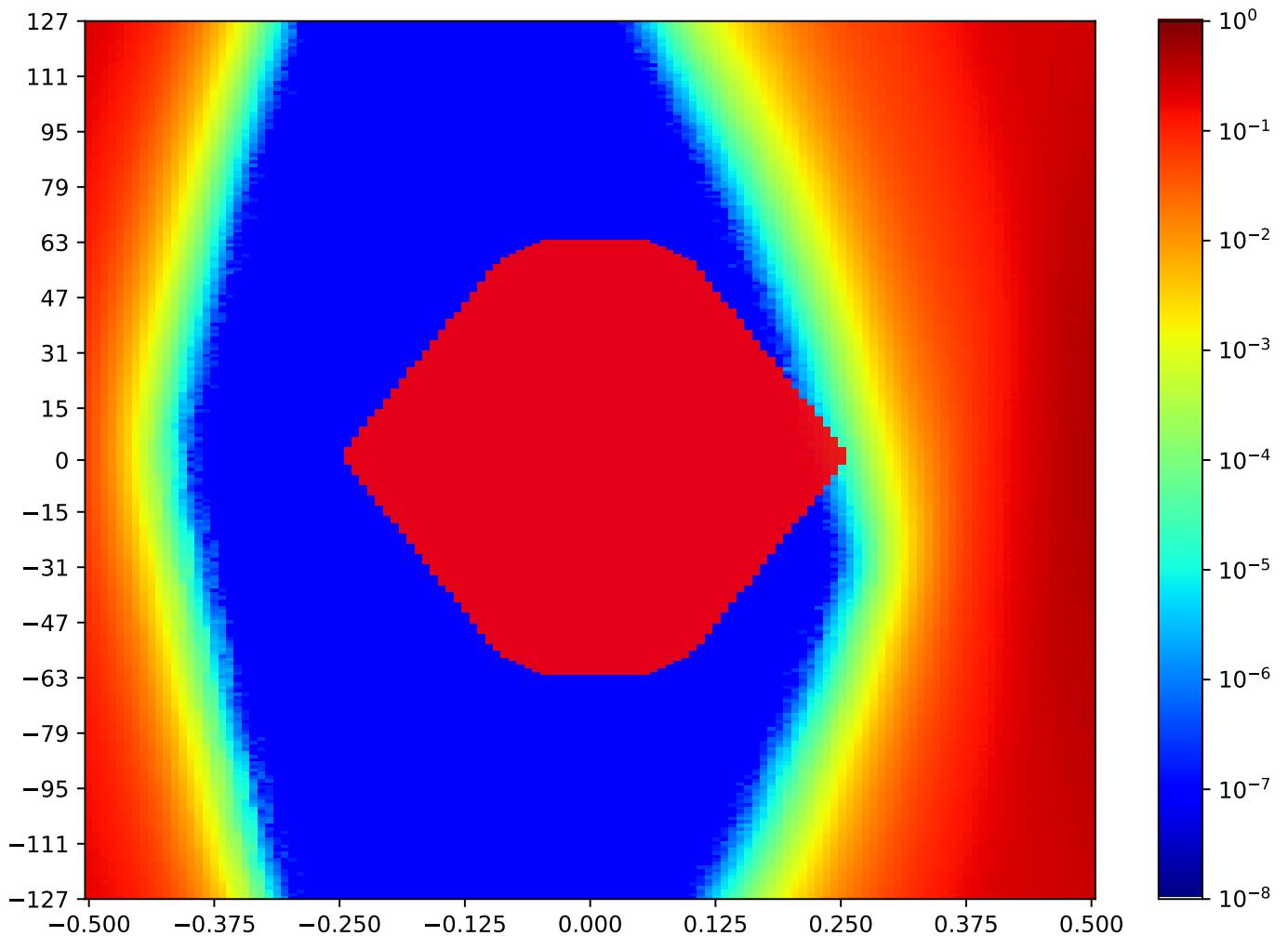


Figure 3.54: TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.5.2 TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

Table 3.50: TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:45:13		2018-Jan-23 23:45:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16378	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

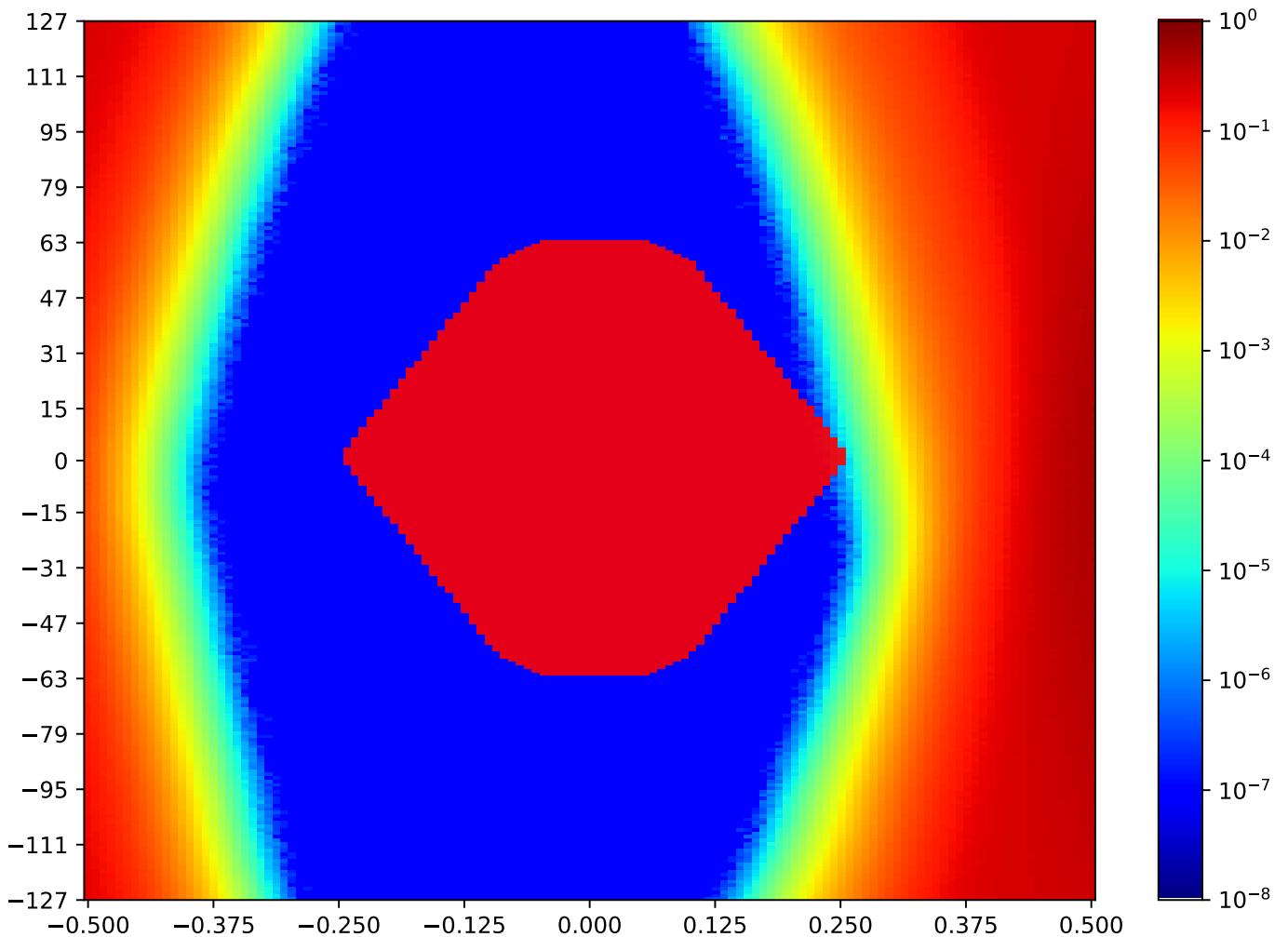


Figure 3.55: TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.5.3 TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

Table 3.51: TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:47:36		2018-Jan-23 23:47:57	
Reset RX	OA	HO		HO (%)	
true	7243	38		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

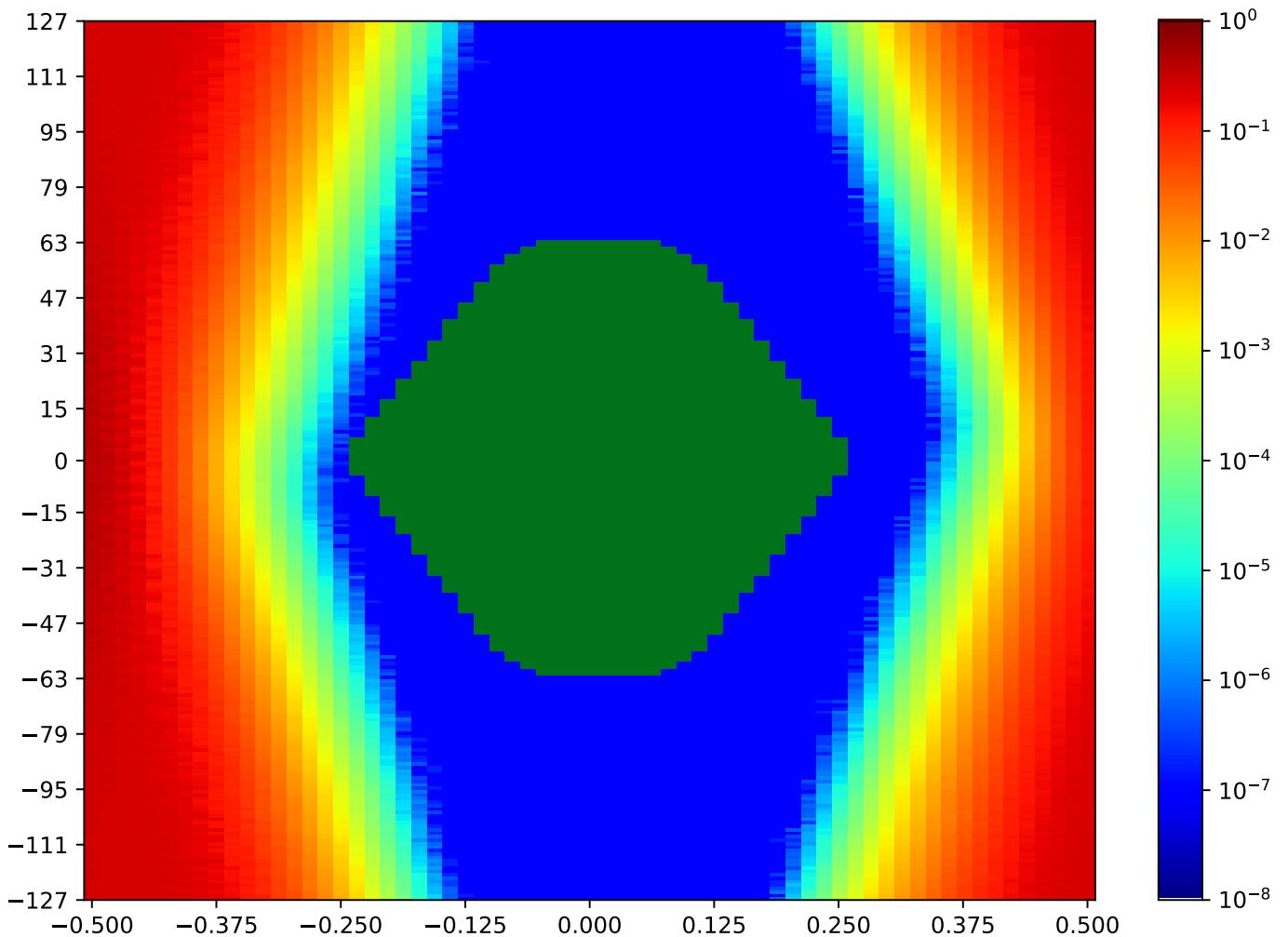


Figure 3.56: TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.5.4 TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

Table 3.52: TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:45:54		2018-Jan-23 23:46:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17293	79	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

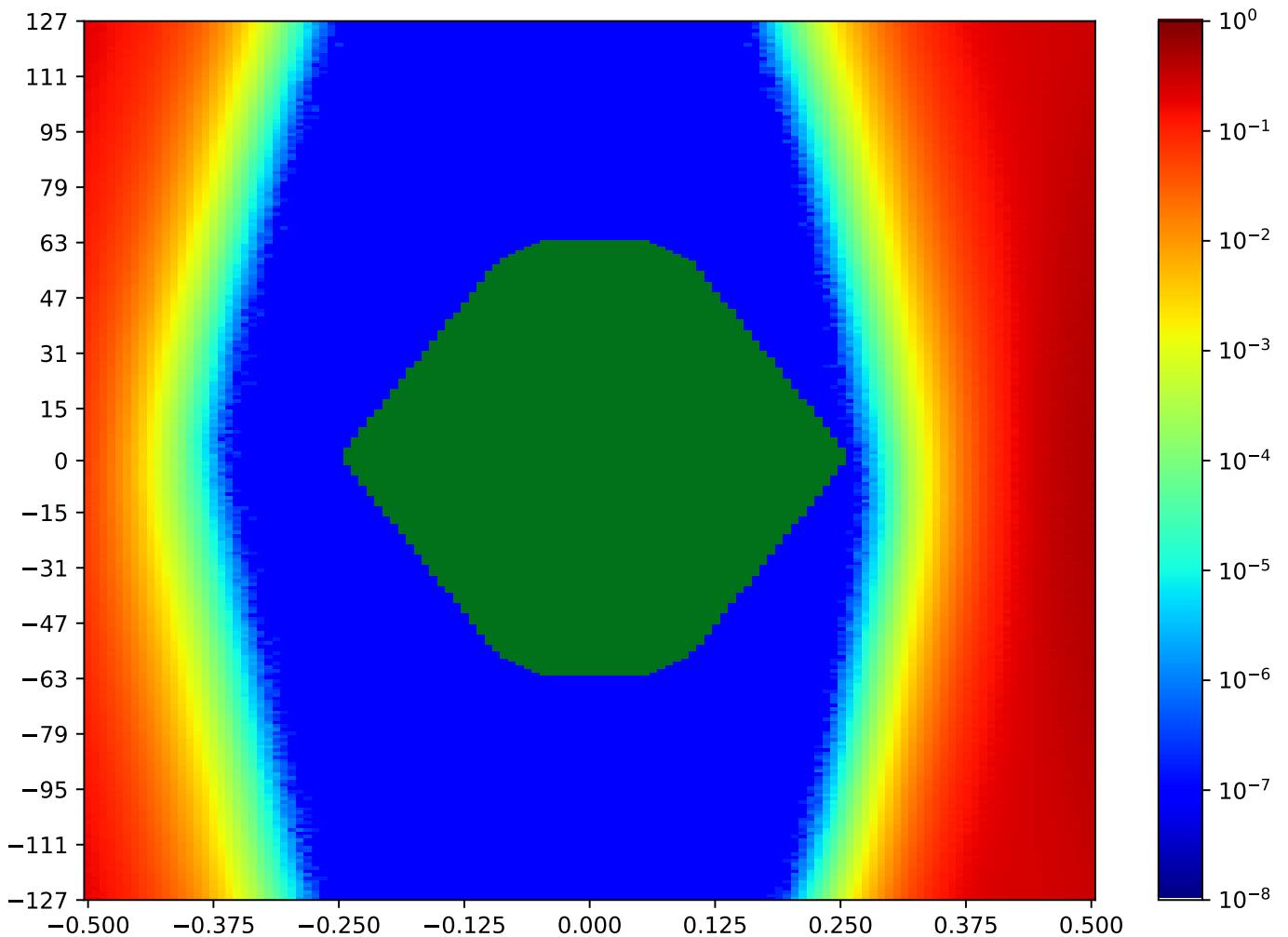


Figure 3.57: TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.5.5 TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

Table 3.53: TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:48:17		2018-Jan-23 23:48:38	
Reset RX	OA	HO		HO (%)	
true	7196	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

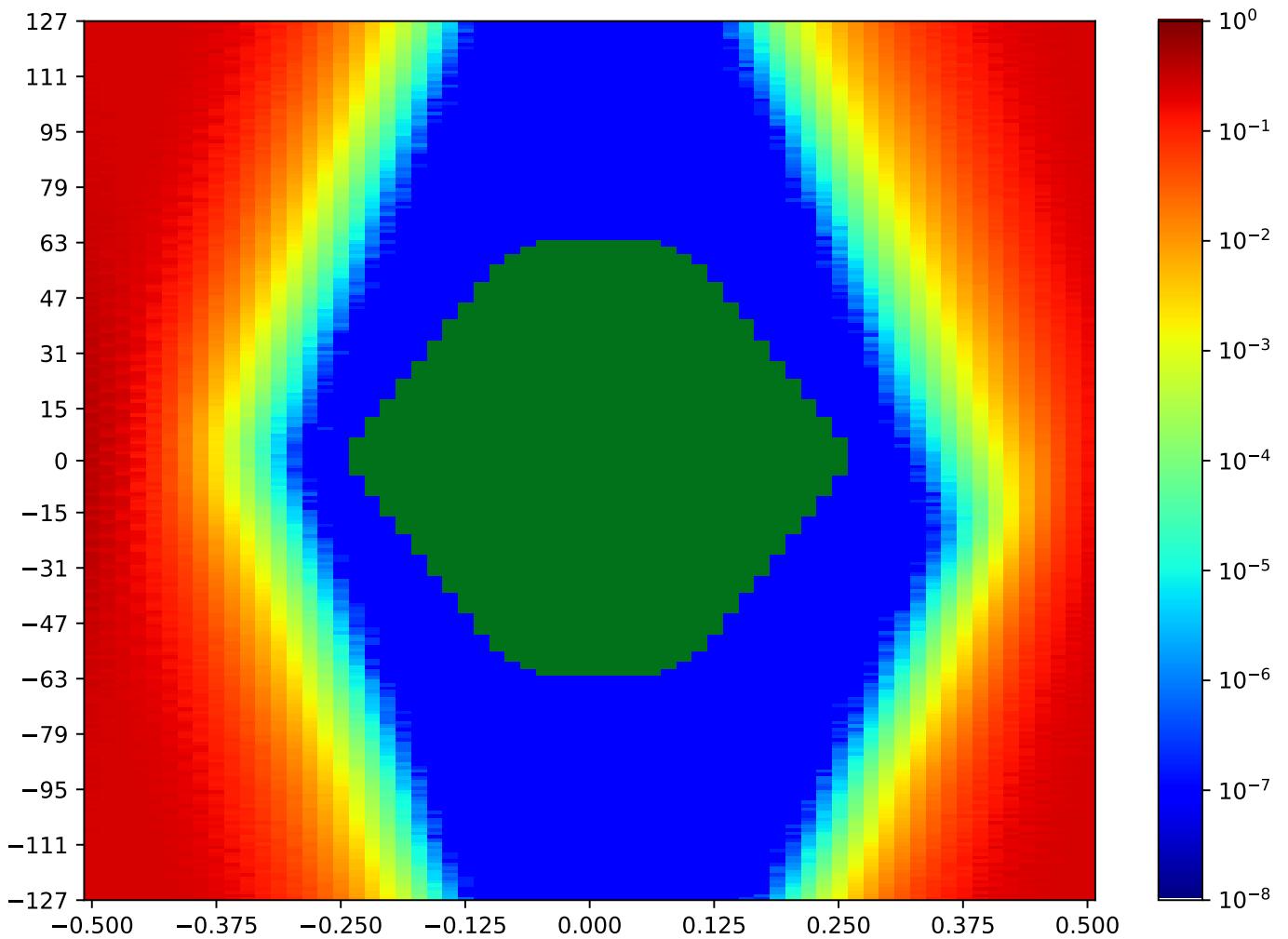


Figure 3.58: TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.5.6 TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

Table 3.54: TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:44:33		2018-Jan-23 23:45:13	
Reset RX	OA	HO		HO (%)	
true	16667	76		58.91%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1		ELF Version: 0x4002 SVN: 0	

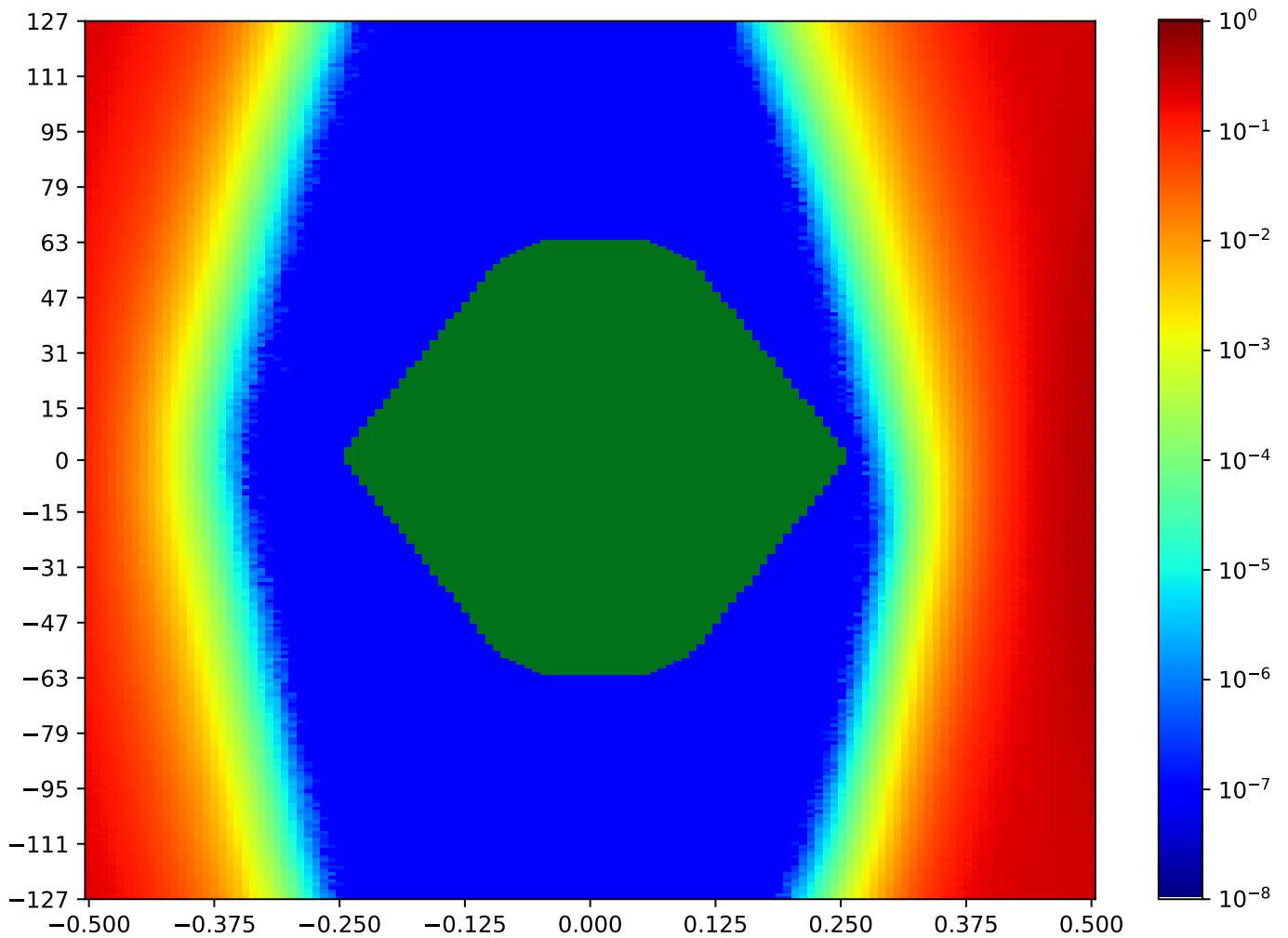


Figure 3.59: TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.5.7 TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

Table 3.55: TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:47:16		2018-Jan-23 23:47:36	
Reset RX	OA	HO		HO (%)	
true	7449	35		53.85%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

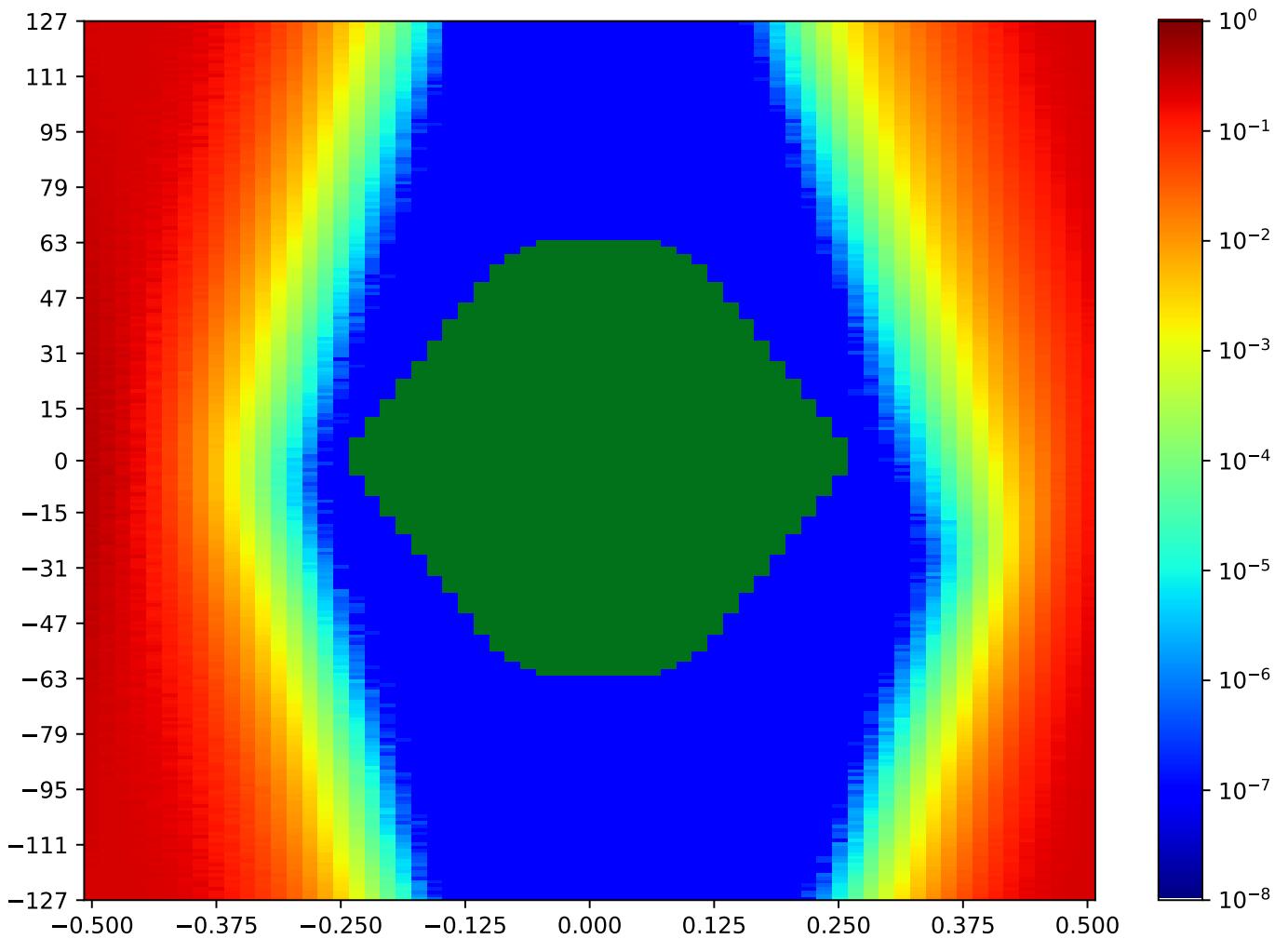


Figure 3.60: TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.5.8 TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

Table 3.56: TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:47:57		2018-Jan-23 23:48:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6612	35	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

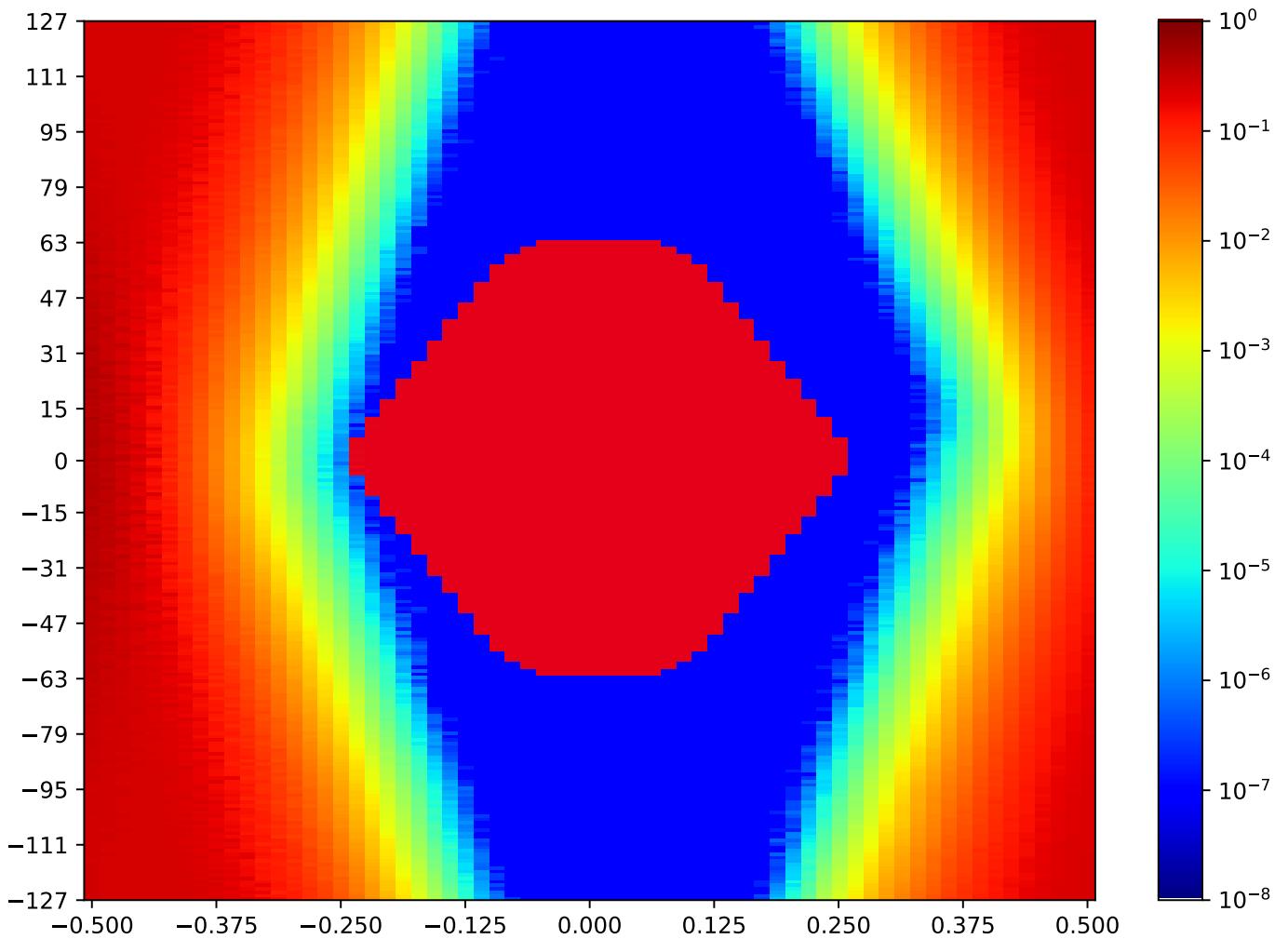


Figure 3.61: TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

Call back to summary Figure 3.53. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.6 TRP J1 QSFP Loopback

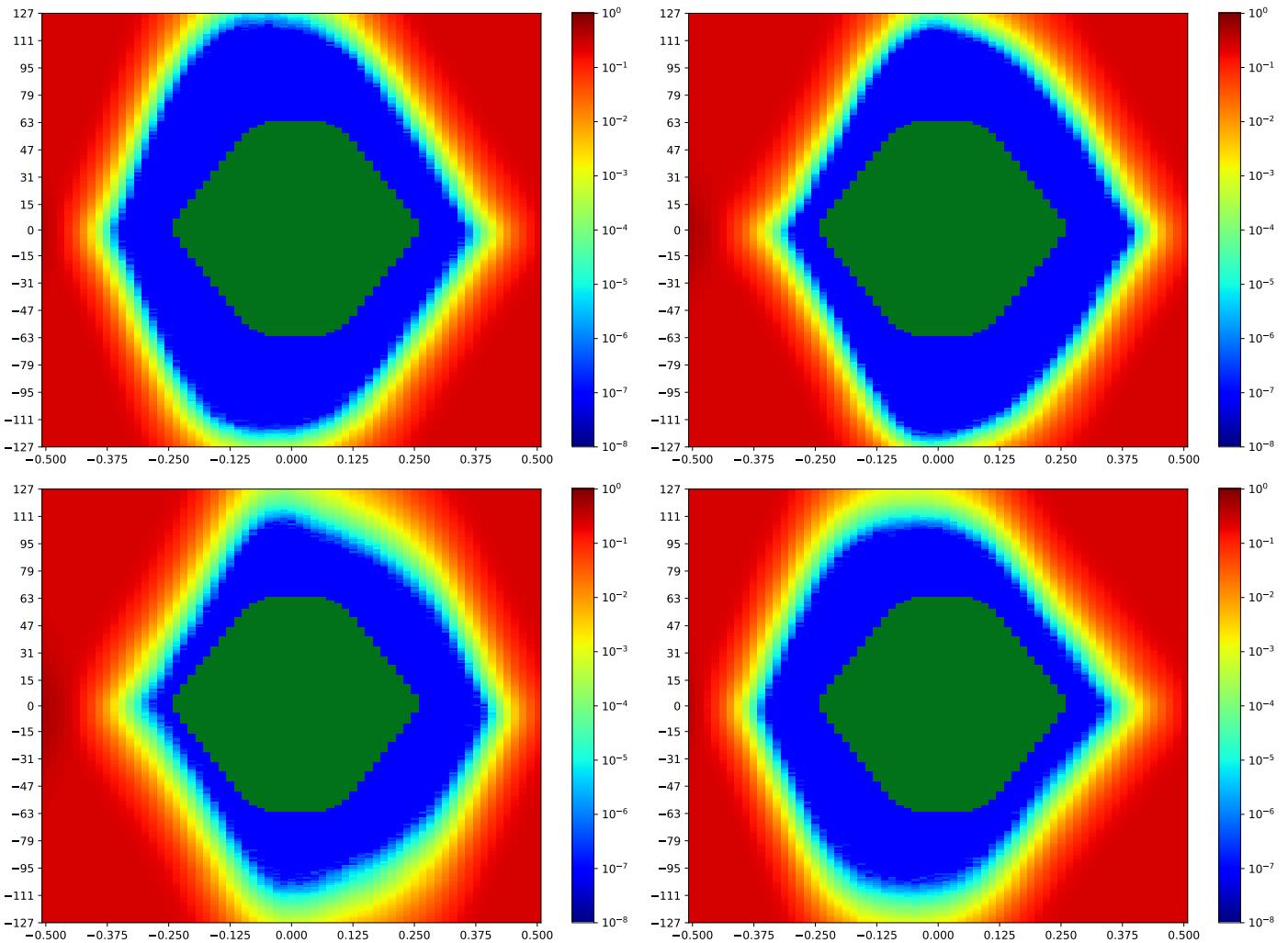


Figure 3.62: TRP J1 QSFP Loopback

A cross-reference to Figure 3.62. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.
Next summary Figure 3.67.

3.6.1 TRP_FPGA-J1-00–J1-00-TRP_FPGA

Table 3.57: TRP_FPGA-J1-00–J1-00-TRP_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:48:38			2018-Jan-23 23:48:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	6960	45	69.23%	228	89.41%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

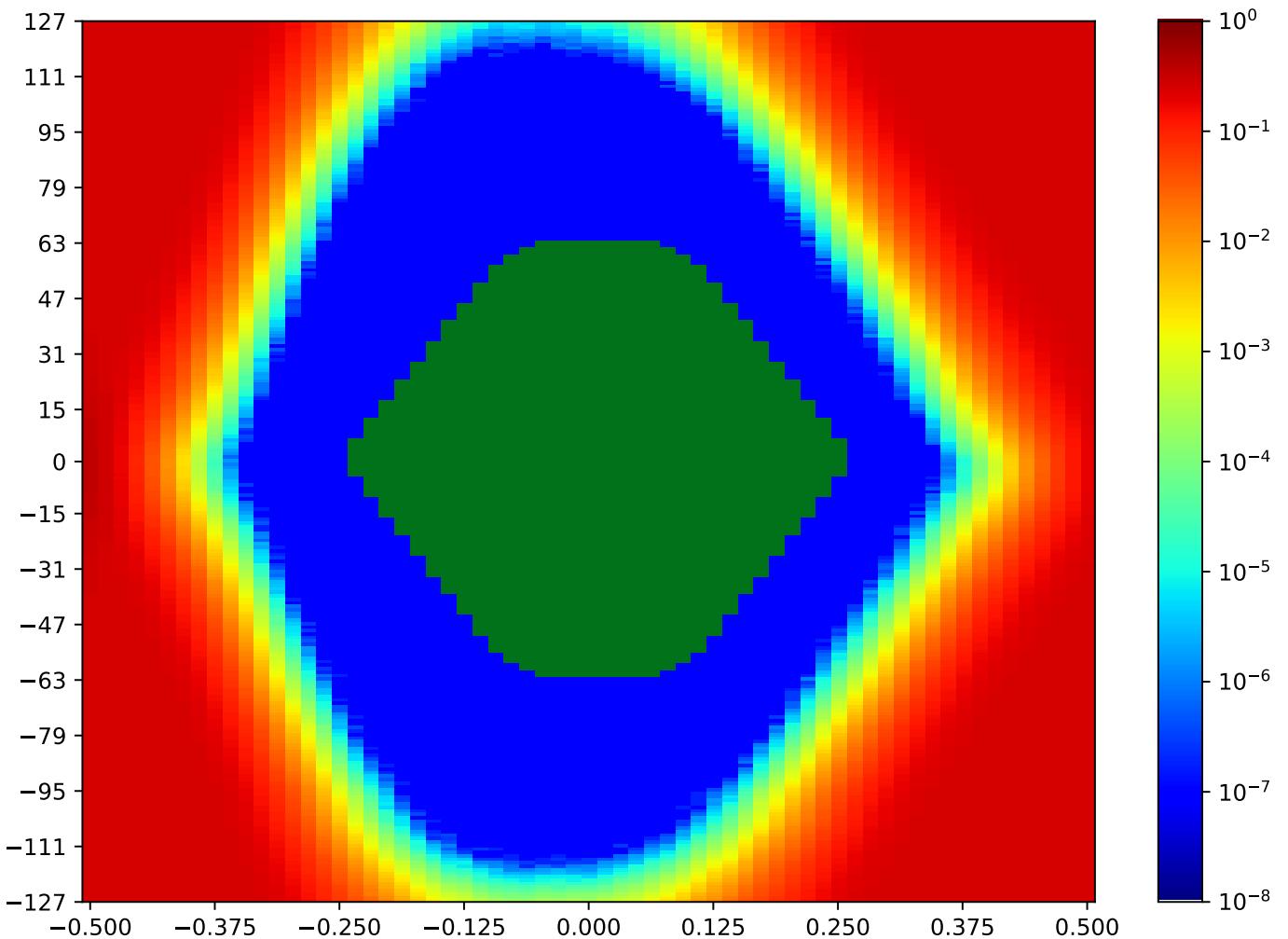


Figure 3.63: TRP_FPGA-J1-00–J1-00-TRP_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.6.2 TRP_FPGA-J1-01–J1-01-TRP_FPGA

Table 3.58: TRP_FPGA-J1-01–J1-01-TRP_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:48:58			2018-Jan-23 23:49:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	6437	44	67.69%	237	92.55%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

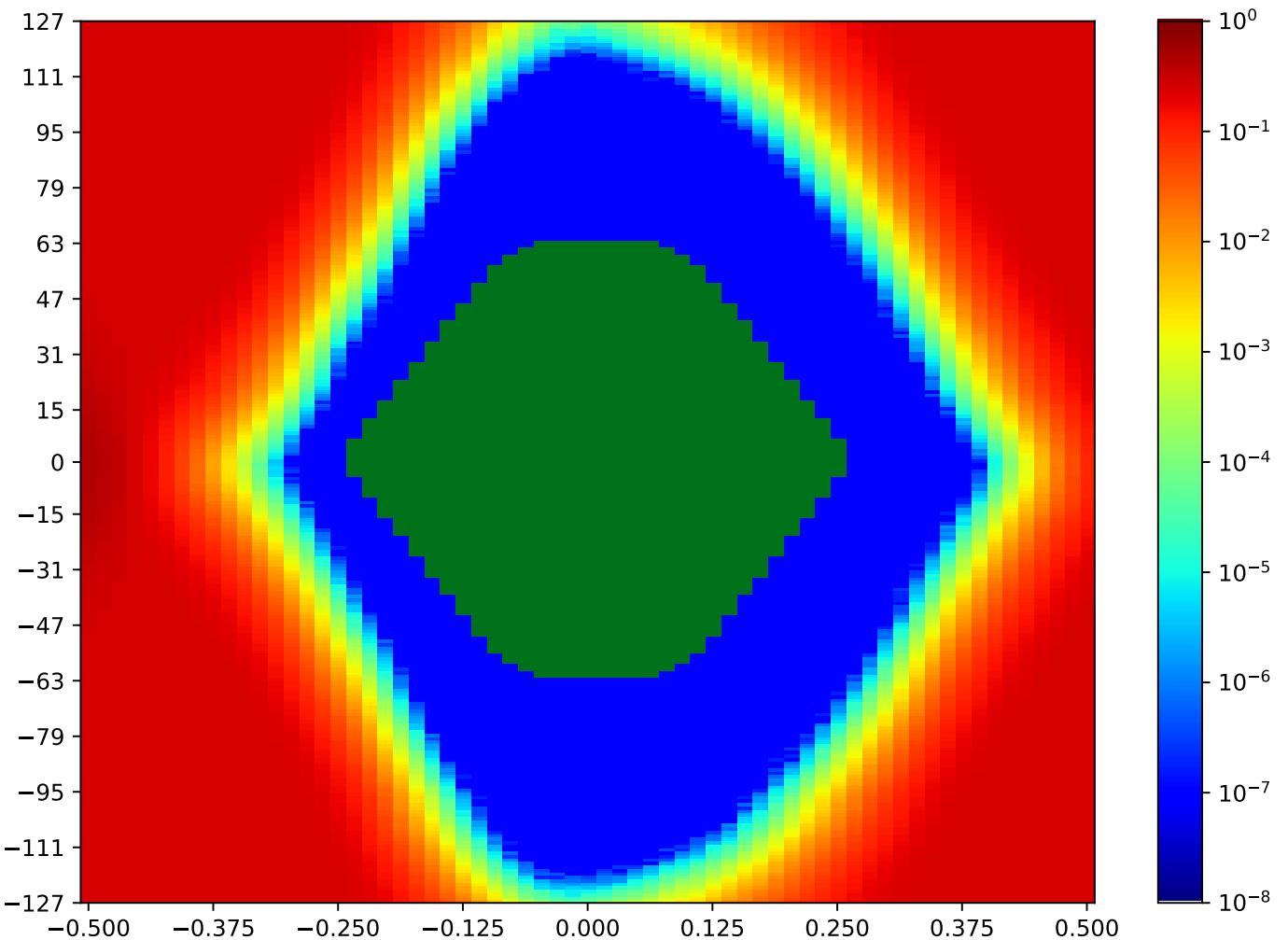


Figure 3.64: TRP_FPGA-J1-01–J1-01-TRP_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.6.3 TRP_FPGA-J1-02–J1-02-TRP_FPGA

Table 3.59: TRP_FPGA-J1-02–J1-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:49:19		2018-Jan-23 23:49:39	
Reset RX	OA	HO		HO (%)	
true	5563	41		63.08%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

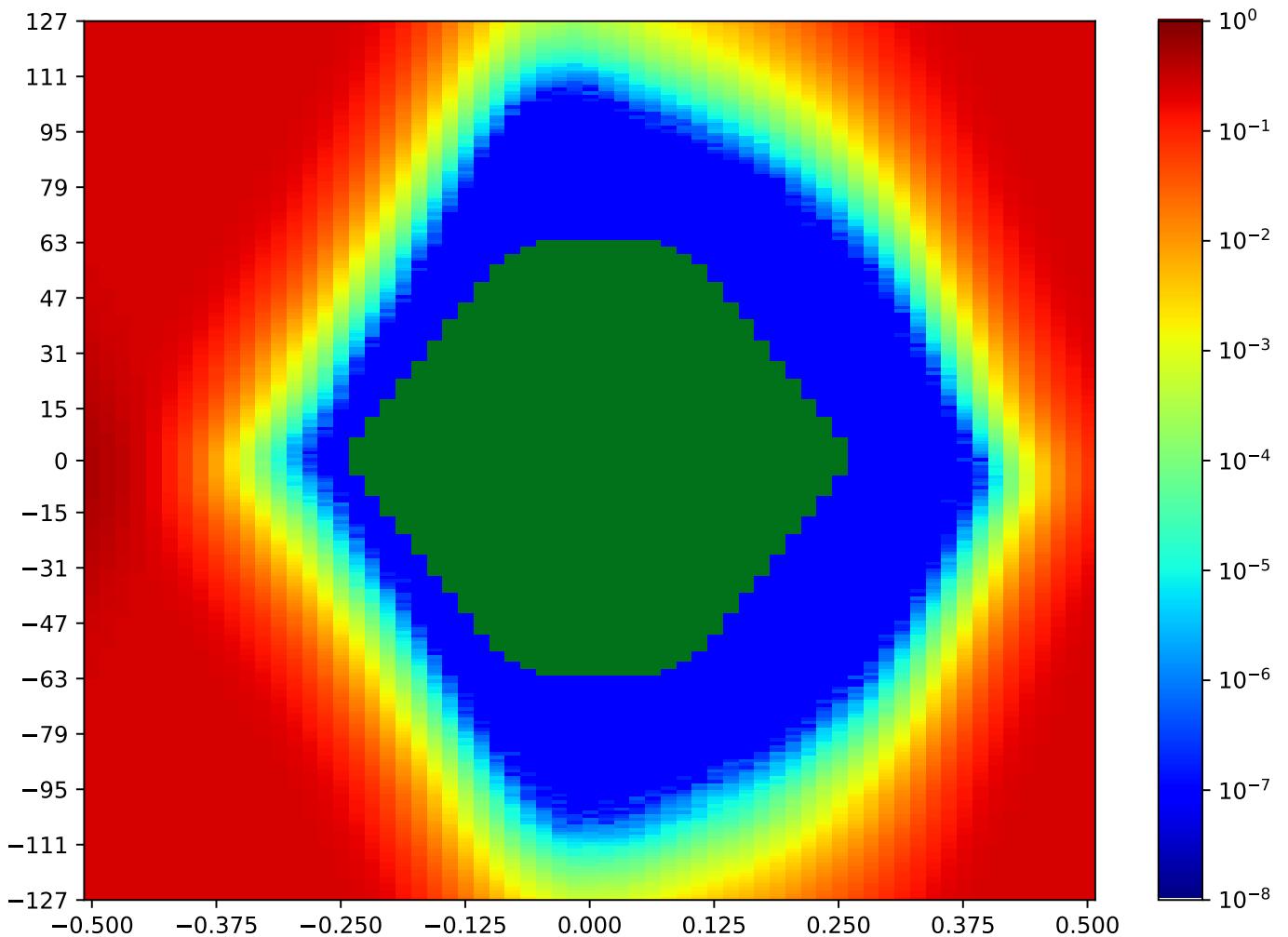


Figure 3.65: TRP_FPGA-J1-02–J1-02-TRP_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.6.4 TRP_FPGA-J1-03–J1-03-TRP_FPGA

Table 3.60: TRP_FPGA-J1-03–J1-03-TRP_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	5864	42	64.62%	201	78.43%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

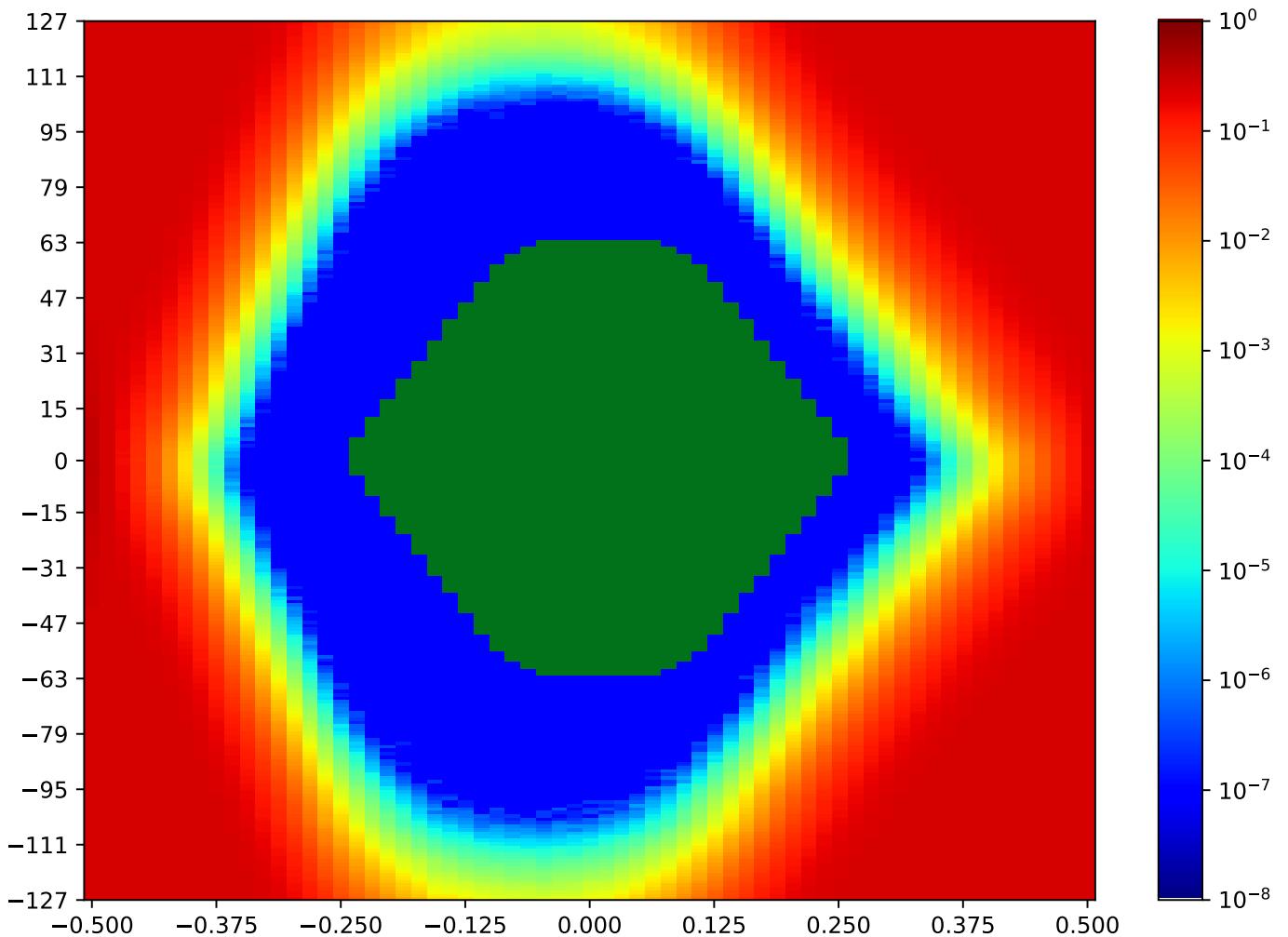


Figure 3.66: TRP_FPGA-J1-03–J1-03-TRP_FPGA

Call back to summary Figure 3.62. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.7 TRP J3 SFP Loopback

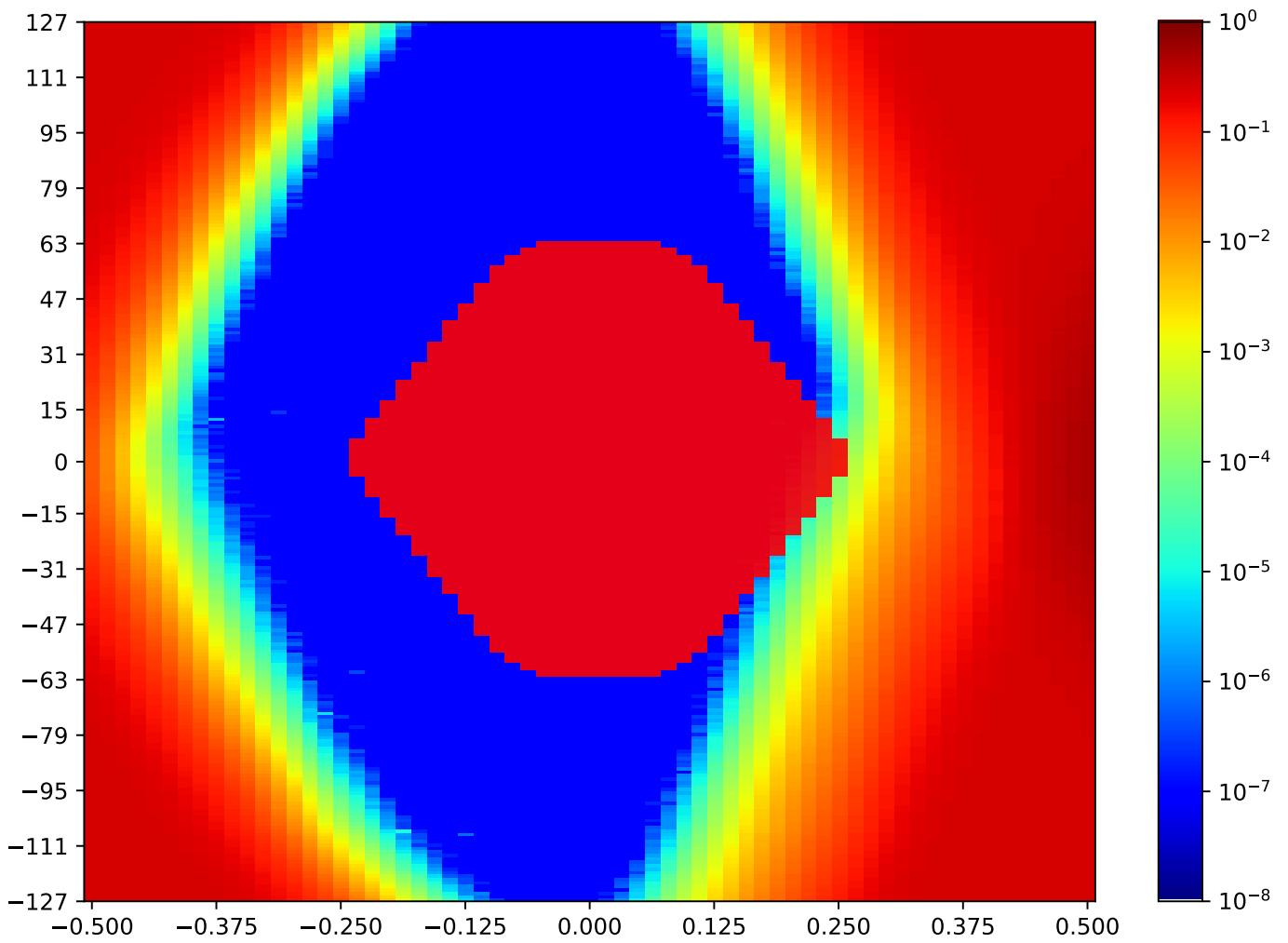


Figure 3.67: TRP J3 SFP Loopback

A cross-reference to Figure 3.67. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.
Next summary Figure 3.69.

3.7.1 TRP_FPGA-J3-00–J3-00-TRP_FPGA

Table 3.61: TRP_FPGA-J3-00–J3-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:50:00		2018-Jan-23 23:50:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6766	36	55.38%	255	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

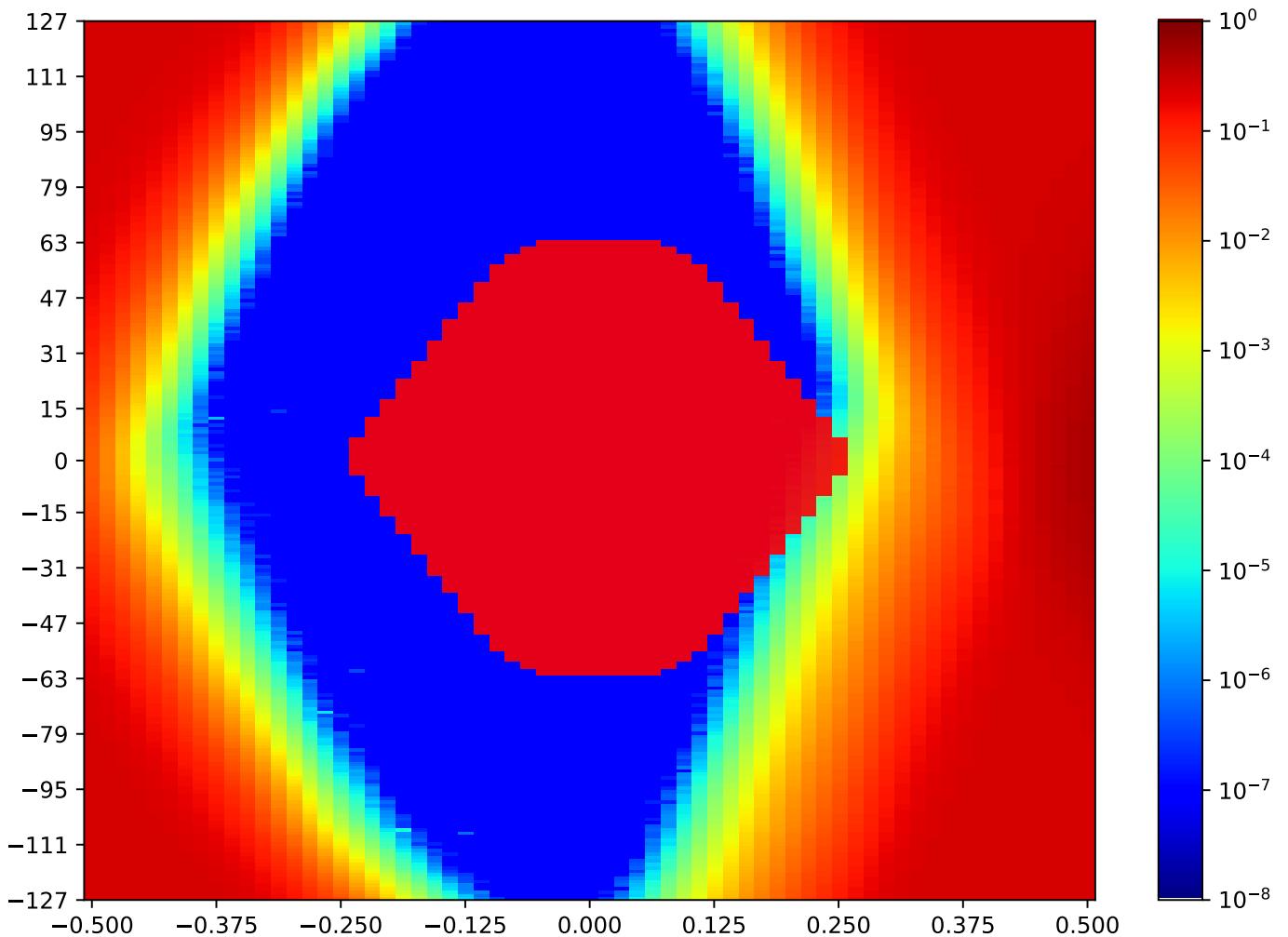


Figure 3.68: TRP_FPGA-J3-00–J3-00-TRP_FPGA

Call back to summary Figure 3.67. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8 MSP_A TRP On board links

A cross-reference to Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.
Next summary Figure 3.98.

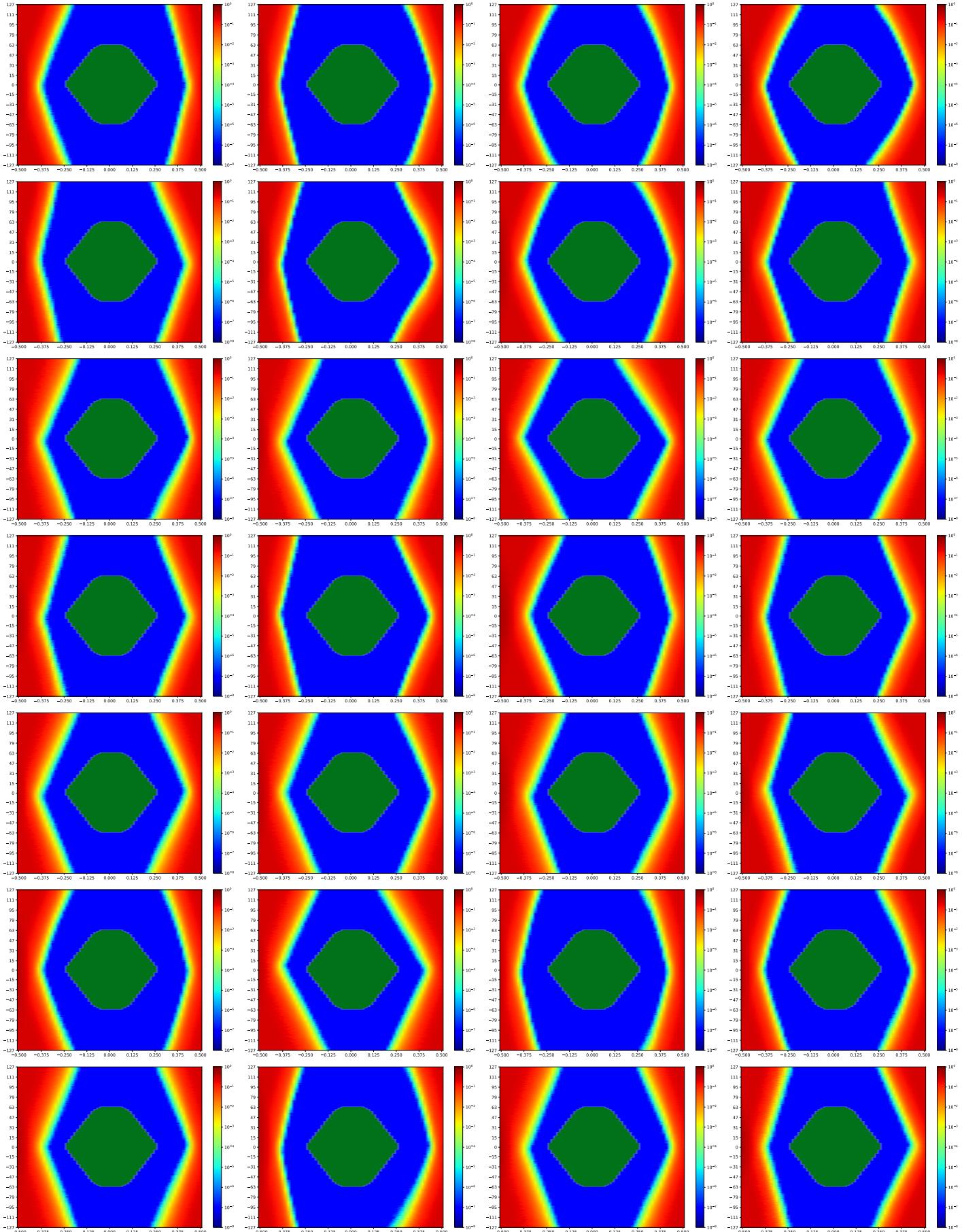


Figure 3.69: MSP_A TRP On board links

3.8.1 MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

Table 3.62: MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:50:21		2018-Jan-23 23:50:41	
Reset RX	OA	HO		HO (%)	
true	10247	48		73.85%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

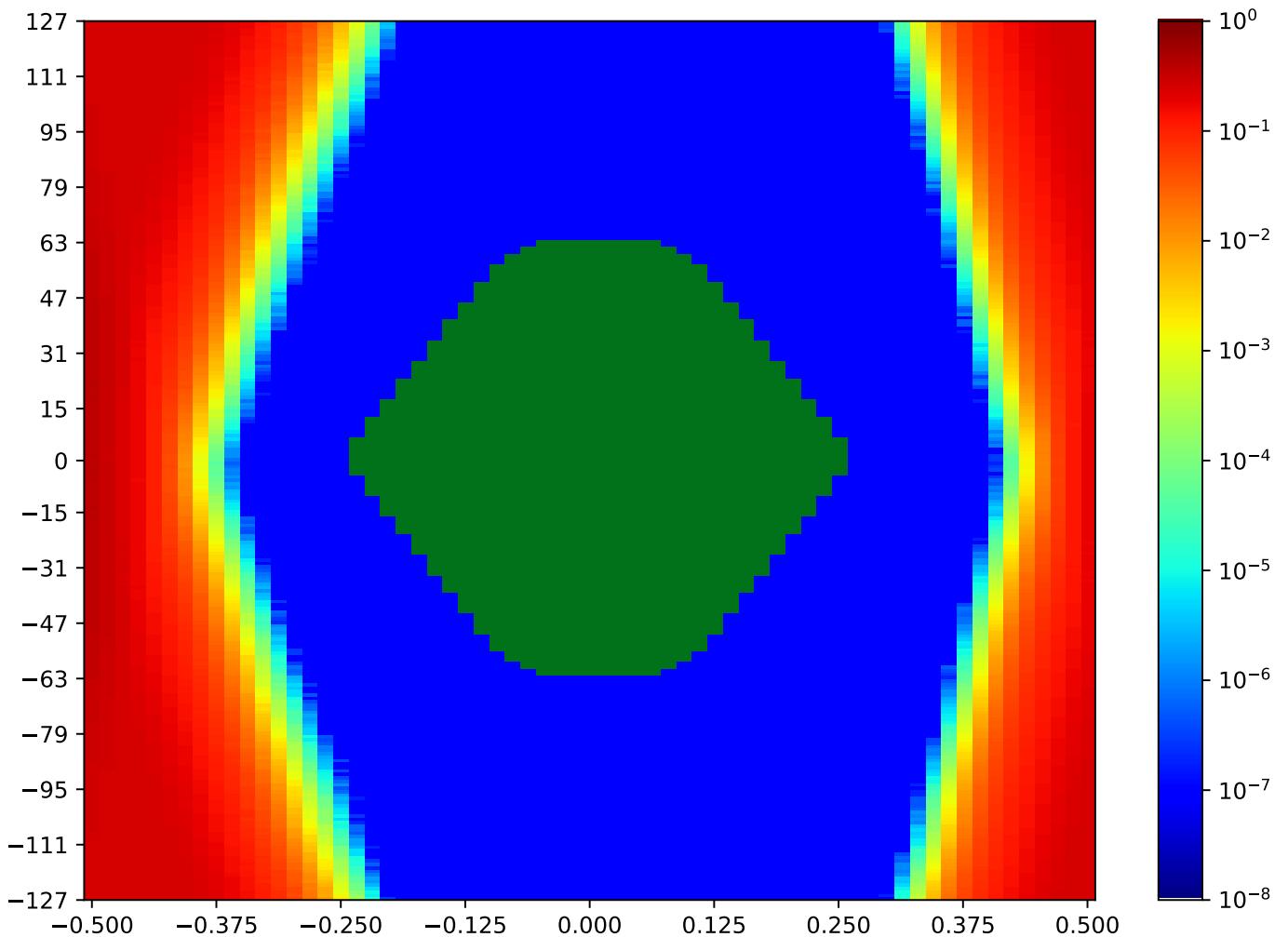


Figure 3.70: MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.2 MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

Table 3.63: MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:50:41		2018-Jan-23 23:51:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11305	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

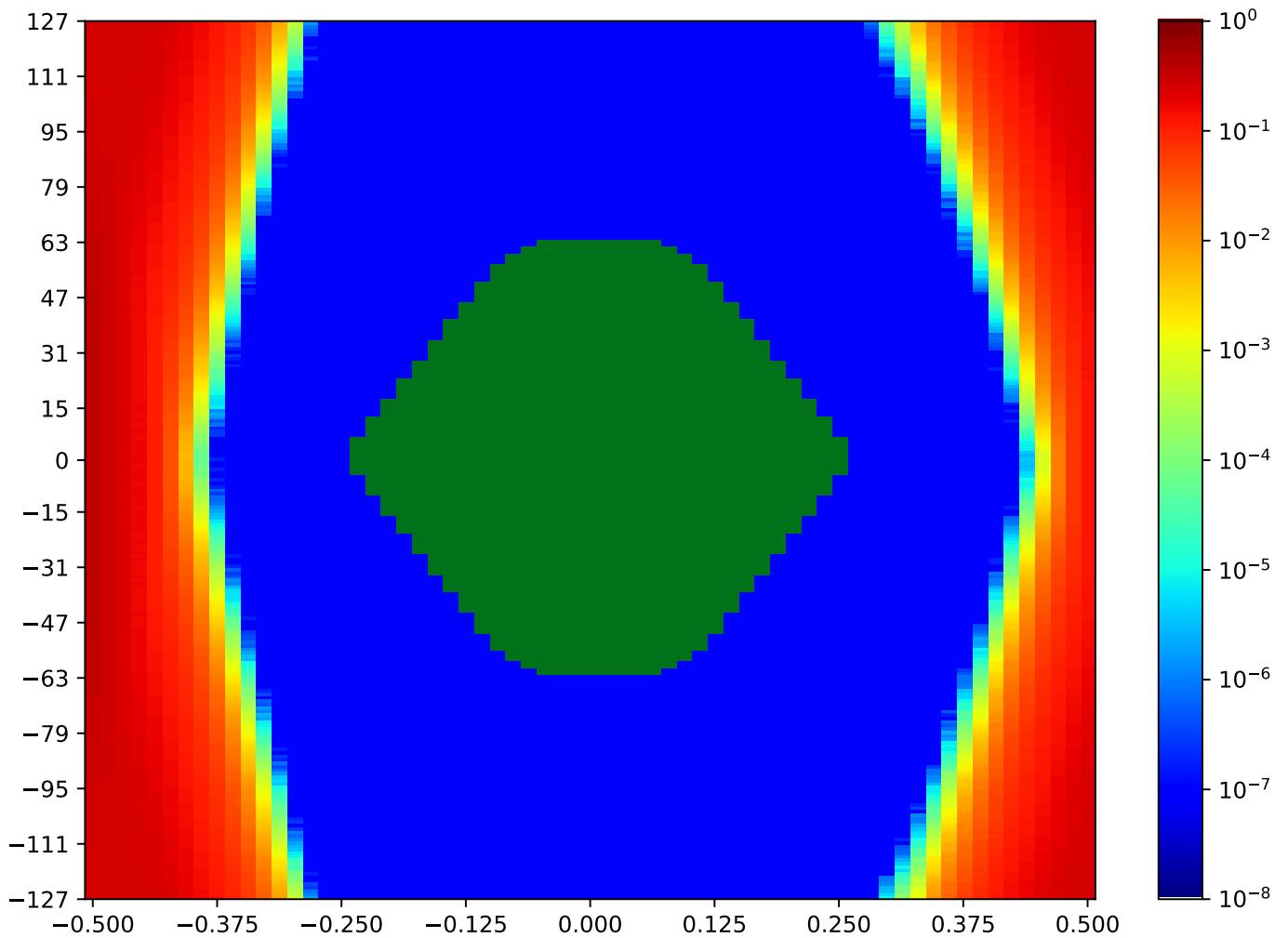


Figure 3.71: MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.3 MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

Table 3.64: MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:51:02		2018-Jan-23 23:51:22	
Reset RX	OA	HO		HO (%)	
true	10054	49		75.38%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

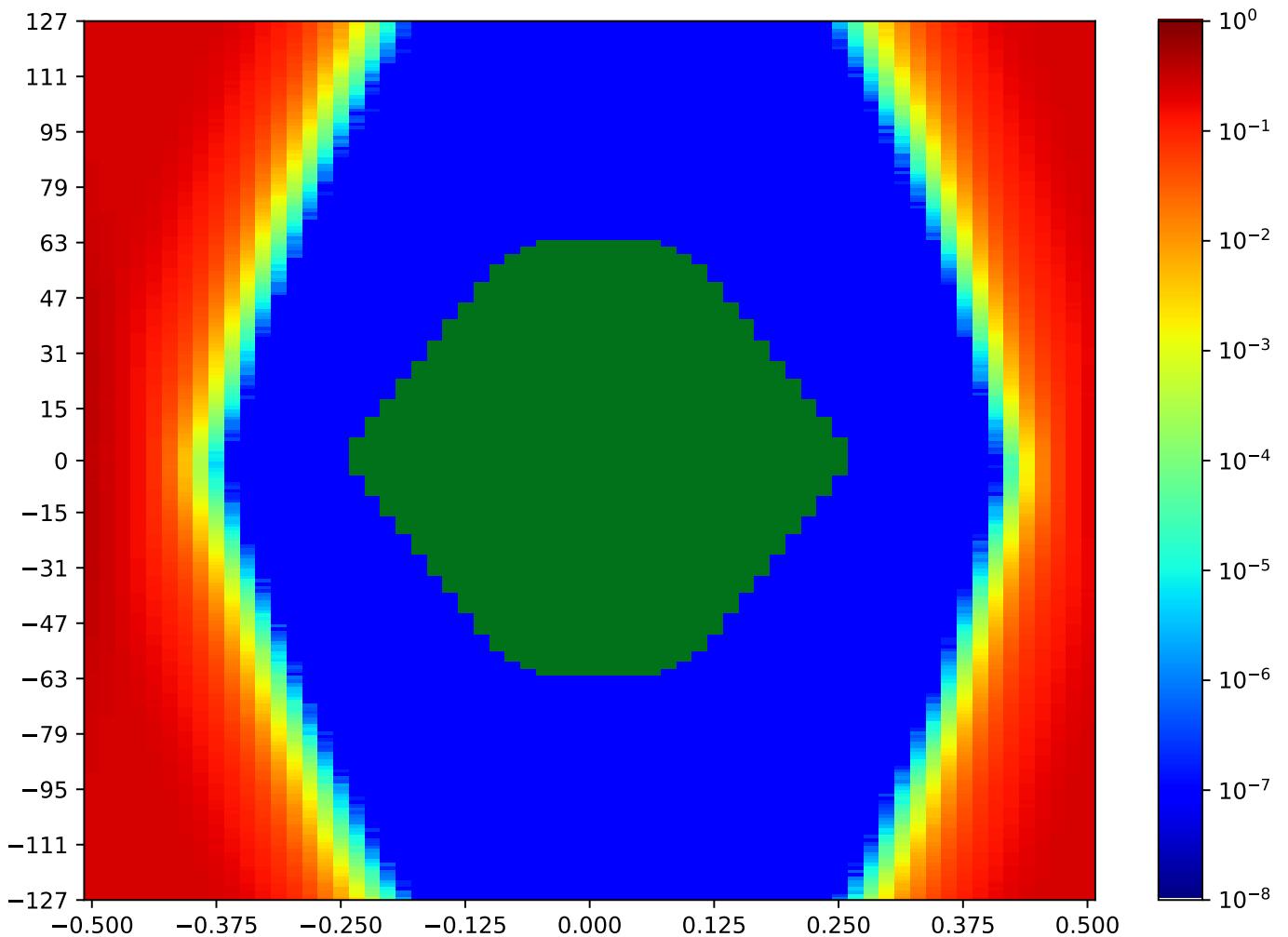


Figure 3.72: MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.4 MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

Table 3.65: MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:51:22		2018-Jan-23 23:51:43	
Reset RX	OA	HO		HO (%)	
true	9717	51		78.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

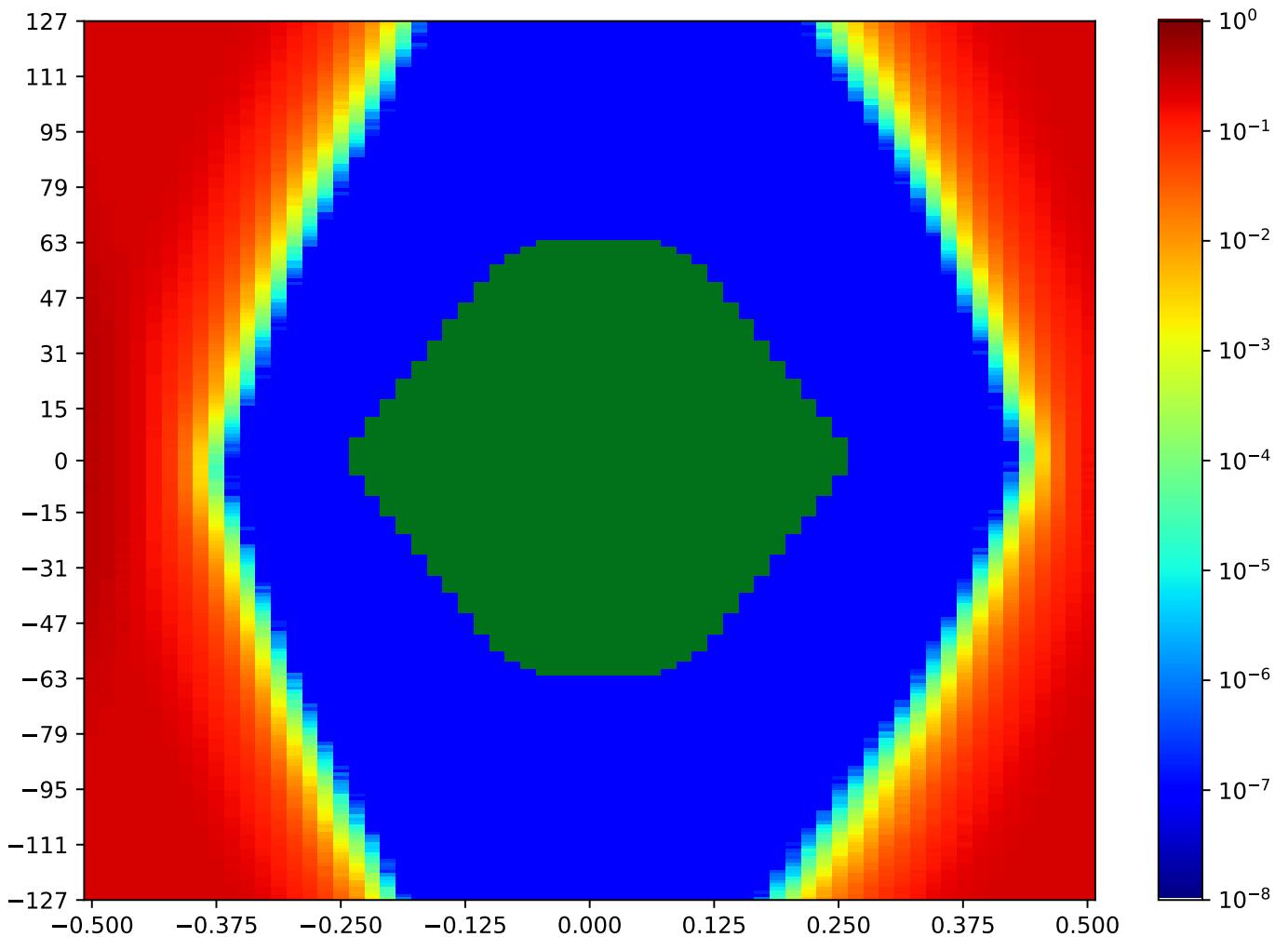


Figure 3.73: MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.5 MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

Table 3.66: MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:51:43		2018-Jan-23 23:52:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10095	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

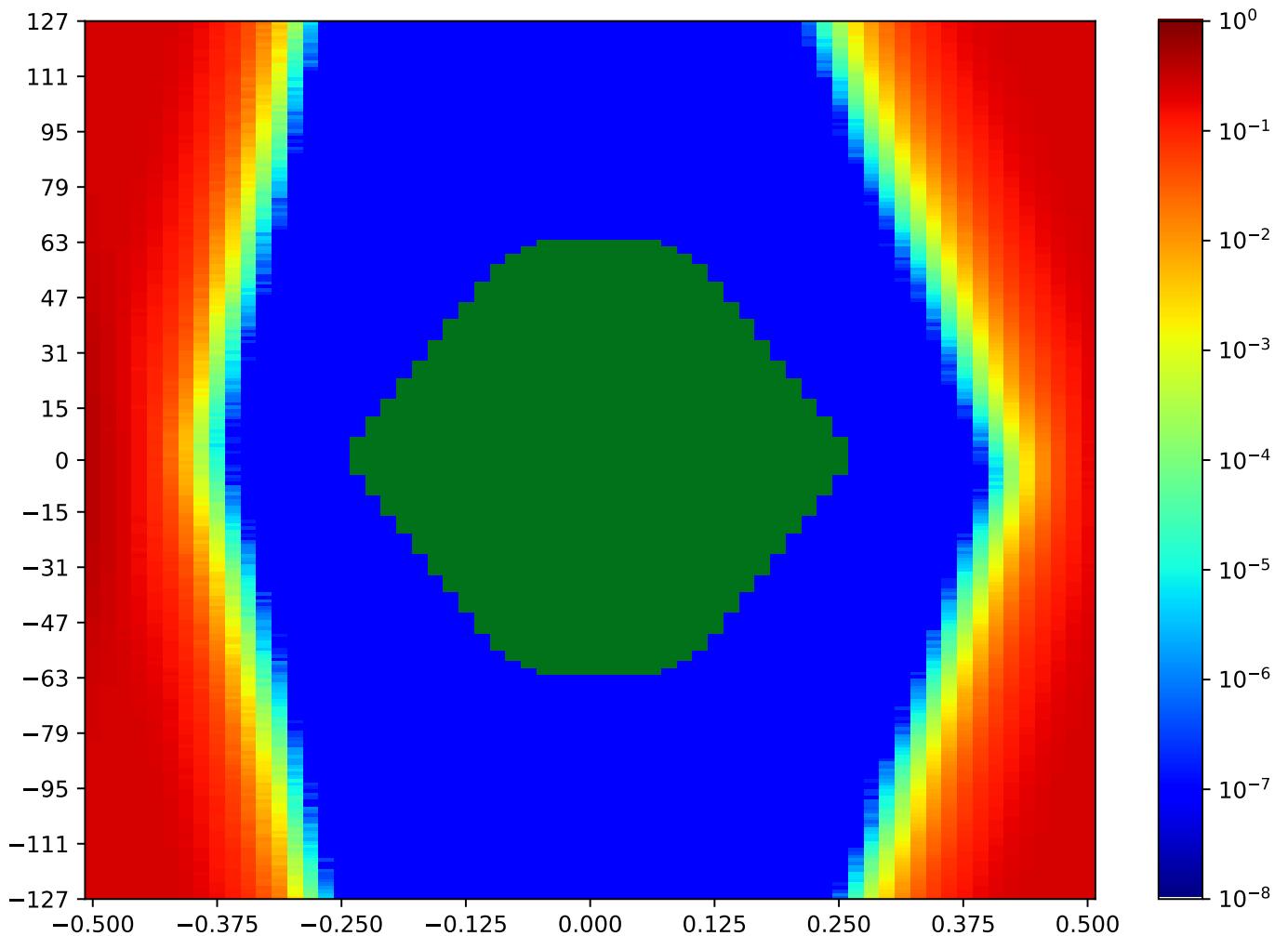


Figure 3.74: MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.6 MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

Table 3.67: MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:52:03		2018-Jan-23 23:52:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10464	51	78.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

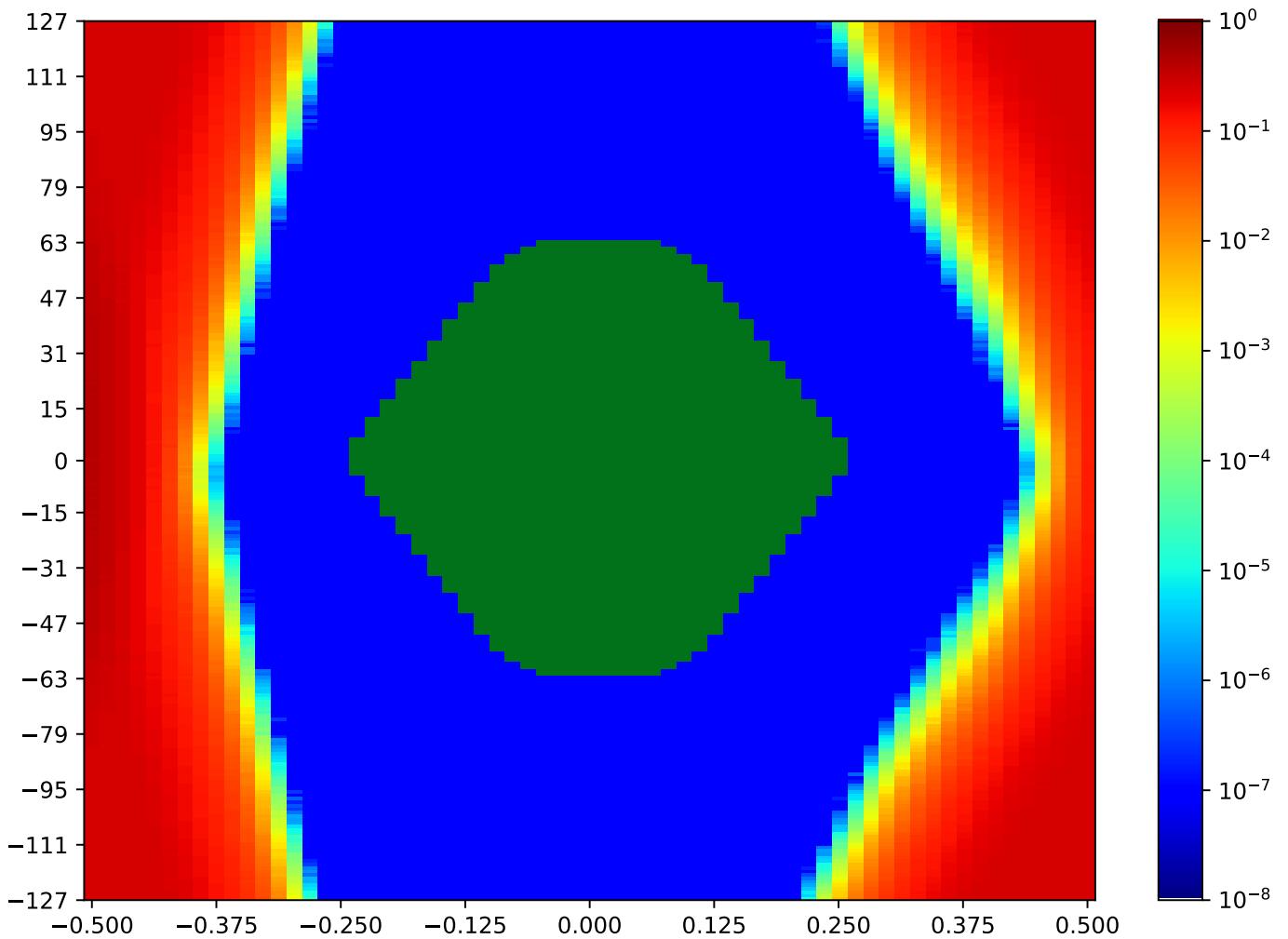


Figure 3.75: MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.7 MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

Table 3.68: MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:52:24		2018-Jan-23 23:52:45	
Reset RX	OA	HO		HO (%)	
true	9795	49		75.38%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

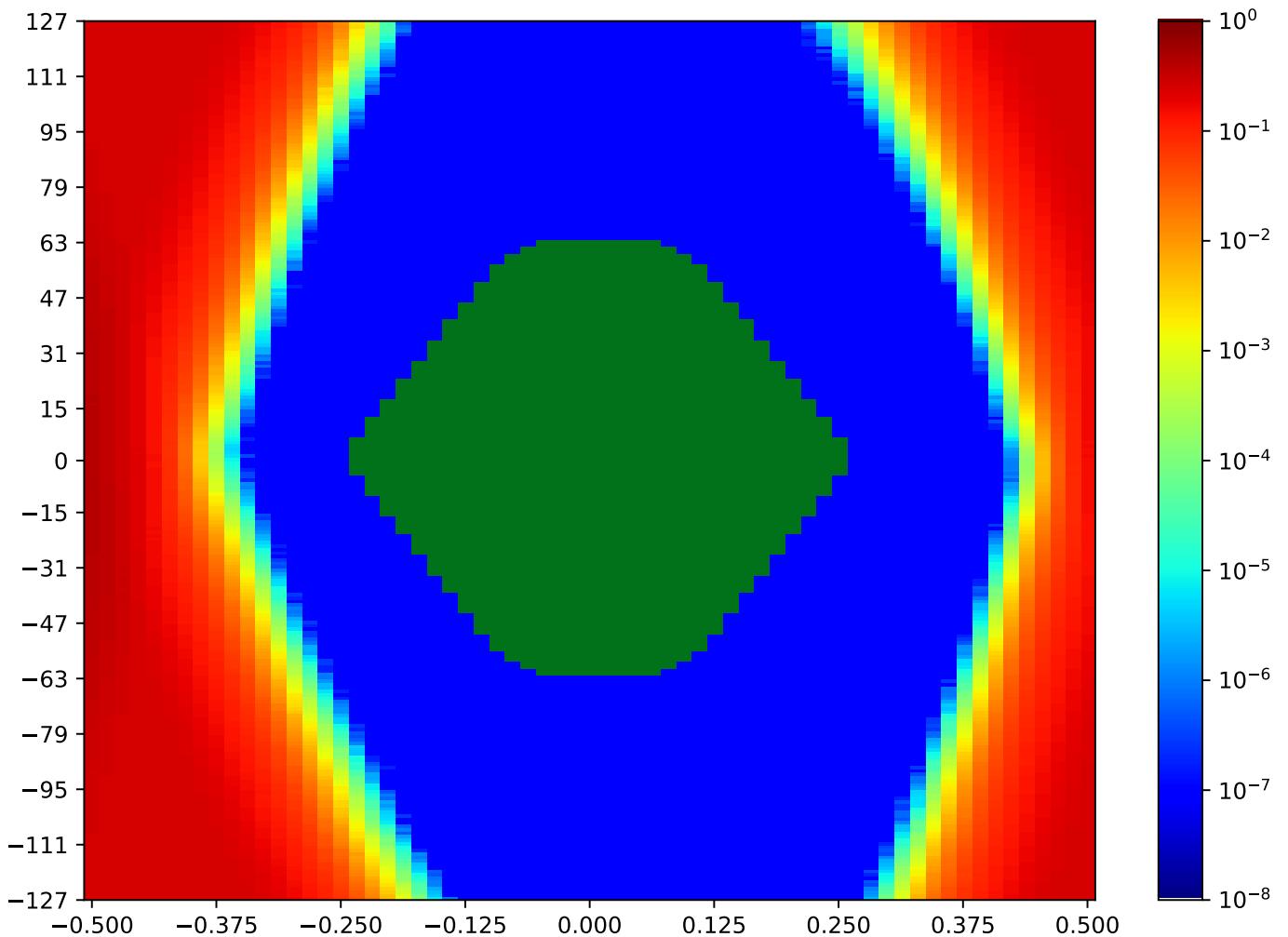


Figure 3.76: MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.8 MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

Table 3.69: MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:52:45		2018-Jan-23 23:53:05	
Reset RX	OA	HO		HO (%)	
true	9901	48		73.85%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

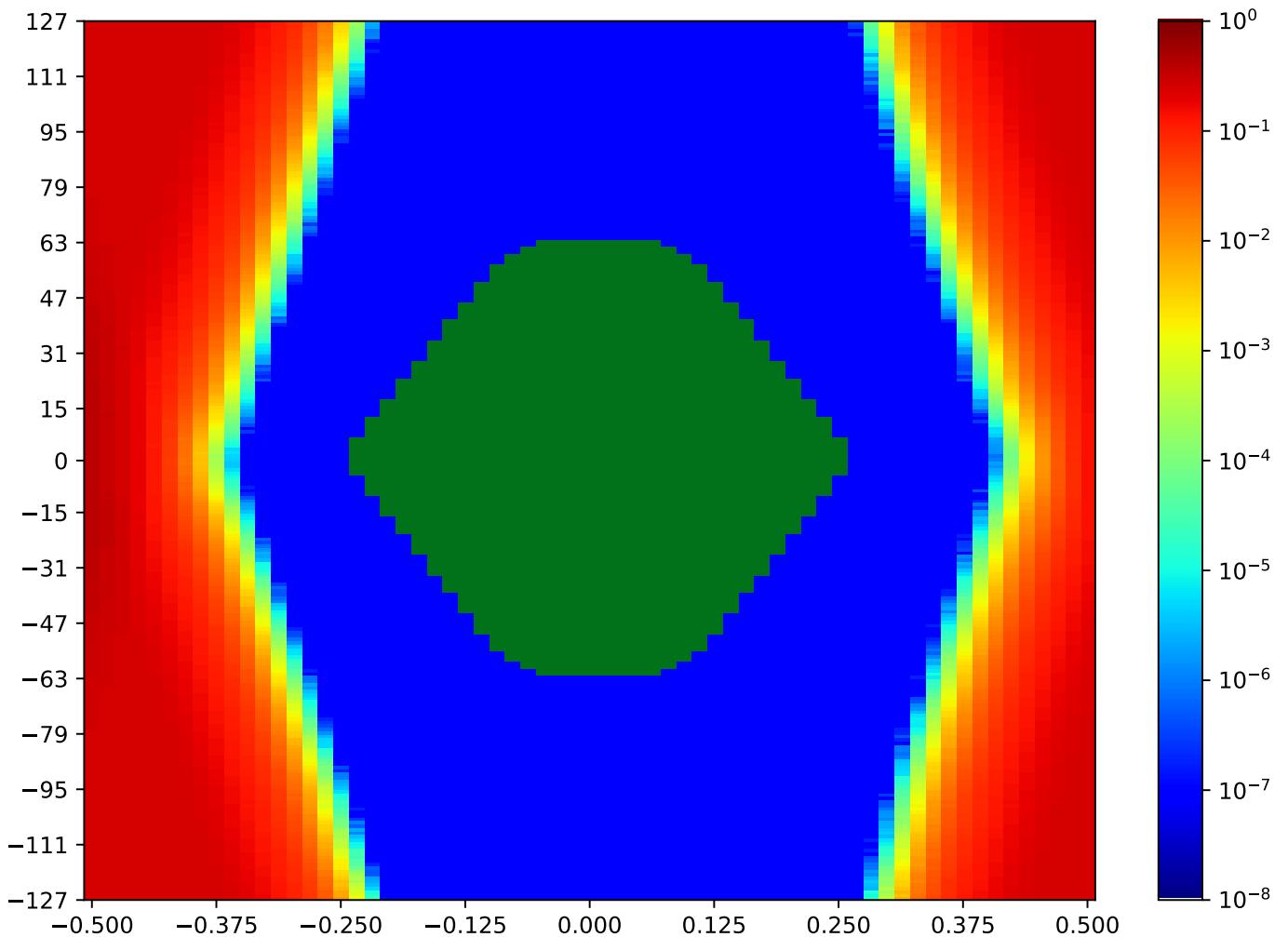


Figure 3.77: MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.9 MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

Table 3.70: MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:53:05		2018-Jan-23 23:53:26	
Reset RX	OA	HO		HO (%)	
true	9364	48		73.85%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

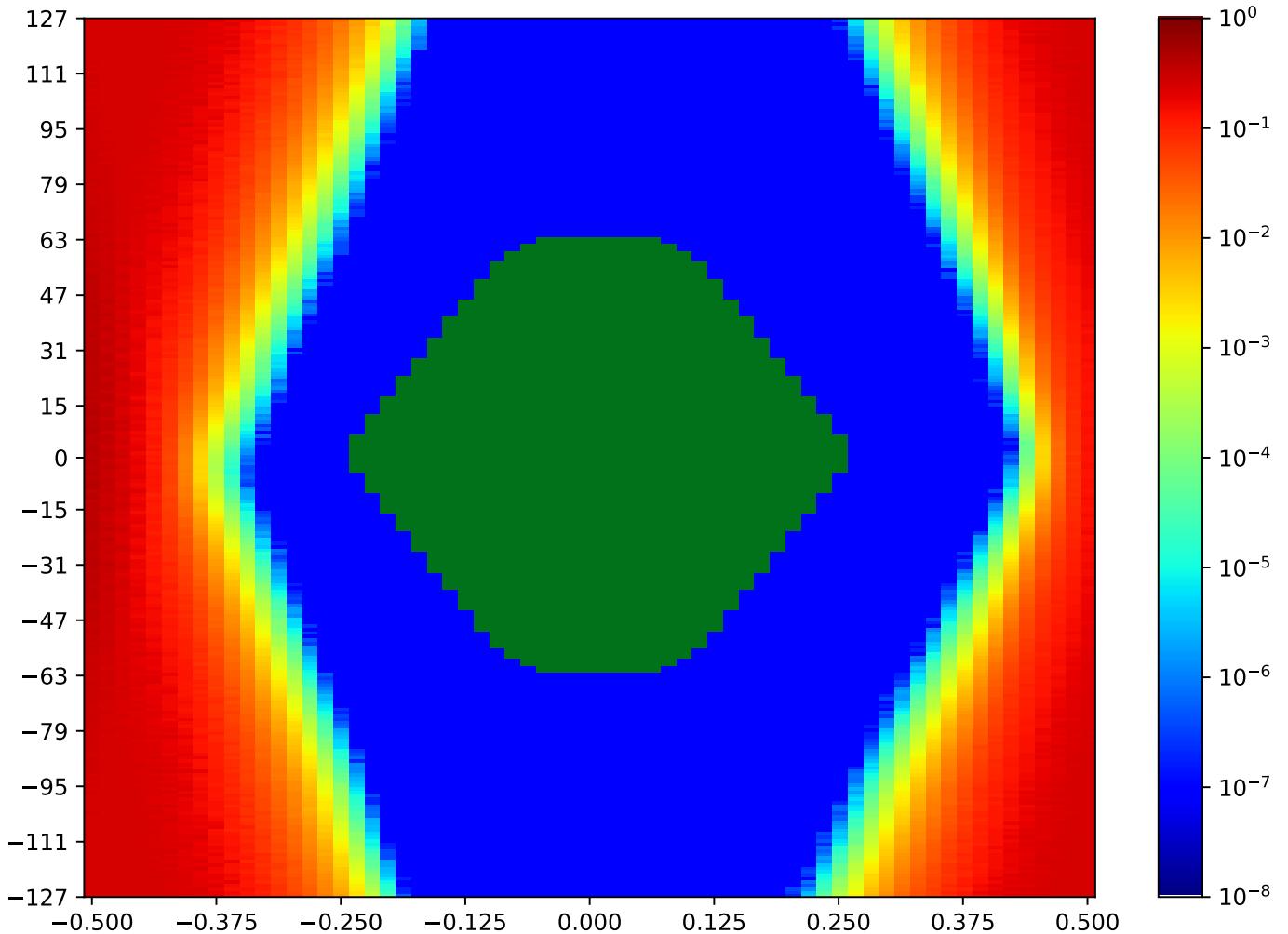


Figure 3.78: MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.10 MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

Table 3.71: MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:53:26		2018-Jan-23 23:53:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9277	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

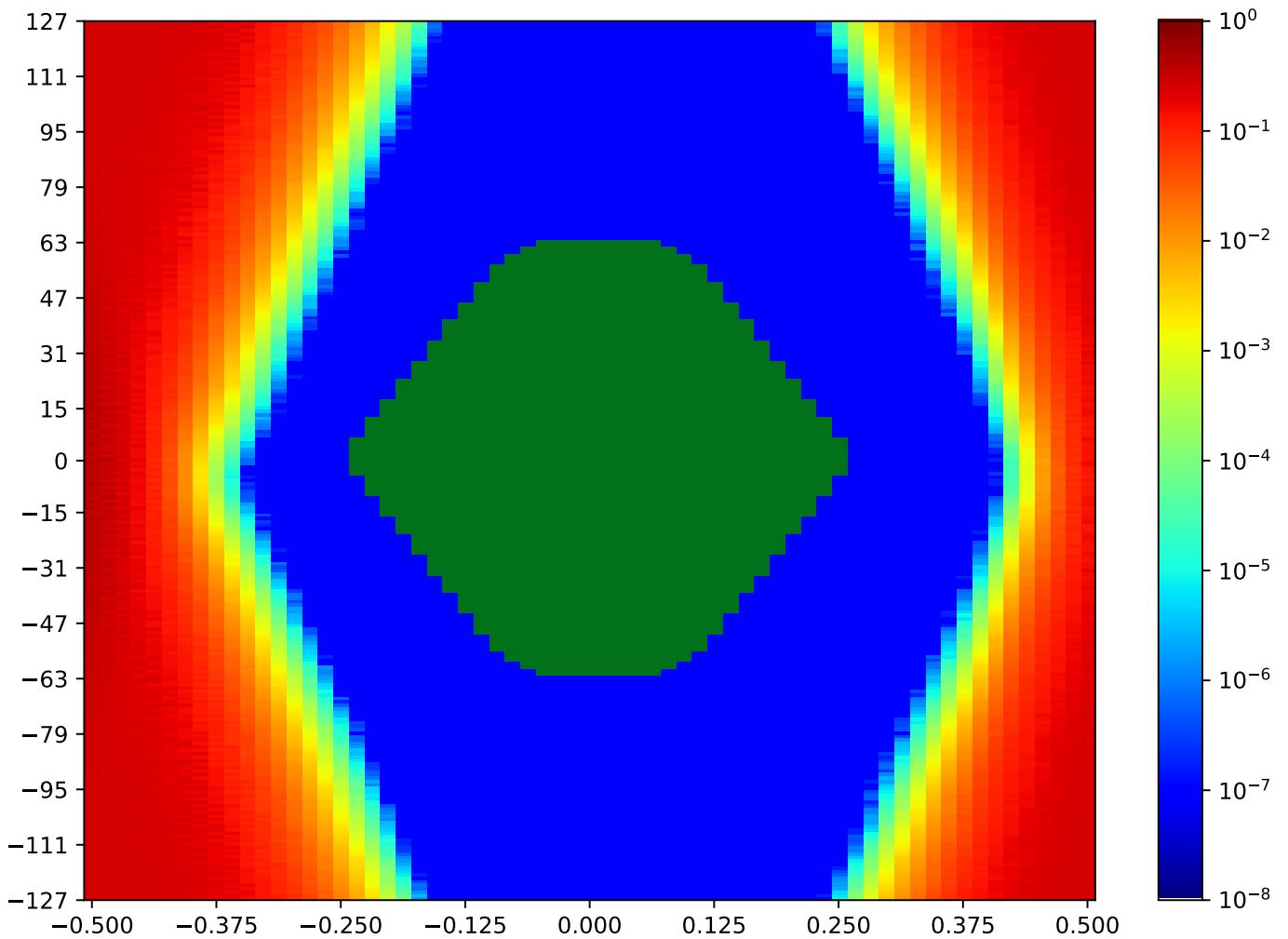


Figure 3.79: MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.11 MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

Table 3.72: MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:53:47		2018-Jan-23 23:54:07	
Reset RX	OA	HO		HO (%)	
true	8367	47		72.31%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

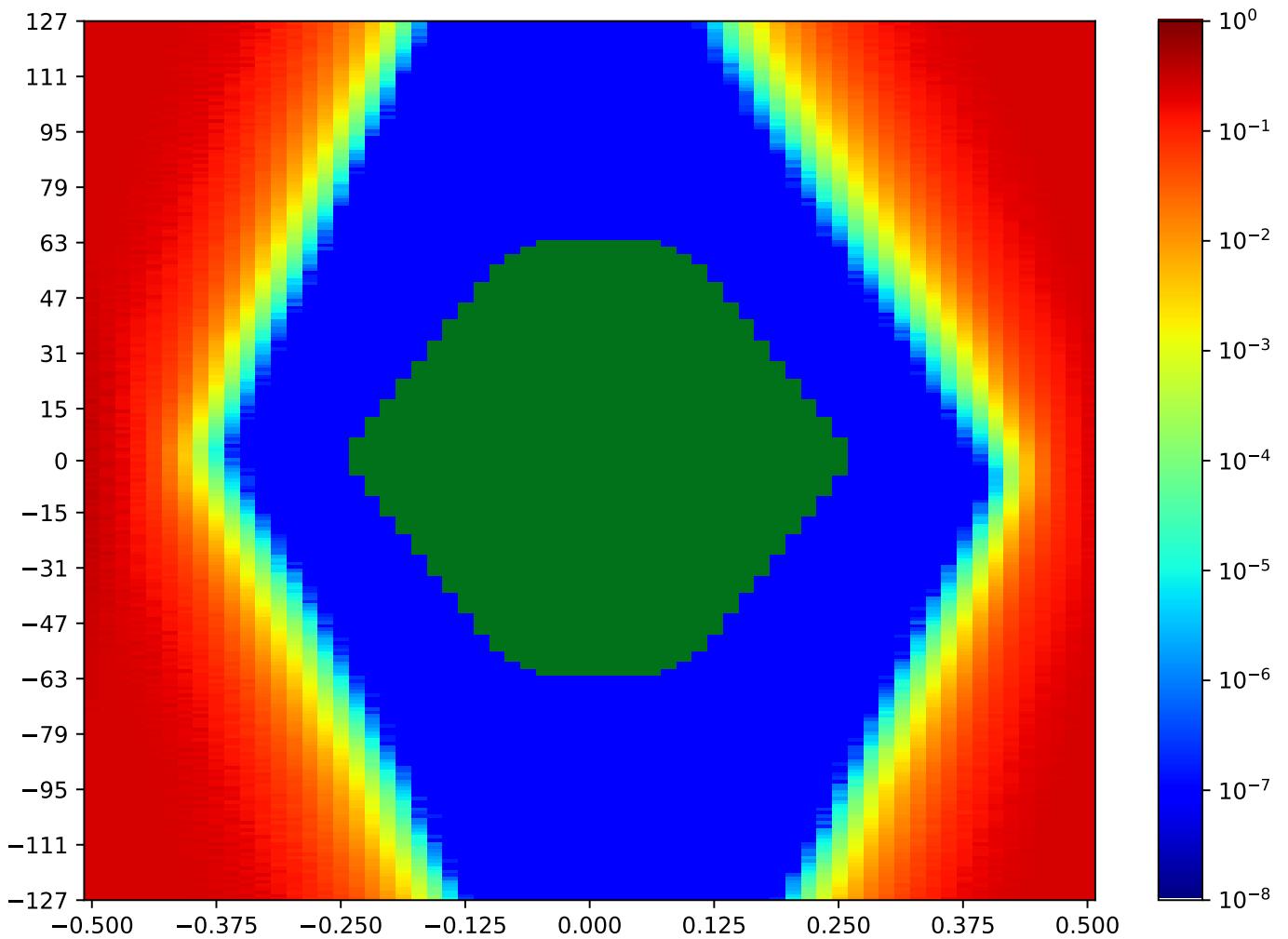


Figure 3.80: MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.12 MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

Table 3.73: MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:54:07		2018-Jan-23 23:54:28	
Reset RX	OA	HO		HO (%)	
true	9246	48		73.85%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

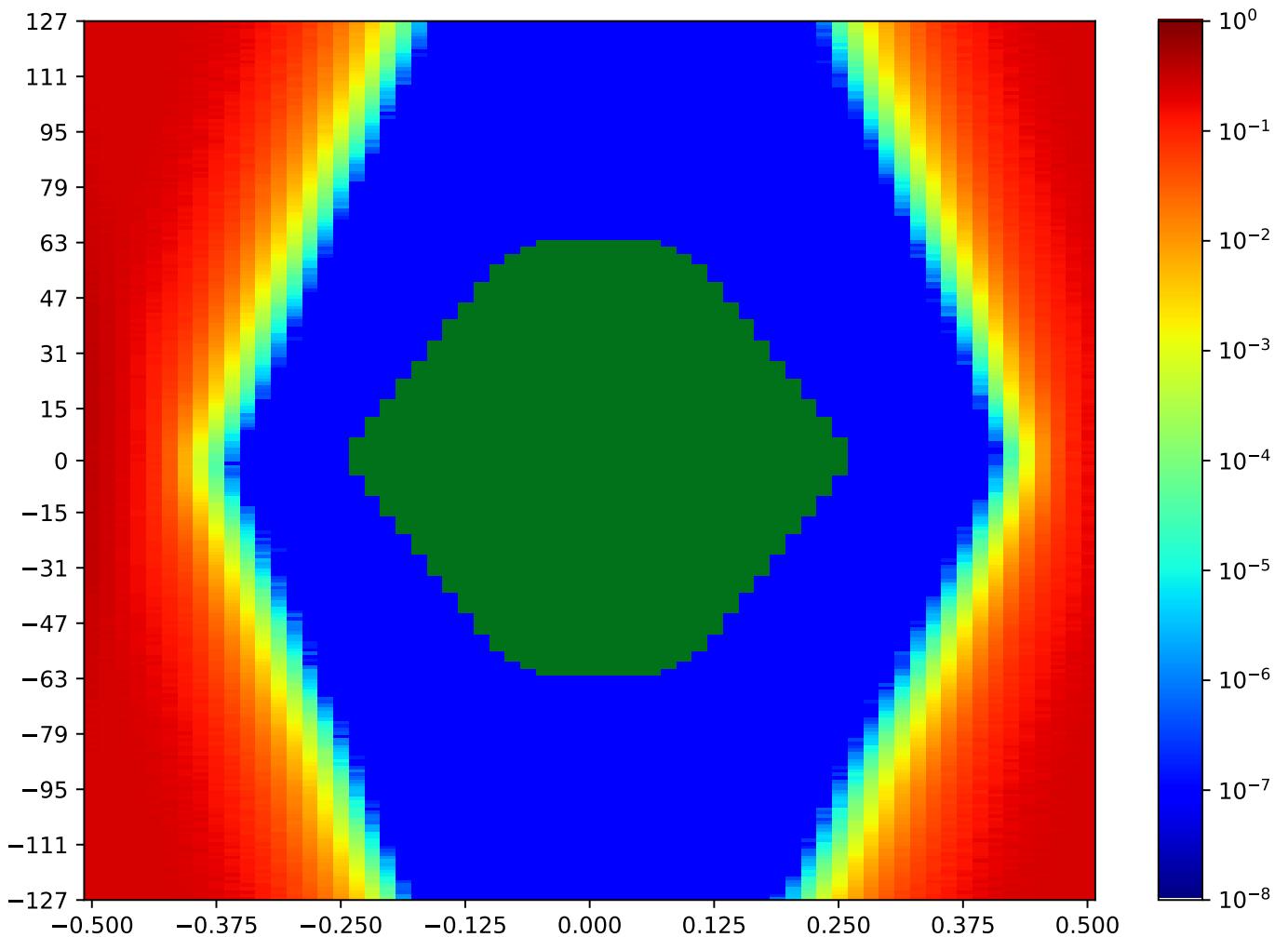


Figure 3.81: MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.13 MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

Table 3.74: MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:54:28		2018-Jan-23 23:54:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9712	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

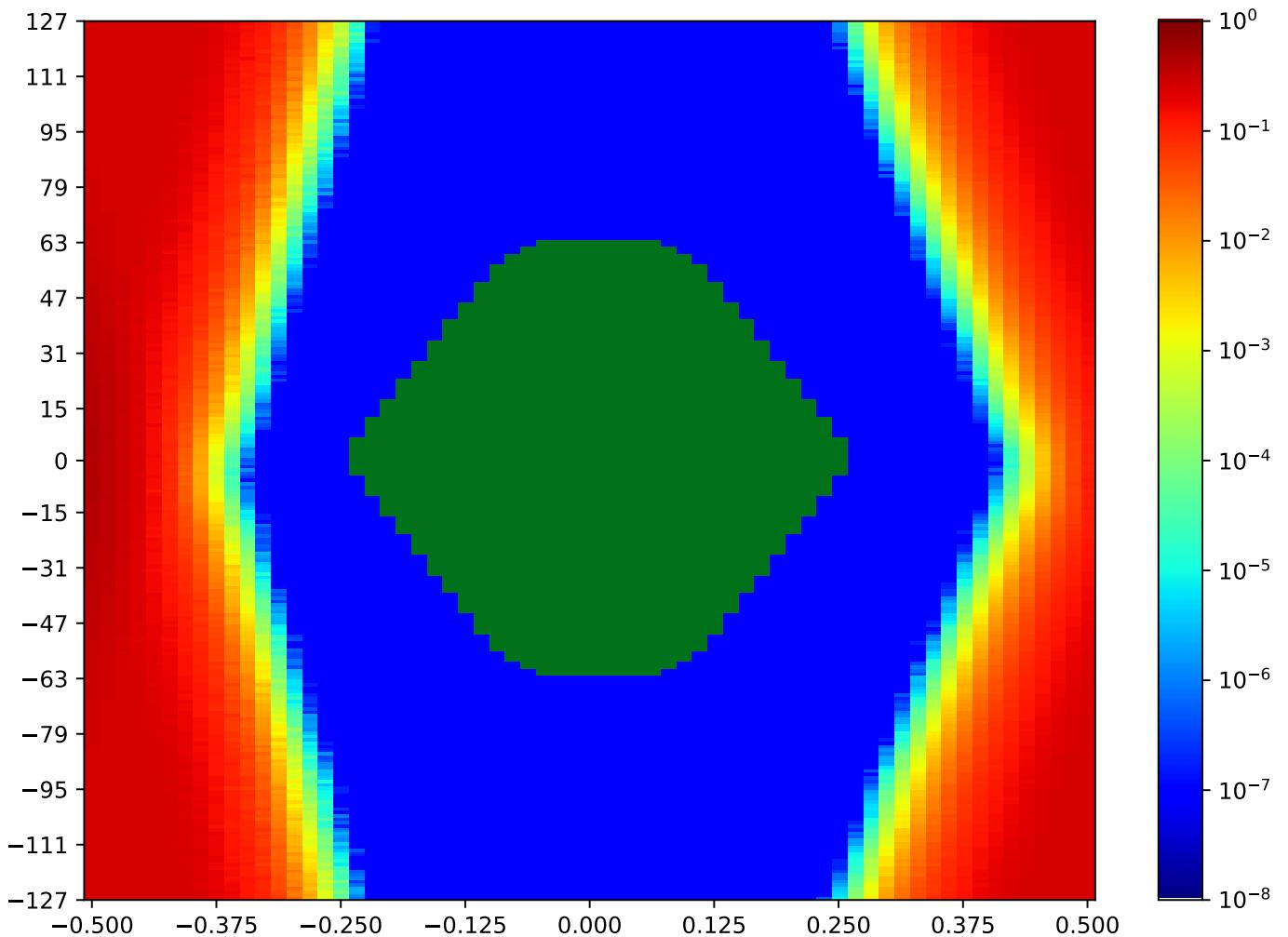


Figure 3.82: MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.14 MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

Table 3.75: MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:54:49		2018-Jan-23 23:55:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10451	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

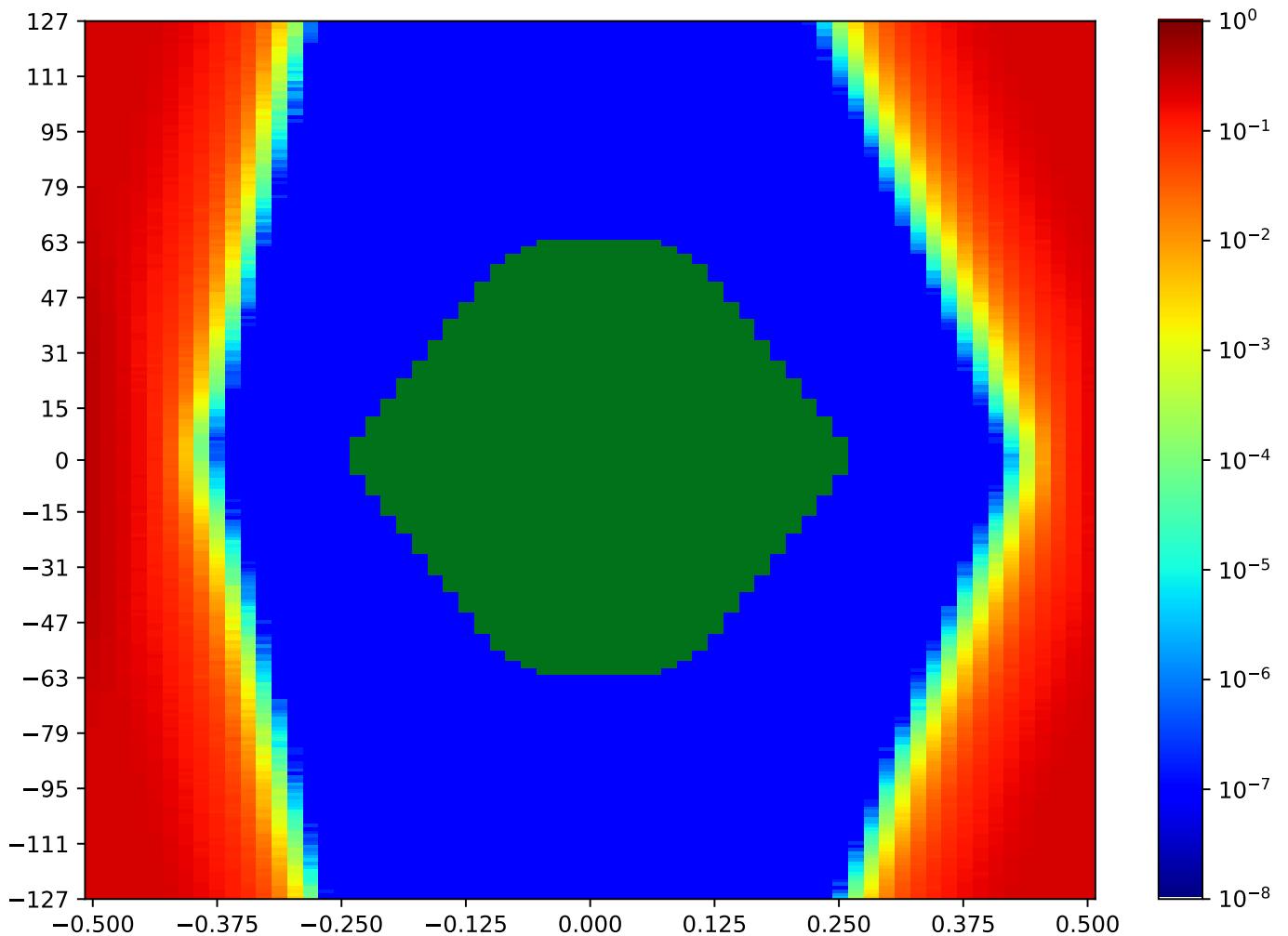


Figure 3.83: MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.15 MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

Table 3.76: MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:55:09		2018-Jan-23 23:55:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9526	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

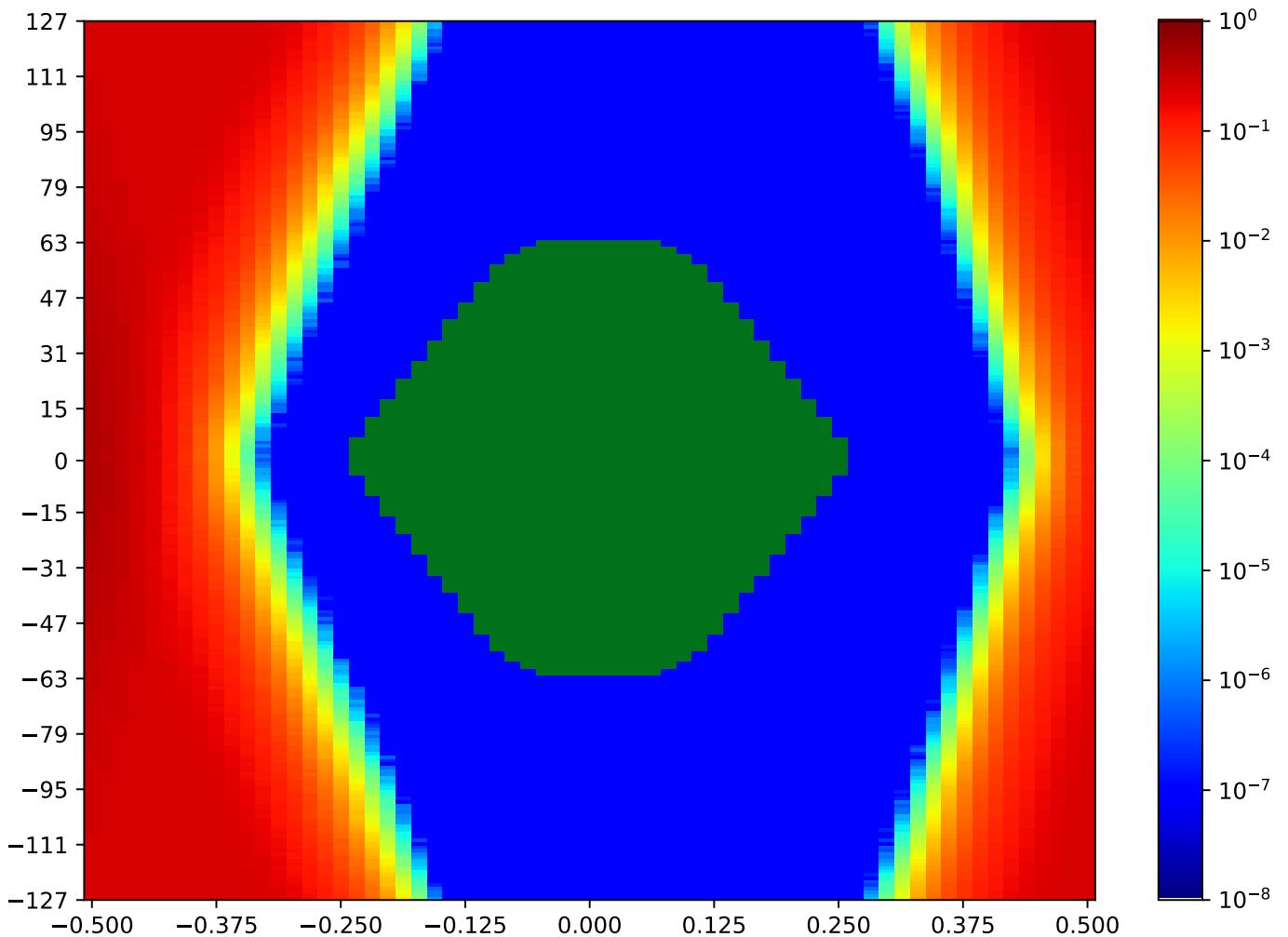


Figure 3.84: MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.16 MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

Table 3.77: MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:55:30		2018-Jan-23 23:55:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9962	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

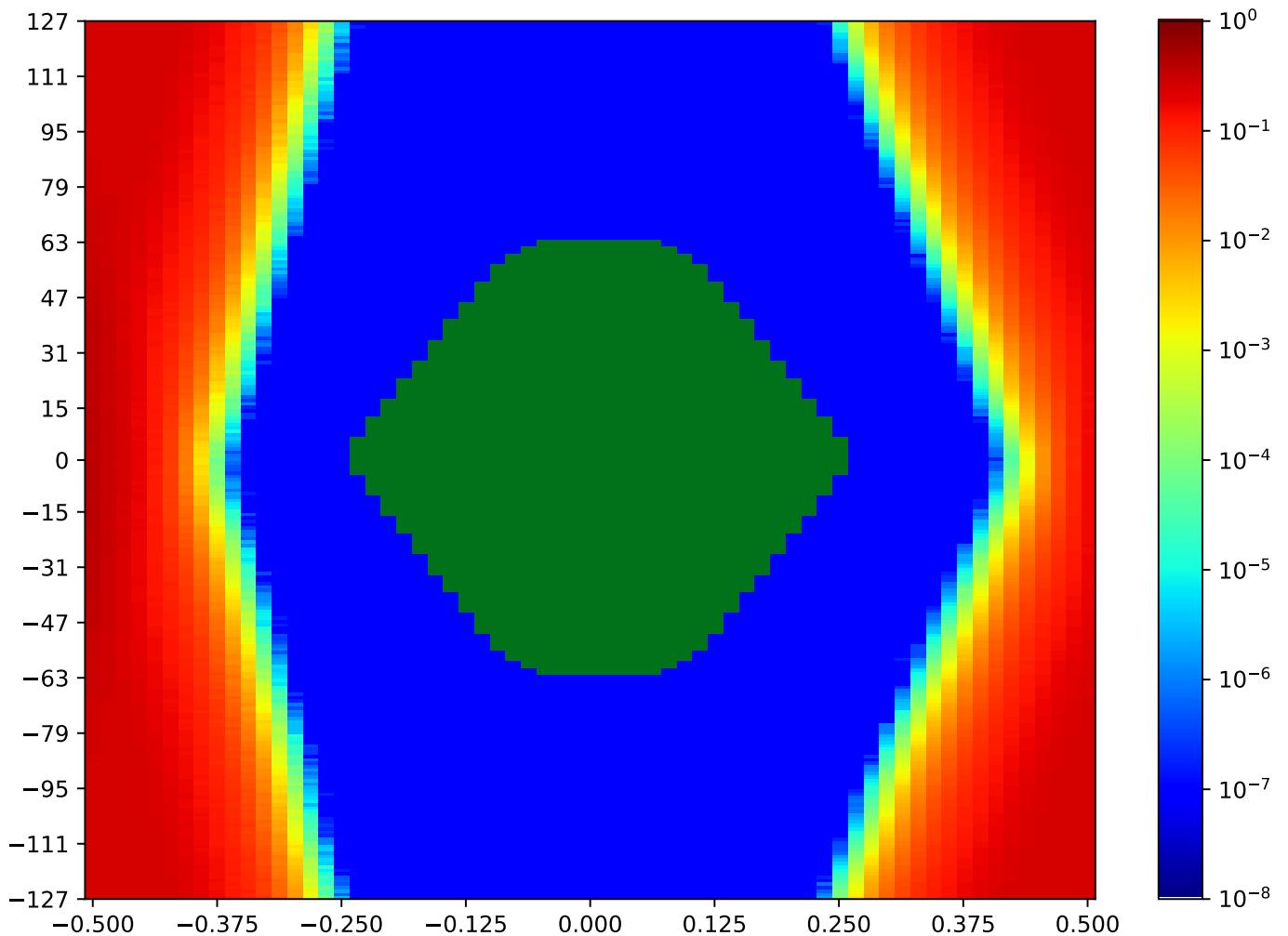


Figure 3.85: MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.17 MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

Table 3.78: MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:55:51		2018-Jan-23 23:56:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9035	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

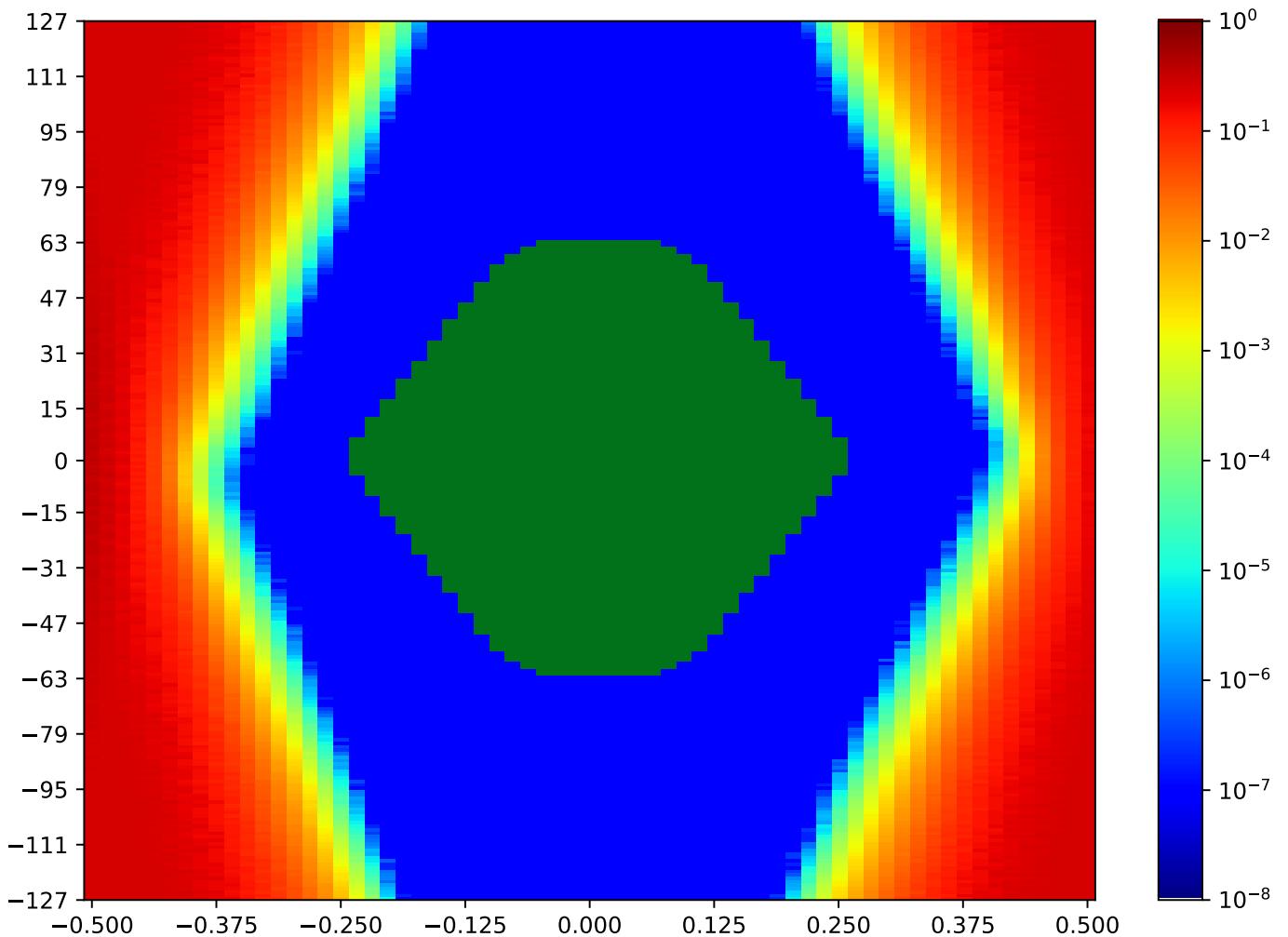


Figure 3.86: MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.18 MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

Table 3.79: MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:56:11		2018-Jan-23 23:56:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9399	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

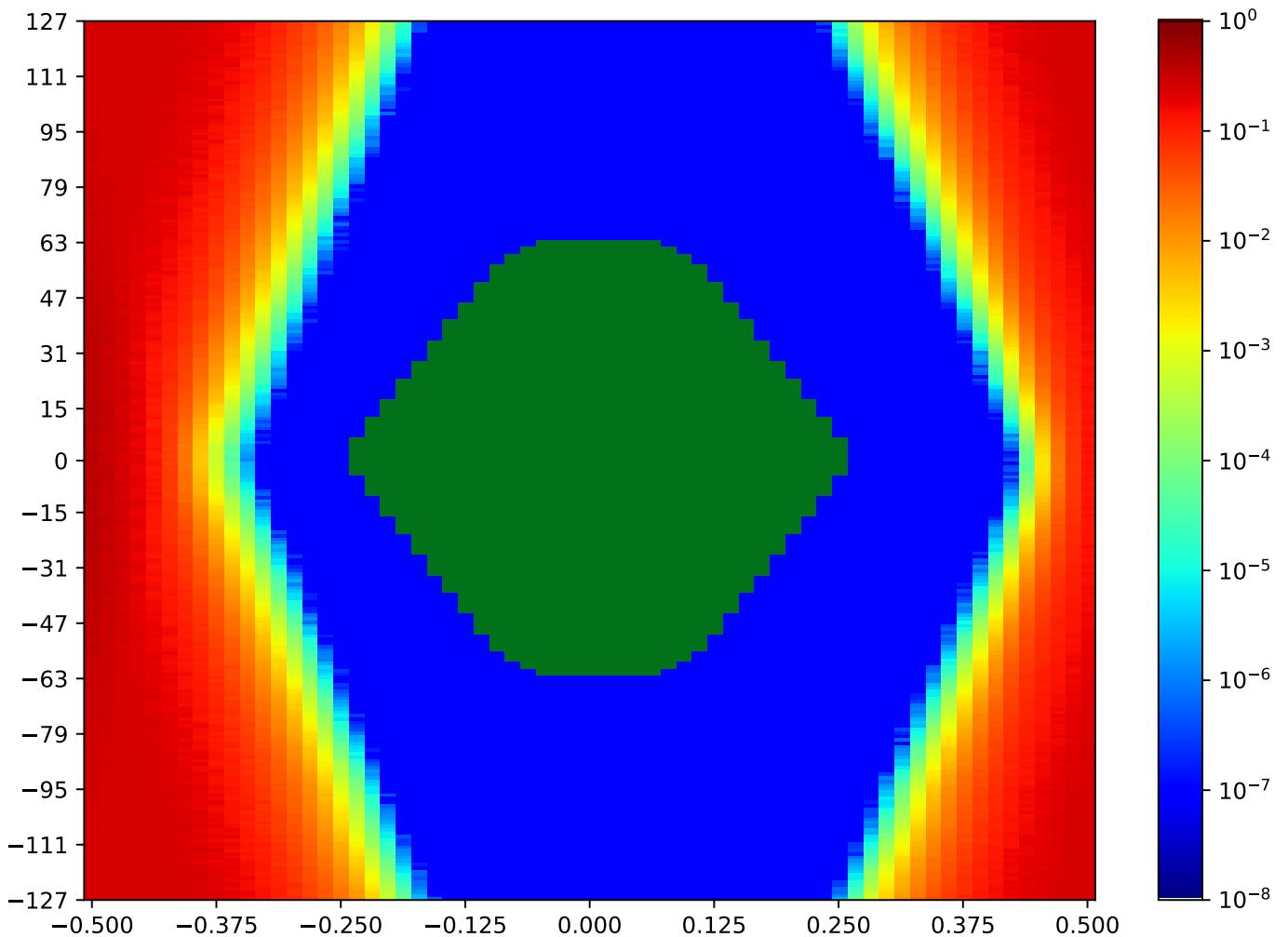


Figure 3.87: MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.19 MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

Table 3.80: MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:56:31		2018-Jan-23 23:56:51	
Reset RX	OA	HO		HO (%)	
true	9075	46		70.77%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

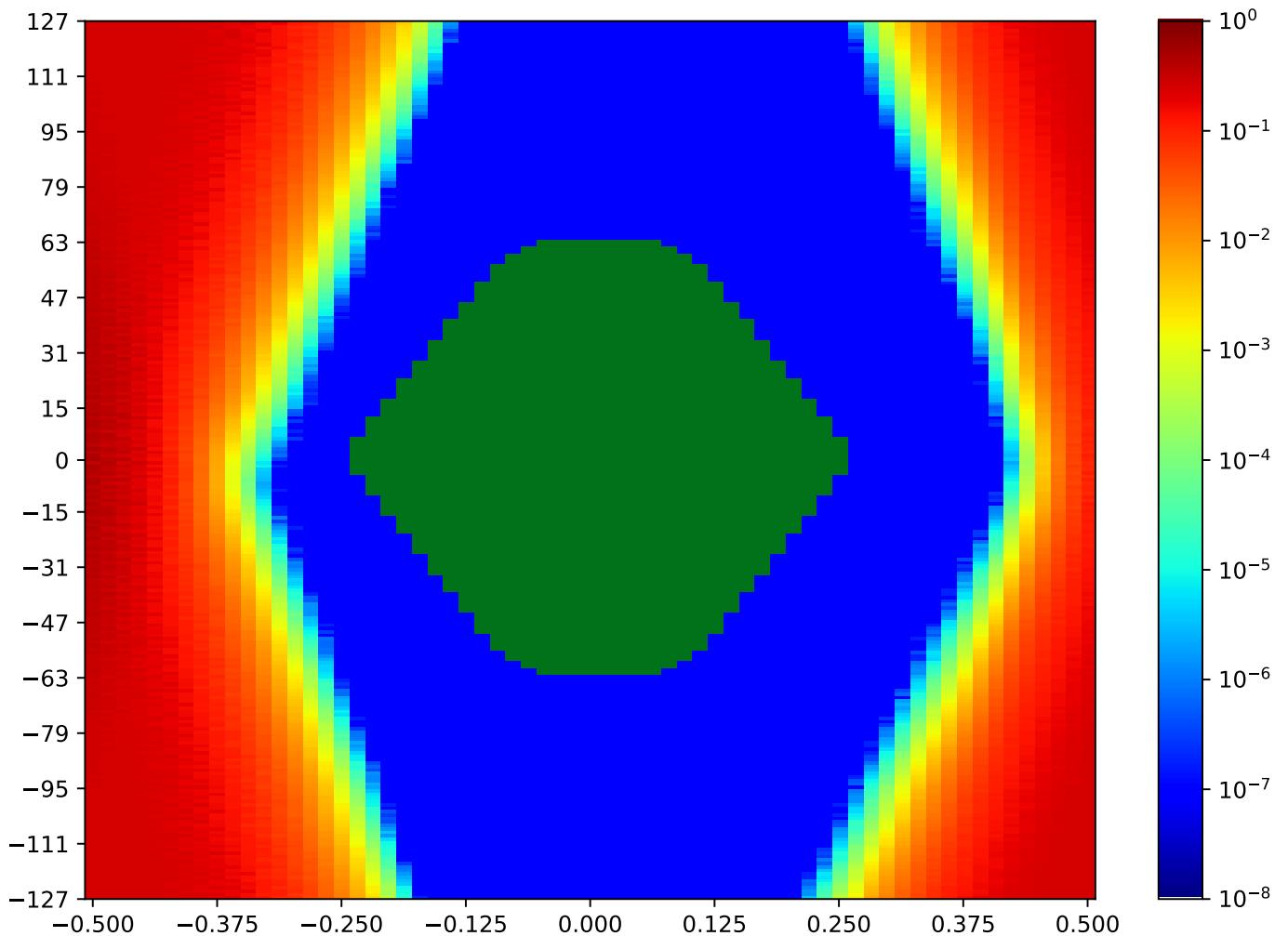


Figure 3.88: MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.20 MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

Table 3.81: MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:56:51		2018-Jan-23 23:57:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9084	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

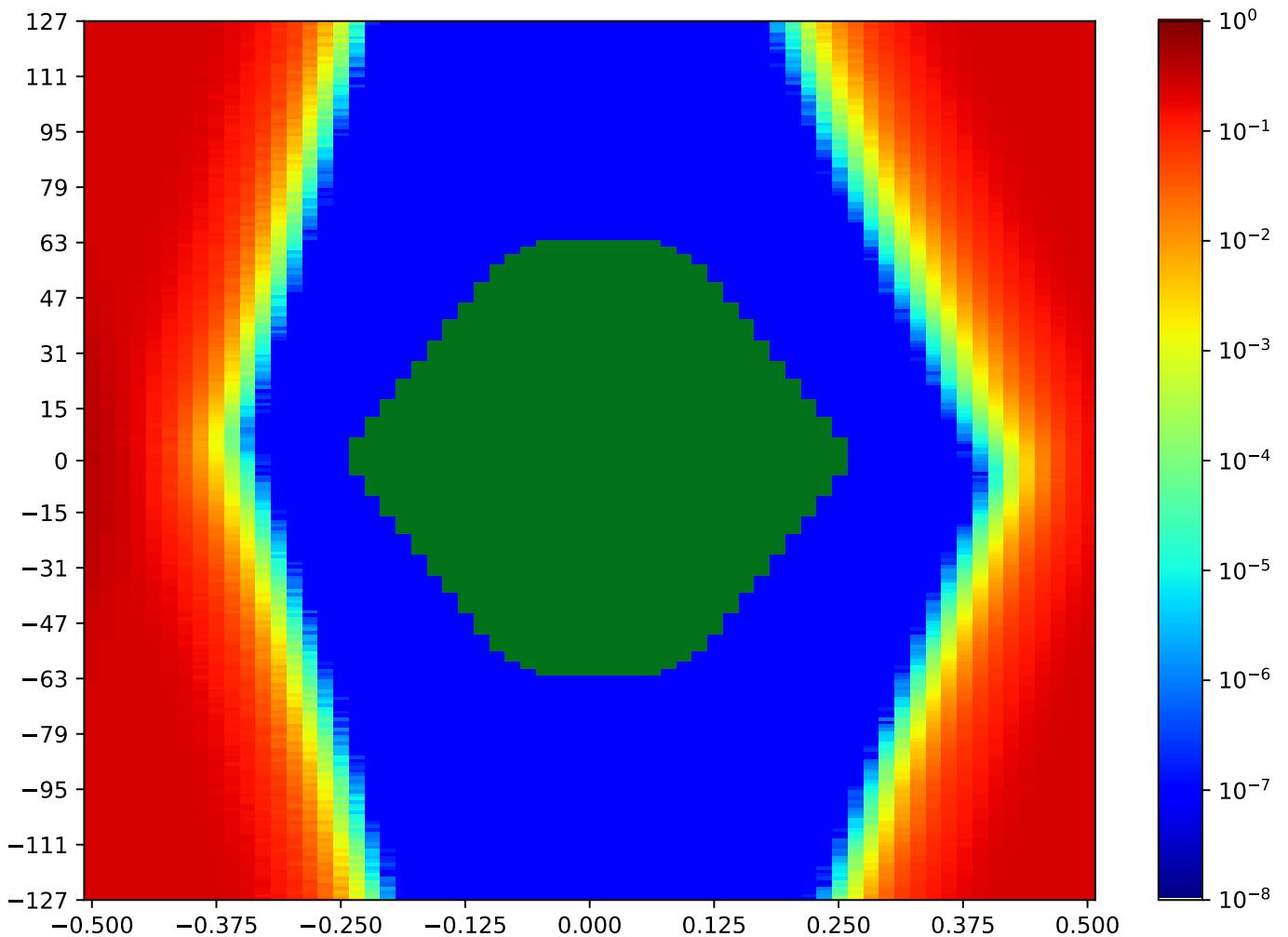


Figure 3.89: MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.21 MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

Table 3.82: MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:57:11		2018-Jan-23 23:57:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10245	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

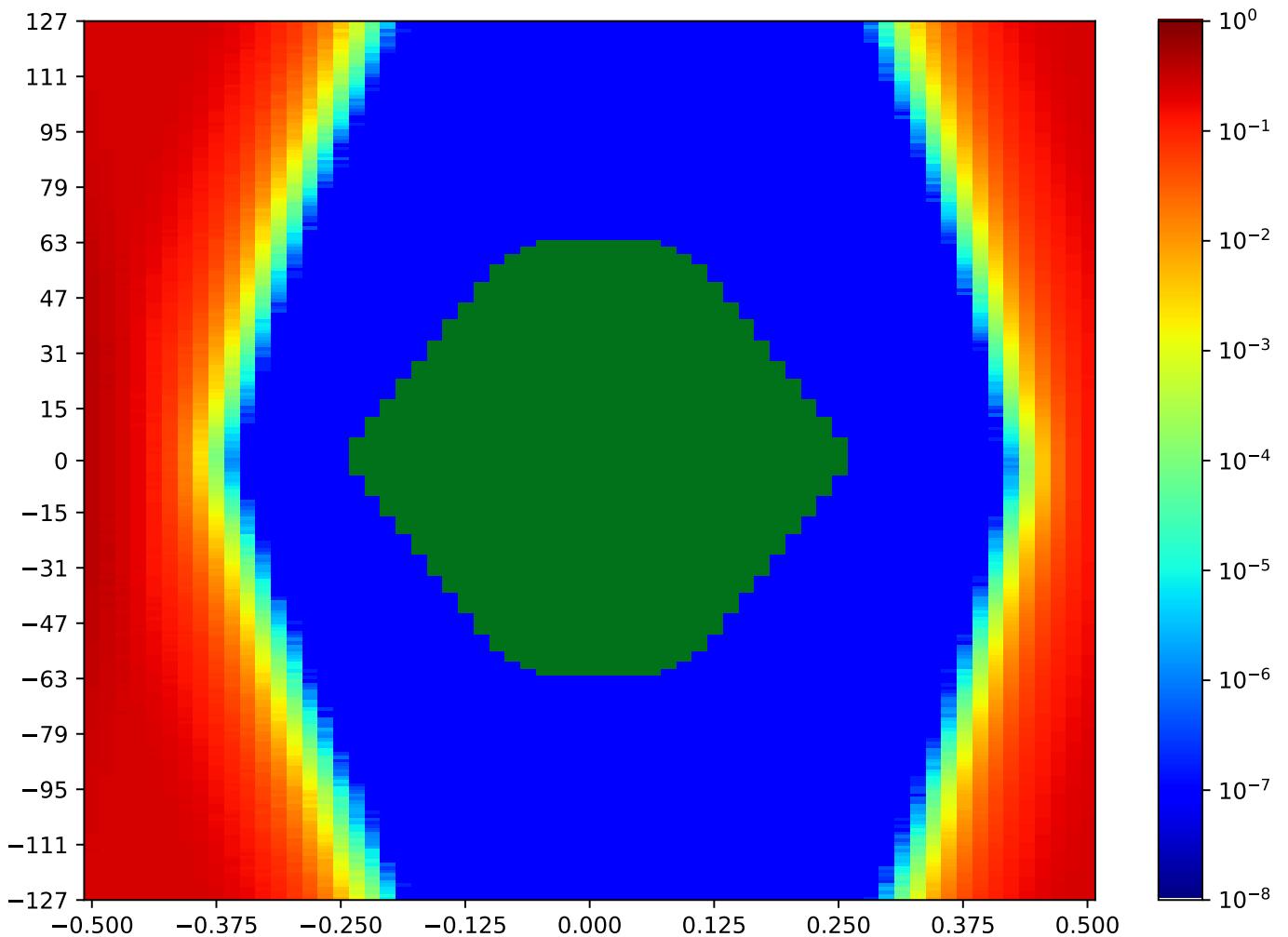


Figure 3.90: MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.22 MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

Table 3.83: MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:57:32		2018-Jan-23 23:57:52	
Reset RX	OA	HO		HO (%)	
true	8343	46		70.77%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

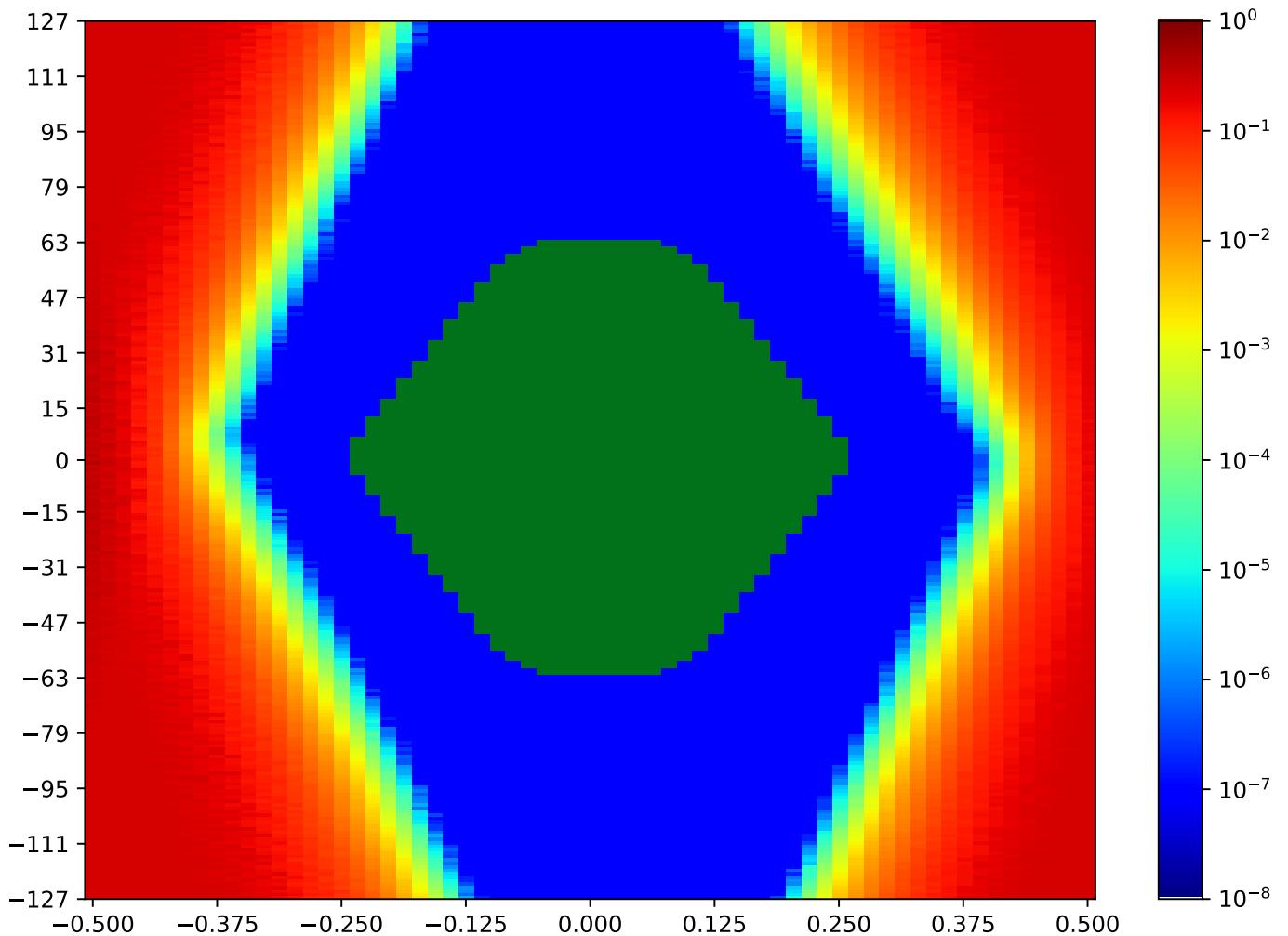


Figure 3.91: MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.23 MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

Table 3.84: MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:57:52		2018-Jan-23 23:58:12	
Reset RX	OA	HO		HO (%)	
true	10865	50		76.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

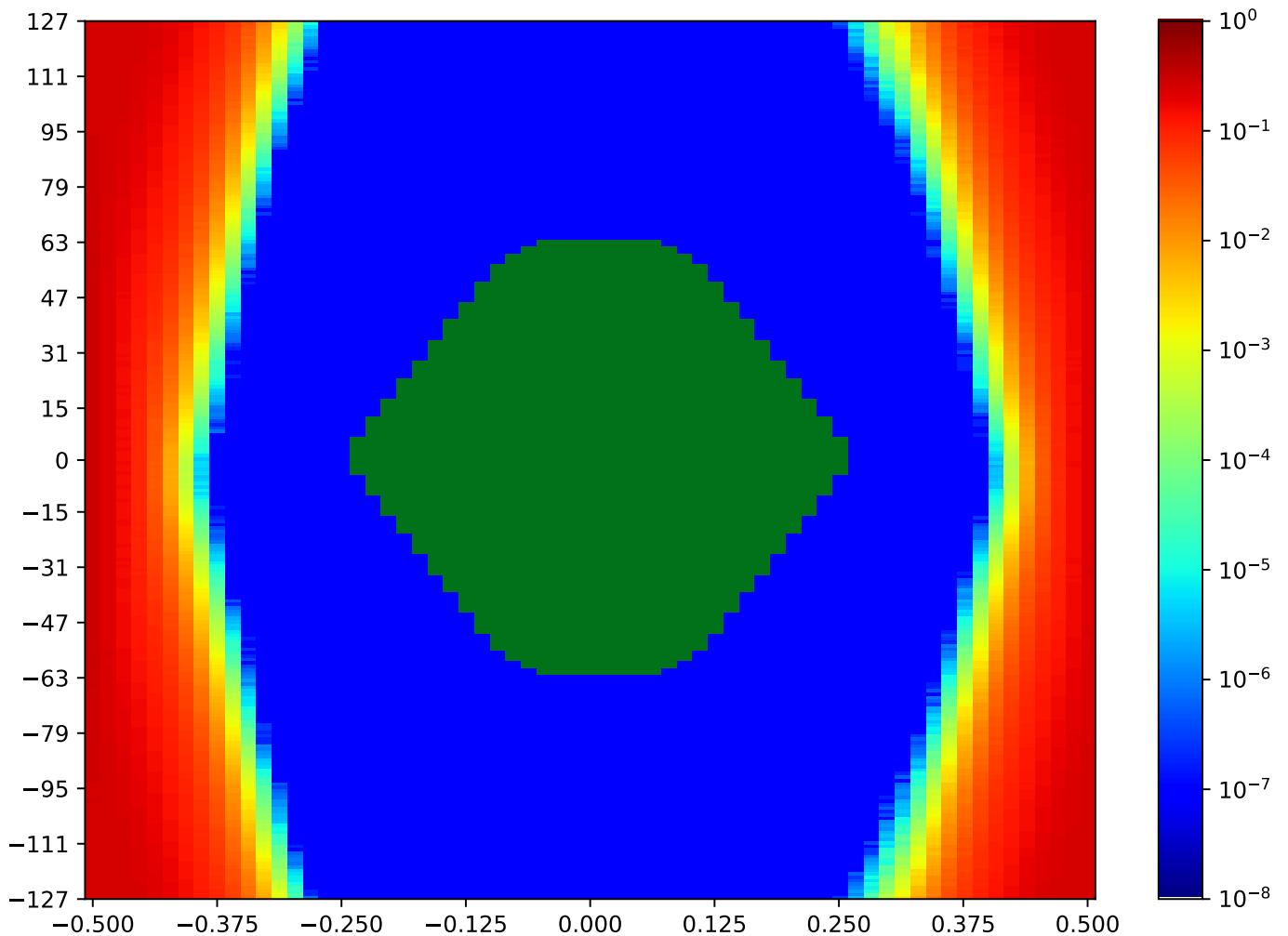


Figure 3.92: MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.24 MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

Table 3.85: MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:58:12		2018-Jan-23 23:58:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10234	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

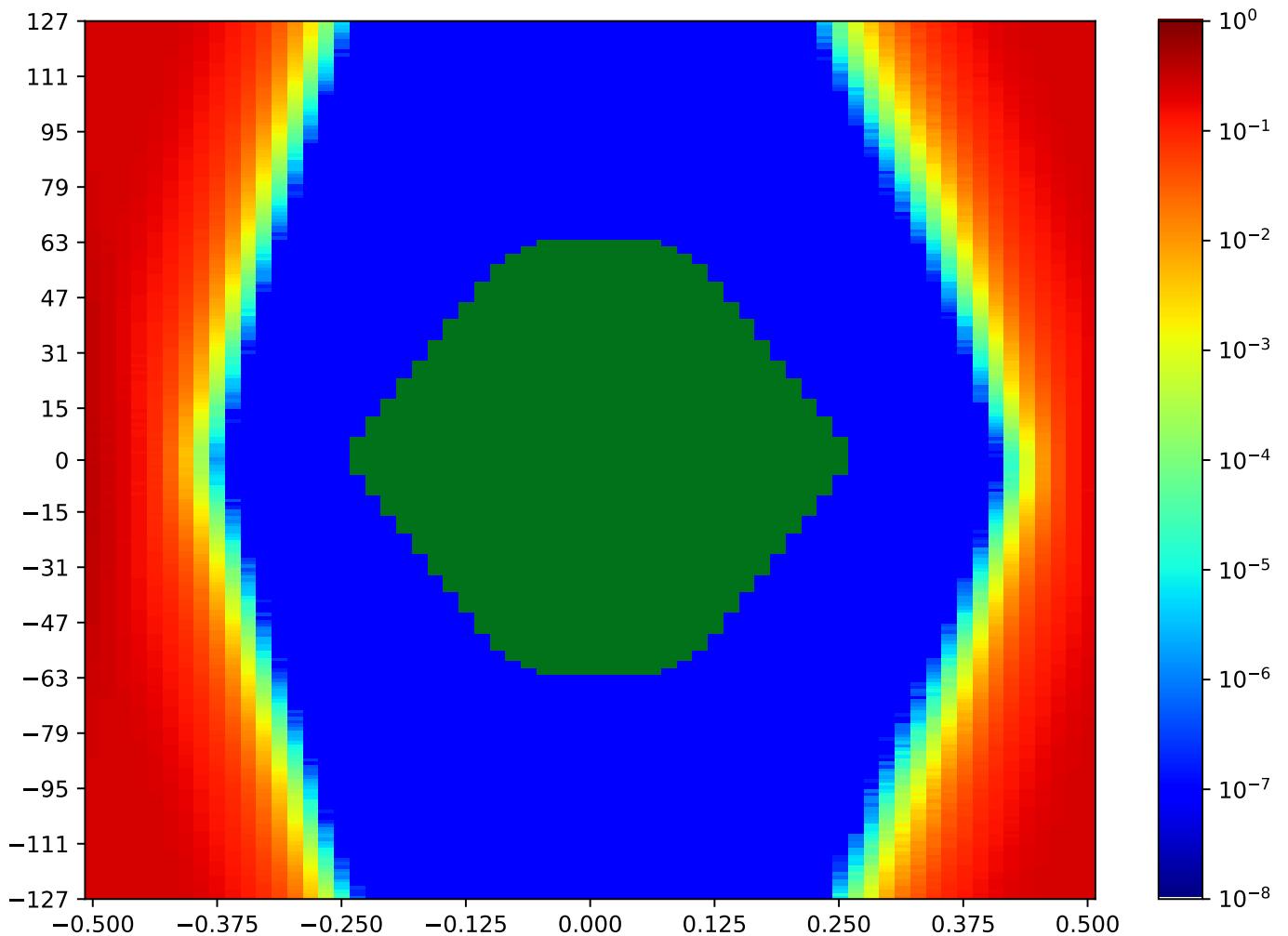


Figure 3.93: MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.25 MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

Table 3.86: MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:58:33		2018-Jan-23 23:58:53	
Reset RX	OA	HO		HO (%)	
true	9128	46		70.77%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

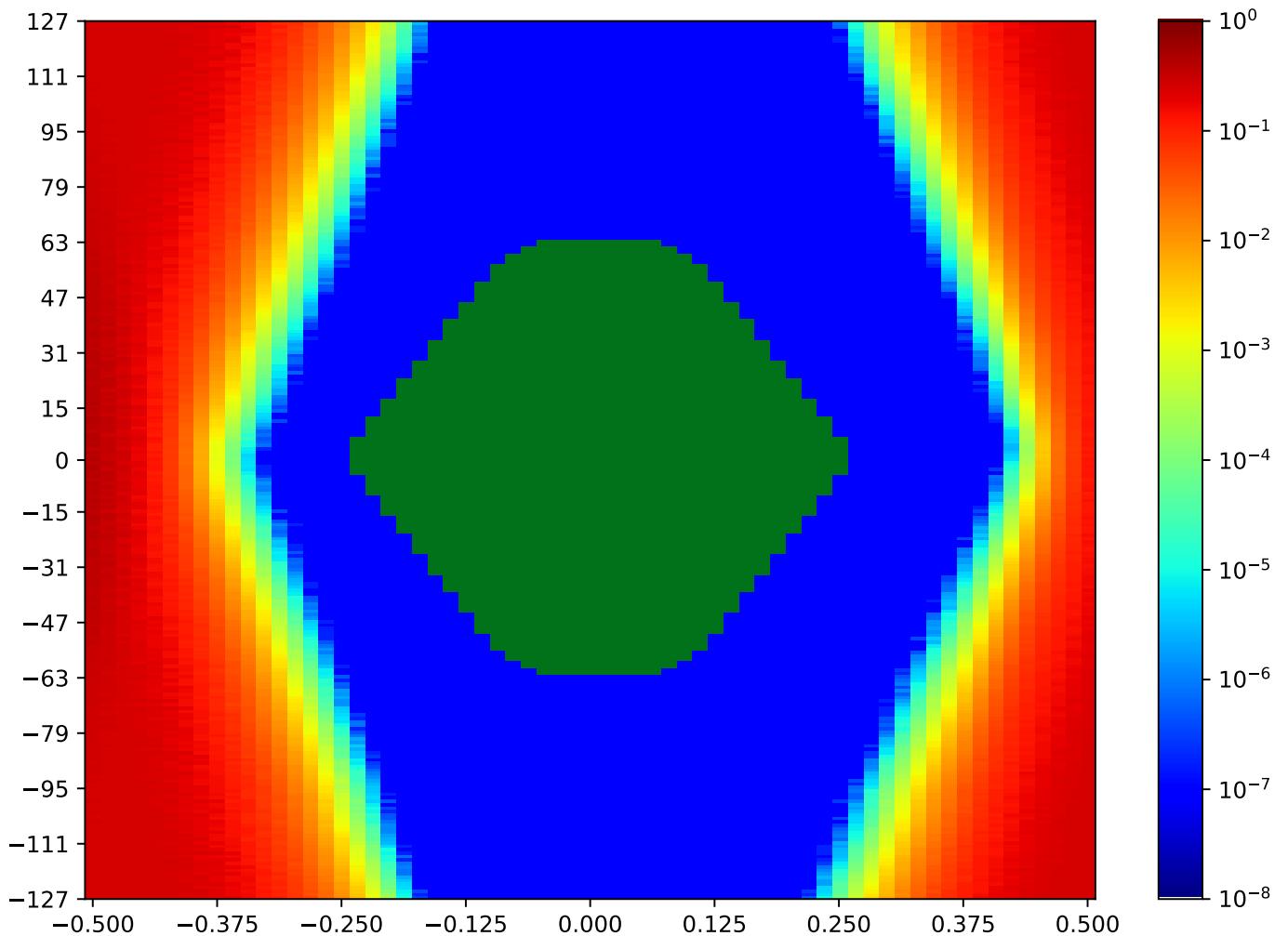


Figure 3.94: MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.26 MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

Table 3.87: MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:58:53		2018-Jan-23 23:59:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10753	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

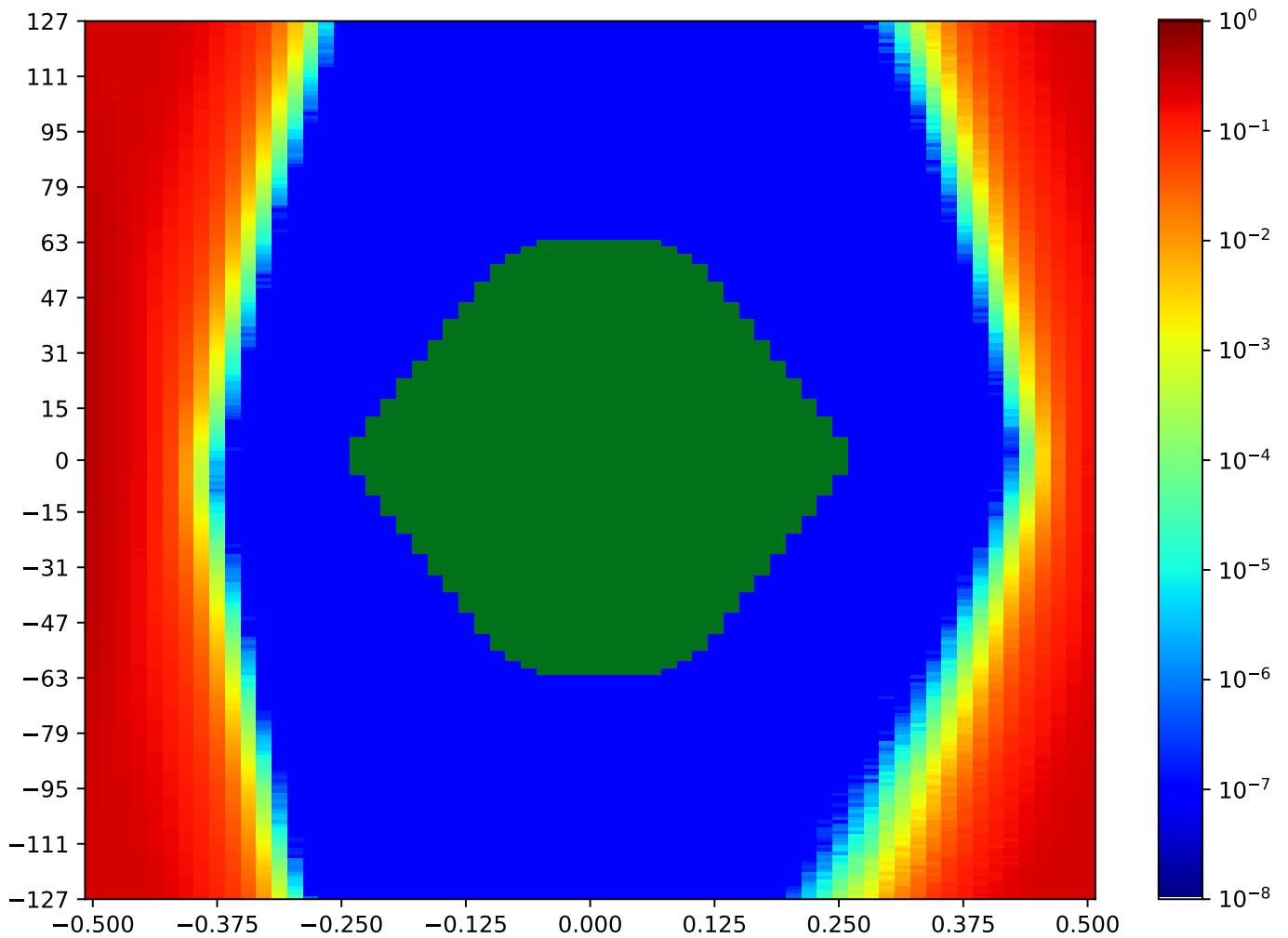


Figure 3.95: MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.27 MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

Table 3.88: MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:59:13		2018-Jan-23 23:59:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9141	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

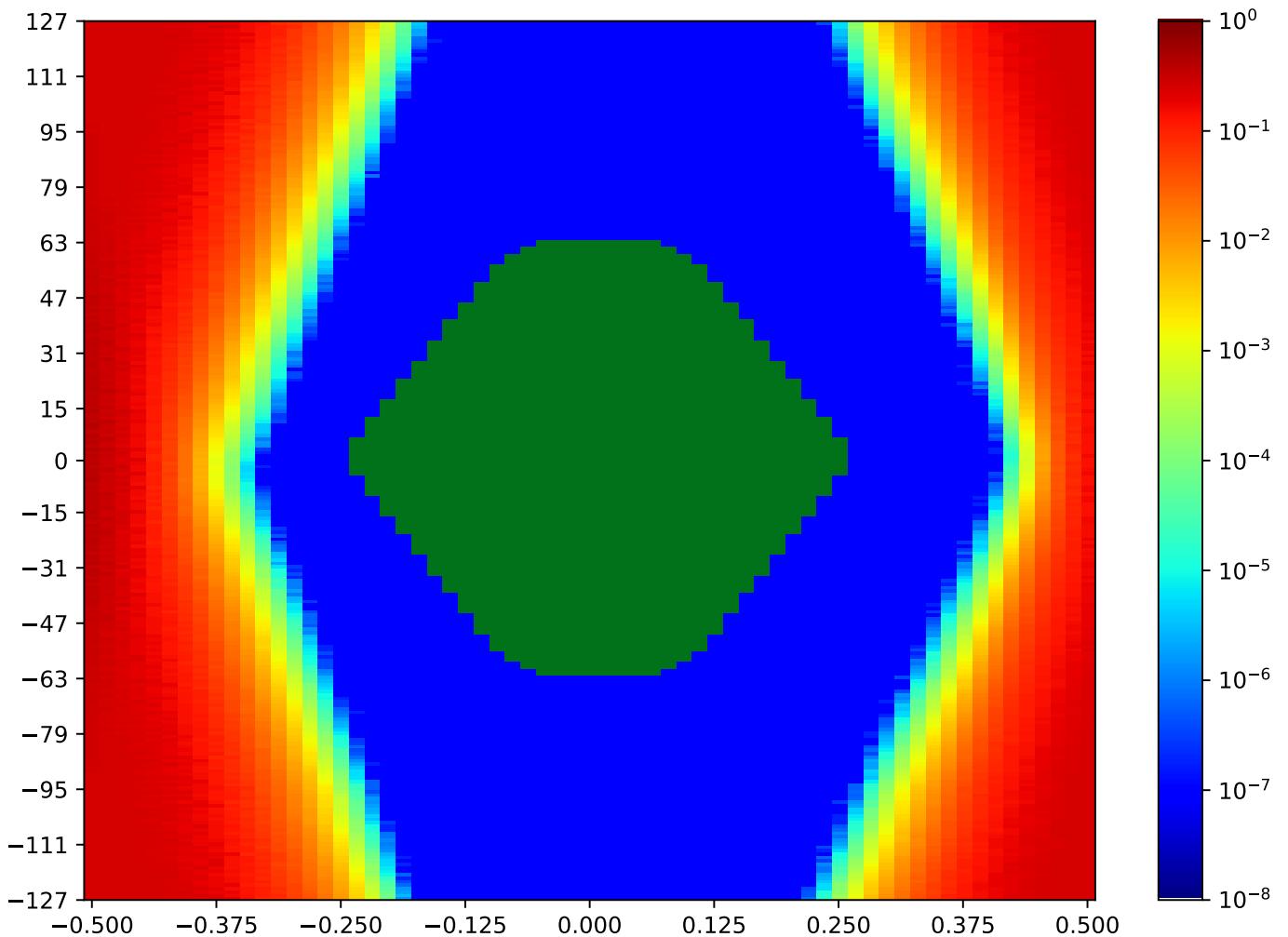


Figure 3.96: MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.8.28 MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

Table 3.89: MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-23 23:59:34		2018-Jan-23 23:59:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9552	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

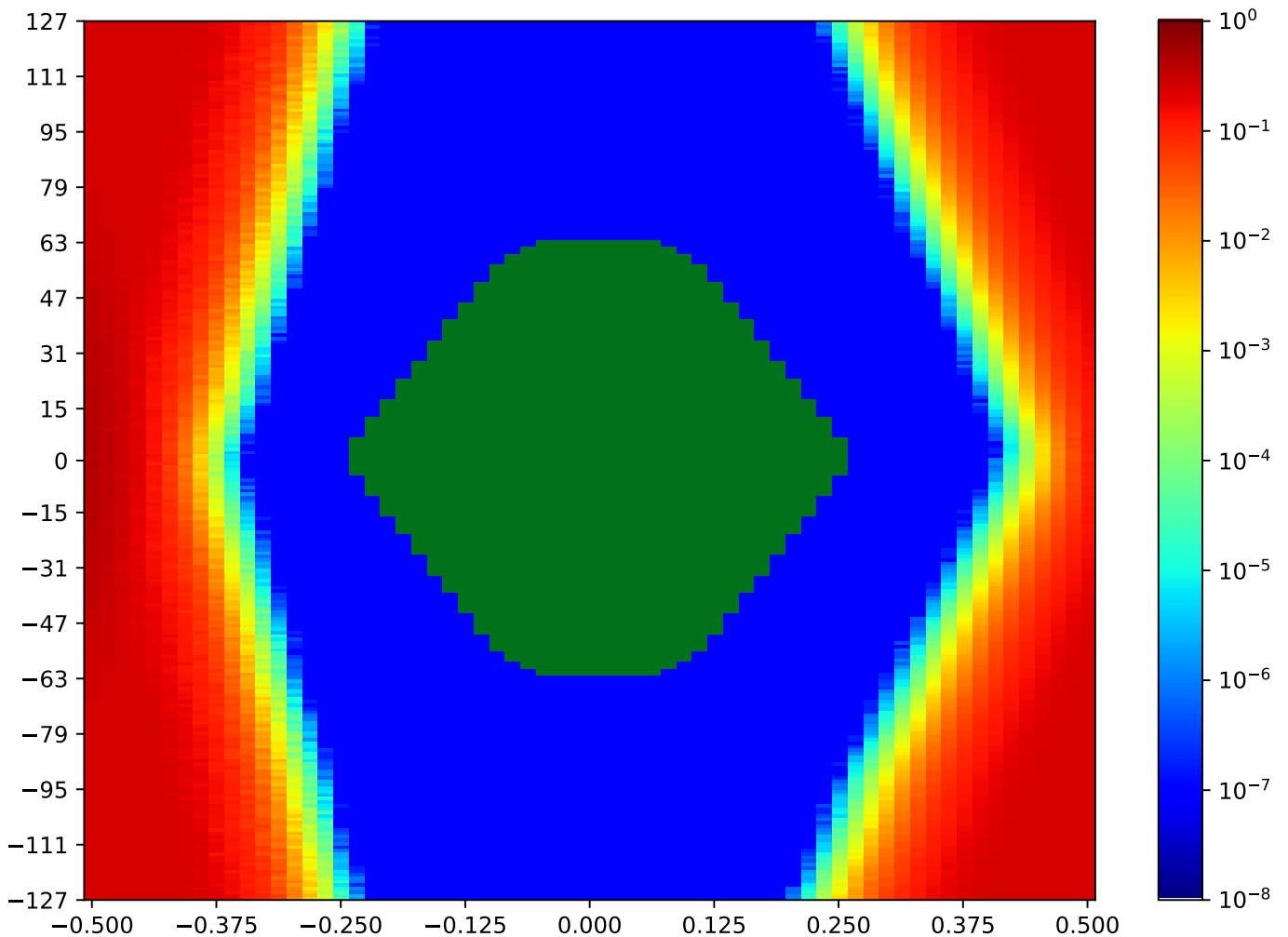


Figure 3.97: MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

Call back to summary Figure 3.69. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9 MSP_C TRP On board links

A cross-reference to Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.
Next summary Figure ??.

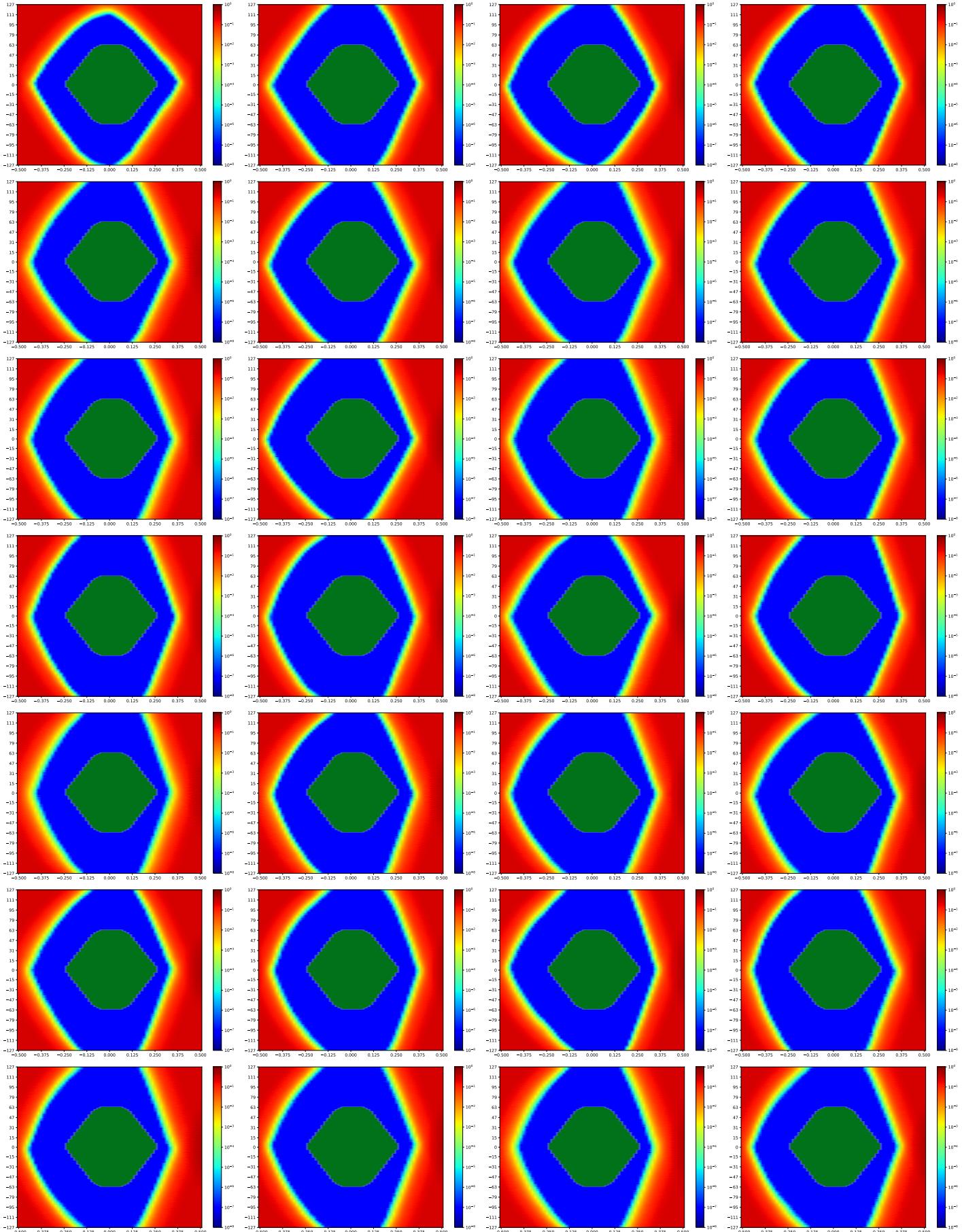


Figure 3.98: MSP_C TRP On board links

3.9.1 MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

Table 3.90: MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-23 23:59:54		2018-Jan-24 00:00:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6936	48	73.85%	236	92.55%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

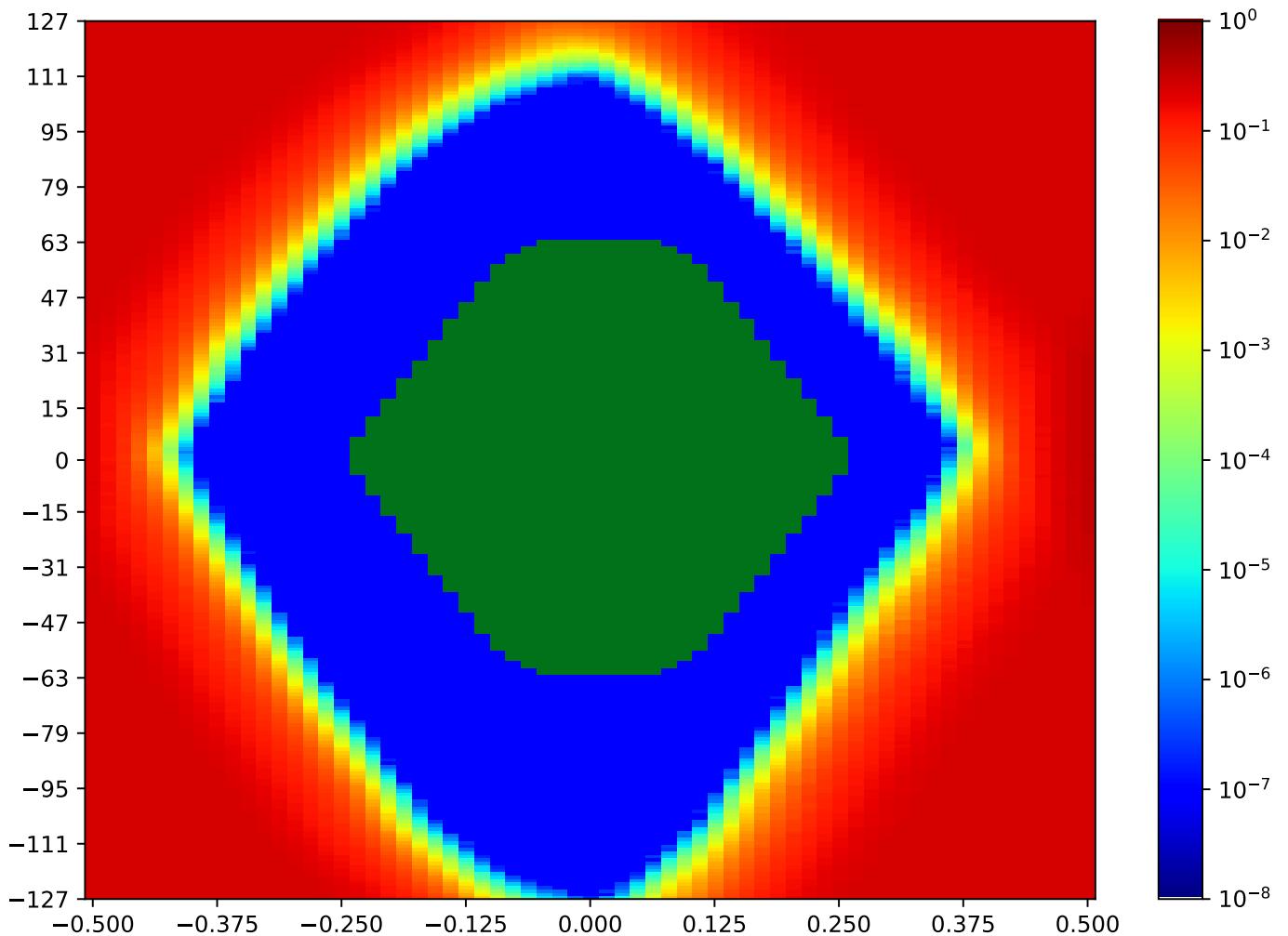


Figure 3.99: MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.2 MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

Table 3.91: MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:00:14		2018-Jan-24 00:00:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8472	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

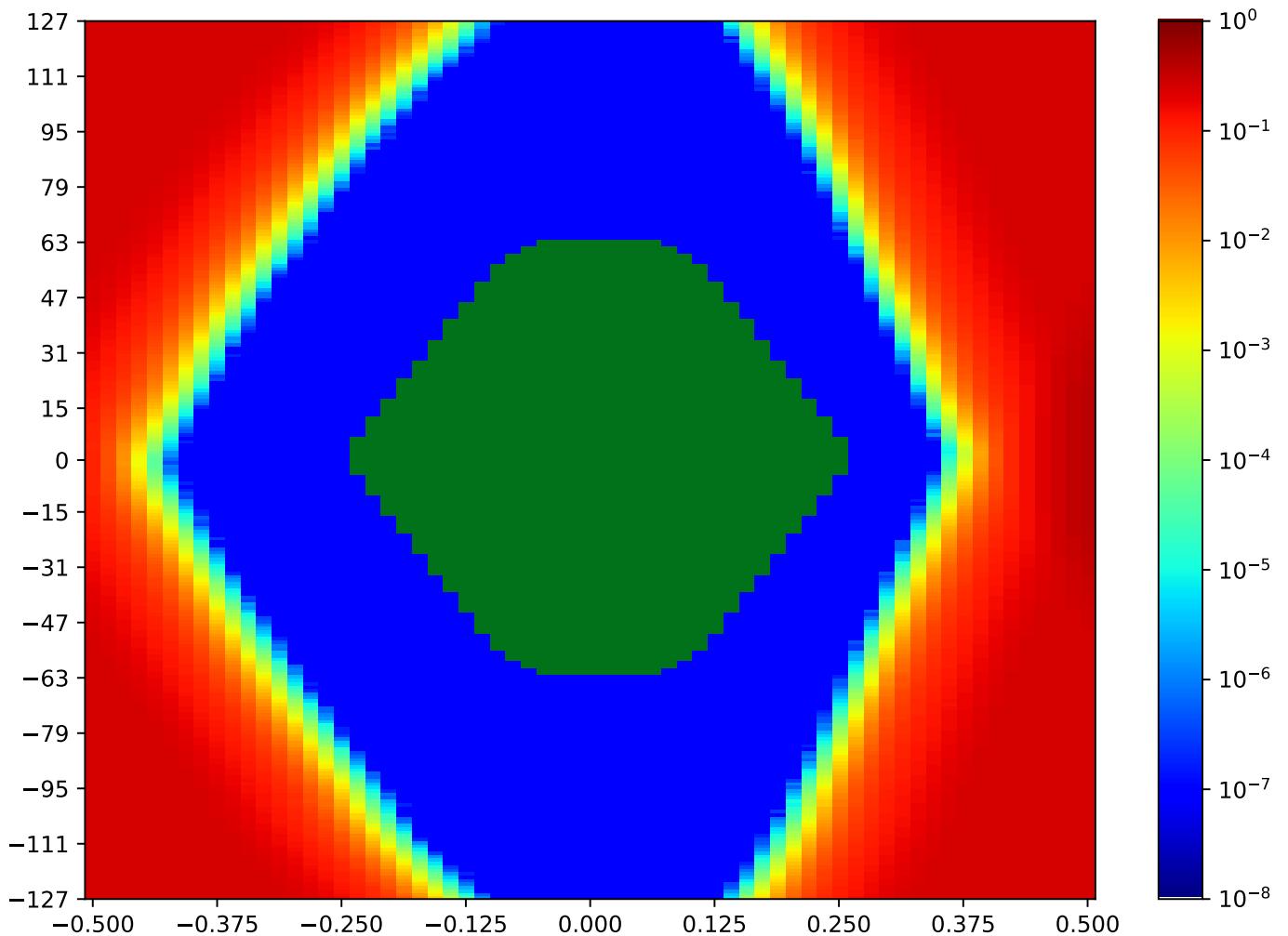


Figure 3.100: MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.3 MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

Table 3.92: MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:00:35		2018-Jan-24 00:00:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8267	49	75.38%	255	99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

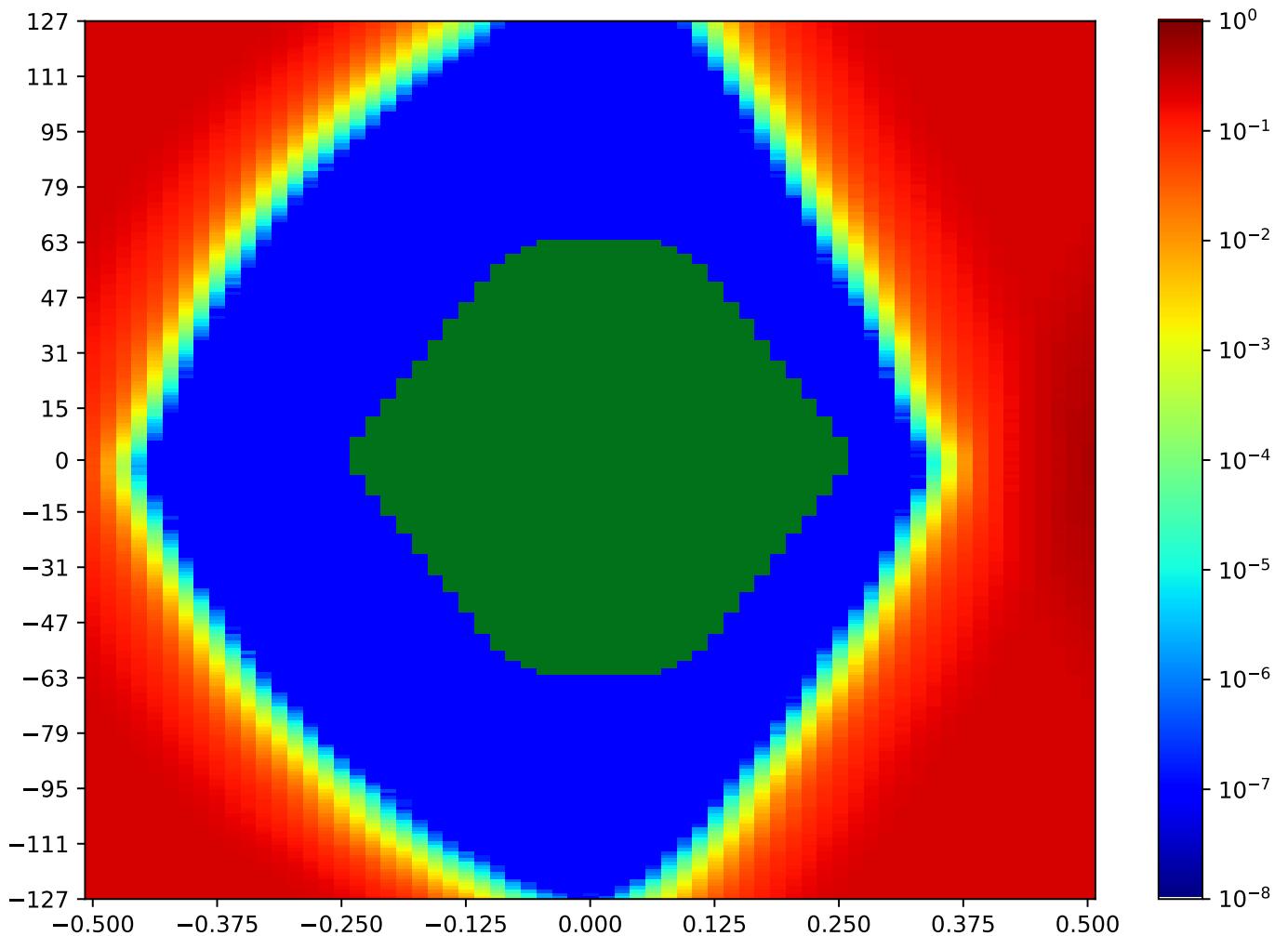


Figure 3.101: MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.4 MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

Table 3.93: MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:00:55		2018-Jan-24 00:01:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8849	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

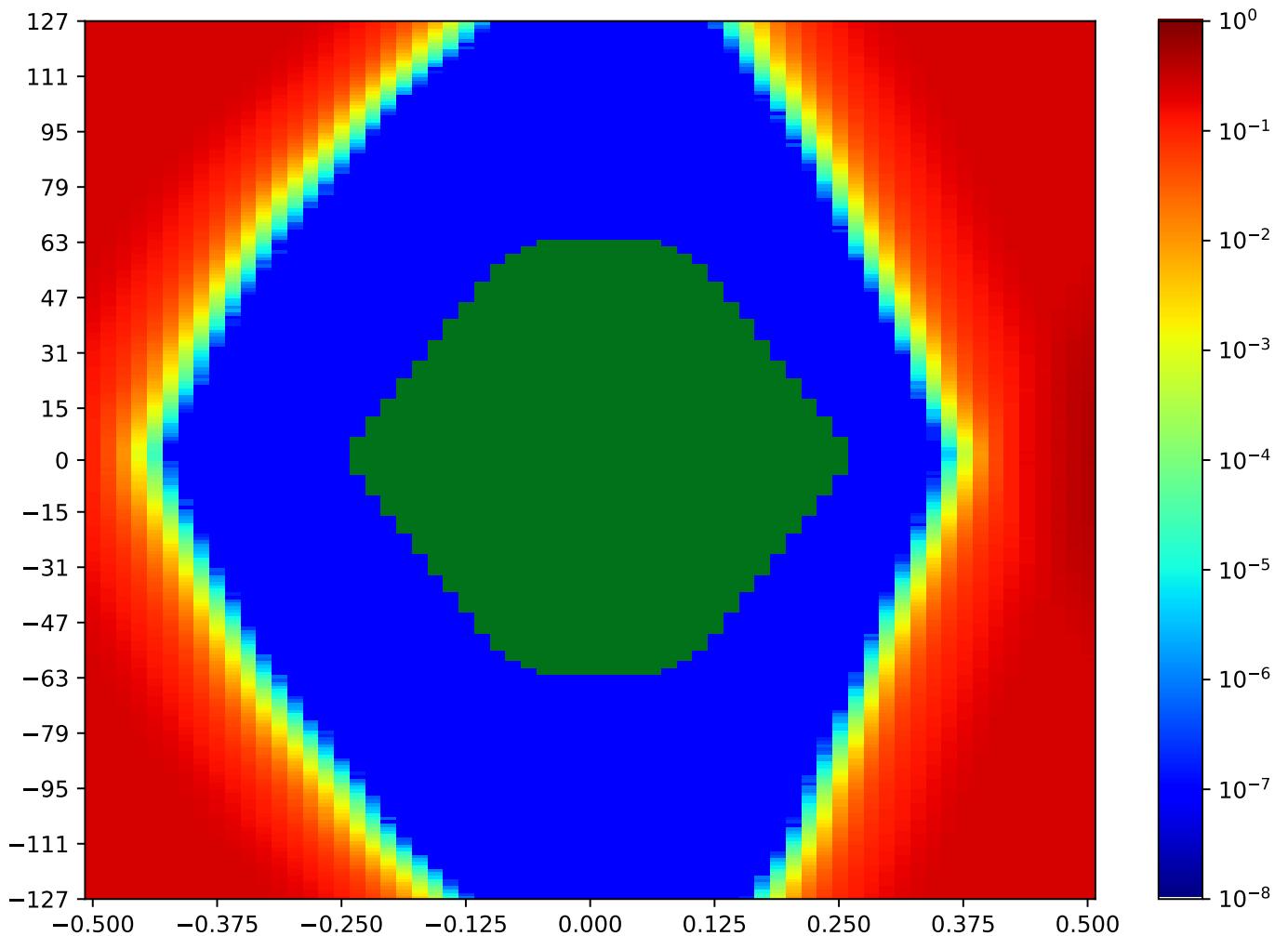


Figure 3.102: MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.5 MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

Table 3.94: MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:01:15		2018-Jan-24 00:01:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8153	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

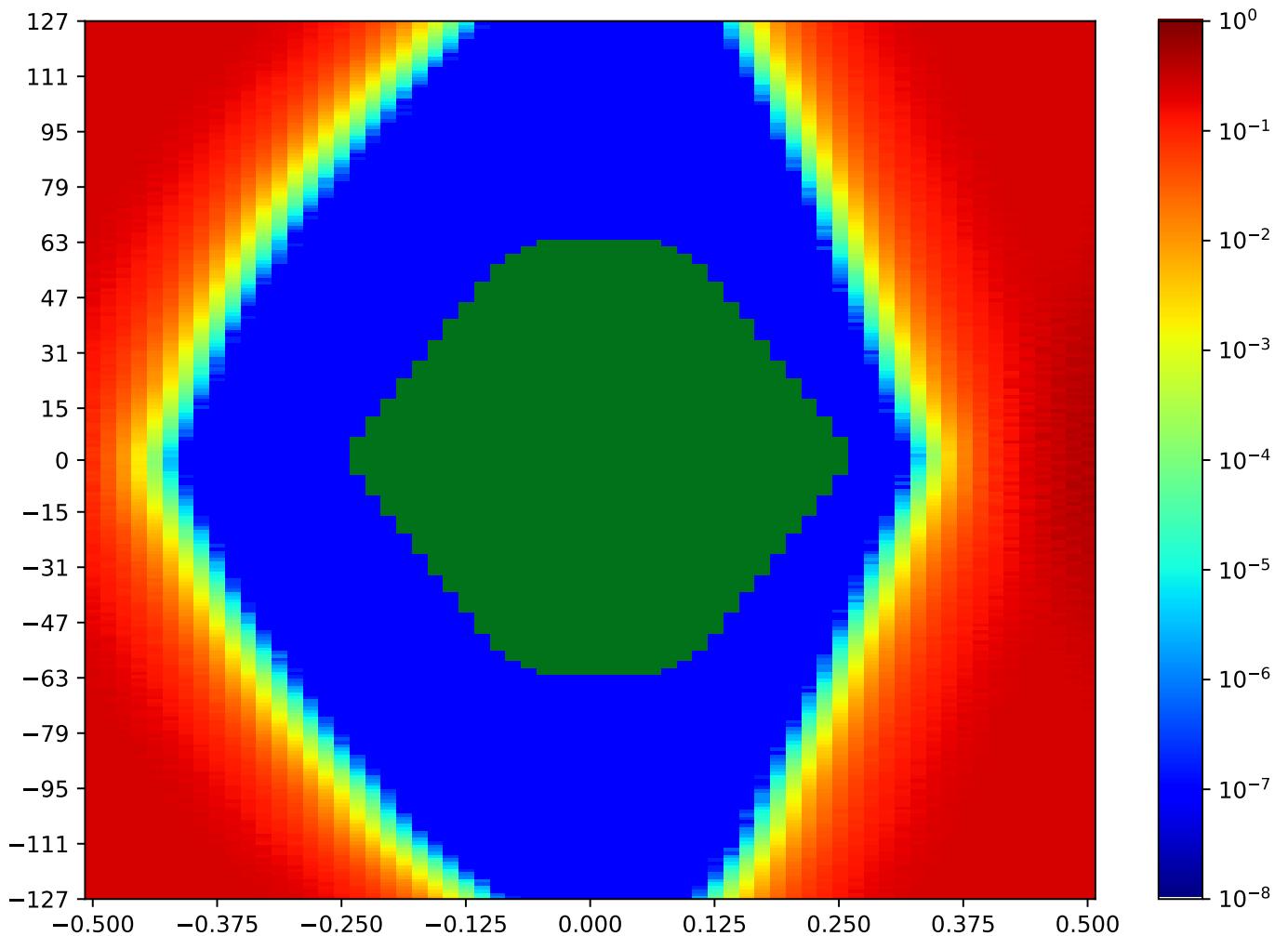


Figure 3.103: MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.6 MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

Table 3.95: MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:01:36		2018-Jan-24 00:01:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8441	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

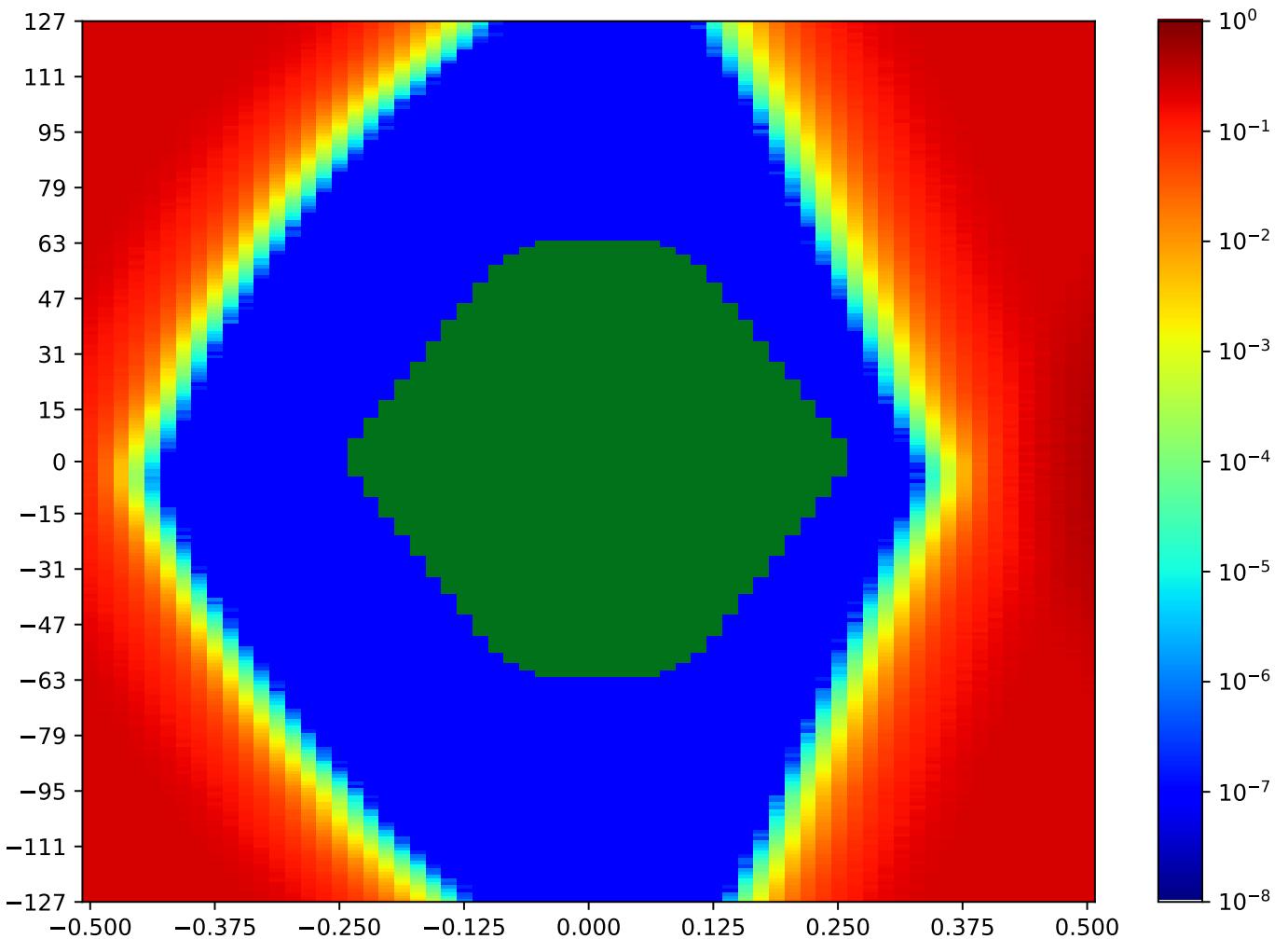


Figure 3.104: MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.7 MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

Table 3.96: MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:01:57		2018-Jan-24 00:02:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8404	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

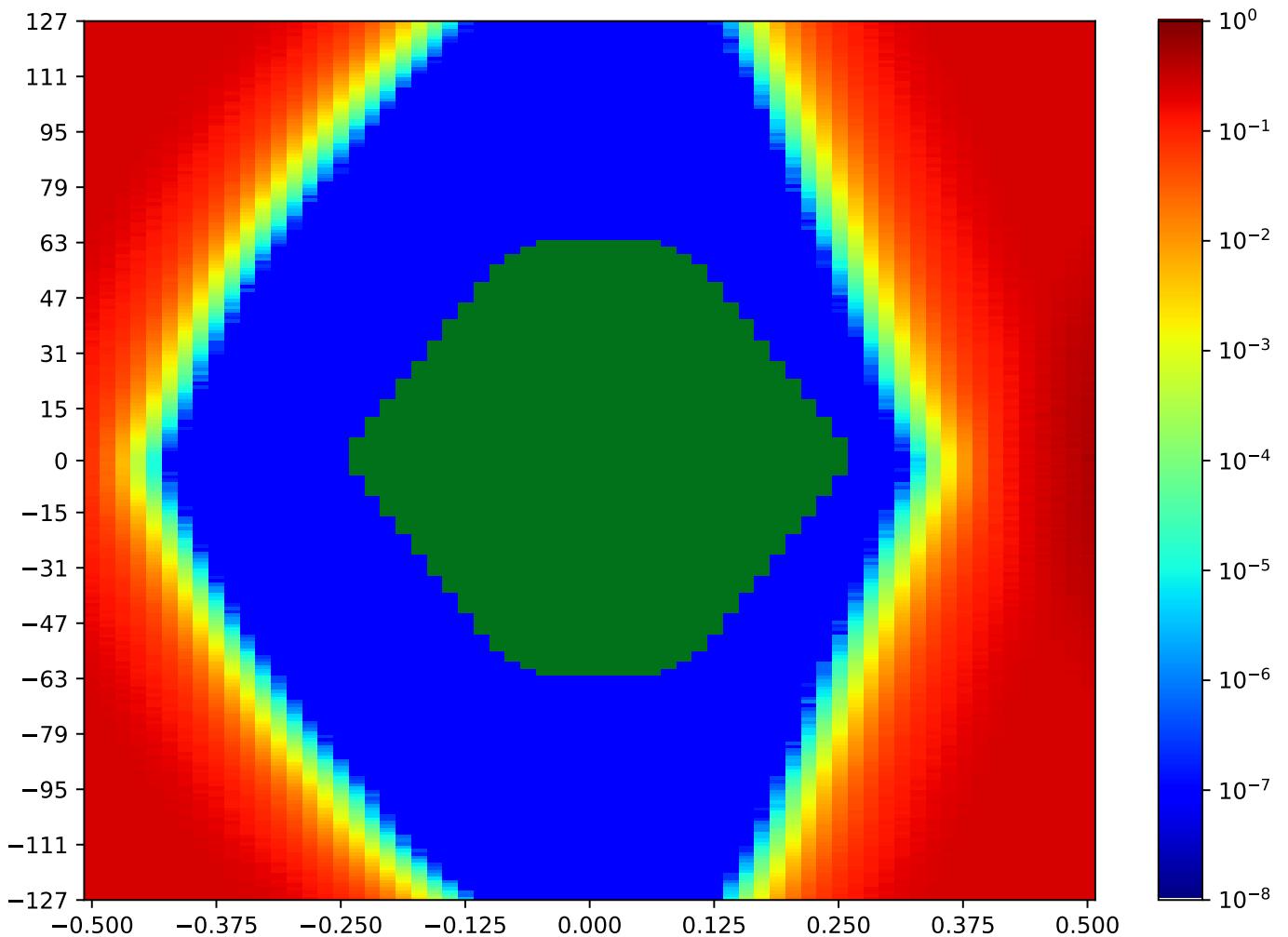


Figure 3.105: MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.8 MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

Table 3.97: MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:02:17		2018-Jan-24 00:02:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8945	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

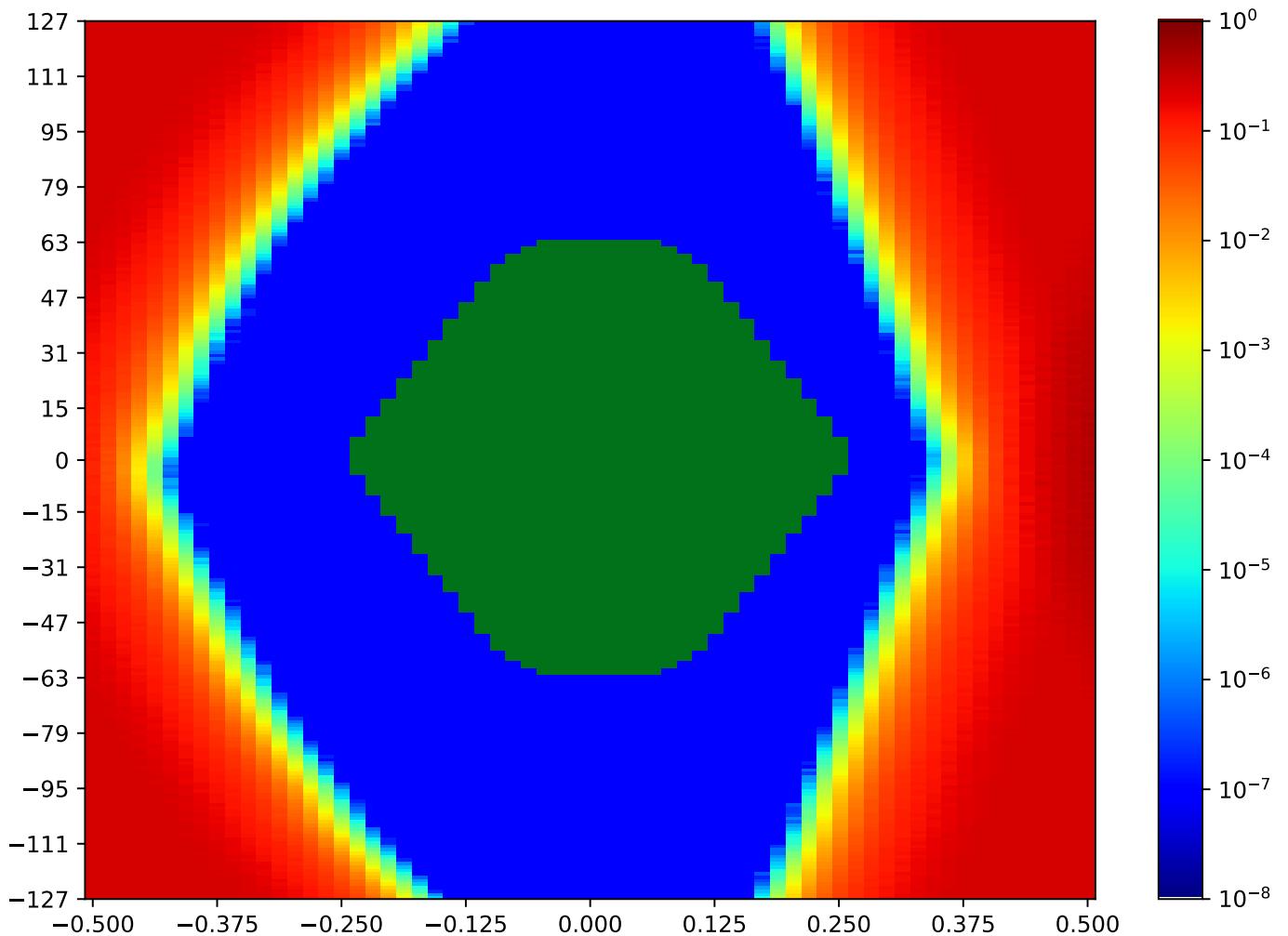


Figure 3.106: MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.9 MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

Table 3.98: MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:02:38		2018-Jan-24 00:02:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8660	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

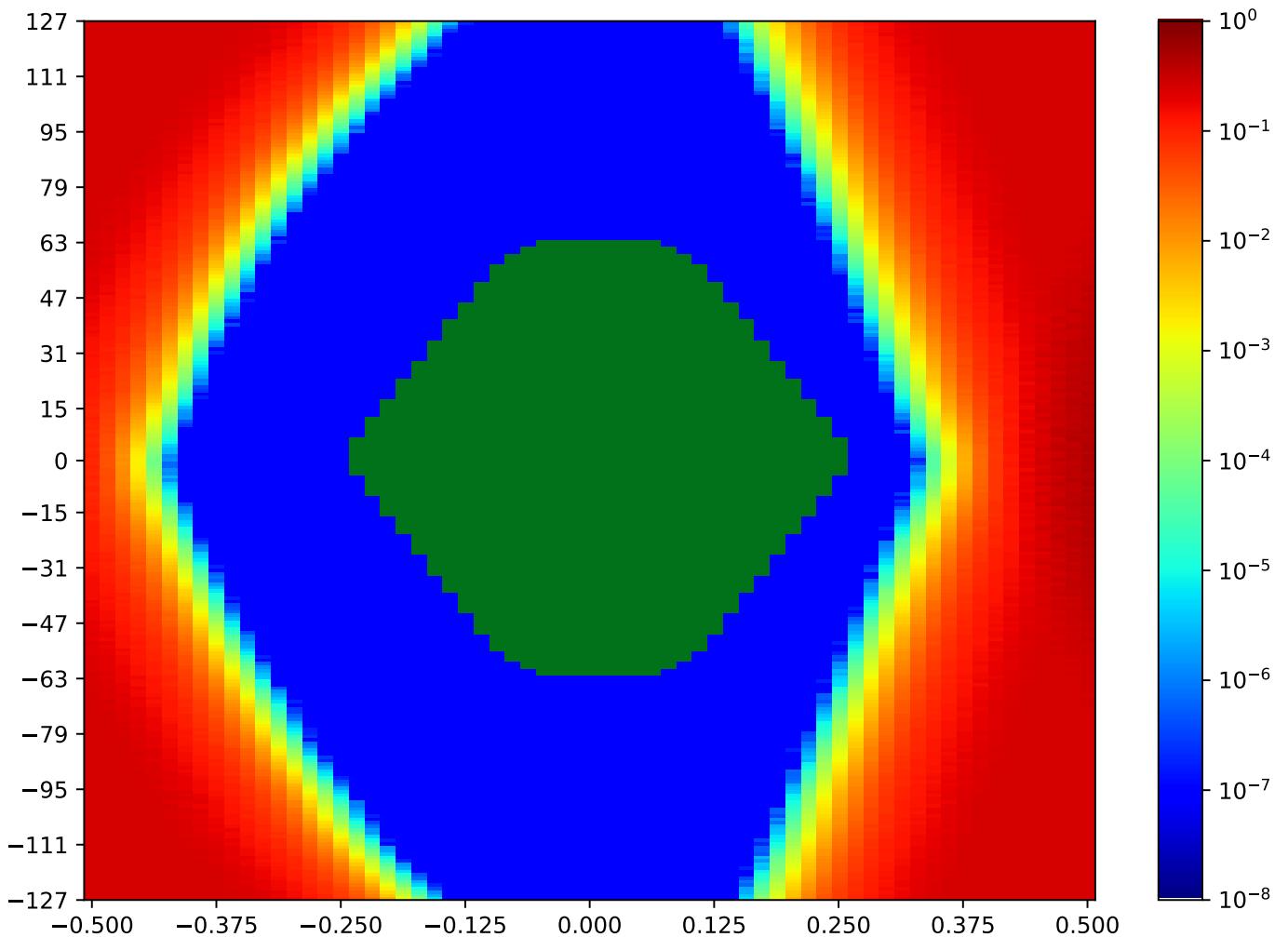


Figure 3.107: MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.10 MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

Table 3.99: MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:02:58		2018-Jan-24 00:03:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8523	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

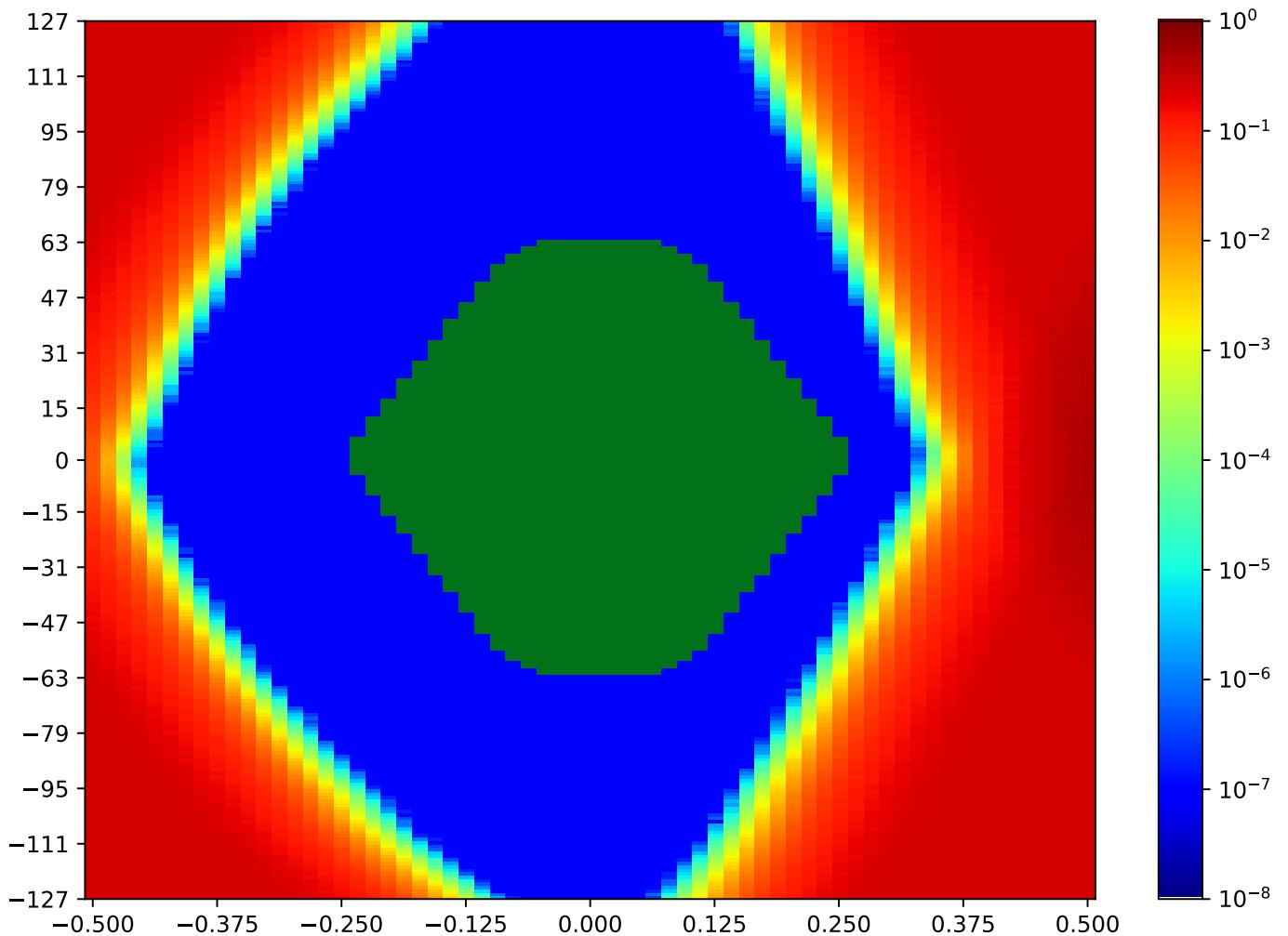


Figure 3.108: MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.11 MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

Table 3.100: MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:03:19		2018-Jan-24 00:03:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8845	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

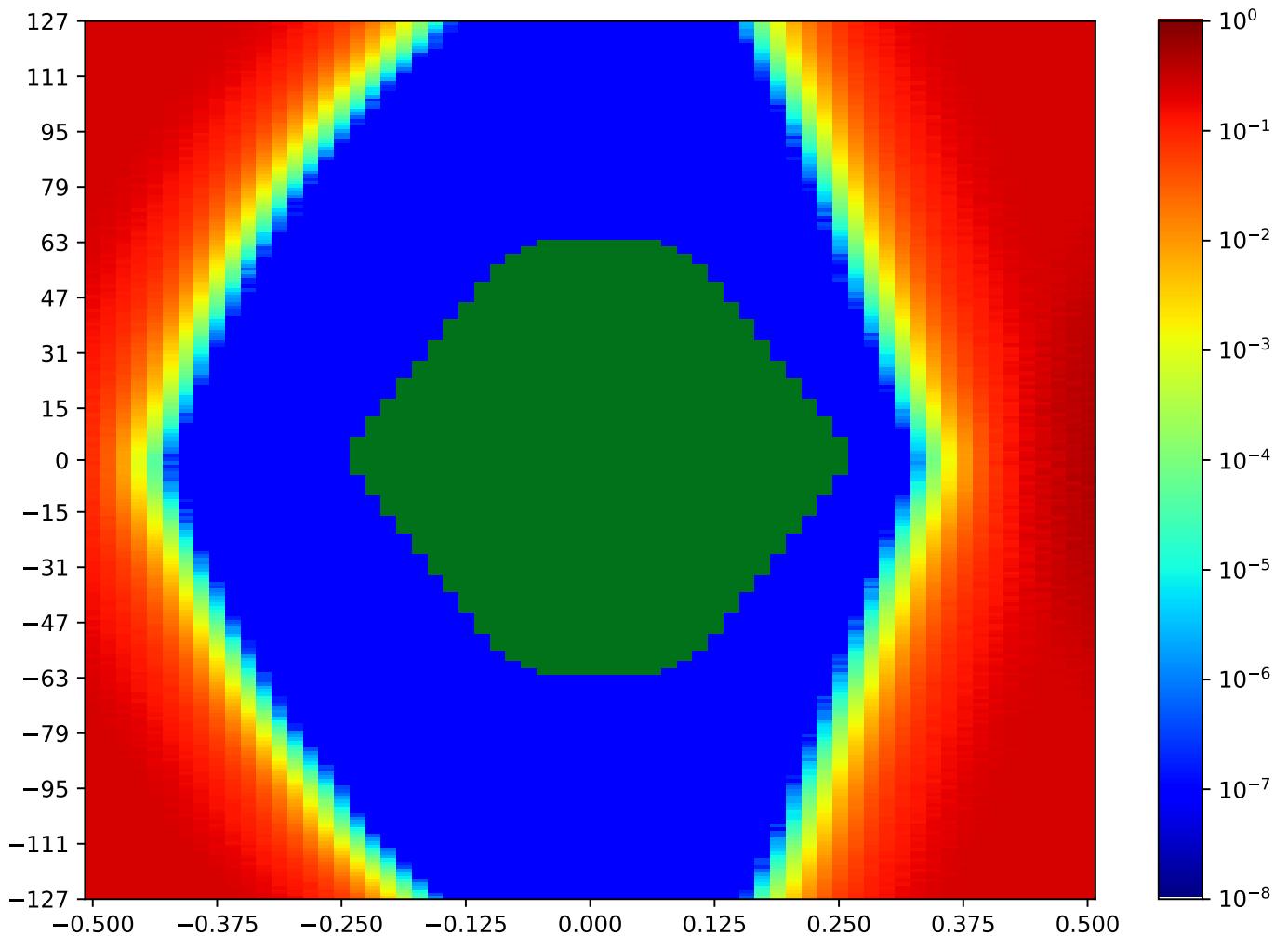


Figure 3.109: MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.12 MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

Table 3.101: MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:03:39		2018-Jan-24 00:04:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8967	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

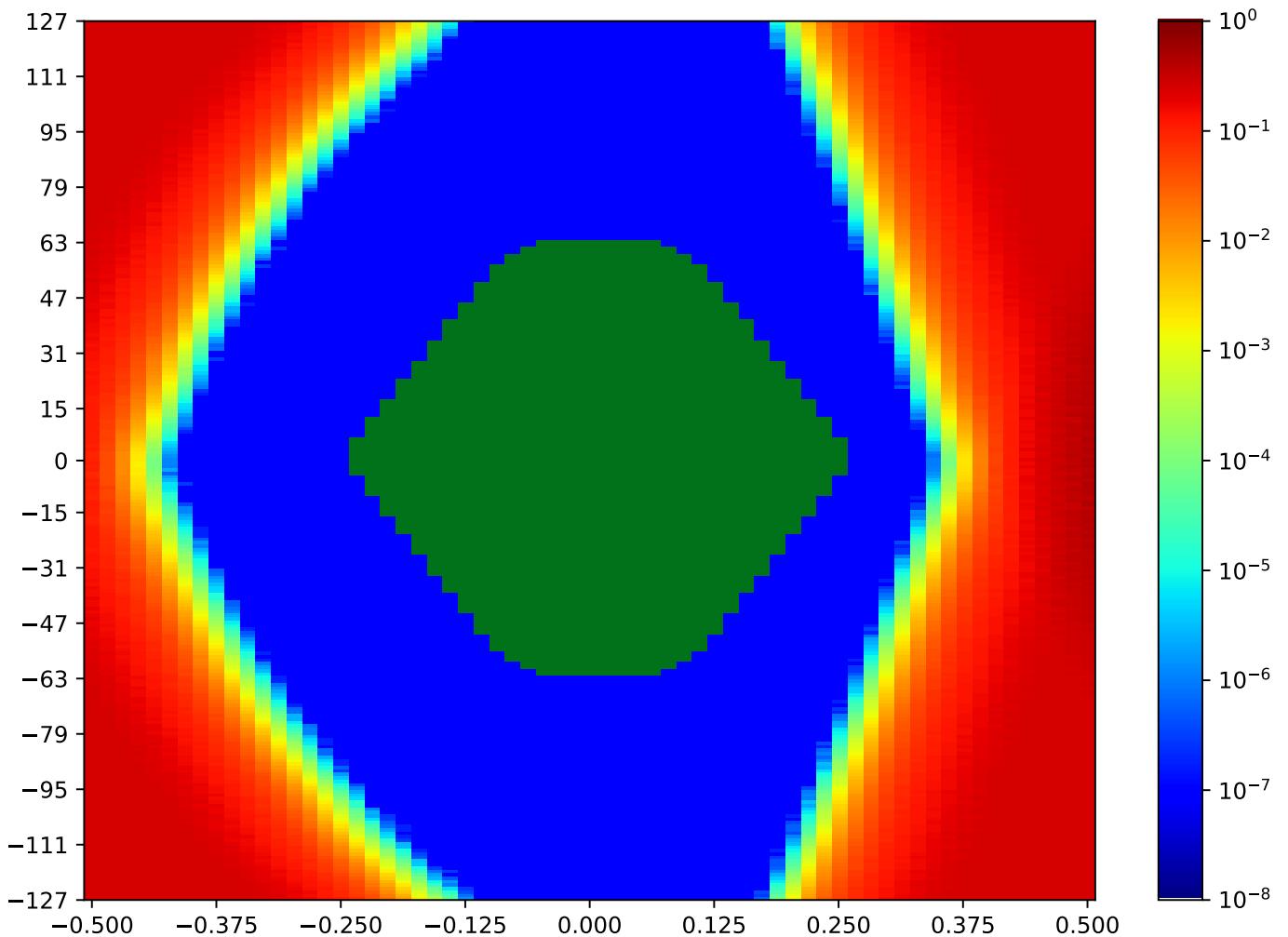


Figure 3.110: MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.13 MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

Table 3.102: MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:04:00		2018-Jan-24 00:04:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9229	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

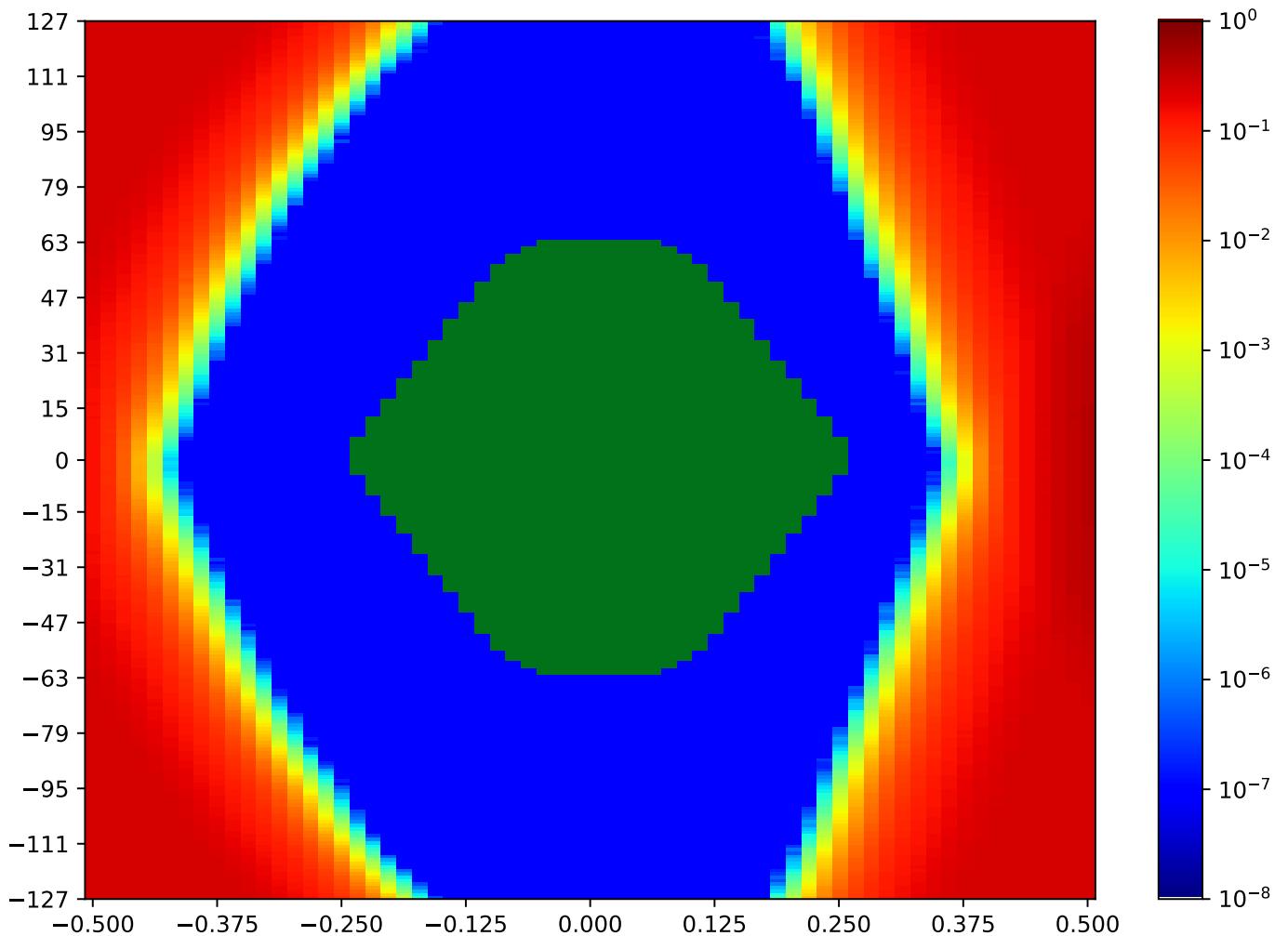


Figure 3.111: MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.14 MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

Table 3.103: MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:04:21		2018-Jan-24 00:04:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9284	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

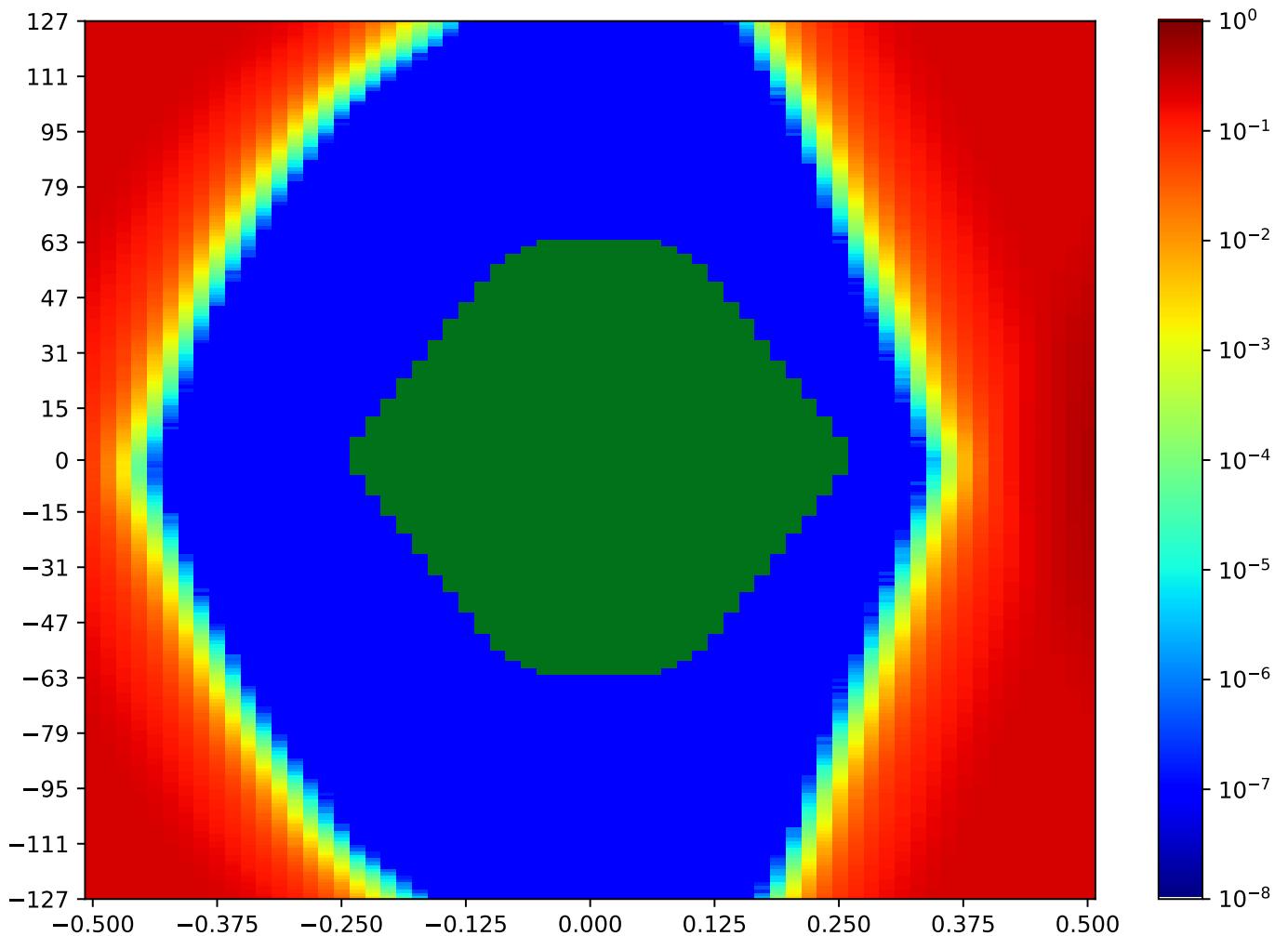


Figure 3.112: MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.15 MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

Table 3.104: MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:04:41		2018-Jan-24 00:05:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8387	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

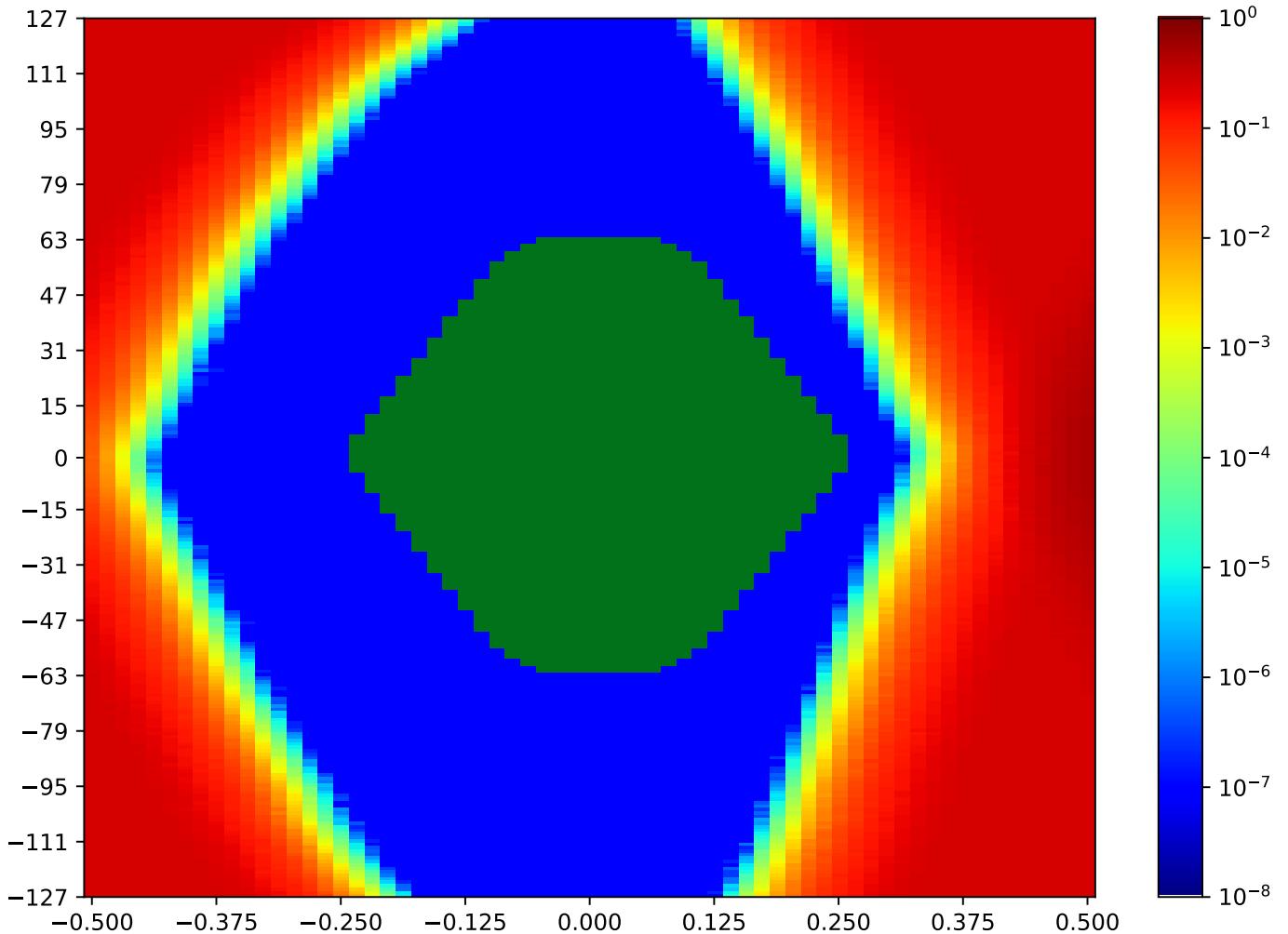


Figure 3.113: MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.16 MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

Table 3.105: MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:05:02		2018-Jan-24 00:05:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9189	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

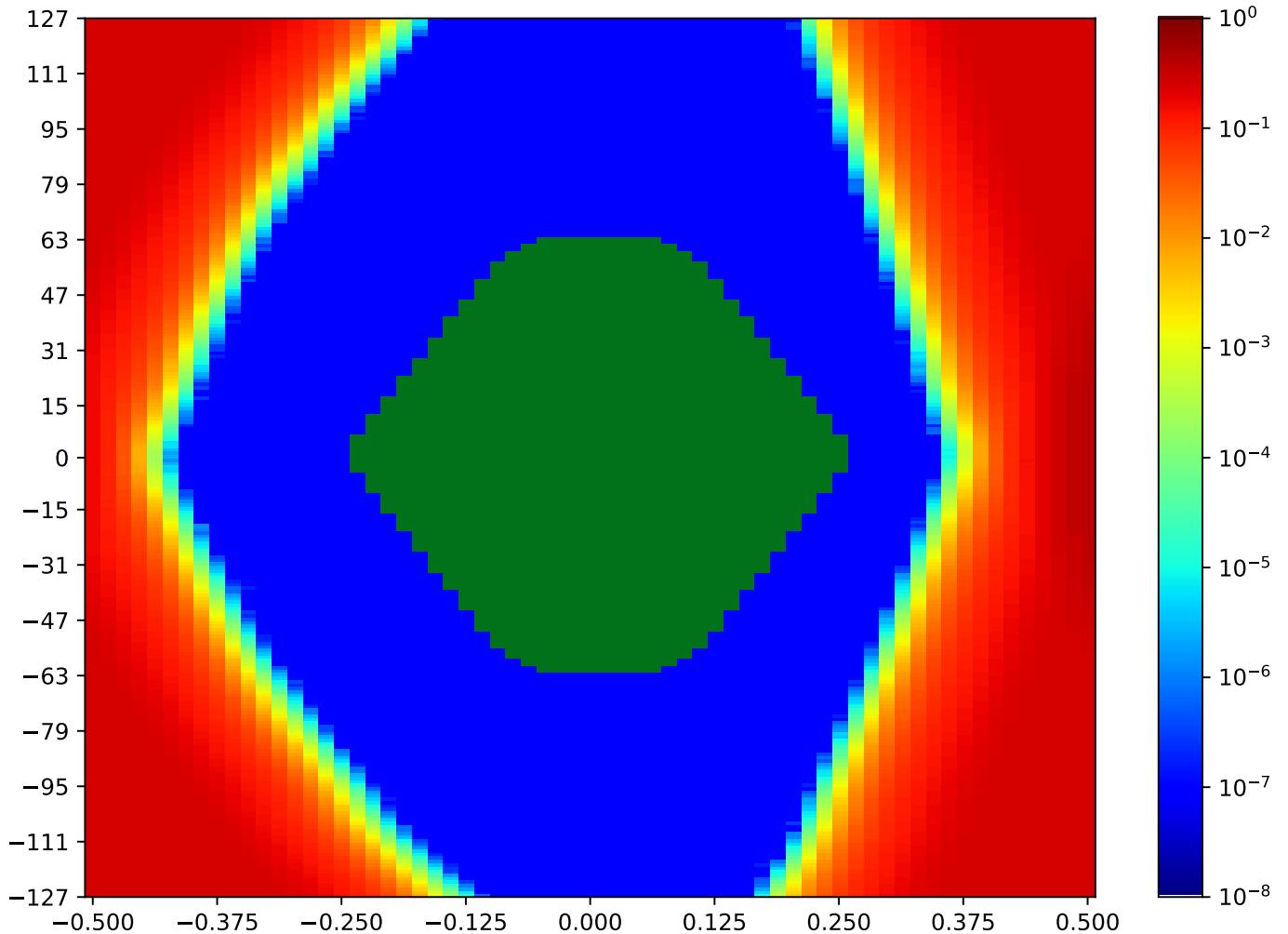


Figure 3.114: MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.17 MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

Table 3.106: MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:05:23		2018-Jan-24 00:05:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8458	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

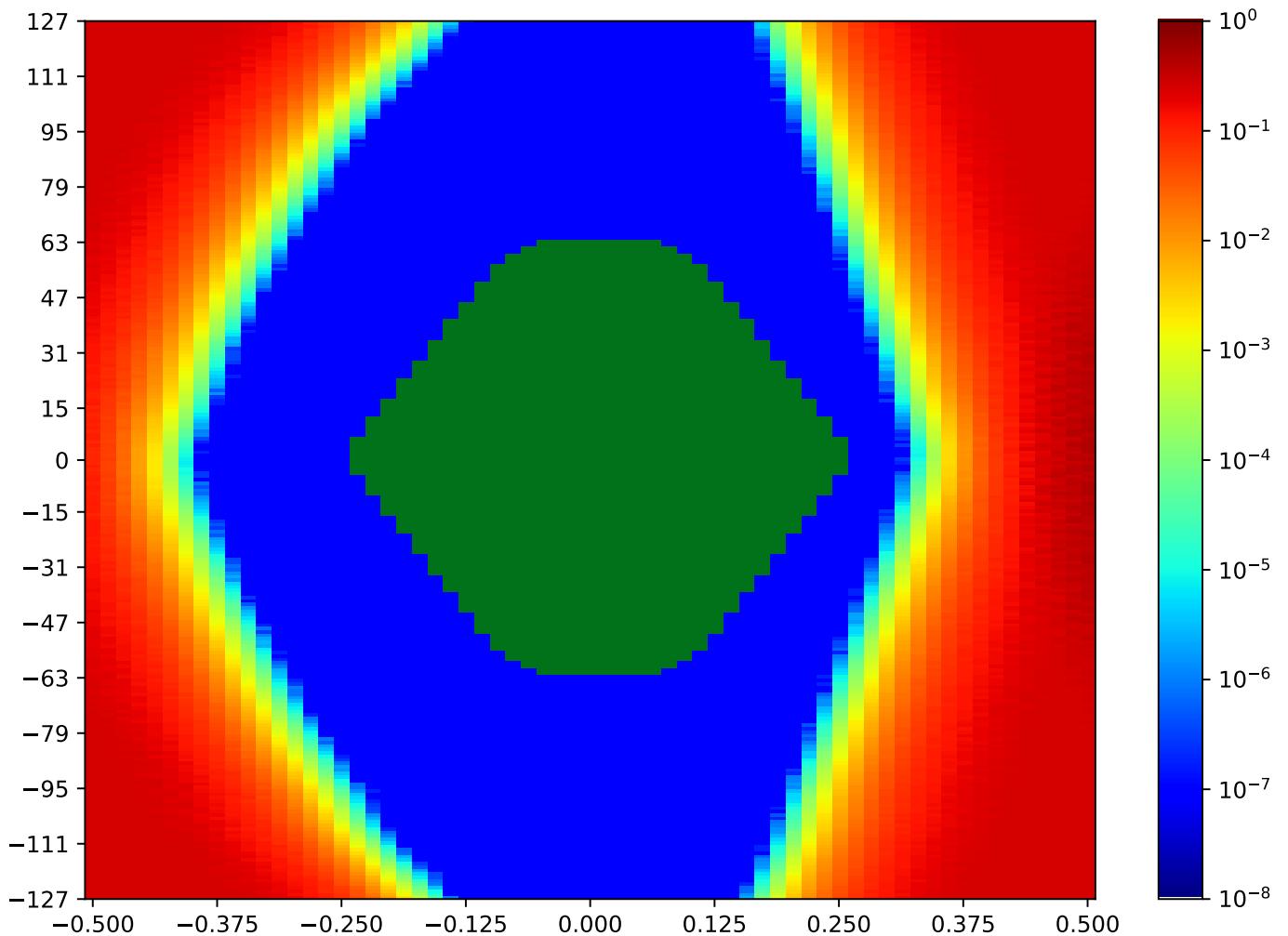


Figure 3.115: MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.18 MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

Table 3.107: MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:05:43		2018-Jan-24 00:06:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8769	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

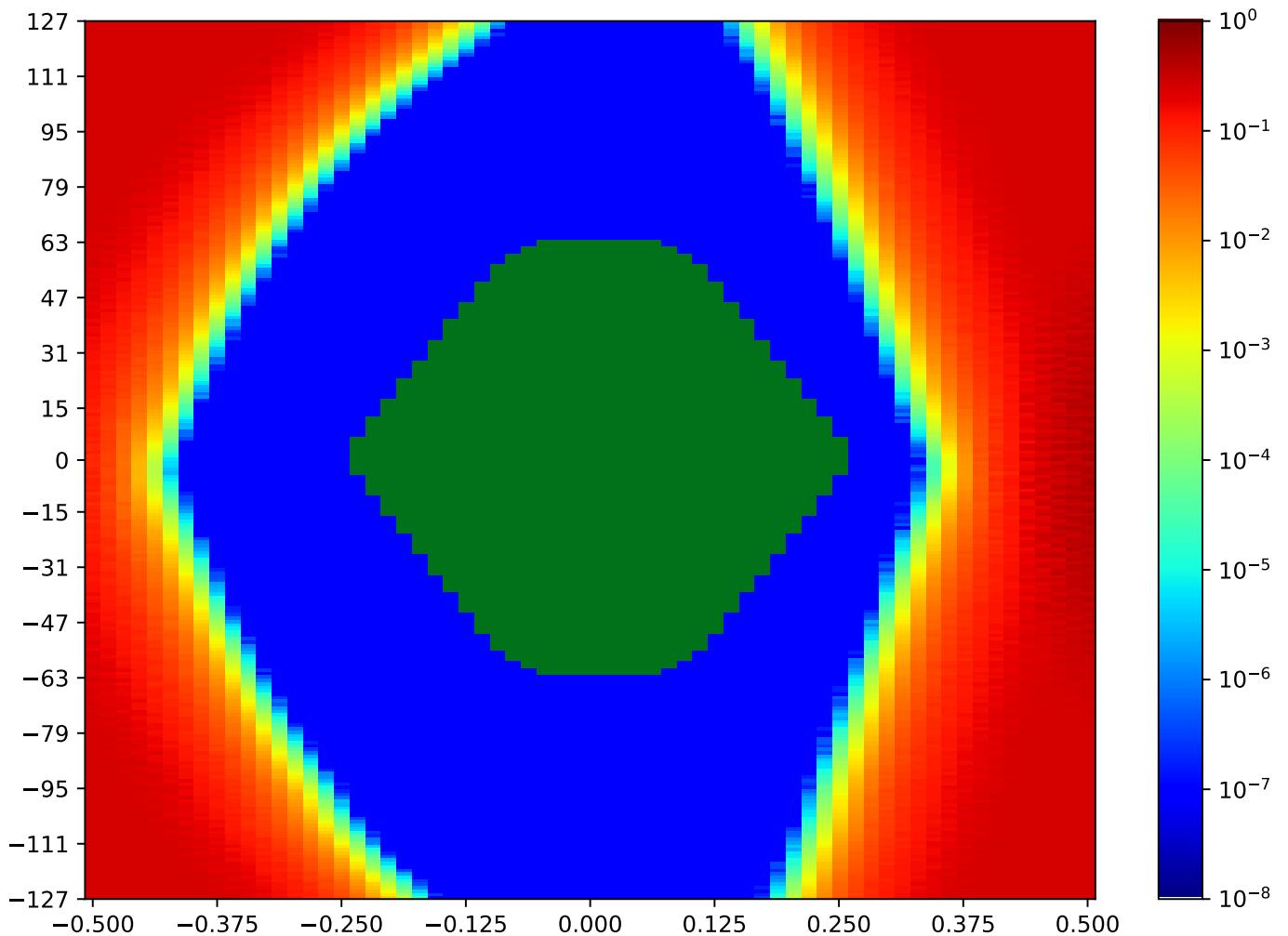


Figure 3.116: MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.19 MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

Table 3.108: MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:06:04		2018-Jan-24 00:06:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9060	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

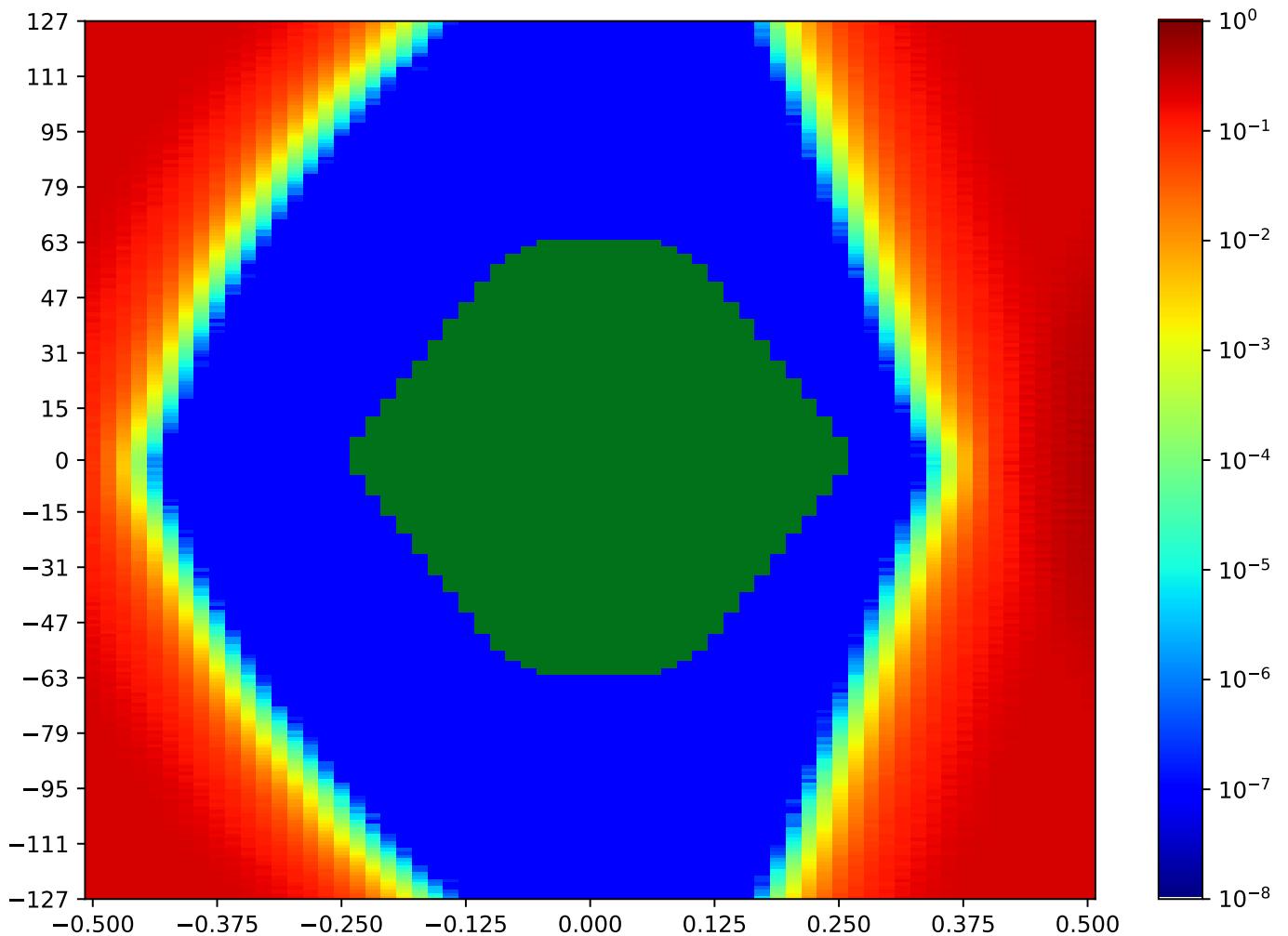


Figure 3.117: MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.20 MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

Table 3.109: MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:06:24		2018-Jan-24 00:06:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8752	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

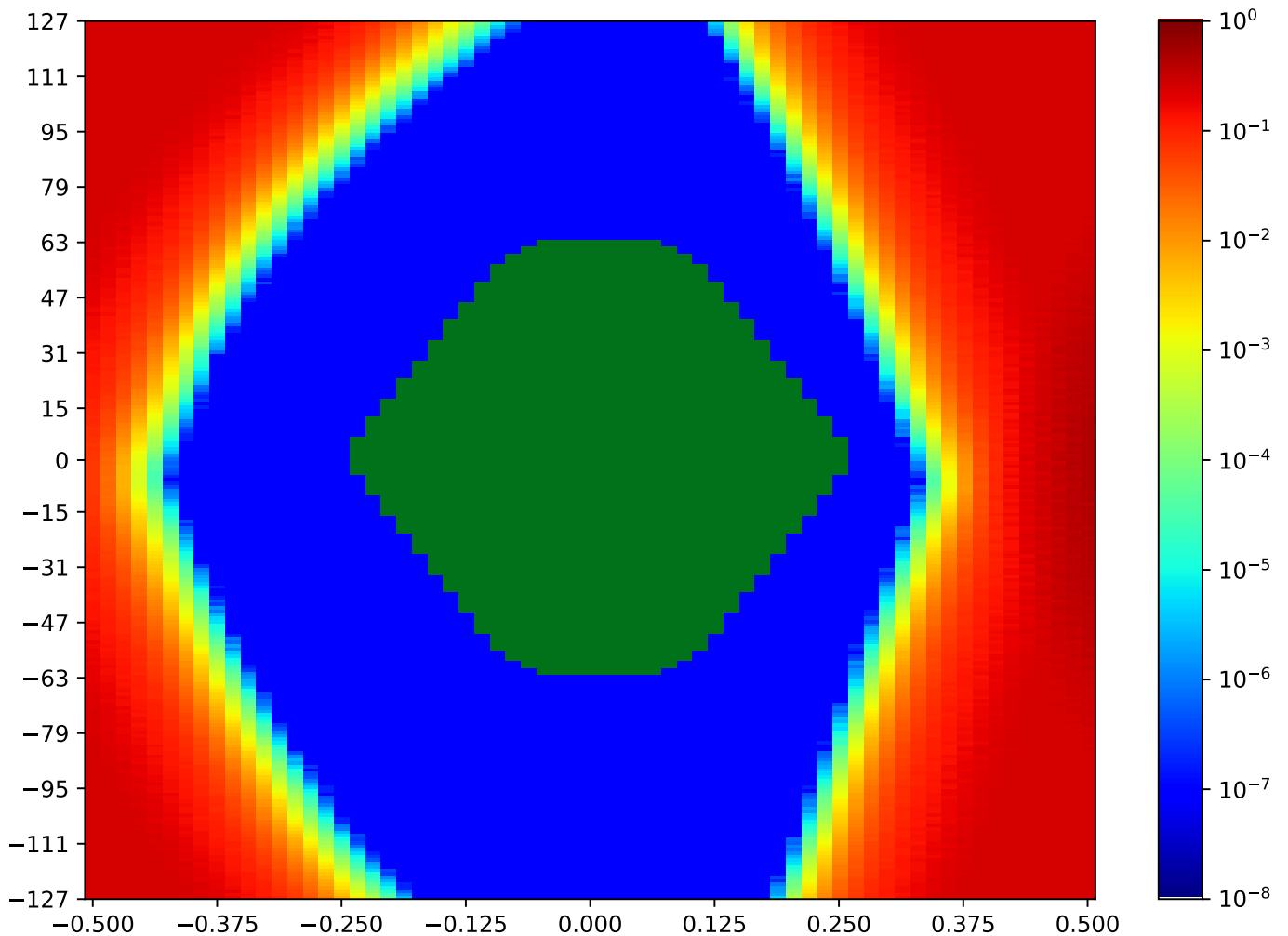


Figure 3.118: MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.21 MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

Table 3.110: MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:06:45		2018-Jan-24 00:07:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8468	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

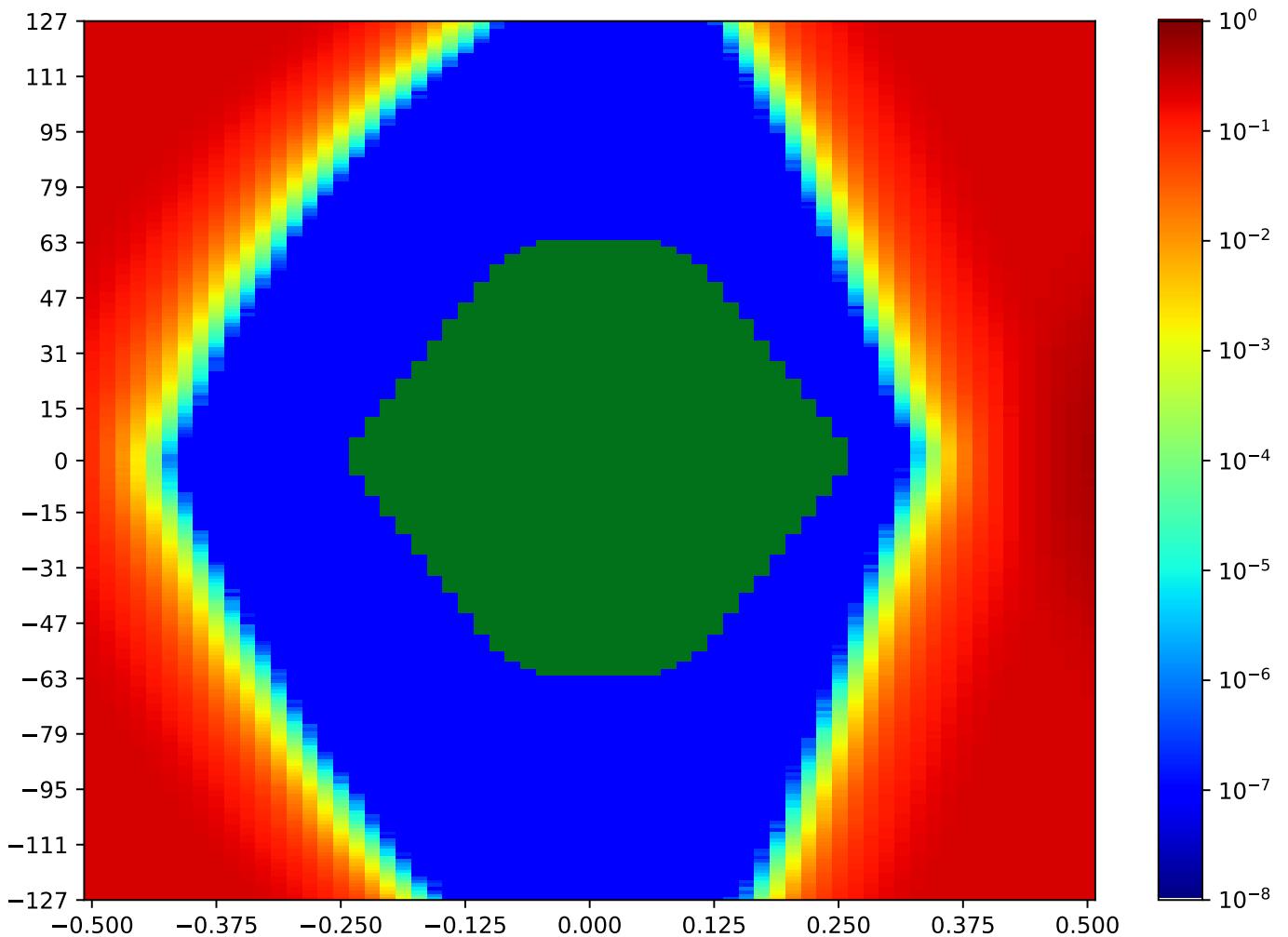


Figure 3.119: MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.22 MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

Table 3.111: MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:07:06		2018-Jan-24 00:07:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9158	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

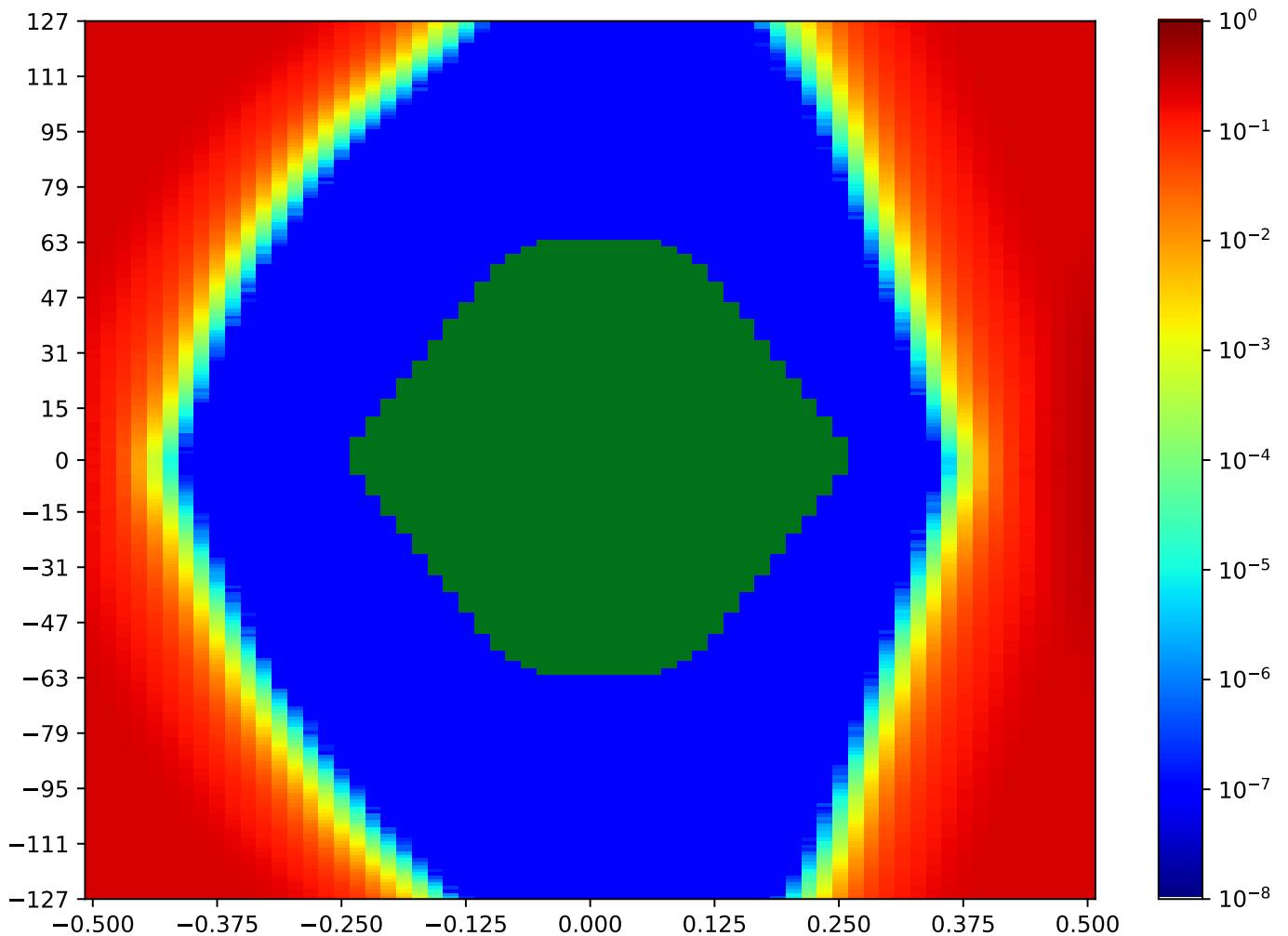


Figure 3.120: MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.23 MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

Table 3.112: MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:07:26		2018-Jan-24 00:07:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9139	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

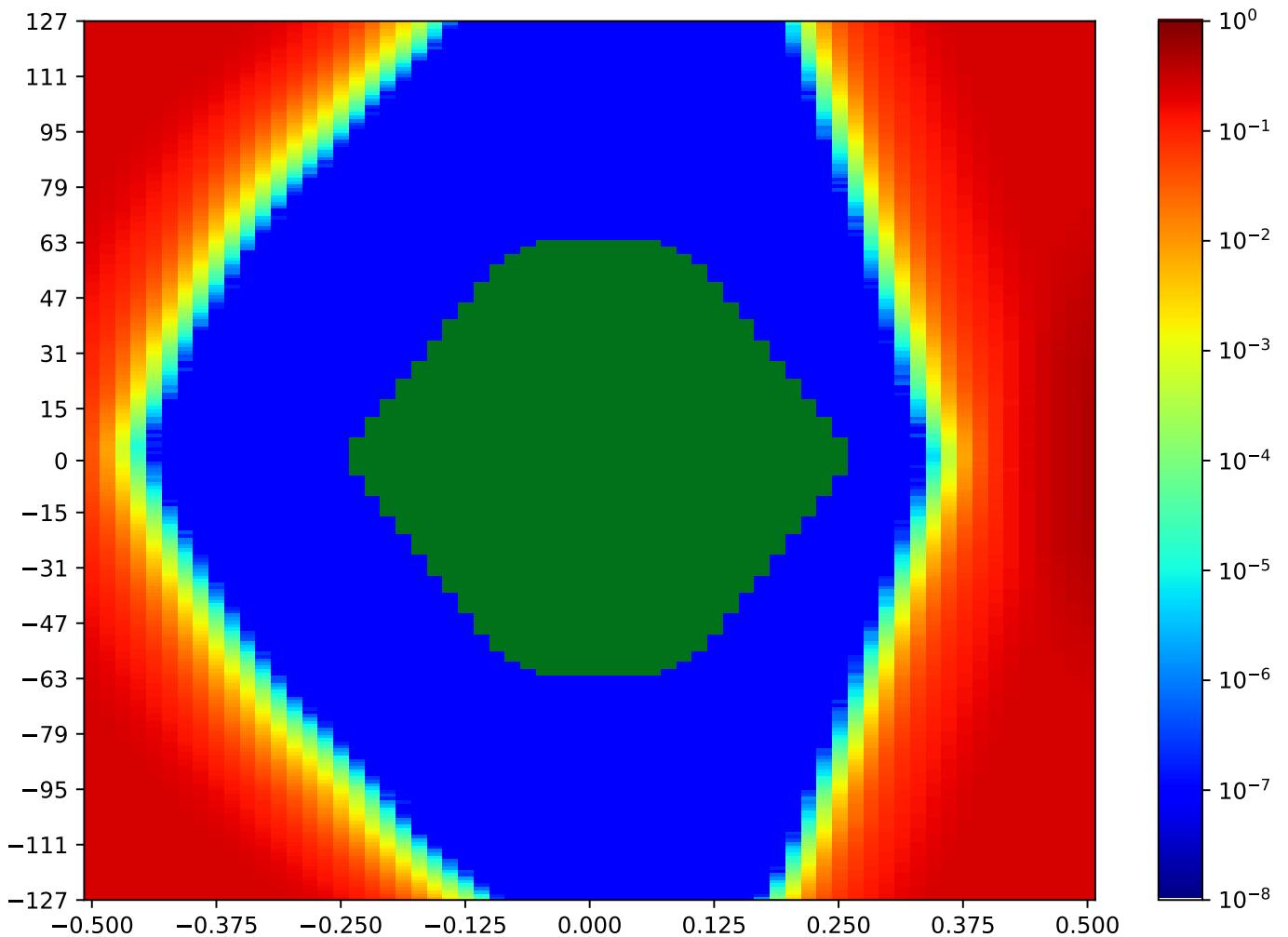


Figure 3.121: MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.24 MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

Table 3.113: MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:07:46		2018-Jan-24 00:08:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9312	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

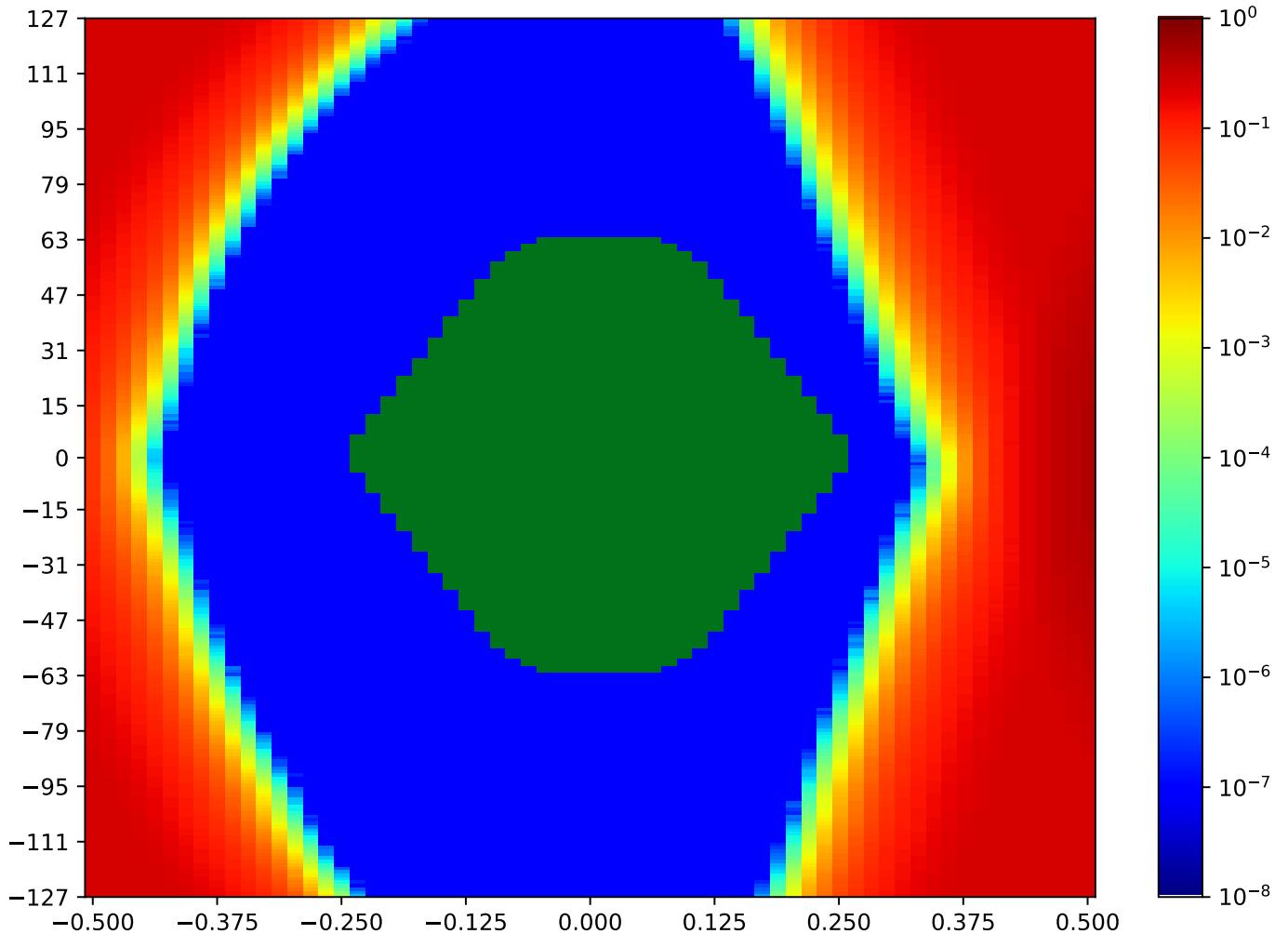


Figure 3.122: MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.25 MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

Table 3.114: MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:08:07		2018-Jan-24 00:08:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8866	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

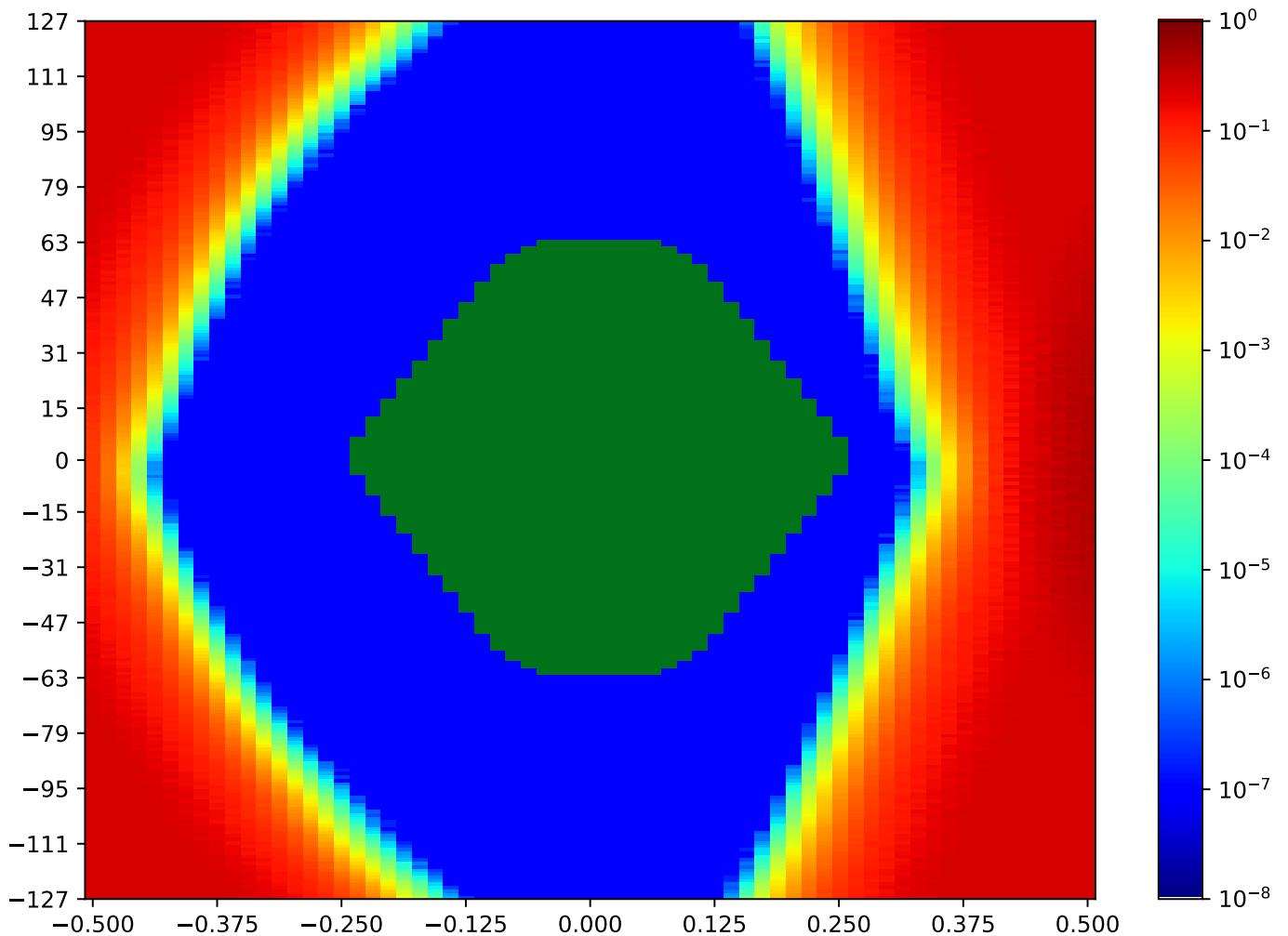


Figure 3.123: MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.26 MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

Table 3.115: MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:08:27		2018-Jan-24 00:08:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8985	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

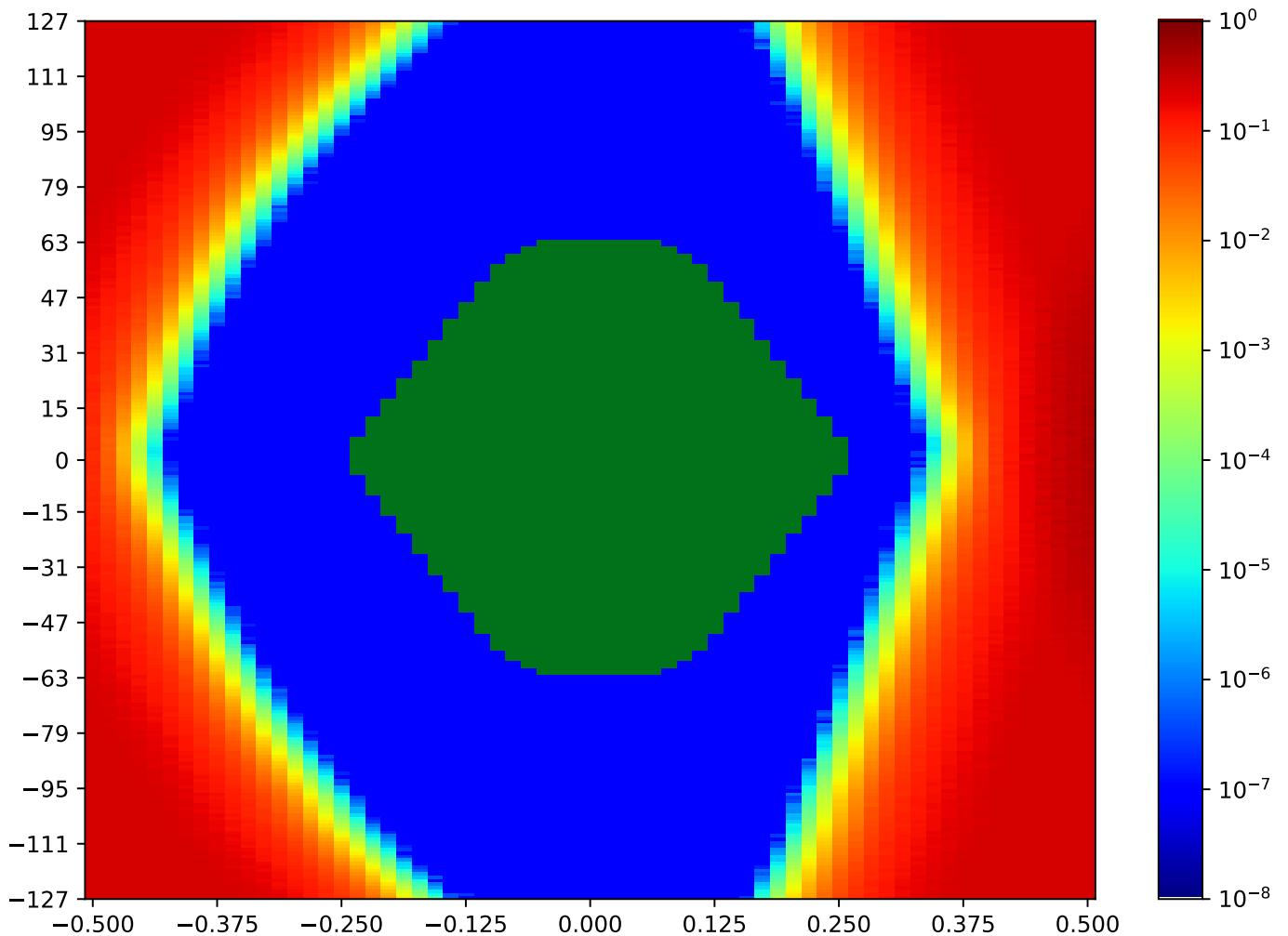


Figure 3.124: MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.27 MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

Table 3.116: MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:08:48		2018-Jan-24 00:09:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8382	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

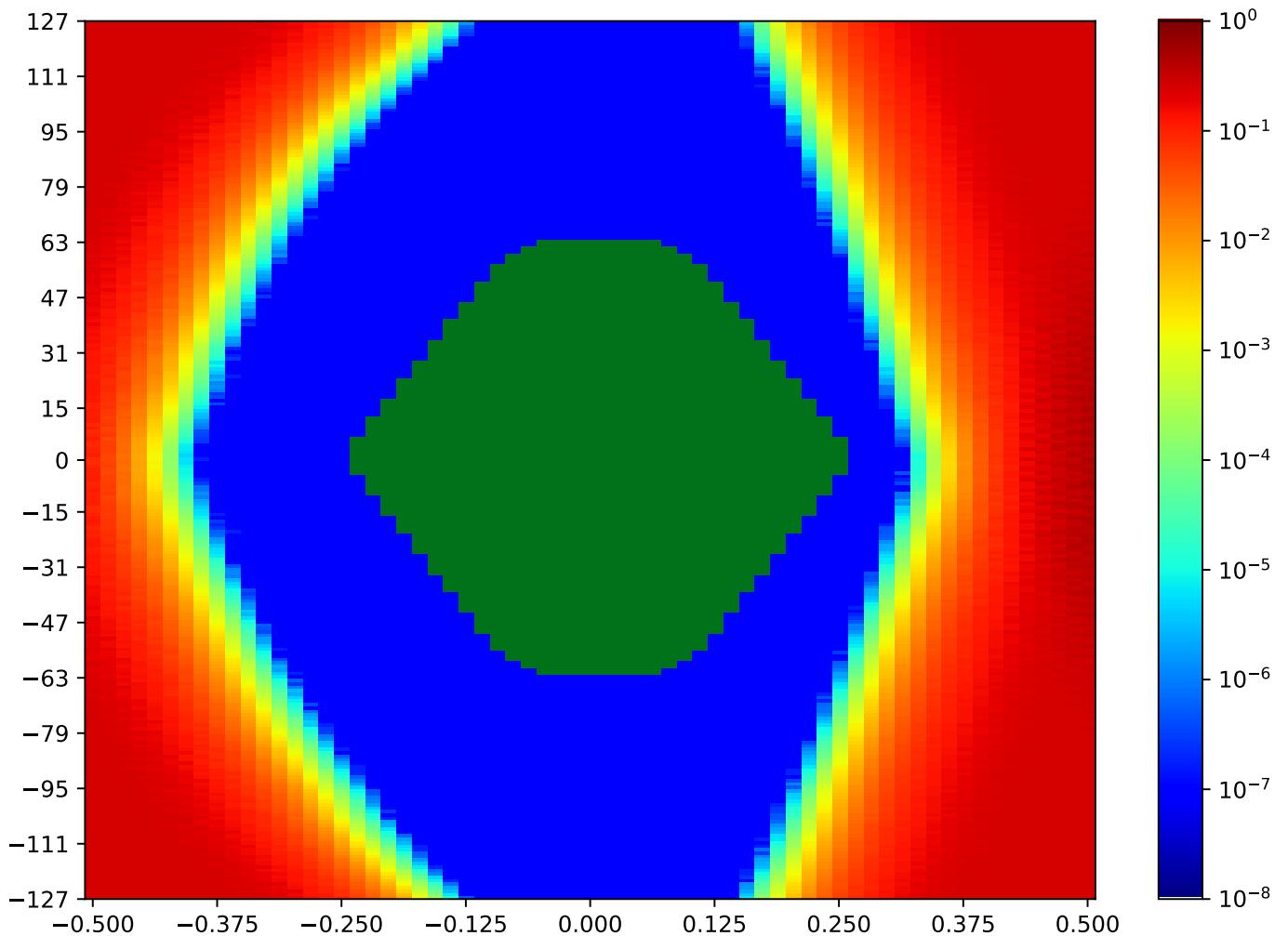


Figure 3.125: MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.9.28 MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

Table 3.117: MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:09:08		2018-Jan-24 00:09:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8954	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

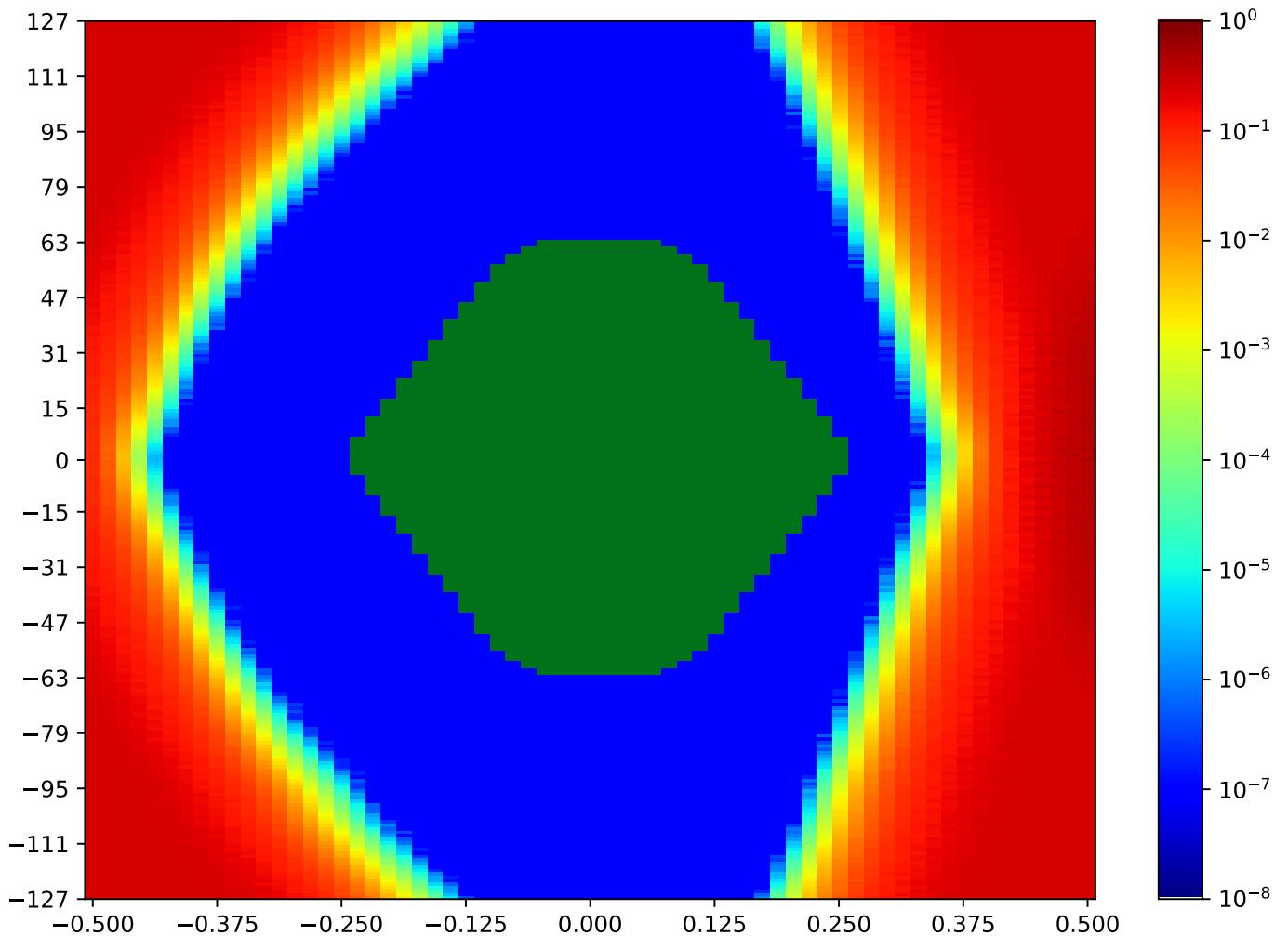


Figure 3.126: MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

Call back to summary Figure 3.98. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.10 MSP_A TX1 MSP_C RX18 Minipod Loopback

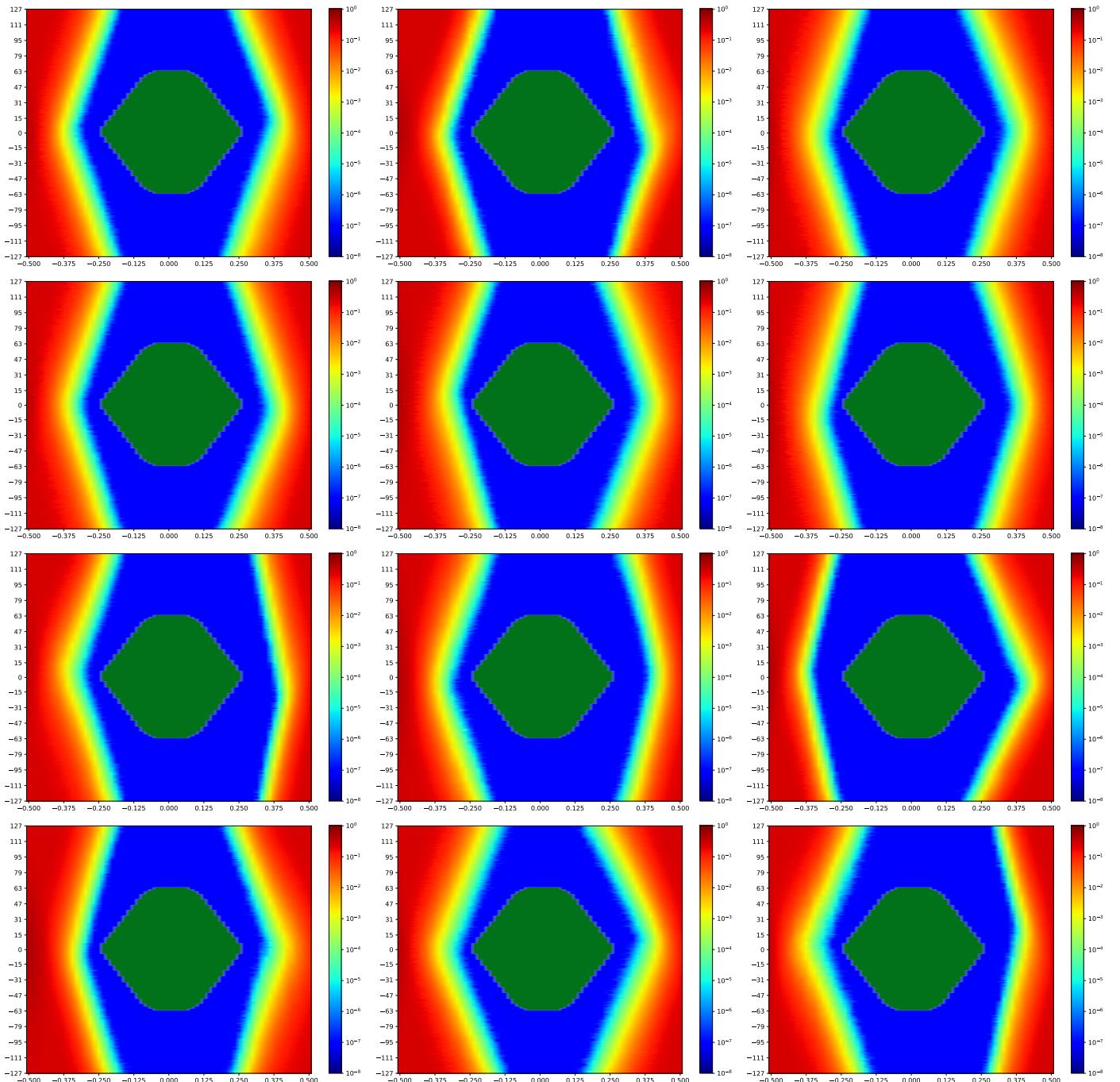


Figure 3.127: MSP_A TX1 MSP_C RX18 Minipod Loopback

A cross-reference to Figure 3.127. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.140.

3.10.1 MSP_A_FPGA-TX1-00-RX18-00-MSP_C_FPGA

Table 3.118: MSP_A_FPGA-TX1-00-RX18-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:28:06			2018-Jan-24 00:28:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7939	39	60.00%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

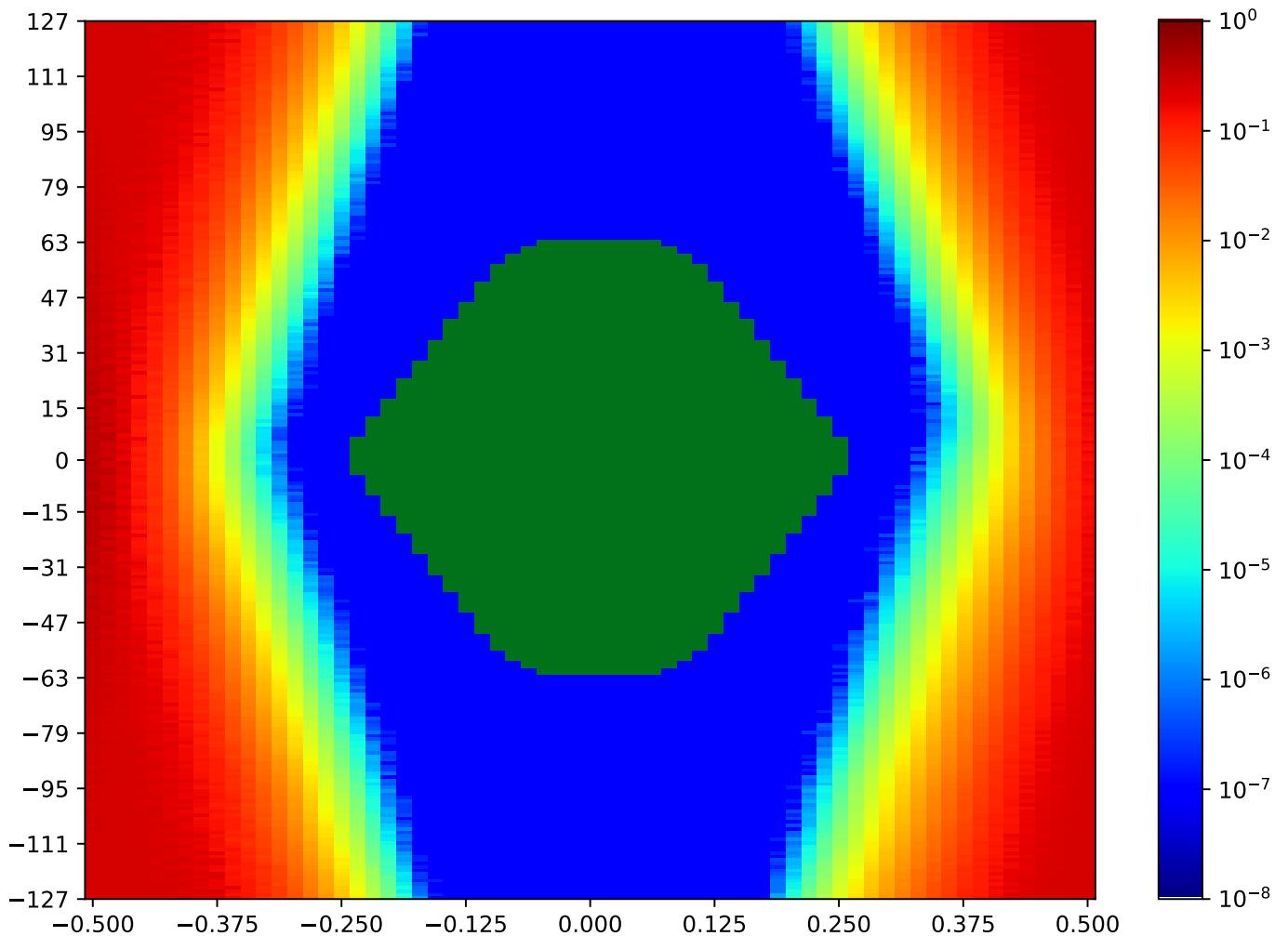


Figure 3.128: MSP_A_FPGA-TX1-00-RX18-00-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.2 MSP_A_FPGA-TX1-01-RX18-01-MSP_C_FPGA

Table 3.119: MSP_A_FPGA-TX1-01-RX18-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:28:49		2018-Jan-24 00:29:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8212	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

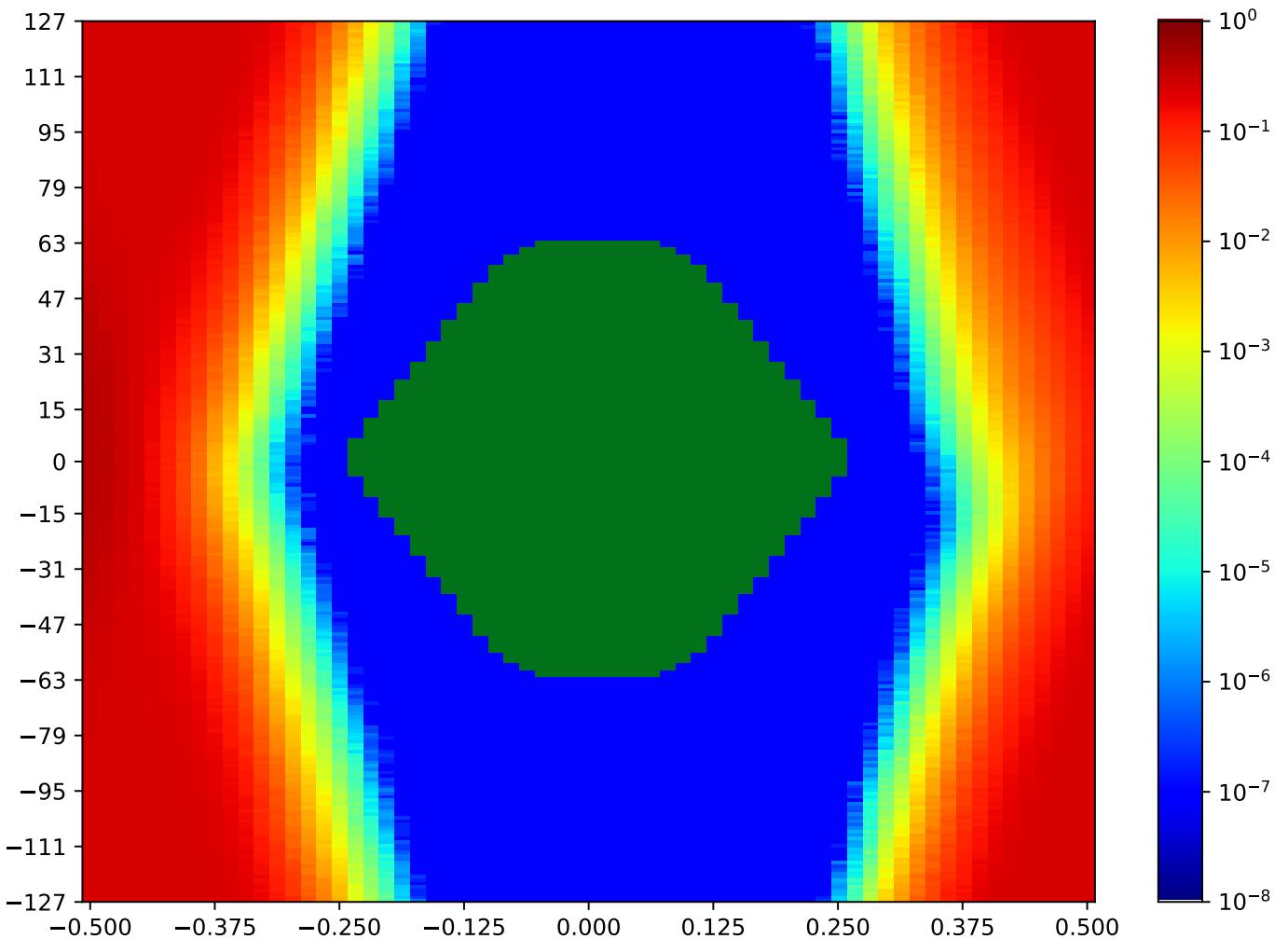


Figure 3.129: MSP_A_FPGA-TX1-01-RX18-01-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.3 MSP_A_FPGA-TX1-02-RX18-02-MSP_C_FPGA

Table 3.120: MSP_A_FPGA-TX1-02-RX18-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:29:10			2018-Jan-24 00:29:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7156	36	55.38%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

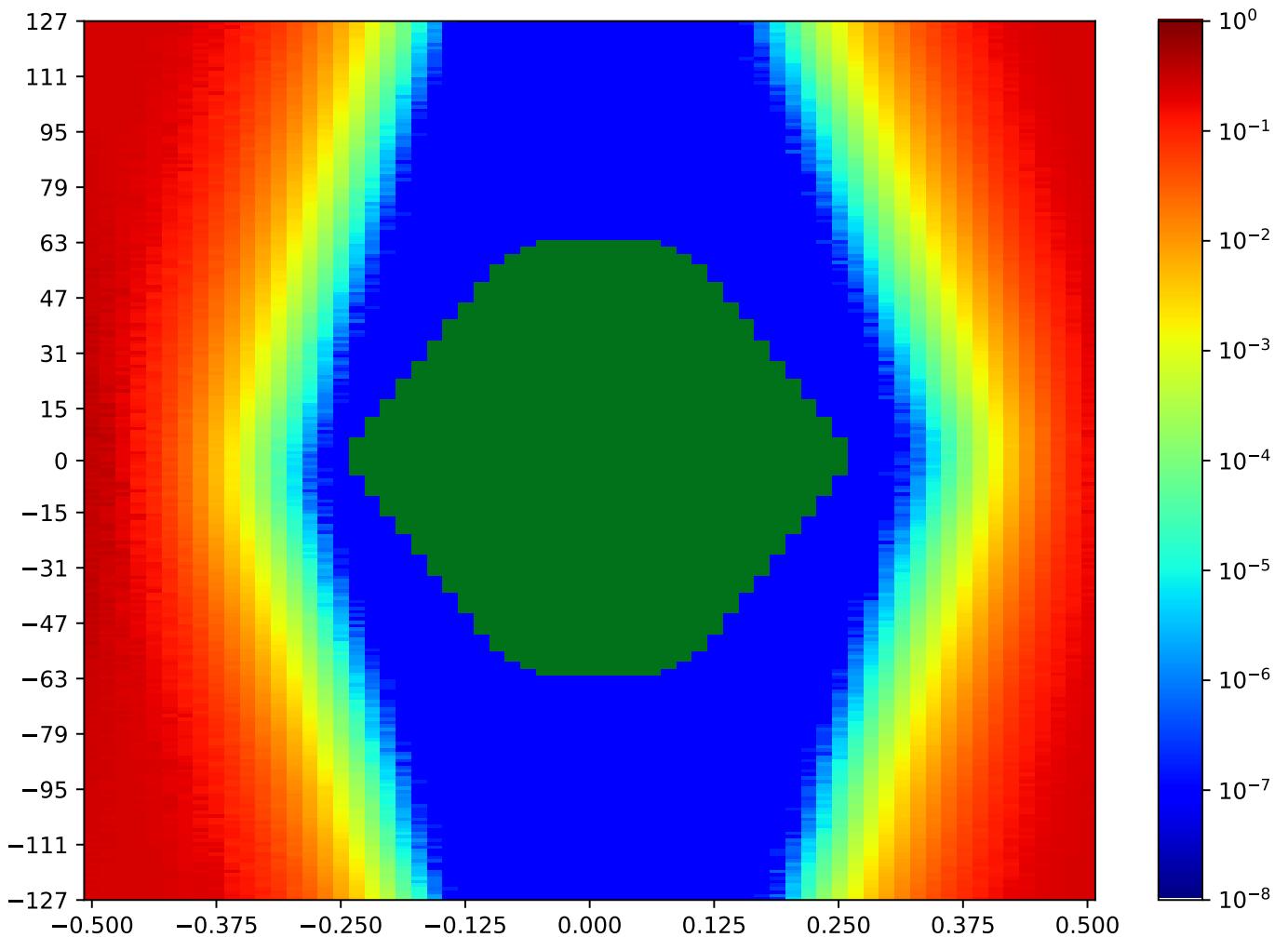


Figure 3.130: MSP_A_FPGA-TX1-02-RX18-02-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.4 MSP_A_FPGA-TX1-03-RX18-03-MSP_C_FPGA

Table 3.121: MSP_A_FPGA-TX1-03-RX18-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:27:23		2018-Jan-24 00:27:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7661	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

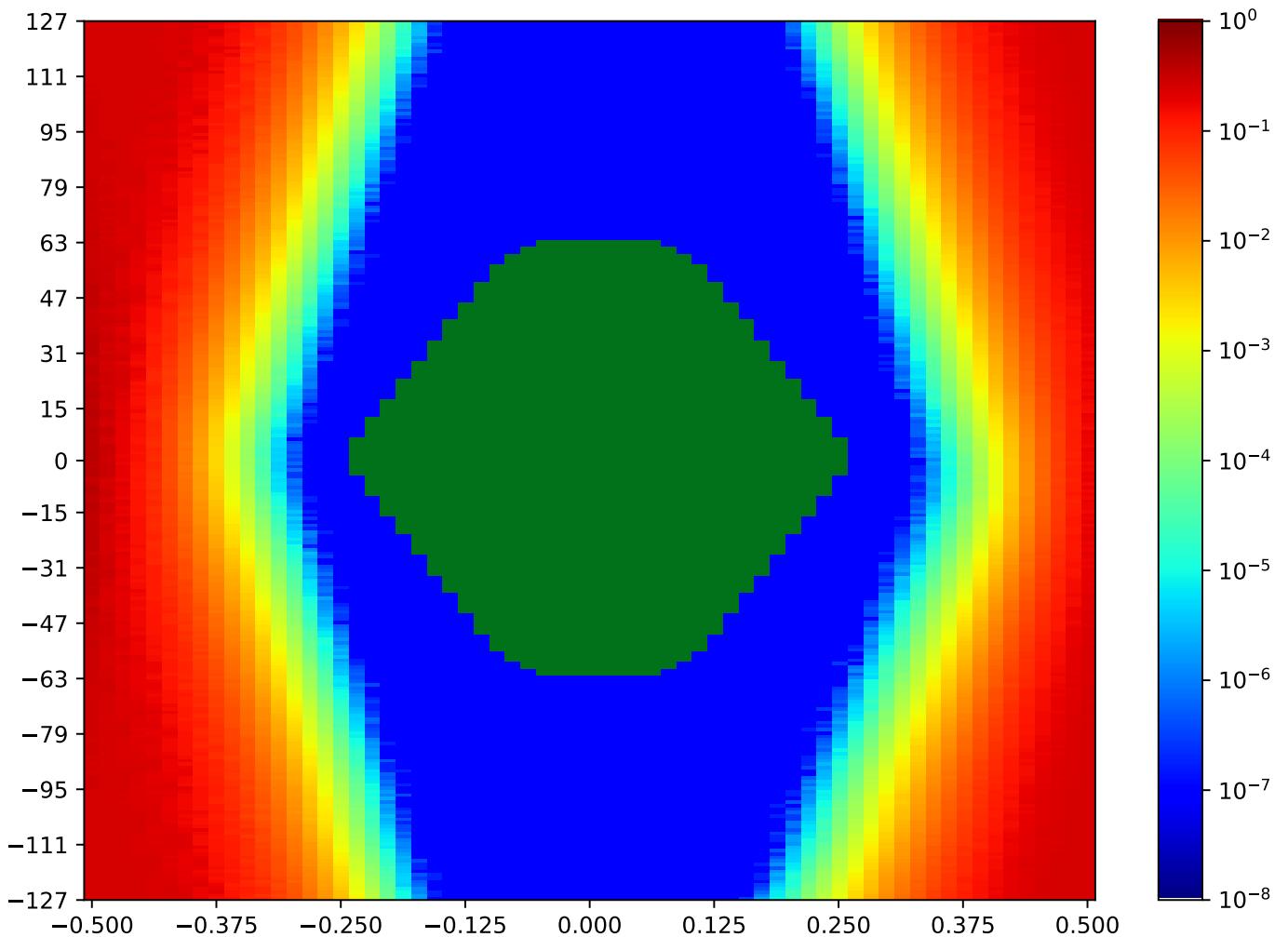


Figure 3.131: MSP_A_FPGA-TX1-03-RX18-03-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.5 MSP_A_FPGA-TX1-04-RX18-04-MSP_C_FPGA

Table 3.122: MSP_A_FPGA-TX1-04-RX18-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:30:15		2018-Jan-24 00:30:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7359	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

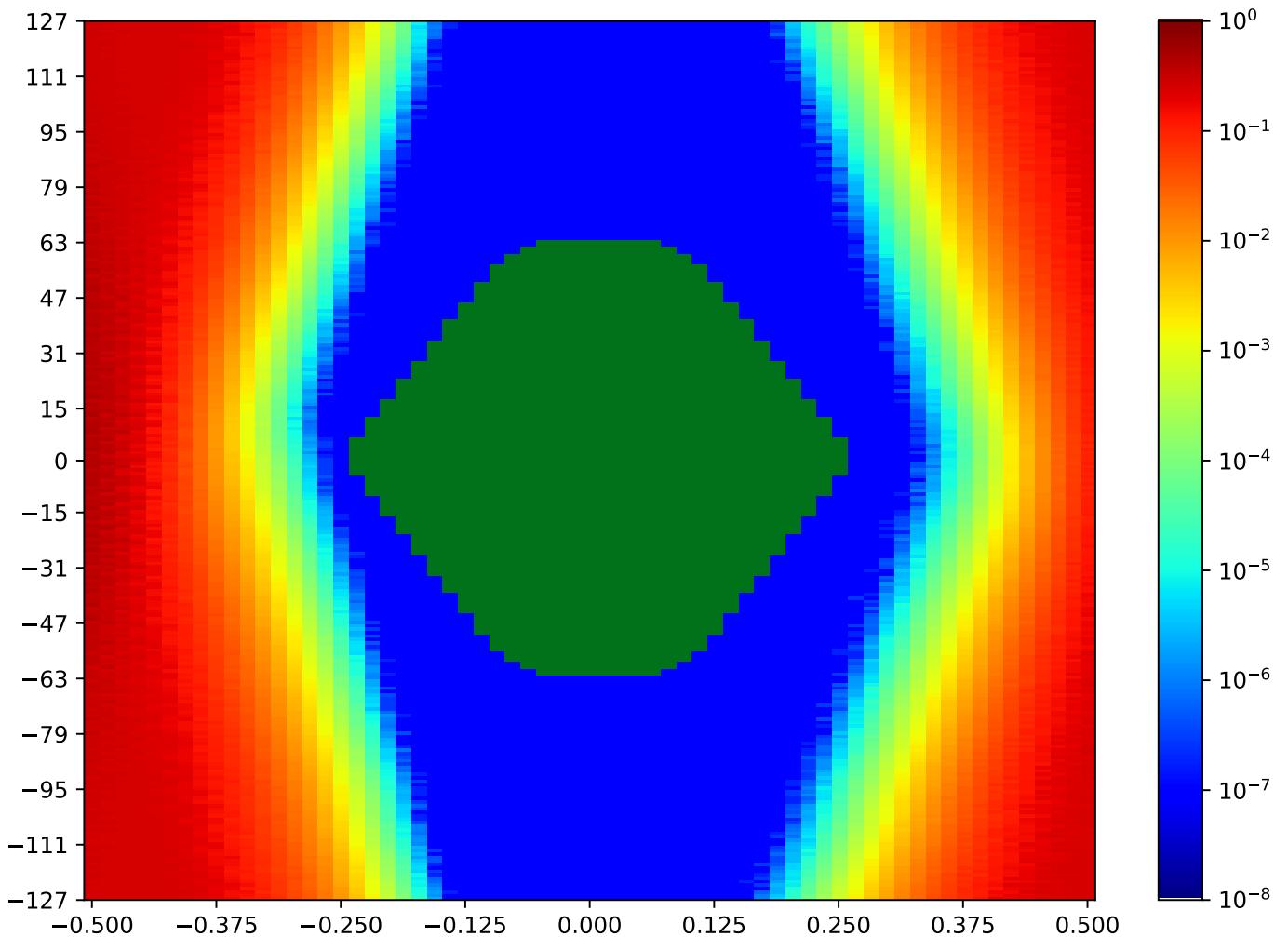


Figure 3.132: MSP_A_FPGA-TX1-04-RX18-04-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.6 MSP_A_FPGA-TX1-05-RX18-05-MSP_C_FPGA

Table 3.123: MSP_A_FPGA-TX1-05-RX18-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:27:02		2018-Jan-24 00:27:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7940	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

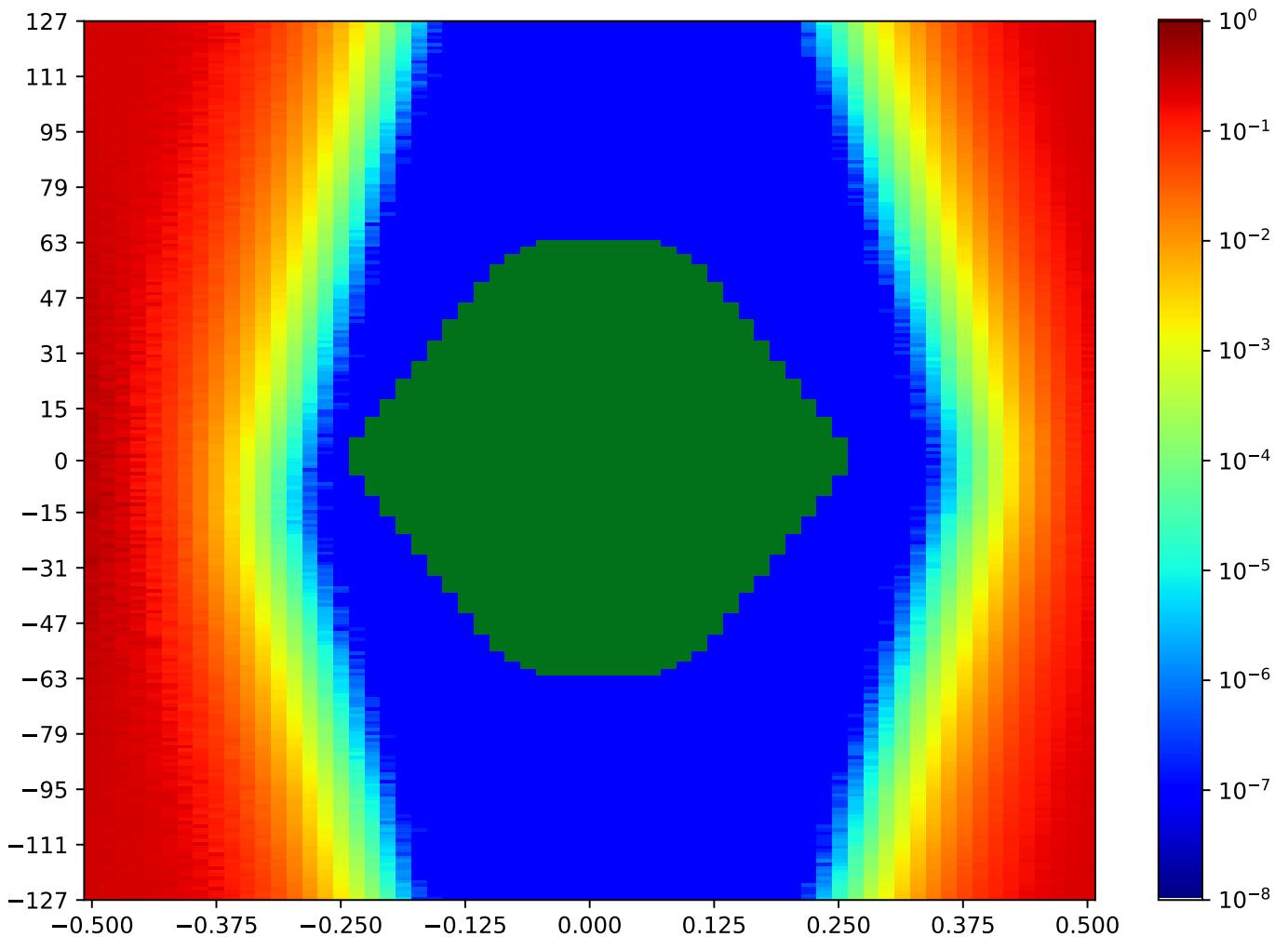


Figure 3.133: MSP_A_FPGA-TX1-05-RX18-05-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.7 MSP_A_FPGA-TX1-06-RX18-06-MSP_C_FPGA

Table 3.124: MSP_A_FPGA-TX1-06-RX18-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:30:58		2018-Jan-24 00:31:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8863	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

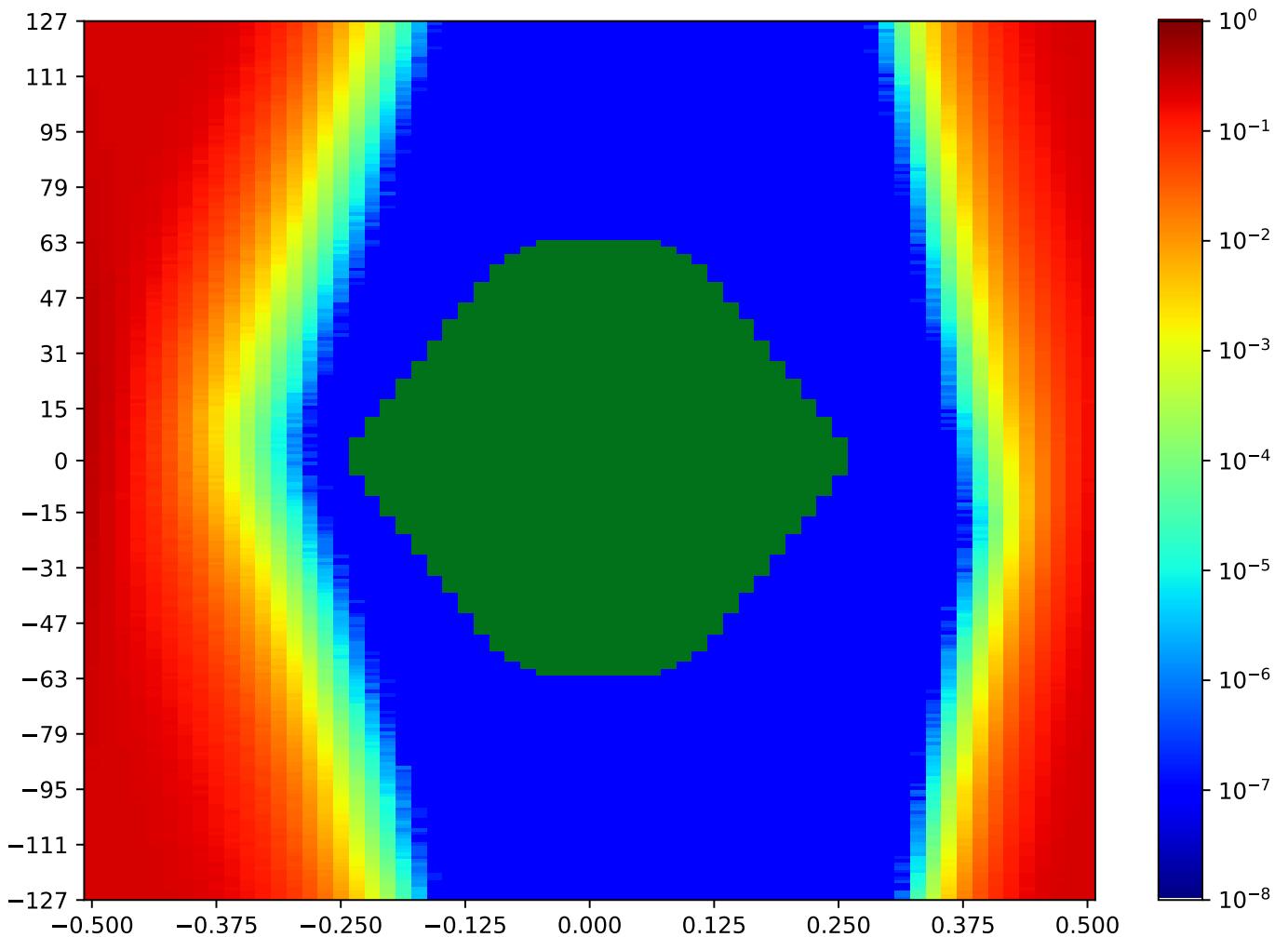


Figure 3.134: MSP_A_FPGA-TX1-06-RX18-06-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.8 MSP_A_FPGA-TX1-07-RX18-07-MSP_C_FPGA

Table 3.125: MSP_A_FPGA-TX1-07-RX18-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:27:44		2018-Jan-24 00:28:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8630	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

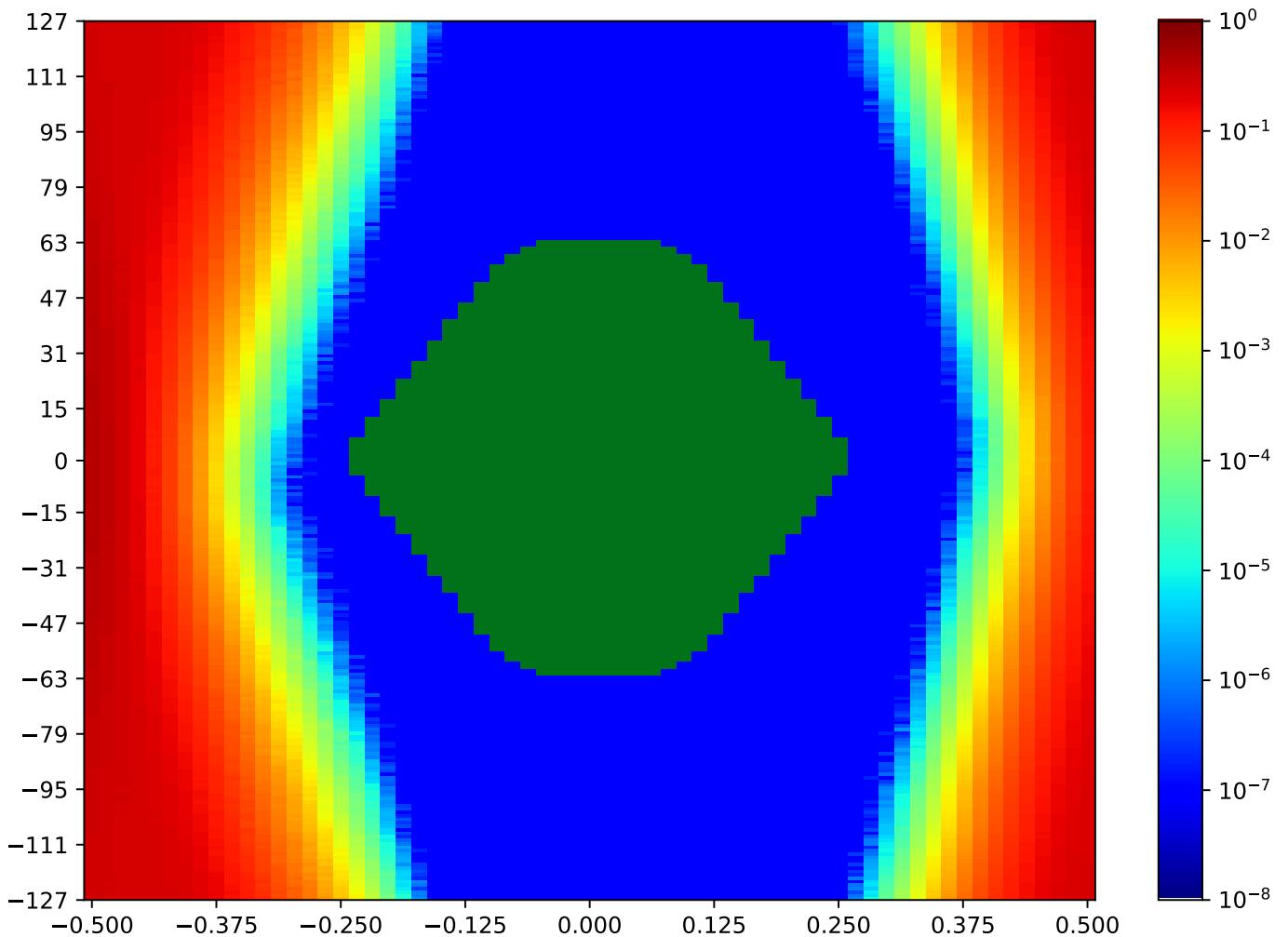


Figure 3.135: MSP_A_FPGA-TX1-07-RX18-07-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.9 MSP_A_FPGA-TX1-08-RX18-08-MSP_C_FPGA

Table 3.126: MSP_A_FPGA-TX1-08-RX18-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:30:37			2018-Jan-24 00:30:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	9062	44	67.69%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

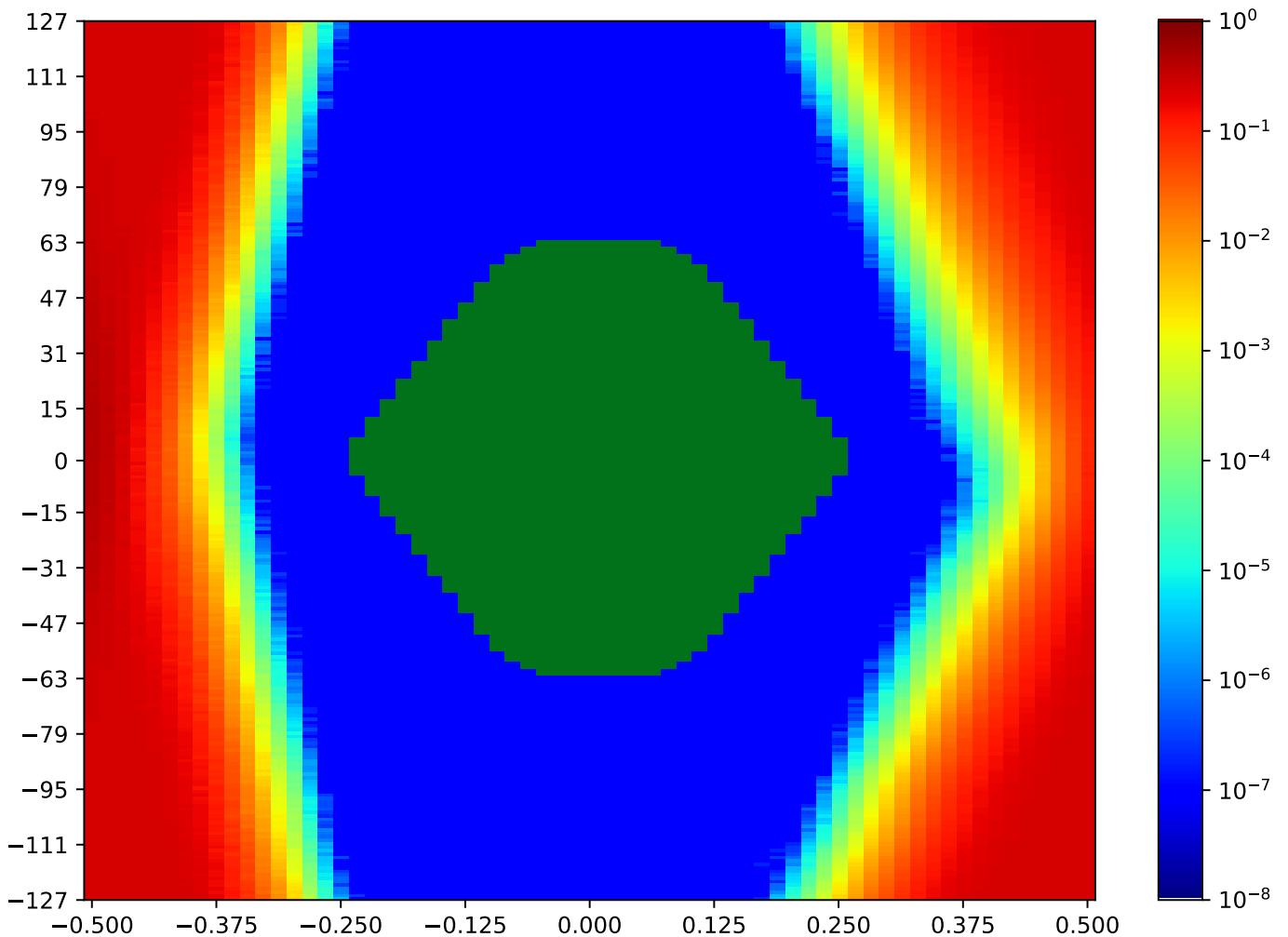


Figure 3.136: MSP_A_FPGA-TX1-08-RX18-08-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.10 MSP_A_FPGA-TX1-09-RX18-09-MSP_C_FPGA

Table 3.127: MSP_A_FPGA-TX1-09-RX18-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:28:27		2018-Jan-24 00:28:49	
Reset RX	OA	HO		HO (%)	
true	7722	38		58.46%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

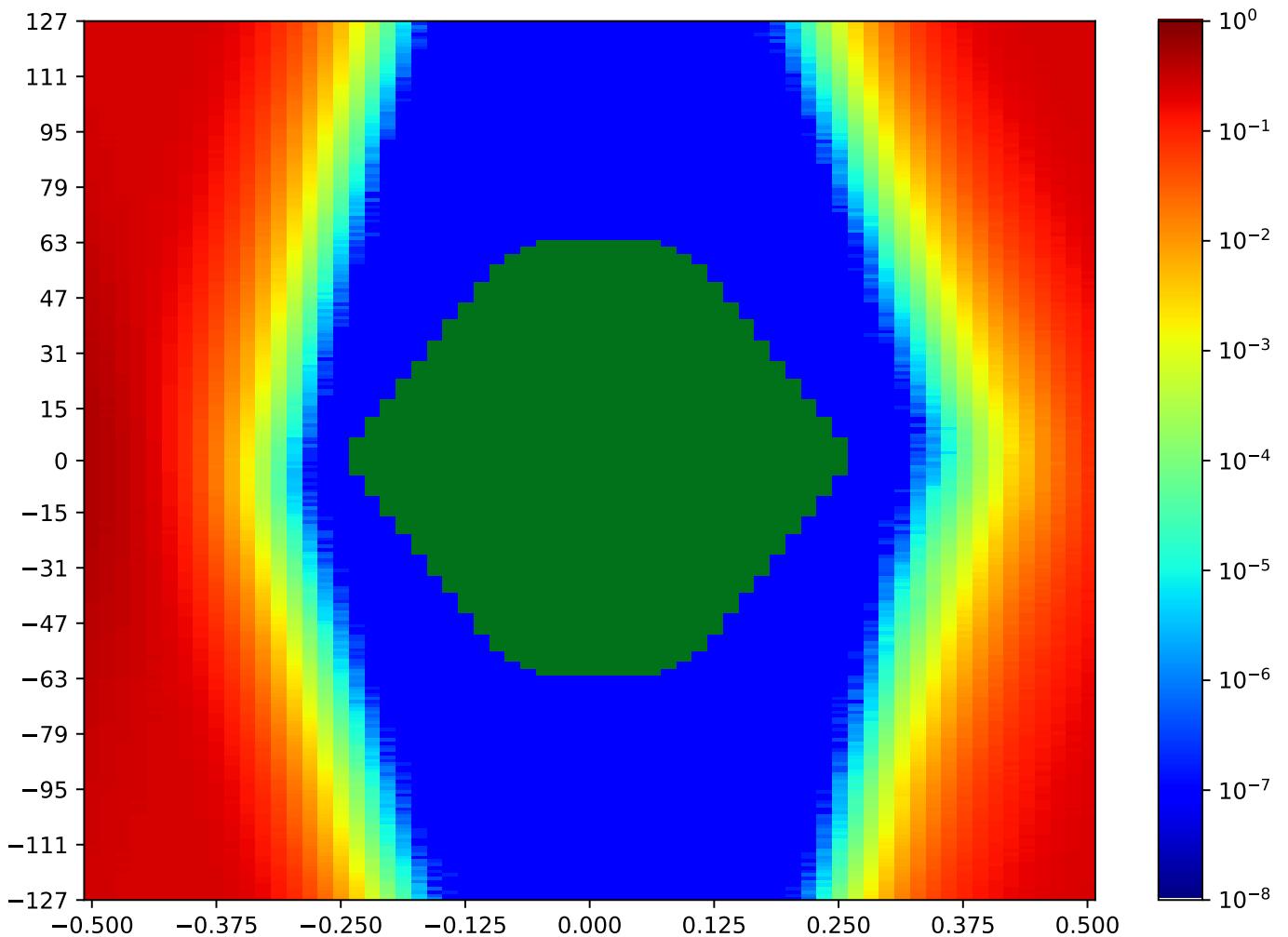


Figure 3.137: MSP_A_FPGA-TX1-09-RX18-09-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.11 MSP_A_FPGA-TX1-10-RX18-10-MSP_C_FPGA

Table 3.128: MSP_A_FPGA-TX1-10-RX18-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:29:54		2018-Jan-24 00:30:15	
Reset RX	OA	HO		VO VO (%)	
true	6686	36		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

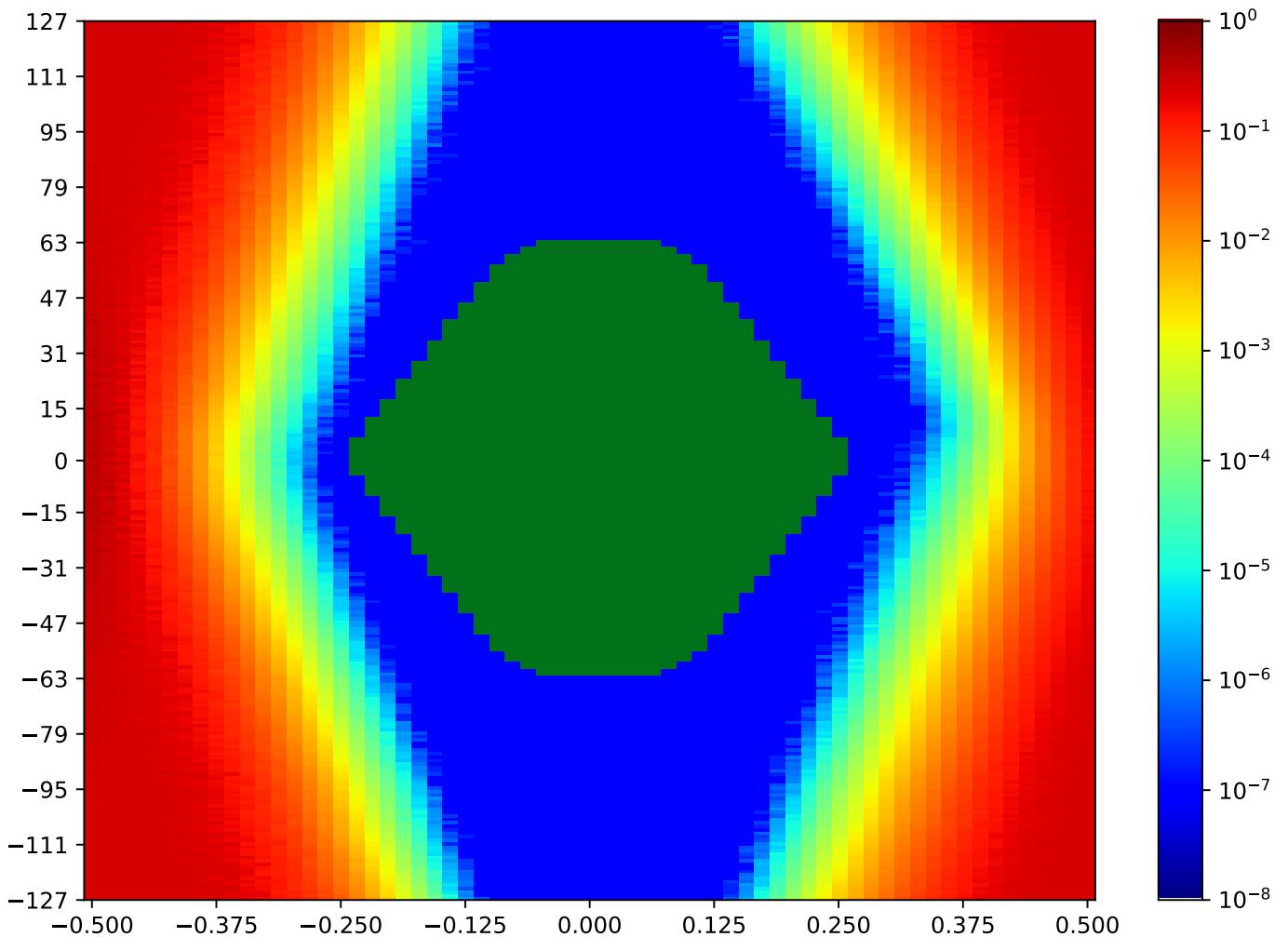


Figure 3.138: MSP_A_FPGA-TX1-10-RX18-10-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.10.12 MSP_A_FPGA-TX1-11-RX18-11-MSP_C_FPGA

Table 3.129: MSP_A_FPGA-TX1-11-RX18-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:29:32		2018-Jan-24 00:29:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8265	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

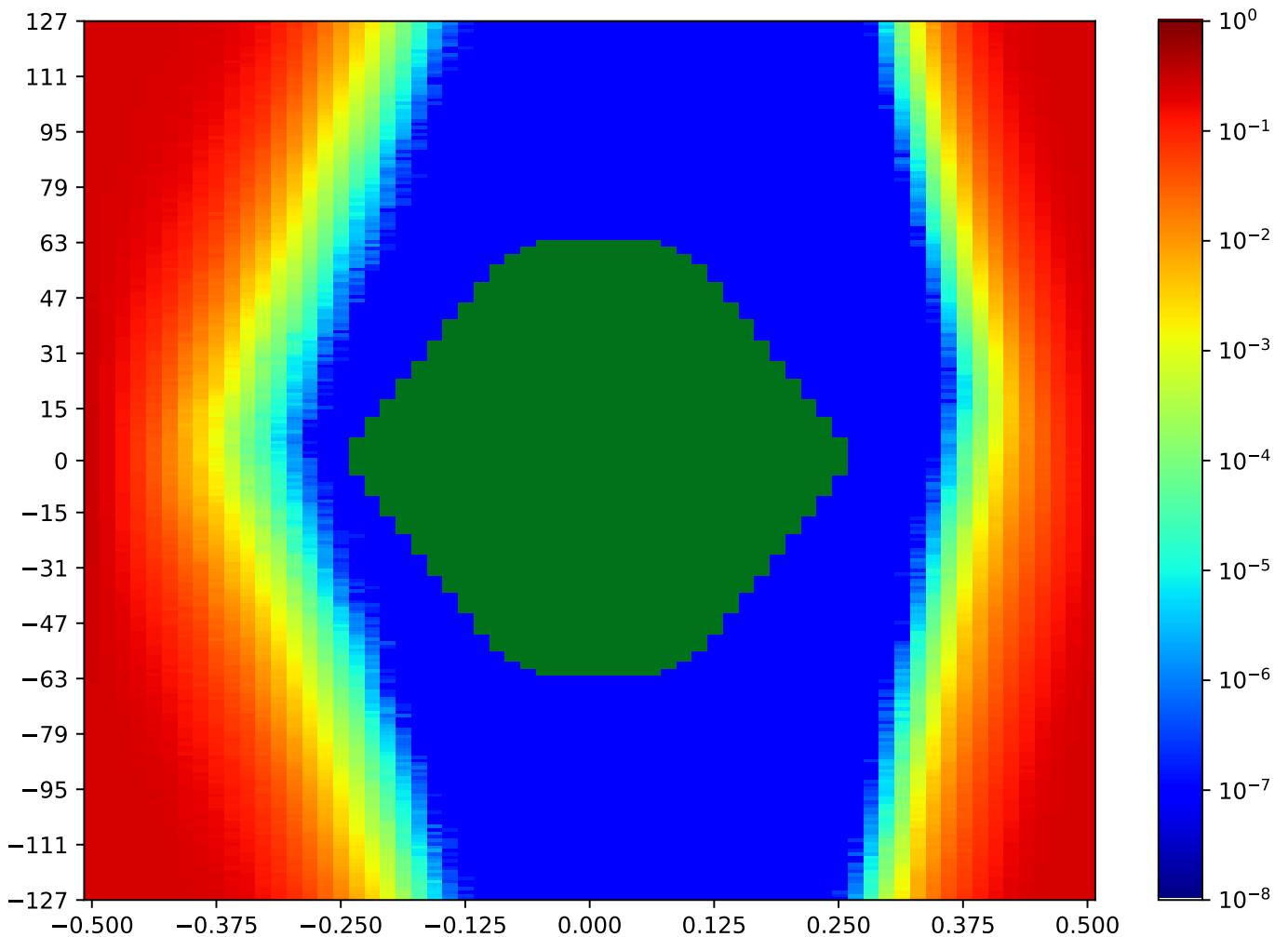


Figure 3.139: MSP_A_FPGA-TX1-11-RX18-11-MSP_C_FPGA

Call back to summary Figure 3.127. Sibling eye diagrams: V1-6.4.

3.11 MSP_A TX2 MSP_C RX17 Minipod Loopback

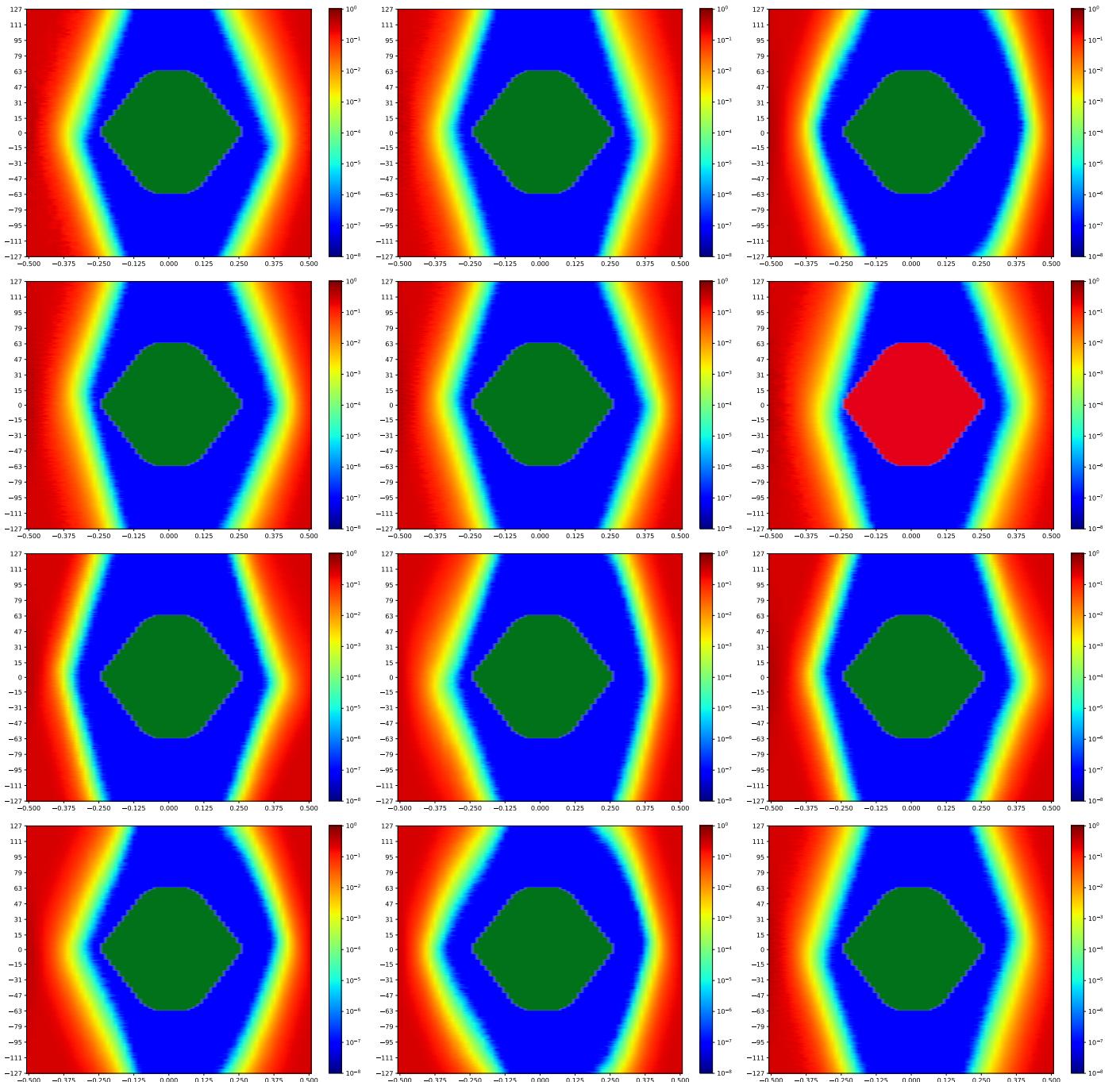


Figure 3.140: MSP_A TX2 MSP_C RX17 Minipod Loopback

A cross-reference to Figure 3.140. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.153.

3.11.1 MSP_A_FPGA-TX2-00-RX17-00-MSP_C_FPGA

Table 3.130: MSP_A_FPGA-TX2-00-RX17-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:32:23		2018-Jan-24 00:32:44	
Reset RX	OA	HO		HO (%)	
true	7332	35		53.85%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

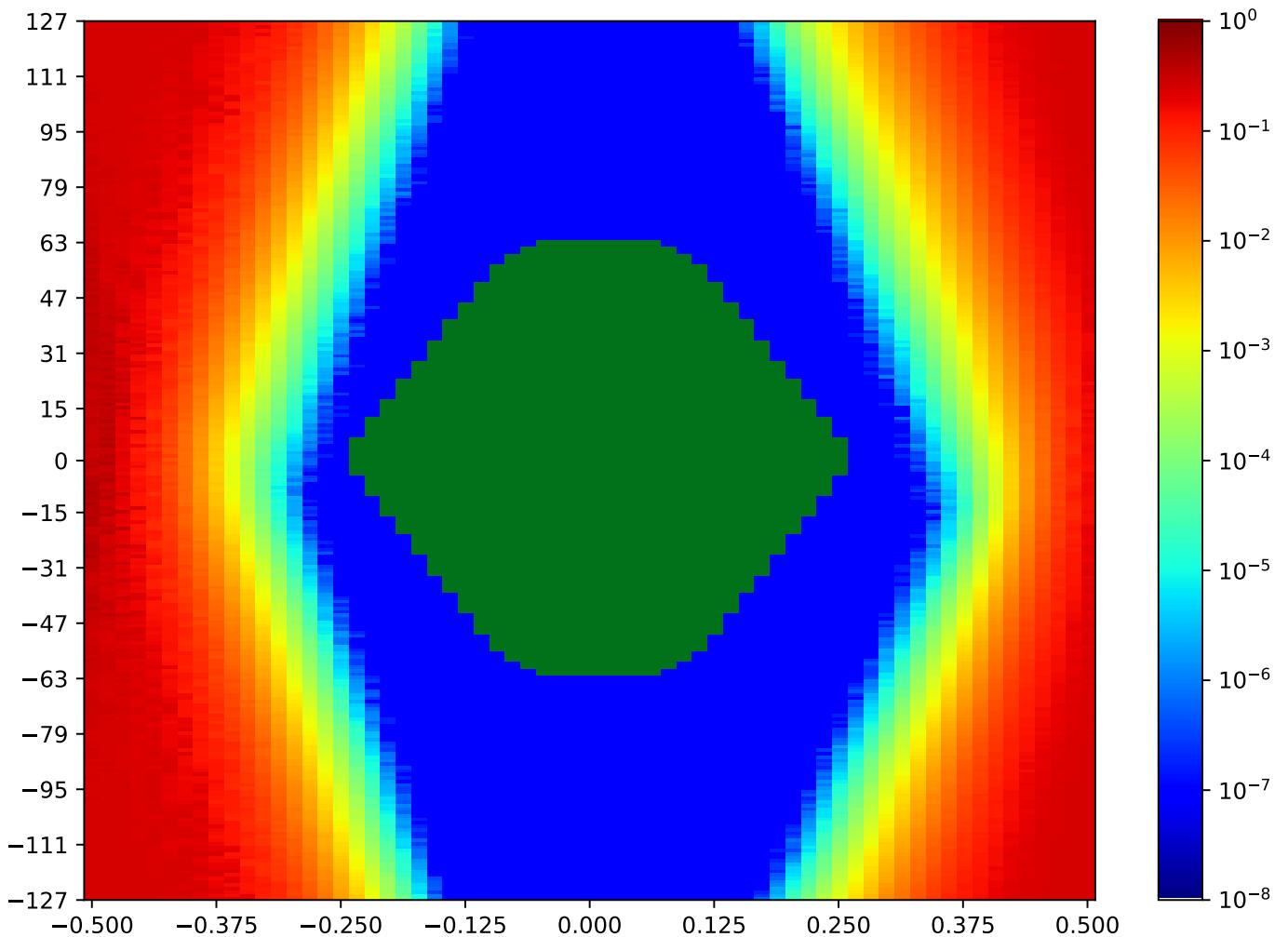


Figure 3.141: MSP_A_FPGA-TX2-00-RX17-00-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.2 MSP_A_FPGA-TX2-01-RX17-01-MSP_C_FPGA

Table 3.131: MSP_A_FPGA-TX2-01-RX17-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:31:40		2018-Jan-24 00:32:01	
Reset RX	OA	HO		HO (%)	
true	7452	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

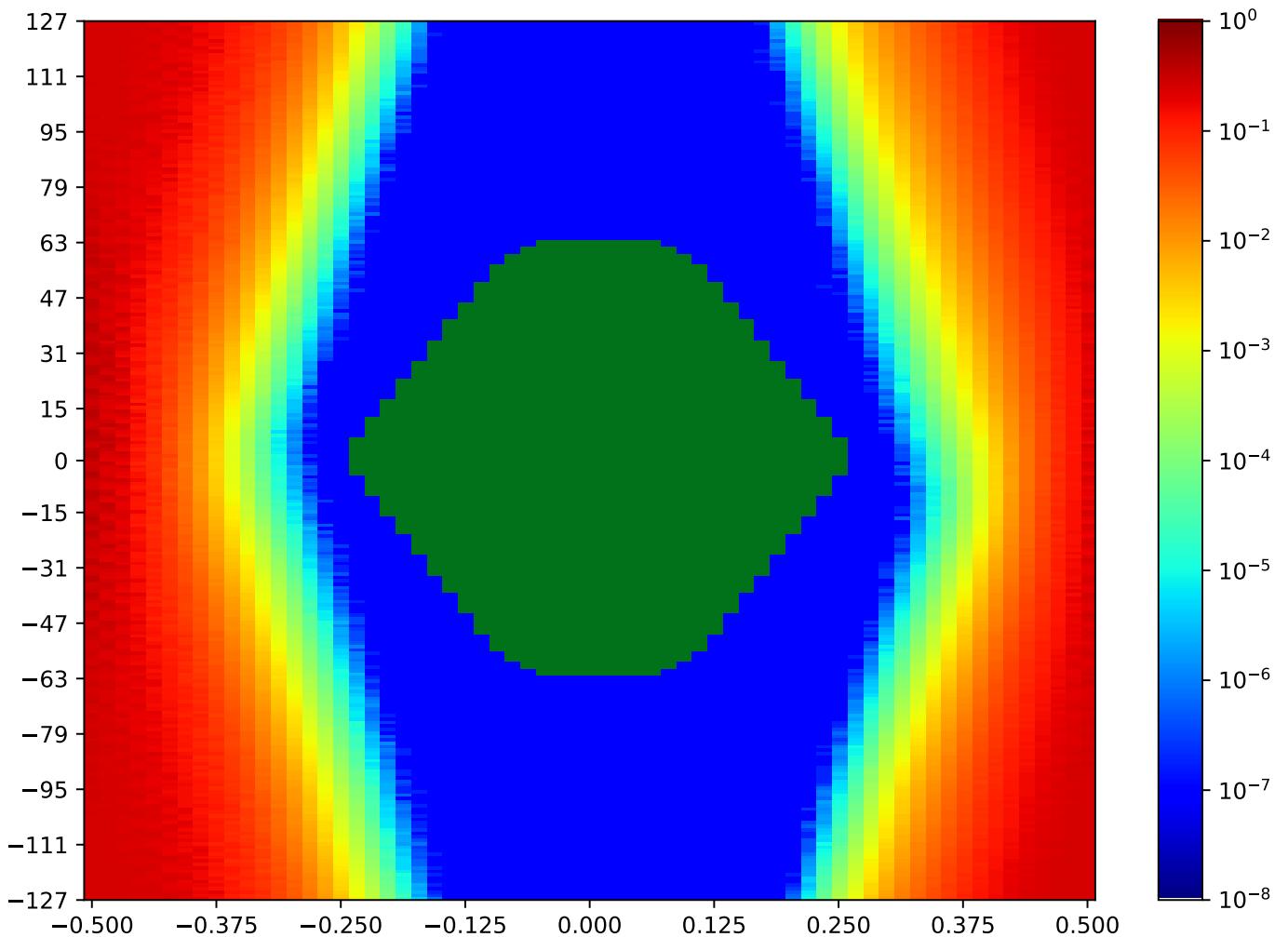


Figure 3.142: MSP_A_FPGA-TX2-01-RX17-01-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.3 MSP_A_FPGA-TX2-02-RX17-02-MSP_C_FPGA

Table 3.132: MSP_A_FPGA-TX2-02-RX17-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:33:27		2018-Jan-24 00:33:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8905	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

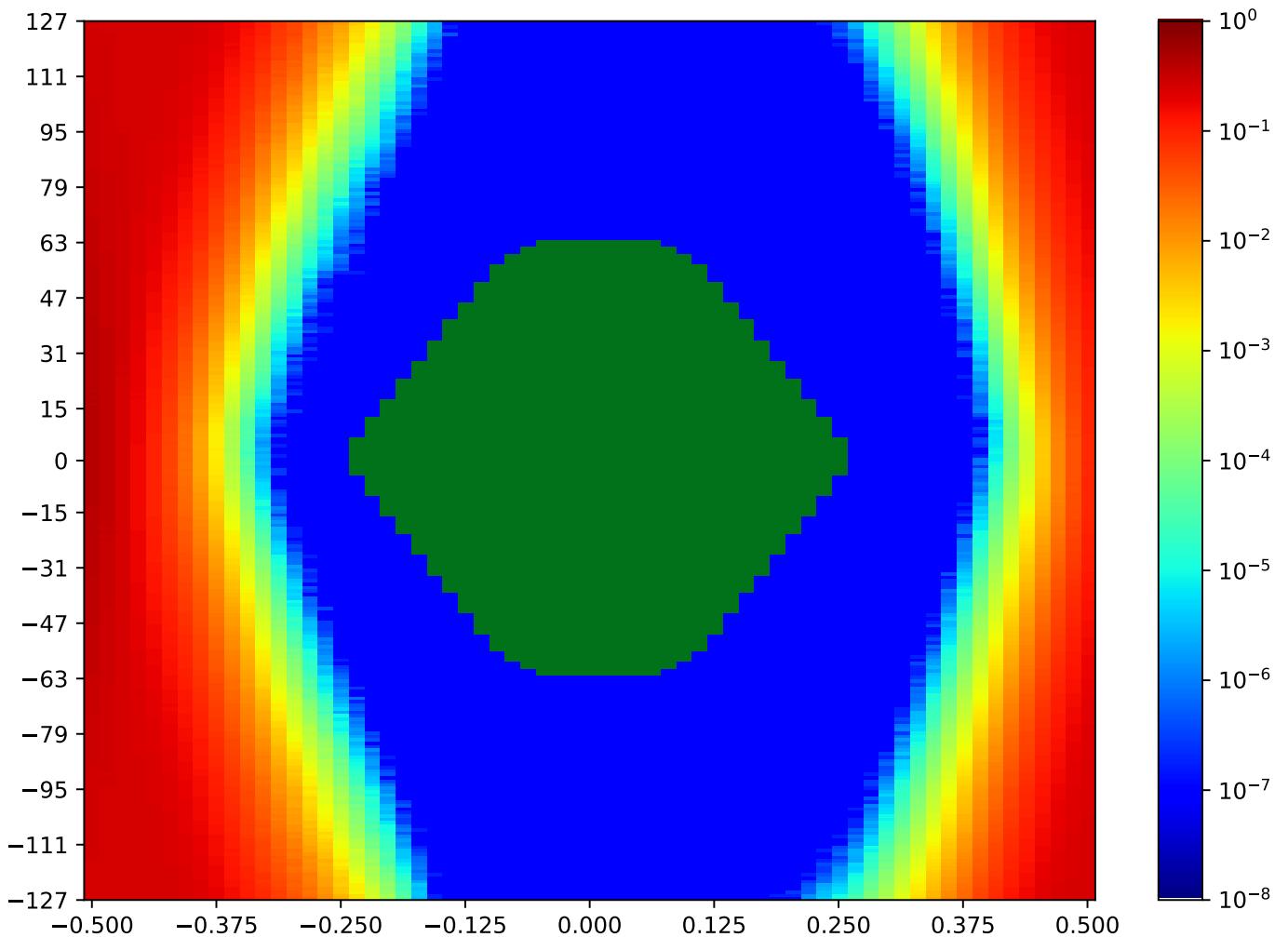


Figure 3.143: MSP_A_FPGA-TX2-02-RX17-02-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.4 MSP_A_FPGA-TX2-03-RX17-03-MSP_C_FPGA

Table 3.133: MSP_A_FPGA-TX2-03-RX17-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:31:19		2018-Jan-24 00:31:40	
Reset RX	OA	HO		HO (%)	
true	7659	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

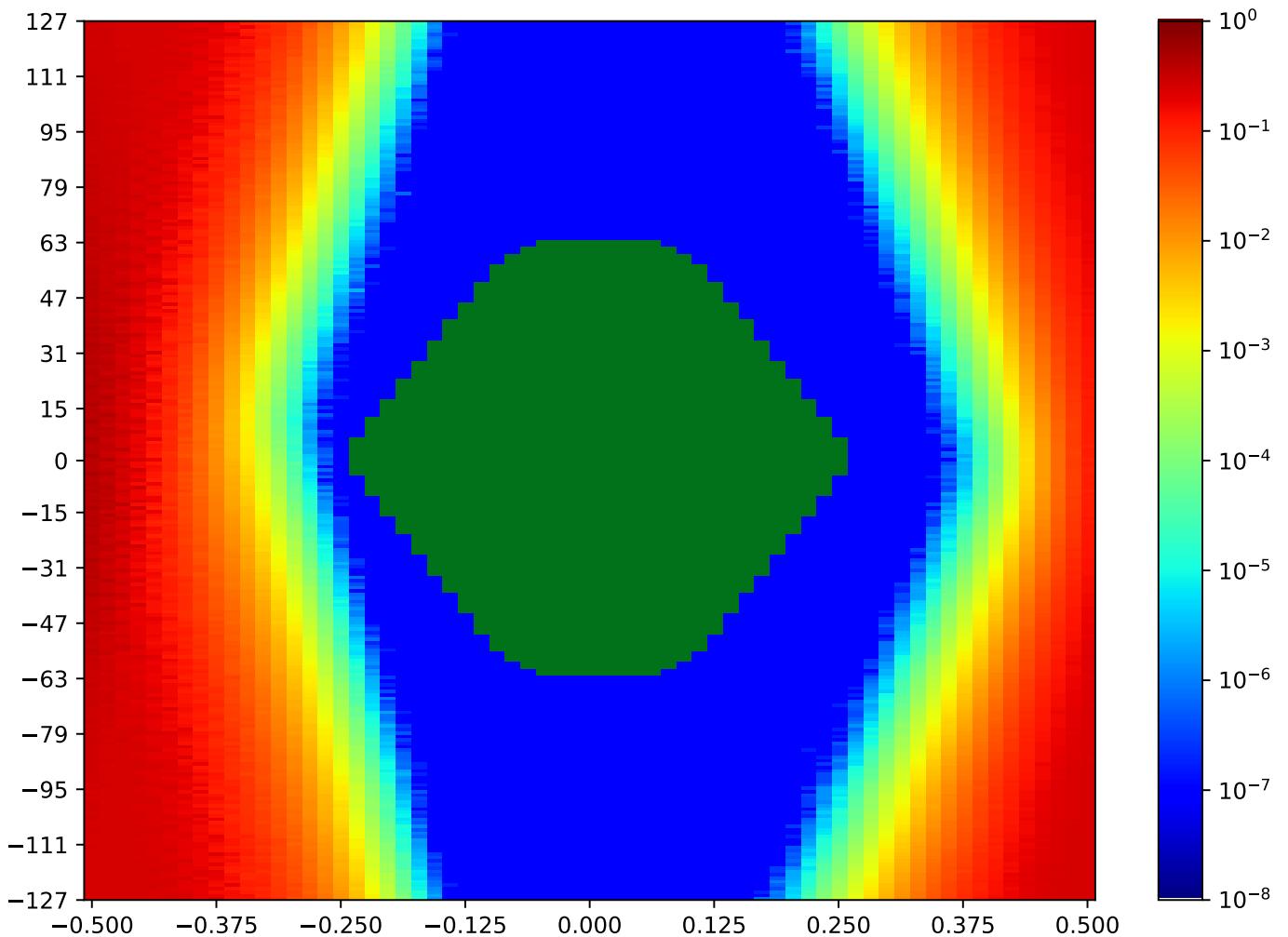


Figure 3.144: MSP_A_FPGA-TX2-03-RX17-03-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.5 MSP_A_FPGA-TX2-04-RX17-04-MSP_C_FPGA

Table 3.134: MSP_A_FPGA-TX2-04-RX17-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:34:31			2018-Jan-24 00:34:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7748	39	60.00%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

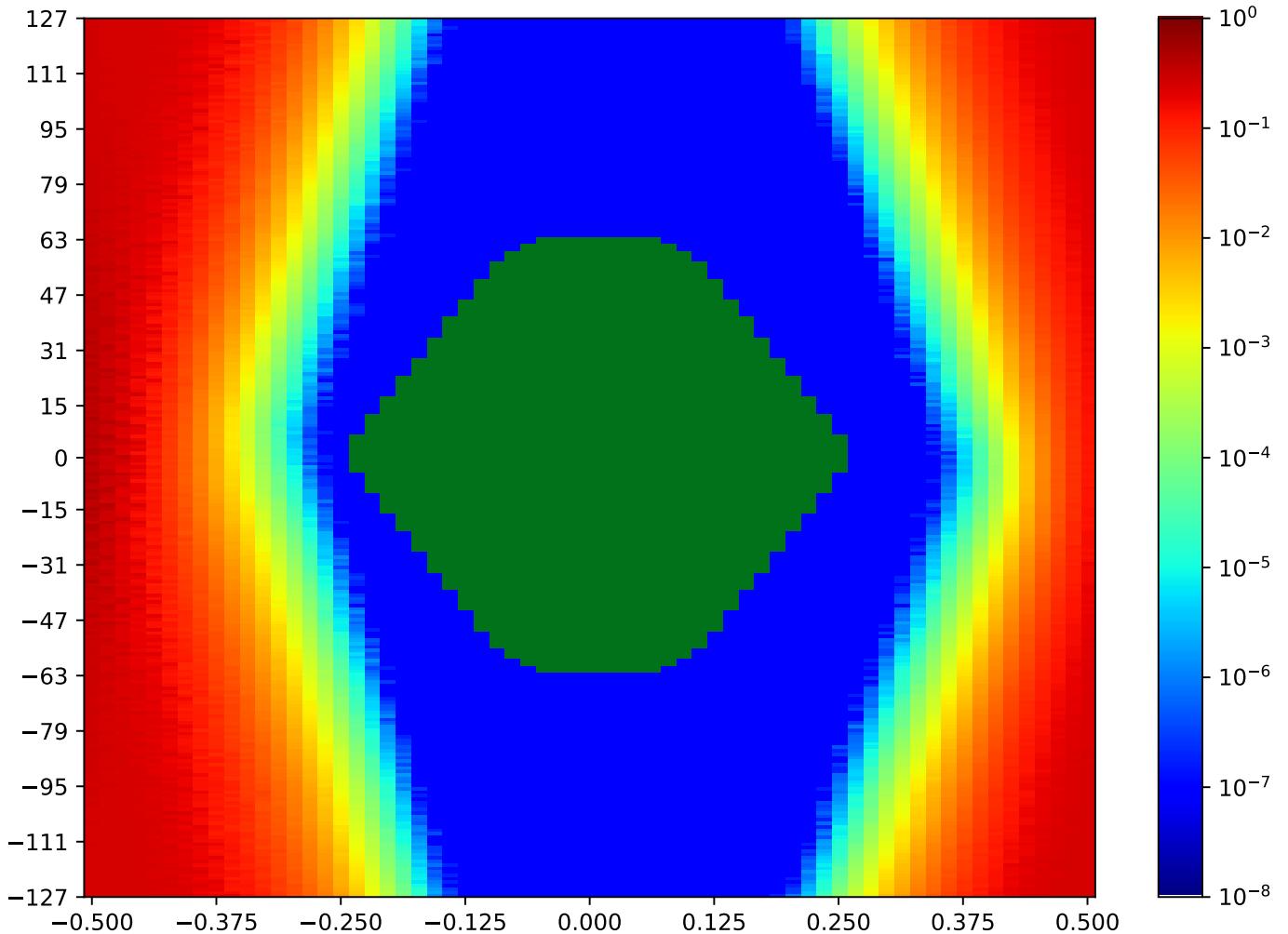


Figure 3.145: MSP_A_FPGA-TX2-04-RX17-04-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.6 MSP_A_FPGA-TX2-05-RX17-05-MSP_C_FPGA

Table 3.135: MSP_A_FPGA-TX2-05-RX17-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:32:02		2018-Jan-24 00:32:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6852	35	53.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

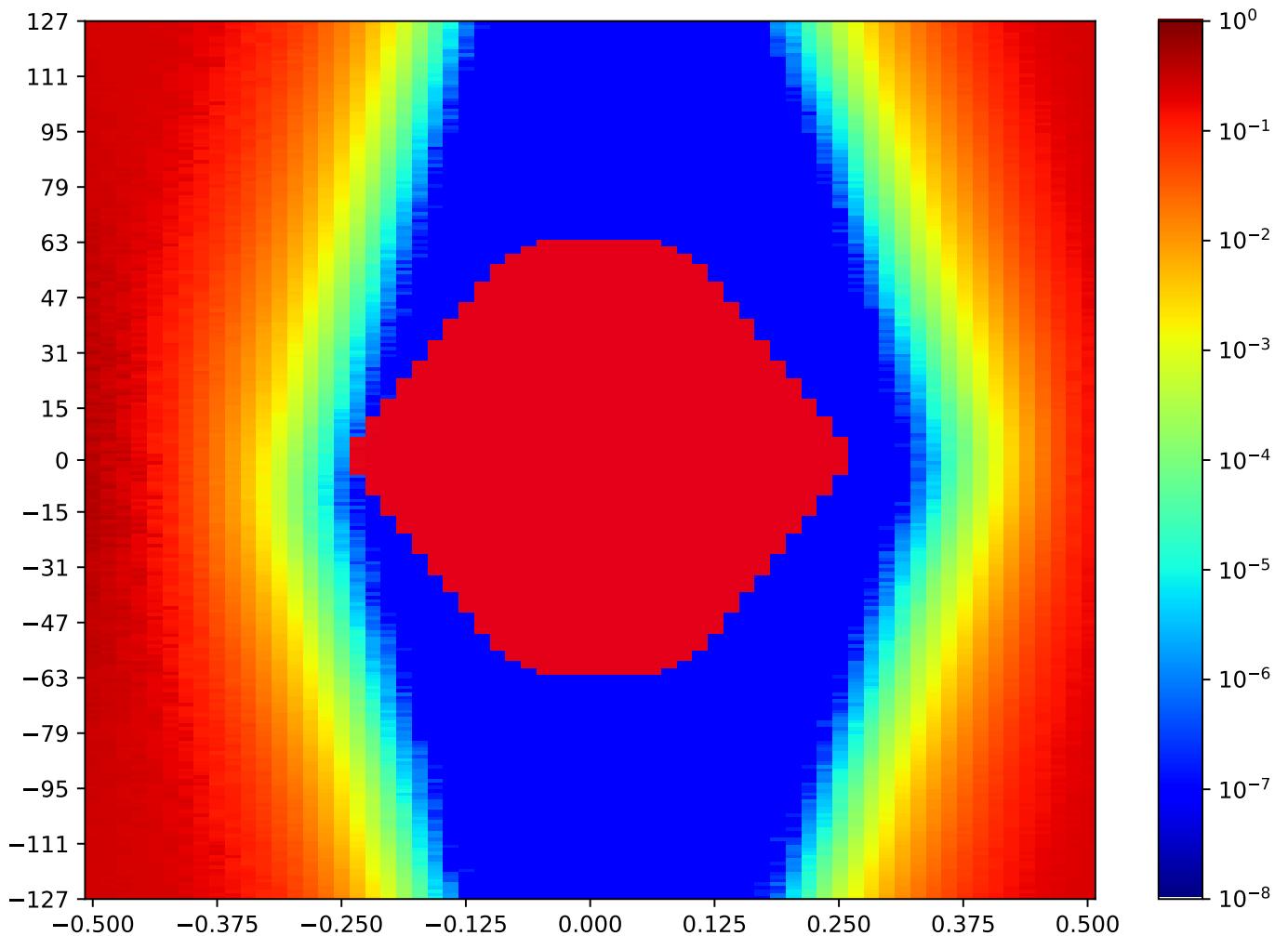


Figure 3.146: MSP_A_FPGA-TX2-05-RX17-05-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.7 MSP_A_FPGA-TX2-06-RX17-06-MSP_C_FPGA

Table 3.136: MSP_A_FPGA-TX2-06-RX17-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:35:13		2018-Jan-24 00:35:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8502	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

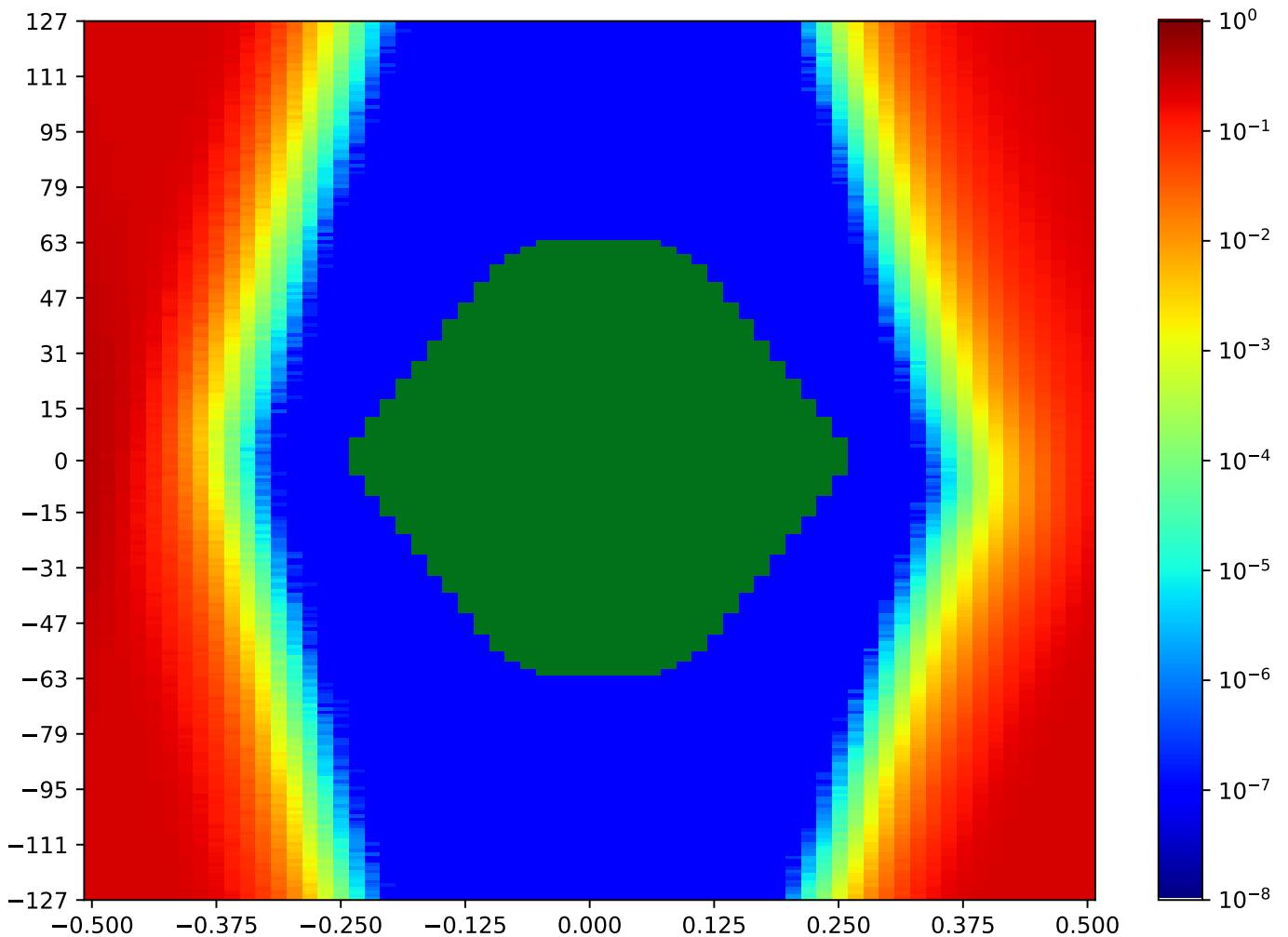


Figure 3.147: MSP_A_FPGA-TX2-06-RX17-06-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.8 MSP_A_FPGA-TX2-07-RX17-07-MSP_C_FPGA

Table 3.137: MSP_A_FPGA-TX2-07-RX17-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:32:44		2018-Jan-24 00:33:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8269	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

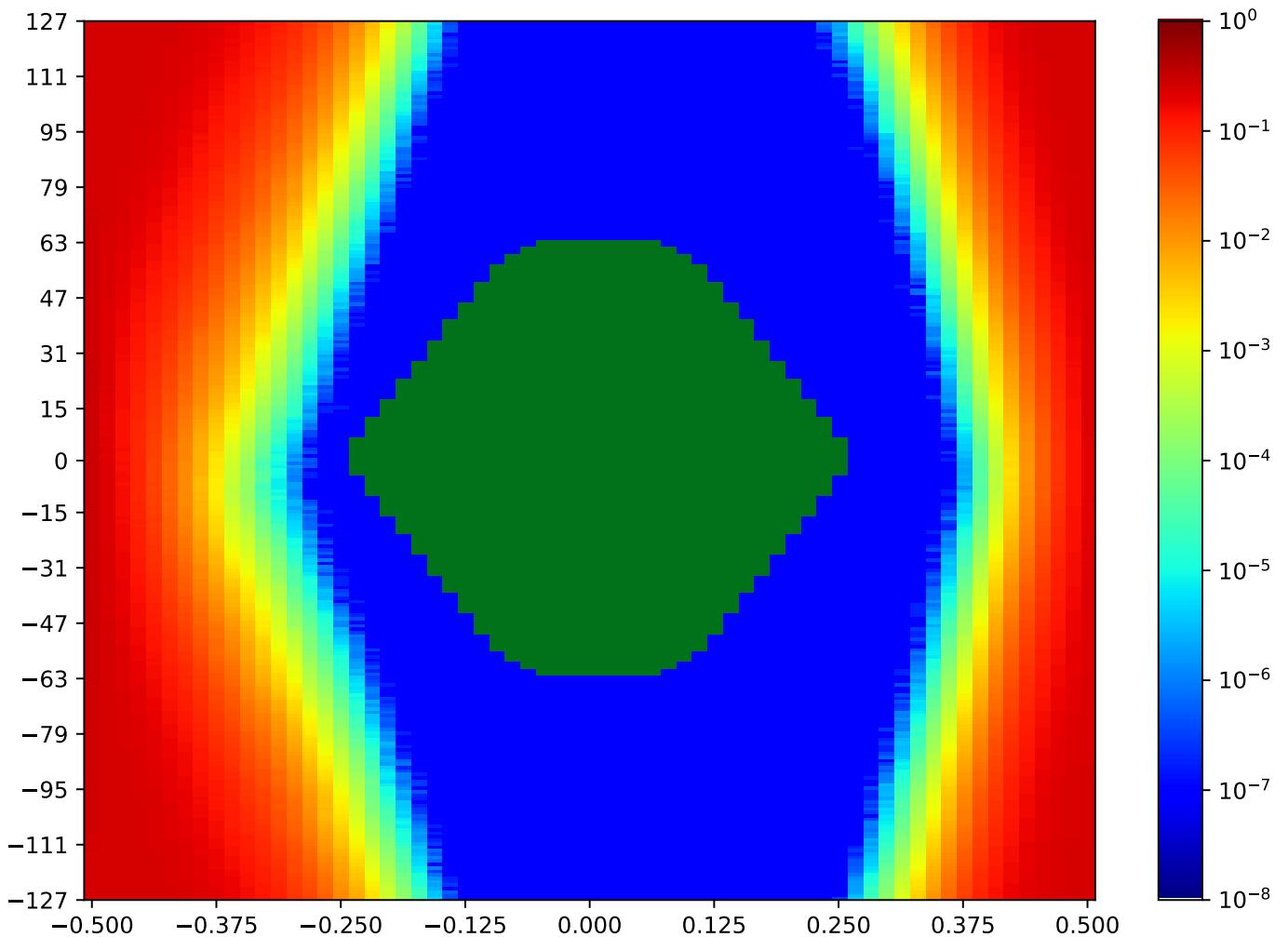


Figure 3.148: MSP_A_FPGA-TX2-07-RX17-07-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.9 MSP_A_FPGA-TX2-08-RX17-08-MSP_C_FPGA

Table 3.138: MSP_A_FPGA-TX2-08-RX17-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:34:52			2018-Jan-24 00:35:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	8119	40	61.54%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

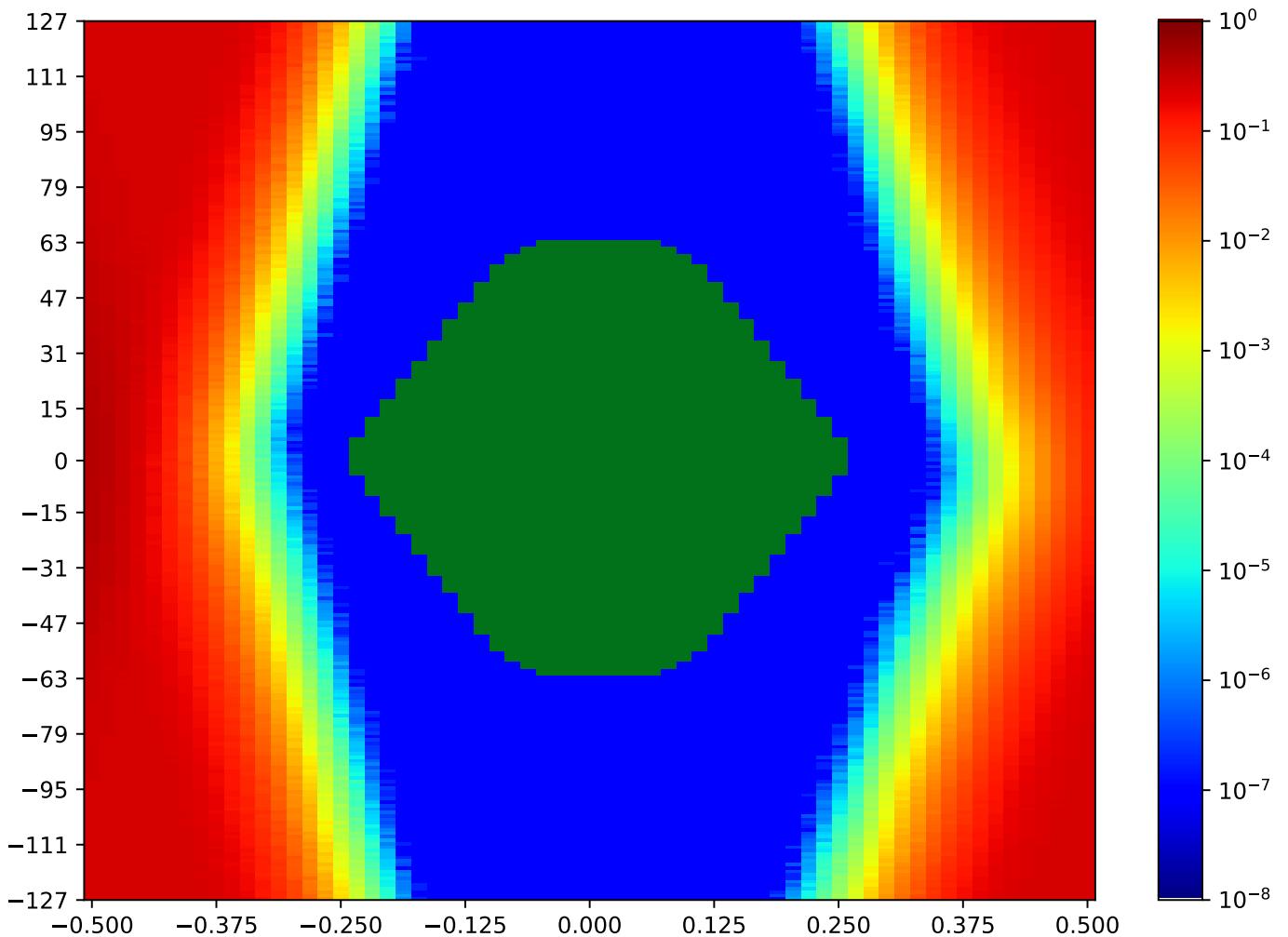


Figure 3.149: MSP_A_FPGA-TX2-08-RX17-08-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.10 MSP_A_FPGA-TX2-09-RX17-09-MSP_C_FPGA

Table 3.139: MSP_A_FPGA-TX2-09-RX17-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:33:05		2018-Jan-24 00:33:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7437	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

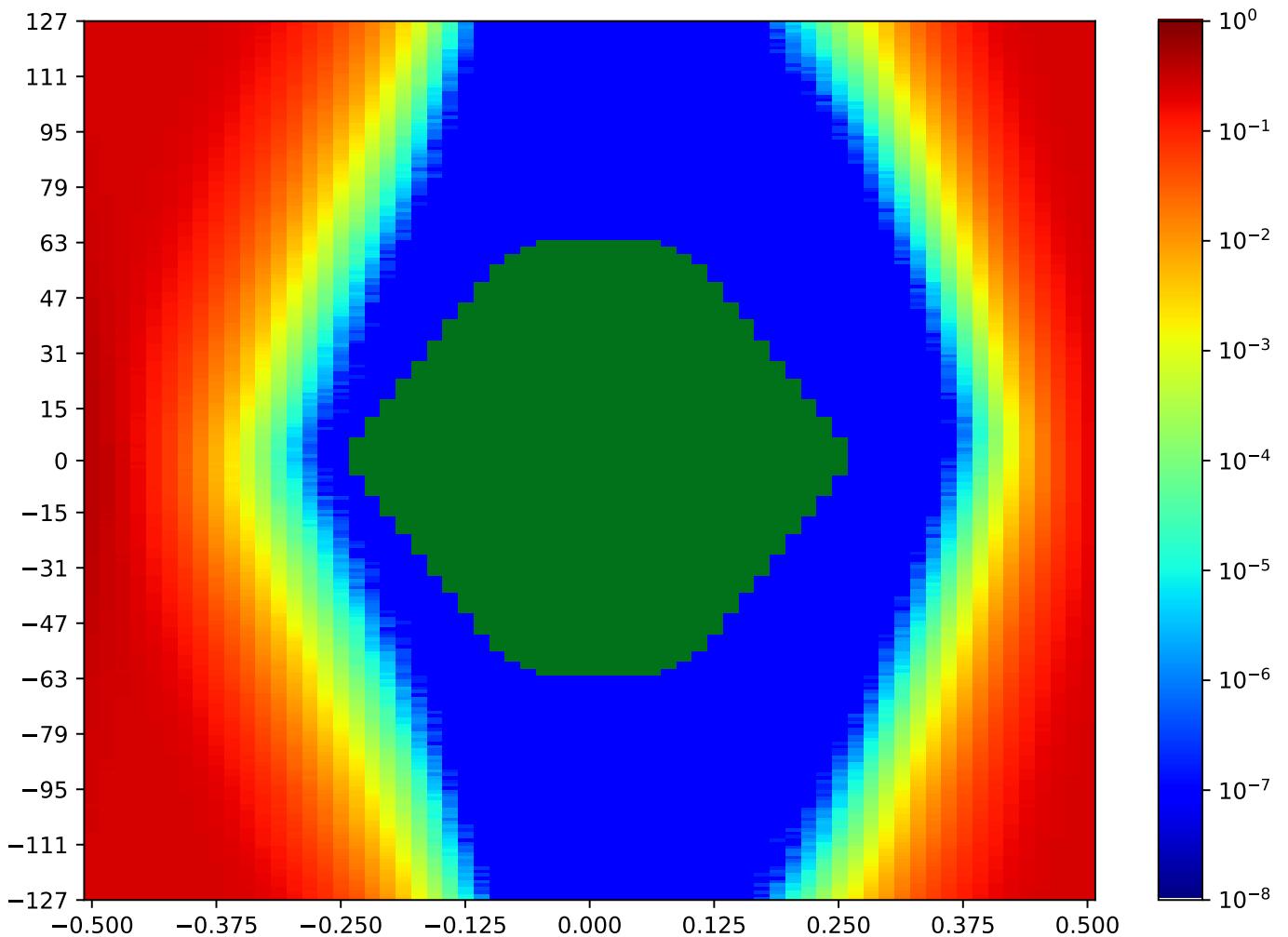


Figure 3.150: MSP_A_FPGA-TX2-09-RX17-09-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.11 MSP_A_FPGA-TX2-10-RX17-10-MSP_C_FPGA

Table 3.140: MSP_A_FPGA-TX2-10-RX17-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:34:09		2018-Jan-24 00:34:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8210	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

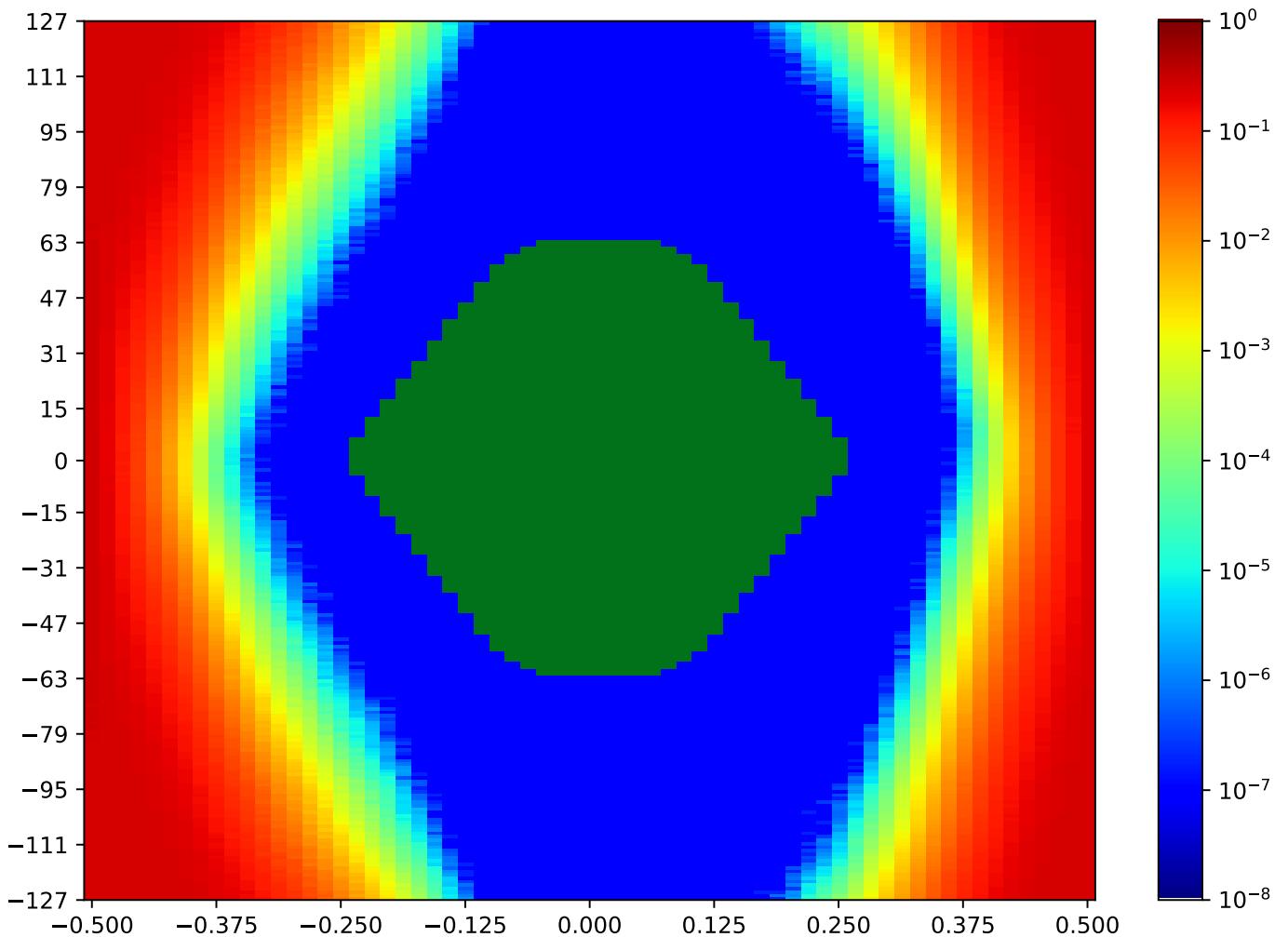


Figure 3.151: MSP_A_FPGA-TX2-10-RX17-10-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.11.12 MSP_A_FPGA-TX2-11-RX17-11-MSP_C_FPGA

Table 3.141: MSP_A_FPGA-TX2-11-RX17-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:33:48			2018-Jan-24 00:34:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7682	38	58.46%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

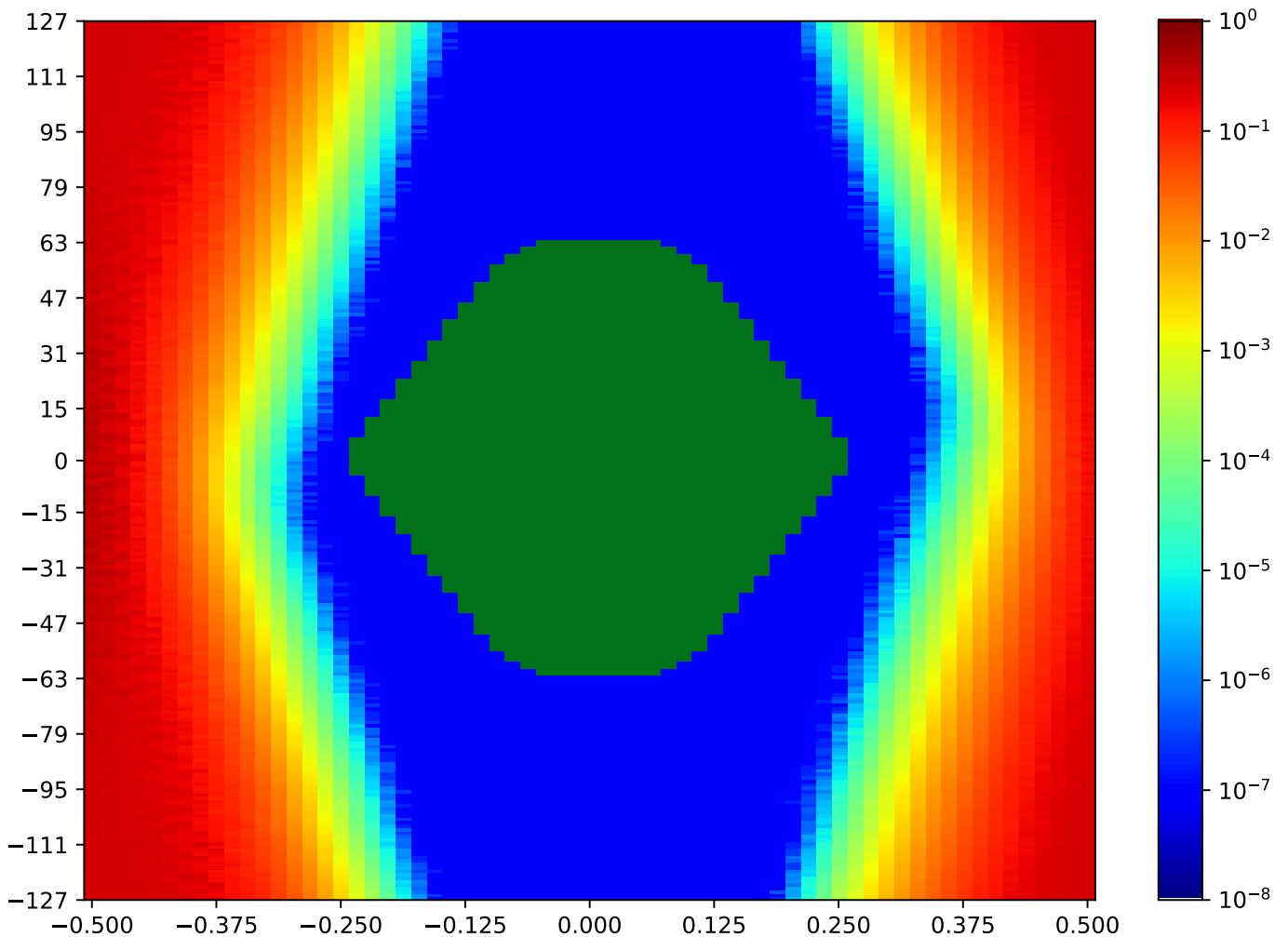


Figure 3.152: MSP_A_FPGA-TX2-11-RX17-11-MSP_C_FPGA

Call back to summary Figure 3.140. Sibling eye diagrams: V1-6.4.

3.12 MSP_C TX3 MSP_A RX9 Minipod Loopback

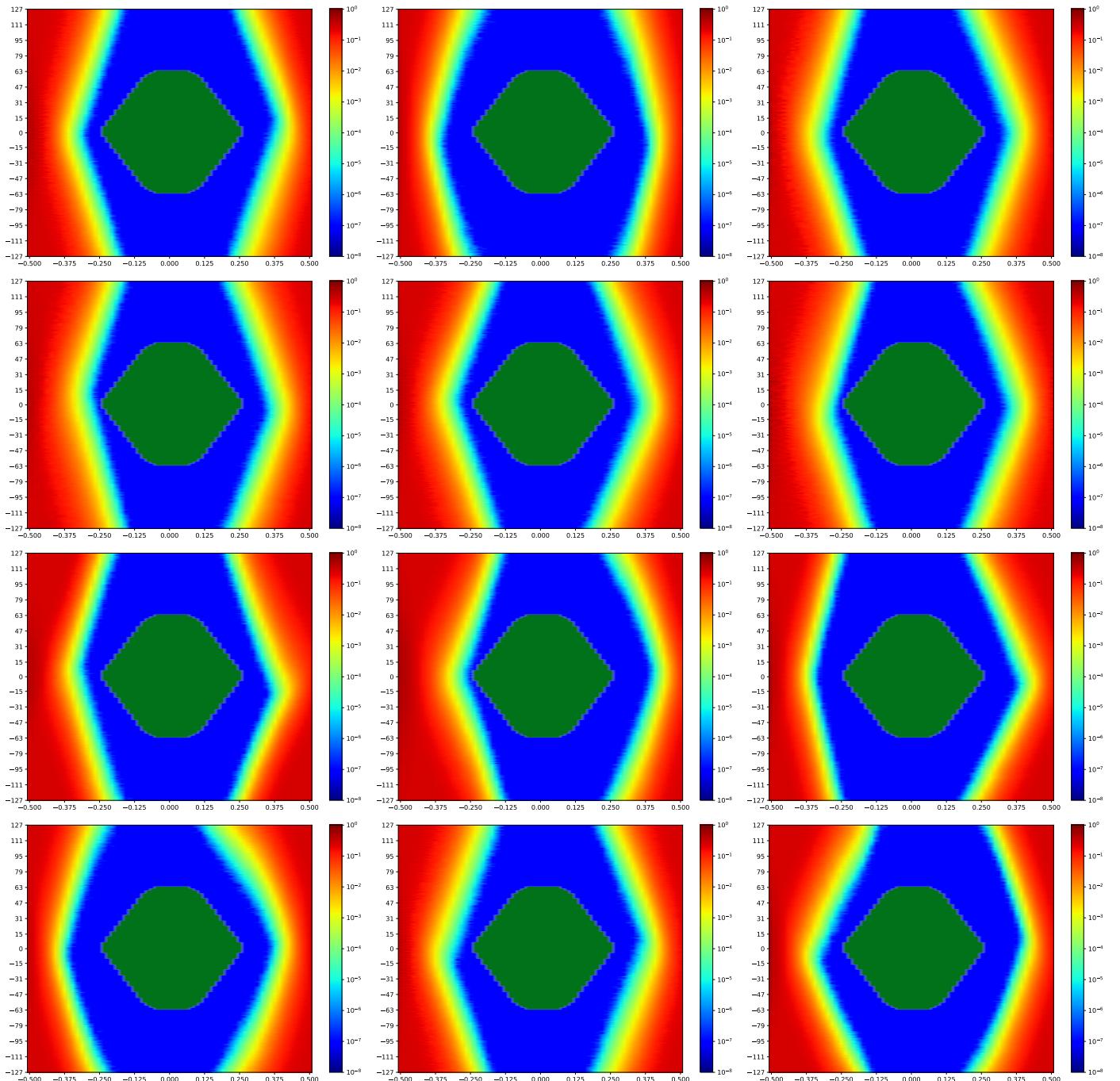


Figure 3.153: MSP_C TX3 MSP_A RX9 Minipod Loopback

A cross-reference to Figure 3.153. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.166.

3.12.1 MSP_C_FPGA-TX3-00-RX9-00-MSP_A_FPGA

Table 3.142: MSP_C_FPGA-TX3-00-RX9-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:36:39		2018-Jan-24 00:37:00	
Reset RX	OA	HO		HO (%)	
true	8023	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

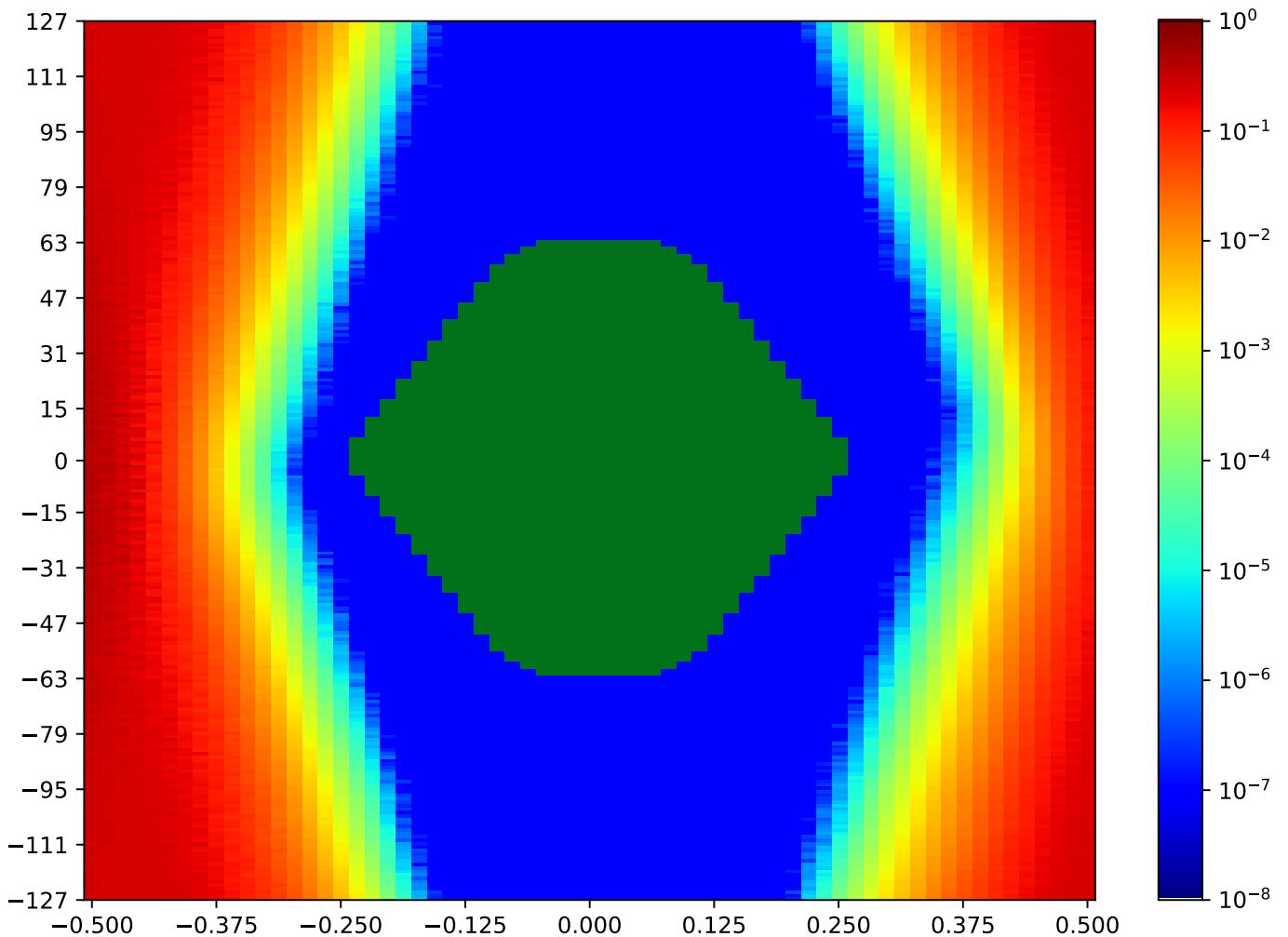


Figure 3.154: MSP_C_FPGA-TX3-00-RX9-00-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.2 MSP_C_FPGA-TX3-01-RX9-01-MSP_A_FPGA

Table 3.143: MSP_C_FPGA-TX3-01-RX9-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:37:22		2018-Jan-24 00:37:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9246	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

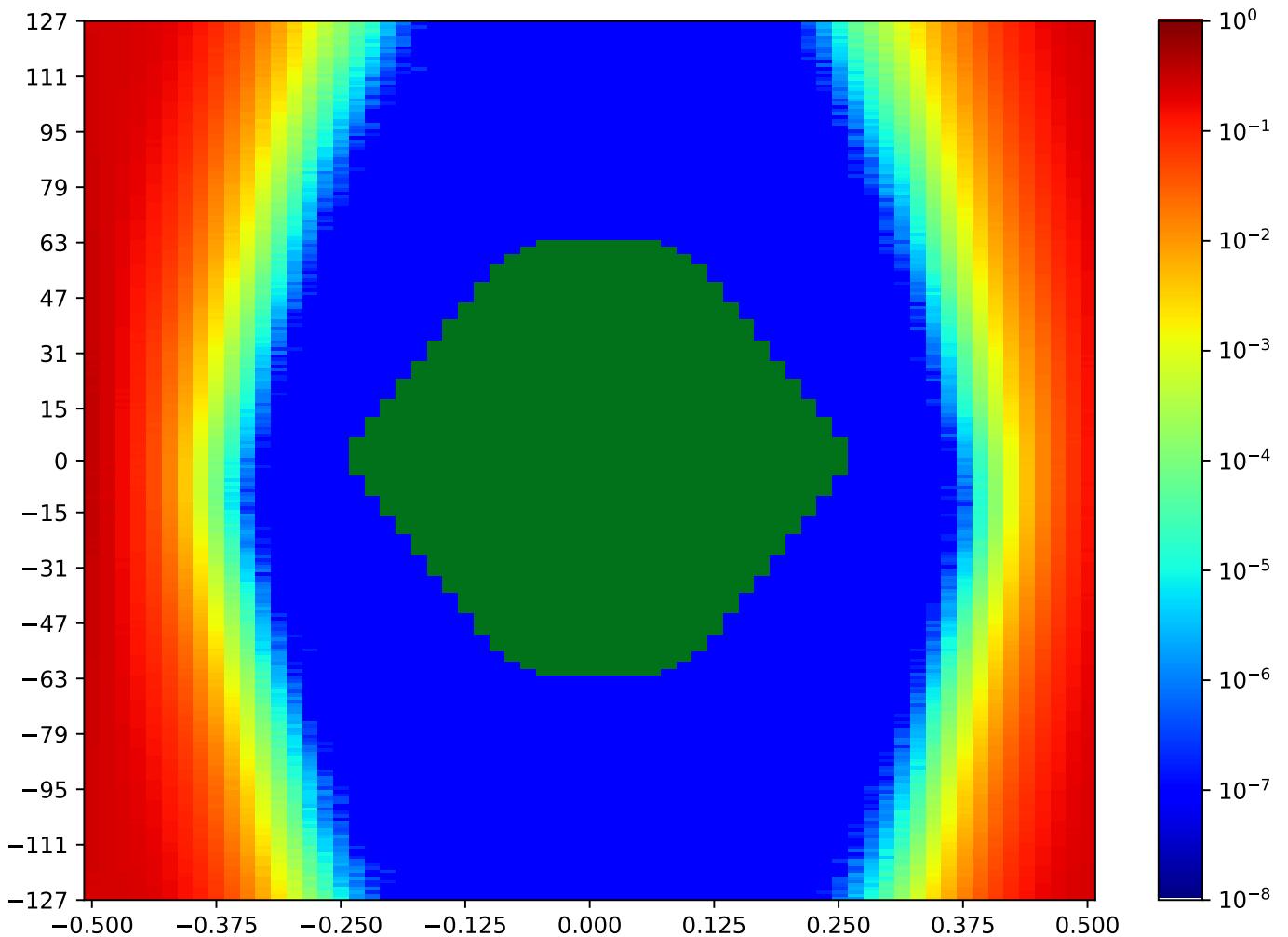


Figure 3.155: MSP_C_FPGA-TX3-01-RX9-01-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.3 MSP_C_FPGA-TX3-02-RX9-02-MSP_A_FPGA

Table 3.144: MSP_C_FPGA-TX3-02-RX9-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:37:43		2018-Jan-24 00:38:04	
Reset RX	OA	HO		HO (%)	
true	7399	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

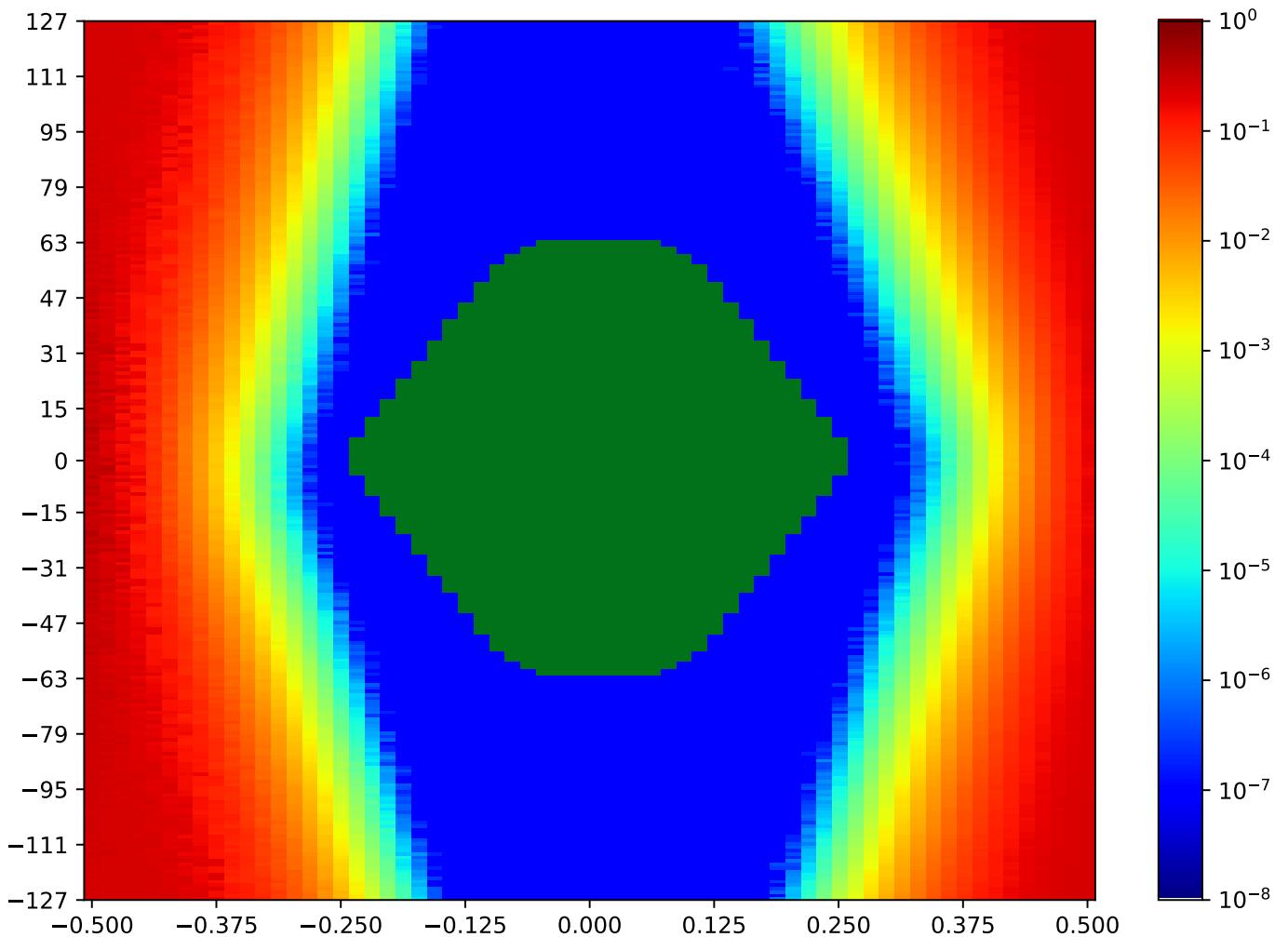


Figure 3.156: MSP_C_FPGA-TX3-02-RX9-02-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.4 MSP_C_FPGA-TX3-03-RX9-03-MSP_A_FPGA

Table 3.145: MSP_C_FPGA-TX3-03-RX9-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:35:56		2018-Jan-24 00:36:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7275	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

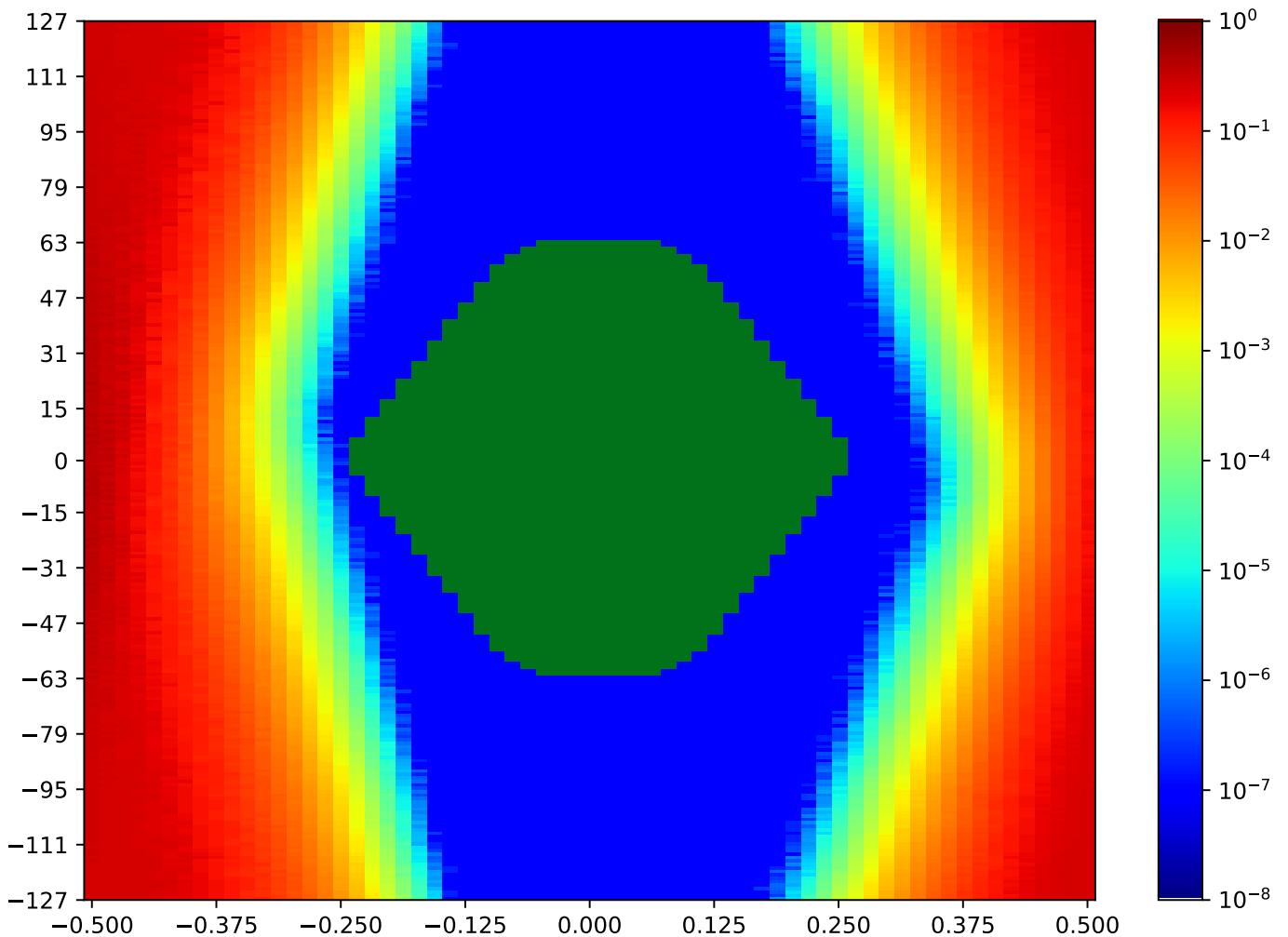


Figure 3.157: MSP_C_FPGA-TX3-03-RX9-03-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.5 MSP_C_FPGA-TX3-04-RX9-04-MSP_A_FPGA

Table 3.146: MSP_C_FPGA-TX3-04-RX9-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:38:47		2018-Jan-24 00:39:08	
Reset RX	OA	HO		HO (%)	
true	7015	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

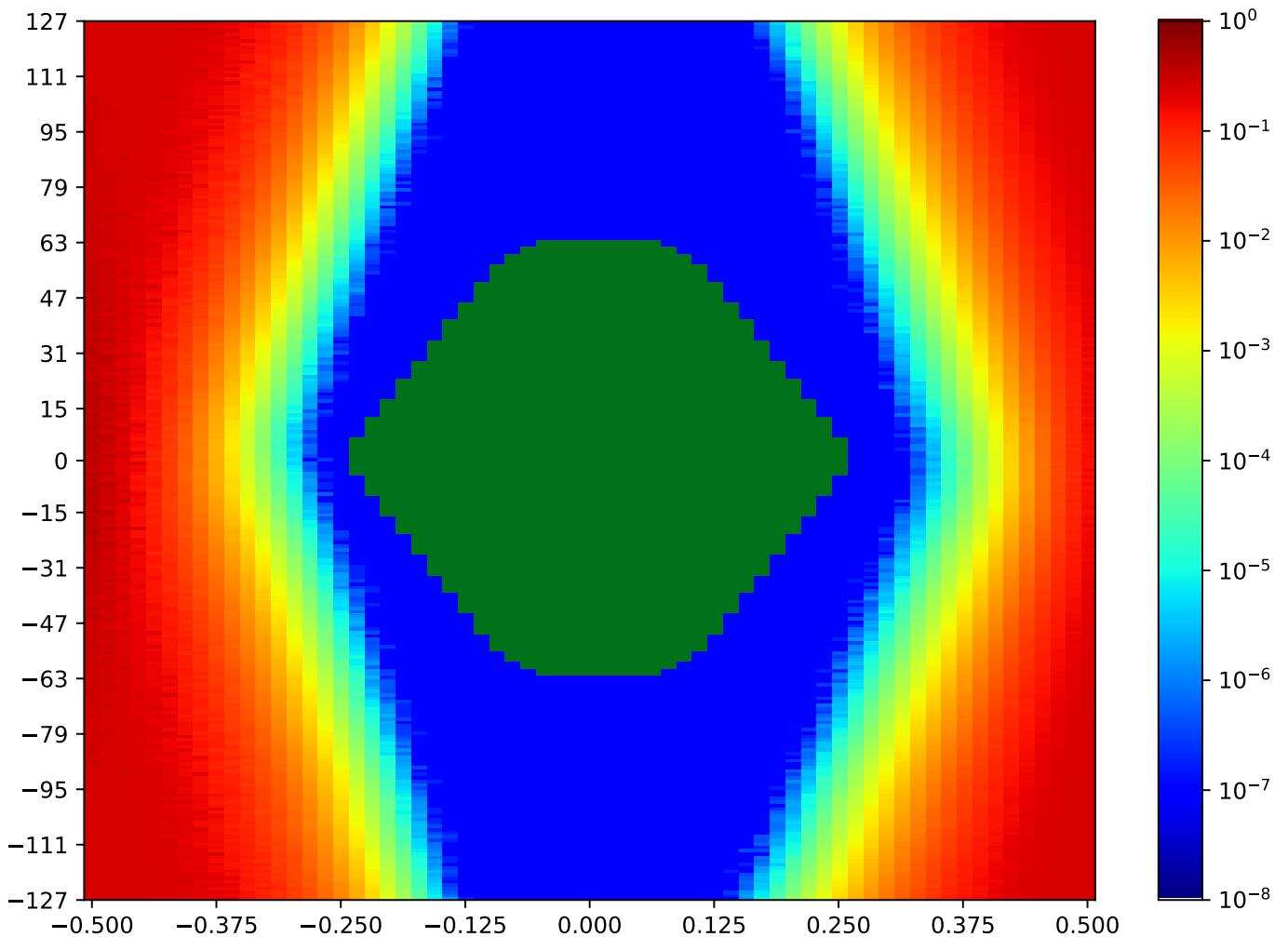


Figure 3.158: MSP_C_FPGA-TX3-04-RX9-04-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.6 MSP_C_FPGA-TX3-05-RX9-05-MSP_A_FPGA

Table 3.147: MSP_C_FPGA-TX3-05-RX9-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:35:35		2018-Jan-24 00:35:56	
Reset RX	OA	HO		HO (%)	
true	6980	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

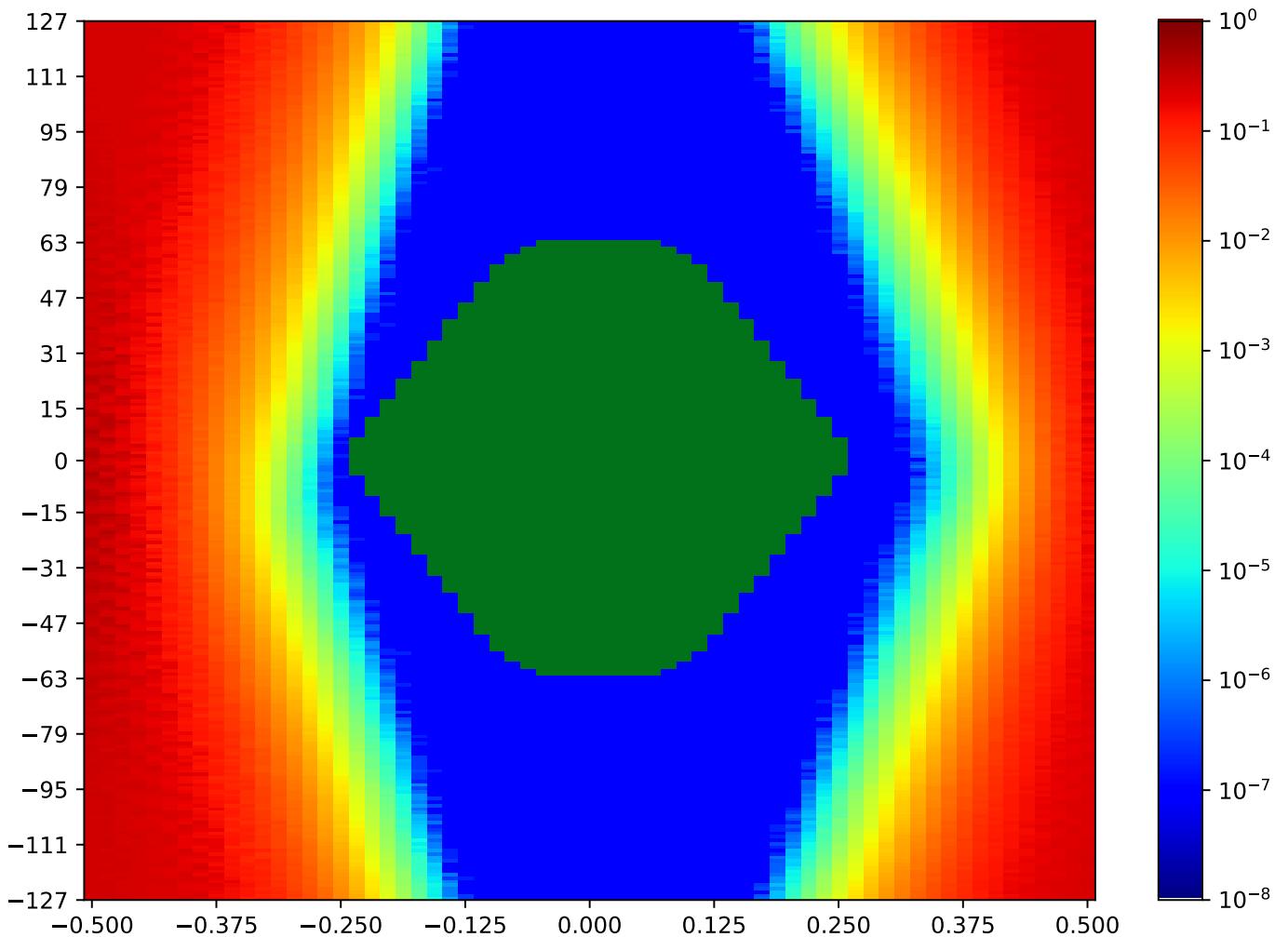


Figure 3.159: MSP_C_FPGA-TX3-05-RX9-05-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.7 MSP_C_FPGA-TX3-06-RX9-06-MSP_A_FPGA

Table 3.148: MSP_C_FPGA-TX3-06-RX9-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:39:30		2018-Jan-24 00:39:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7974	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

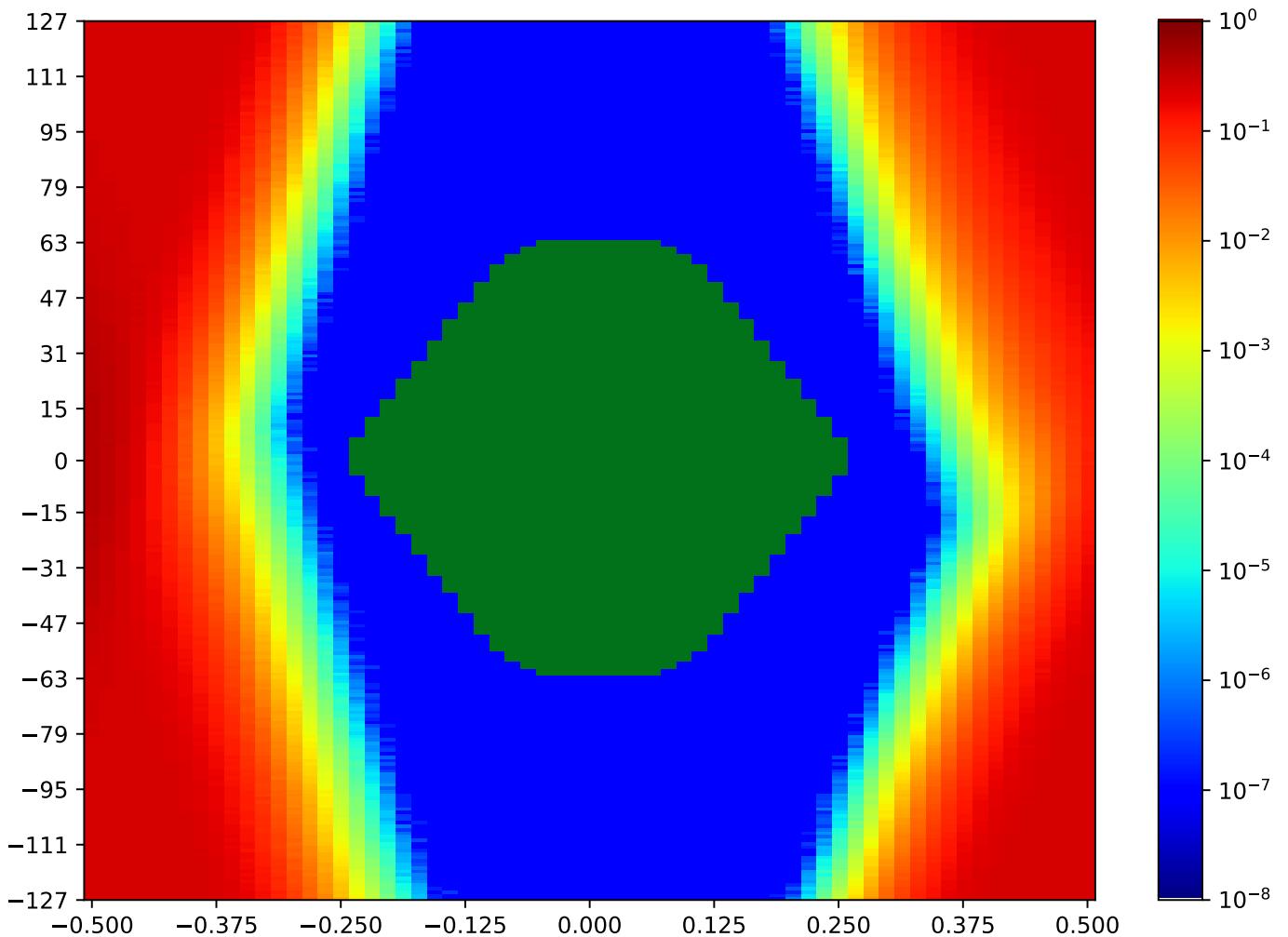


Figure 3.160: MSP_C_FPGA-TX3-06-RX9-06-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.8 MSP_C_FPGA-TX3-07-RX9-07-MSP_A_FPGA

Table 3.149: MSP_C_FPGA-TX3-07-RX9-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:36:18		2018-Jan-24 00:36:39	
Reset RX	OA	HO		HO (%)	
true	7712	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

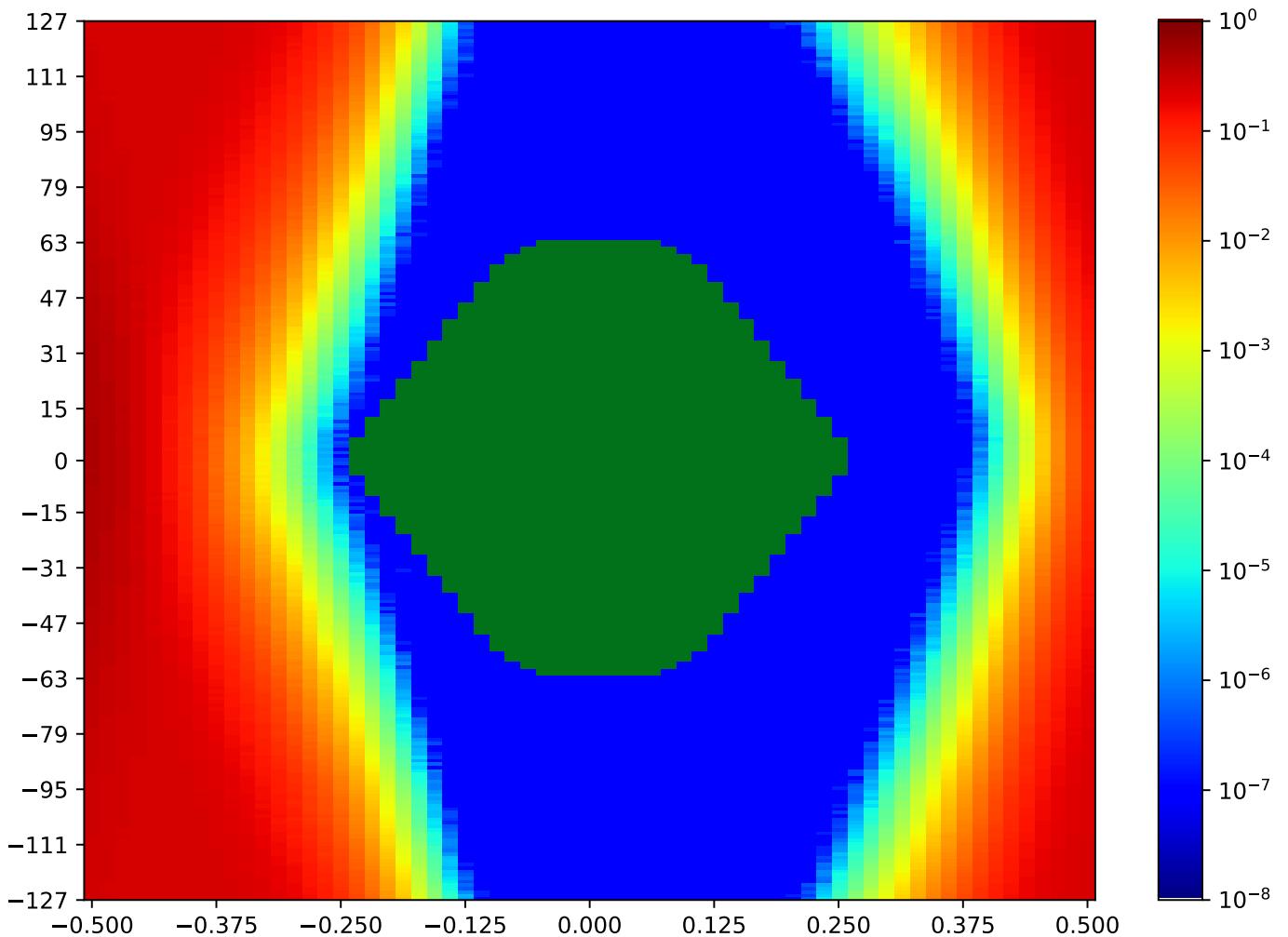


Figure 3.161: MSP_C_FPGA-TX3-07-RX9-07-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.9 MSP_C_FPGA-TX3-08-RX9-08-MSP_A_FPGA

Table 3.150: MSP_C_FPGA-TX3-08-RX9-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:39:09		2018-Jan-24 00:39:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8819	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

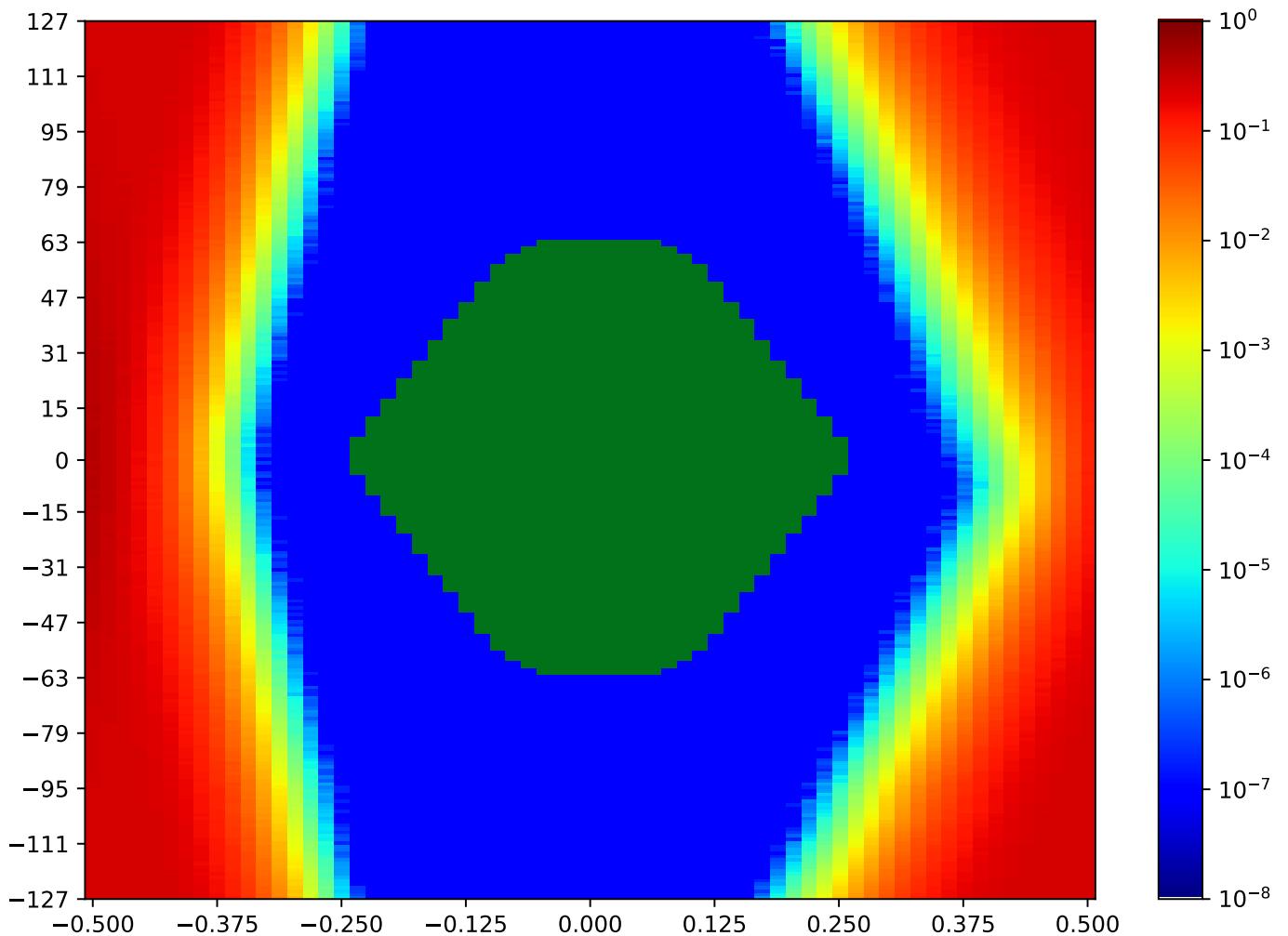


Figure 3.162: MSP_C_FPGA-TX3-08-RX9-08-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.10 MSP_C_FPGA-TX3-09-RX9-09-MSP_A_FPGA

Table 3.151: MSP_C_FPGA-TX3-09-RX9-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:37:01		2018-Jan-24 00:37:22	
Reset RX	OA	HO		HO (%)	
true	8423	45		69.23%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

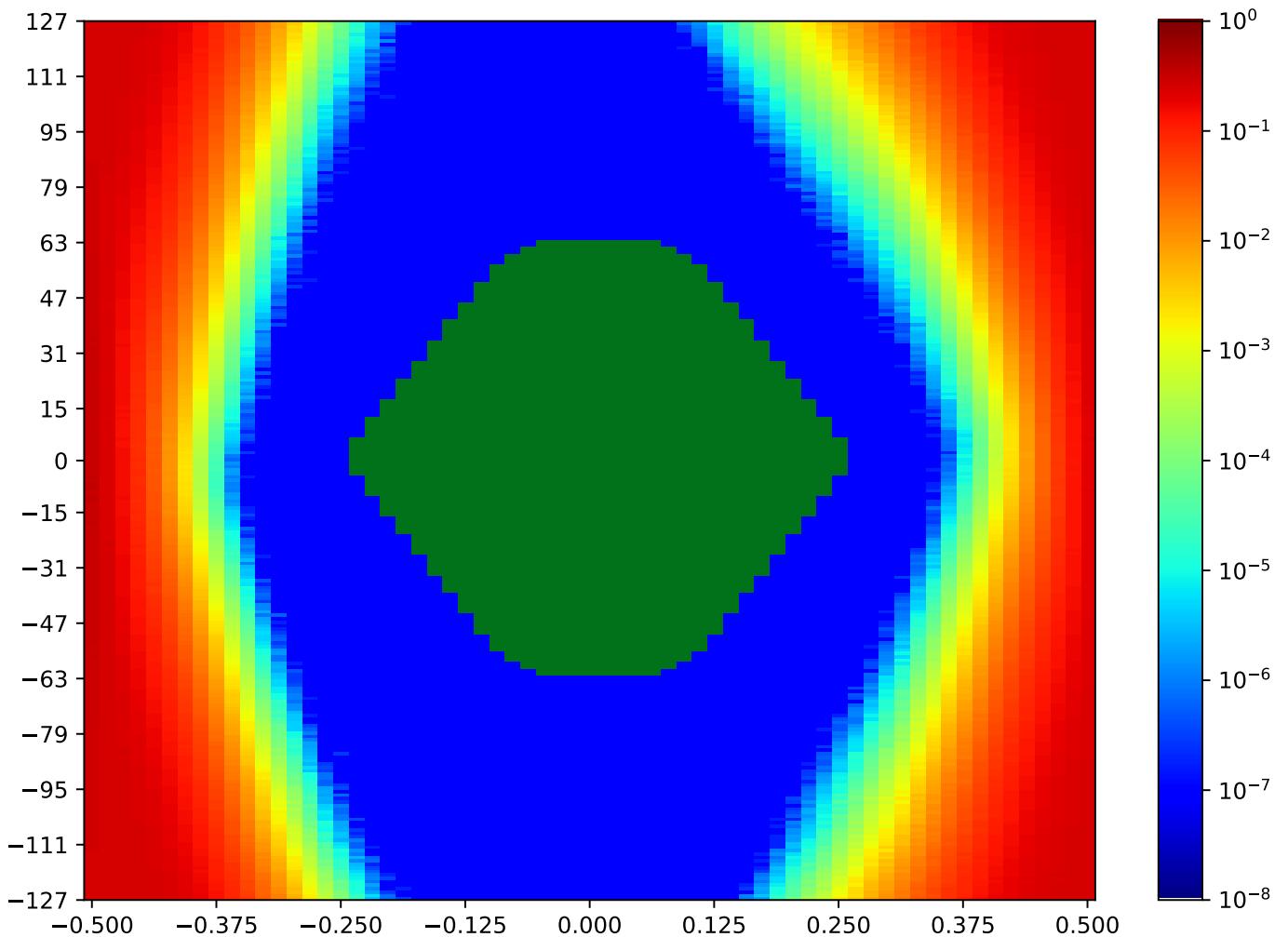


Figure 3.163: MSP_C_FPGA-TX3-09-RX9-09-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.11 MSP_C_FPGA-TX3-10-RX9-10-MSP_A_FPGA

Table 3.152: MSP_C_FPGA-TX3-10-RX9-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:38:26		2018-Jan-24 00:38:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7521	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

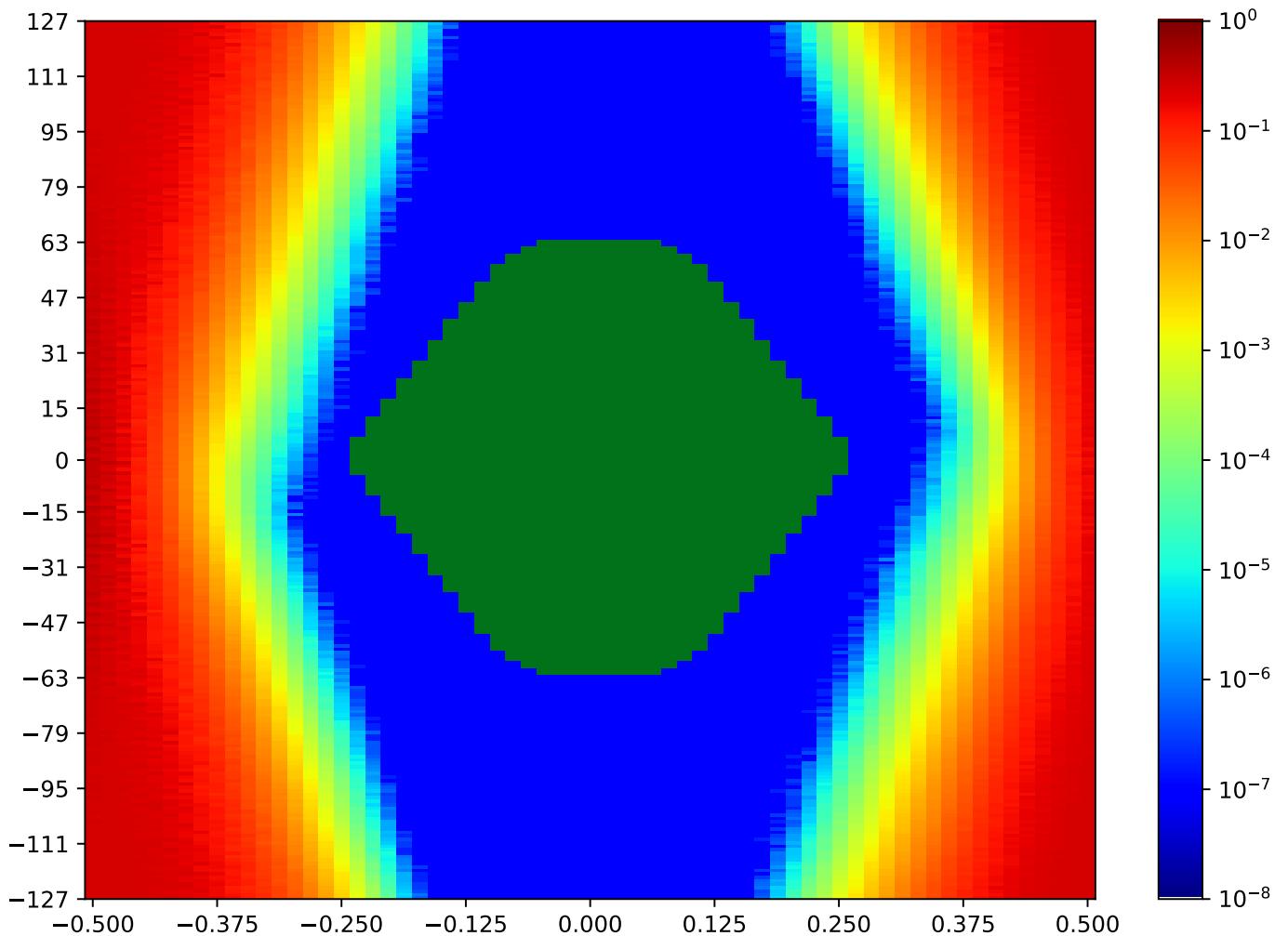


Figure 3.164: MSP_C_FPGA-TX3-10-RX9-10-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.12.12 MSP_C_FPGA-TX3-11-RX9-11-MSP_A_FPGA

Table 3.153: MSP_C_FPGA-TX3-11-RX9-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:38:05		2018-Jan-24 00:38:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8226	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

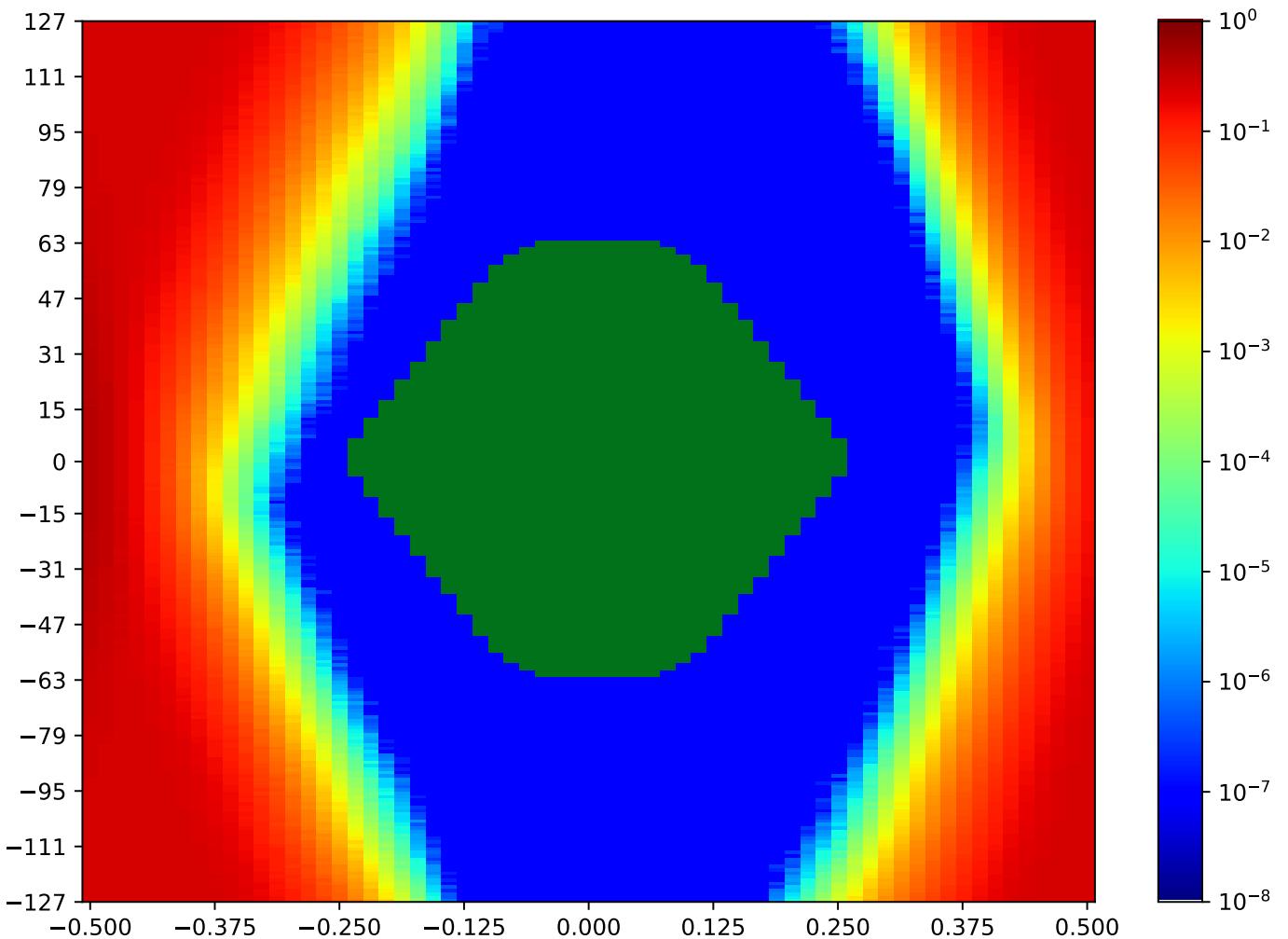


Figure 3.165: MSP_C_FPGA-TX3-11-RX9-11-MSP_A_FPGA

Call back to summary Figure 3.153. Sibling eye diagrams: V1-6.4.

3.13 MSP_C TX4 MSP_A RX8 Minipod Loopback

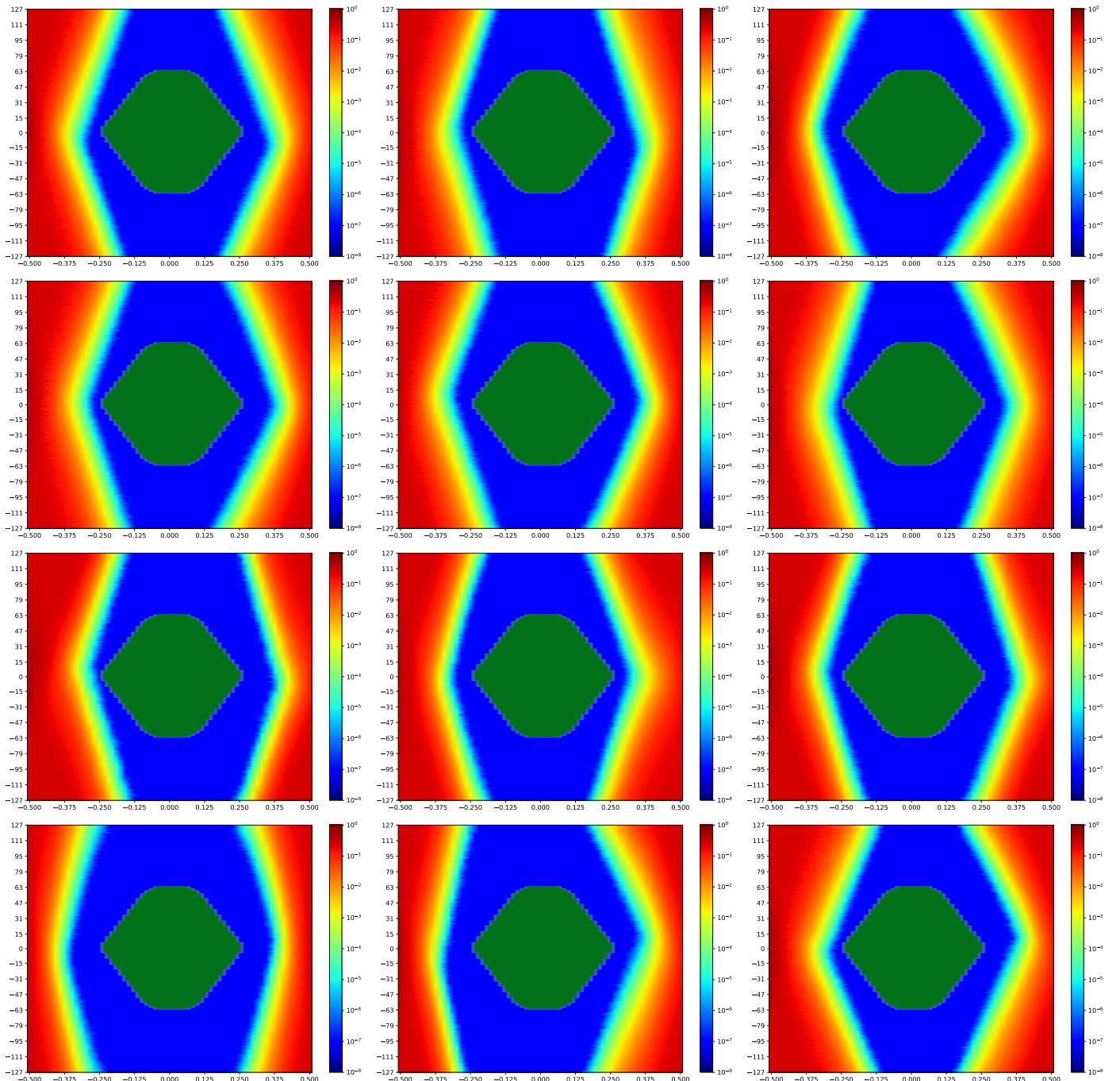


Figure 3.166: MSP_C TX4 MSP_A RX8 Minipod Loopback

A cross-reference to Figure 3.166. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.179.

3.13.1 MSP_C_FPGA-TX4-00-RX8-00-MSP_A_FPGA

Table 3.154: MSP_C_FPGA-TX4-00-RX8-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:40:55		2018-Jan-24 00:41:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7377	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

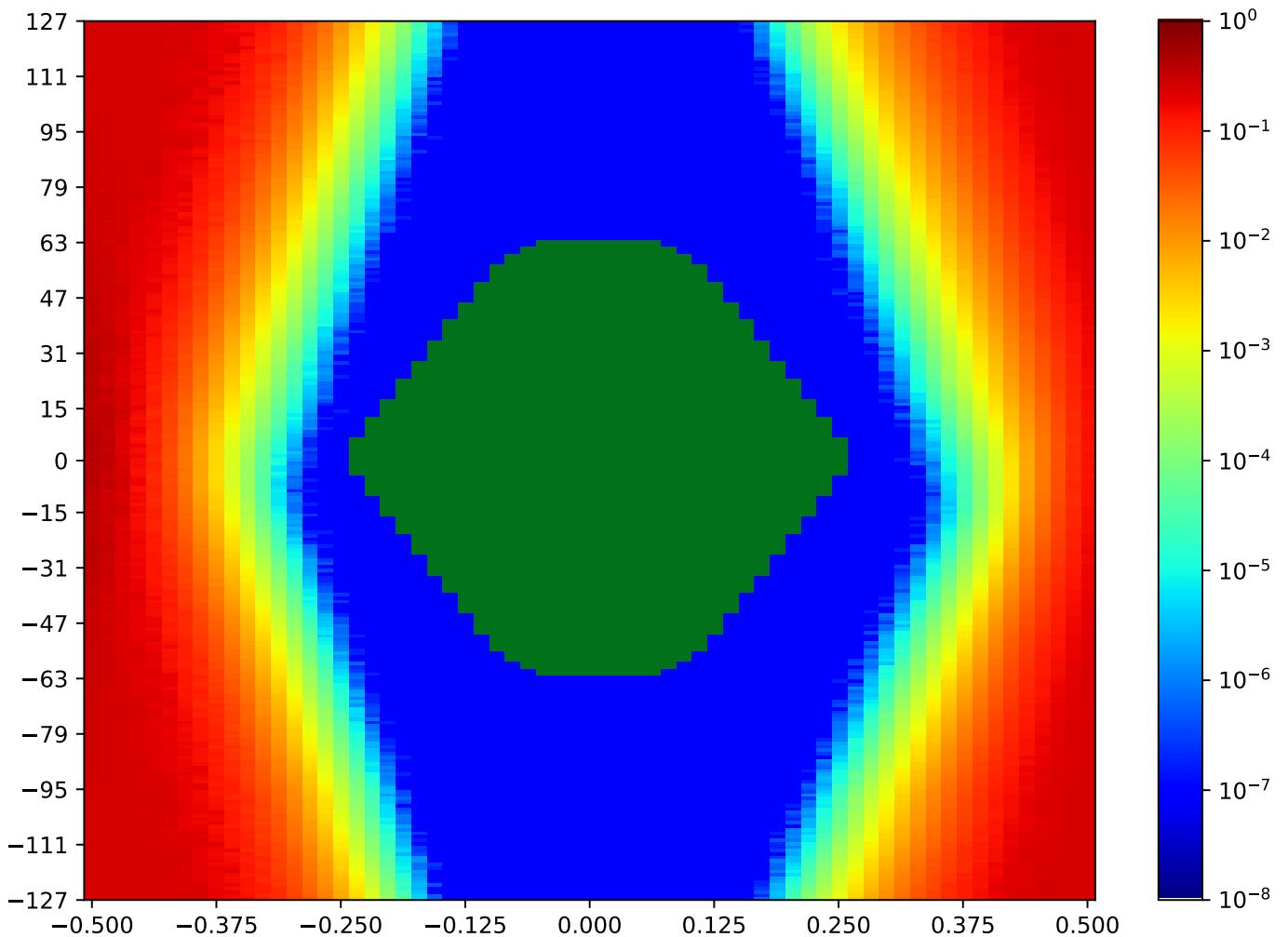


Figure 3.167: MSP_C_FPGA-TX4-00-RX8-00-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.2 MSP_C_FPGA-TX4-01-RX8-01-MSP_A_FPGA

Table 3.155: MSP_C_FPGA-TX4-01-RX8-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:40:13		2018-Jan-24 00:40:34	
Reset RX	OA	HO		HO (%)	
true	7590	37		56.92%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

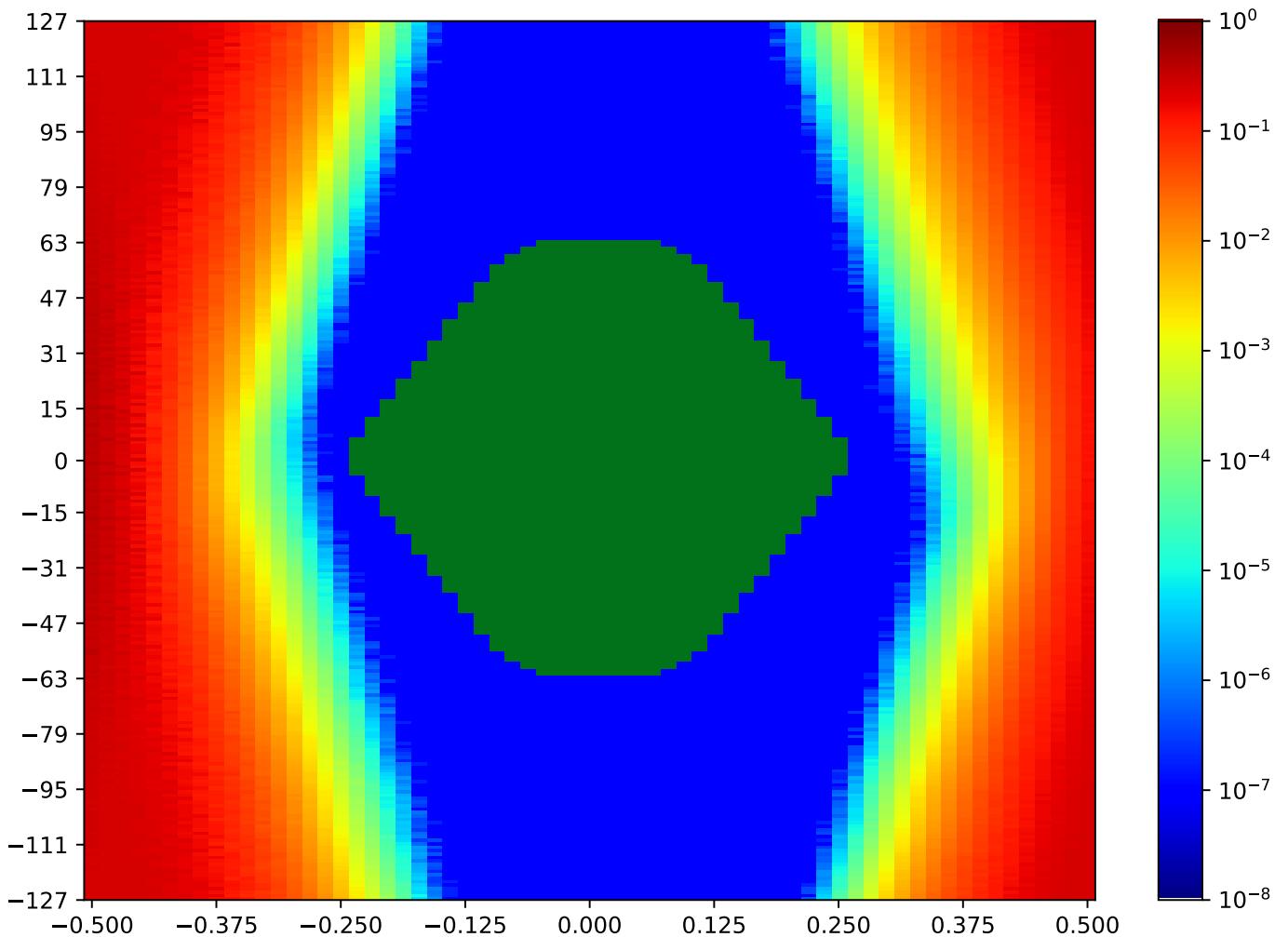


Figure 3.168: MSP_C_FPGA-TX4-01-RX8-01-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.3 MSP_C_FPGA-TX4-02-RX8-02-MSP_A_FPGA

Table 3.156: MSP_C_FPGA-TX4-02-RX8-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:41:59		2018-Jan-24 00:42:20	
Reset RX	OA	HO		HO (%)	
true	7354	42		64.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

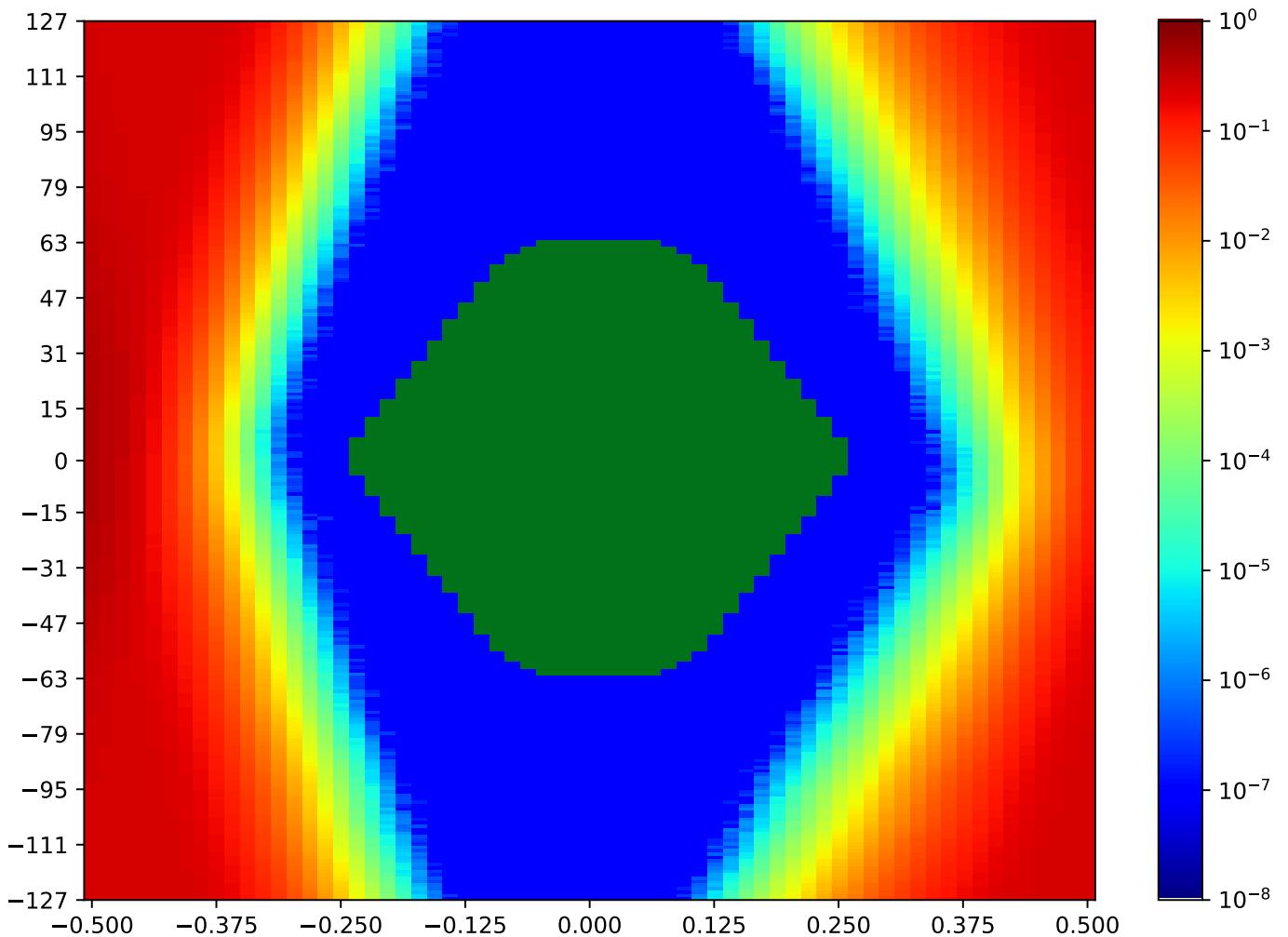


Figure 3.169: MSP_C_FPGA-TX4-02-RX8-02-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.4 MSP_C_FPGA-TX4-03-RX8-03-MSP_A_FPGA

Table 3.157: MSP_C_FPGA-TX4-03-RX8-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:39:52			2018-Jan-24 00:40:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7256	39	60.00%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

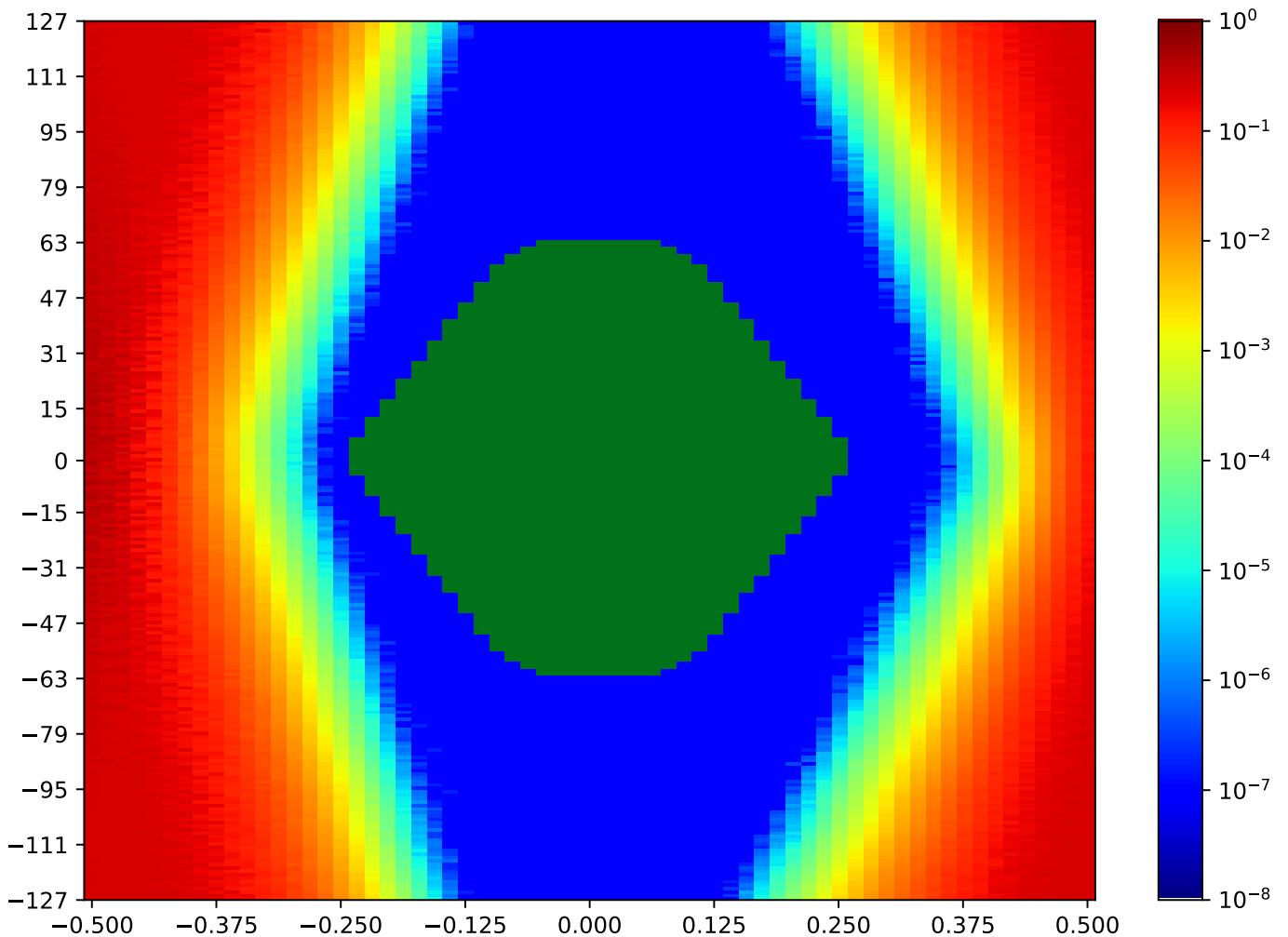


Figure 3.170: MSP_C_FPGA-TX4-03-RX8-03-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.5 MSP_C_FPGA-TX4-04-RX8-04-MSP_A_FPGA

Table 3.158: MSP_C_FPGA-TX4-04-RX8-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:43:03		2018-Jan-24 00:43:24	
Reset RX	OA	HO		HO (%)	
true	7584	39		60.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

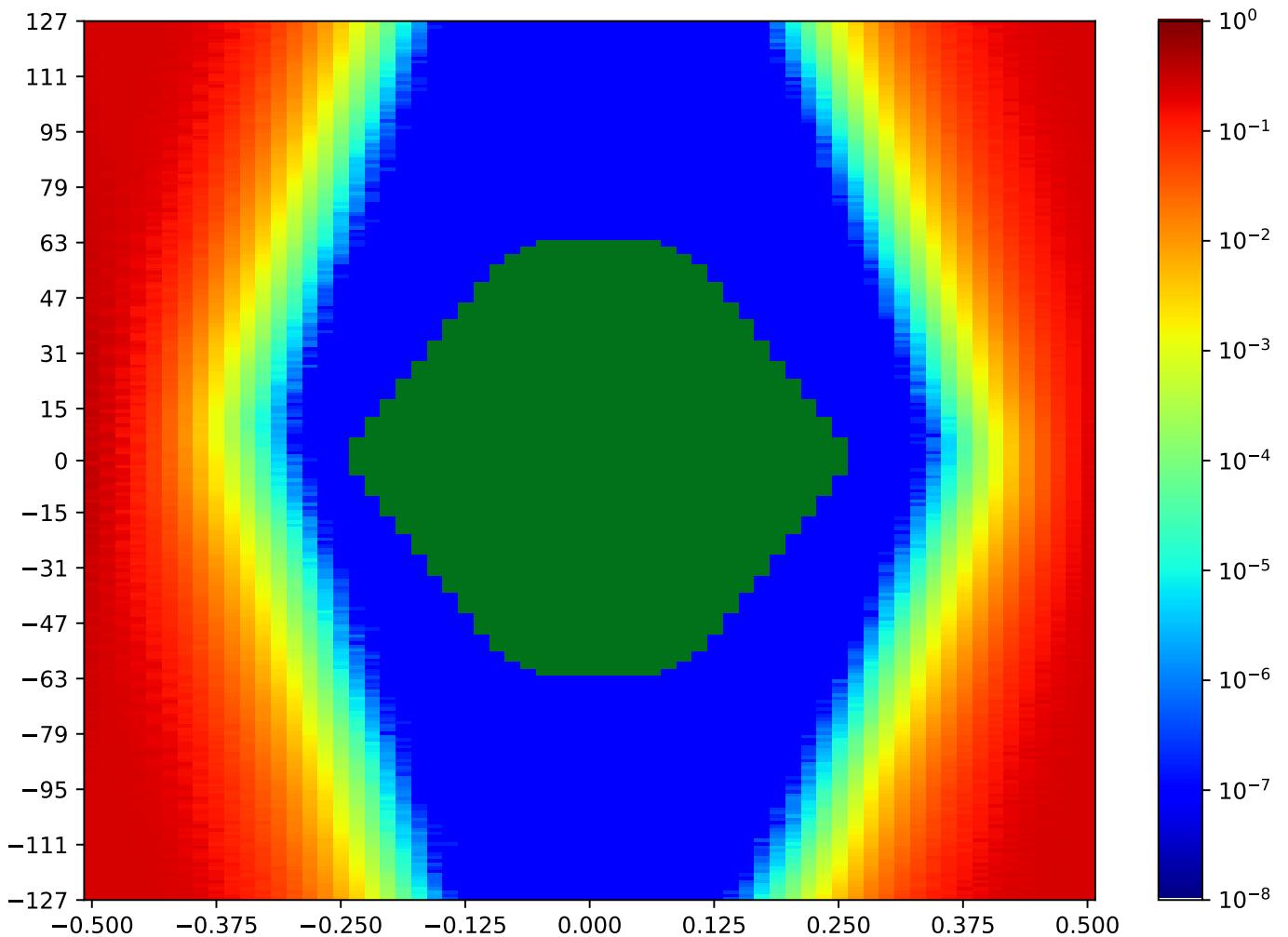


Figure 3.171: MSP_C_FPGA-TX4-04-RX8-04-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.6 MSP_C_FPGA-TX4-05-RX8-05-MSP_A_FPGA

Table 3.159: MSP_C_FPGA-TX4-05-RX8-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:40:34		2018-Jan-24 00:40:55	
Reset RX	OA	HO		HO (%)	
true	6895	36		55.38%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

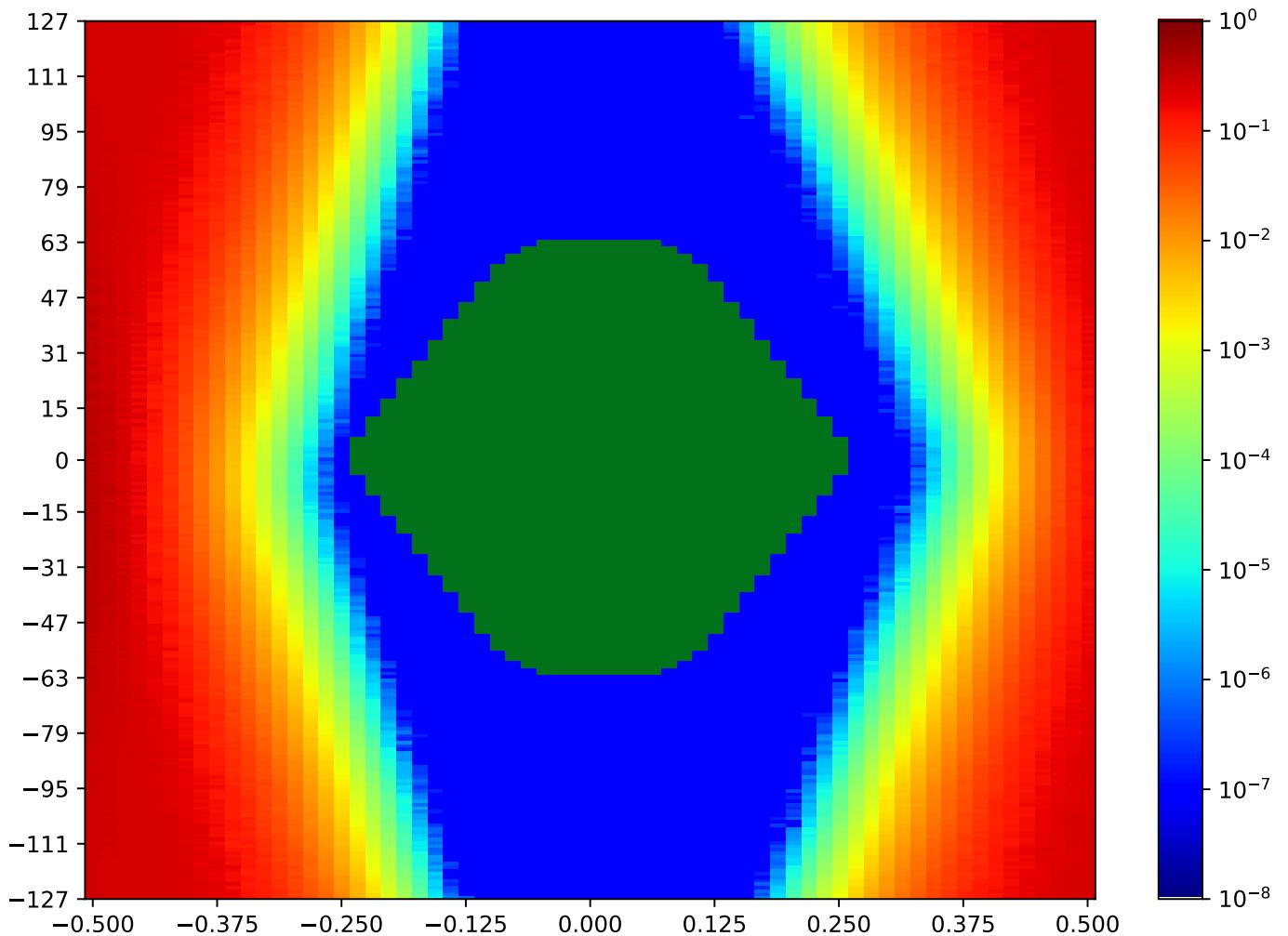


Figure 3.172: MSP_C_FPGA-TX4-05-RX8-05-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.7 MSP_C_FPGA-TX4-06-RX8-06-MSP_A_FPGA

Table 3.160: MSP_C_FPGA-TX4-06-RX8-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:43:46		2018-Jan-24 00:44:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7888	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

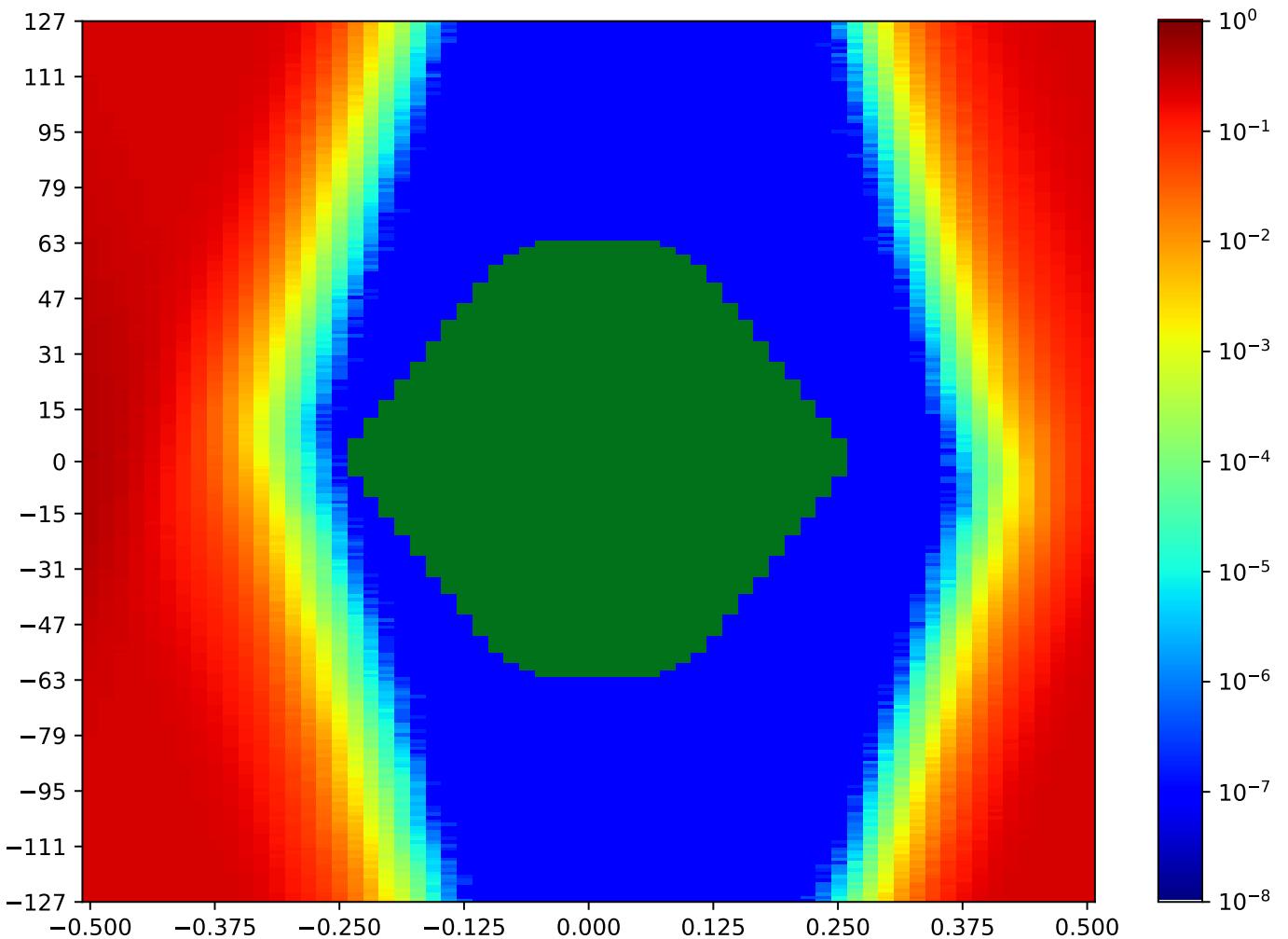


Figure 3.173: MSP_C_FPGA-TX4-06-RX8-06-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.8 MSP_C_FPGA-TX4-07-RX8-07-MSP_A_FPGA

Table 3.161: MSP_C_FPGA-TX4-07-RX8-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:41:17		2018-Jan-24 00:41:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7517	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

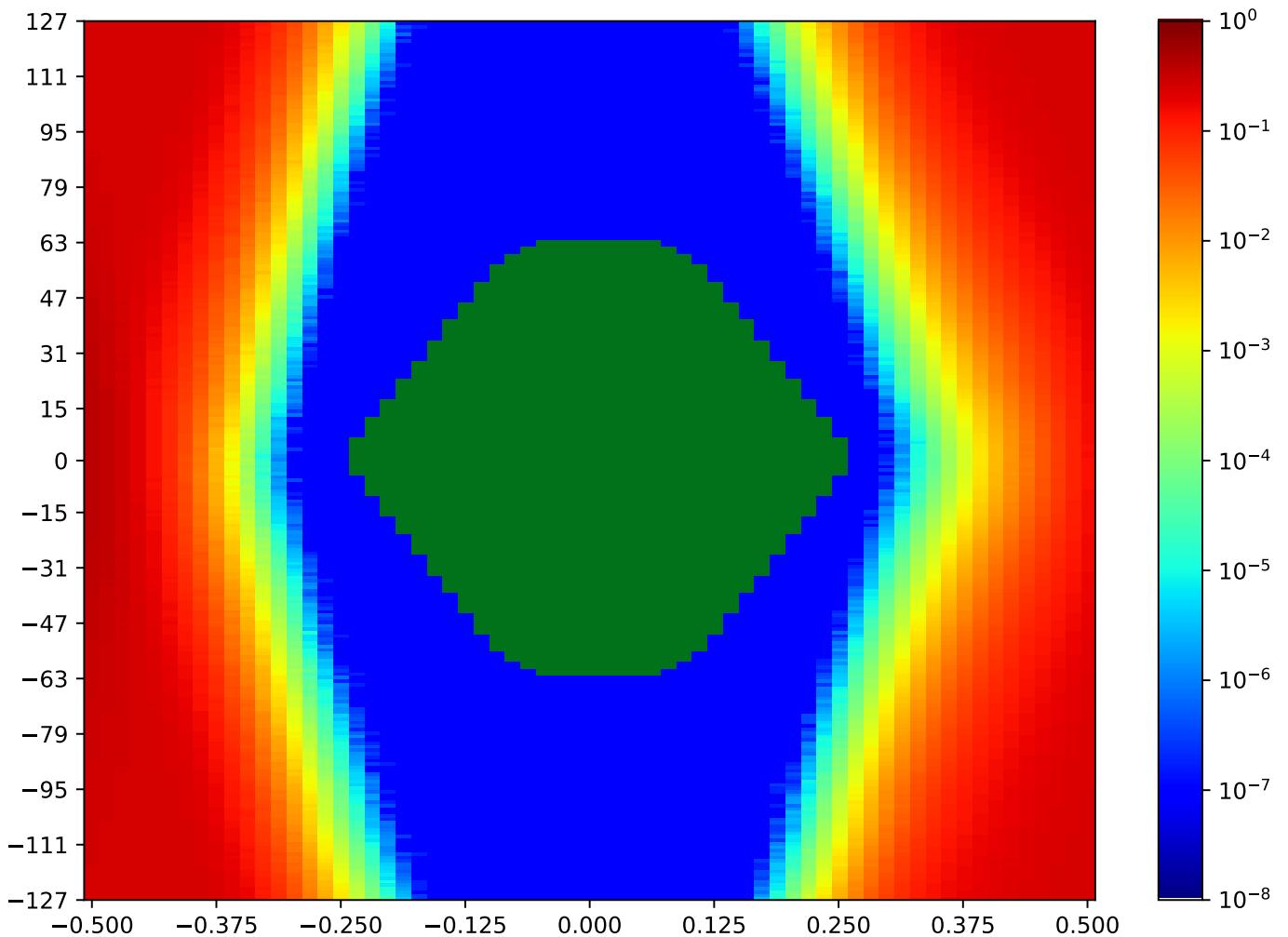


Figure 3.174: MSP_C_FPGA-TX4-07-RX8-07-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.9 MSP_C_FPGA-TX4-08-RX8-08-MSP_A_FPGA

Table 3.162: MSP_C_FPGA-TX4-08-RX8-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:43:24		2018-Jan-24 00:43:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7816	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

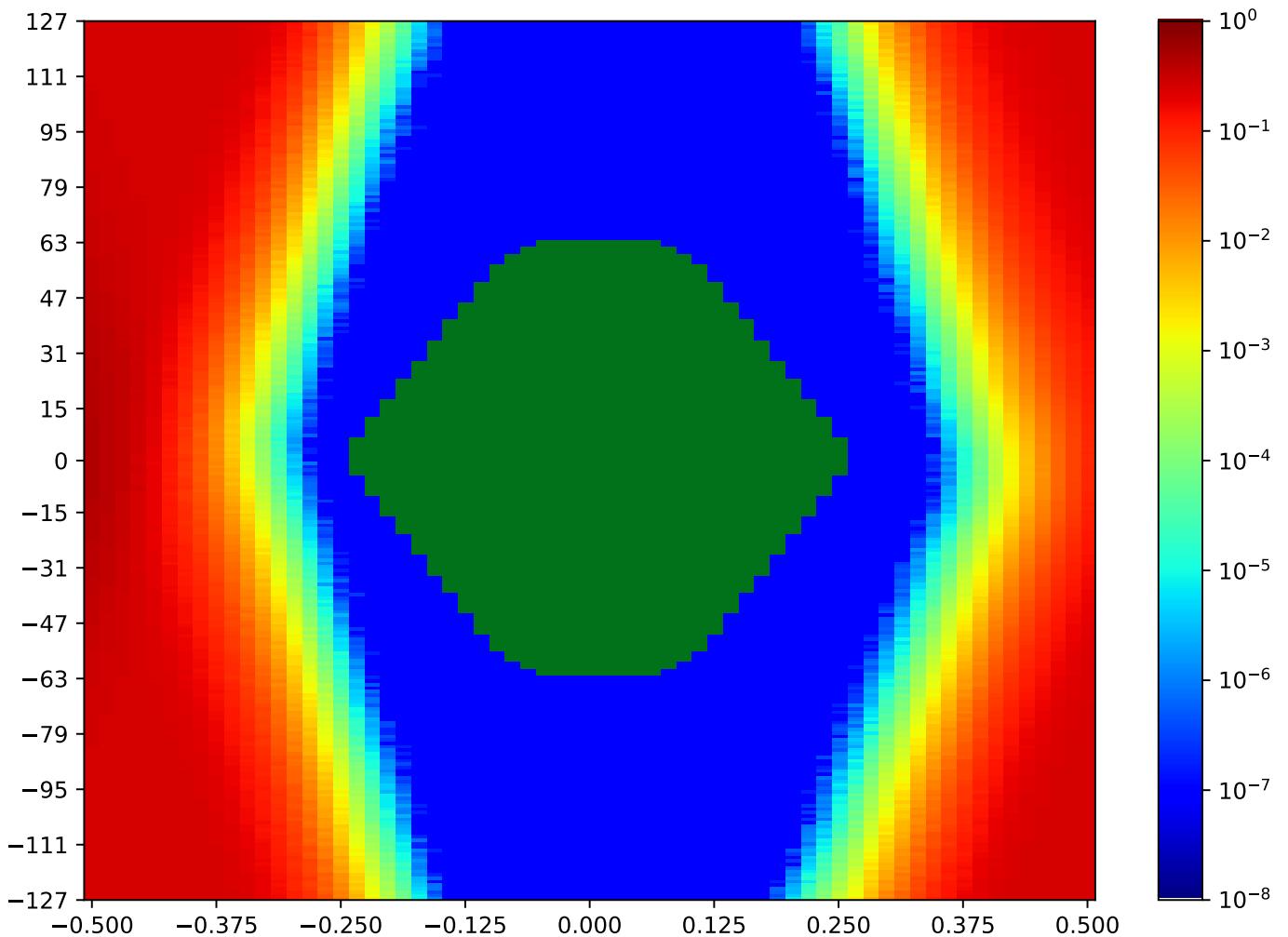


Figure 3.175: MSP_C_FPGA-TX4-08-RX8-08-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.10 MSP_C_FPGA-TX4-09-RX8-09-MSP_A_FPGA

Table 3.163: MSP_C_FPGA-TX4-09-RX8-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:41:38		2018-Jan-24 00:41:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9428	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

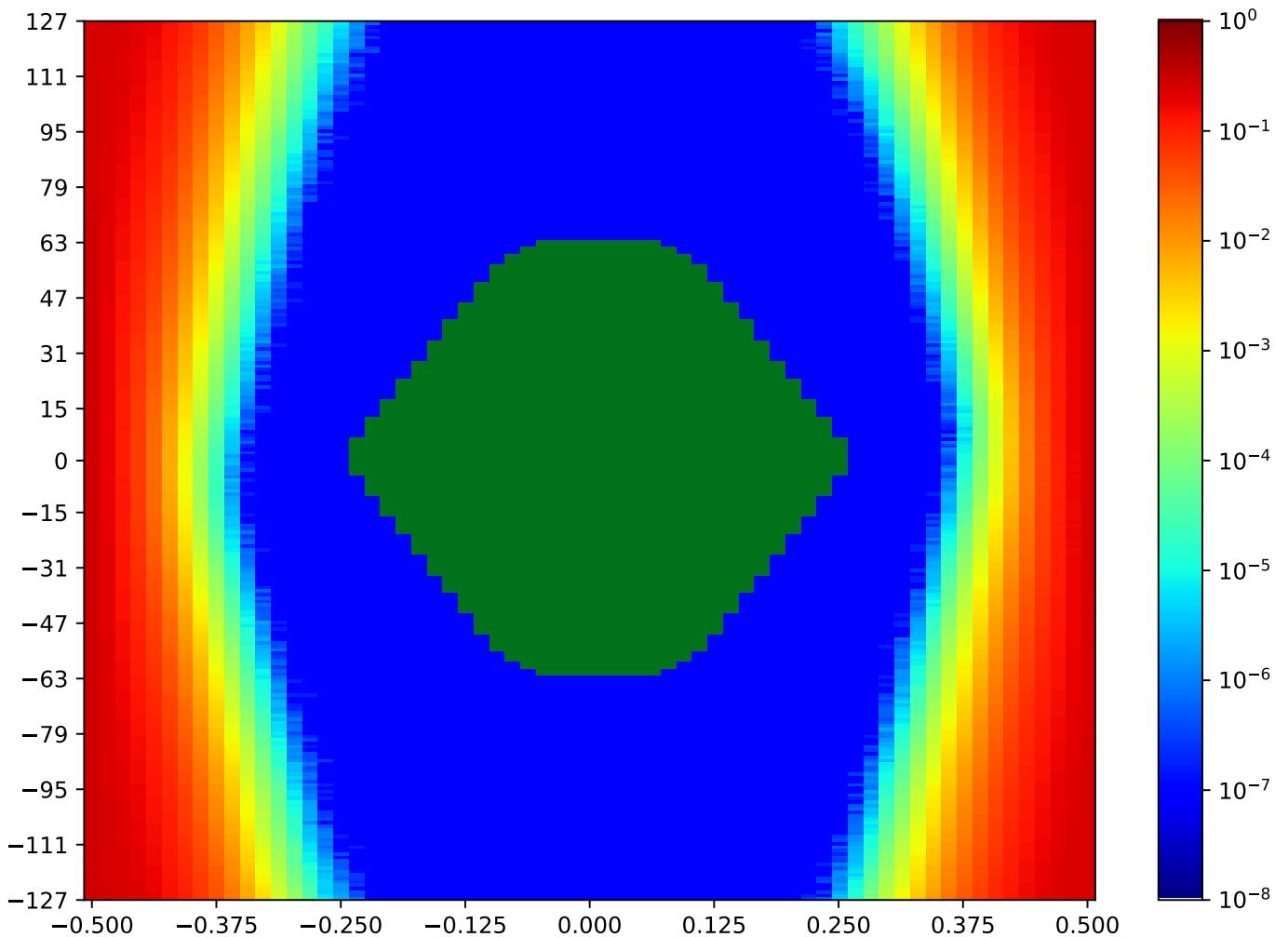


Figure 3.176: MSP_C_FPGA-TX4-09-RX8-09-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.11 MSP_C_FPGA-TX4-10-RX8-10-MSP_A_FPGA

Table 3.164: MSP_C_FPGA-TX4-10-RX8-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:42:42		2018-Jan-24 00:43:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8564	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

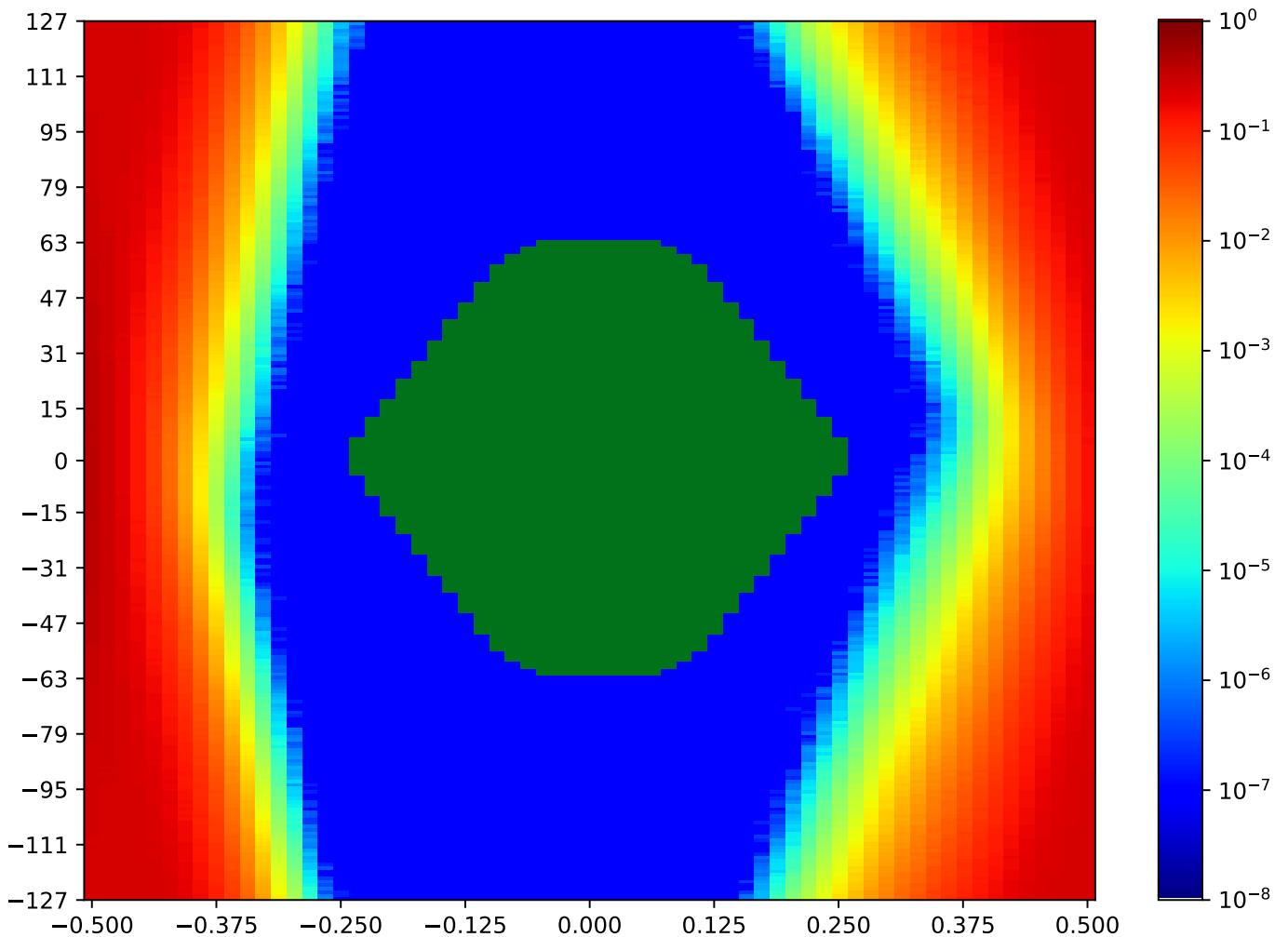


Figure 3.177: MSP_C_FPGA-TX4-10-RX8-10-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.13.12 MSP_C_FPGA-TX4-11-RX8-11-MSP_A_FPGA

Table 3.165: MSP_C_FPGA-TX4-11-RX8-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:42:21		2018-Jan-24 00:42:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7103	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

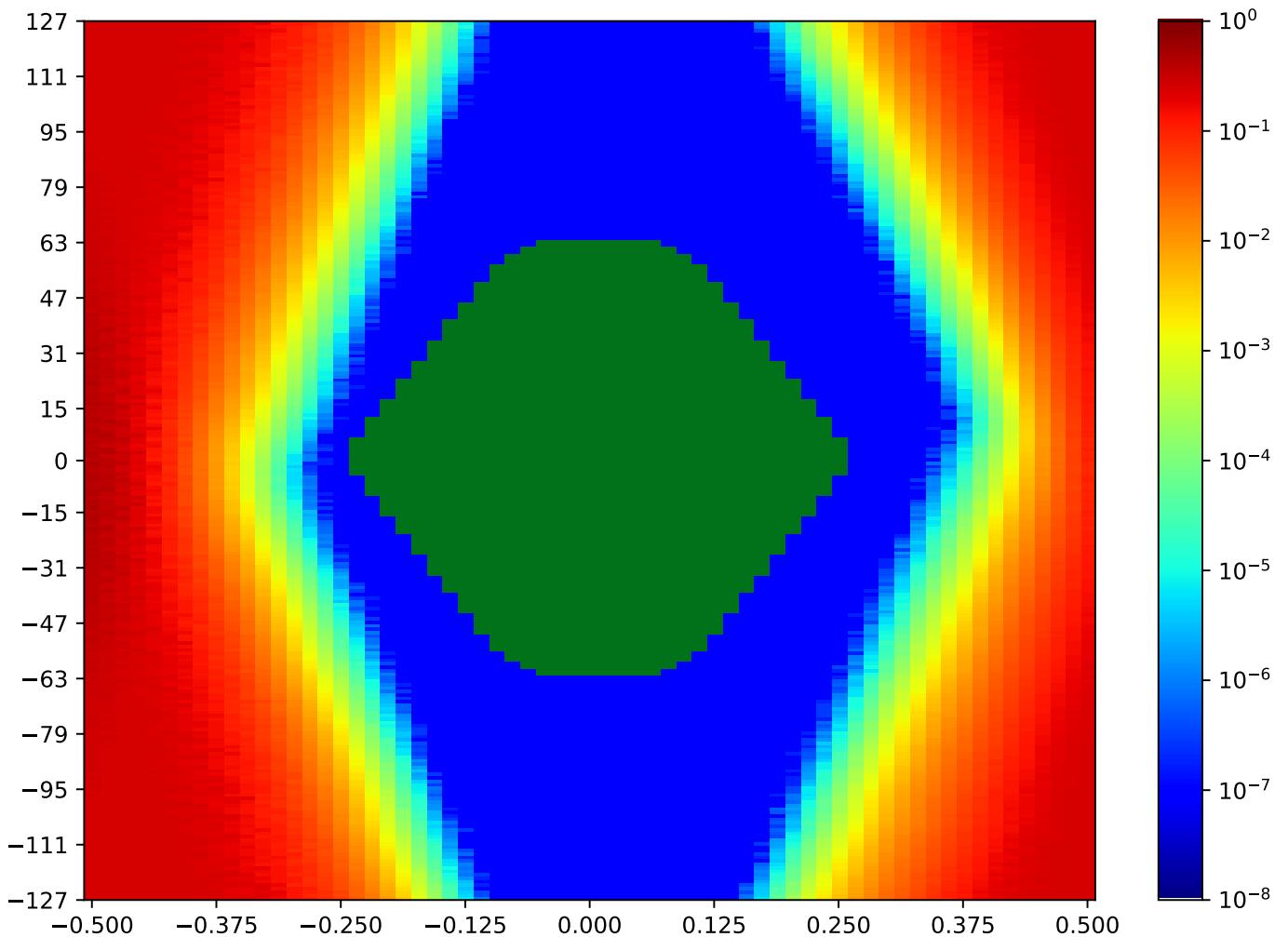


Figure 3.178: MSP_C_FPGA-TX4-11-RX8-11-MSP_A_FPGA

Call back to summary Figure 3.166. Sibling eye diagrams: V1-6.4.

3.14 Partial TRP TX5 MSP_C RX14 Minipod Loopback

A cross-reference to Figure 3.179. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.
Next summary Figure ??.

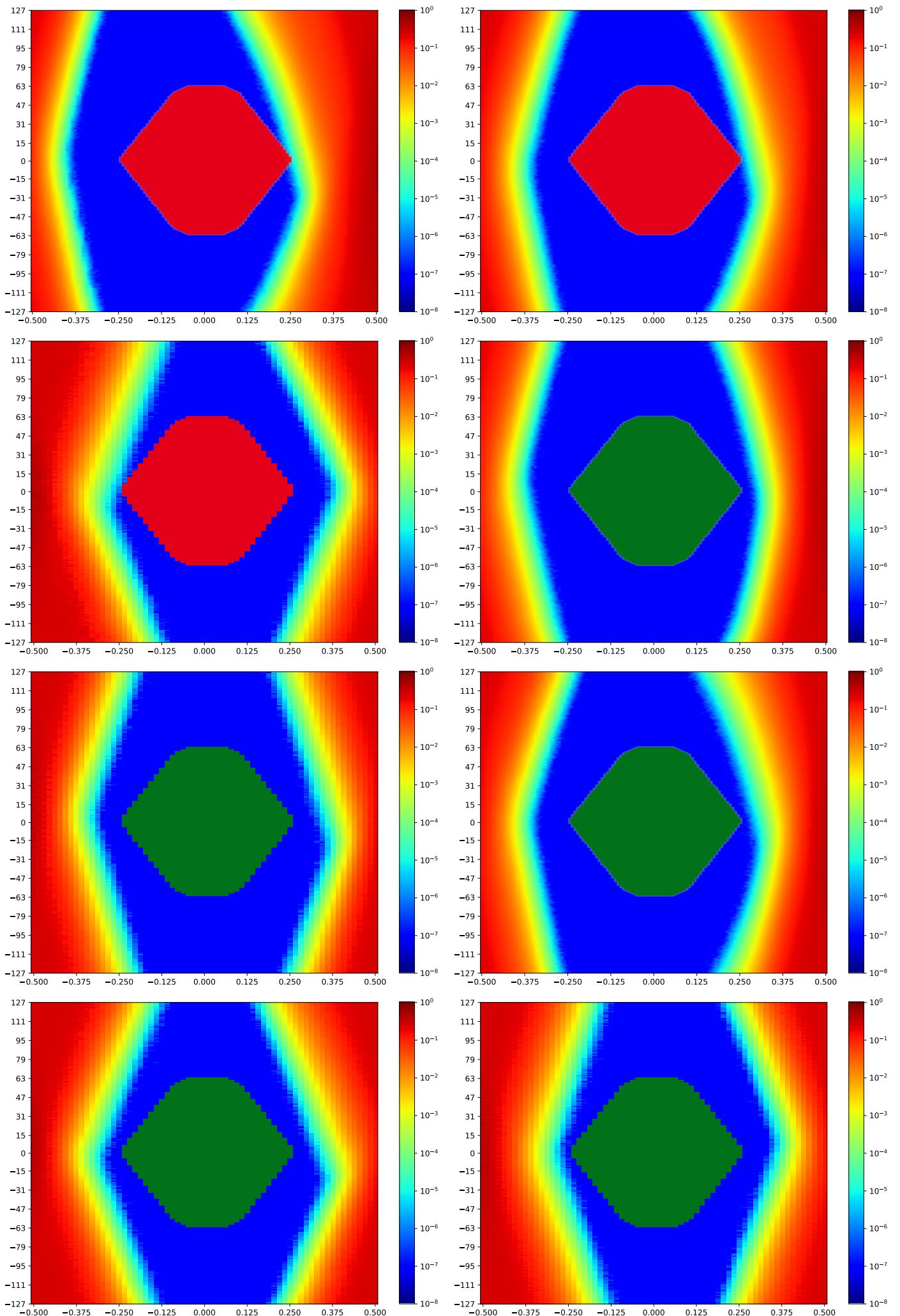


Figure 3.179: Partial TRP TX5 MSP_C RX14 Minipod Loopback
500

3.14.1 TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

Table 3.166: TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:46:15		2018-Jan-24 00:46:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16345	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

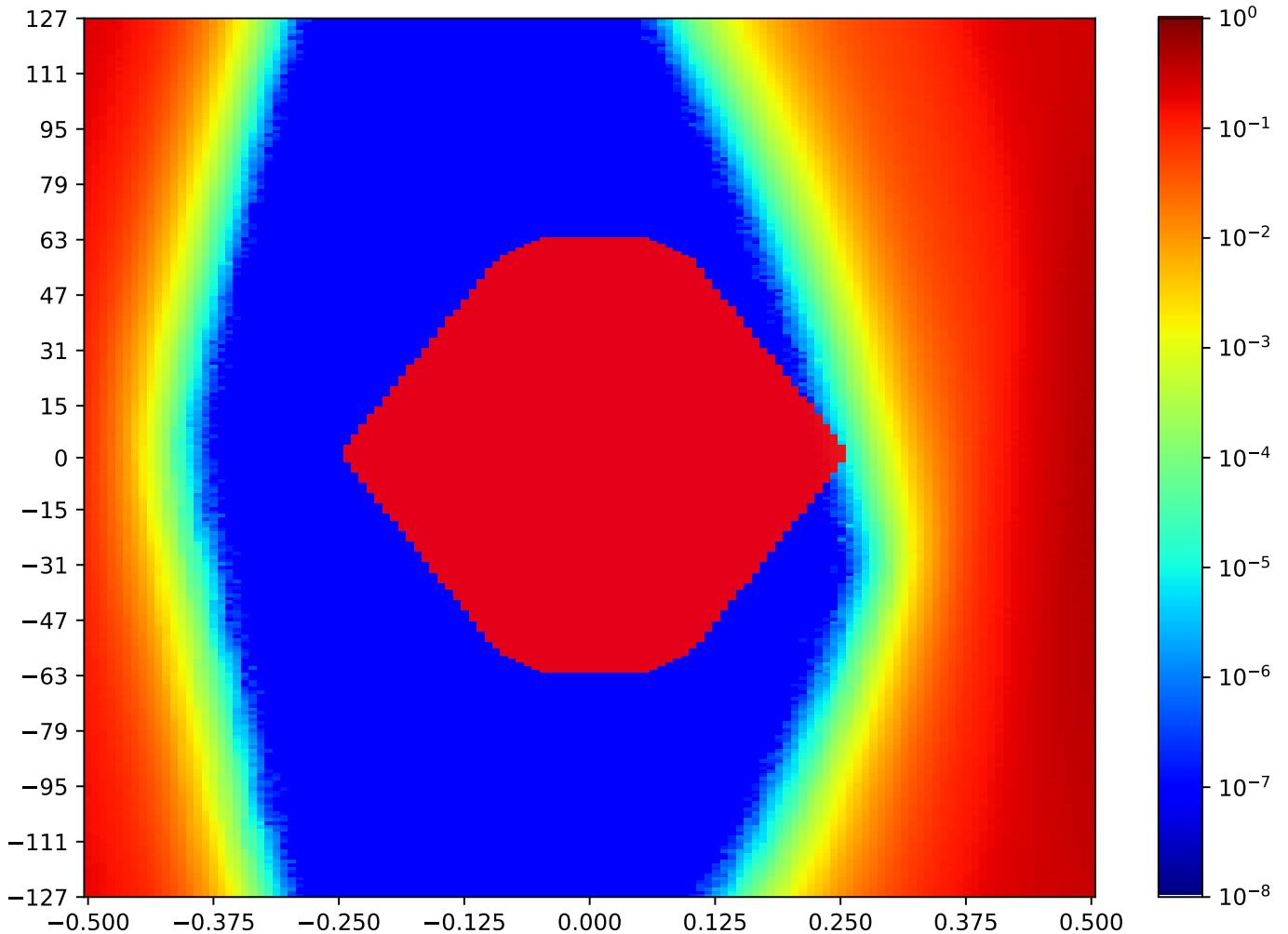


Figure 3.180: TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.14.2 TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

Table 3.167: TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:44:50		2018-Jan-24 00:45:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15685	73	56.59%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

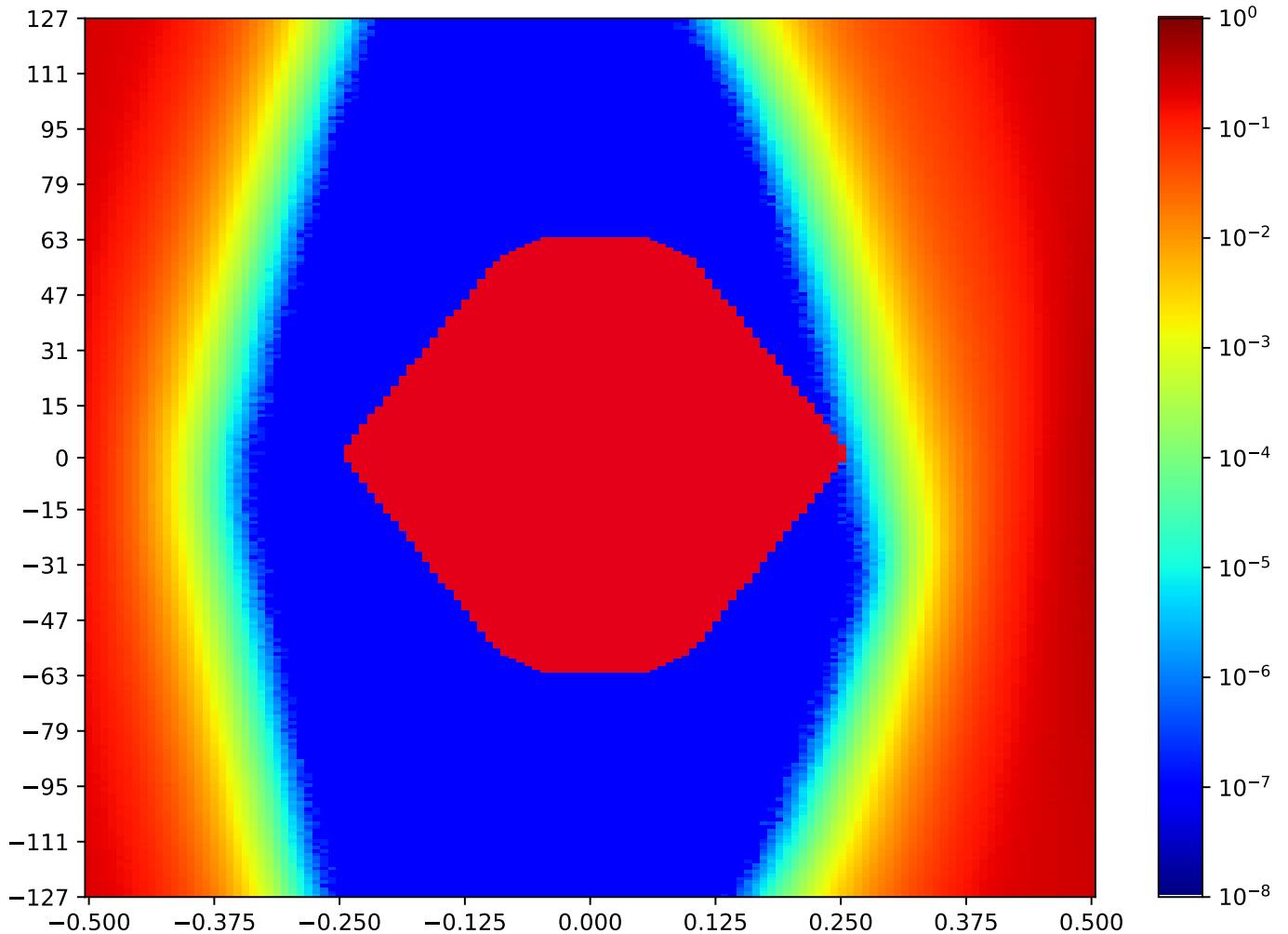


Figure 3.181: TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.14.3 TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

Table 3.168: TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:47:19		2018-Jan-24 00:47:40	
Reset RX	OA	HO		HO (%)	
true	6915	36		55.38%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

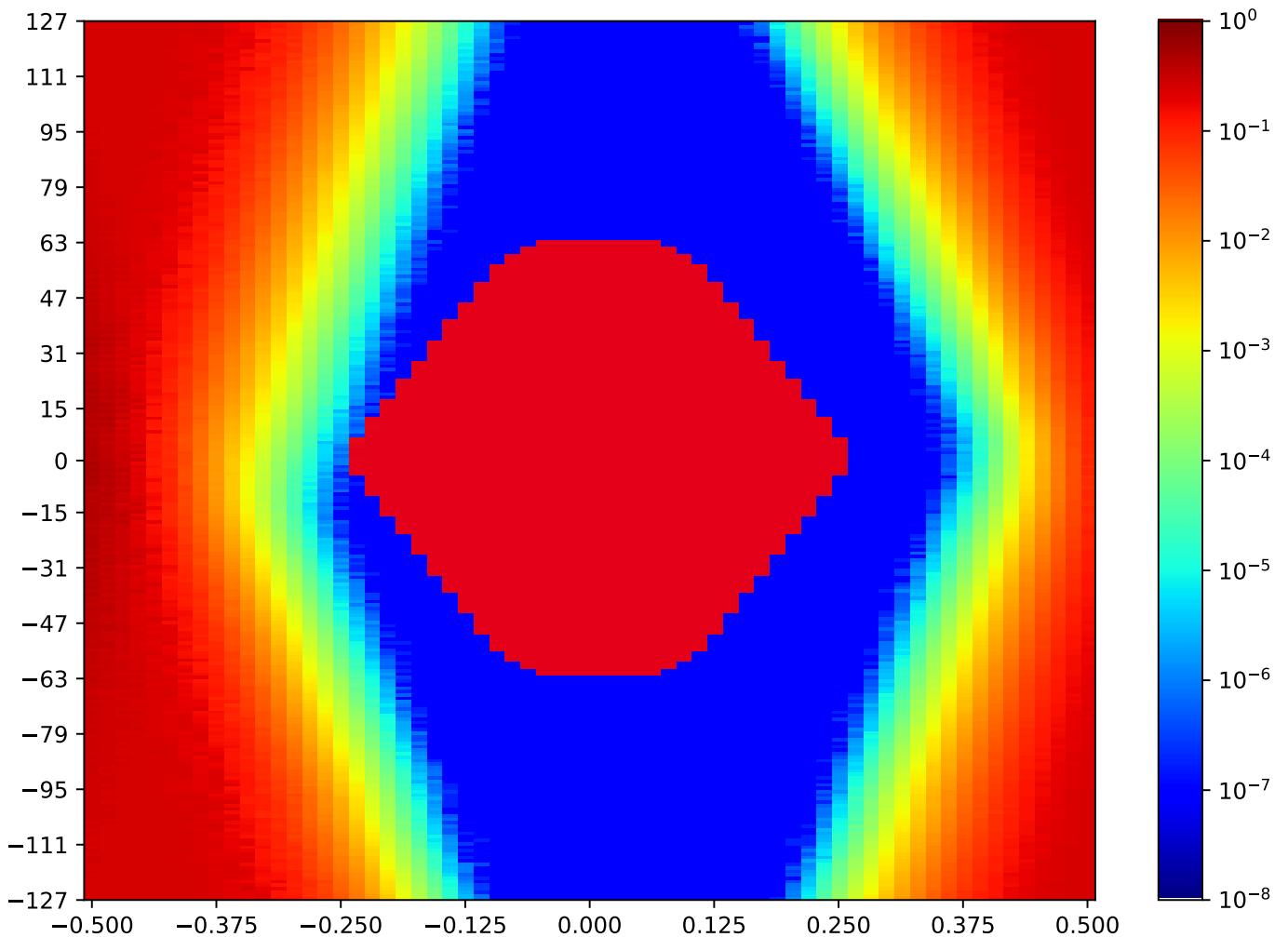


Figure 3.182: TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.14.4 TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

Table 3.169: TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:45:33		2018-Jan-24 00:46:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17179	79	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

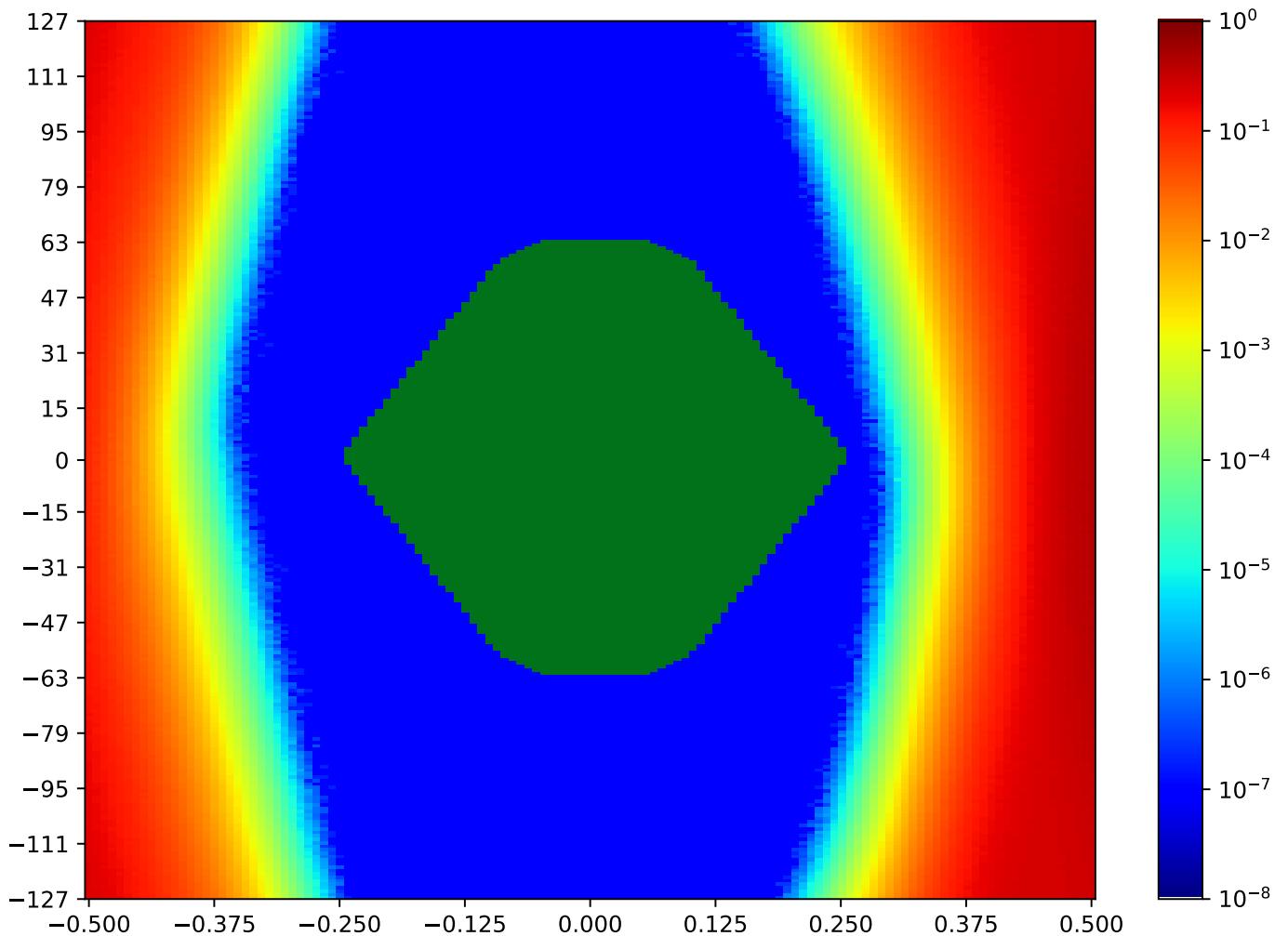


Figure 3.183: TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.14.5 TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

Table 3.170: TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:48:02		2018-Jan-24 00:48:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8057	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

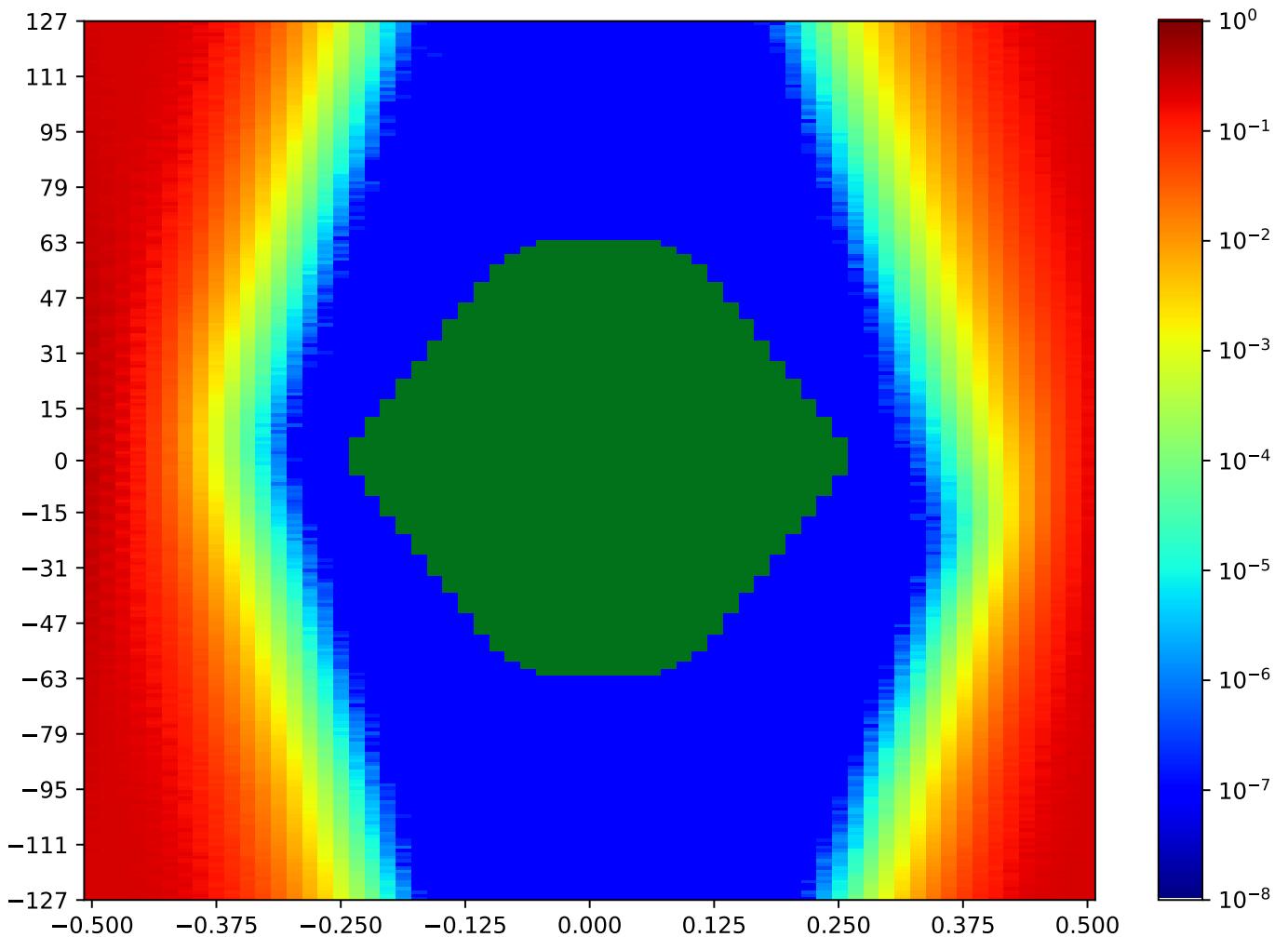


Figure 3.184: TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.14.6 TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

Table 3.171: TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:44:07		2018-Jan-24 00:44:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15909	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

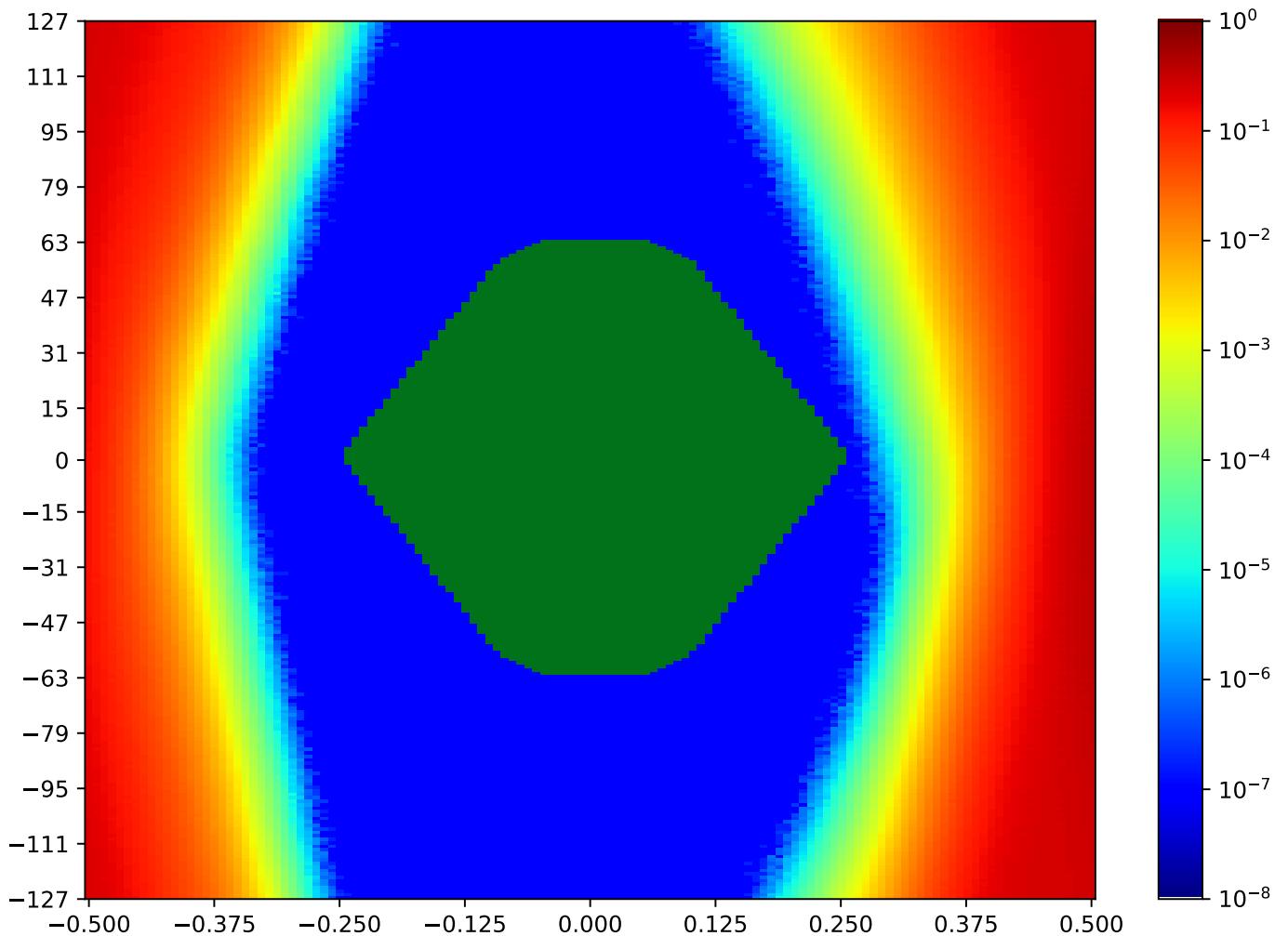


Figure 3.185: TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.14.7 TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

Table 3.172: TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:46:57		2018-Jan-24 00:47:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6982	37	56.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

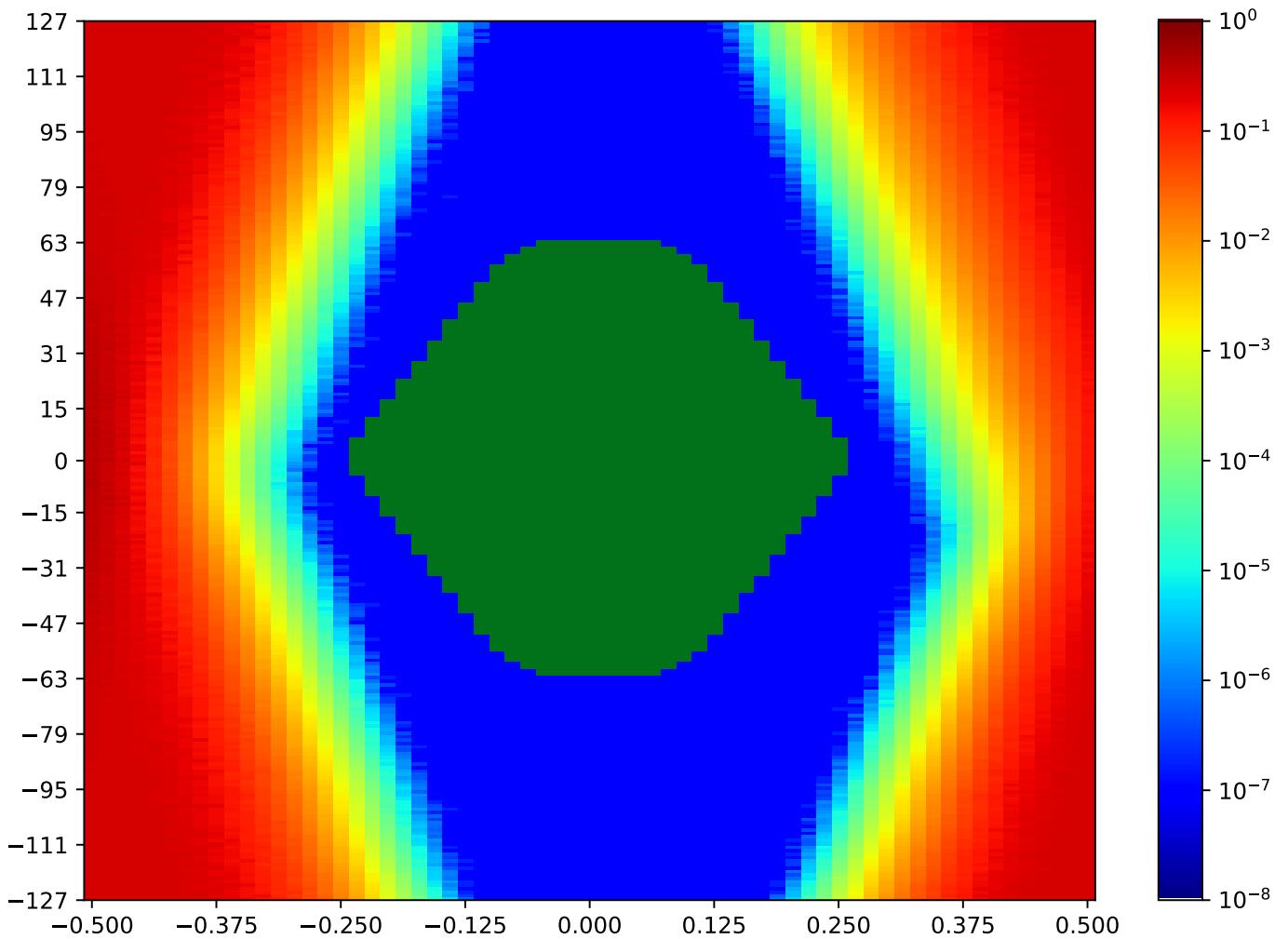


Figure 3.186: TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.14.8 TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

Table 3.173: TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTH	2018-Jan-24 00:47:40			2018-Jan-24 00:48:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	7070	37	56.92%	255	100.00%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

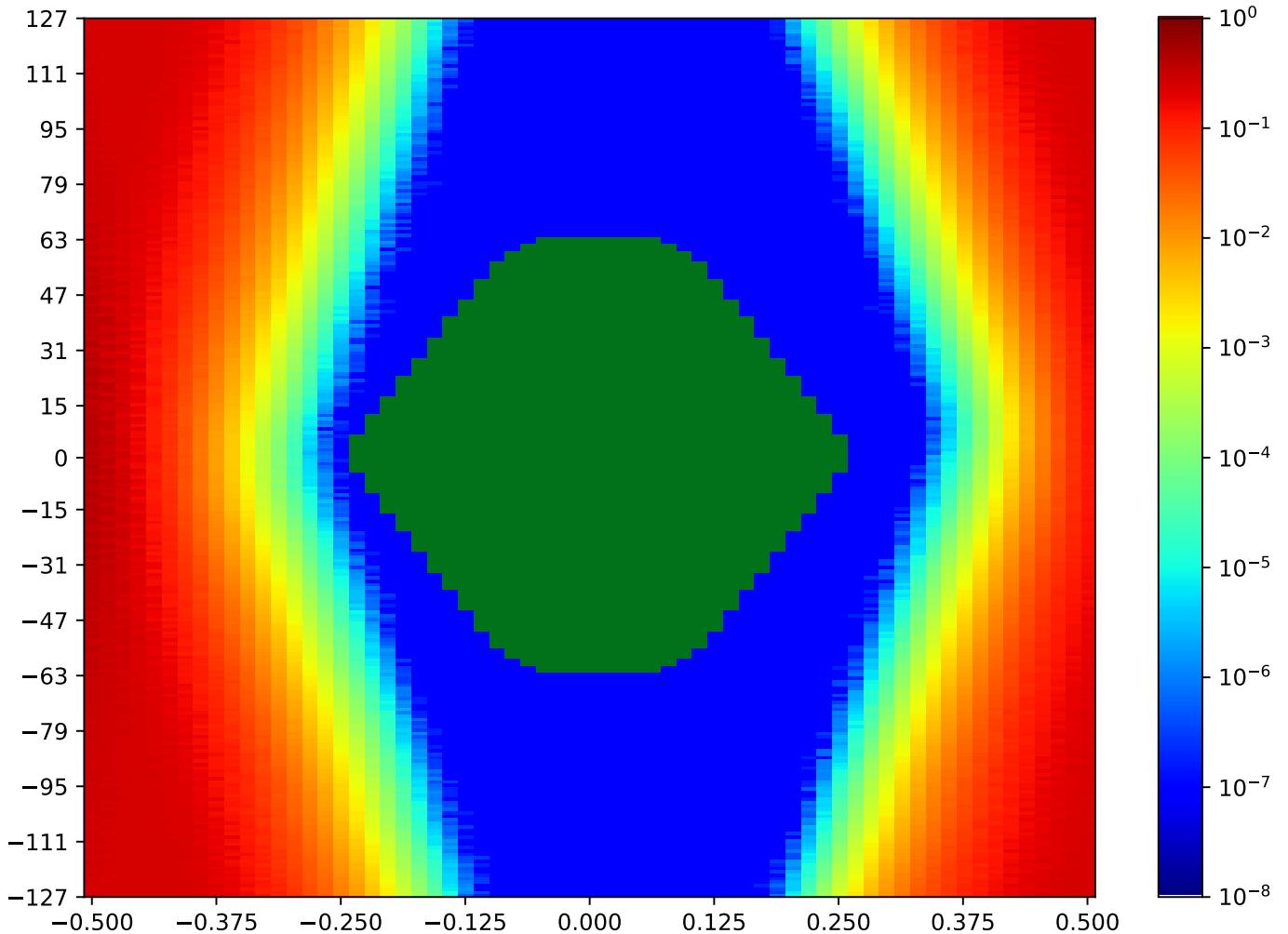


Figure 3.187: TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

Call back to summary Figure 3.179. Sibling eye diagrams: V1-6.4, V2-6.4, V2-12.8.

3.15 MSP_A TX1 MSP_C RX11 Minipod Loopback

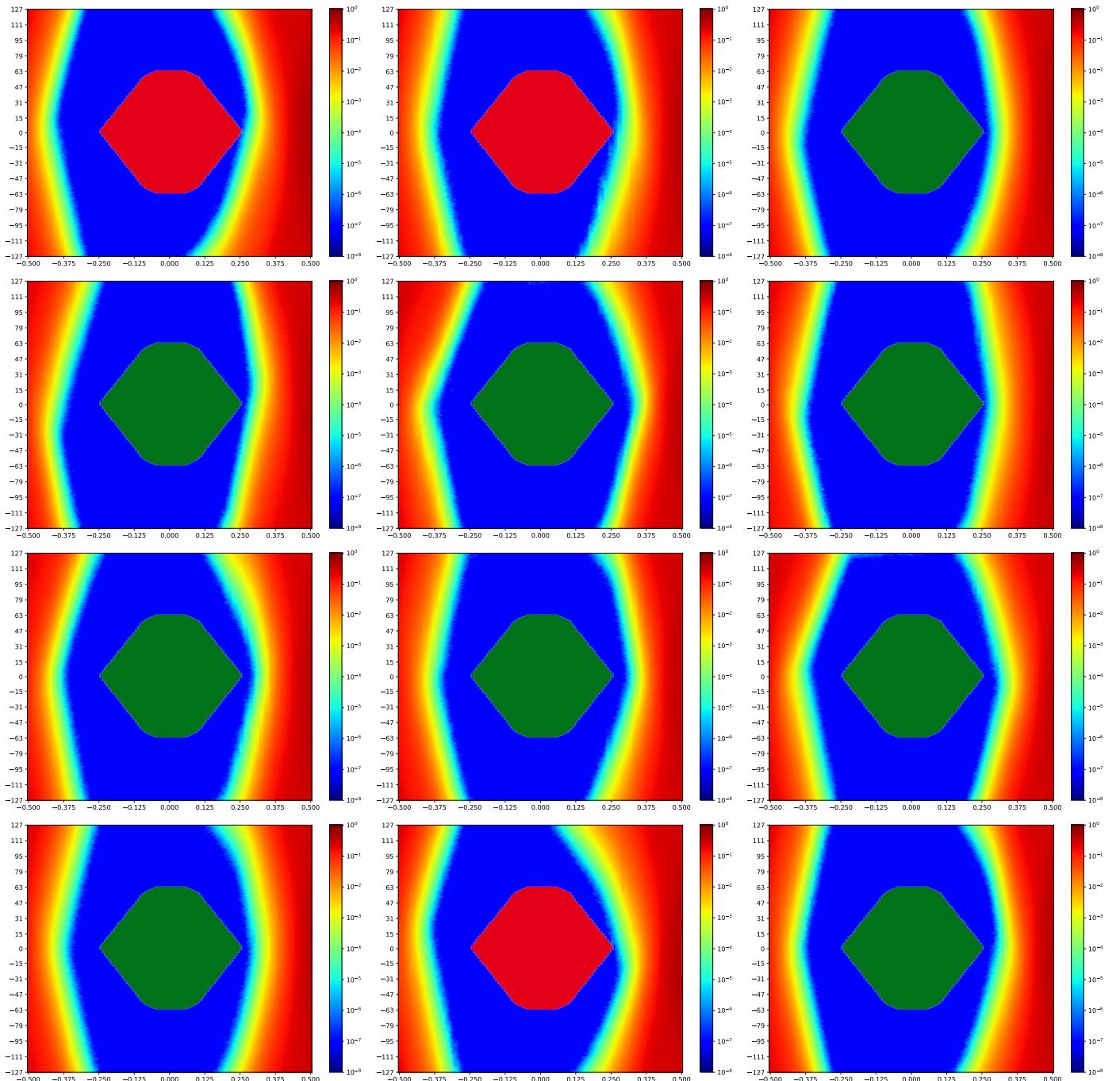


Figure 3.188: MSP_A TX1 MSP_C RX11 Minipod Loopback

A cross-reference to Figure 3.188. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.201.

3.15.1 MSP_A_FPGA-TX1-00-RX11-00-MSP_C_FPGA

Table 3.174: MSP_A_FPGA-TX1-00-RX11-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:57:58		2018-Jan-24 00:58:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17249	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

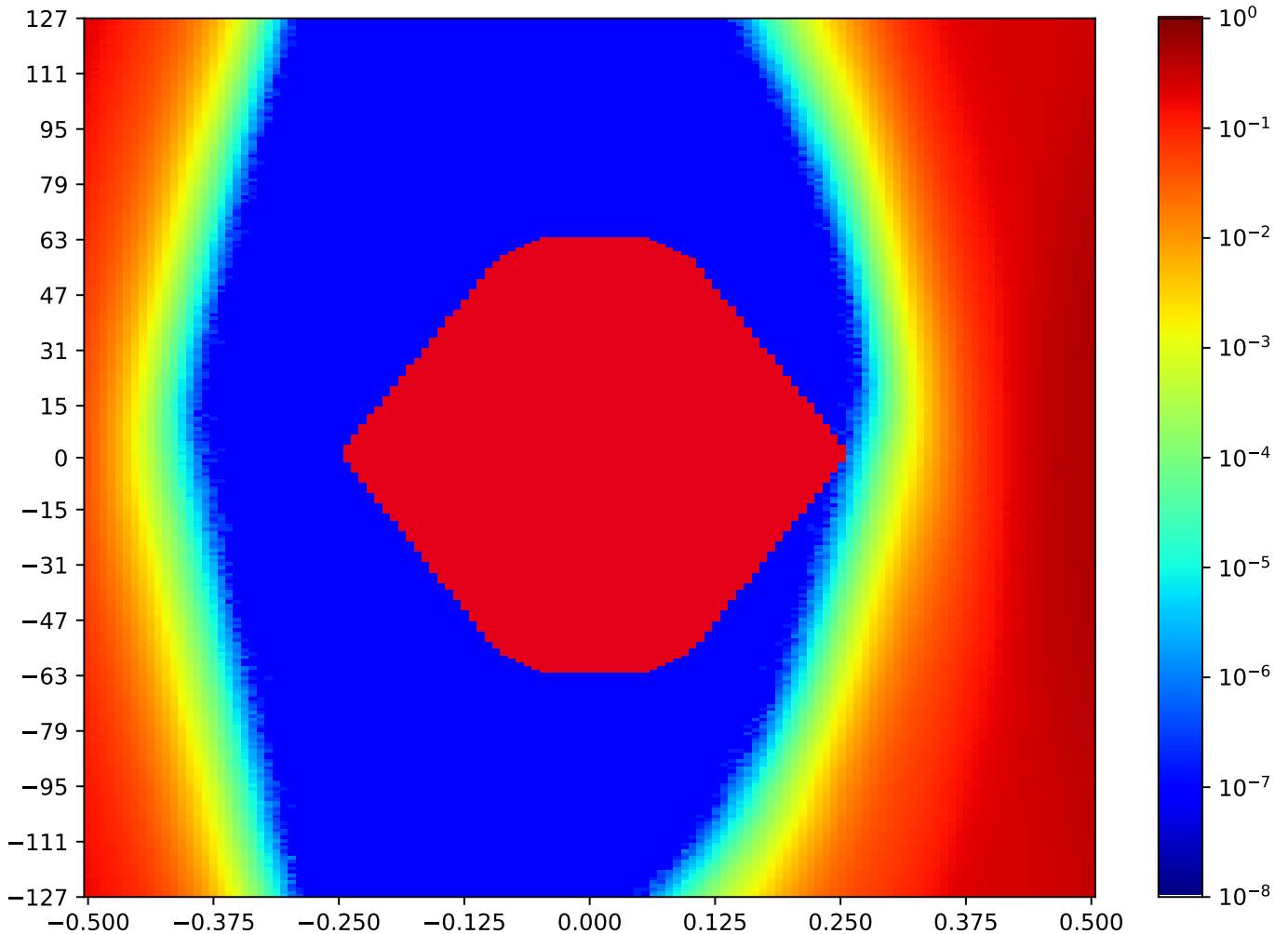


Figure 3.189: MSP_A_FPGA-TX1-00-RX11-00-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.2 MSP_A_FPGA-TX1-01-RX11-01-MSP_C_FPGA

Table 3.175: MSP_A_FPGA-TX1-01-RX11-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:59:22		2018-Jan-24 01:00:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16714	75	57.36%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

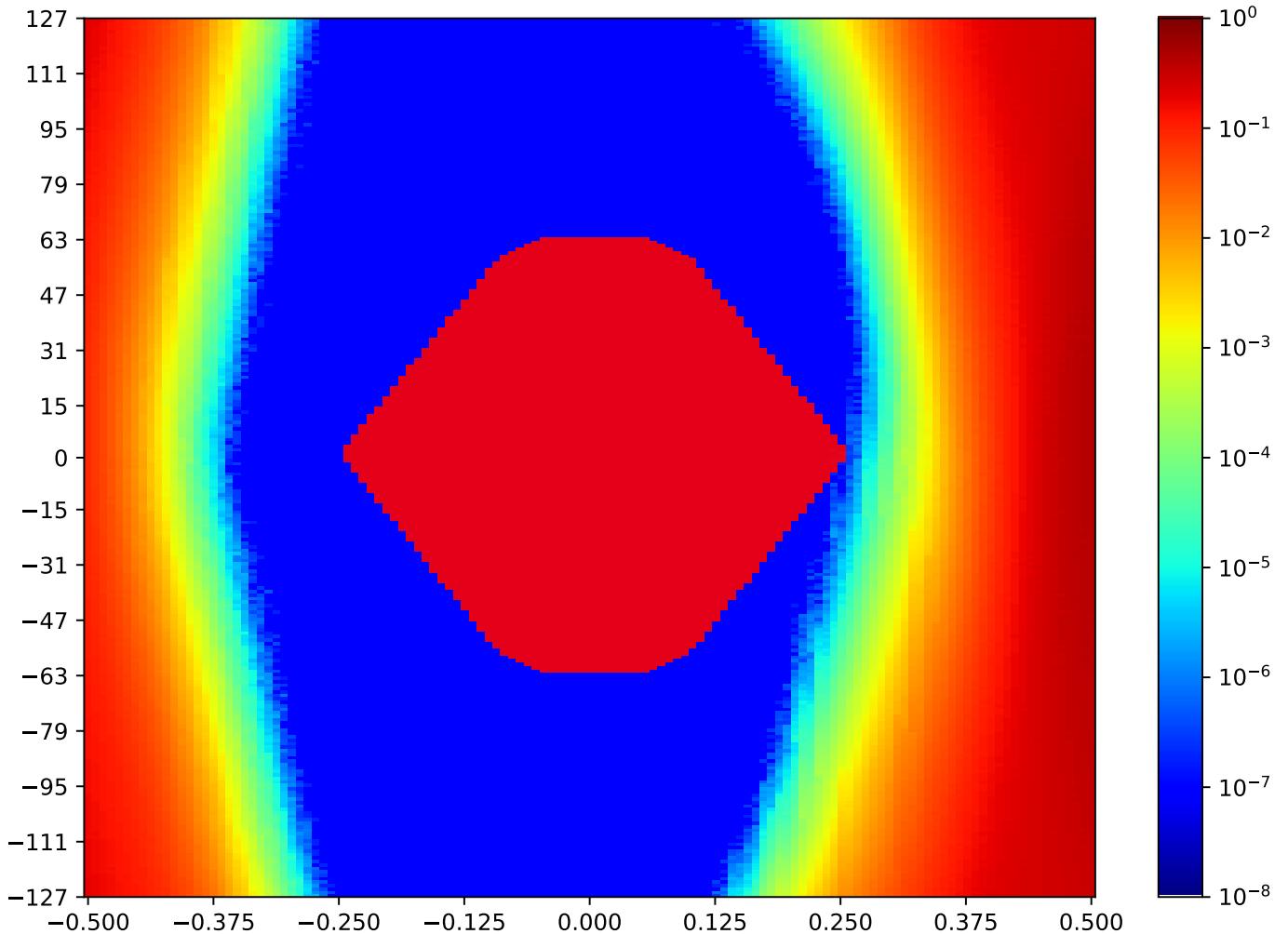


Figure 3.190: MSP_A_FPGA-TX1-01-RX11-01-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.3 MSP_A_FPGA-TX1-02-RX11-02-MSP_C_FPGA

Table 3.176: MSP_A_FPGA-TX1-02-RX11-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:00:03		2018-Jan-24 01:00:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17537	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

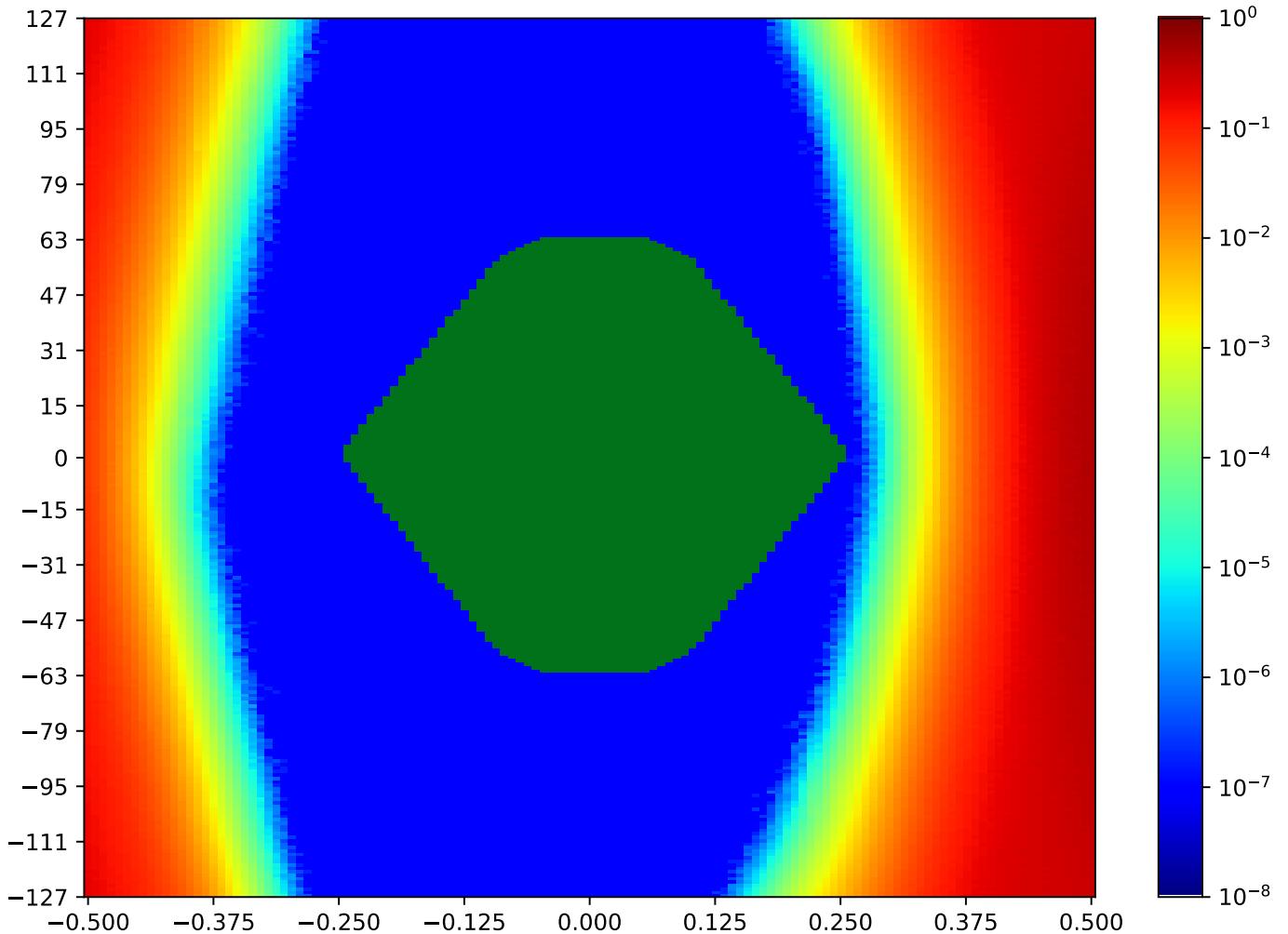


Figure 3.191: MSP_A_FPGA-TX1-02-RX11-02-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.4 MSP_A_FPGA-TX1-03-RX11-03-MSP_C_FPGA

Table 3.177: MSP_A_FPGA-TX1-03-RX11-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:56:34		2018-Jan-24 00:57:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17809	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

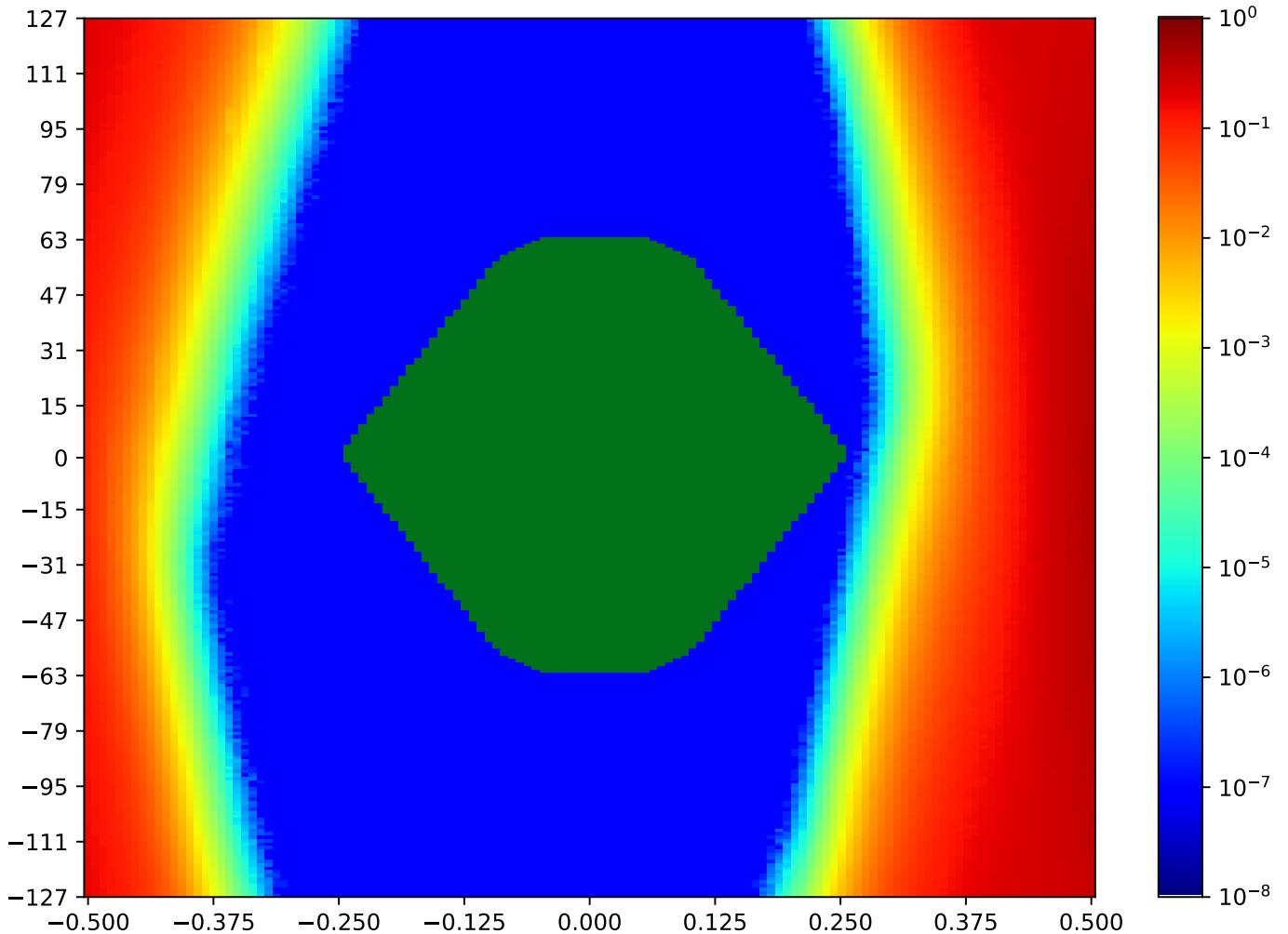


Figure 3.192: MSP_A_FPGA-TX1-03-RX11-03-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.5 MSP_A_FPGA-TX1-04-RX11-04-MSP_C_FPGA

Table 3.178: MSP_A_FPGA-TX1-04-RX11-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:02:08		2018-Jan-24 01:02:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17296	83	64.34%	250	97.65%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

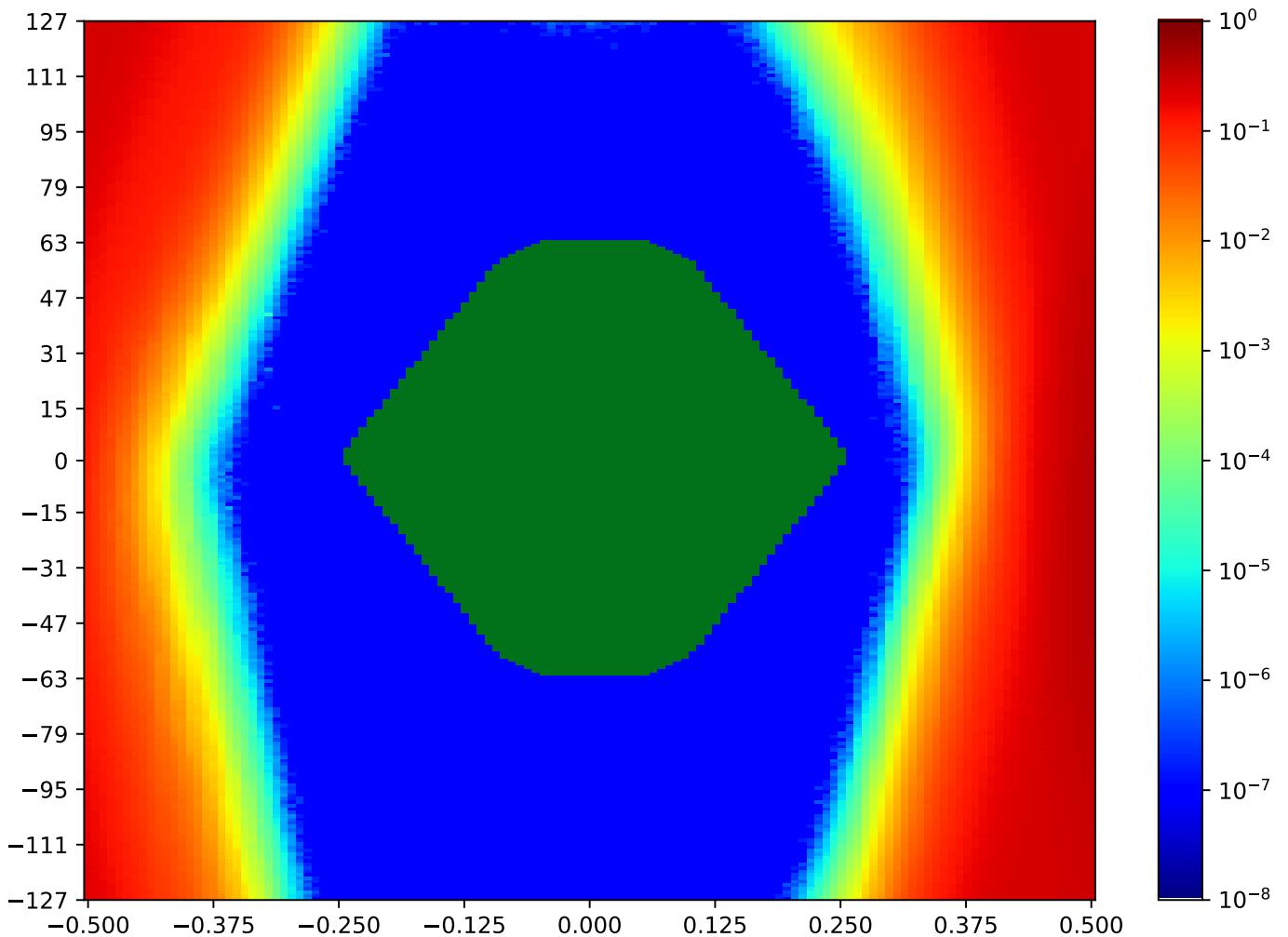


Figure 3.193: MSP_A_FPGA-TX1-04-RX11-04-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.6 MSP_A_FPGA-TX1-05-RX11-05-MSP_C_FPGA

Table 3.179: MSP_A_FPGA-TX1-05-RX11-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:55:52		2018-Jan-24 00:56:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17106	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

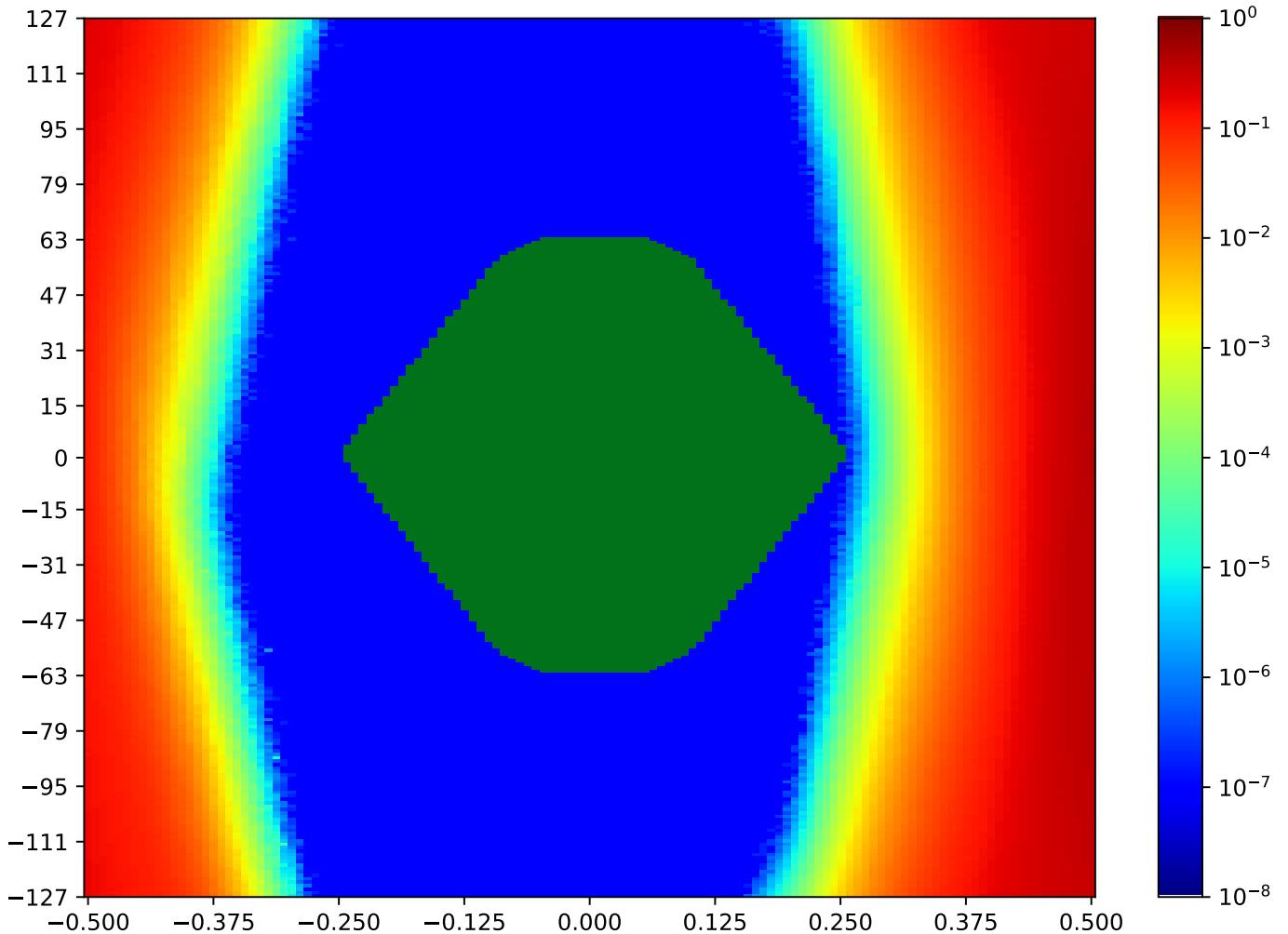


Figure 3.194: MSP_A_FPGA-TX1-05-RX11-05-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.7 MSP_A_FPGA-TX1-06-RX11-06-MSP_C_FPGA

Table 3.180: MSP_A_FPGA-TX1-06-RX11-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:03:31		2018-Jan-24 01:04:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16989	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

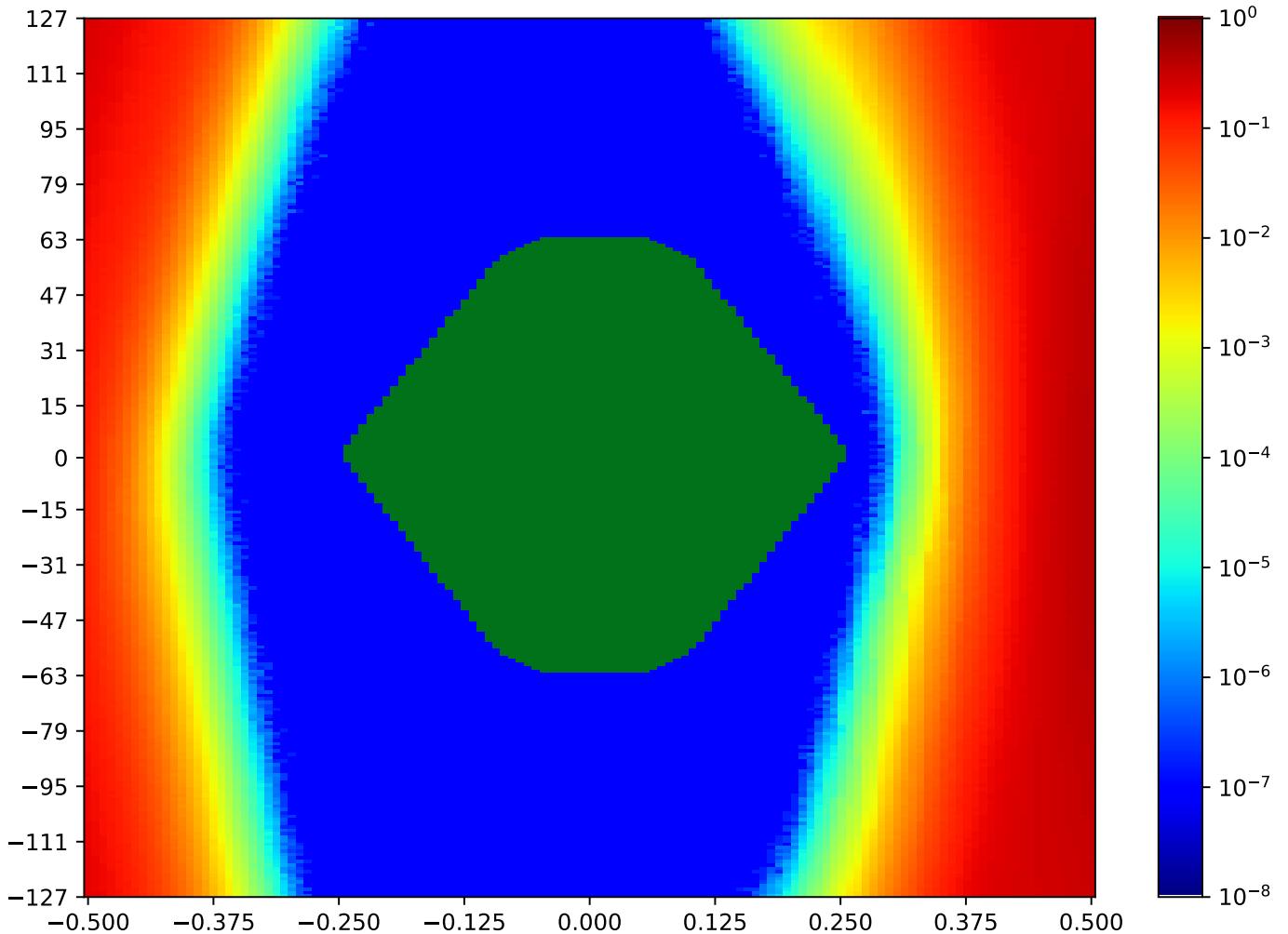


Figure 3.195: MSP_A_FPGA-TX1-06-RX11-06-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.8 MSP_A_FPGA-TX1-07-RX11-07-MSP_C_FPGA

Table 3.181: MSP_A_FPGA-TX1-07-RX11-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:57:16		2018-Jan-24 00:57:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17159	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

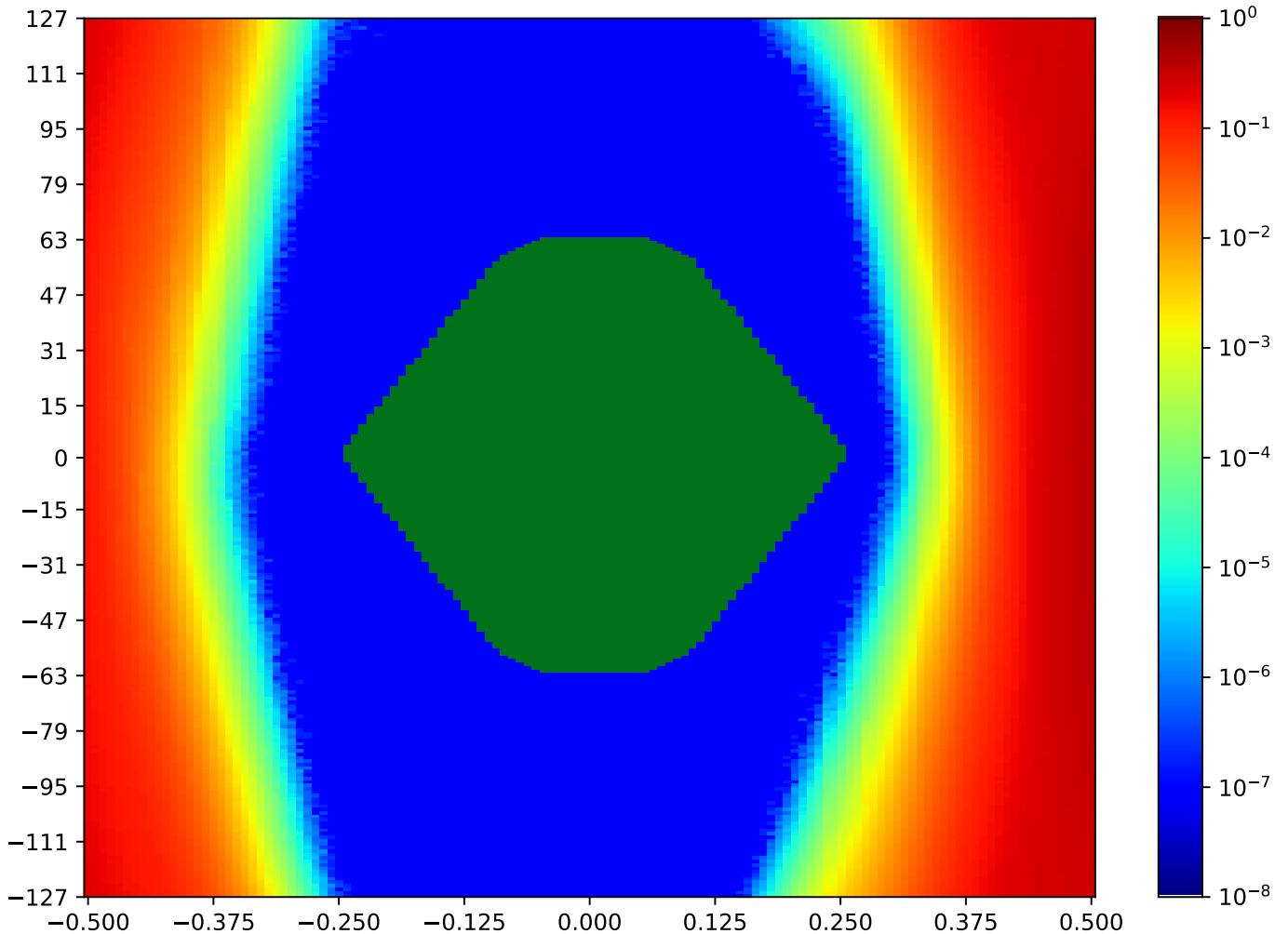


Figure 3.196: MSP_A_FPGA-TX1-07-RX11-07-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.9 MSP_A_FPGA-TX1-08-RX11-08-MSP_C_FPGA

Table 3.182: MSP_A_FPGA-TX1-08-RX11-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:02:50		2018-Jan-24 01:03:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16678	79	61.24%	248	97.25%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

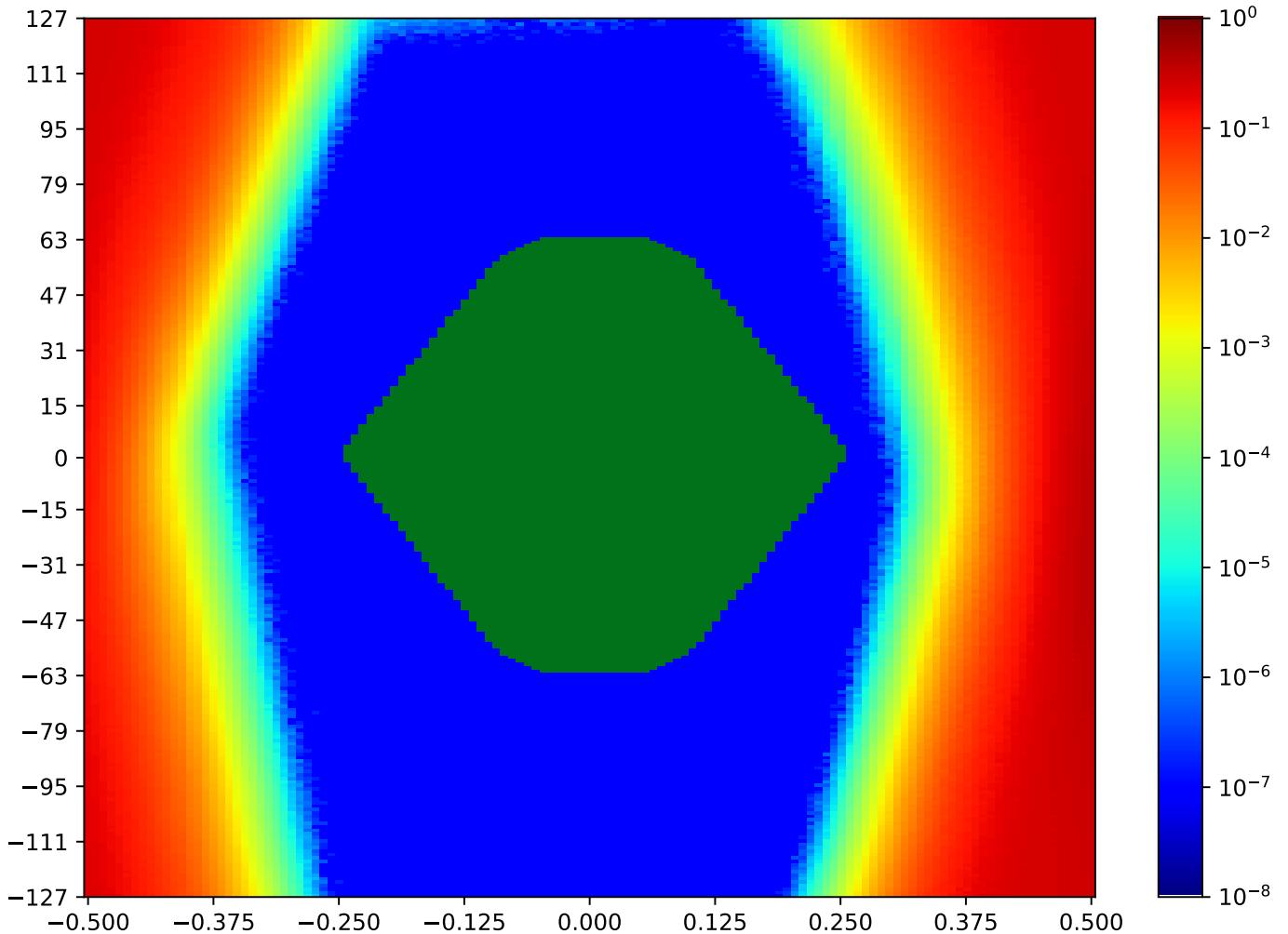


Figure 3.197: MSP_A_FPGA-TX1-08-RX11-08-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.10 MSP_A_FPGA-TX1-09-RX11-09-MSP_C_FPGA

Table 3.183: MSP_A_FPGA-TX1-09-RX11-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 00:58:40		2018-Jan-24 00:59:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16654	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

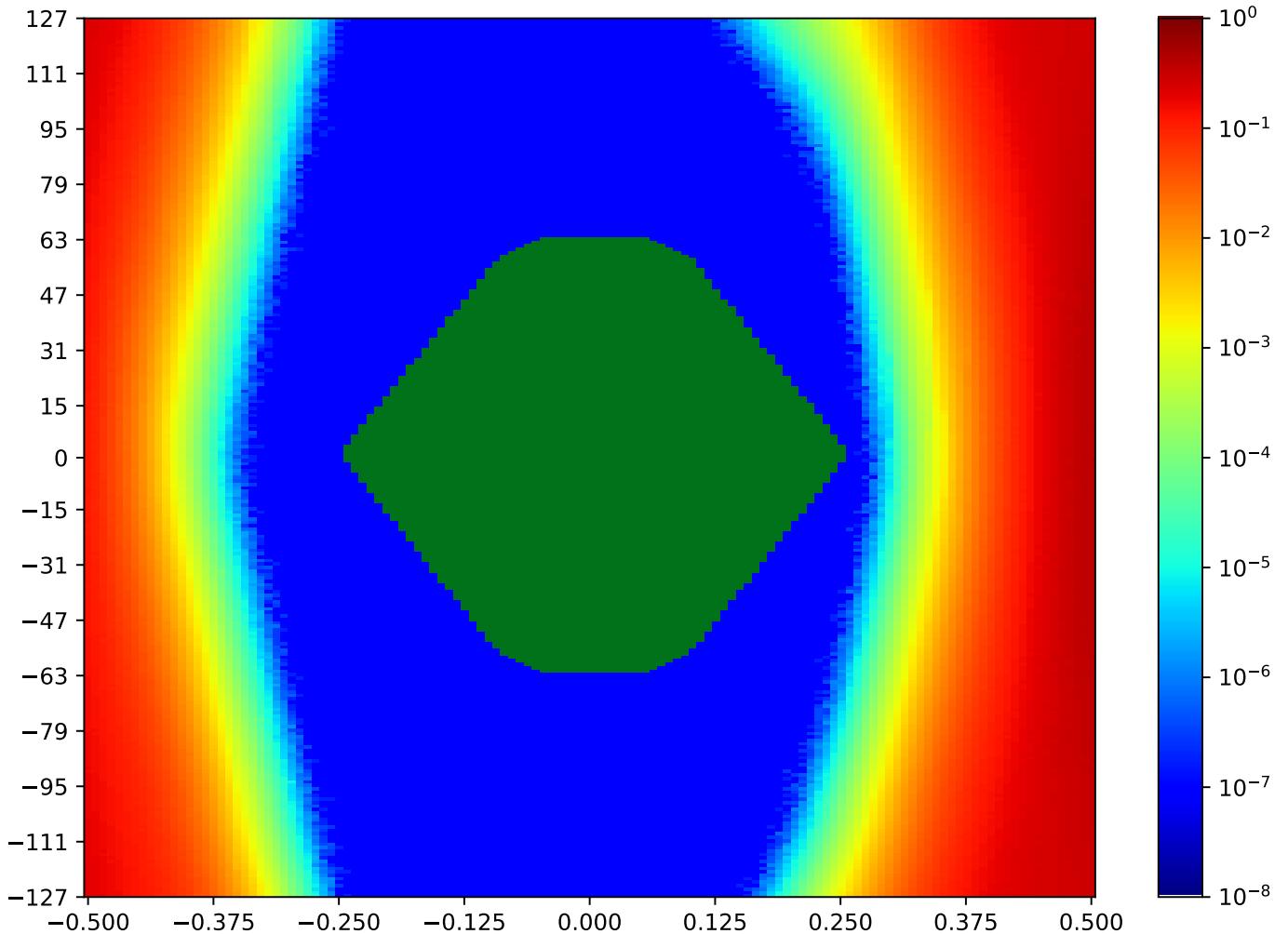


Figure 3.198: MSP_A_FPGA-TX1-09-RX11-09-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.11 MSP_A_FPGA-TX1-10-RX11-10-MSP_C_FPGA

Table 3.184: MSP_A_FPGA-TX1-10-RX11-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:01:27		2018-Jan-24 01:02:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16396	77	59.69%	255	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

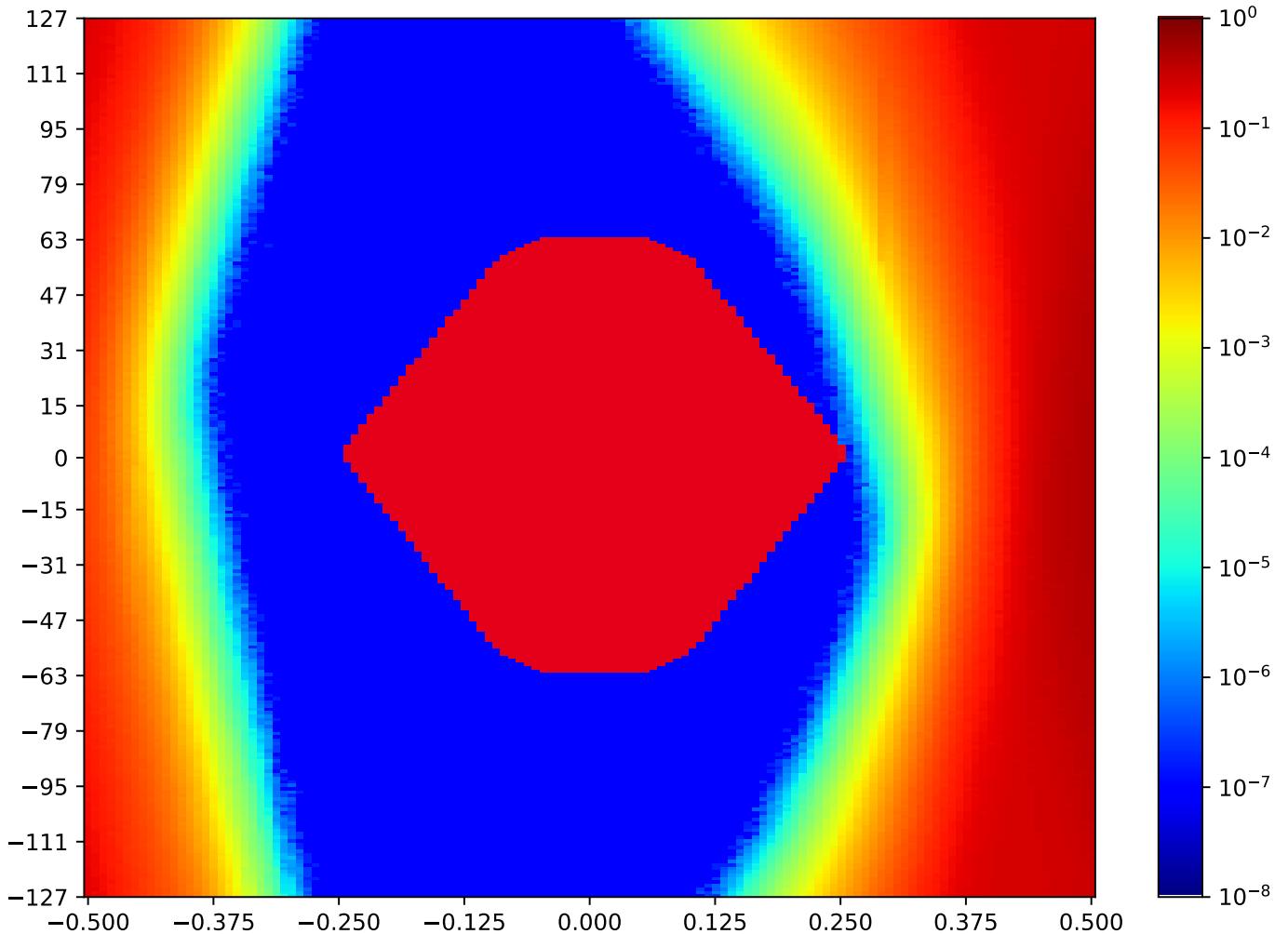


Figure 3.199: MSP_A_FPGA-TX1-10-RX11-10-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.15.12 MSP_A_FPGA-TX1-11-RX11-11-MSP_C_FPGA

Table 3.185: MSP_A_FPGA-TX1-11-RX11-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:00:45		2018-Jan-24 01:01:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17919	81	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

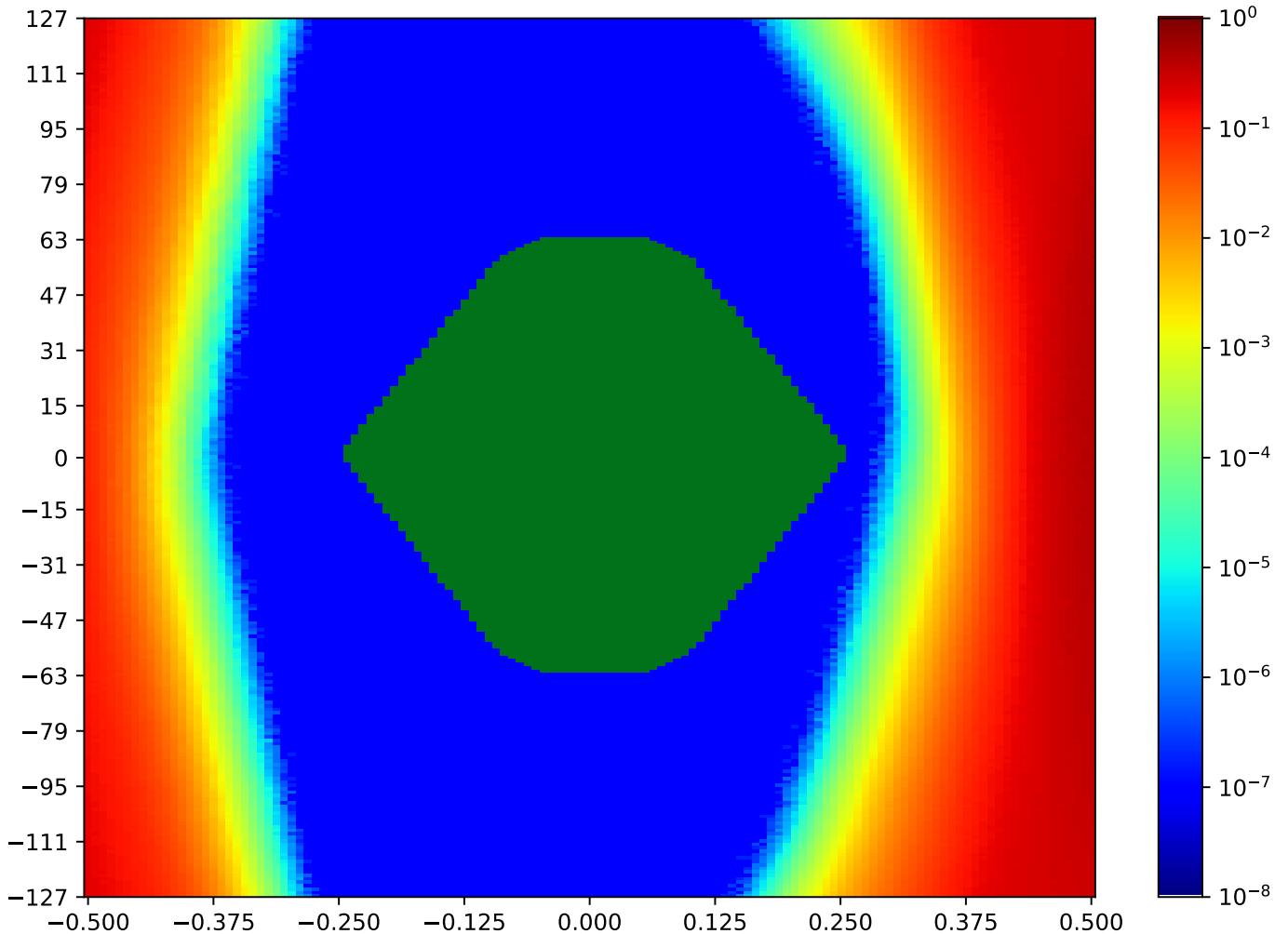


Figure 3.200: MSP_A_FPGA-TX1-11-RX11-11-MSP_C_FPGA

Call back to summary Figure 3.188. Sibling eye diagrams: V1-6.4.

3.16 MSP_A TX2 MSP_C RX10 Minipod Loopback

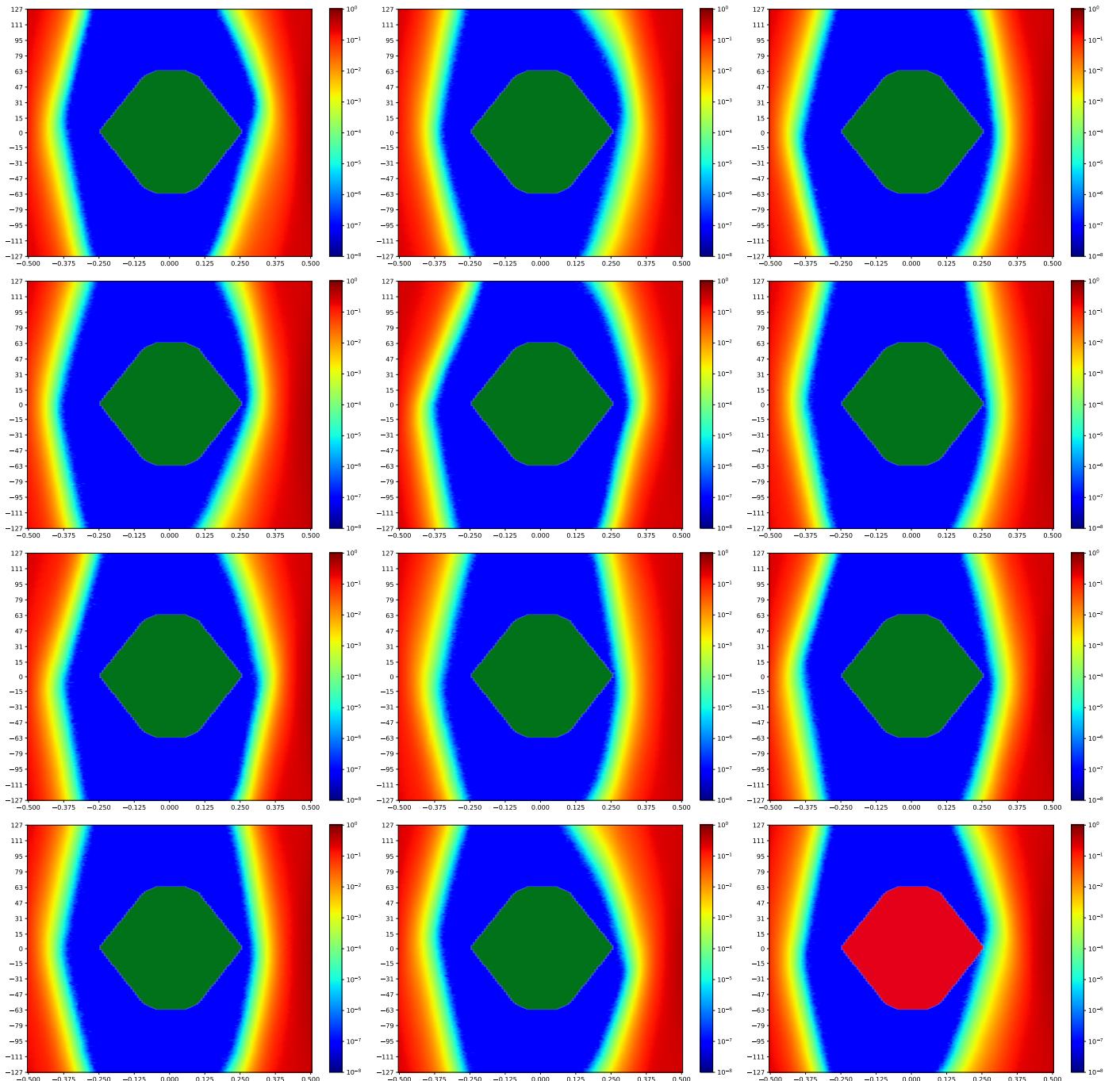


Figure 3.201: MSP_A TX2 MSP_C RX10 Minipod Loopback

A cross-reference to Figure 3.201. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.214.

3.16.1 MSP_A_FPGA-TX2-00-RX10-00-MSP_C_FPGA

Table 3.186: MSP_A_FPGA-TX2-00-RX10-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:06:19		2018-Jan-24 01:07:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17317	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

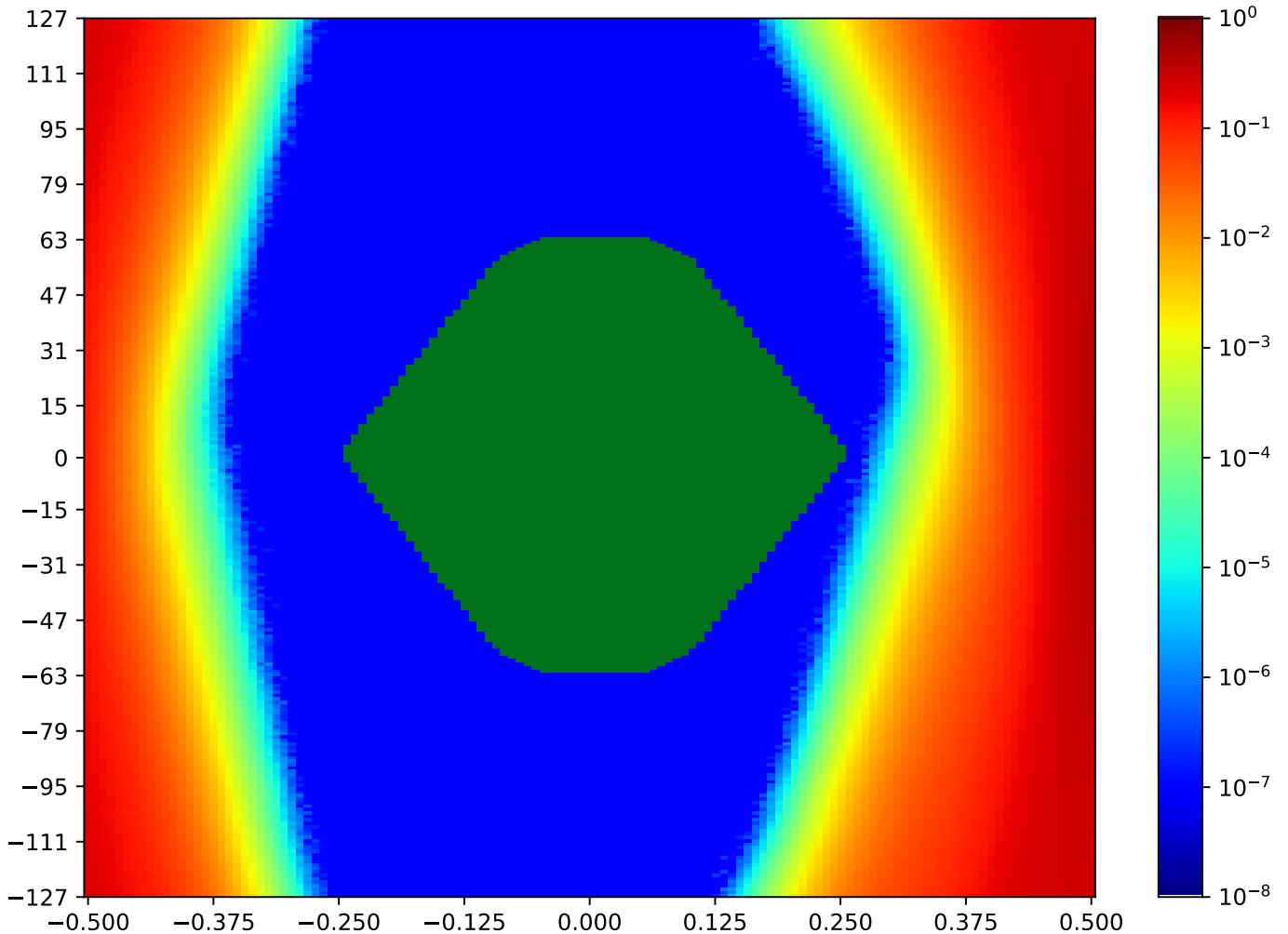


Figure 3.202: MSP_A_FPGA-TX2-00-RX10-00-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.2 MSP_A_FPGA-TX2-01-RX10-01-MSP_C_FPGA

Table 3.187: MSP_A_FPGA-TX2-01-RX10-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:04:55		2018-Jan-24 01:05:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16212	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

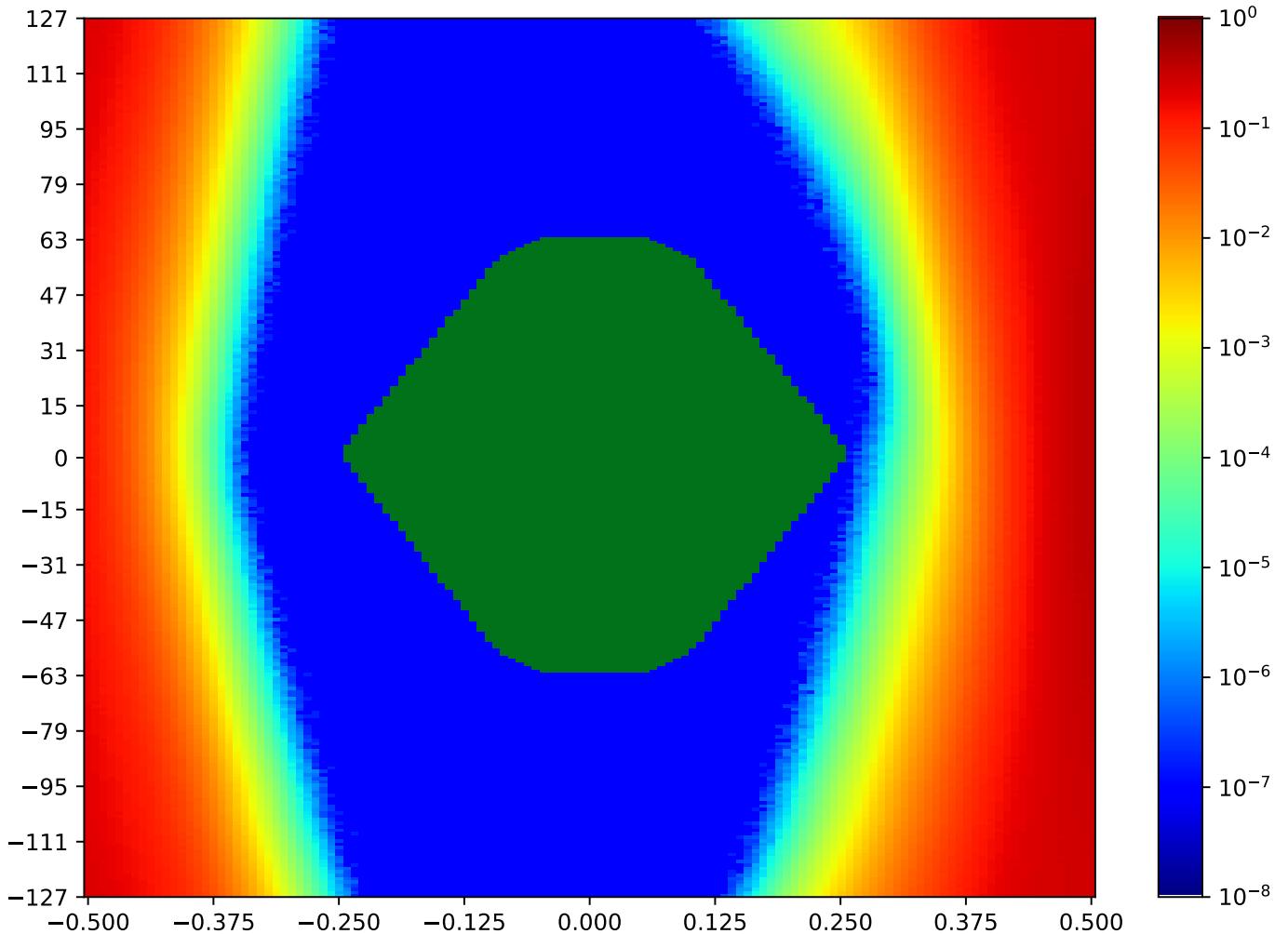


Figure 3.203: MSP_A_FPGA-TX2-01-RX10-01-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.3 MSP_A_FPGA-TX2-02-RX10-02-MSP_C_FPGA

Table 3.188: MSP_A_FPGA-TX2-02-RX10-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:08:27		2018-Jan-24 01:09:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17974	83	64.34%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

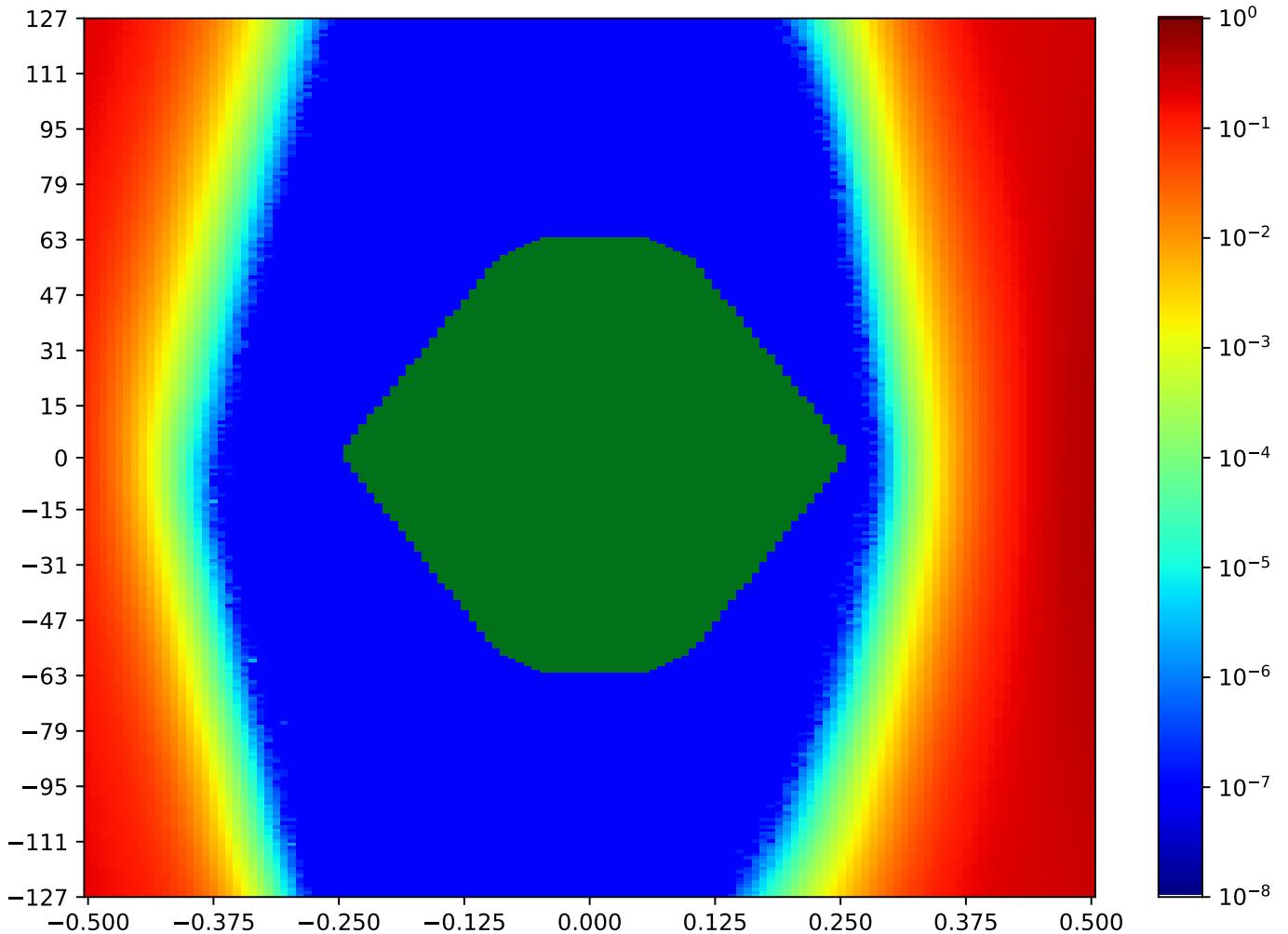


Figure 3.204: MSP_A_FPGA-TX2-02-RX10-02-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.4 MSP_A_FPGA-TX2-03-RX10-03-MSP_C_FPGA

Table 3.189: MSP_A_FPGA-TX2-03-RX10-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:04:13		2018-Jan-24 01:04:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16942	83	64.34%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

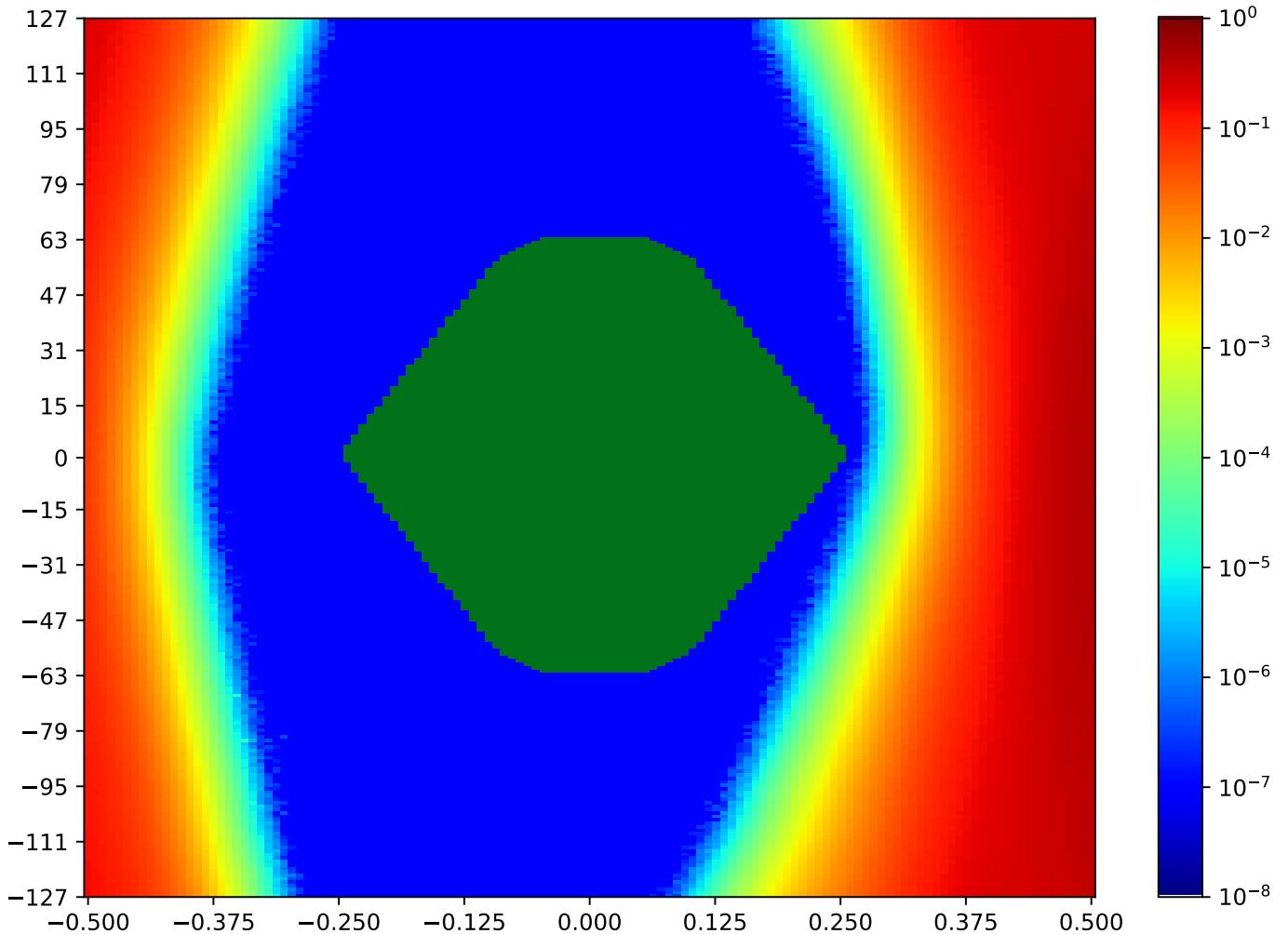


Figure 3.205: MSP_A_FPGA-TX2-03-RX10-03-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.5 MSP_A_FPGA-TX2-04-RX10-04-MSP_C_FPGA

Table 3.190: MSP_A_FPGA-TX2-04-RX10-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:10:35		2018-Jan-24 01:11:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17434	84	65.12%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

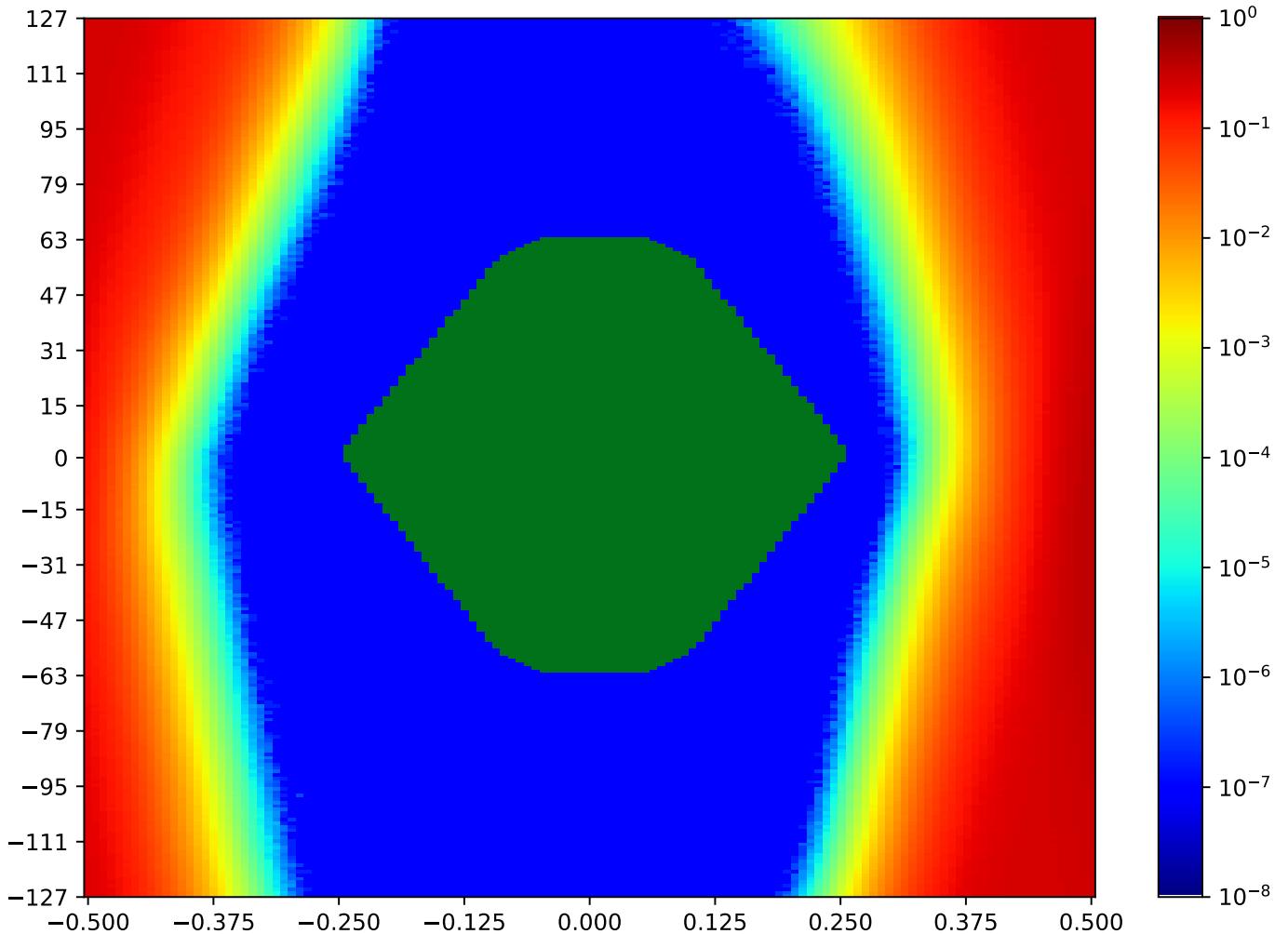


Figure 3.206: MSP_A_FPGA-TX2-04-RX10-04-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.6 MSP_A_FPGA-TX2-05-RX10-05-MSP_C_FPGA

Table 3.191: MSP_A_FPGA-TX2-05-RX10-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:05:37		2018-Jan-24 01:06:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16786	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

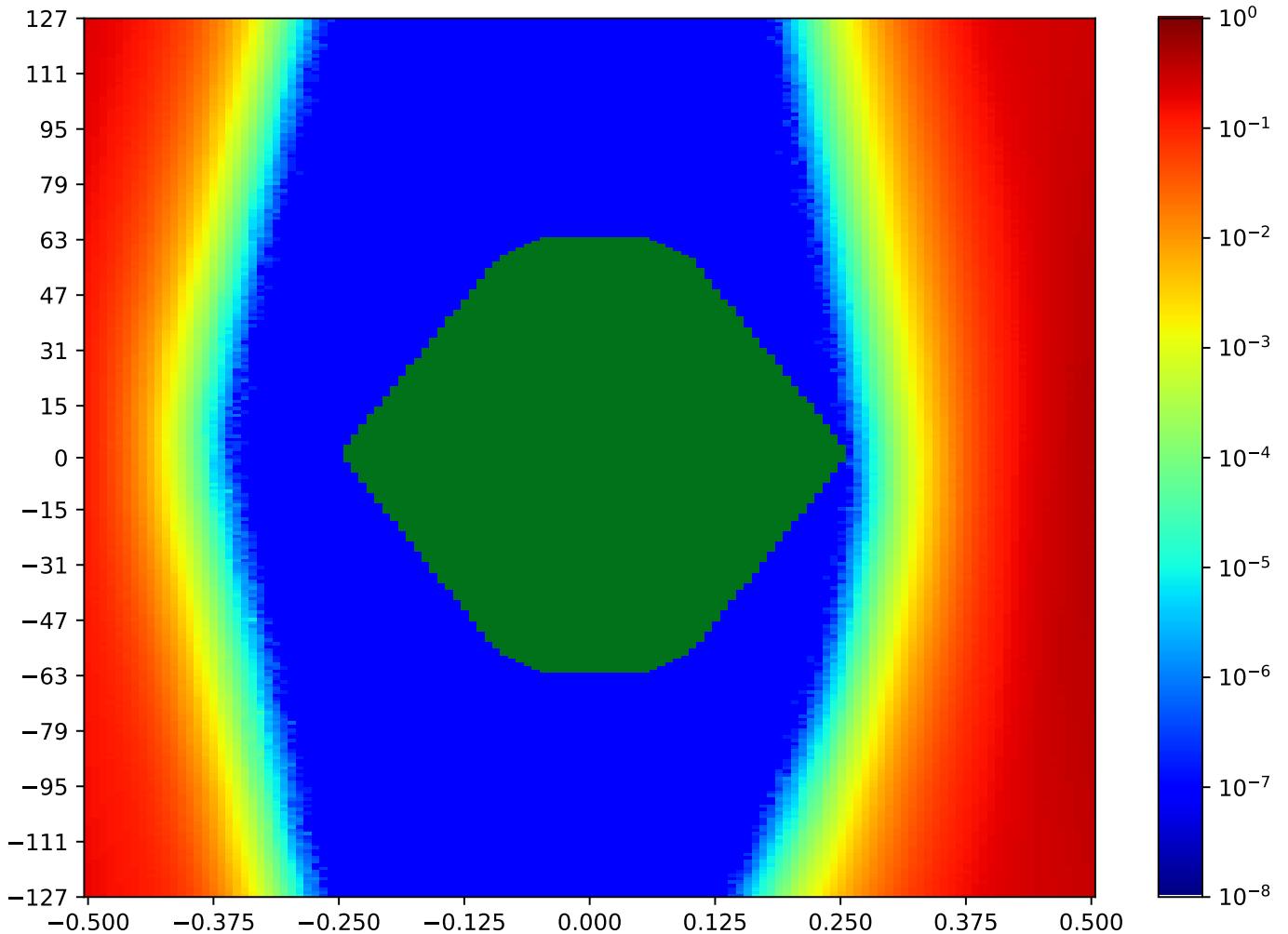


Figure 3.207: MSP_A_FPGA-TX2-05-RX10-05-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.7 MSP_A_FPGA-TX2-06-RX10-06-MSP_C_FPGA

Table 3.192: MSP_A_FPGA-TX2-06-RX10-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:12:00		2018-Jan-24 01:12:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17901	83	64.34%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

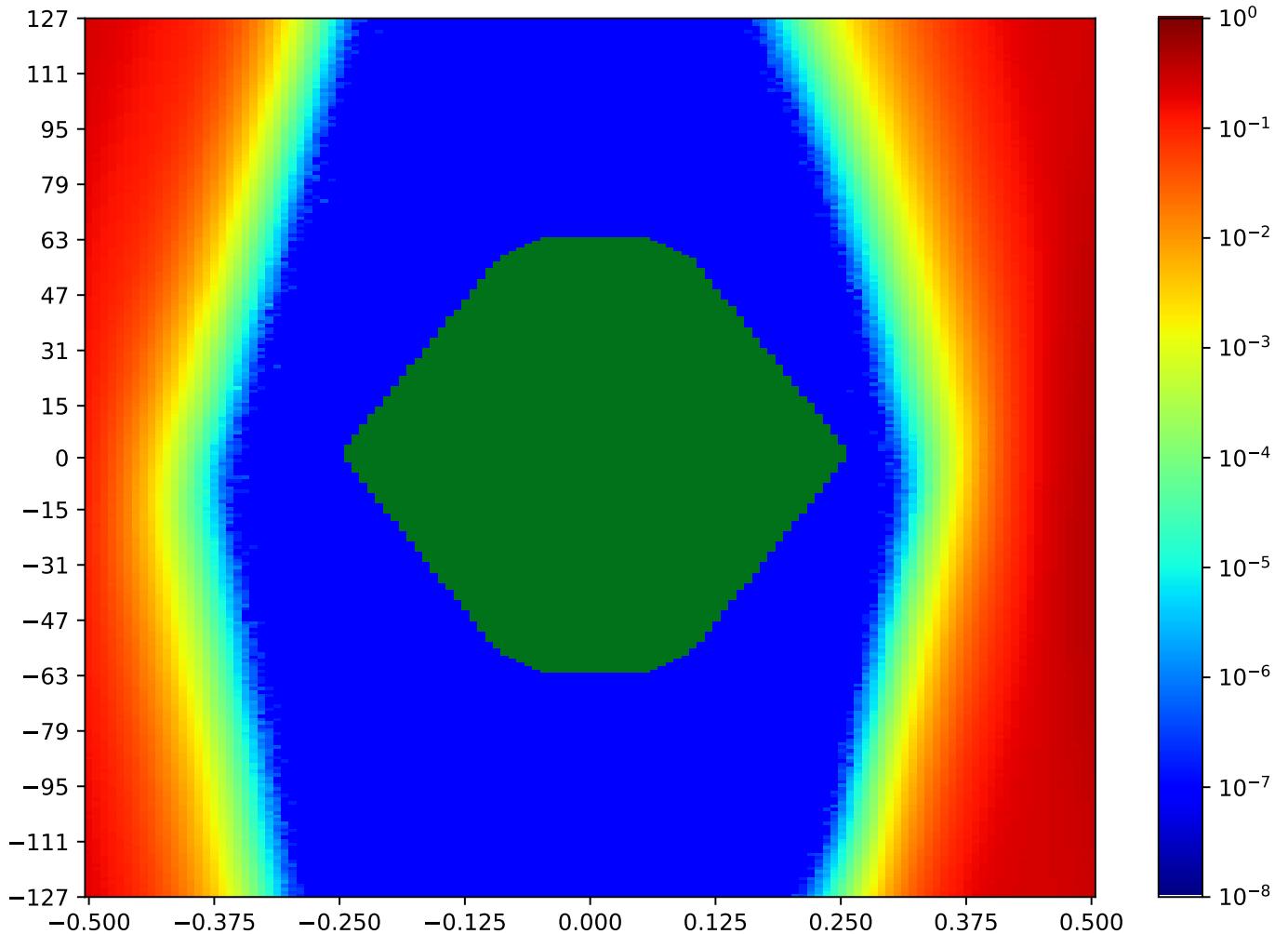


Figure 3.208: MSP_A_FPGA-TX2-06-RX10-06-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.8 MSP_A_FPGA-TX2-07-RX10-07-MSP_C_FPGA

Table 3.193: MSP_A_FPGA-TX2-07-RX10-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:07:02		2018-Jan-24 01:07:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16150	74	56.59%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

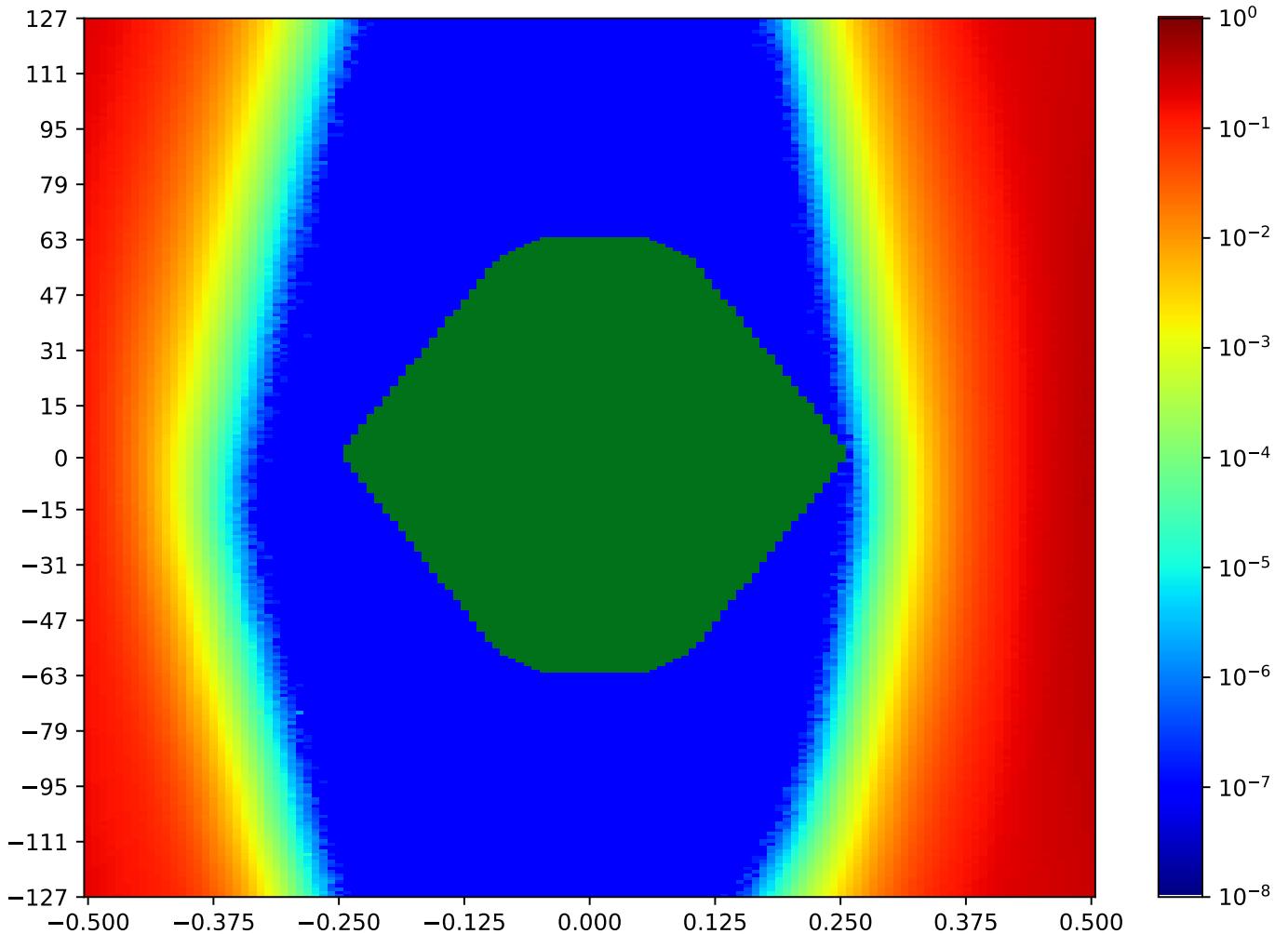


Figure 3.209: MSP_A_FPGA-TX2-07-RX10-07-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.9 MSP_A_FPGA-TX2-08-RX10-08-MSP_C_FPGA

Table 3.194: MSP_A_FPGA-TX2-08-RX10-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:11:17		2018-Jan-24 01:12:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17522	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

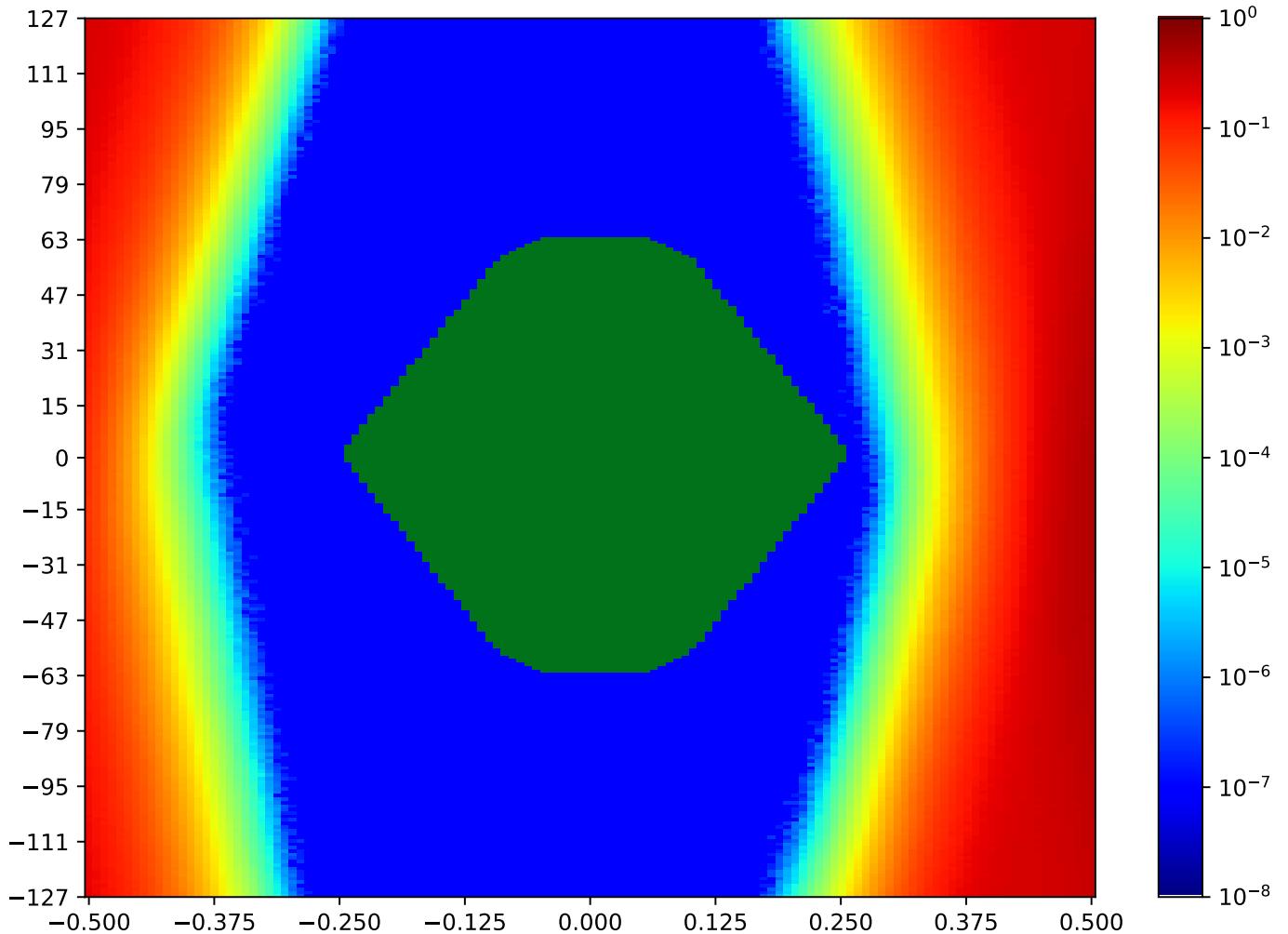


Figure 3.210: MSP_A_FPGA-TX2-08-RX10-08-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.10 MSP_A_FPGA-TX2-09-RX10-09-MSP_C_FPGA

Table 3.195: MSP_A_FPGA-TX2-09-RX10-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:07:44		2018-Jan-24 01:08:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17951	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

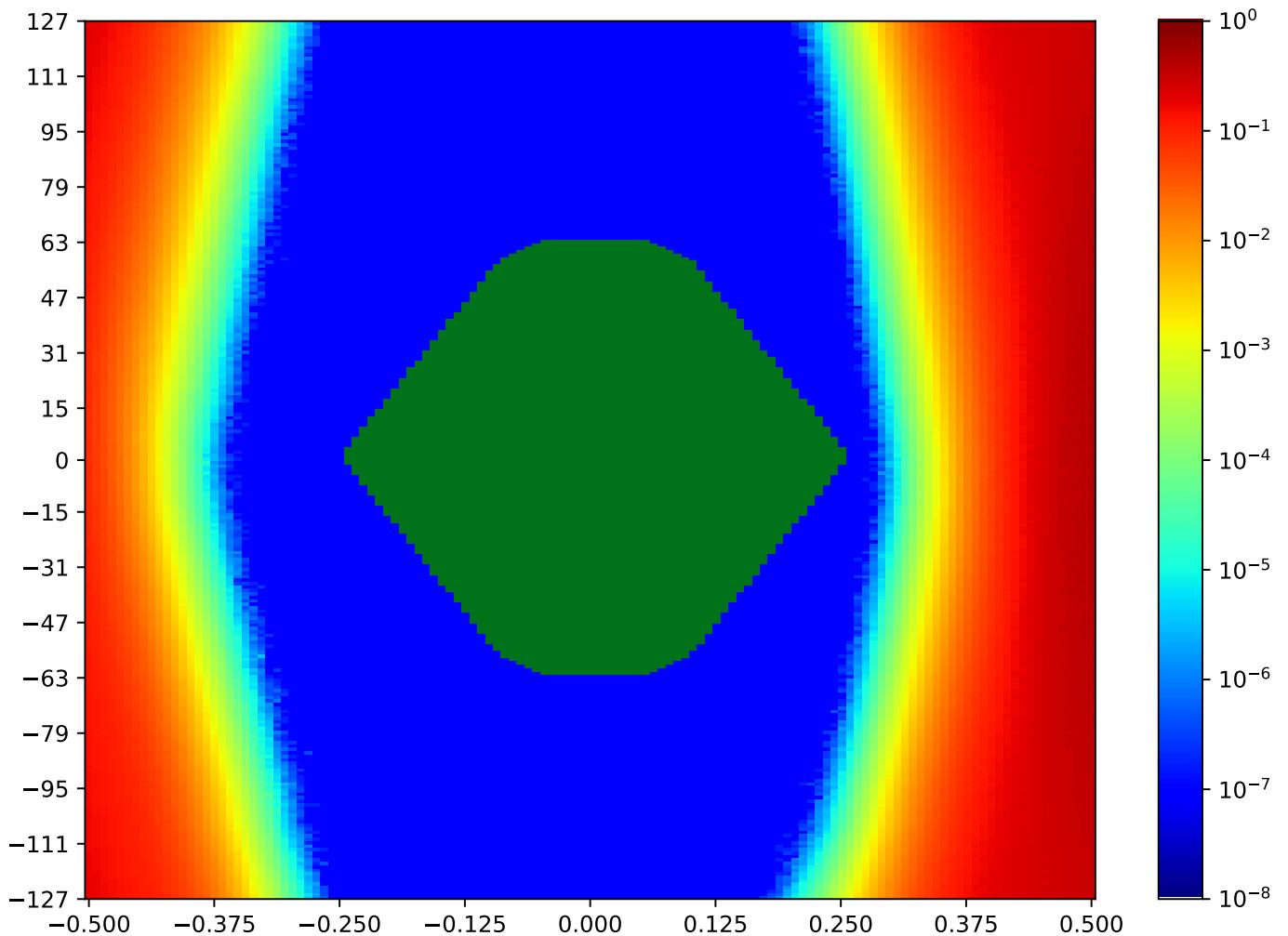


Figure 3.211: MSP_A_FPGA-TX2-09-RX10-09-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.11 MSP_A_FPGA-TX2-10-RX10-10-MSP_C_FPGA

Table 3.196: MSP_A_FPGA-TX2-10-RX10-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:09:52		2018-Jan-24 01:10:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16343	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

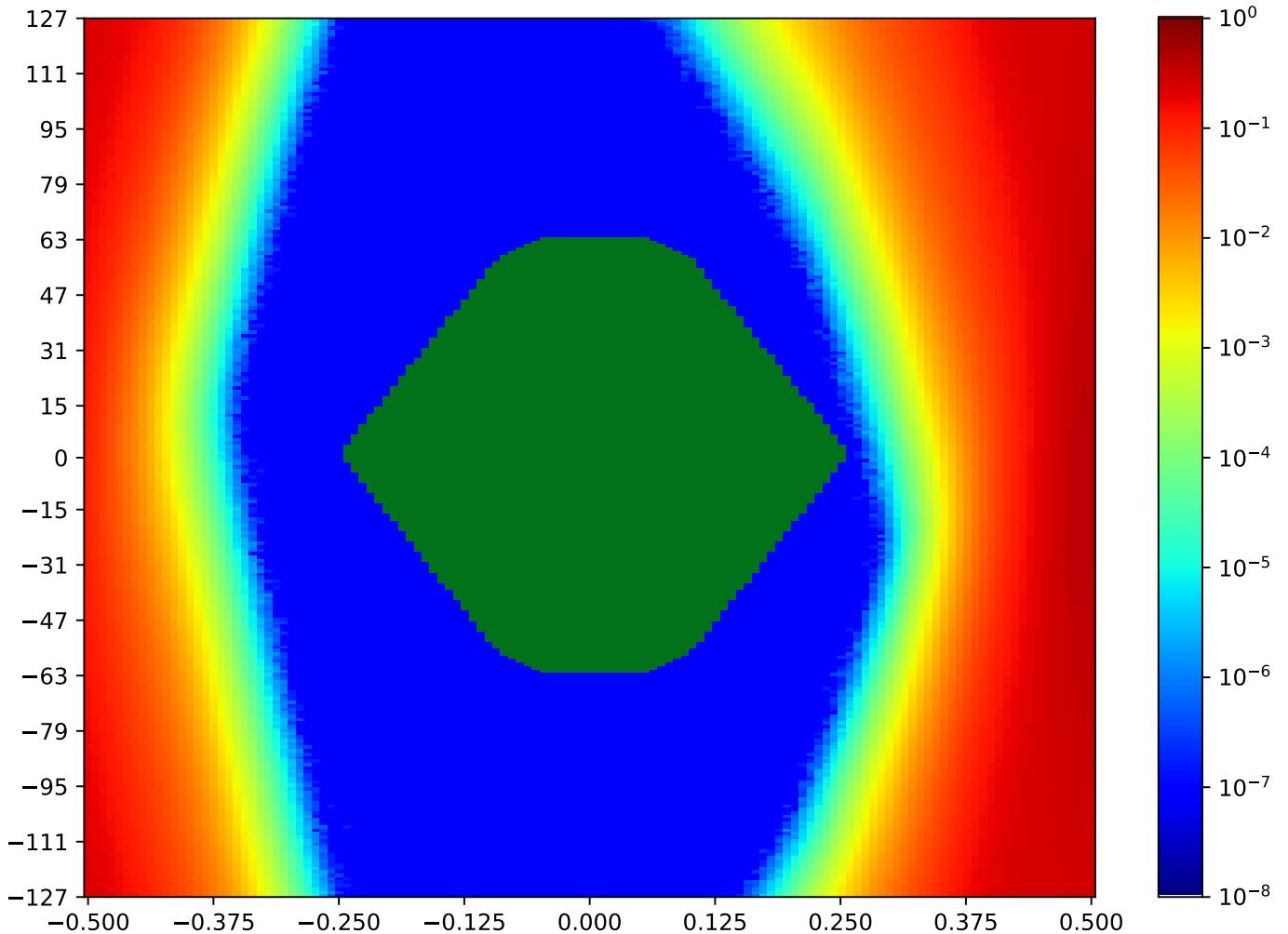


Figure 3.212: MSP_A_FPGA-TX2-10-RX10-10-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.16.12 MSP_A_FPGA-TX2-11-RX10-11-MSP_C_FPGA

Table 3.197: MSP_A_FPGA-TX2-11-RX10-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:09:10		2018-Jan-24 01:09:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16534	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

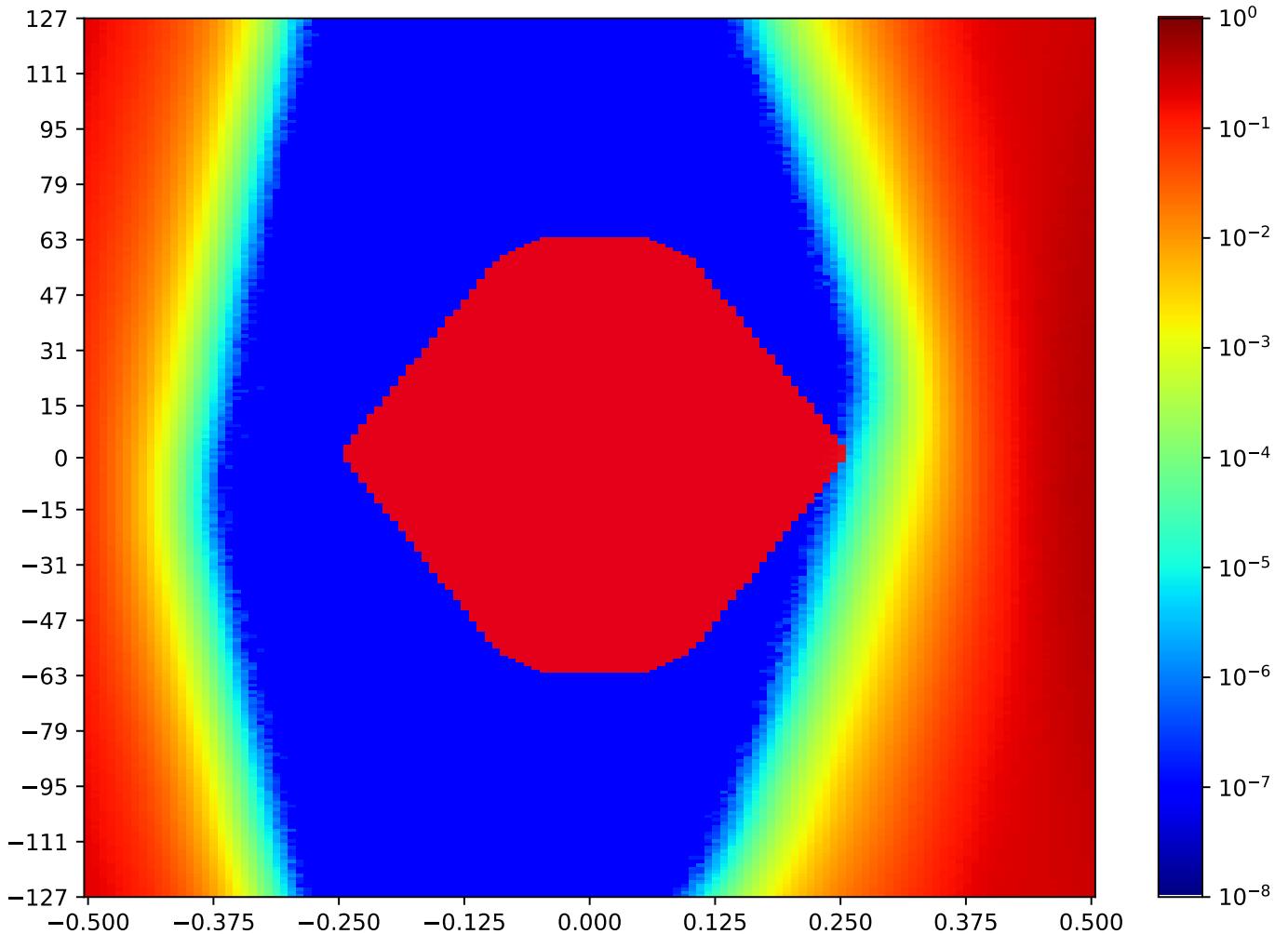


Figure 3.213: MSP_A_FPGA-TX2-11-RX10-11-MSP_C_FPGA

Call back to summary Figure 3.201. Sibling eye diagrams: V1-6.4.

3.17 MSP_C TX3 MSP_A RX2 Minipod Loopback

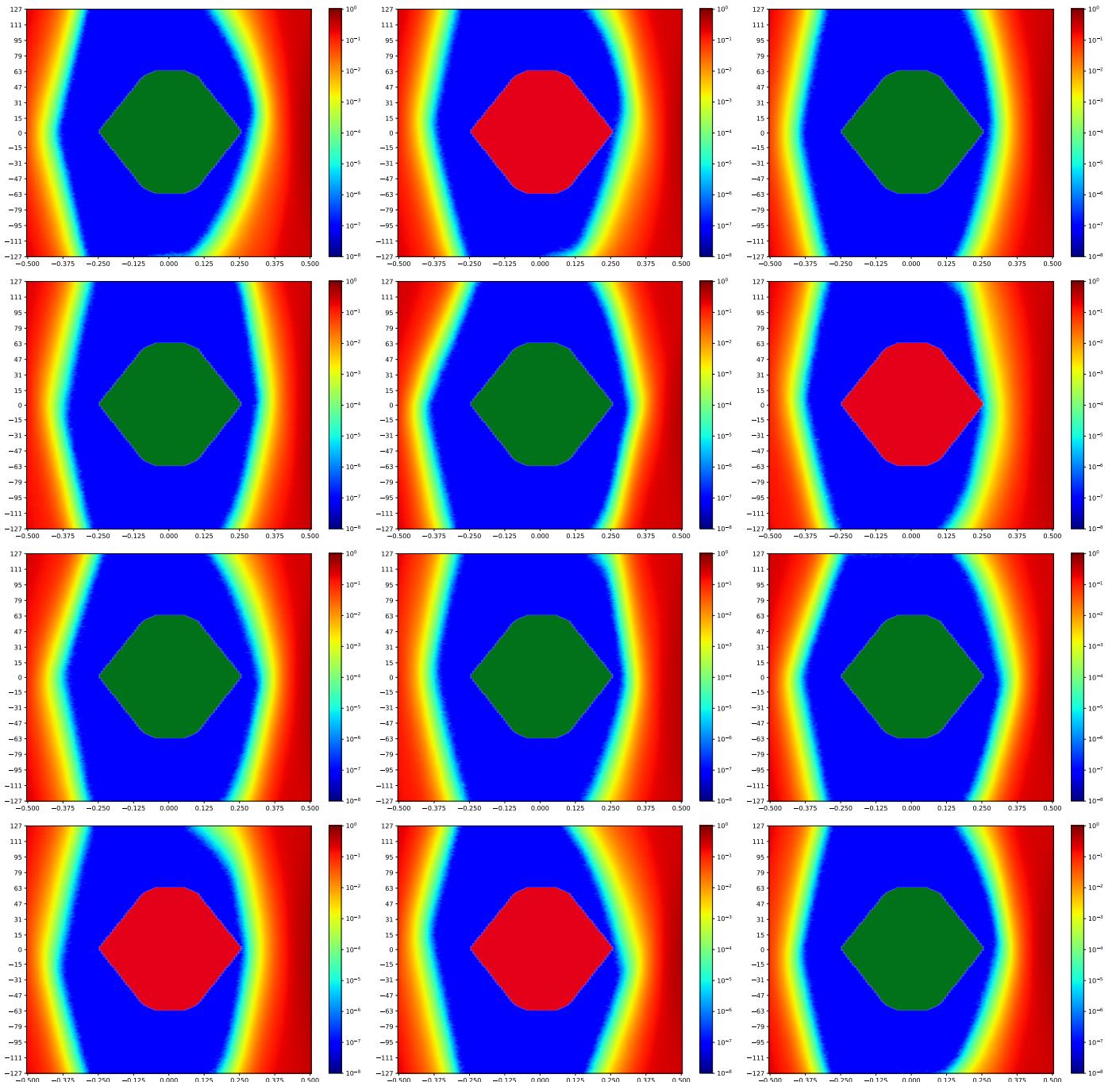


Figure 3.214: MSP_C TX3 MSP_A RX2 Minipod Loopback

A cross-reference to Figure 3.214. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.227.

3.17.1 MSP_C_FPGA-TX3-00-RX2-00-MSP_A_FPGA

Table 3.198: MSP_C_FPGA-TX3-00-RX2-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:14:51		2018-Jan-24 01:15:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17145	82	63.57%	249	97.65%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

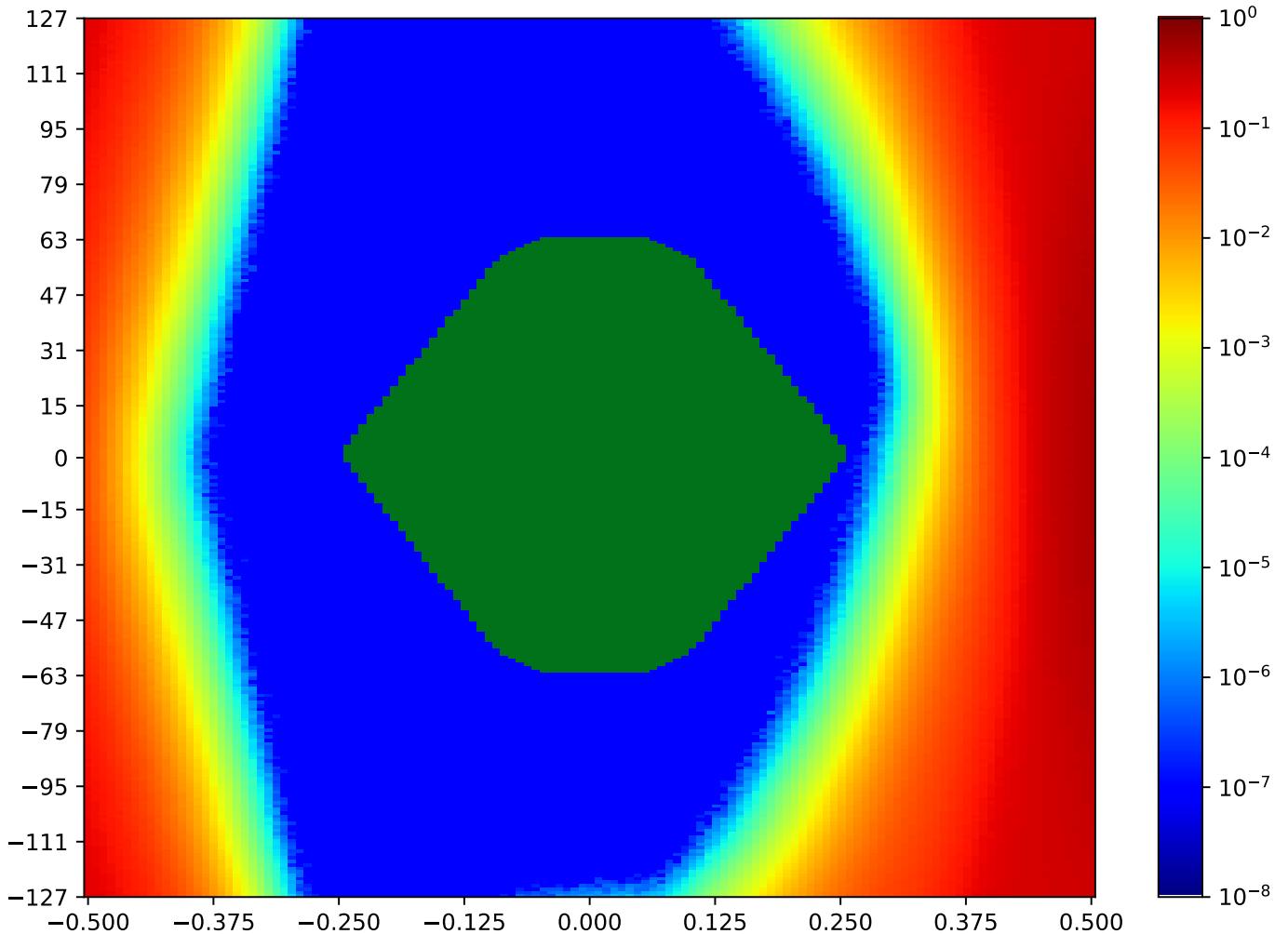


Figure 3.215: MSP_C_FPGA-TX3-00-RX2-00-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.2 MSP_C_FPGA-TX3-01-RX2-01-MSP_A_FPGA

Table 3.199: MSP_C_FPGA-TX3-01-RX2-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:16:16		2018-Jan-24 01:16:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16708	78	60.47%	251	98.04%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

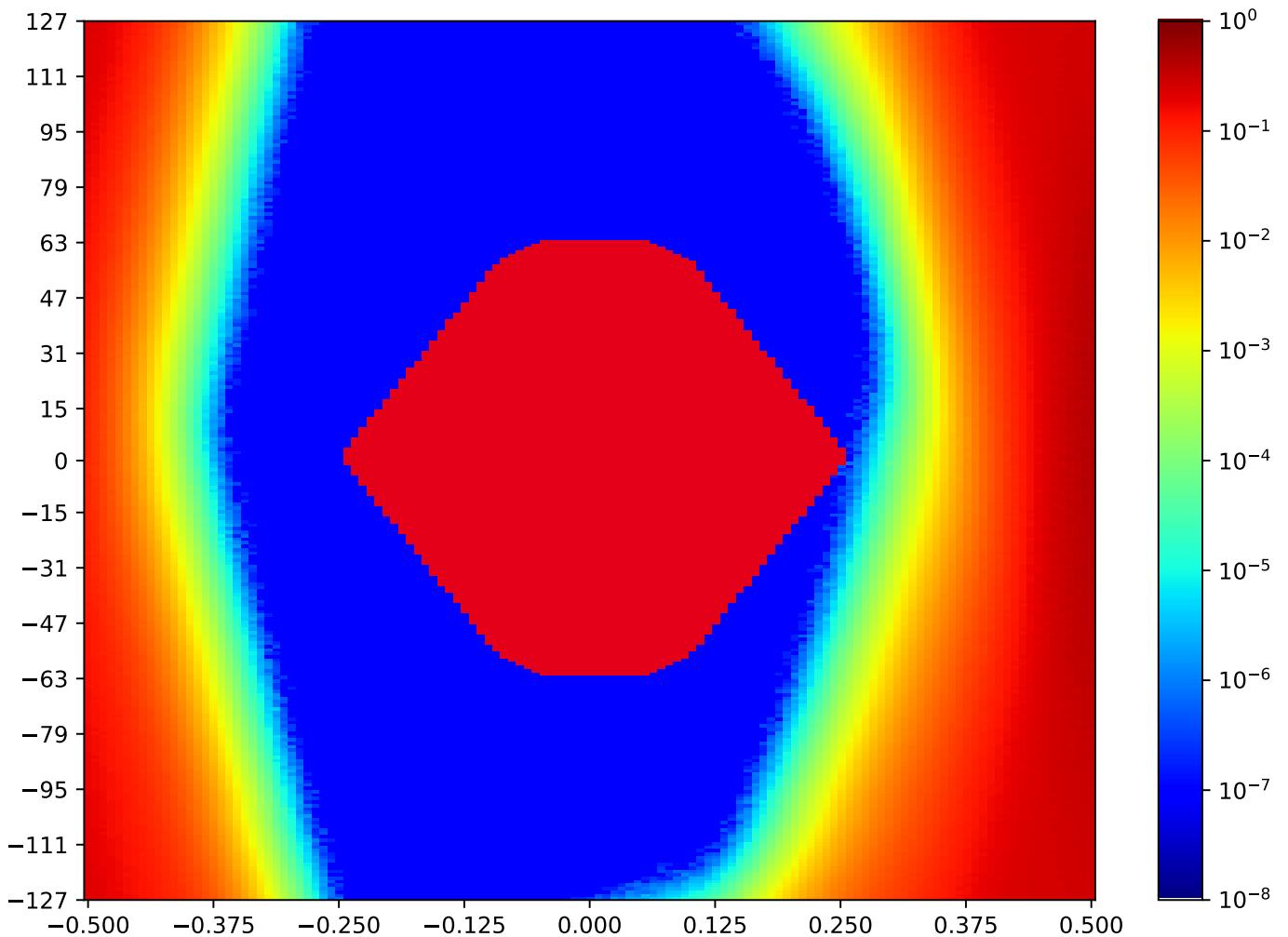


Figure 3.216: MSP_C_FPGA-TX3-01-RX2-01-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.3 MSP_C_FPGA-TX3-02-RX2-02-MSP_A_FPGA

Table 3.200: MSP_C_FPGA-TX3-02-RX2-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:16:58		2018-Jan-24 01:17:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17918	83	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

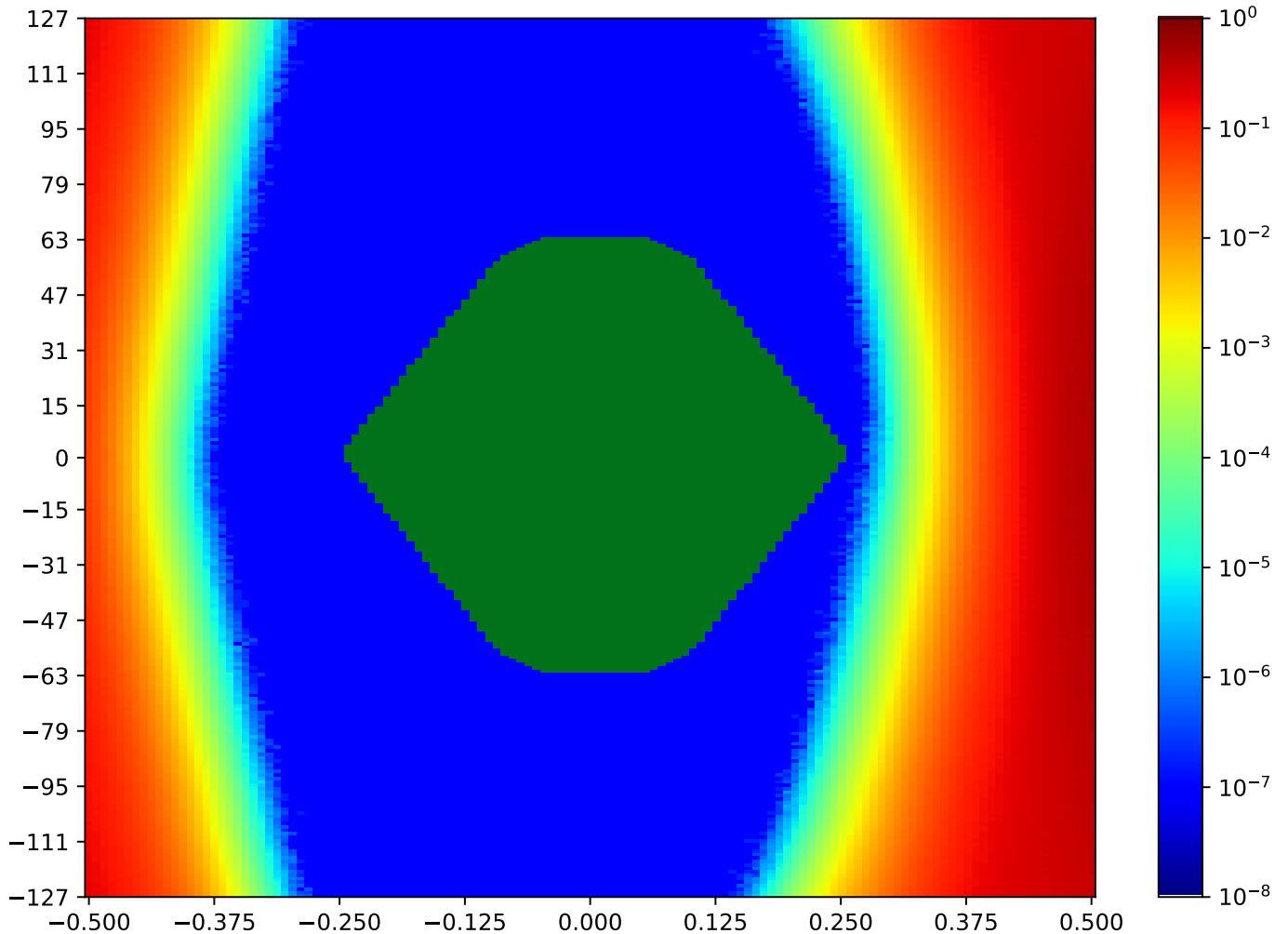


Figure 3.217: MSP_C_FPGA-TX3-02-RX2-02-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.4 MSP_C_FPGA-TX3-03-RX2-03-MSP_A_FPGA

Table 3.201: MSP_C_FPGA-TX3-03-RX2-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:13:25		2018-Jan-24 01:14:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18307	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

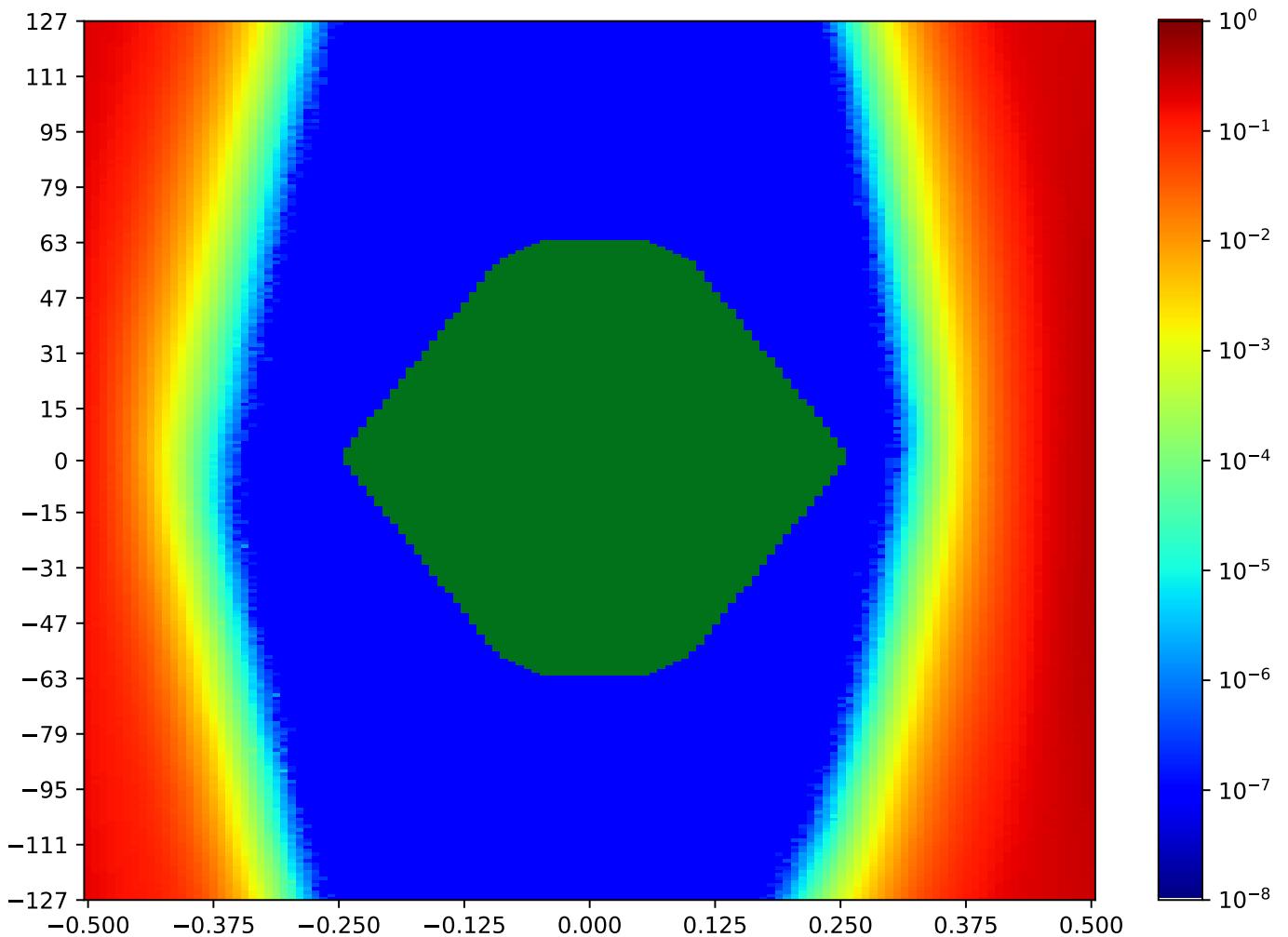


Figure 3.218: MSP_C_FPGA-TX3-03-RX2-03-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.5 MSP_C_FPGA-TX3-04-RX2-04-MSP_A_FPGA

Table 3.202: MSP_C_FPGA-TX3-04-RX2-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:19:06		2018-Jan-24 01:19:49	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18110	85	65.89%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

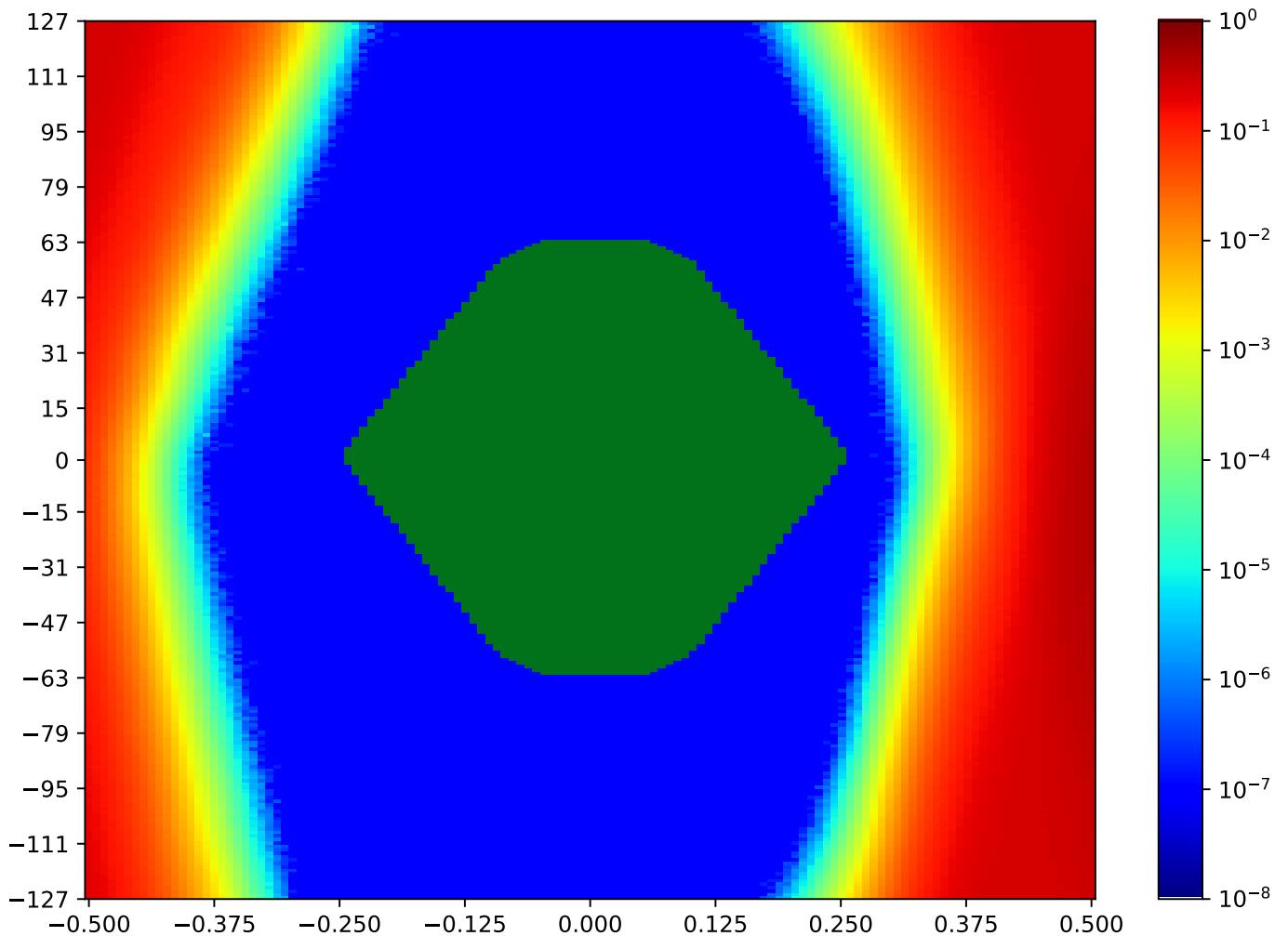


Figure 3.219: MSP_C_FPGA-TX3-04-RX2-04-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.6 MSP_C_FPGA-TX3-05-RX2-05-MSP_A_FPGA

Table 3.203: MSP_C_FPGA-TX3-05-RX2-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:12:42		2018-Jan-24 01:13:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16217	77	58.14%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

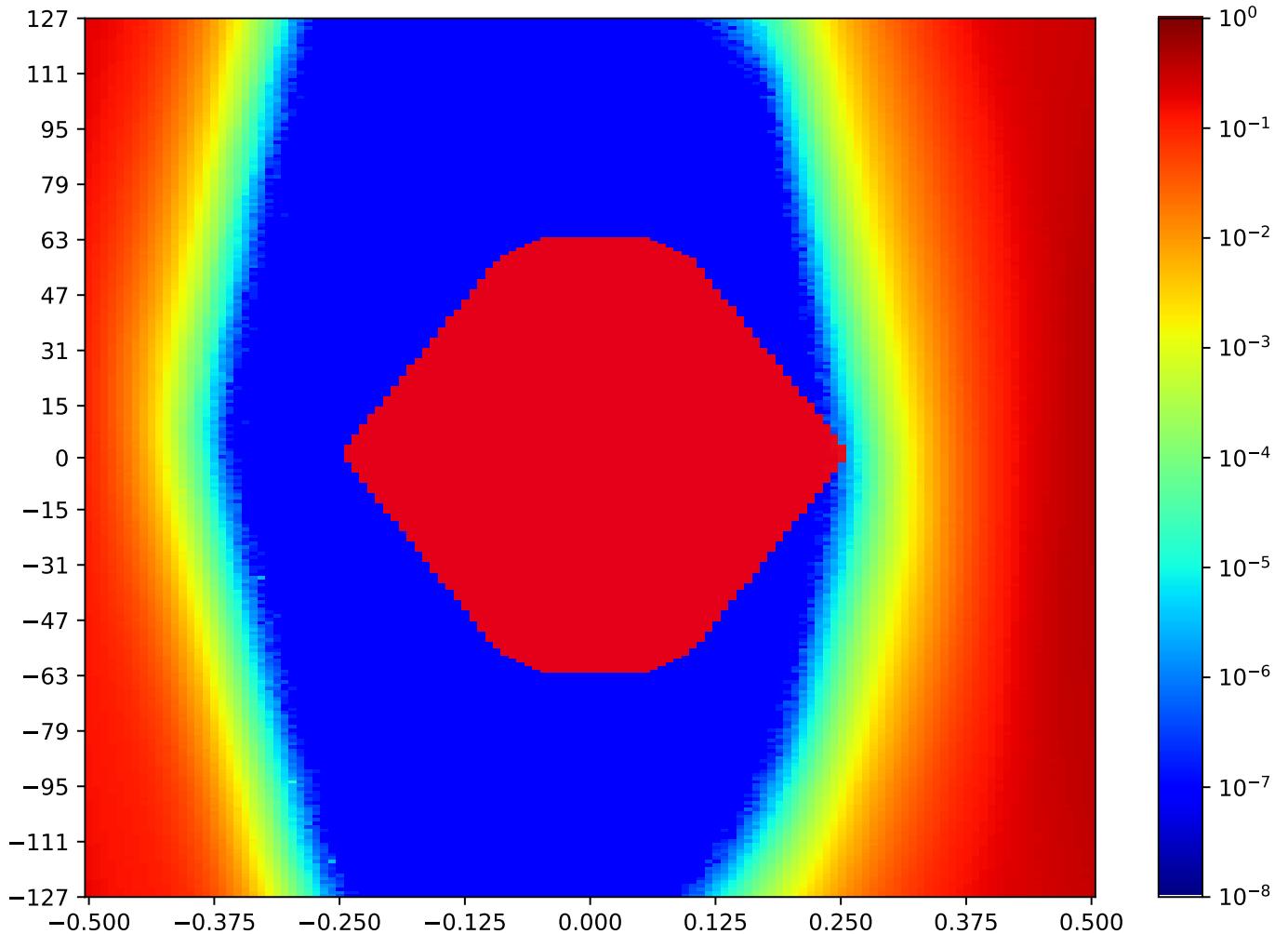


Figure 3.220: MSP_C_FPGA-TX3-05-RX2-05-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.7 MSP_C_FPGA-TX3-06-RX2-06-MSP_A_FPGA

Table 3.204: MSP_C_FPGA-TX3-06-RX2-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:20:32		2018-Jan-24 01:21:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17423	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

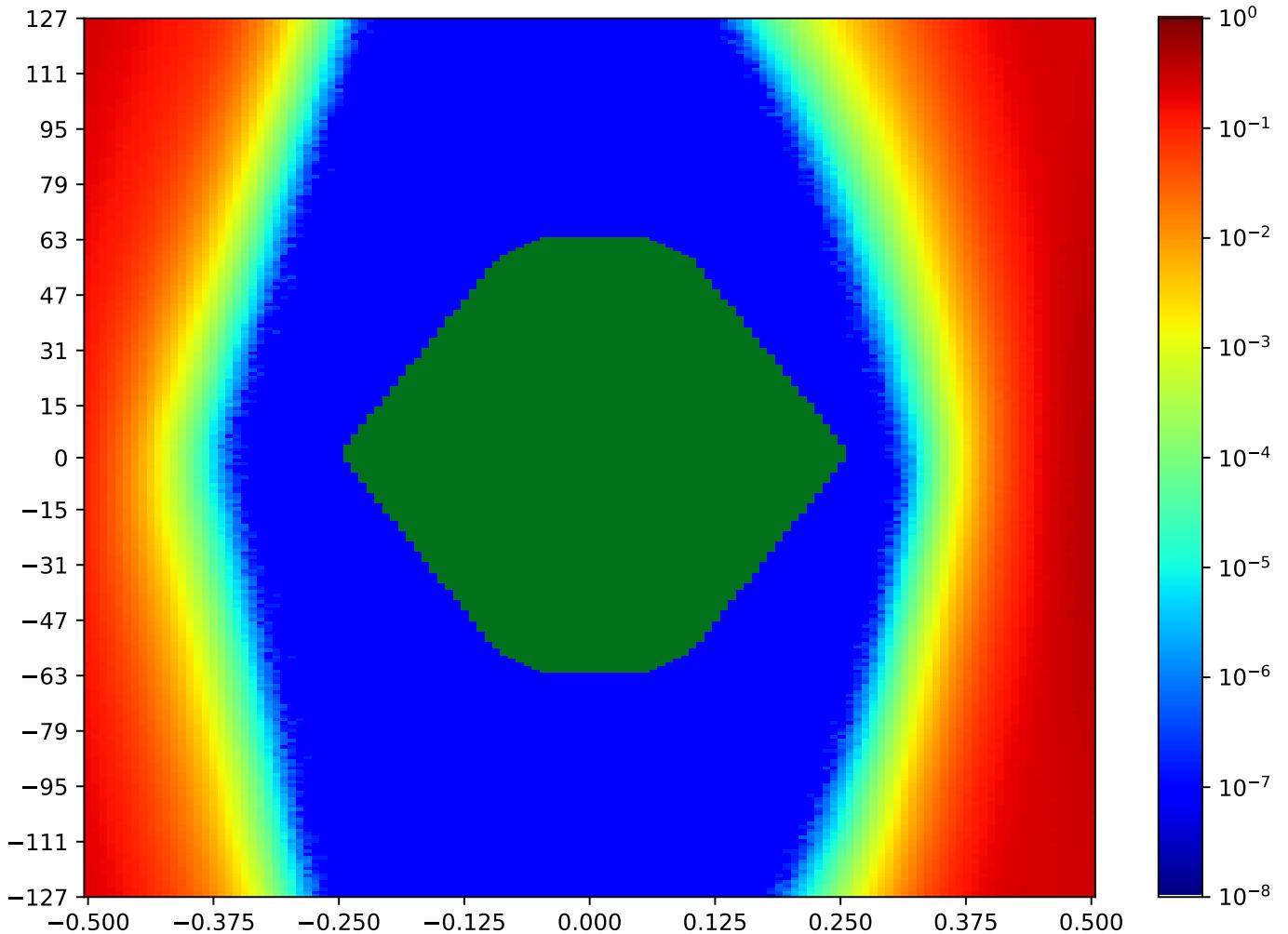


Figure 3.221: MSP_C_FPGA-TX3-06-RX2-06-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.8 MSP_C_FPGA-TX3-07-RX2-07-MSP_A_FPGA

Table 3.205: MSP_C_FPGA-TX3-07-RX2-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:14:07		2018-Jan-24 01:14:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17349	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

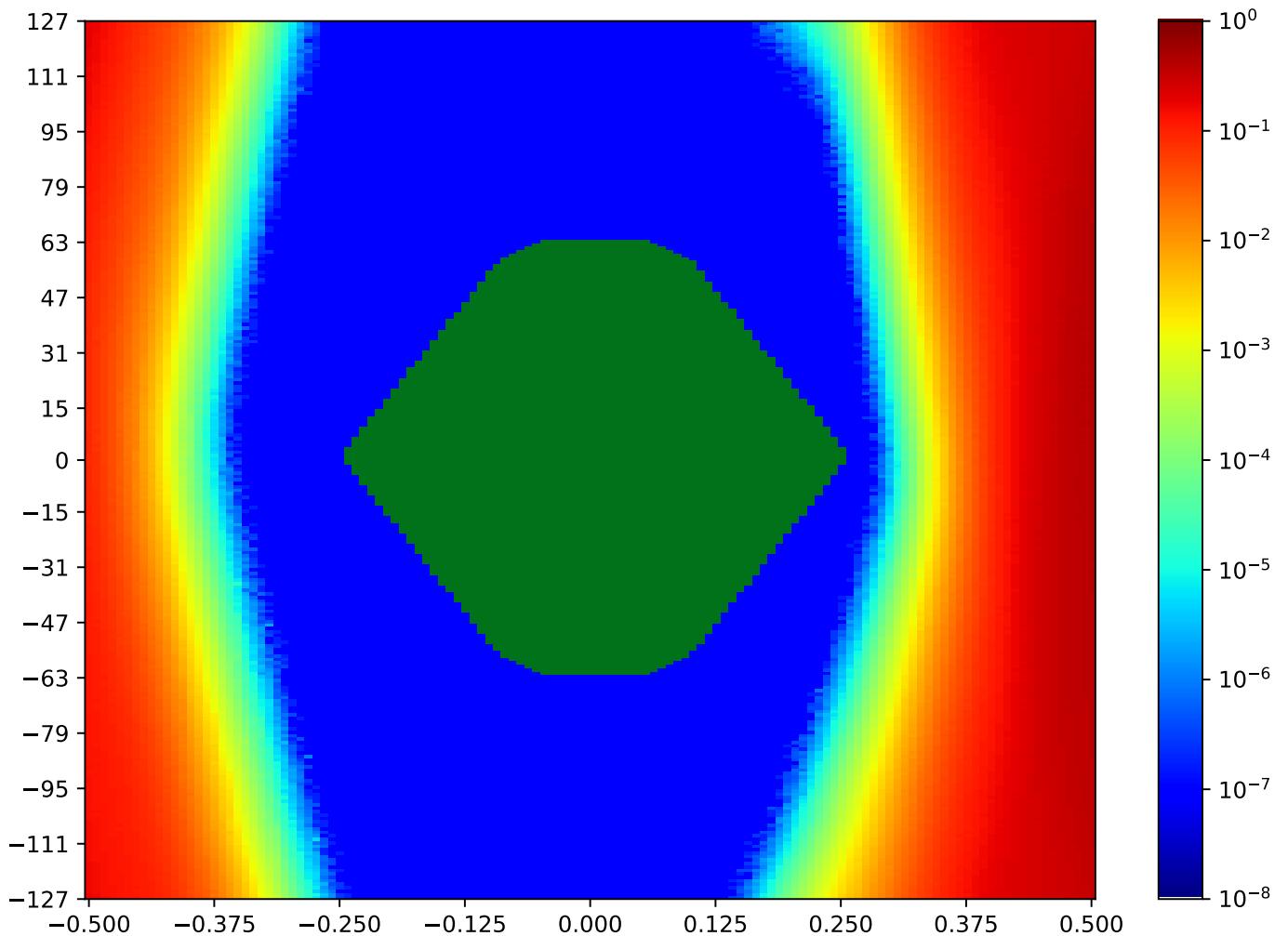


Figure 3.222: MSP_C_FPGA-TX3-07-RX2-07-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.9 MSP_C_FPGA-TX3-08-RX2-08-MSP_A_FPGA

Table 3.206: MSP_C_FPGA-TX3-08-RX2-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:19:49		2018-Jan-24 01:20:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17708	86	65.12%	252	97.25%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

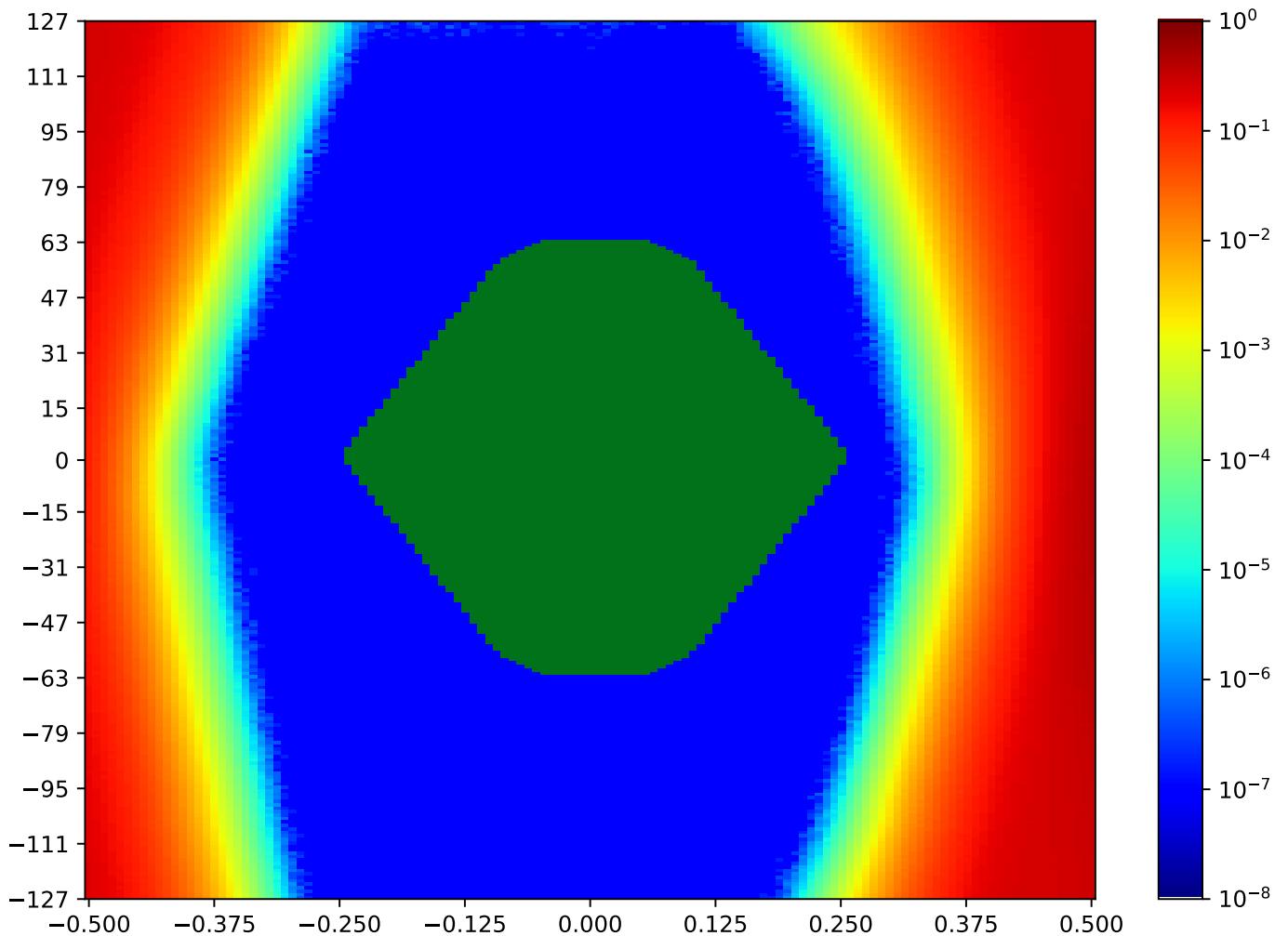


Figure 3.223: MSP_C_FPGA-TX3-08-RX2-08-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.10 MSP_C_FPGA-TX3-09-RX2-09-MSP_A_FPGA

Table 3.207: MSP_C_FPGA-TX3-09-RX2-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:15:33		2018-Jan-24 01:16:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16793	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

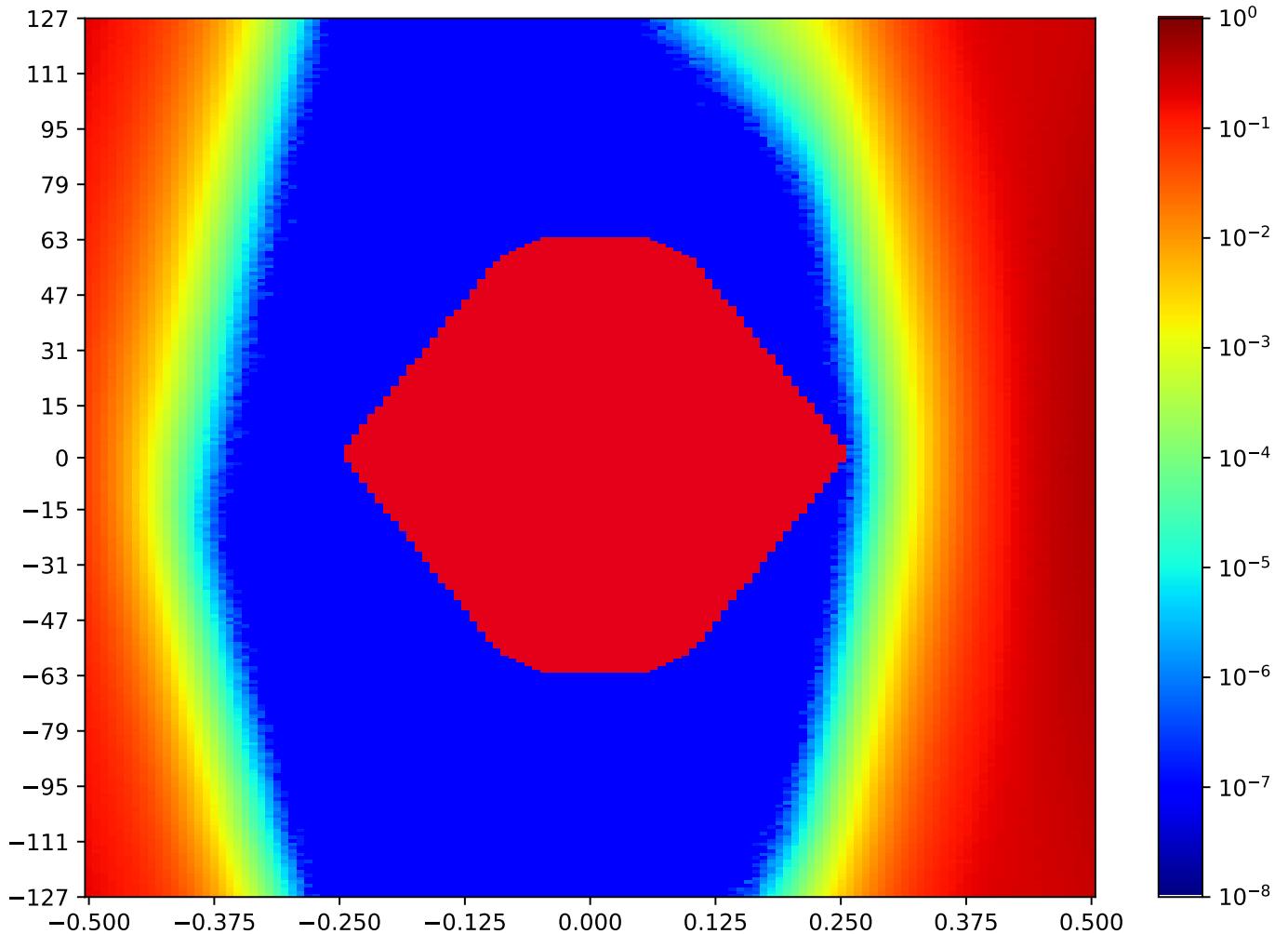


Figure 3.224: MSP_C_FPGA-TX3-09-RX2-09-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.11 MSP_C_FPGA-TX3-10-RX2-10-MSP_A_FPGA

Table 3.208: MSP_C_FPGA-TX3-10-RX2-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:18:23		2018-Jan-24 01:19:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16894	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

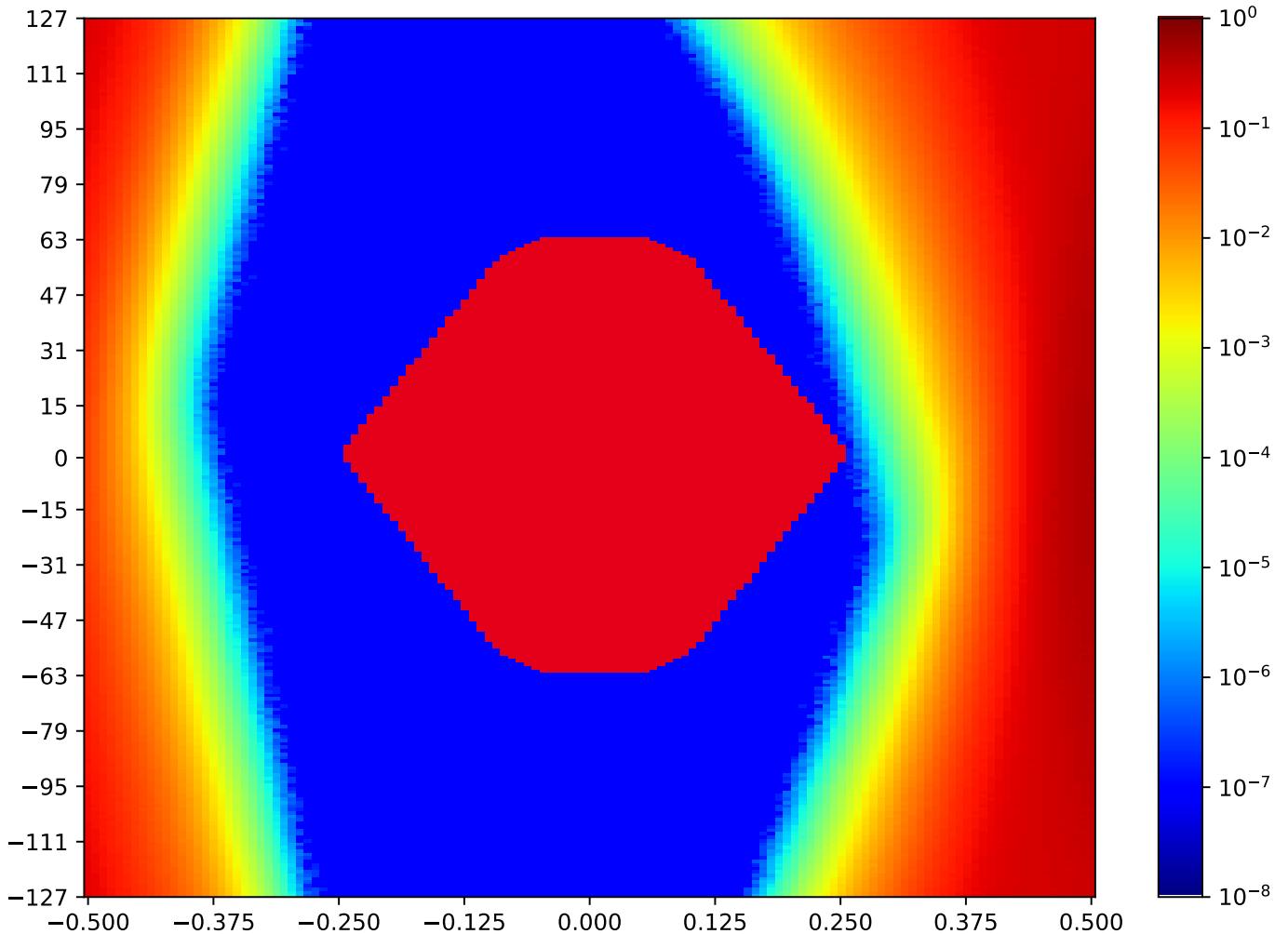


Figure 3.225: MSP_C_FPGA-TX3-10-RX2-10-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.17.12 MSP_C_FPGA-TX3-11-RX2-11-MSP_A_FPGA

Table 3.209: MSP_C_FPGA-TX3-11-RX2-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:17:41		2018-Jan-24 01:18:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17792	83	64.34%	254	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

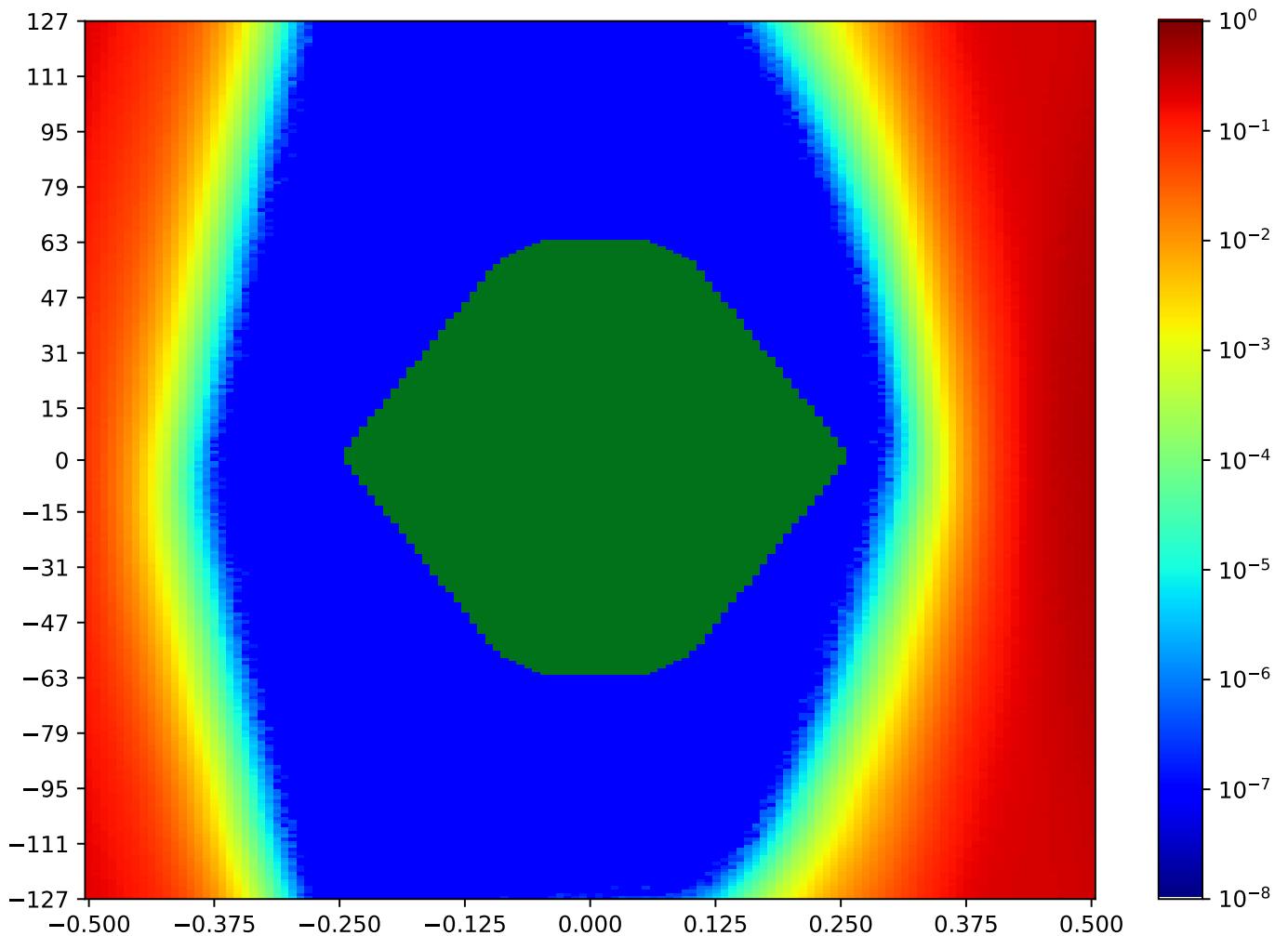


Figure 3.226: MSP_C_FPGA-TX3-11-RX2-11-MSP_A_FPGA

Call back to summary Figure 3.214. Sibling eye diagrams: V1-6.4.

3.18 MSP_C TX4 MSP_A RX1 Minipod Loopback

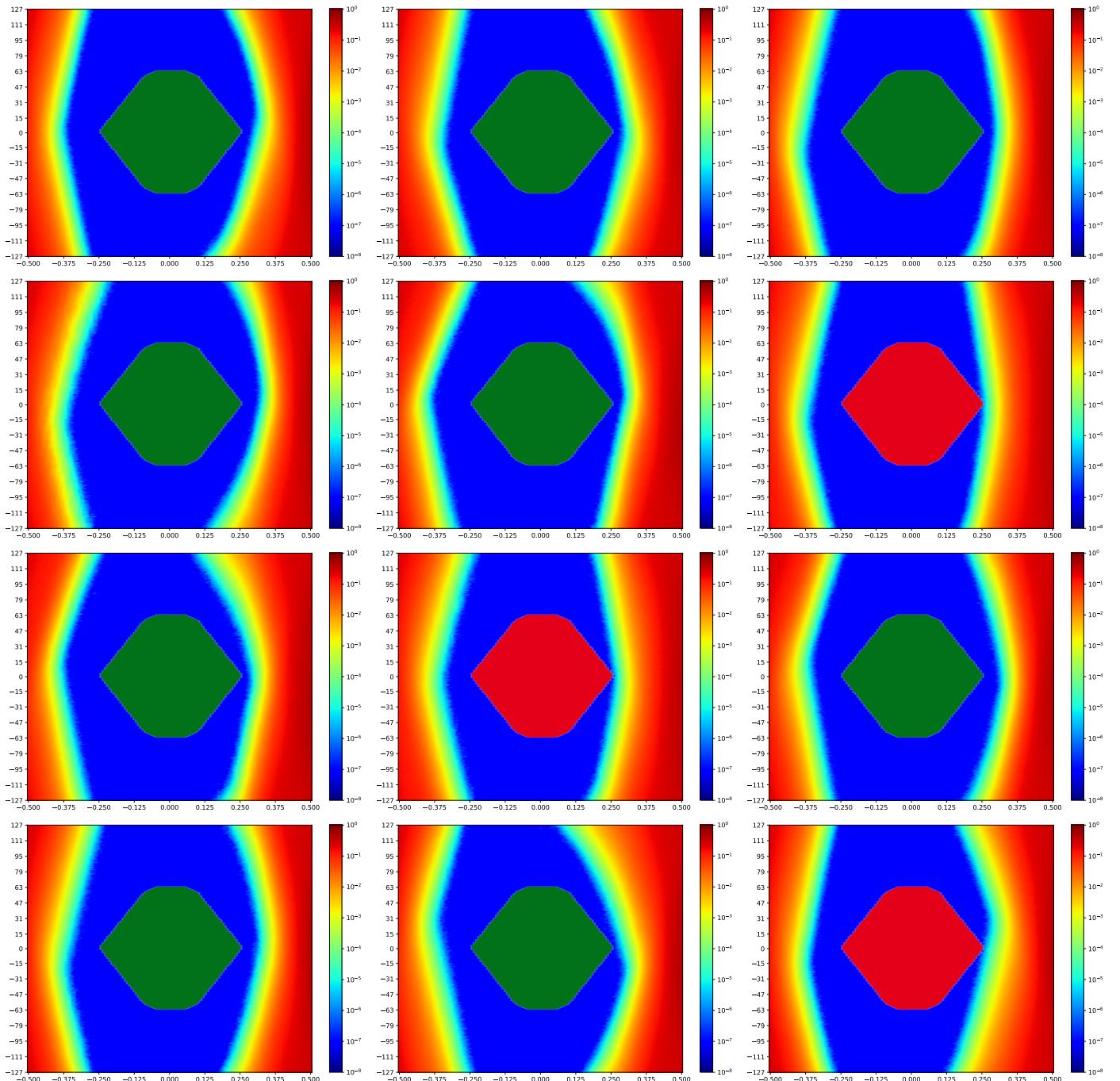


Figure 3.227: MSP_C TX4 MSP_A RX1 Minipod Loopback

A cross-reference to Figure 3.227. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.240.

3.18.1 MSP_C_FPGA-TX4-00-RX1-00-MSP_A_FPGA

Table 3.210: MSP_C_FPGA-TX4-00-RX1-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:23:23		2018-Jan-24 01:24:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17729	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

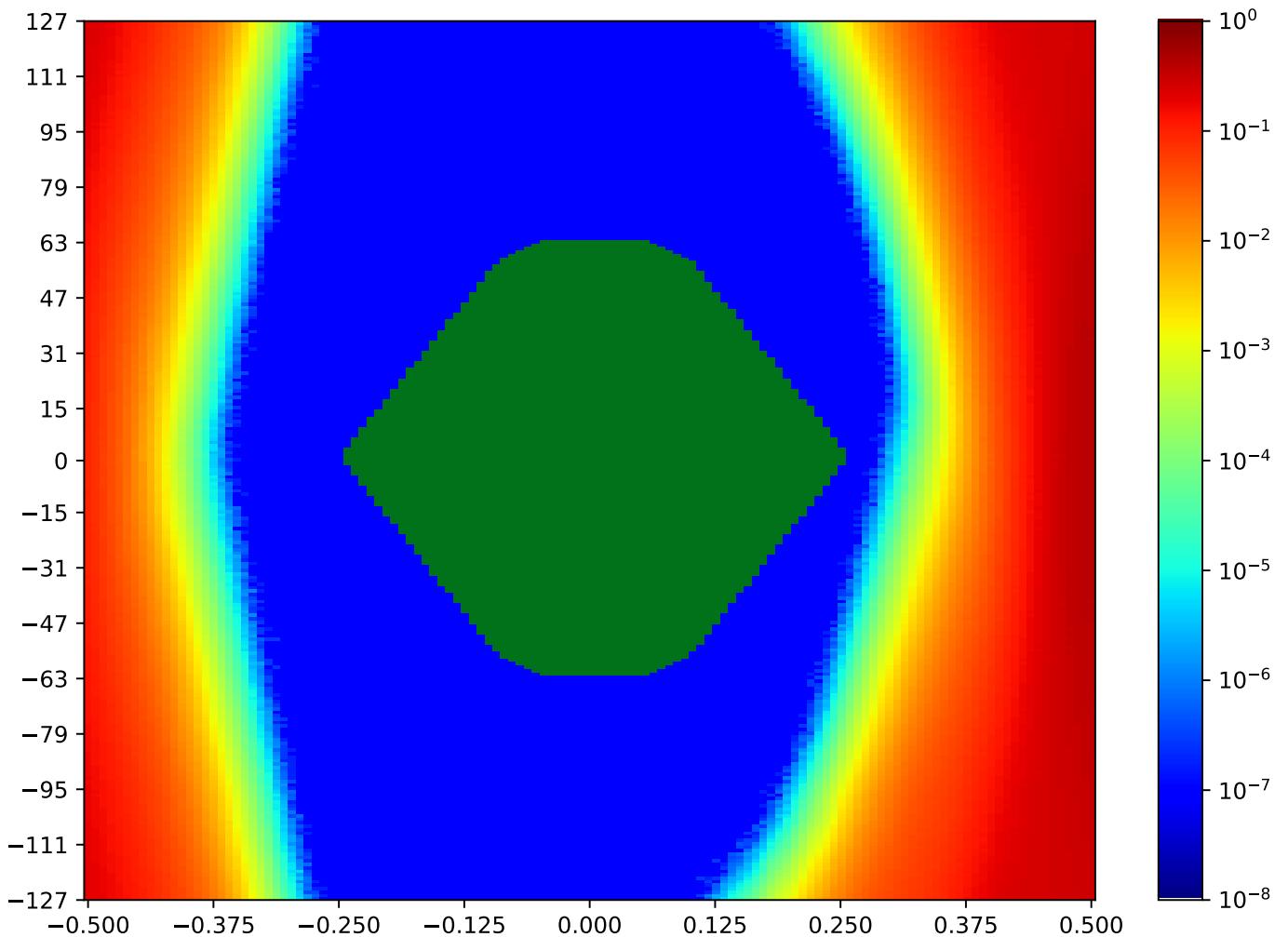


Figure 3.228: MSP_C_FPGA-TX4-00-RX1-00-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.2 MSP_C_FPGA-TX4-01-RX1-01-MSP_A_FPGA

Table 3.211: MSP_C_FPGA-TX4-01-RX1-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:21:57		2018-Jan-24 01:22:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16237	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

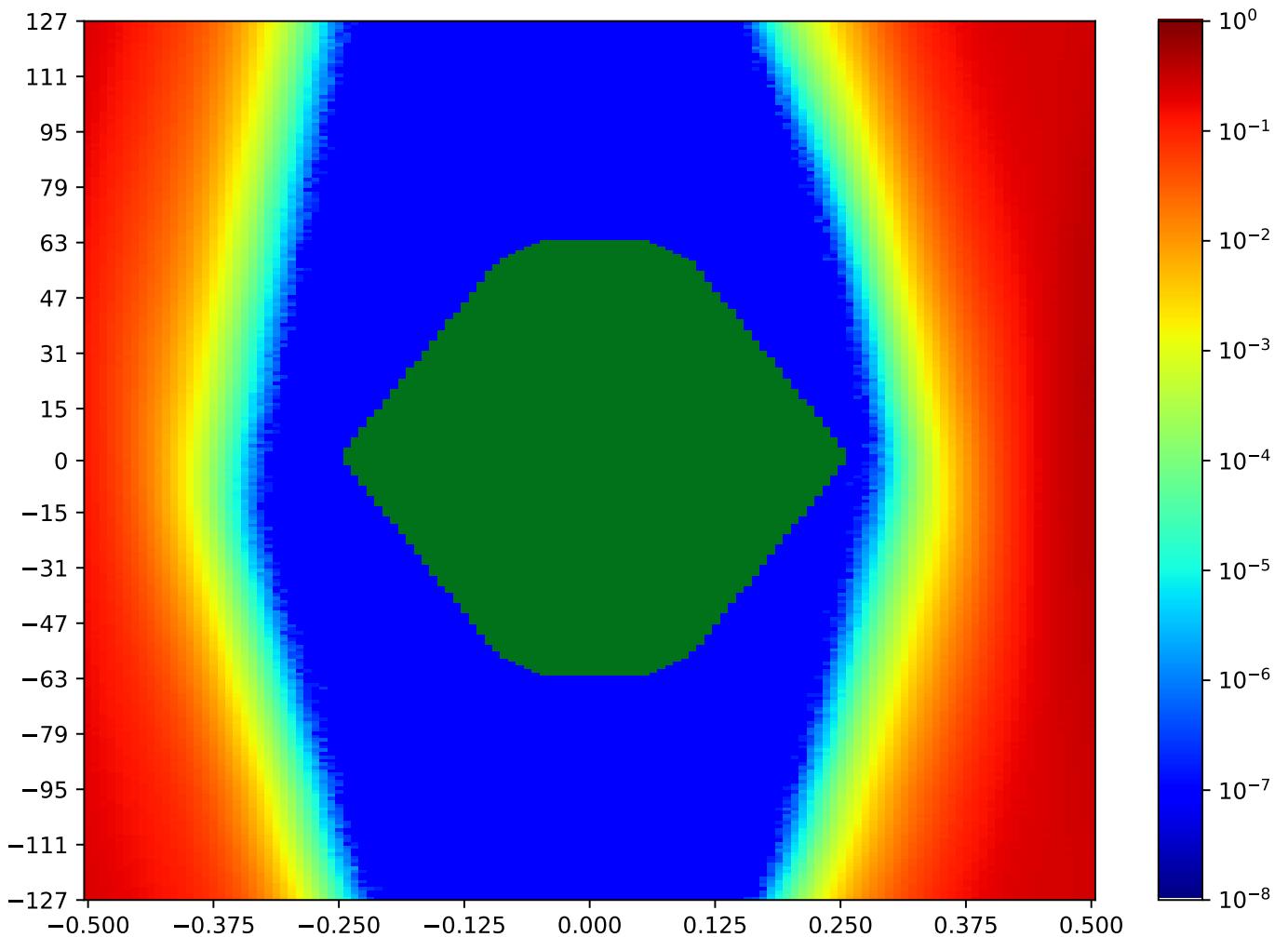


Figure 3.229: MSP_C_FPGA-TX4-01-RX1-01-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.3 MSP_C_FPGA-TX4-02-RX1-02-MSP_A_FPGA

Table 3.212: MSP_C_FPGA-TX4-02-RX1-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:25:30		2018-Jan-24 01:26:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17892	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

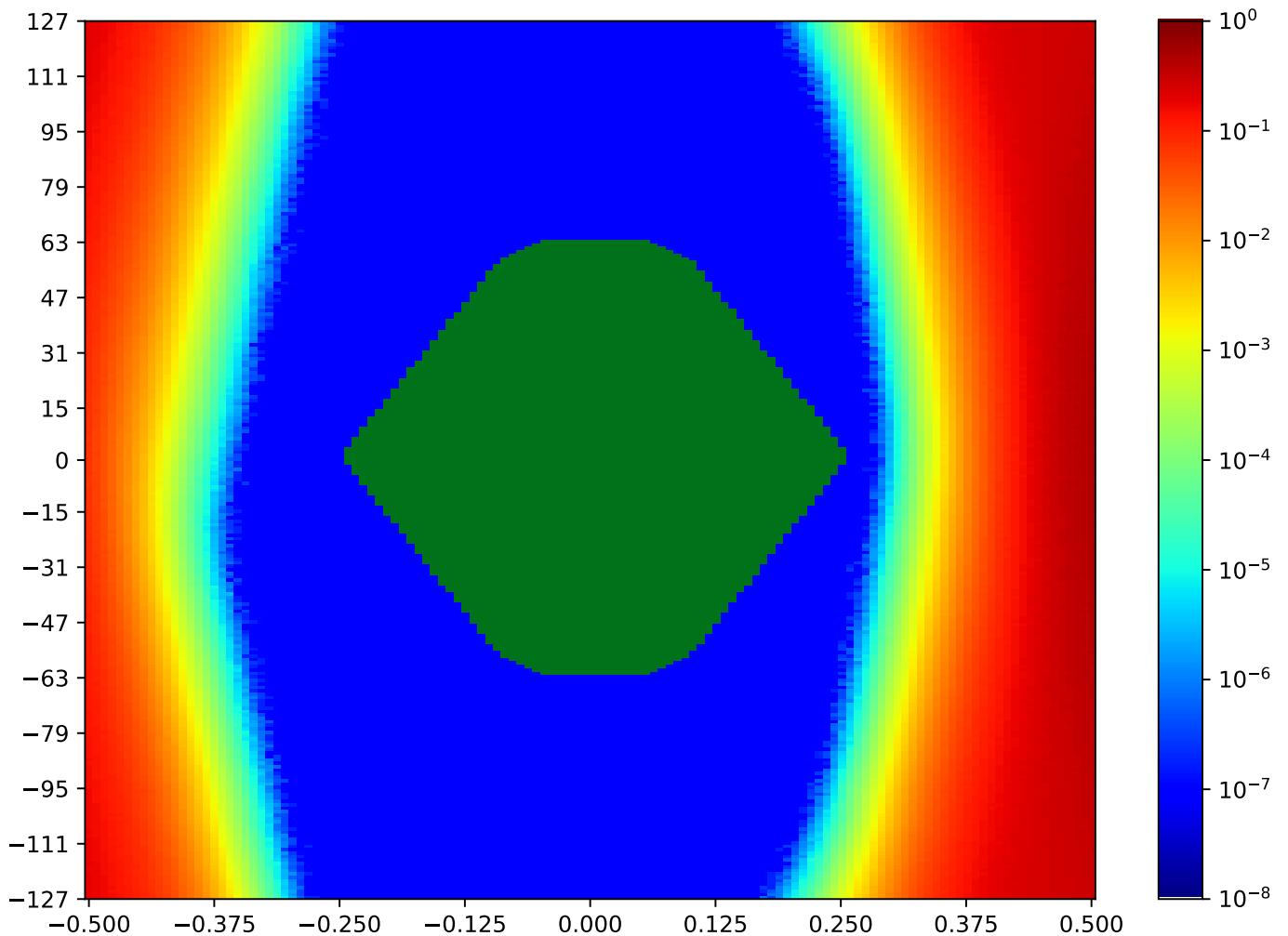


Figure 3.230: MSP_C_FPGA-TX4-02-RX1-02-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.4 MSP_C_FPGA-TX4-03-RX1-03-MSP_A_FPGA

Table 3.213: MSP_C_FPGA-TX4-03-RX1-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:21:15		2018-Jan-24 01:21:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17150	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

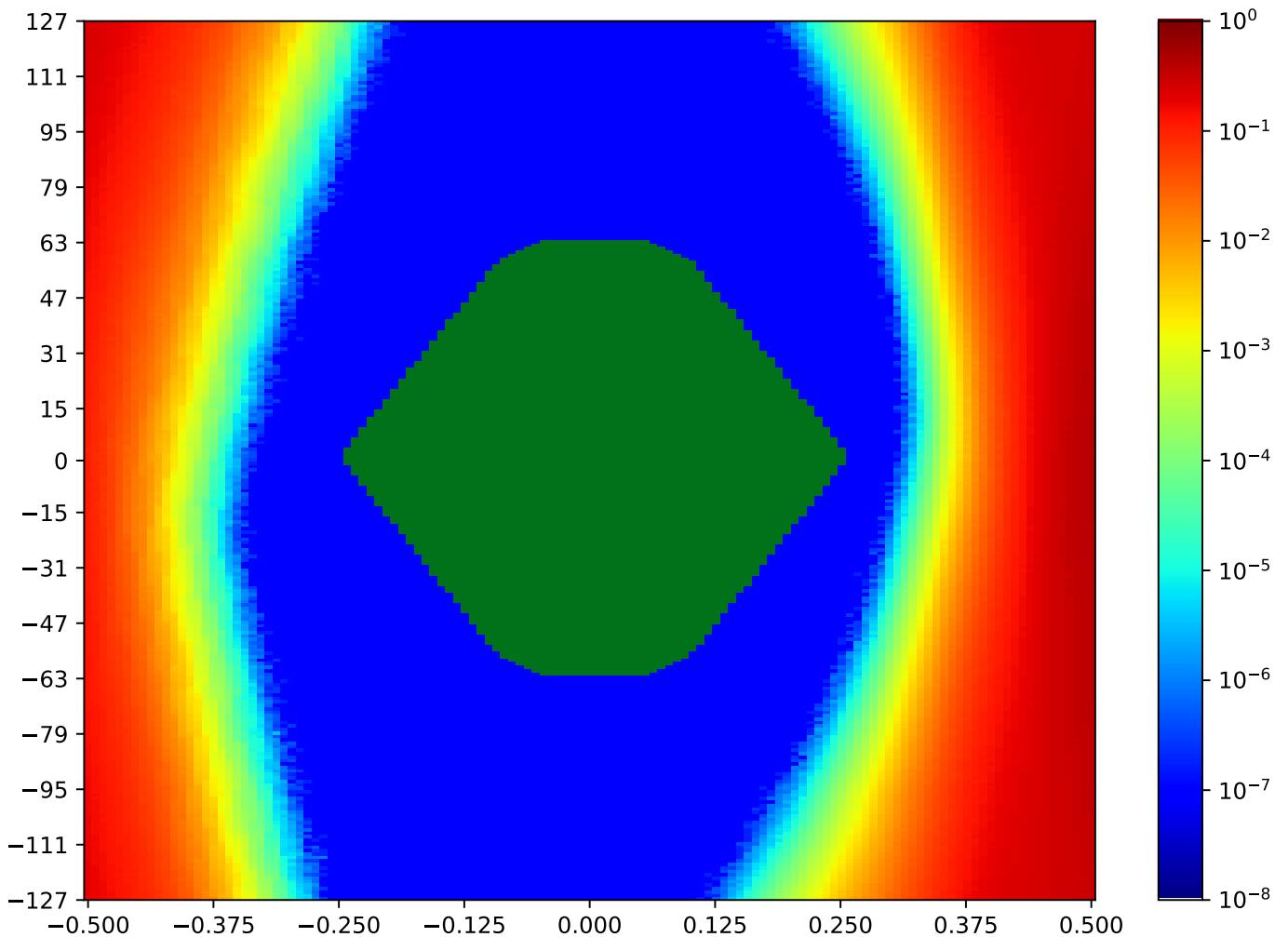


Figure 3.231: MSP_C_FPGA-TX4-03-RX1-03-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.5 MSP_C_FPGA-TX4-04-RX1-04-MSP_A_FPGA

Table 3.214: MSP_C_FPGA-TX4-04-RX1-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:27:37		2018-Jan-24 01:28:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17181	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

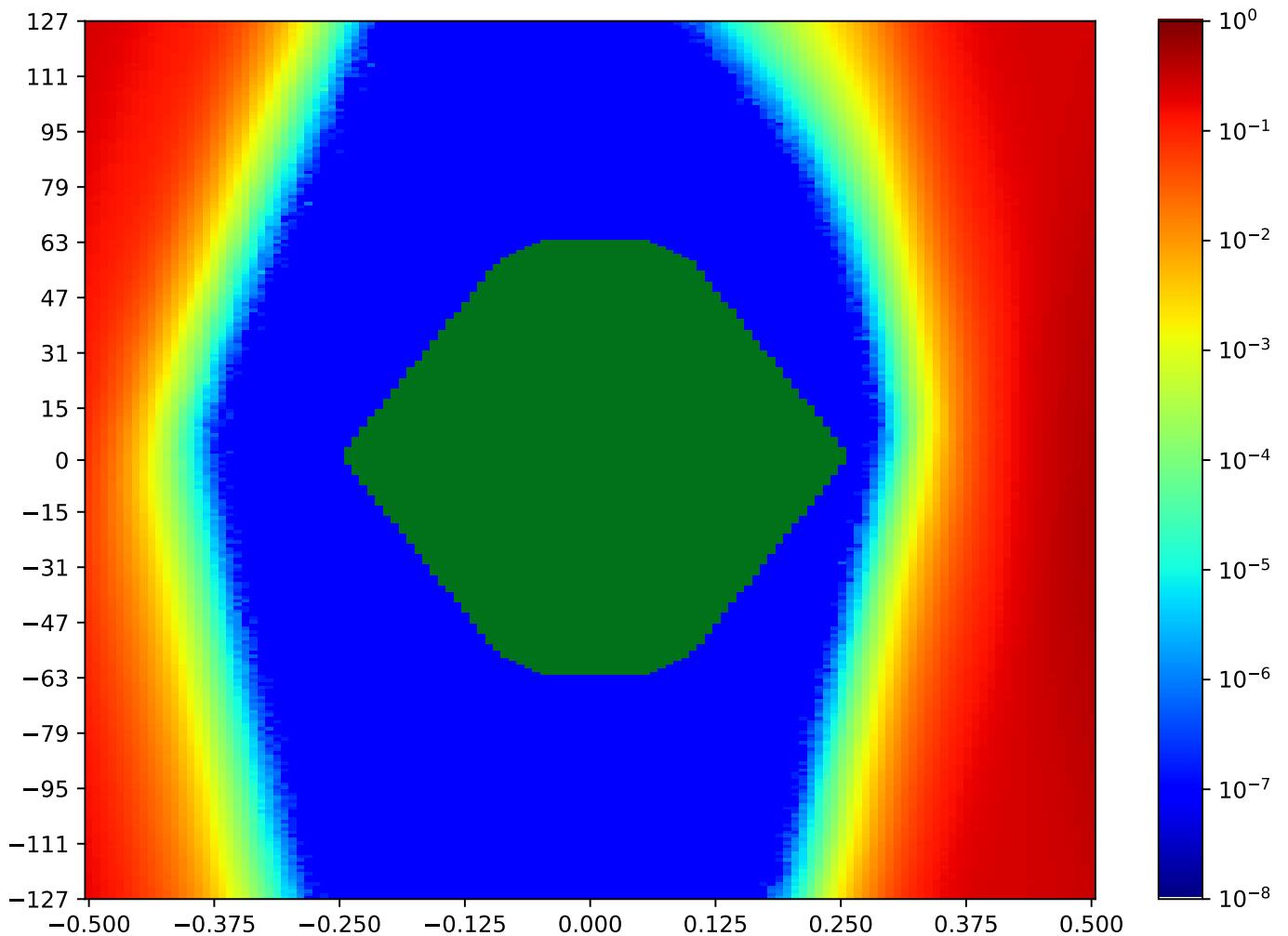


Figure 3.232: MSP_C_FPGA-TX4-04-RX1-04-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.6 MSP_C_FPGA-TX4-05-RX1-05-MSP_A_FPGA

Table 3.215: MSP_C_FPGA-TX4-05-RX1-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:22:40		2018-Jan-24 01:23:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16407	72	55.81%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

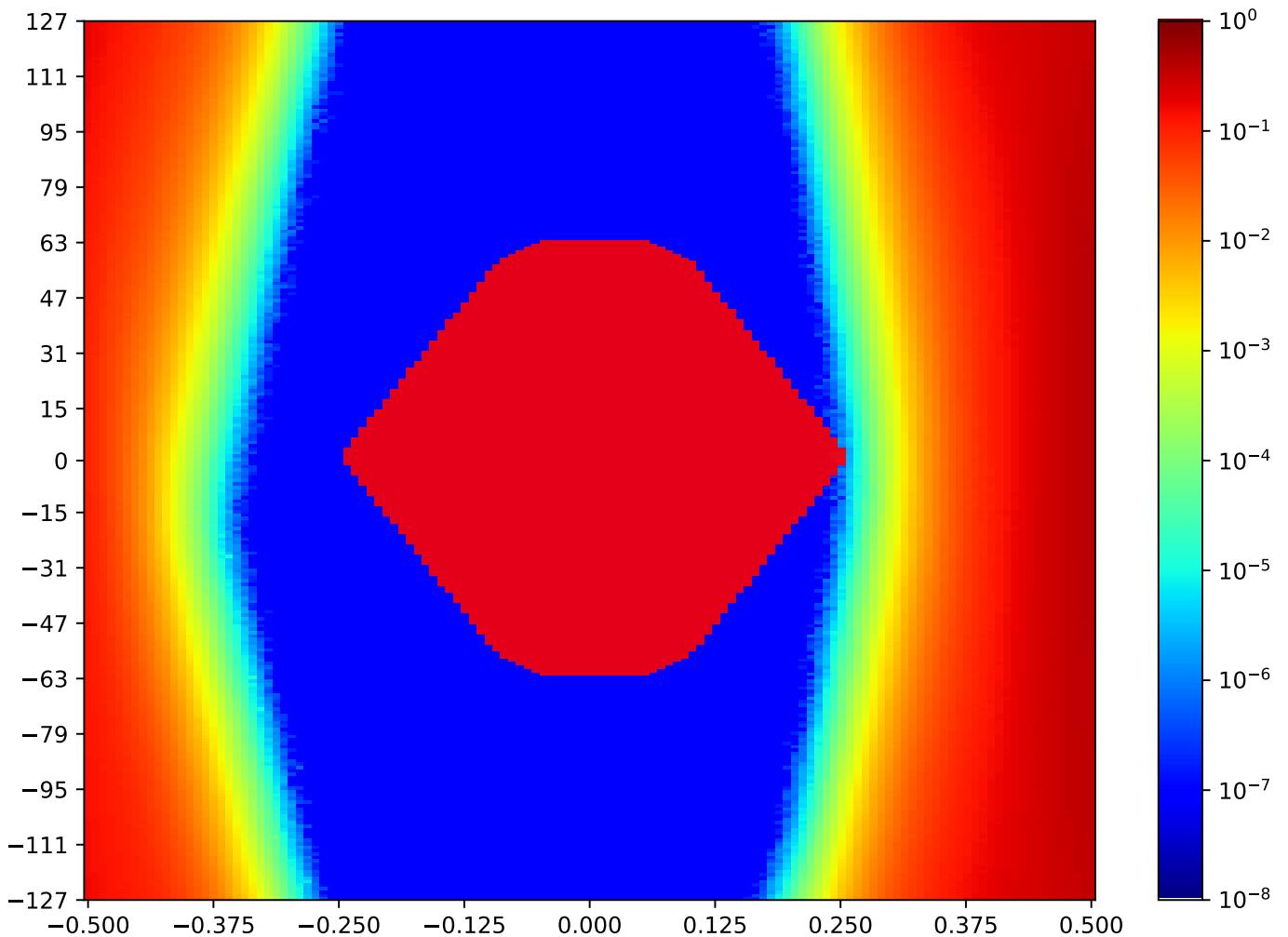


Figure 3.233: MSP_C_FPGA-TX4-05-RX1-05-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.7 MSP_C_FPGA-TX4-06-RX1-06-MSP_A_FPGA

Table 3.216: MSP_C_FPGA-TX4-06-RX1-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:29:02		2018-Jan-24 01:29:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16495	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

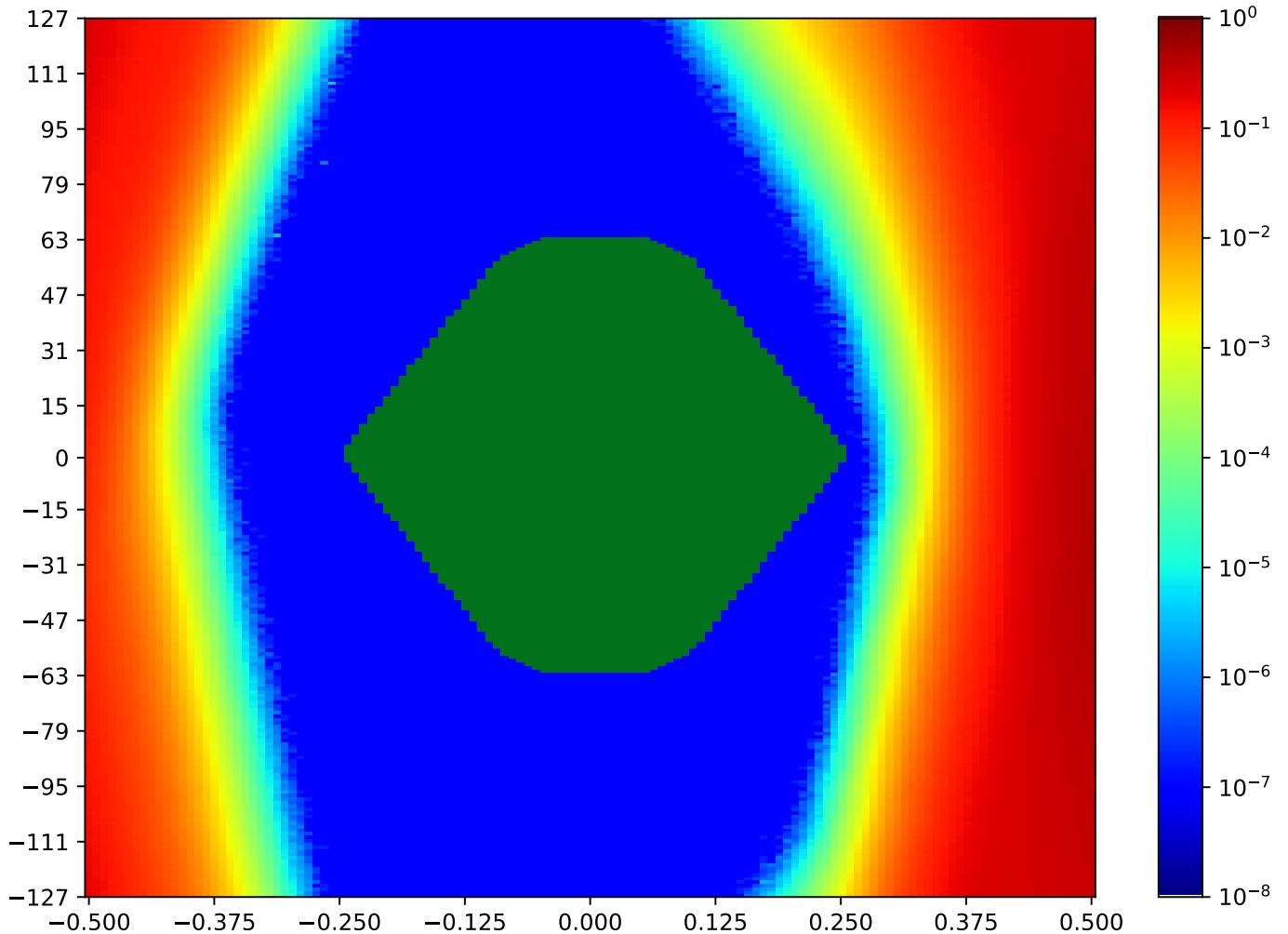


Figure 3.234: MSP_C_FPGA-TX4-06-RX1-06-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.8 MSP_C_FPGA-TX4-07-RX1-07-MSP_A_FPGA

Table 3.217: MSP_C_FPGA-TX4-07-RX1-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:24:05		2018-Jan-24 01:24:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15499	72	55.81%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

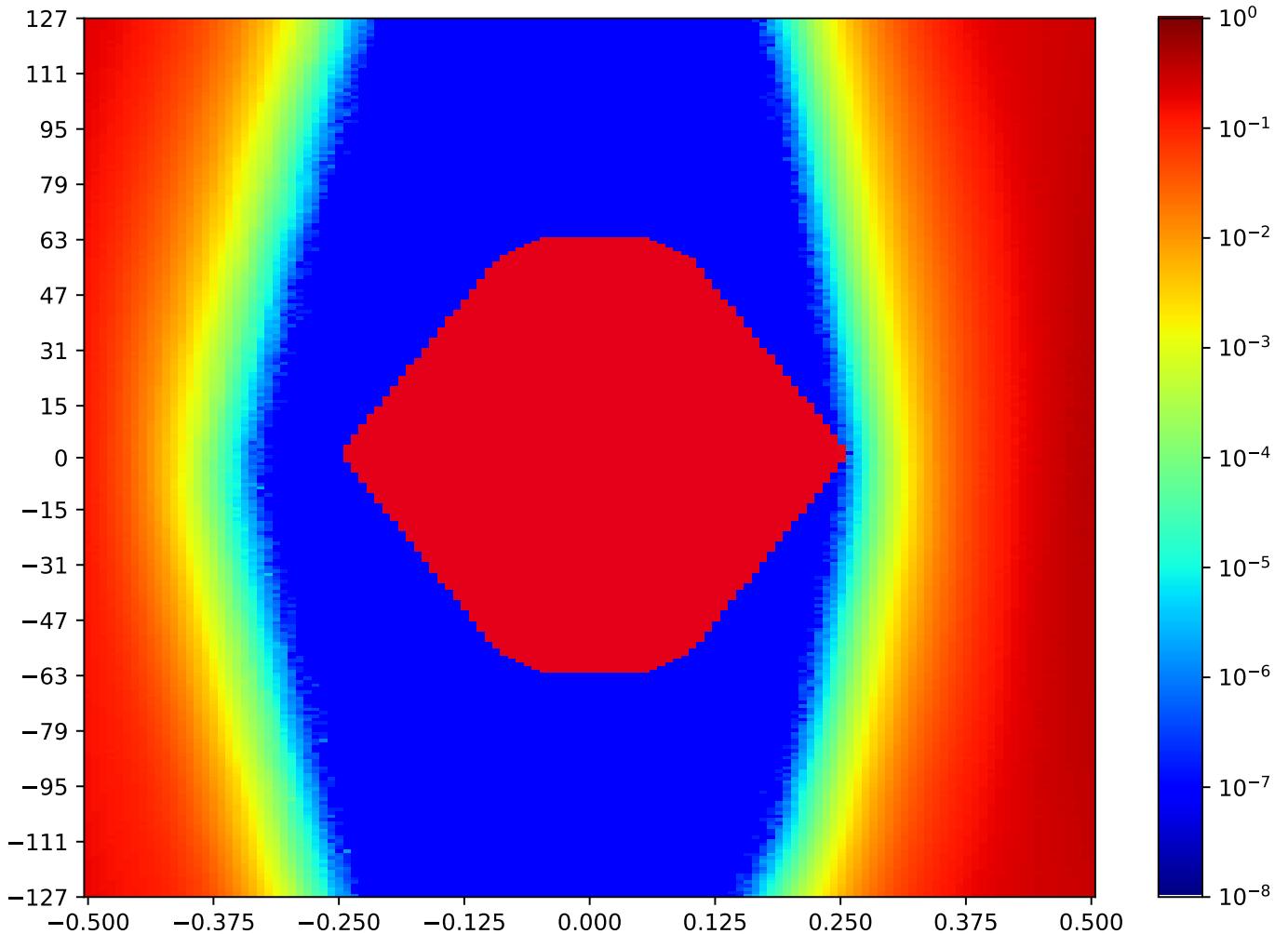


Figure 3.235: MSP_C_FPGA-TX4-07-RX1-07-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.9 MSP_C_FPGA-TX4-08-RX1-08-MSP_A_FPGA

Table 3.218: MSP_C_FPGA-TX4-08-RX1-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:28:19		2018-Jan-24 01:29:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17418	80	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

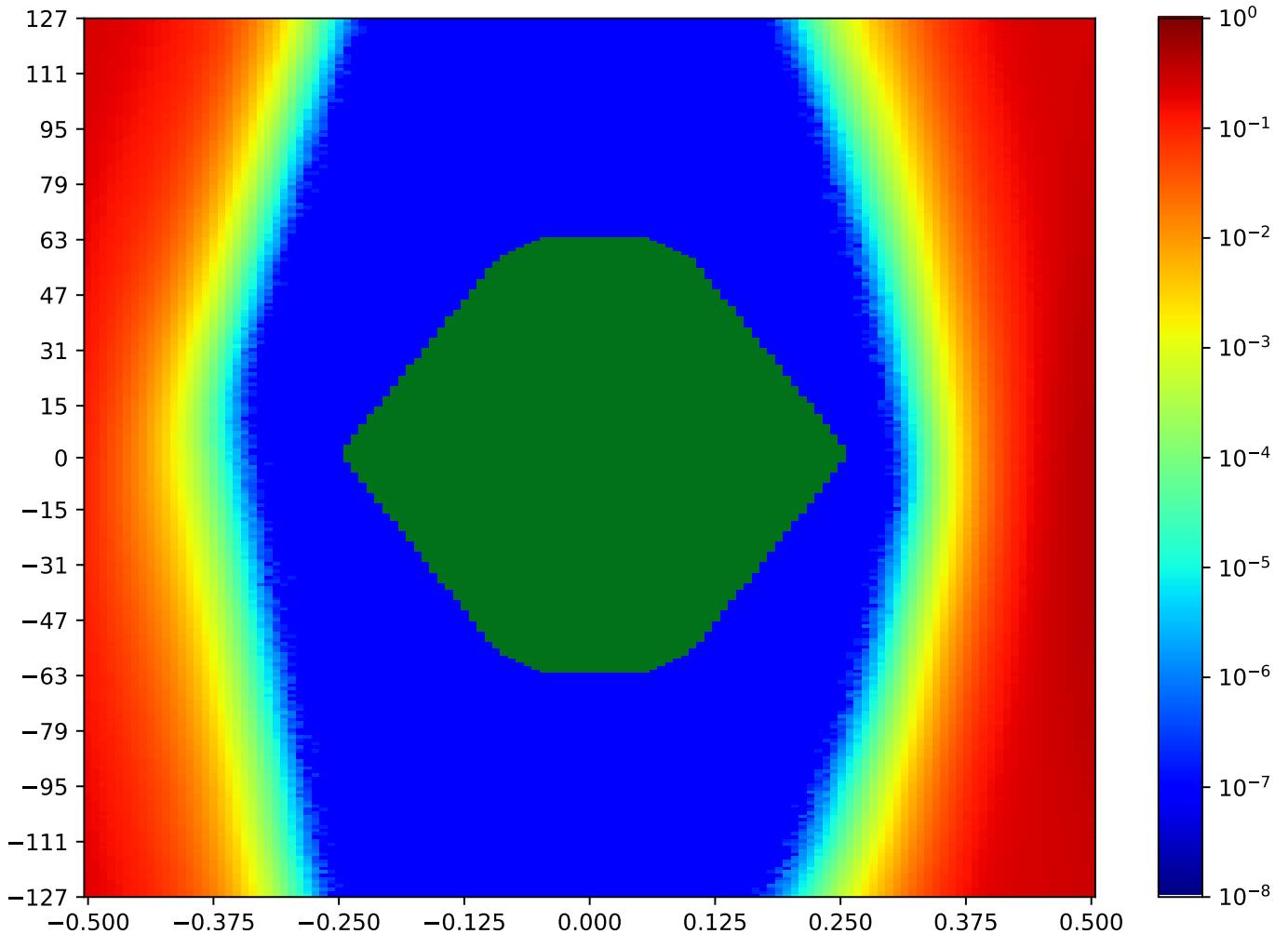


Figure 3.236: MSP_C_FPGA-TX4-08-RX1-08-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.10 MSP_C_FPGA-TX4-09-RX1-09-MSP_A_FPGA

Table 3.219: MSP_C_FPGA-TX4-09-RX1-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:24:48		2018-Jan-24 01:25:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17442	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

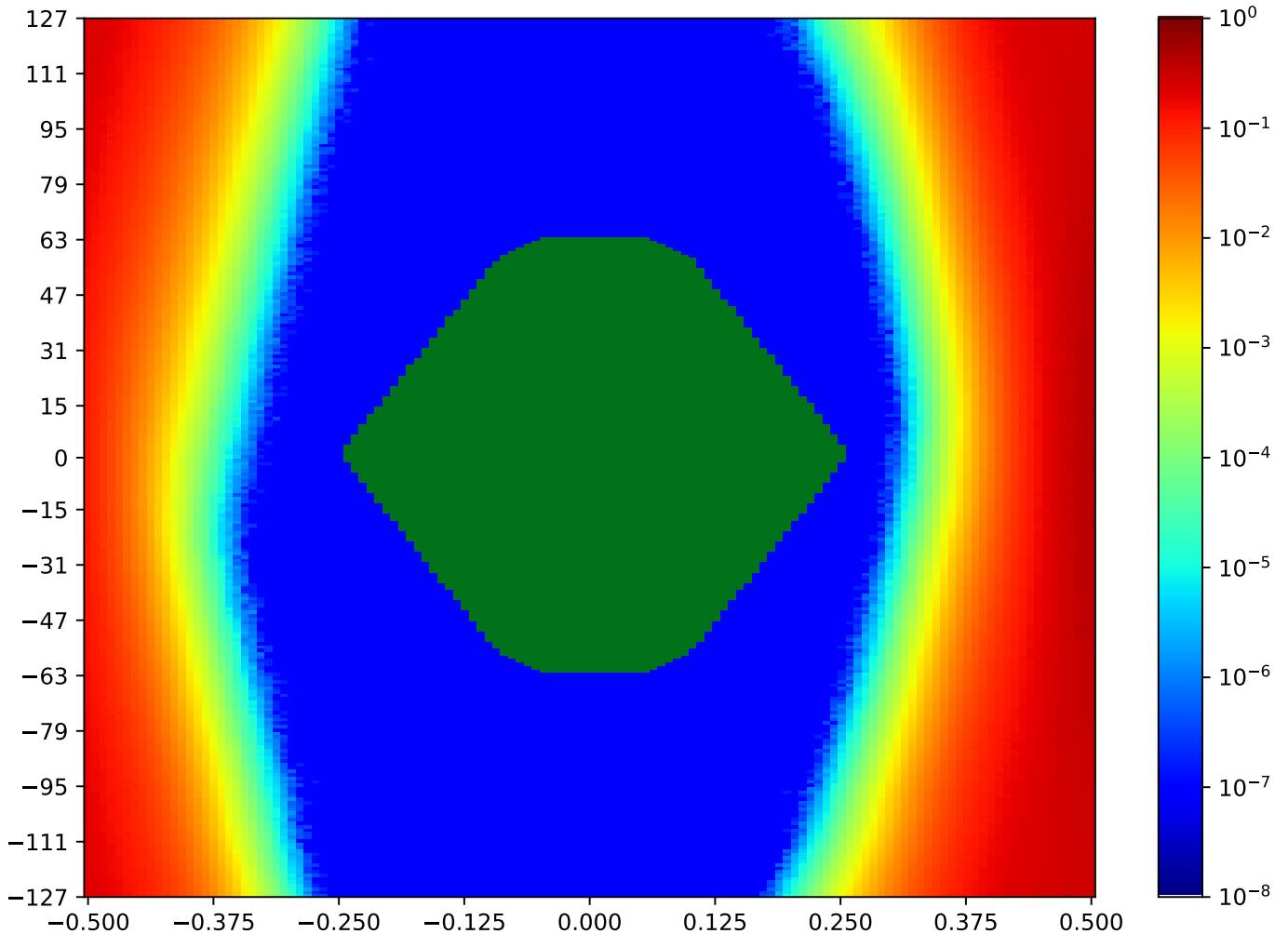


Figure 3.237: MSP_C_FPGA-TX4-09-RX1-09-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.11 MSP_C_FPGA-TX4-10-RX1-10-MSP_A_FPGA

Table 3.220: MSP_C_FPGA-TX4-10-RX1-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:26:55		2018-Jan-24 01:27:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15751	74	55.81%	250	98.04%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

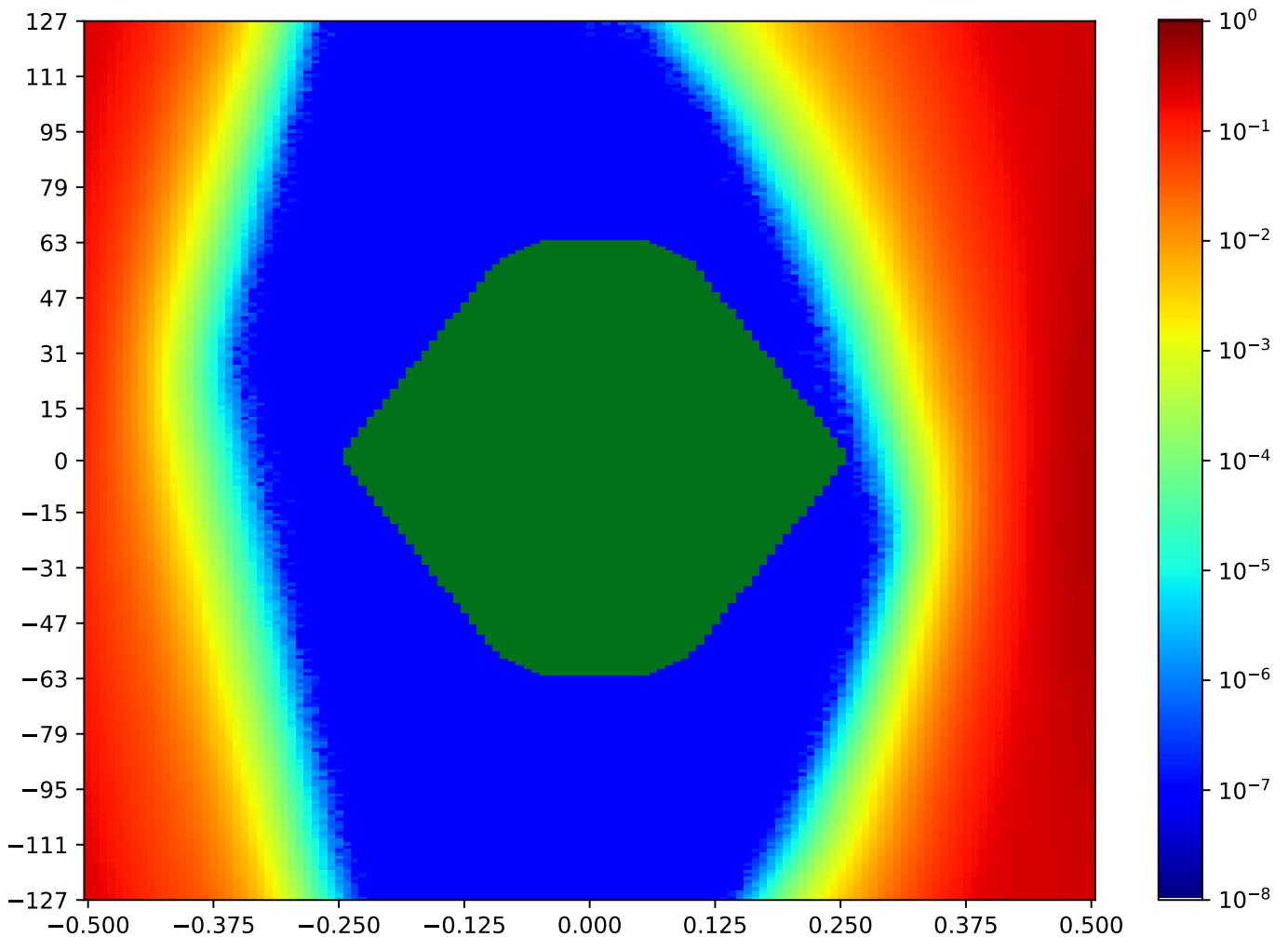


Figure 3.238: MSP_C_FPGA-TX4-10-RX1-10-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.18.12 MSP_C_FPGA-TX4-11-RX1-11-MSP_A_FPGA

Table 3.221: MSP_C_FPGA-TX4-11-RX1-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:26:12		2018-Jan-24 01:26:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16183	72	55.81%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

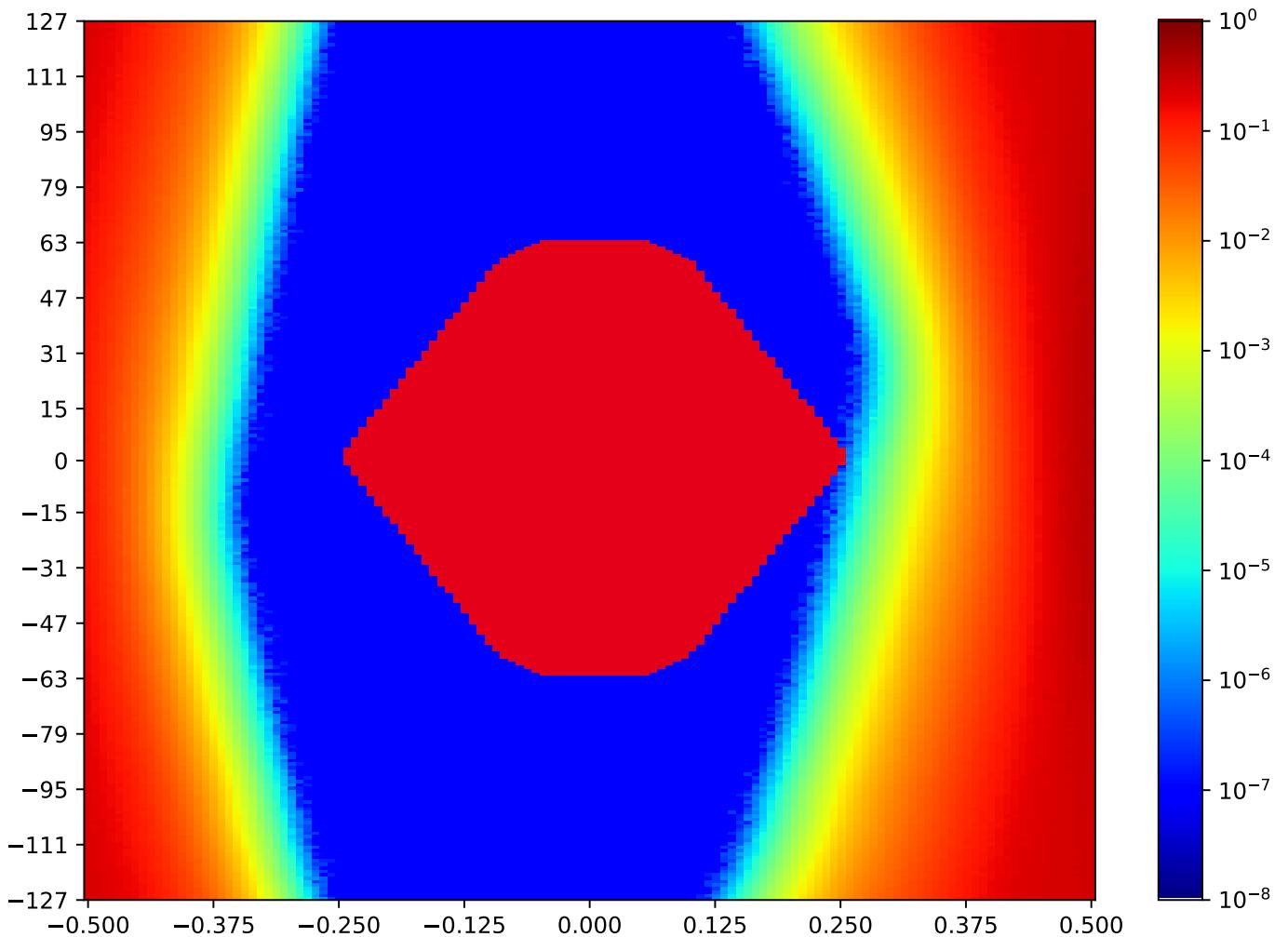


Figure 3.239: MSP_C_FPGA-TX4-11-RX1-11-MSP_A_FPGA

Call back to summary Figure 3.227. Sibling eye diagrams: V1-6.4.

3.19 MSP_A TX1 MSP_C RX13 Minipod Loopback

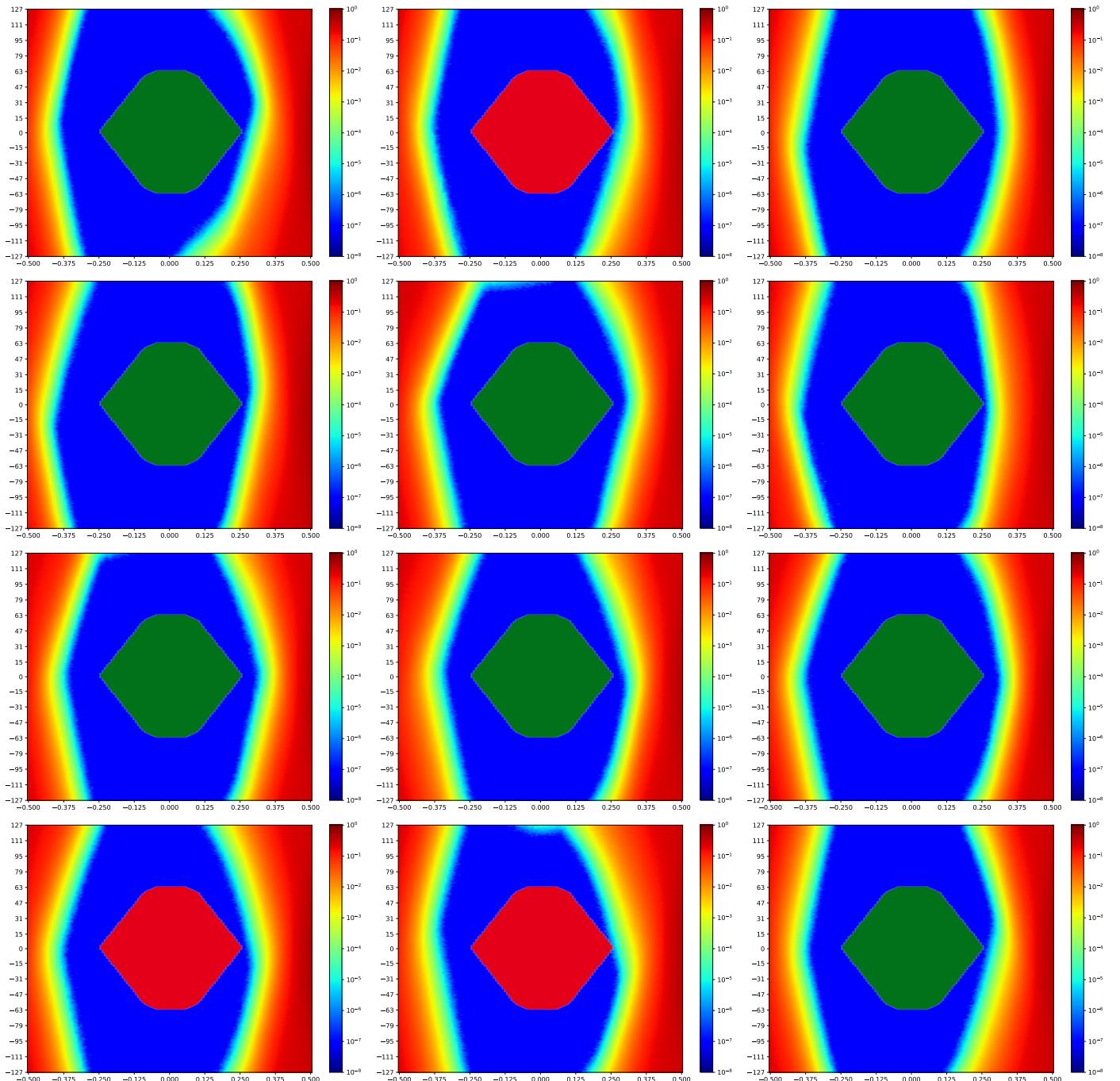


Figure 3.240: MSP_A TX1 MSP_C RX13 Minipod Loopback

A cross-reference to Figure 3.240. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.253.

3.19.1 MSP_A_FPGA-TX1-00-RX13-00-MSP_C_FPGA

Table 3.222: MSP_A_FPGA-TX1-00-RX13-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:39:55			2018-Jan-24 01:40:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	17182	81	62.79%	252	98.82%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0		

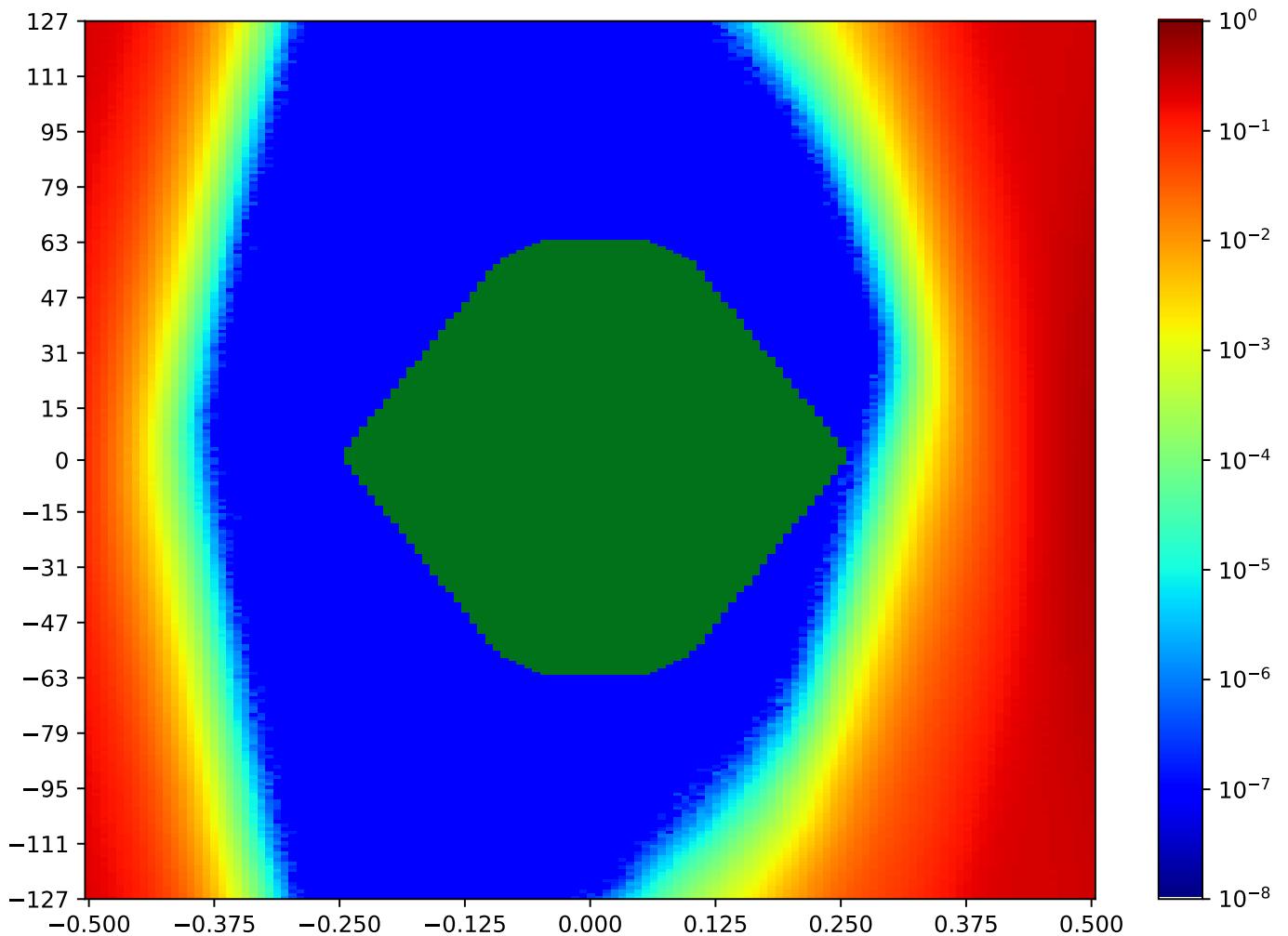


Figure 3.241: MSP_A_FPGA-TX1-00-RX13-00-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.2 MSP_A_FPGA-TX1-01-RX13-01-MSP_C_FPGA

Table 3.223: MSP_A_FPGA-TX1-01-RX13-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:41:19		2018-Jan-24 01:42:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16992	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

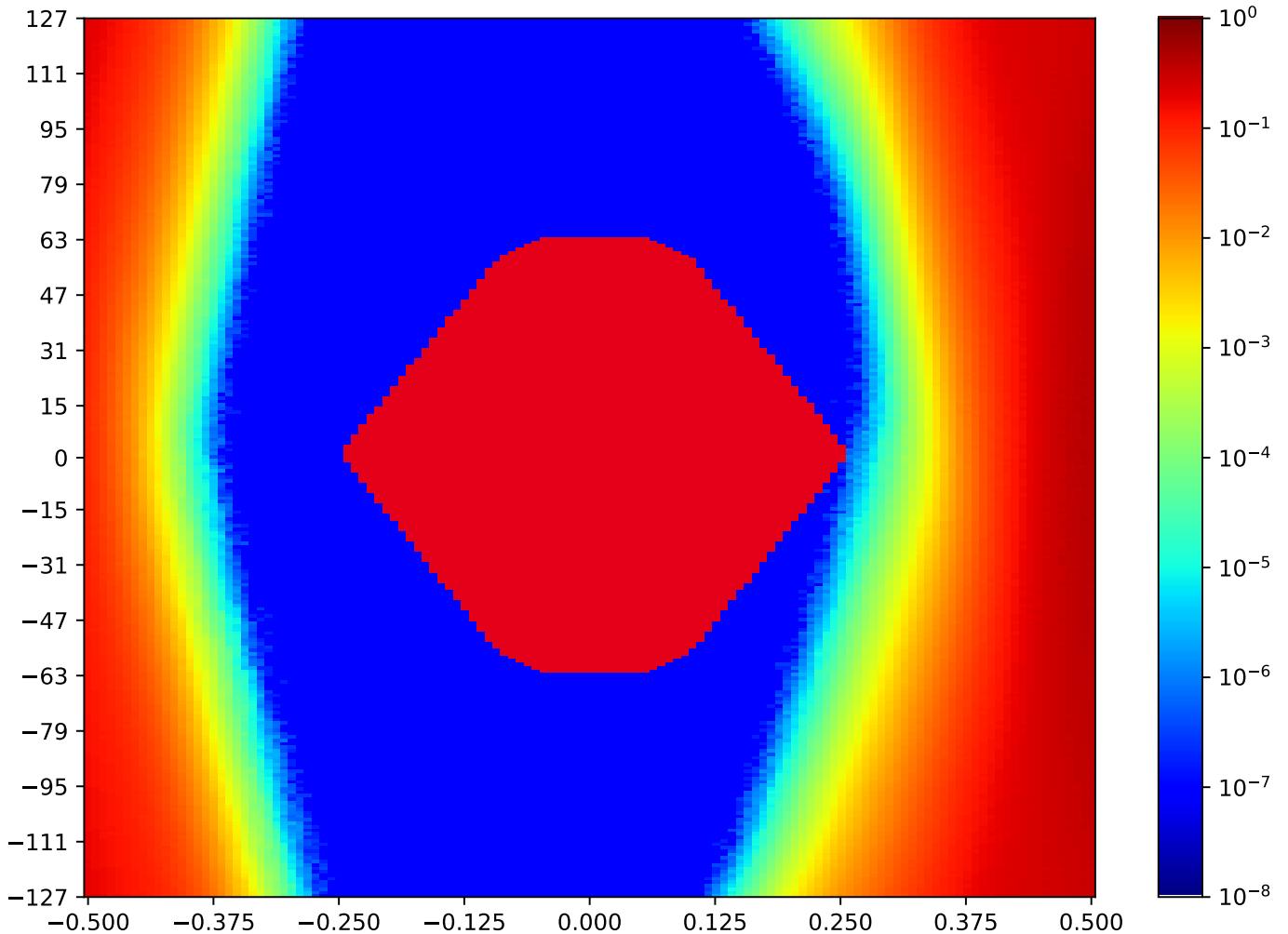


Figure 3.242: MSP_A_FPGA-TX1-01-RX13-01-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.3 MSP_A_FPGA-TX1-02-RX13-02-MSP_C_FPGA

Table 3.224: MSP_A_FPGA-TX1-02-RX13-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:42:00		2018-Jan-24 01:42:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18291	84	65.12%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

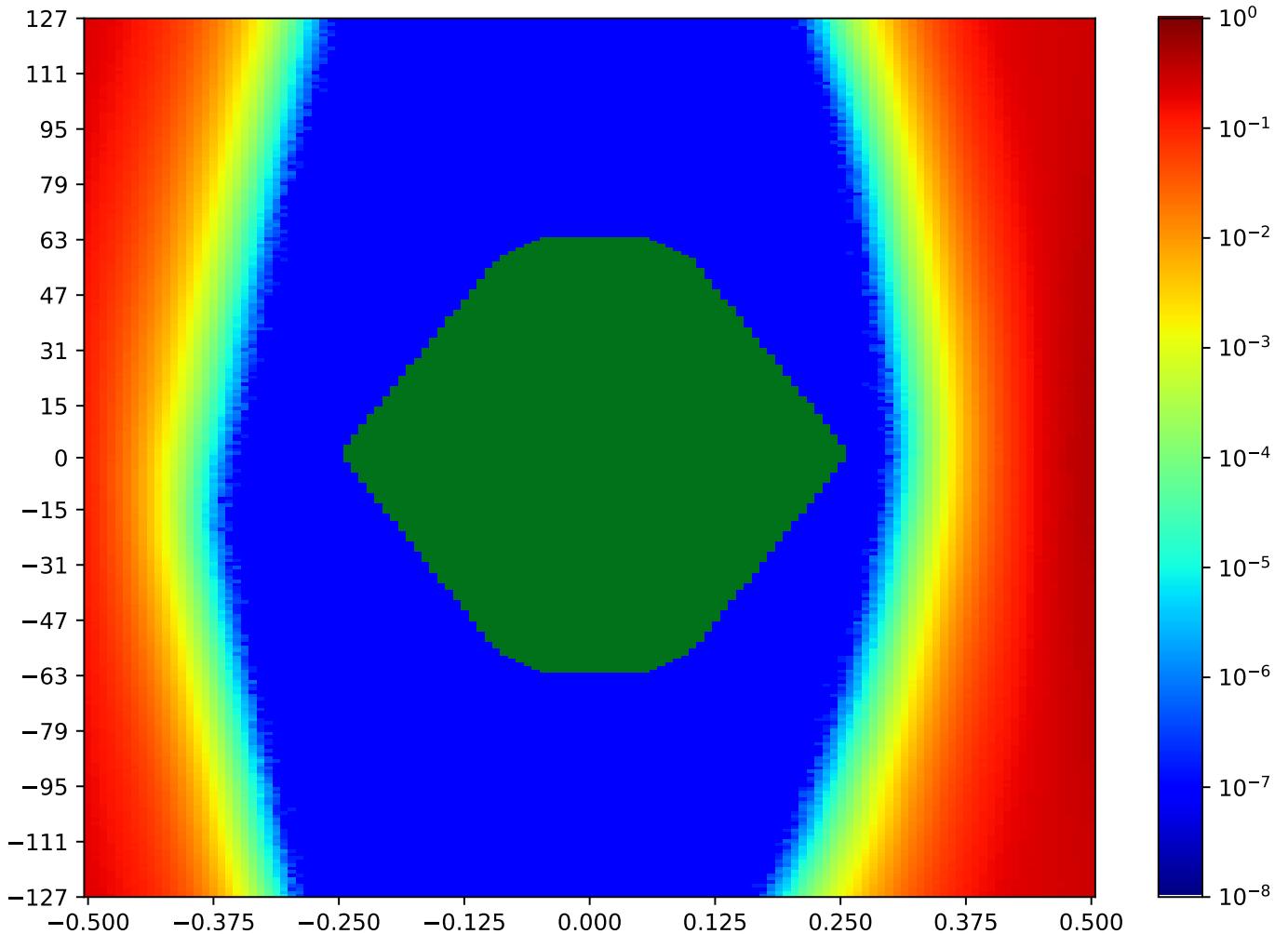


Figure 3.243: MSP_A_FPGA-TX1-02-RX13-02-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.4 MSP_A_FPGA-TX1-03-RX13-03-MSP_C_FPGA

Table 3.225: MSP_A_FPGA-TX1-03-RX13-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:38:32		2018-Jan-24 01:39:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18521	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

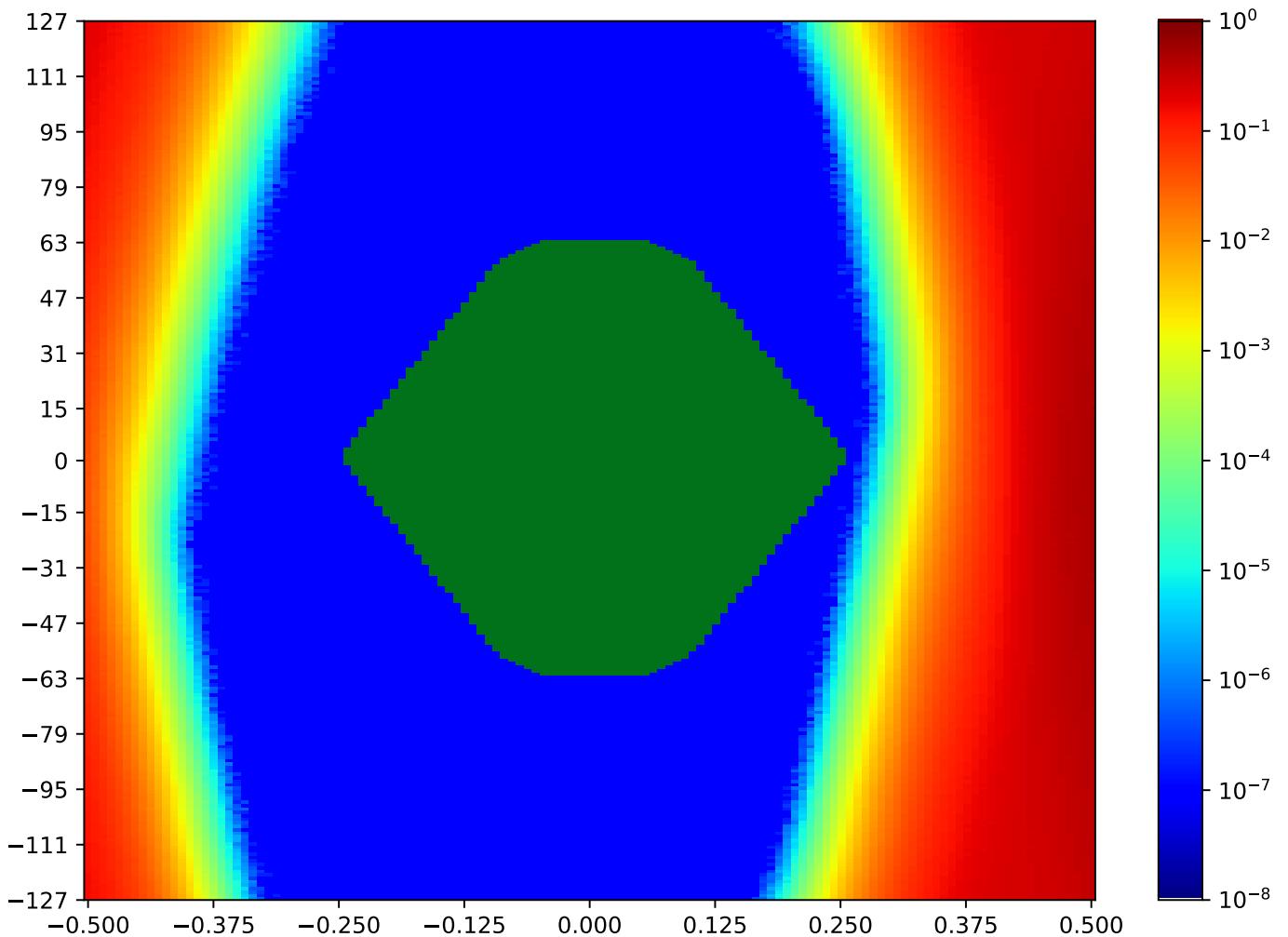


Figure 3.244: MSP_A_FPGA-TX1-03-RX13-03-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.5 MSP_A_FPGA-TX1-04-RX13-04-MSP_C_FPGA

Table 3.226: MSP_A_FPGA-TX1-04-RX13-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:44:05		2018-Jan-24 01:44:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16172	80	62.02%	249	96.86%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

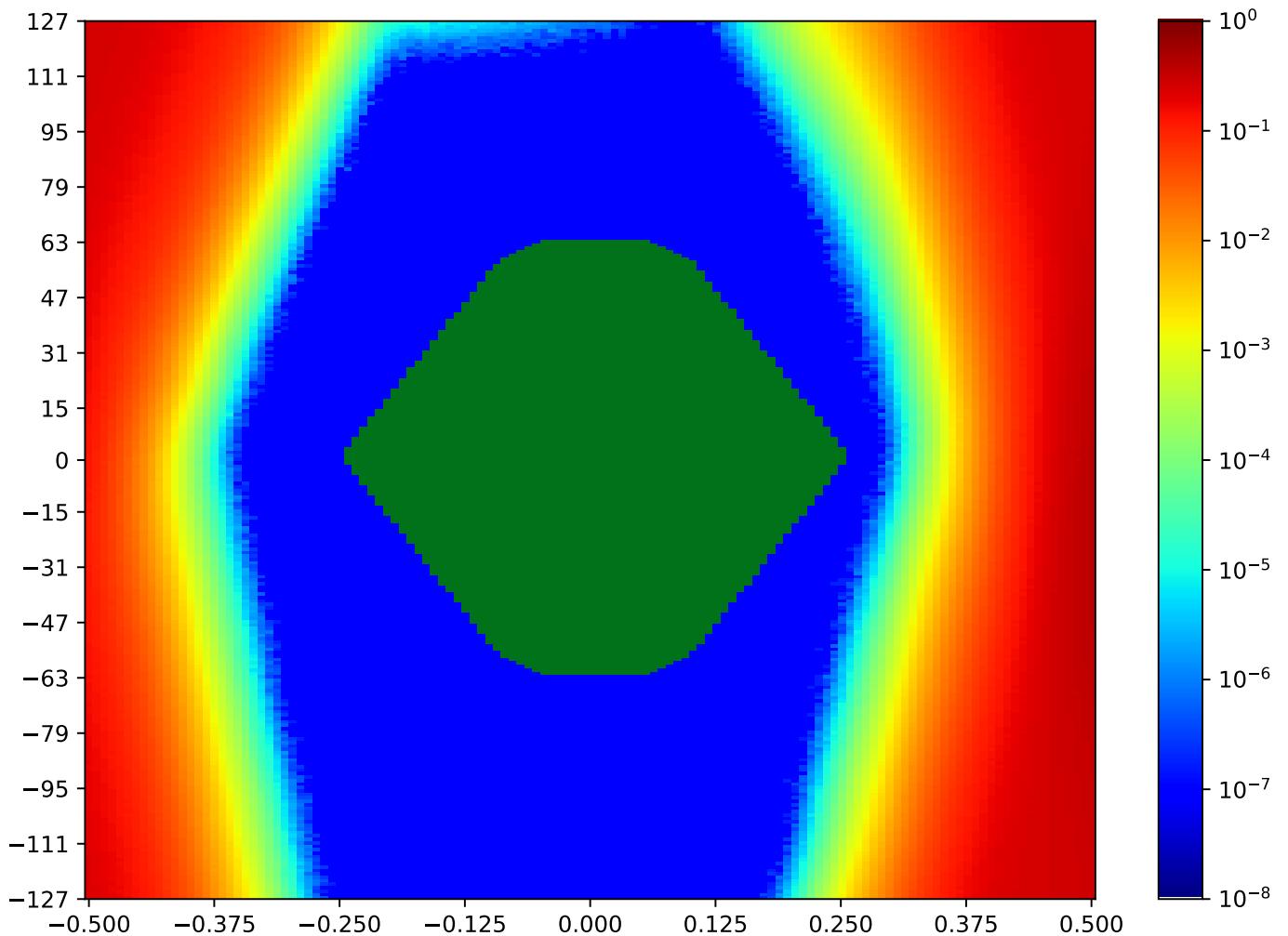


Figure 3.245: MSP_A_FPGA-TX1-04-RX13-04-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.6 MSP_A_FPGA-TX1-05-RX13-05-MSP_C_FPGA

Table 3.227: MSP_A_FPGA-TX1-05-RX13-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:37:50		2018-Jan-24 01:38:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17474	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

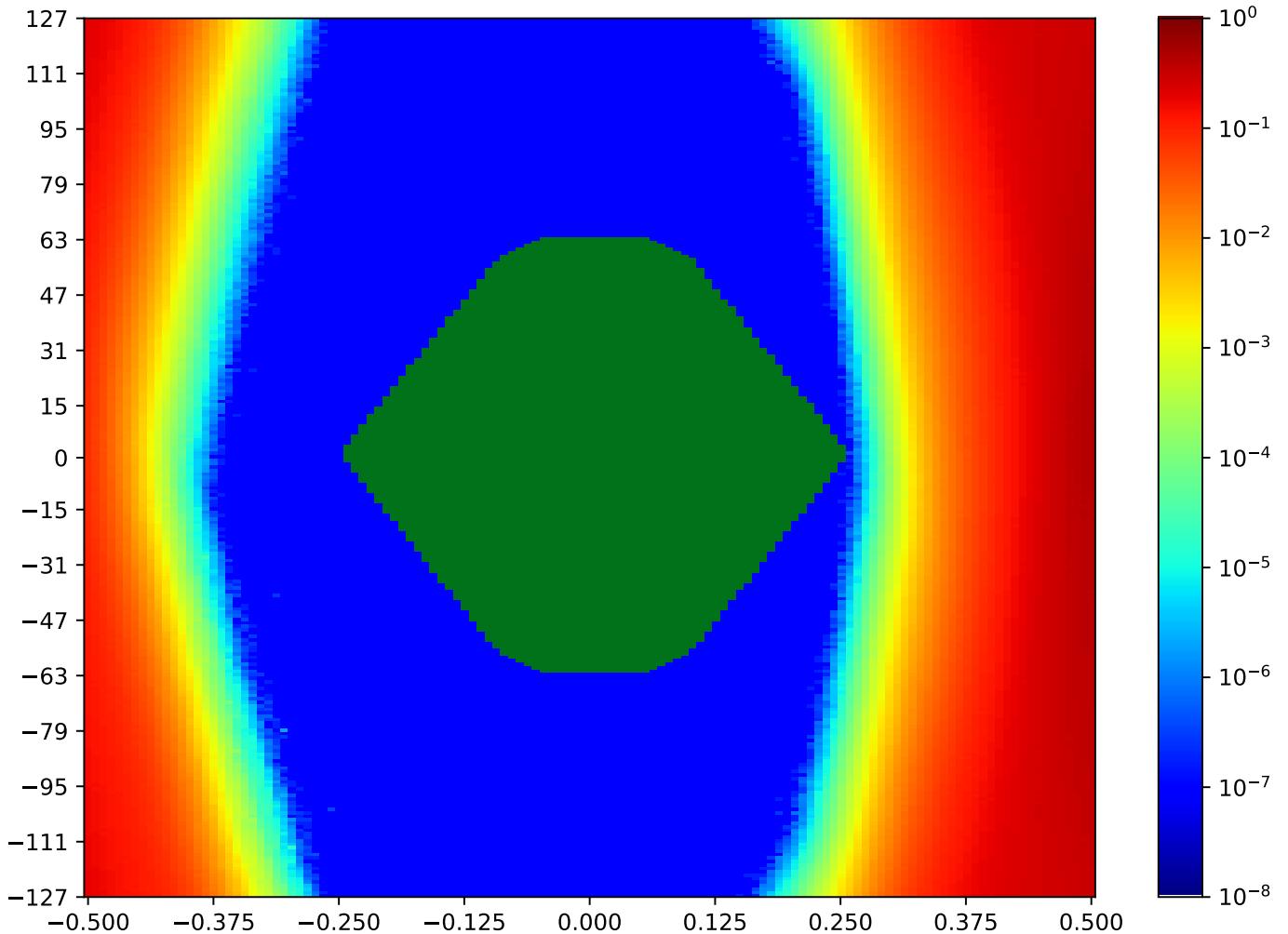


Figure 3.246: MSP_A_FPGA-TX1-05-RX13-05-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.7 MSP_A_FPGA-TX1-06-RX13-06-MSP_C_FPGA

Table 3.228: MSP_A_FPGA-TX1-06-RX13-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:45:28		2018-Jan-24 01:46:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17401	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

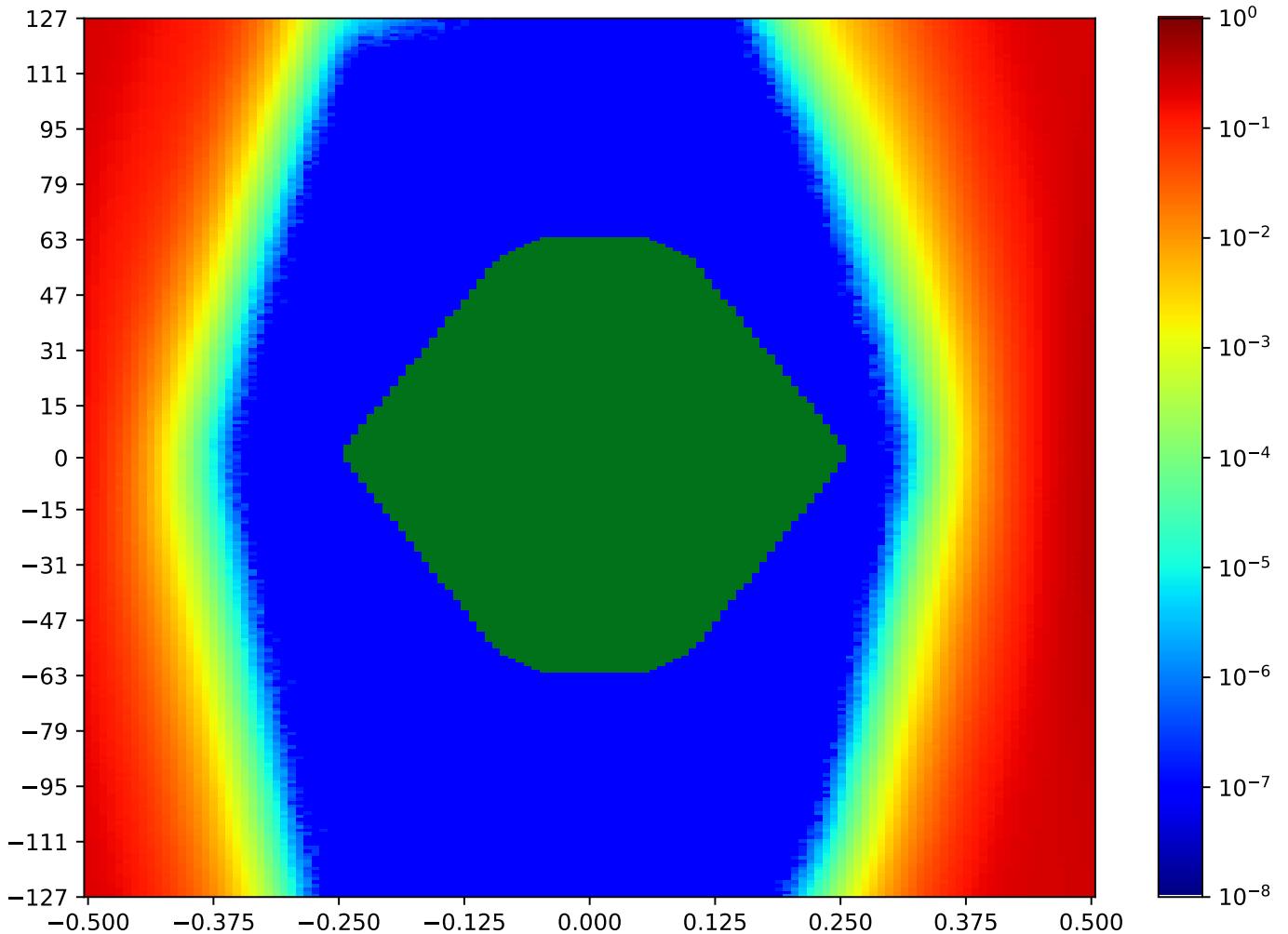


Figure 3.247: MSP_A_FPGA-TX1-06-RX13-06-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.8 MSP_A_FPGA-TX1-07-RX13-07-MSP_C_FPGA

Table 3.229: MSP_A_FPGA-TX1-07-RX13-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:39:14		2018-Jan-24 01:39:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16071	78	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

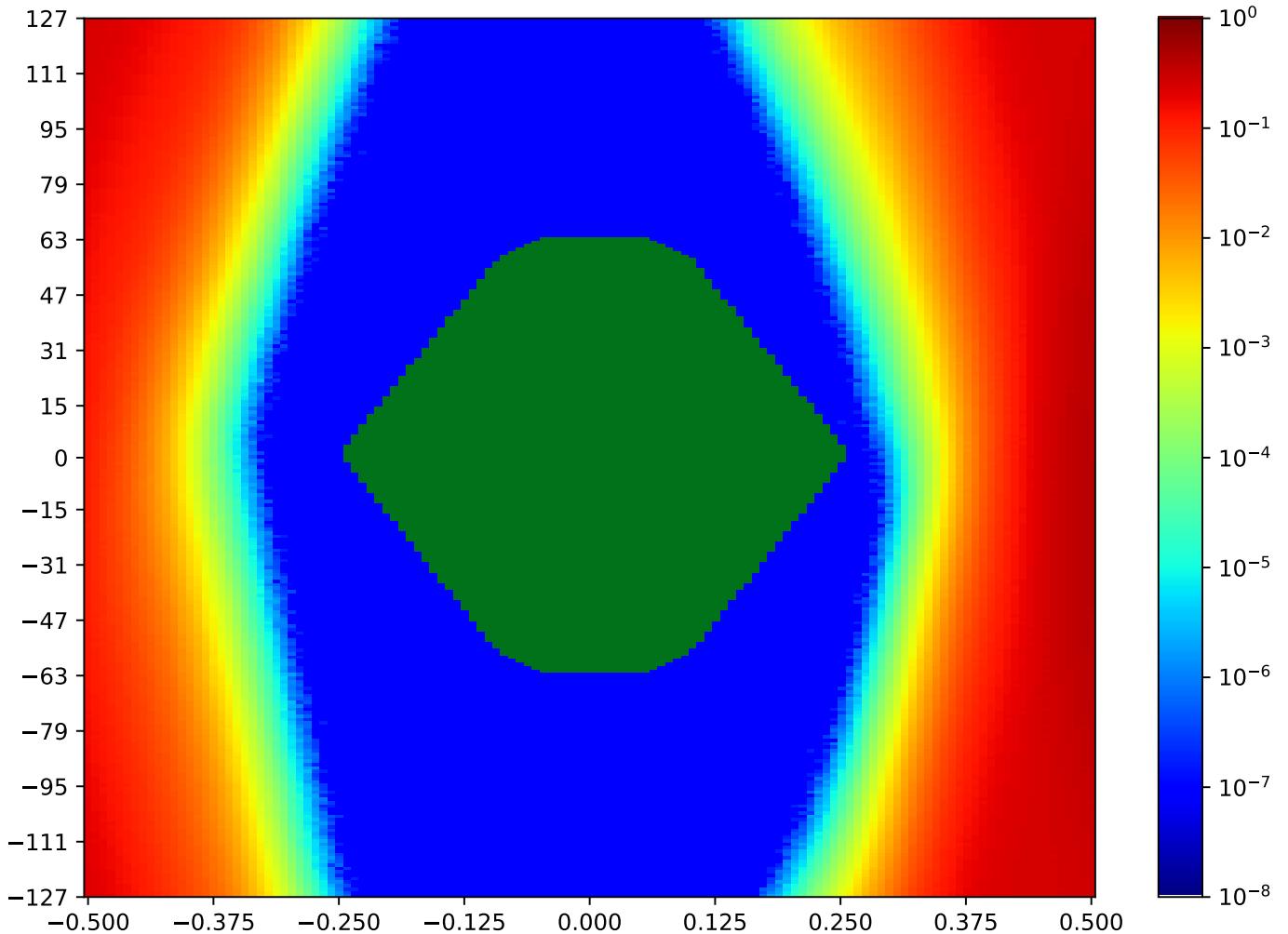


Figure 3.248: MSP_A_FPGA-TX1-07-RX13-07-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.9 MSP_A_FPGA-TX1-08-RX13-08-MSP_C_FPGA

Table 3.230: MSP_A_FPGA-TX1-08-RX13-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:44:46		2018-Jan-24 01:45:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17977	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

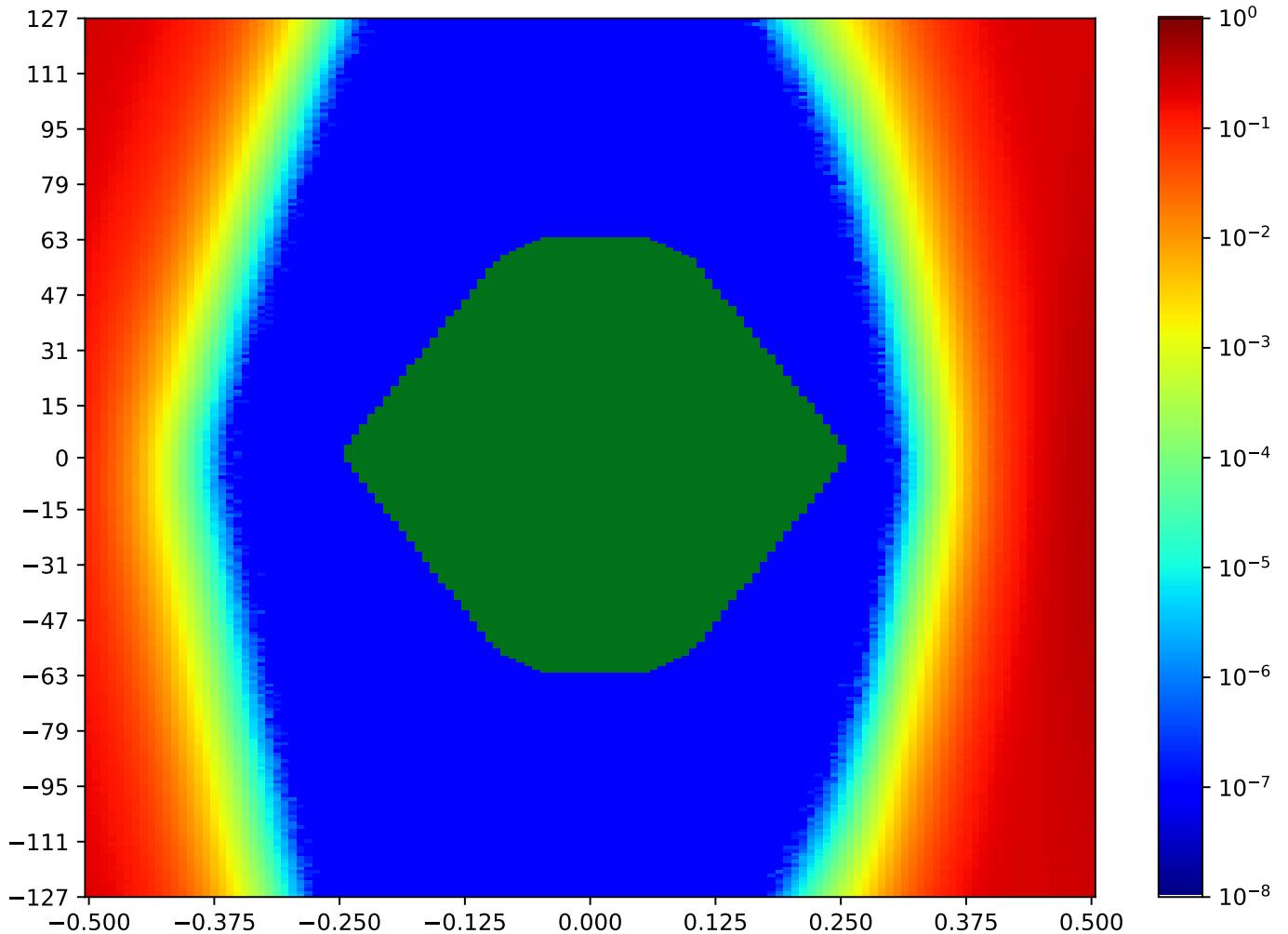


Figure 3.249: MSP_A_FPGA-TX1-08-RX13-08-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.10 MSP_A_FPGA-TX1-09-RX13-09-MSP_C_FPGA

Table 3.231: MSP_A_FPGA-TX1-09-RX13-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:40:37		2018-Jan-24 01:41:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16842	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

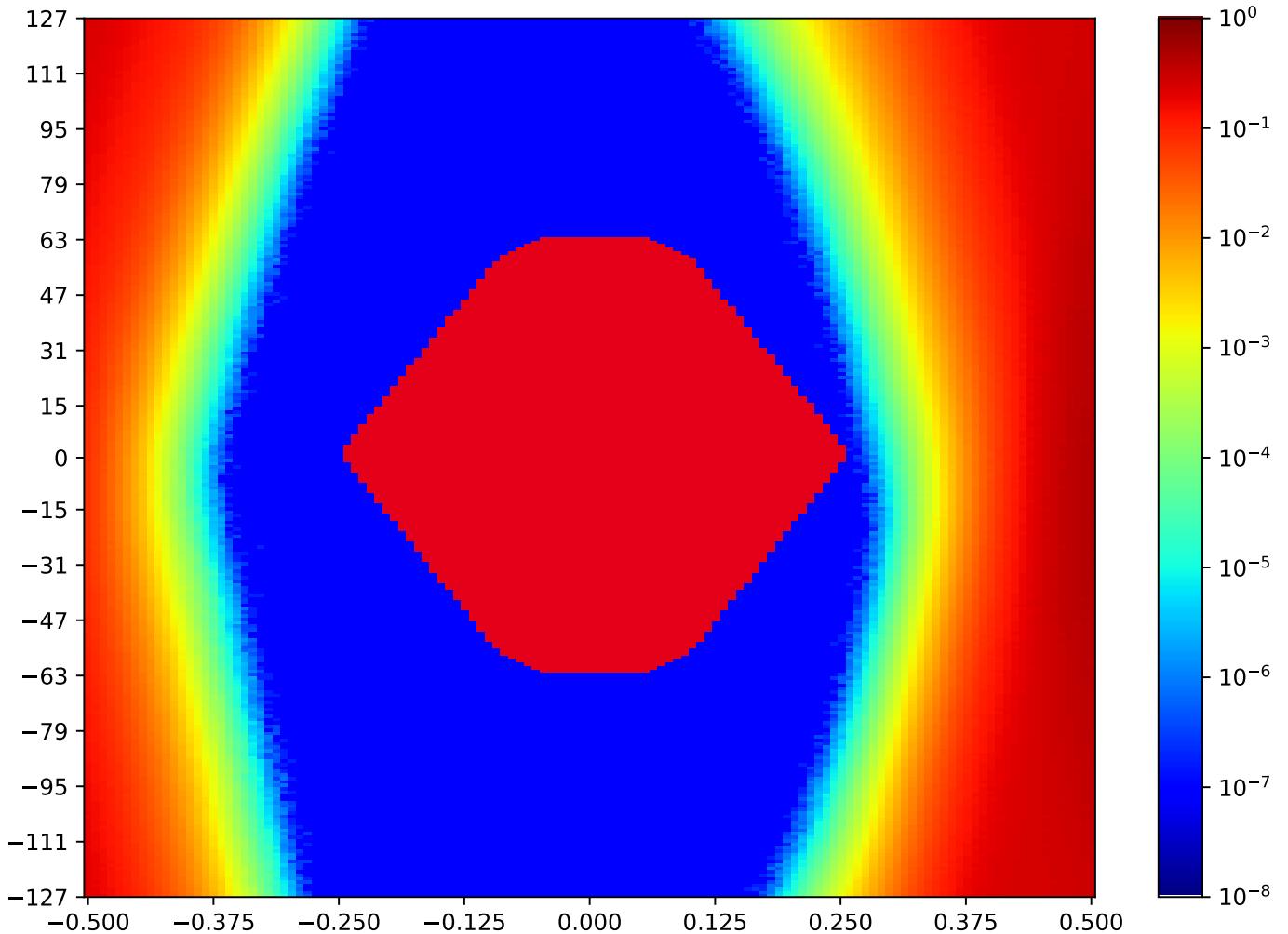


Figure 3.250: MSP_A_FPGA-TX1-09-RX13-09-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.11 MSP_A_FPGA-TX1-10-RX13-10-MSP_C_FPGA

Table 3.232: MSP_A_FPGA-TX1-10-RX13-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:43:23		2018-Jan-24 01:44:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15461	73	56.59%	242	94.51%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

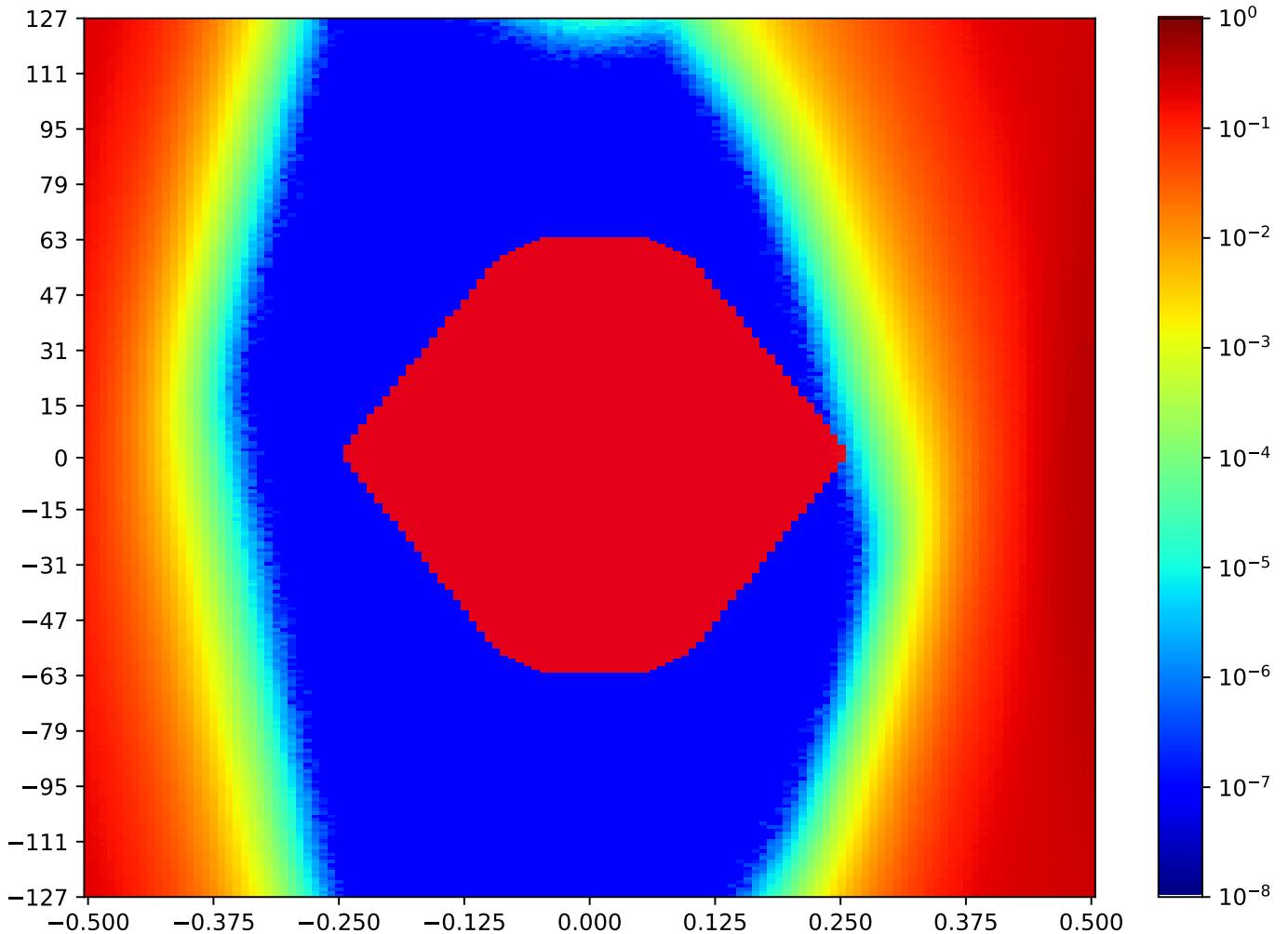


Figure 3.251: MSP_A_FPGA-TX1-10-RX13-10-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.19.12 MSP_A_FPGA-TX1-11-RX13-11-MSP_C_FPGA

Table 3.233: MSP_A_FPGA-TX1-11-RX13-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:42:42		2018-Jan-24 01:43:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16938	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

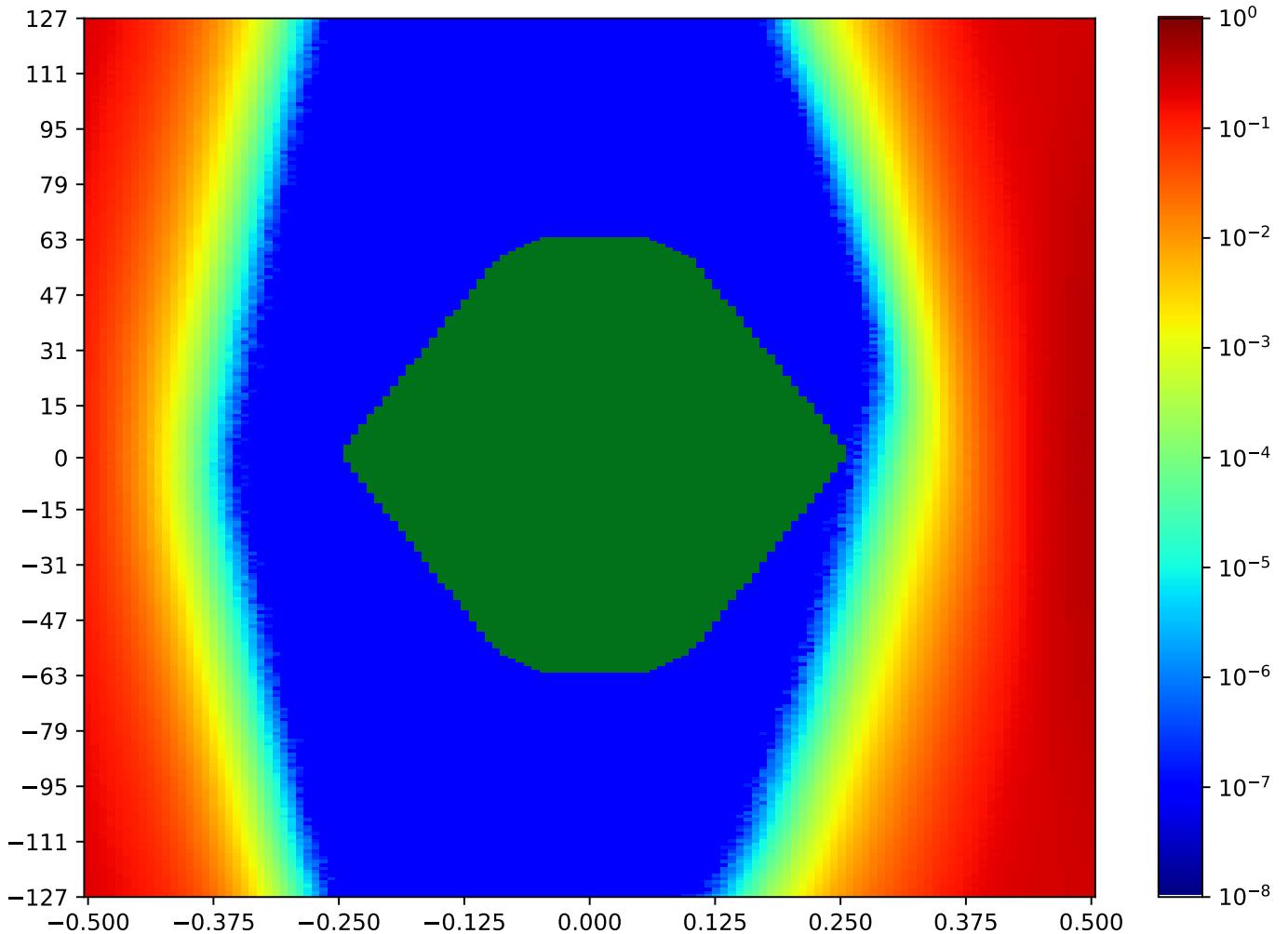


Figure 3.252: MSP_A_FPGA-TX1-11-RX13-11-MSP_C_FPGA

Call back to summary Figure 3.240. Sibling eye diagrams: V1-6.4.

3.20 MSP_A TX2 MSP_C RX12 Minipod Loopback

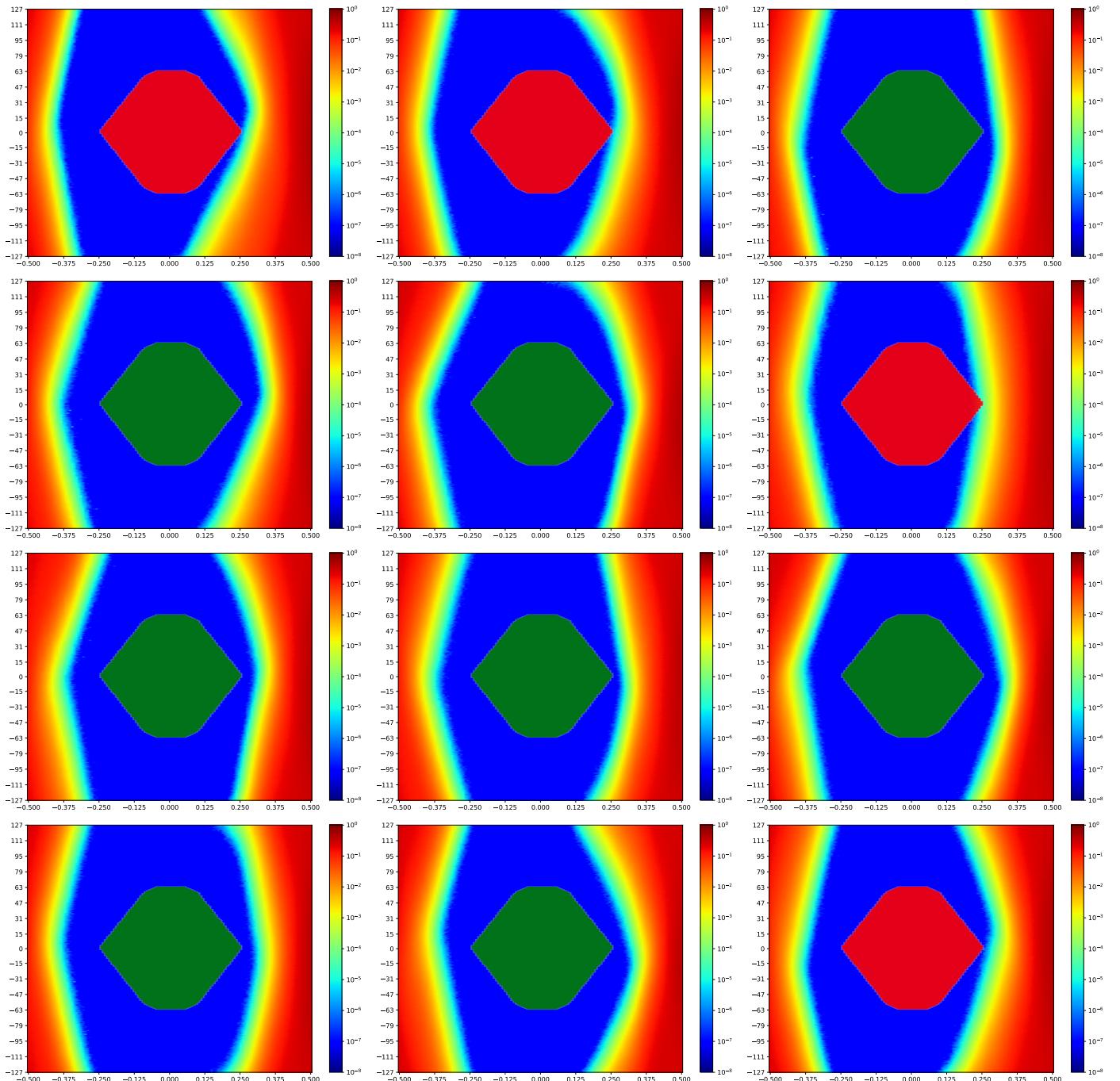


Figure 3.253: MSP_A TX2 MSP_C RX12 Minipod Loopback

A cross-reference to Figure 3.253. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.266.

3.20.1 MSP_A_FPGA-TX2-00-RX12-00-MSP_C_FPGA

Table 3.234: MSP_A_FPGA-TX2-00-RX12-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:48:15		2018-Jan-24 01:48:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16566	79	61.24%	254	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

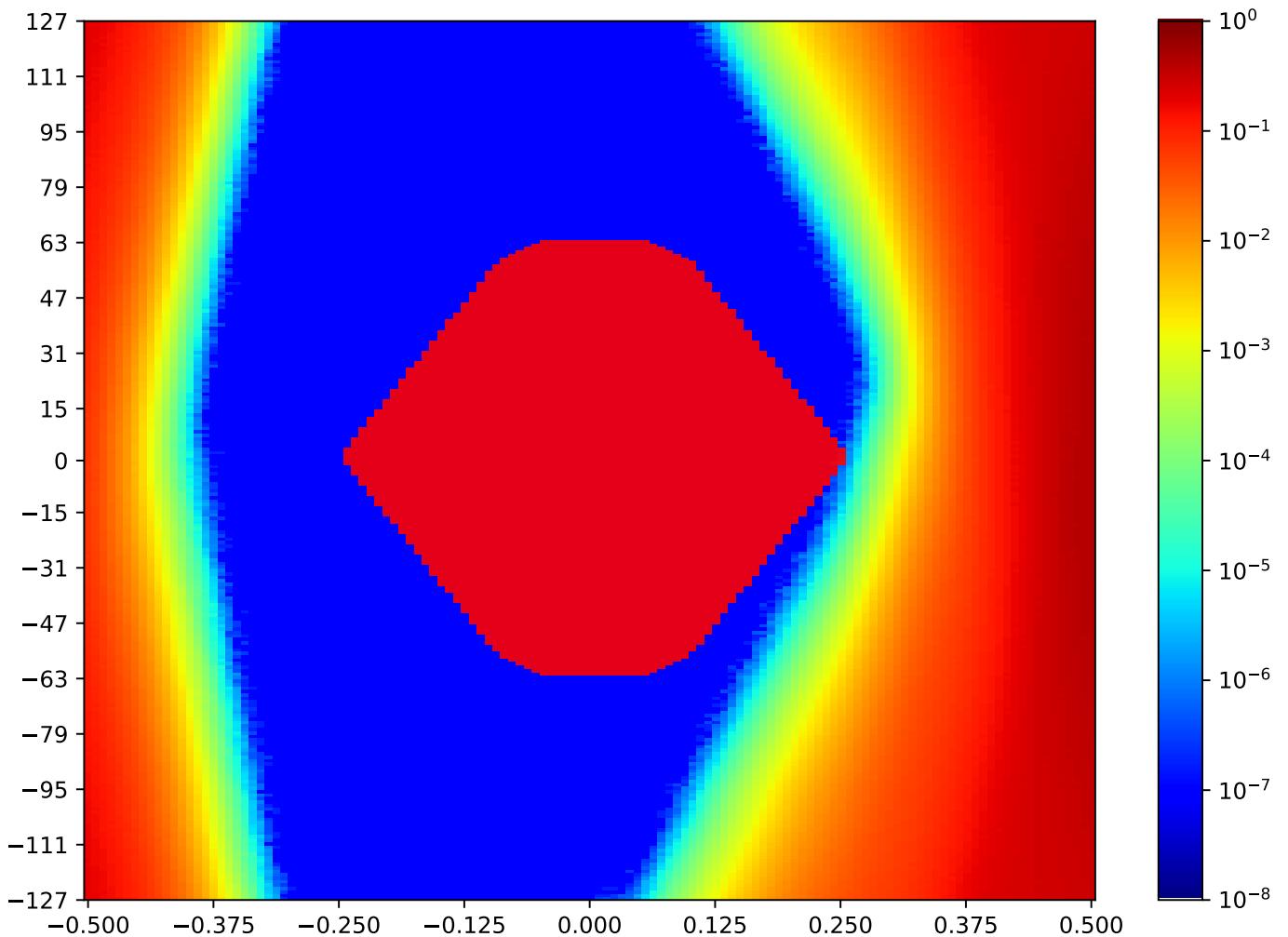


Figure 3.254: MSP_A_FPGA-TX2-00-RX12-00-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.2 MSP_A_FPGA-TX2-01-RX12-01-MSP_C_FPGA

Table 3.235: MSP_A_FPGA-TX2-01-RX12-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:46:51		2018-Jan-24 01:47:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16221	78	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

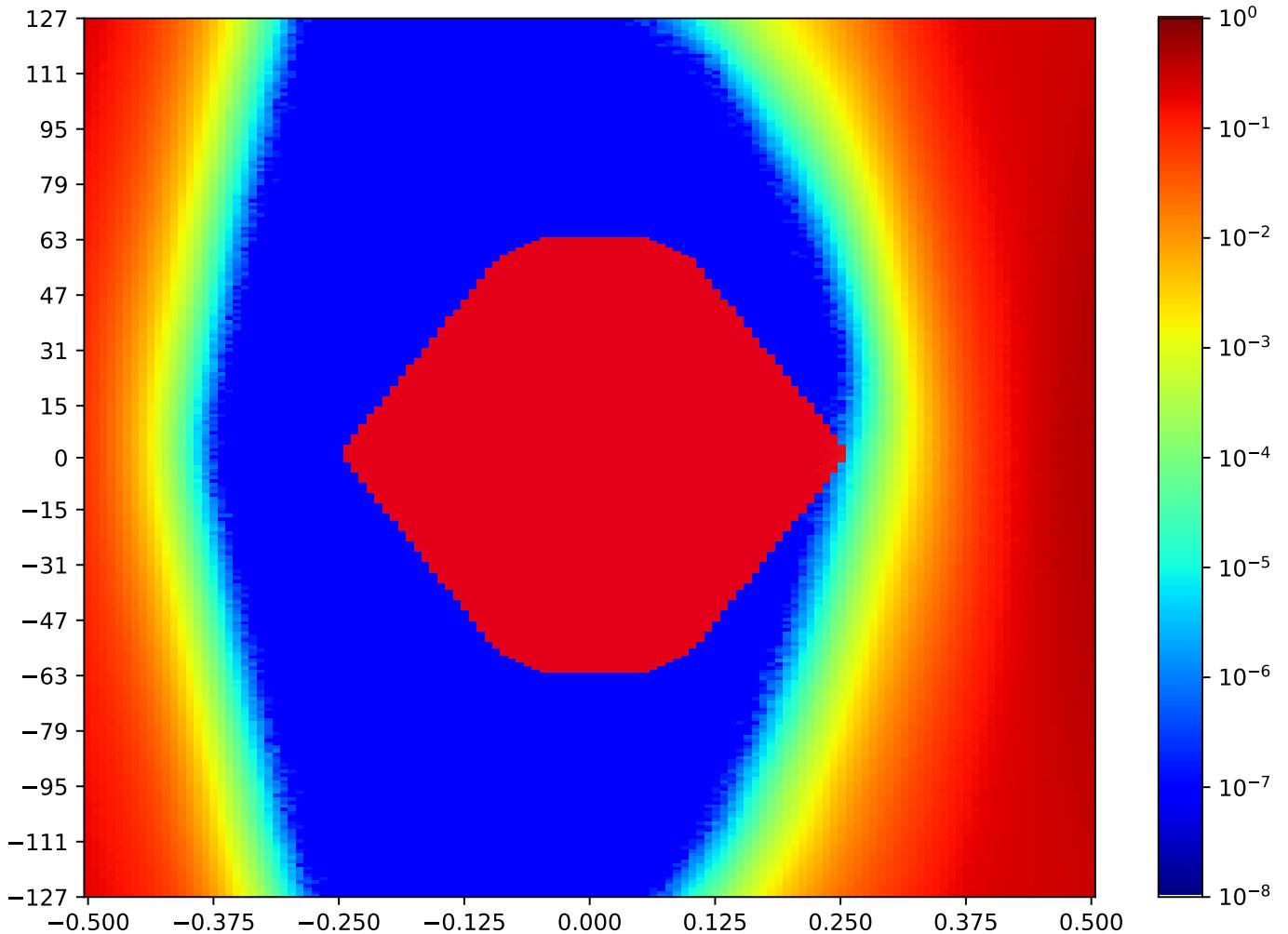


Figure 3.255: MSP_A_FPGA-TX2-01-RX12-01-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.3 MSP_A_FPGA-TX2-02-RX12-02-MSP_C_FPGA

Table 3.236: MSP_A_FPGA-TX2-02-RX12-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:50:22		2018-Jan-24 01:51:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18133	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

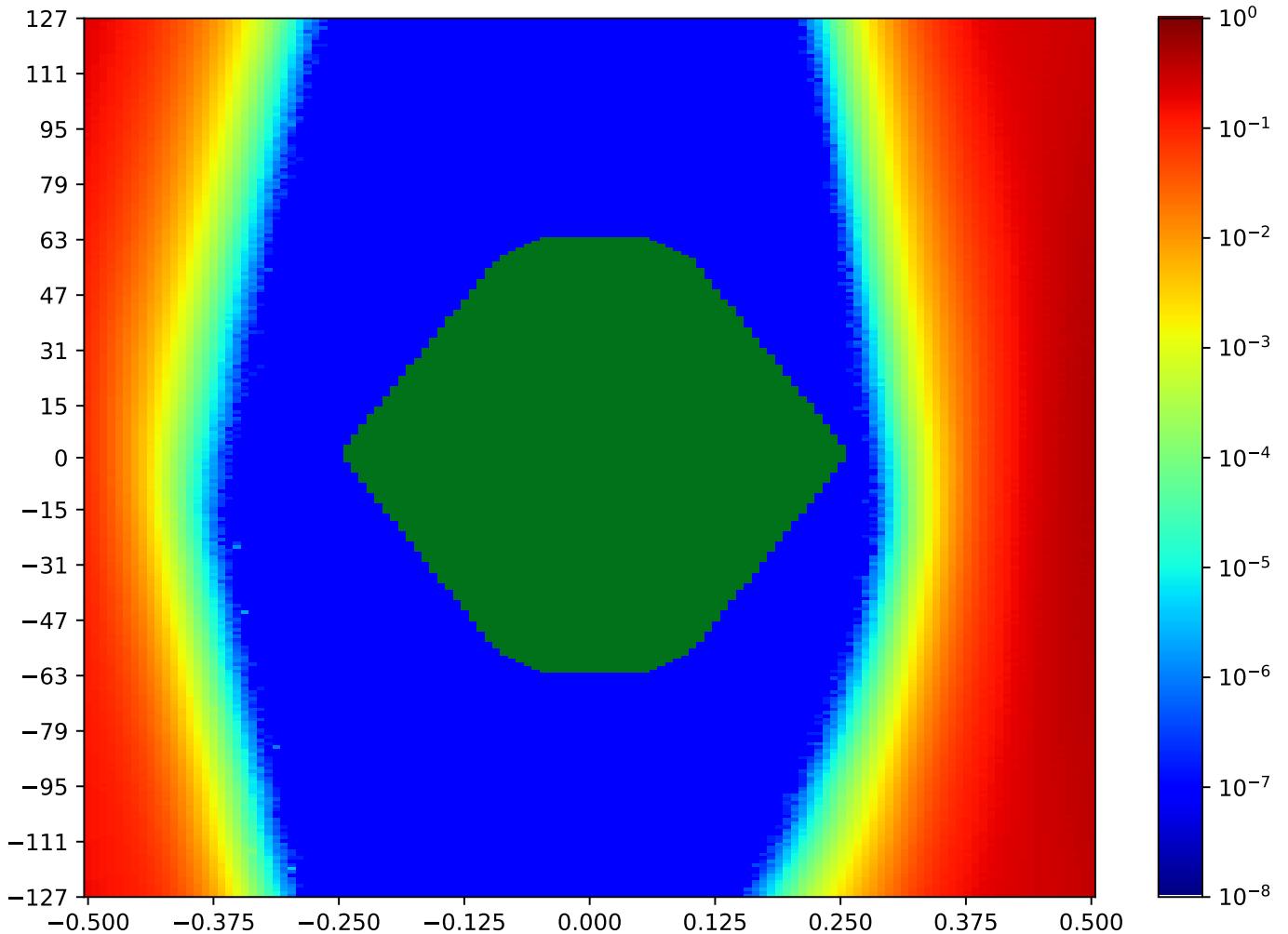


Figure 3.256: MSP_A_FPGA-TX2-02-RX12-02-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.4 MSP_A_FPGA-TX2-03-RX12-03-MSP_C_FPGA

Table 3.237: MSP_A_FPGA-TX2-03-RX12-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:46:09		2018-Jan-24 01:46:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17192	84	65.12%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

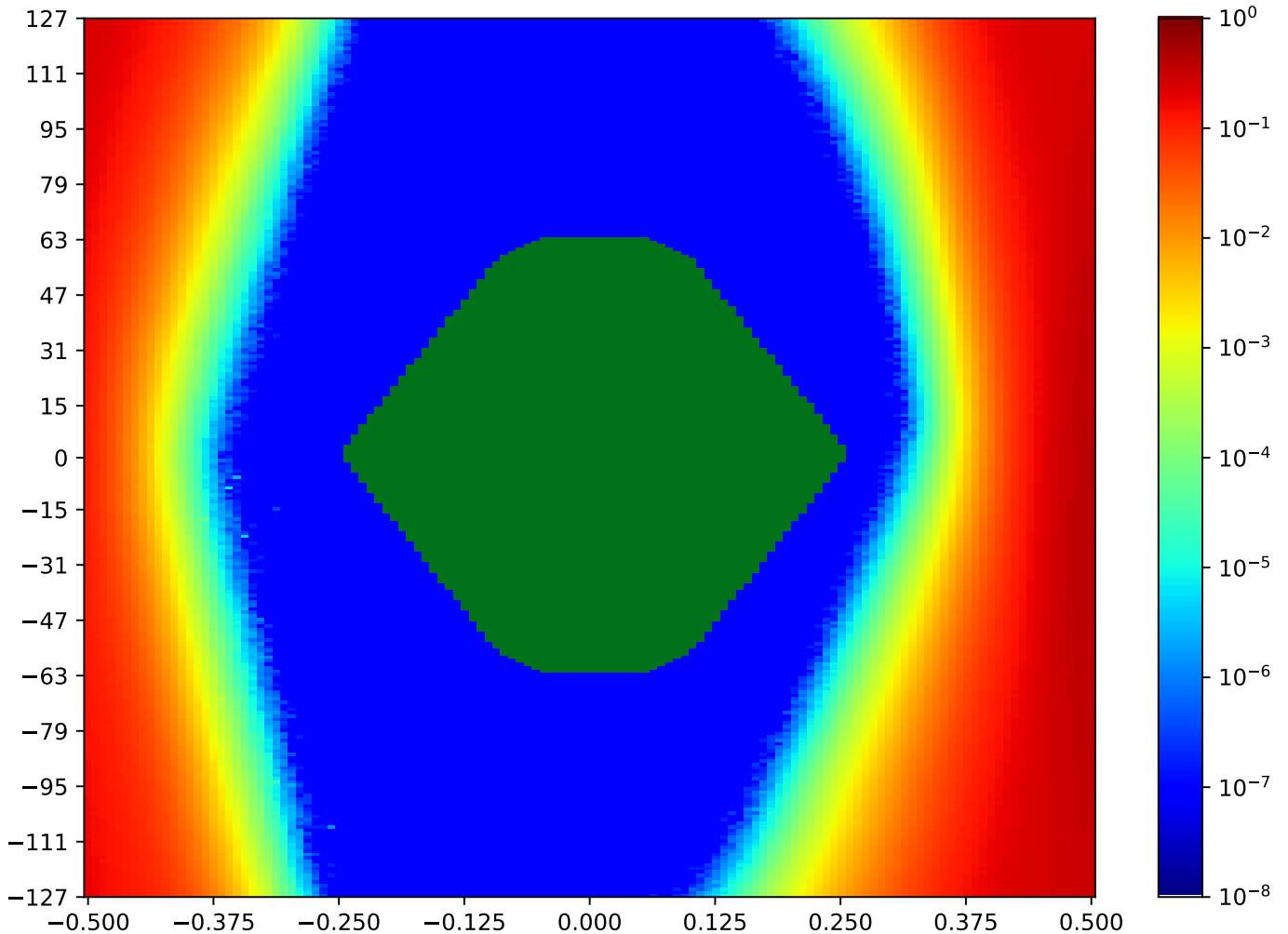


Figure 3.257: MSP_A_FPGA-TX2-03-RX12-03-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.5 MSP_A_FPGA-TX2-04-RX12-04-MSP_C_FPGA

Table 3.238: MSP_A_FPGA-TX2-04-RX12-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:52:30		2018-Jan-24 01:53:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16962	83	64.34%	254	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

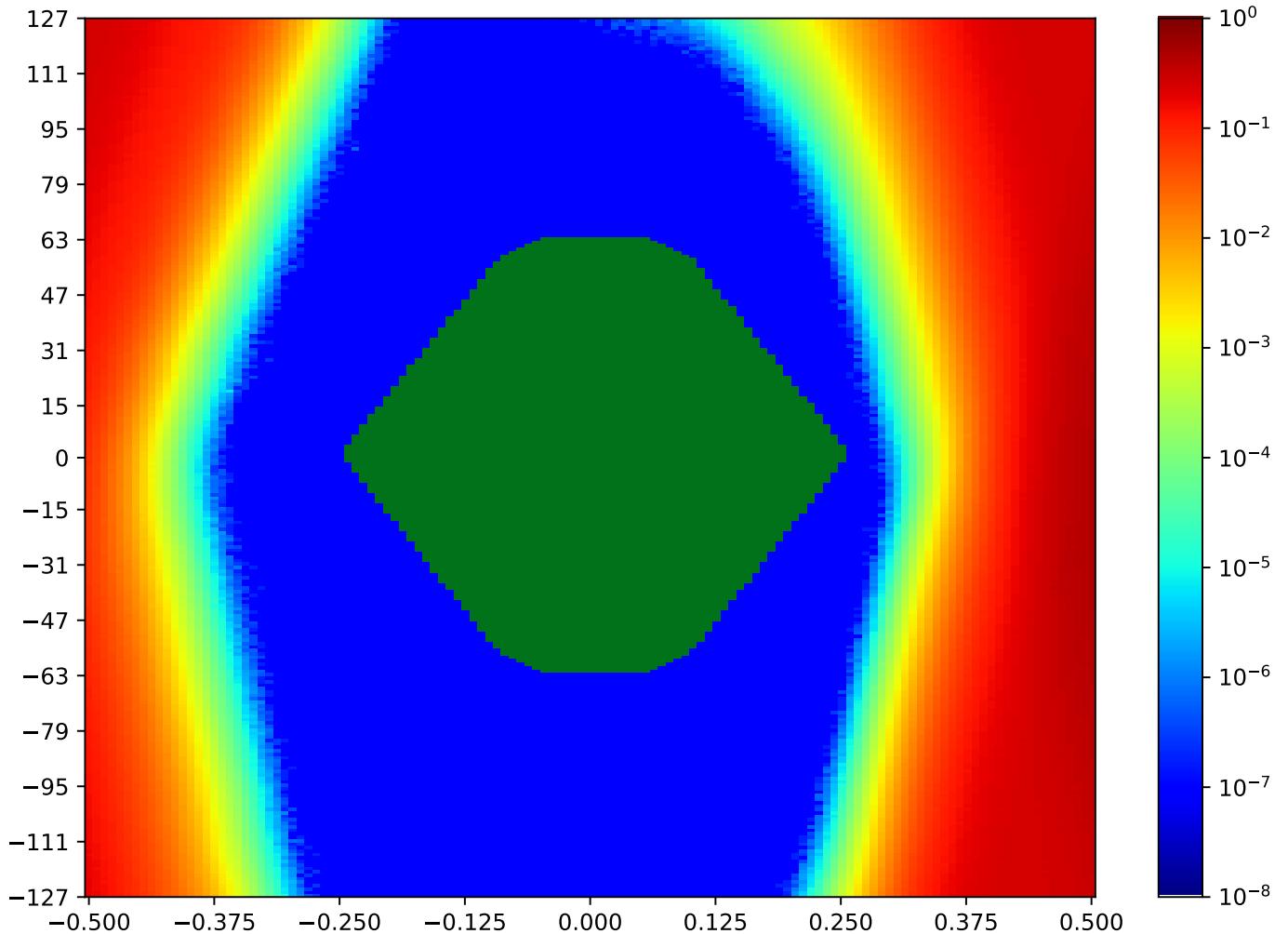


Figure 3.258: MSP_A_FPGA-TX2-04-RX12-04-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.6 MSP_A_FPGA-TX2-05-RX12-05-MSP_C_FPGA

Table 3.239: MSP_A_FPGA-TX2-05-RX12-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:47:33		2018-Jan-24 01:48:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	15140	70	53.49%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

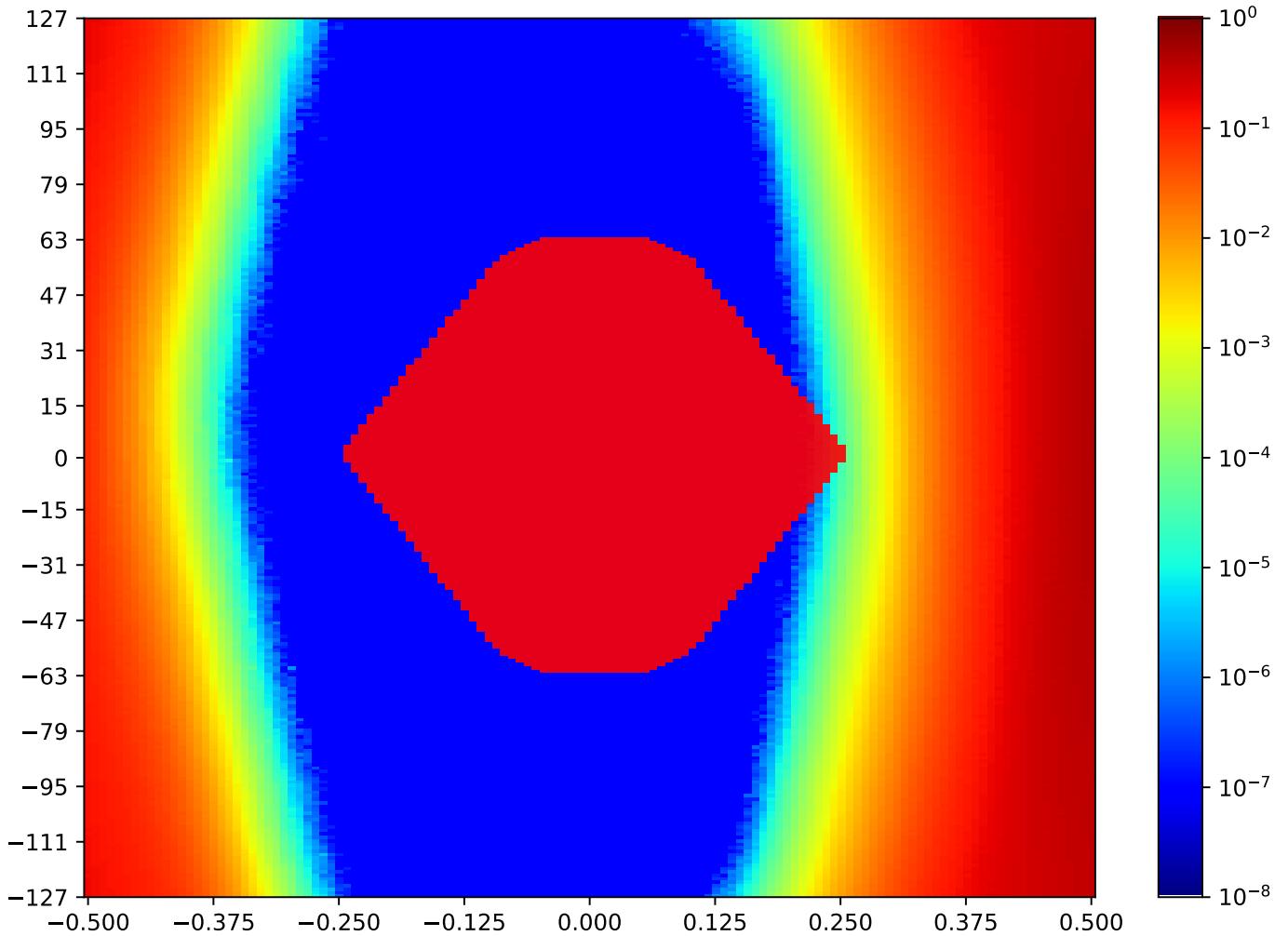


Figure 3.259: MSP_A_FPGA-TX2-05-RX12-05-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.7 MSP_A_FPGA-TX2-06-RX12-06-MSP_C_FPGA

Table 3.240: MSP_A_FPGA-TX2-06-RX12-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:53:55		2018-Jan-24 01:54:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16925	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

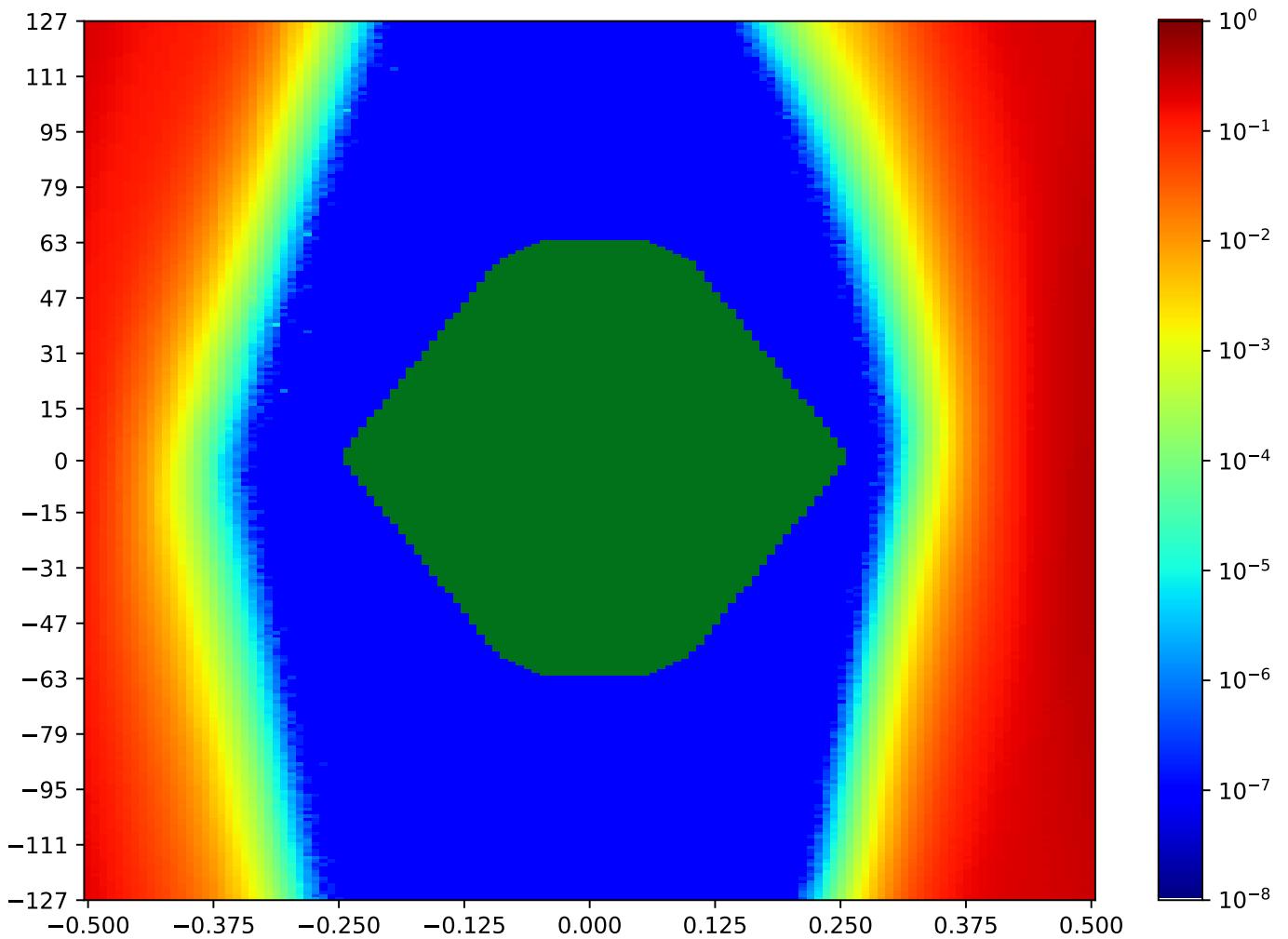


Figure 3.260: MSP_A_FPGA-TX2-06-RX12-06-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.8 MSP_A_FPGA-TX2-07-RX12-07-MSP_C_FPGA

Table 3.241: MSP_A_FPGA-TX2-07-RX12-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:48:57		2018-Jan-24 01:49:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16707	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

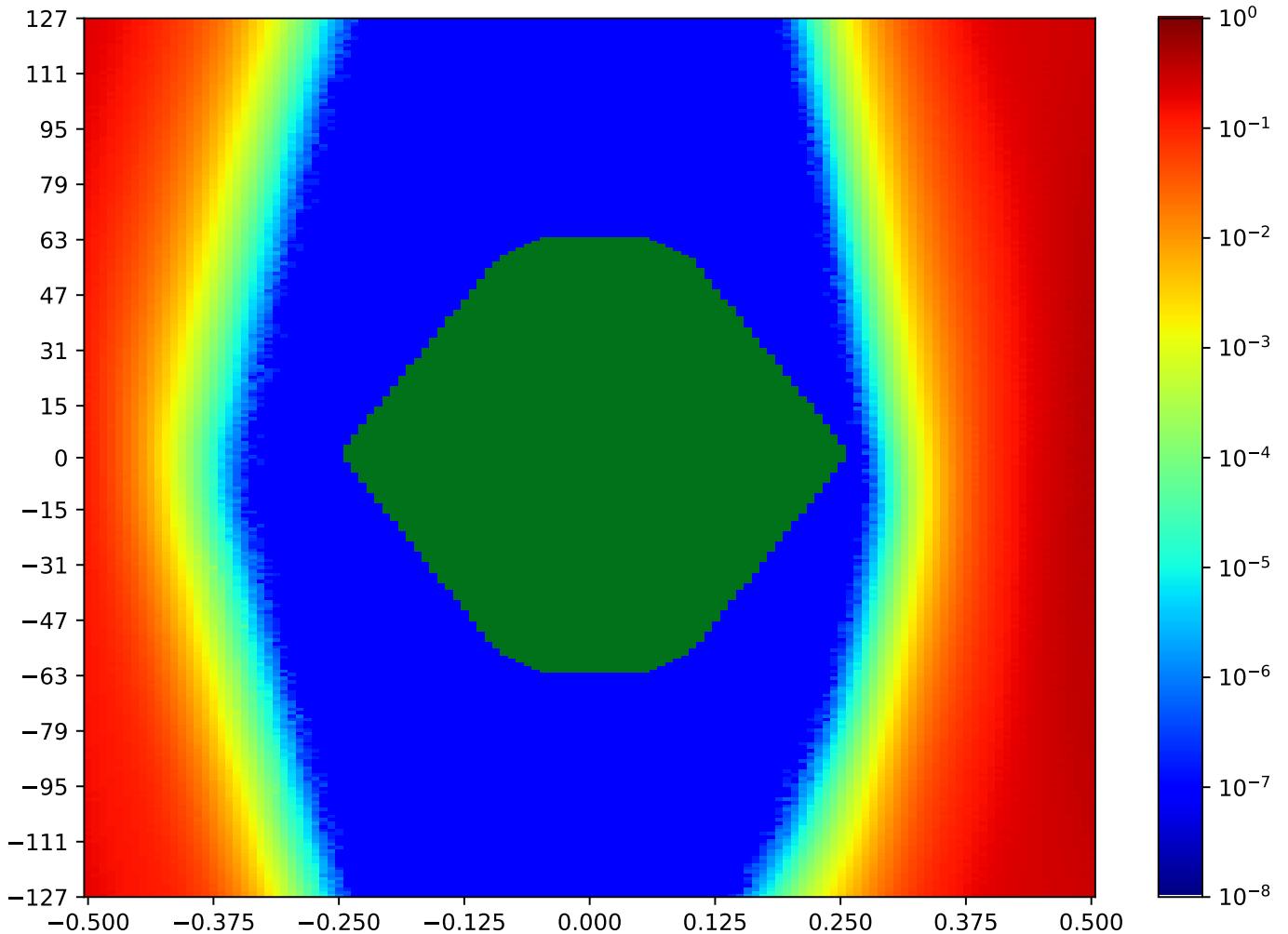


Figure 3.261: MSP_A_FPGA-TX2-07-RX12-07-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.9 MSP_A_FPGA-TX2-08-RX12-08-MSP_C_FPGA

Table 3.242: MSP_A_FPGA-TX2-08-RX12-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:53:13		2018-Jan-24 01:53:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17393	82	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

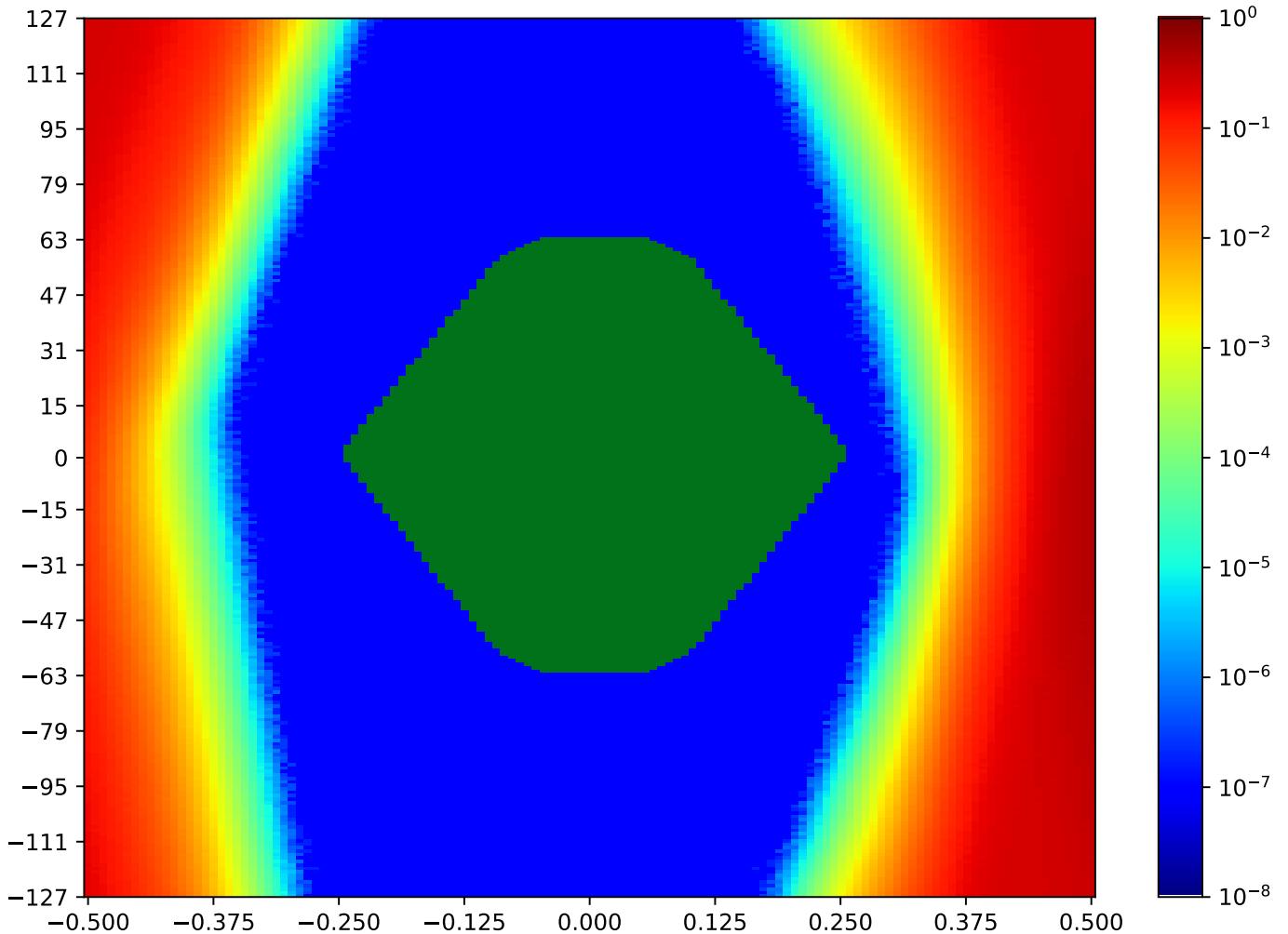


Figure 3.262: MSP_A_FPGA-TX2-08-RX12-08-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.10 MSP_A_FPGA-TX2-09-RX12-09-MSP_C_FPGA

Table 3.243: MSP_A_FPGA-TX2-09-RX12-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:49:40		2018-Jan-24 01:50:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17948	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

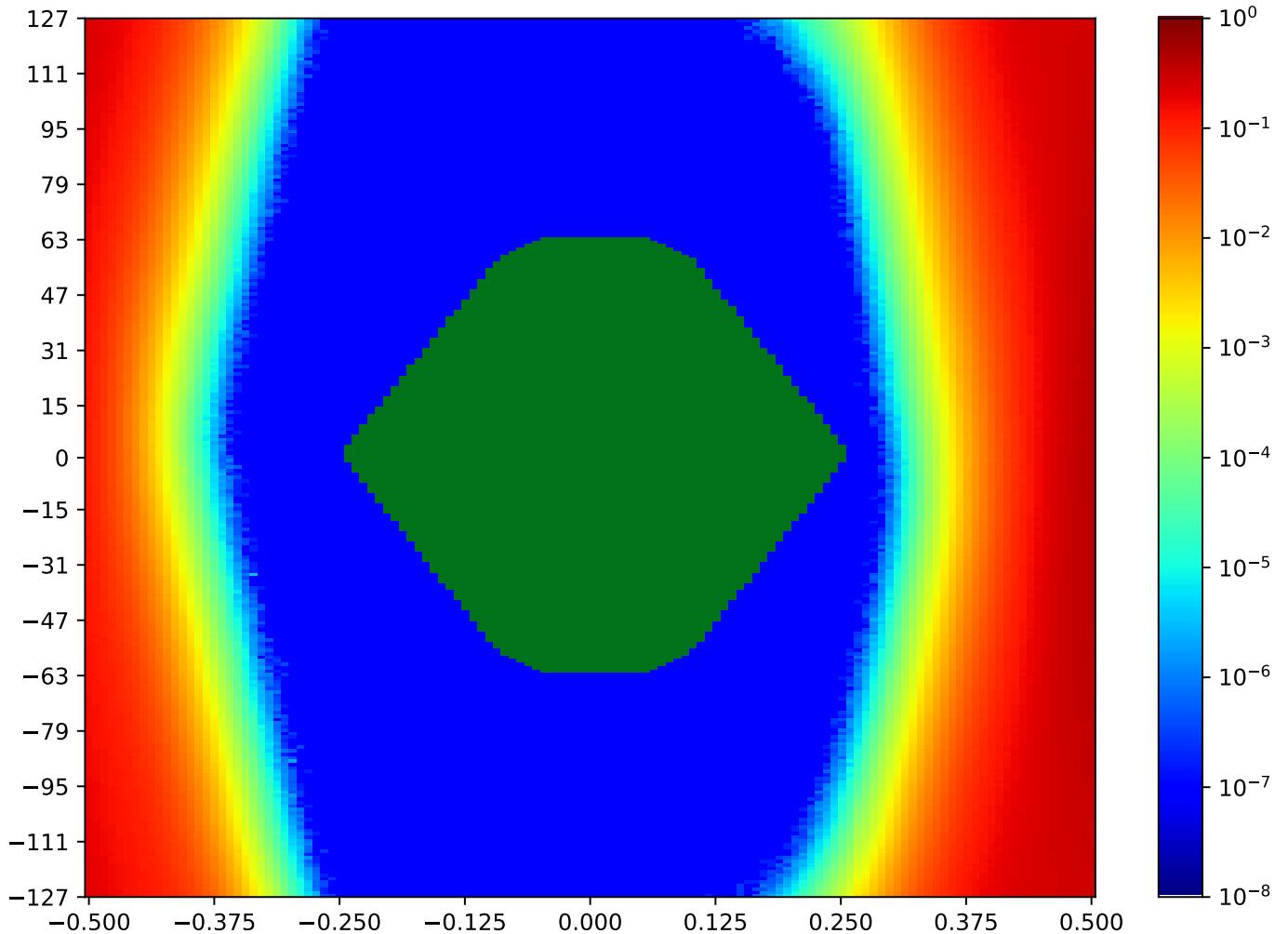


Figure 3.263: MSP_A_FPGA-TX2-09-RX12-09-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.11 MSP_A_FPGA-TX2-10-RX12-10-MSP_C_FPGA

Table 3.244: MSP_A_FPGA-TX2-10-RX12-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:51:48		2018-Jan-24 01:52:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16336	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

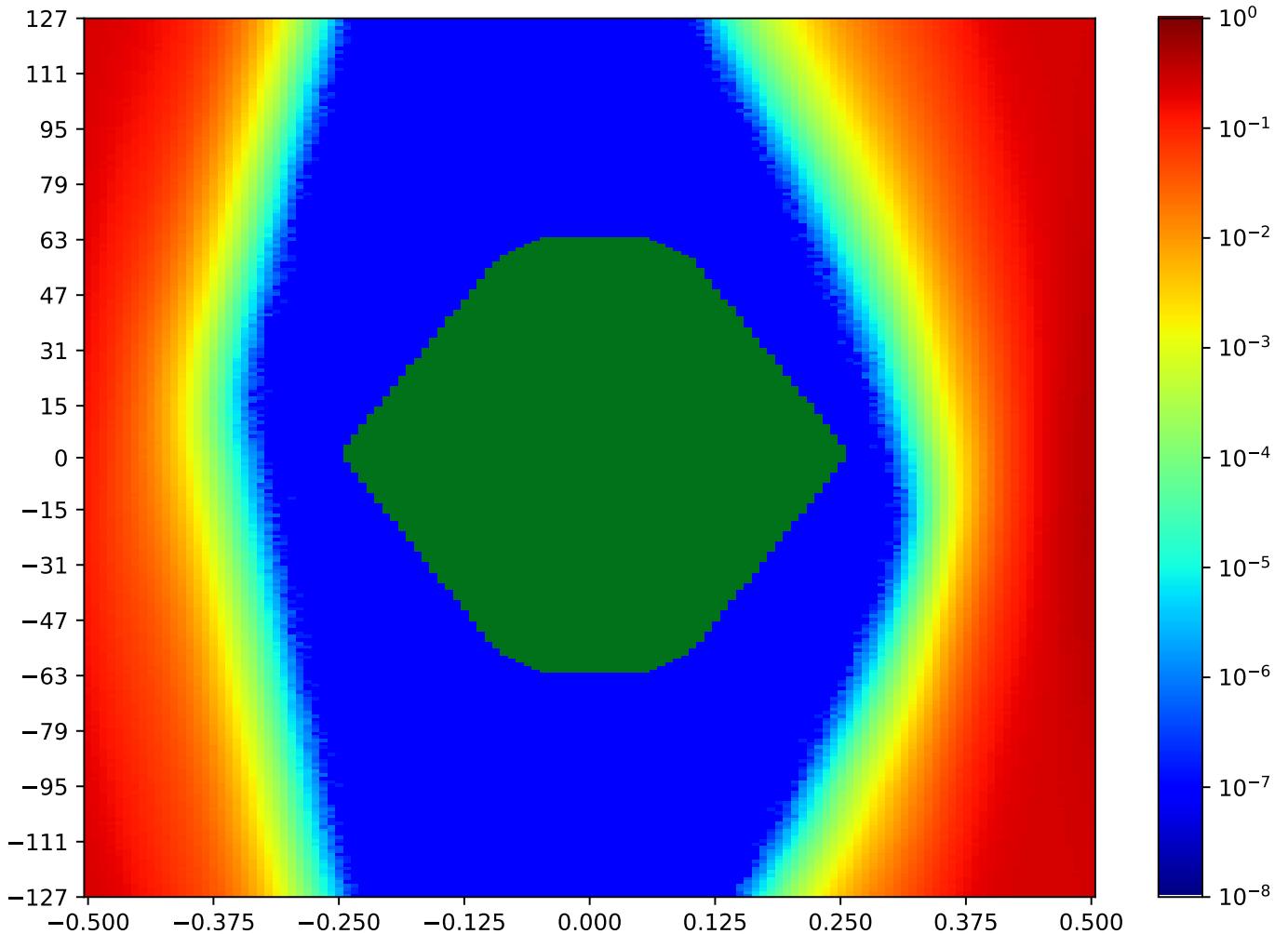


Figure 3.264: MSP_A_FPGA-TX2-10-RX12-10-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.20.12 MSP_A_FPGA-TX2-11-RX12-11-MSP_C_FPGA

Table 3.245: MSP_A_FPGA-TX2-11-RX12-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:51:05		2018-Jan-24 01:51:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16455	74	57.36%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

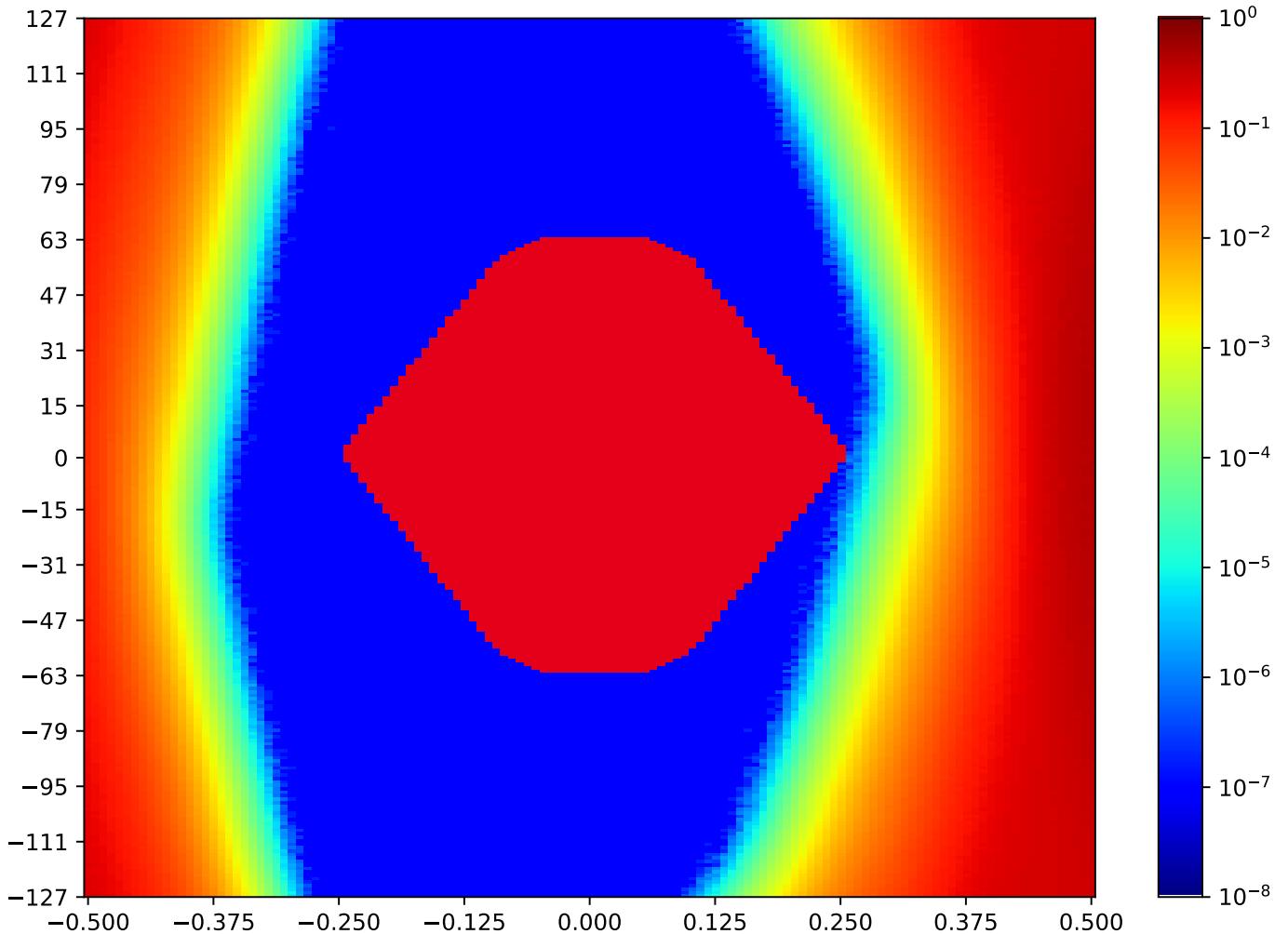


Figure 3.265: MSP_A_FPGA-TX2-11-RX12-11-MSP_C_FPGA

Call back to summary Figure 3.253. Sibling eye diagrams: V1-6.4.

3.21 MSP_C TX3 MSP_A RX4 Minipod Loopback

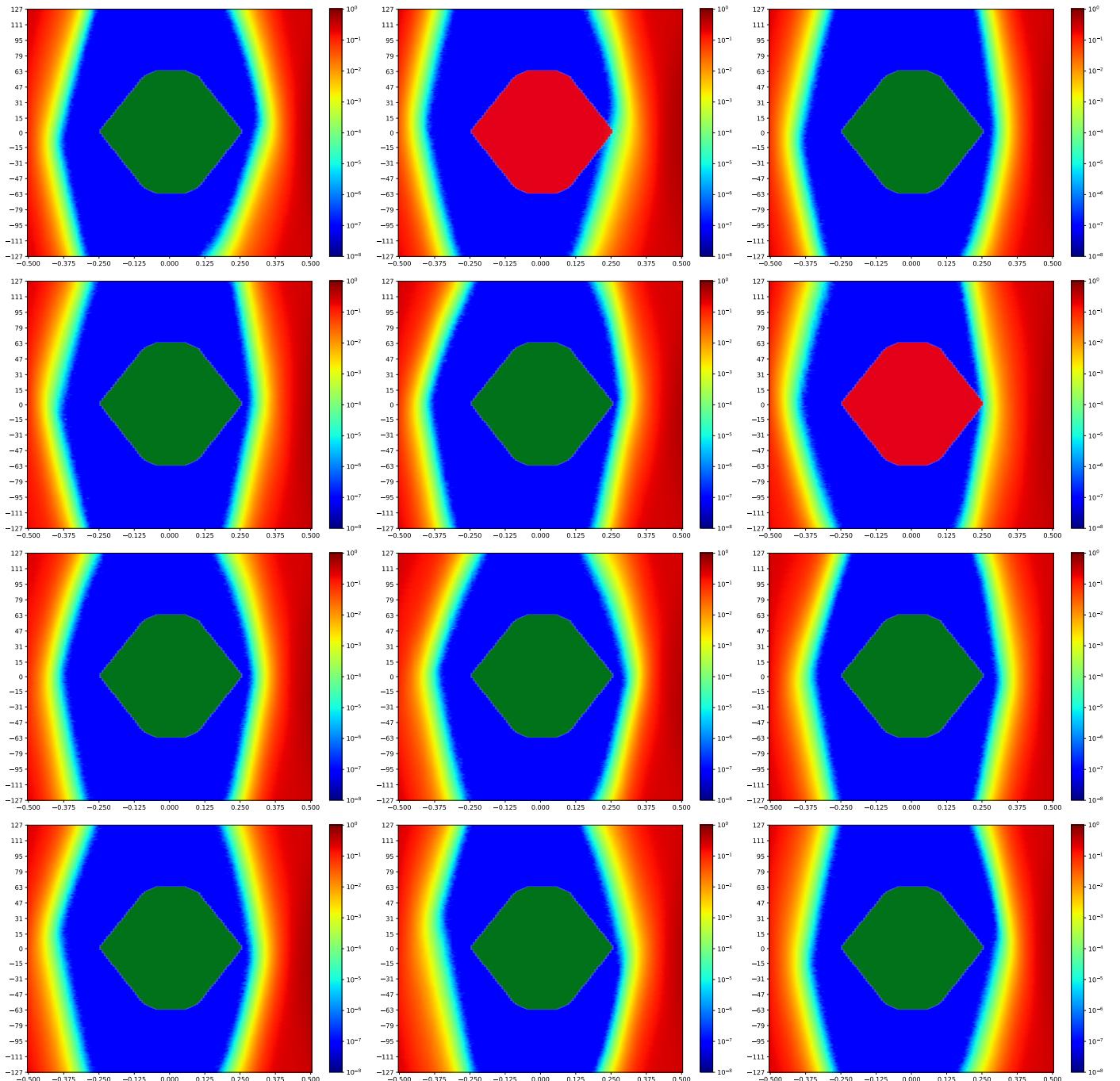


Figure 3.266: MSP_C TX3 MSP_A RX4 Minipod Loopback

A cross-reference to Figure 3.266. Sibling eye diagrams: V1-6.4.

Next summary Figure 3.279.

3.21.1 MSP_C_FPGA-TX3-00-RX4-00-MSP_A_FPGA

Table 3.246: MSP_C_FPGA-TX3-00-RX4-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:56:47		2018-Jan-24 01:57:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18014	83	64.34%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

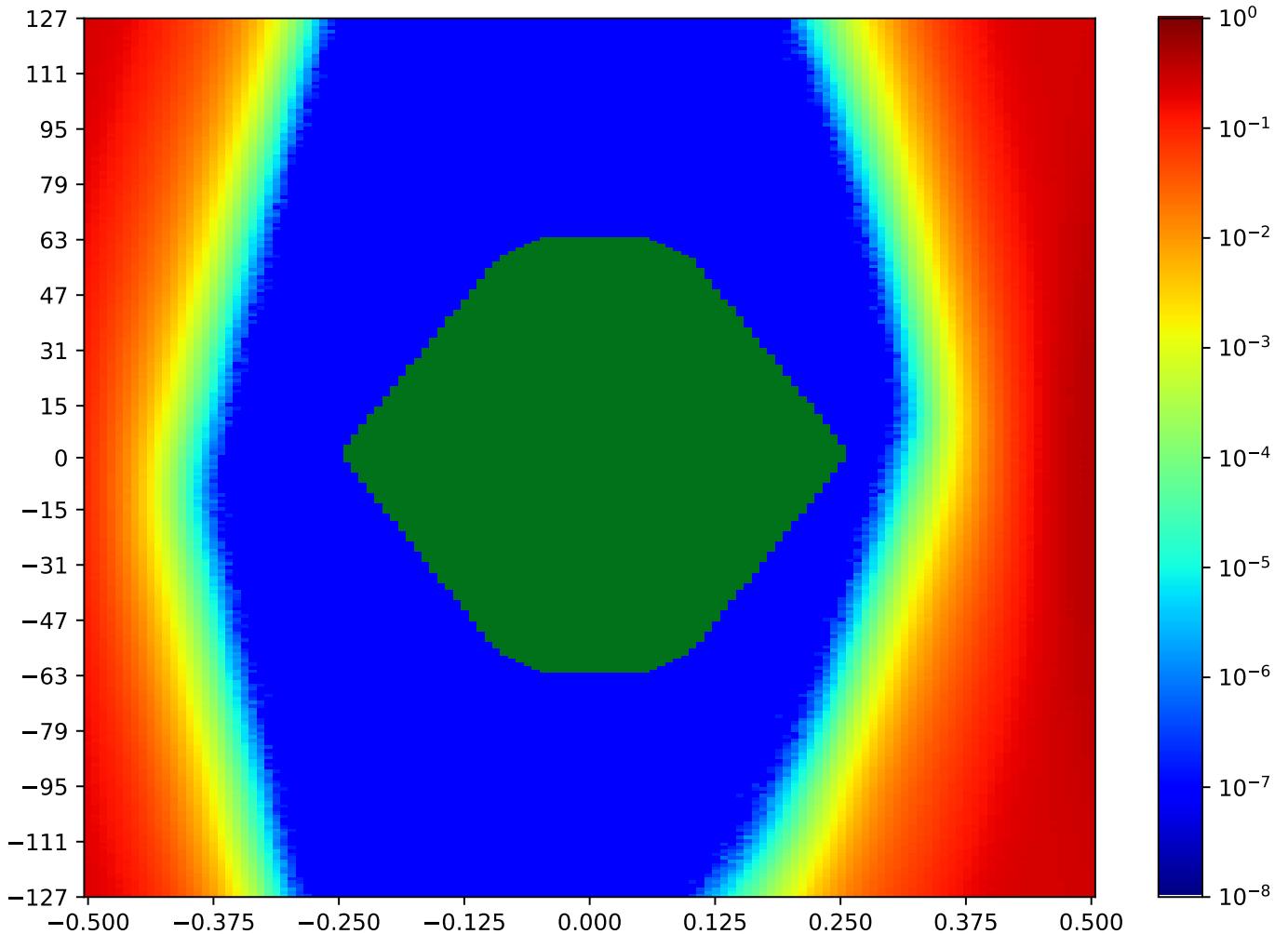


Figure 3.267: MSP_C_FPGA-TX3-00-RX4-00-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.2 MSP_C_FPGA-TX3-01-RX4-01-MSP_A_FPGA

Table 3.247: MSP_C_FPGA-TX3-01-RX4-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:58:12		2018-Jan-24 01:58:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16973	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

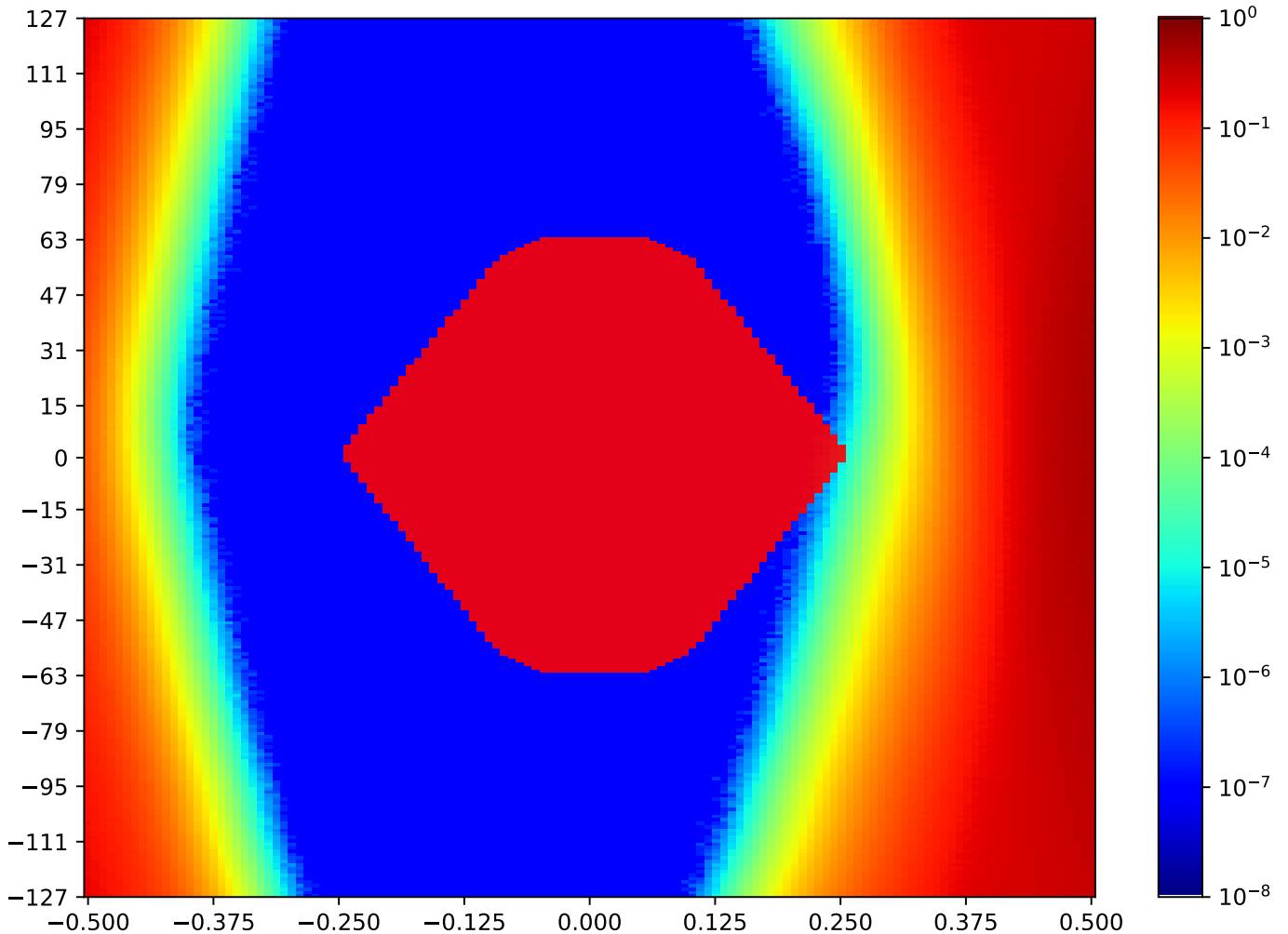


Figure 3.268: MSP_C_FPGA-TX3-01-RX4-01-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.3 MSP_C_FPGA-TX3-02-RX4-02-MSP_A_FPGA

Table 3.248: MSP_C_FPGA-TX3-02-RX4-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:58:55		2018-Jan-24 01:59:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	18448	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

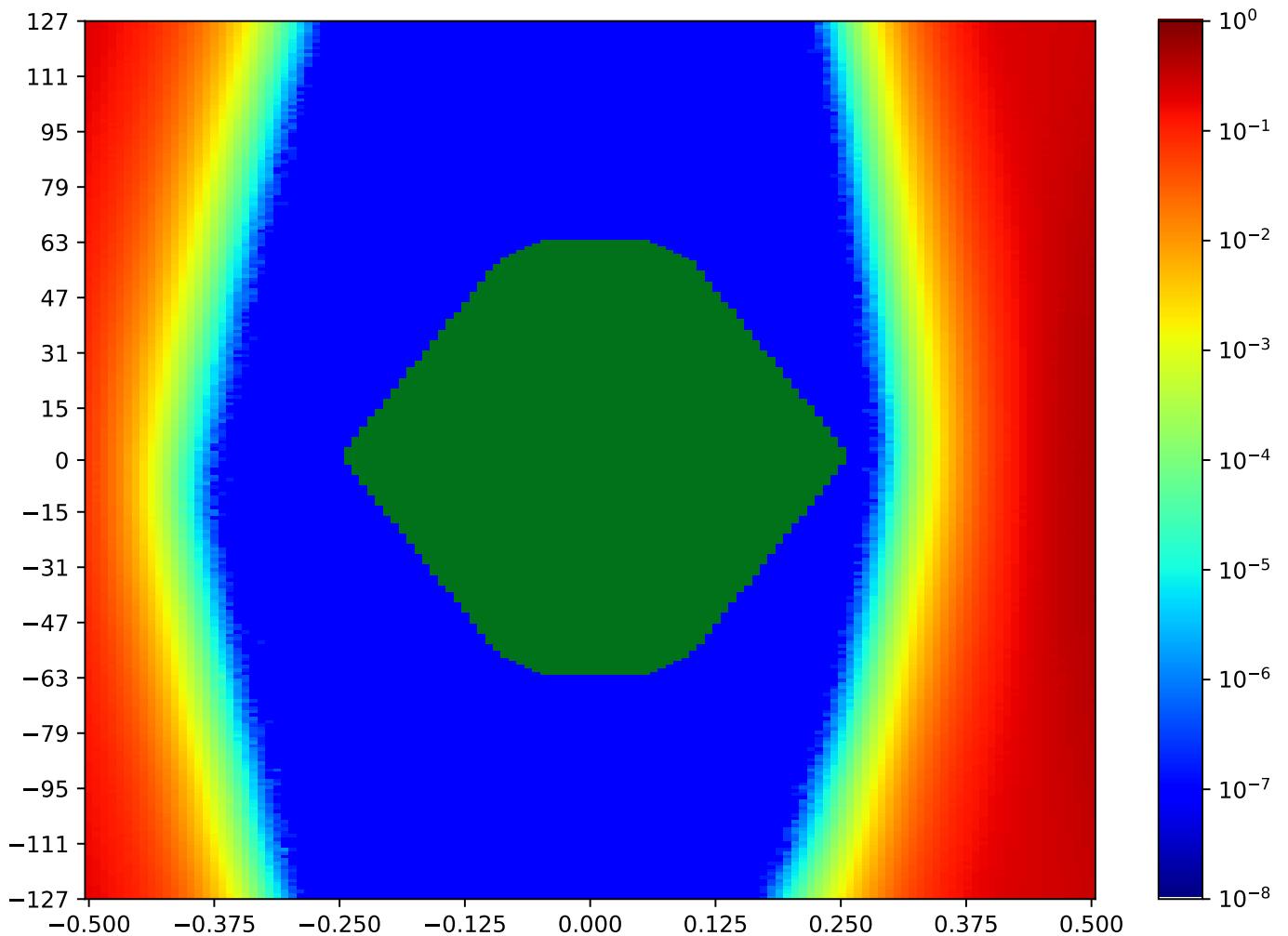


Figure 3.269: MSP_C_FPGA-TX3-02-RX4-02-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.4 MSP_C_FPGA-TX3-03-RX4-03-MSP_A_FPGA

Table 3.249: MSP_C_FPGA-TX3-03-RX4-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:55:21		2018-Jan-24 01:56:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17991	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

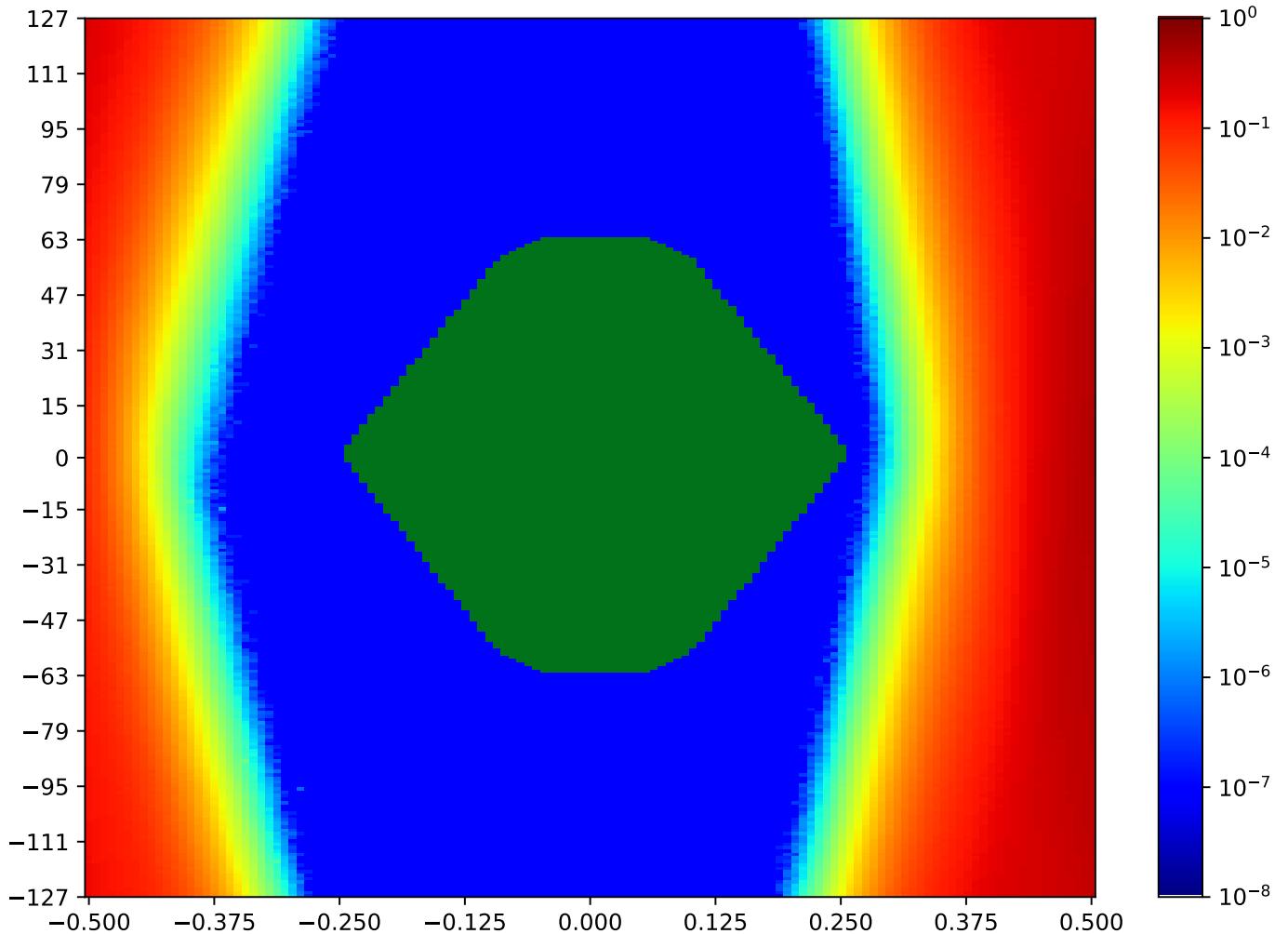


Figure 3.270: MSP_C_FPGA-TX3-03-RX4-03-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.5 MSP_C_FPGA-TX3-04-RX4-04-MSP_A_FPGA

Table 3.250: MSP_C_FPGA-TX3-04-RX4-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:01:03		2018-Jan-24 02:01:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17509	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

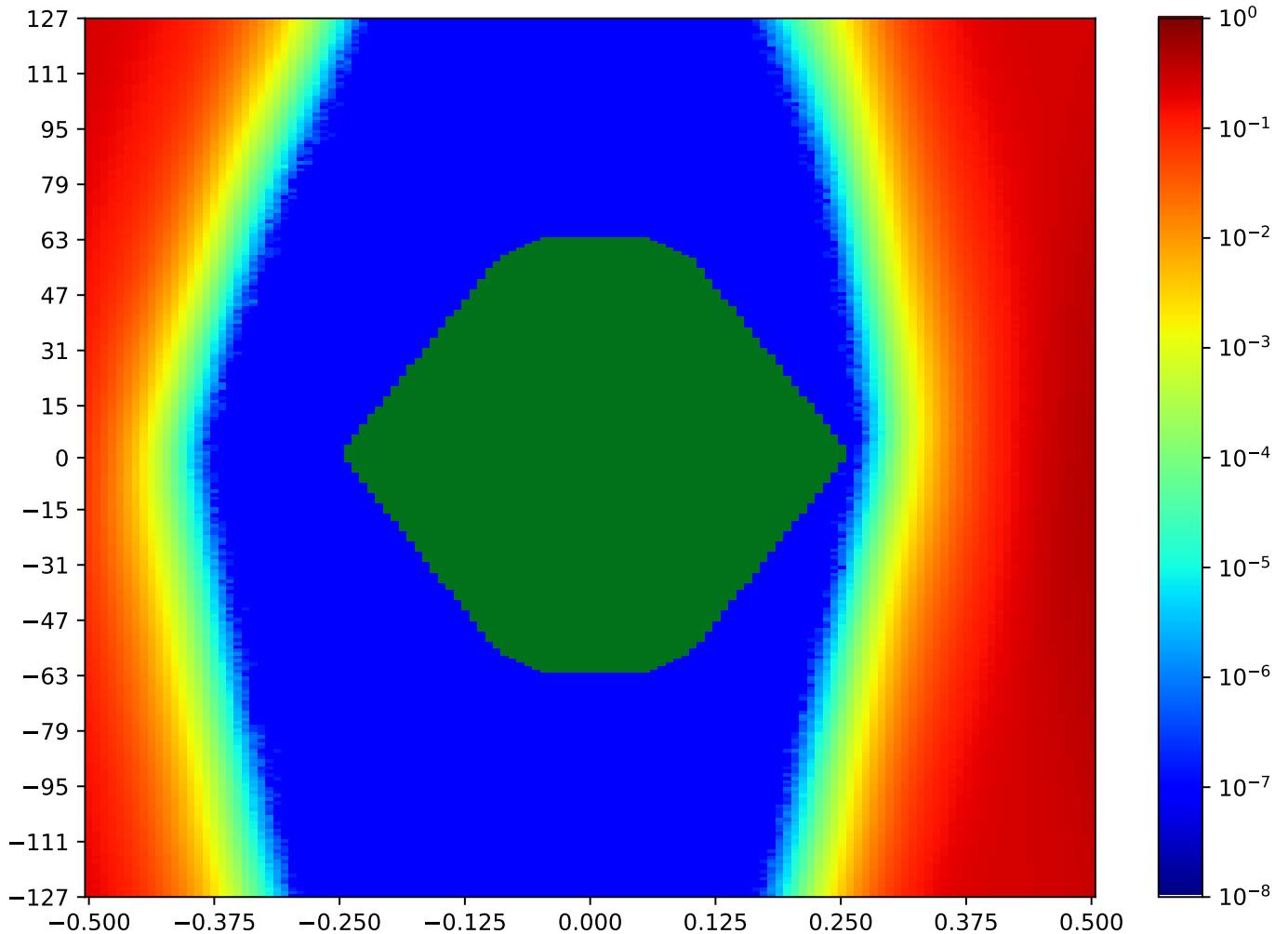


Figure 3.271: MSP_C_FPGA-TX3-04-RX4-04-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.6 MSP_C_FPGA-TX3-05-RX4-05-MSP_A_FPGA

Table 3.251: MSP_C_FPGA-TX3-05-RX4-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:54:38		2018-Jan-24 01:55:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16706	79	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

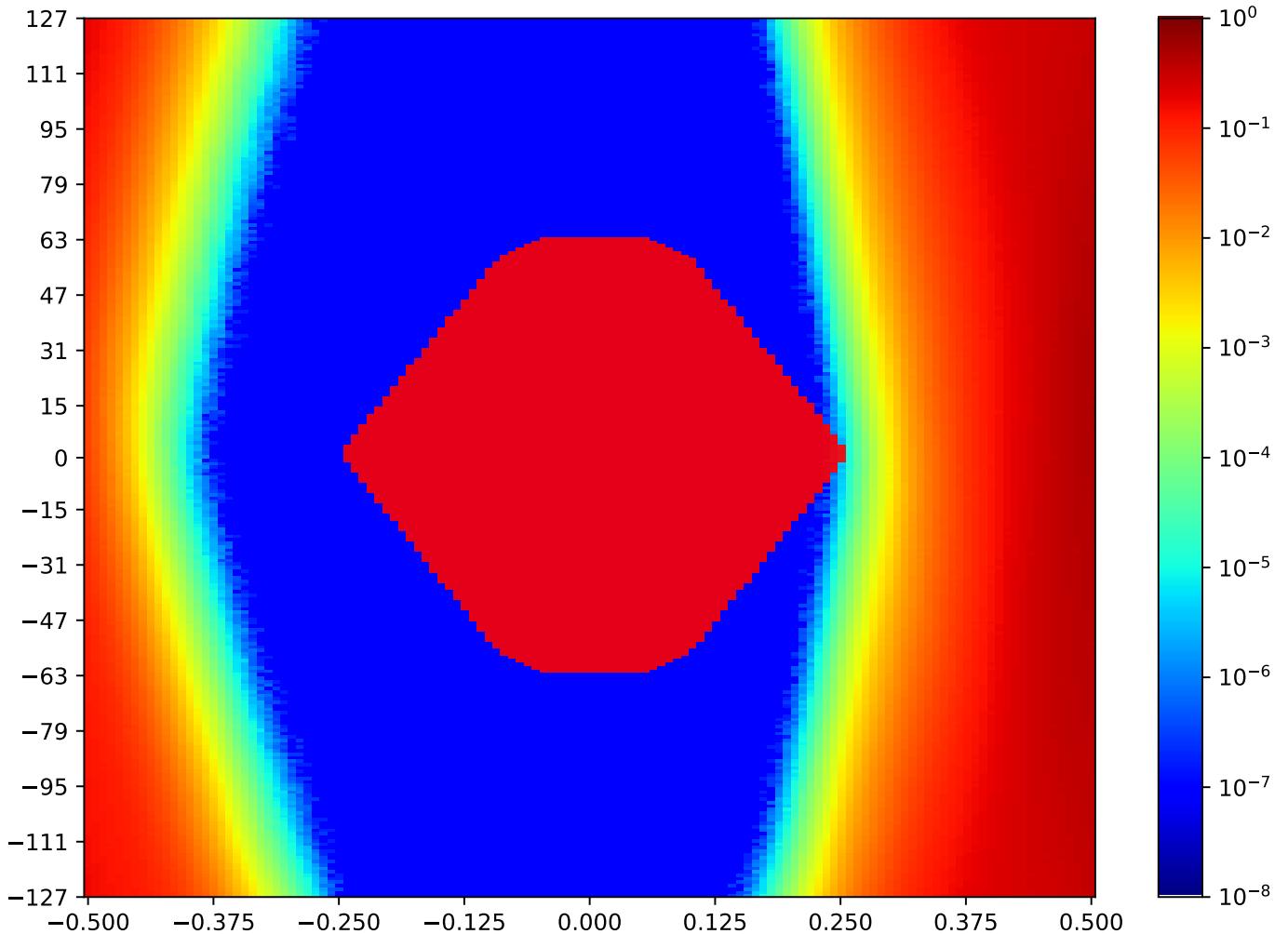


Figure 3.272: MSP_C_FPGA-TX3-05-RX4-05-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.7 MSP_C_FPGA-TX3-06-RX4-06-MSP_A_FPGA

Table 3.252: MSP_C_FPGA-TX3-06-RX4-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:02:28		2018-Jan-24 02:03:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17653	82	63.57%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

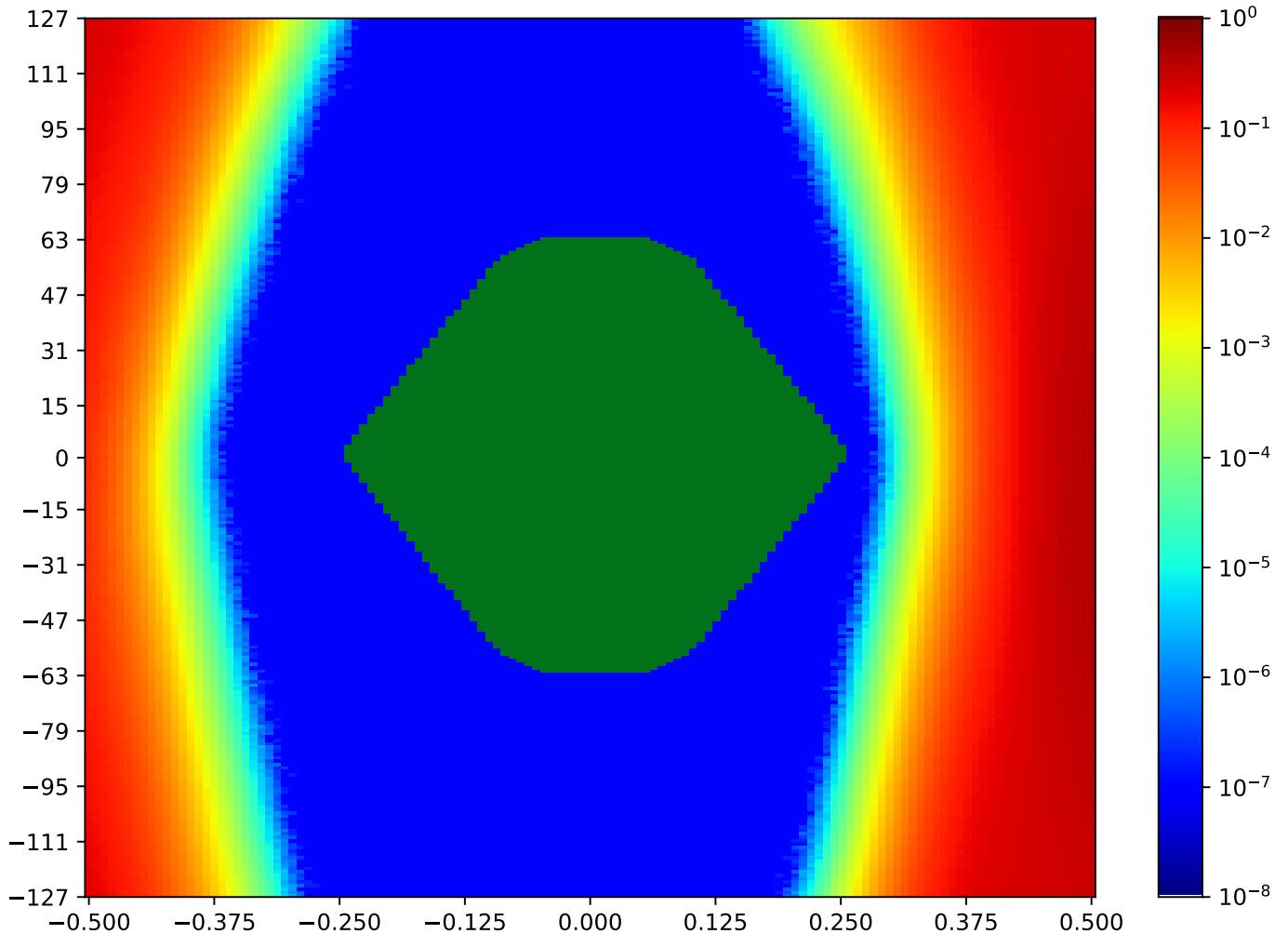


Figure 3.273: MSP_C_FPGA-TX3-06-RX4-06-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.8 MSP_C_FPGA-TX3-07-RX4-07-MSP_A_FPGA

Table 3.253: MSP_C_FPGA-TX3-07-RX4-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:56:04		2018-Jan-24 01:56:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16549	79	61.24%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

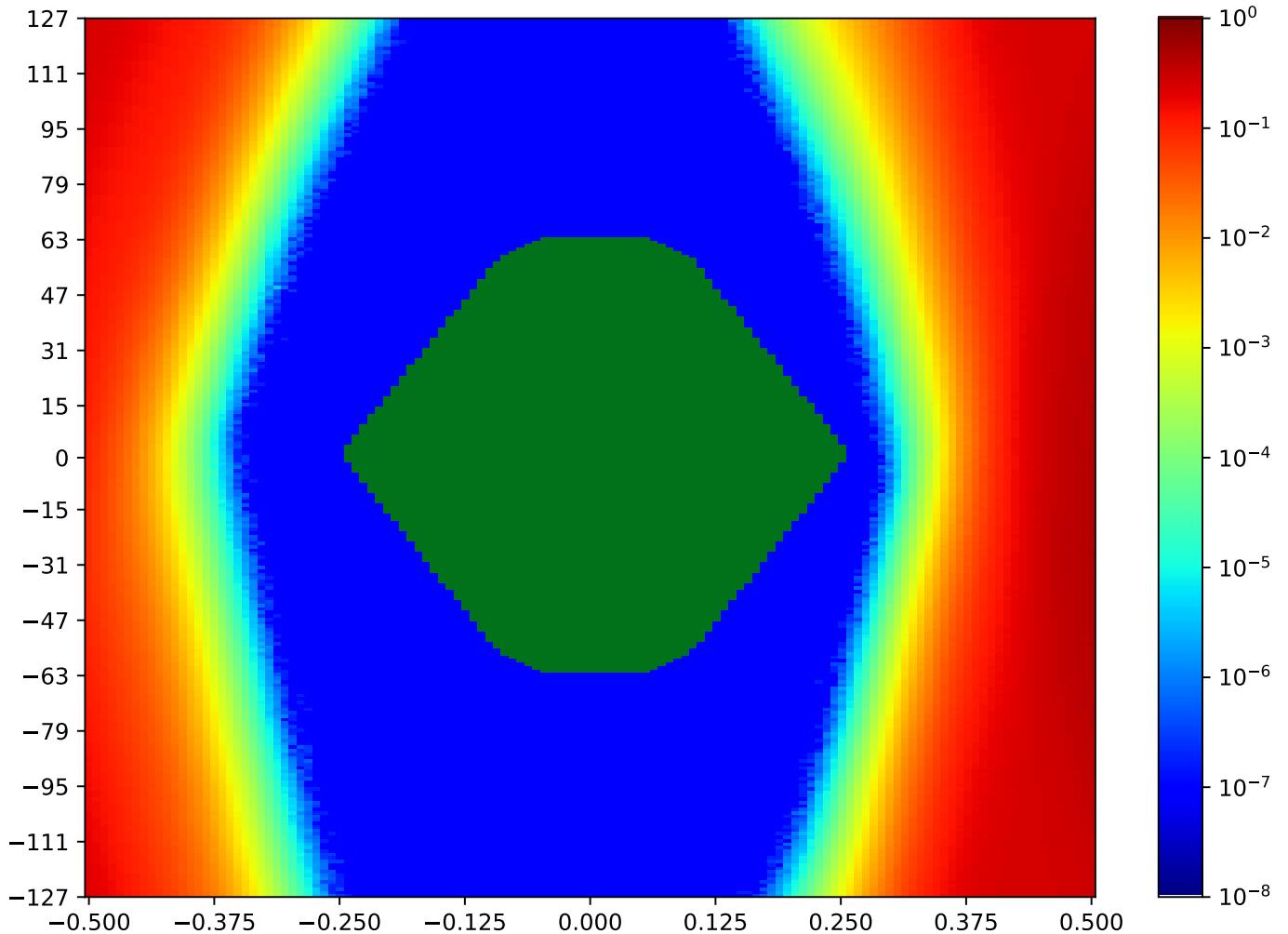


Figure 3.274: MSP_C_FPGA-TX3-07-RX4-07-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.9 MSP_C_FPGA-TX3-08-RX4-08-MSP_A_FPGA

Table 3.254: MSP_C_FPGA-TX3-08-RX4-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:01:45		2018-Jan-24 02:02:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17330	77	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

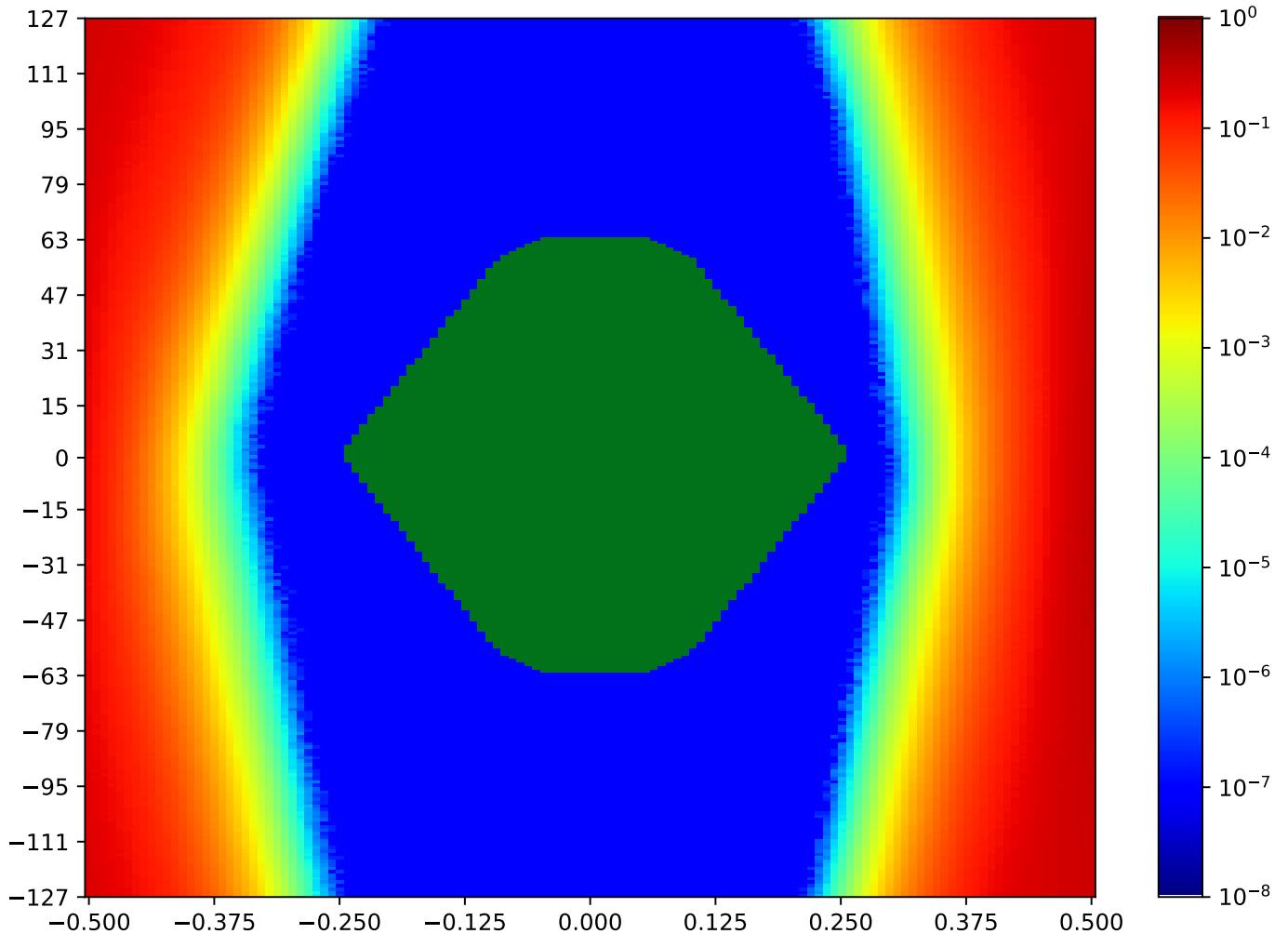


Figure 3.275: MSP_C_FPGA-TX3-08-RX4-08-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.10 MSP_C_FPGA-TX3-09-RX4-09-MSP_A_FPGA

Table 3.255: MSP_C_FPGA-TX3-09-RX4-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:57:30		2018-Jan-24 01:58:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17489	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

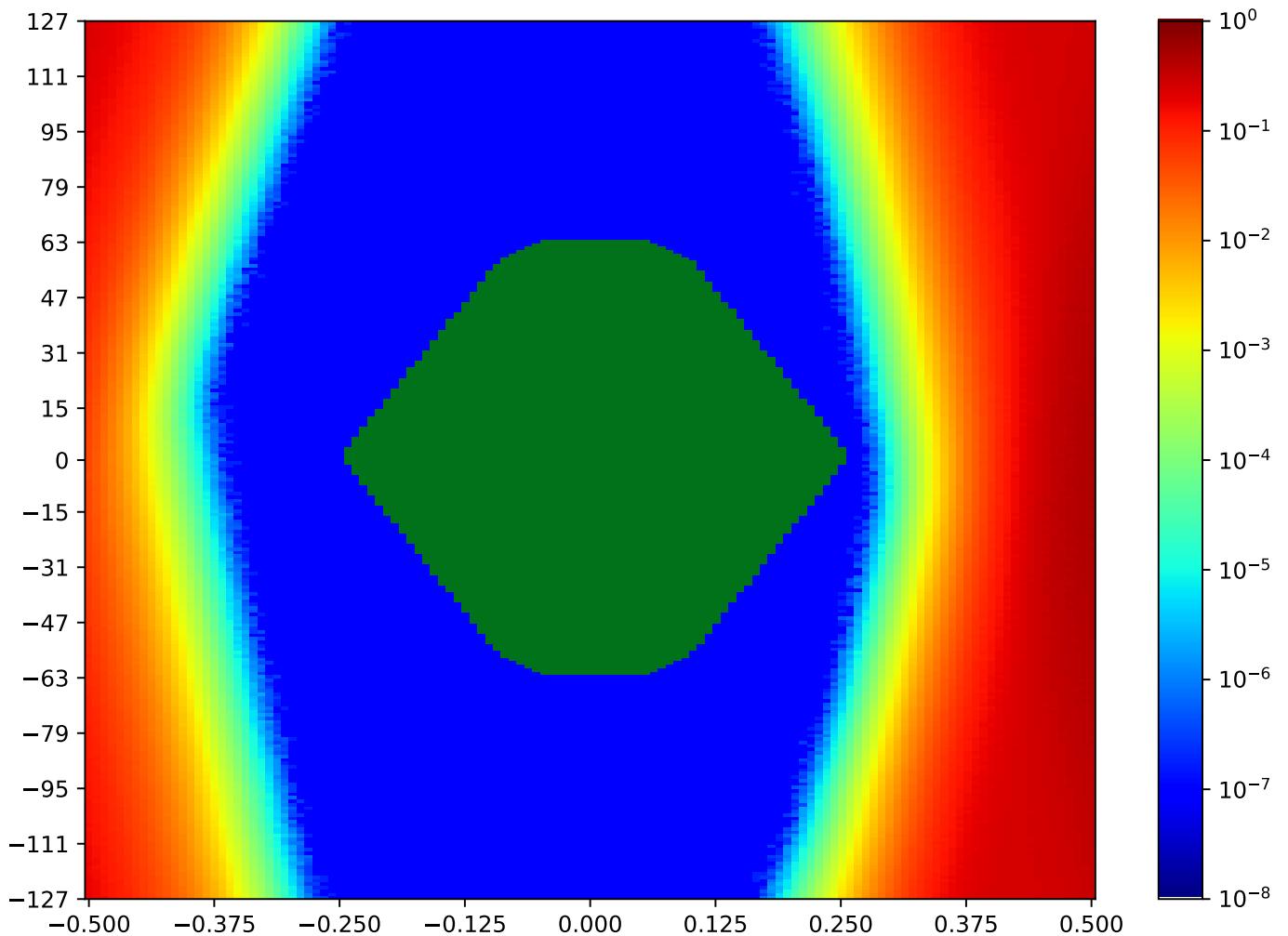


Figure 3.276: MSP_C_FPGA-TX3-09-RX4-09-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.11 MSP_C_FPGA-TX3-10-RX4-10-MSP_A_FPGA

Table 3.256: MSP_C_FPGA-TX3-10-RX4-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:00:20		2018-Jan-24 02:01:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16258	75	57.36%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

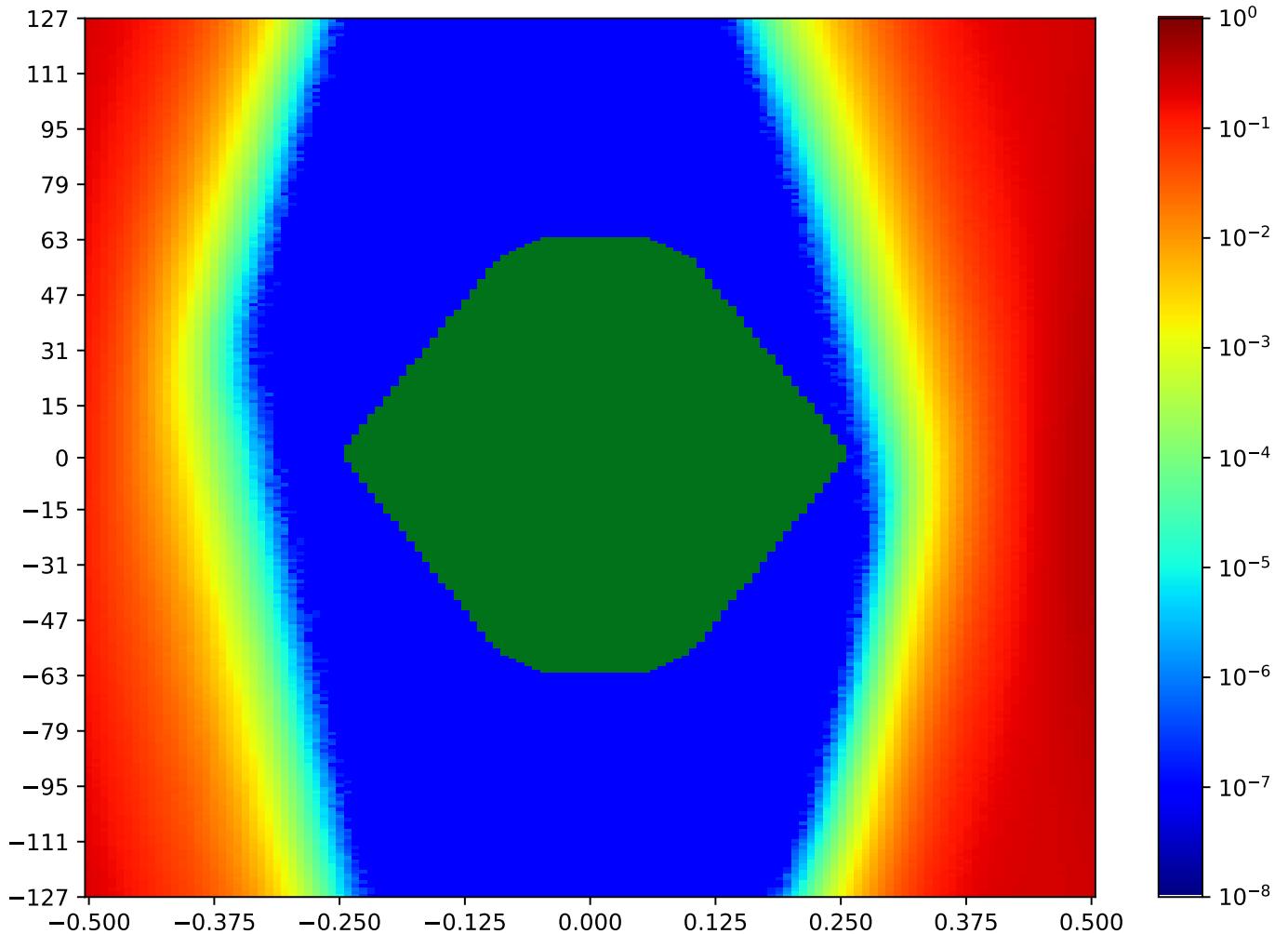


Figure 3.277: MSP_C_FPGA-TX3-10-RX4-10-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.21.12 MSP_C_FPGA-TX3-11-RX4-11-MSP_A_FPGA

Table 3.257: MSP_C_FPGA-TX3-11-RX4-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 01:59:37		2018-Jan-24 02:00:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17379	78	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

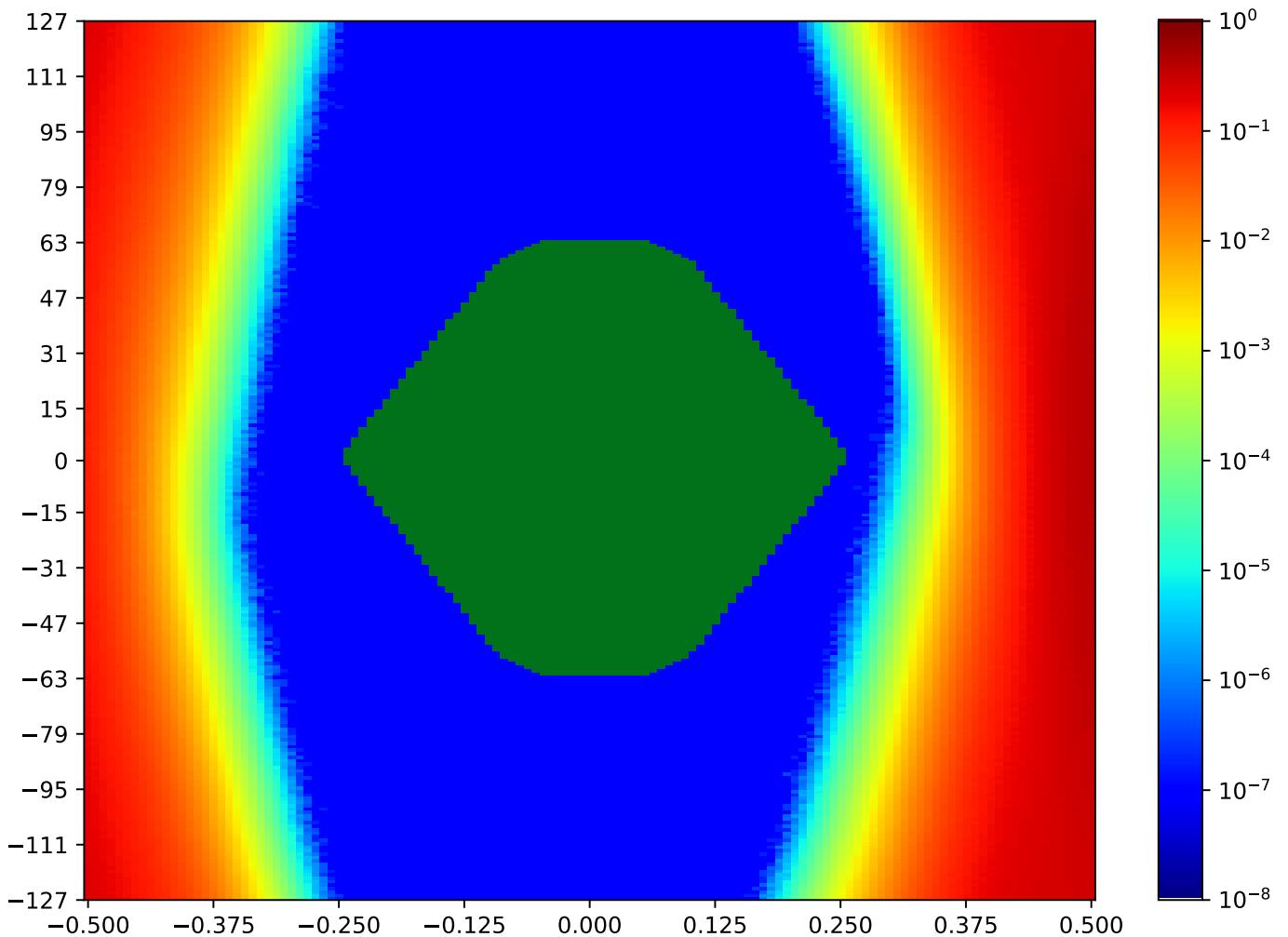


Figure 3.278: MSP_C_FPGA-TX3-11-RX4-11-MSP_A_FPGA

Call back to summary Figure 3.266. Sibling eye diagrams: V1-6.4.

3.22 MSP_C TX4 MSP_A RX3 Minipod Loopback

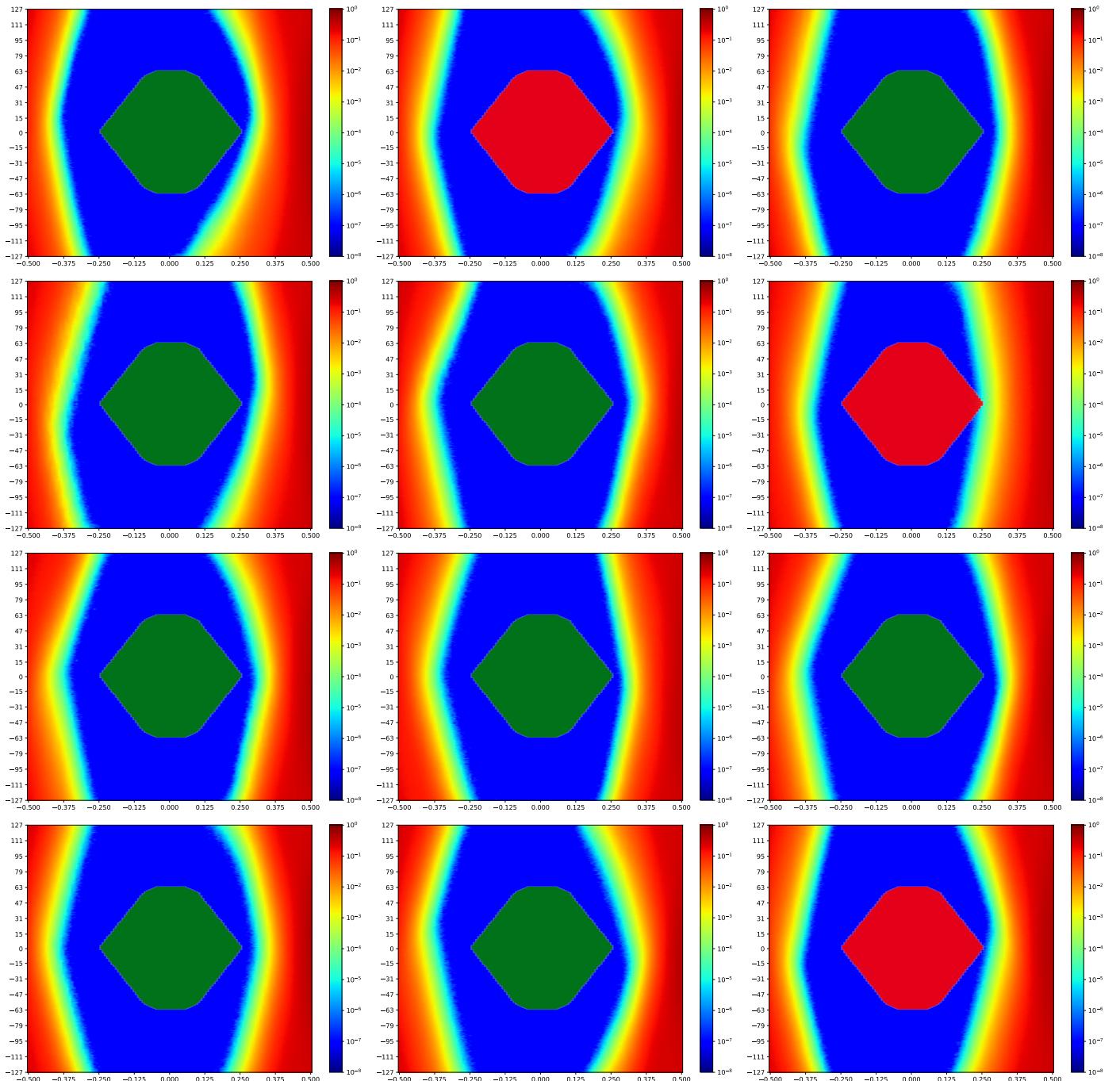


Figure 3.279: MSP_C TX4 MSP_A RX3 Minipod Loopback

A cross-reference to Figure 3.279. Sibling eye diagrams: V1-6.4.

Next summary Figure ??.

3.22.1 MSP_C_FPGA-TX4-00-RX3-00-MSP_A_FPGA

Table 3.258: MSP_C_FPGA-TX4-00-RX3-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:05:18		2018-Jan-24 02:06:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16722	80	62.02%	254	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

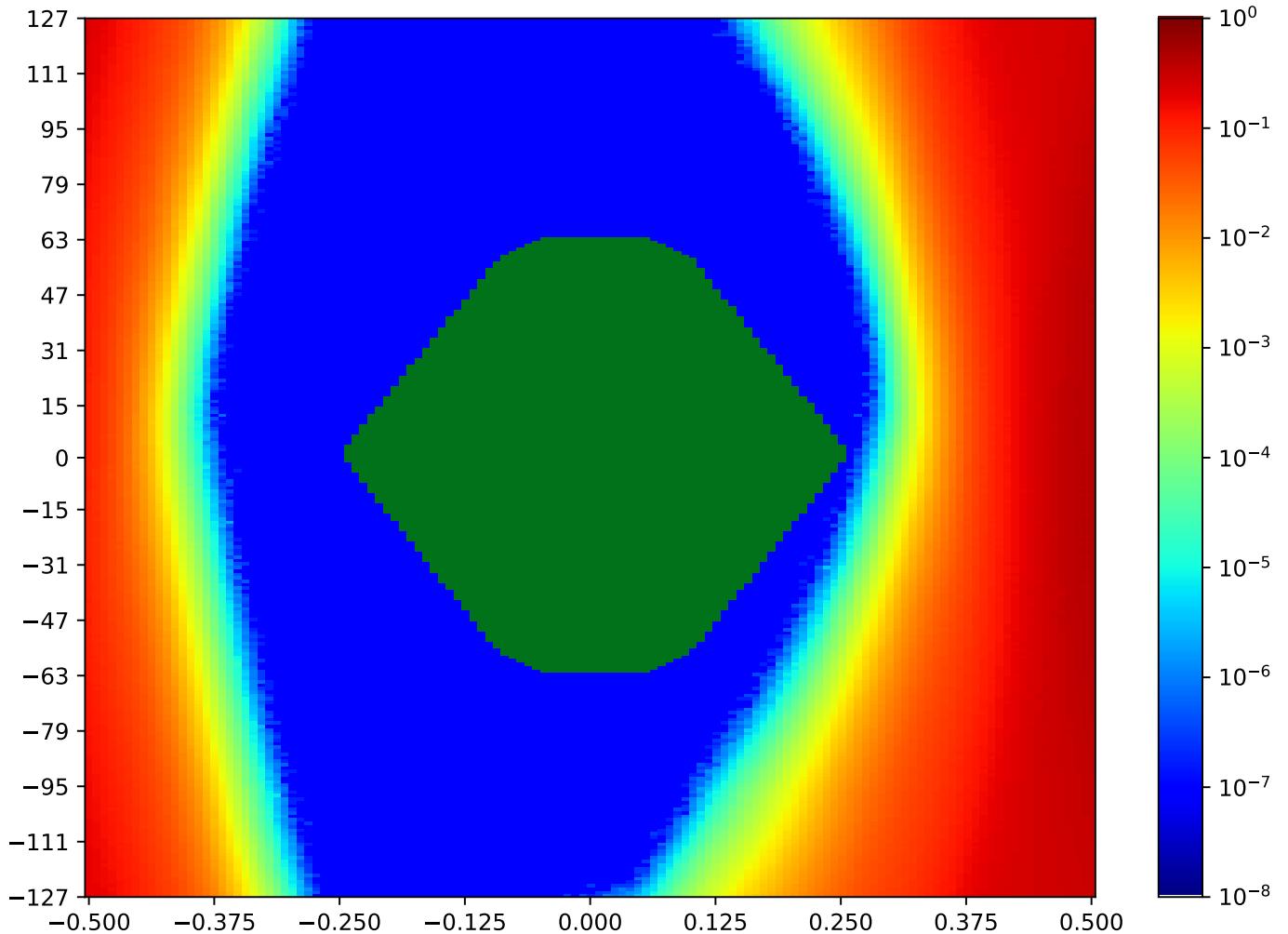


Figure 3.280: MSP_C_FPGA-TX4-00-RX3-00-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.2 MSP_C_FPGA-TX4-01-RX3-01-MSP_A_FPGA

Table 3.259: MSP_C_FPGA-TX4-01-RX3-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:03:53		2018-Jan-24 02:04:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16727	77	59.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

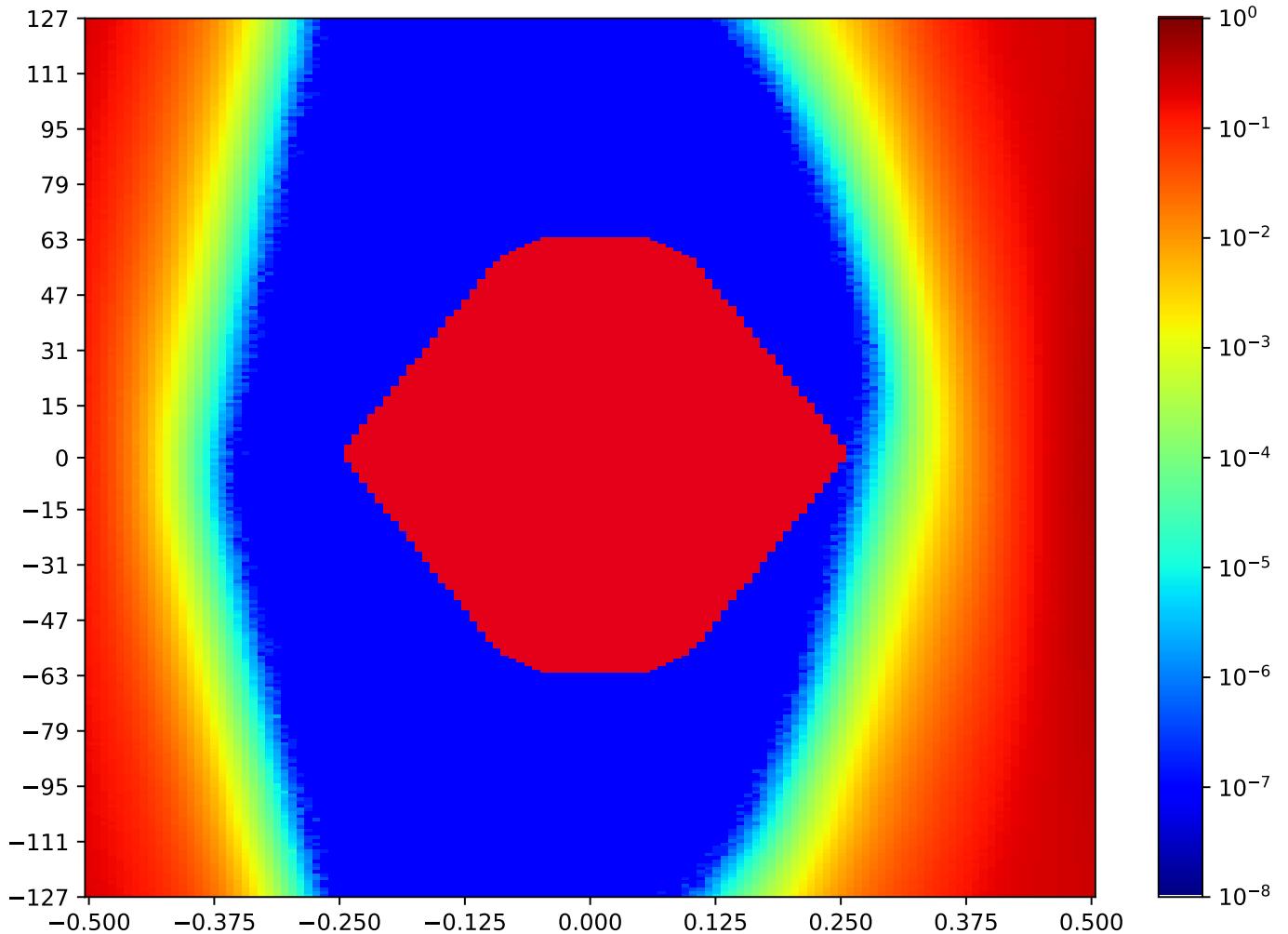


Figure 3.281: MSP_C_FPGA-TX4-01-RX3-01-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.3 MSP_C_FPGA-TX4-02-RX3-02-MSP_A_FPGA

Table 3.260: MSP_C_FPGA-TX4-02-RX3-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:07:29		2018-Jan-24 02:08:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17942	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

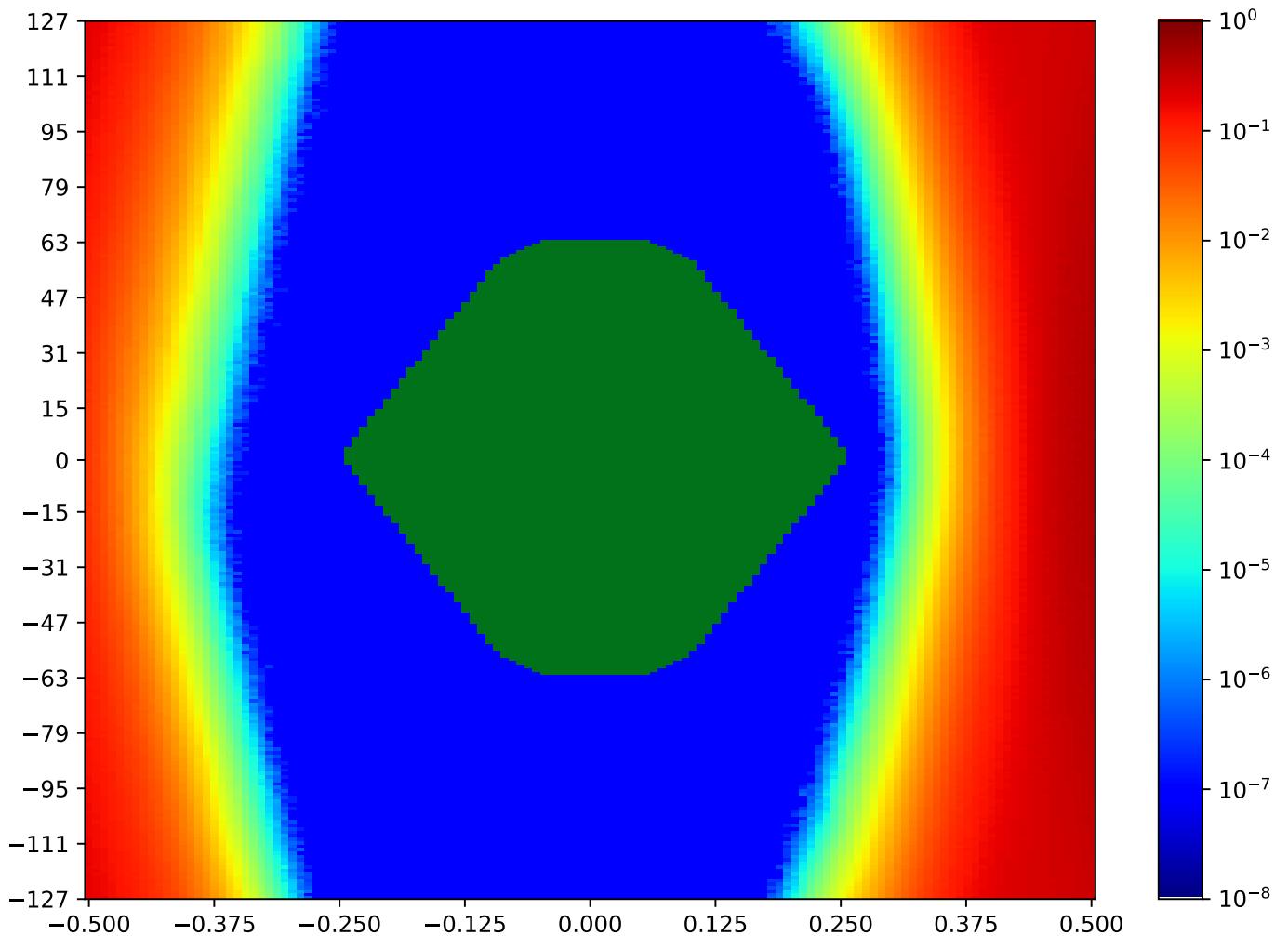


Figure 3.282: MSP_C_FPGA-TX4-02-RX3-02-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.4 MSP_C_FPGA-TX4-03-RX3-03-MSP_A_FPGA

Table 3.261: MSP_C_FPGA-TX4-03-RX3-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:03:10		2018-Jan-24 02:03:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16756	76	58.91%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

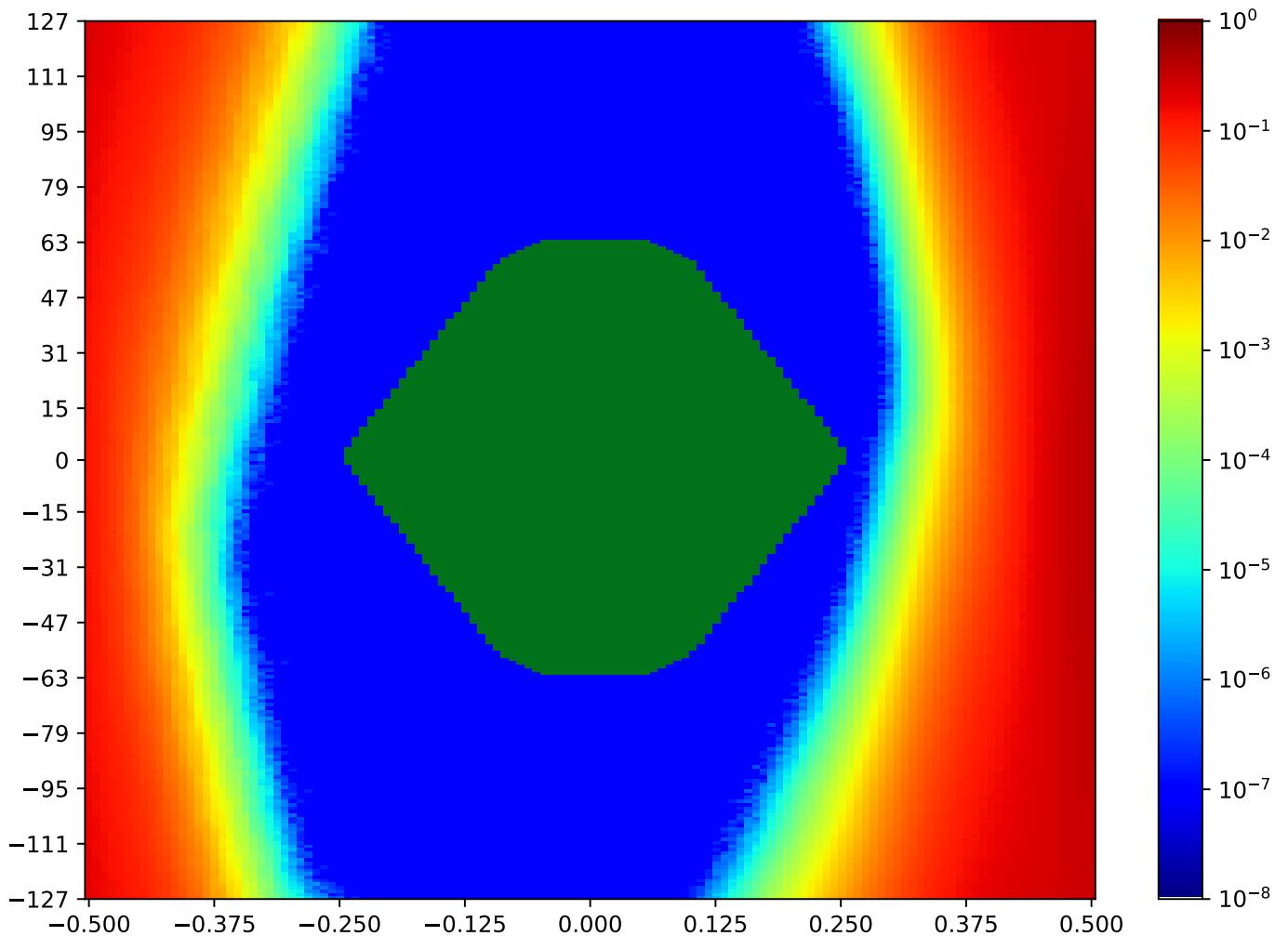


Figure 3.283: MSP_C_FPGA-TX4-03-RX3-03-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.5 MSP_C_FPGA-TX4-04-RX3-04-MSP_A_FPGA

Table 3.262: MSP_C_FPGA-TX4-04-RX3-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:09:36		2018-Jan-24 02:10:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17150	82	63.57%	254	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

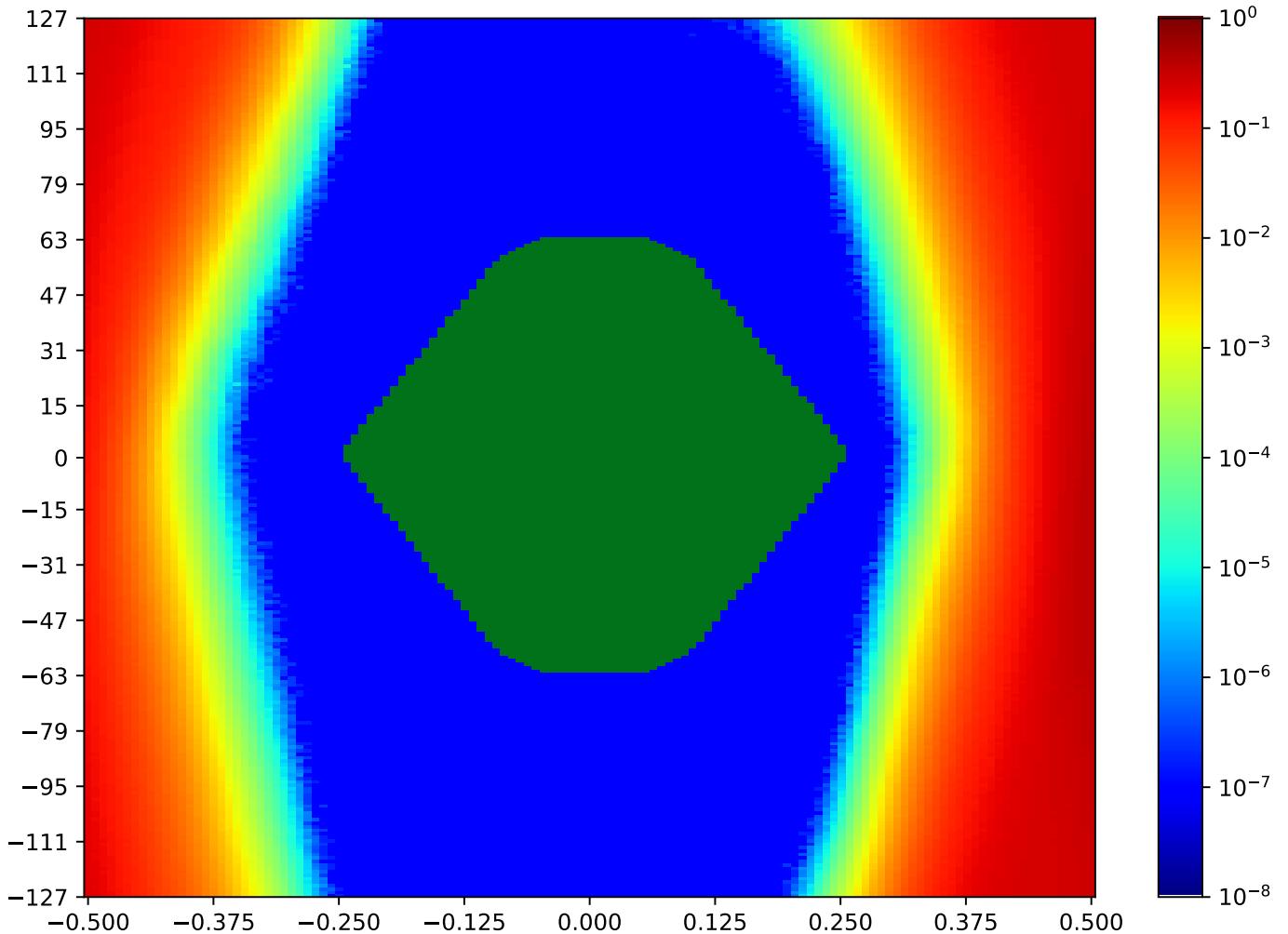


Figure 3.284: MSP_C_FPGA-TX4-04-RX3-04-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.6 MSP_C_FPGA-TX4-05-RX3-05-MSP_A_FPGA

Table 3.263: MSP_C_FPGA-TX4-05-RX3-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:04:36		2018-Jan-24 02:05:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	14794	68	52.71%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

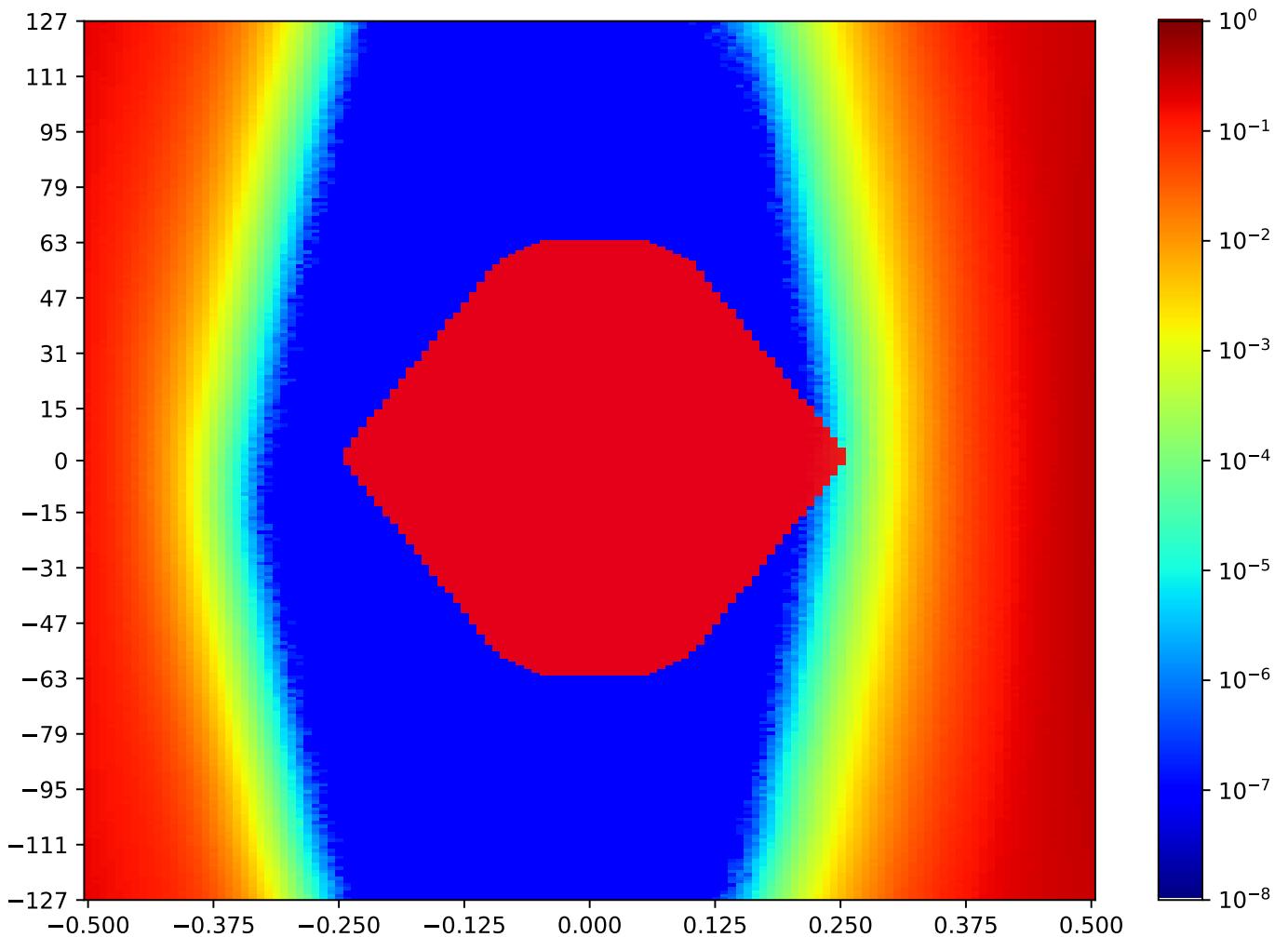


Figure 3.285: MSP_C_FPGA-TX4-05-RX3-05-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.7 MSP_C_FPGA-TX4-06-RX3-06-MSP_A_FPGA

Table 3.264: MSP_C_FPGA-TX4-06-RX3-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:11:01		2018-Jan-24 02:11:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16823	80	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

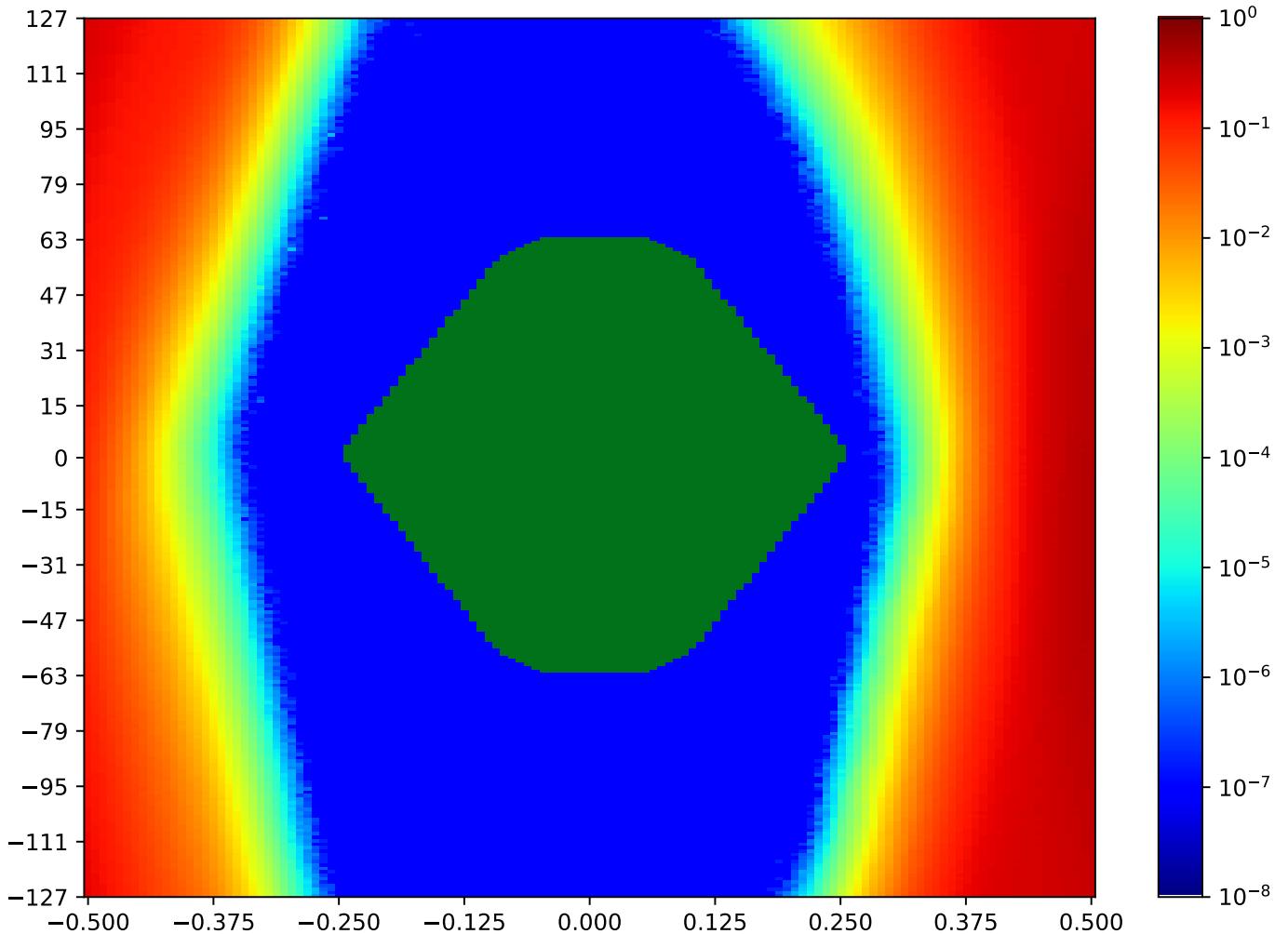


Figure 3.286: MSP_C_FPGA-TX4-06-RX3-06-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.8 MSP_C_FPGA-TX4-07-RX3-07-MSP_A_FPGA

Table 3.265: MSP_C_FPGA-TX4-07-RX3-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:06:01		2018-Jan-24 02:06:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16527	75	58.14%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

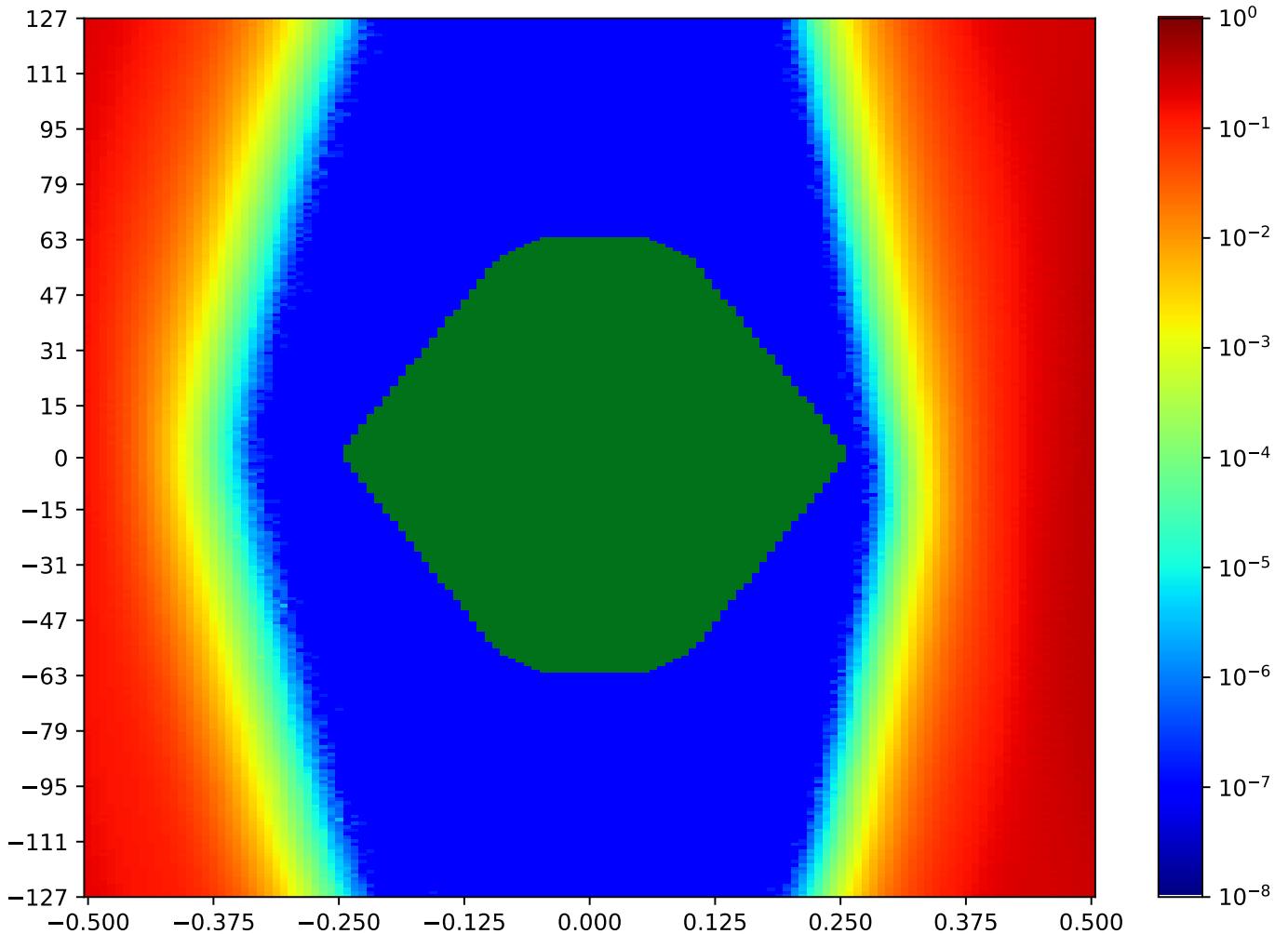


Figure 3.287: MSP_C_FPGA-TX4-07-RX3-07-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.9 MSP_C_FPGA-TX4-08-RX3-08-MSP_A_FPGA

Table 3.266: MSP_C_FPGA-TX4-08-RX3-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:10:19		2018-Jan-24 02:11:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17015	81	62.02%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

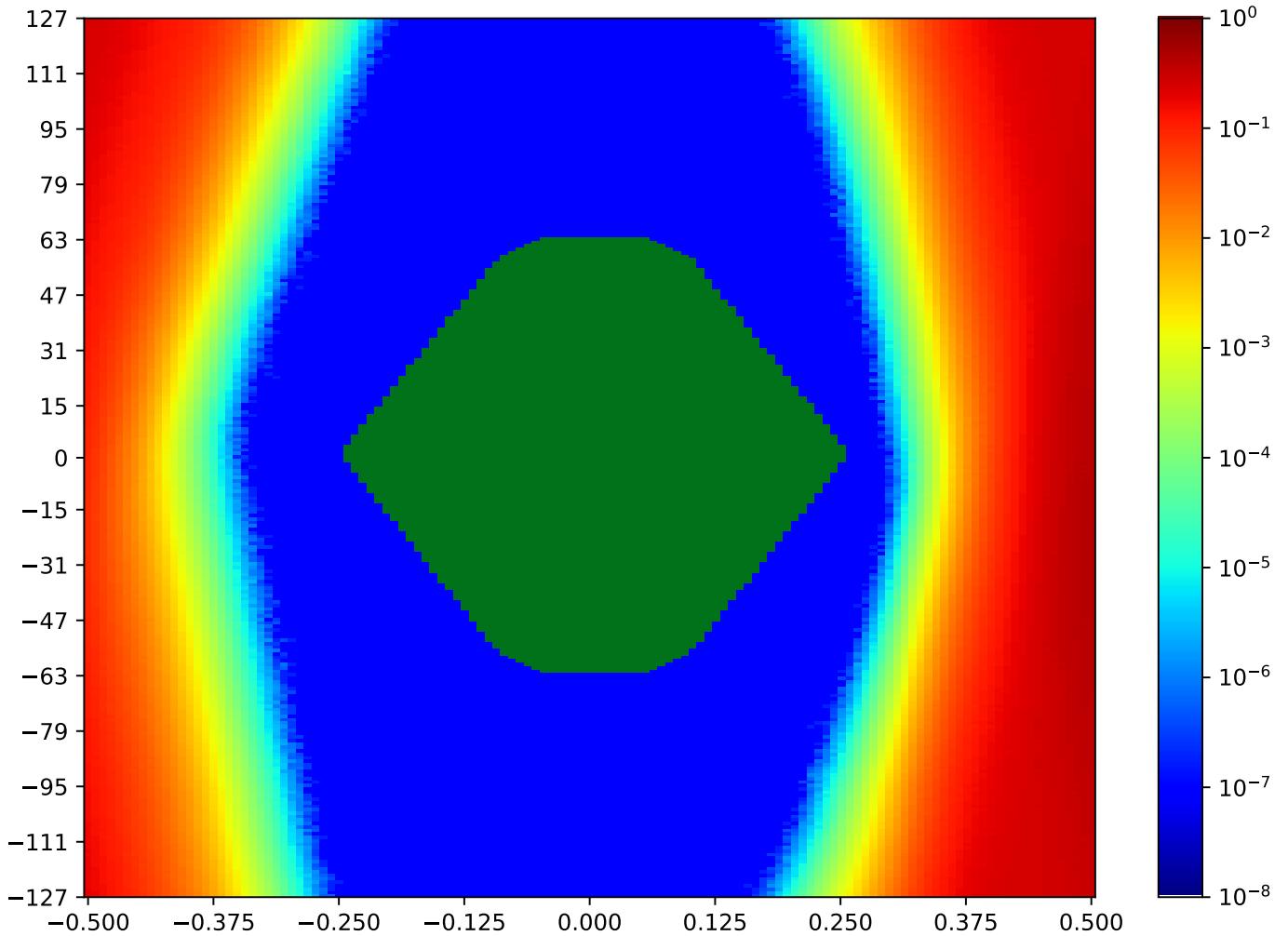


Figure 3.288: MSP_C_FPGA-TX4-08-RX3-08-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.10 MSP_C_FPGA-TX4-09-RX3-09-MSP_A_FPGA

Table 3.267: MSP_C_FPGA-TX4-09-RX3-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:06:45		2018-Jan-24 02:07:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17443	81	62.79%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

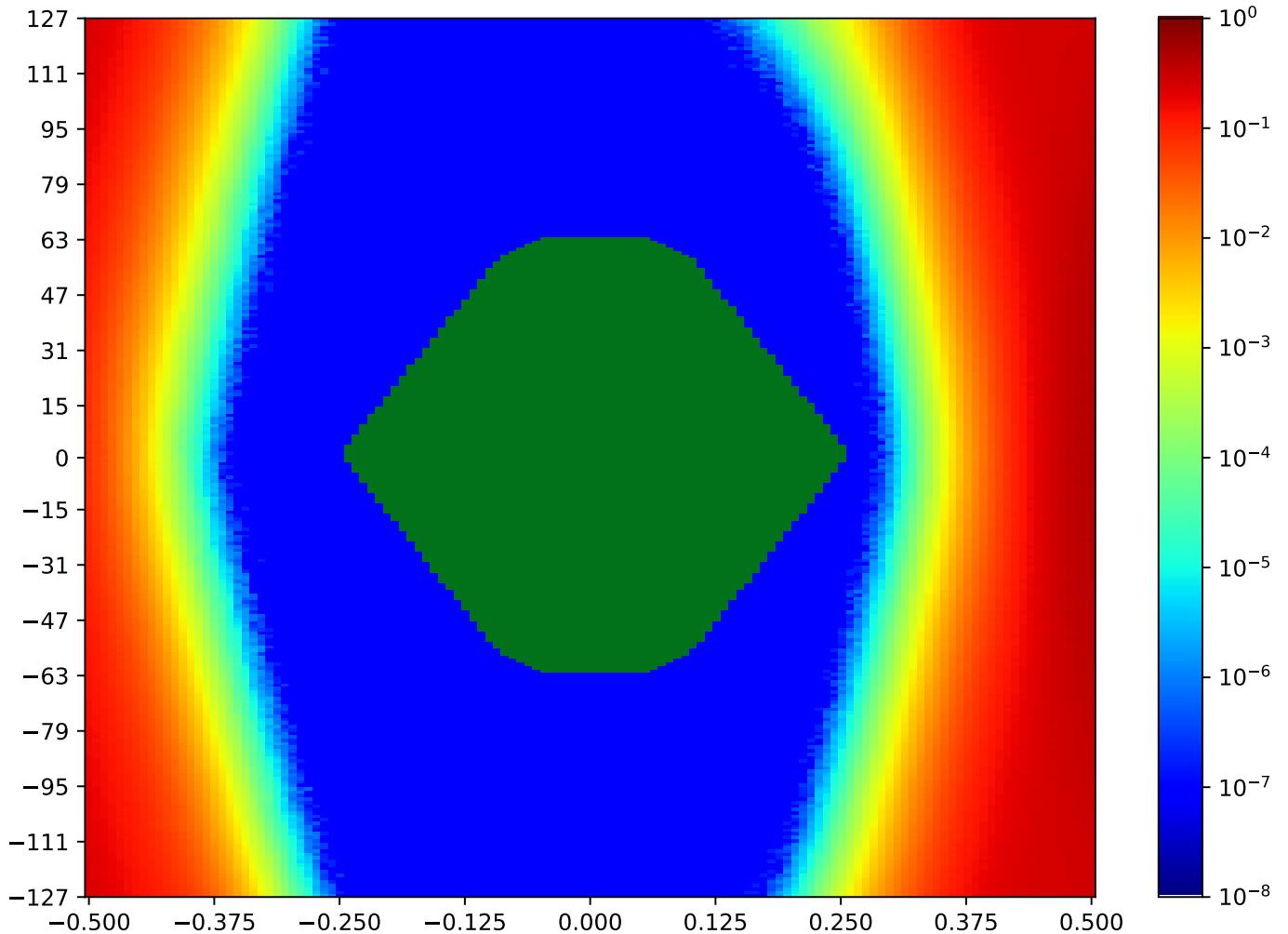


Figure 3.289: MSP_C_FPGA-TX4-09-RX3-09-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.11 MSP_C_FPGA-TX4-10-RX3-10-MSP_A_FPGA

Table 3.268: MSP_C_FPGA-TX4-10-RX3-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:08:54		2018-Jan-24 02:09:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	16654	79	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

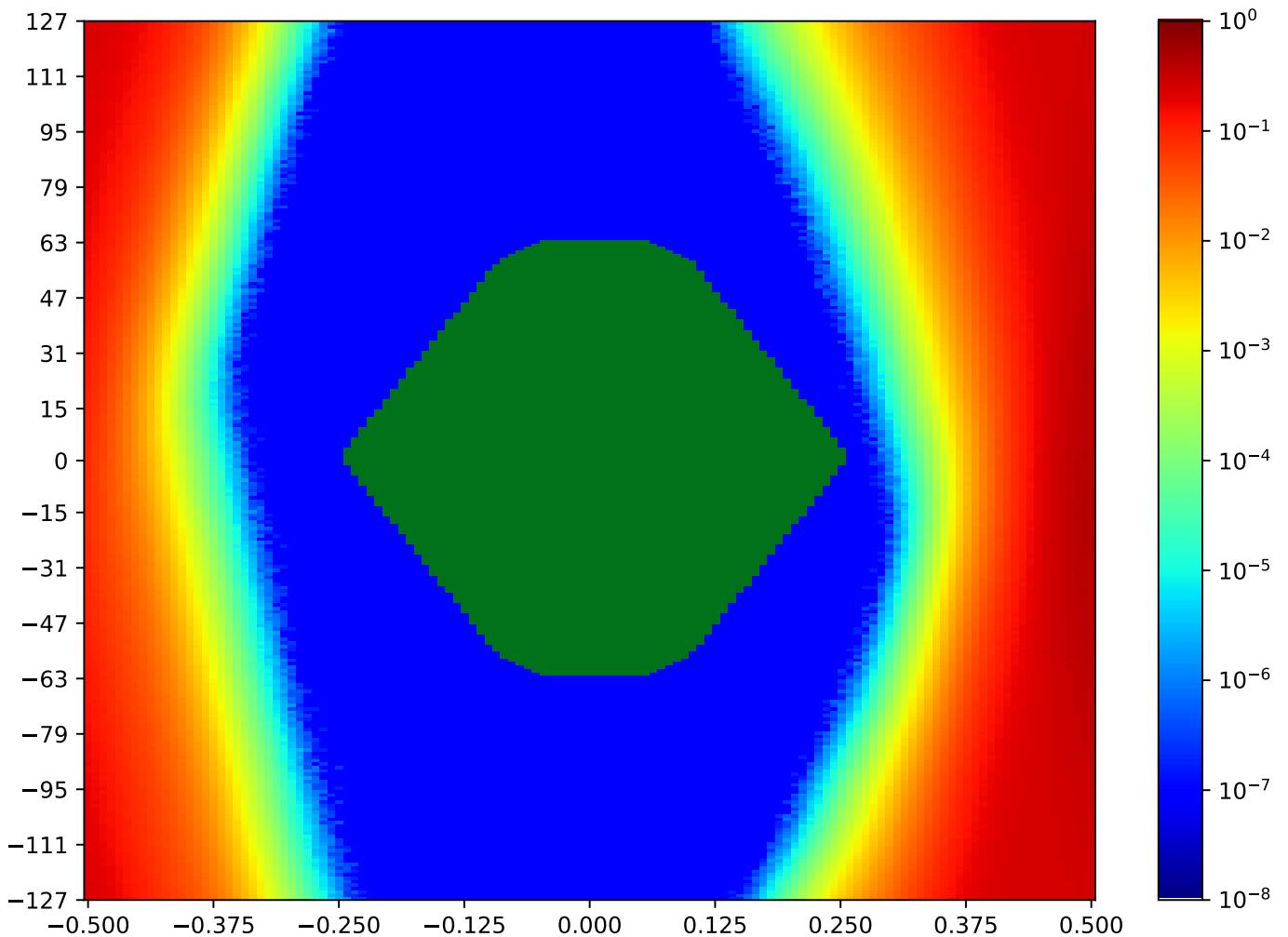


Figure 3.290: MSP_C_FPGA-TX4-10-RX3-10-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

3.22.12 MSP_C_FPGA-TX4-11-RX3-11-MSP_A_FPGA

Table 3.269: MSP_C_FPGA-TX4-11-RX3-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.2	UltraScale GTY	2018-Jan-24 02:08:11		2018-Jan-24 02:08:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	17251	78	60.47%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

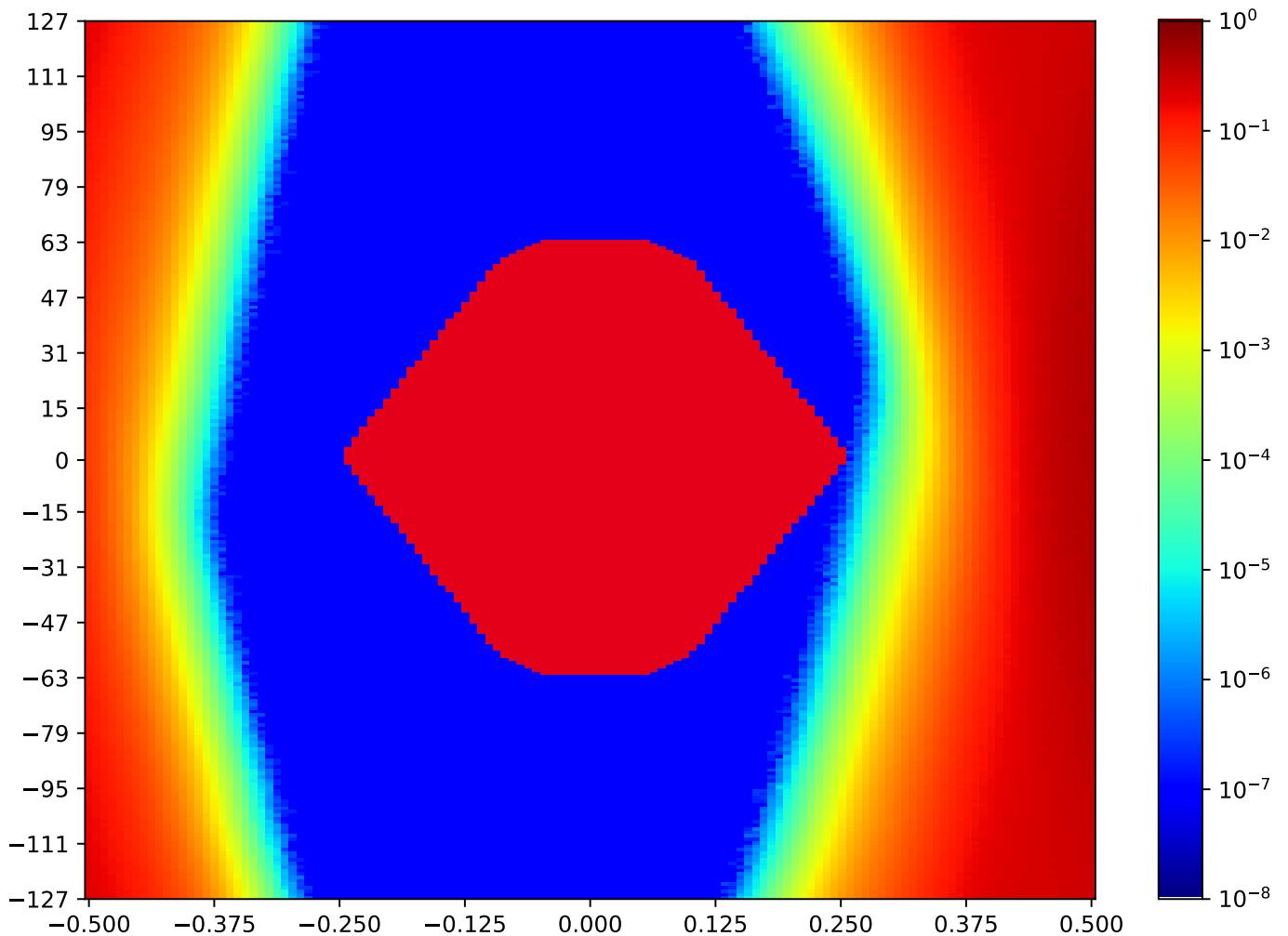


Figure 3.291: MSP_C_FPGA-TX4-11-RX3-11-MSP_A_FPGA

Call back to summary Figure 3.279. Sibling eye diagrams: V1-6.4.

Chapter 4

MUCTPI V2 6.4 Gbps

4.1 MSP_A TX1 MSP_C RX15 Minipod Loopback

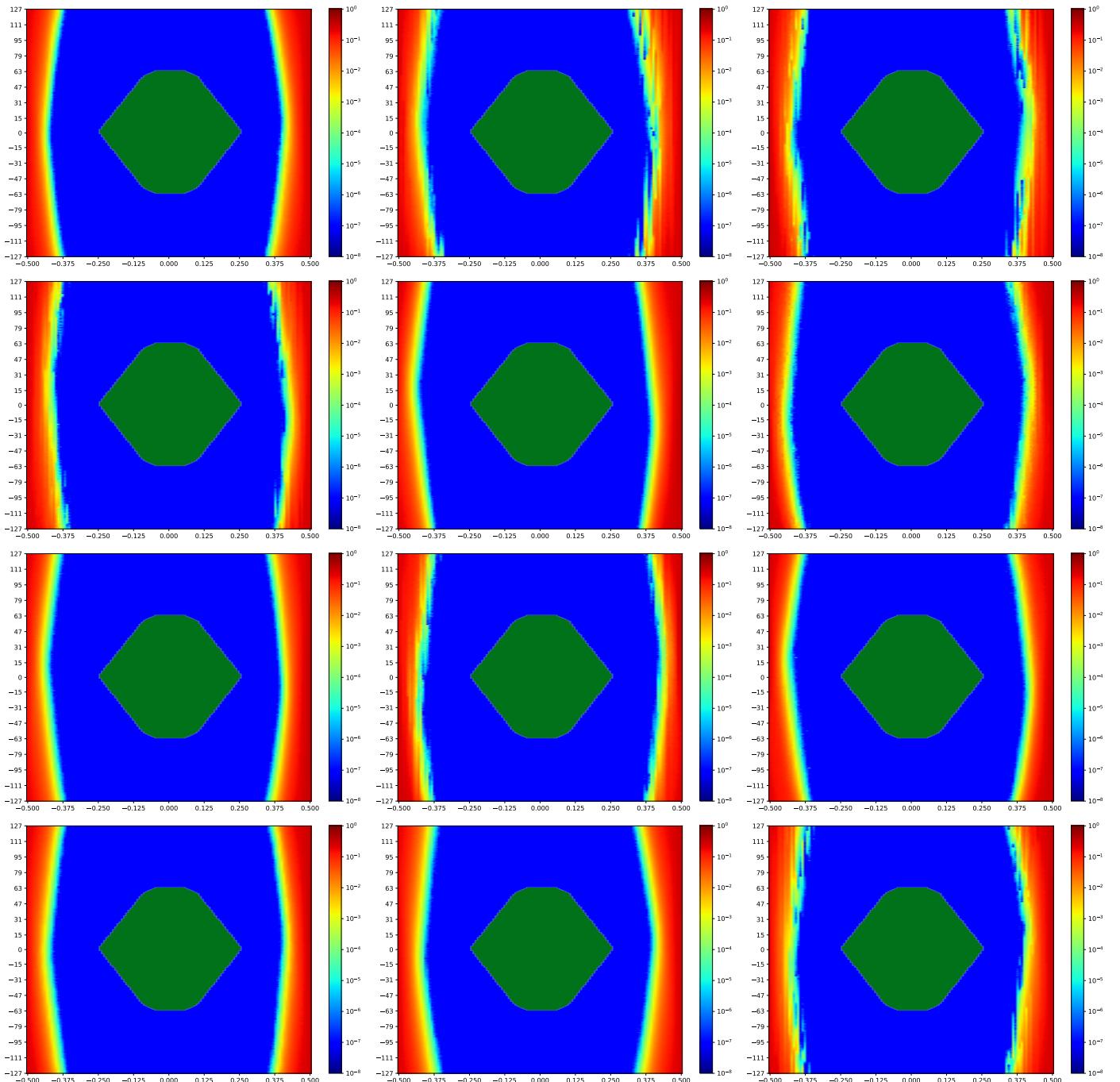


Figure 4.1: MSP_A TX1 MSP_C RX15 Minipod Loopback

A cross-reference to Figure 4.1. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.14.

4.1.1 MSP_A_FPGA-TX1-00-RX15-00-MSP_C_FPGA

Table 4.1: MSP_A_FPGA-TX1-00-RX15-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:44:28		2018-Sep-26 16:45:43	
Reset RX	OA	HO		VO	VO (%)
true	24704	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

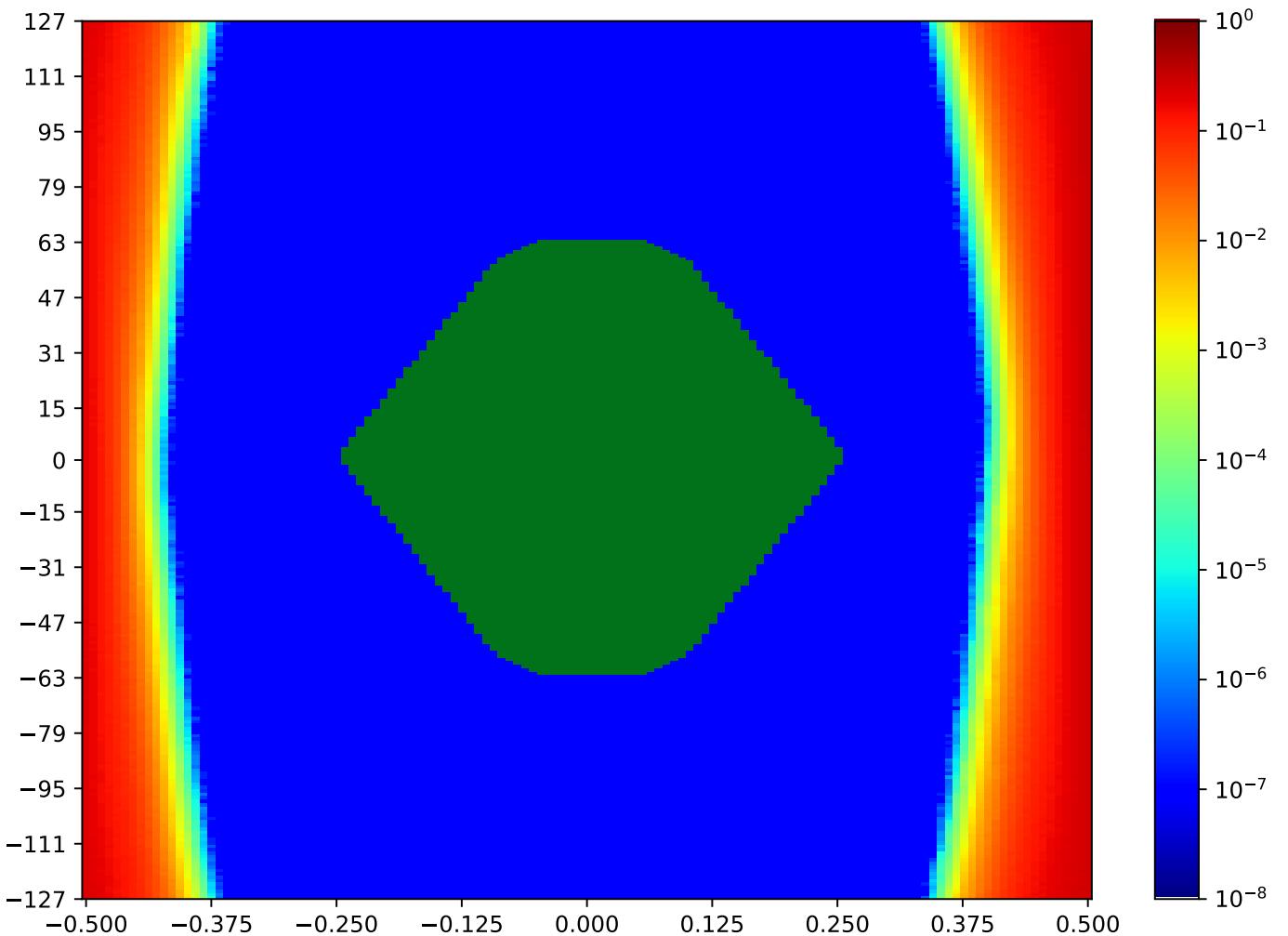


Figure 4.2: MSP_A_FPGA-TX1-00-RX15-00-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.2 MSP_A_FPGA-TX1-01-RX15-01-MSP_C_FPGA

Table 4.2: MSP_A_FPGA-TX1-01-RX15-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:46:58		2018-Sep-26 16:48:12	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23680	98		75.97%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

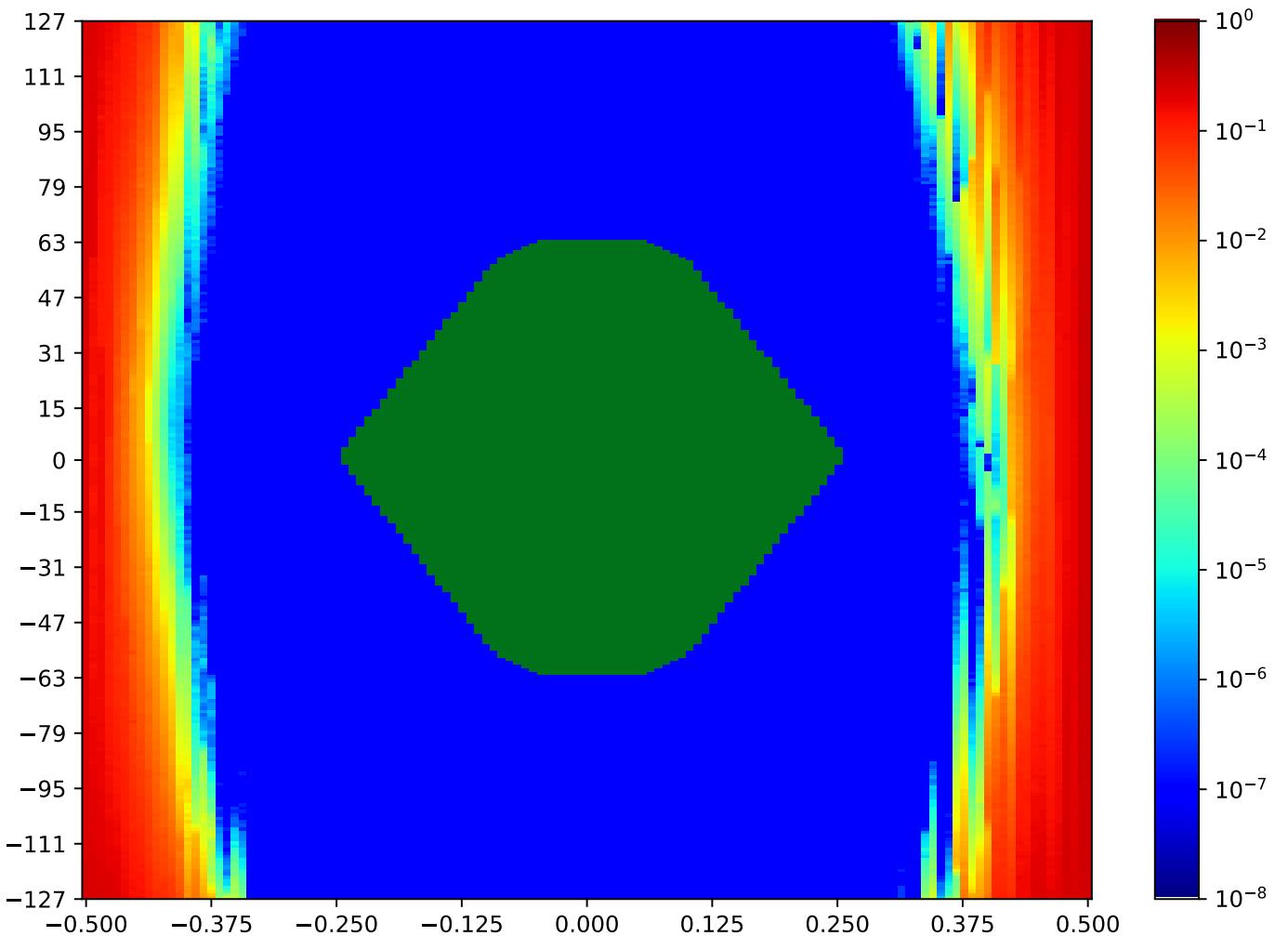


Figure 4.3: MSP_A_FPGA-TX1-01-RX15-01-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.3 MSP_A_FPGA-TX1-02-RX15-02-MSP_C_FPGA

Table 4.3: MSP_A_FPGA-TX1-02-RX15-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:48:12		2018-Sep-26 16:49:27	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24026	99		75.97%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

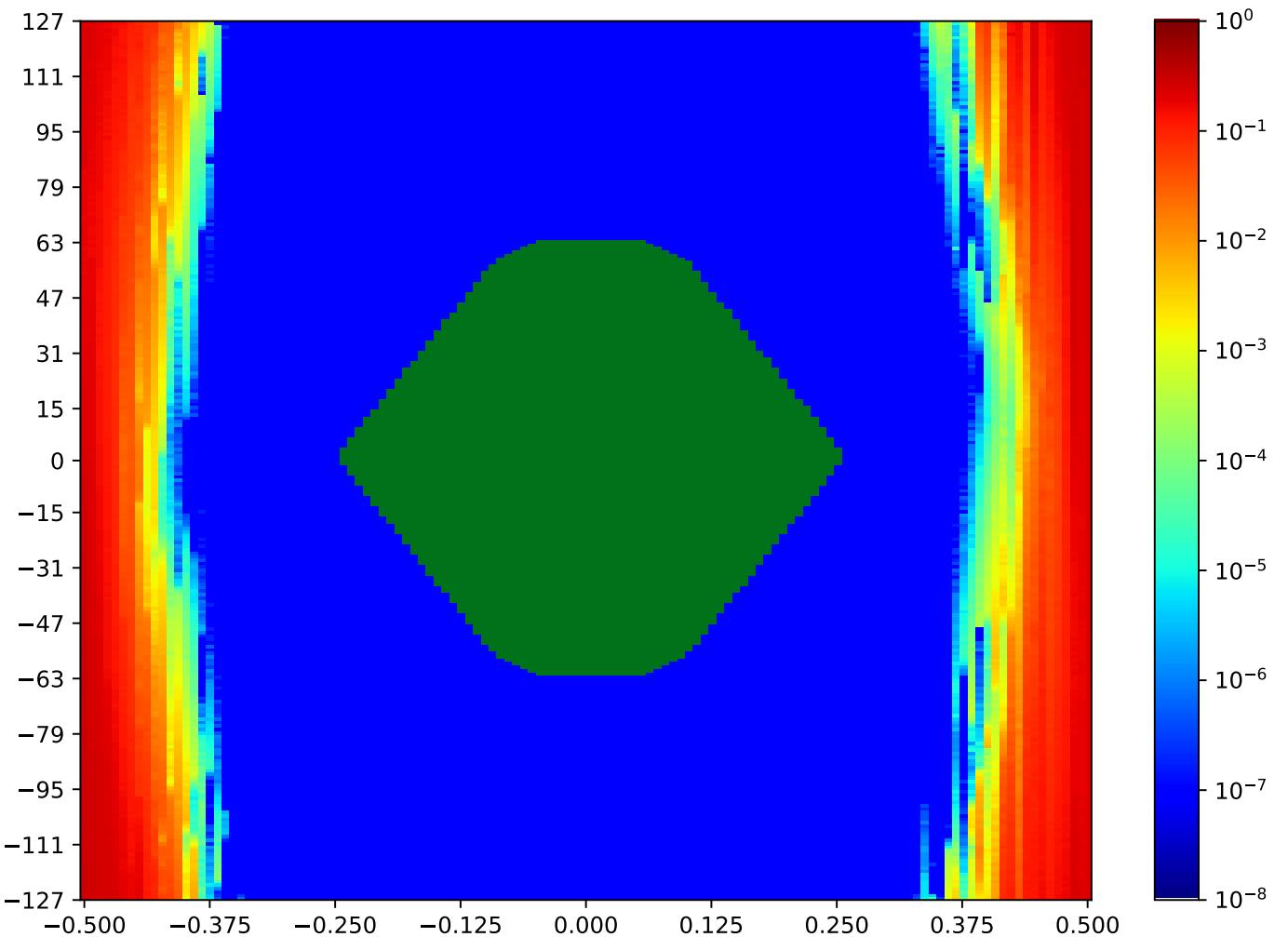


Figure 4.4: MSP_A_FPGA-TX1-02-RX15-02-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.4 MSP_A_FPGA-TX1-03-RX15-03-MSP_C_FPGA

Table 4.4: MSP_A_FPGA-TX1-03-RX15-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:41:59		2018-Sep-26 16:43:14	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24702	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

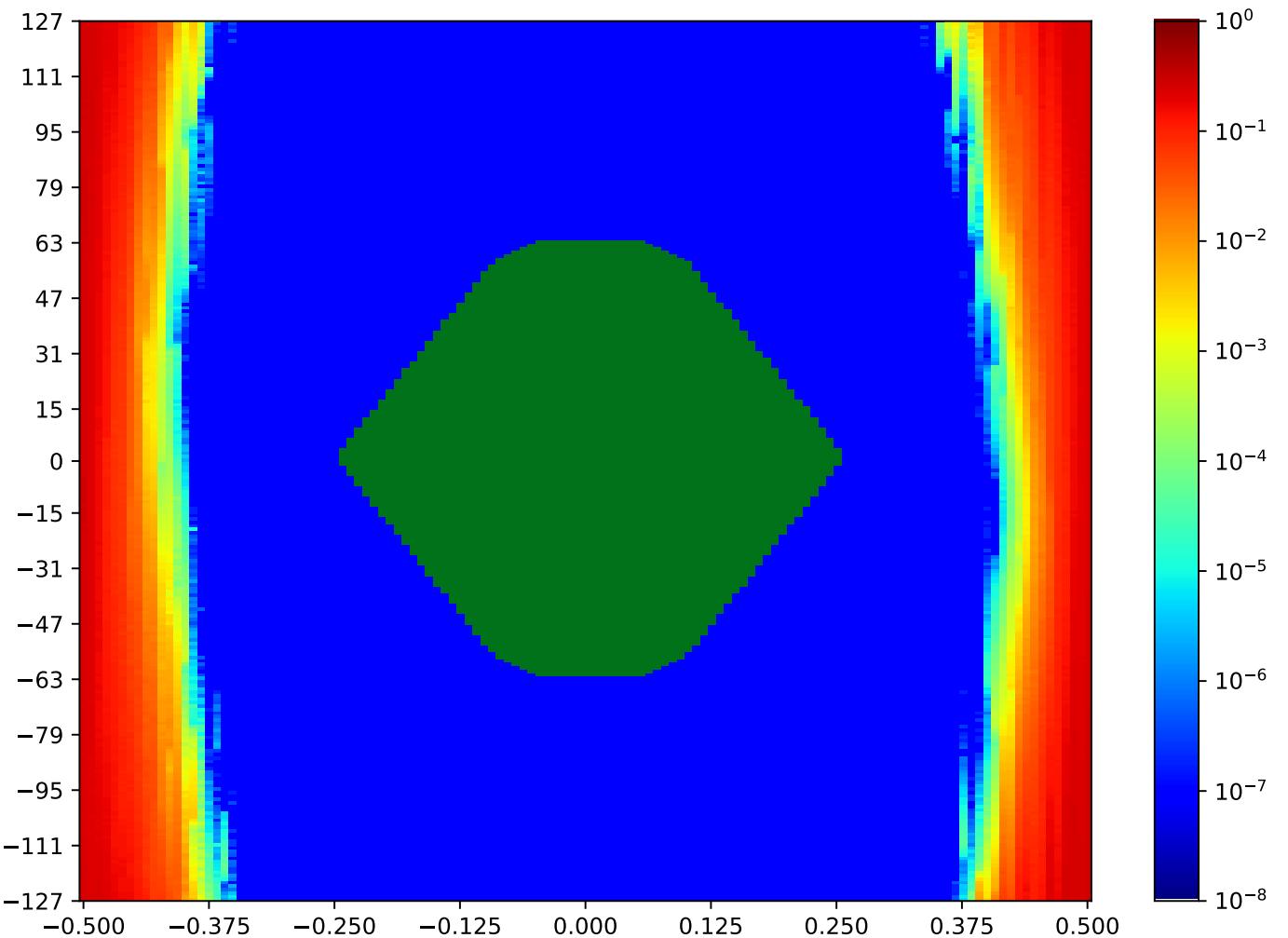


Figure 4.5: MSP_A_FPGA-TX1-03-RX15-03-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.5 MSP_A_FPGA-TX1-04-RX15-04-MSP_C_FPGA

Table 4.5: MSP_A_FPGA-TX1-04-RX15-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:51:55		2018-Sep-26 16:53:09	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24615	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

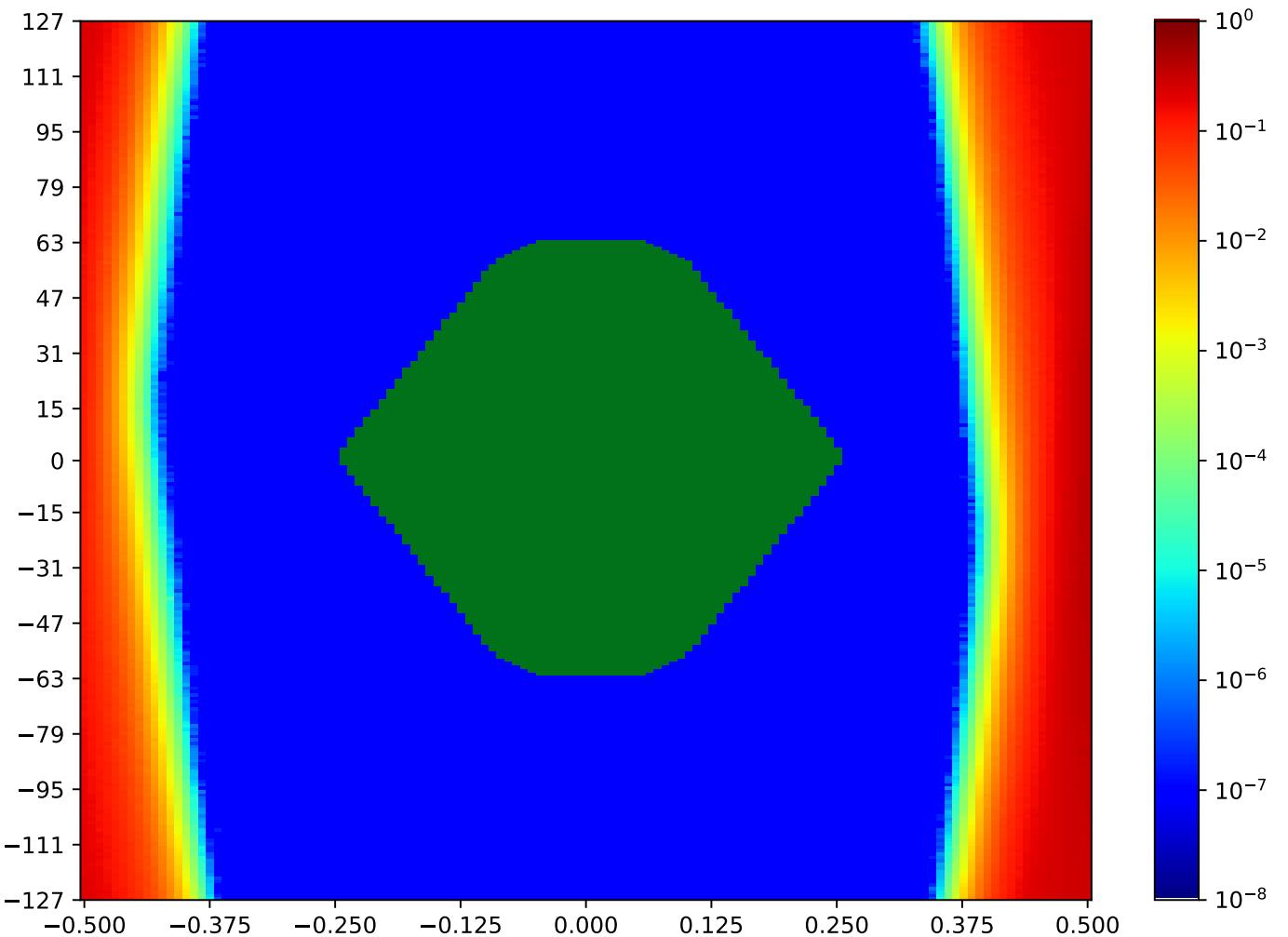


Figure 4.6: MSP_A_FPGA-TX1-04-RX15-04-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.6 MSP_A_FPGA-TX1-05-RX15-05-MSP_C_FPGA

Table 4.6: MSP_A_FPGA-TX1-05-RX15-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:40:45		2018-Sep-26 16:41:59	
Reset RX	OA	HO		VO	VO (%)
true	24643	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

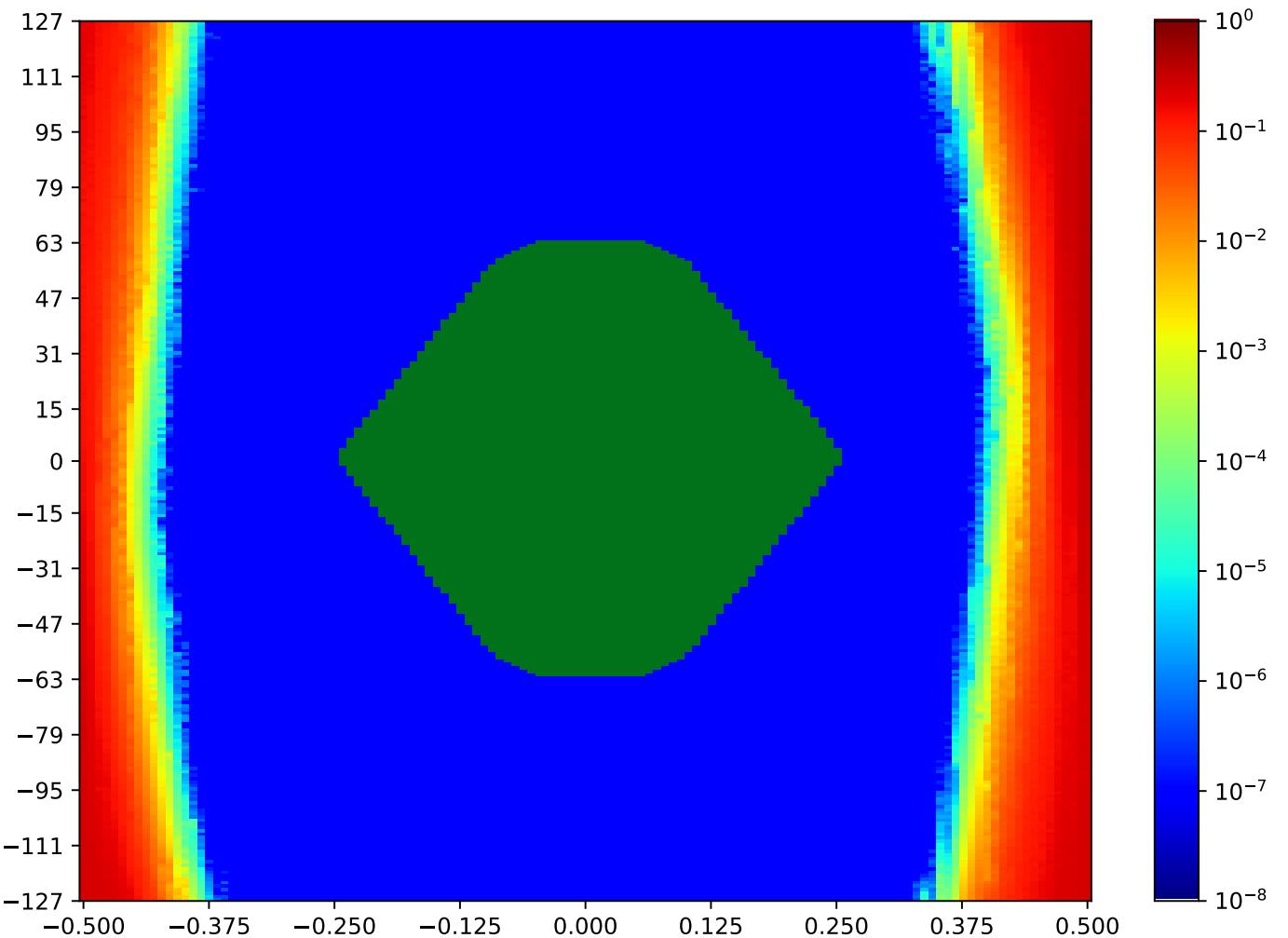


Figure 4.7: MSP_A_FPGA-TX1-05-RX15-05-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.7 MSP_A_FPGA-TX1-06-RX15-06-MSP_C_FPGA

Table 4.7: MSP_A_FPGA-TX1-06-RX15-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:54:24		2018-Sep-26 16:55:38	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24542	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

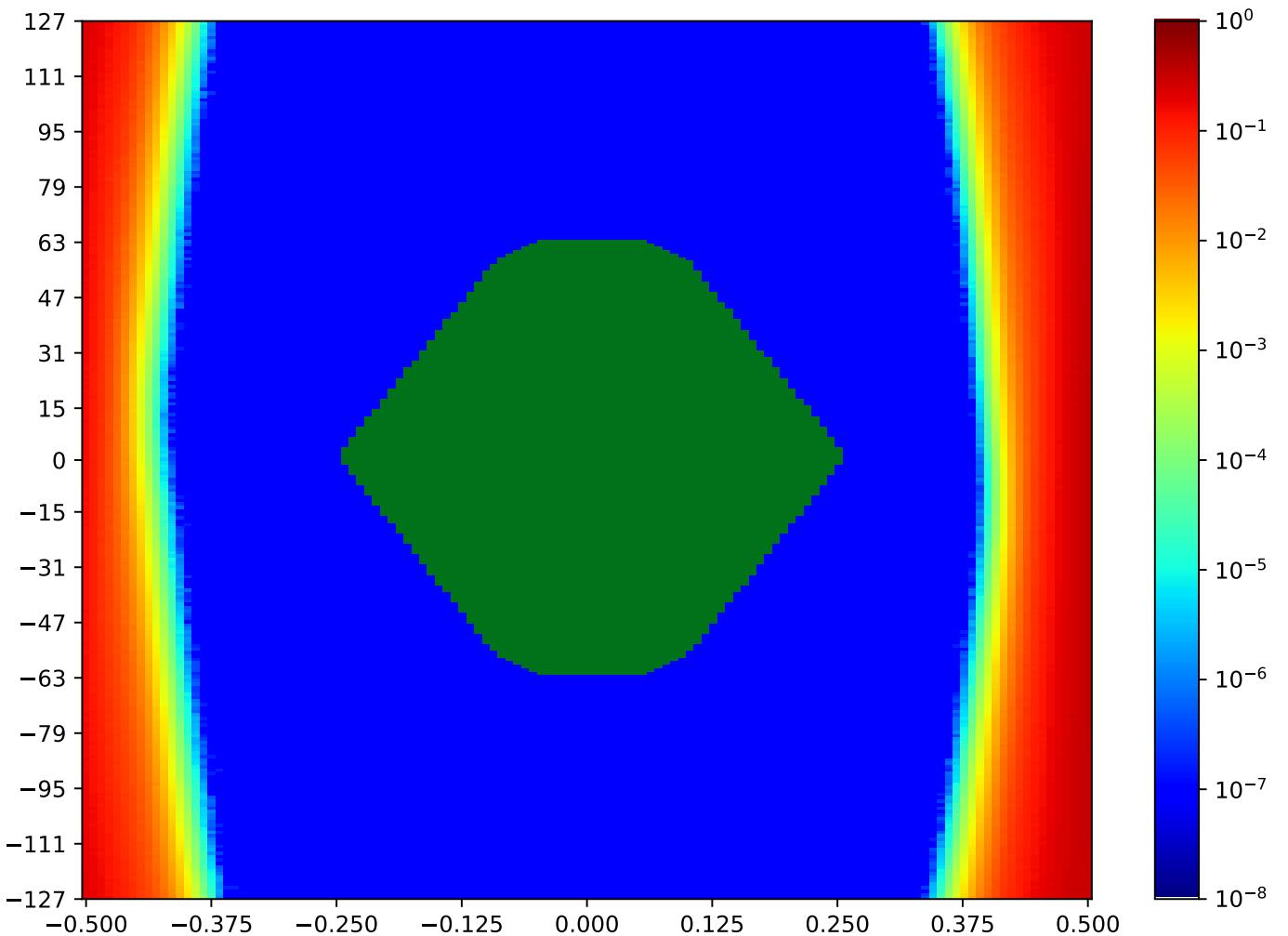


Figure 4.8: MSP_A_FPGA-TX1-06-RX15-06-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.8 MSP_A_FPGA-TX1-07-RX15-07-MSP_C_FPGA

Table 4.8: MSP_A_FPGA-TX1-07-RX15-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:43:14		2018-Sep-26 16:44:28	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	25354	104		80.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

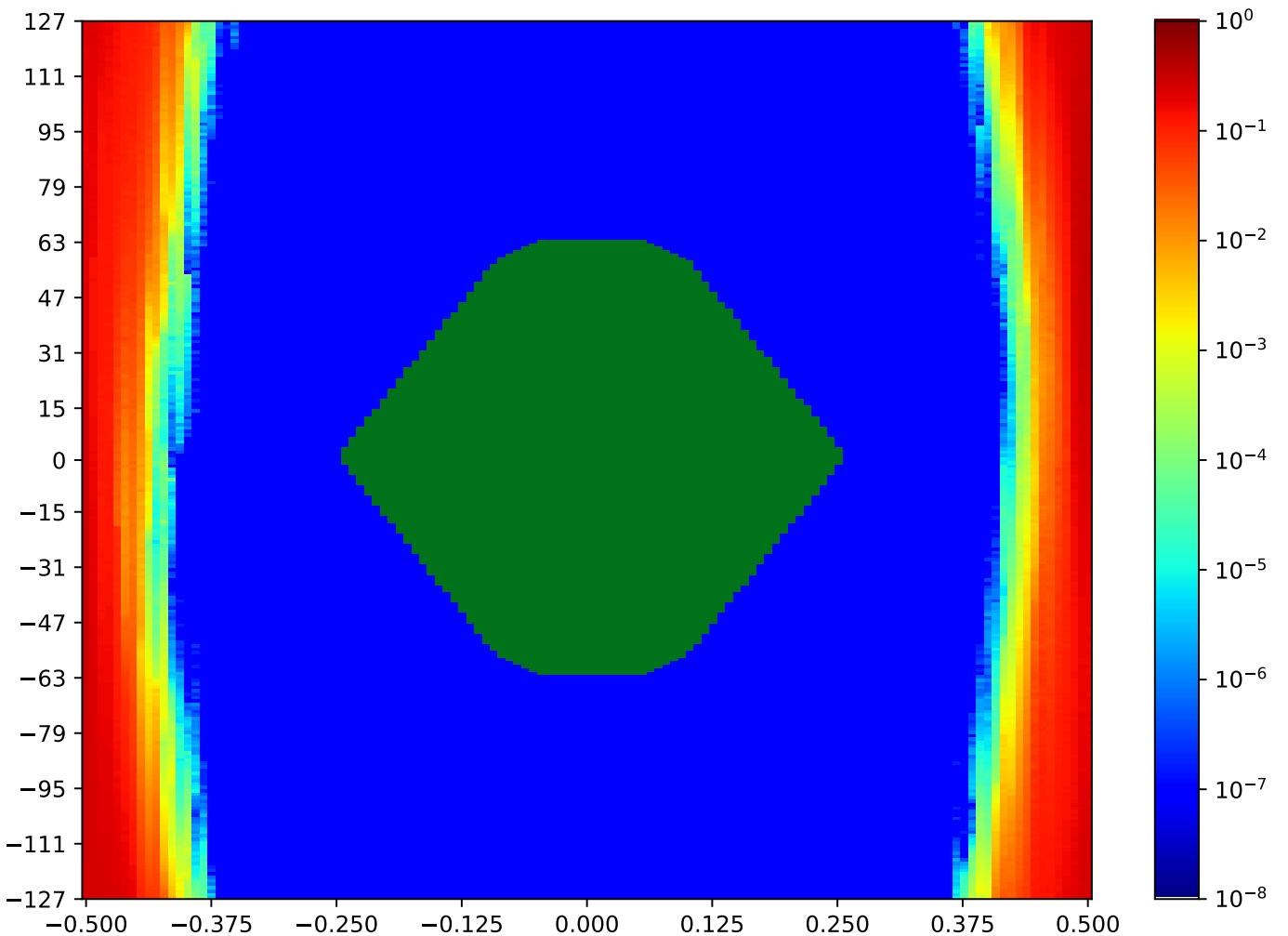


Figure 4.9: MSP_A_FPGA-TX1-07-RX15-07-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.9 MSP_A_FPGA-TX1-08-RX15-08-MSP_C_FPGA

Table 4.9: MSP_A_FPGA-TX1-08-RX15-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:53:09		2018-Sep-26 16:54:24	
Reset RX	OA	HO		VO	VO (%)
true	24555	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

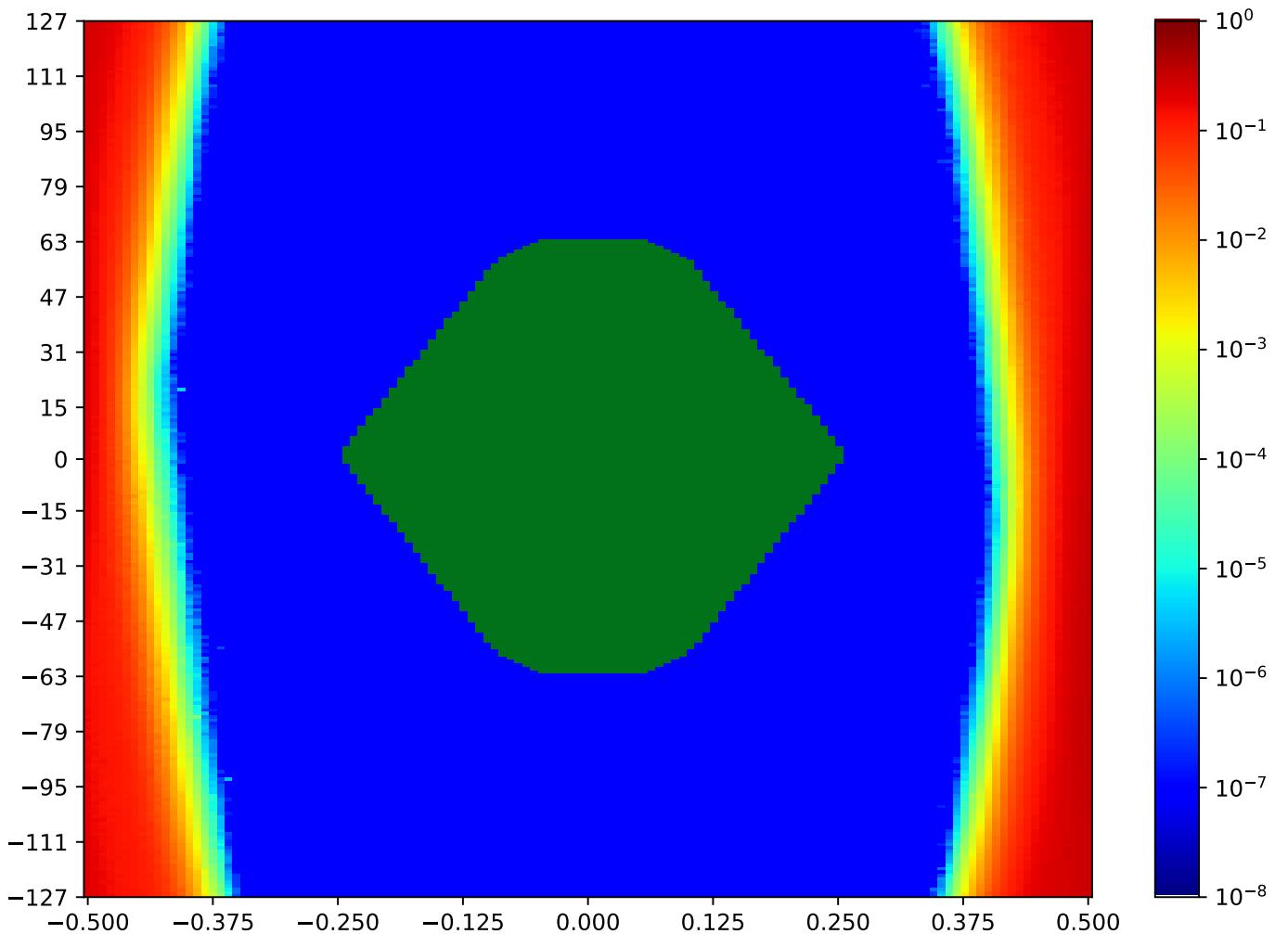


Figure 4.10: MSP_A_FPGA-TX1-08-RX15-08-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.10 MSP_A_FPGA-TX1-09-RX15-09-MSP_C_FPGA

Table 4.10: MSP_A_FPGA-TX1-09-RX15-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:45:43		2018-Sep-26 16:46:58	
Reset RX	OA	HO		VO	VO (%)
true	24620	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

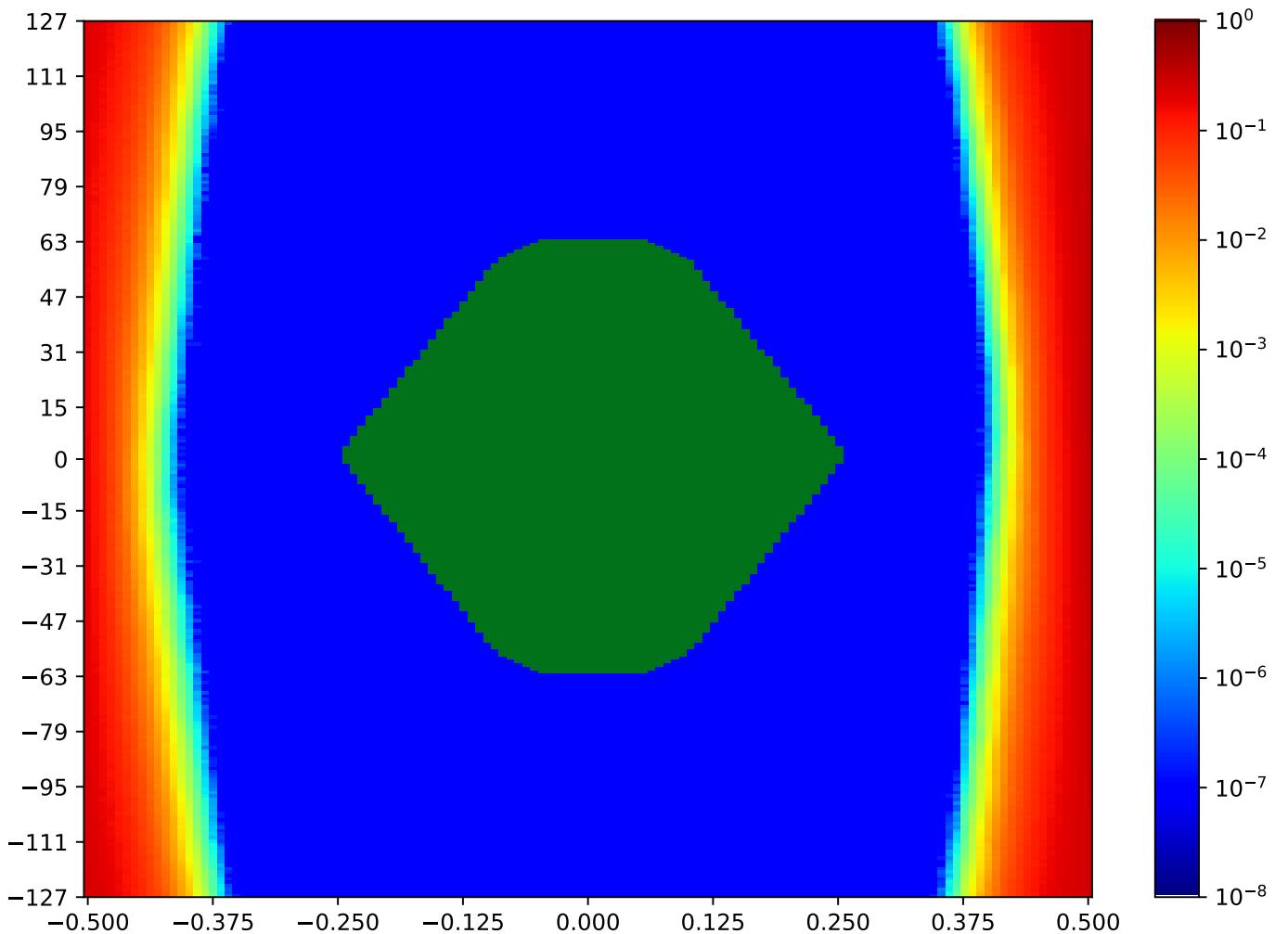


Figure 4.11: MSP_A_FPGA-TX1-09-RX15-09-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.11 MSP_A_FPGA-TX1-10-RX15-10-MSP_C_FPGA

Table 4.11: MSP_A_FPGA-TX1-10-RX15-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:50:41		2018-Sep-26 16:51:55	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23820	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

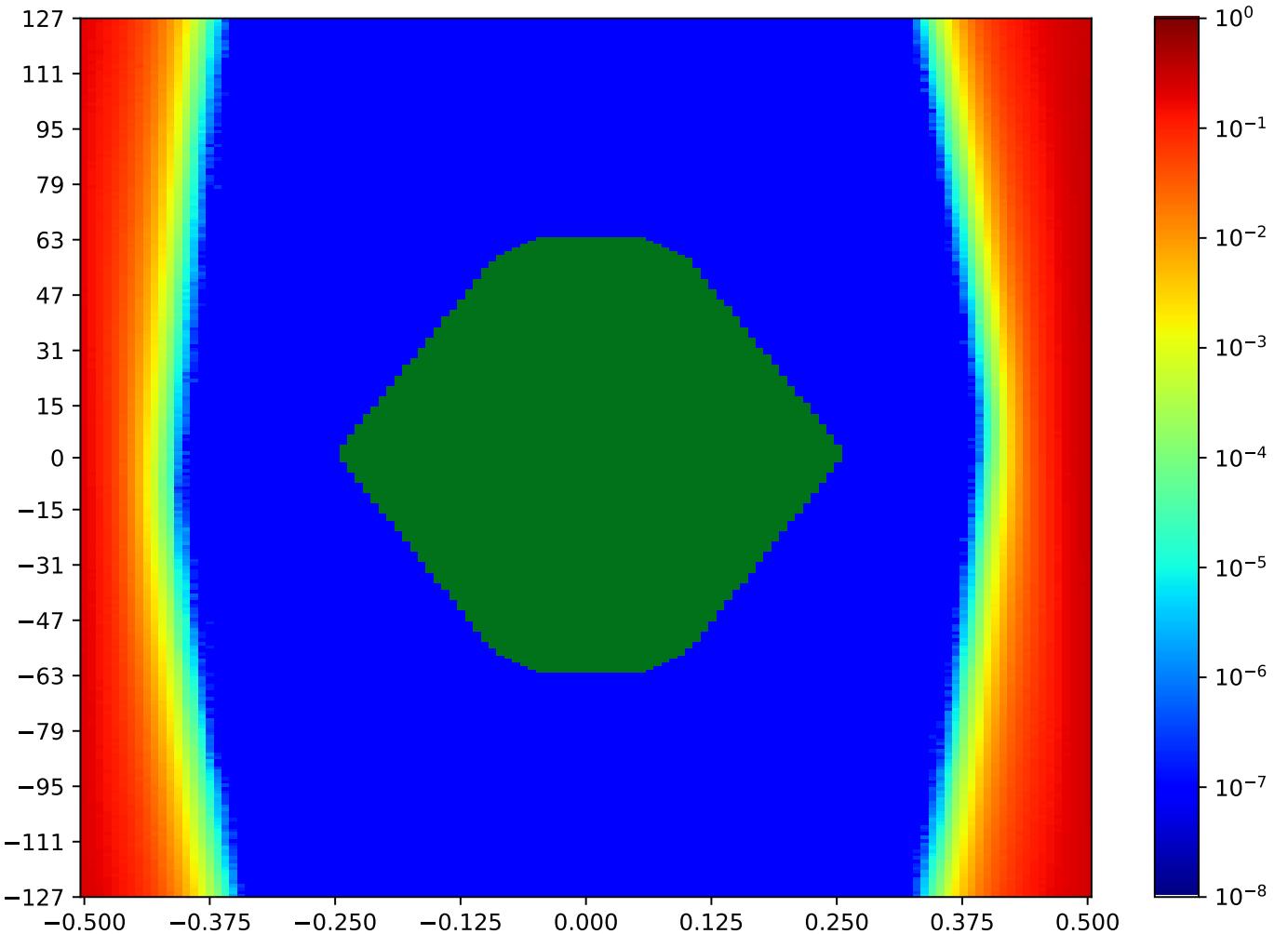


Figure 4.12: MSP_A_FPGA-TX1-10-RX15-10-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.1.12 MSP_A_FPGA-TX1-11-RX15-11-MSP_C_FPGA

Table 4.12: MSP_A_FPGA-TX1-11-RX15-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:49:27		2018-Sep-26 16:50:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24230	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

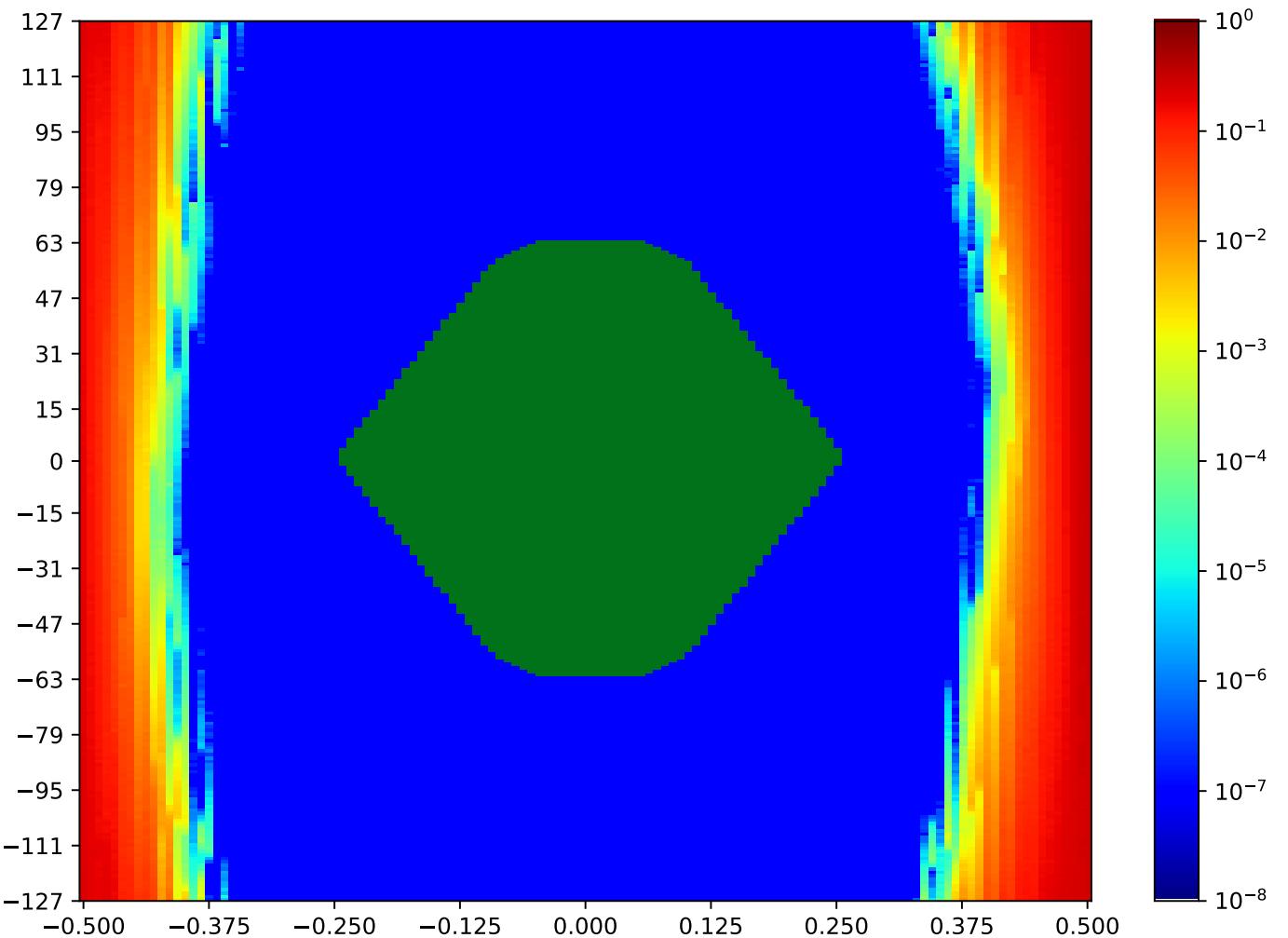


Figure 4.13: MSP_A_FPGA-TX1-11-RX15-11-MSP_C_FPGA

Call back to summary Figure 4.1. Sibling eye diagrams: V2-12.8.

4.2 MSP_A TX2 MSP_C RX16 Minipod Loopback

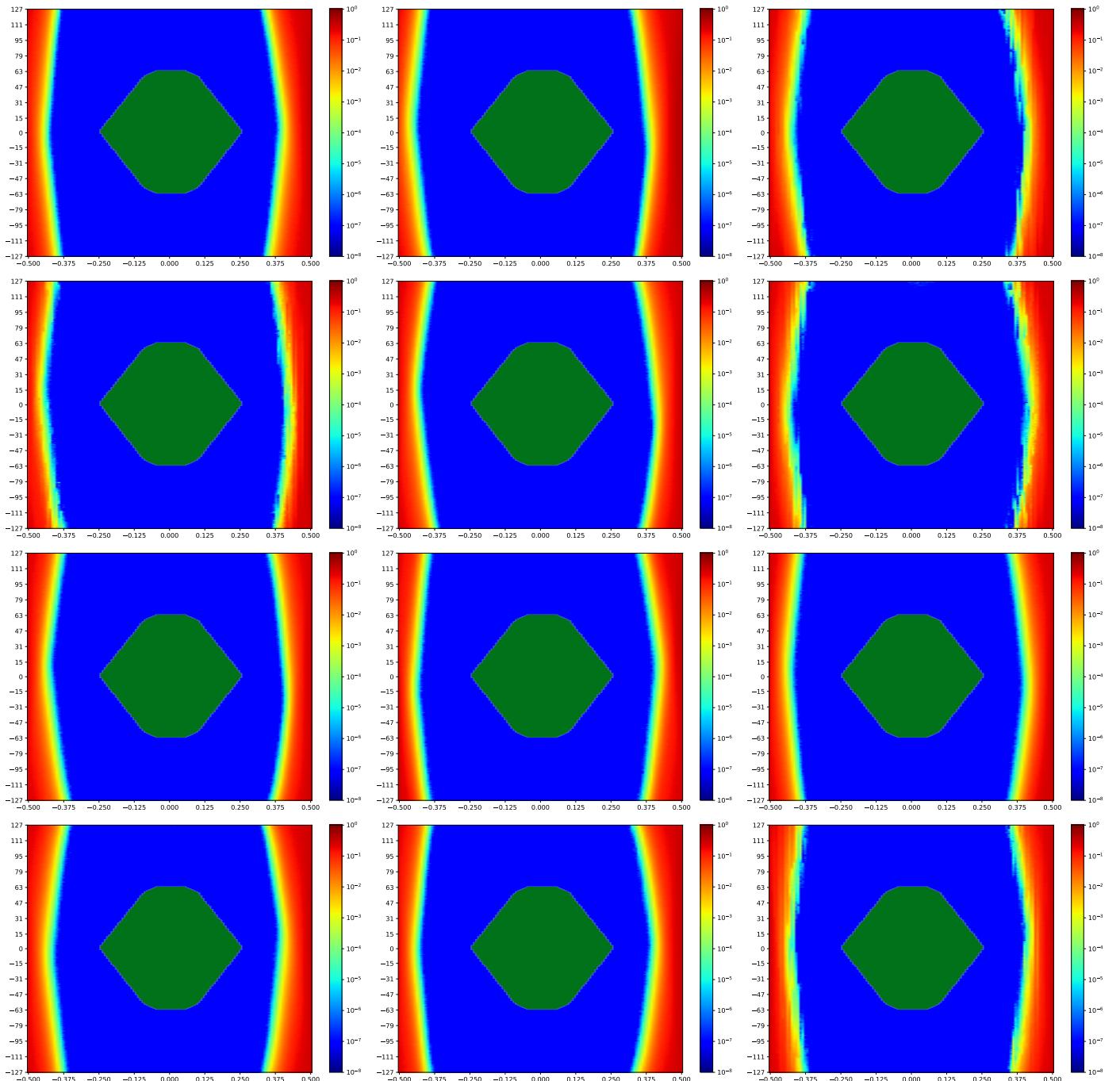


Figure 4.14: MSP_A TX2 MSP_C RX16 Minipod Loopback

A cross-reference to Figure 4.14. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.27.

4.2.1 MSP_A_FPGA-TX2-00-RX16-00-MSP_C_FPGA

Table 4.13: MSP_A_FPGA-TX2-00-RX16-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:59:24		2018-Sep-26 17:00:39	
Reset RX	OA	HO		VO	VO (%)
true	24312	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

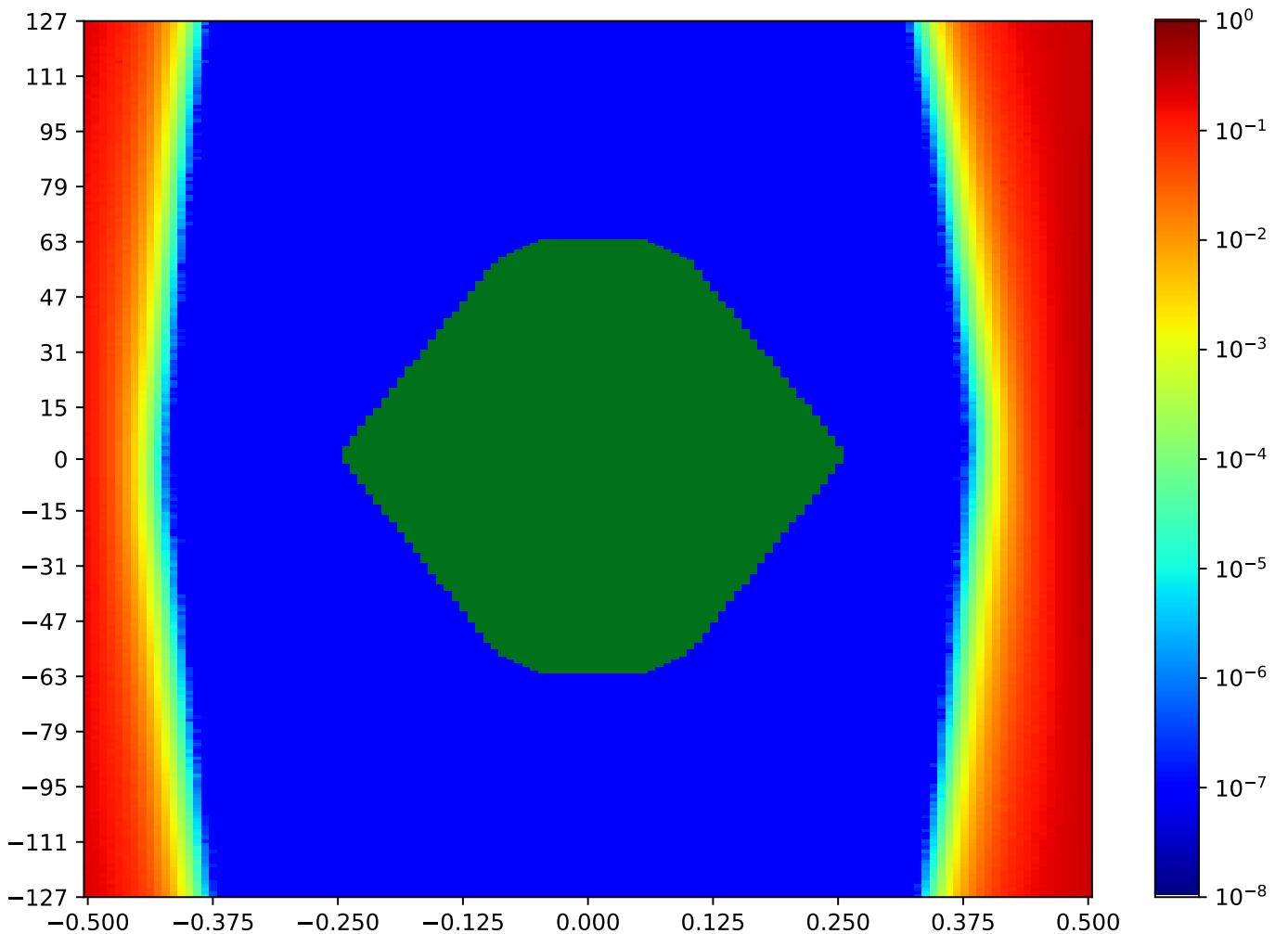


Figure 4.15: MSP_A_FPGA-TX2-00-RX16-00-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.2 MSP_A_FPGA-TX2-01-RX16-01-MSP_C_FPGA

Table 4.14: MSP_A_FPGA-TX2-01-RX16-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:56:54		2018-Sep-26 16:58:08	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24387	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

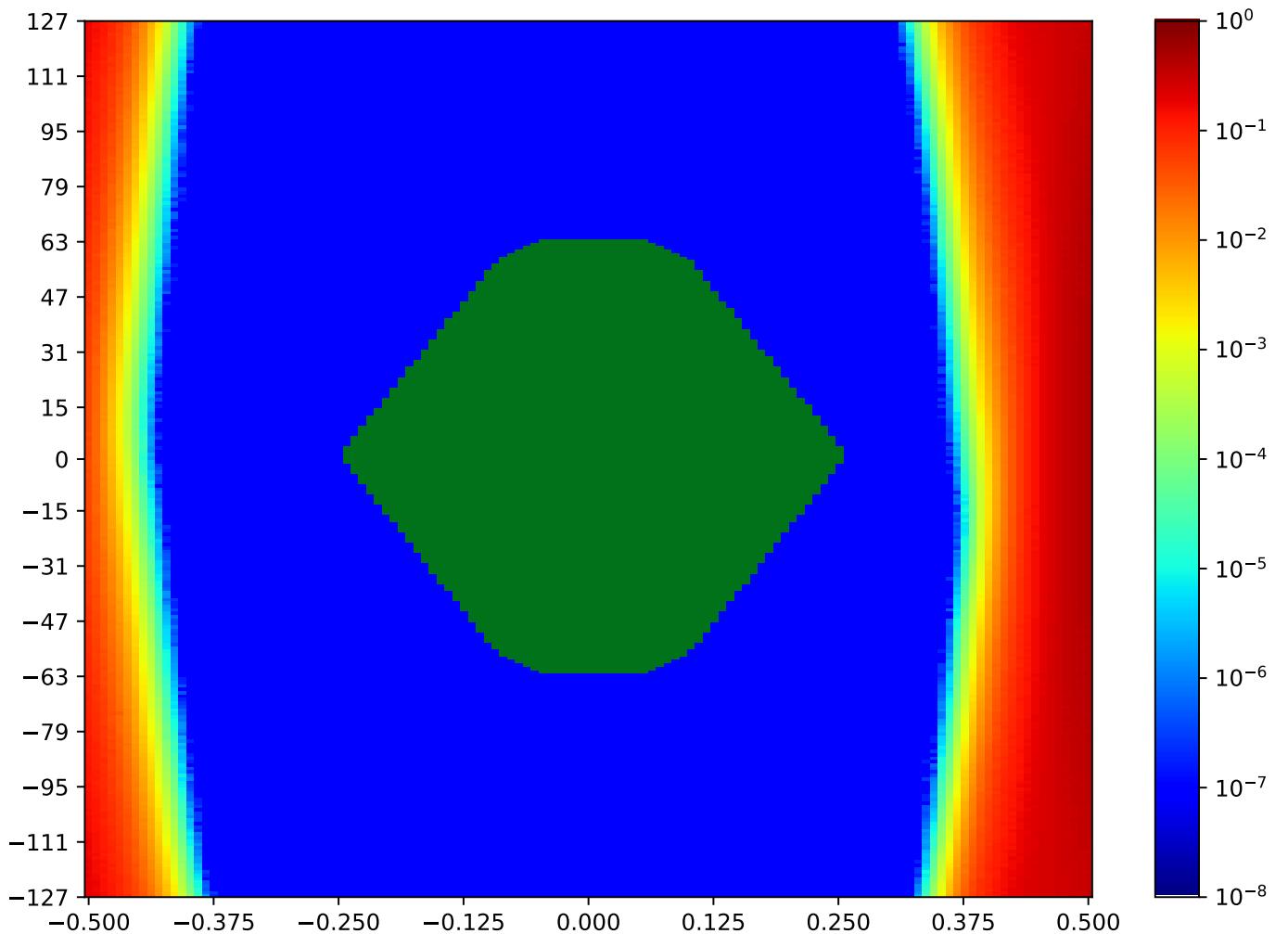


Figure 4.16: MSP_A_FPGA-TX2-01-RX16-01-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.3 MSP_A_FPGA-TX2-02-RX16-02-MSP_C_FPGA

Table 4.15: MSP_A_FPGA-TX2-02-RX16-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:03:09		2018-Sep-26 17:04:24	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24119	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

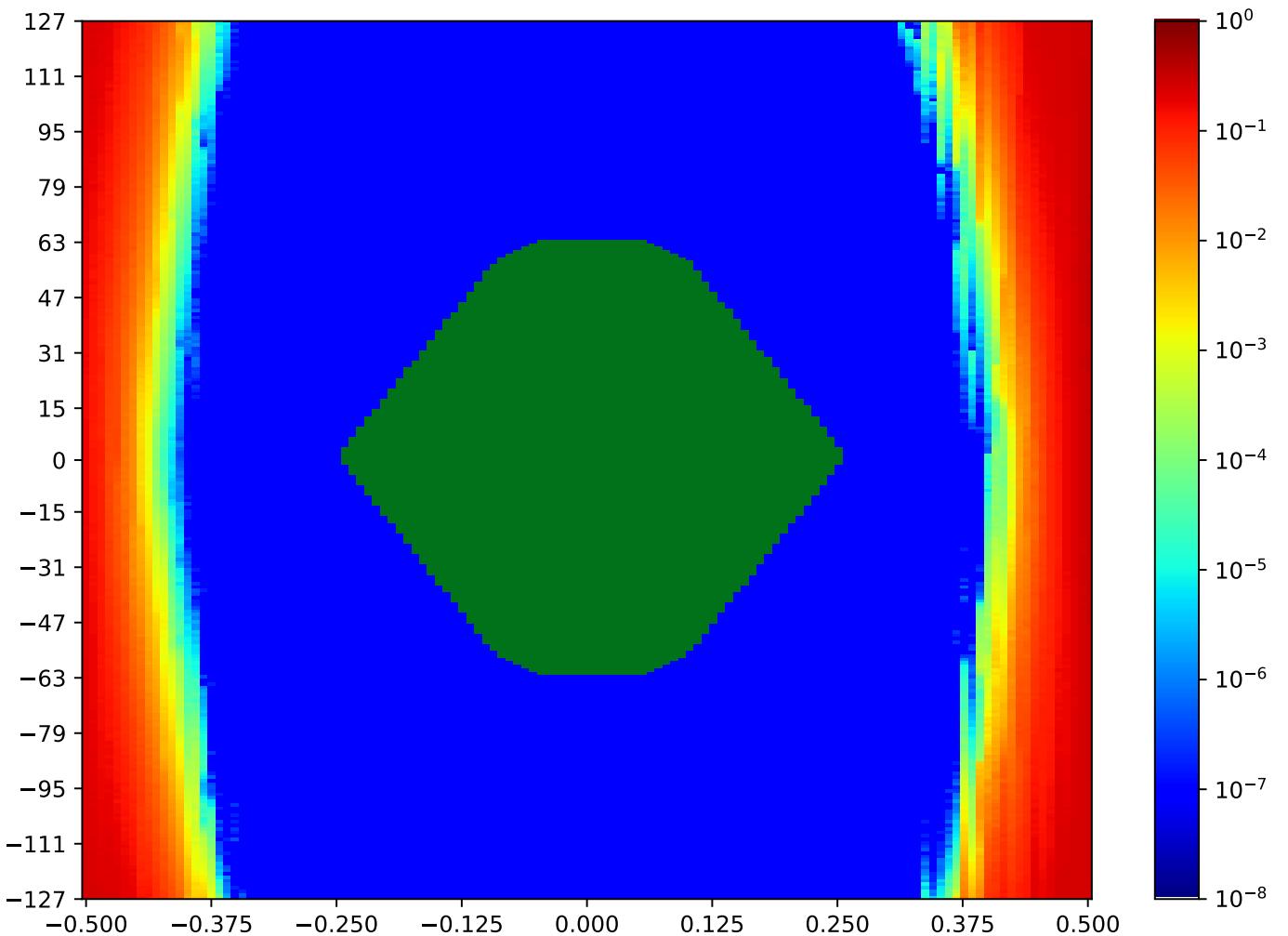


Figure 4.17: MSP_A_FPGA-TX2-02-RX16-02-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.4 MSP_A_FPGA-TX2-03-RX16-03-MSP_C_FPGA

Table 4.16: MSP_A_FPGA-TX2-03-RX16-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:55:39		2018-Sep-26 16:56:54	
Reset RX	OA	HO		VO	VO (%)
true	25382	105		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

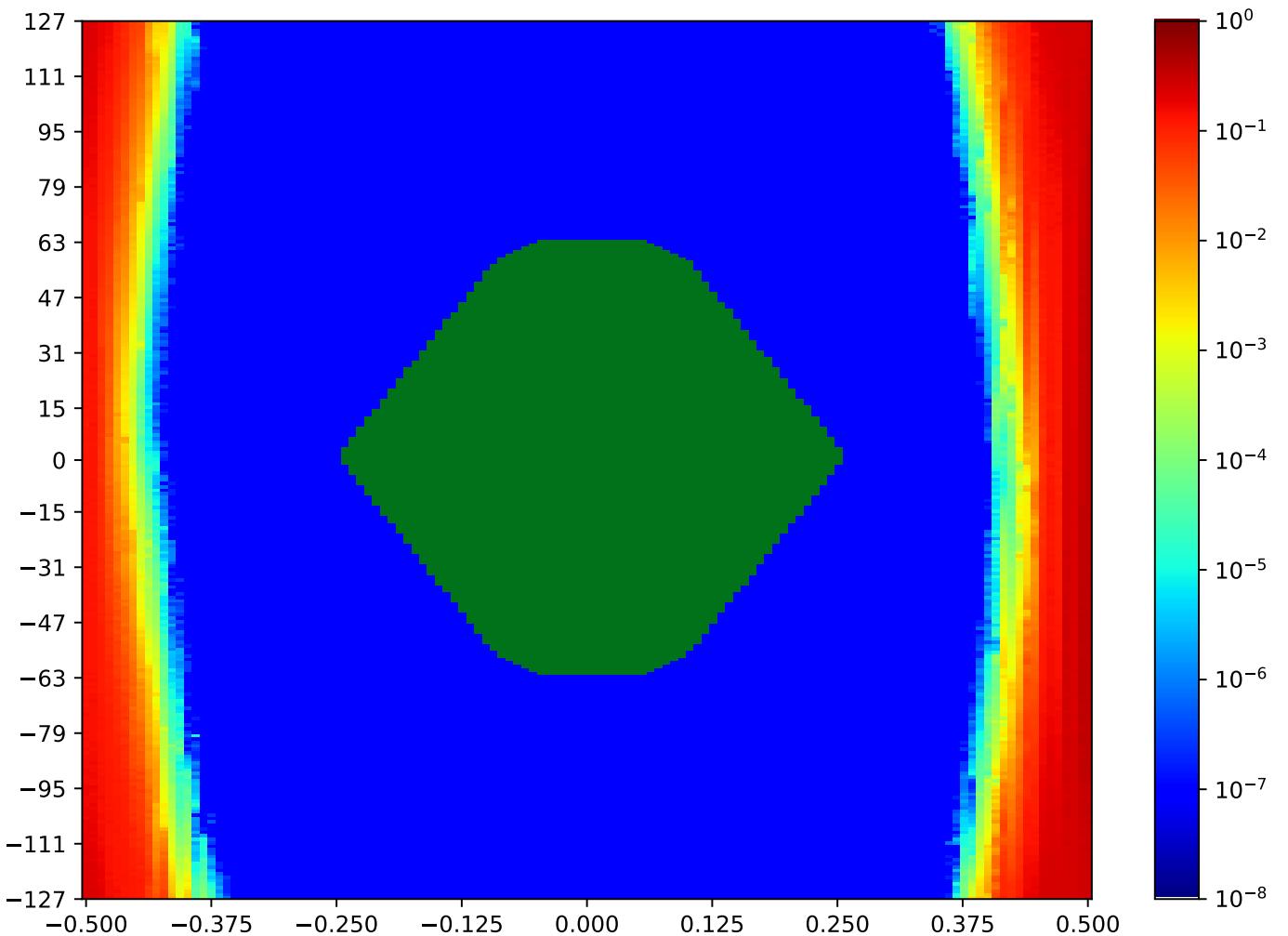


Figure 4.18: MSP_A_FPGA-TX2-03-RX16-03-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.5 MSP_A_FPGA-TX2-04-RX16-04-MSP_C_FPGA

Table 4.17: MSP_A_FPGA-TX2-04-RX16-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:06:55		2018-Sep-26 17:08:10	
Reset RX	OA	HO		VO	VO (%)
true	24484	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

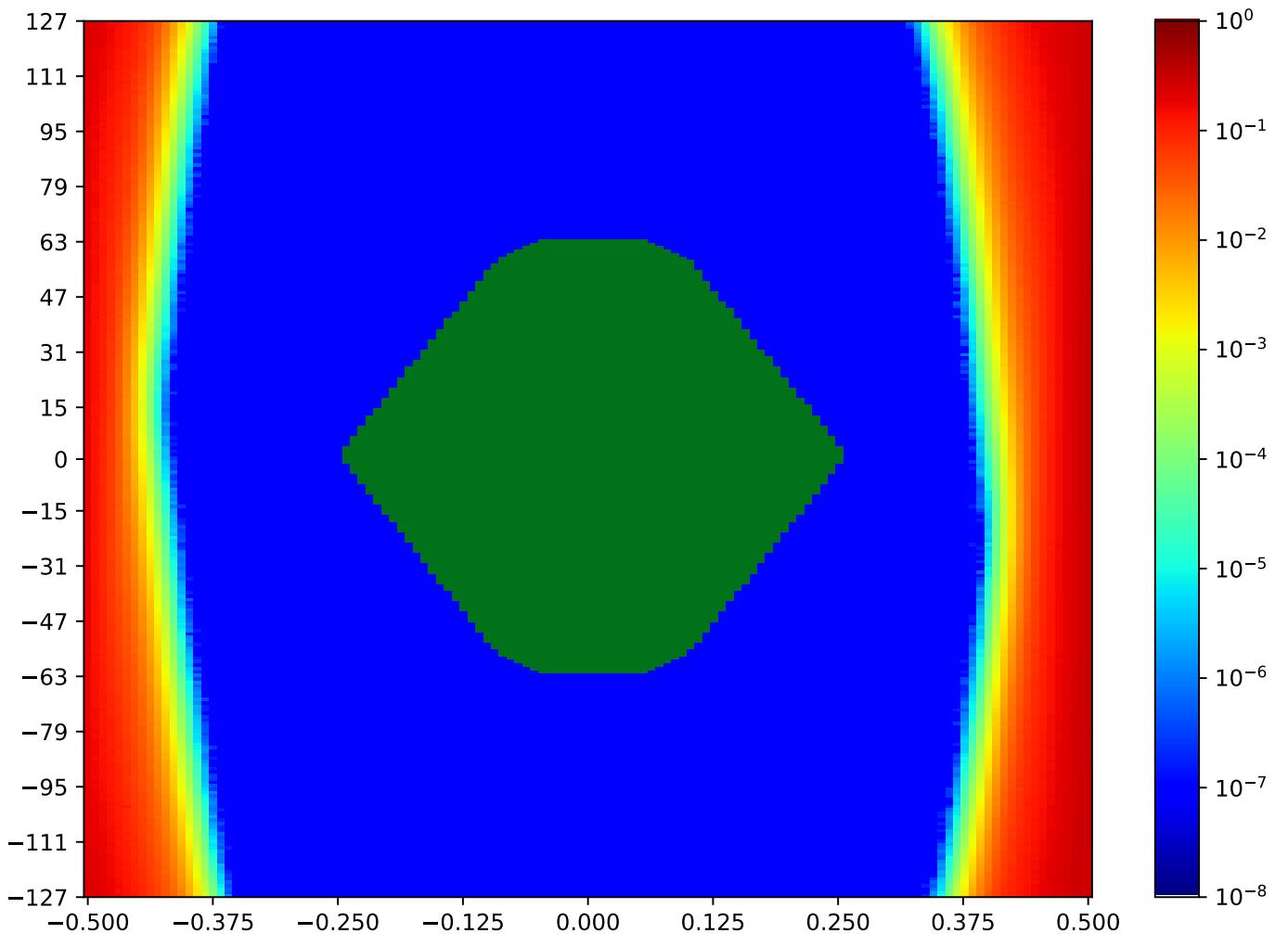


Figure 4.19: MSP_A_FPGA-TX2-04-RX16-04-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.6 MSP_A_FPGA-TX2-05-RX16-05-MSP_C_FPGA

Table 4.18: MSP_A_FPGA-TX2-05-RX16-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 16:58:08		2018-Sep-26 16:59:24	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24436	104		80.62%	252 98.43%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

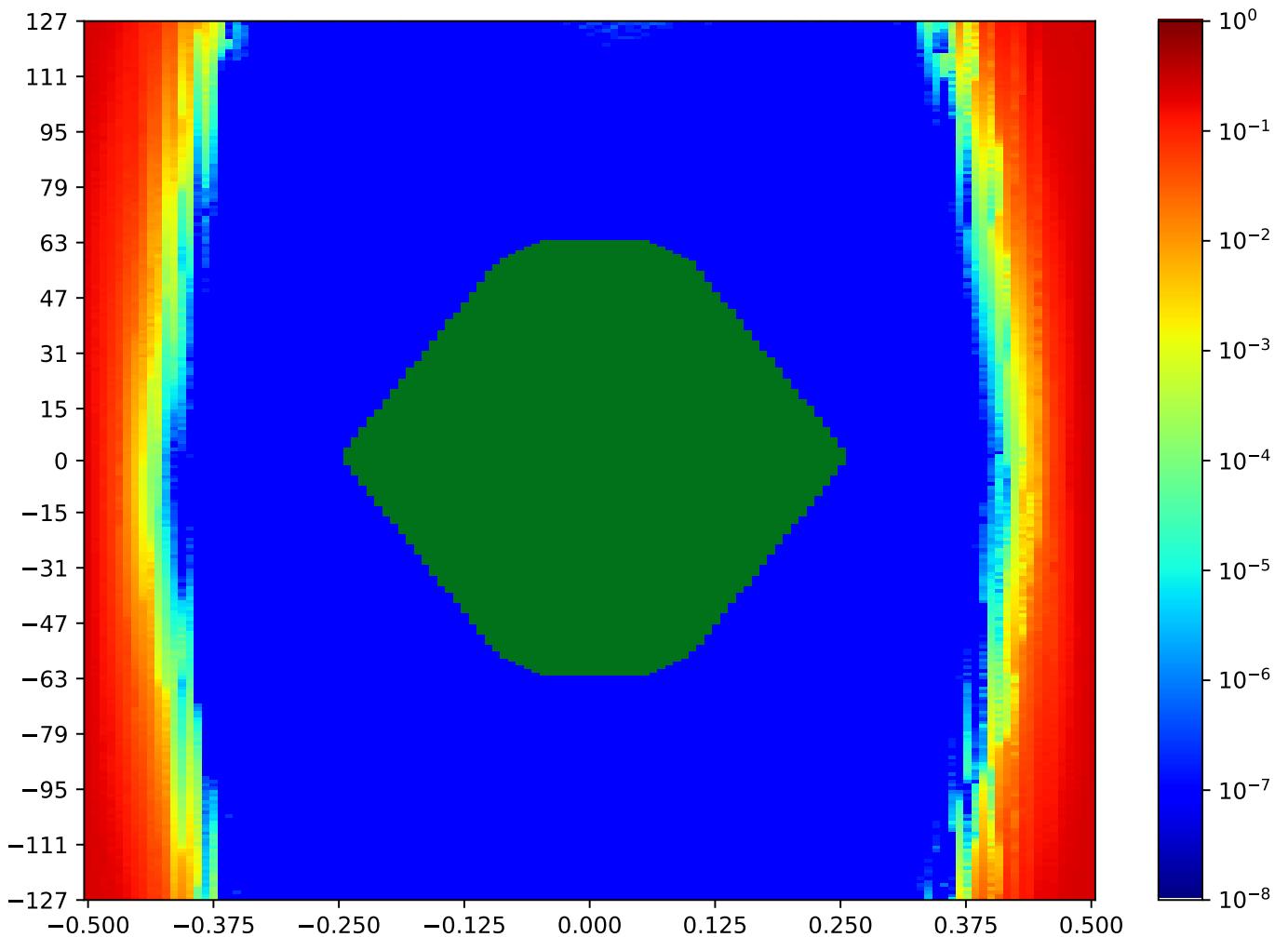


Figure 4.20: MSP_A_FPGA-TX2-05-RX16-05-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.7 MSP_A_FPGA-TX2-06-RX16-06-MSP_C_FPGA

Table 4.19: MSP_A_FPGA-TX2-06-RX16-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:09:26		2018-Sep-26 17:10:42	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24497	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

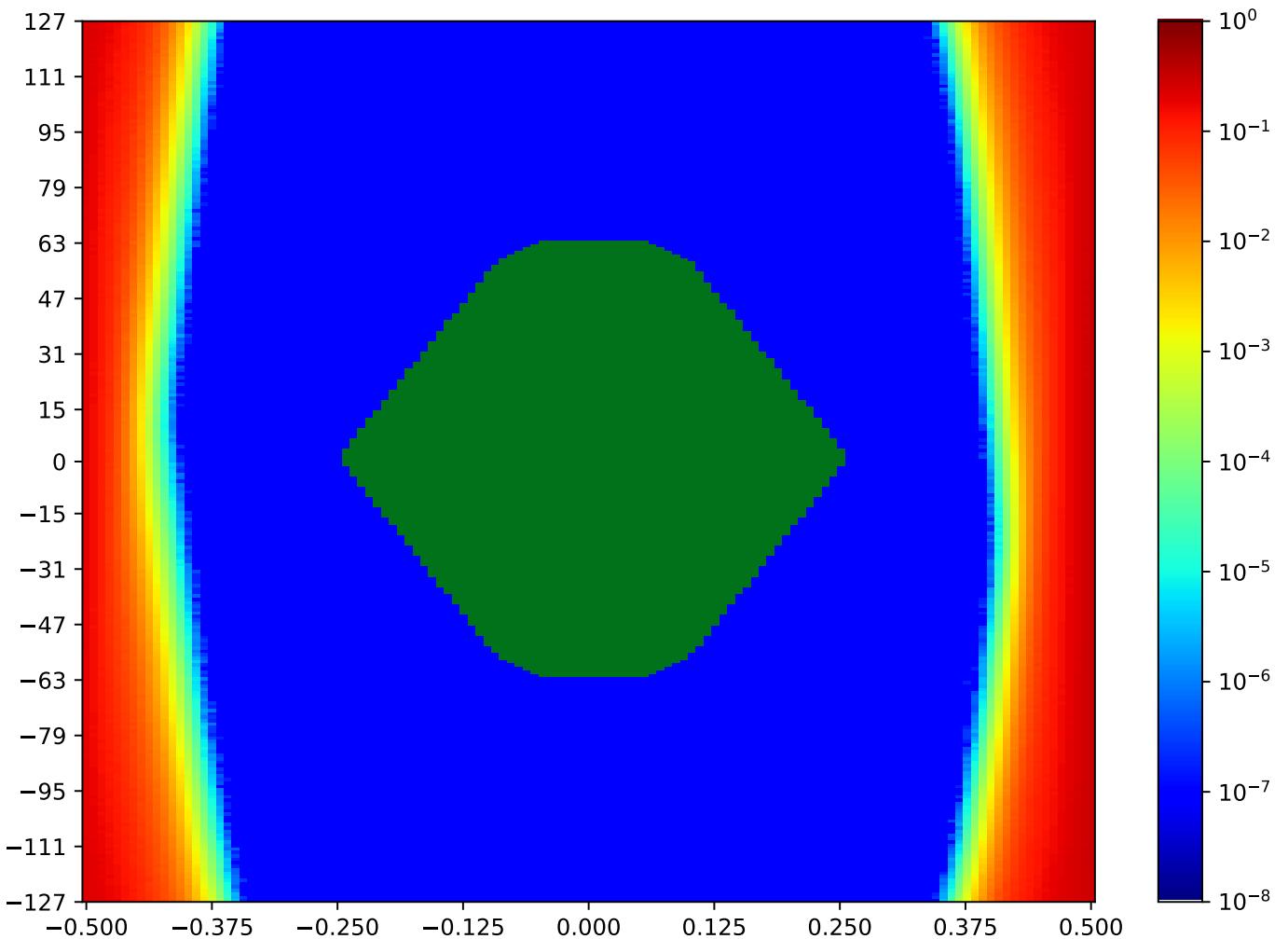


Figure 4.21: MSP_A_FPGA-TX2-06-RX16-06-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.8 MSP_A_FPGA-TX2-07-RX16-07-MSP_C_FPGA

Table 4.20: MSP_A_FPGA-TX2-07-RX16-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:00:39		2018-Sep-26 17:01:54	
Reset RX	OA	HO		VO	VO (%)
true	24939	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

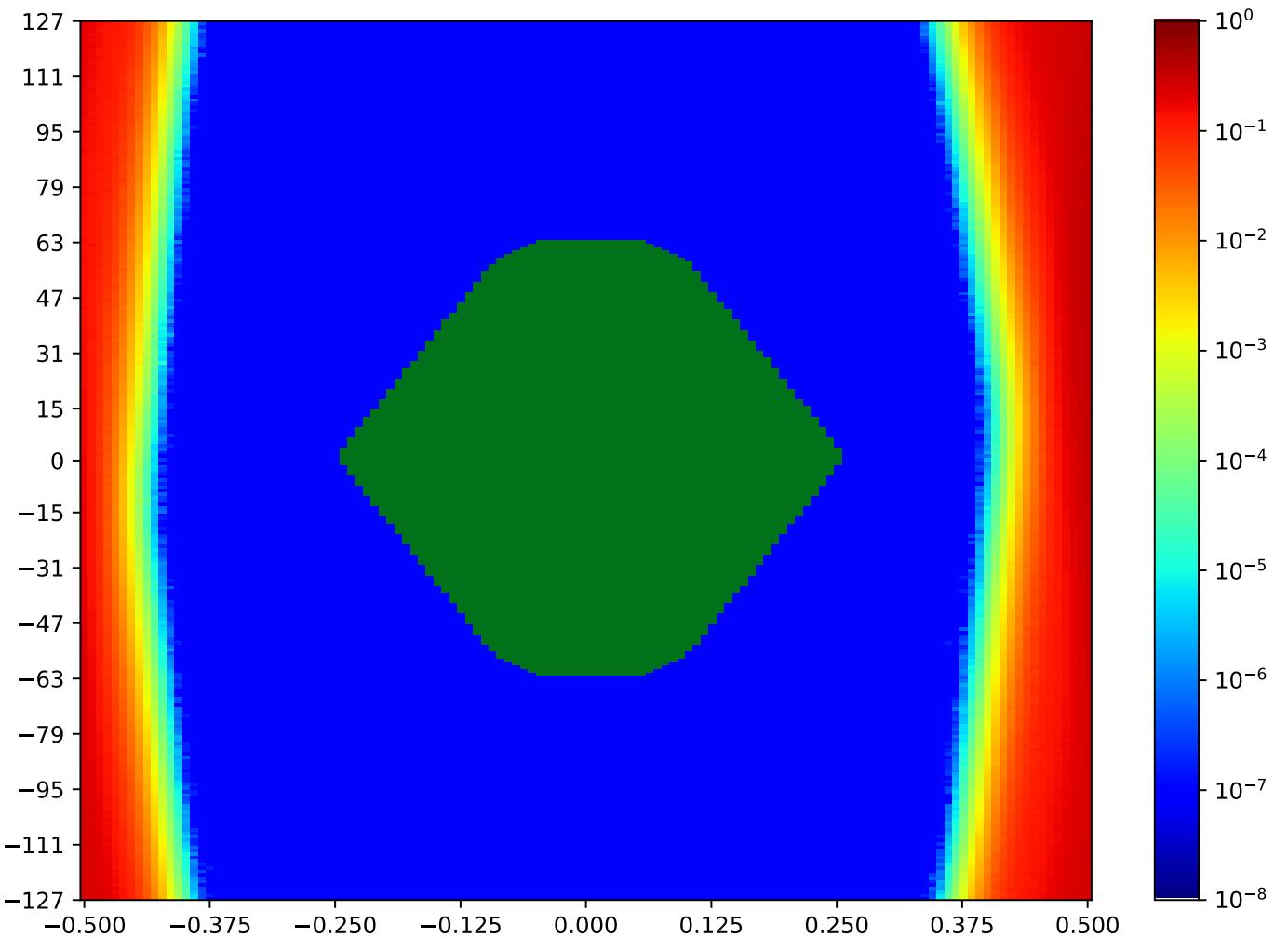


Figure 4.22: MSP_A_FPGA-TX2-07-RX16-07-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.9 MSP_A_FPGA-TX2-08-RX16-08-MSP_C_FPGA

Table 4.21: MSP_A_FPGA-TX2-08-RX16-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:08:10		2018-Sep-26 17:09:26	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24383	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

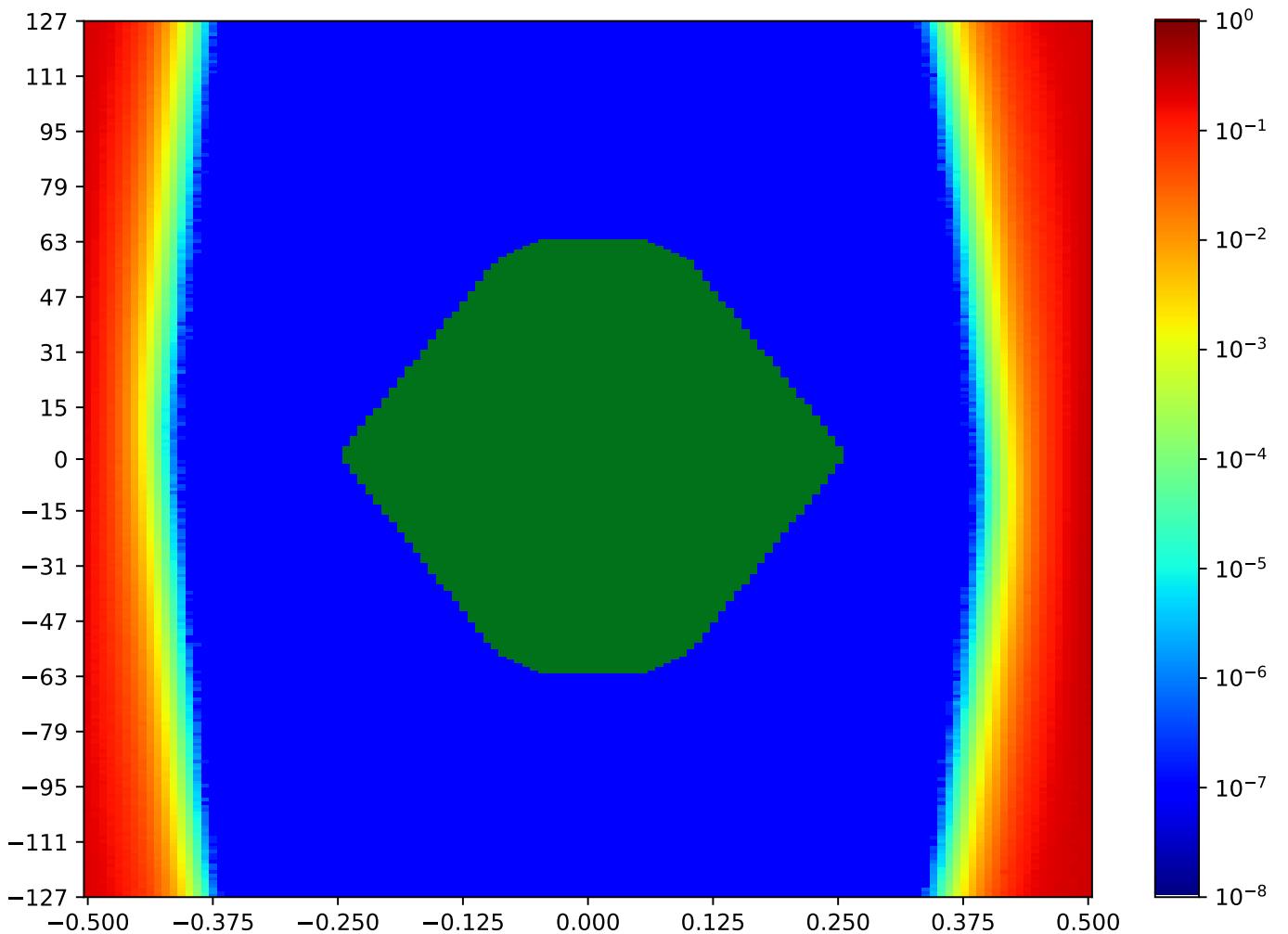


Figure 4.23: MSP_A_FPGA-TX2-08-RX16-08-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.10 MSP_A_FPGA-TX2-09-RX16-09-MSP_C_FPGA

Table 4.22: MSP_A_FPGA-TX2-09-RX16-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:01:54		2018-Sep-26 17:03:09	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23606	98		75.97%	254 99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

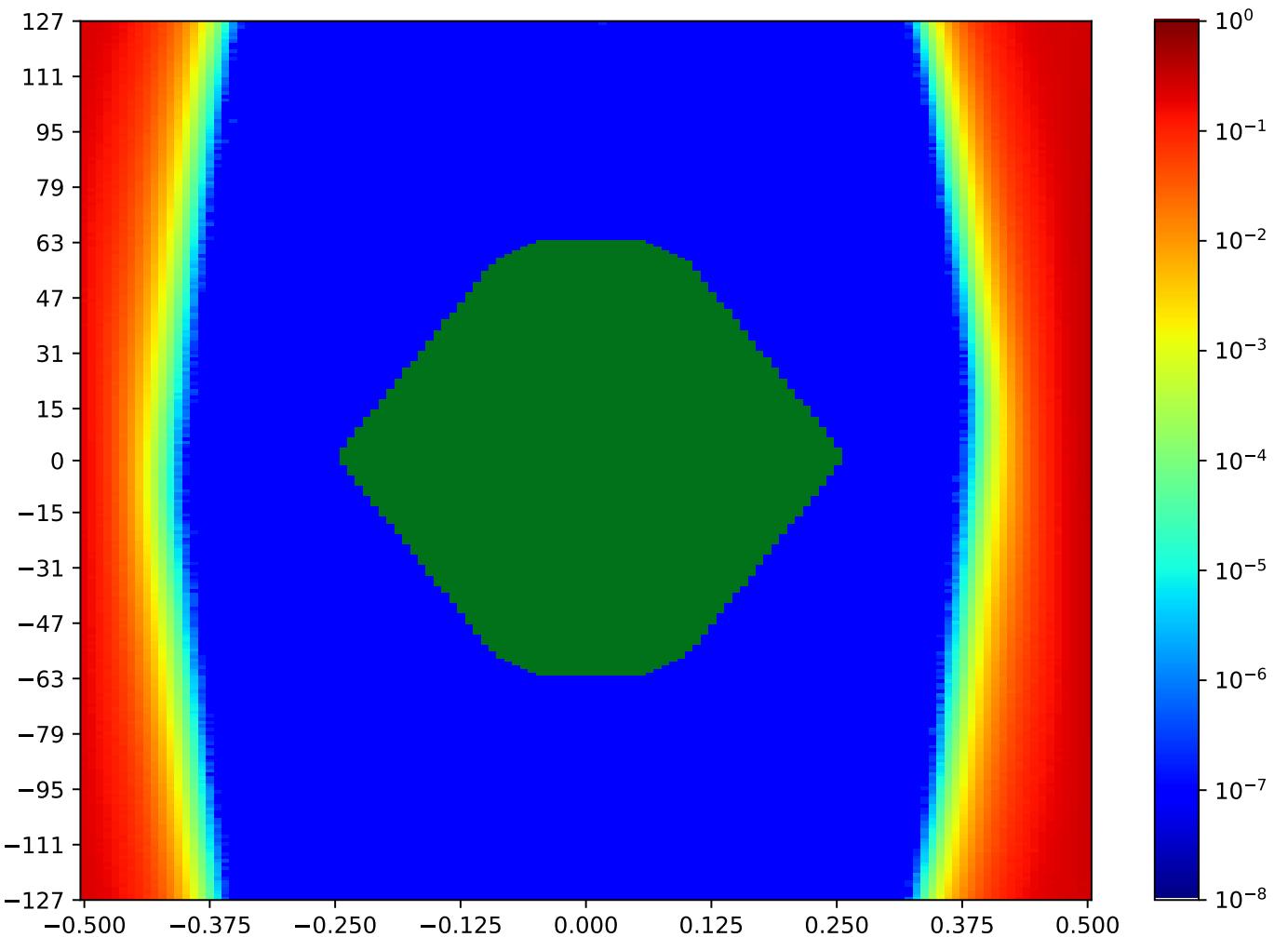


Figure 4.24: MSP_A_FPGA-TX2-09-RX16-09-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.11 MSP_A_FPGA-TX2-10-RX16-10-MSP_C_FPGA

Table 4.23: MSP_A_FPGA-TX2-10-RX16-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:05:40		2018-Sep-26 17:06:55	
Reset RX	OA	HO		VO	VO (%)
true	24310	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

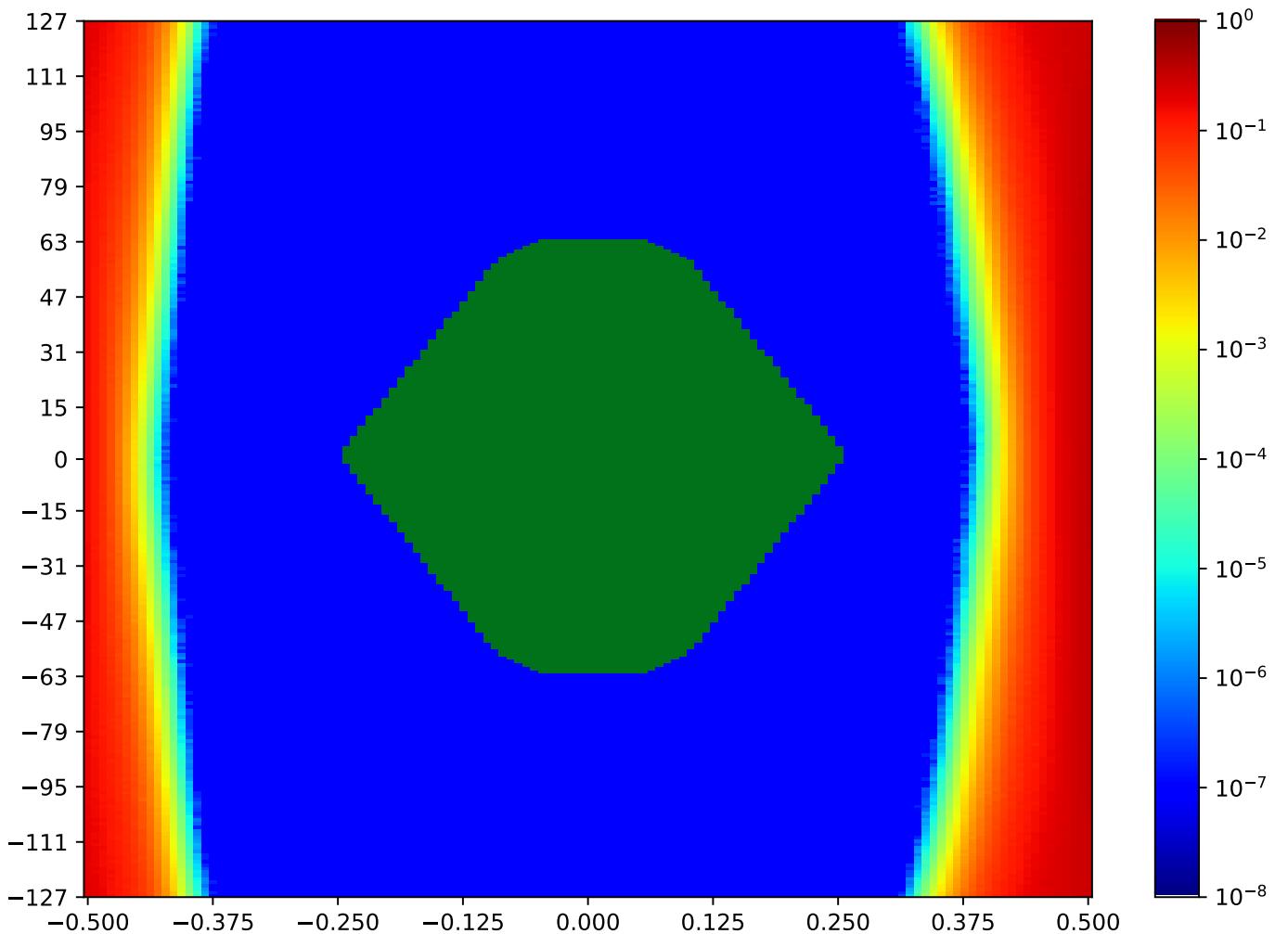


Figure 4.25: MSP_A_FPGA-TX2-10-RX16-10-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.2.12 MSP_A_FPGA-TX2-11-RX16-11-MSP_C_FPGA

Table 4.24: MSP_A_FPGA-TX2-11-RX16-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:04:24		2018-Sep-26 17:05:39	
Reset RX	OA	HO		VO	VO (%)
true	24496	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

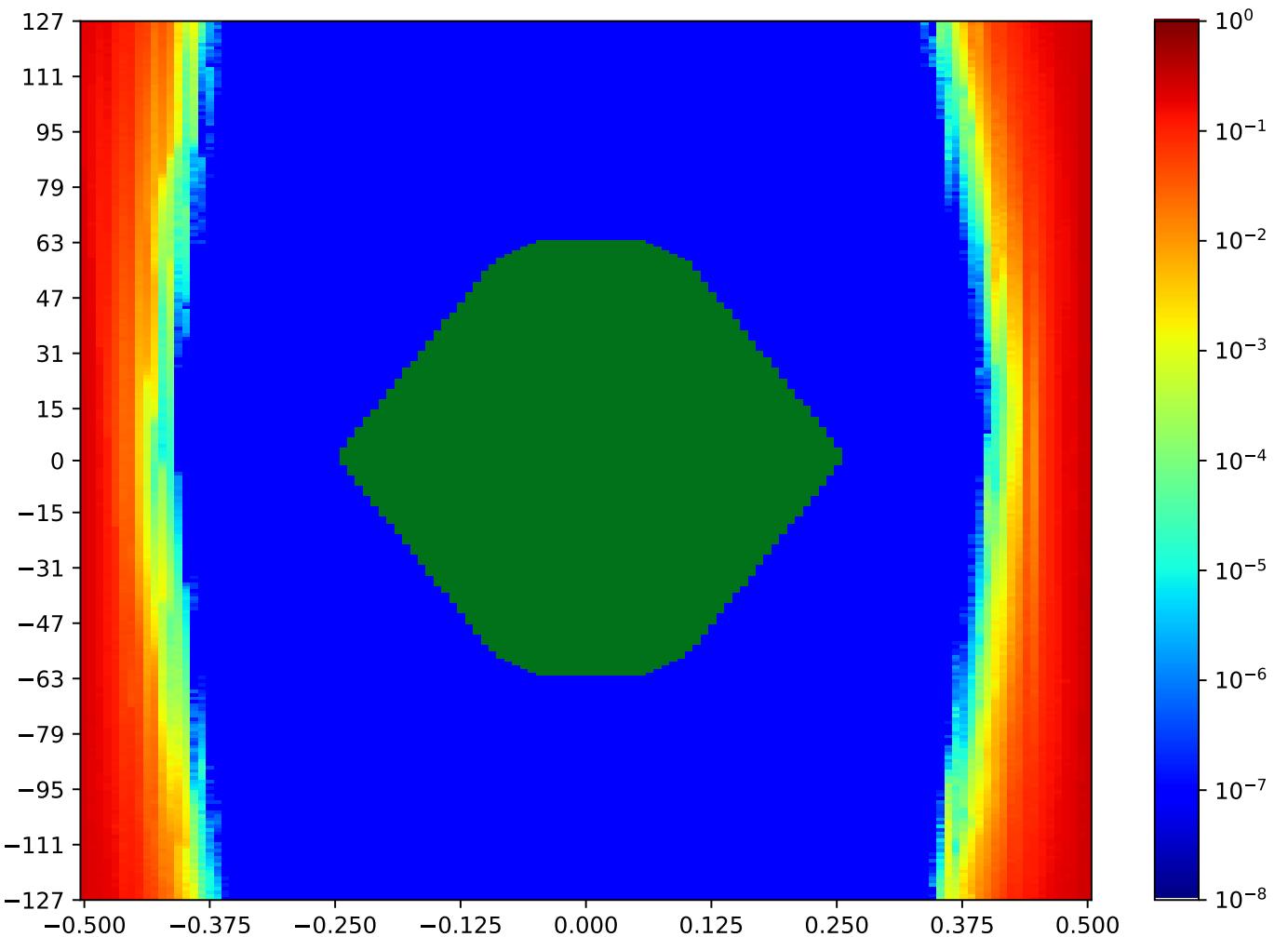


Figure 4.26: MSP_A_FPGA-TX2-11-RX16-11-MSP_C_FPGA

Call back to summary Figure 4.14. Sibling eye diagrams: V2-12.8.

4.3 MSP_C TX3 MSP_A RX6 Minipod Loopback

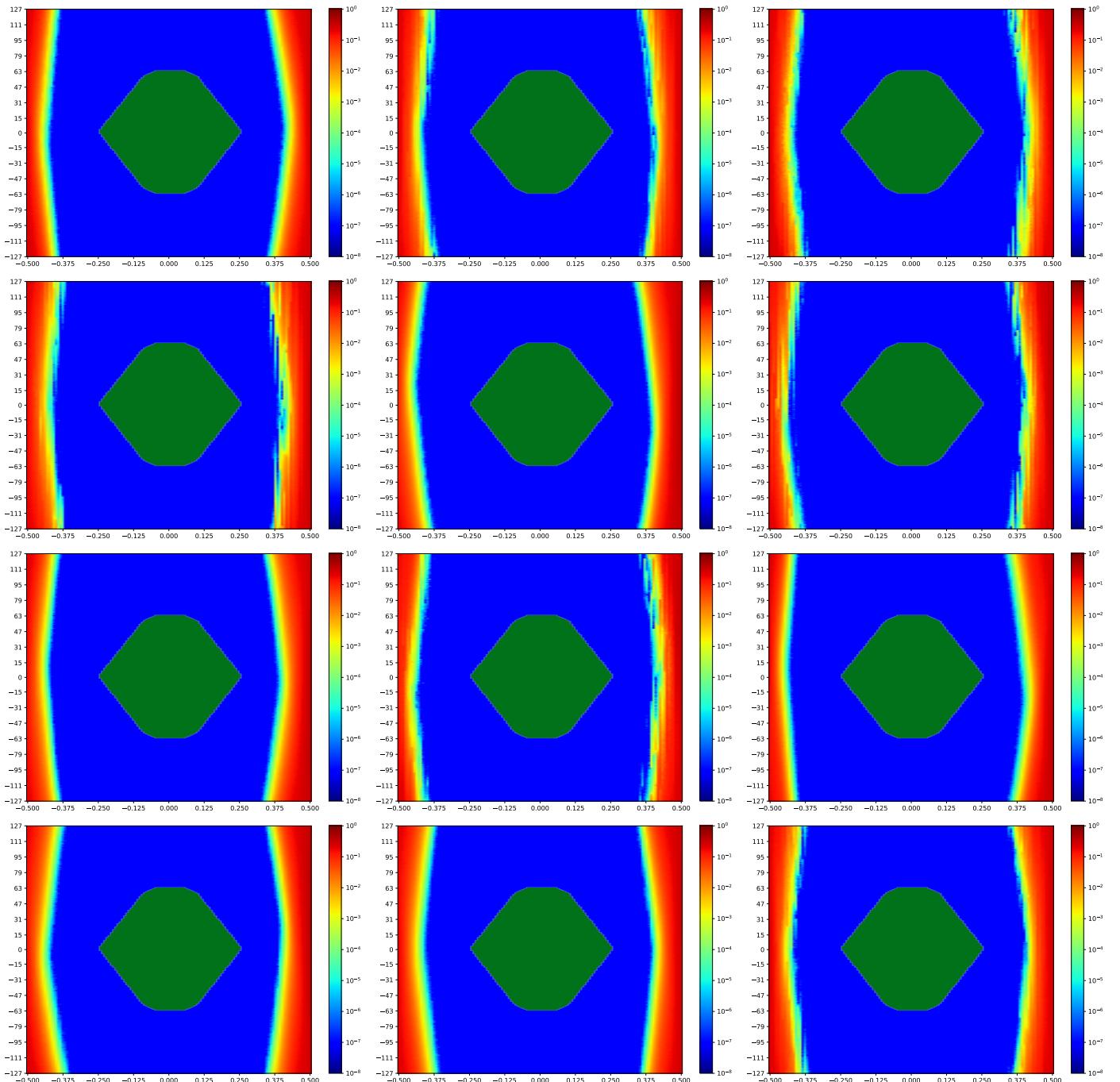


Figure 4.27: MSP_C TX3 MSP_A RX6 Minipod Loopback

A cross-reference to Figure 4.27. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.40.

4.3.1 MSP_C_FPGA-TX3-00-RX6-00-MSP_A_FPGA

Table 4.25: MSP_C_FPGA-TX3-00-RX6-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:14:31		2018-Sep-26 17:15:47	
Reset RX	OA	HO		VO	VO (%)
true	25021	104		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

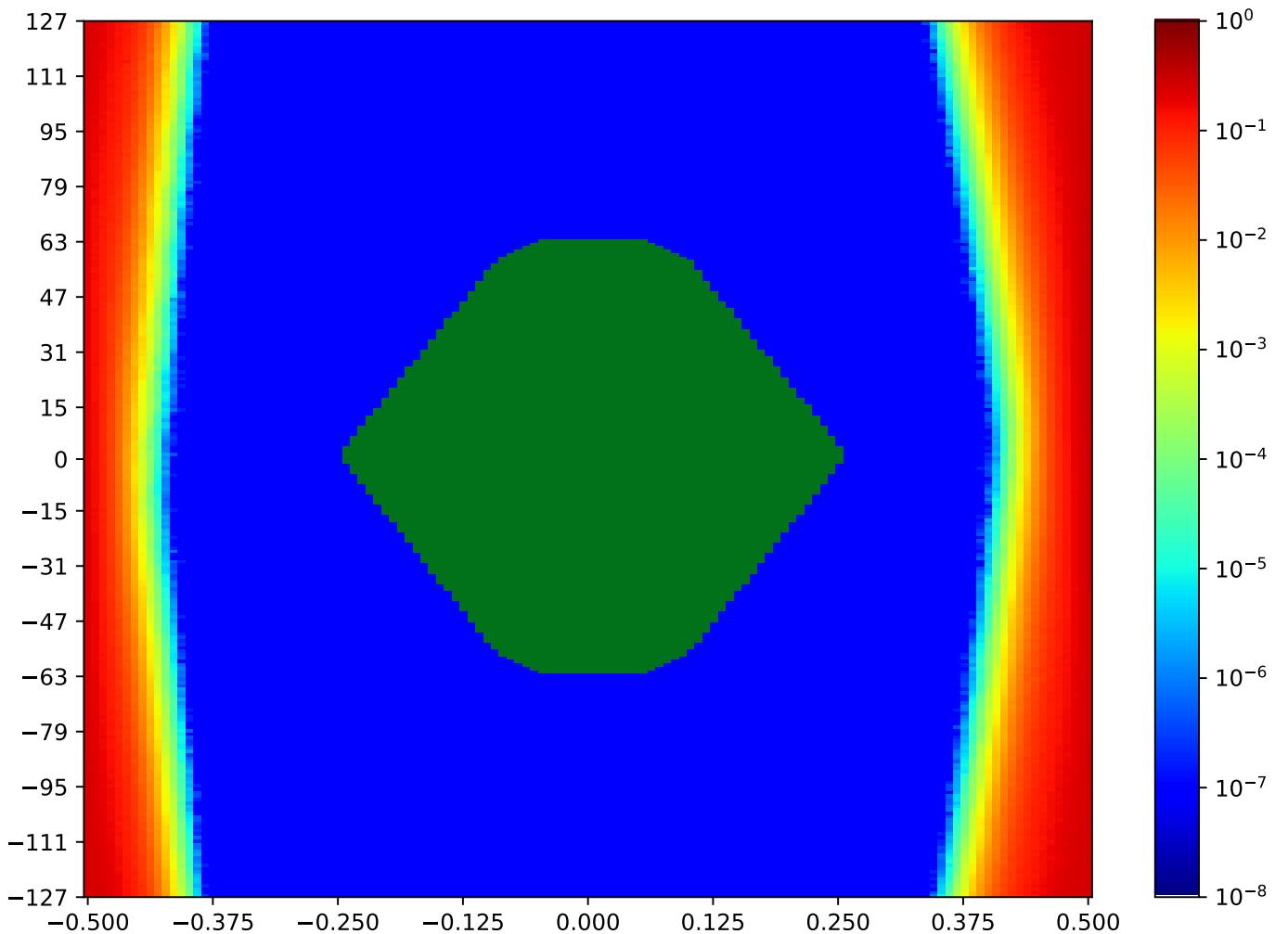


Figure 4.28: MSP_C_FPGA-TX3-00-RX6-00-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.2 MSP_C_FPGA-TX3-01-RX6-01-MSP_A_FPGA

Table 4.26: MSP_C_FPGA-TX3-01-RX6-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:17:03		2018-Sep-26 17:18:19	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24435	102		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

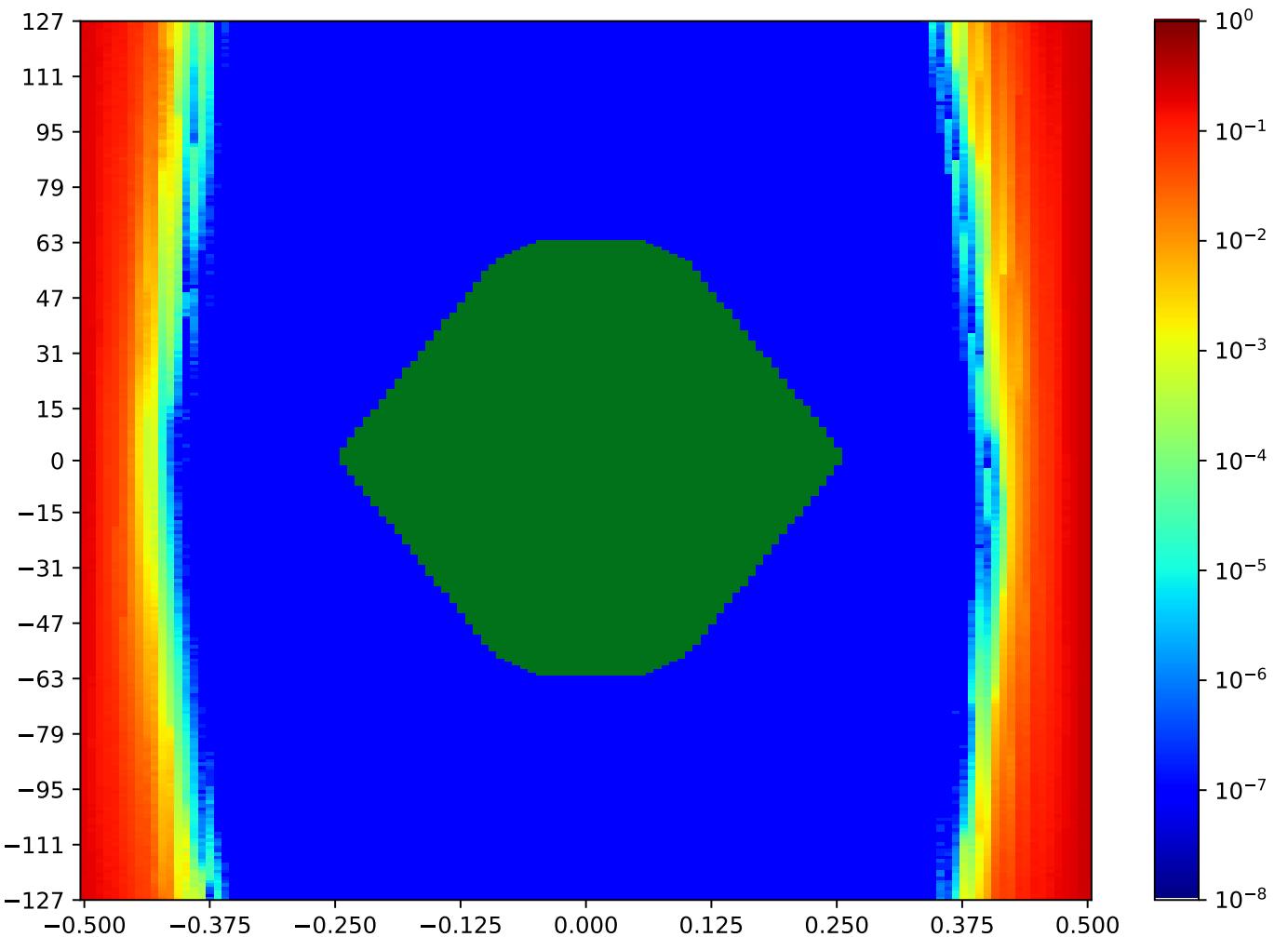


Figure 4.29: MSP_C_FPGA-TX3-01-RX6-01-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.3 MSP_C_FPGA-TX3-02-RX6-02-MSP_A_FPGA

Table 4.27: MSP_C_FPGA-TX3-02-RX6-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:18:19		2018-Sep-26 17:19:35	
Reset RX	OA	HO		VO	VO (%)
true	24560	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

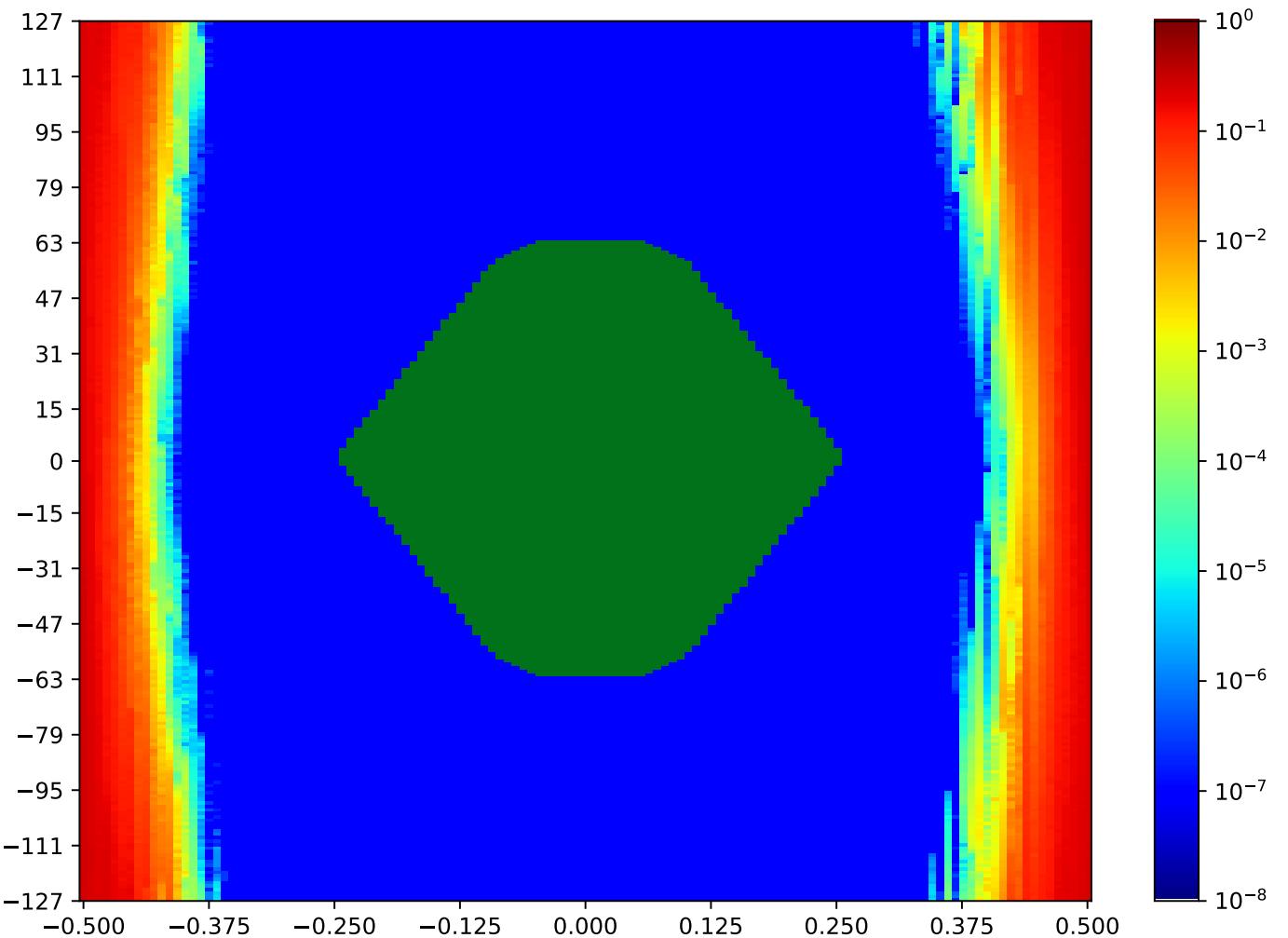


Figure 4.30: MSP_C_FPGA-TX3-02-RX6-02-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.4 MSP_C_FPGA-TX3-03-RX6-03-MSP_A_FPGA

Table 4.28: MSP_C_FPGA-TX3-03-RX6-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:11:58		2018-Sep-26 17:13:14	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24559	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

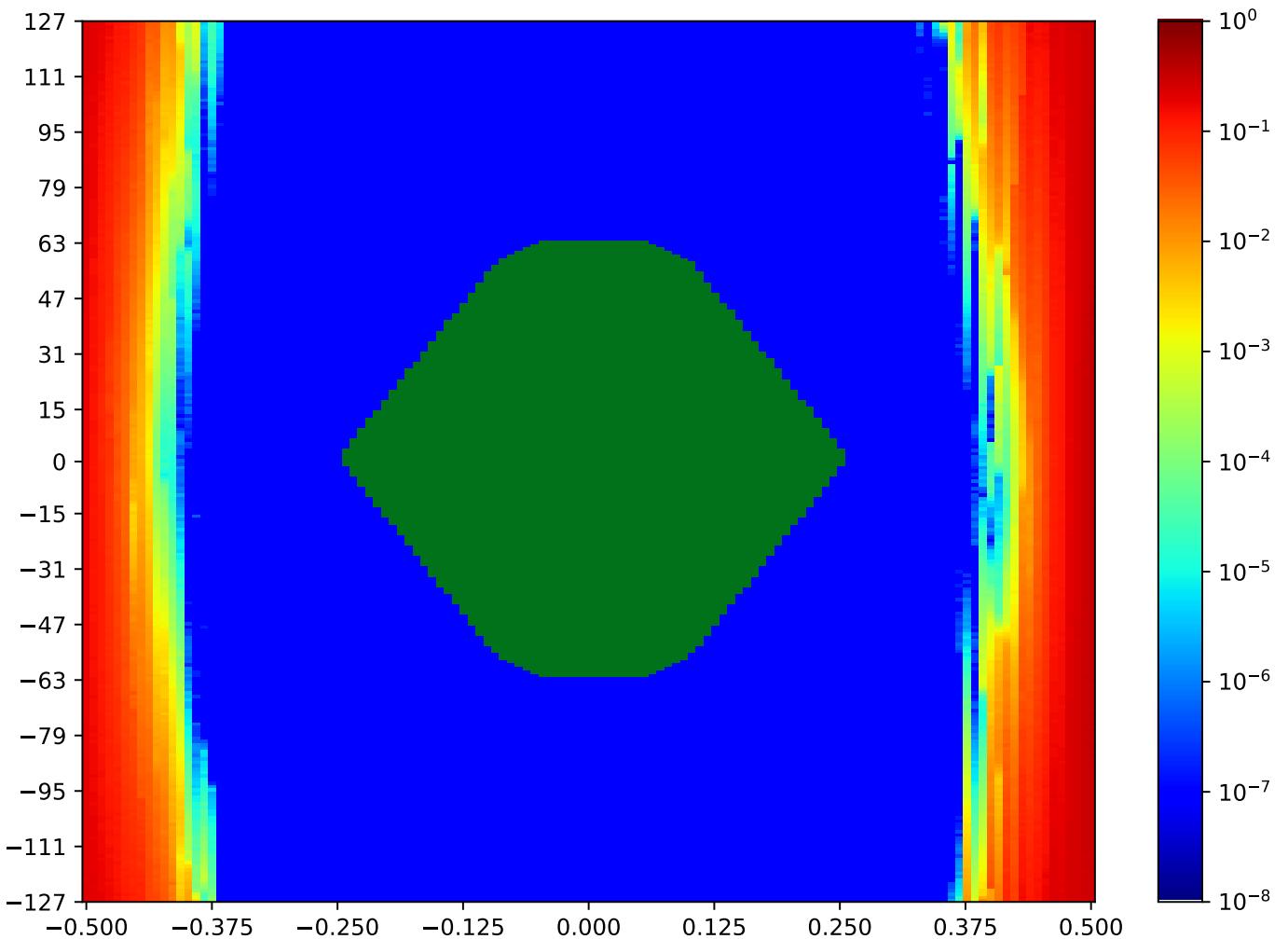


Figure 4.31: MSP_C_FPGA-TX3-03-RX6-03-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.5 MSP_C_FPGA-TX3-04-RX6-04-MSP_A_FPGA

Table 4.29: MSP_C_FPGA-TX3-04-RX6-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:22:04		2018-Sep-26 17:23:19	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24910	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

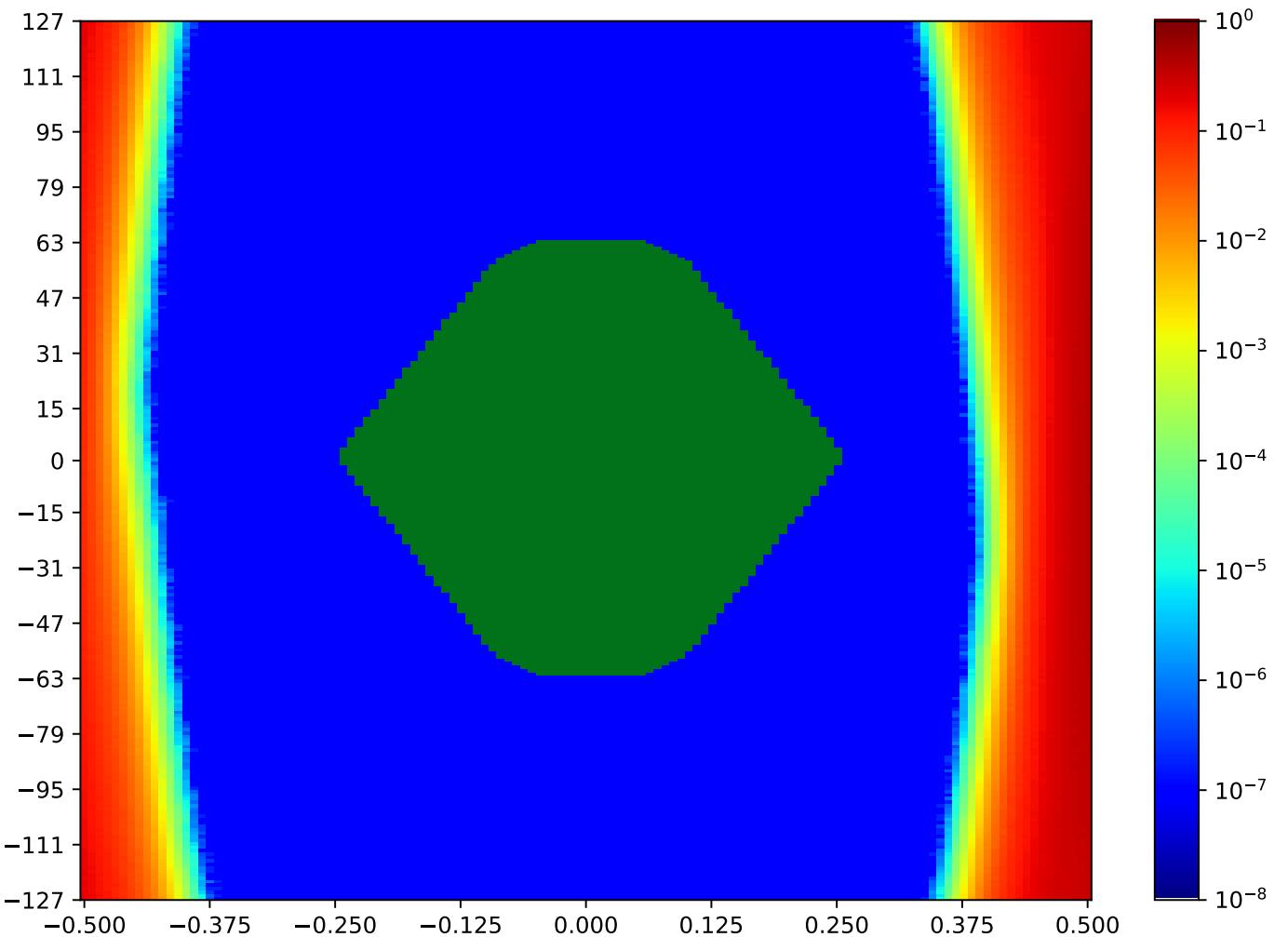


Figure 4.32: MSP_C_FPGA-TX3-04-RX6-04-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.6 MSP_C_FPGA-TX3-05-RX6-05-MSP_A_FPGA

Table 4.30: MSP_C_FPGA-TX3-05-RX6-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:10:42		2018-Sep-26 17:11:57	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24910	104		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

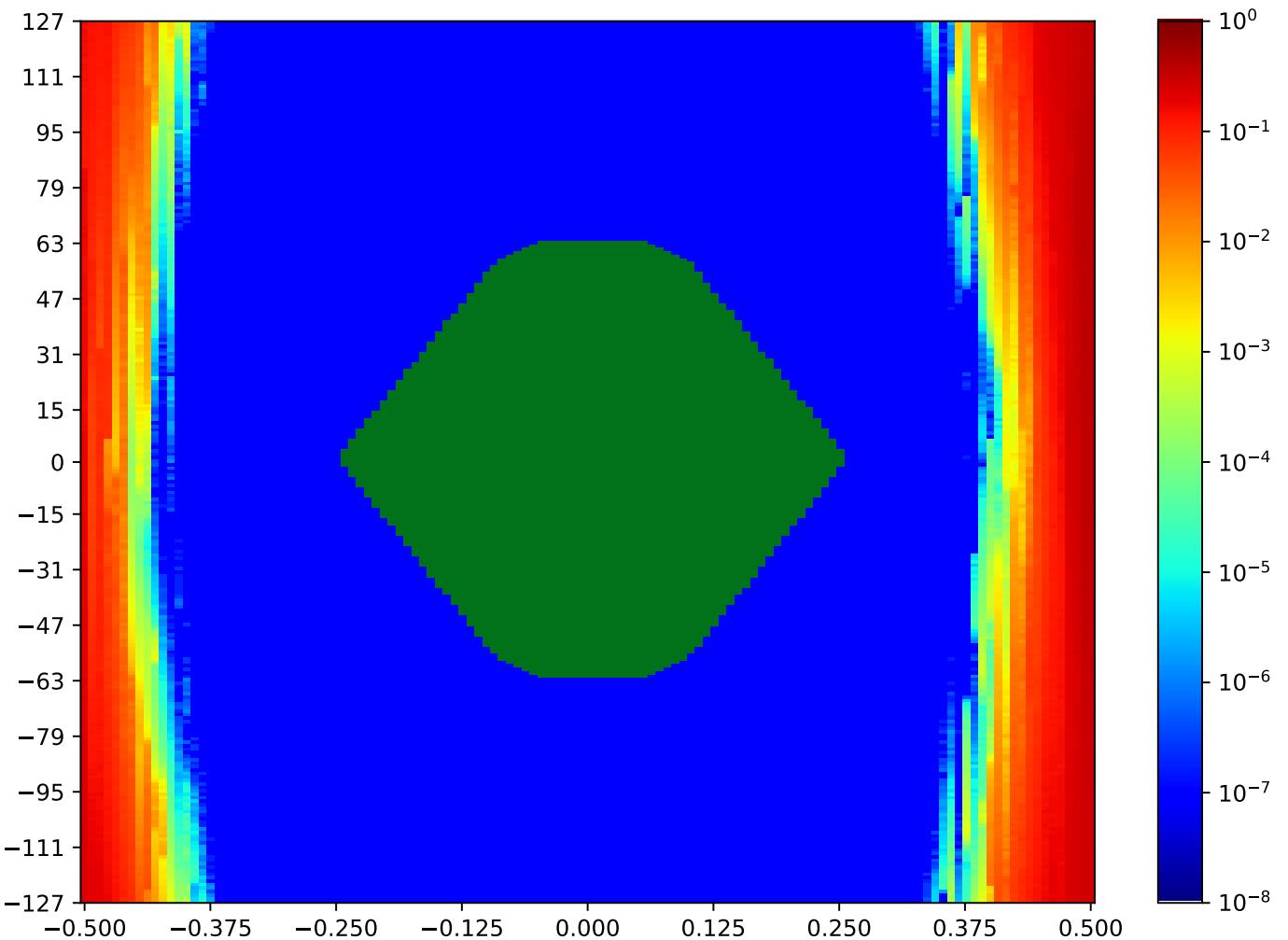


Figure 4.33: MSP_C_FPGA-TX3-05-RX6-05-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.7 MSP_C_FPGA-TX3-06-RX6-06-MSP_A_FPGA

Table 4.31: MSP_C_FPGA-TX3-06-RX6-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:24:35		2018-Sep-26 17:25:50	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24588	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

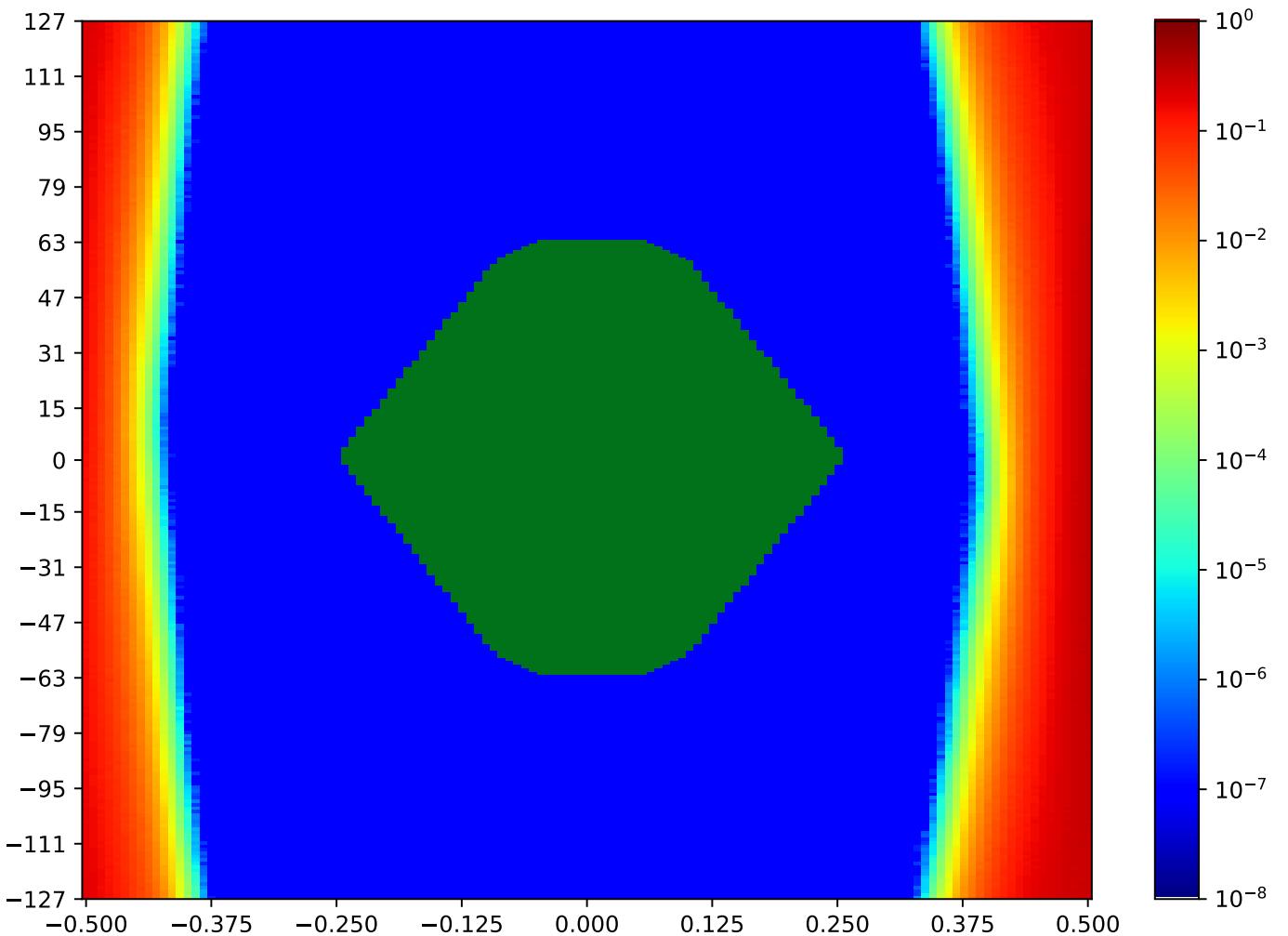


Figure 4.34: MSP_C_FPGA-TX3-06-RX6-06-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.8 MSP_C_FPGA-TX3-07-RX6-07-MSP_A_FPGA

Table 4.32: MSP_C_FPGA-TX3-07-RX6-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:13:14		2018-Sep-26 17:14:30	
Reset RX	OA	HO		VO	VO (%)
true	25525	105		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

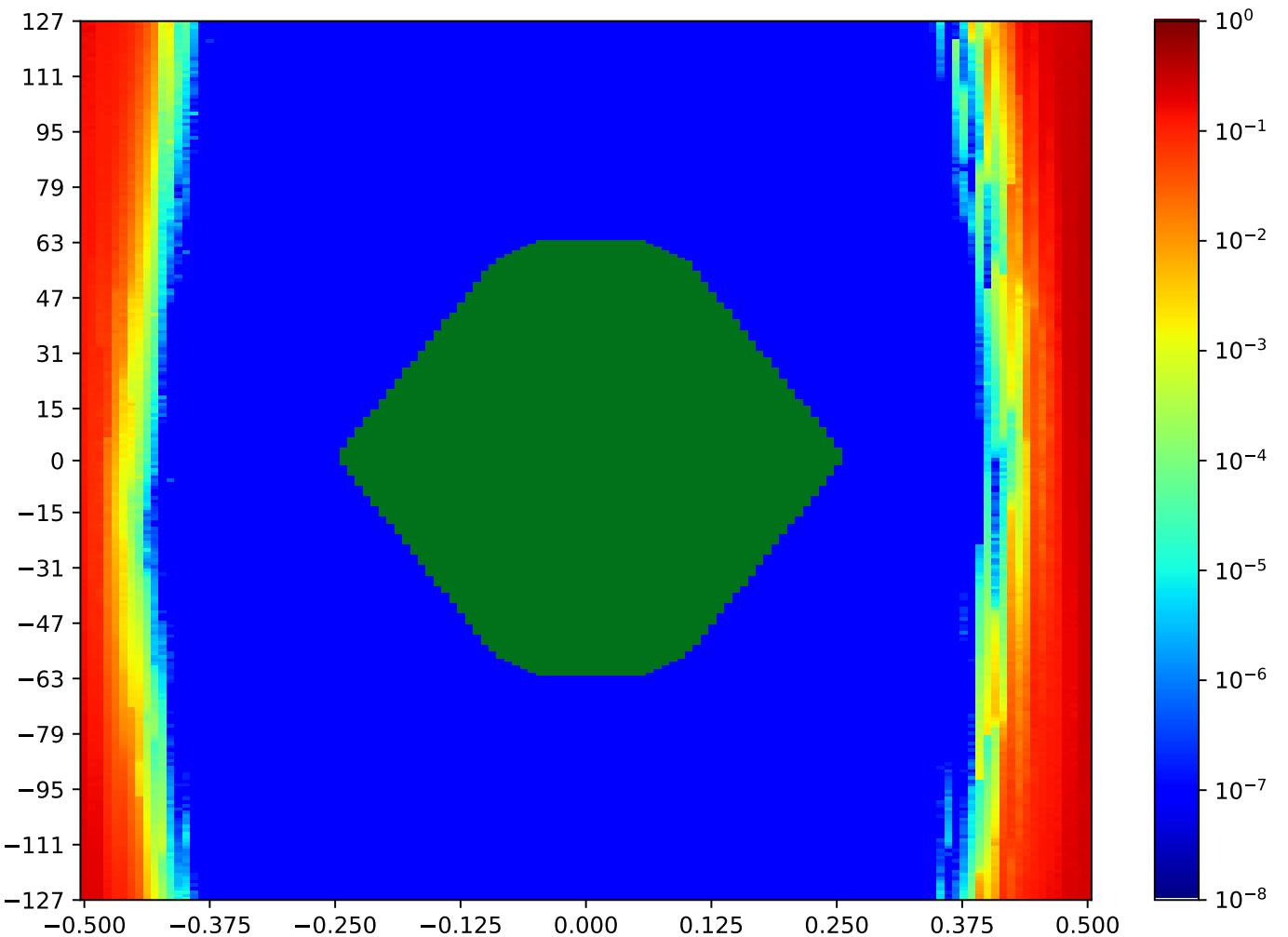


Figure 4.35: MSP_C_FPGA-TX3-07-RX6-07-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.9 MSP_C_FPGA-TX3-08-RX6-08-MSP_A_FPGA

Table 4.33: MSP_C_FPGA-TX3-08-RX6-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:23:19		2018-Sep-26 17:24:35	
Reset RX	OA	HO		VO	VO (%)
true	25074	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

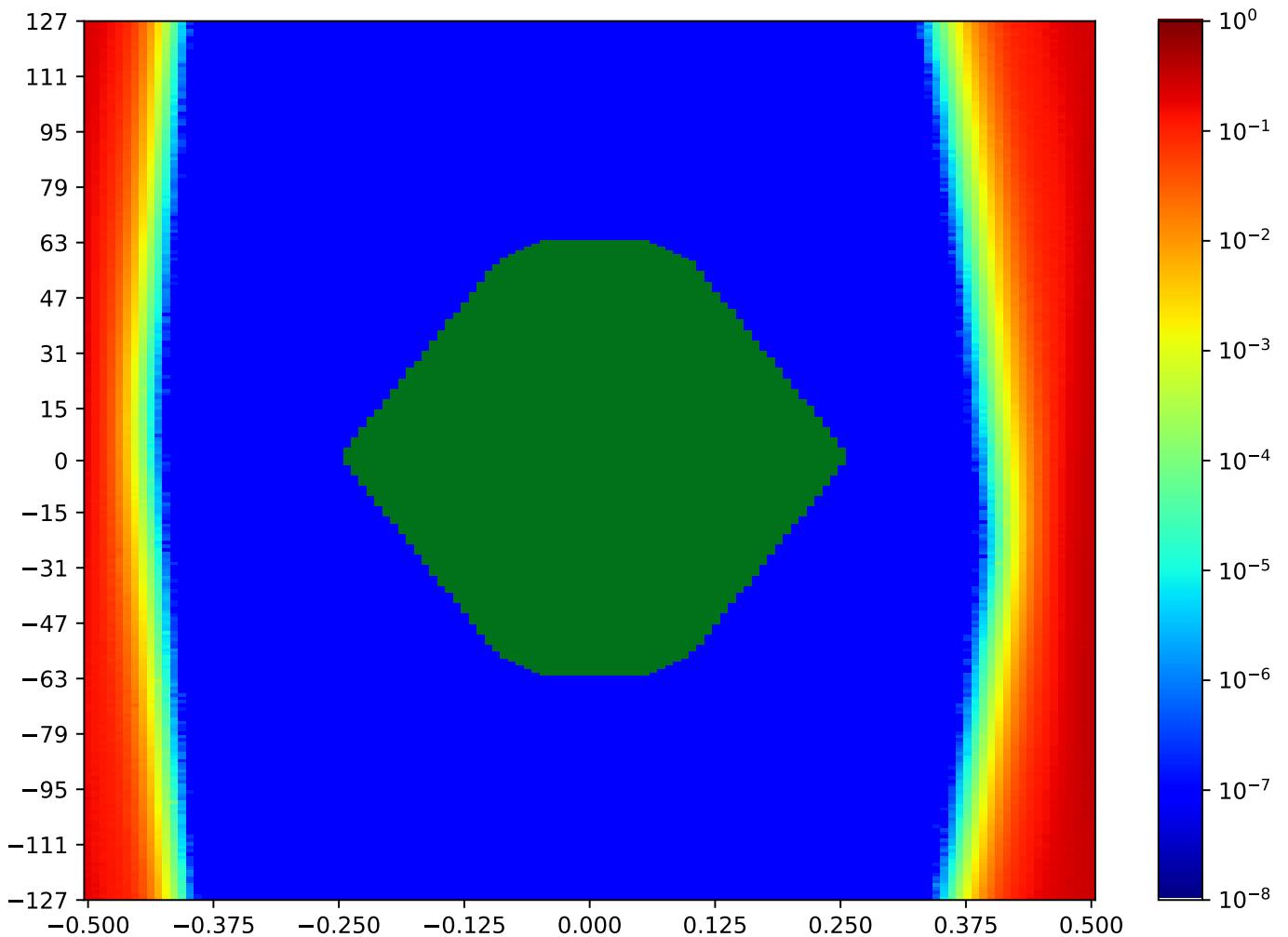


Figure 4.36: MSP_C_FPGA-TX3-08-RX6-08-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.10 MSP_C_FPGA-TX3-09-RX6-09-MSP_A_FPGA

Table 4.34: MSP_C_FPGA-TX3-09-RX6-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:15:47		2018-Sep-26 17:17:03	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24341	101		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

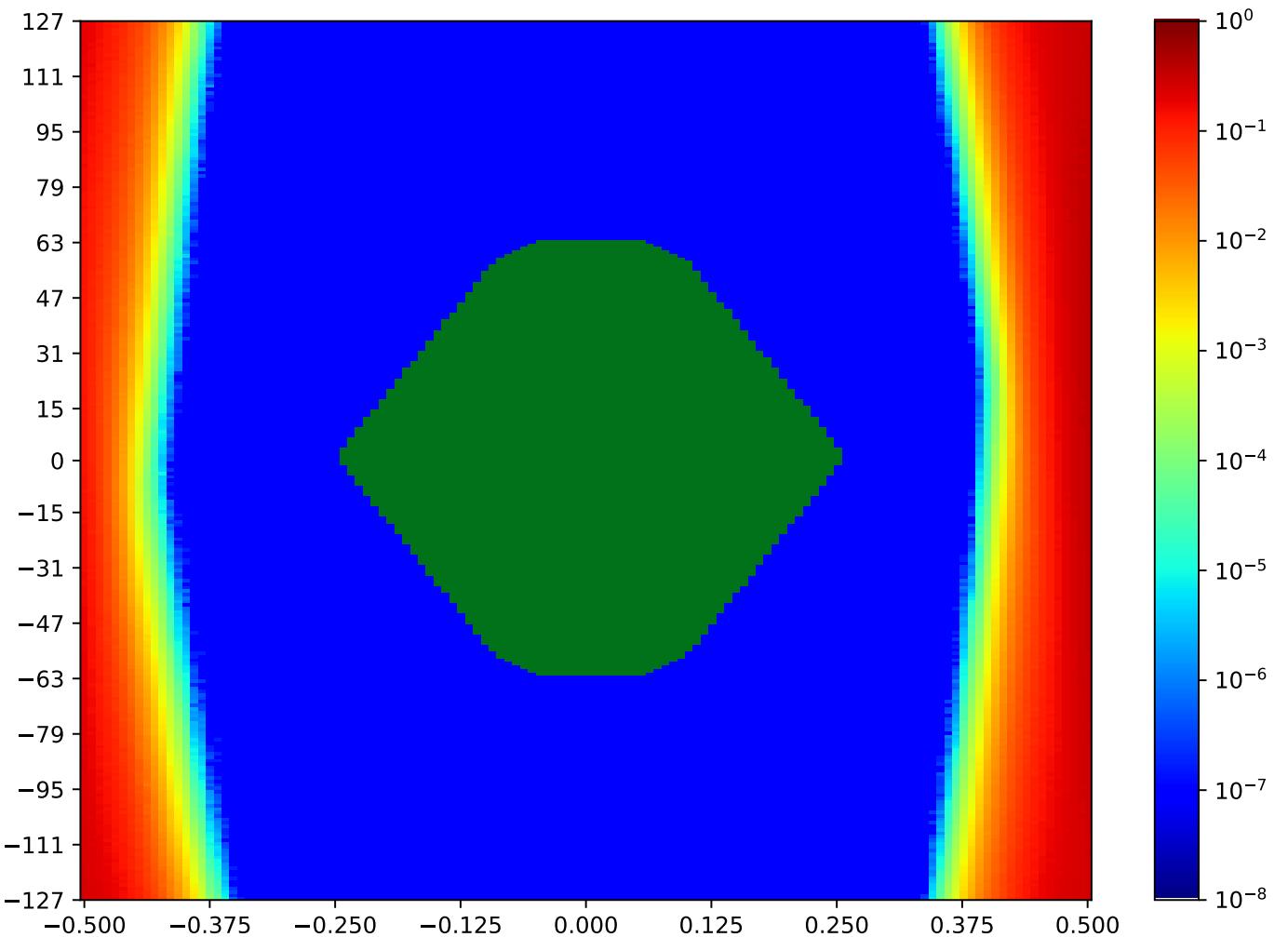


Figure 4.37: MSP_C_FPGA-TX3-09-RX6-09-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.11 MSP_C_FPGA-TX3-10-RX6-10-MSP_A_FPGA

Table 4.35: MSP_C_FPGA-TX3-10-RX6-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:20:50		2018-Sep-26 17:22:04	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24235	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

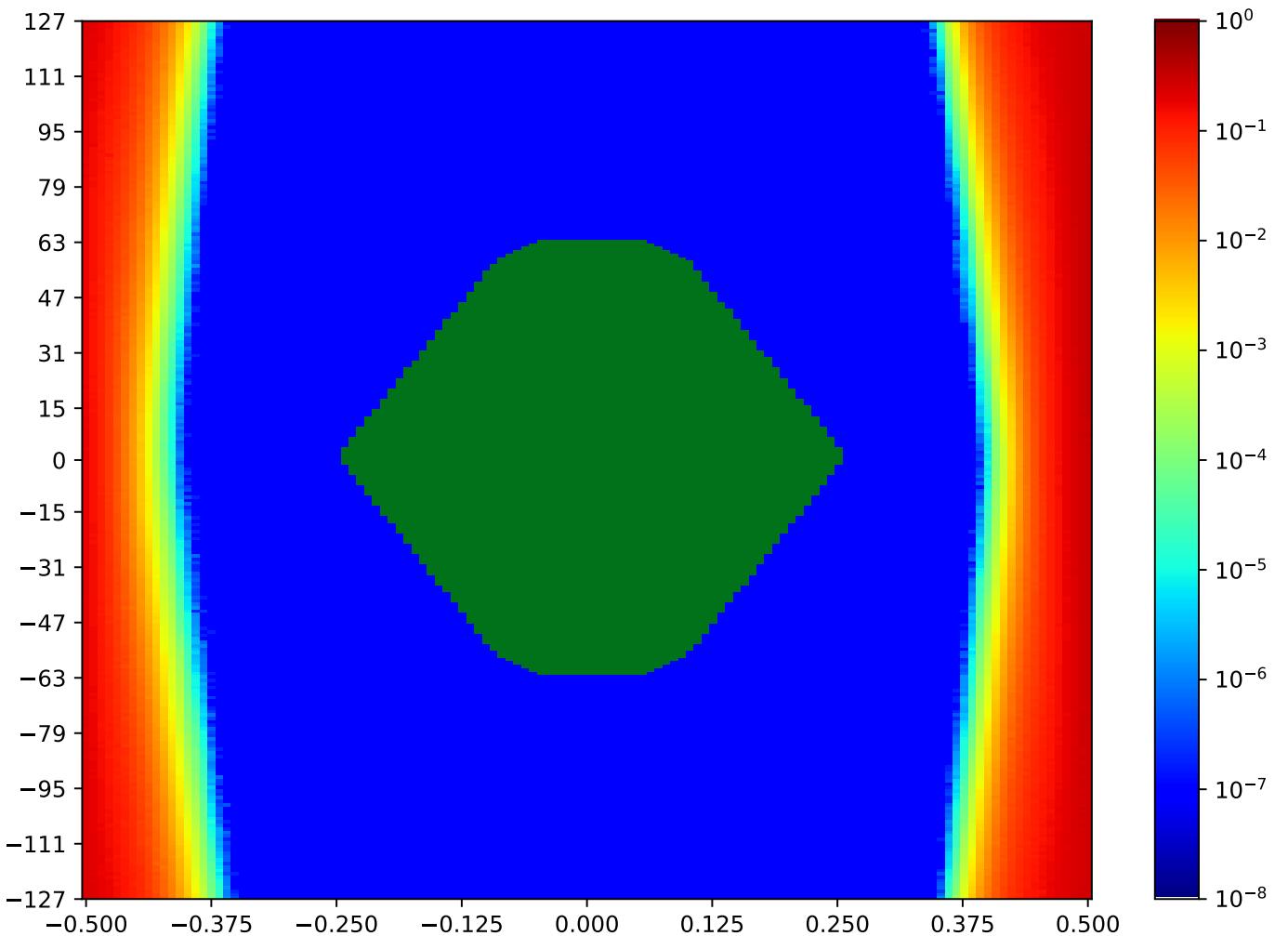


Figure 4.38: MSP_C_FPGA-TX3-10-RX6-10-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.3.12 MSP_C_FPGA-TX3-11-RX6-11-MSP_A_FPGA

Table 4.36: MSP_C_FPGA-TX3-11-RX6-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:19:35		2018-Sep-26 17:20:49	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24756	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

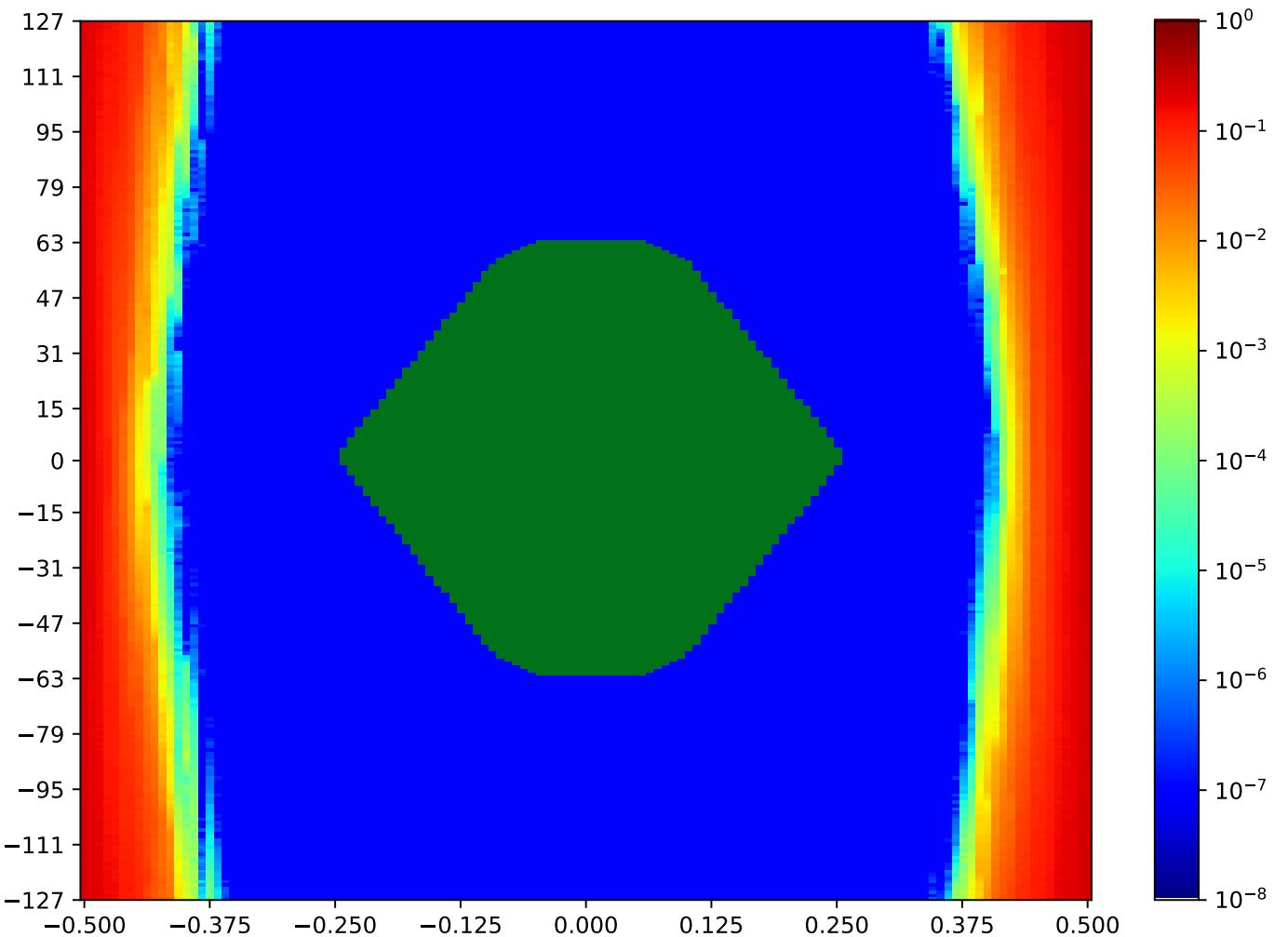


Figure 4.39: MSP_C_FPGA-TX3-11-RX6-11-MSP_A_FPGA

Call back to summary Figure 4.27. Sibling eye diagrams: V2-12.8.

4.4 MSP_C TX4 MSP_A RX7 Minipod Loopback

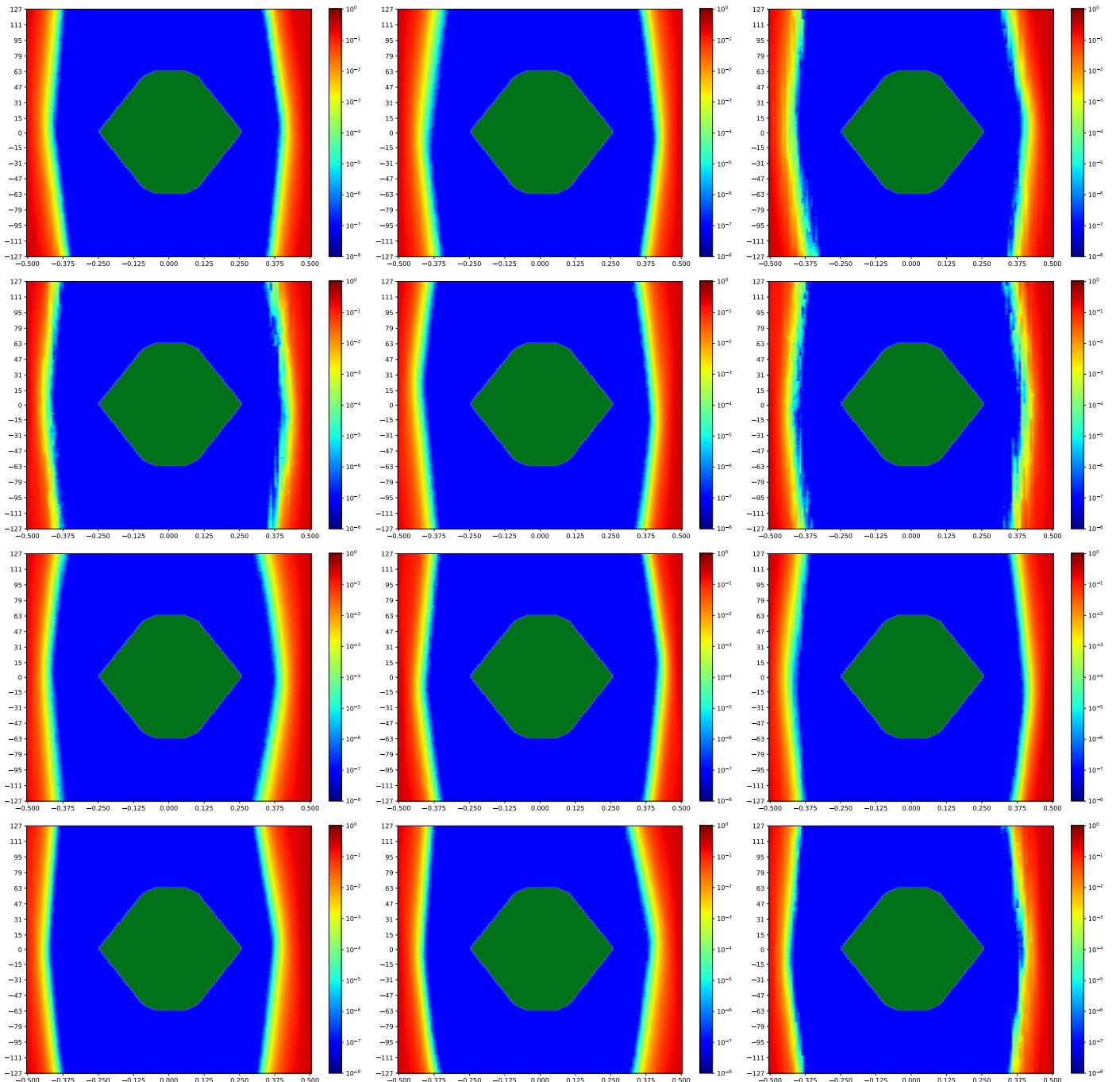


Figure 4.40: MSP_C TX4 MSP_A RX7 Minipod Loopback

A cross-reference to Figure 4.40. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.53.

4.4.1 MSP_C_FPGA-TX4-00-RX7-00-MSP_A_FPGA

Table 4.37: MSP_C_FPGA-TX4-00-RX7-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:29:35		2018-Sep-26 17:30:50	
Reset RX	OA	HO		VO	VO (%)
true	23933	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

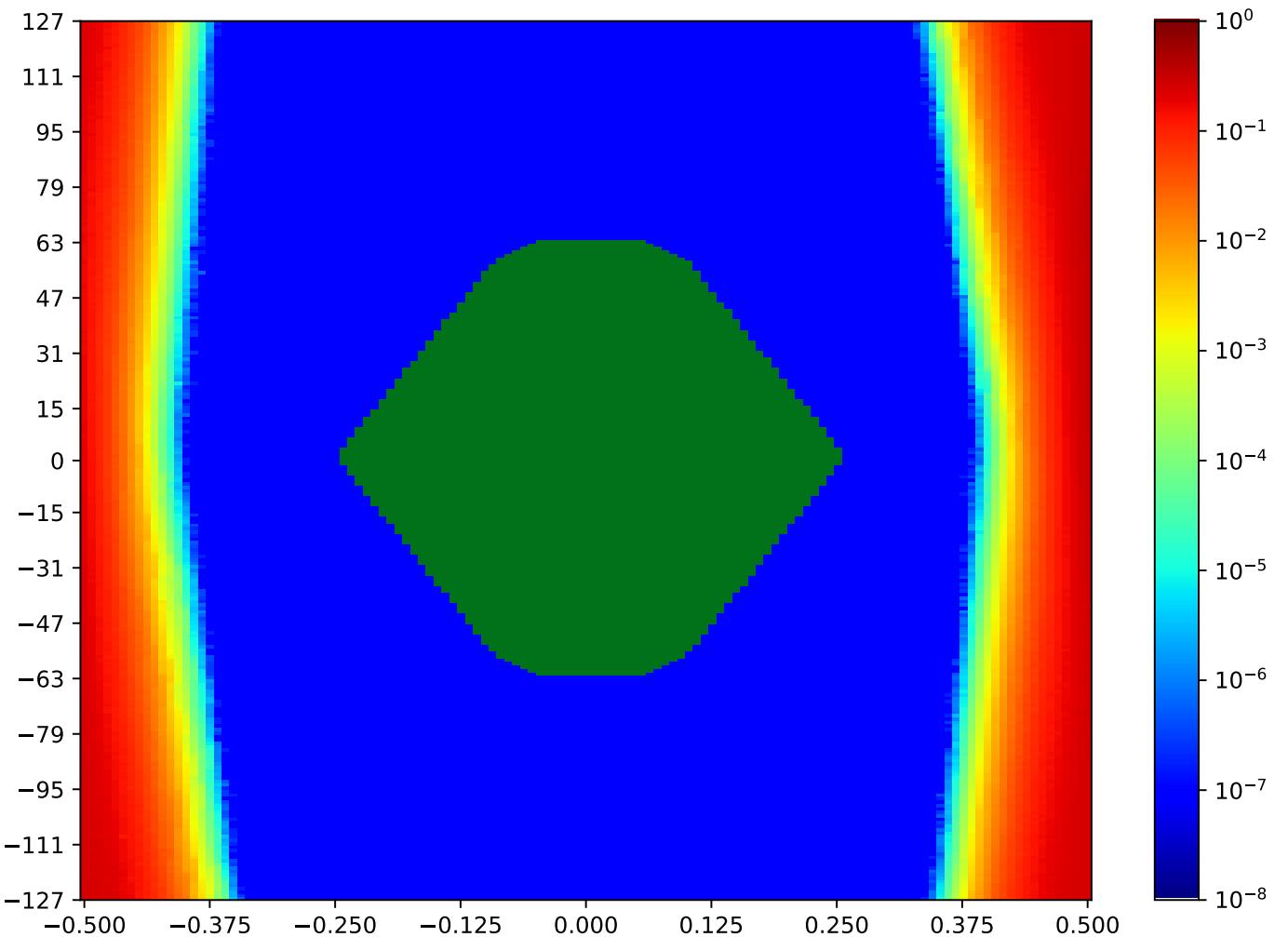


Figure 4.41: MSP_C_FPGA-TX4-00-RX7-00-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.2 MSP_C_FPGA-TX4-01-RX7-01-MSP_A_FPGA

Table 4.38: MSP_C_FPGA-TX4-01-RX7-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:27:05		2018-Sep-26 17:28:20	
Reset RX	OA	HO		VO	VO (%)
true	23686	99		75.97%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

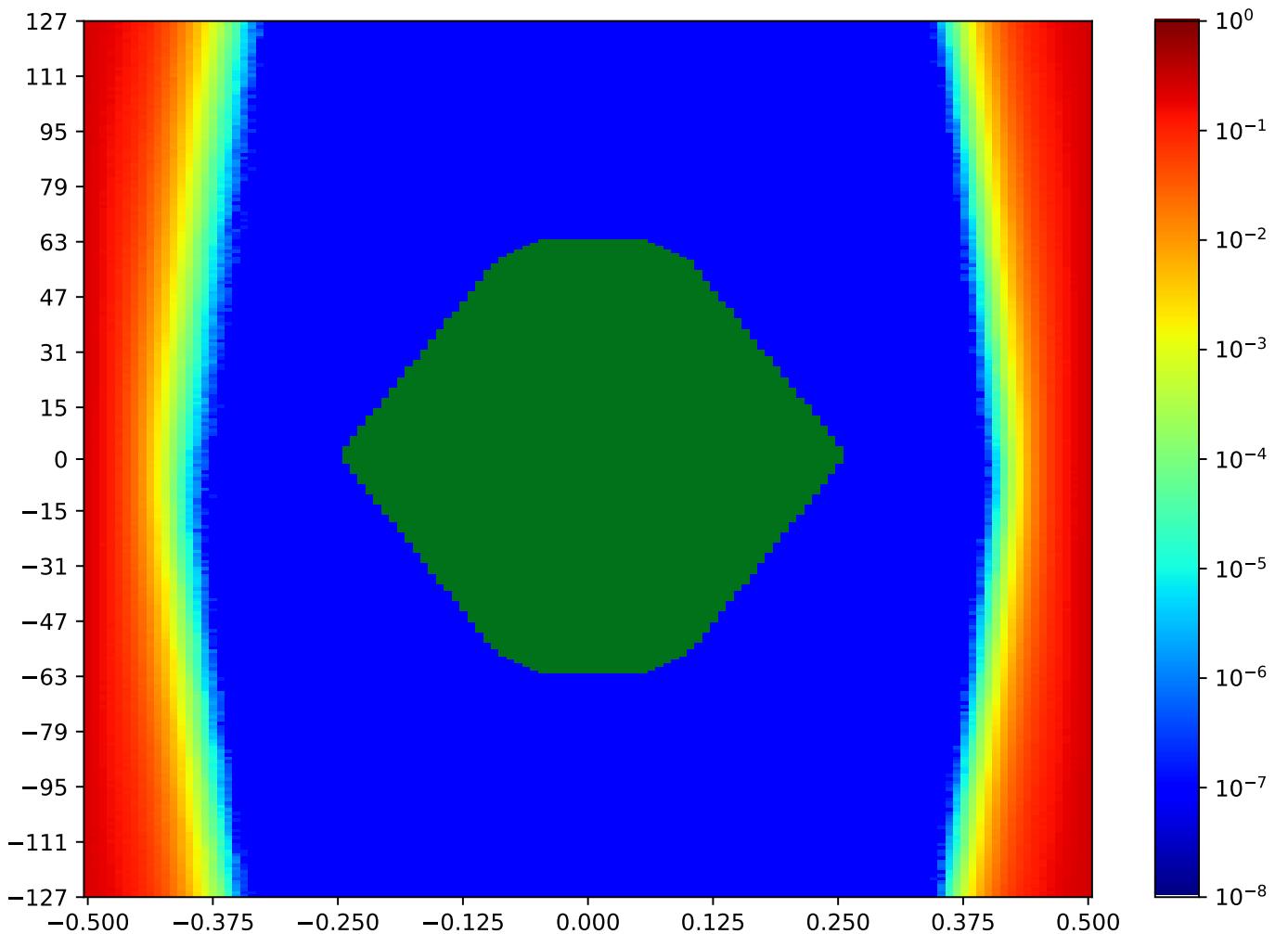


Figure 4.42: MSP_C_FPGA-TX4-01-RX7-01-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.3 MSP_C_FPGA-TX4-02-RX7-02-MSP_A_FPGA

Table 4.39: MSP_C_FPGA-TX4-02-RX7-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:33:21		2018-Sep-26 17:34:35	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23610	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

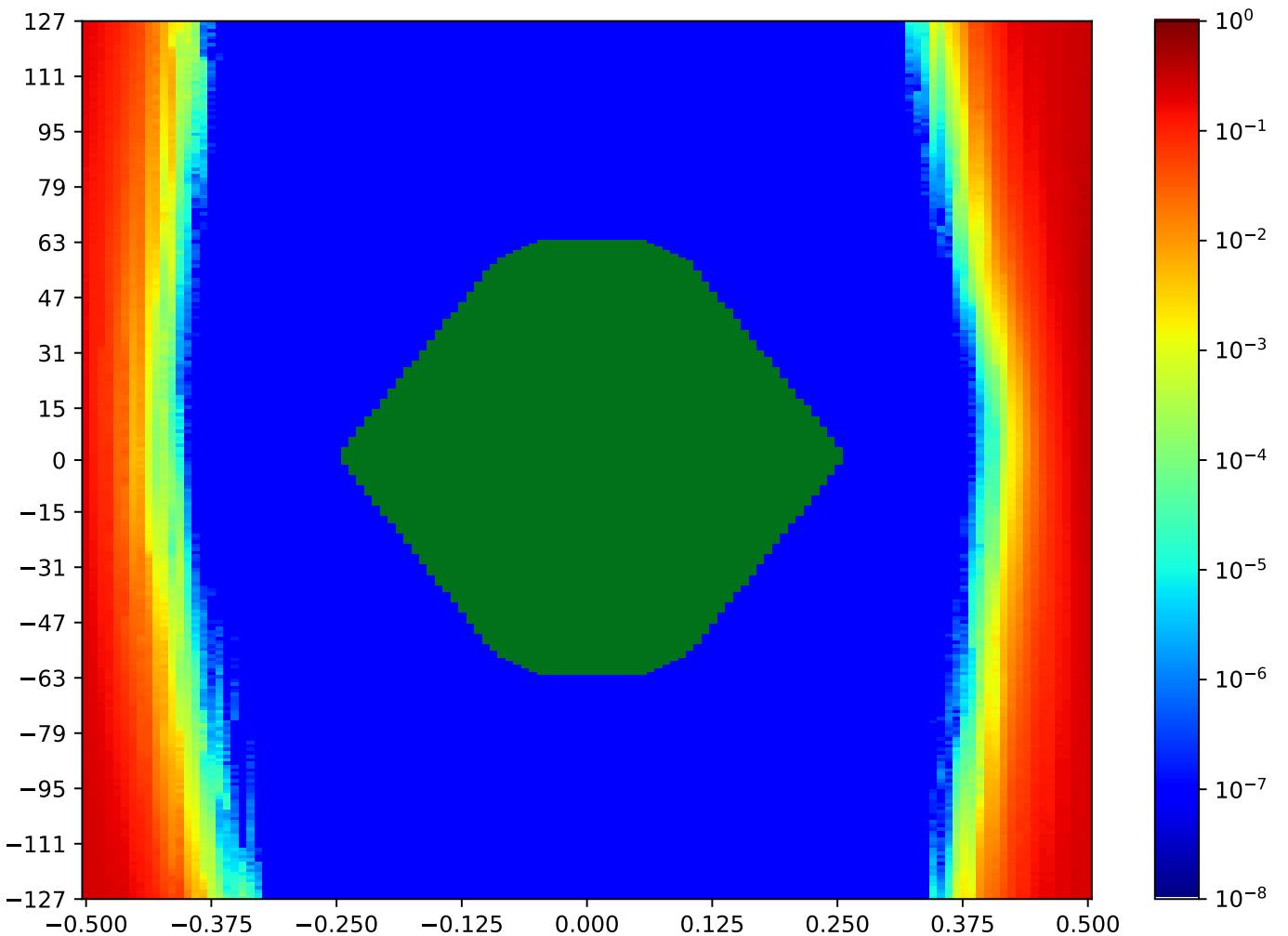


Figure 4.43: MSP_C_FPGA-TX4-02-RX7-02-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.4 MSP_C_FPGA-TX4-03-RX7-03-MSP_A_FPGA

Table 4.40: MSP_C_FPGA-TX4-03-RX7-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:25:50		2018-Sep-26 17:27:05	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24552	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

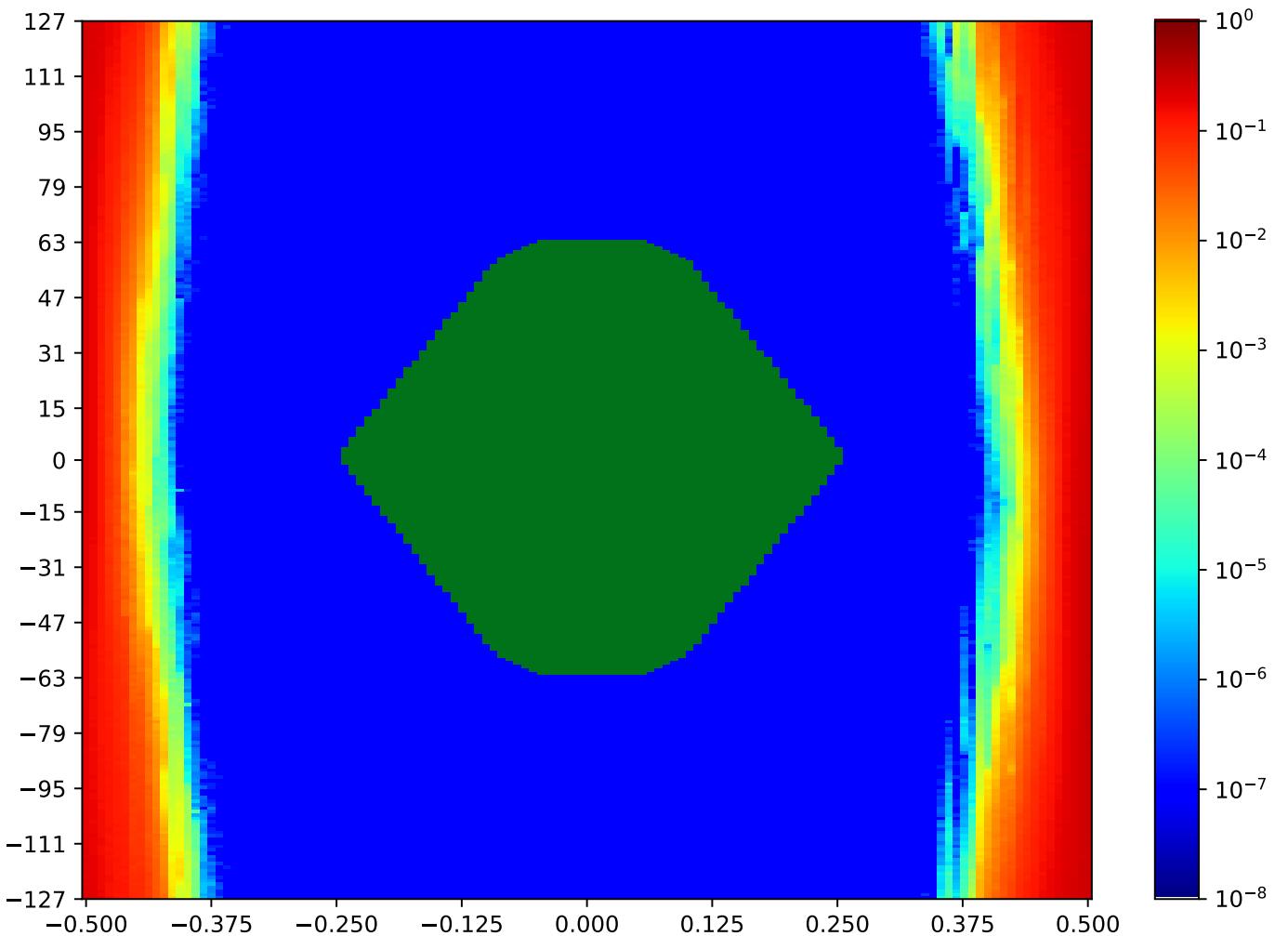


Figure 4.44: MSP_C_FPGA-TX4-03-RX7-03-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.5 MSP_C_FPGA-TX4-04-RX7-04-MSP_A_FPGA

Table 4.41: MSP_C_FPGA-TX4-04-RX7-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:37:06		2018-Sep-26 17:38:20	
Reset RX	OA	HO		VO	VO (%)
true	24029	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

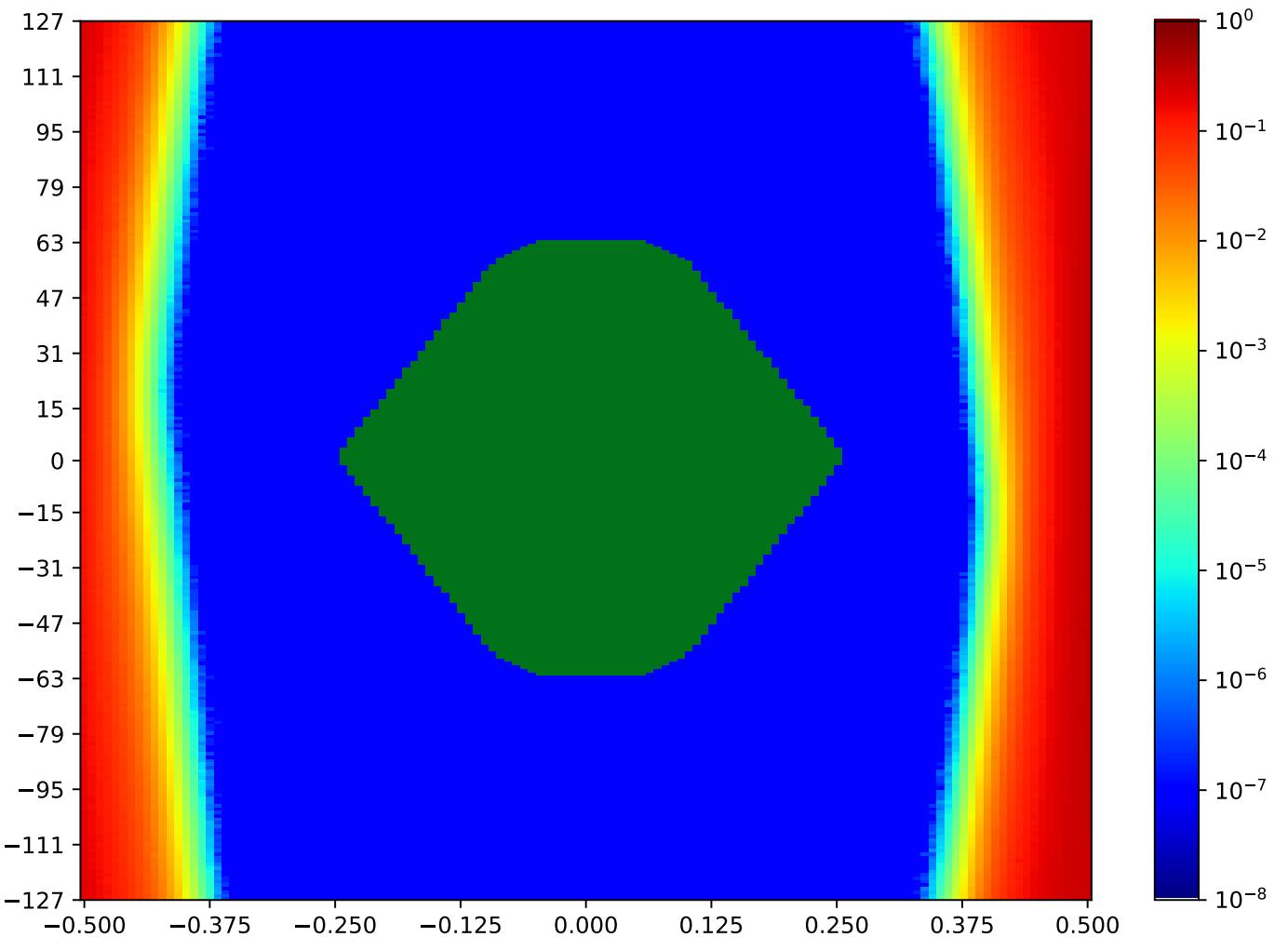


Figure 4.45: MSP_C_FPGA-TX4-04-RX7-04-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.6 MSP_C_FPGA-TX4-05-RX7-05-MSP_A_FPGA

Table 4.42: MSP_C_FPGA-TX4-05-RX7-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:28:20		2018-Sep-26 17:29:35	
Reset RX	OA	HO		VO	VO (%)
true	23714	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

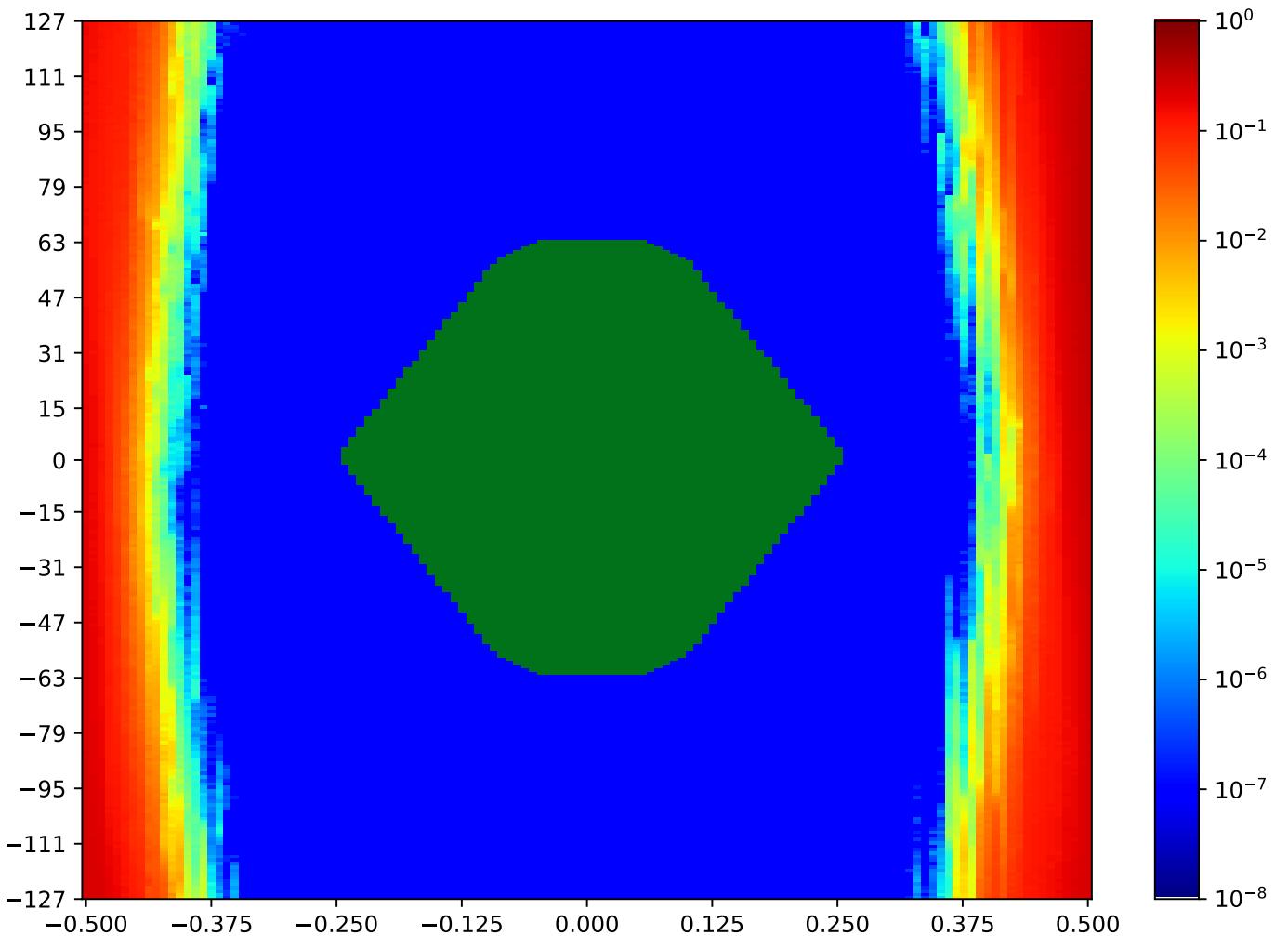


Figure 4.46: MSP_C_FPGA-TX4-05-RX7-05-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.7 MSP_C_FPGA-TX4-06-RX7-06-MSP_A_FPGA

Table 4.43: MSP_C_FPGA-TX4-06-RX7-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:39:35		2018-Sep-26 17:40:50	
Reset RX	OA	HO		VO	VO (%)
true	23313	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

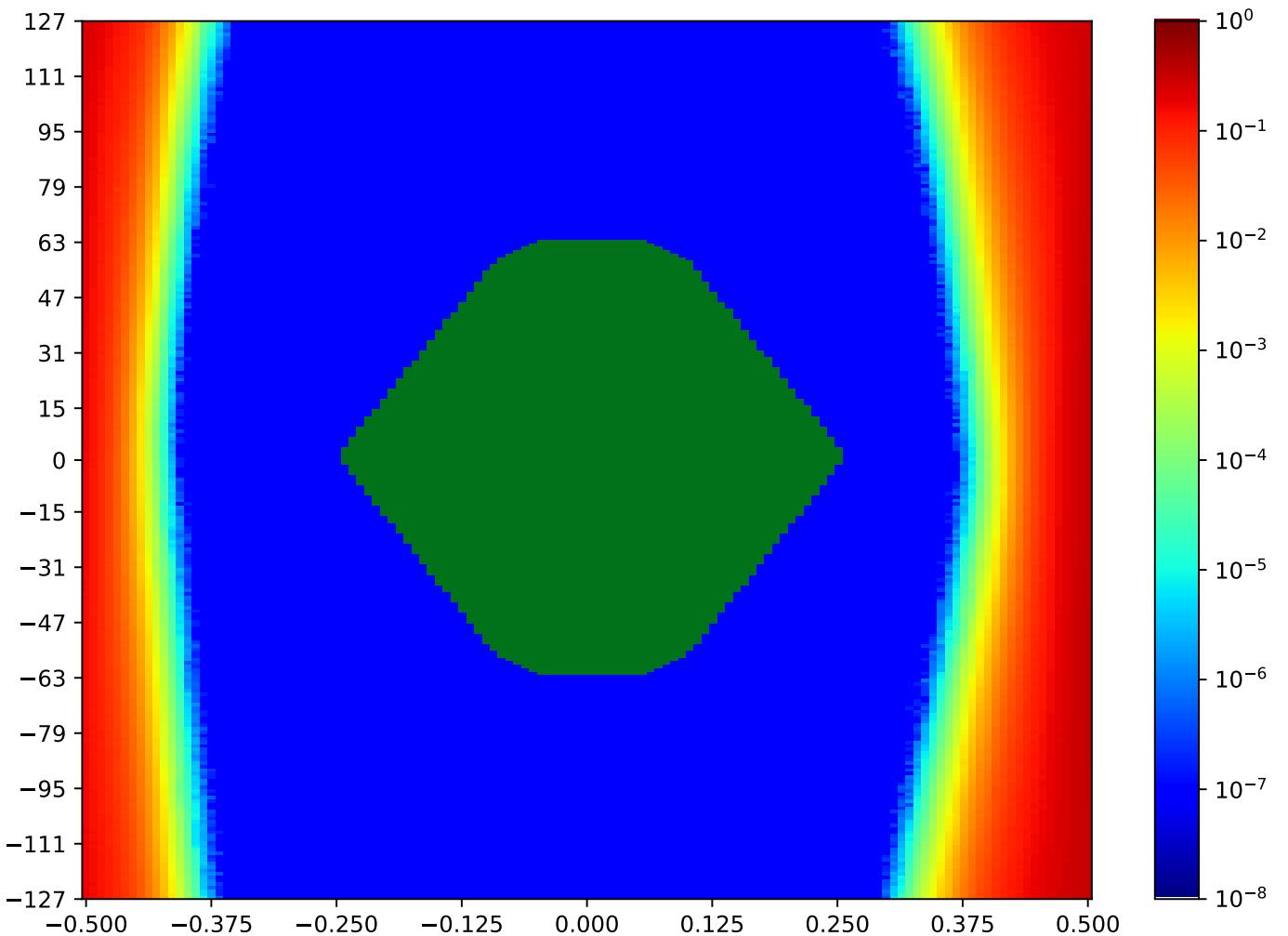


Figure 4.47: MSP_C_FPGA-TX4-06-RX7-06-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.8 MSP_C_FPGA-TX4-07-RX7-07-MSP_A_FPGA

Table 4.44: MSP_C_FPGA-TX4-07-RX7-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:30:50		2018-Sep-26 17:32:05	
Reset RX	OA	HO		VO	VO (%)
true	24507	102		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

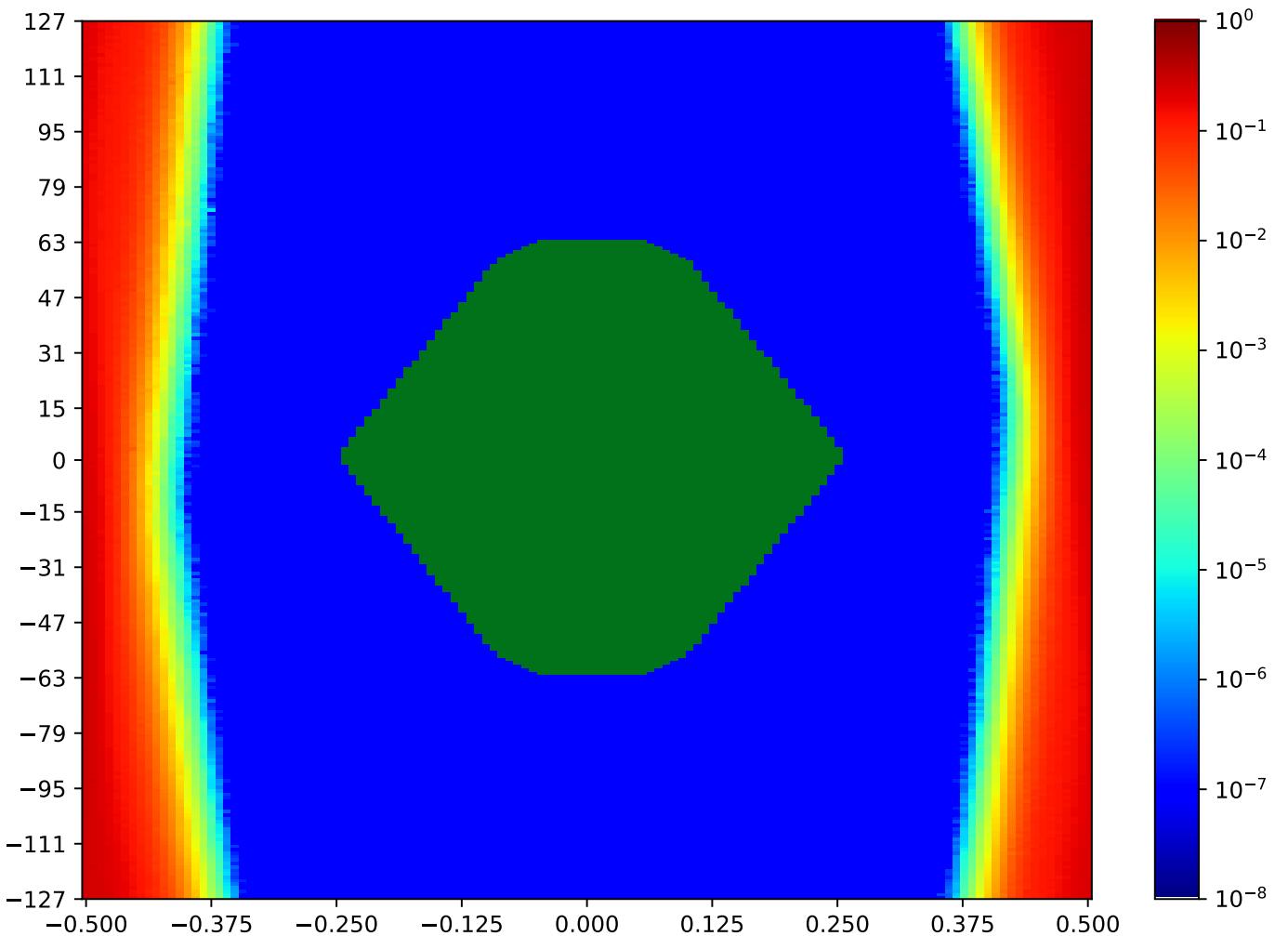


Figure 4.48: MSP_C_FPGA-TX4-07-RX7-07-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.9 MSP_C_FPGA-TX4-08-RX7-08-MSP_A_FPGA

Table 4.45: MSP_C_FPGA-TX4-08-RX7-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:38:20		2018-Sep-26 17:39:35	
Reset RX	OA	HO		VO	VO (%)
true	24391	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

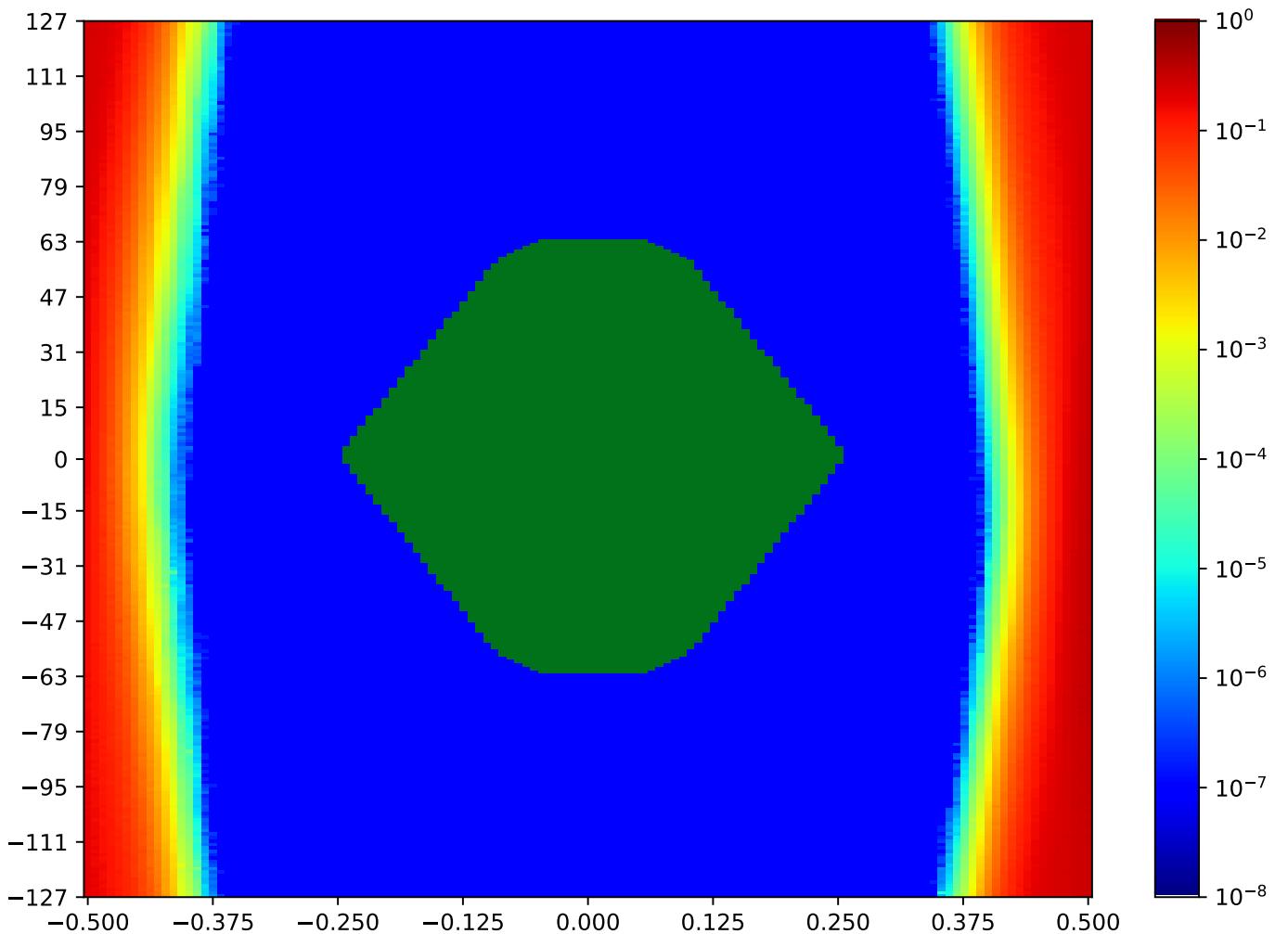


Figure 4.49: MSP_C_FPGA-TX4-08-RX7-08-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.10 MSP_C_FPGA-TX4-09-RX7-09-MSP_A_FPGA

Table 4.46: MSP_C_FPGA-TX4-09-RX7-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:32:05		2018-Sep-26 17:33:21	
Reset RX	OA	HO		VO	VO (%)
true	23734	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

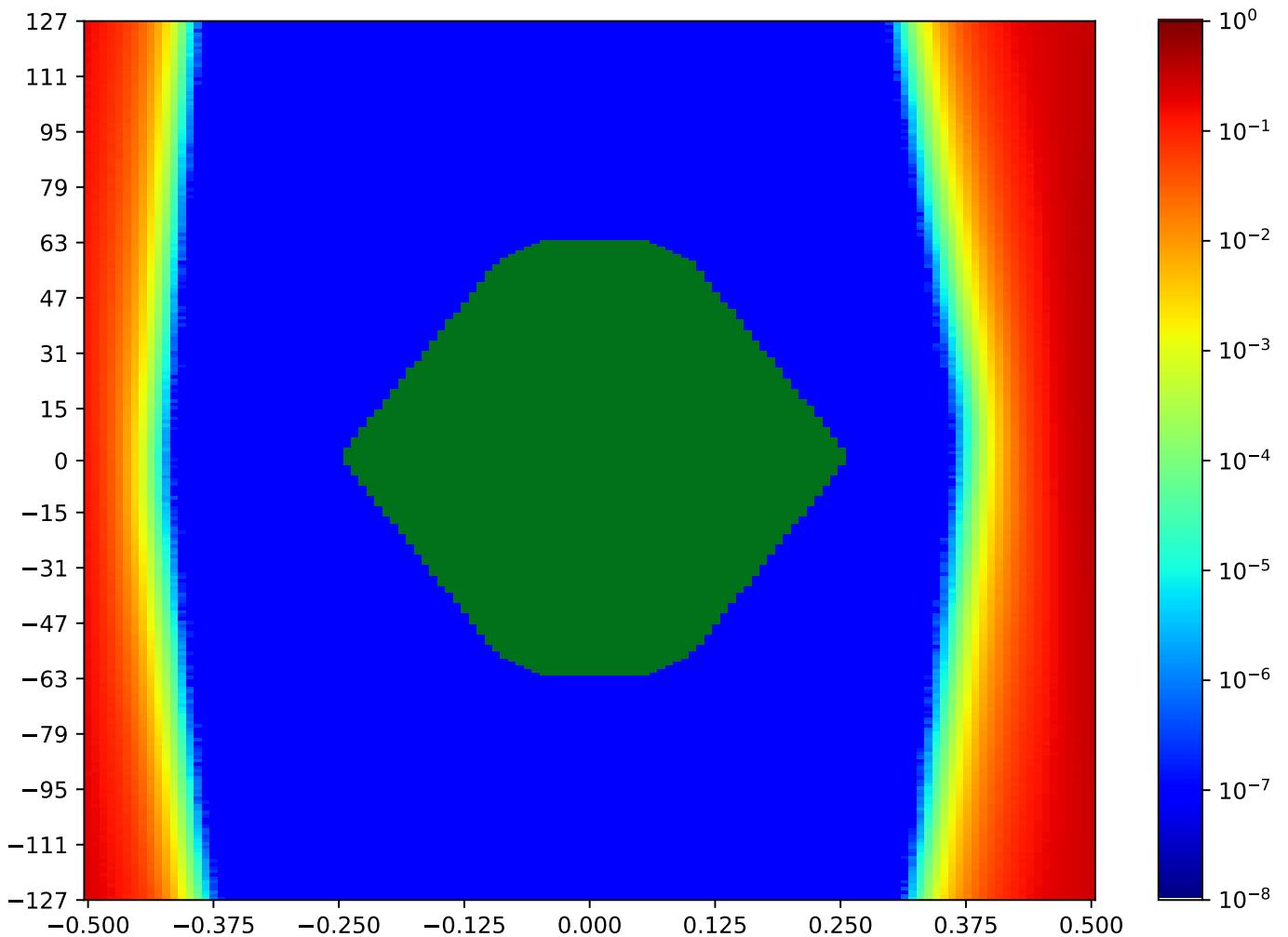


Figure 4.50: MSP_C_FPGA-TX4-09-RX7-09-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.11 MSP_C_FPGA-TX4-10-RX7-10-MSP_A_FPGA

Table 4.47: MSP_C_FPGA-TX4-10-RX7-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:35:51		2018-Sep-26 17:37:06	
Reset RX	OA	HO		VO	VO (%)
true	23627	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

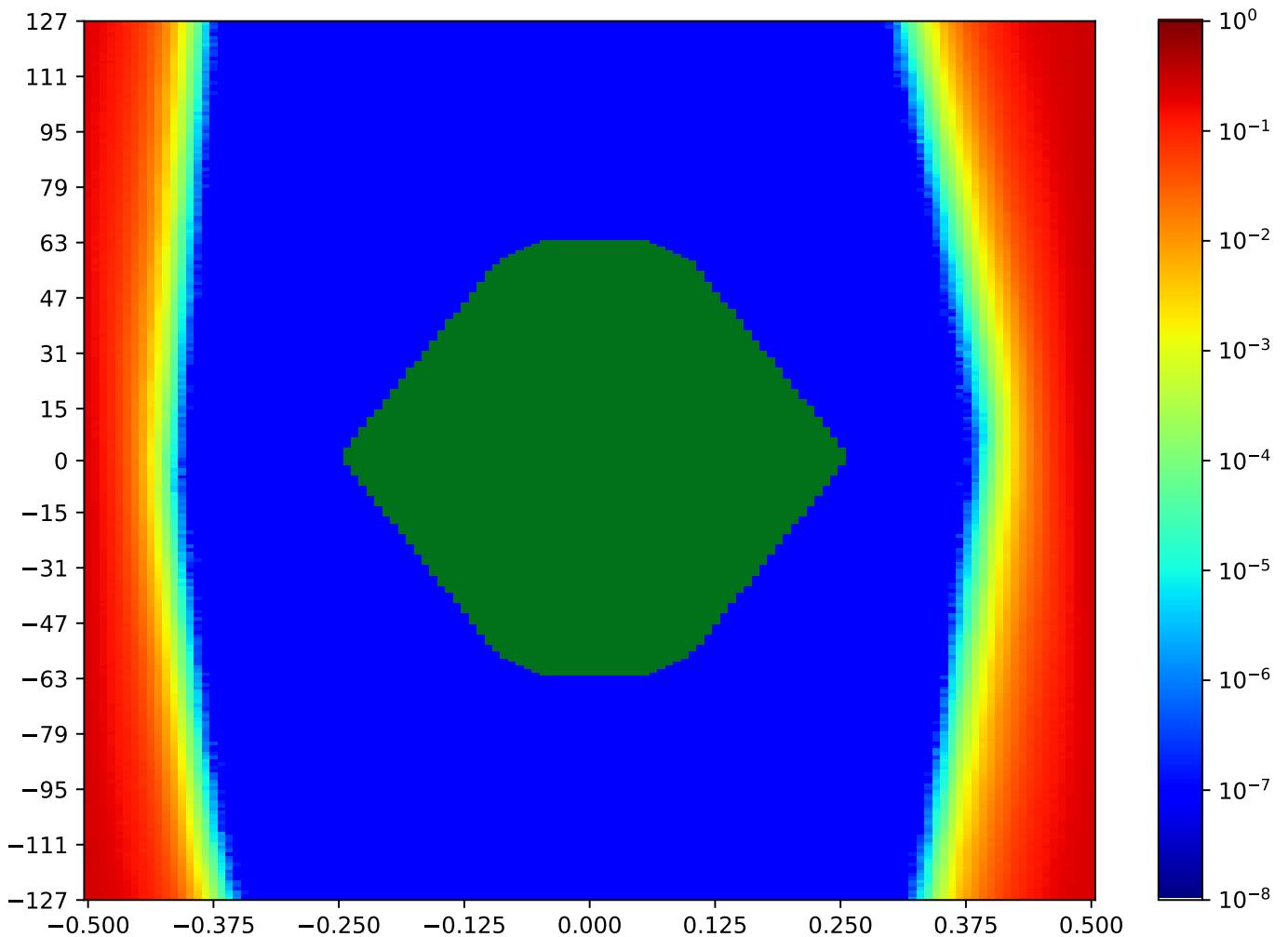


Figure 4.51: MSP_C_FPGA-TX4-10-RX7-10-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.4.12 MSP_C_FPGA-TX4-11-RX7-11-MSP_A_FPGA

Table 4.48: MSP_C_FPGA-TX4-11-RX7-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:34:36		2018-Sep-26 17:35:51	
Reset RX	OA	HO		VO	VO (%)
true	24622	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

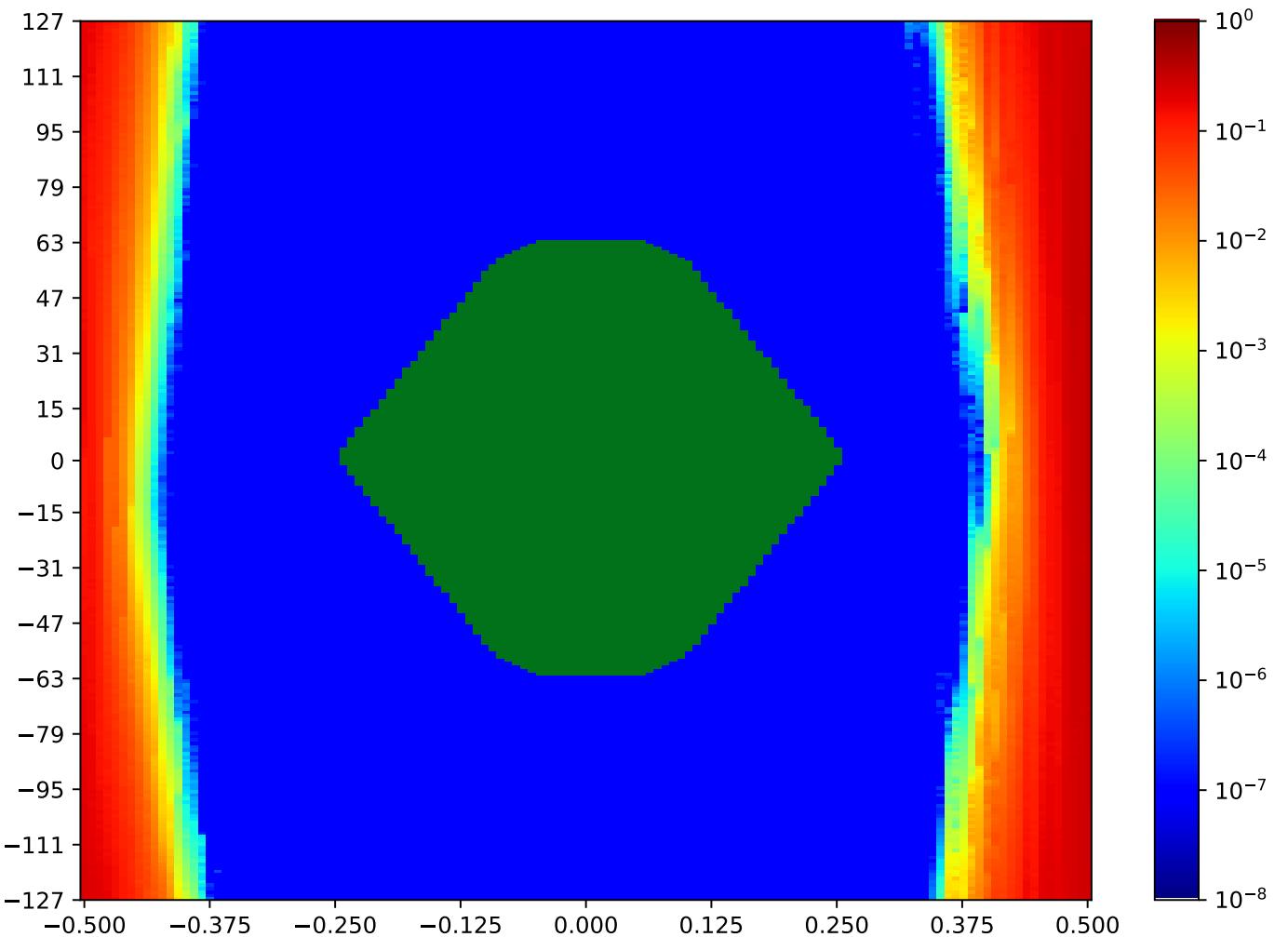


Figure 4.52: MSP_C_FPGA-TX4-11-RX7-11-MSP_A_FPGA

Call back to summary Figure 4.40. Sibling eye diagrams: V2-12.8.

4.5 Partial TRP TX5 MSP_A RX5 Minipod Loopback

A cross-reference to Figure 4.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.
Next summary Figure 4.62.

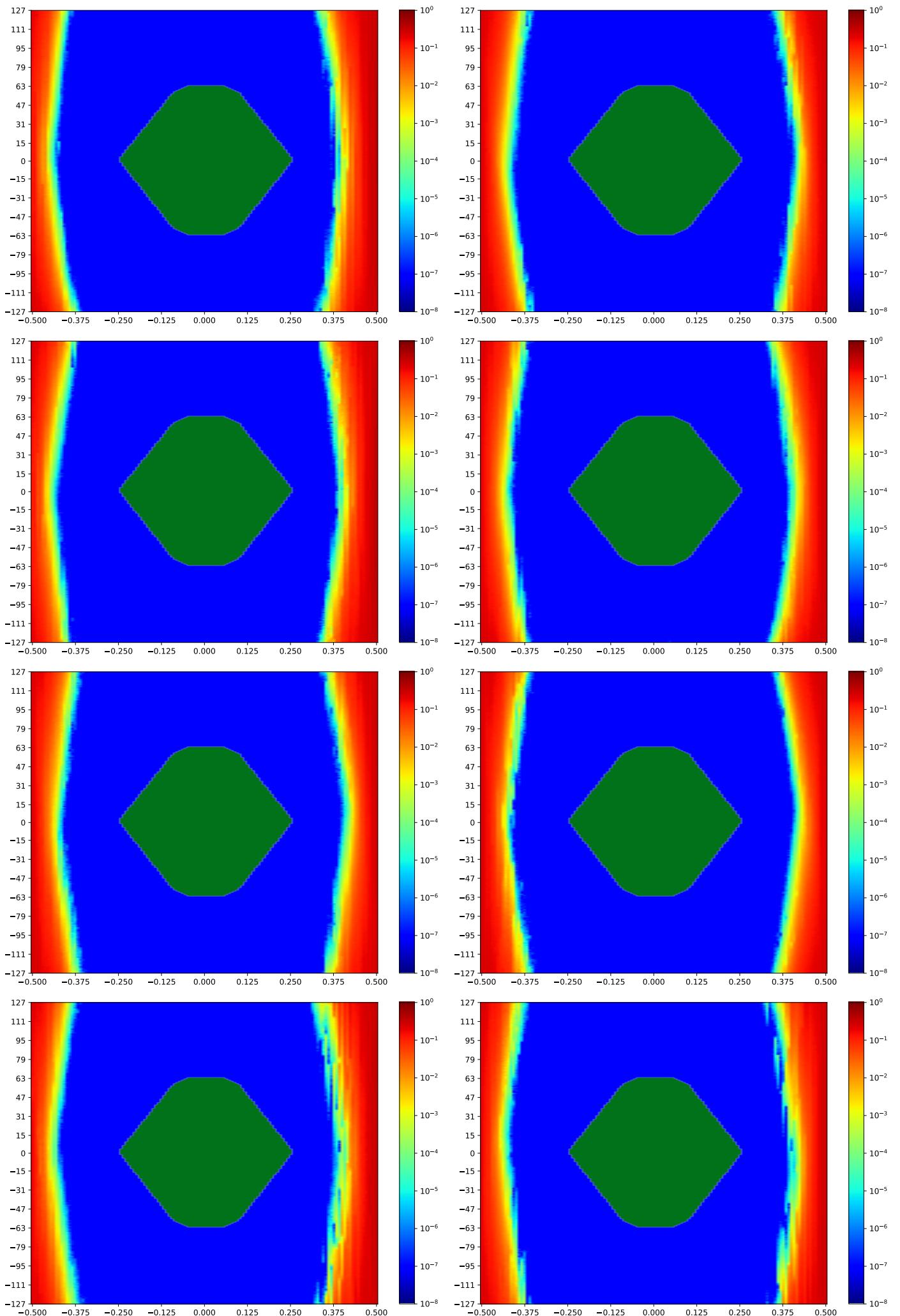


Figure 4.53: Partial TRP TX5 MSP_A RX5 Minipod Loopback

4.5.1 TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

Table 4.49: TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:44:34		2018-Sep-26 17:45:48	
Reset RX	OA	HO		VO	VO (%)
true	24485	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

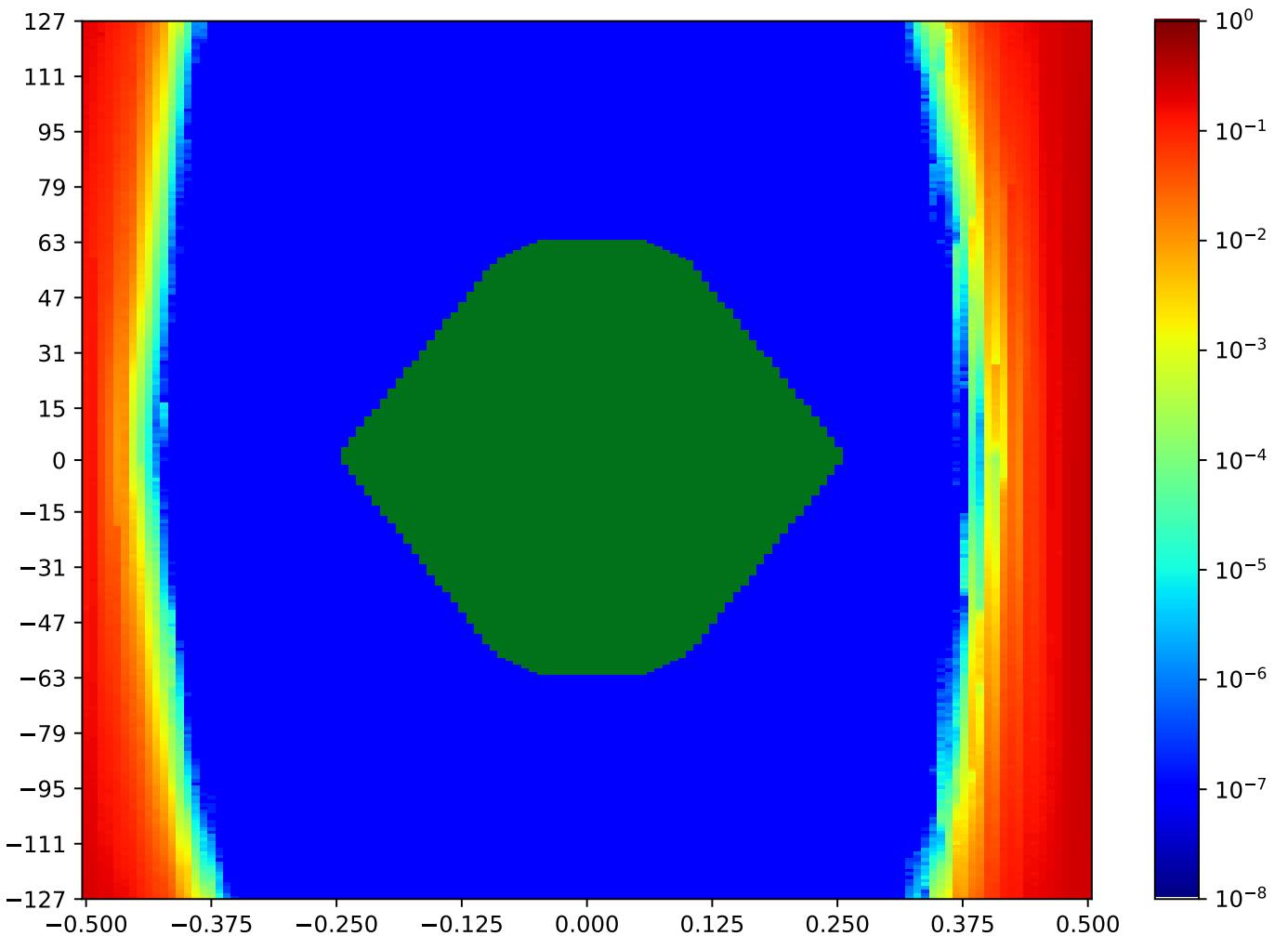


Figure 4.54: TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.5.2 TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

Table 4.50: TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:42:05		2018-Sep-26 17:43:20	
Reset RX	OA	HO		VO	VO (%)
true	24335	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

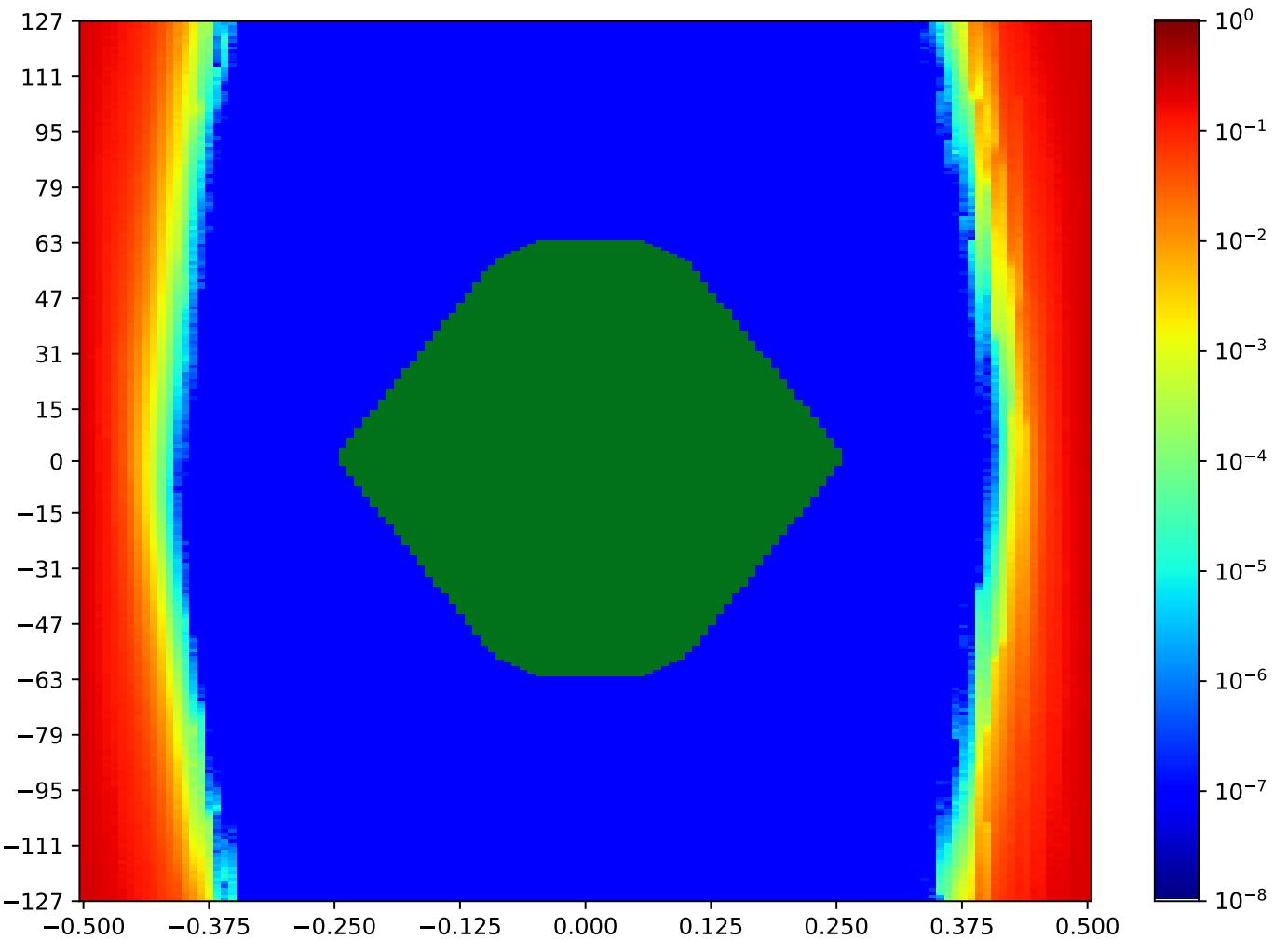


Figure 4.55: TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.5.3 TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

Table 4.51: TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:47:03		2018-Sep-26 17:48:18	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24509	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

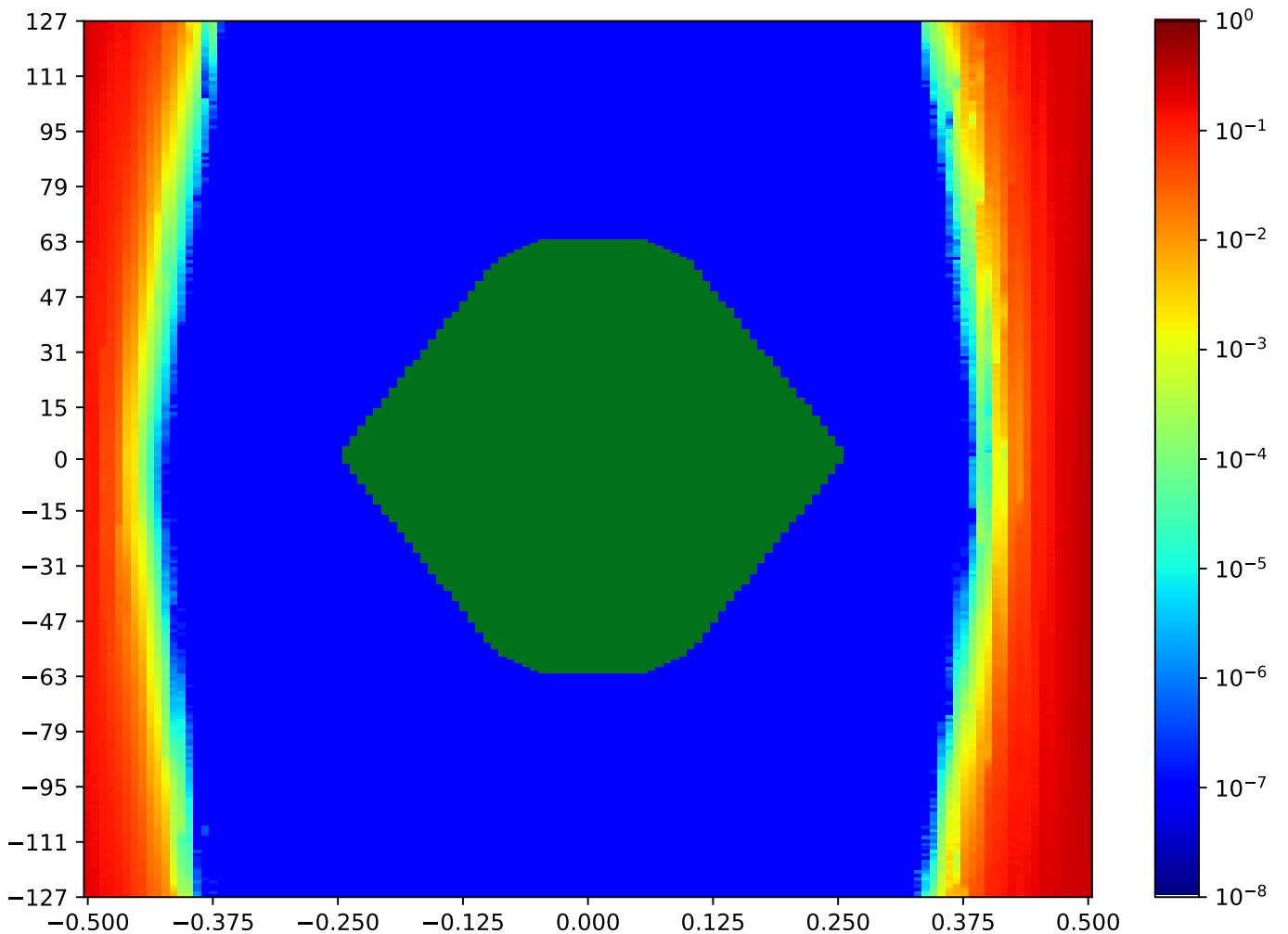


Figure 4.56: TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.5.4 TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

Table 4.52: TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:43:20		2018-Sep-26 17:44:34	
Reset RX	OA	HO		VO	VO (%)
true	24171	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

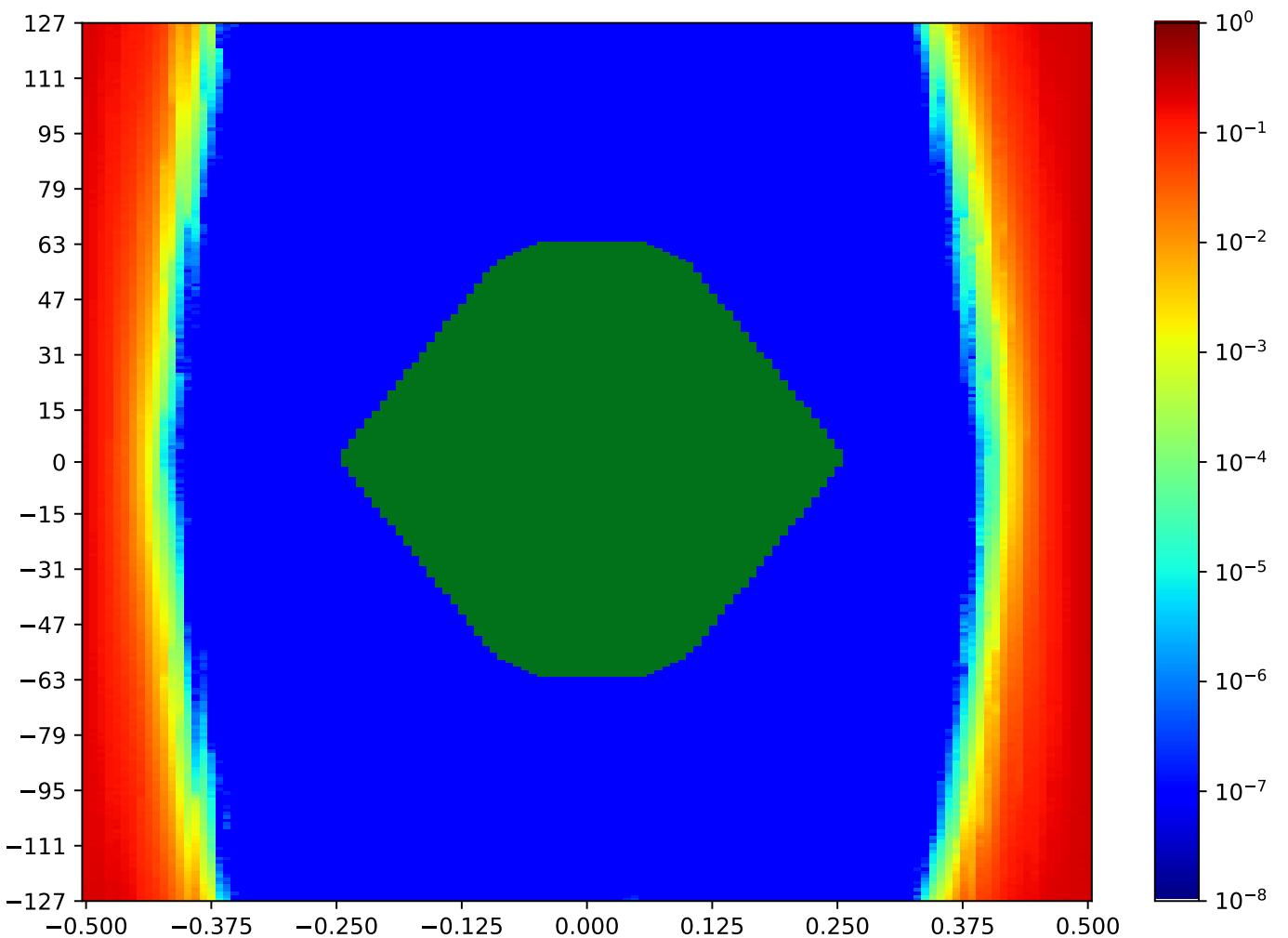


Figure 4.57: TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.5.5 TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

Table 4.53: TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:49:32		2018-Sep-26 17:50:47	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24322	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

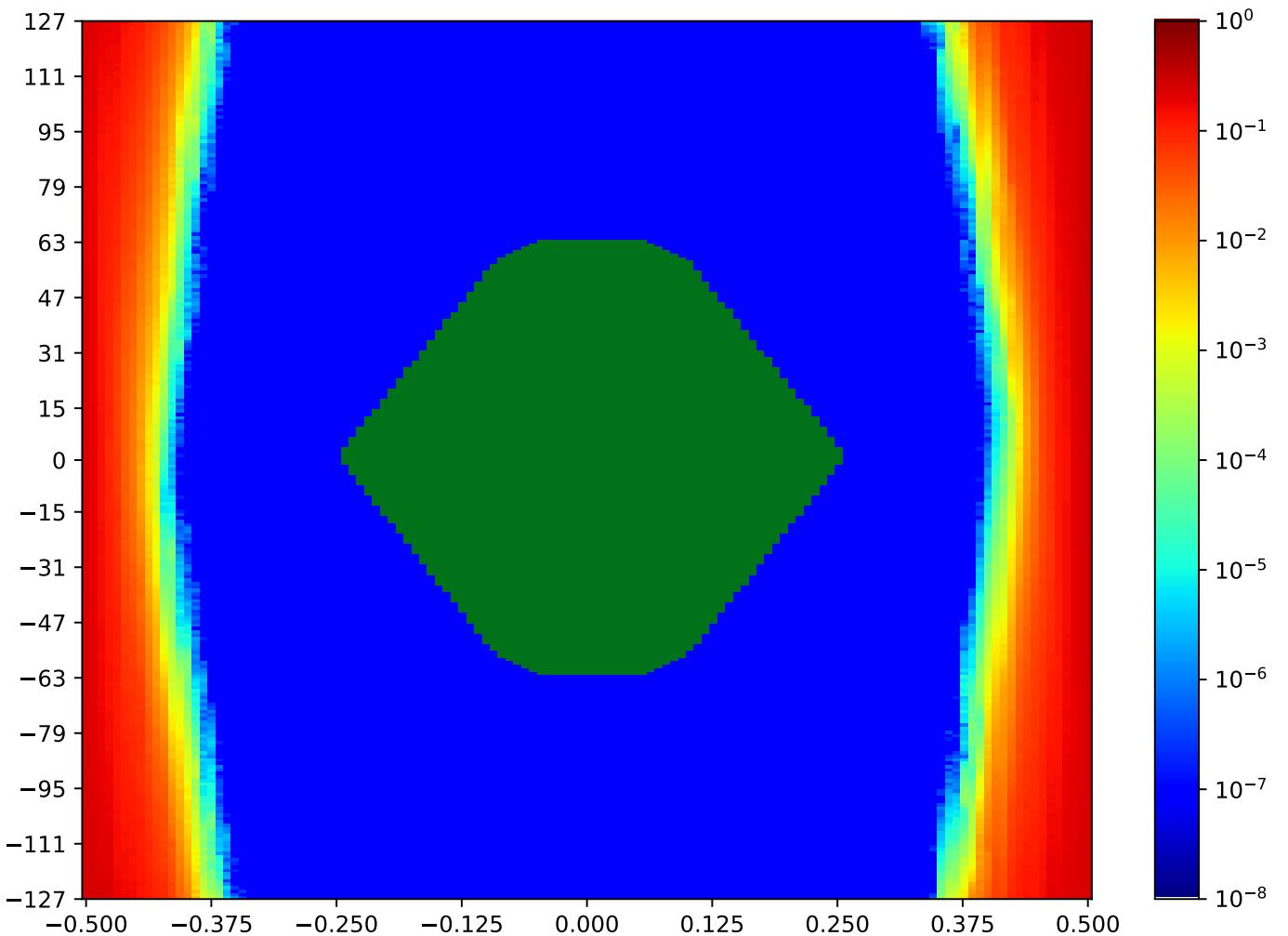


Figure 4.58: TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.5.6 TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

Table 4.54: TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:40:50		2018-Sep-26 17:42:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24489	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

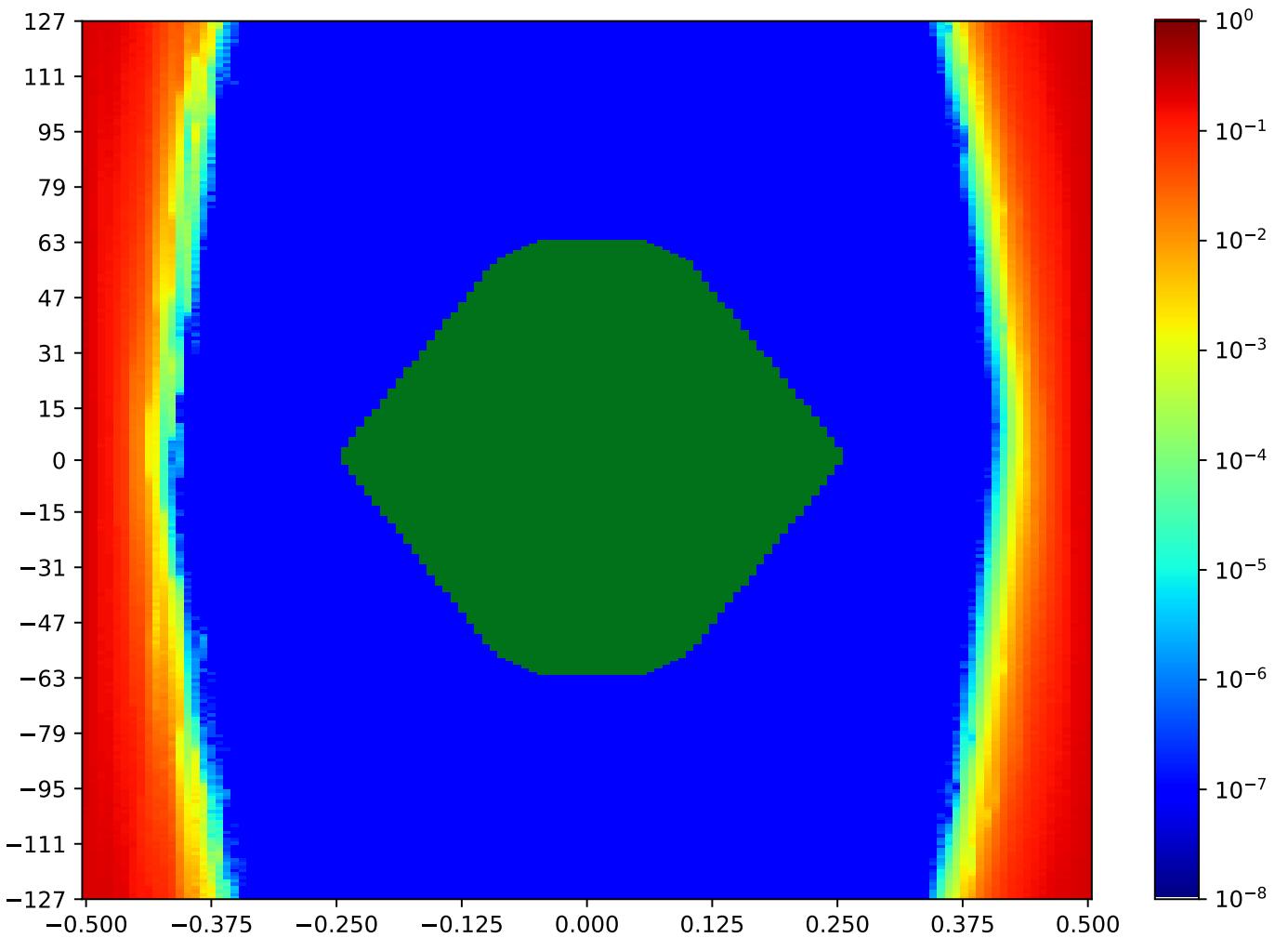


Figure 4.59: TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.5.7 TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

Table 4.55: TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:45:49		2018-Sep-26 17:47:03	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24001	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

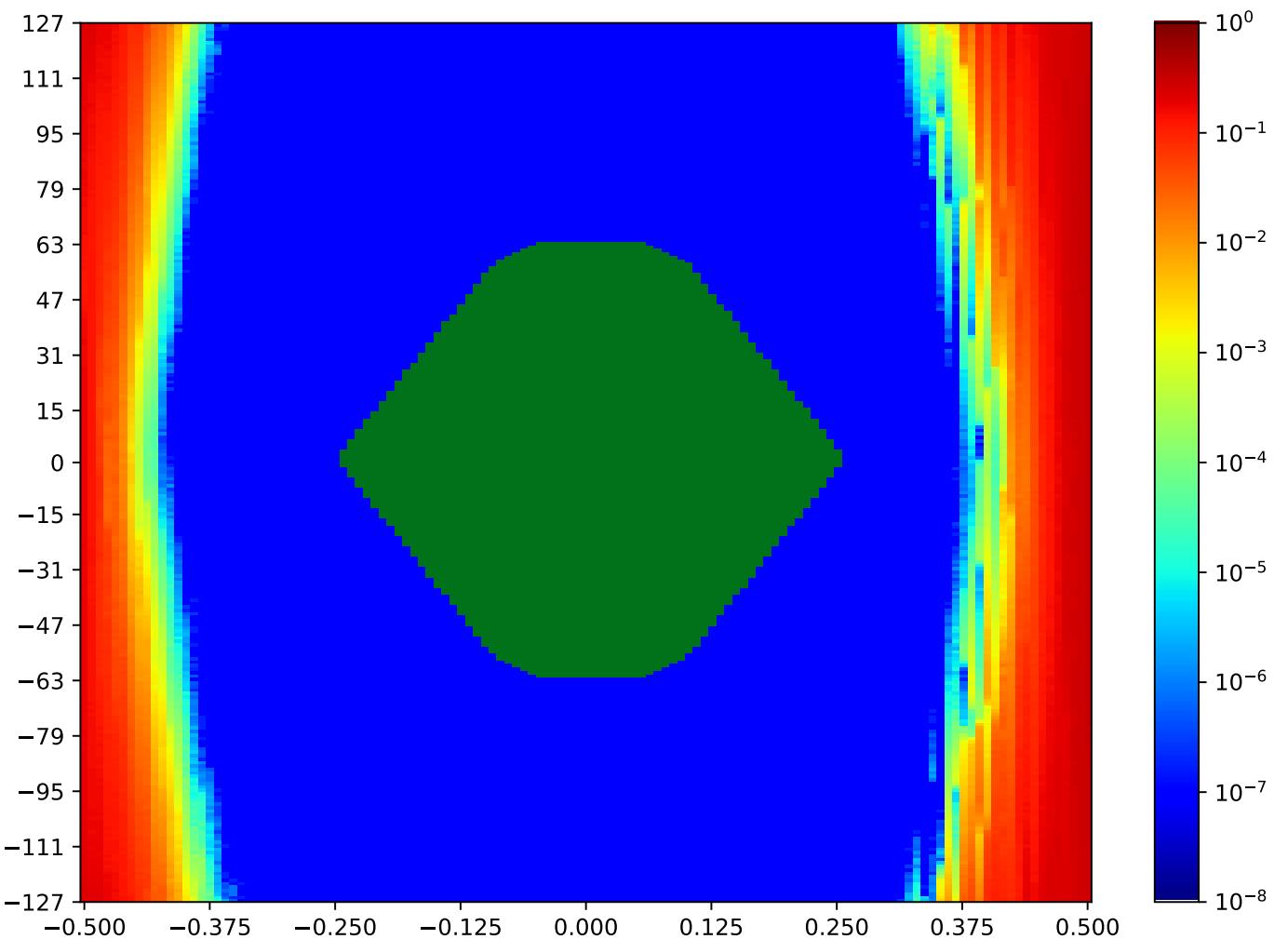


Figure 4.60: TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.5.8 TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

Table 4.56: TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 17:48:18		2018-Sep-26 17:49:32	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24492	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

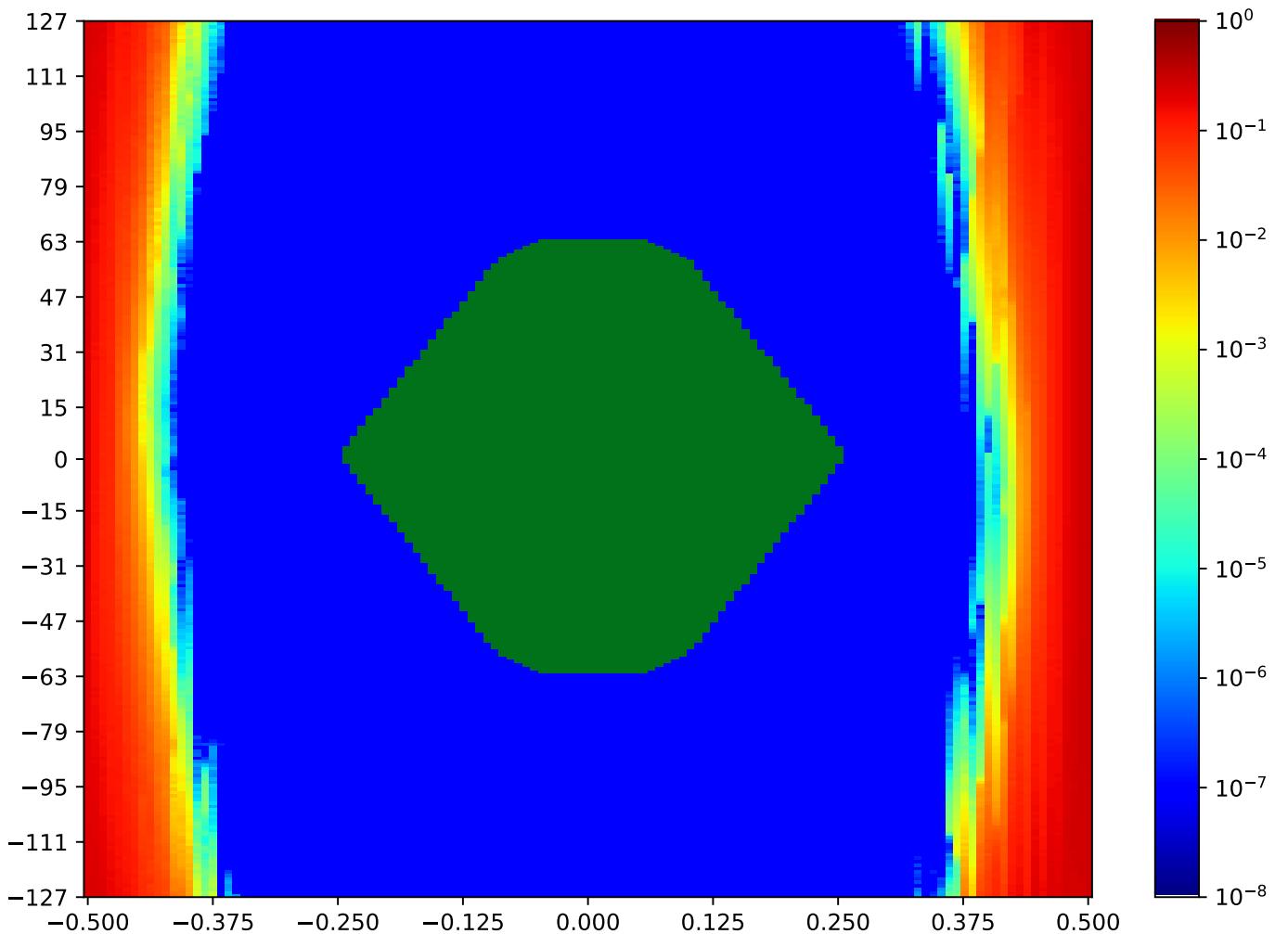


Figure 4.61: TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

Call back to summary Figure 4.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.6 TRP J1 QSFP Loopback

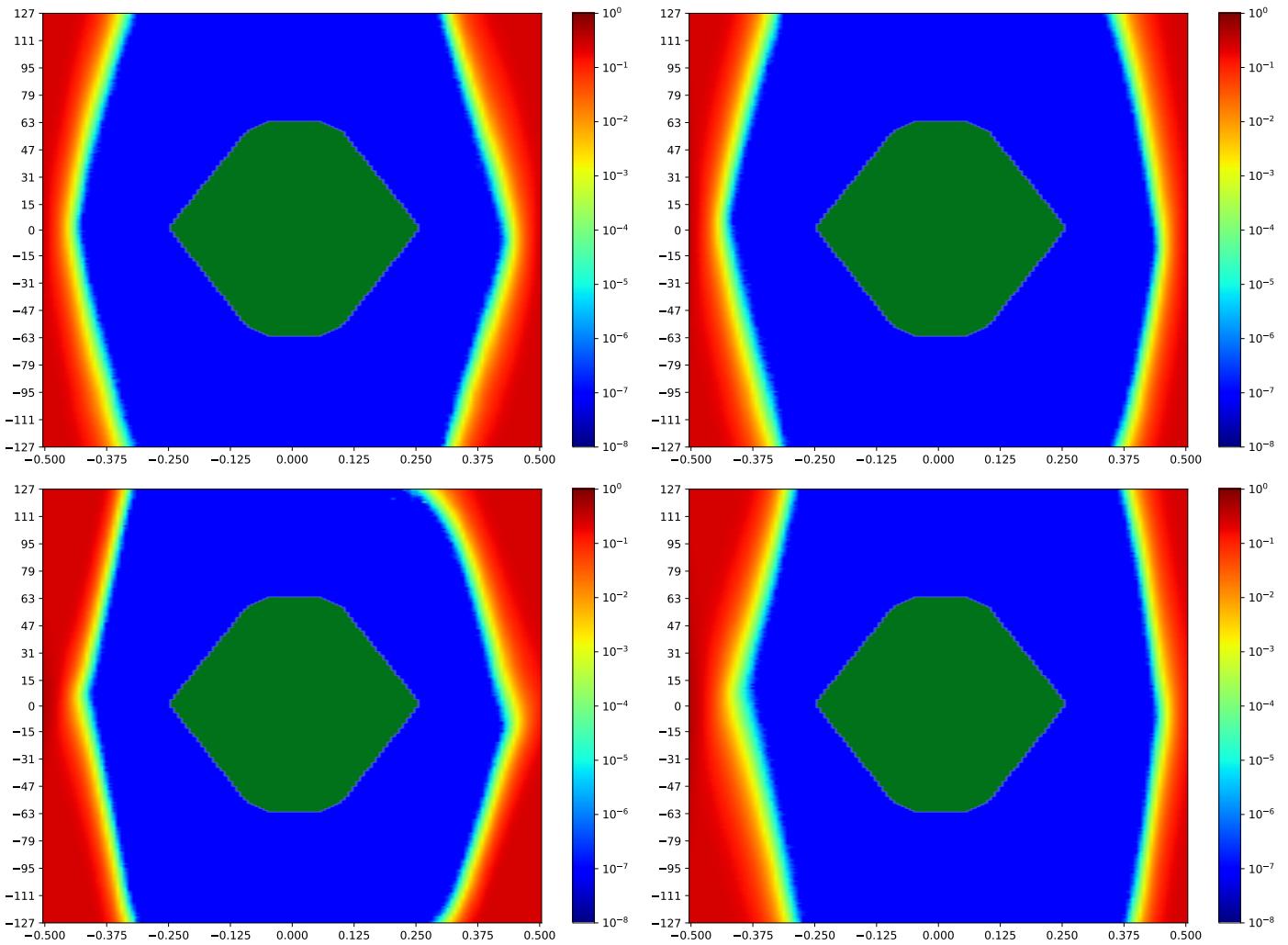


Figure 4.62: TRP J1 QSFP Loopback

A cross-reference to Figure 4.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.
Next summary Figure 4.67.

4.6.1 TRP_FPGA-J1-00–J1-00-TRP_FPGA

Table 4.57: TRP_FPGA-J1-00–J1-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:50:47		2018-Sep-26 17:51:59	
Reset RX	OA	HO		HO (%)	
true	23744	108		83.72%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

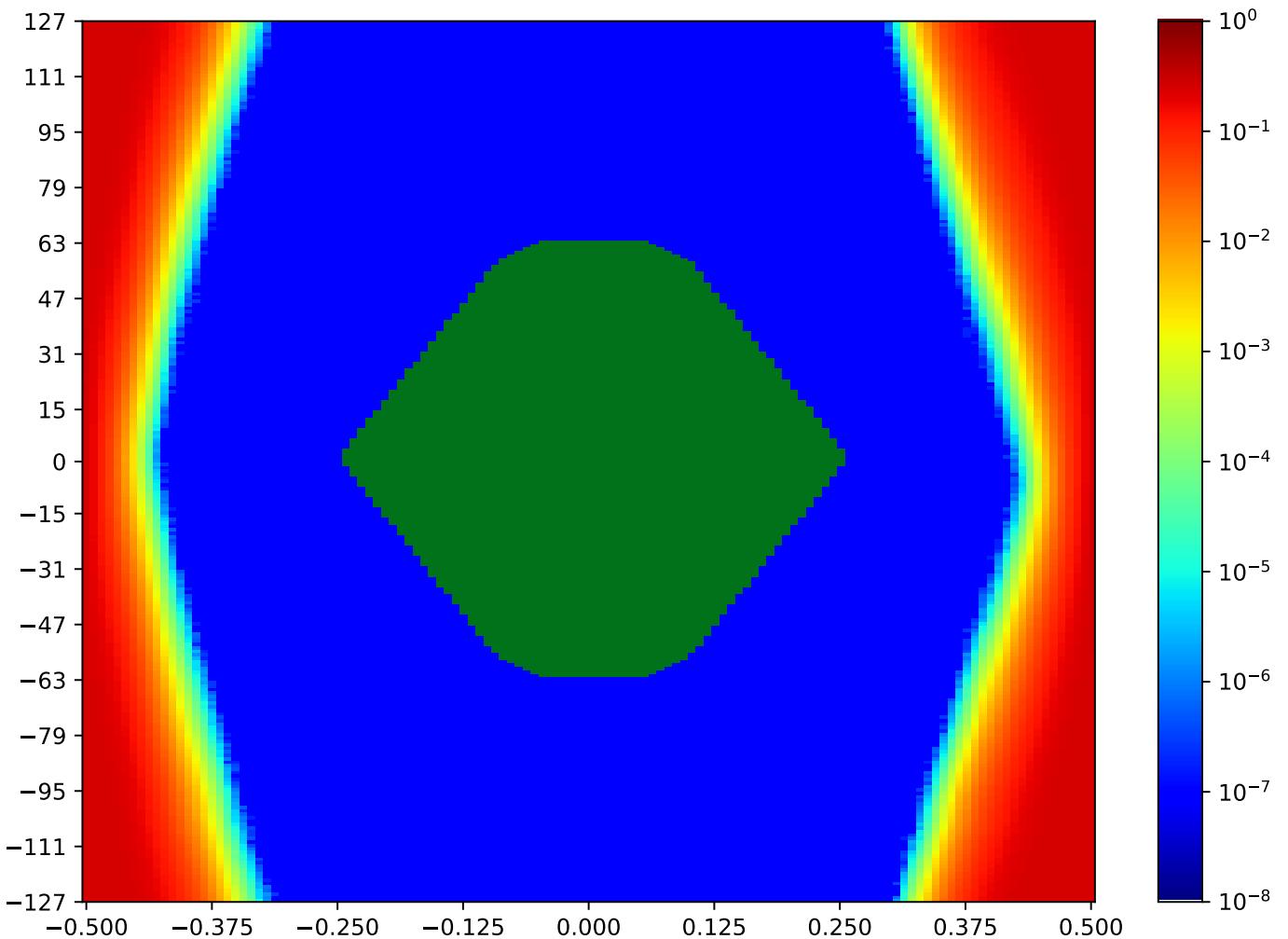


Figure 4.63: TRP_FPGA-J1-00–J1-00-TRP_FPGA

Call back to summary Figure 4.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.6.2 TRP_FPGA-J1-01–J1-01-TRP_FPGA

Table 4.58: TRP_FPGA-J1-01–J1-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:51:59		2018-Sep-26 17:53:12	
Reset RX	OA	HO		HO (%)	
true	24532	107		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

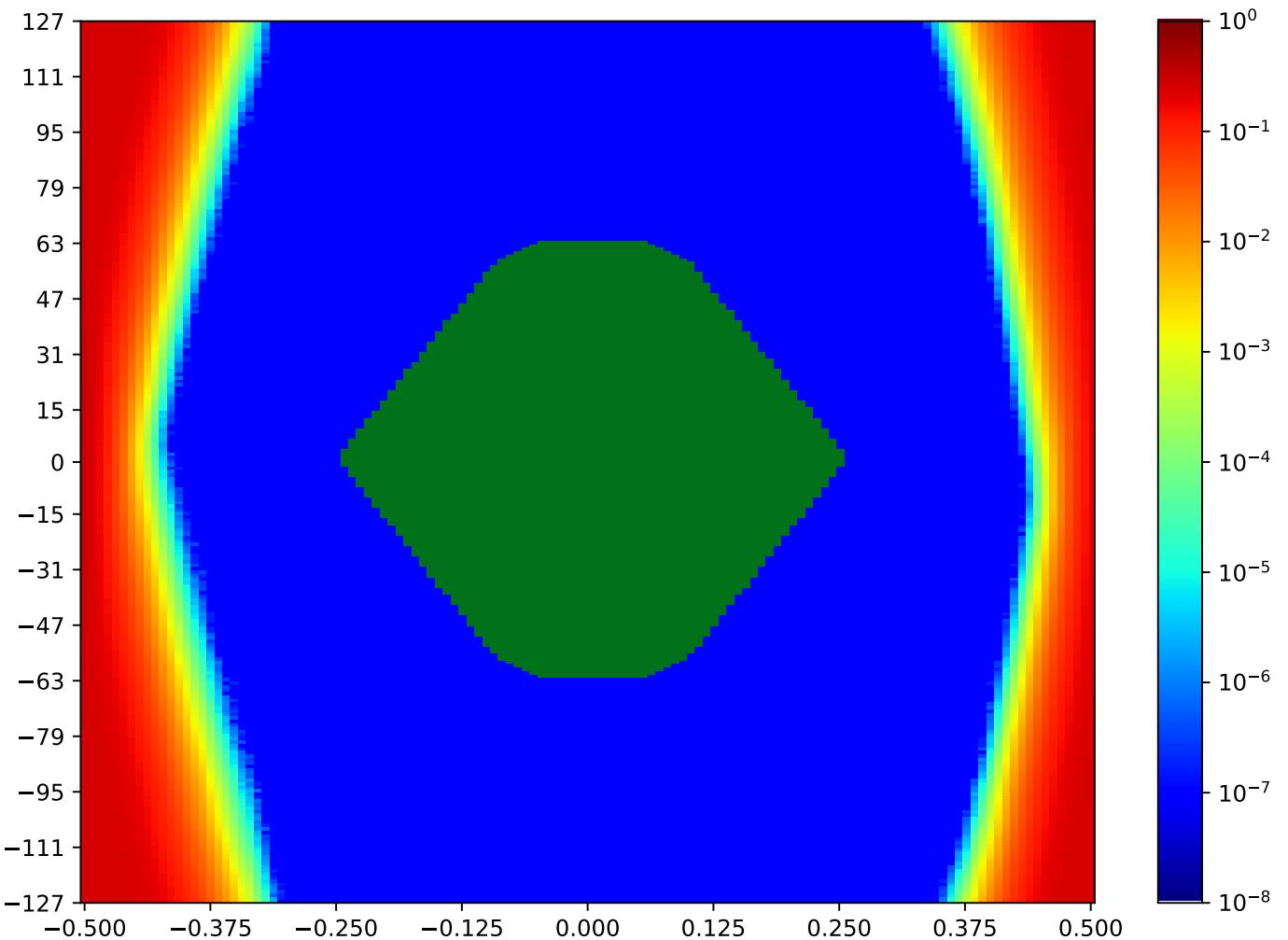


Figure 4.64: TRP_FPGA-J1-01–J1-01-TRP_FPGA

Call back to summary Figure 4.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.6.3 TRP_FPGA-J1-02–J1-02-TRP_FPGA

Table 4.59: TRP_FPGA-J1-02–J1-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:53:12		2018-Sep-26 17:54:22	
Reset RX	OA	HO		VO	VO (%)
true	23141	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

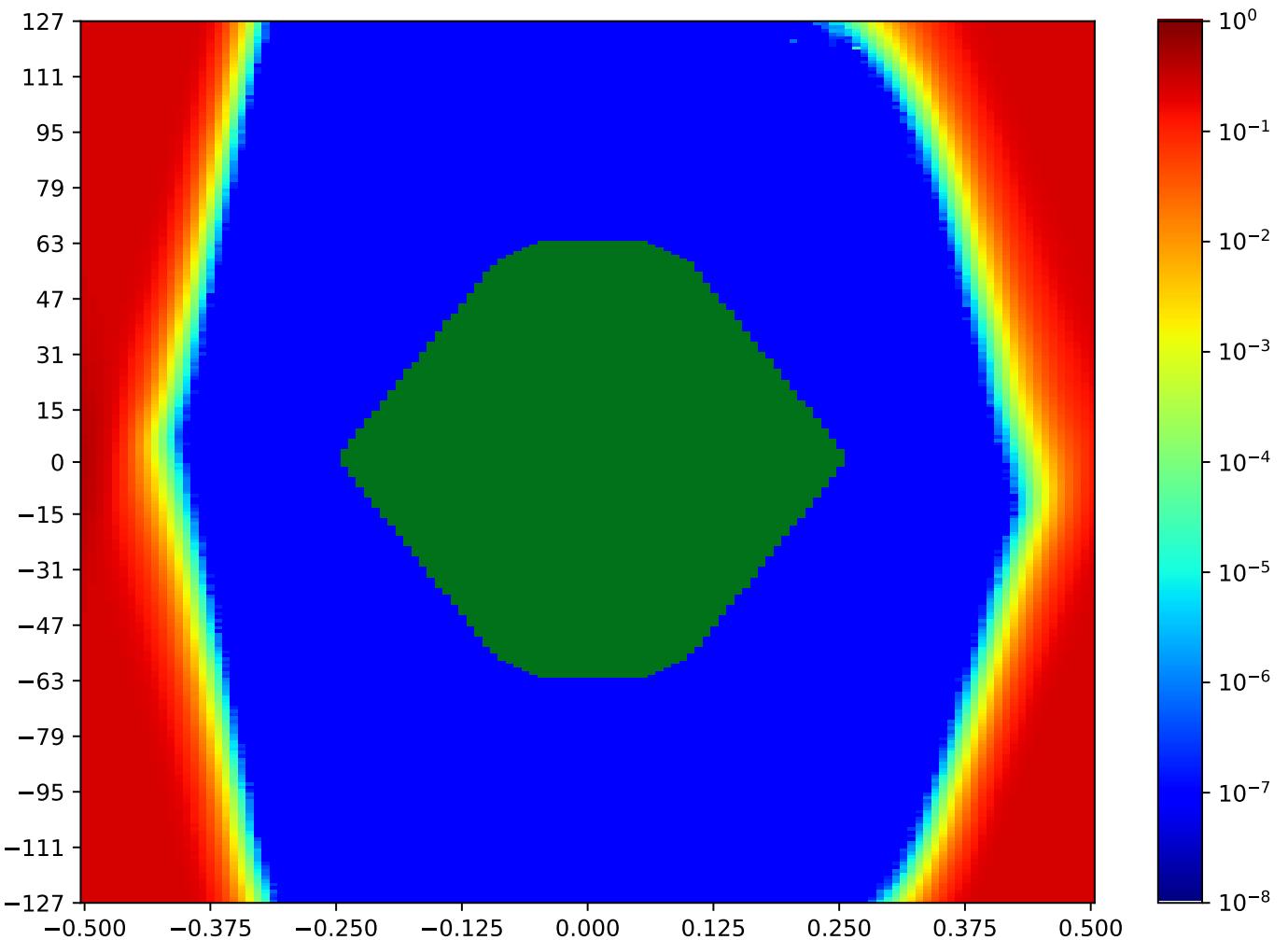


Figure 4.65: TRP_FPGA-J1-02–J1-02-TRP_FPGA

Call back to summary Figure 4.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.6.4 TRP_FPGA-J1-03–J1-03-TRP_FPGA

Table 4.60: TRP_FPGA-J1-03–J1-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:54:22		2018-Sep-26 17:55:33	
Reset RX	OA	HO		VO VO (%)	
true	23546	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

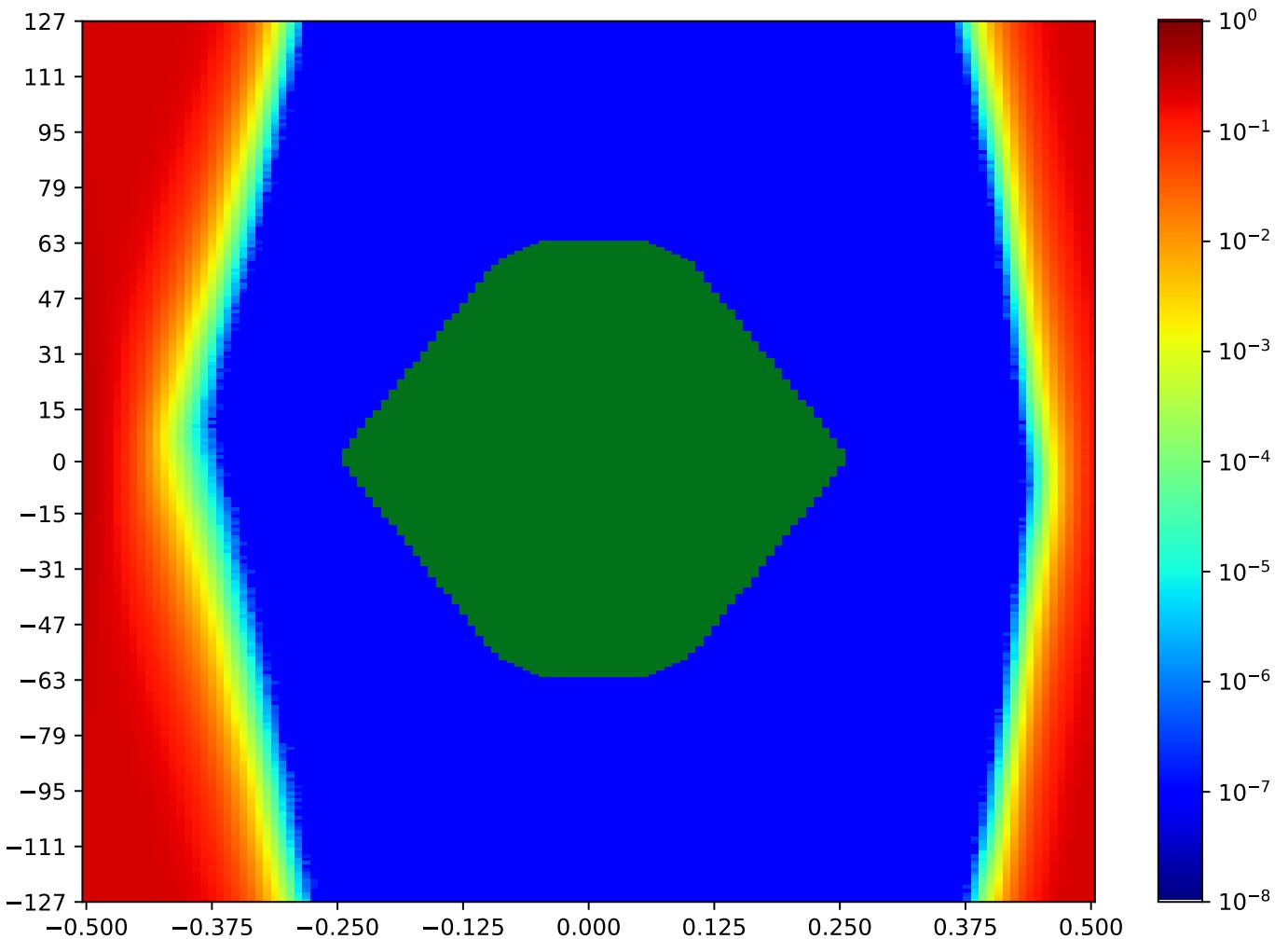


Figure 4.66: TRP_FPGA-J1-03–J1-03-TRP_FPGA

Call back to summary Figure 4.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.7 TRP J3 SFP Loopback

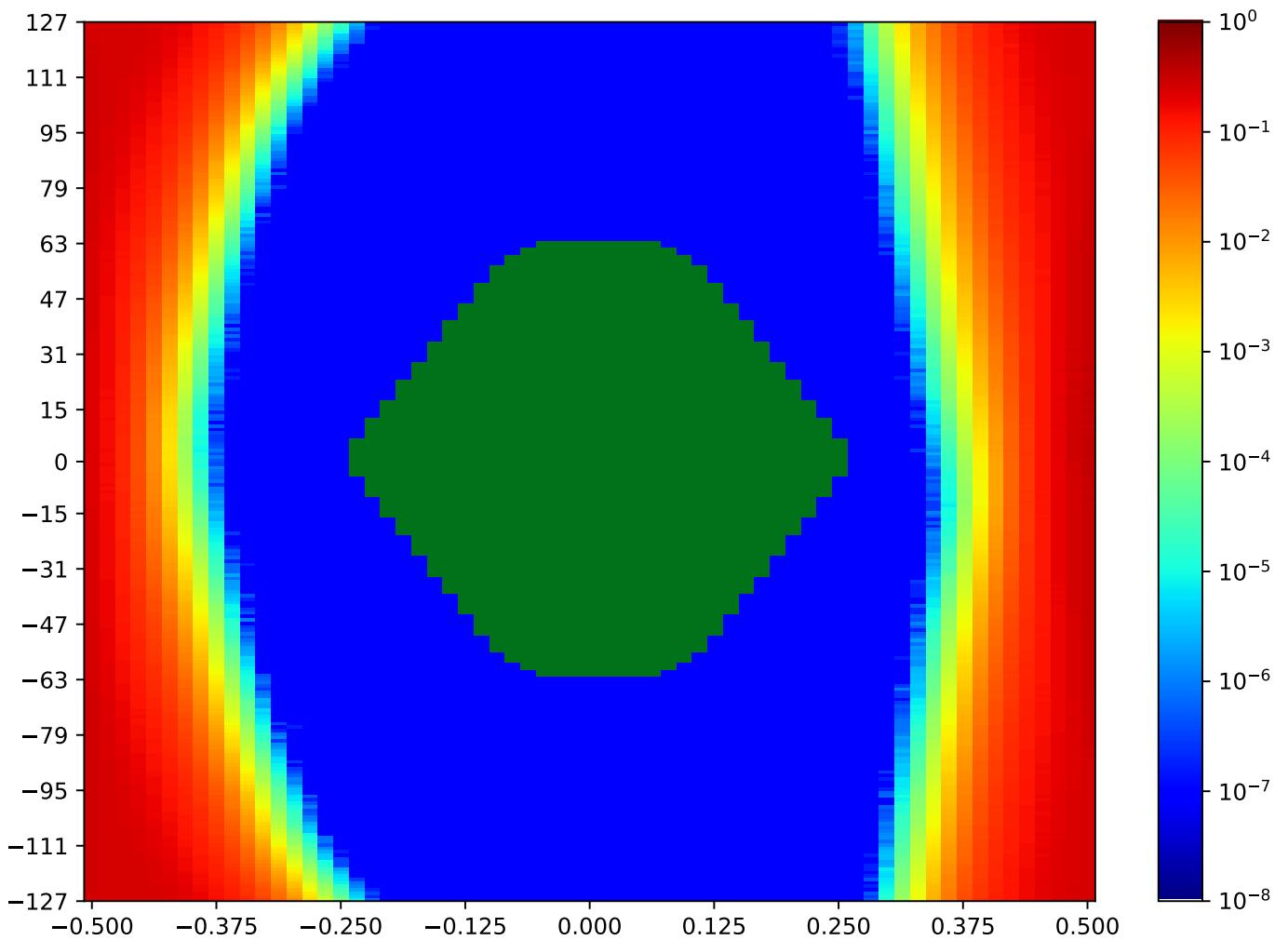


Figure 4.67: TRP J3 SFP Loopback

A cross-reference to Figure 4.67. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.
Next summary Figure 4.69.

4.7.1 TRP_FPGA-J3-00–J3-00-TRP_FPGA

Table 4.61: TRP_FPGA-J3-00–J3-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 17:55:33		2018-Sep-26 17:56:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9992	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

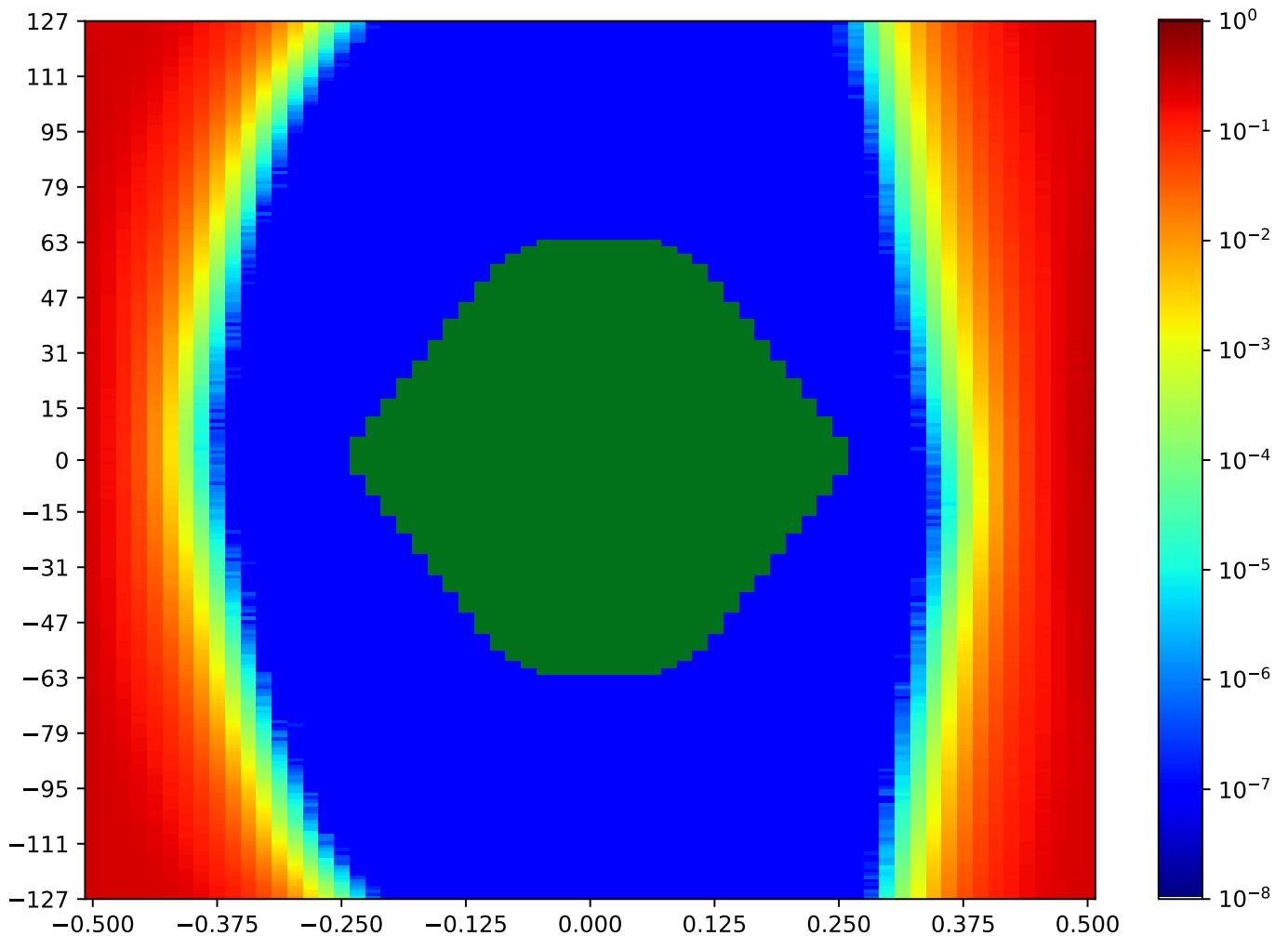


Figure 4.68: TRP_FPGA-J3-00–J3-00-TRP_FPGA

Call back to summary Figure 4.67. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8 MSP_A TRP On board links

A cross-reference to Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.
Next summary Figure 4.98.

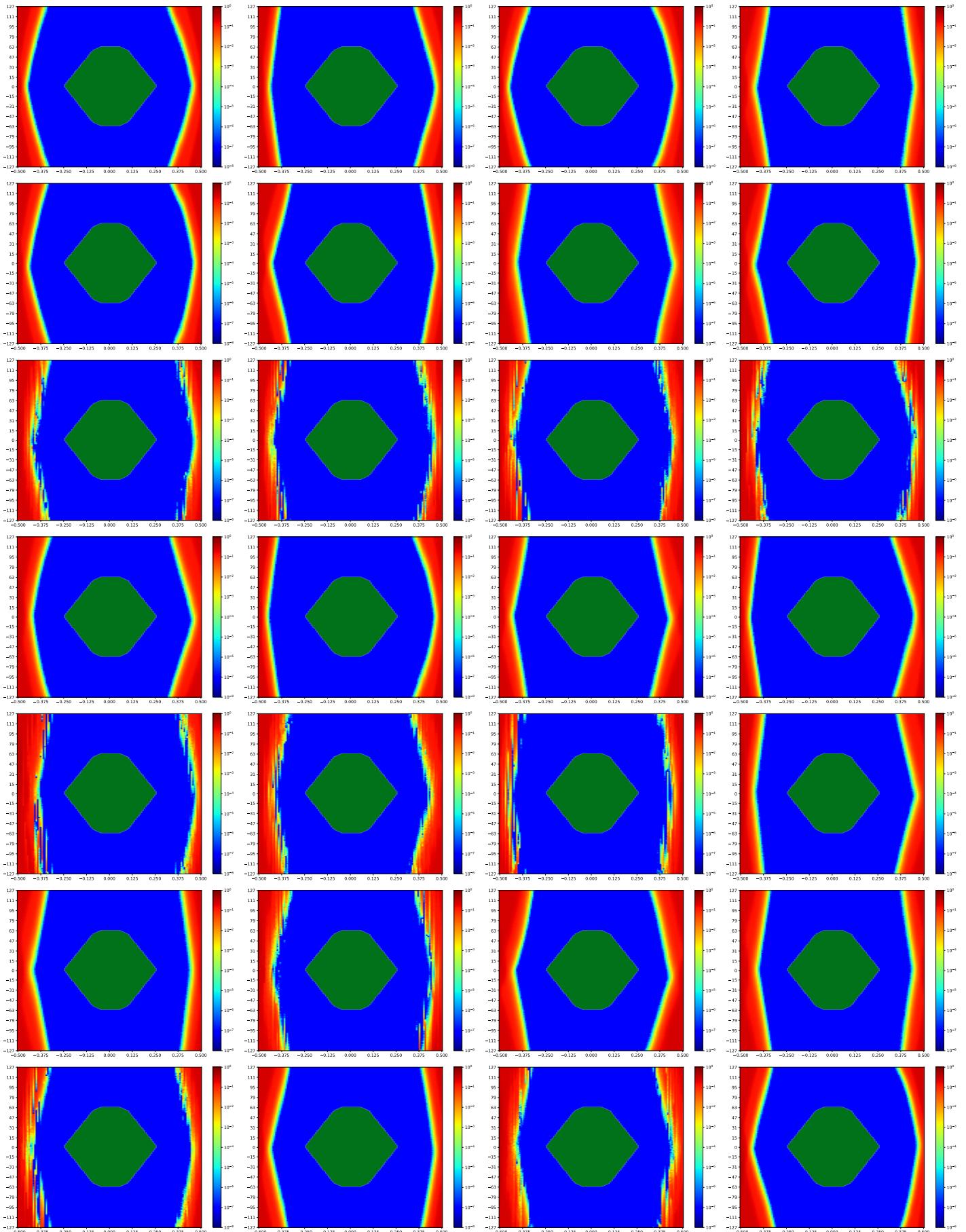


Figure 4.69: MSP_A TRP On board links

4.8.1 MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

Table 4.62: MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:56:10		2018-Sep-26 17:57:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24960	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

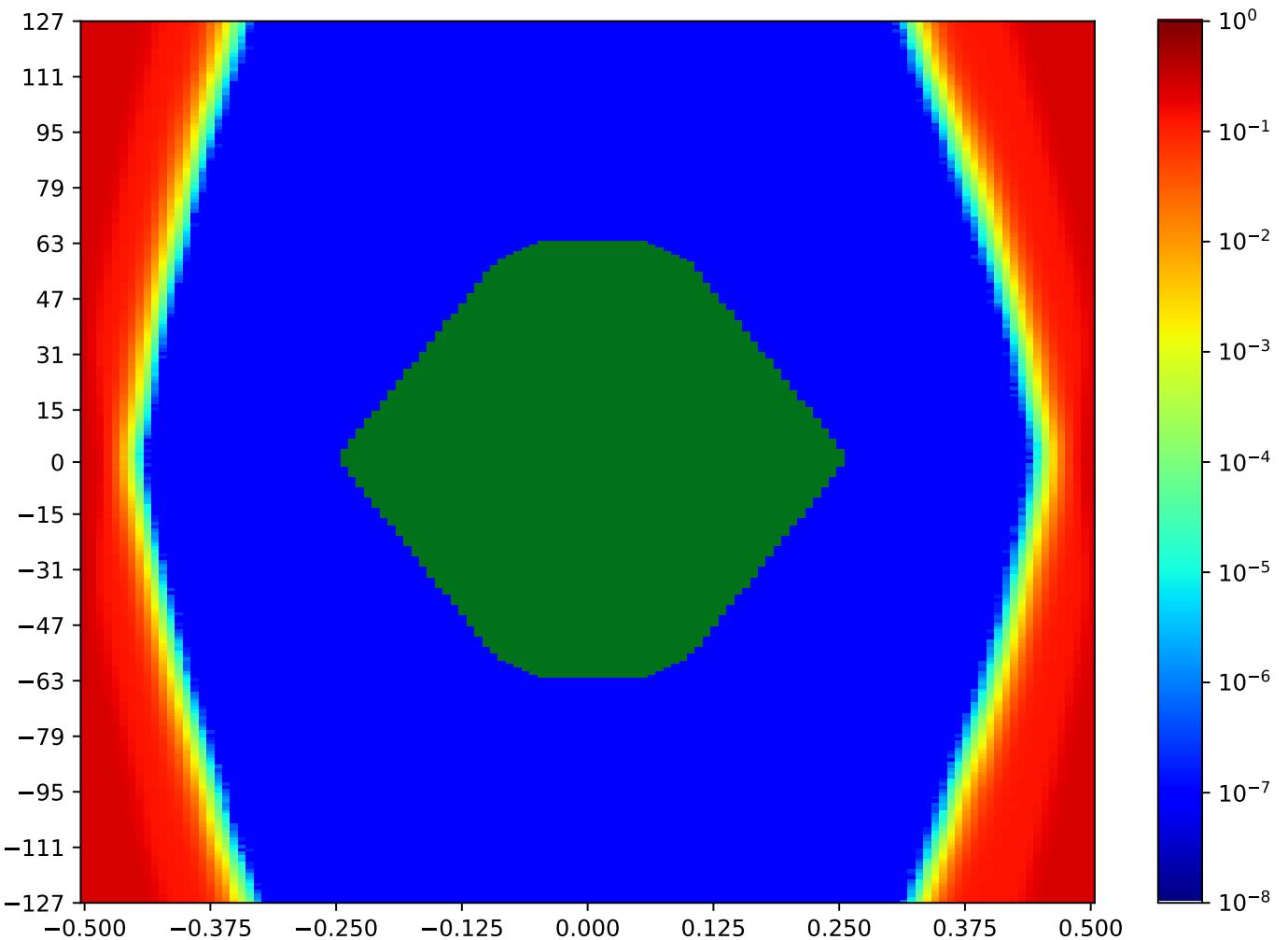


Figure 4.70: MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.2 MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

Table 4.63: MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:57:23		2018-Sep-26 17:58:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25874	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

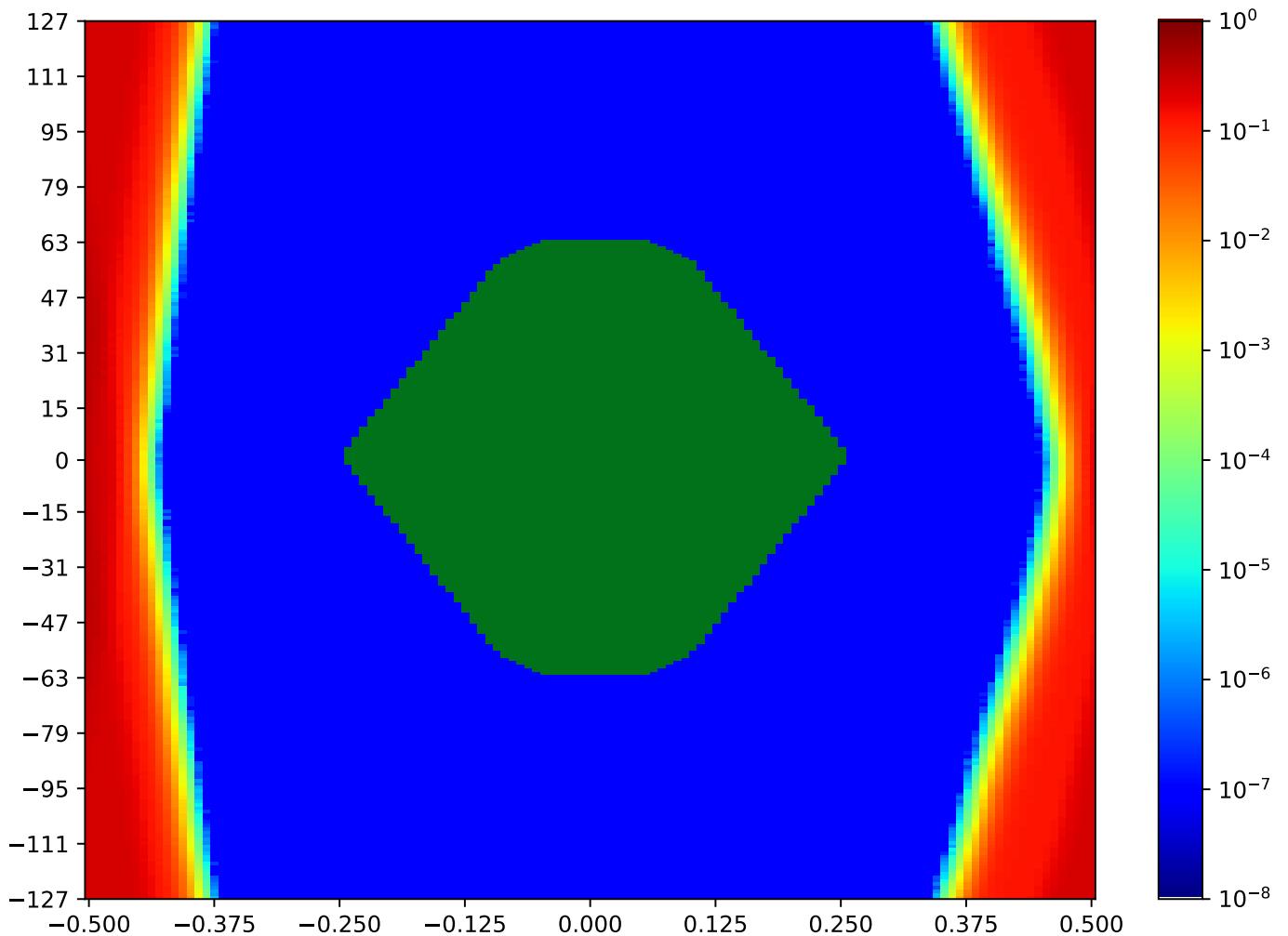


Figure 4.71: MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.3 MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

Table 4.64: MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:58:36		2018-Sep-26 17:59:49	
Reset RX	OA	HO		VO	VO (%)
true	25279	112		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

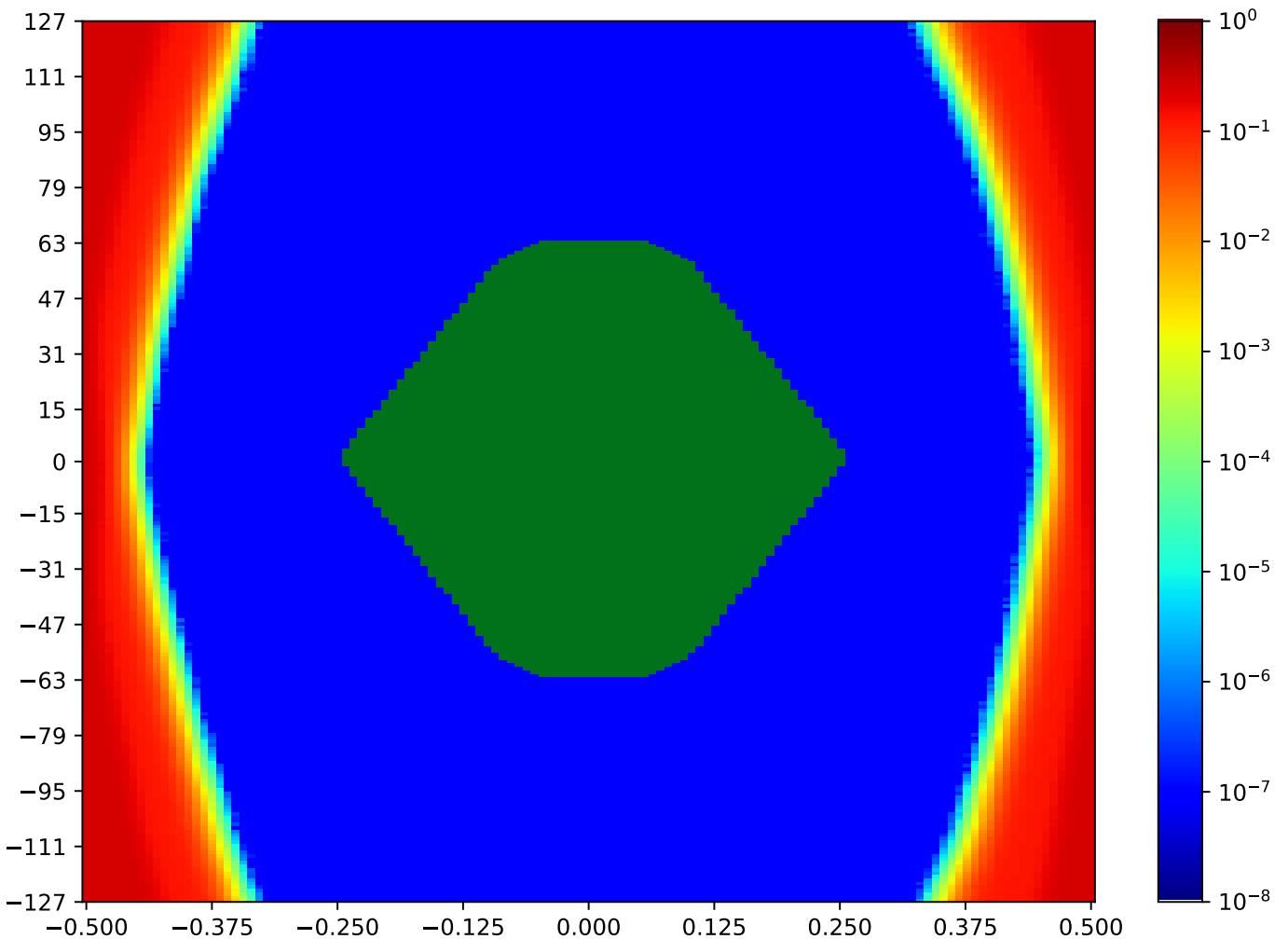


Figure 4.72: MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.4 MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

Table 4.65: MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 17:59:49		2018-Sep-26 18:01:01	
Reset RX	OA	HO		VO	VO (%)
true	24909	106		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

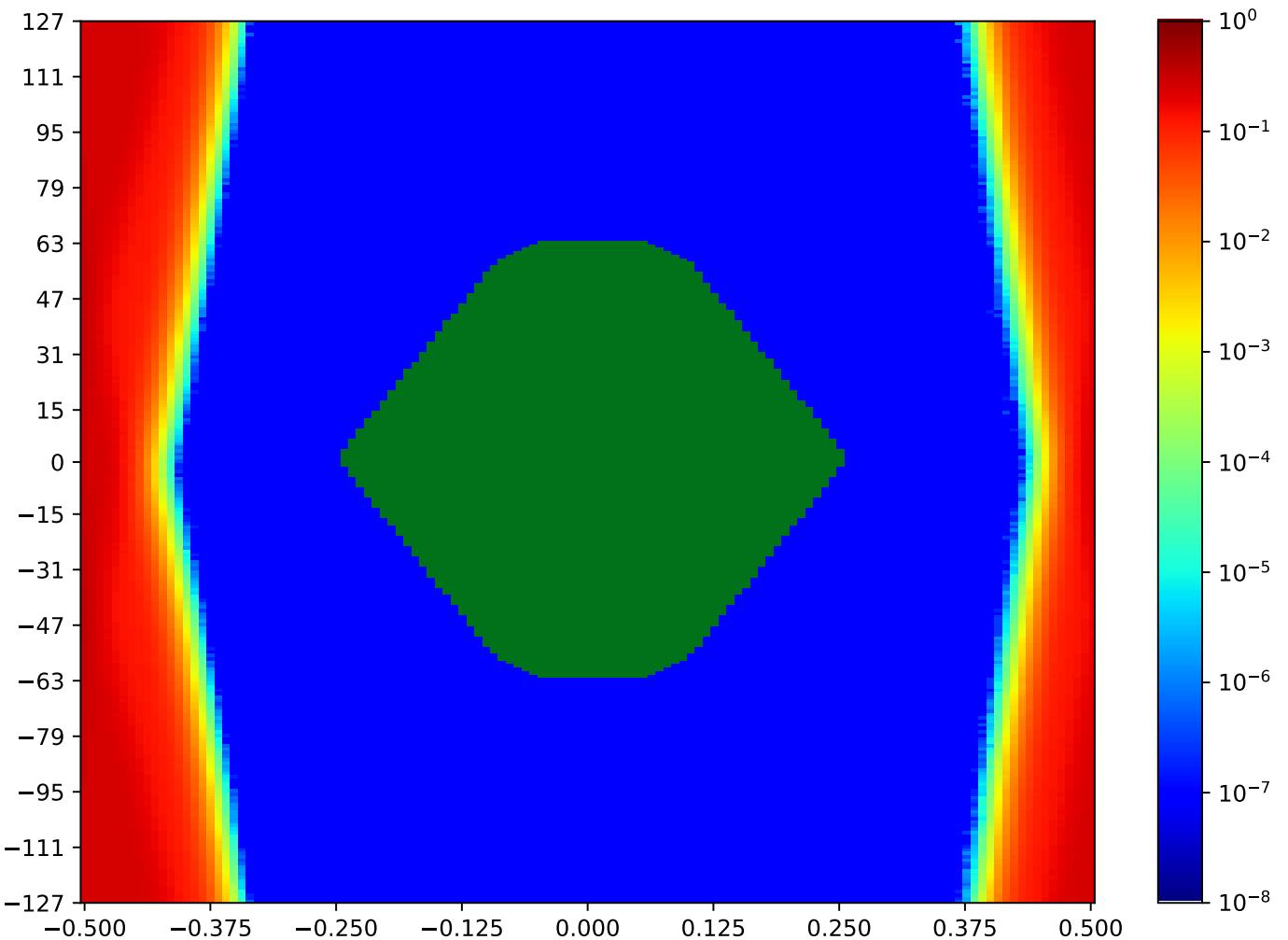


Figure 4.73: MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.5 MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

Table 4.66: MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:01:02		2018-Sep-26 18:02:14	
Reset RX	OA	HO		HO (%)	
true	25324	112		86.82%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

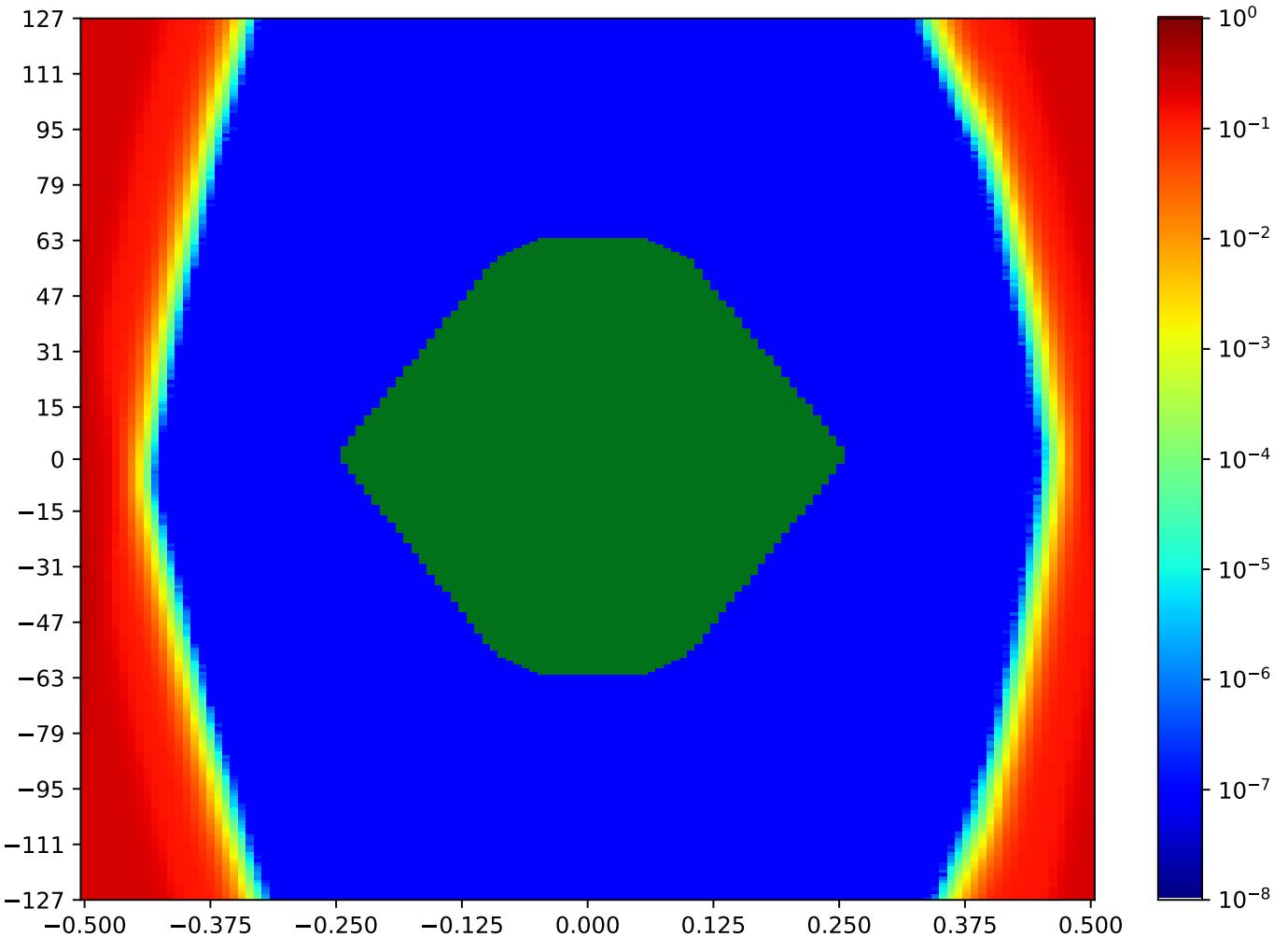


Figure 4.74: MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.6 MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

Table 4.67: MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:02:15		2018-Sep-26 18:03:27	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25263	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

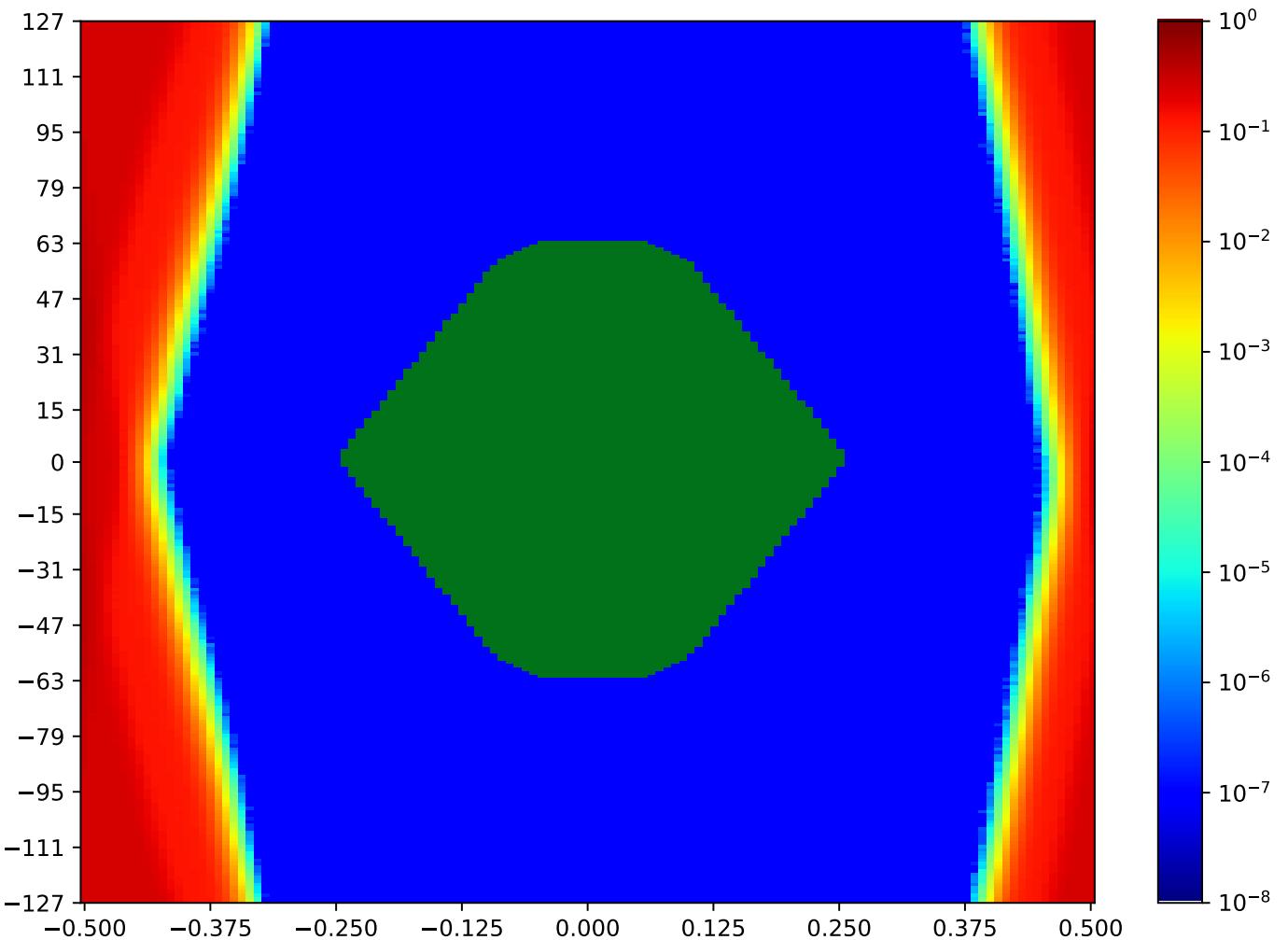


Figure 4.75: MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.7 MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

Table 4.68: MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:03:27		2018-Sep-26 18:04:38	
Reset RX	OA	HO		HO (%)	
true	24060	104		80.62%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

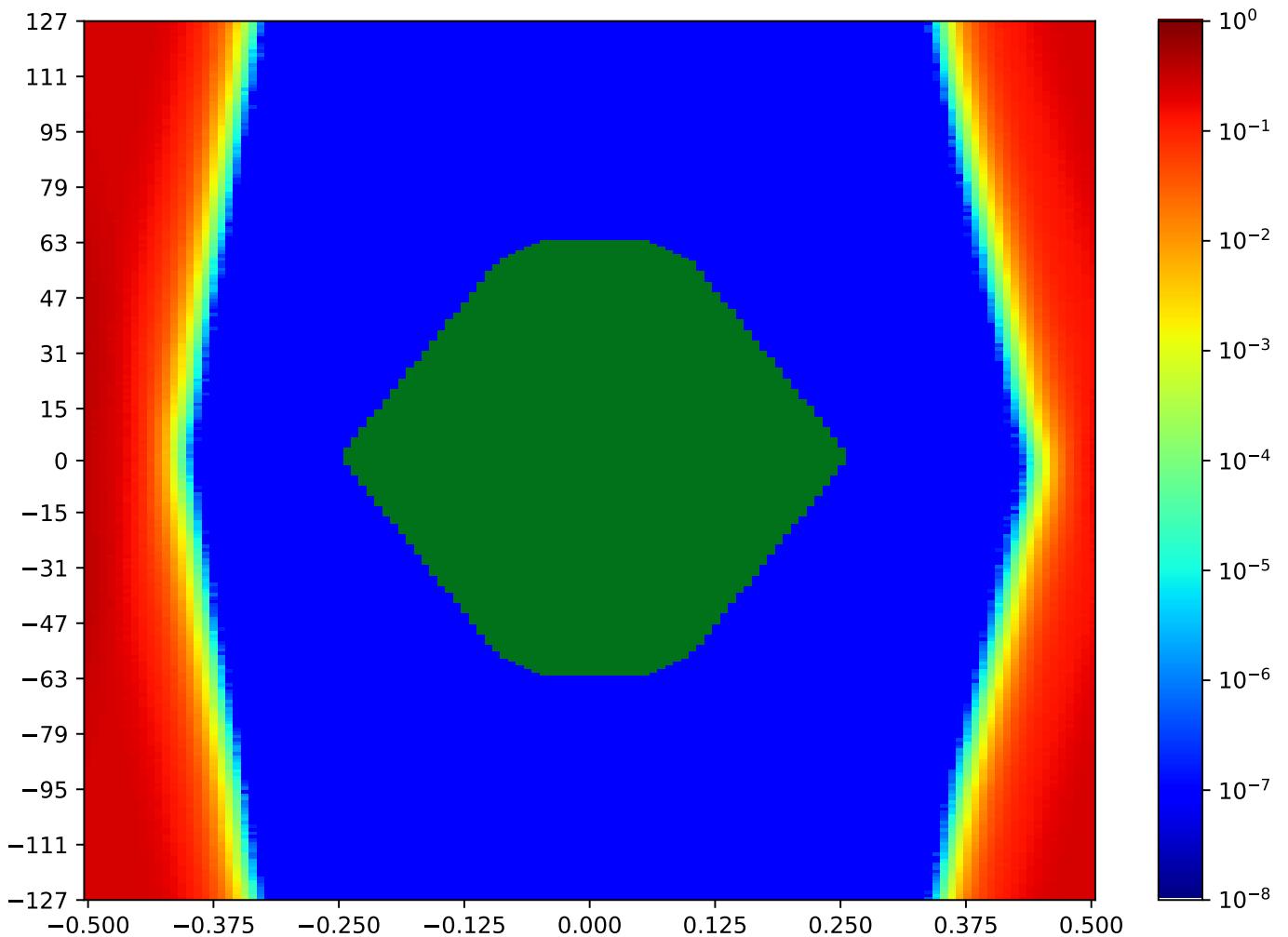


Figure 4.76: MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.8 MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

Table 4.69: MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:04:38		2018-Sep-26 18:05:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25403	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

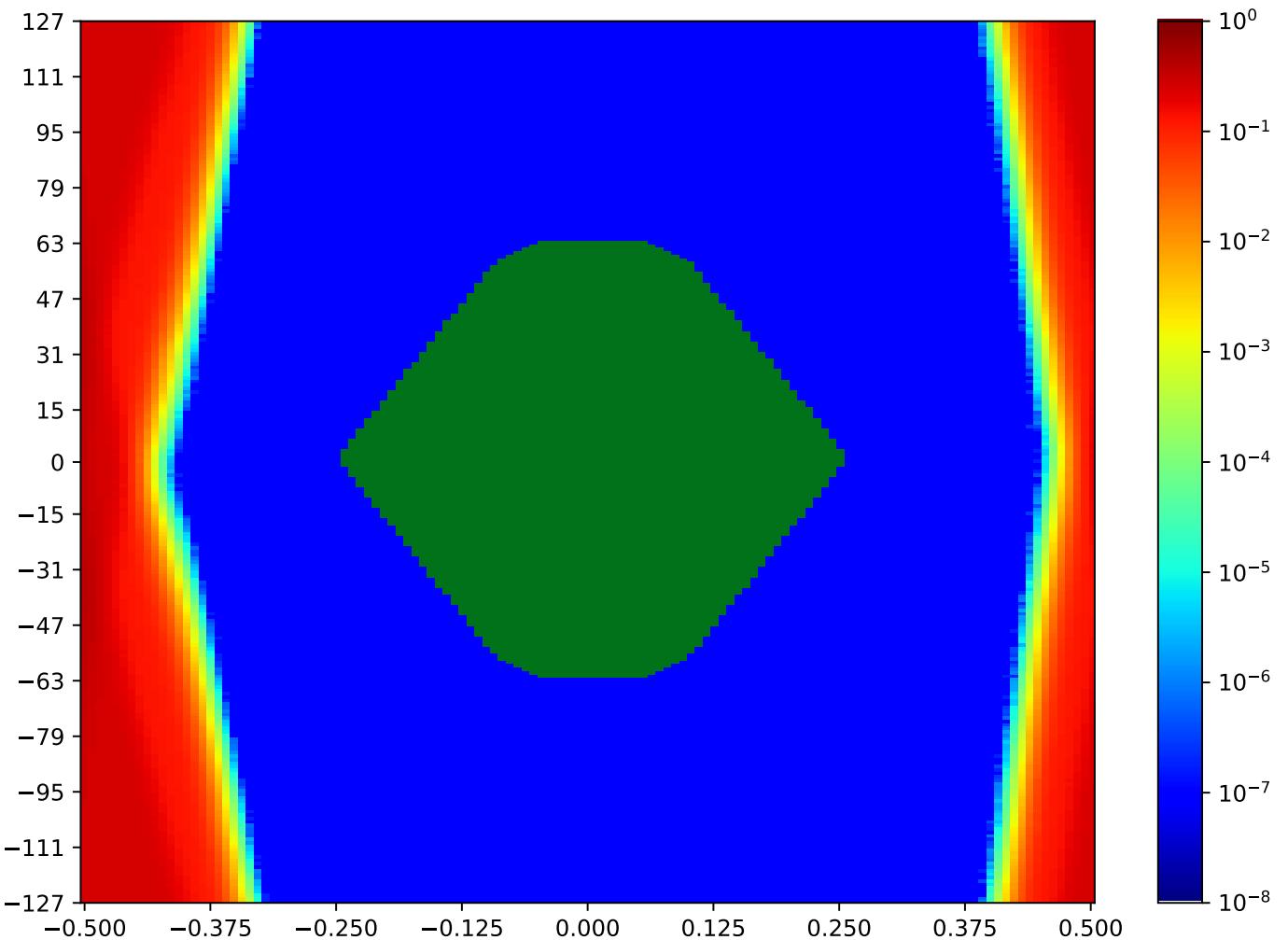


Figure 4.77: MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.9 MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

Table 4.70: MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:05:51		2018-Sep-26 18:07:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25194	111	85.27%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

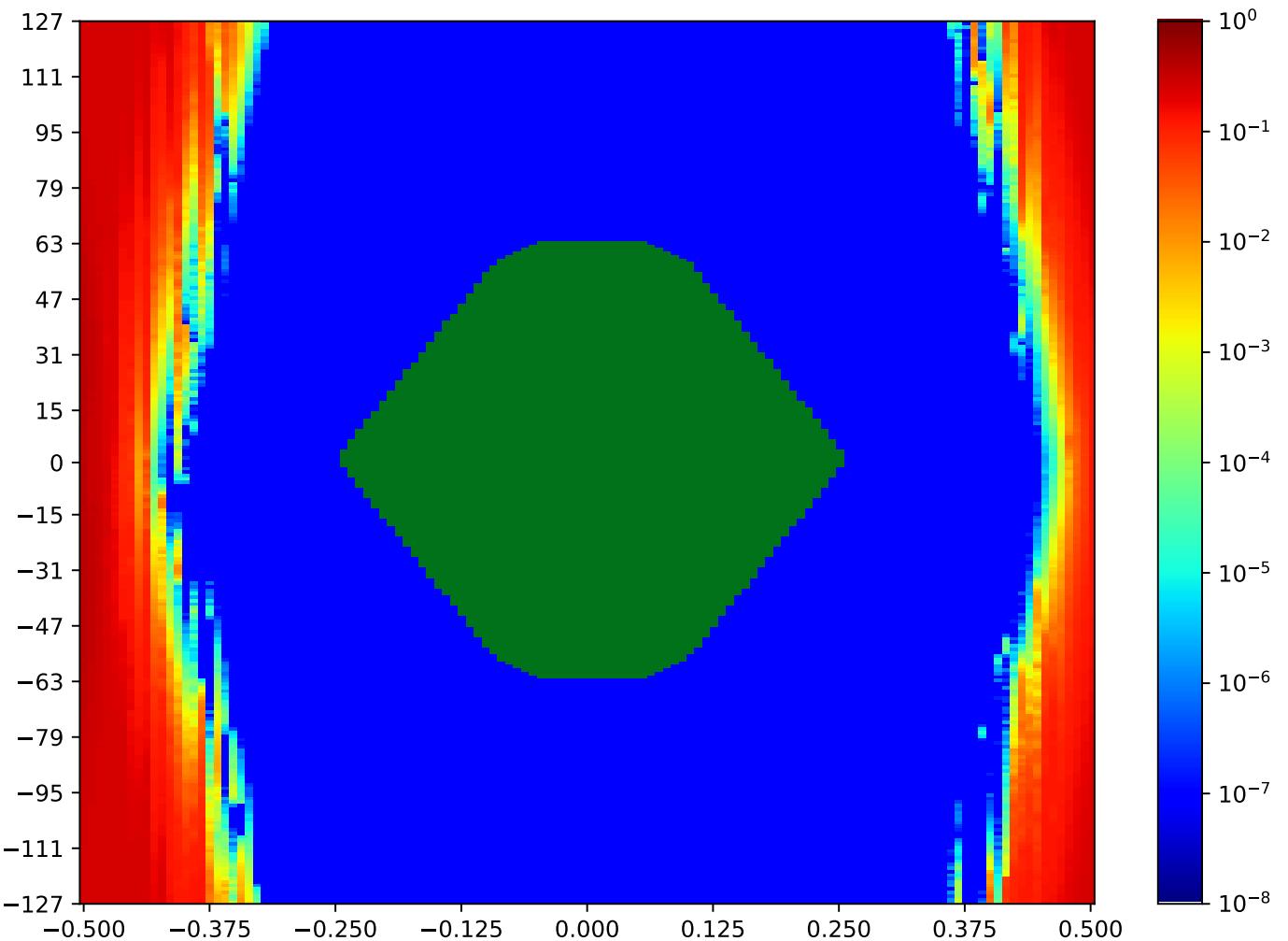


Figure 4.78: MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.10 MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

Table 4.71: MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:07:04		2018-Sep-26 18:08:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25468	110	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

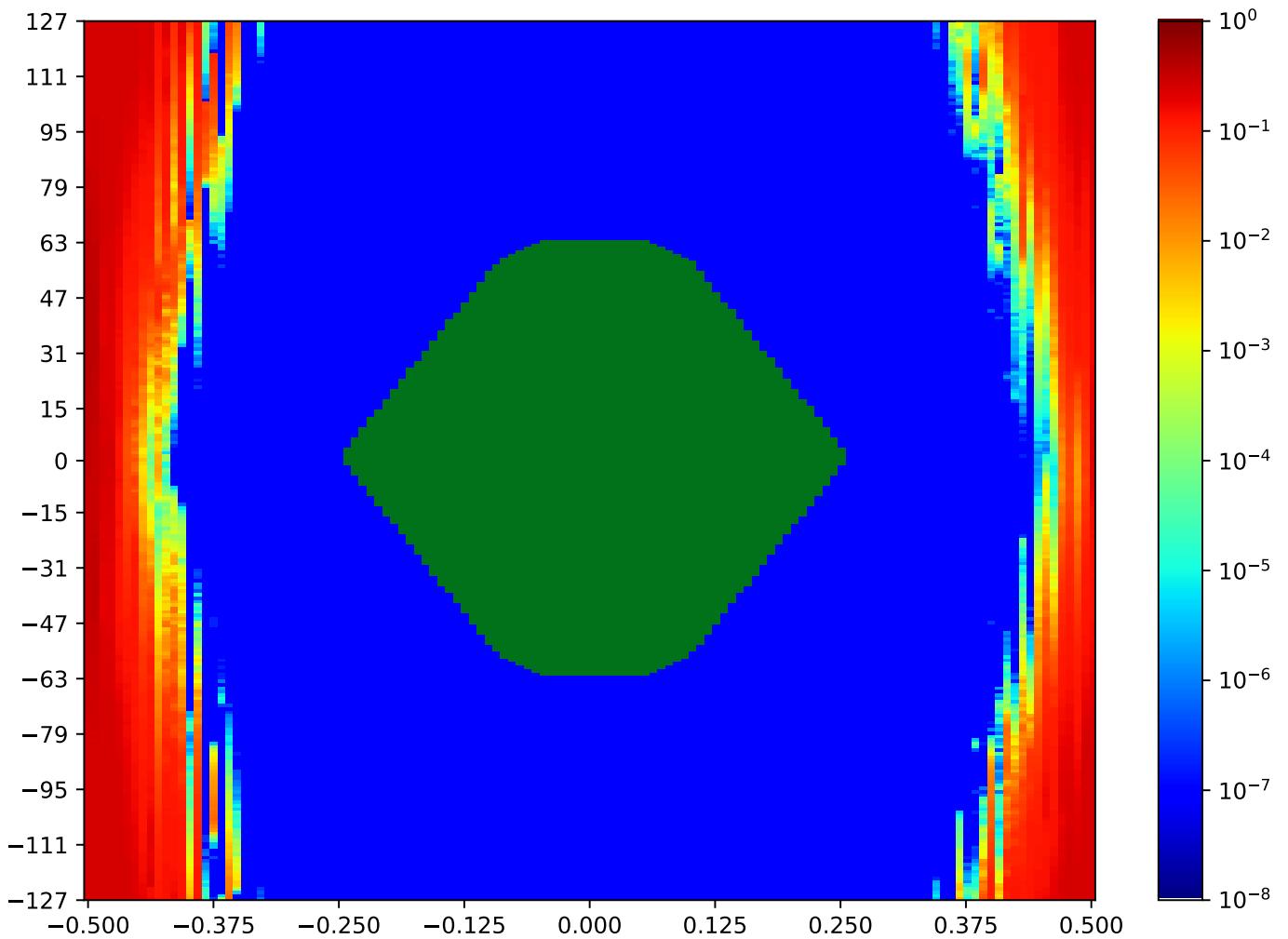


Figure 4.79: MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.11 MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

Table 4.72: MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:08:16		2018-Sep-26 18:09:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25142	108	83.72%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

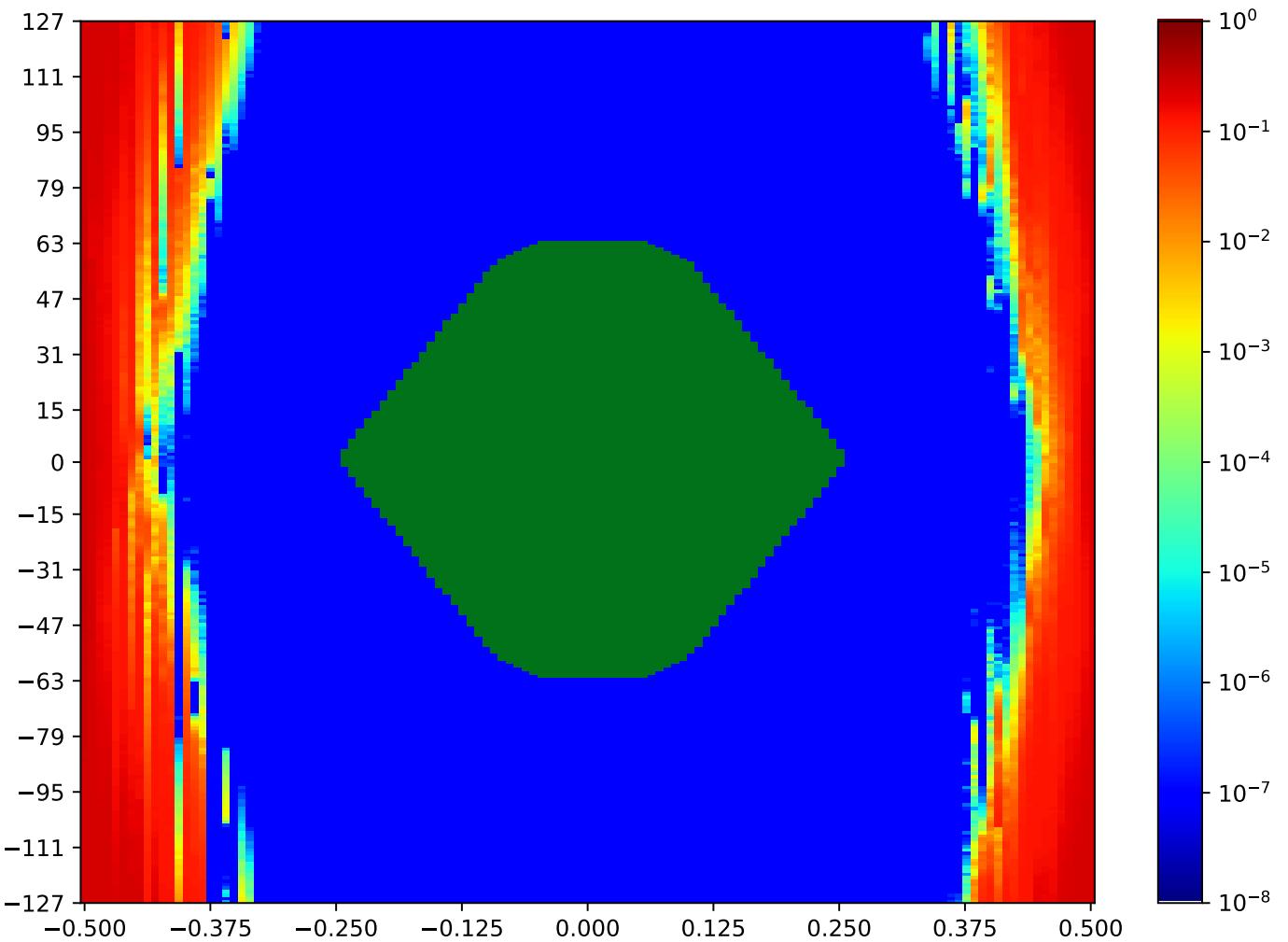


Figure 4.80: MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.12 MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

Table 4.73: MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:09:28		2018-Sep-26 18:10:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25176	107	82.95%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

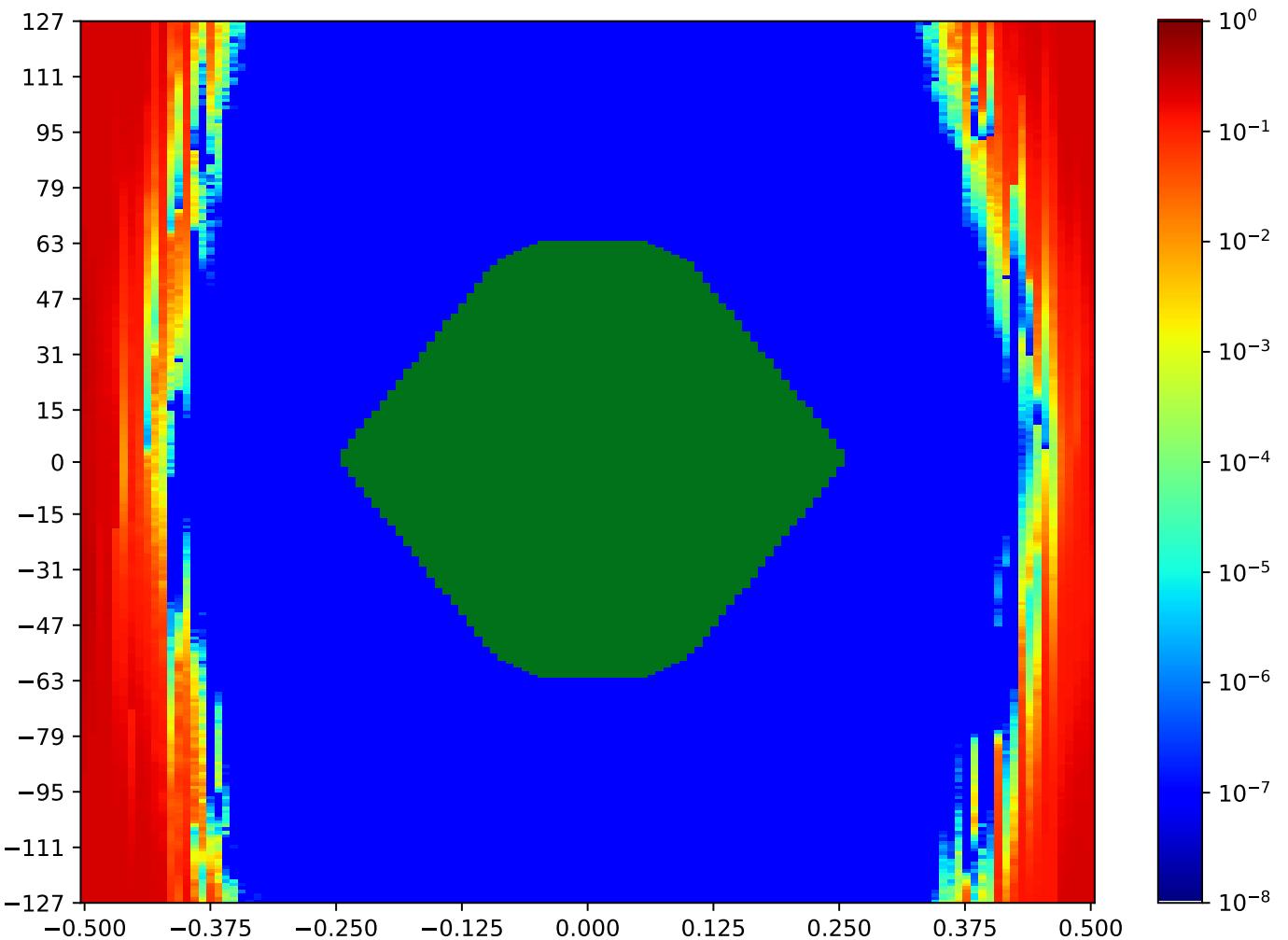


Figure 4.81: MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.13 MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

Table 4.74: MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:10:41		2018-Sep-26 18:11:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24242	108	83.72%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

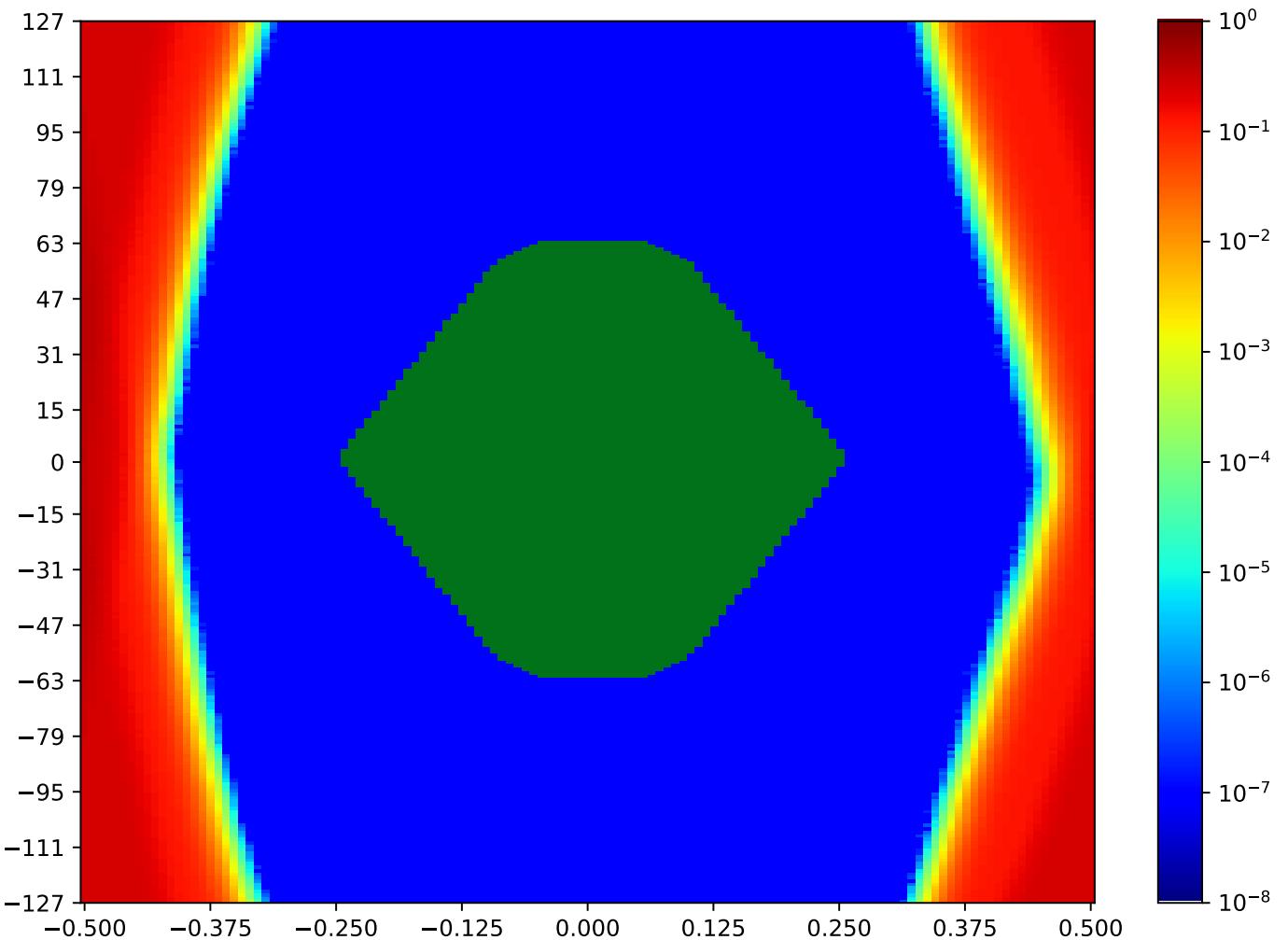


Figure 4.82: MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.14 MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

Table 4.75: MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:11:53		2018-Sep-26 18:13:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26331	113	87.60%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

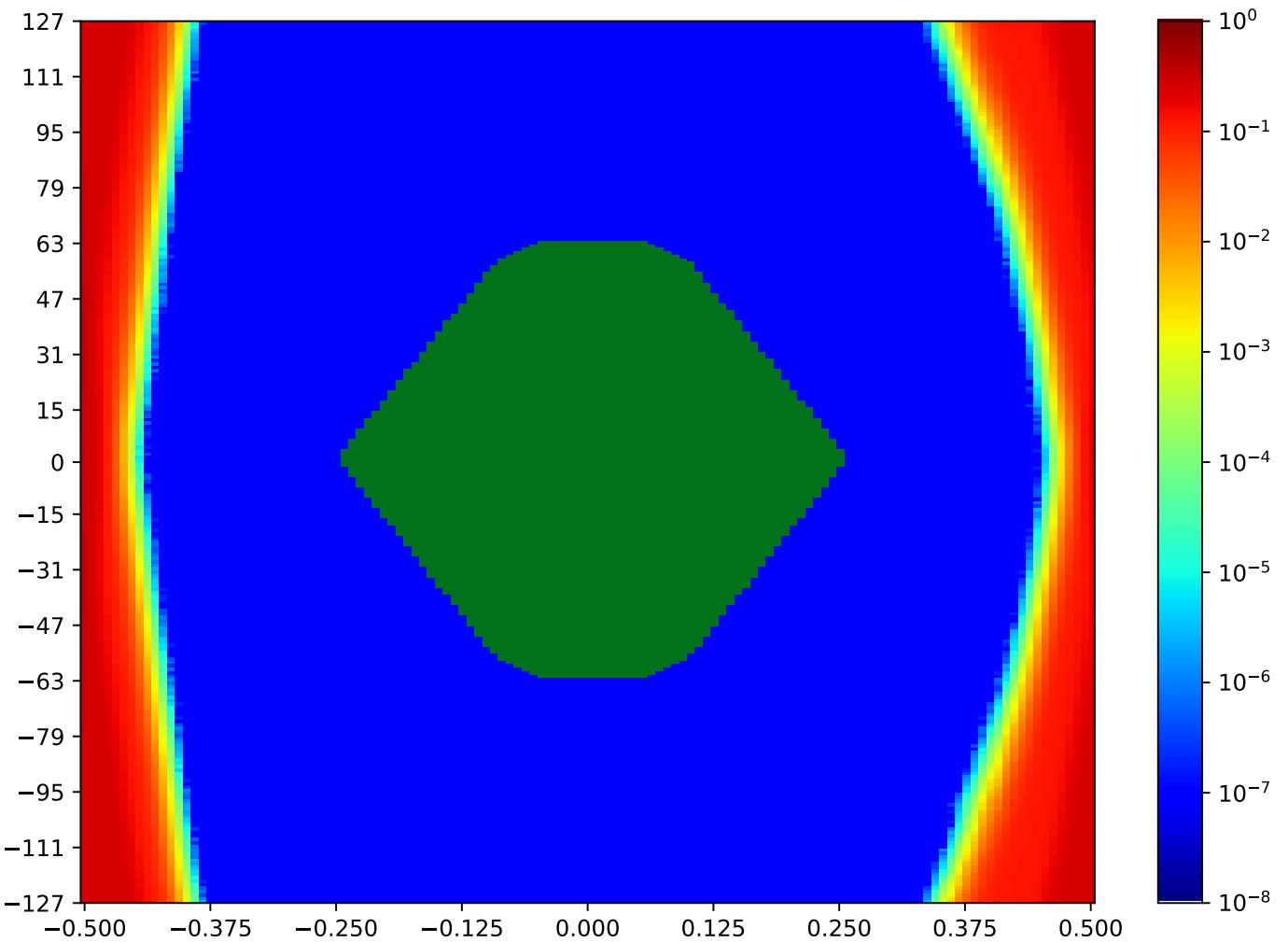


Figure 4.83: MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.15 MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

Table 4.76: MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:13:06		2018-Sep-26 18:14:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23881	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

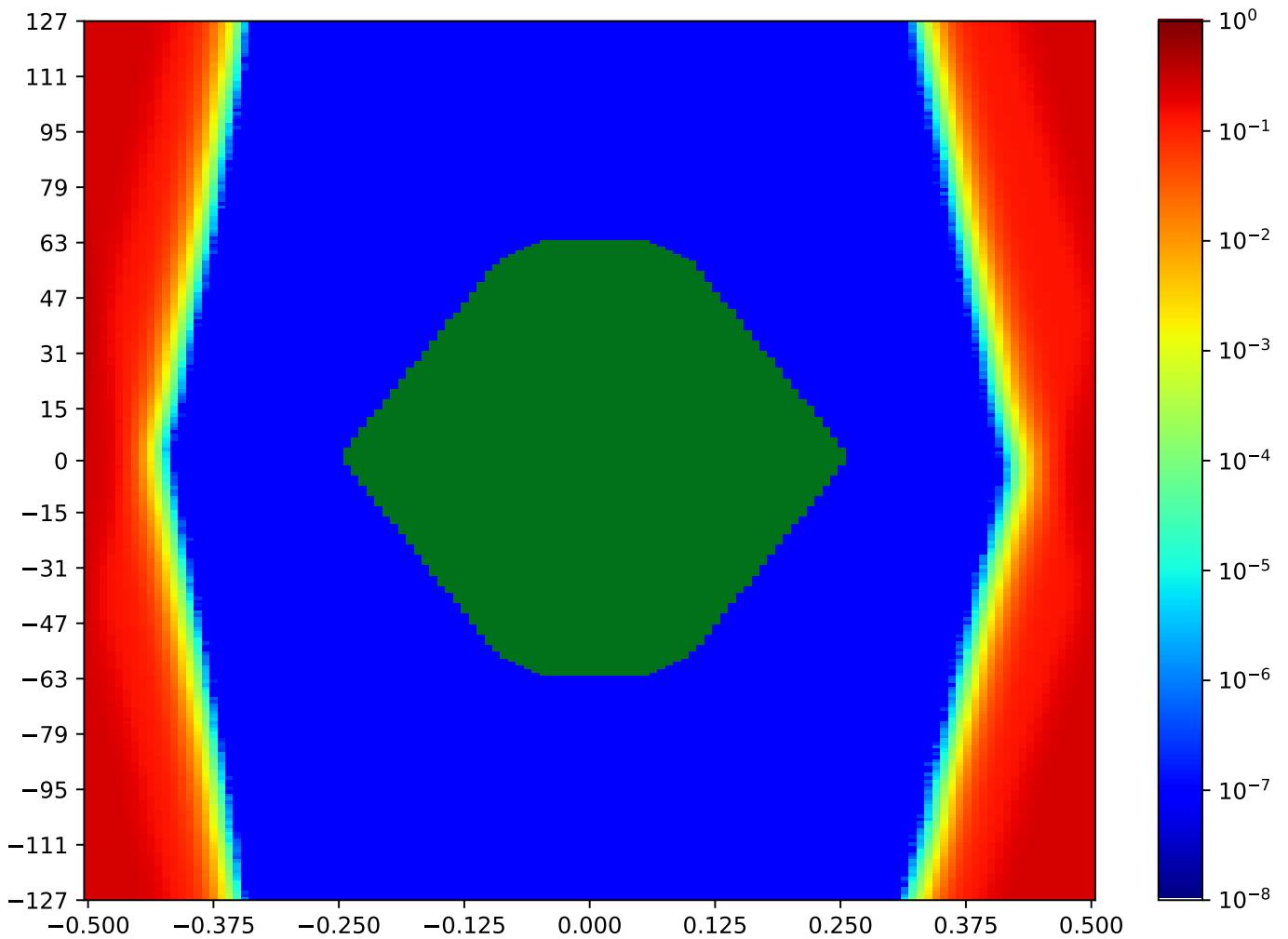


Figure 4.84: MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.16 MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

Table 4.77: MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:14:17		2018-Sep-26 18:15:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25577	112	86.82%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

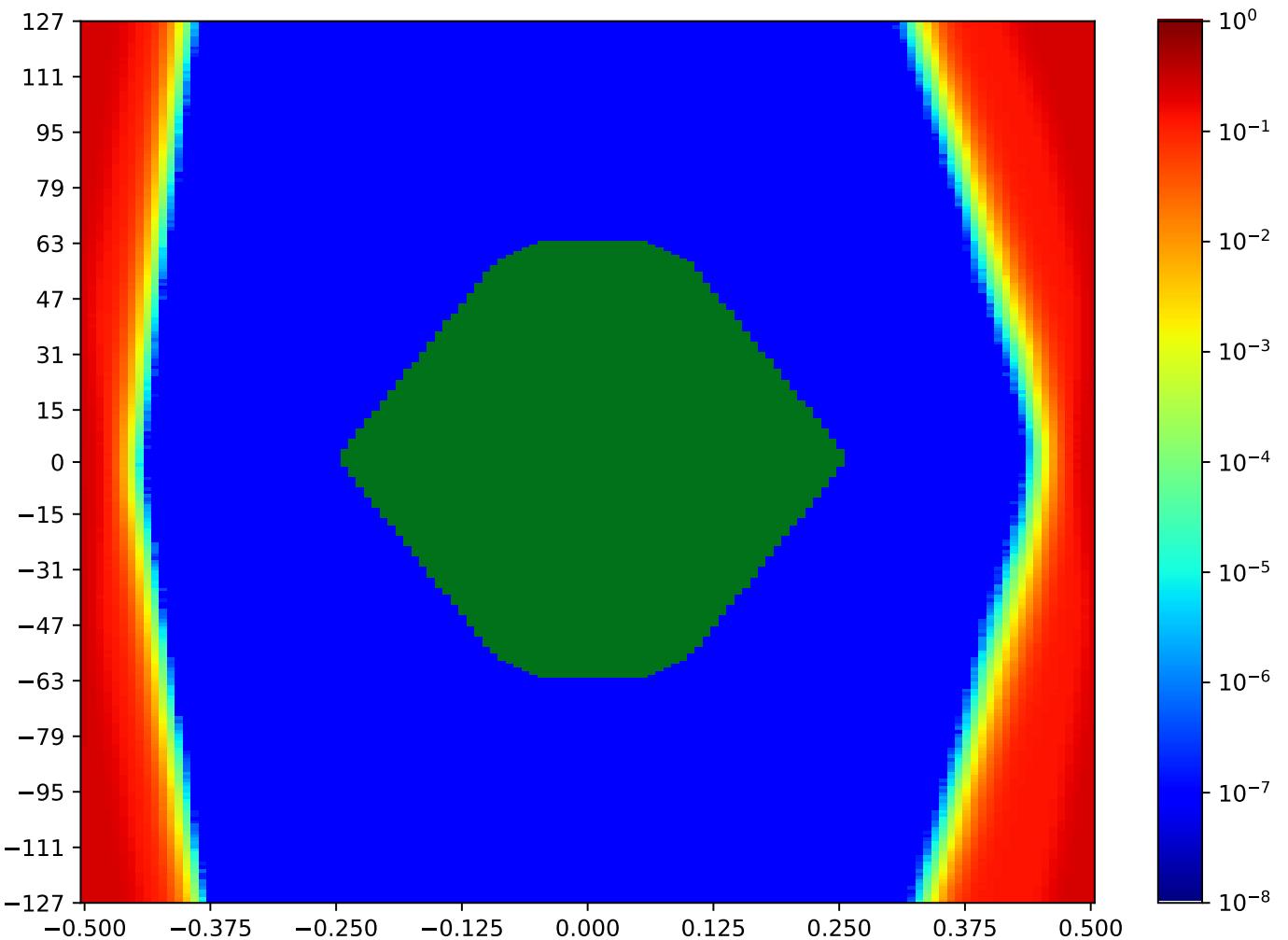


Figure 4.85: MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.17 MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

Table 4.78: MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:15:30		2018-Sep-26 18:16:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25259	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

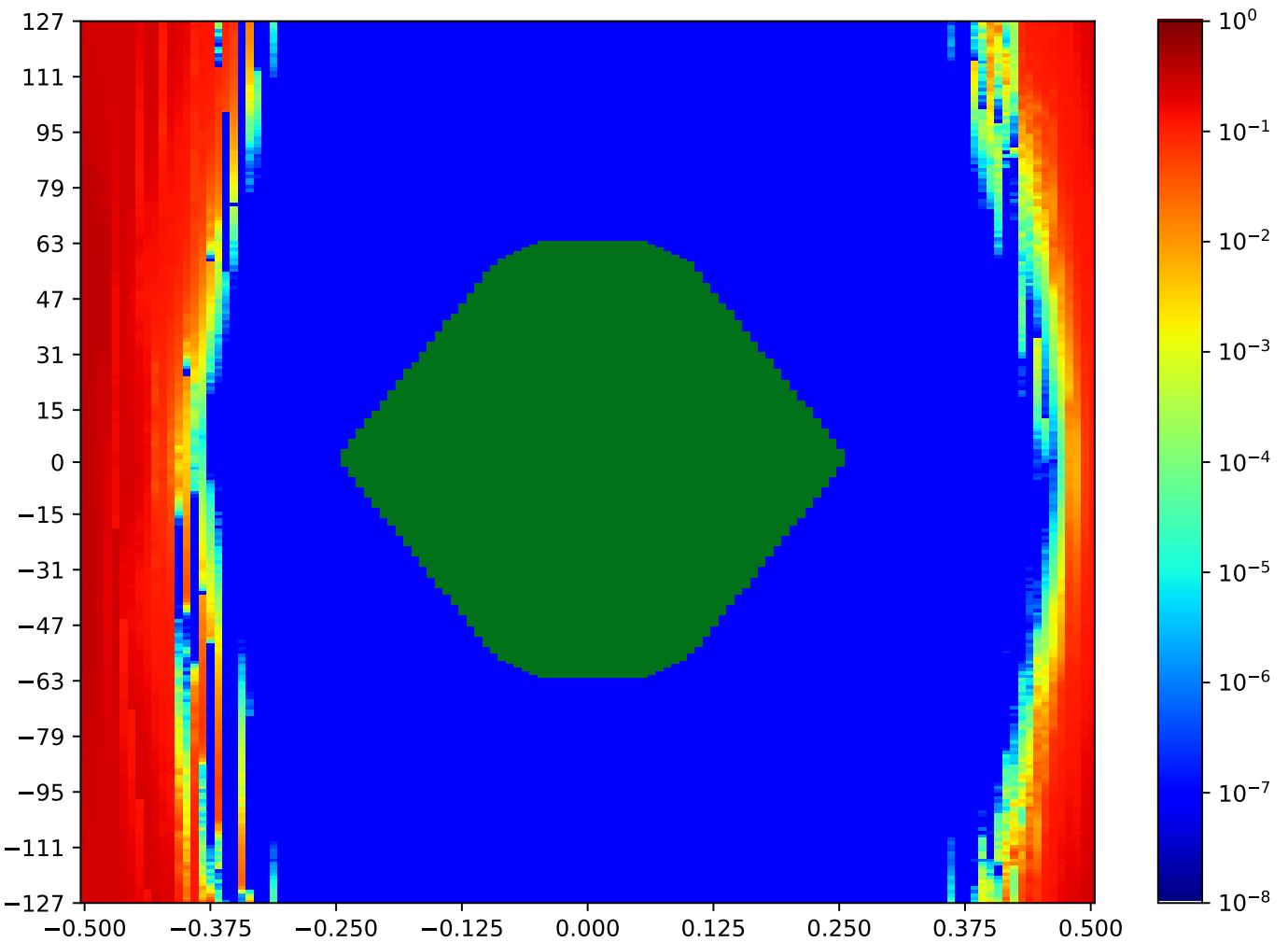


Figure 4.86: MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.18 MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

Table 4.79: MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:16:43		2018-Sep-26 18:17:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23968	106	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

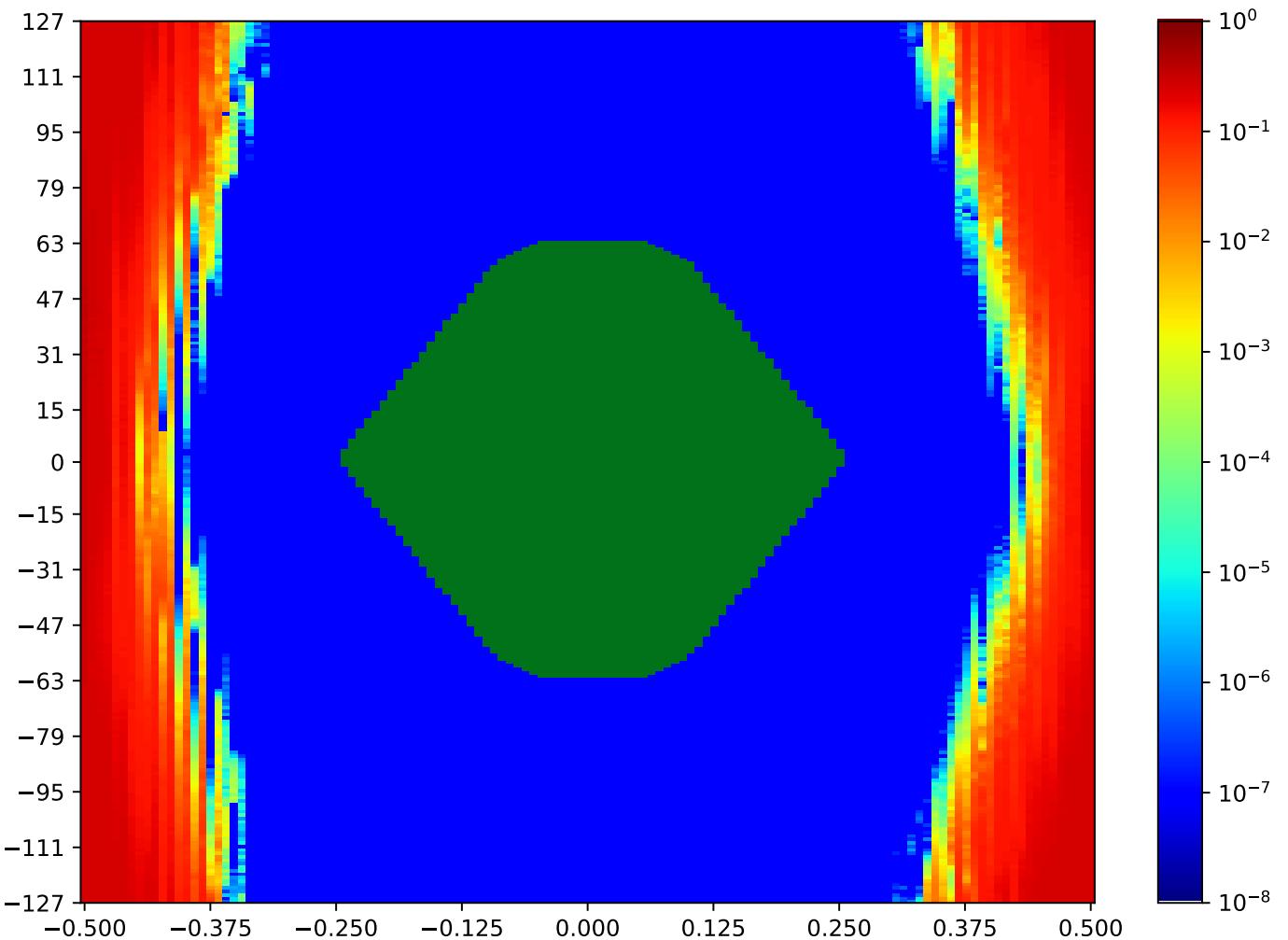


Figure 4.87: MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.19 MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

Table 4.80: MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:17:54		2018-Sep-26 18:19:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	26039	111	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

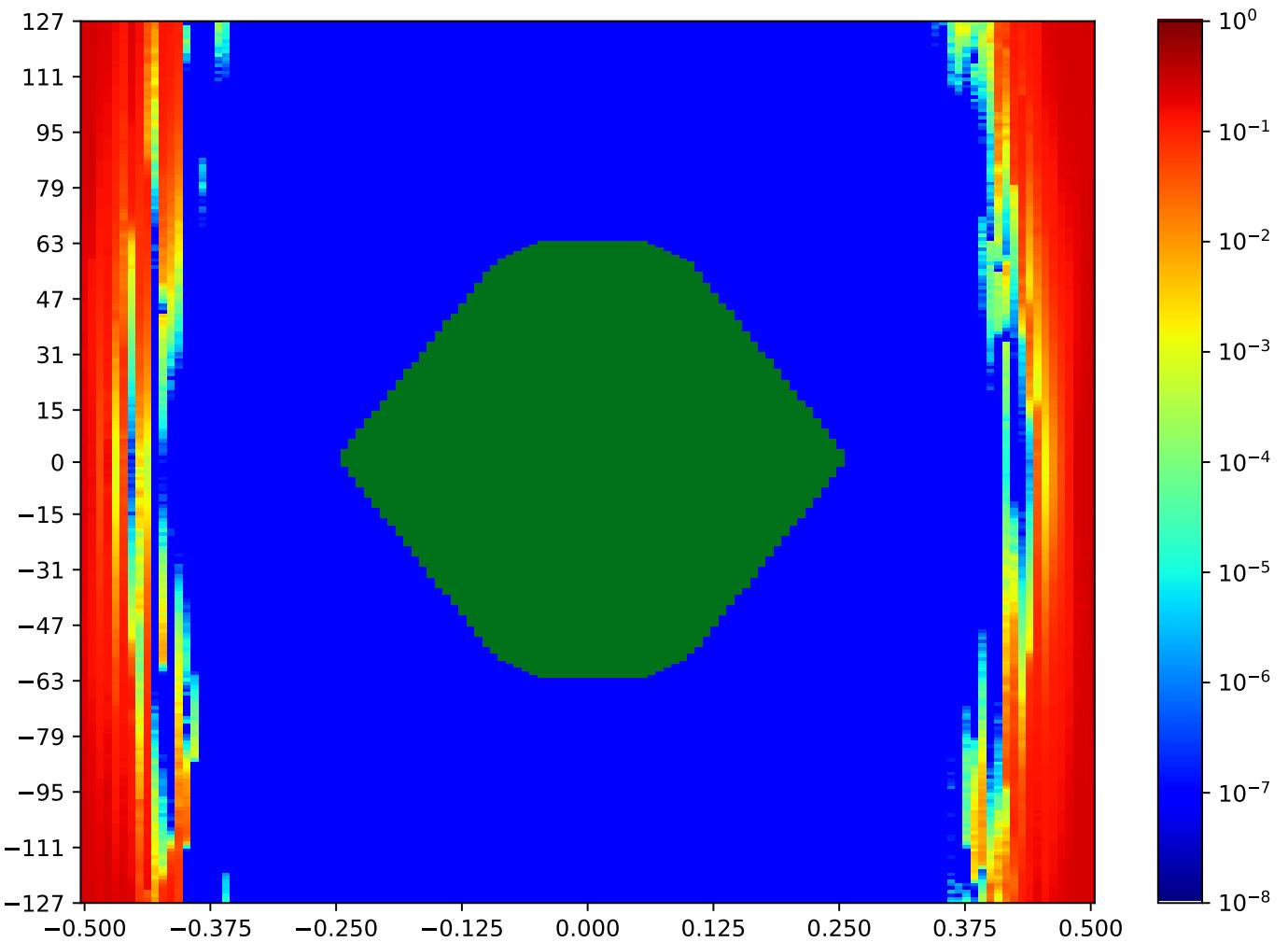


Figure 4.88: MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.20 MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

Table 4.81: MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:19:08		2018-Sep-26 18:20:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25028	108	83.72%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

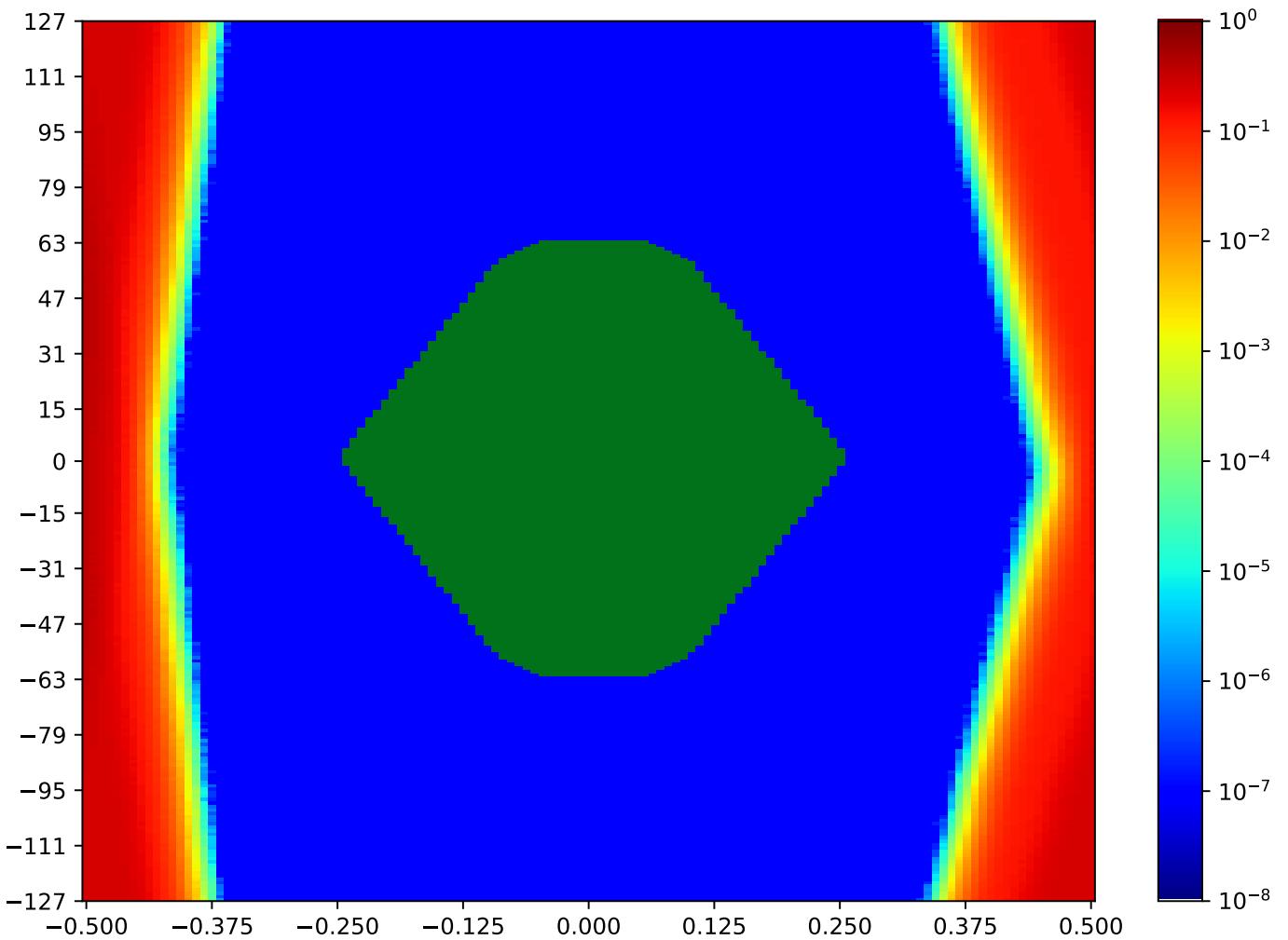


Figure 4.89: MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.21 MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

Table 4.82: MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:20:21		2018-Sep-26 18:21:33	
Reset RX	OA	HO		HO (%)	
true	24922	106		82.17%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

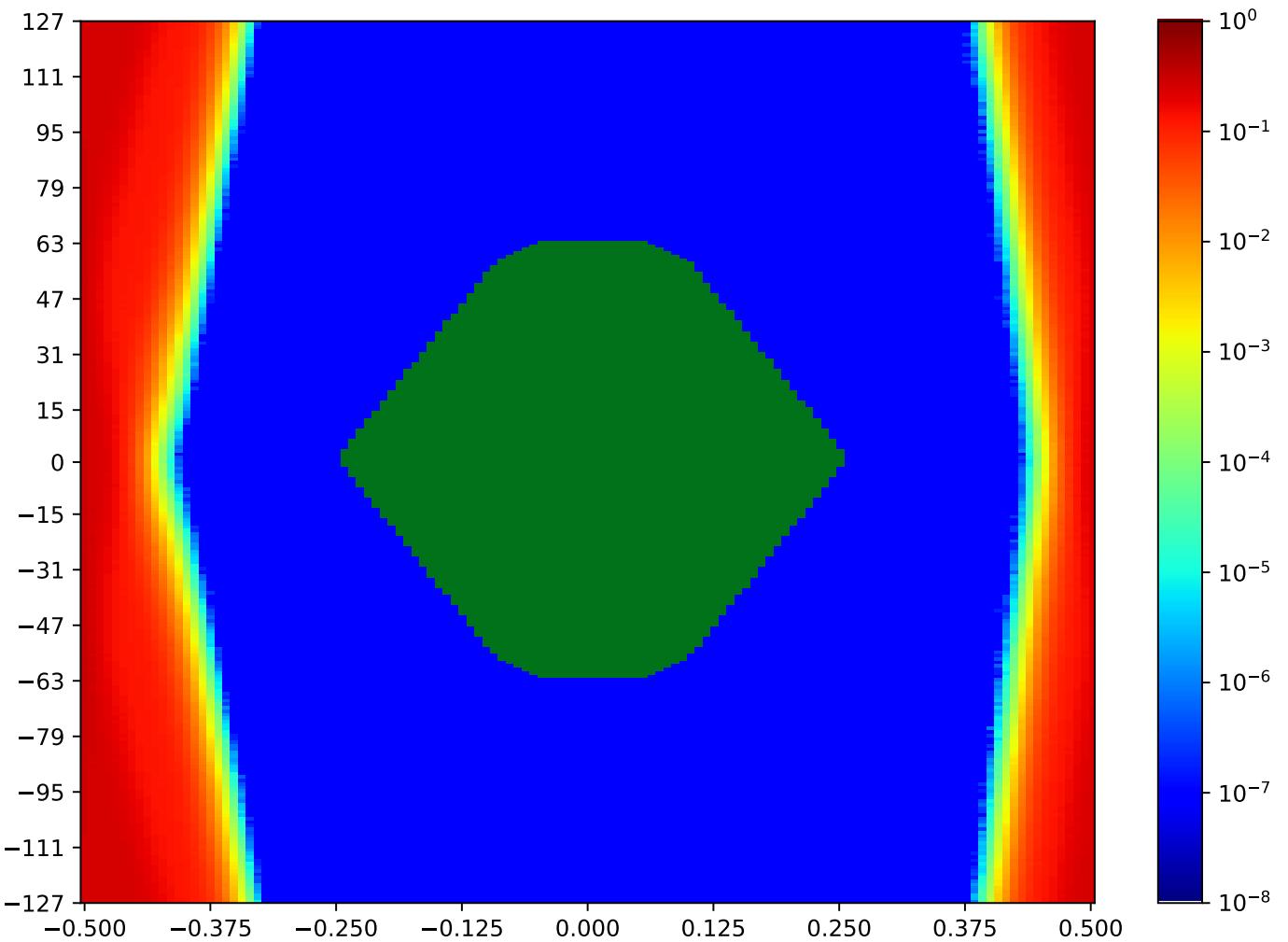


Figure 4.90: MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.22 MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

Table 4.83: MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:21:33		2018-Sep-26 18:22:45	
Reset RX	OA	HO		HO (%)	
true	24925	109		82.95%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

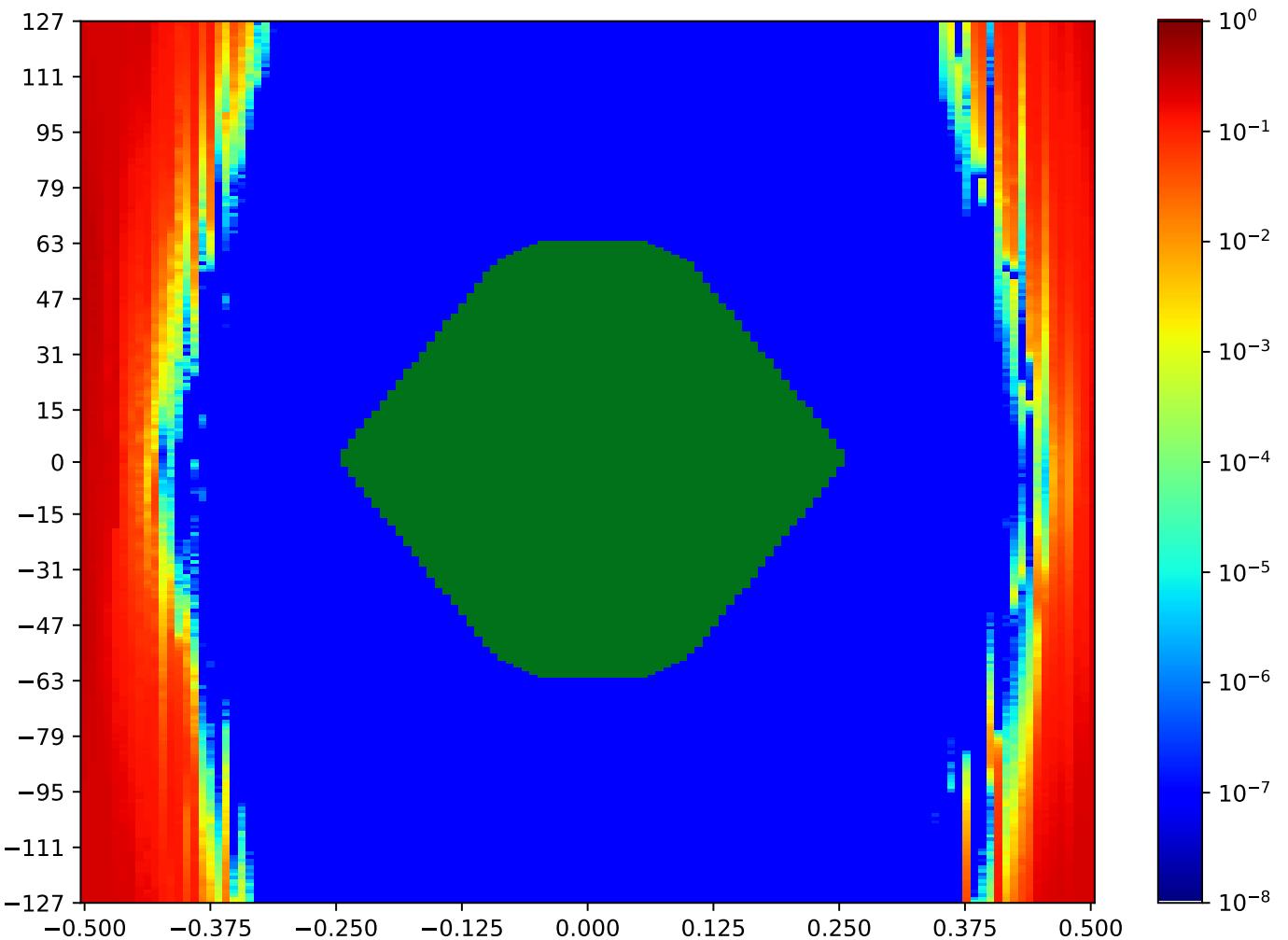


Figure 4.91: MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.23 MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

Table 4.84: MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:22:45		2018-Sep-26 18:23:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23346	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

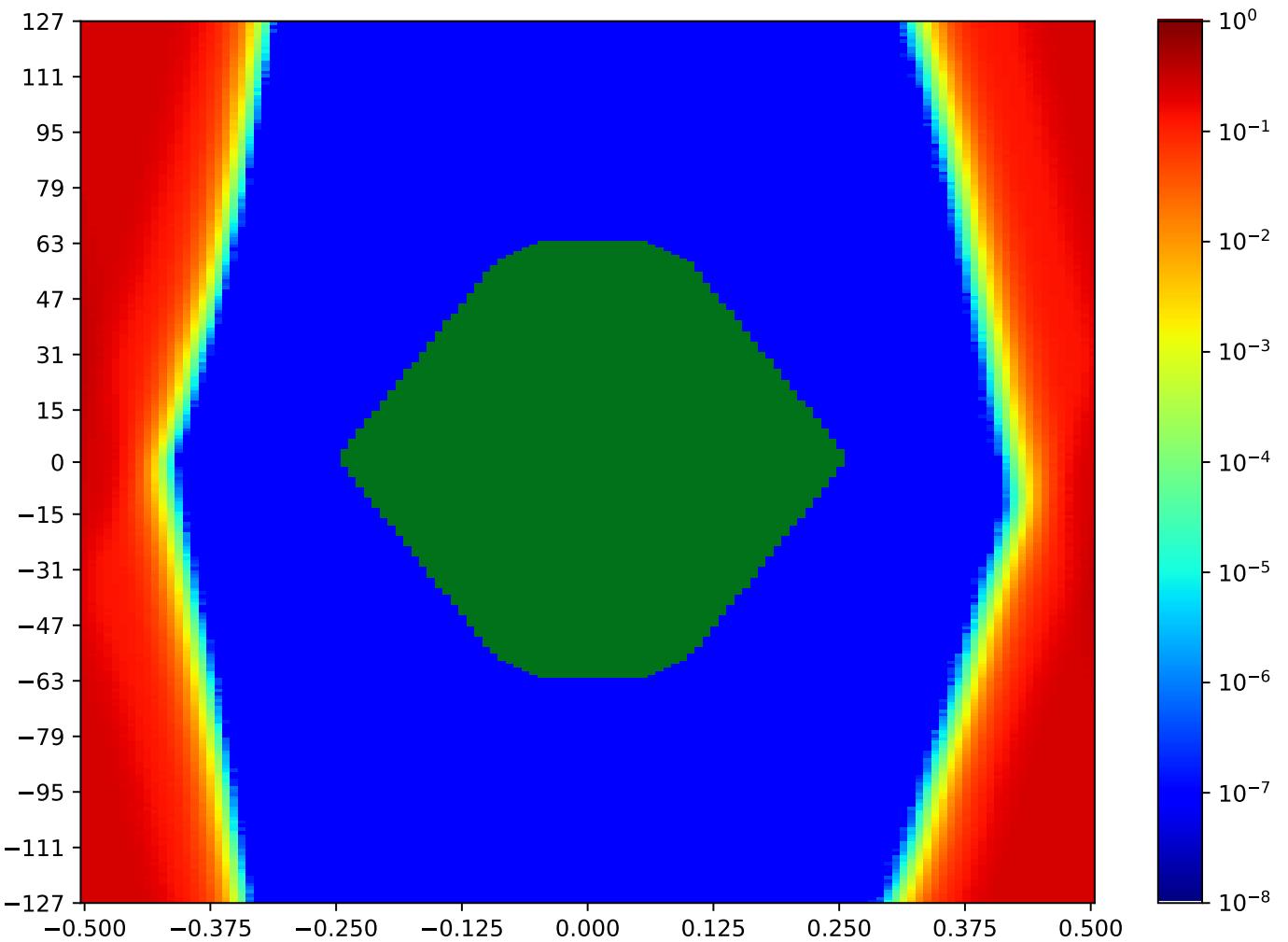


Figure 4.92: MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.24 MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

Table 4.85: MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:23:55		2018-Sep-26 18:25:06	
Reset RX	OA	HO		VO	VO (%)
true	24495	105		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

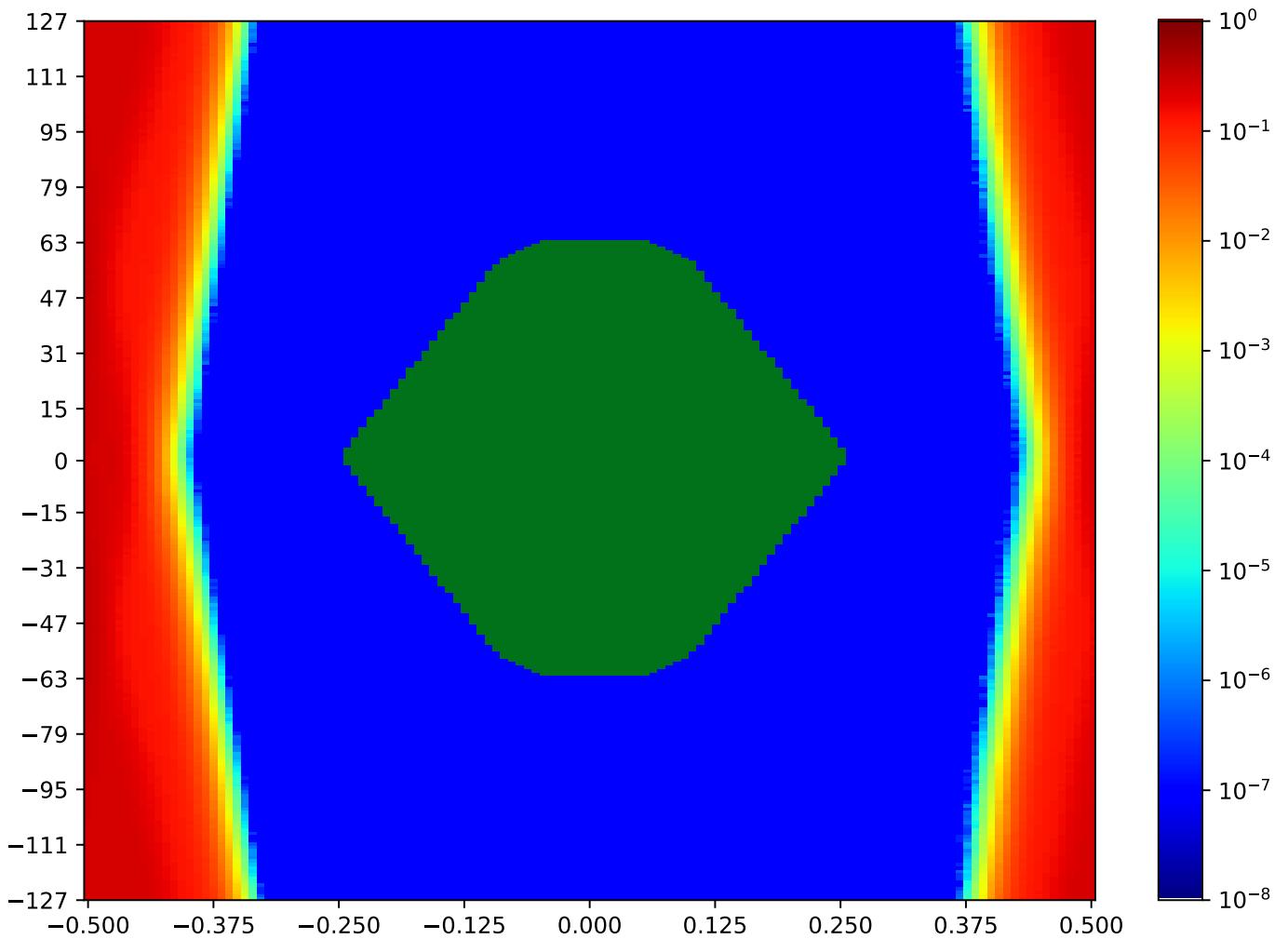


Figure 4.93: MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.25 MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

Table 4.86: MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:25:07		2018-Sep-26 18:26:19	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25186	109	84.50%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

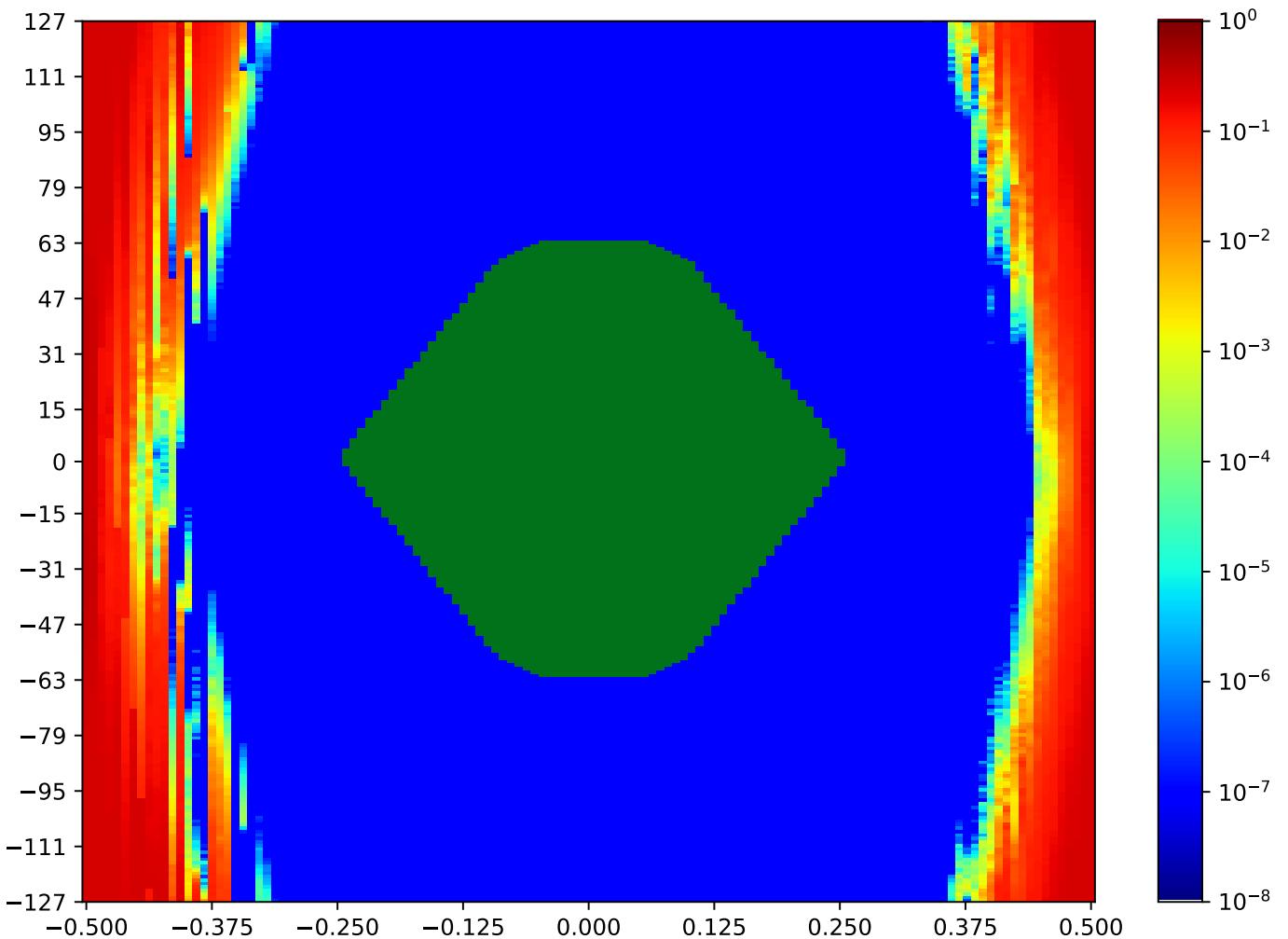


Figure 4.94: MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.26 MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

Table 4.87: MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:26:19		2018-Sep-26 18:27:32	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25548	111	86.05%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

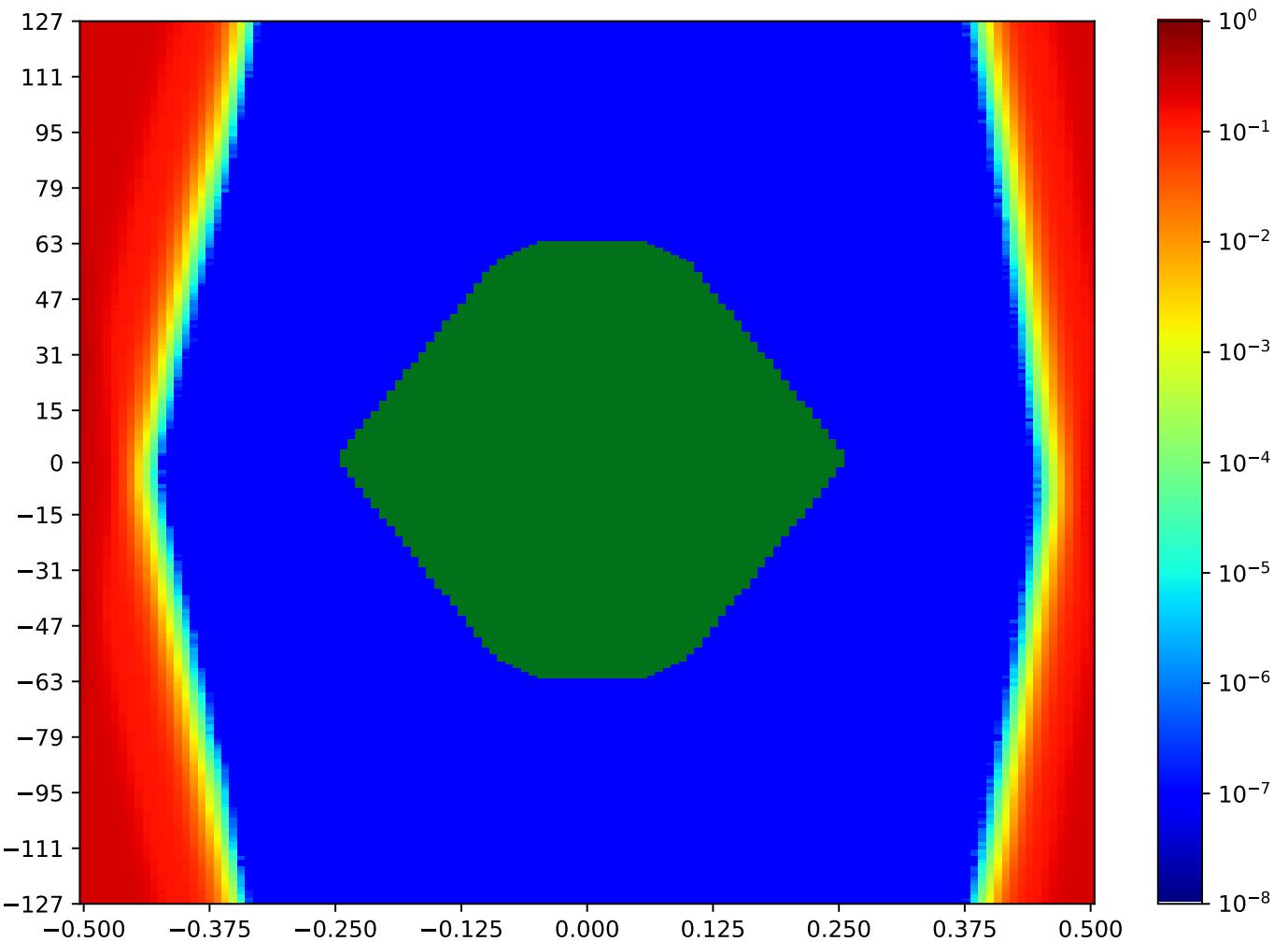


Figure 4.95: MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.27 MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

Table 4.88: MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:27:33		2018-Sep-26 18:28:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24290	105	81.40%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

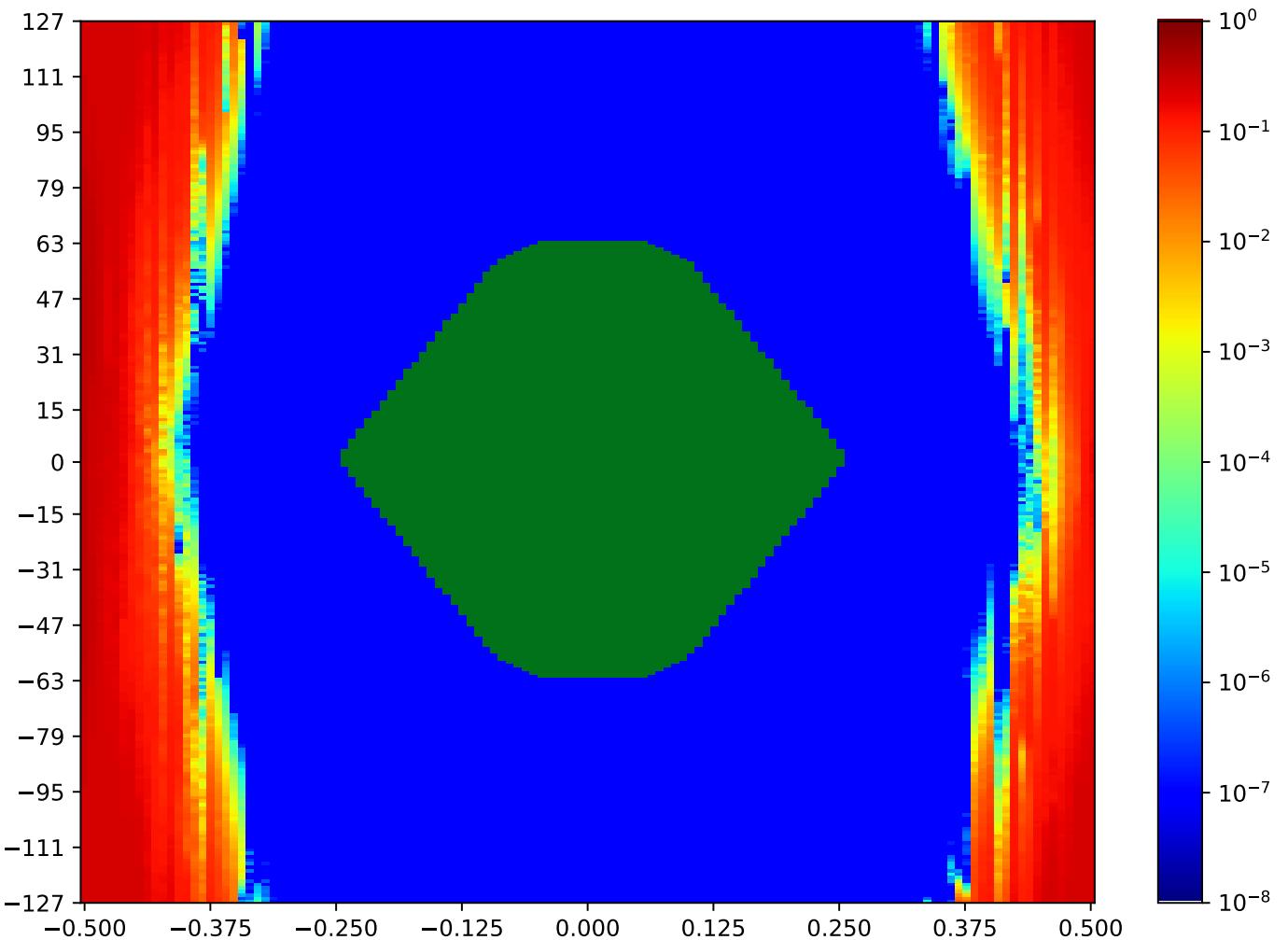


Figure 4.96: MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.8.28 MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

Table 4.89: MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-26 18:28:44		2018-Sep-26 18:29:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	25253	111	86.05%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

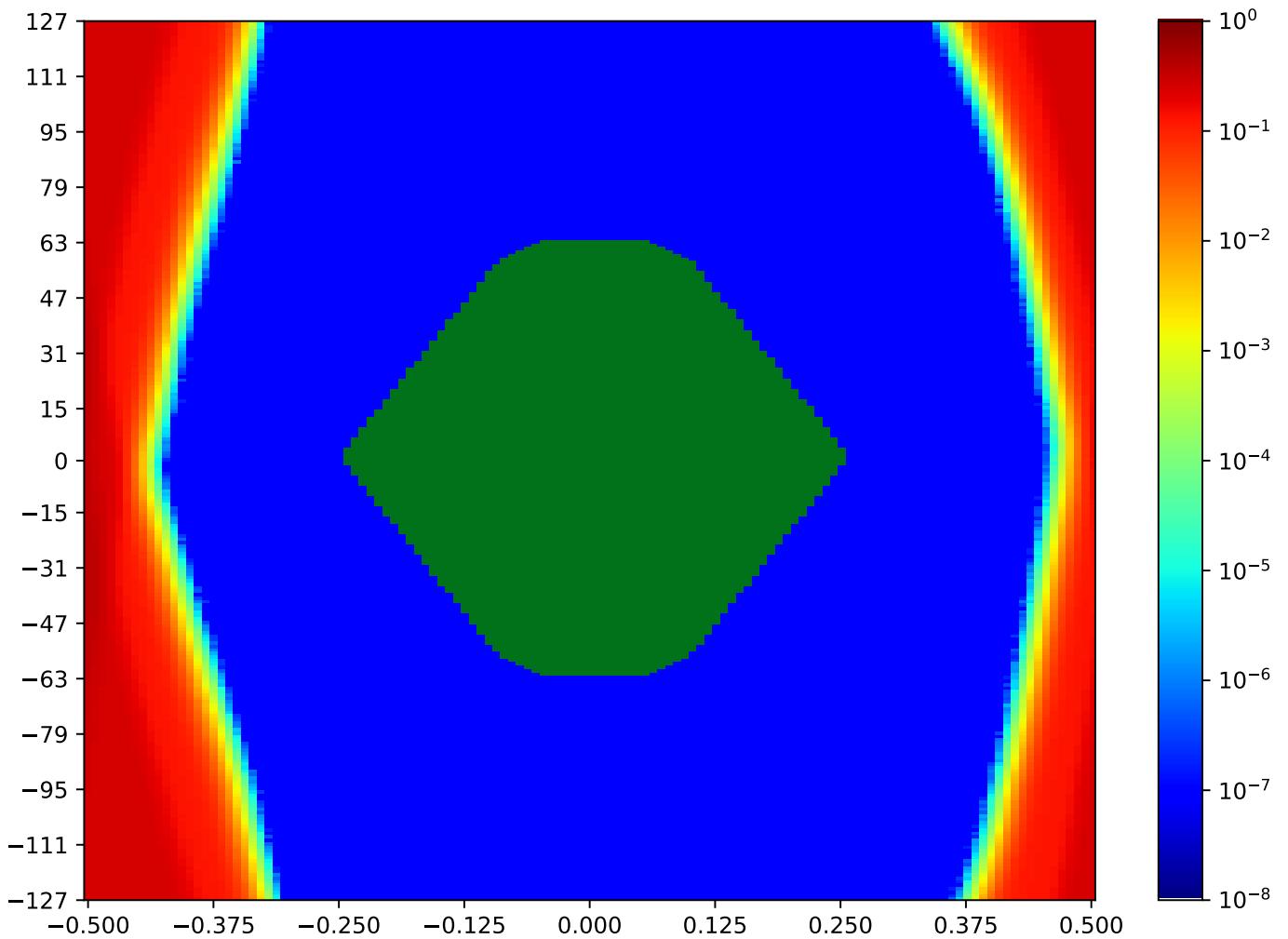


Figure 4.97: MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

Call back to summary Figure 4.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9 MSP_C TRP On board links

A cross-reference to Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.
Next summary Figure 4.127.

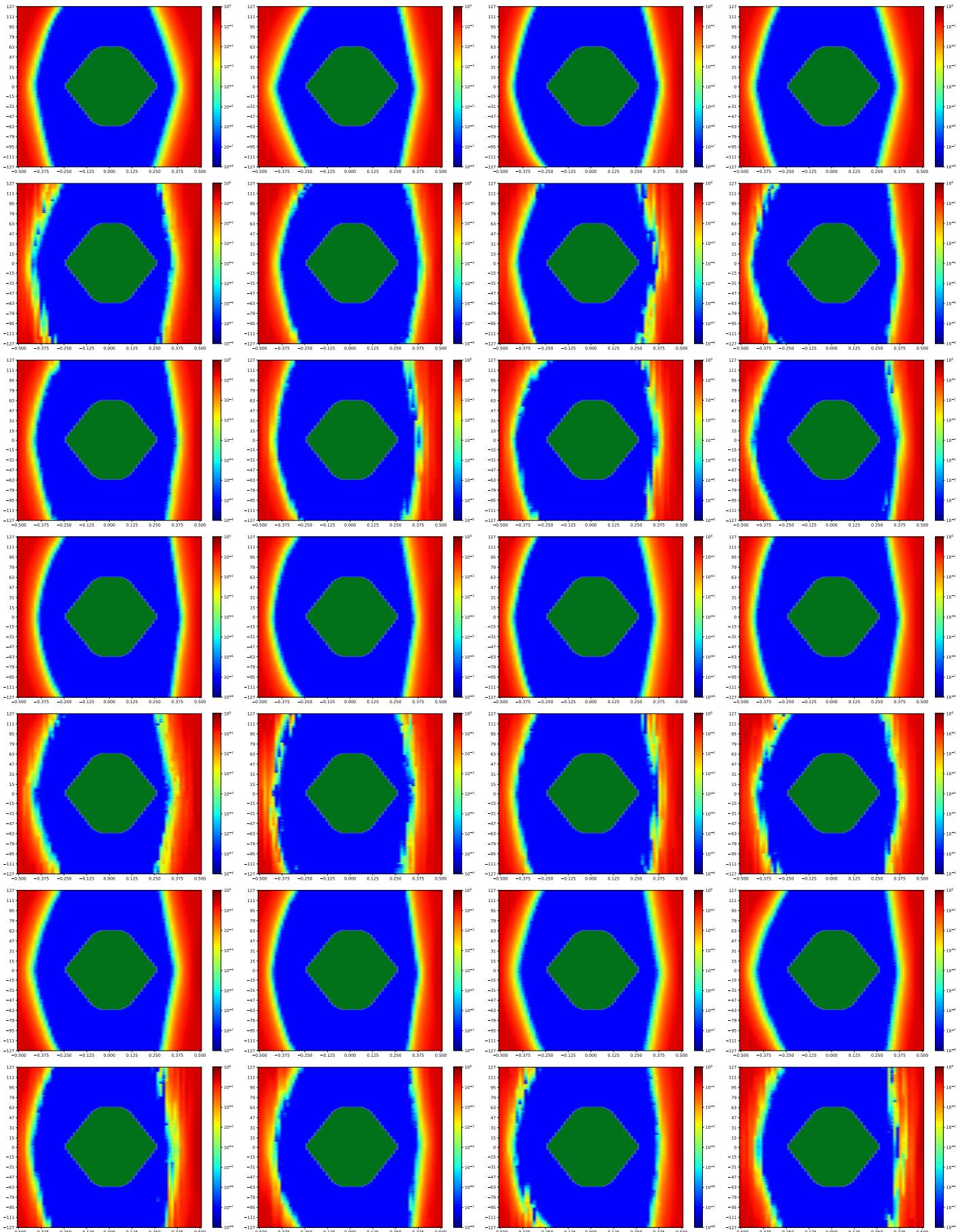


Figure 4.98: MSP_C TRP On board links

4.9.1 MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

Table 4.90: MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:29:56		2018-Sep-26 18:30:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10292	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

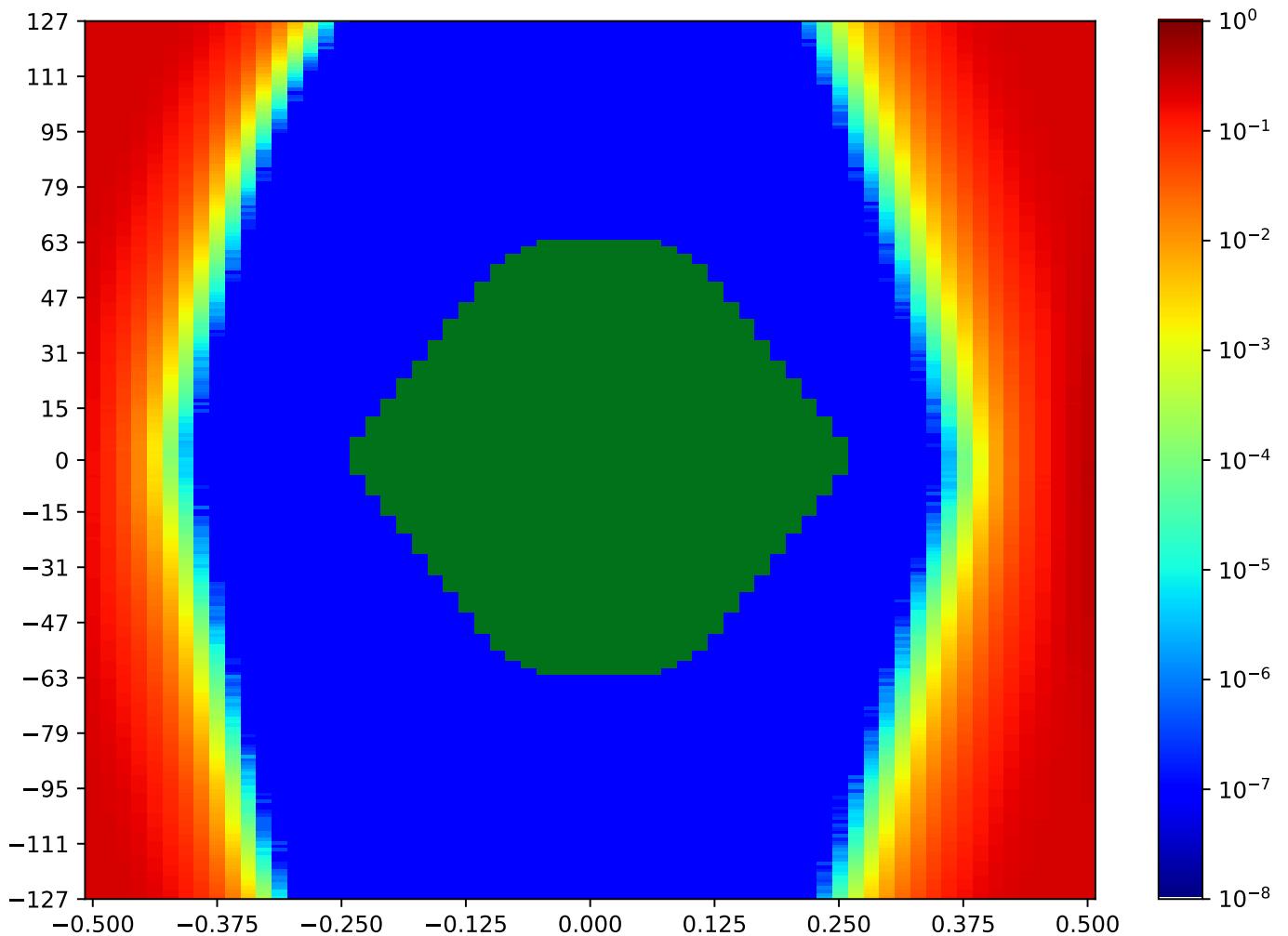


Figure 4.99: MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.2 MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

Table 4.91: MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:30:34		2018-Sep-26 18:31:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10005	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

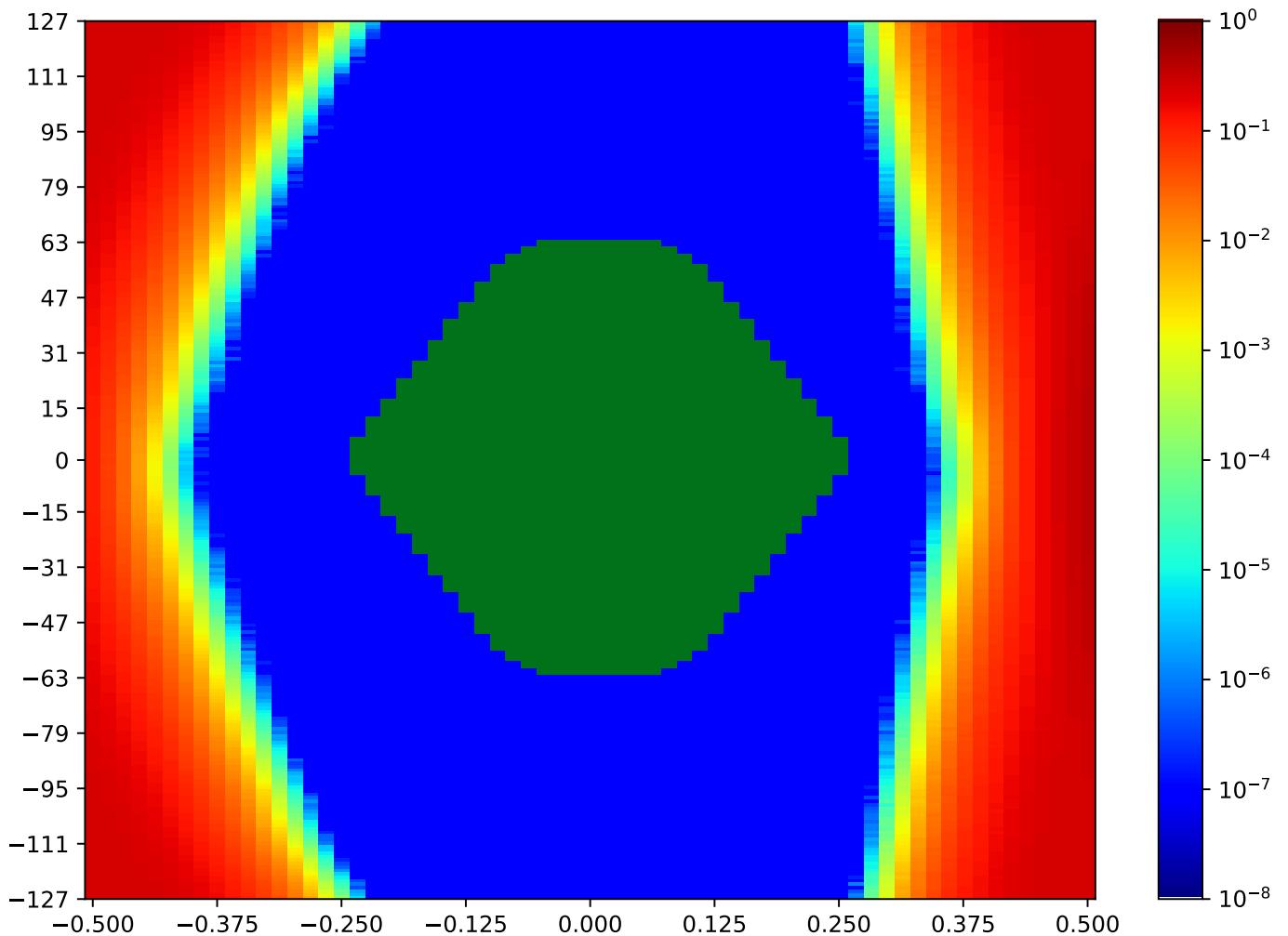


Figure 4.100: MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.3 MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

Table 4.92: MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:31:10		2018-Sep-26 18:31:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10876	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

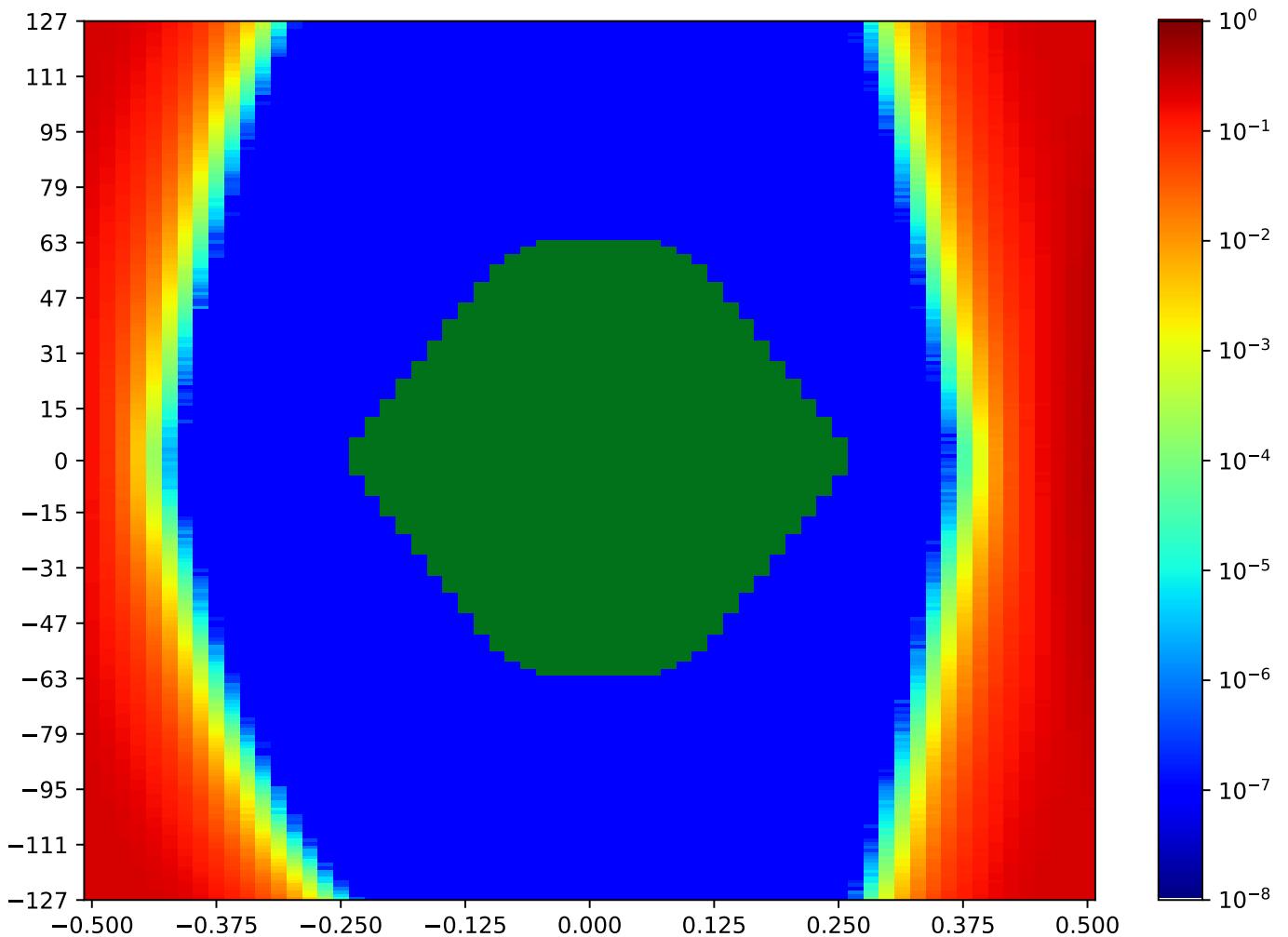


Figure 4.101: MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.4 MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

Table 4.93: MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:31:47		2018-Sep-26 18:32:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10389	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

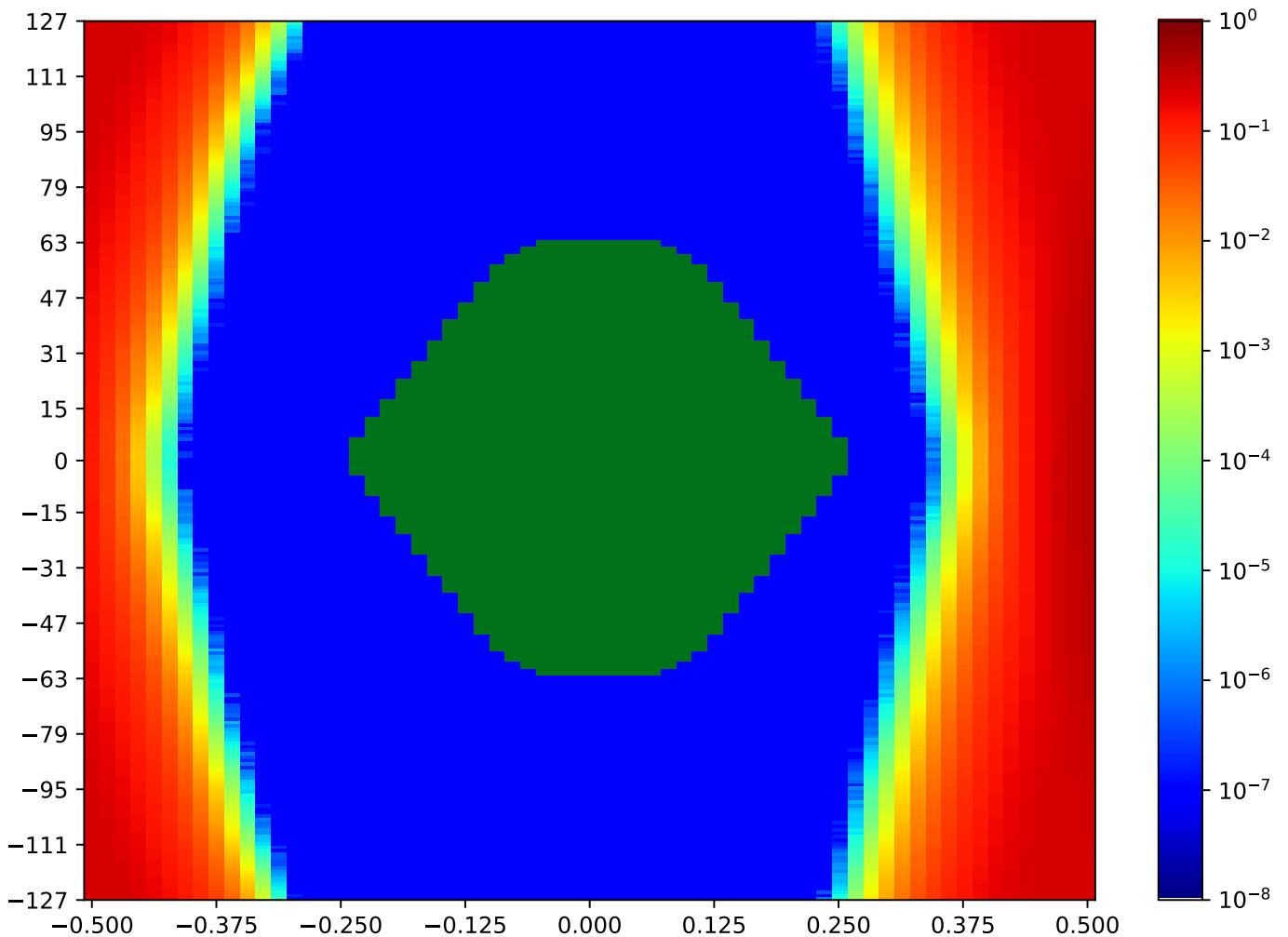


Figure 4.102: MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.5 MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

Table 4.94: MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:32:25		2018-Sep-26 18:33:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10376	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

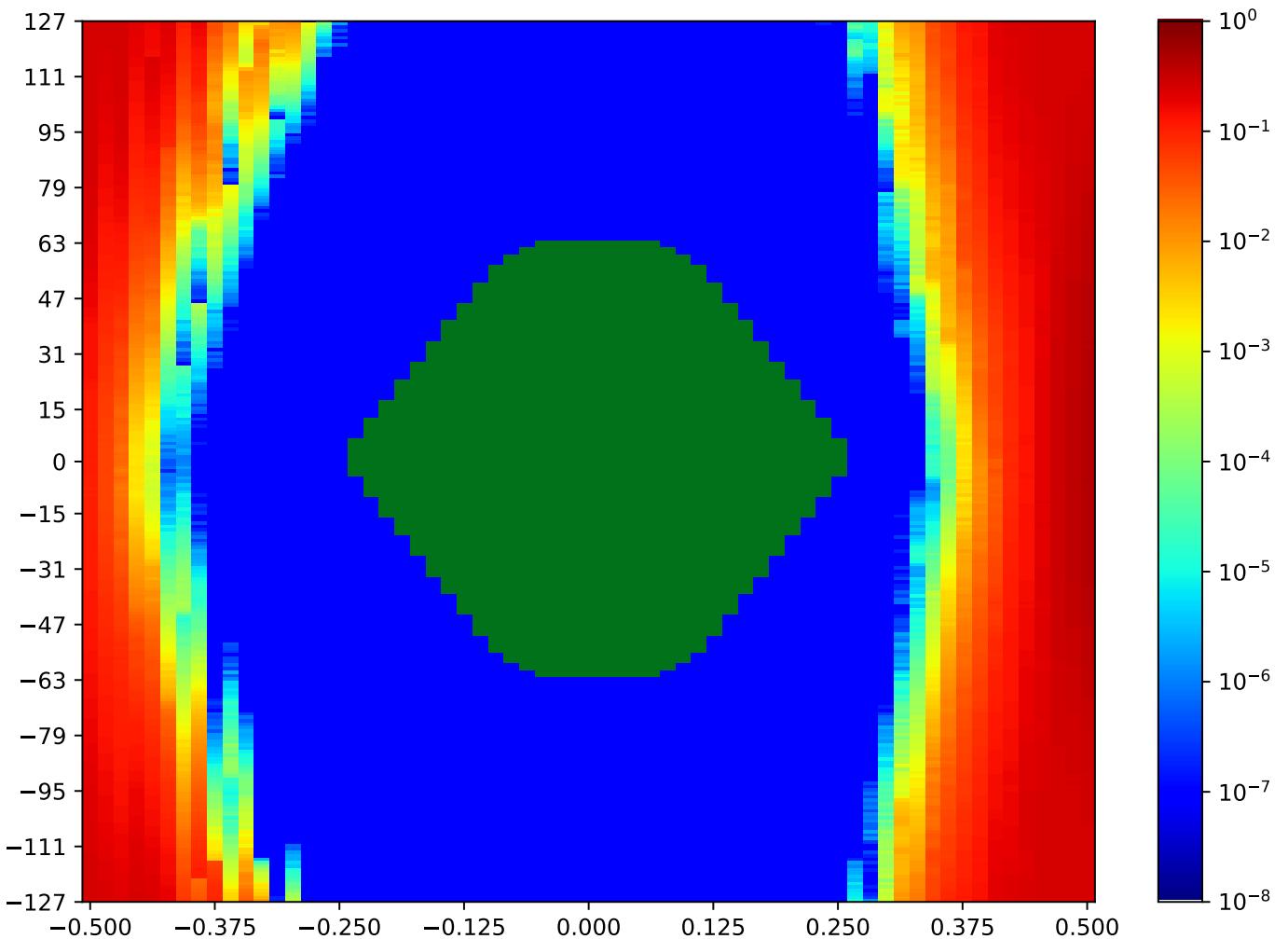


Figure 4.103: MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.6 MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

Table 4.95: MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:33:02		2018-Sep-26 18:33:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10708	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

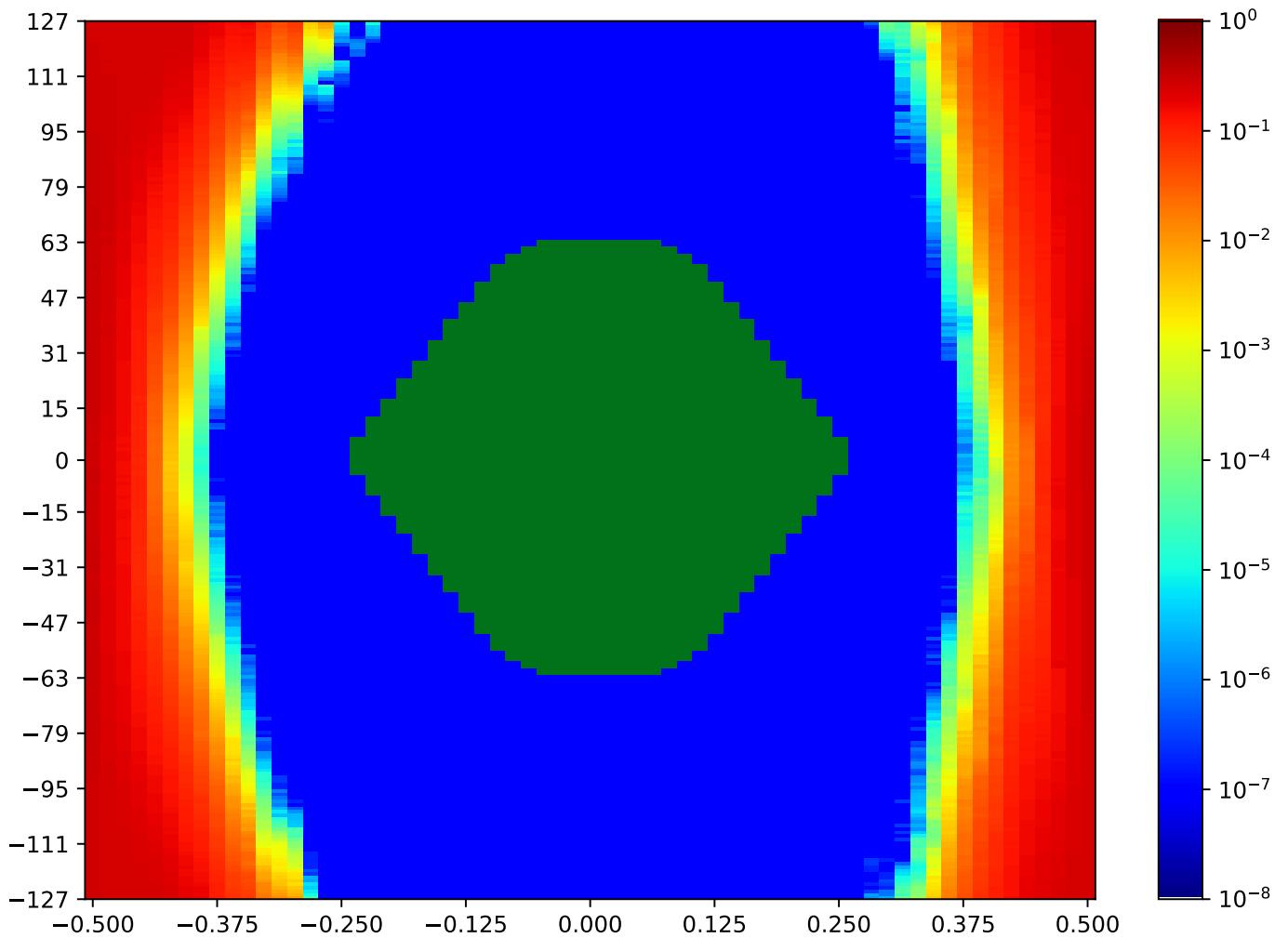


Figure 4.104: MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.7 MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

Table 4.96: MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:33:40		2018-Sep-26 18:34:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10391	48	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

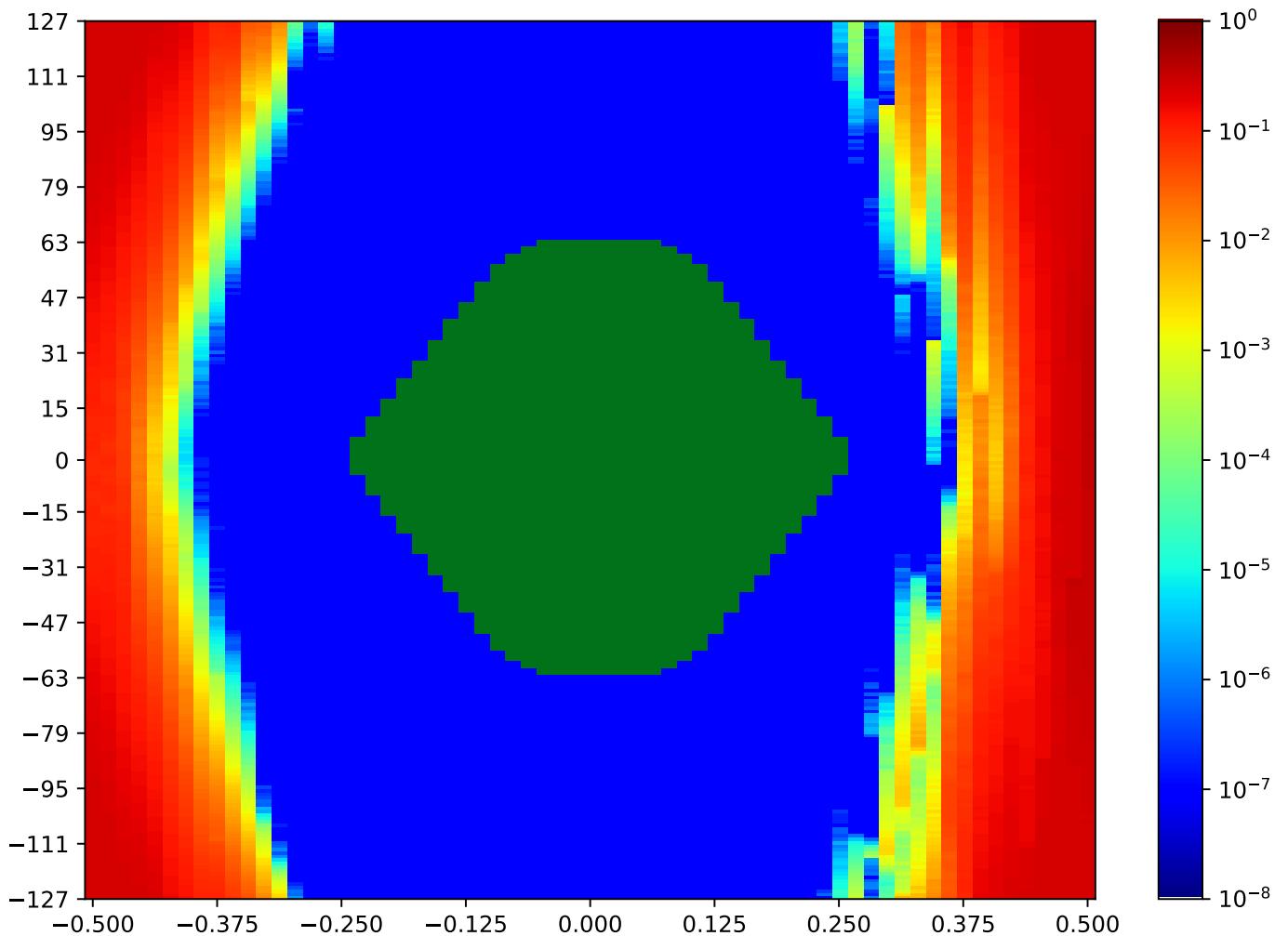


Figure 4.105: MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.8 MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

Table 4.97: MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:34:17		2018-Sep-26 18:34:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11218	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

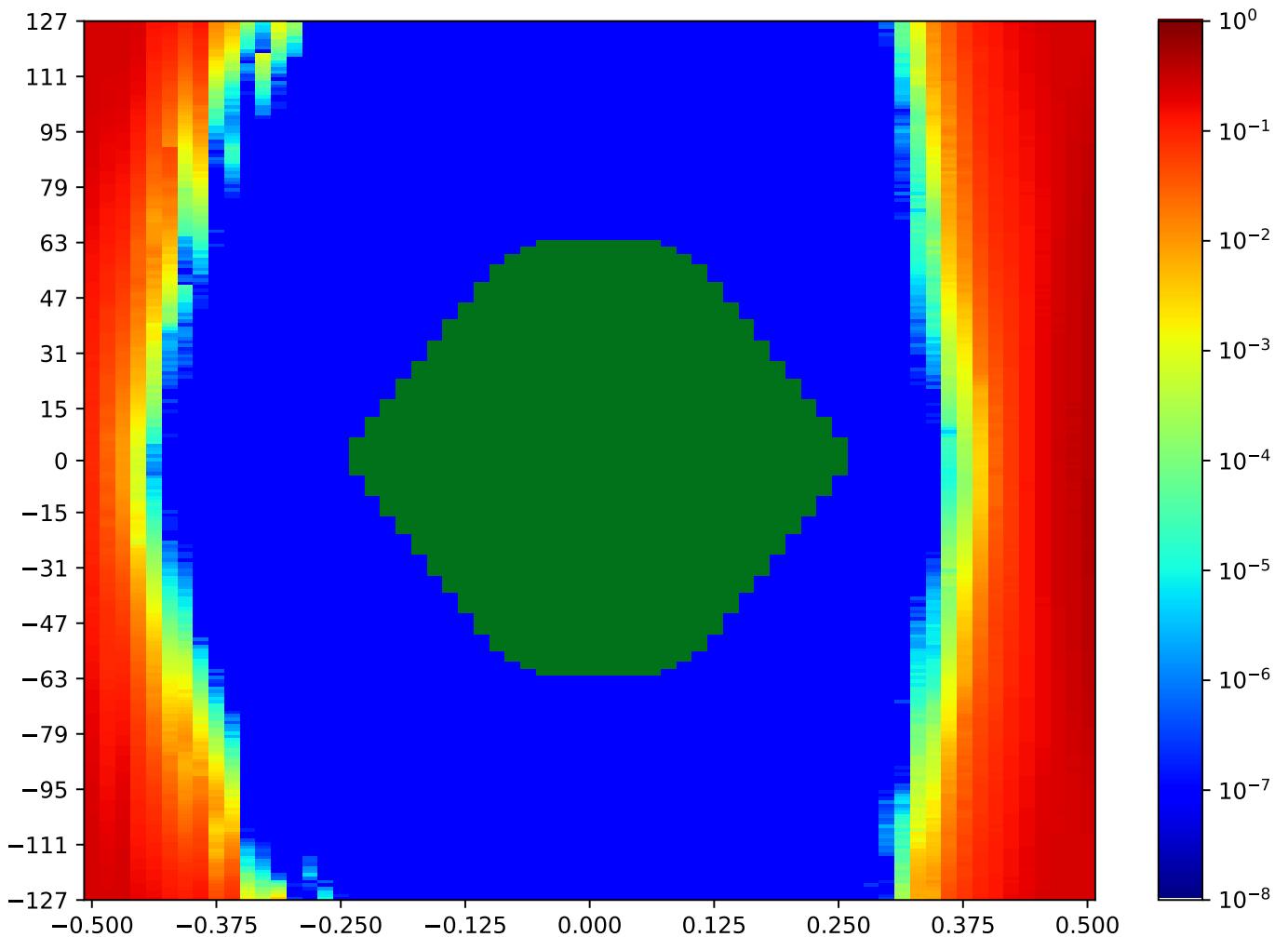


Figure 4.106: MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.9 MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

Table 4.98: MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:34:54		2018-Sep-26 18:35:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10998	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

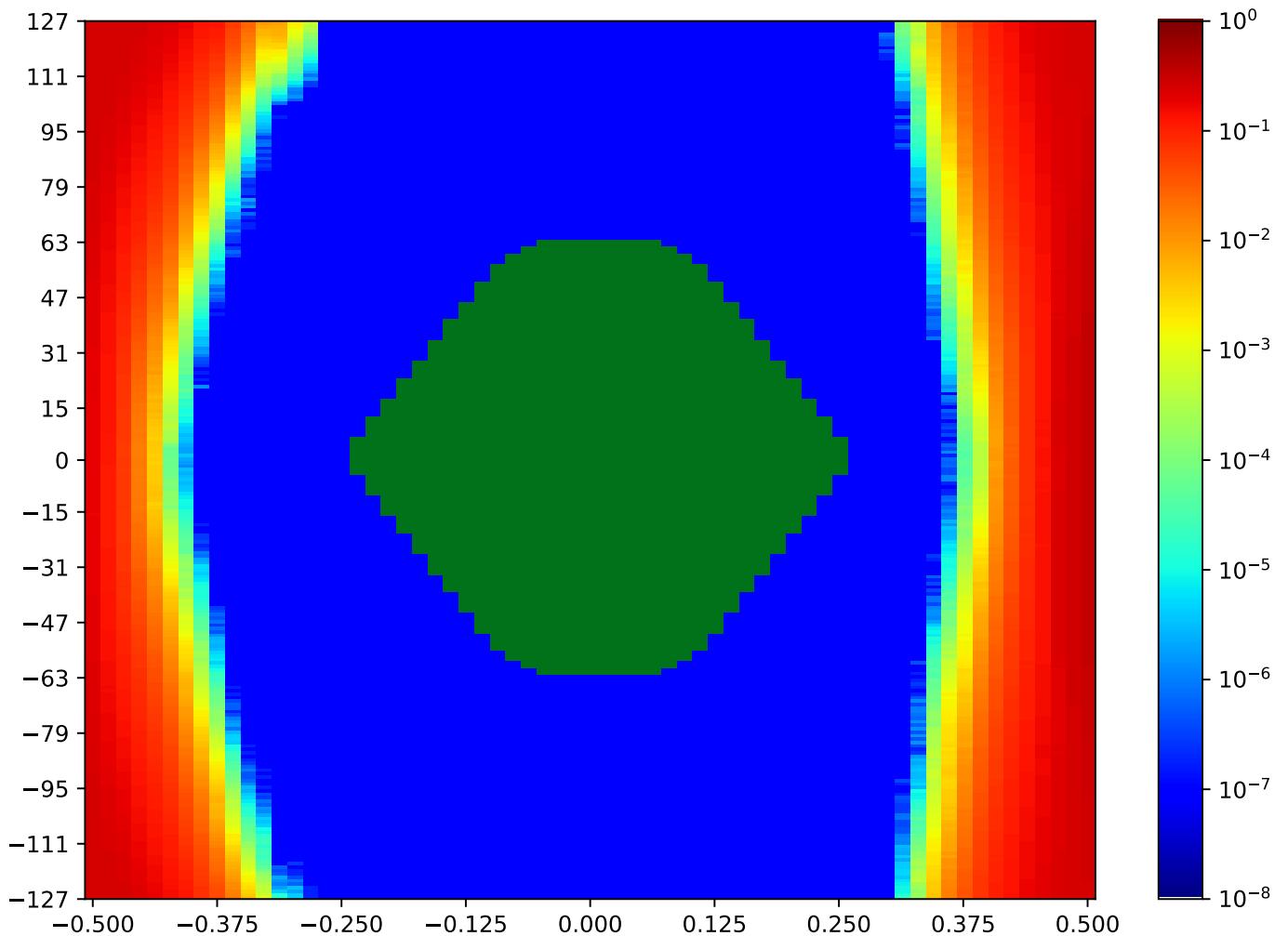


Figure 4.107: MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.10 MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

Table 4.99: MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:35:32		2018-Sep-26 18:36:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10978	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

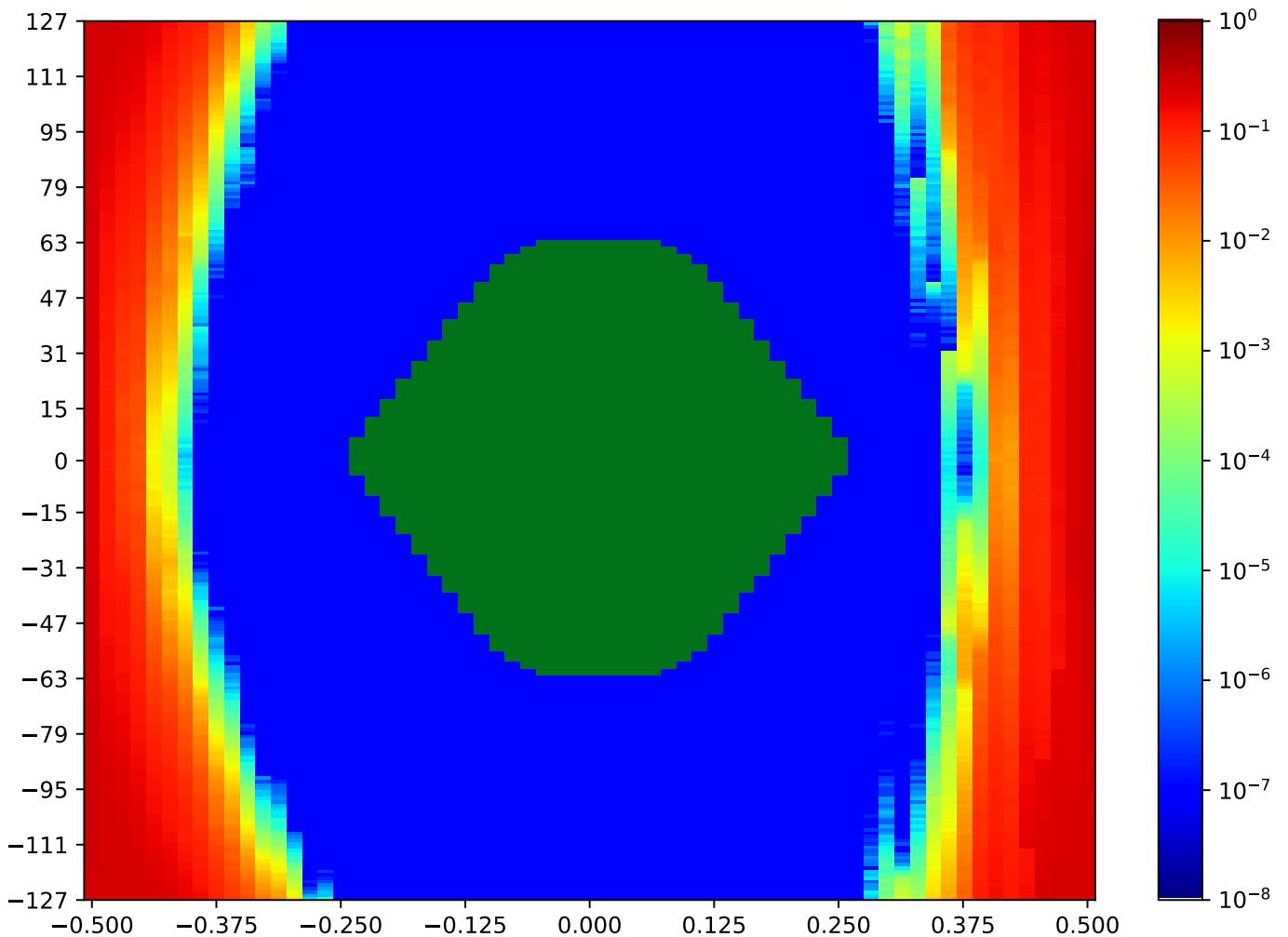


Figure 4.108: MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.11 MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

Table 4.100: MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:36:09		2018-Sep-26 18:36:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10700	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

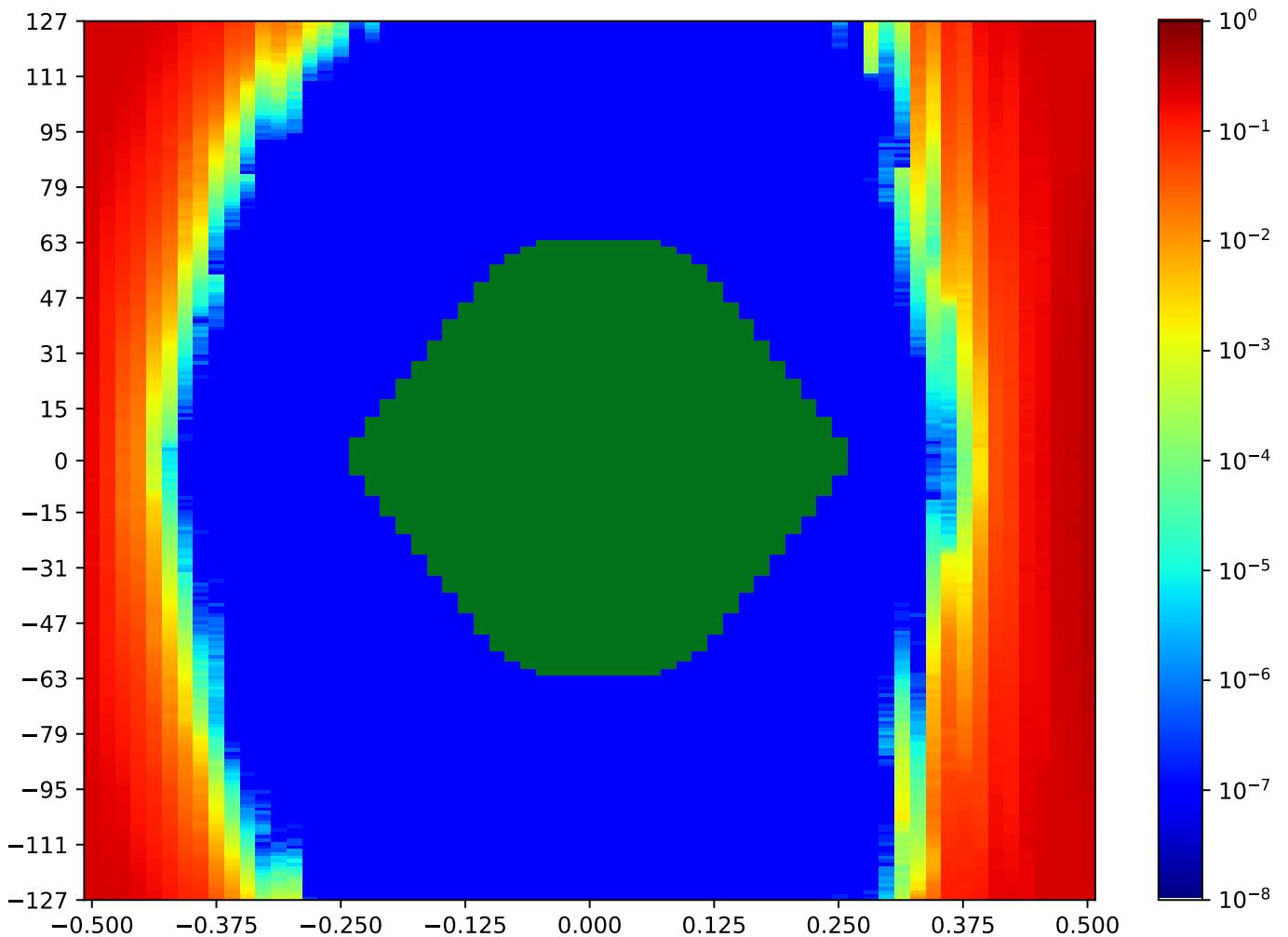


Figure 4.109: MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.12 MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

Table 4.101: MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:36:47		2018-Sep-26 18:37:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11002	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

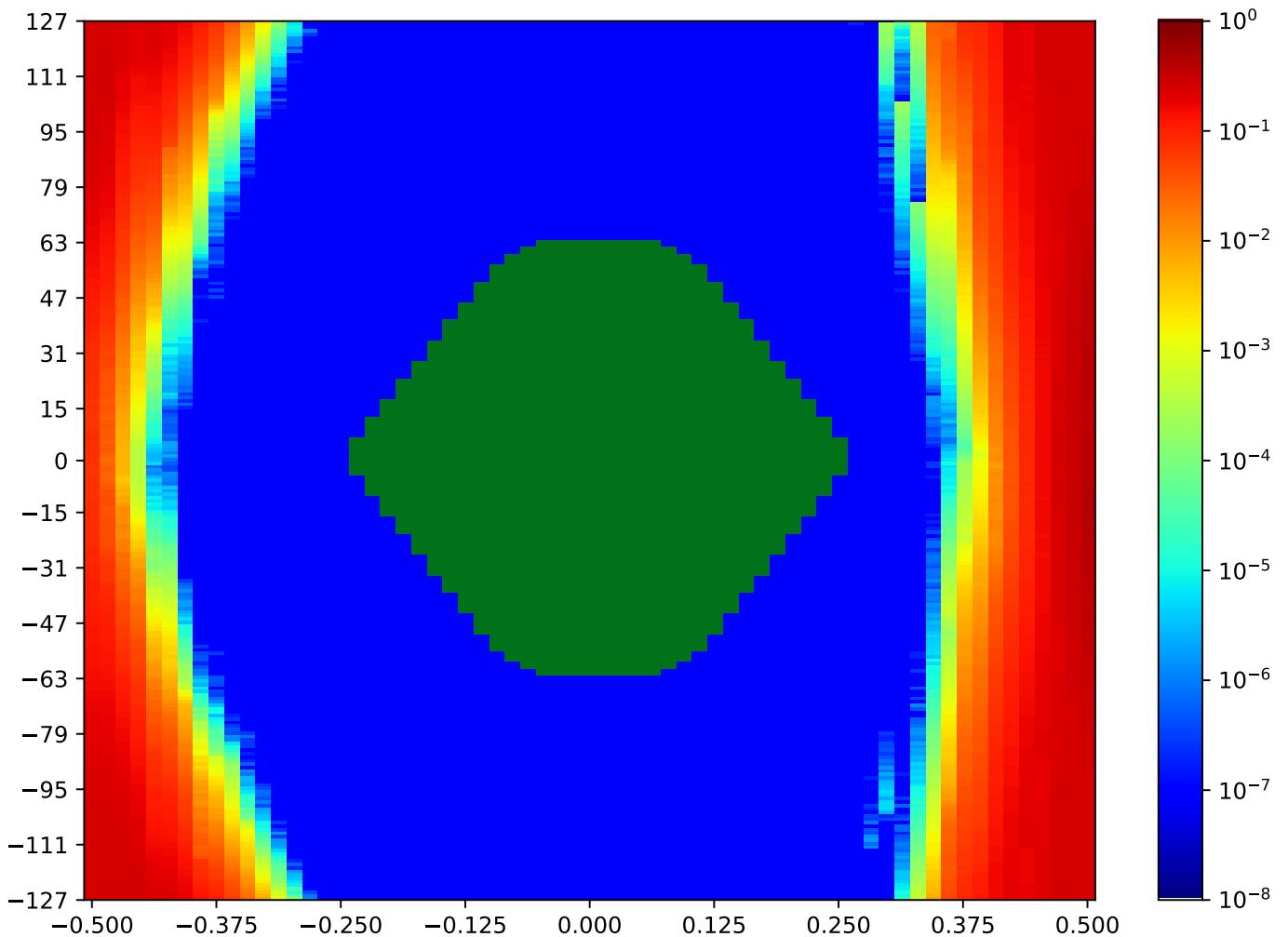


Figure 4.110: MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.13 MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

Table 4.102: MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:37:24		2018-Sep-26 18:38:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11112	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

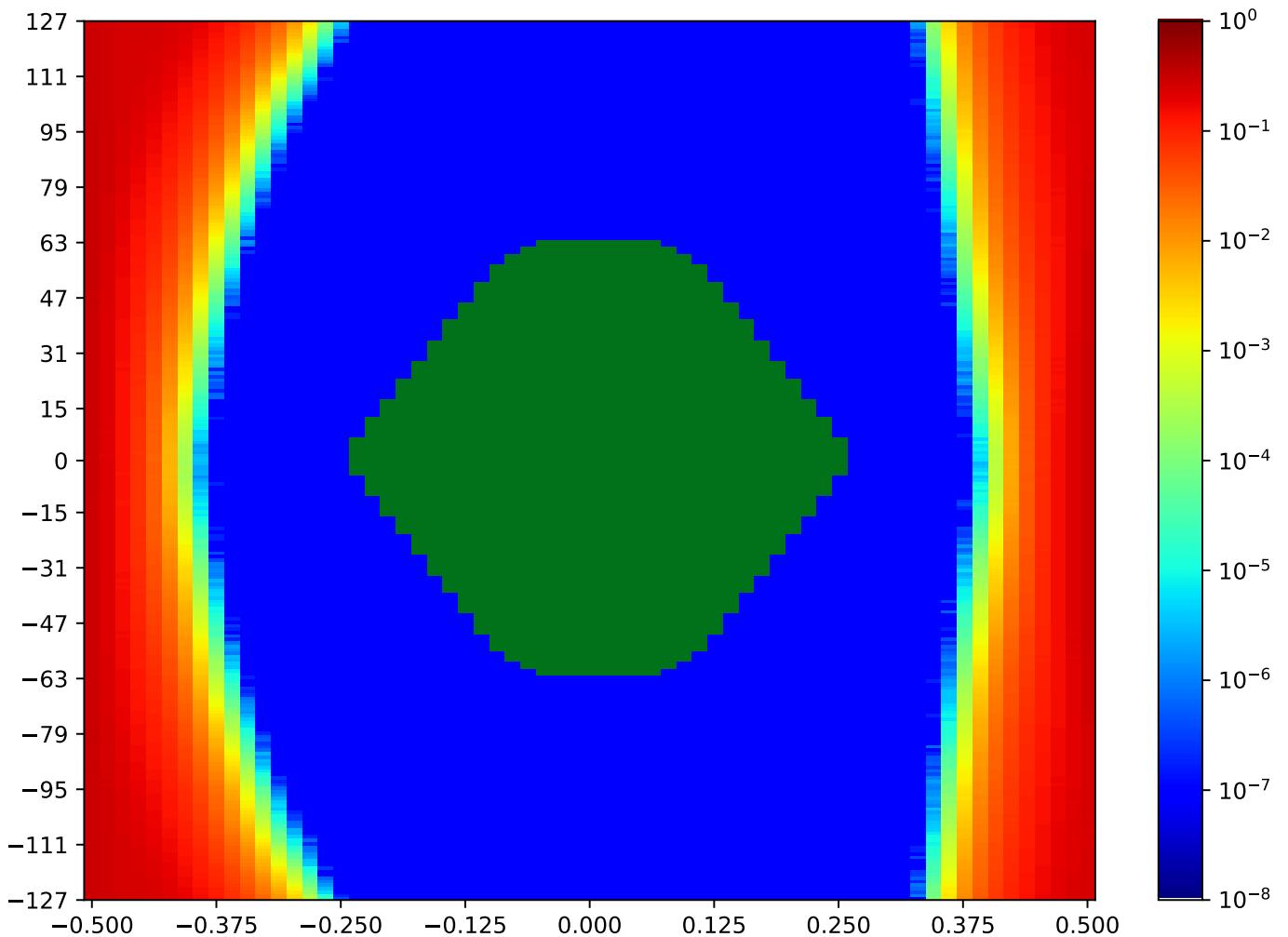


Figure 4.111: MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.14 MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

Table 4.103: MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:38:01		2018-Sep-26 18:38:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10808	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

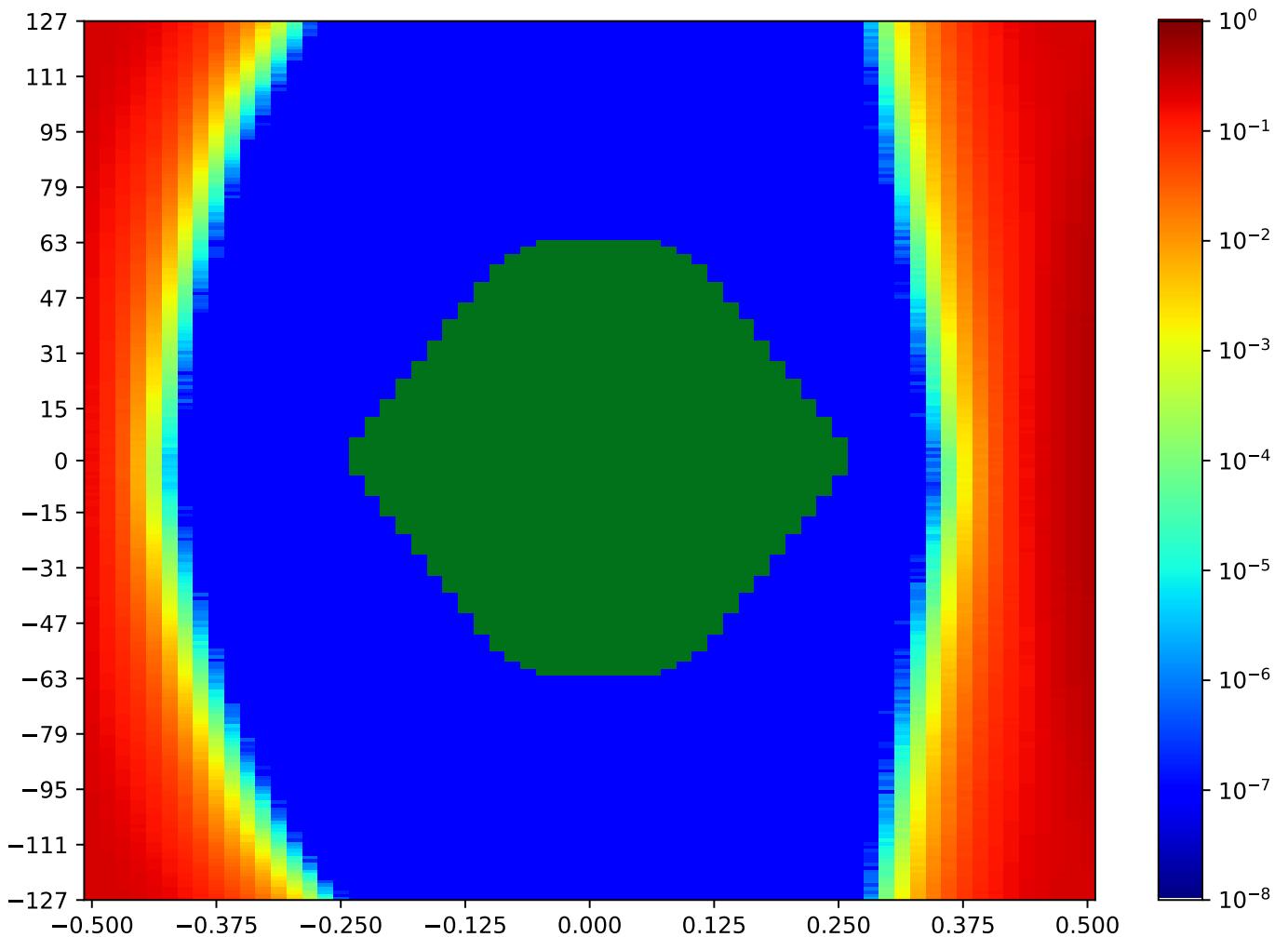


Figure 4.112: MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.15 MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

Table 4.104: MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:38:39		2018-Sep-26 18:39:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10801	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

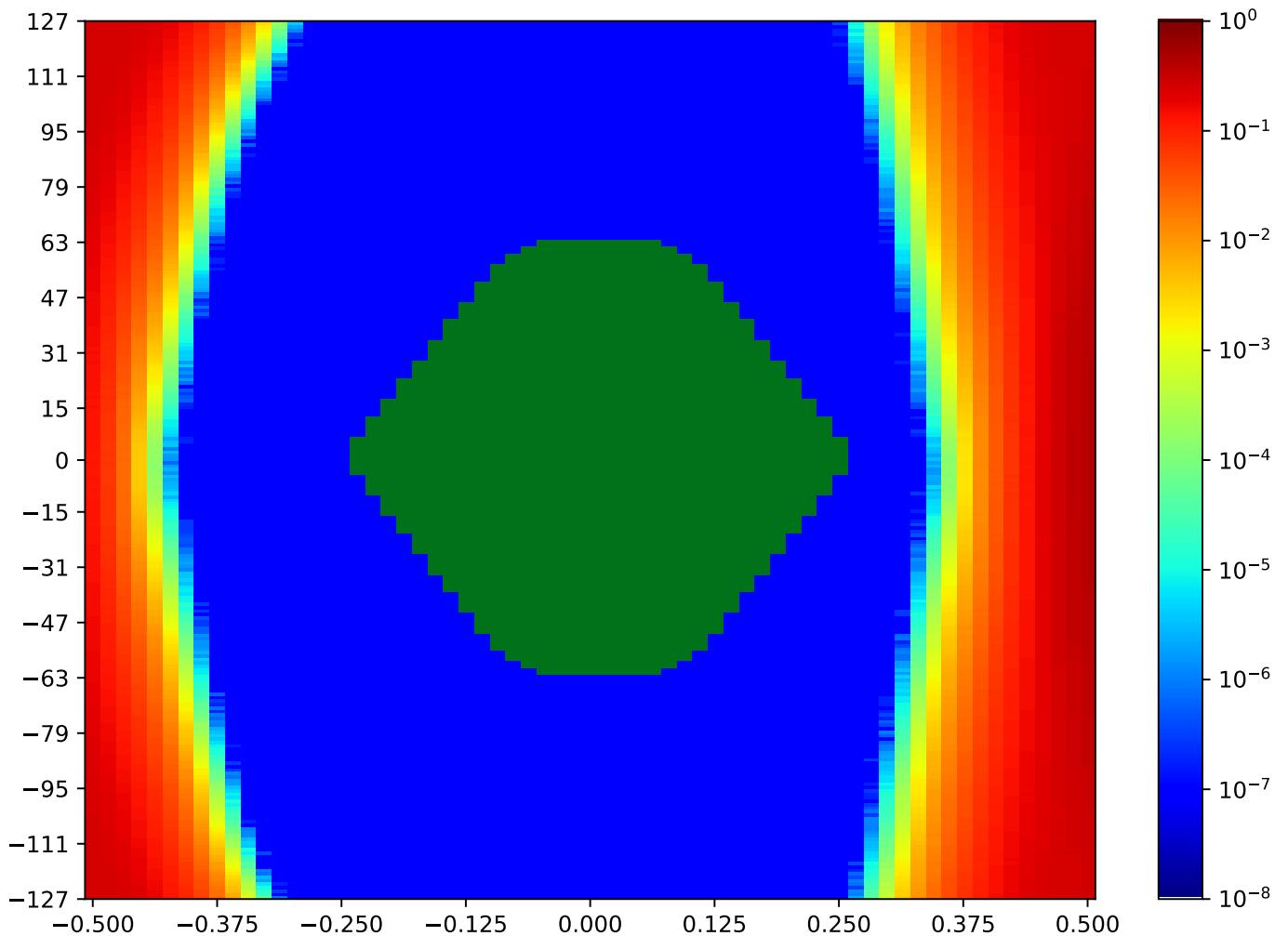


Figure 4.113: MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.16 MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

Table 4.105: MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:39:16		2018-Sep-26 18:39:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11215	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

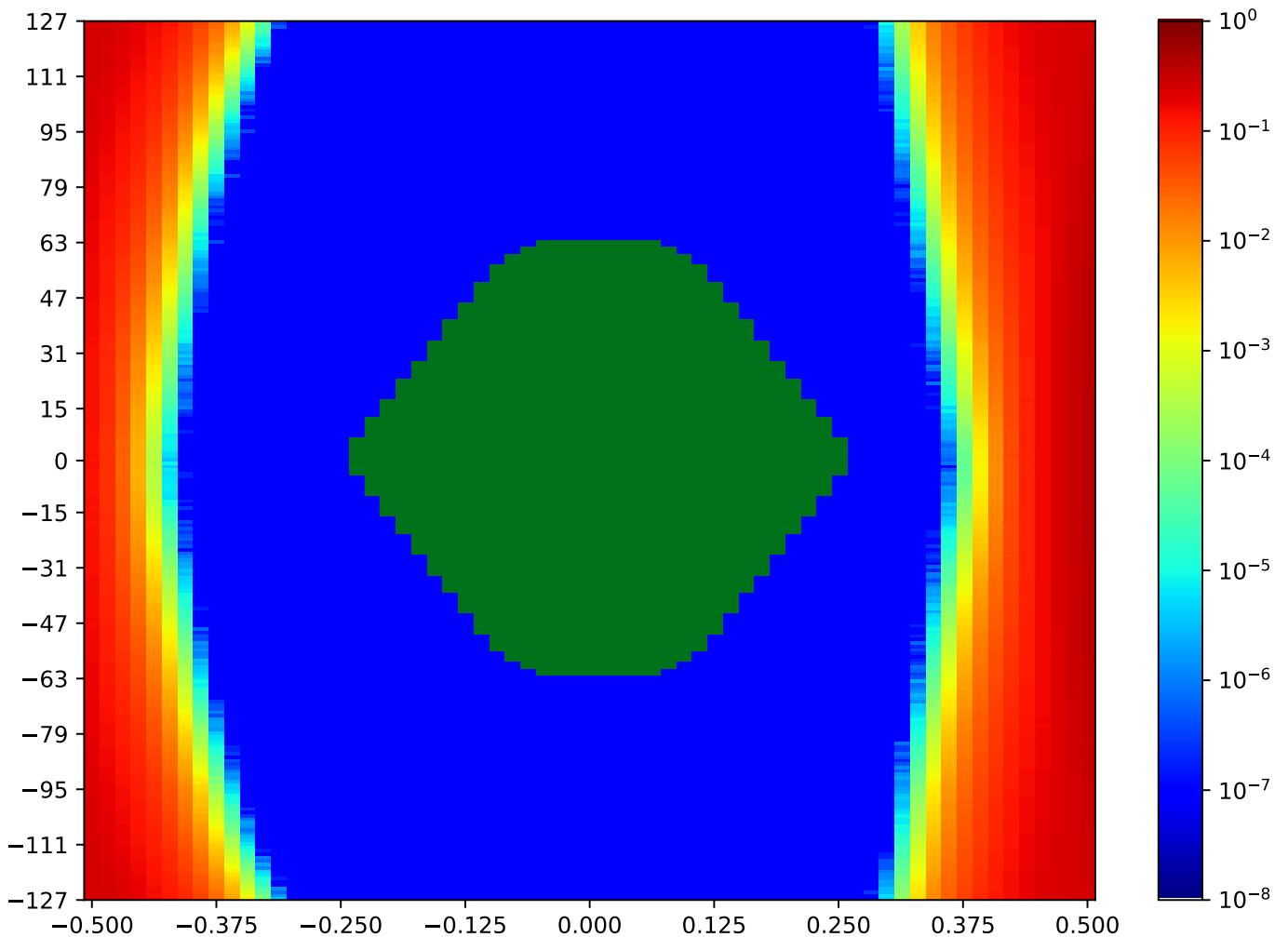


Figure 4.114: MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.17 MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

Table 4.106: MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:39:54		2018-Sep-26 18:40:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9975	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

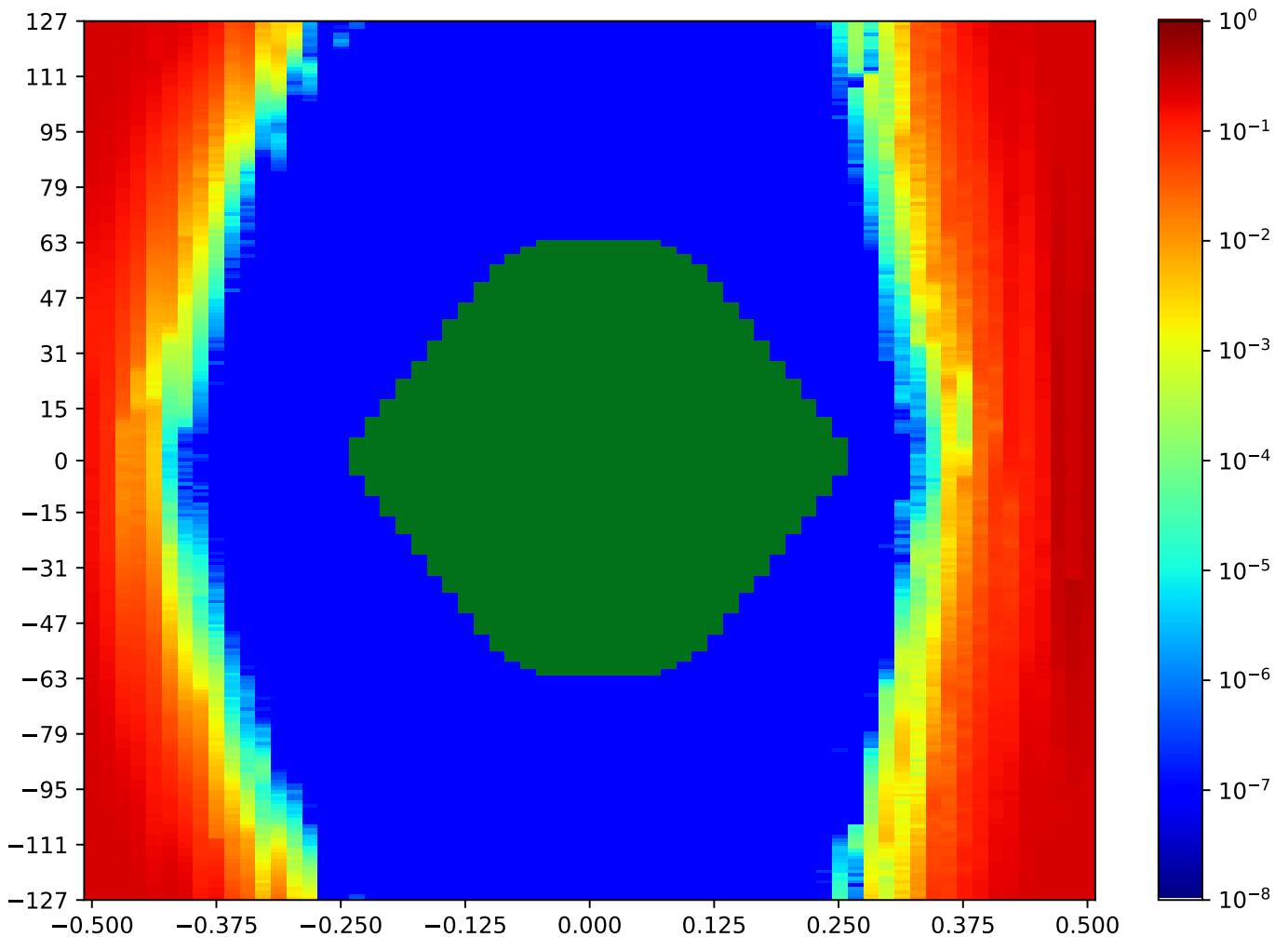


Figure 4.115: MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.18 MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

Table 4.107: MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:40:30		2018-Sep-26 18:41:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10660	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

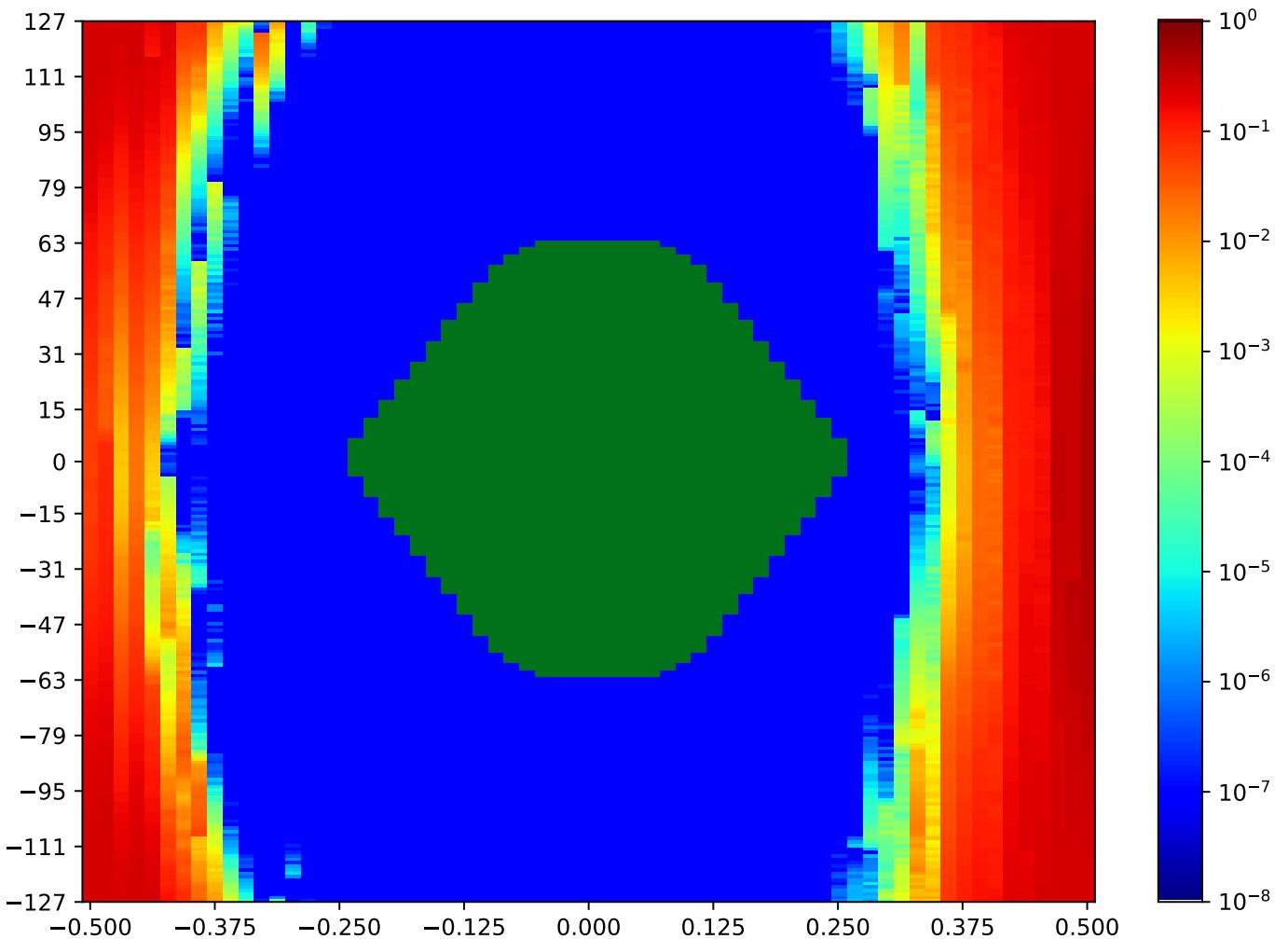


Figure 4.116: MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.19 MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

Table 4.108: MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:41:08		2018-Sep-26 18:41:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10995	49	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

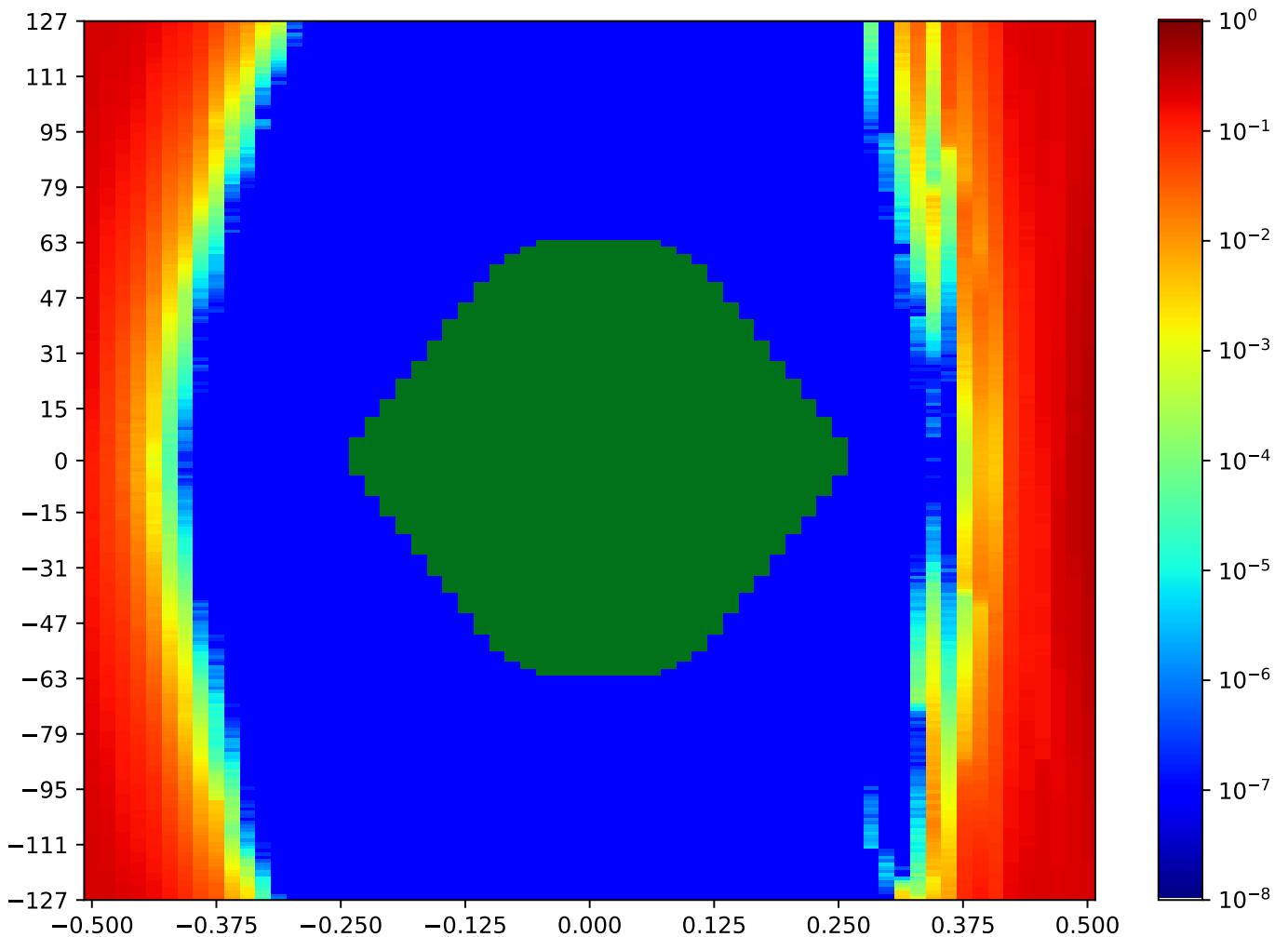


Figure 4.117: MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.20 MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

Table 4.109: MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:41:45		2018-Sep-26 18:42:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10488	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

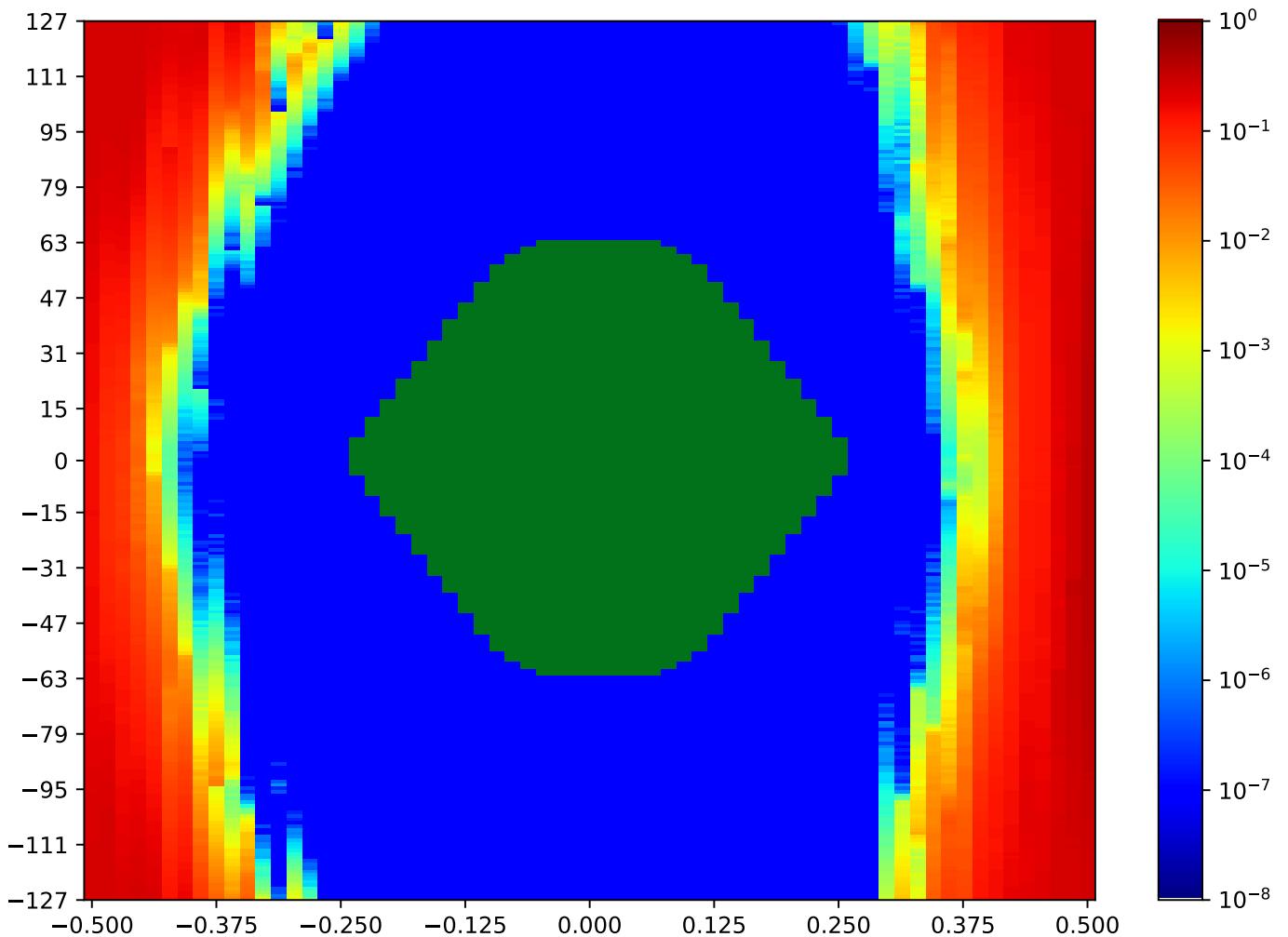


Figure 4.118: MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.21 MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

Table 4.110: MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:42:23		2018-Sep-26 18:43:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10524	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

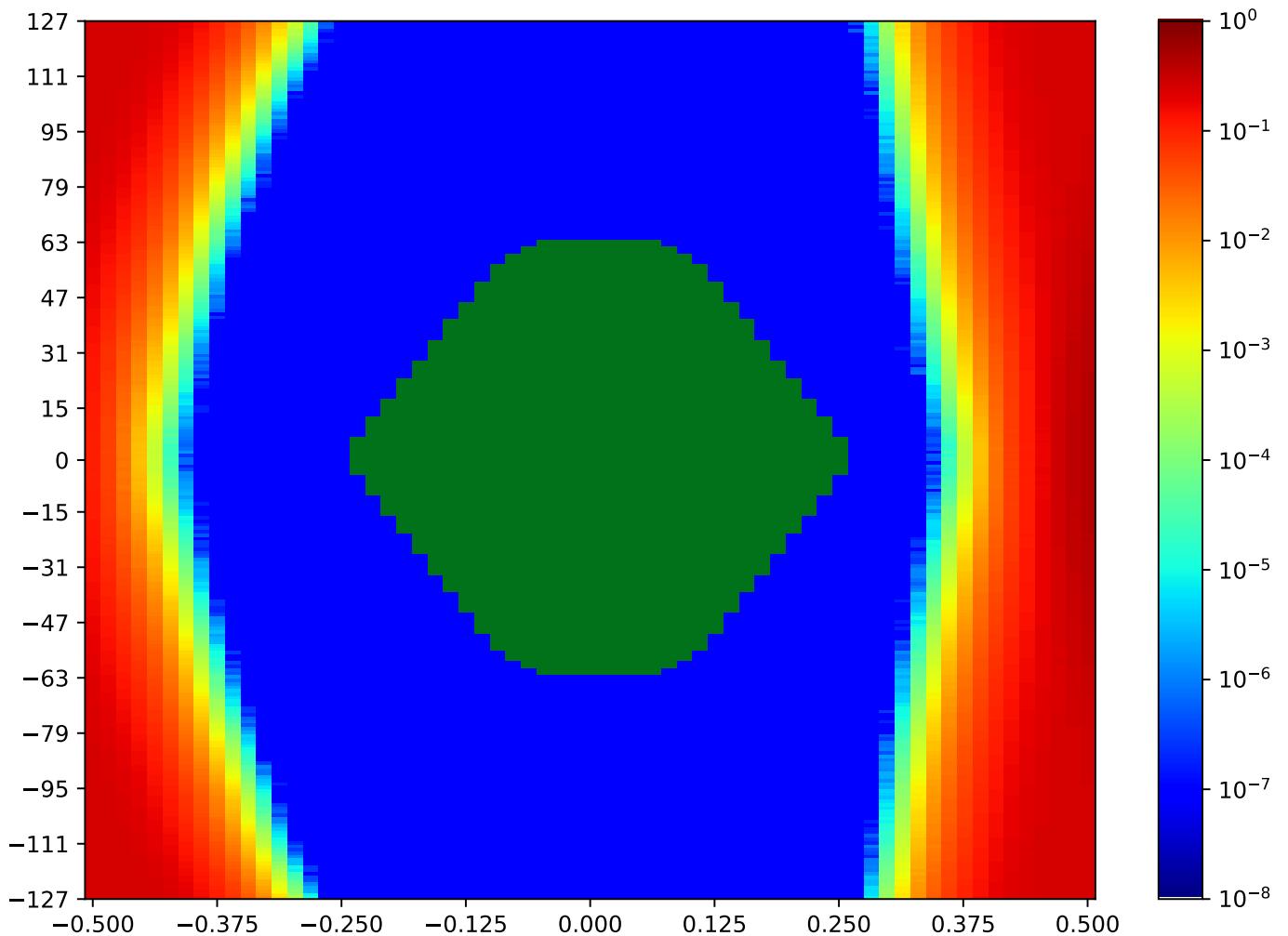


Figure 4.119: MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.22 MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

Table 4.111: MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:43:00		2018-Sep-26 18:43:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11315	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

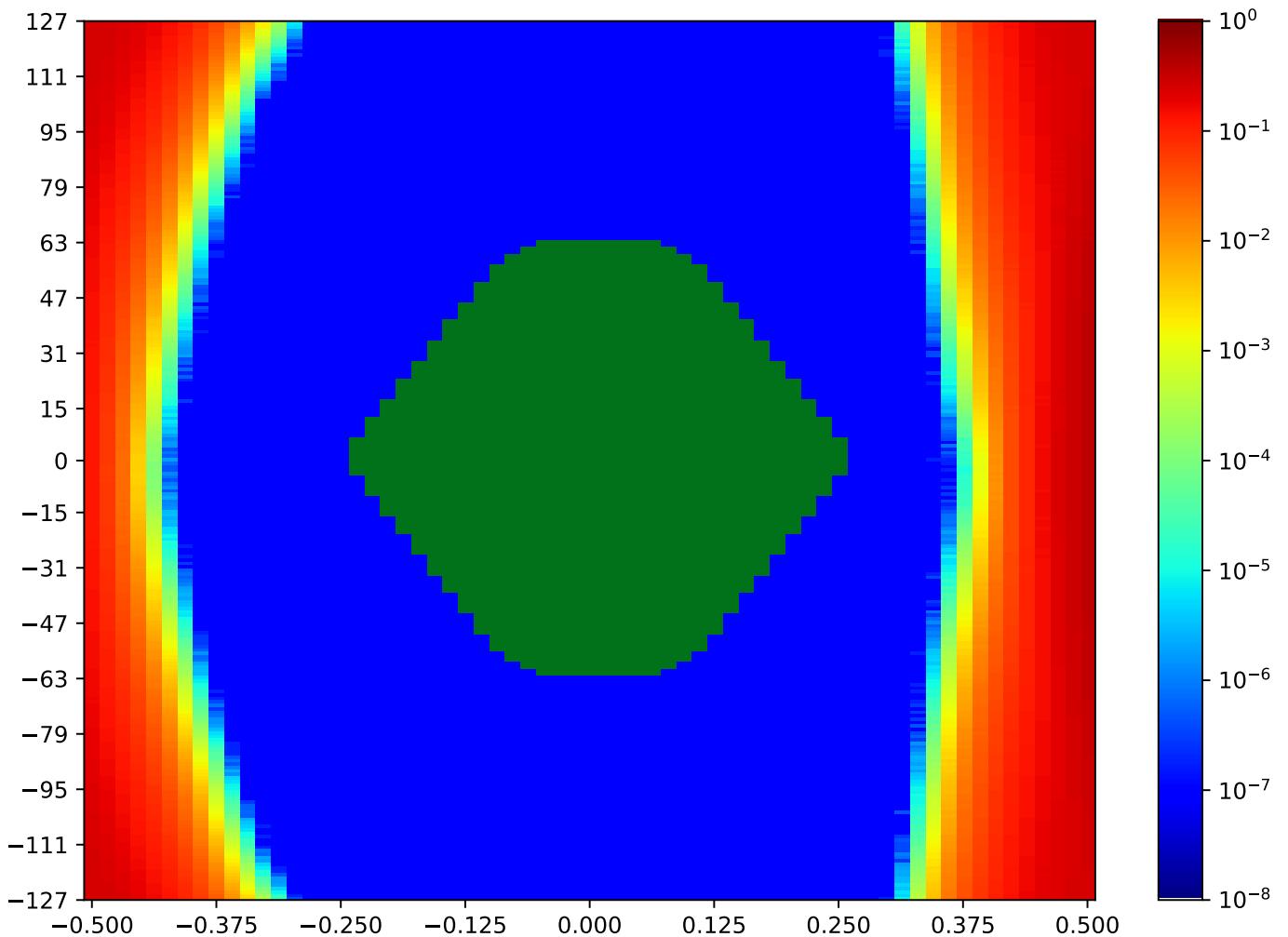


Figure 4.120: MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.23 MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

Table 4.112: MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:43:38		2018-Sep-26 18:44:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10523	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

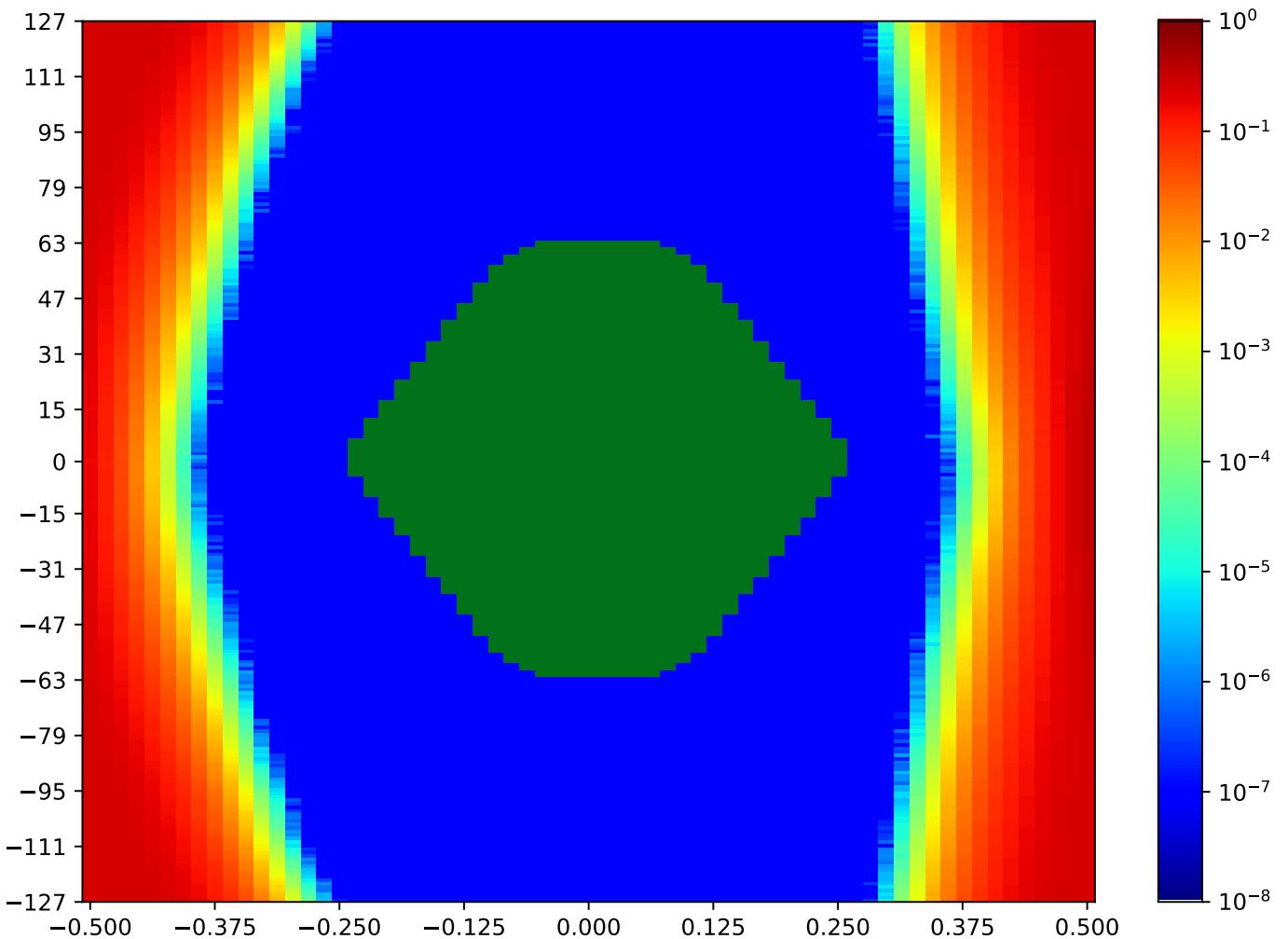


Figure 4.121: MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.24 MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

Table 4.113: MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:44:15		2018-Sep-26 18:44:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10607	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

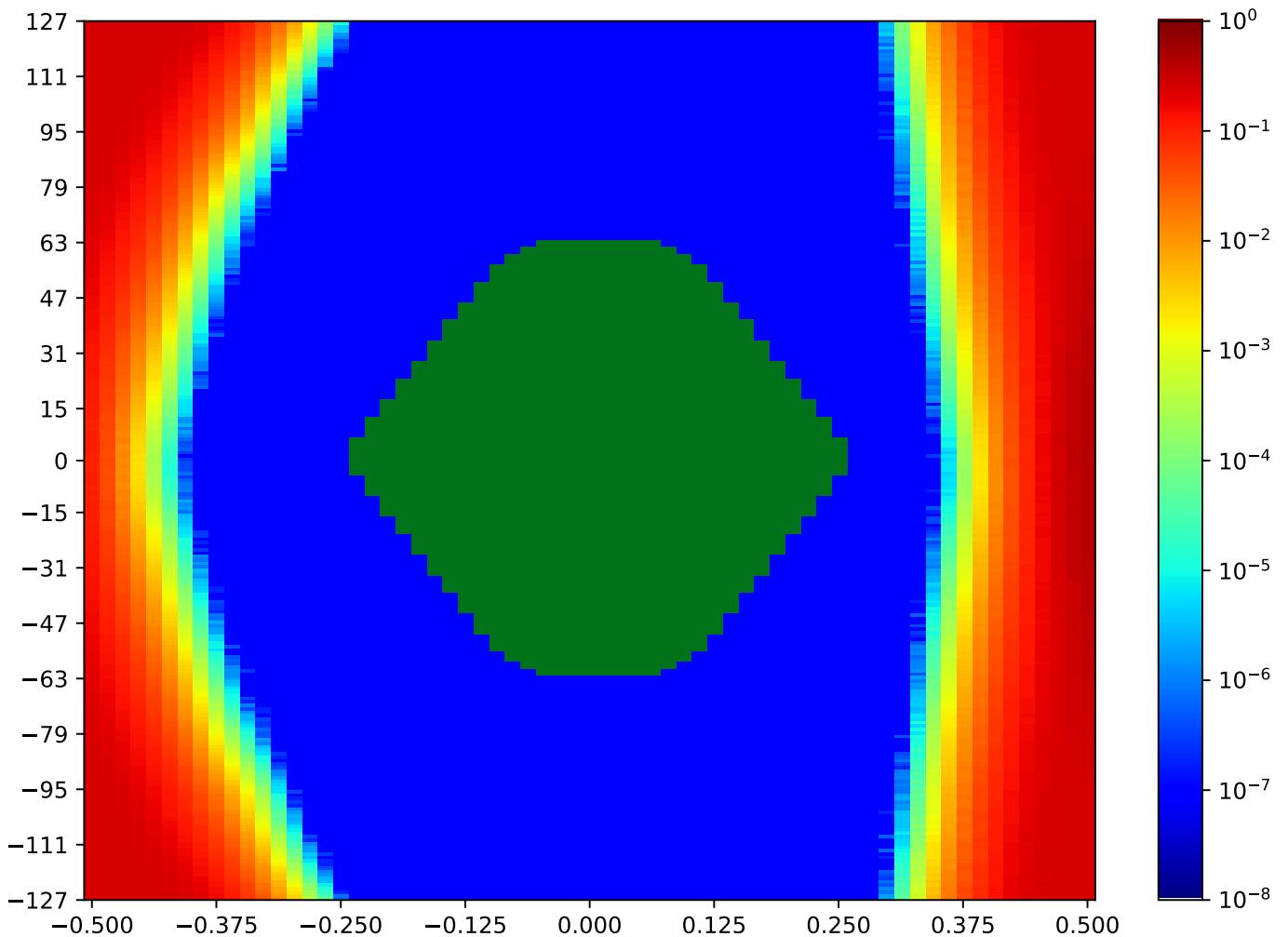


Figure 4.122: MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.25 MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

Table 4.114: MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:44:53		2018-Sep-26 18:45:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10903	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

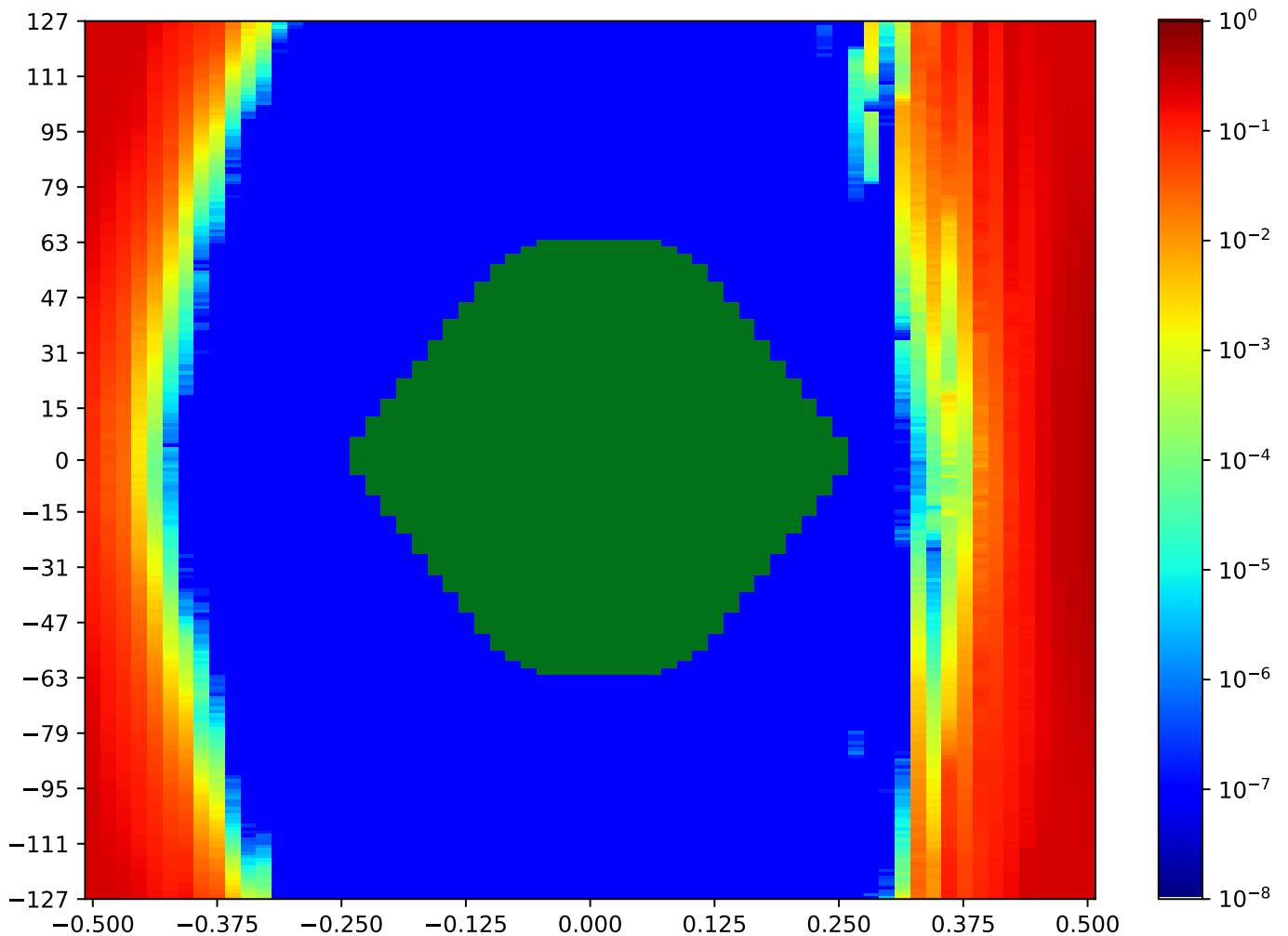


Figure 4.123: MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.26 MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

Table 4.115: MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:45:30		2018-Sep-26 18:46:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11082	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

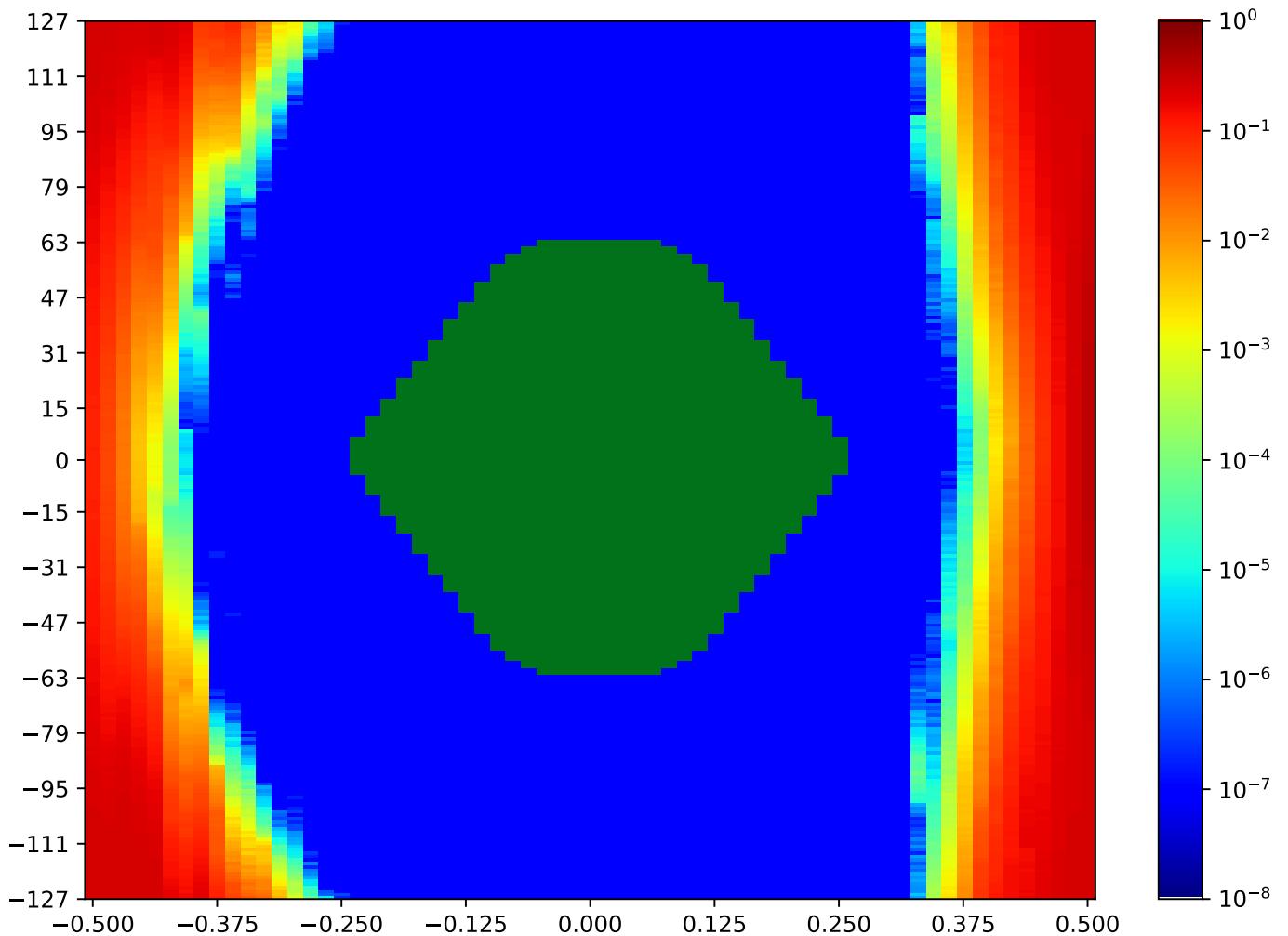


Figure 4.124: MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.27 MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

Table 4.116: MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:46:08		2018-Sep-26 18:46:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	11147	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

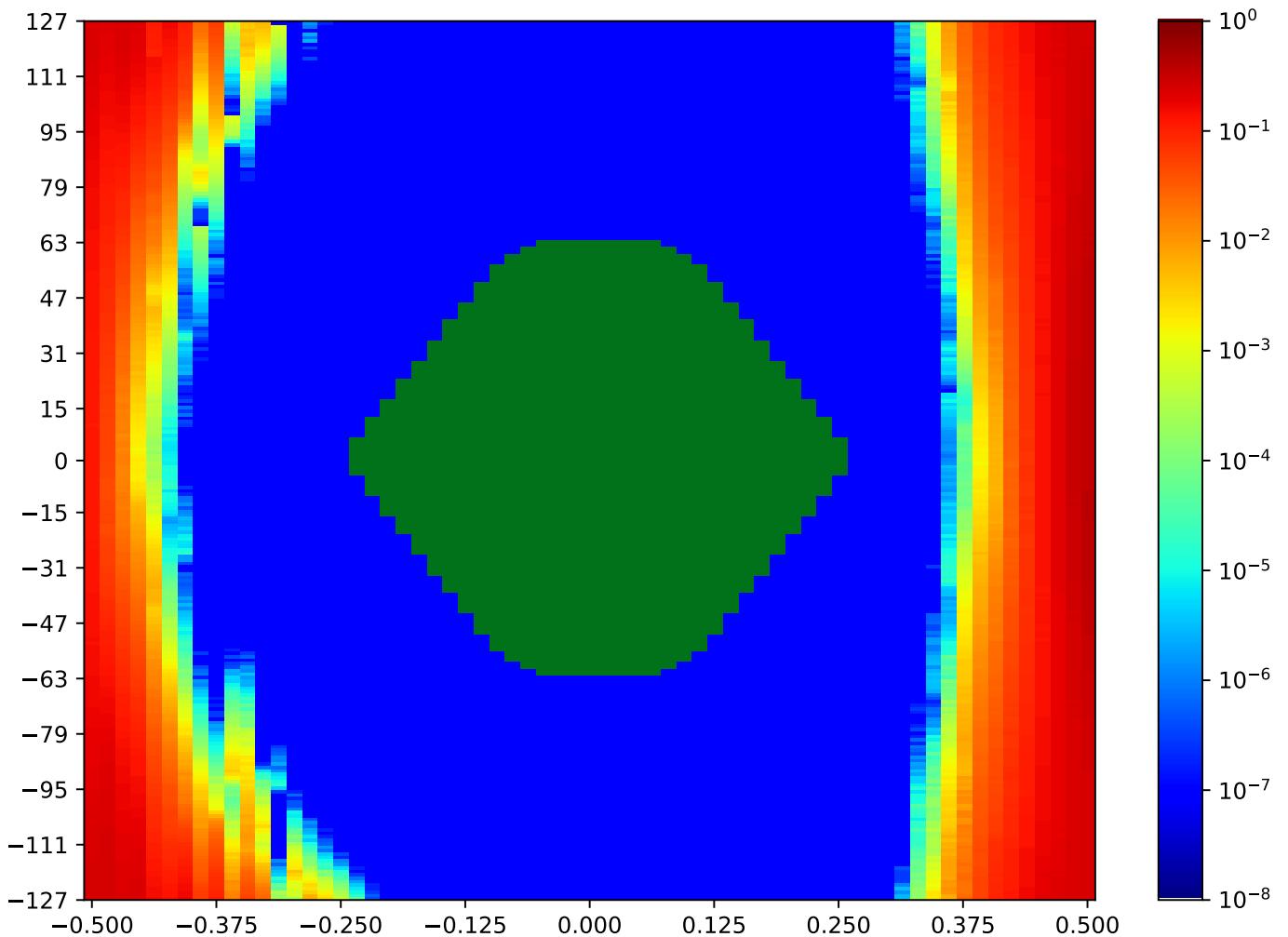


Figure 4.125: MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.9.28 MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

Table 4.117: MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-26 18:46:45		2018-Sep-26 18:47:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10693	48	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

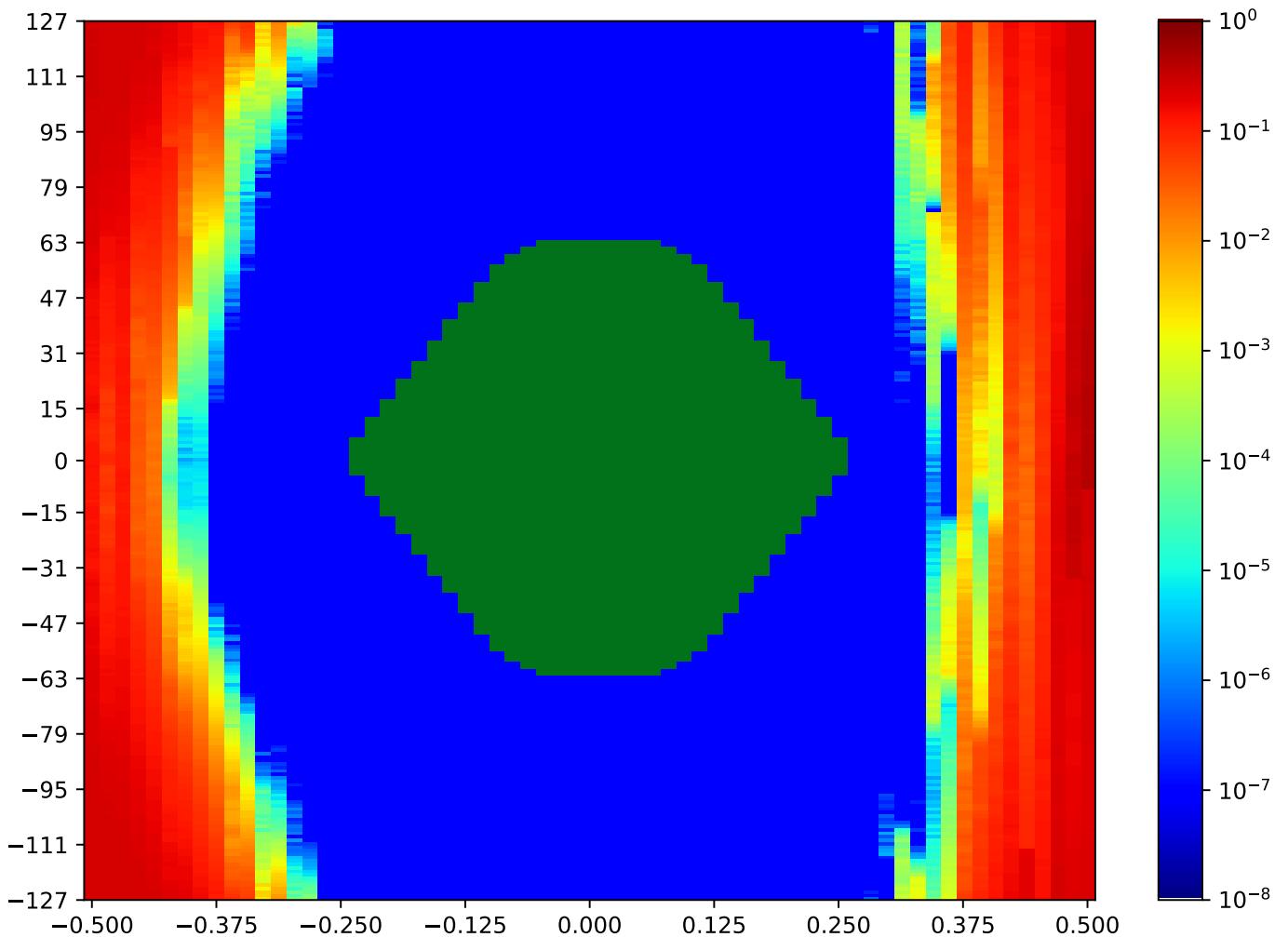


Figure 4.126: MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

Call back to summary Figure 4.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.10 MSP_A TX1 MSP_C RX17 Minipod Loopback

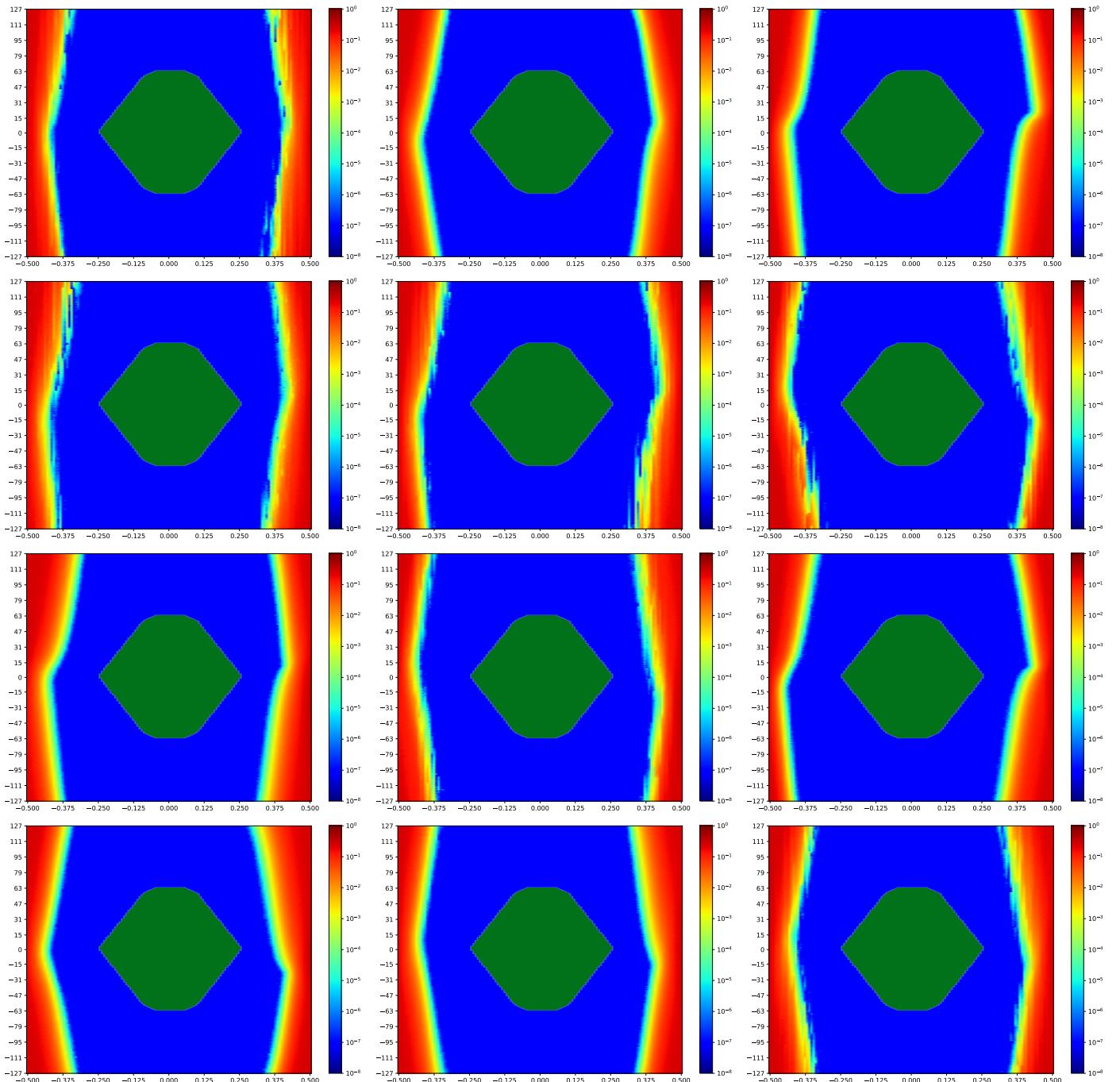


Figure 4.127: MSP_A TX1 MSP_C RX17 Minipod Loopback

A cross-reference to Figure 4.127. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.140.

4.10.1 MSP_A_FPGA-TX1-00-RX17-00-MSP_C_FPGA

Table 4.118: MSP_A_FPGA-TX1-00-RX17-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:55:55		2018-Sep-26 18:57:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24022	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x00009 SVN: 16356	

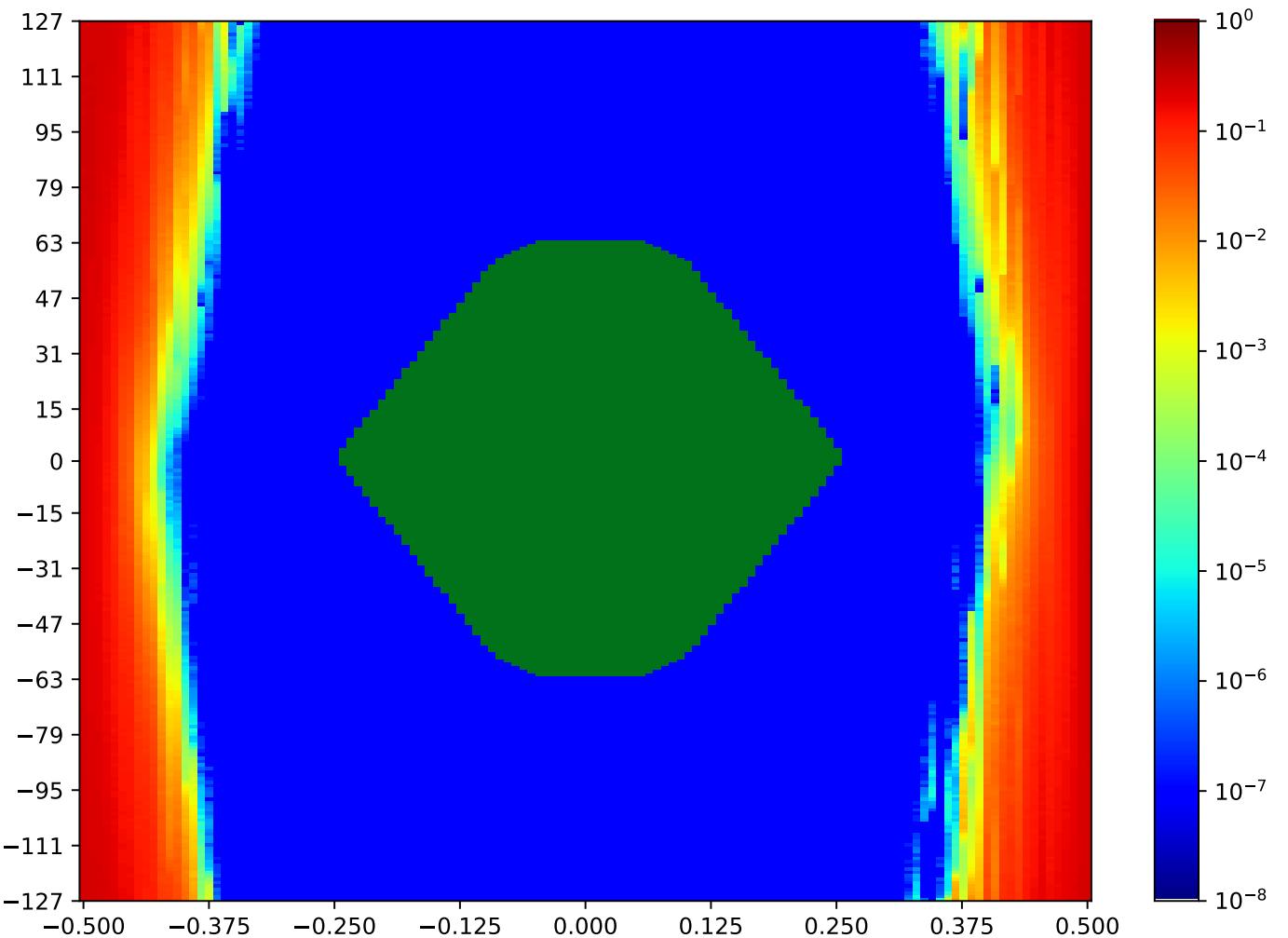


Figure 4.128: MSP_A_FPGA-TX1-00-RX17-00-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.2 MSP_A_FPGA-TX1-01-RX17-01-MSP_C_FPGA

Table 4.119: MSP_A_FPGA-TX1-01-RX17-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:58:21		2018-Sep-26 18:59:34	
Reset RX	OA	HO		VO	VO (%)
true	23067	98		75.97%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

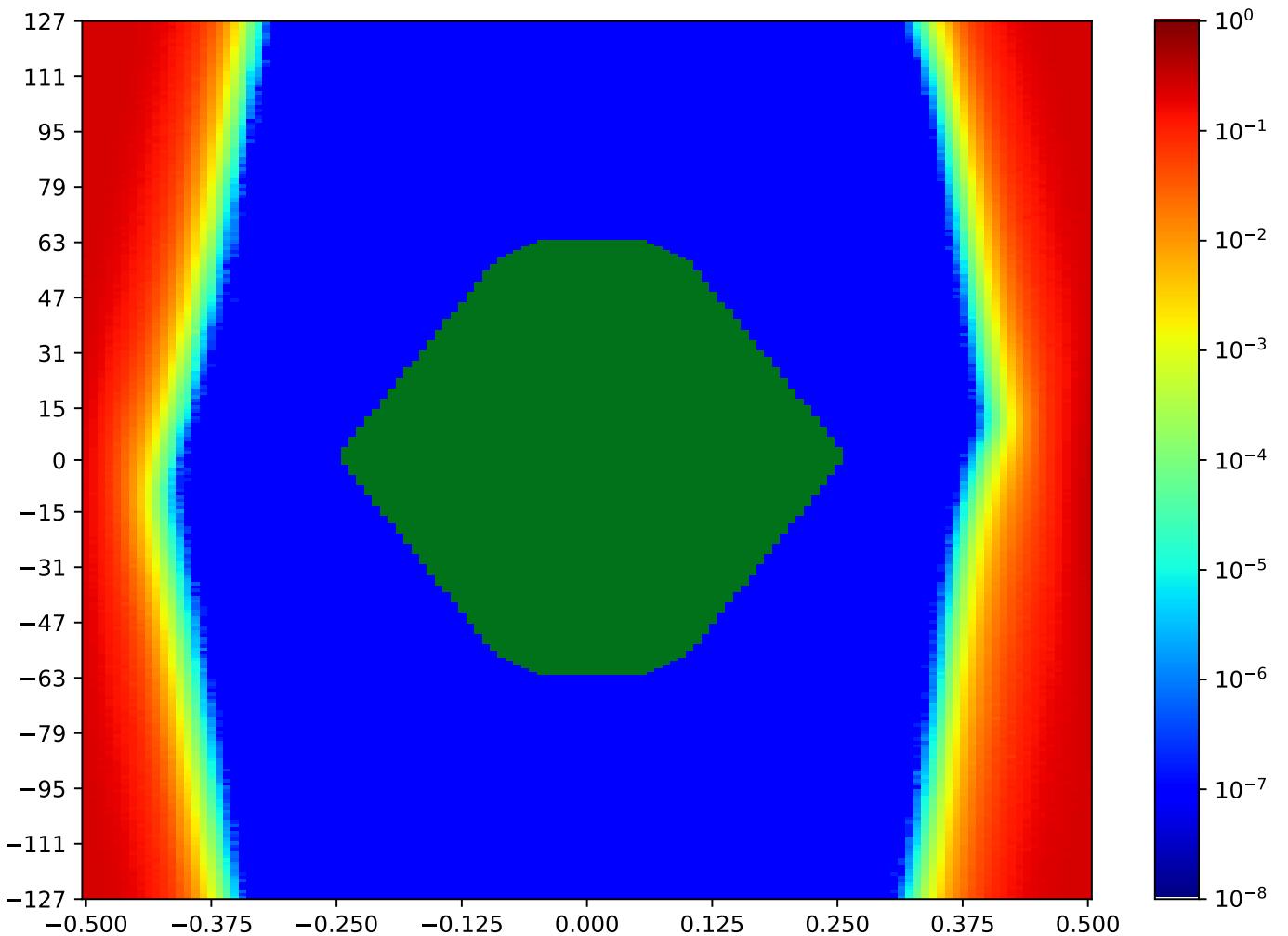


Figure 4.129: MSP_A_FPGA-TX1-01-RX17-01-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.3 MSP_A_FPGA-TX1-02-RX17-02-MSP_C_FPGA

Table 4.120: MSP_A_FPGA-TX1-02-RX17-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:59:34		2018-Sep-26 19:00:47	
Reset RX	OA	HO		VO	VO (%)
true	23497	97		75.19%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

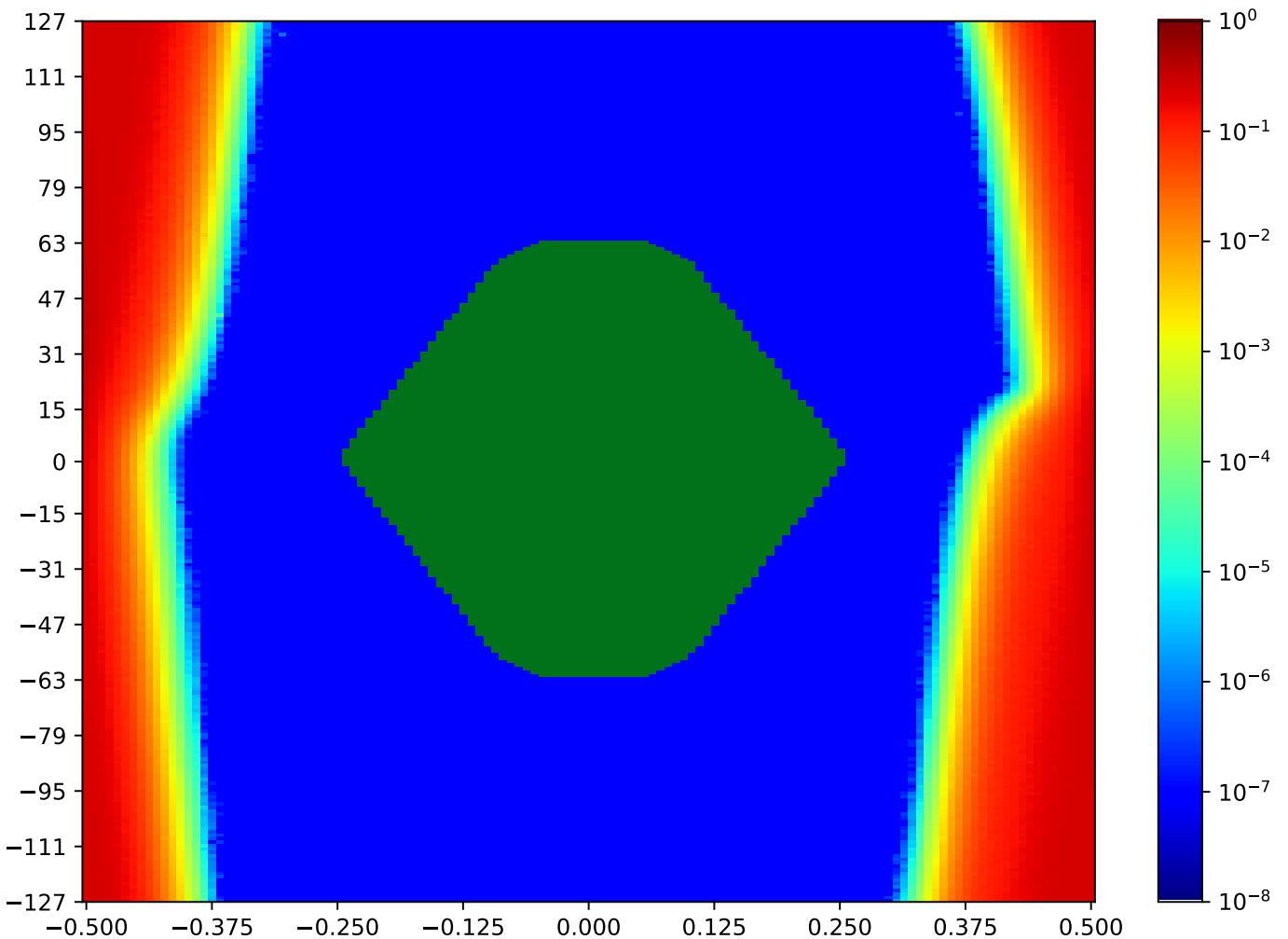


Figure 4.130: MSP_A_FPGA-TX1-02-RX17-02-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.4 MSP_A_FPGA-TX1-03-RX17-03-MSP_C_FPGA

Table 4.121: MSP_A_FPGA-TX1-03-RX17-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:53:28		2018-Sep-26 18:54:42	
Reset RX	OA	HO		VO	VO (%)
true	23609	98		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

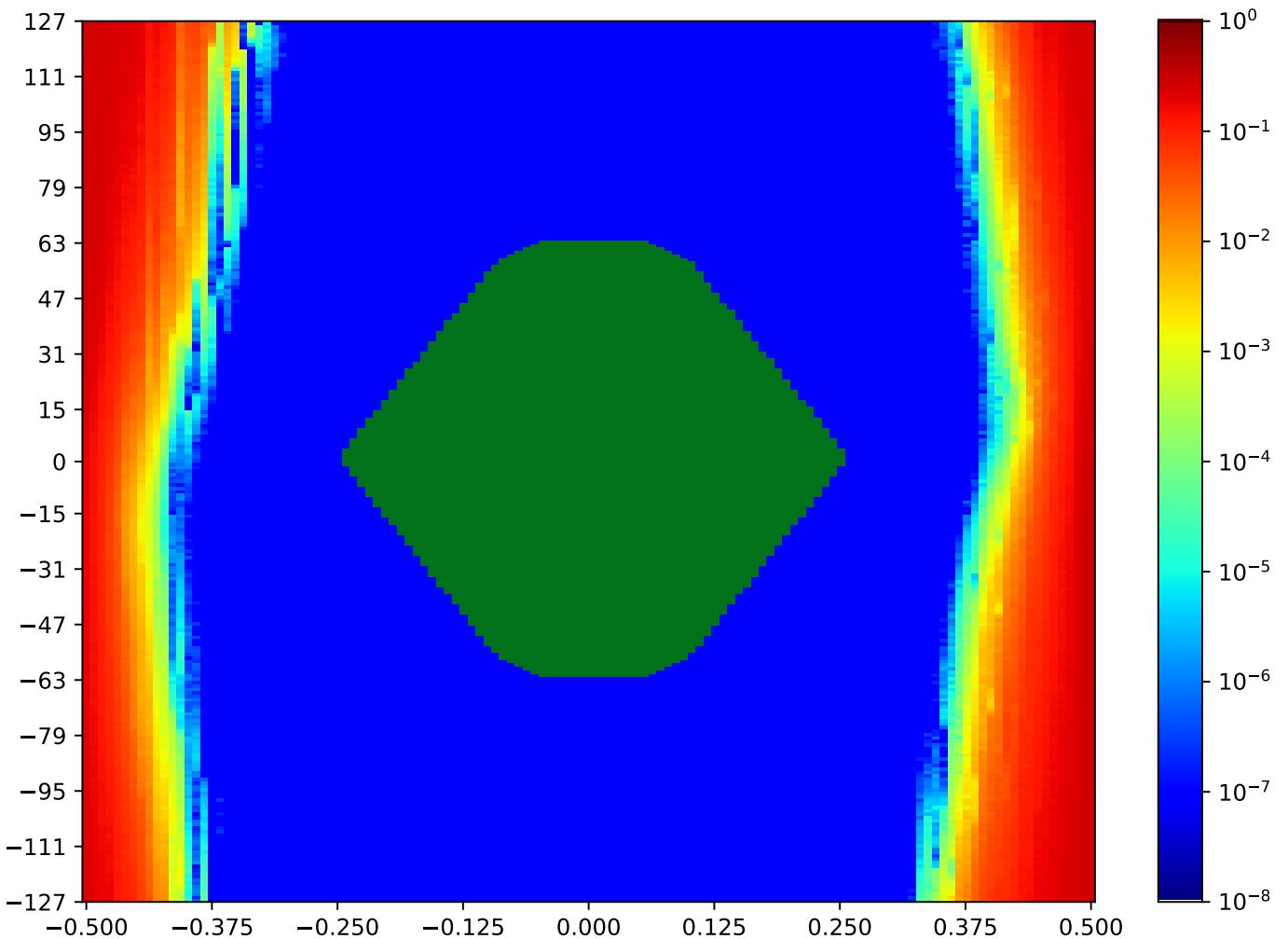


Figure 4.131: MSP_A_FPGA-TX1-03-RX17-03-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.5 MSP_A_FPGA-TX1-04-RX17-04-MSP_C_FPGA

Table 4.122: MSP_A_FPGA-TX1-04-RX17-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:03:14		2018-Sep-26 19:04:28	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23832	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

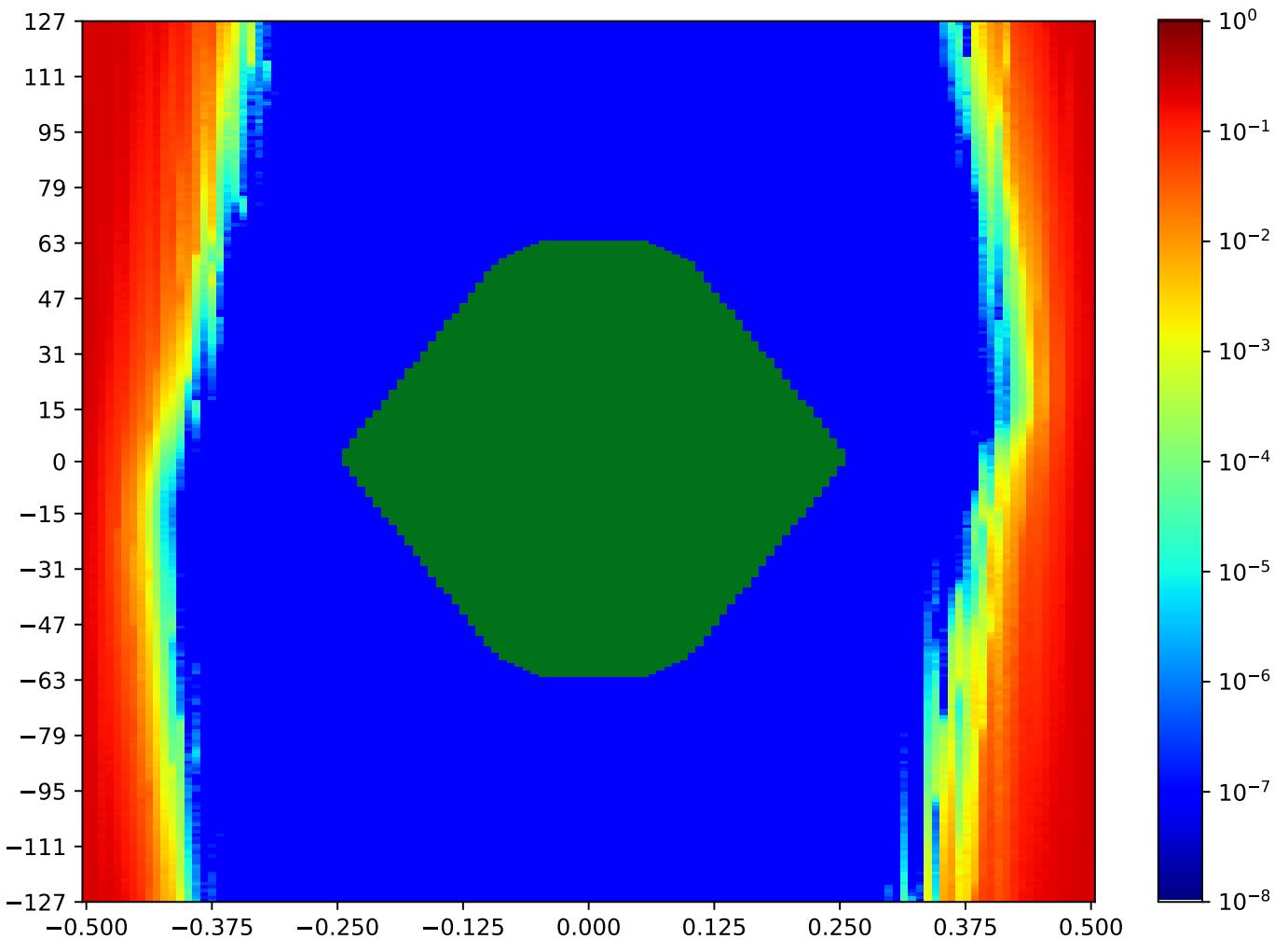


Figure 4.132: MSP_A_FPGA-TX1-04-RX17-04-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.6 MSP_A_FPGA-TX1-05-RX17-05-MSP_C_FPGA

Table 4.123: MSP_A_FPGA-TX1-05-RX17-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:52:15		2018-Sep-26 18:53:28	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23817	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

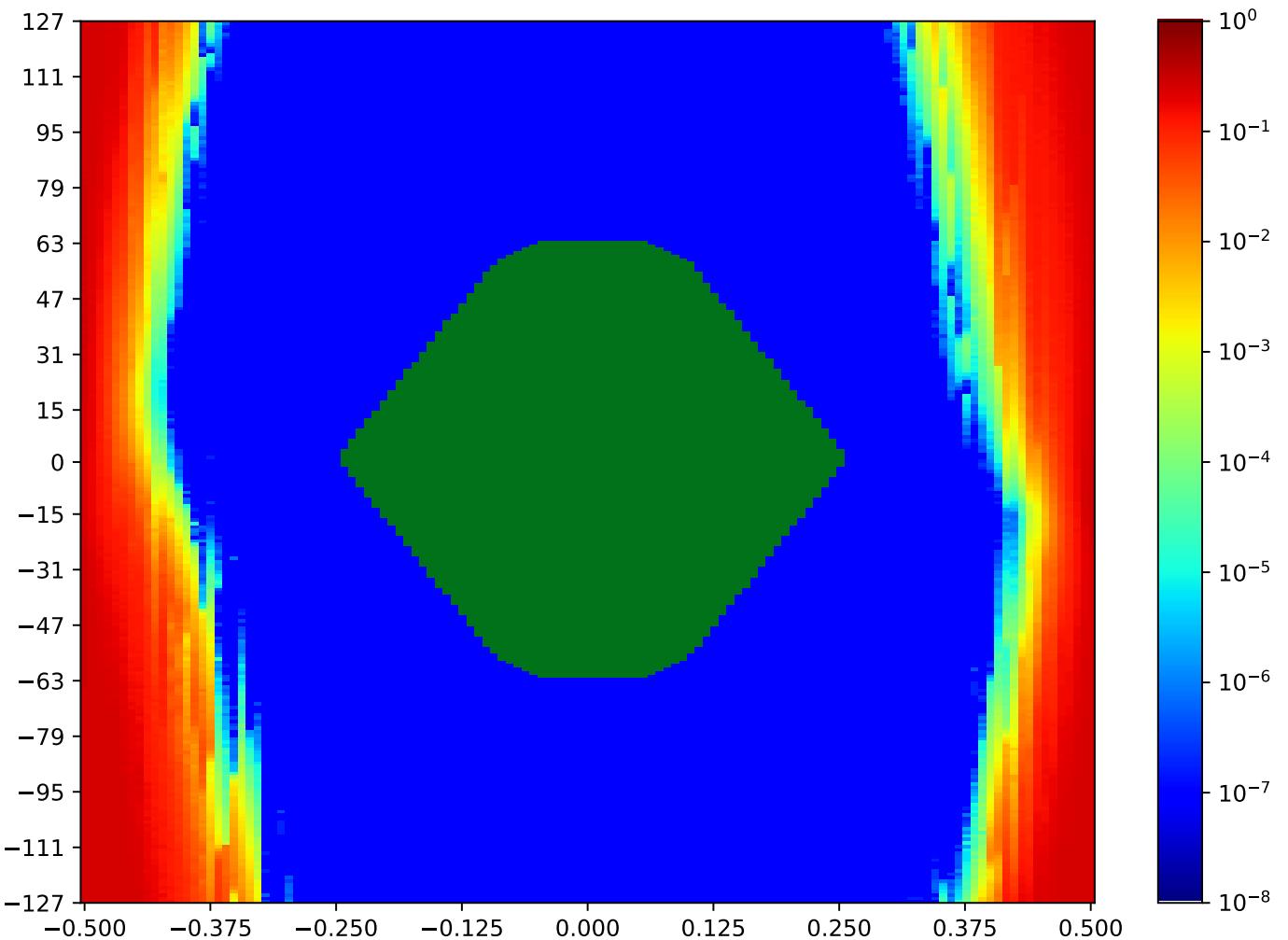


Figure 4.133: MSP_A_FPGA-TX1-05-RX17-05-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.7 MSP_A_FPGA-TX1-06-RX17-06-MSP_C_FPGA

Table 4.124: MSP_A_FPGA-TX1-06-RX17-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:05:43		2018-Sep-26 19:06:56	
Reset RX	OA	HO		VO	VO (%)
true	22950	99		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

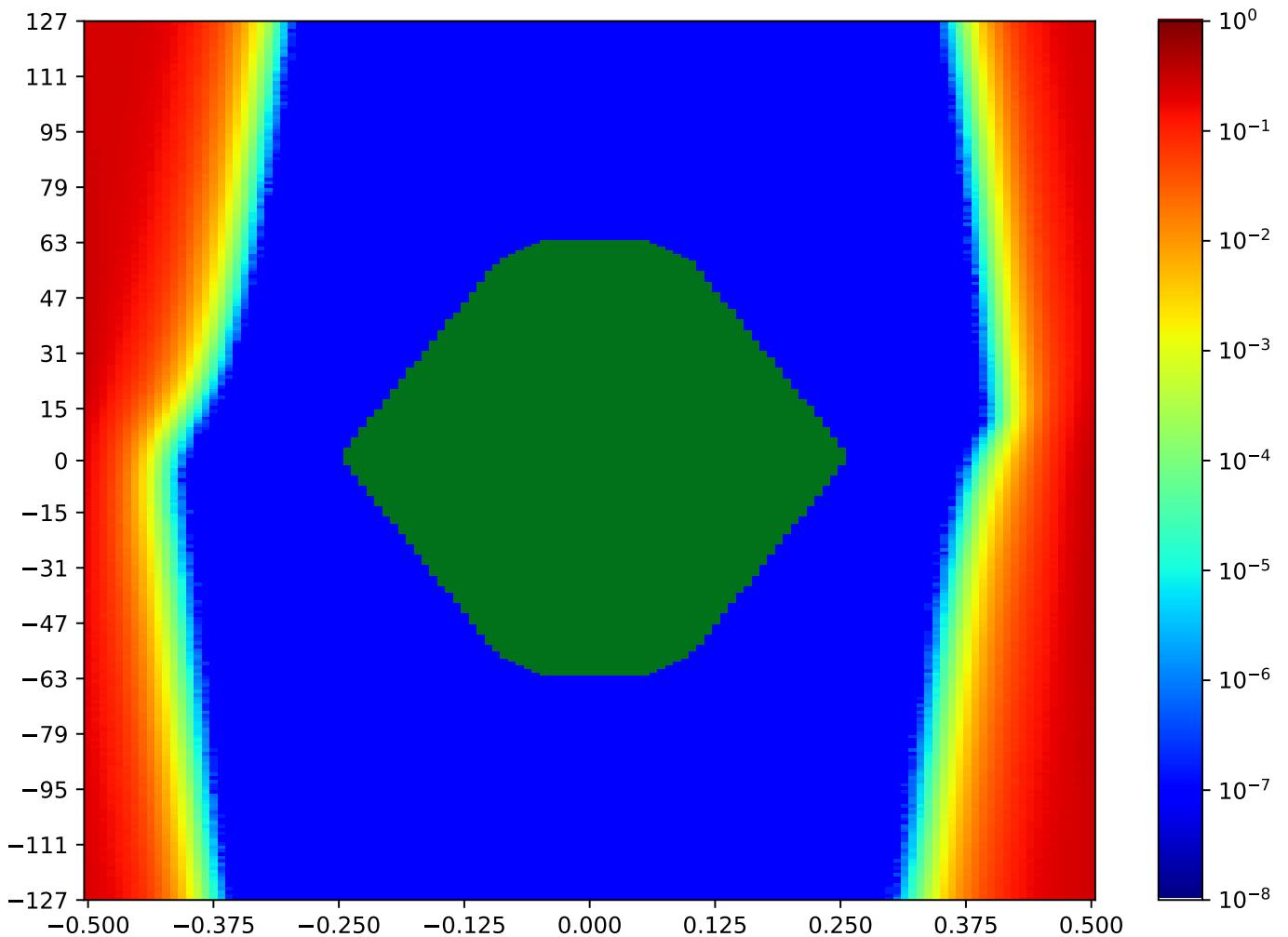


Figure 4.134: MSP_A_FPGA-TX1-06-RX17-06-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.8 MSP_A_FPGA-TX1-07-RX17-07-MSP_C_FPGA

Table 4.125: MSP_A_FPGA-TX1-07-RX17-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:54:42		2018-Sep-26 18:55:55	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24254	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

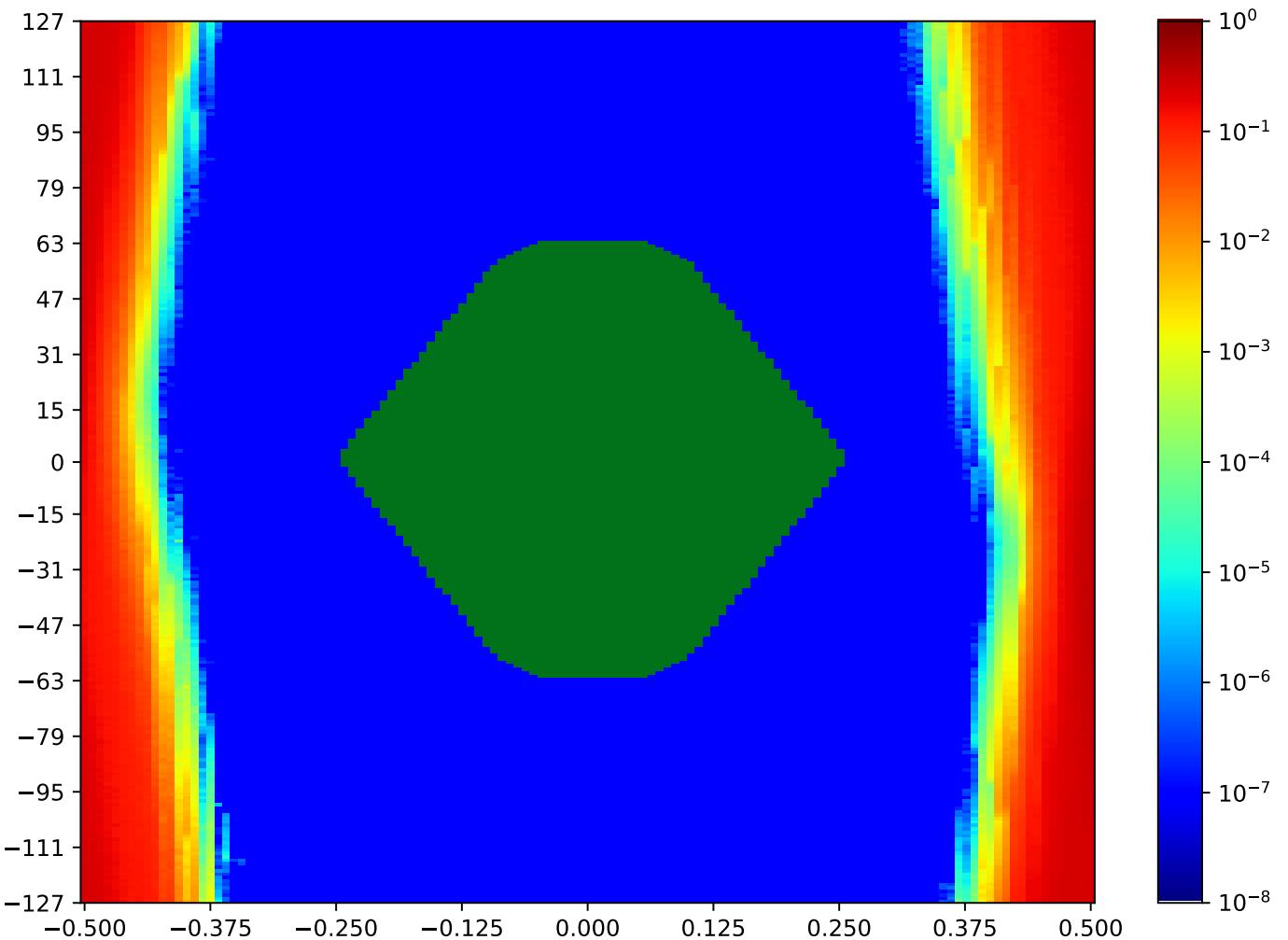


Figure 4.135: MSP_A_FPGA-TX1-07-RX17-07-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.9 MSP_A_FPGA-TX1-08-RX17-08-MSP_C_FPGA

Table 4.126: MSP_A_FPGA-TX1-08-RX17-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:04:28		2018-Sep-26 19:05:42	
Reset RX	OA	HO		VO	VO (%)
true	23733	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

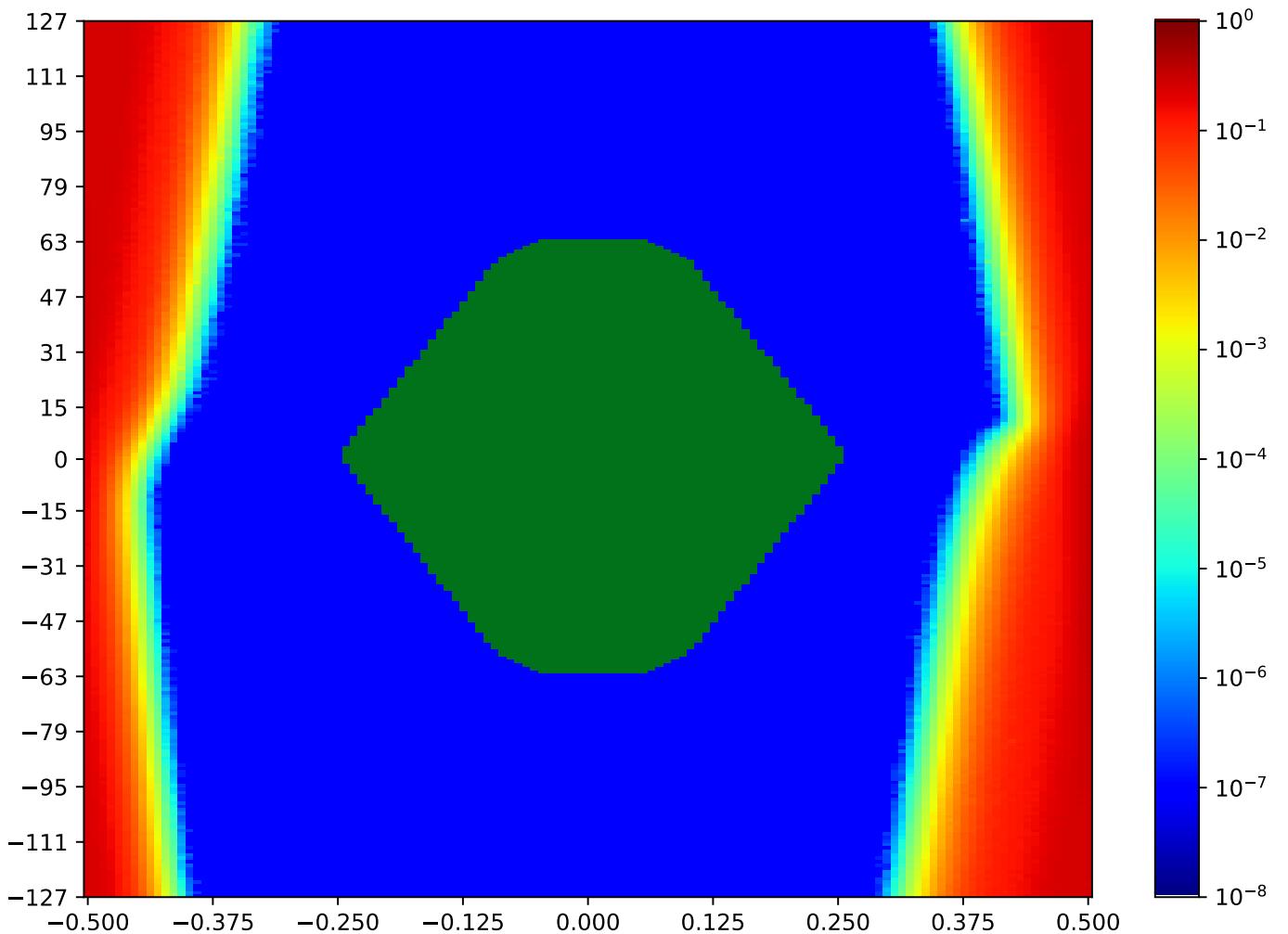


Figure 4.136: MSP_A_FPGA-TX1-08-RX17-08-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.10 MSP_A_FPGA-TX1-09-RX17-09-MSP_C_FPGA

Table 4.127: MSP_A_FPGA-TX1-09-RX17-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 18:57:09		2018-Sep-26 18:58:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	22984	98	75.97%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

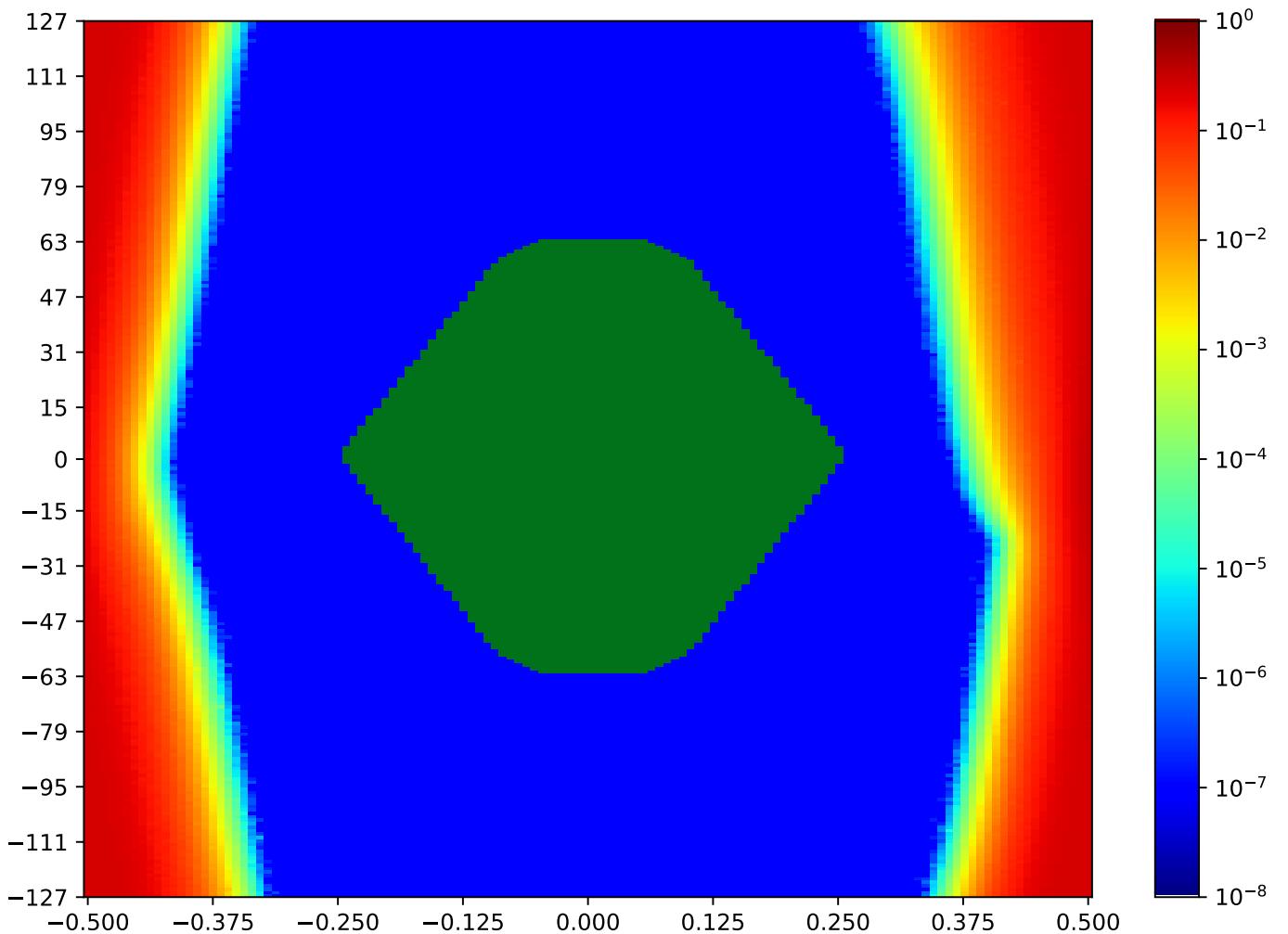


Figure 4.137: MSP_A_FPGA-TX1-09-RX17-09-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.11 MSP_A_FPGA-TX1-10-RX17-10-MSP_C_FPGA

Table 4.128: MSP_A_FPGA-TX1-10-RX17-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:02:00		2018-Sep-26 19:03:14	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23256	97		75.19%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

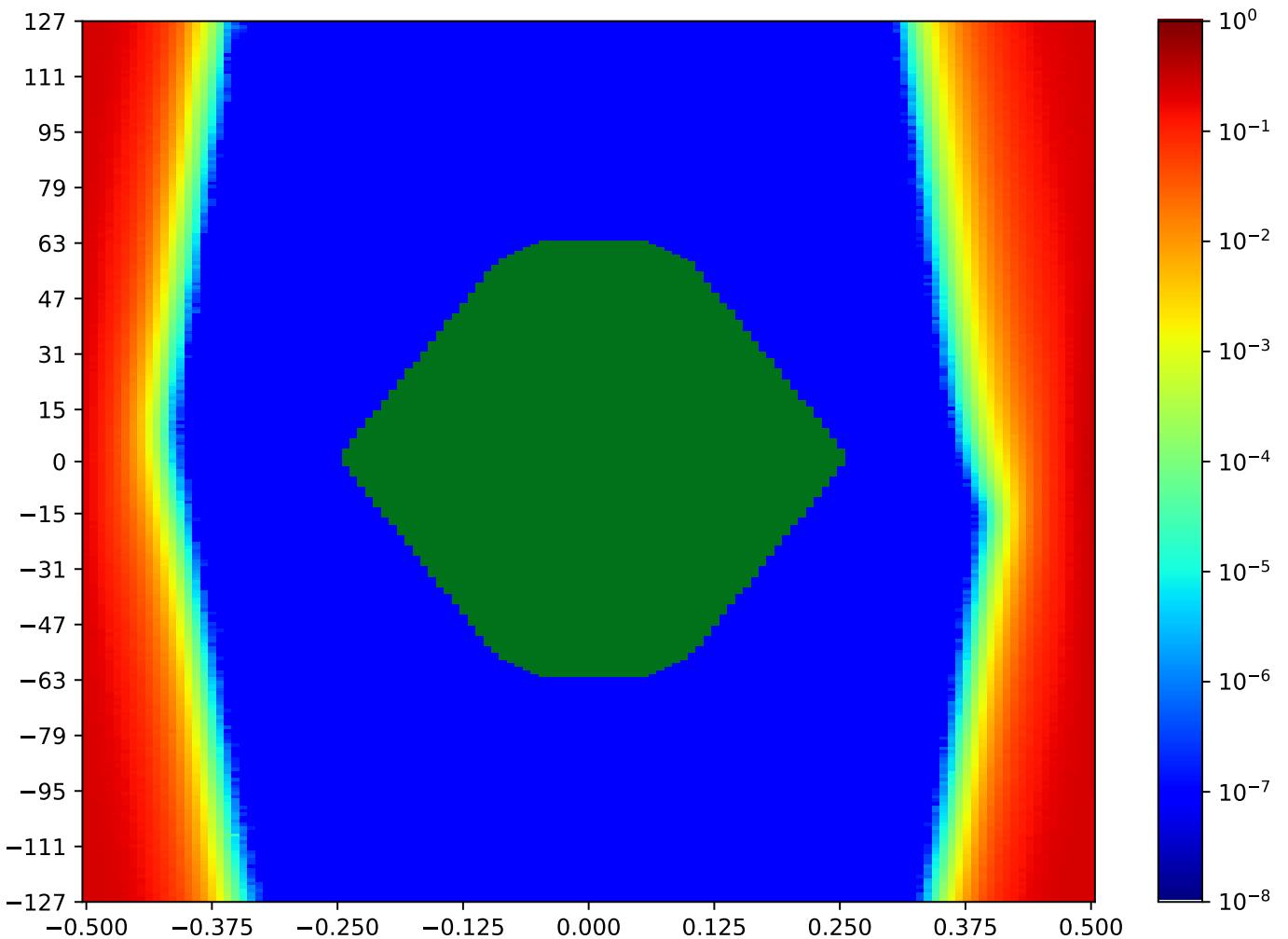


Figure 4.138: MSP_A_FPGA-TX1-10-RX17-10-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.10.12 MSP_A_FPGA-TX1-11-RX17-11-MSP_C_FPGA

Table 4.129: MSP_A_FPGA-TX1-11-RX17-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:00:47		2018-Sep-26 19:02:00	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23183	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

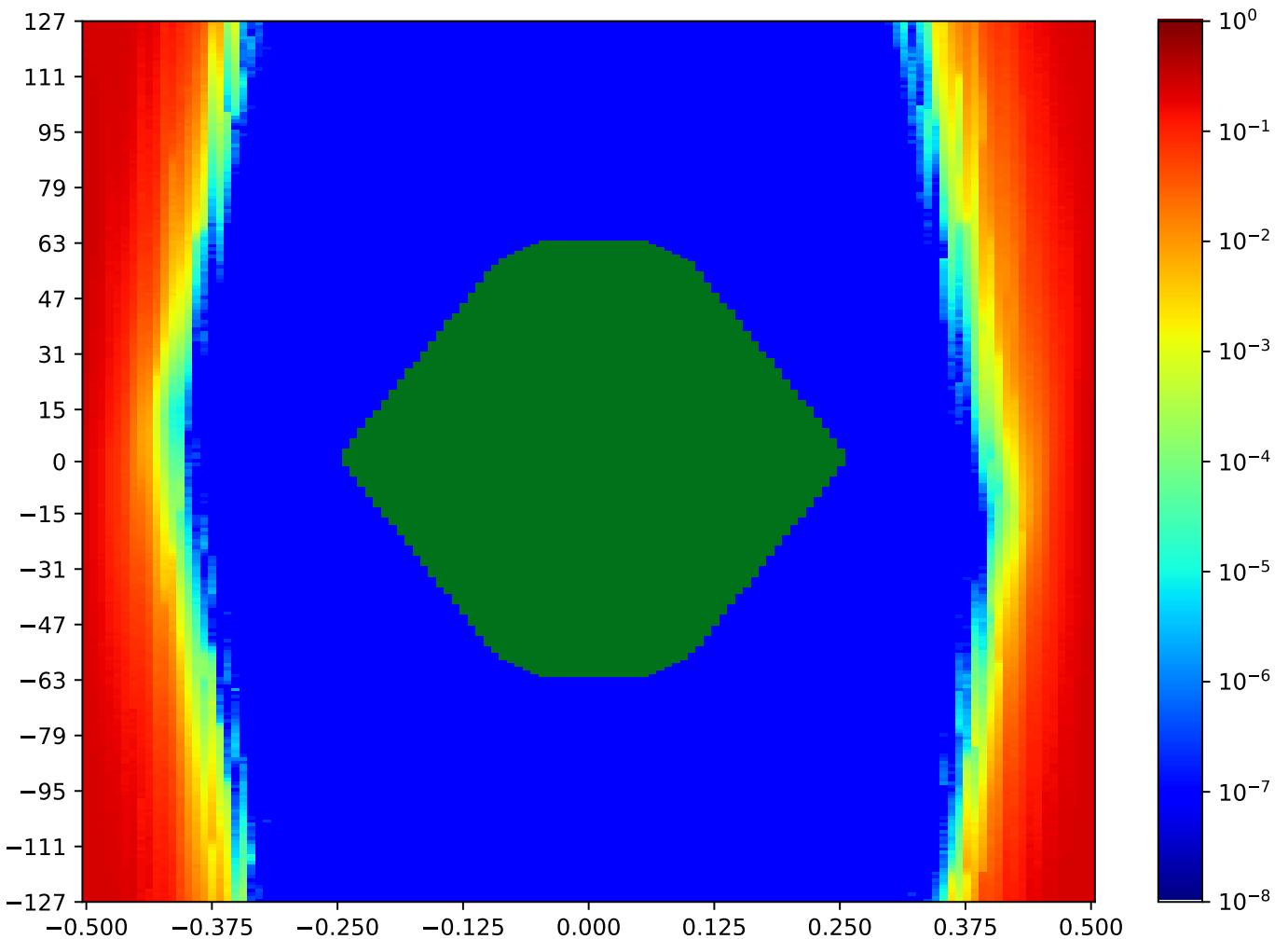


Figure 4.139: MSP_A_FPGA-TX1-11-RX17-11-MSP_C_FPGA

Call back to summary Figure 4.127. Sibling eye diagrams: V2-12.8.

4.11 MSP_A TX2 MSP_C RX18 Minipod Loopback

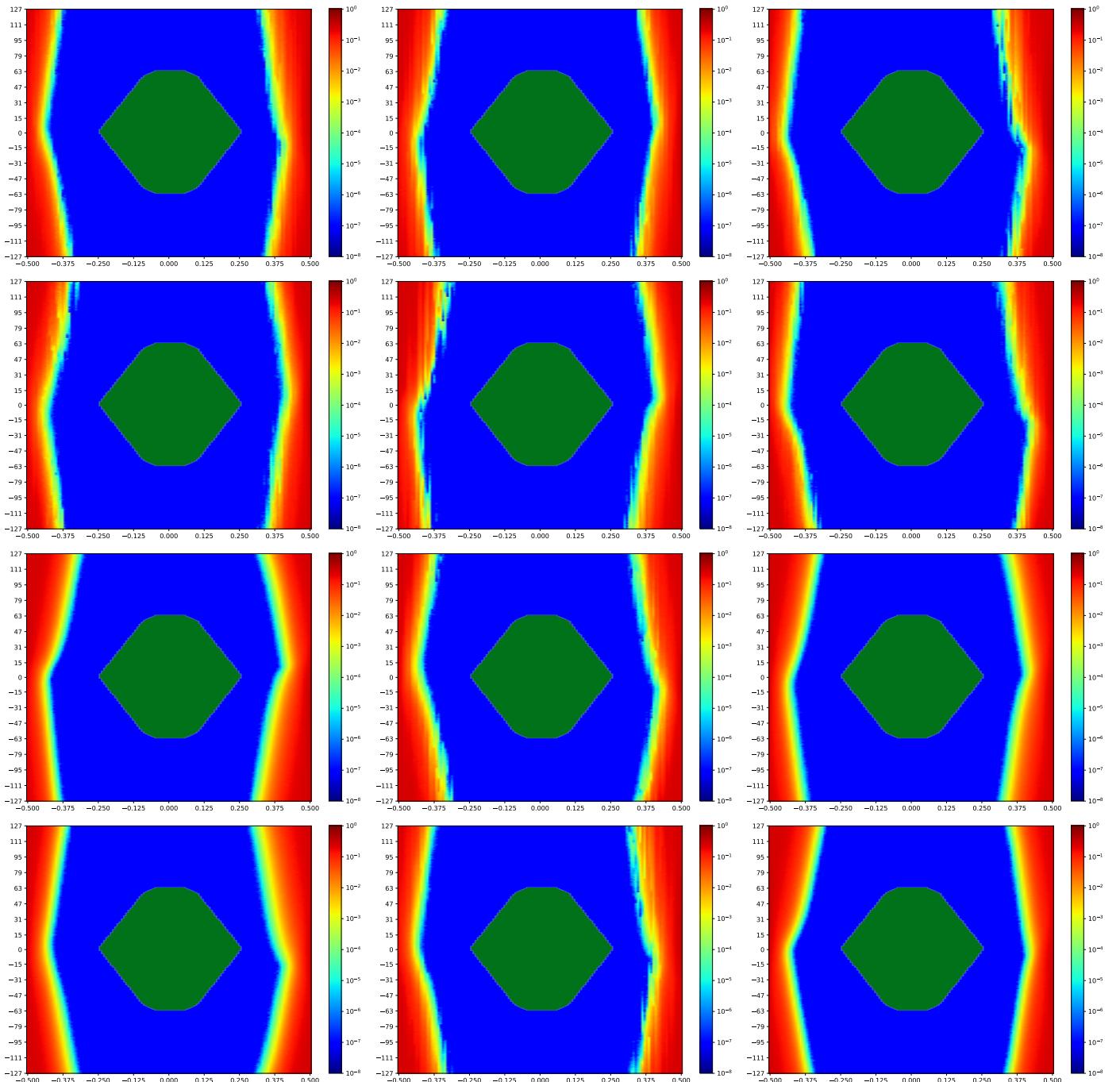


Figure 4.140: MSP_A TX2 MSP_C RX18 Minipod Loopback

A cross-reference to Figure 4.140. Sibling eye diagrams: V2-12.8.
Next summary Figure 4.153.

4.11.1 MSP_A_FPGA-TX2-00-RX18-00-MSP_C_FPGA

Table 4.130: MSP_A_FPGA-TX2-00-RX18-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:10:37		2018-Sep-26 19:11:50	
Reset RX	OA	HO		VO	VO (%)
true	23565	99		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

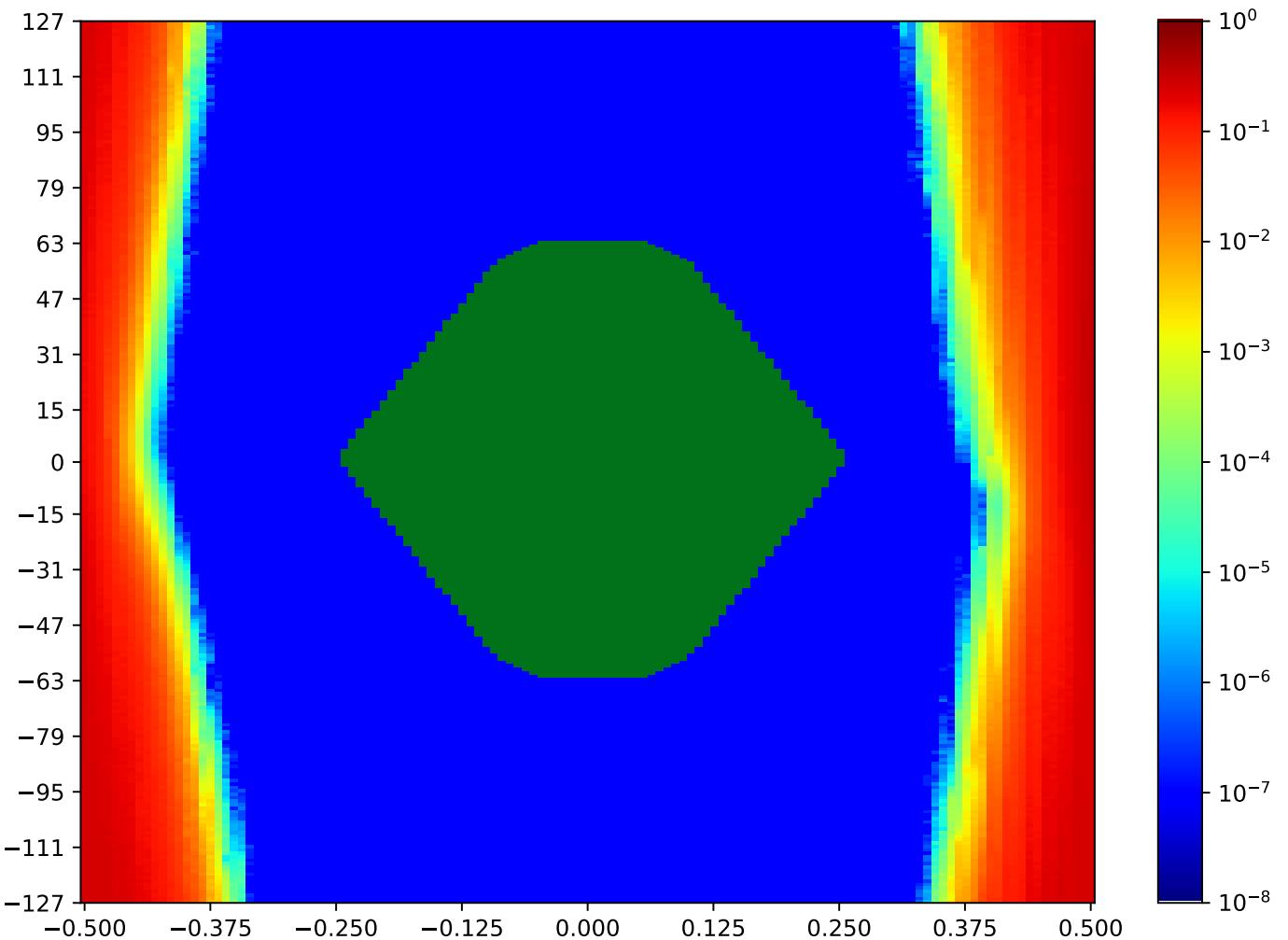


Figure 4.141: MSP_A_FPGA-TX2-00-RX18-00-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.2 MSP_A_FPGA-TX2-01-RX18-01-MSP_C_FPGA

Table 4.131: MSP_A_FPGA-TX2-01-RX18-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:08:10		2018-Sep-26 19:09:23	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23712	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

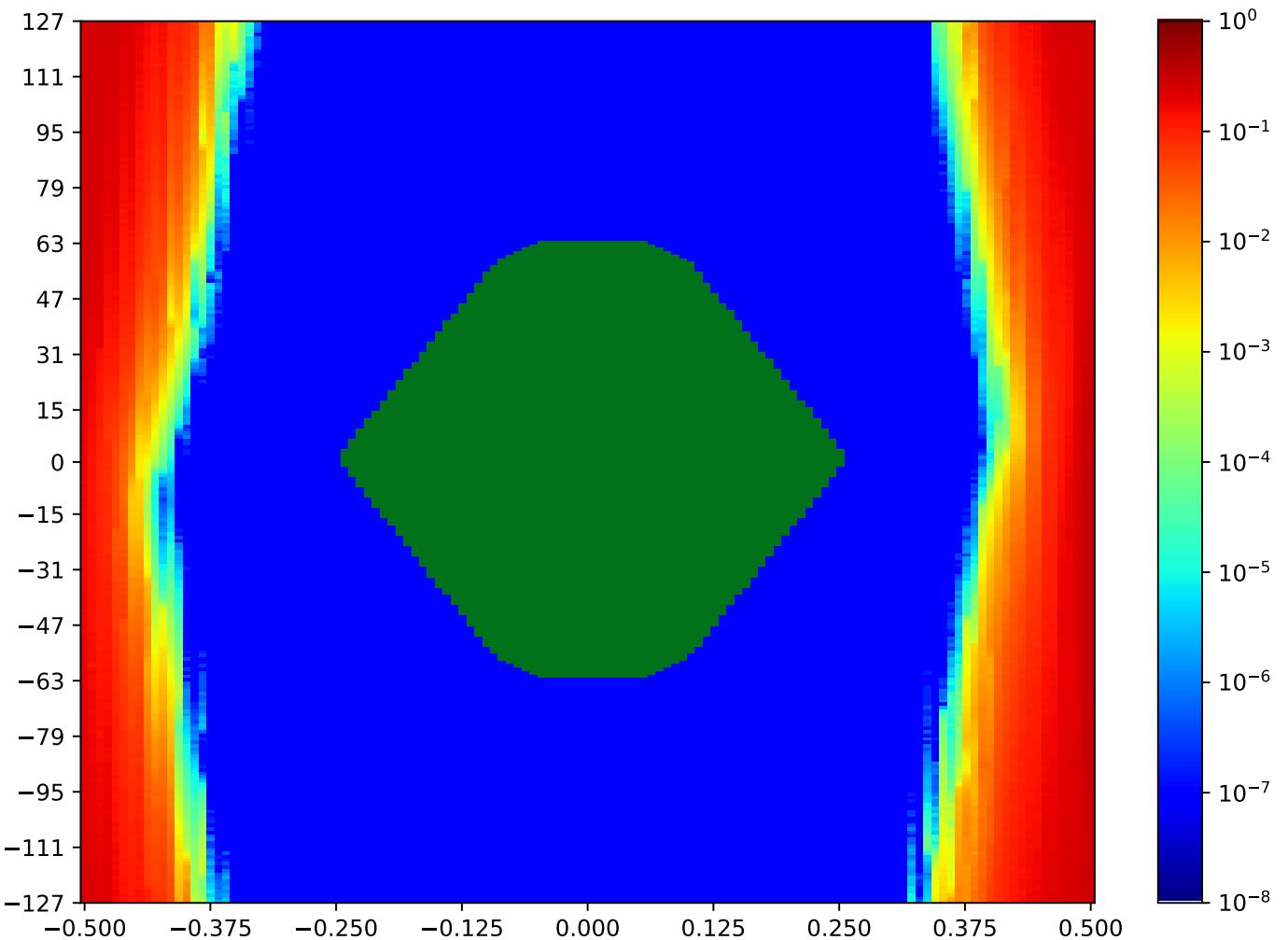


Figure 4.142: MSP_A_FPGA-TX2-01-RX18-01-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.3 MSP_A_FPGA-TX2-02-RX18-02-MSP_C_FPGA

Table 4.132: MSP_A_FPGA-TX2-02-RX18-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:14:17		2018-Sep-26 19:15:31	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23326	98		75.97%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

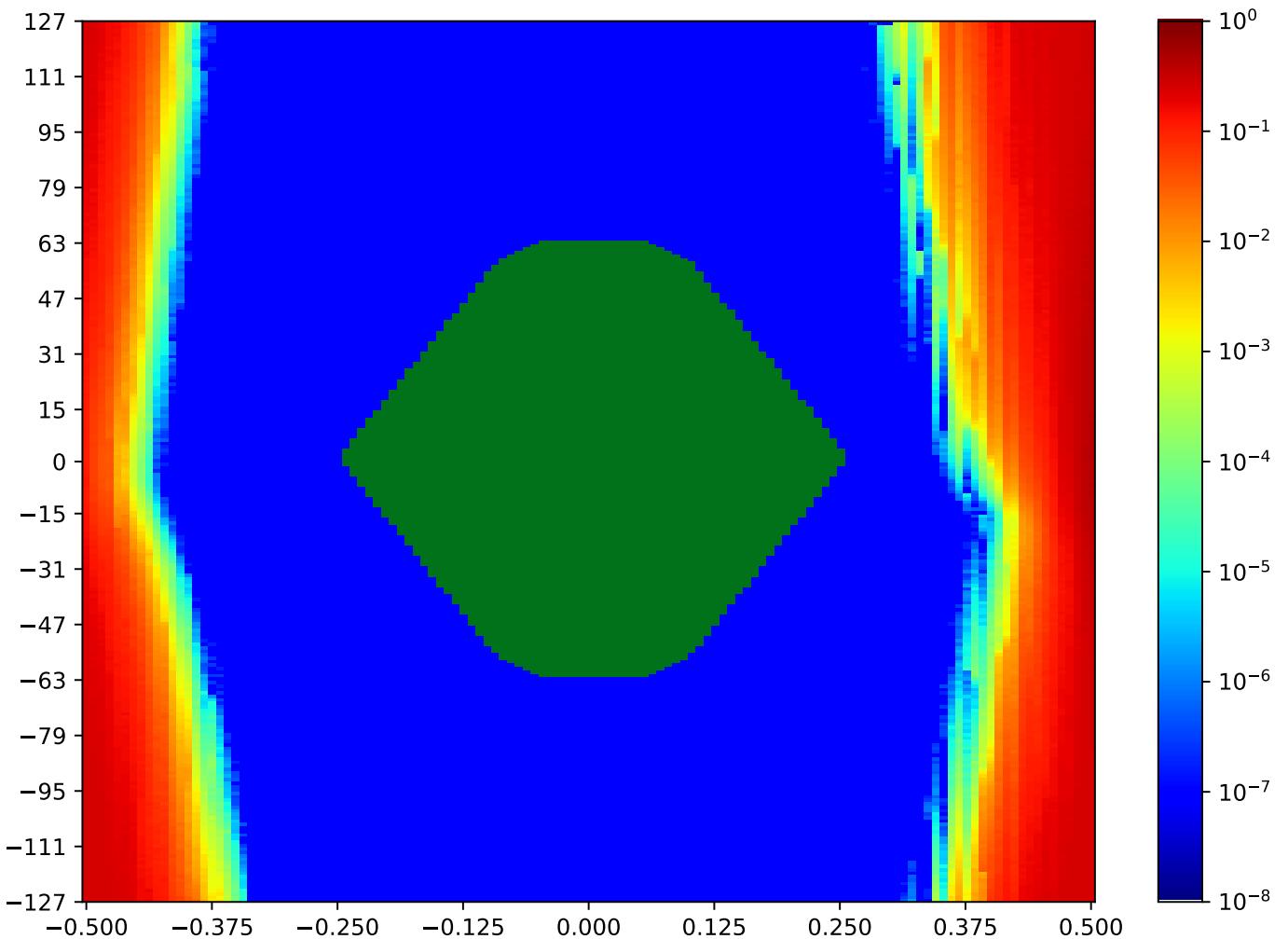


Figure 4.143: MSP_A_FPGA-TX2-02-RX18-02-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.4 MSP_A_FPGA-TX2-03-RX18-03-MSP_C_FPGA

Table 4.133: MSP_A_FPGA-TX2-03-RX18-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:06:56		2018-Sep-26 19:08:10	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23679	102		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

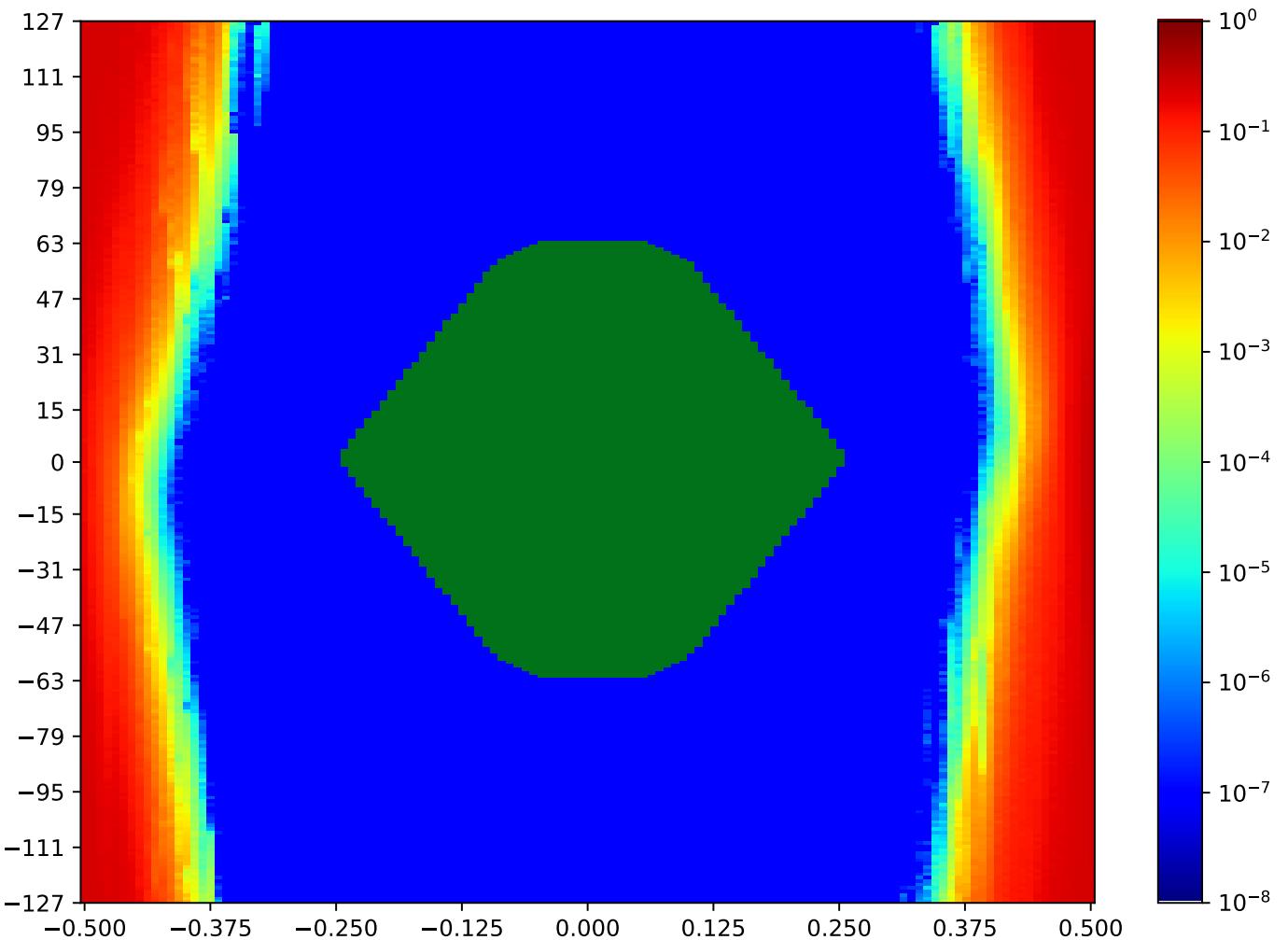


Figure 4.144: MSP_A_FPGA-TX2-03-RX18-03-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.5 MSP_A_FPGA-TX2-04-RX18-04-MSP_C_FPGA

Table 4.134: MSP_A_FPGA-TX2-04-RX18-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:17:58		2018-Sep-26 19:19:11	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23262	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

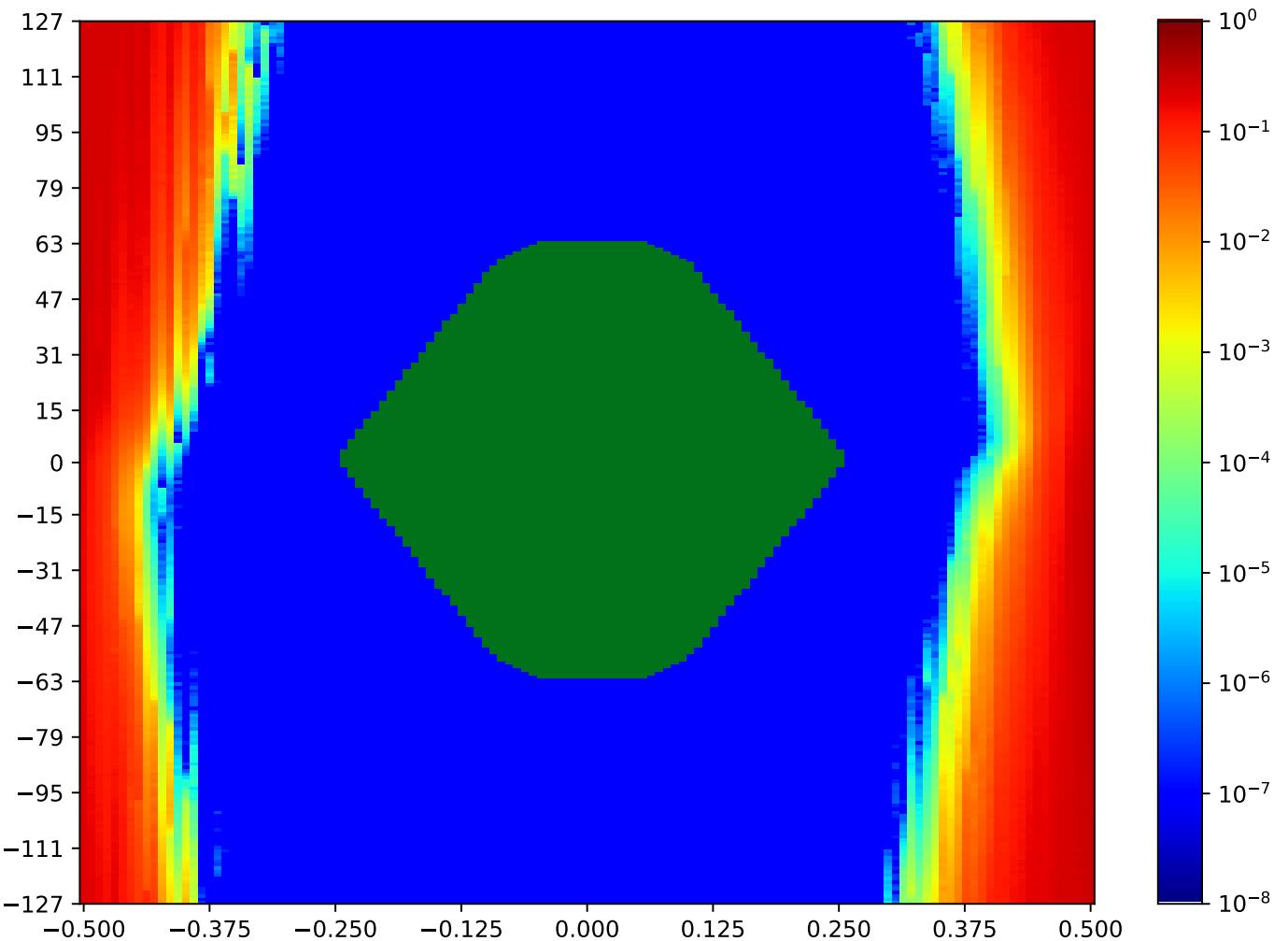


Figure 4.145: MSP_A_FPGA-TX2-04-RX18-04-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.6 MSP_A_FPGA-TX2-05-RX18-05-MSP_C_FPGA

Table 4.135: MSP_A_FPGA-TX2-05-RX18-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:09:23		2018-Sep-26 19:10:37	
Reset RX	OA	HO		VO	VO (%)
true	23670	99		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

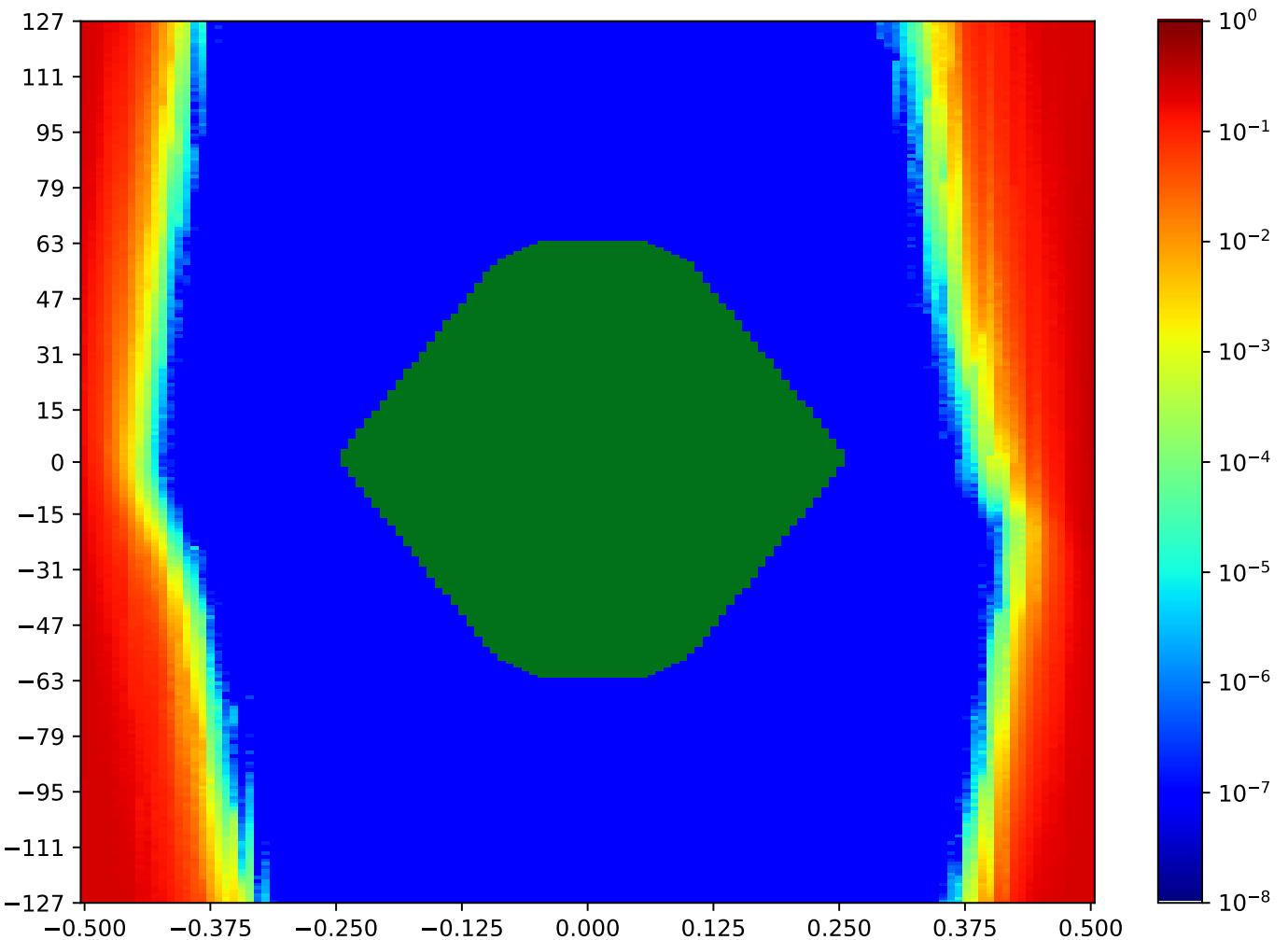


Figure 4.146: MSP_A_FPGA-TX2-05-RX18-05-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.7 MSP_A_FPGA-TX2-06-RX18-06-MSP_C_FPGA

Table 4.136: MSP_A_FPGA-TX2-06-RX18-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:20:24		2018-Sep-26 19:21:37	
Reset RX	OA	HO		VO	VO (%)
true	22712	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

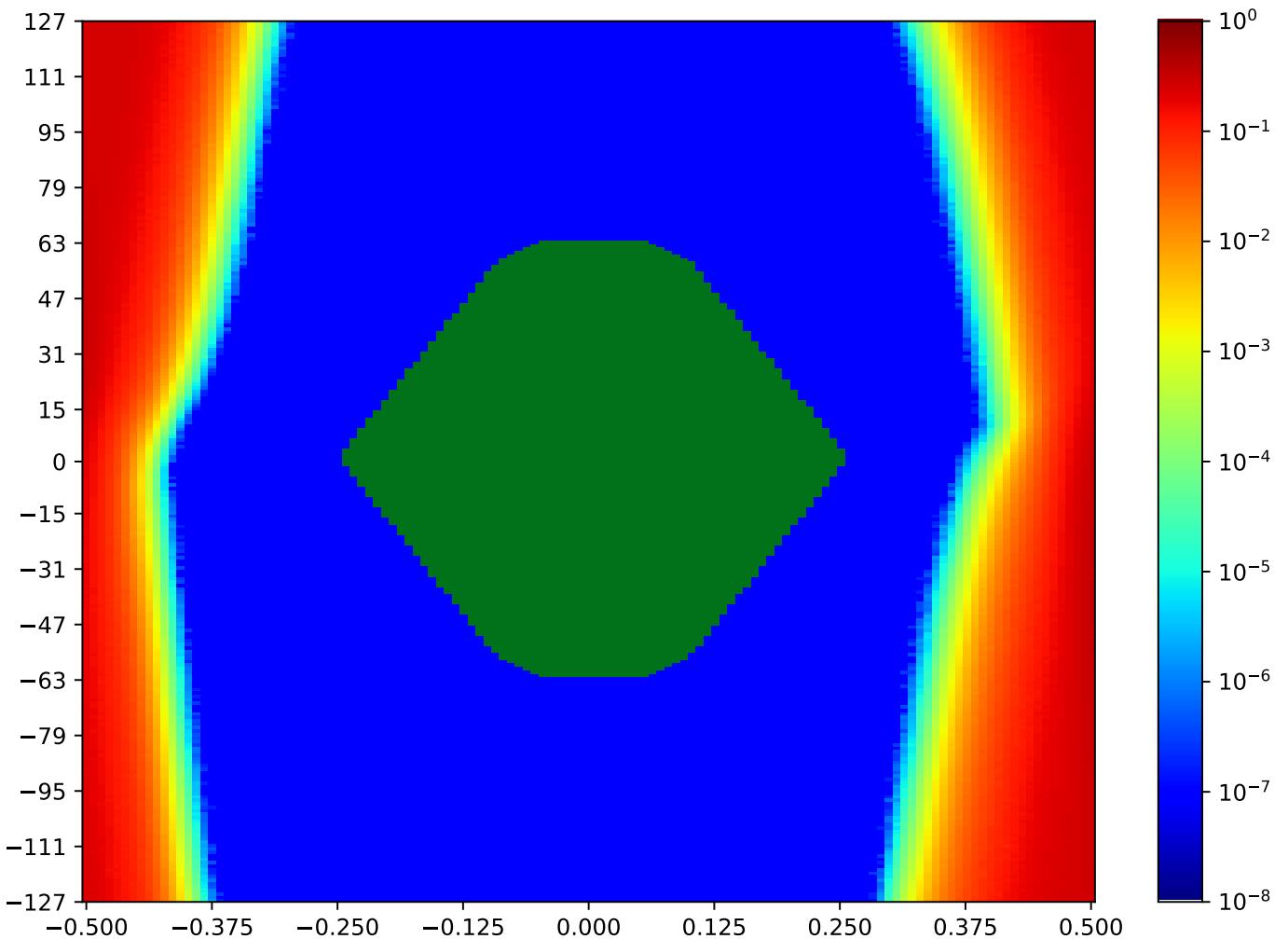


Figure 4.147: MSP_A_FPGA-TX2-06-RX18-06-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.8 MSP_A_FPGA-TX2-07-RX18-07-MSP_C_FPGA

Table 4.137: MSP_A_FPGA-TX2-07-RX18-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:11:50		2018-Sep-26 19:13:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23048	98	75.97%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

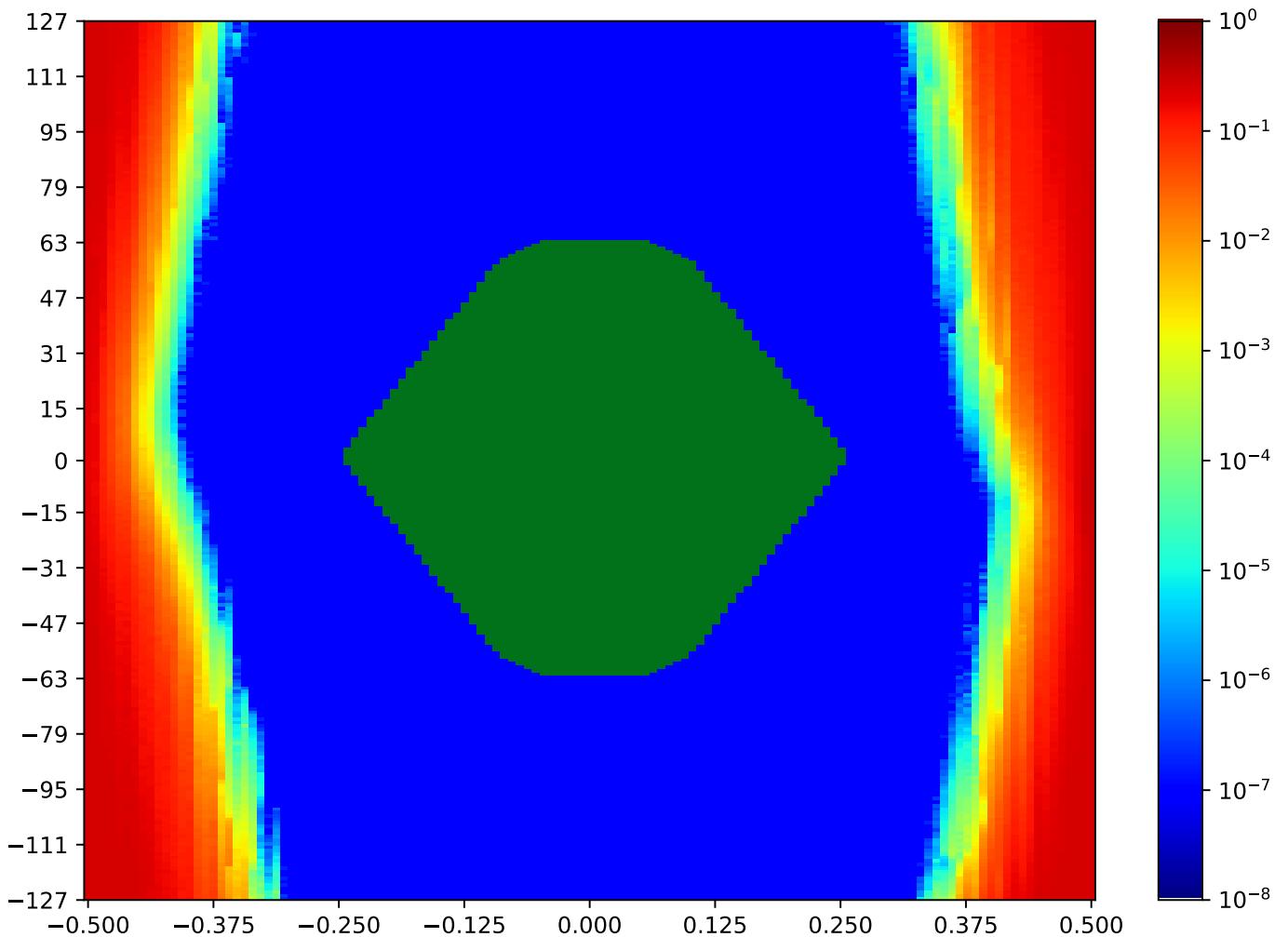


Figure 4.148: MSP_A_FPGA-TX2-07-RX18-07-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.9 MSP_A_FPGA-TX2-08-RX18-08-MSP_C_FPGA

Table 4.138: MSP_A_FPGA-TX2-08-RX18-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:19:11		2018-Sep-26 19:20:24	
Reset RX	OA	HO		VO	VO (%)
true	22838	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

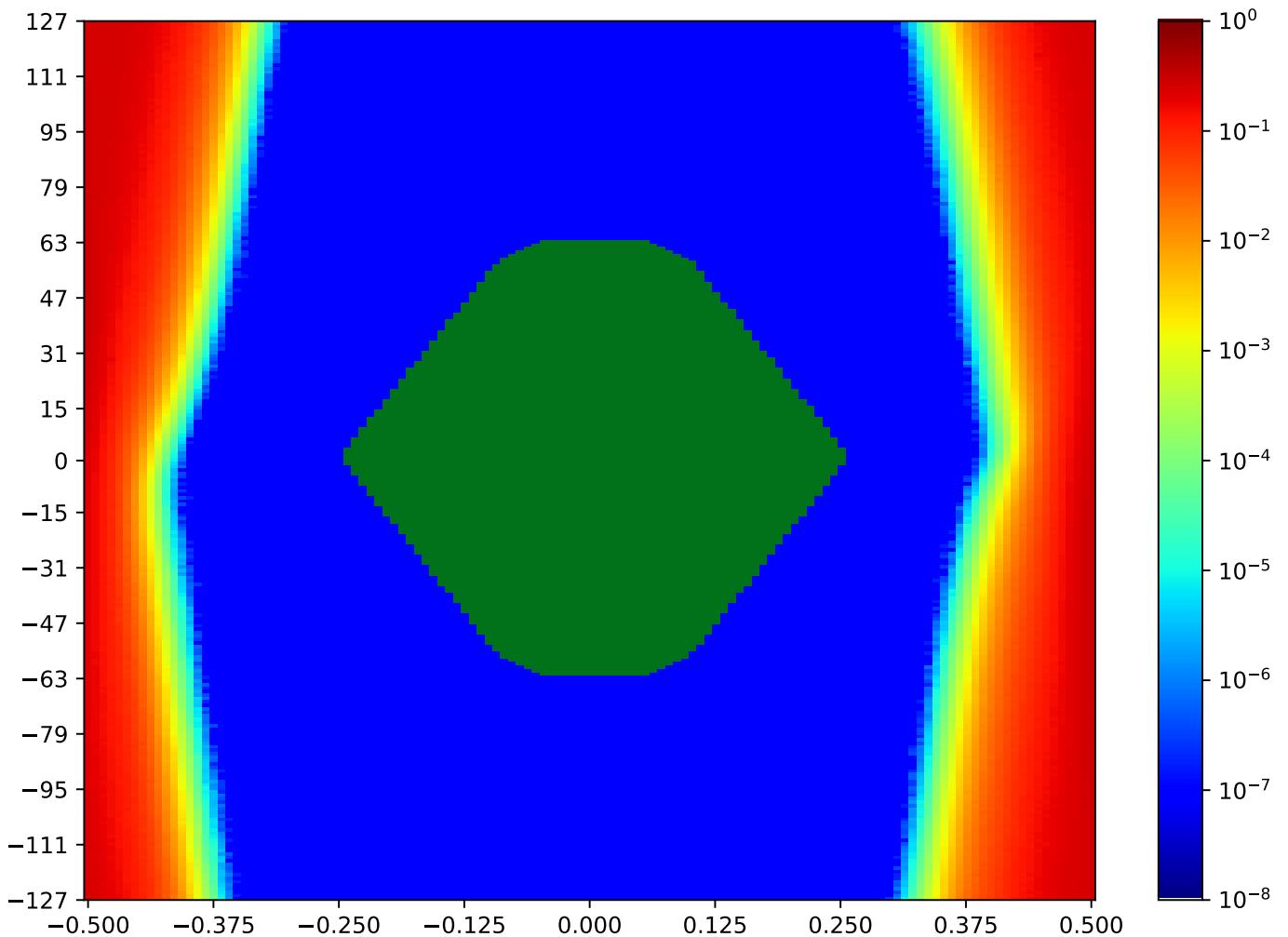


Figure 4.149: MSP_A_FPGA-TX2-08-RX18-08-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.10 MSP_A_FPGA-TX2-09-RX18-09-MSP_C_FPGA

Table 4.139: MSP_A_FPGA-TX2-09-RX18-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:13:04		2018-Sep-26 19:14:17	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	22490	95		73.64%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

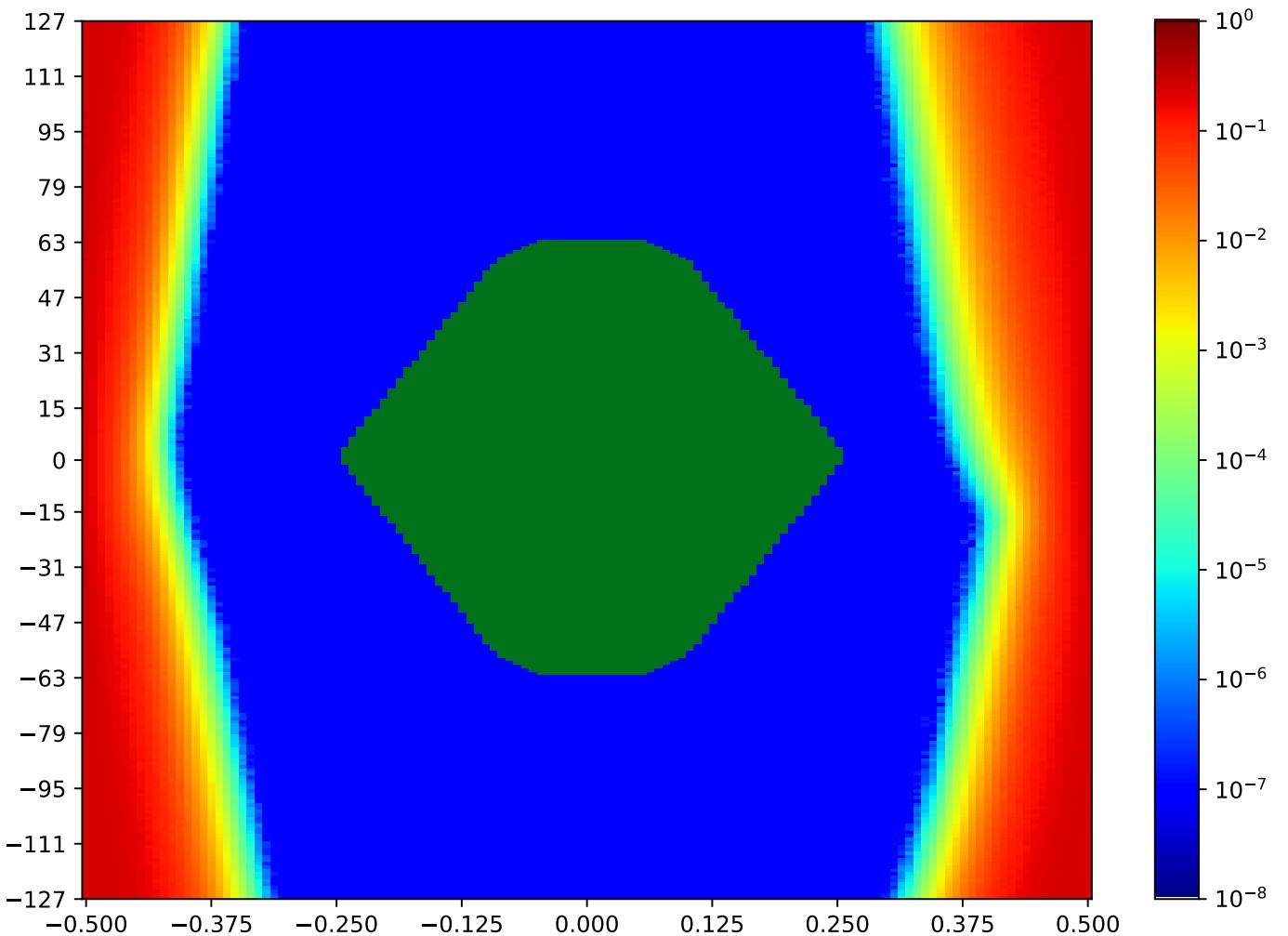


Figure 4.150: MSP_A_FPGA-TX2-09-RX18-09-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.11 MSP_A_FPGA-TX2-10-RX18-10-MSP_C_FPGA

Table 4.140: MSP_A_FPGA-TX2-10-RX18-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:16:44		2018-Sep-26 19:17:58	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23129	98		75.97%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

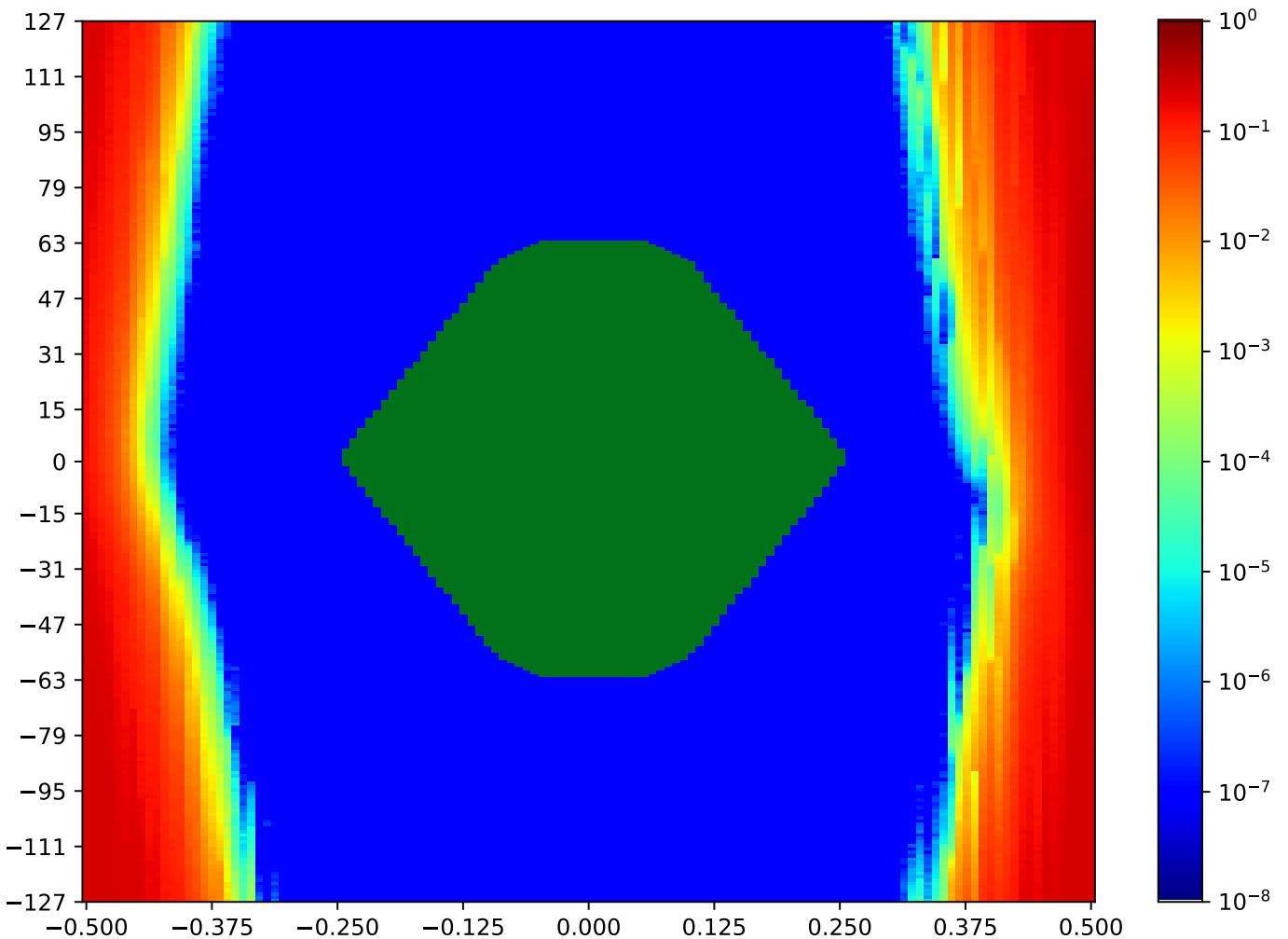


Figure 4.151: MSP_A_FPGA-TX2-10-RX18-10-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.11.12 MSP_A_FPGA-TX2-11-RX18-11-MSP_C_FPGA

Table 4.141: MSP_A_FPGA-TX2-11-RX18-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:15:31		2018-Sep-26 19:16:44	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23312	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

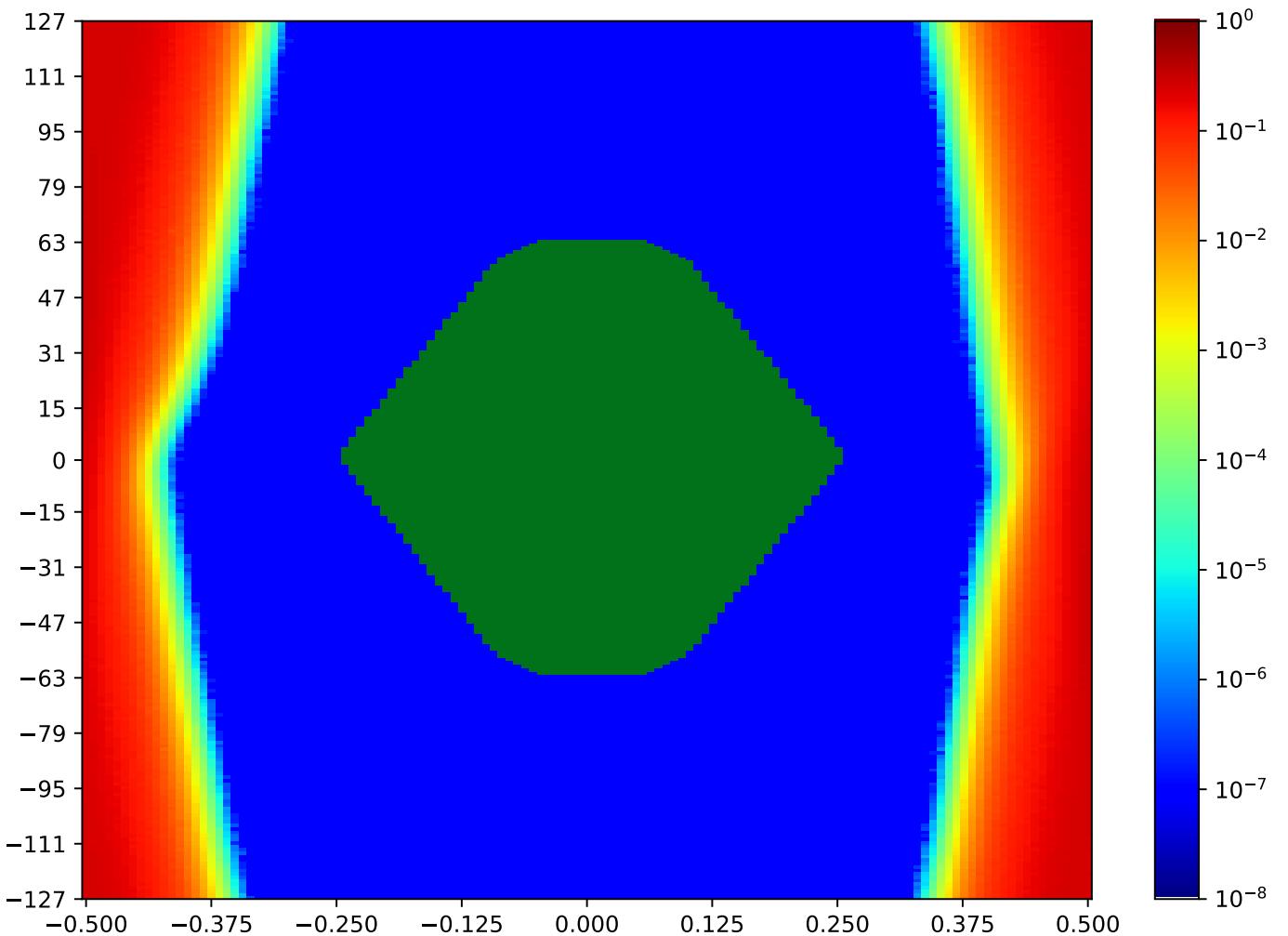


Figure 4.152: MSP_A_FPGA-TX2-11-RX18-11-MSP_C_FPGA

Call back to summary Figure 4.140. Sibling eye diagrams: V2-12.8.

4.12 MSP_C TX3 MSP_A RX8 Minipod Loopback

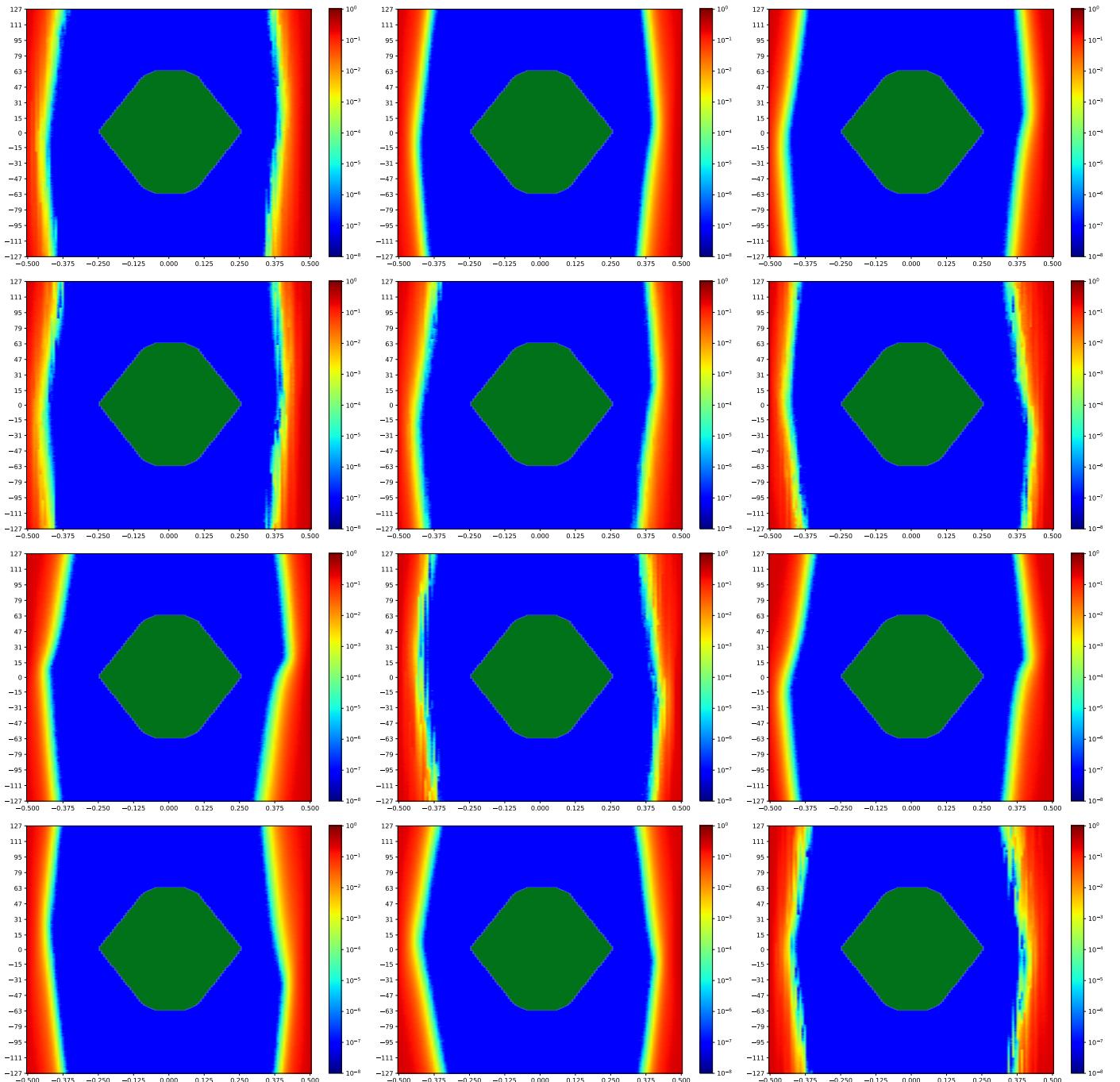


Figure 4.153: MSP_C TX3 MSP_A RX8 Minipod Loopback

A cross-reference to Figure 4.153. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.166.

4.12.1 MSP_C_FPGA-TX3-00-RX8-00-MSP_A_FPGA

Table 4.142: MSP_C_FPGA-TX3-00-RX8-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:25:23		2018-Sep-26 19:26:38	
Reset RX	OA	HO		VO	VO (%)
true	24408	100		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

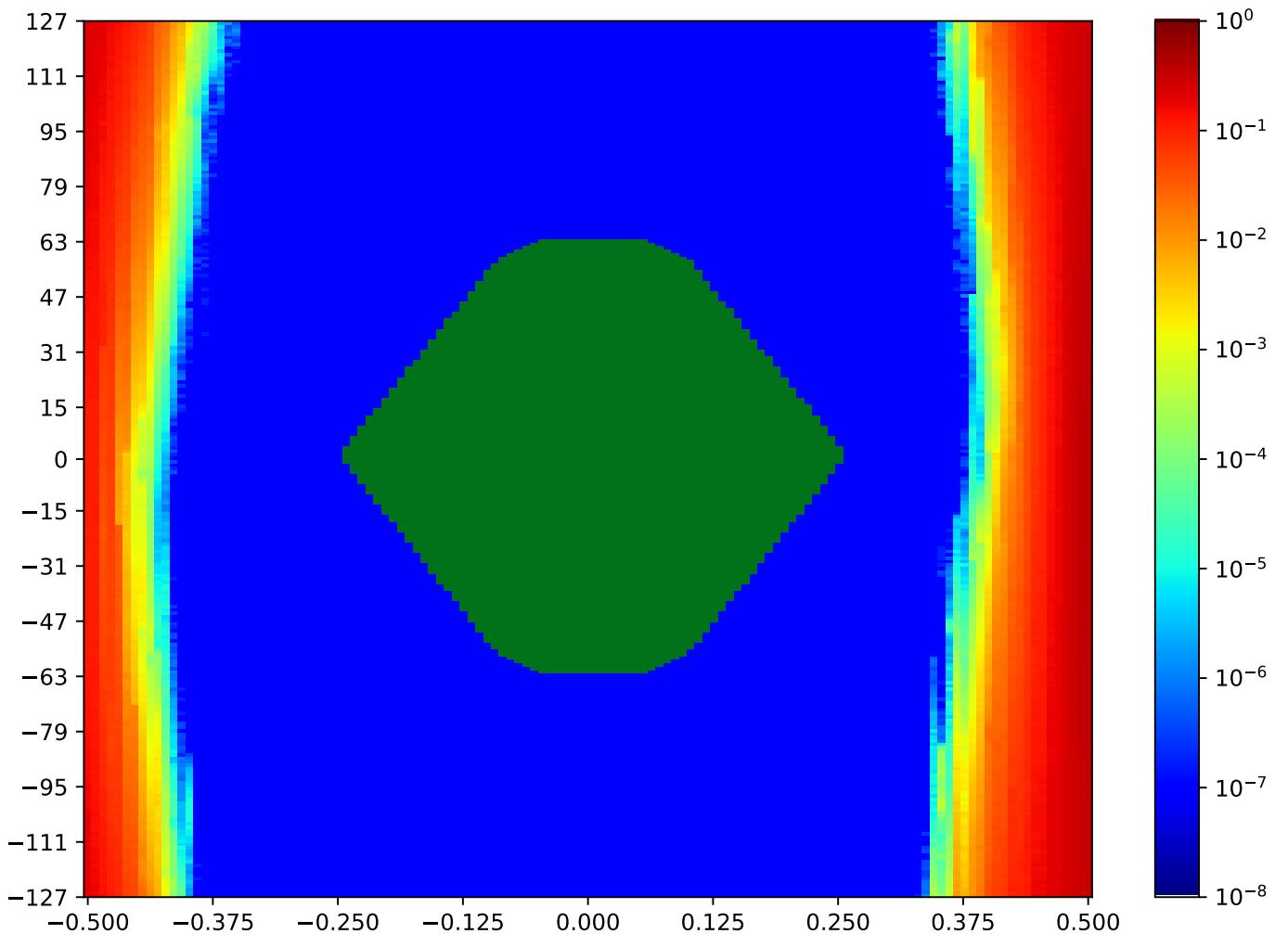


Figure 4.154: MSP_C_FPGA-TX3-00-RX8-00-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.2 MSP_C_FPGA-TX3-01-RX8-01-MSP_A_FPGA

Table 4.143: MSP_C_FPGA-TX3-01-RX8-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:27:53		2018-Sep-26 19:29:08	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24641	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

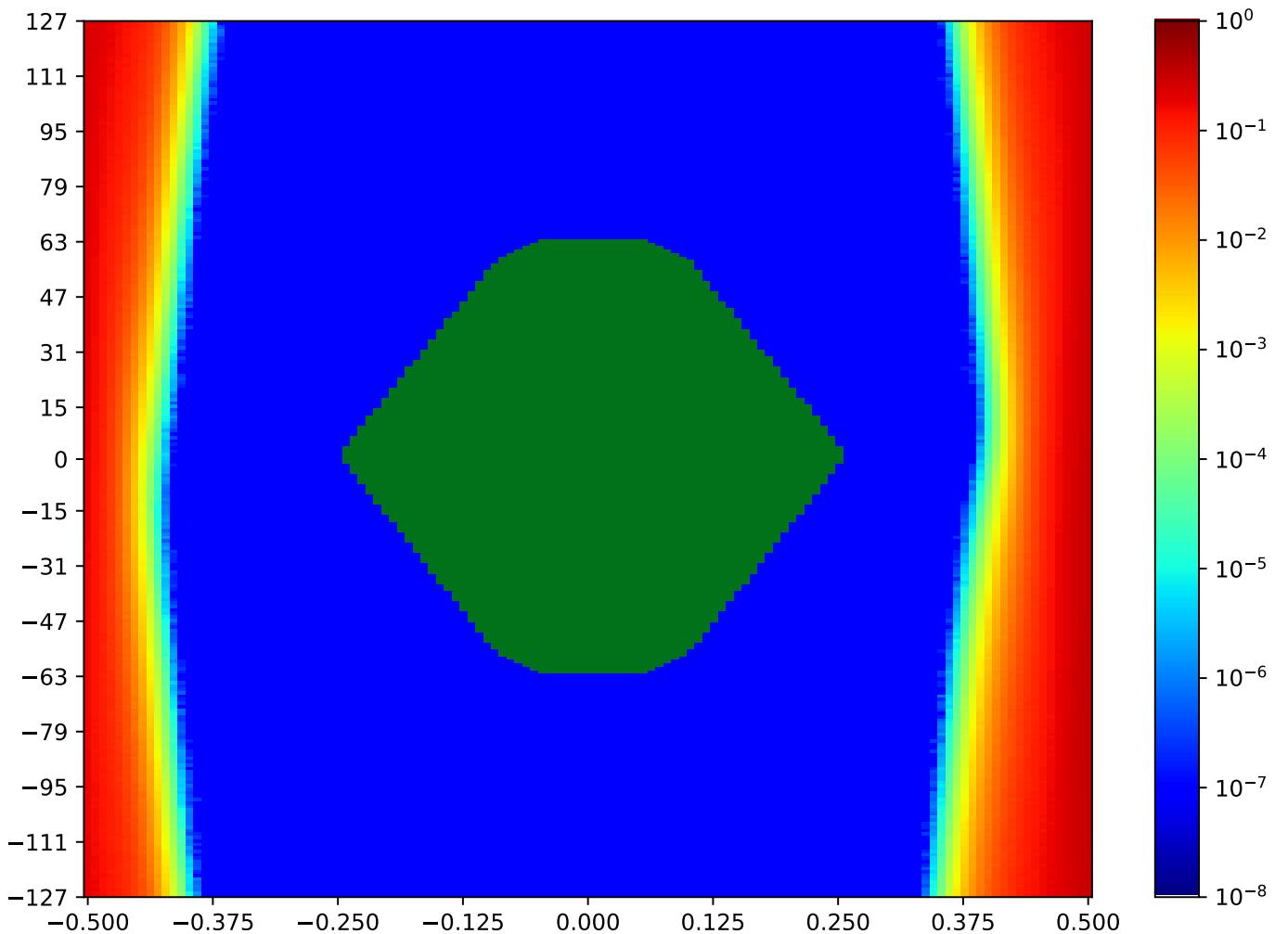


Figure 4.155: MSP_C_FPGA-TX3-01-RX8-01-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.3 MSP_C_FPGA-TX3-02-RX8-02-MSP_A_FPGA

Table 4.144: MSP_C_FPGA-TX3-02-RX8-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:29:08		2018-Sep-26 19:30:23	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24652	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

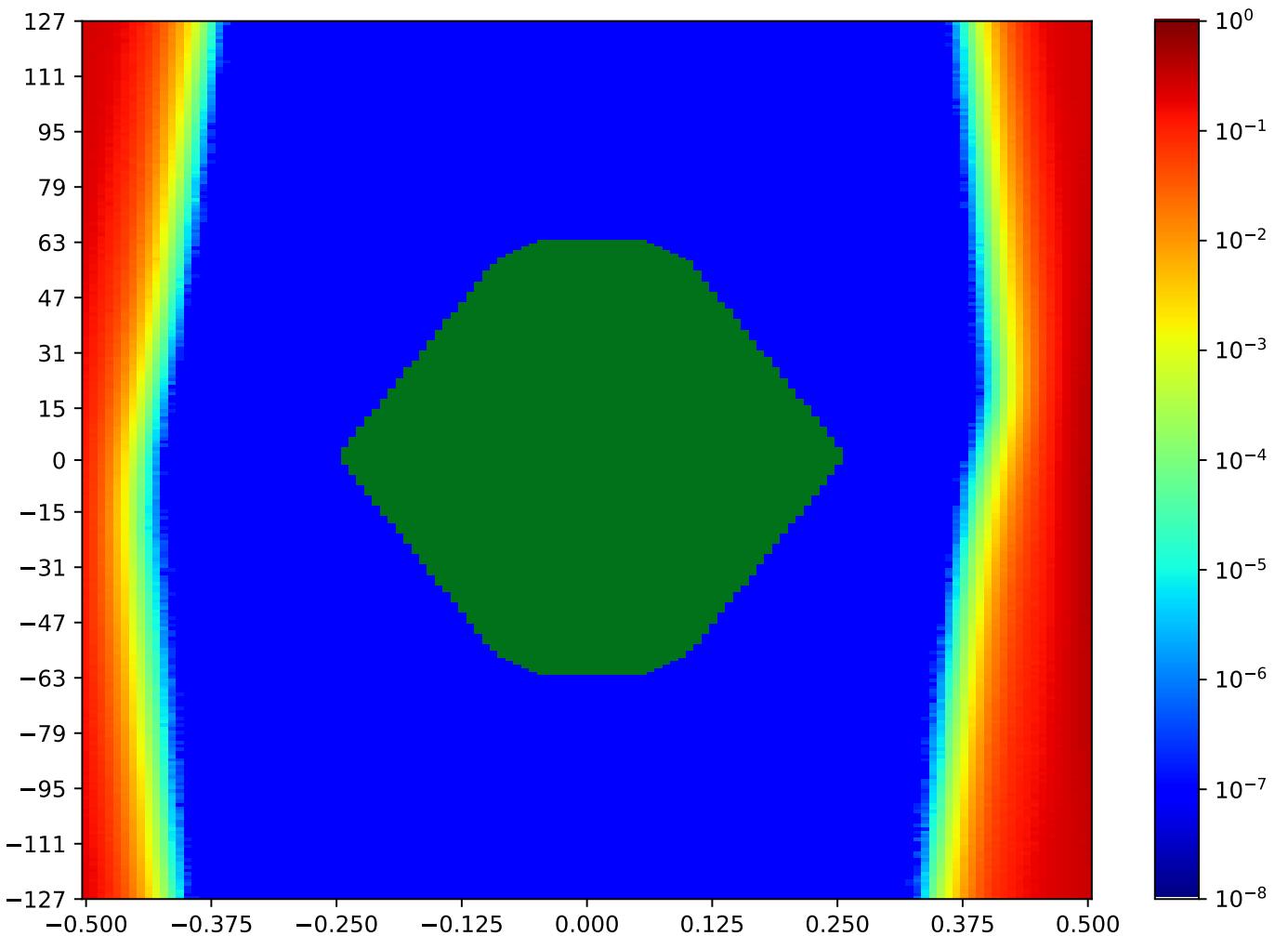


Figure 4.156: MSP_C_FPGA-TX3-02-RX8-02-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.4 MSP_C_FPGA-TX3-03-RX8-03-MSP_A_FPGA

Table 4.145: MSP_C_FPGA-TX3-03-RX8-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:22:53		2018-Sep-26 19:24:08	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24709	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

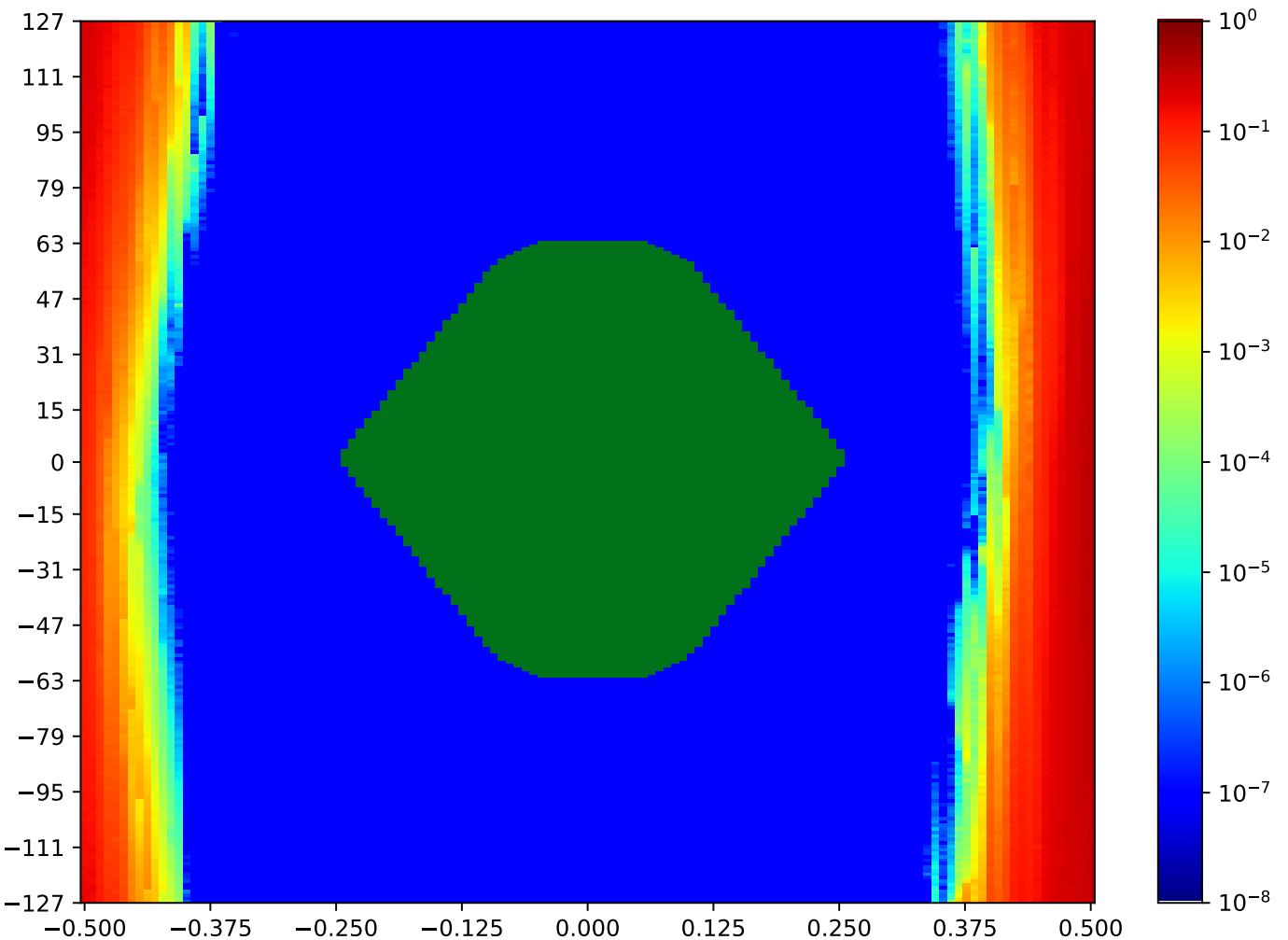


Figure 4.157: MSP_C_FPGA-TX3-03-RX8-03-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.5 MSP_C_FPGA-TX3-04-RX8-04-MSP_A_FPGA

Table 4.146: MSP_C_FPGA-TX3-04-RX8-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:32:51		2018-Sep-26 19:34:06	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24249	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

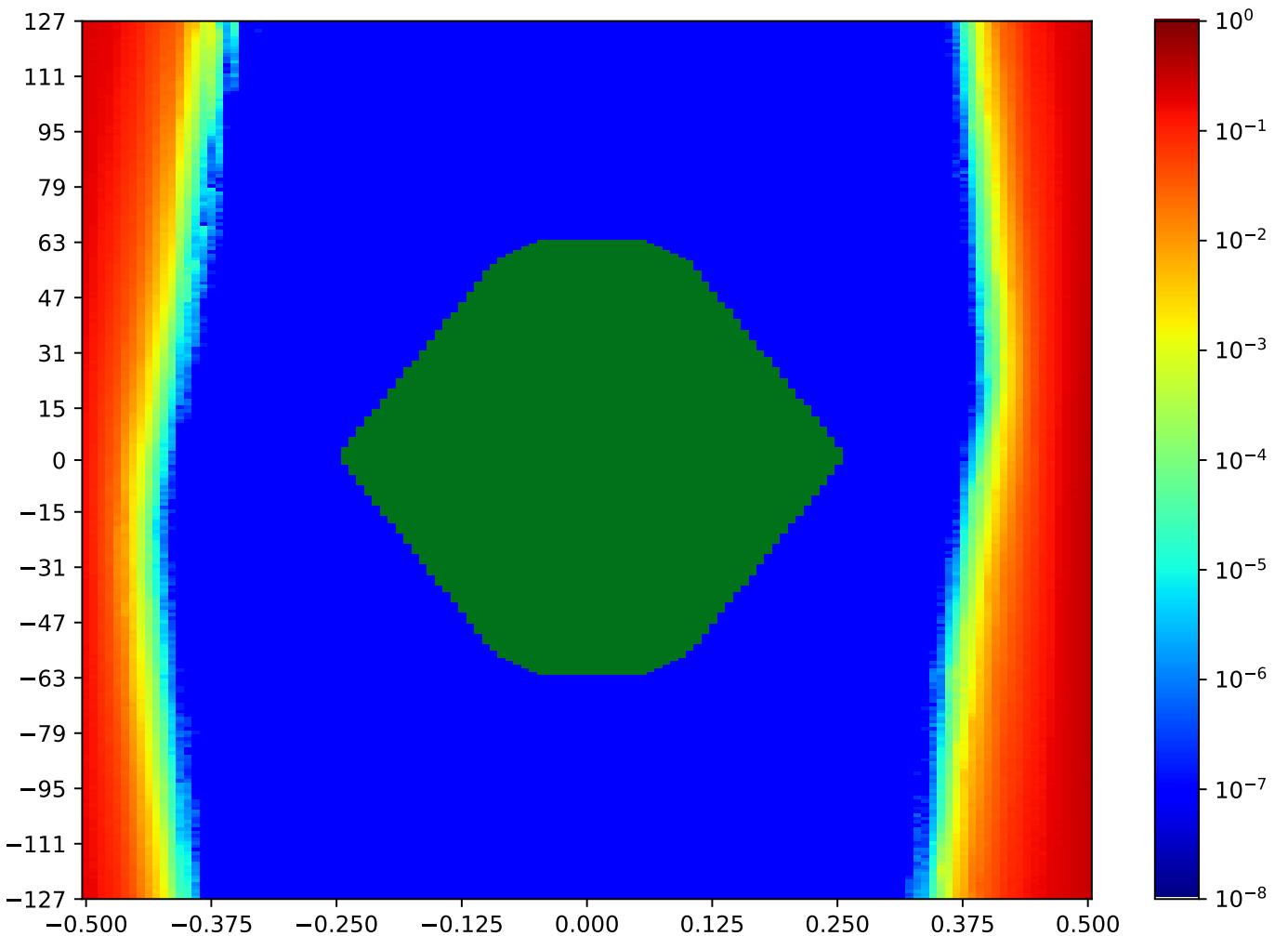


Figure 4.158: MSP_C_FPGA-TX3-04-RX8-04-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.6 MSP_C_FPGA-TX3-05-RX8-05-MSP_A_FPGA

Table 4.147: MSP_C_FPGA-TX3-05-RX8-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:21:37		2018-Sep-26 19:22:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24870	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

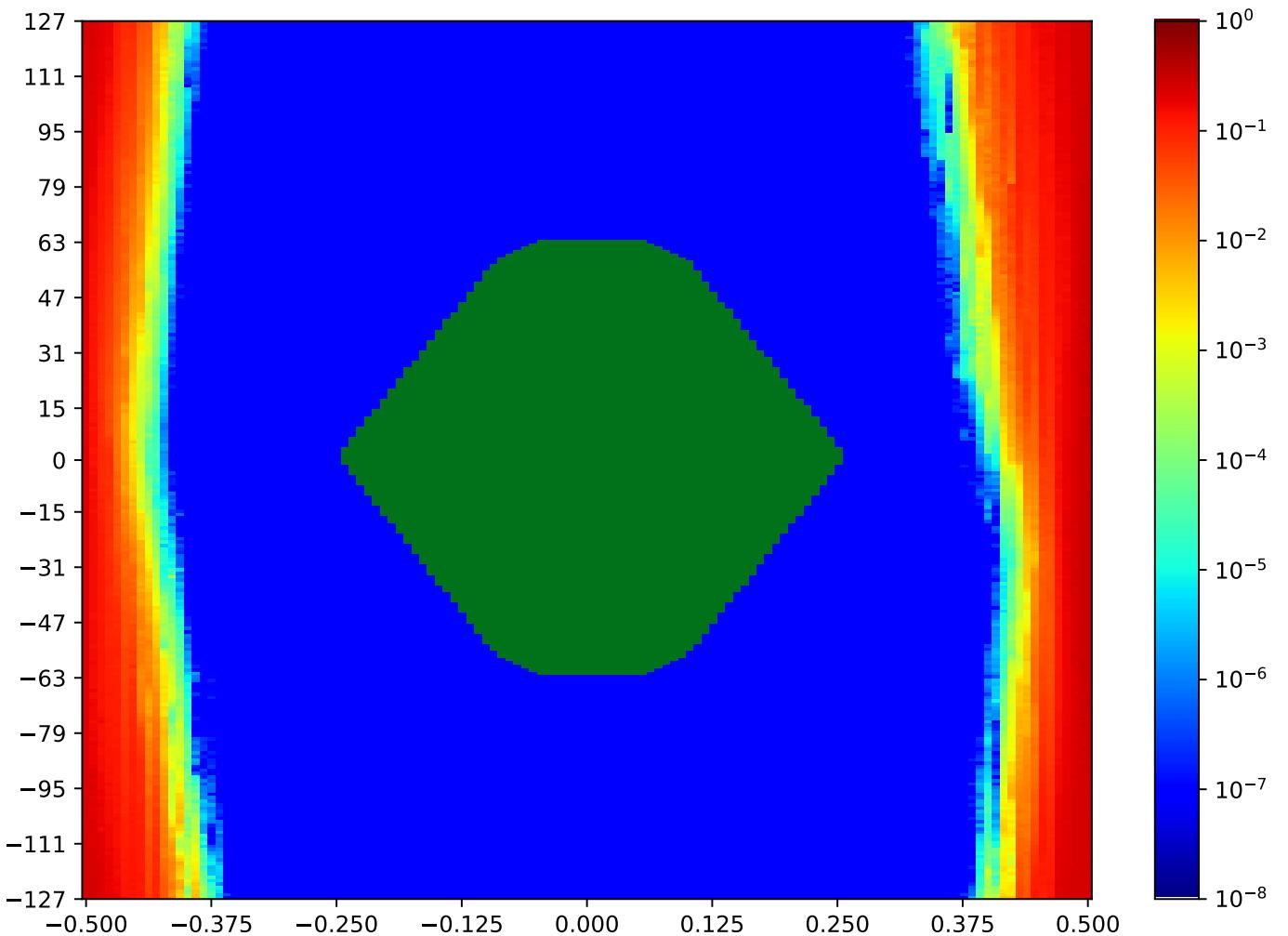


Figure 4.159: MSP_C_FPGA-TX3-05-RX8-05-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.7 MSP_C_FPGA-TX3-06-RX8-06-MSP_A_FPGA

Table 4.148: MSP_C_FPGA-TX3-06-RX8-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:35:20		2018-Sep-26 19:36:35	
Reset RX	OA	HO		VO	VO (%)
true	23838	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

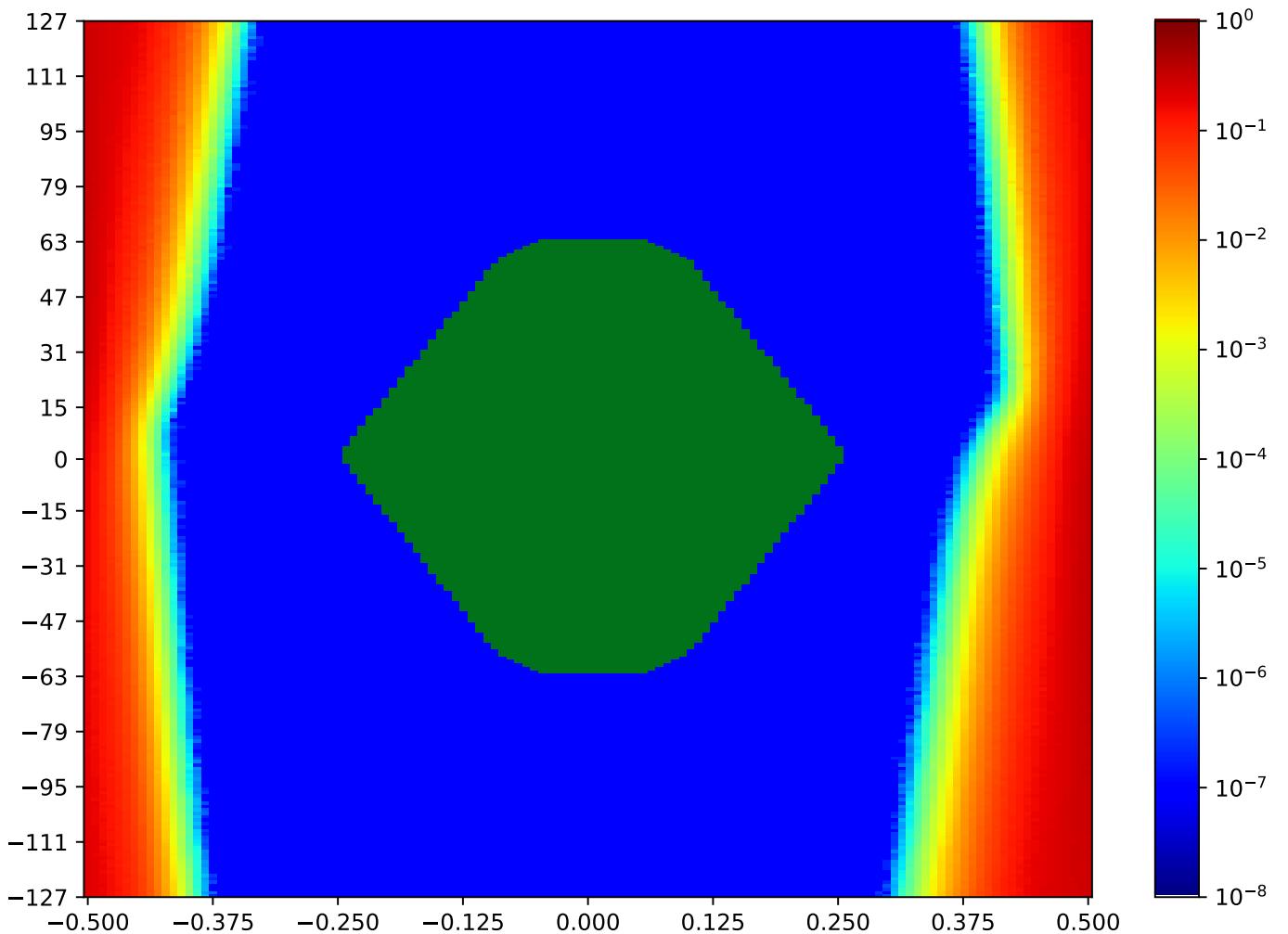


Figure 4.160: MSP_C_FPGA-TX3-06-RX8-06-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.8 MSP_C_FPGA-TX3-07-RX8-07-MSP_A_FPGA

Table 4.149: MSP_C_FPGA-TX3-07-RX8-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:24:08		2018-Sep-26 19:25:23	
Reset RX	OA	HO		VO	VO (%)
true	24542	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

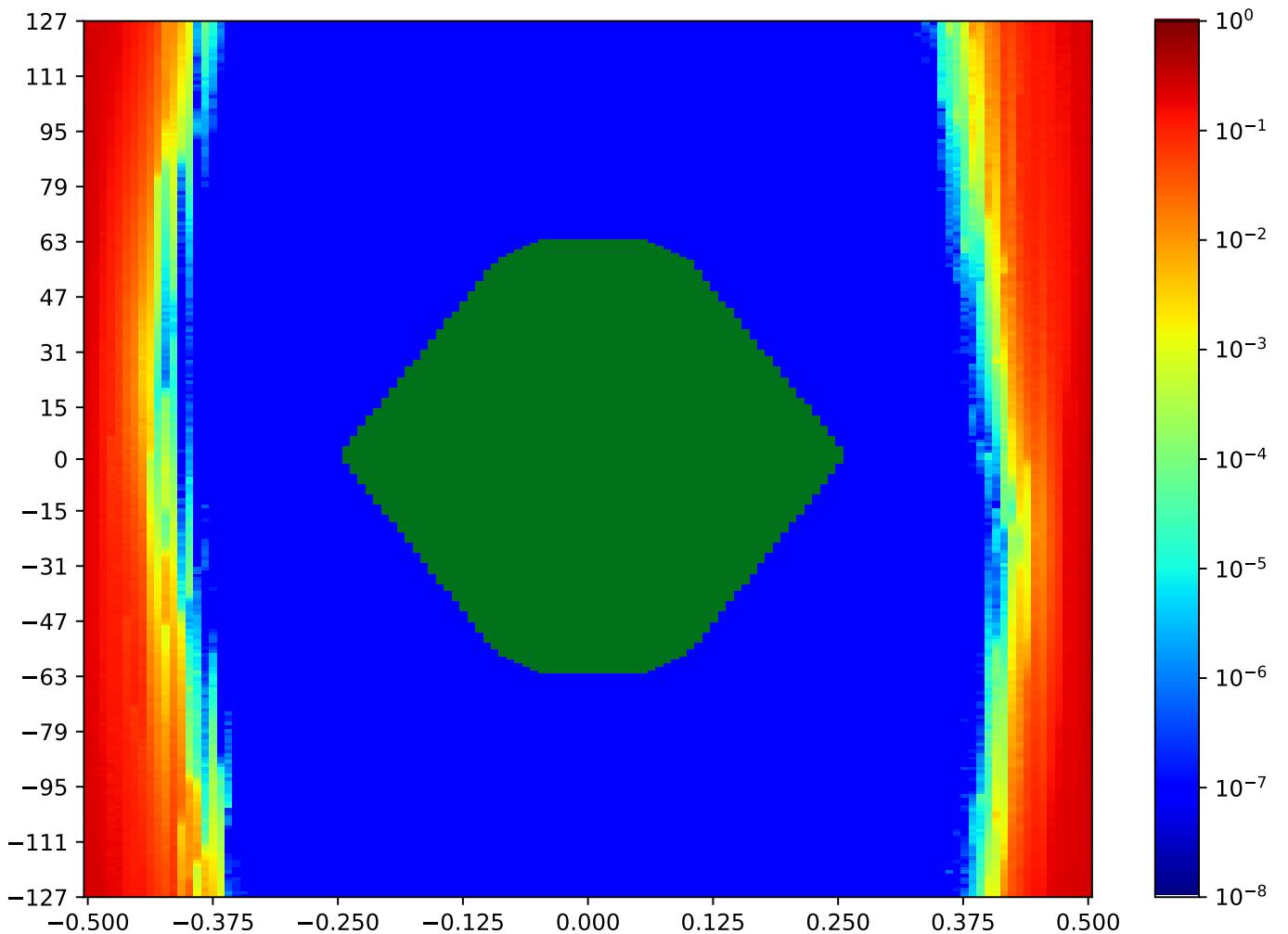


Figure 4.161: MSP_C_FPGA-TX3-07-RX8-07-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.9 MSP_C_FPGA-TX3-08-RX8-08-MSP_A_FPGA

Table 4.150: MSP_C_FPGA-TX3-08-RX8-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:34:06		2018-Sep-26 19:35:20	
Reset RX	OA	HO		VO	VO (%)
true	23939	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

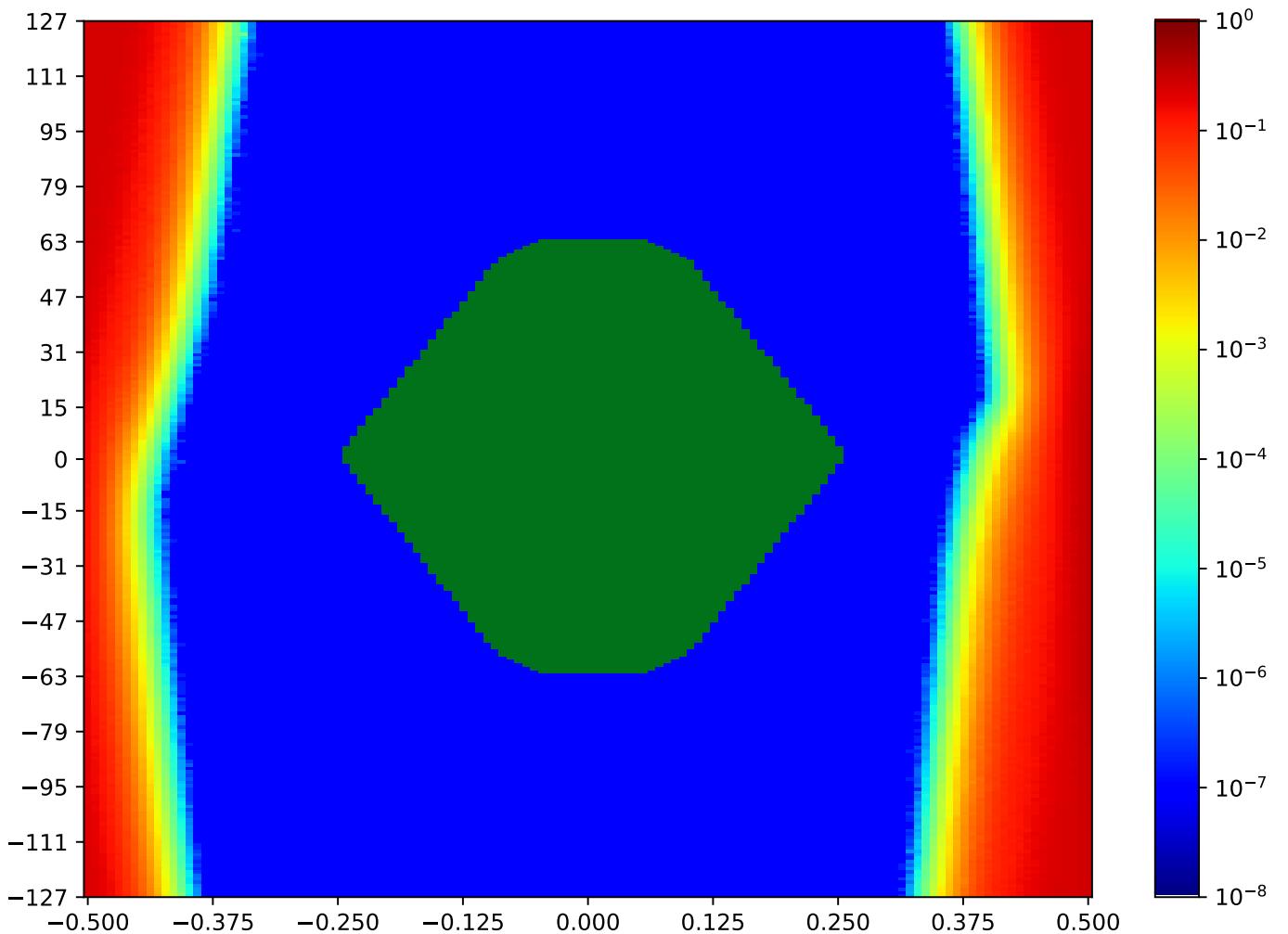


Figure 4.162: MSP_C_FPGA-TX3-08-RX8-08-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.10 MSP_C_FPGA-TX3-09-RX8-09-MSP_A_FPGA

Table 4.151: MSP_C_FPGA-TX3-09-RX8-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:26:39		2018-Sep-26 19:27:53	
Reset RX	OA	HO		VO	VO (%)
true	24312	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

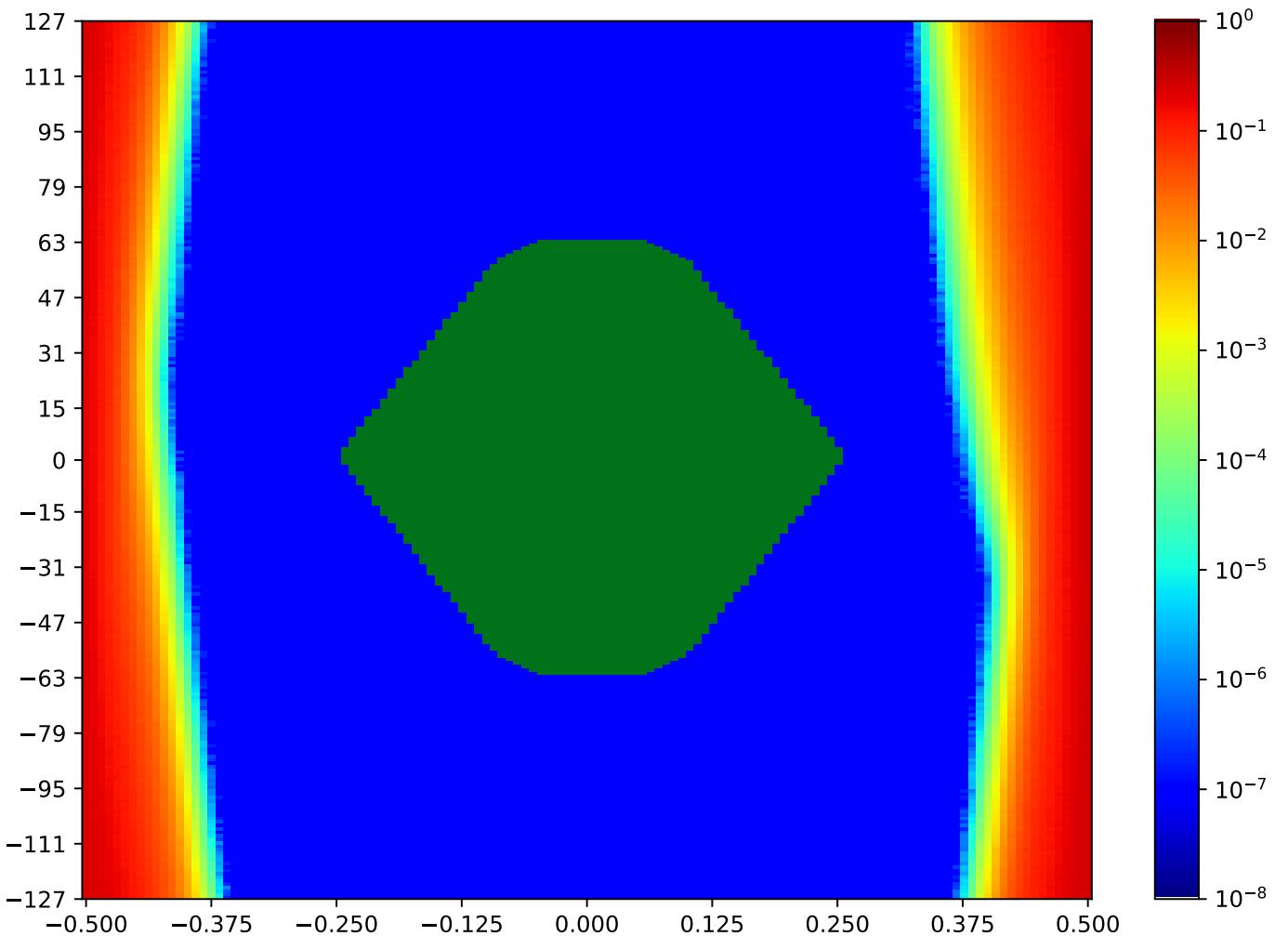


Figure 4.163: MSP_C_FPGA-TX3-09-RX8-09-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.11 MSP_C_FPGA-TX3-10-RX8-10-MSP_A_FPGA

Table 4.152: MSP_C_FPGA-TX3-10-RX8-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:31:37		2018-Sep-26 19:32:51	
Reset RX	OA	HO		VO	VO (%)
true	23773	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

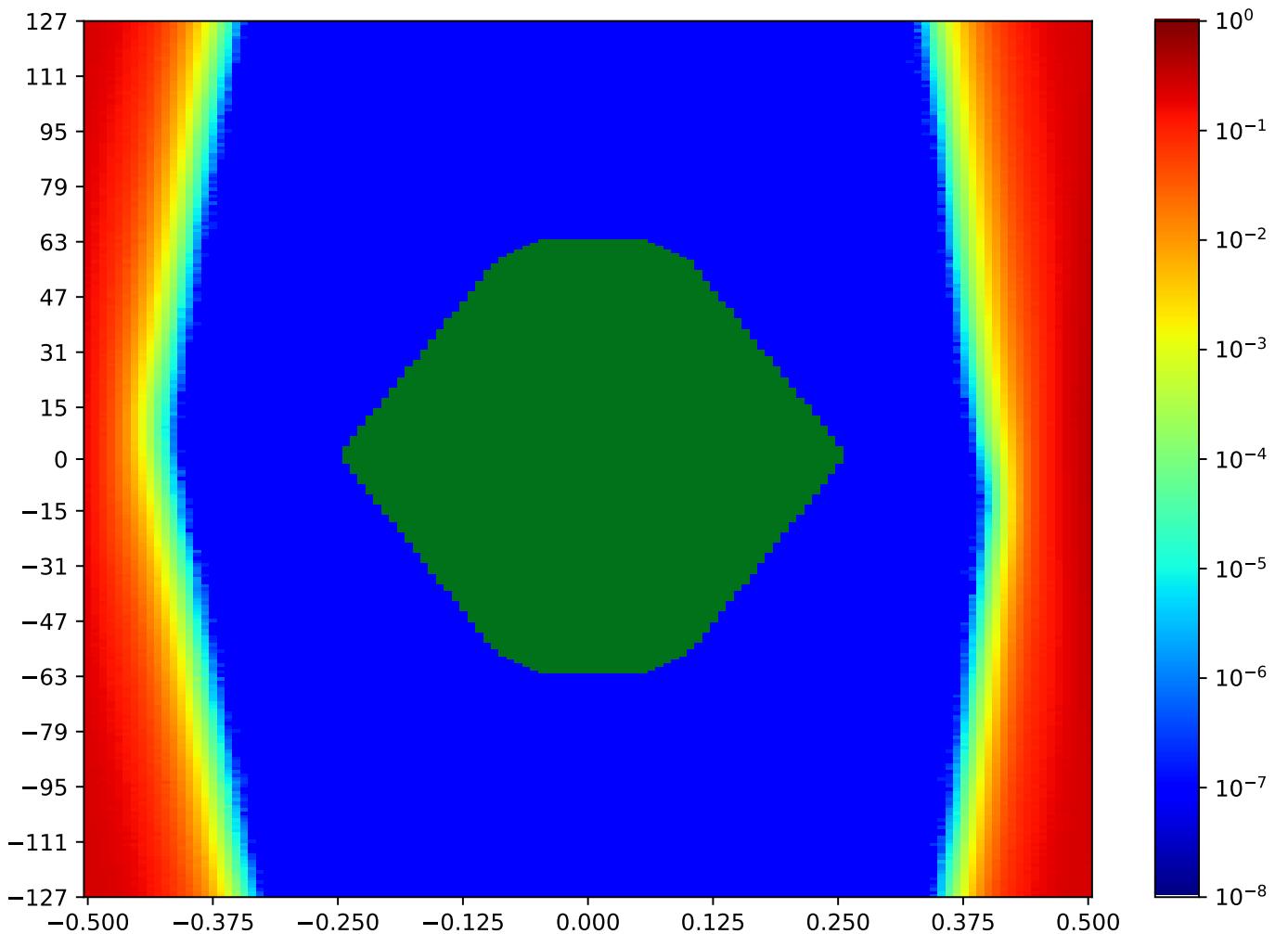


Figure 4.164: MSP_C_FPGA-TX3-10-RX8-10-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.12.12 MSP_C_FPGA-TX3-11-RX8-11-MSP_A_FPGA

Table 4.153: MSP_C_FPGA-TX3-11-RX8-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:30:23		2018-Sep-26 19:31:37	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23812	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

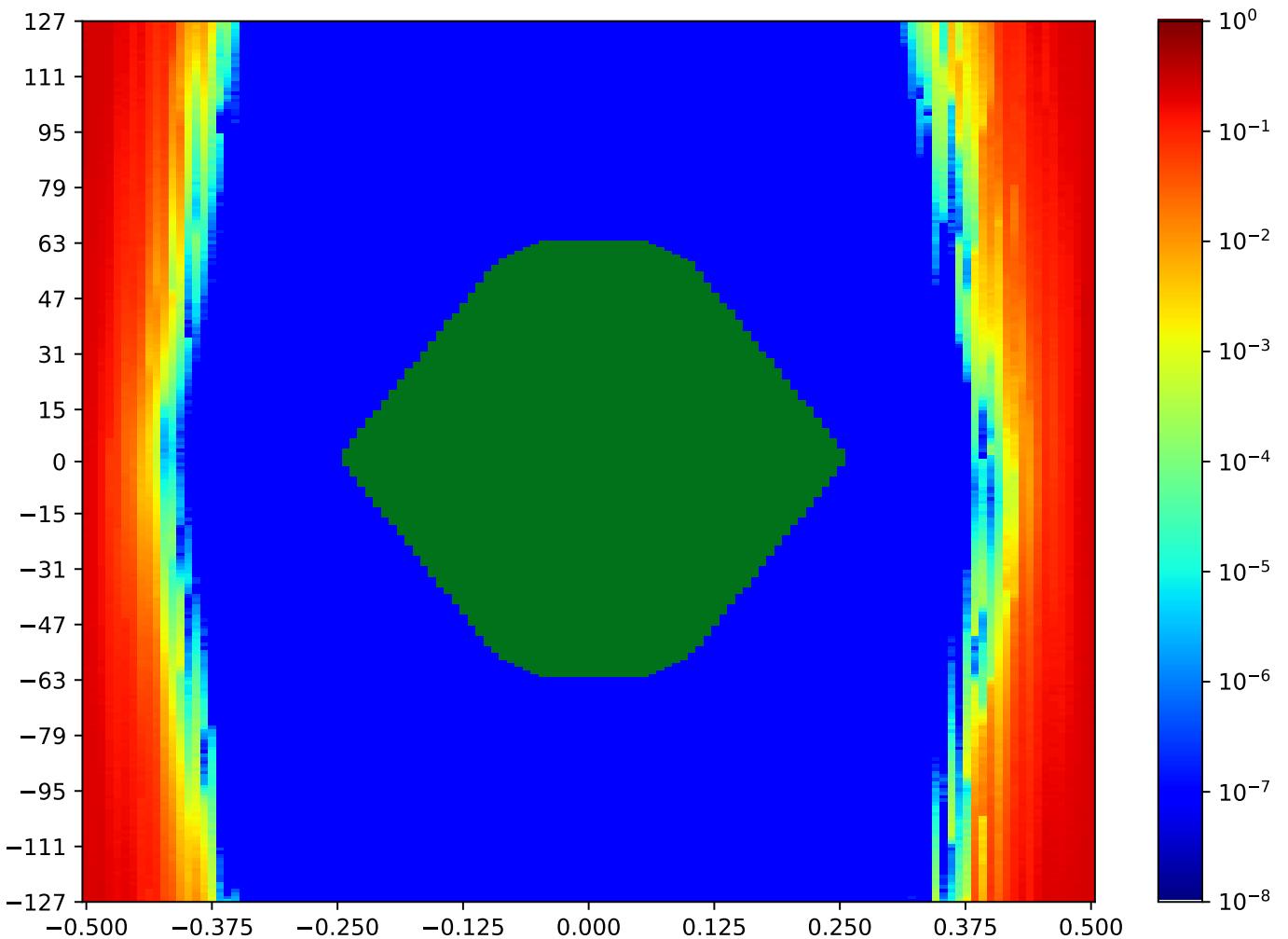


Figure 4.165: MSP_C_FPGA-TX3-11-RX8-11-MSP_A_FPGA

Call back to summary Figure 4.153. Sibling eye diagrams: V2-12.8.

4.13 MSP_C TX4 MSP_A RX9 Minipod Loopback

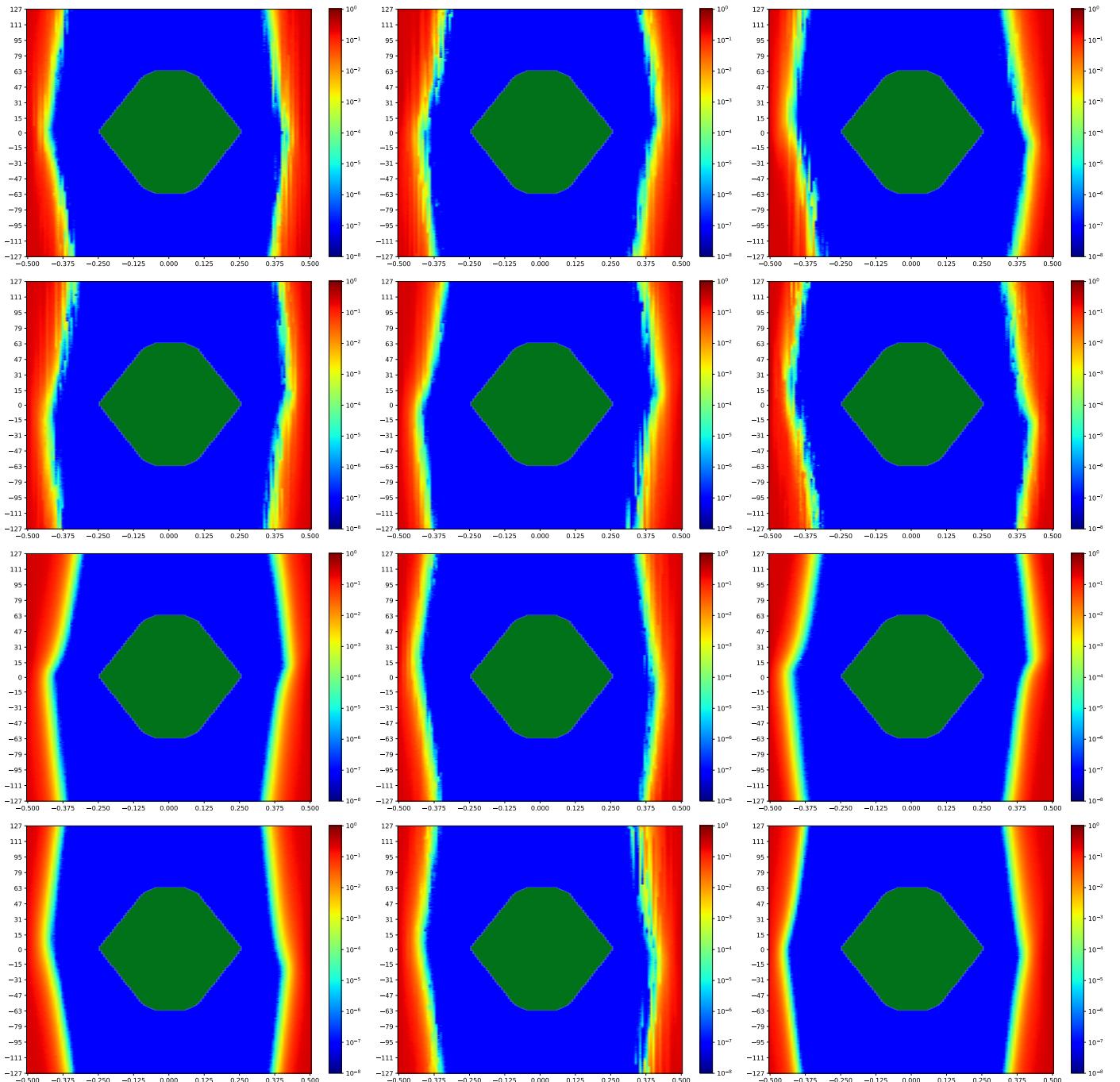


Figure 4.166: MSP_C TX4 MSP_A RX9 Minipod Loopback

A cross-reference to Figure 4.166. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.179.

4.13.1 MSP_C_FPGA-TX4-00-RX9-00-MSP_A_FPGA

Table 4.154: MSP_C_FPGA-TX4-00-RX9-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:40:17		2018-Sep-26 19:41:30	
Reset RX	OA	HO		VO	VO (%)
true	23864	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

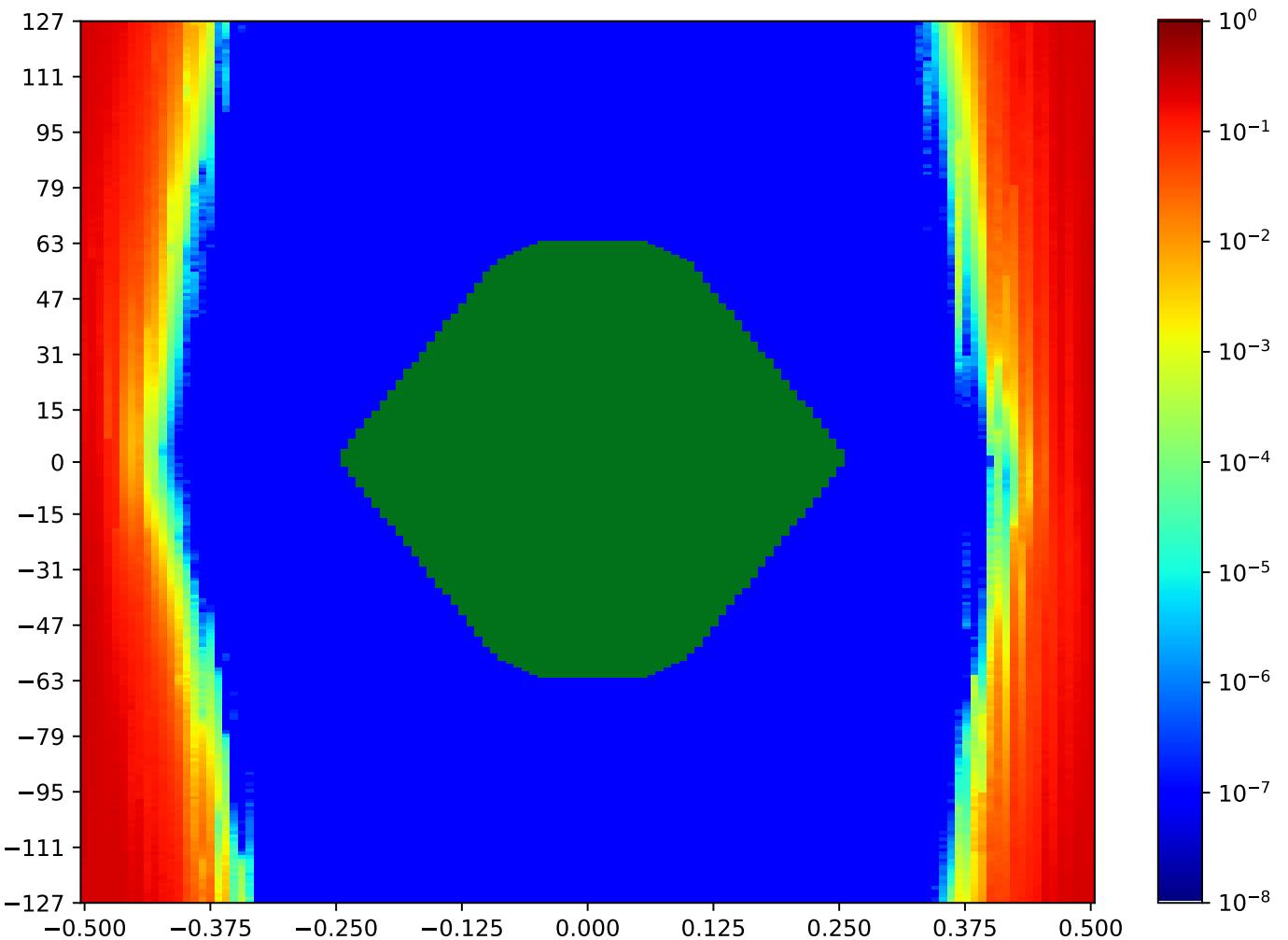


Figure 4.167: MSP_C_FPGA-TX4-00-RX9-00-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.2 MSP_C_FPGA-TX4-01-RX9-01-MSP_A_FPGA

Table 4.155: MSP_C_FPGA-TX4-01-RX9-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:37:50		2018-Sep-26 19:39:03	
Reset RX	OA	HO		VO	VO (%)
true	23327	99		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

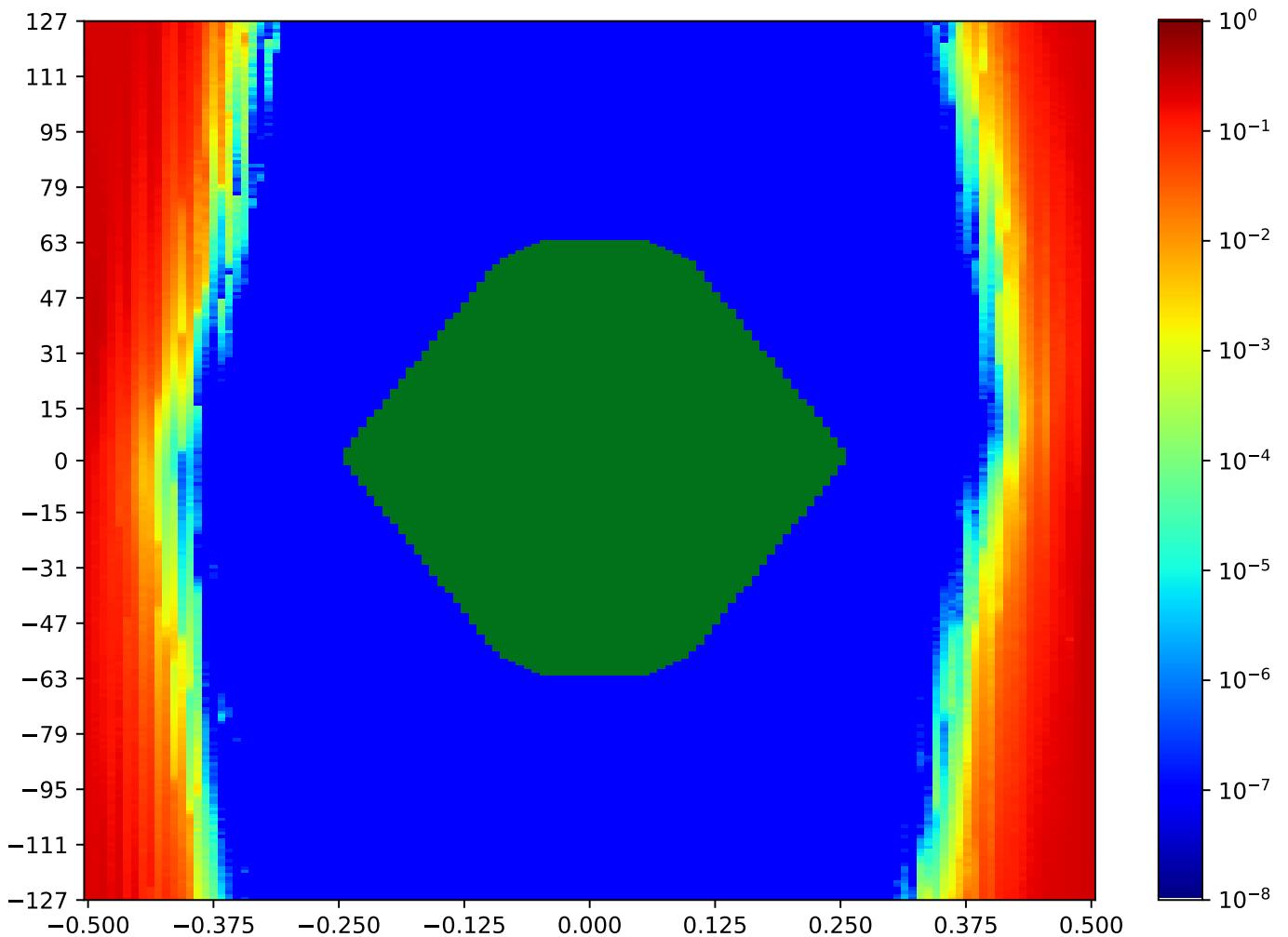


Figure 4.168: MSP_C_FPGA-TX4-01-RX9-01-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.3 MSP_C_FPGA-TX4-02-RX9-02-MSP_A_FPGA

Table 4.156: MSP_C_FPGA-TX4-02-RX9-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:44:00		2018-Sep-26 19:45:14	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23292	101		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

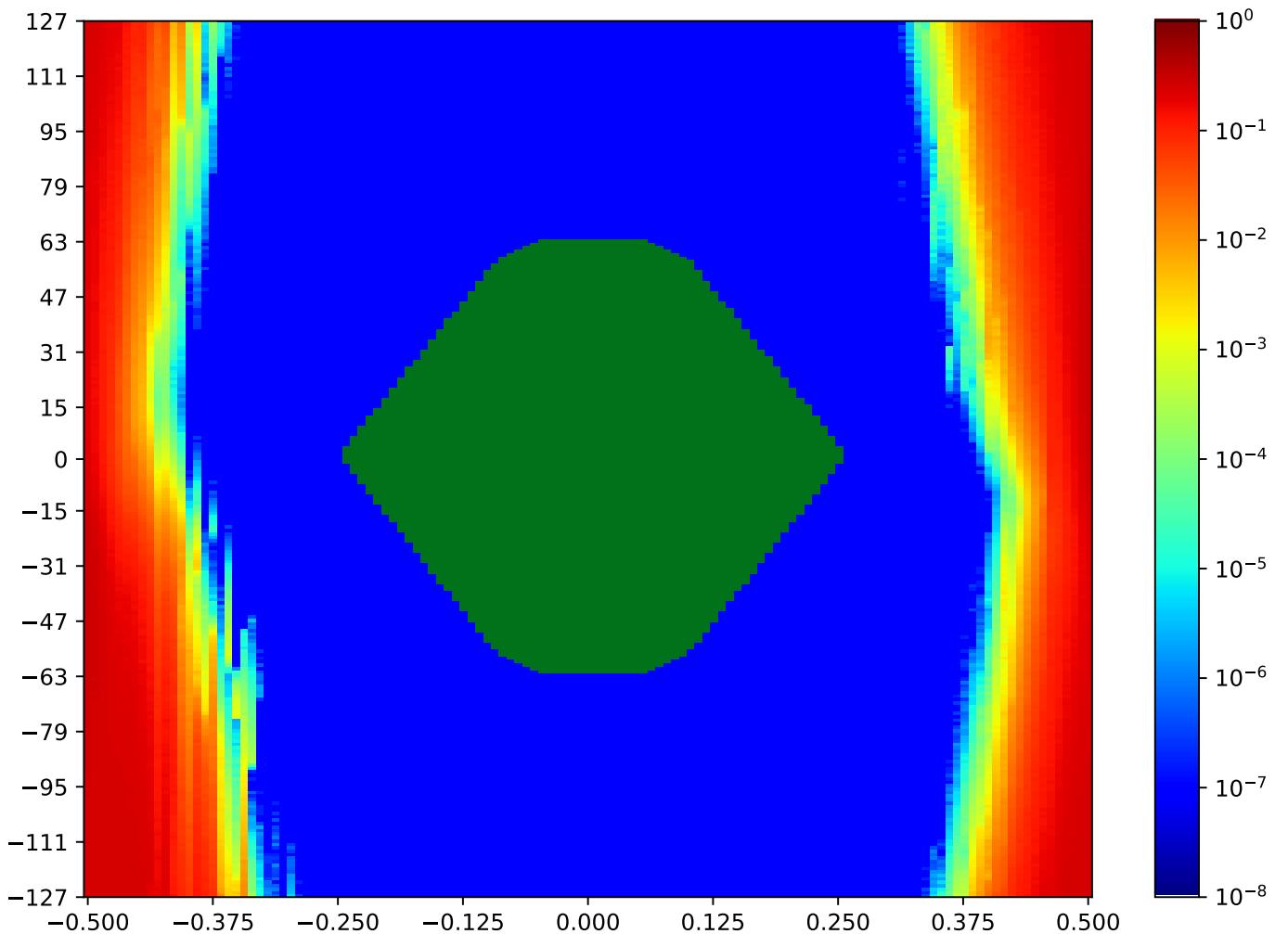


Figure 4.169: MSP_C_FPGA-TX4-02-RX9-02-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.4 MSP_C_FPGA-TX4-03-RX9-03-MSP_A_FPGA

Table 4.157: MSP_C_FPGA-TX4-03-RX9-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:36:35		2018-Sep-26 19:37:50	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23795	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

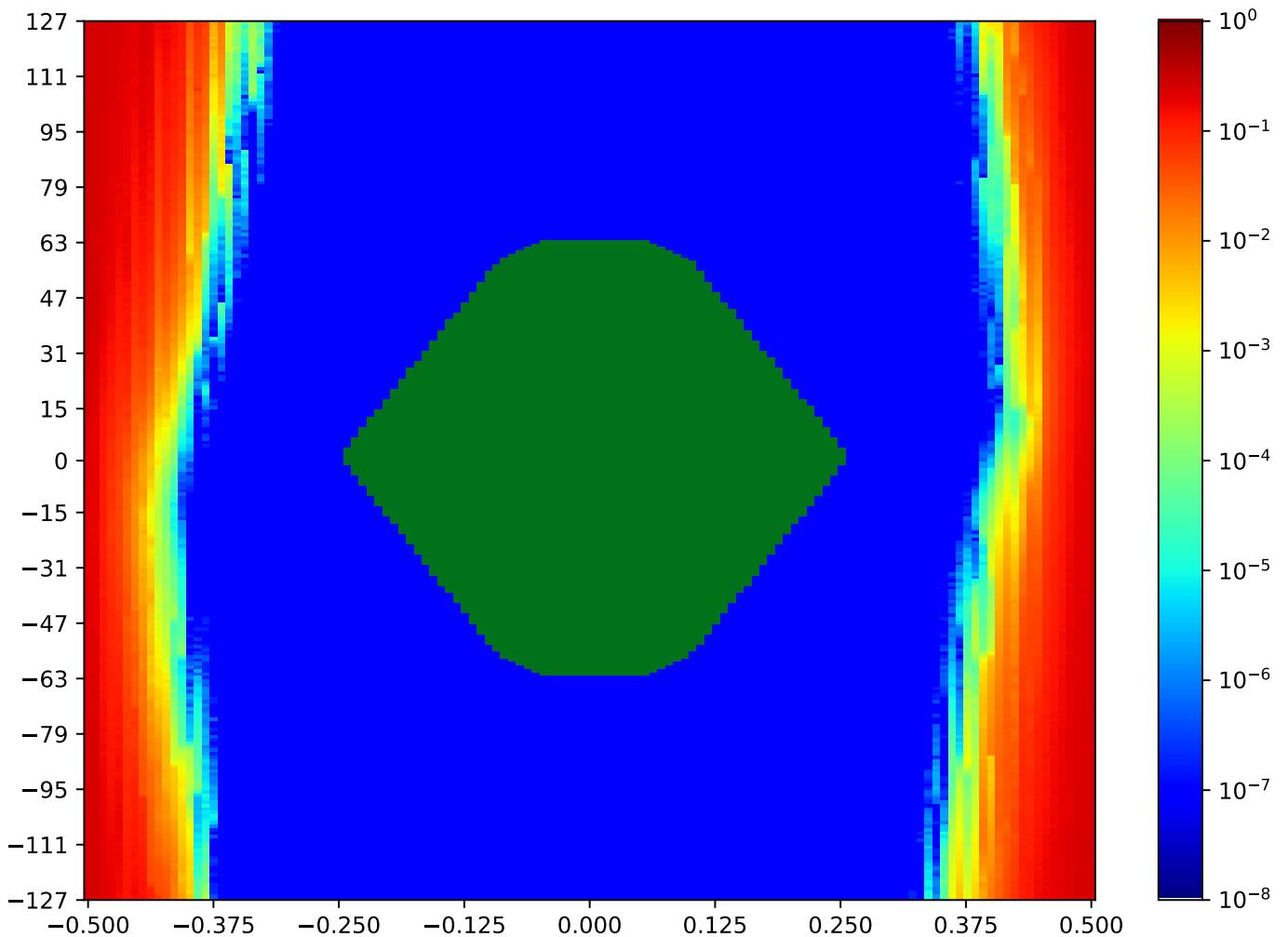


Figure 4.170: MSP_C_FPGA-TX4-03-RX9-03-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.5 MSP_C_FPGA-TX4-04-RX9-04-MSP_A_FPGA

Table 4.158: MSP_C_FPGA-TX4-04-RX9-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:47:41		2018-Sep-26 19:48:54	
Reset RX	OA	HO		VO	VO (%)
true	23410	99		75.97%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

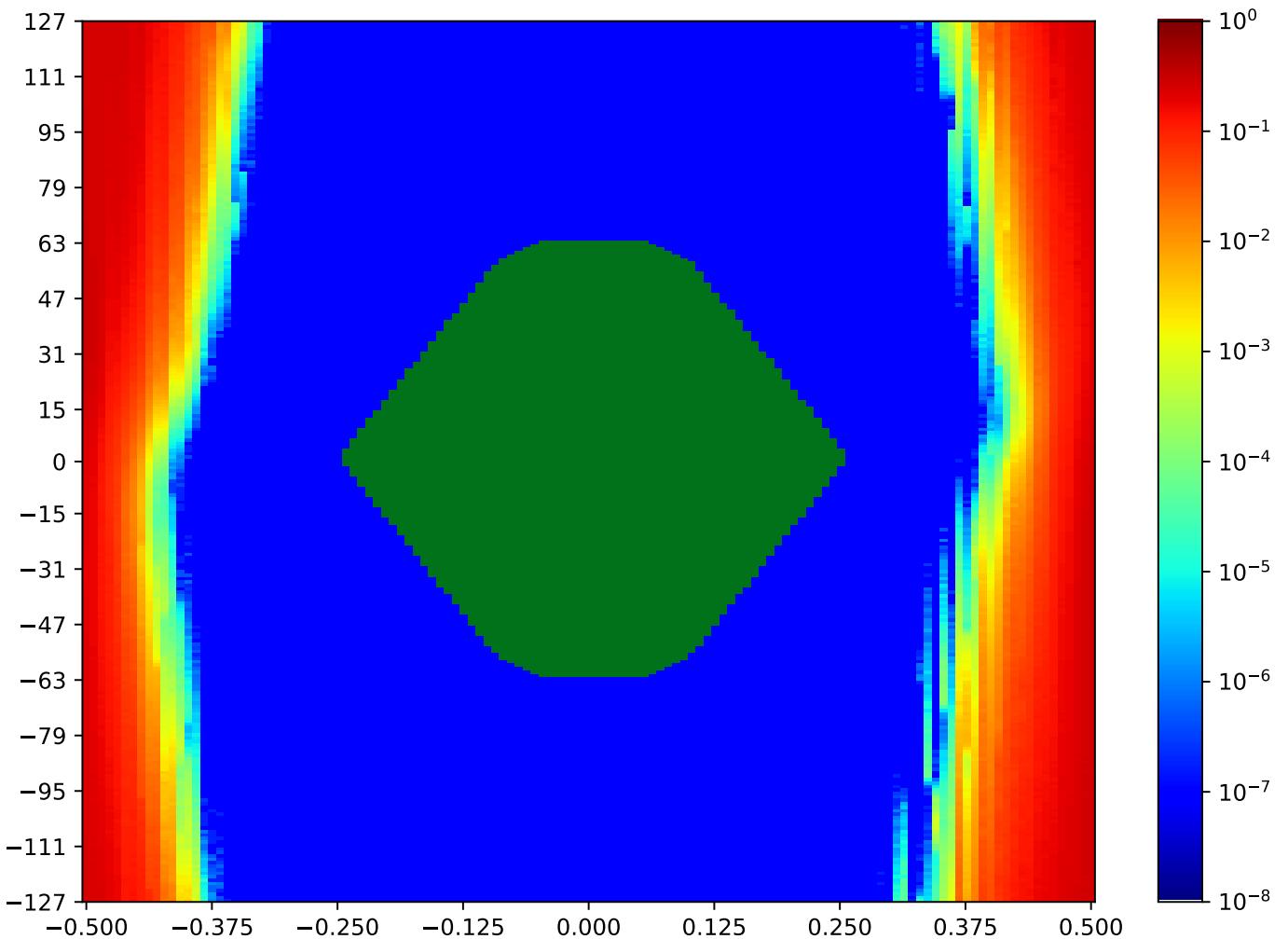


Figure 4.171: MSP_C_FPGA-TX4-04-RX9-04-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.6 MSP_C_FPGA-TX4-05-RX9-05-MSP_A_FPGA

Table 4.159: MSP_C_FPGA-TX4-05-RX9-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:39:03		2018-Sep-26 19:40:16	
Reset RX	OA	HO		VO	VO (%)
true	23629	100		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

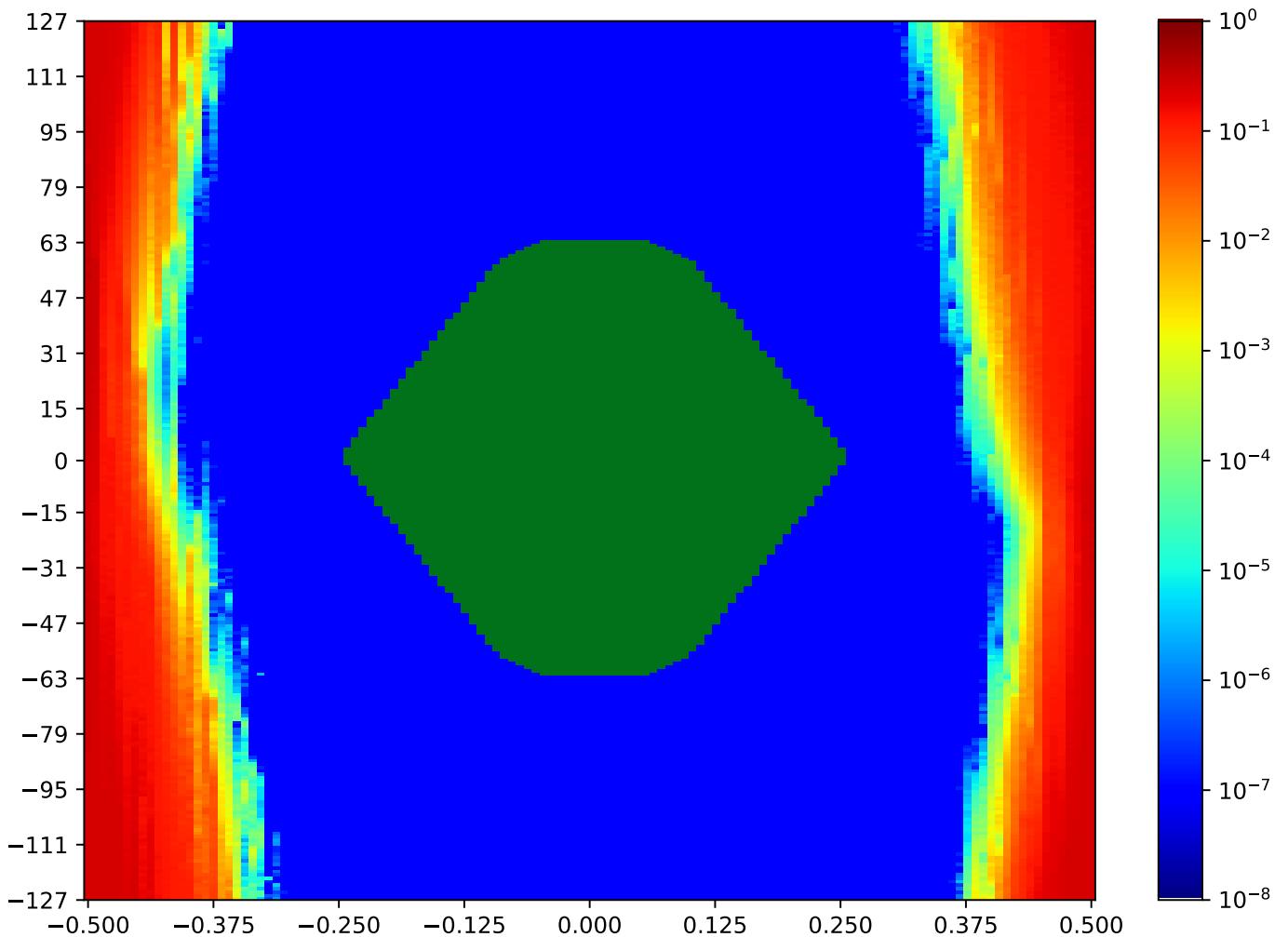


Figure 4.172: MSP_C_FPGA-TX4-05-RX9-05-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.7 MSP_C_FPGA-TX4-06-RX9-06-MSP_A_FPGA

Table 4.160: MSP_C_FPGA-TX4-06-RX9-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:50:08		2018-Sep-26 19:51:21	
Reset RX	OA	HO		VO	VO (%)
true	23291	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

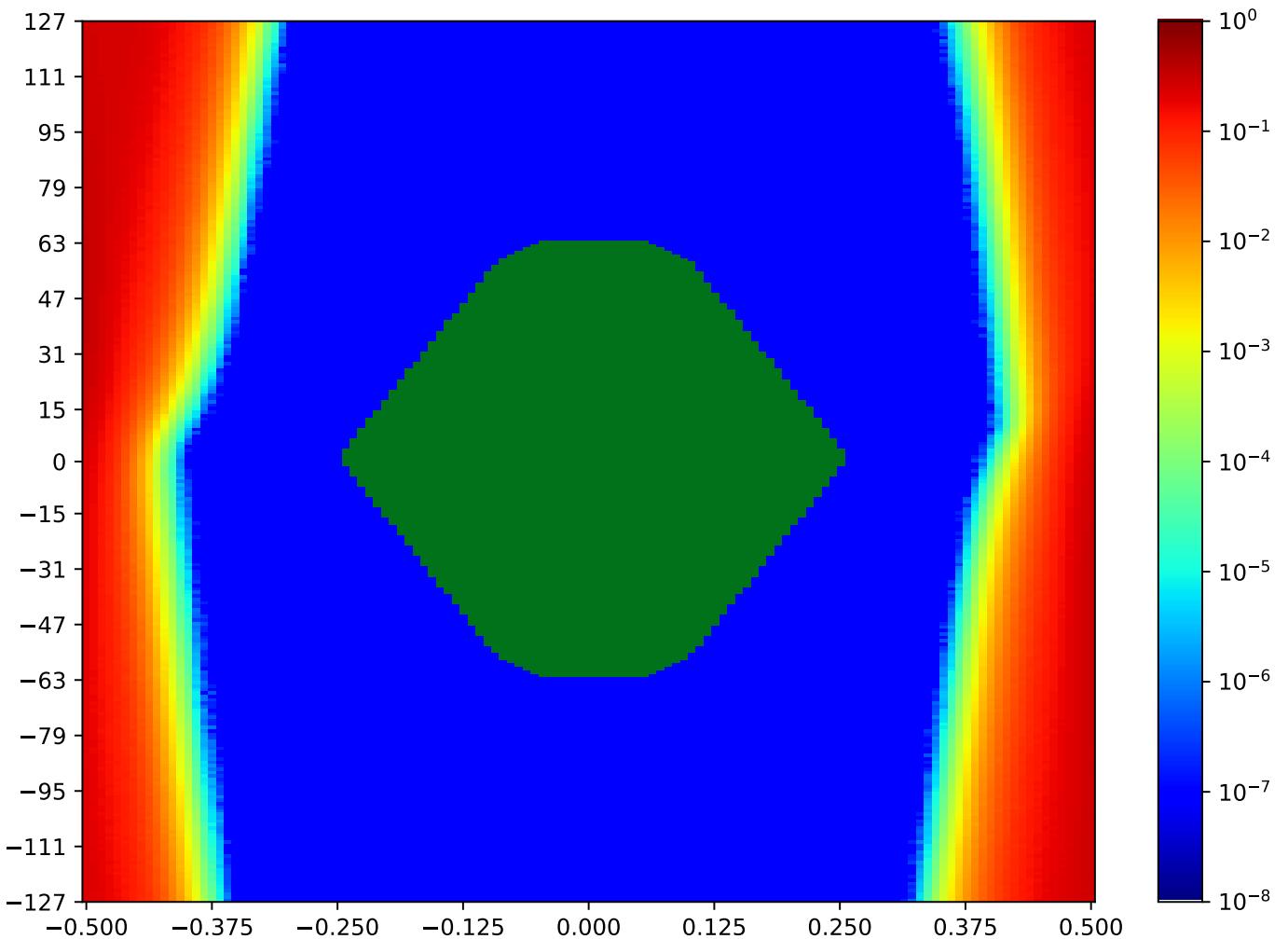


Figure 4.173: MSP_C_FPGA-TX4-06-RX9-06-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.8 MSP_C_FPGA-TX4-07-RX9-07-MSP_A_FPGA

Table 4.161: MSP_C_FPGA-TX4-07-RX9-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:41:31		2018-Sep-26 19:42:45	
Reset RX	OA	HO		VO	VO (%)
true	24013	100		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

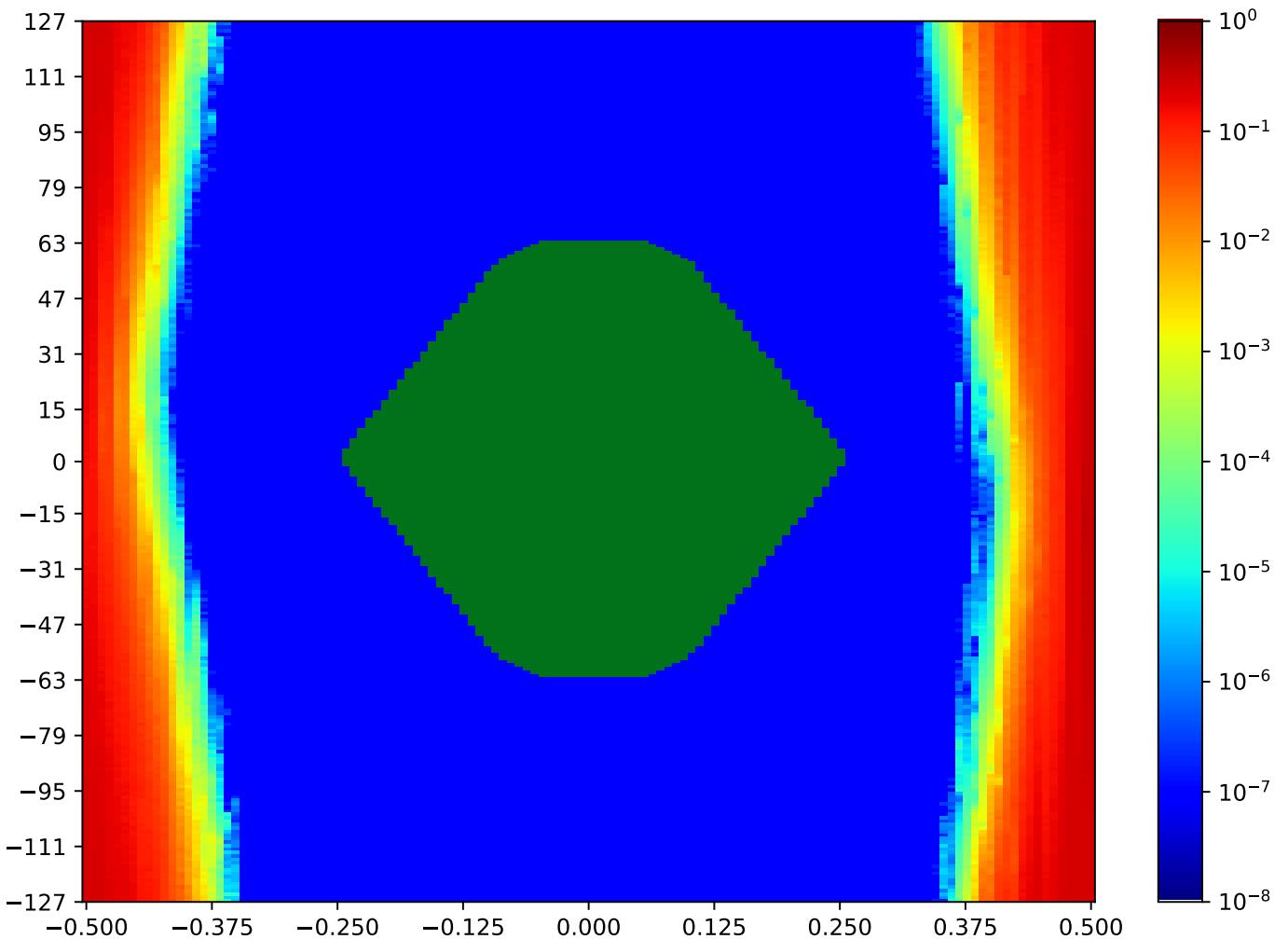


Figure 4.174: MSP_C_FPGA-TX4-07-RX9-07-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.9 MSP_C_FPGA-TX4-08-RX9-08-MSP_A_FPGA

Table 4.162: MSP_C_FPGA-TX4-08-RX9-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:48:54		2018-Sep-26 19:50:08	
Reset RX	OA	HO		VO	VO (%)
true	23585	98		75.97%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

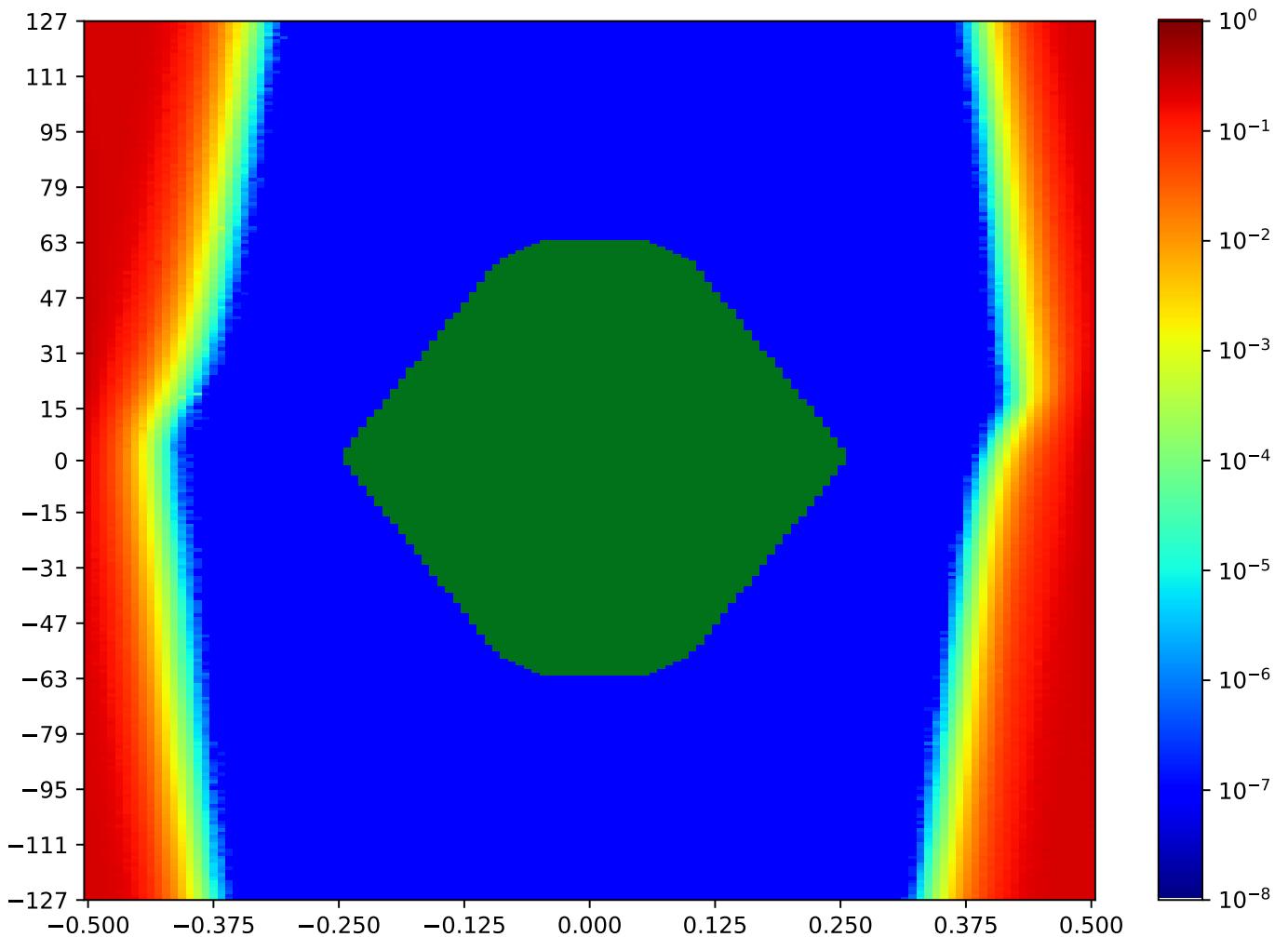


Figure 4.175: MSP_C_FPGA-TX4-08-RX9-08-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.10 MSP_C_FPGA-TX4-09-RX9-09-MSP_A_FPGA

Table 4.163: MSP_C_FPGA-TX4-09-RX9-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:42:46		2018-Sep-26 19:44:00	
Reset RX	OA	HO		VO	VO (%)
true	23722	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

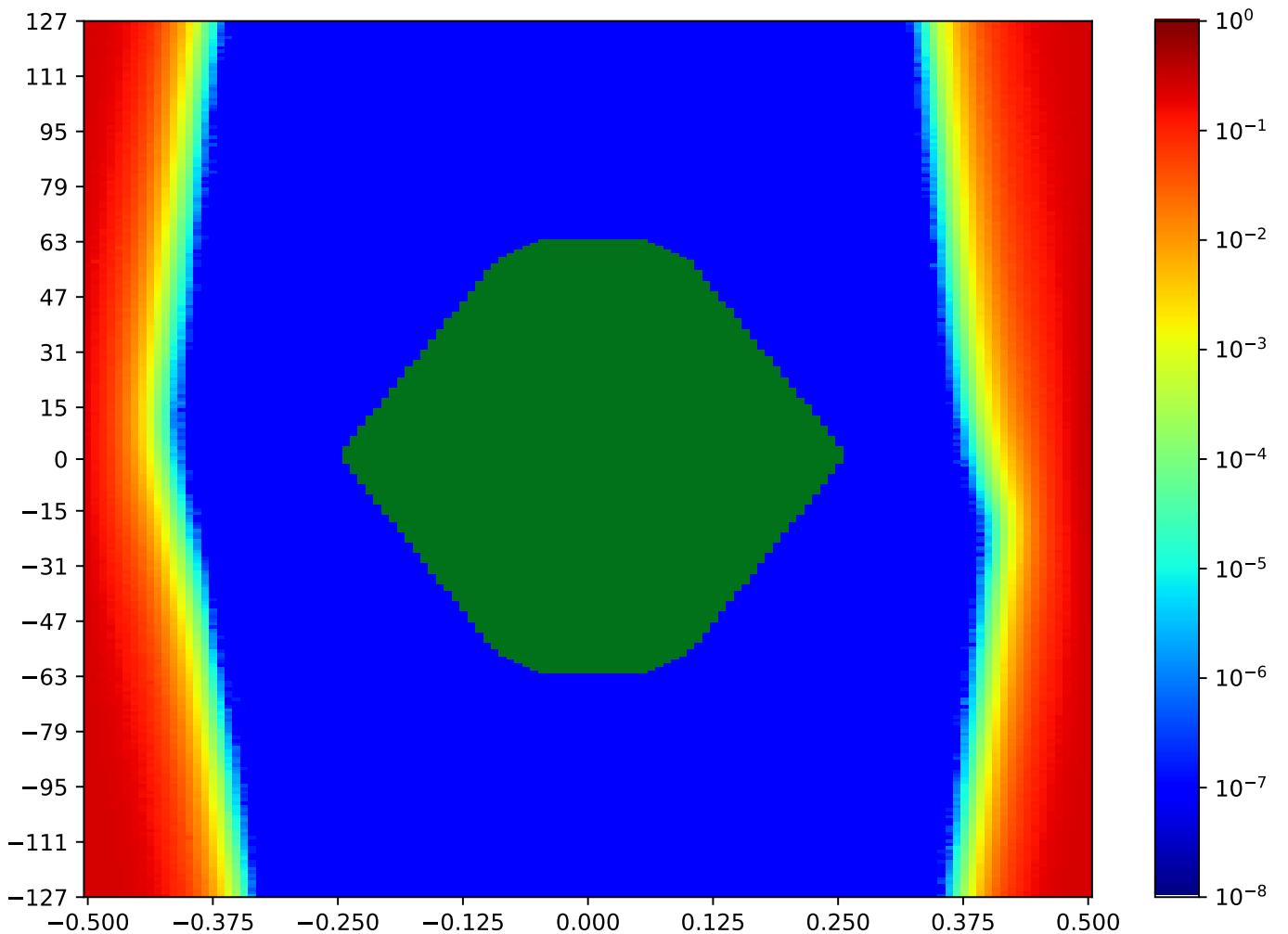


Figure 4.176: MSP_C_FPGA-TX4-09-RX9-09-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.11 MSP_C_FPGA-TX4-10-RX9-10-MSP_A_FPGA

Table 4.164: MSP_C_FPGA-TX4-10-RX9-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:46:28		2018-Sep-26 19:47:41	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	23438	98		75.97%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

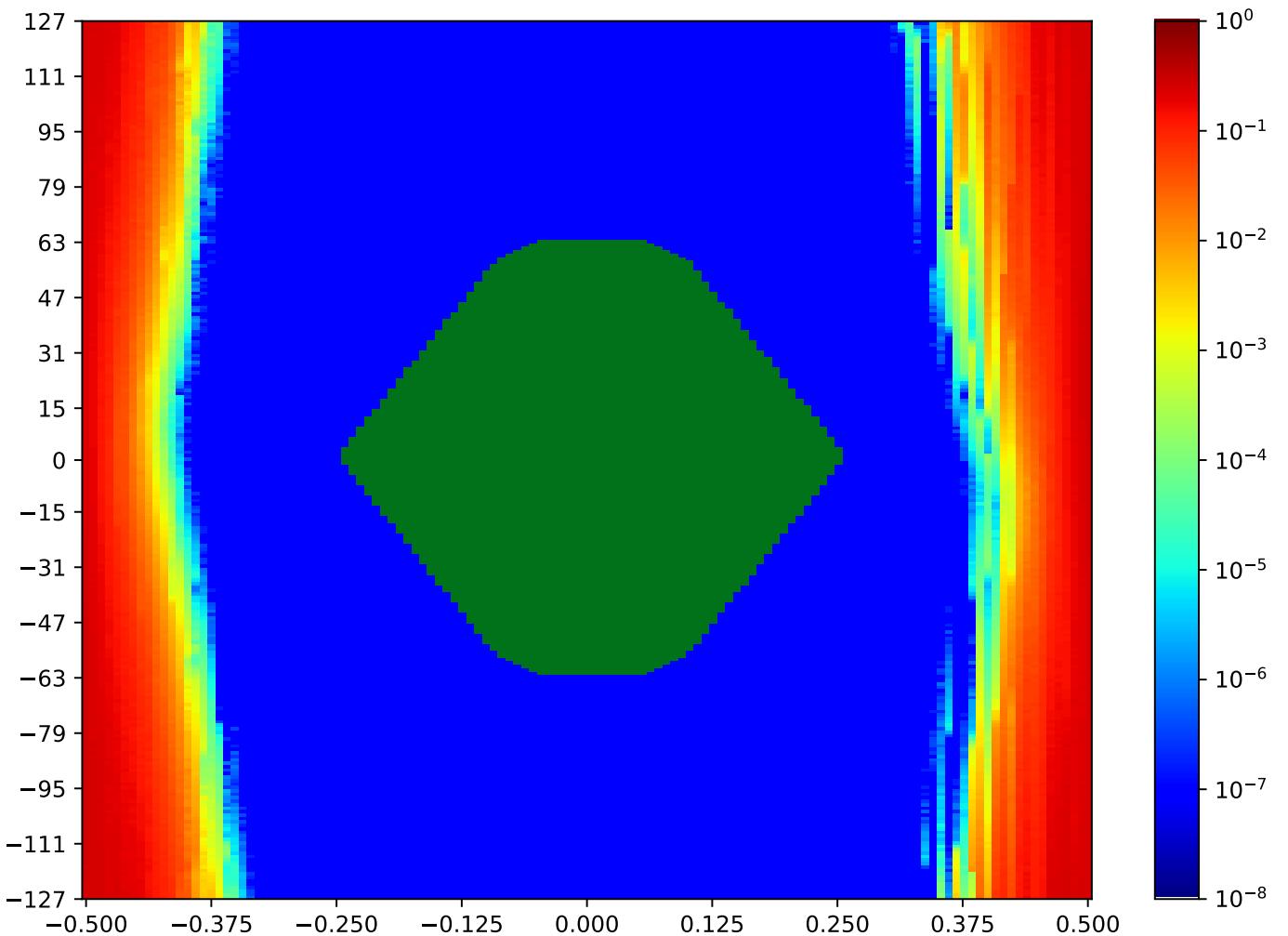


Figure 4.177: MSP_C_FPGA-TX4-10-RX9-10-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.13.12 MSP_C_FPGA-TX4-11-RX9-11-MSP_A_FPGA

Table 4.165: MSP_C_FPGA-TX4-11-RX9-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:45:14		2018-Sep-26 19:46:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24102	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

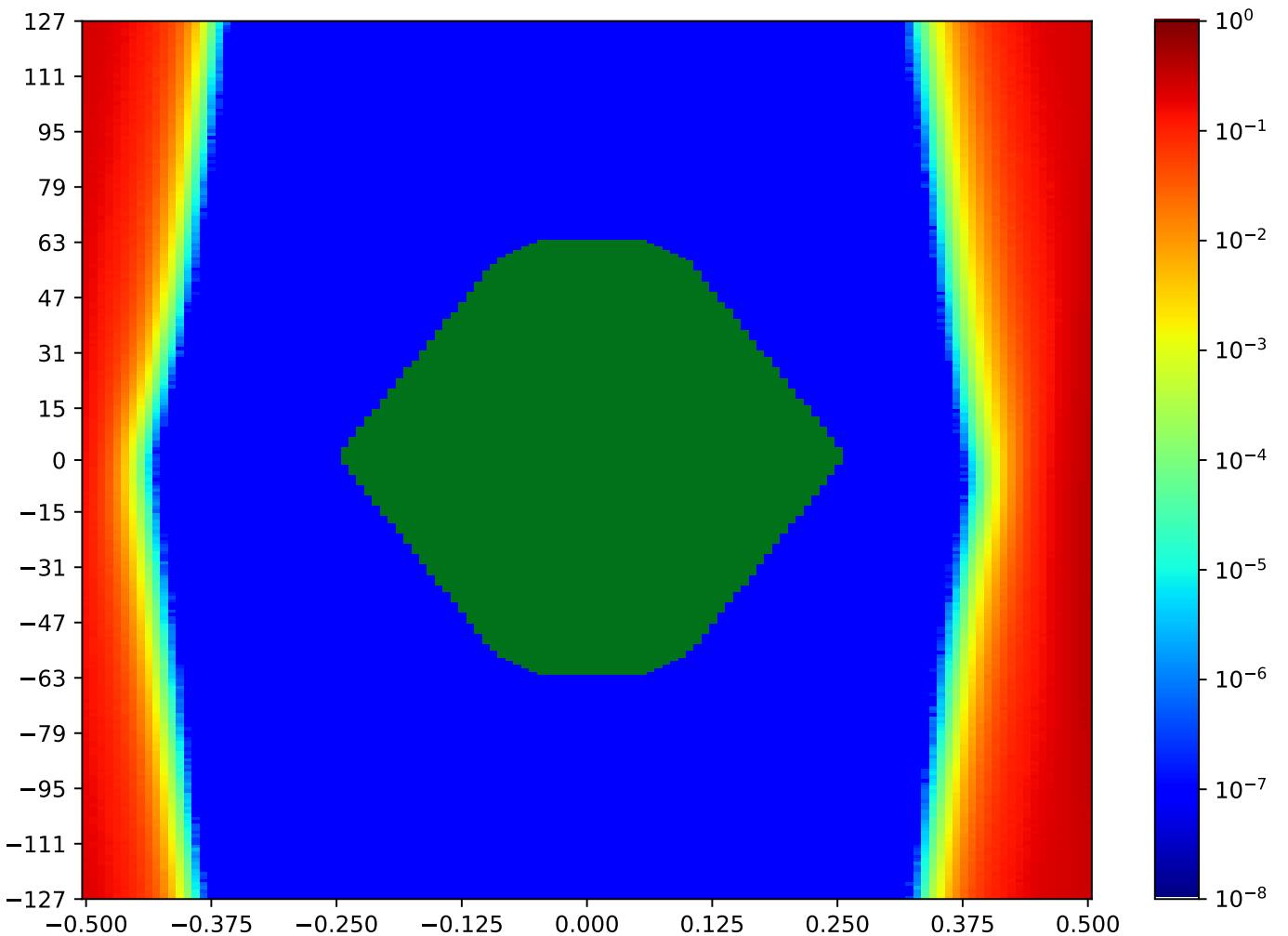


Figure 4.178: MSP_C_FPGA-TX4-11-RX9-11-MSP_A_FPGA

Call back to summary Figure 4.166. Sibling eye diagrams: V2-12.8.

4.14 Partial TRP TX5 MSP_C RX14 Minipod Loopback

A cross-reference to Figure 4.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.
Next summary Figure 4.188.

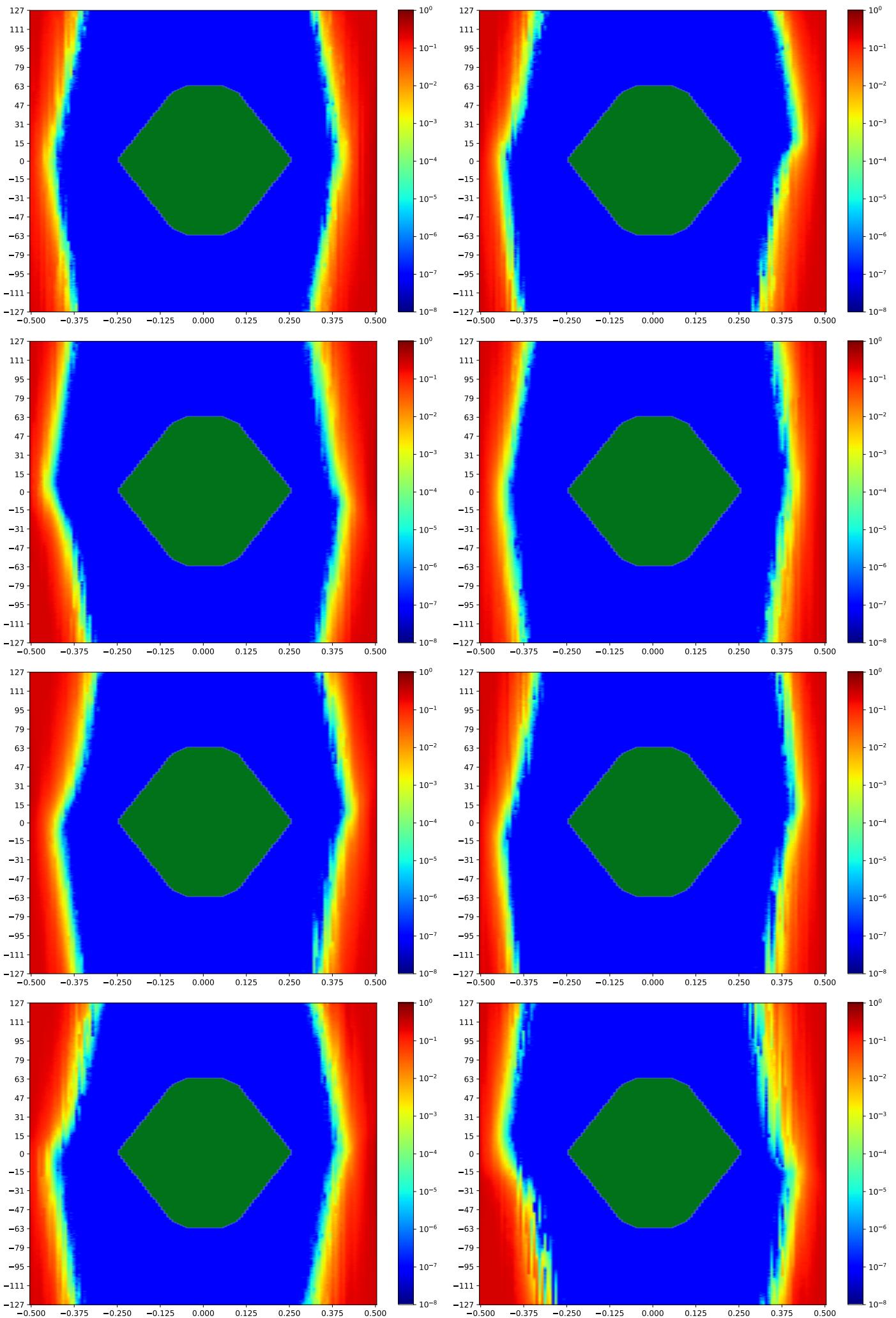


Figure 4.179: Partial TRP TX5 MSP_C RX14 Minipod Loopback

4.14.1 TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

Table 4.166: TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:55:02		2018-Sep-26 19:56:15	
Reset RX	OA	HO		VO	VO (%)
true	23282	100		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

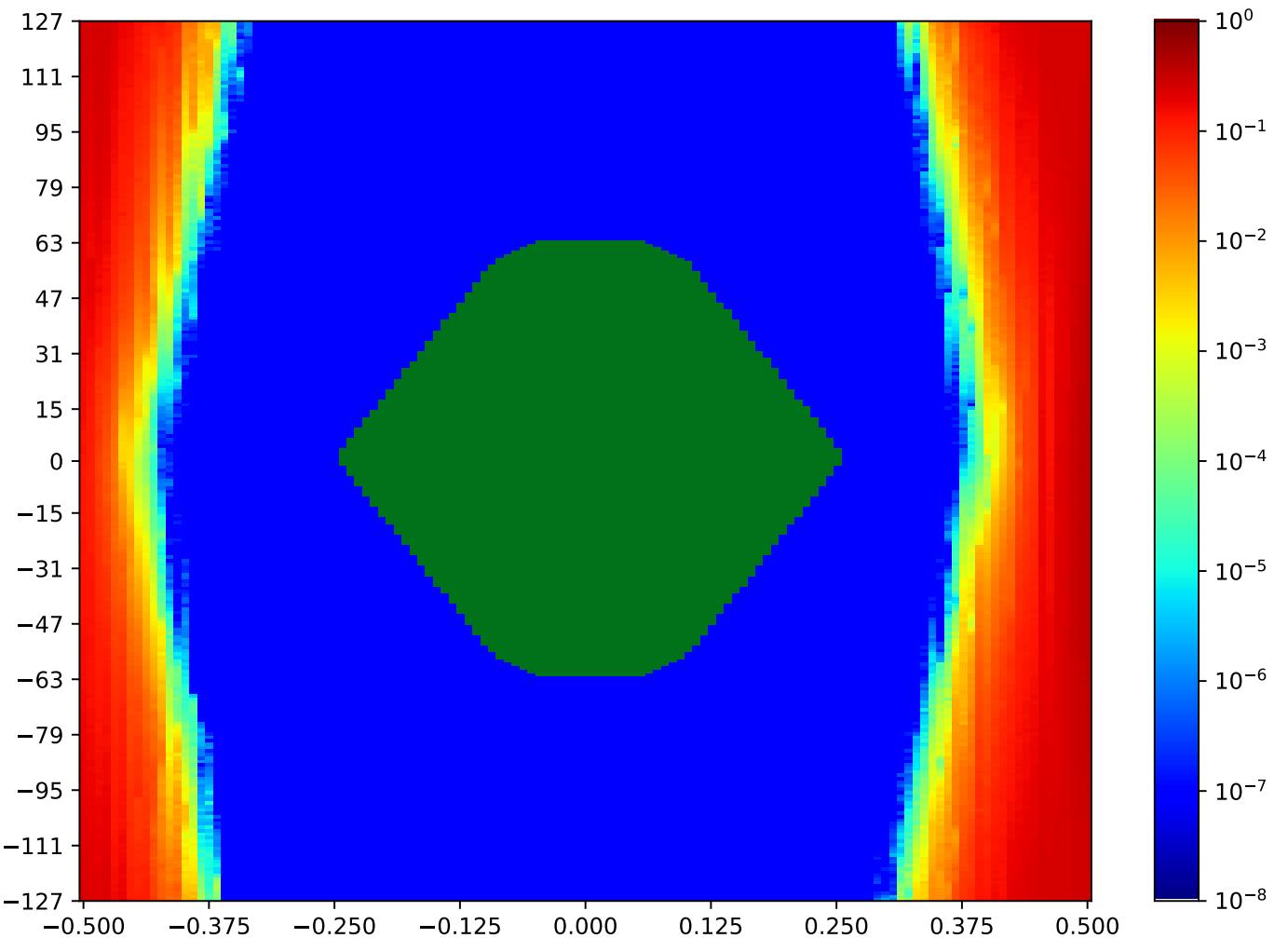


Figure 4.180: TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.14.2 TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

Table 4.167: TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:52:35		2018-Sep-26 19:53:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23337	98	75.97%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

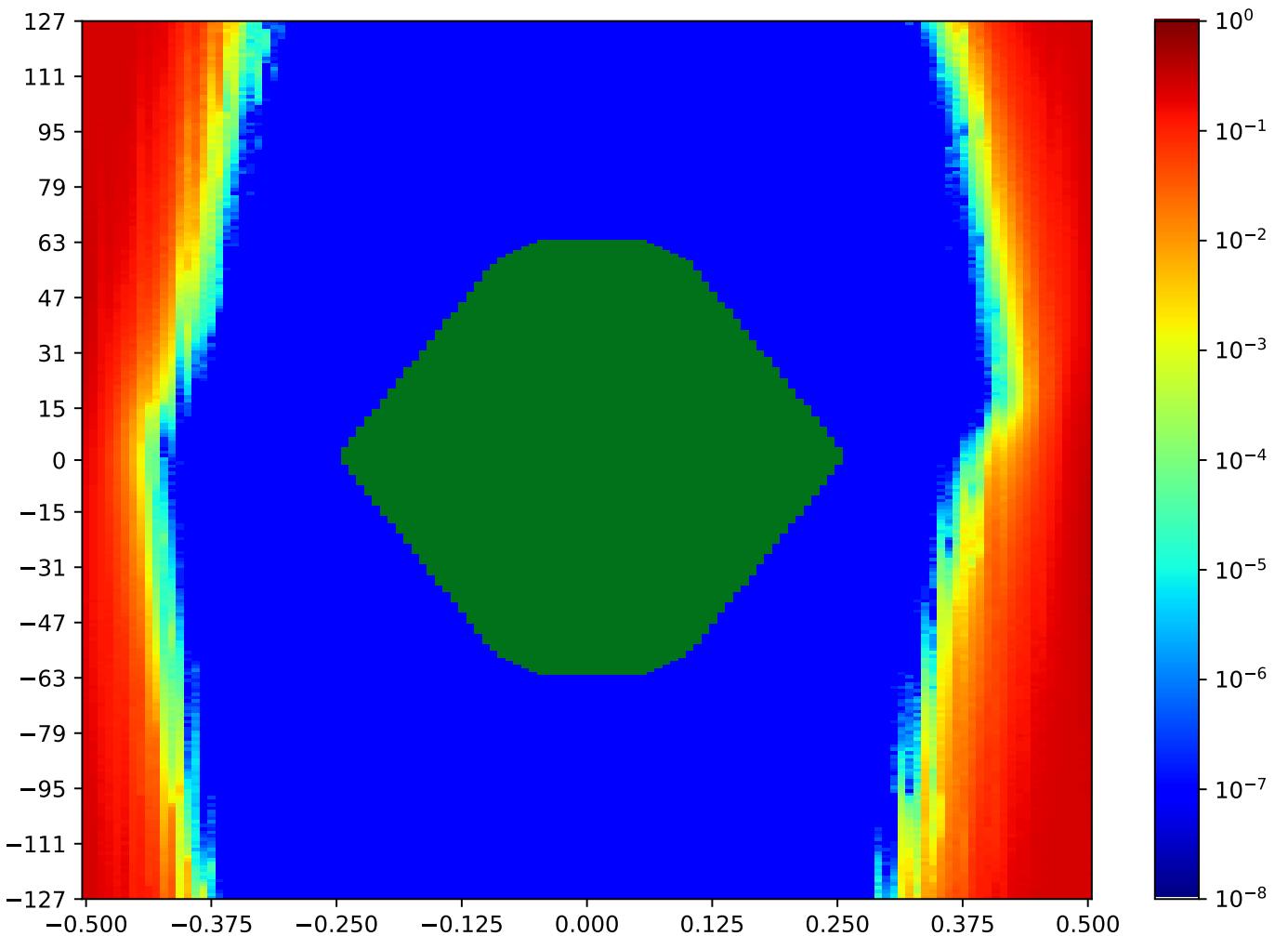


Figure 4.181: TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.14.3 TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

Table 4.168: TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:57:29		2018-Sep-26 19:58:42	
Reset RX	OA	HO		VO	VO (%)
true	23164	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

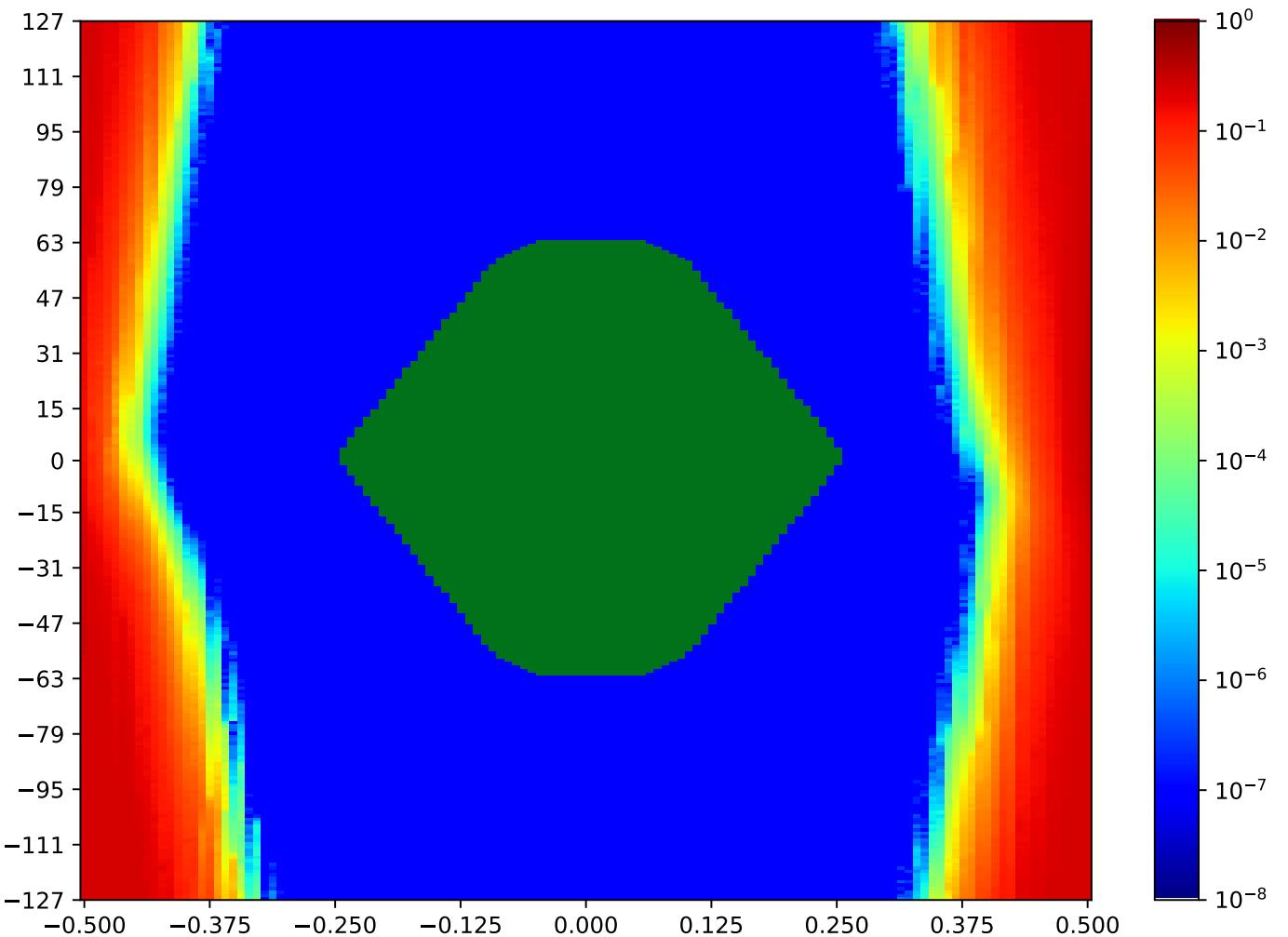


Figure 4.182: TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.14.4 TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

Table 4.169: TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:53:49		2018-Sep-26 19:55:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23523	100	77.52%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

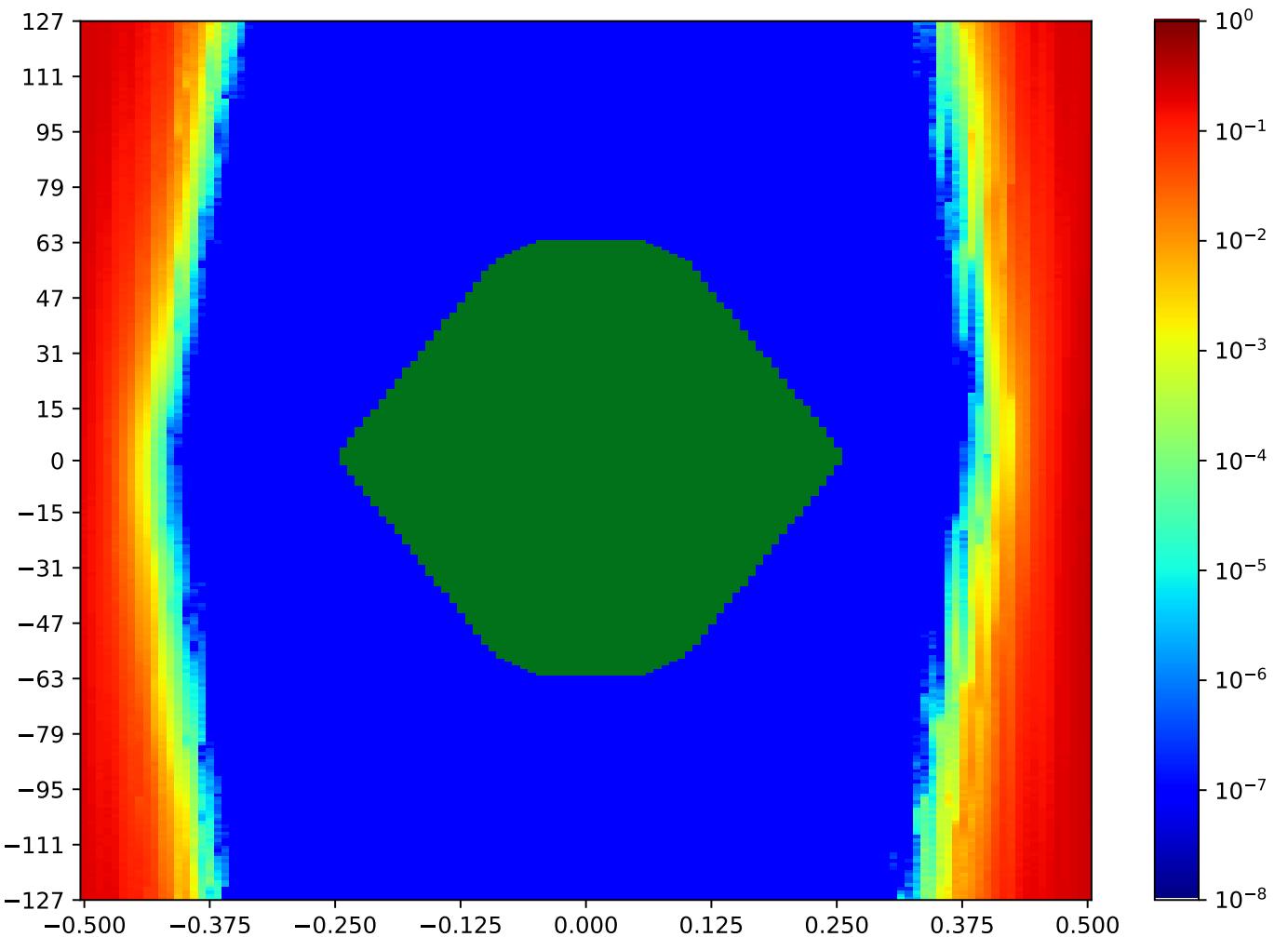


Figure 4.183: TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.14.5 TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

Table 4.170: TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:59:56		2018-Sep-26 20:01:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	22896	98	75.97%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

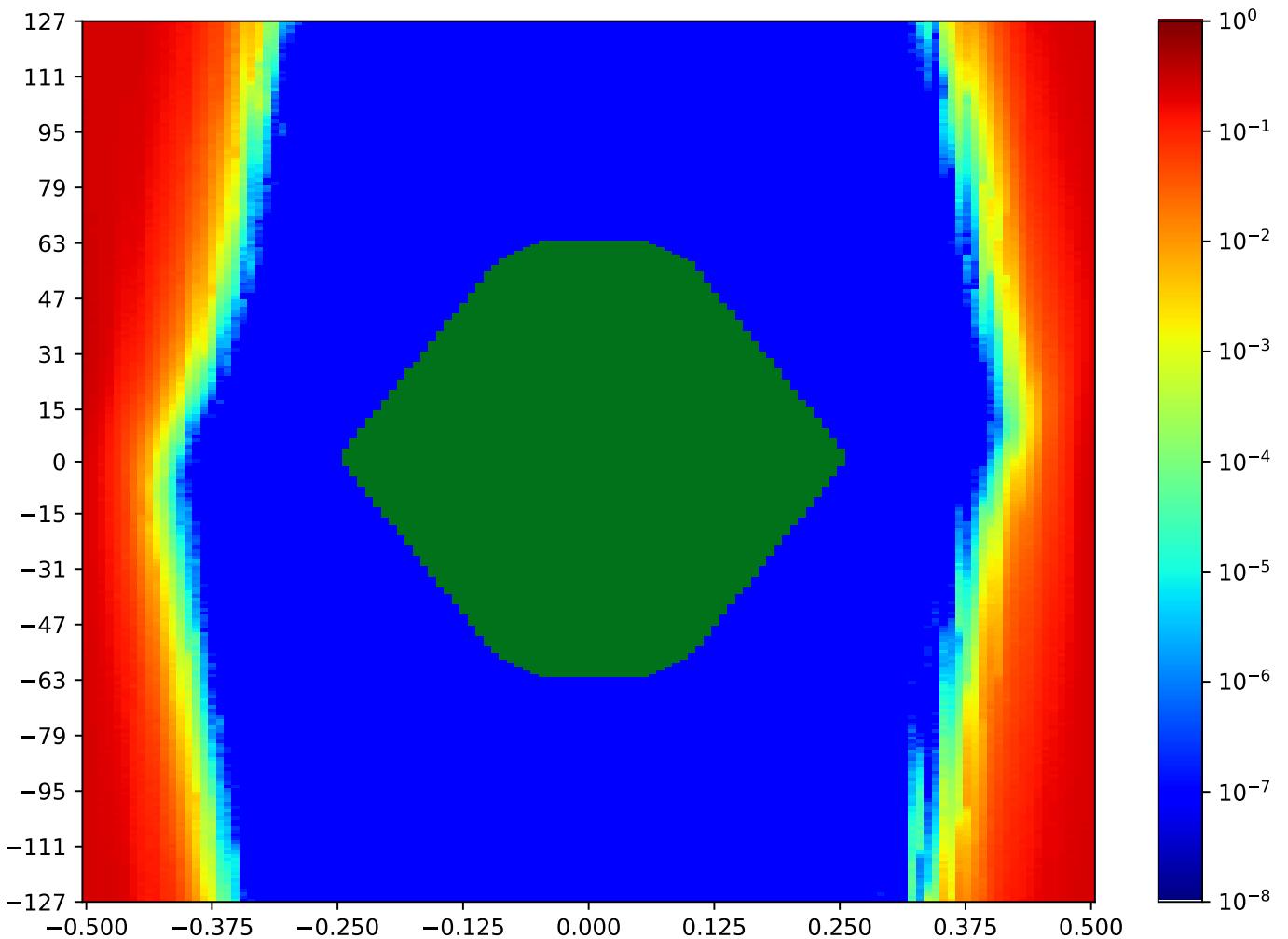


Figure 4.184: TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.14.6 TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

Table 4.171: TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:51:21		2018-Sep-26 19:52:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23857	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

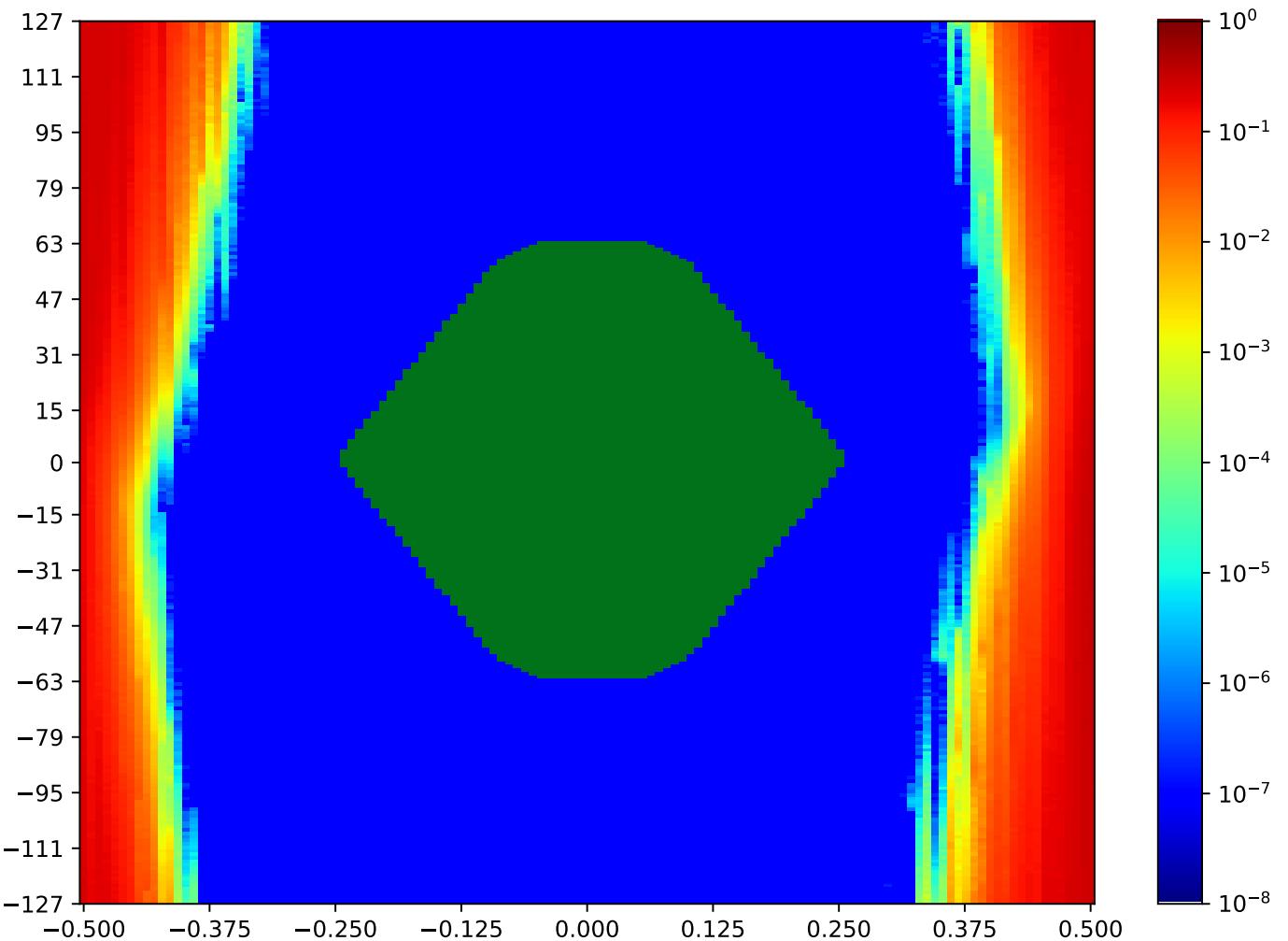


Figure 4.185: TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.14.7 TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

Table 4.172: TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:56:15		2018-Sep-26 19:57:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	22360	99	76.74%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

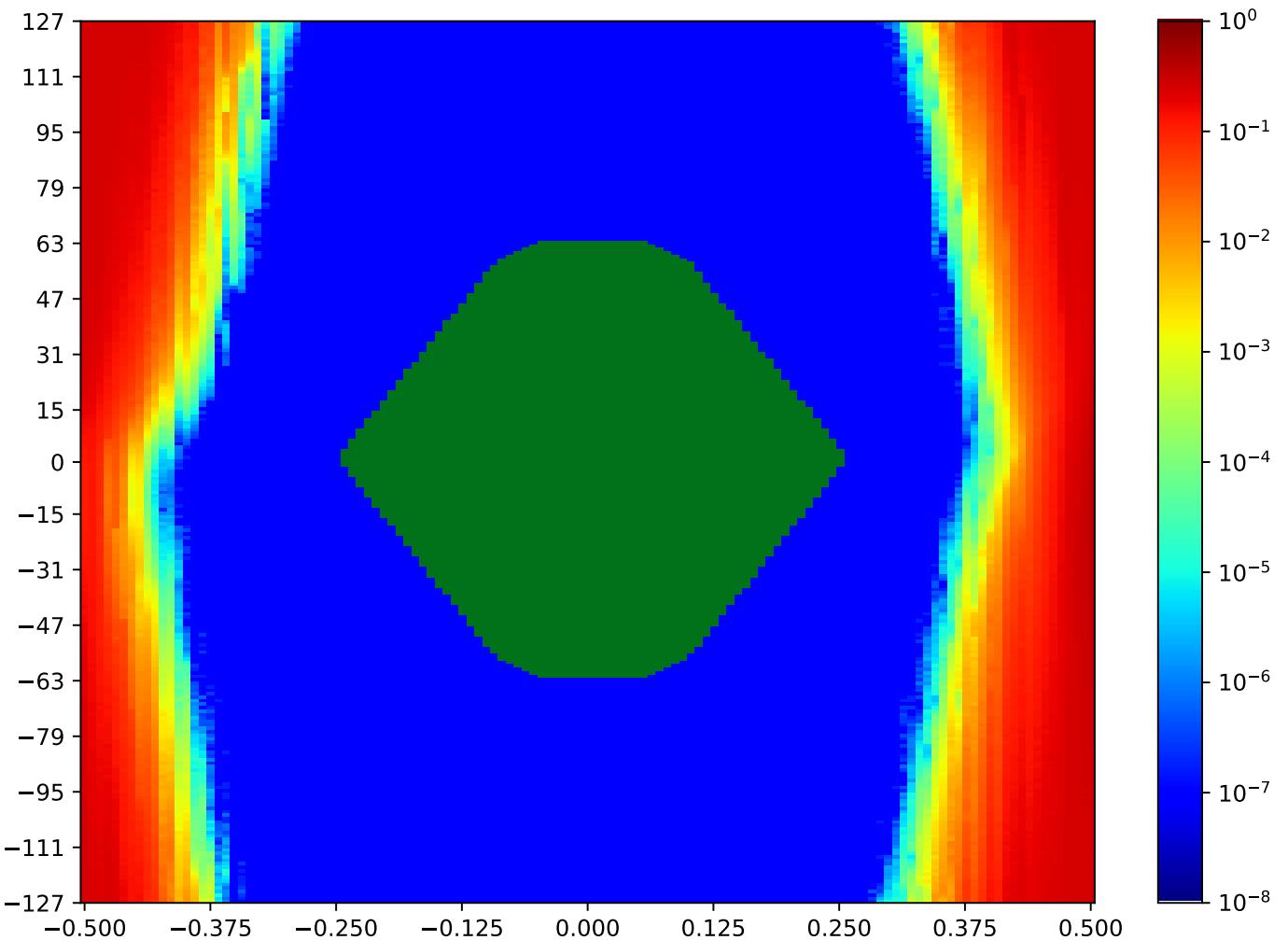


Figure 4.186: TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.14.8 TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

Table 4.173: TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-26 19:58:43		2018-Sep-26 19:59:55	
Reset RX	OA	HO		VO	VO (%)
true	21932	93		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

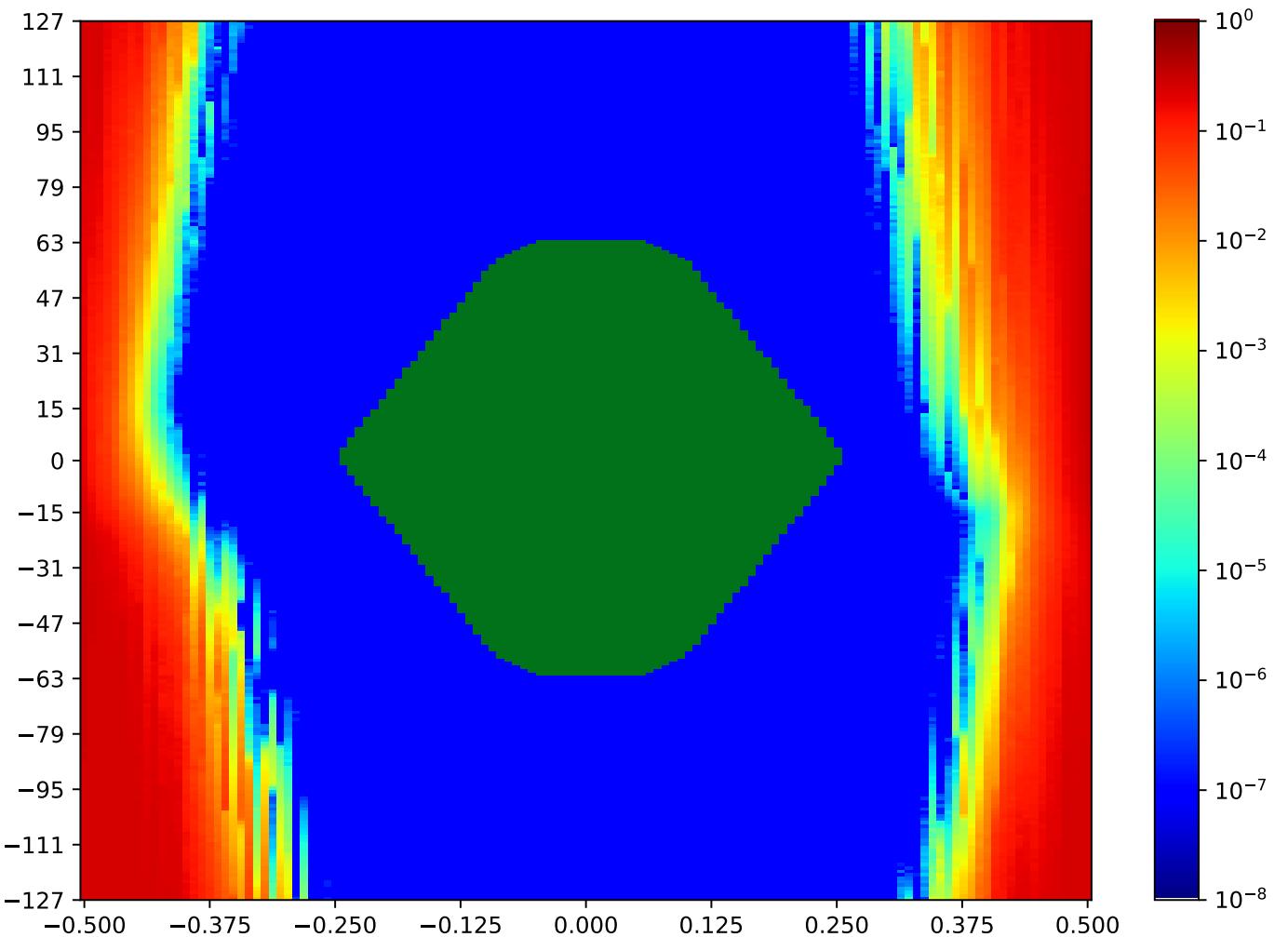


Figure 4.187: TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

Call back to summary Figure 4.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-12.8.

4.15 MSP_A TX1 MSP_C RX10 Minipod Loopback

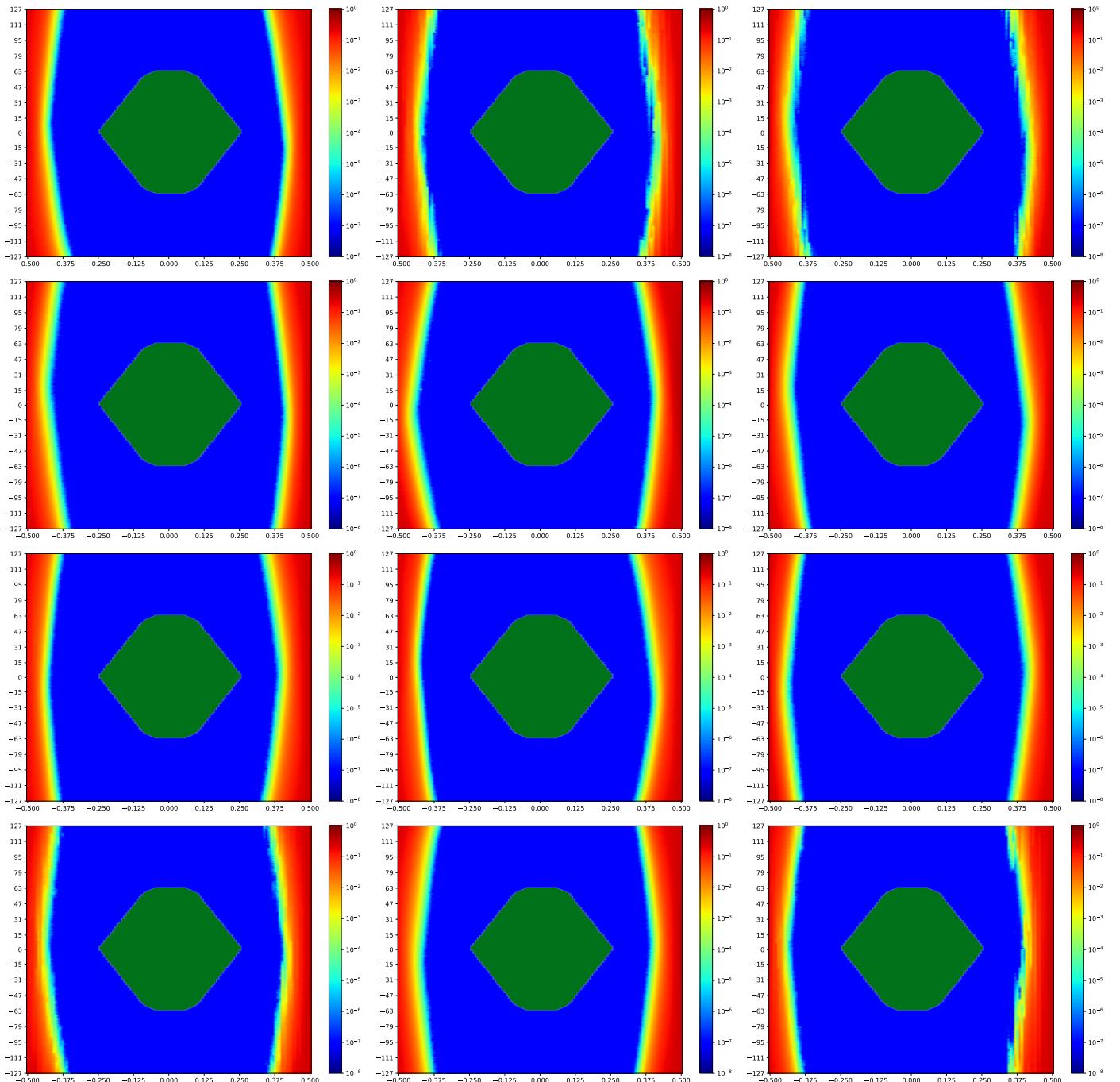


Figure 4.188: MSP_A TX1 MSP_C RX10 Minipod Loopback

A cross-reference to Figure 4.188. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.201.

4.15.1 MSP_A_FPGA-TX1-00-RX10-00-MSP_C_FPGA

Table 4.174: MSP_A_FPGA-TX1-00-RX10-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:53:09		2018-Sep-28 09:54:23	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24571	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

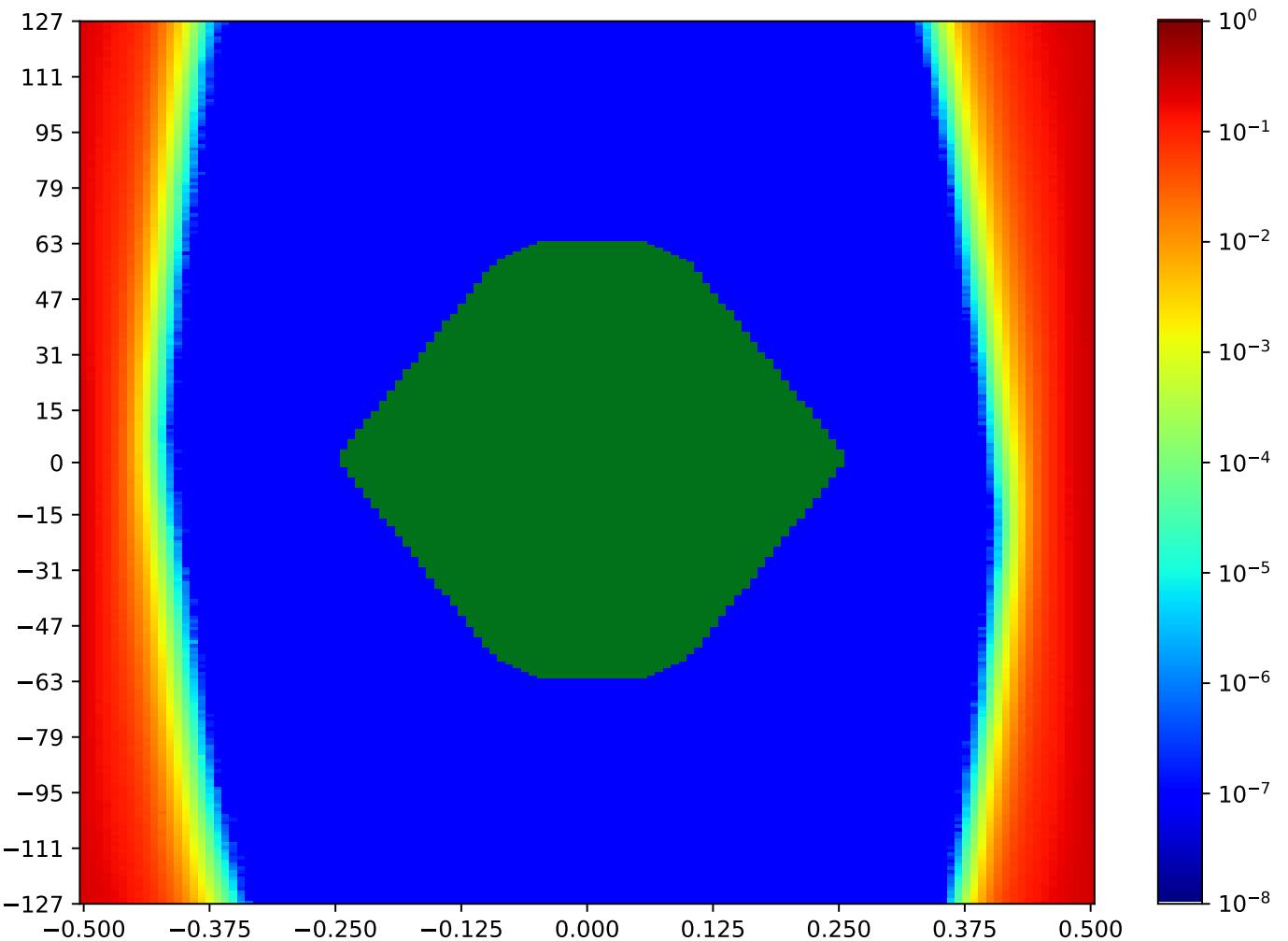


Figure 4.189: MSP_A_FPGA-TX1-00-RX10-00-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.2 MSP_A_FPGA-TX1-01-RX10-01-MSP_C_FPGA

Table 4.175: MSP_A_FPGA-TX1-01-RX10-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:55:38		2018-Sep-28 09:56:53	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24264	103		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

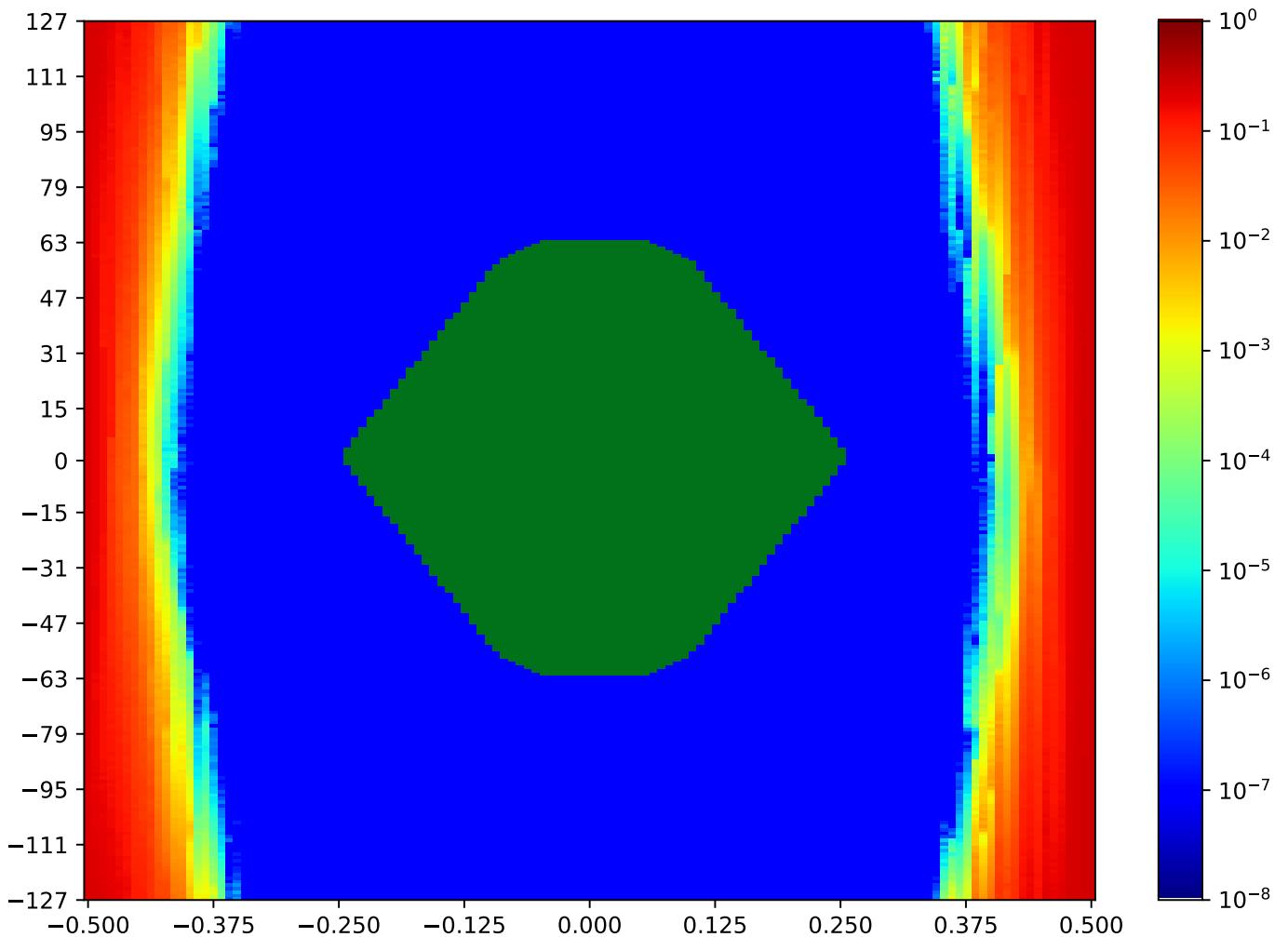


Figure 4.190: MSP_A_FPGA-TX1-01-RX10-01-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.3 MSP_A_FPGA-TX1-02-RX10-02-MSP_C_FPGA

Table 4.176: MSP_A_FPGA-TX1-02-RX10-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:56:53		2018-Sep-28 09:58:08	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24252	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

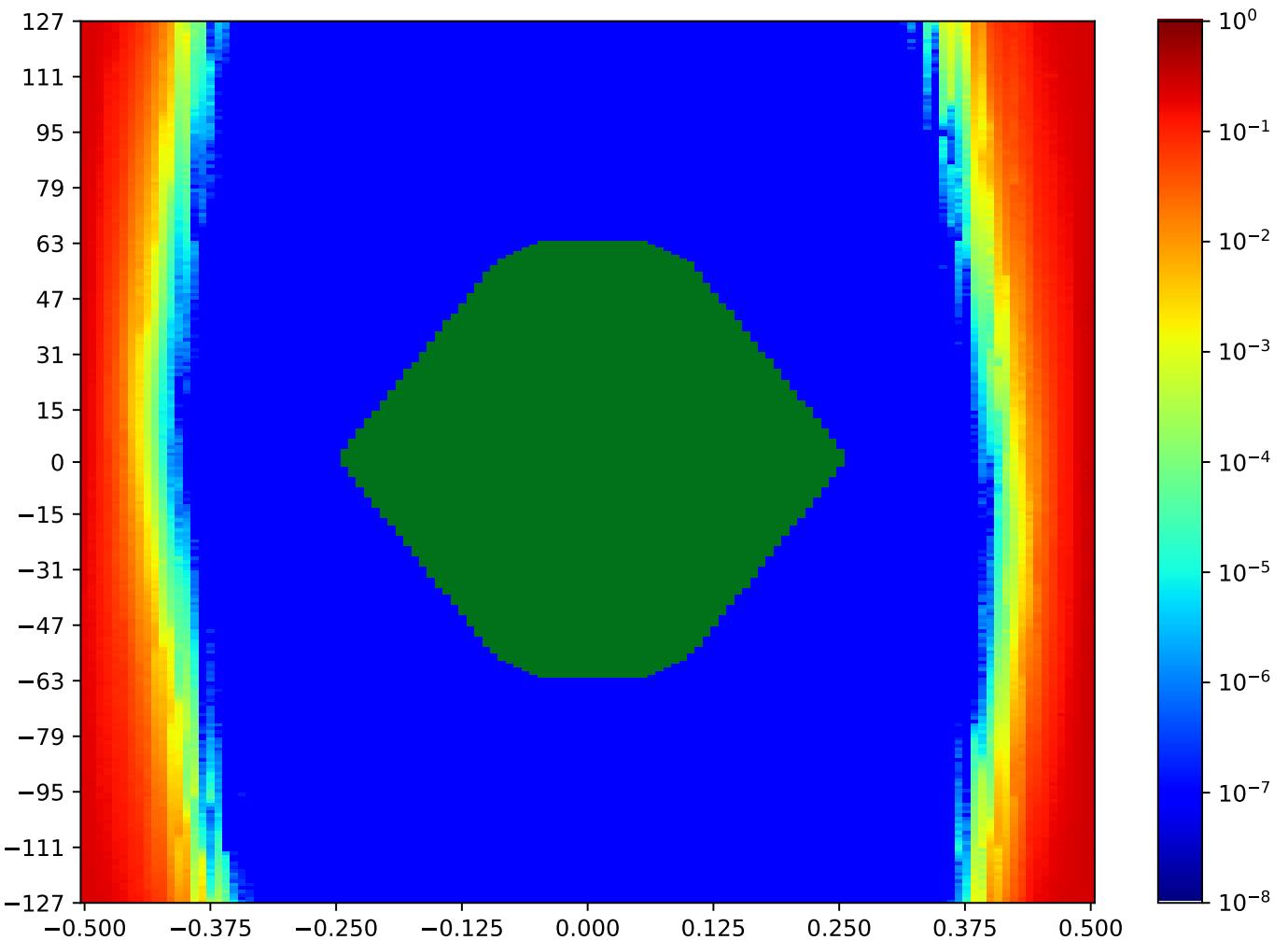


Figure 4.191: MSP_A_FPGA-TX1-02-RX10-02-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.4 MSP_A_FPGA-TX1-03-RX10-03-MSP_C_FPGA

Table 4.177: MSP_A_FPGA-TX1-03-RX10-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:50:41		2018-Sep-28 09:51:55	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24549	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

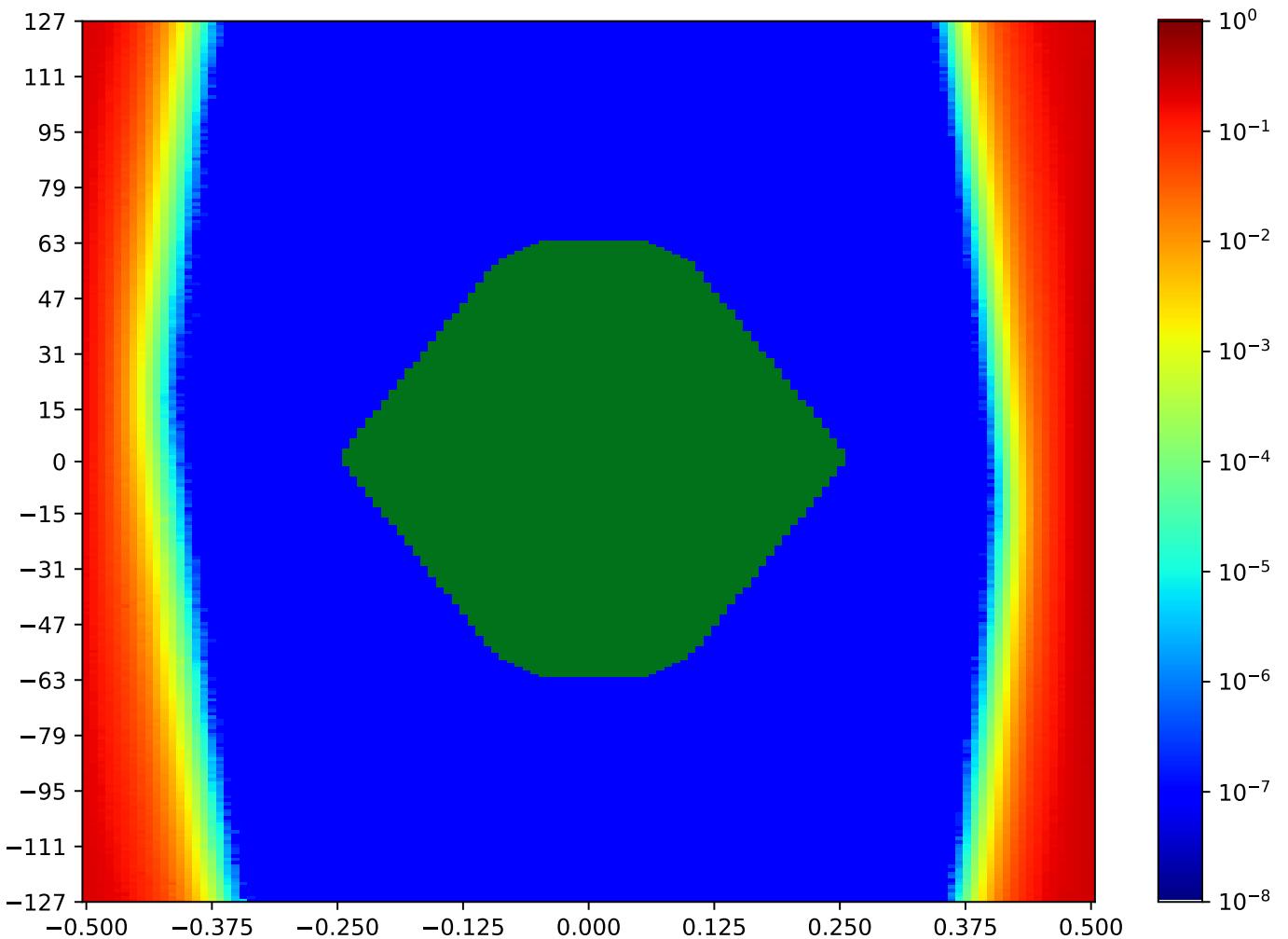


Figure 4.192: MSP_A_FPGA-TX1-03-RX10-03-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.5 MSP_A_FPGA-TX1-04-RX10-04-MSP_C_FPGA

Table 4.178: MSP_A_FPGA-TX1-04-RX10-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:00:37		2018-Sep-28 10:01:52	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24479	104		80.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

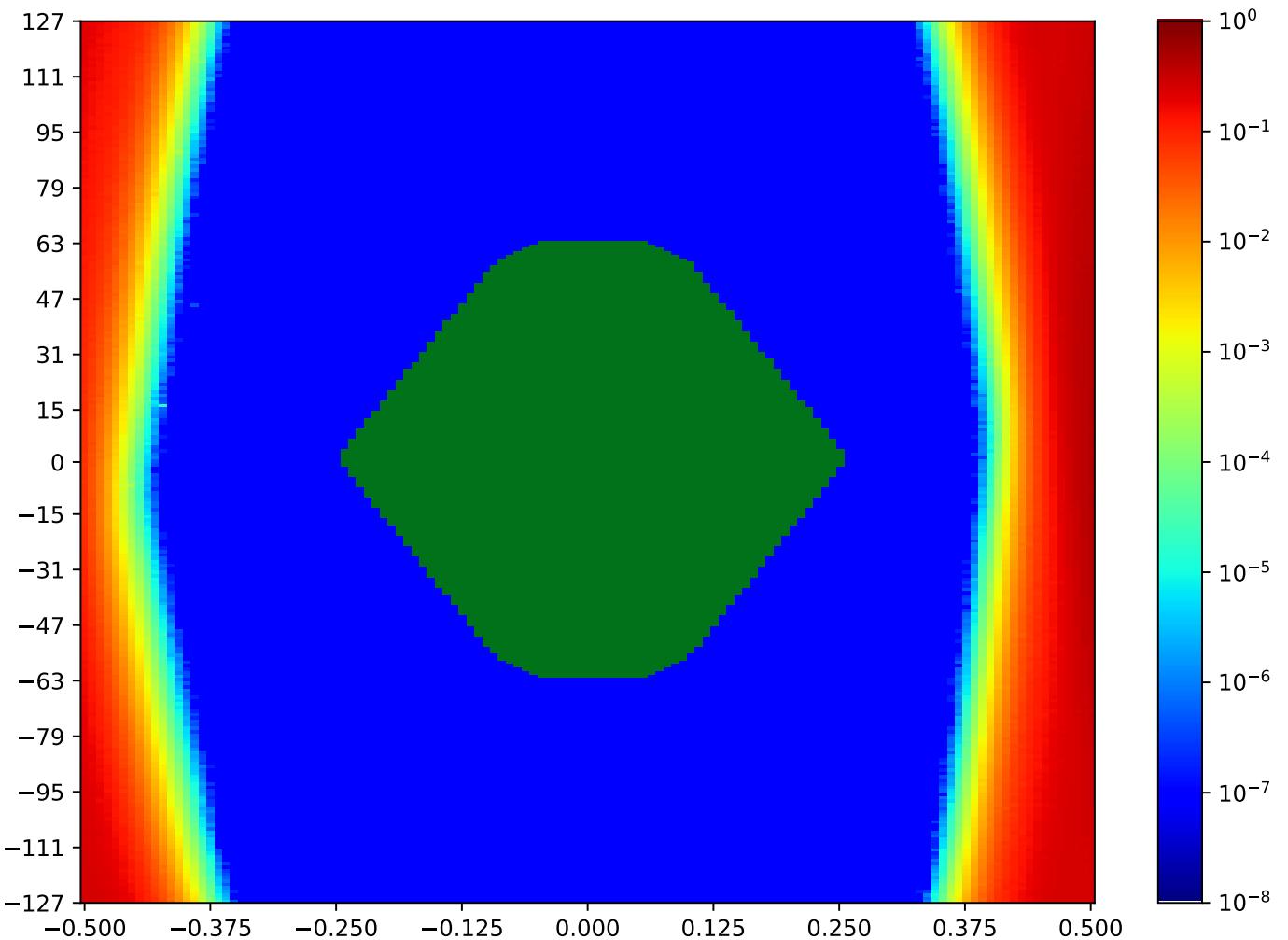


Figure 4.193: MSP_A_FPGA-TX1-04-RX10-04-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.6 MSP_A_FPGA-TX1-05-RX10-05-MSP_C_FPGA

Table 4.179: MSP_A_FPGA-TX1-05-RX10-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:49:26		2018-Sep-28 09:50:40	
Reset RX	OA	HO		VO	VO (%)
true	24131	100		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

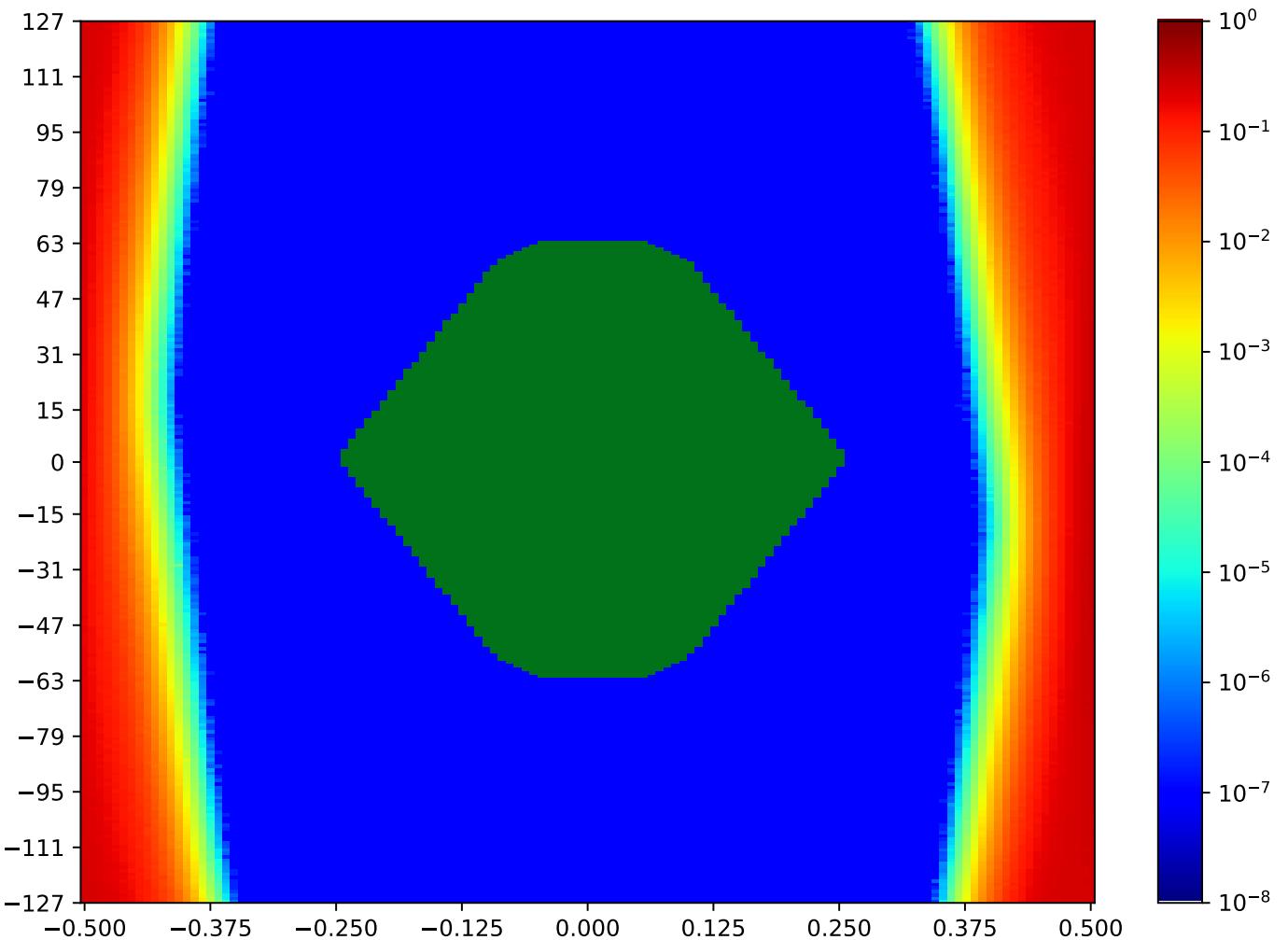


Figure 4.194: MSP_A_FPGA-TX1-05-RX10-05-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.7 MSP_A_FPGA-TX1-06-RX10-06-MSP_C_FPGA

Table 4.180: MSP_A_FPGA-TX1-06-RX10-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:03:07		2018-Sep-28 10:04:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24232	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

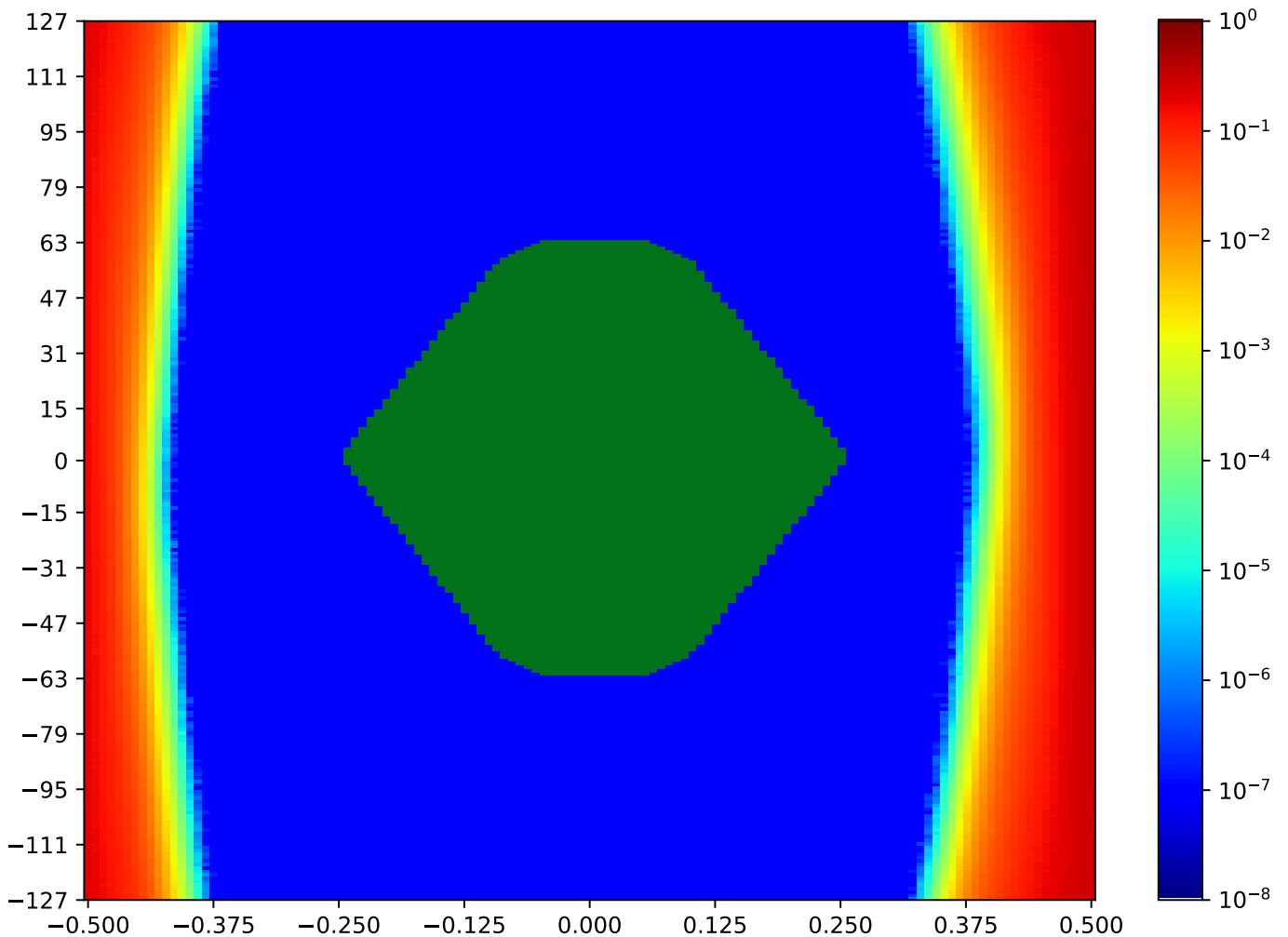


Figure 4.195: MSP_A_FPGA-TX1-06-RX10-06-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.8 MSP_A_FPGA-TX1-07-RX10-07-MSP_C_FPGA

Table 4.181: MSP_A_FPGA-TX1-07-RX10-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:51:55		2018-Sep-28 09:53:09	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24365	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

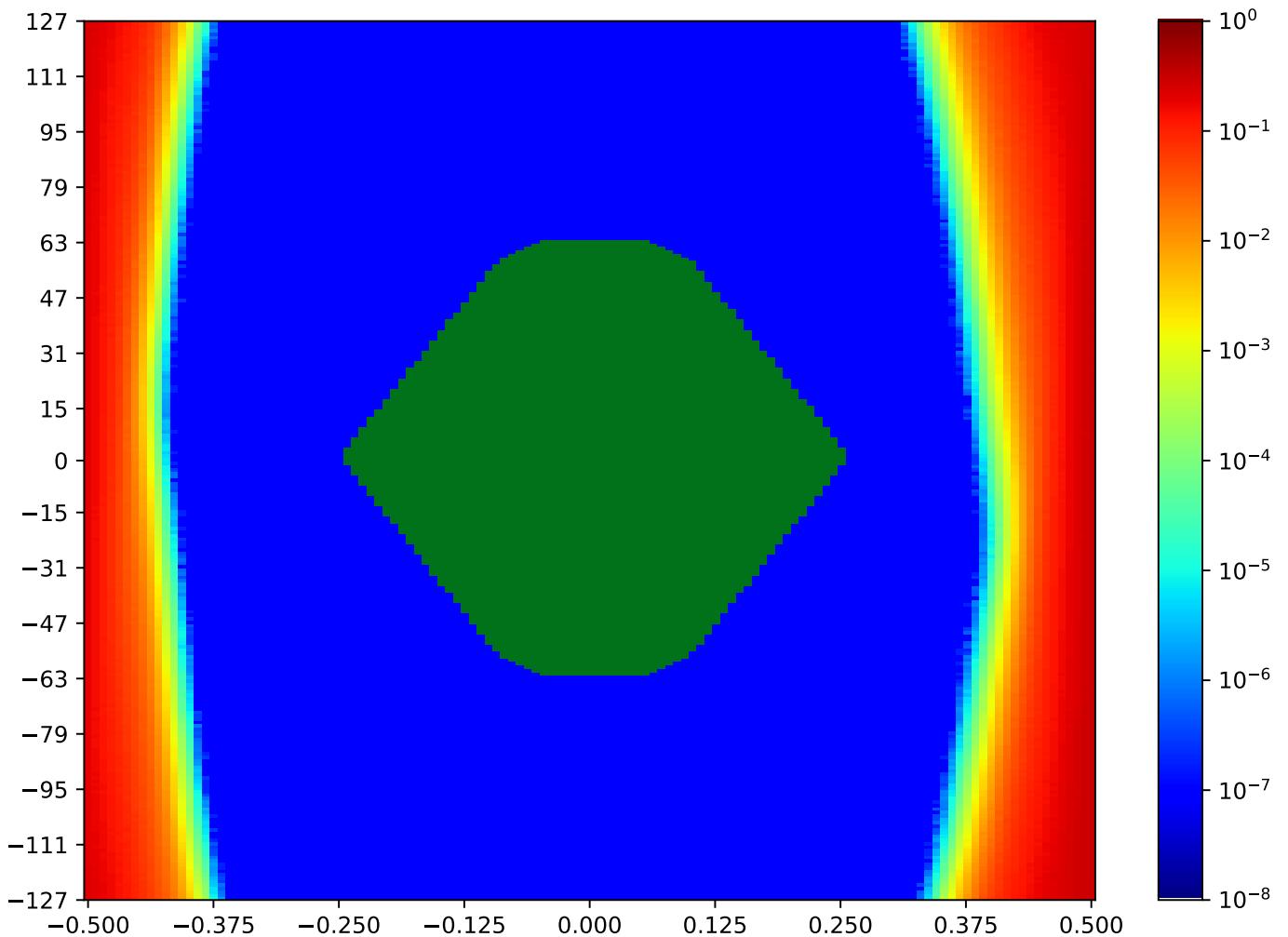


Figure 4.196: MSP_A_FPGA-TX1-07-RX10-07-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.9 MSP_A_FPGA-TX1-08-RX10-08-MSP_C_FPGA

Table 4.182: MSP_A_FPGA-TX1-08-RX10-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:01:52		2018-Sep-28 10:03:07	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24655	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

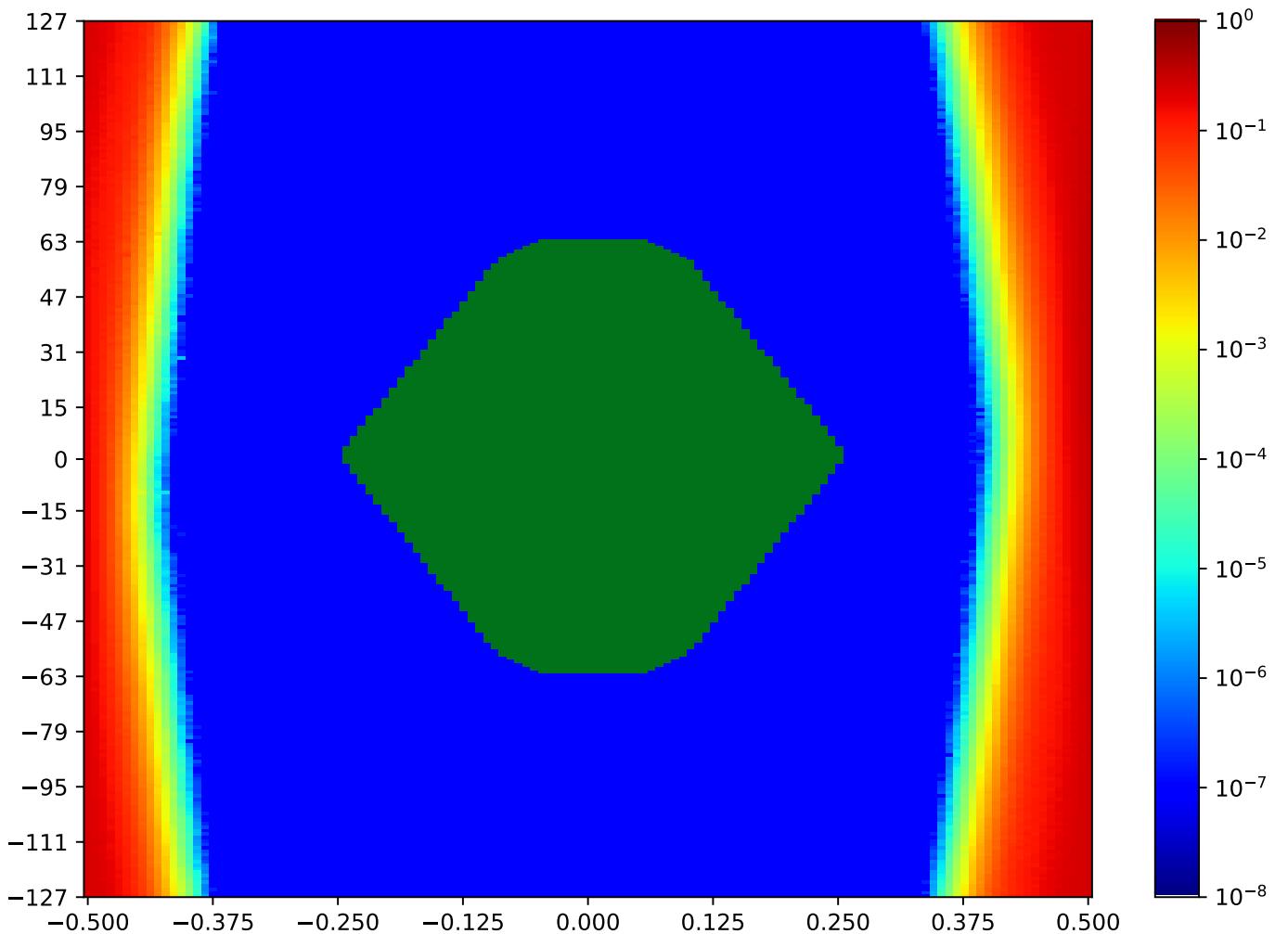


Figure 4.197: MSP_A_FPGA-TX1-08-RX10-08-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.10 MSP_A_FPGA-TX1-09-RX10-09-MSP_C_FPGA

Table 4.183: MSP_A_FPGA-TX1-09-RX10-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:54:23		2018-Sep-28 09:55:38	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24738	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

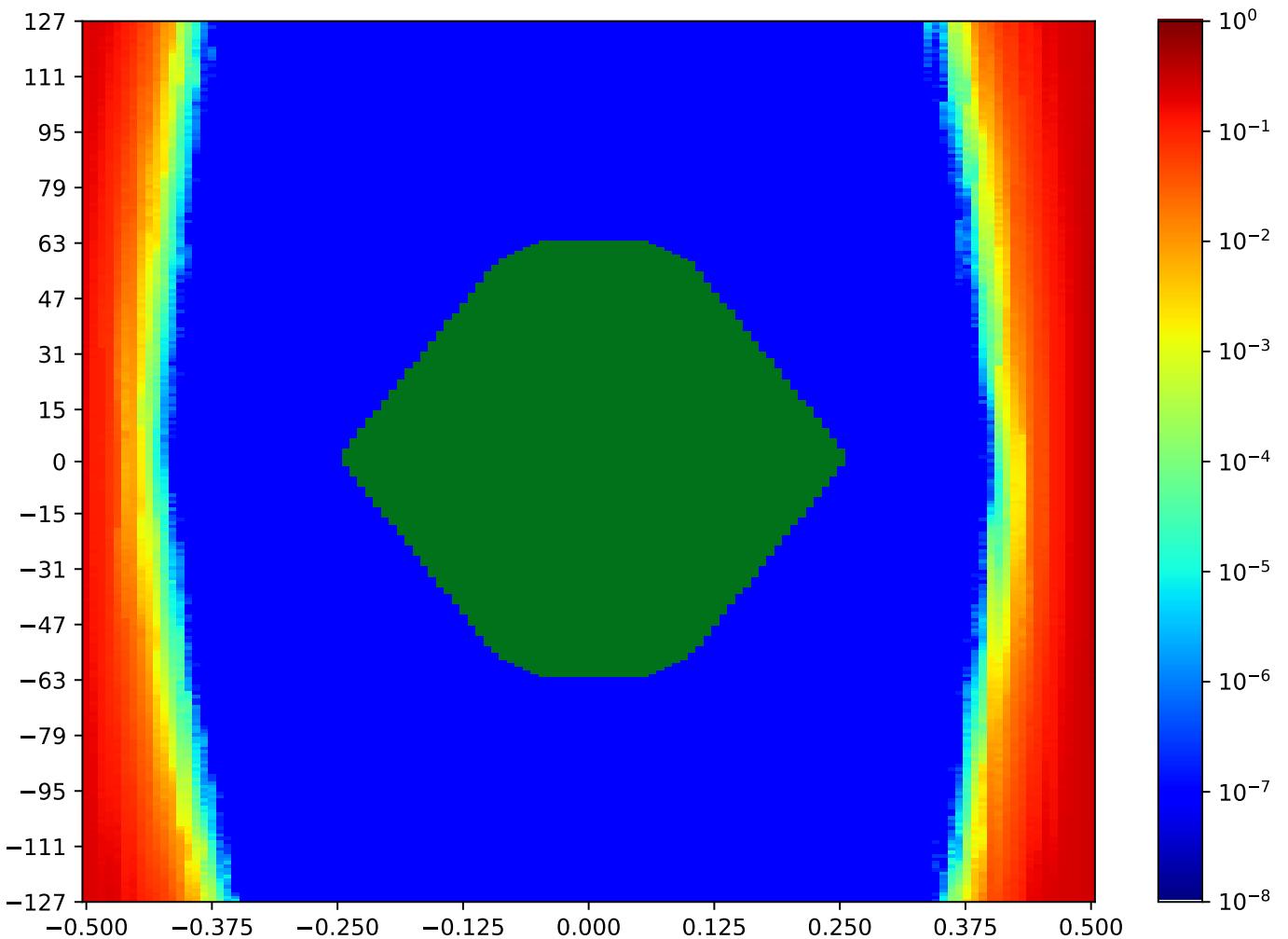


Figure 4.198: MSP_A_FPGA-TX1-09-RX10-09-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.11 MSP_A_FPGA-TX1-10-RX10-10-MSP_C_FPGA

Table 4.184: MSP_A_FPGA-TX1-10-RX10-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:59:23		2018-Sep-28 10:00:37	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24015	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

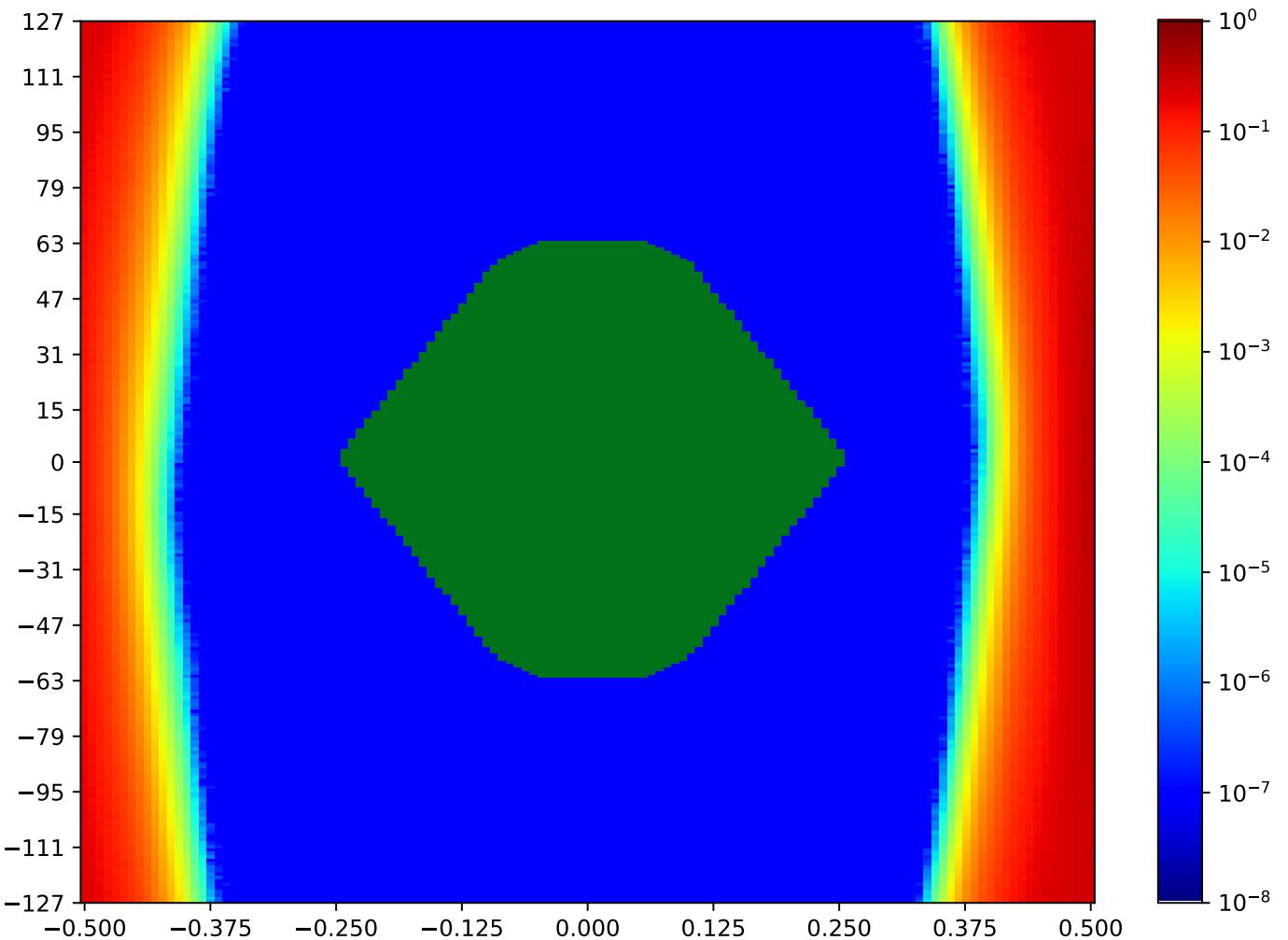


Figure 4.199: MSP_A_FPGA-TX1-10-RX10-10-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.15.12 MSP_A_FPGA-TX1-11-RX10-11-MSP_C_FPGA

Table 4.185: MSP_A_FPGA-TX1-11-RX10-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 09:58:08		2018-Sep-28 09:59:23	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24716	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

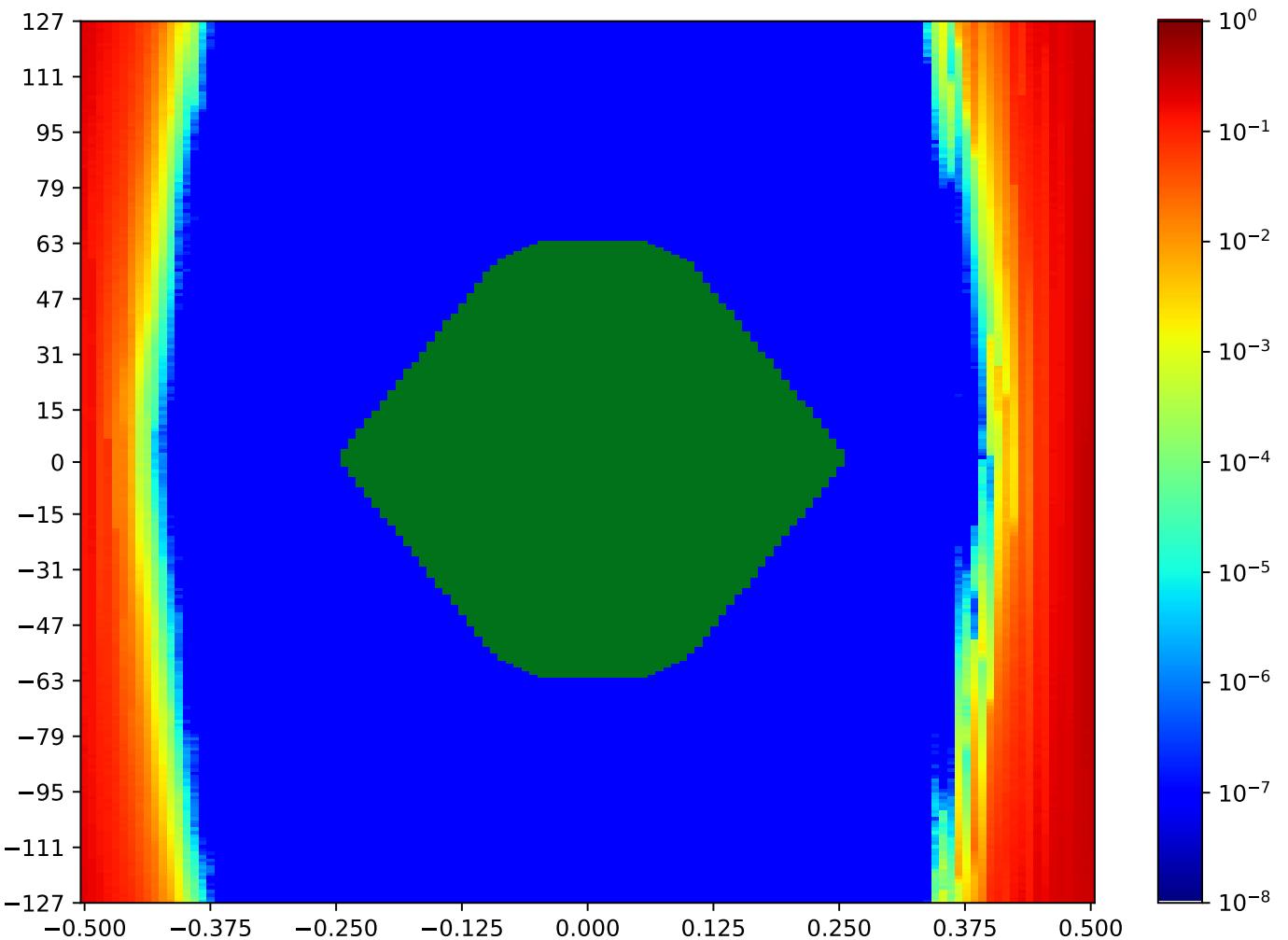


Figure 4.200: MSP_A_FPGA-TX1-11-RX10-11-MSP_C_FPGA

Call back to summary Figure 4.188. Sibling eye diagrams: V2-12.8.

4.16 MSP_A TX2 MSP_C RX11 Minipod Loopback

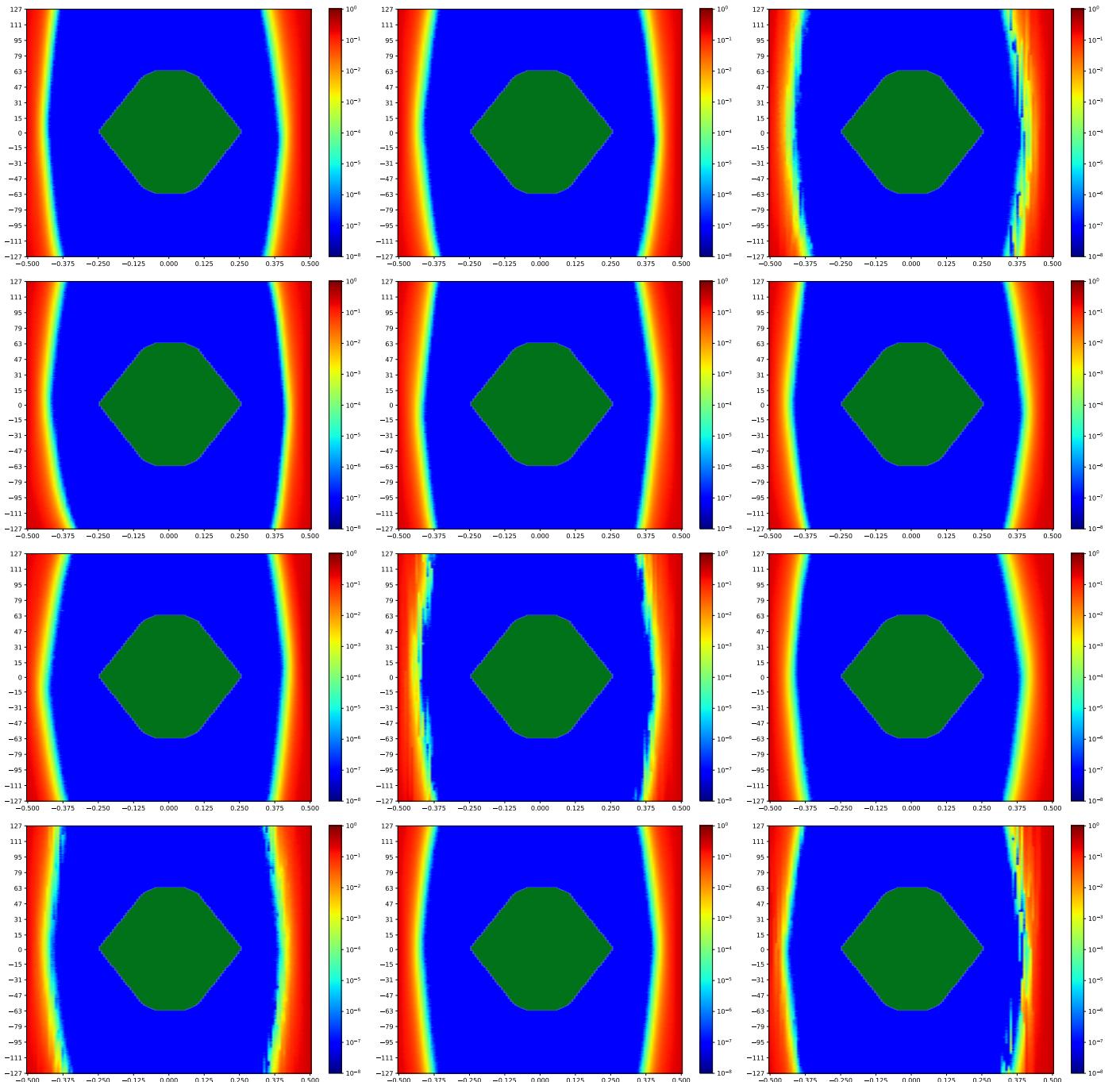


Figure 4.201: MSP_A TX2 MSP_C RX11 Minipod Loopback

A cross-reference to Figure 4.201. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.214.

4.16.1 MSP_A_FPGA-TX2-00-RX11-00-MSP_C_FPGA

Table 4.186: MSP_A_FPGA-TX2-00-RX11-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:08:07		2018-Sep-28 10:09:22	
Reset RX	OA	HO		VO	VO (%)
true	24614	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

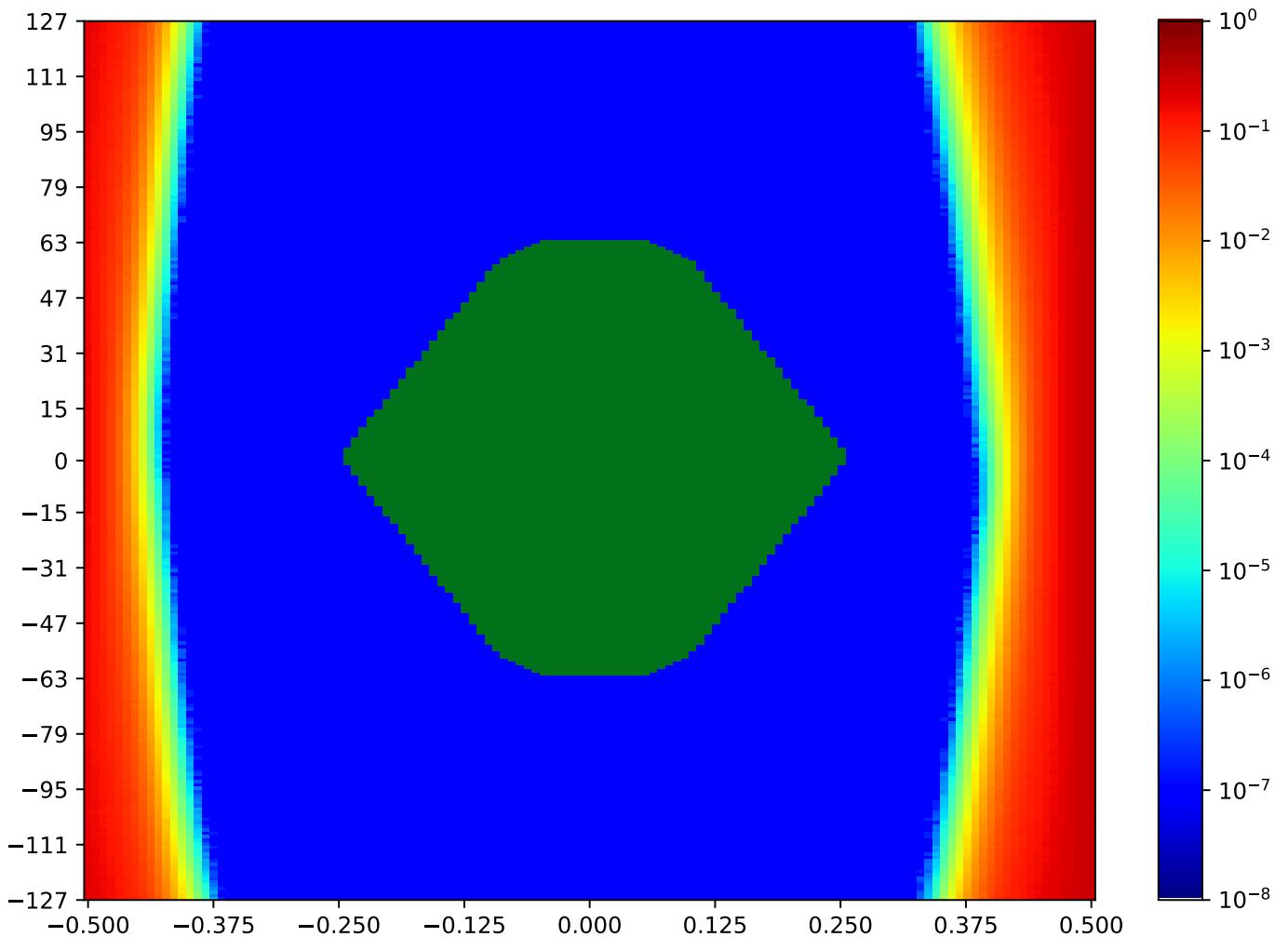


Figure 4.202: MSP_A_FPGA-TX2-00-RX11-00-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.2 MSP_A_FPGA-TX2-01-RX11-01-MSP_C_FPGA

Table 4.187: MSP_A_FPGA-TX2-01-RX11-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:05:37		2018-Sep-28 10:06:52	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24513	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

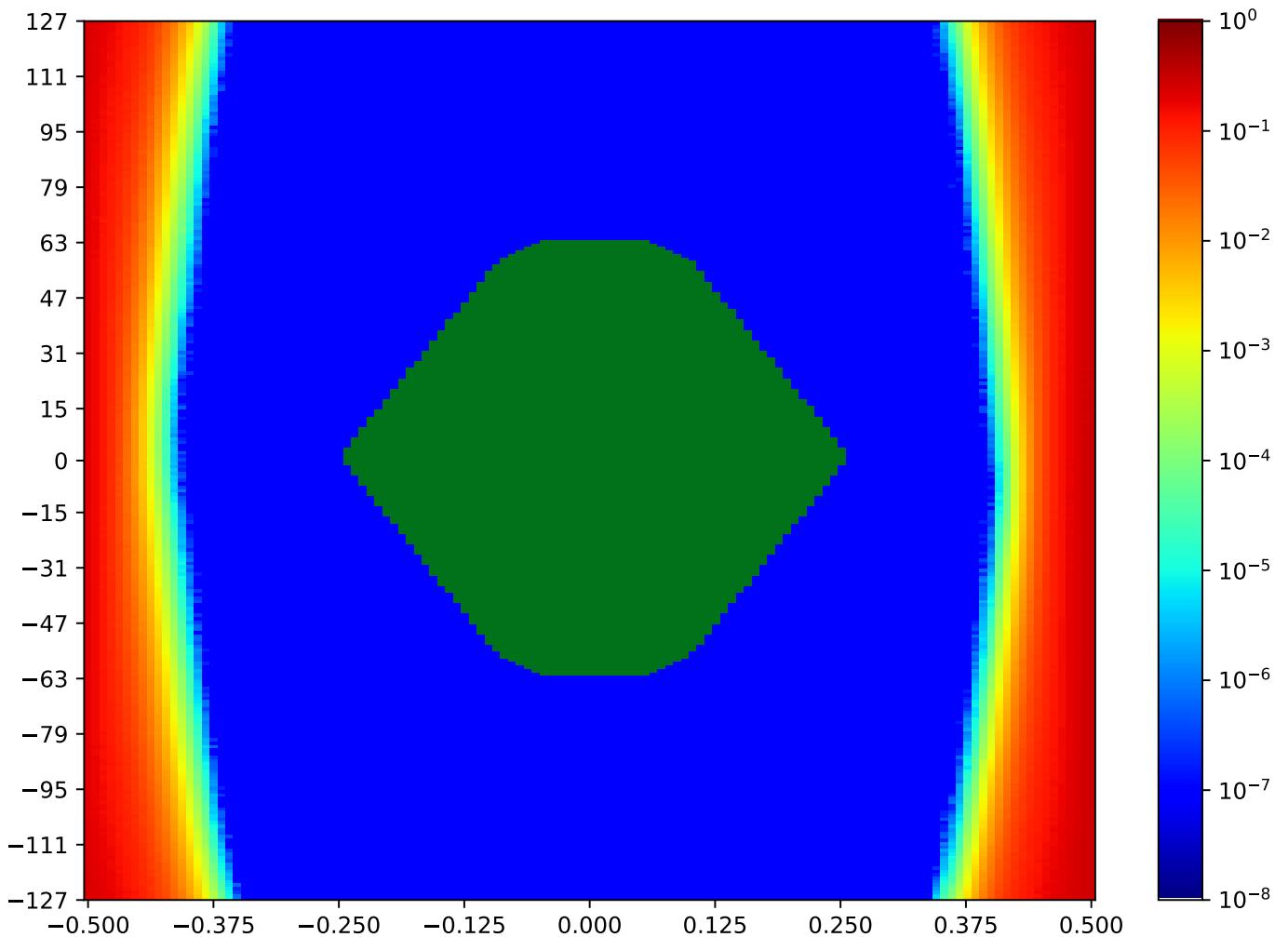


Figure 4.203: MSP_A_FPGA-TX2-01-RX11-01-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.3 MSP_A_FPGA-TX2-02-RX11-02-MSP_C_FPGA

Table 4.188: MSP_A_FPGA-TX2-02-RX11-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:11:53		2018-Sep-28 10:13:09	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23833	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

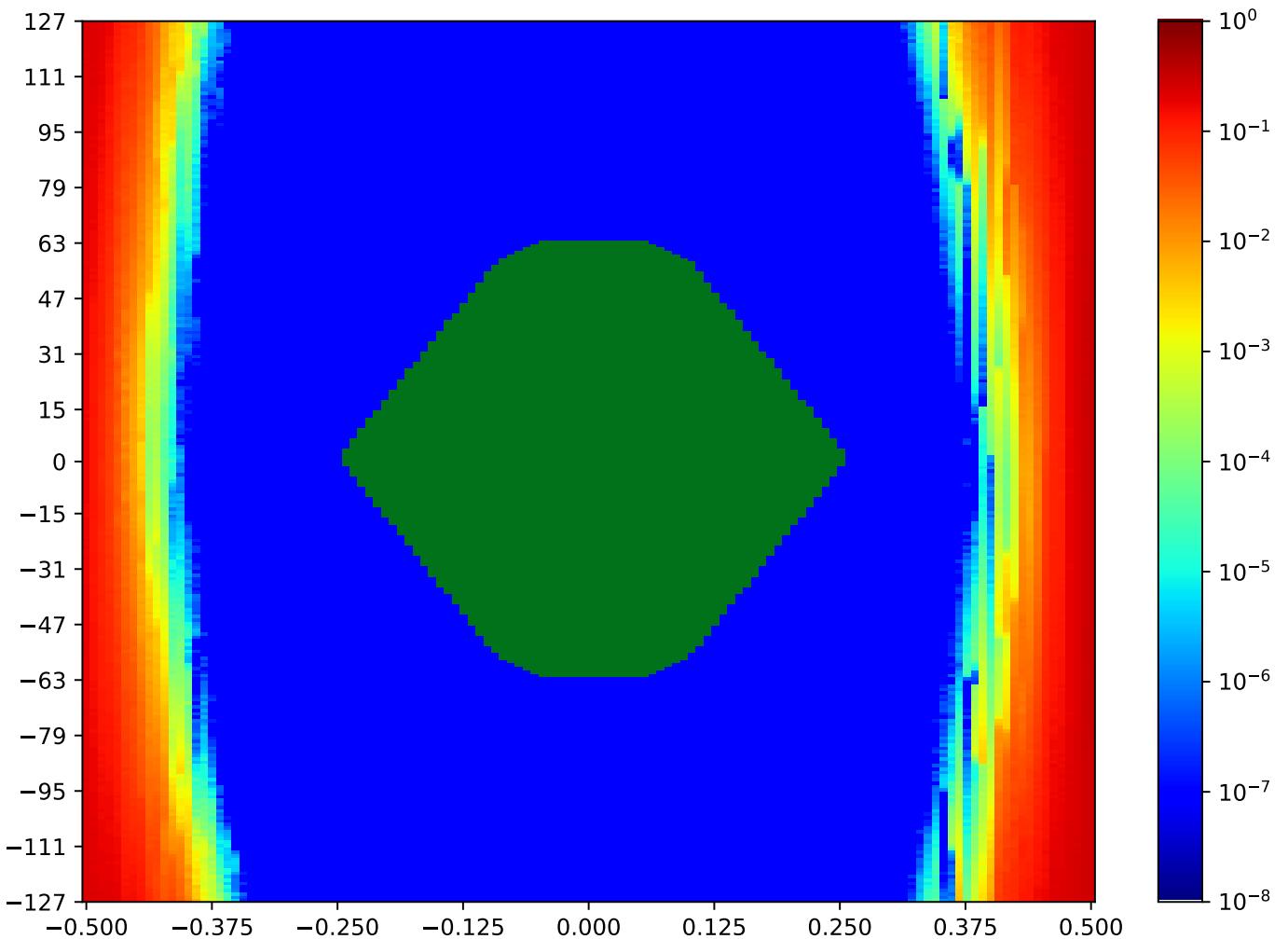


Figure 4.204: MSP_A_FPGA-TX2-02-RX11-02-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.4 MSP_A_FPGA-TX2-03-RX11-03-MSP_C_FPGA

Table 4.189: MSP_A_FPGA-TX2-03-RX11-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:04:22		2018-Sep-28 10:05:37	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24778	104		80.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

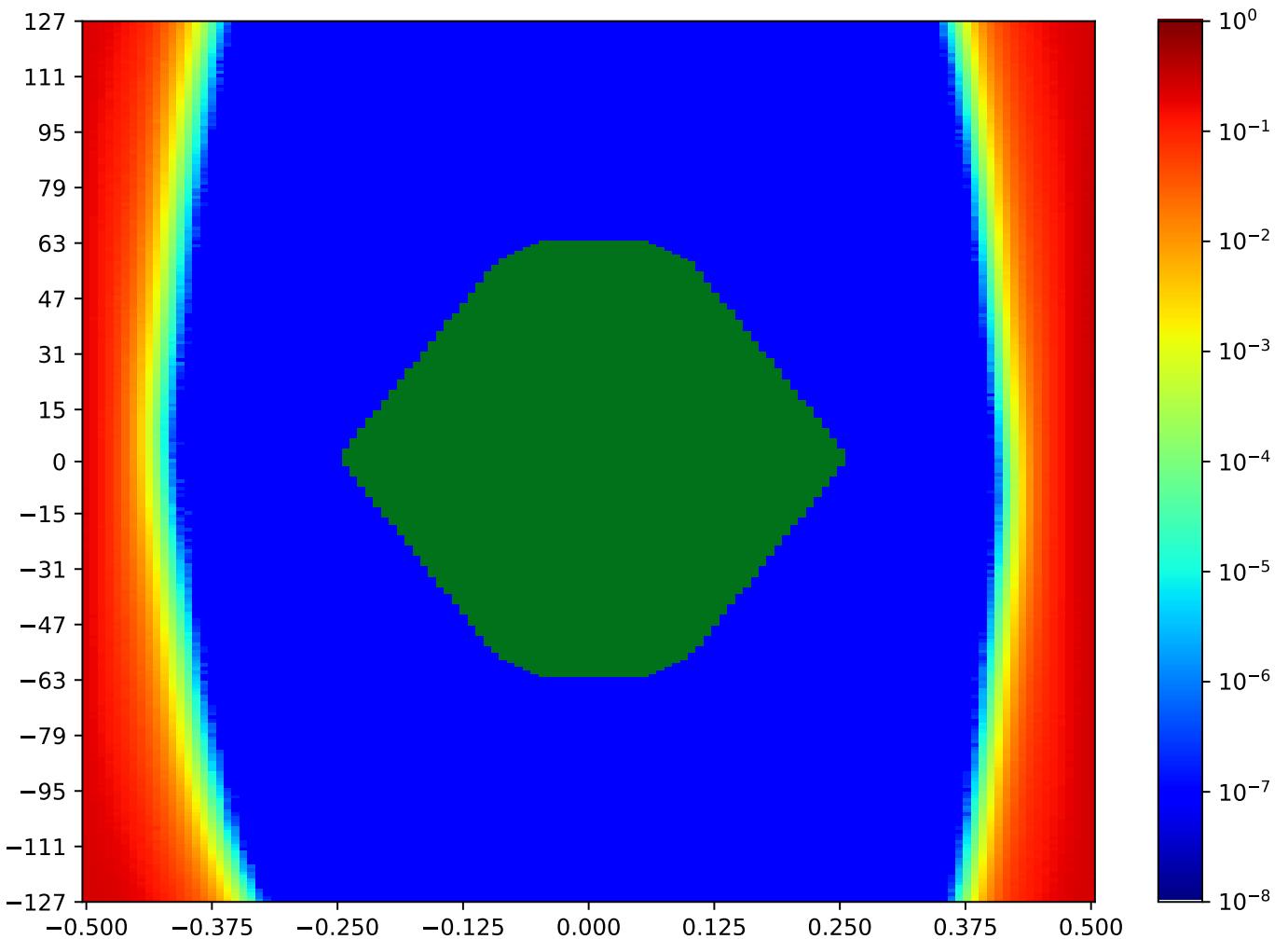


Figure 4.205: MSP_A_FPGA-TX2-03-RX11-03-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.5 MSP_A_FPGA-TX2-04-RX11-04-MSP_C_FPGA

Table 4.190: MSP_A_FPGA-TX2-04-RX11-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:15:40		2018-Sep-28 10:16:55	
Reset RX	OA	HO		VO	VO (%)
true	24188	100		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

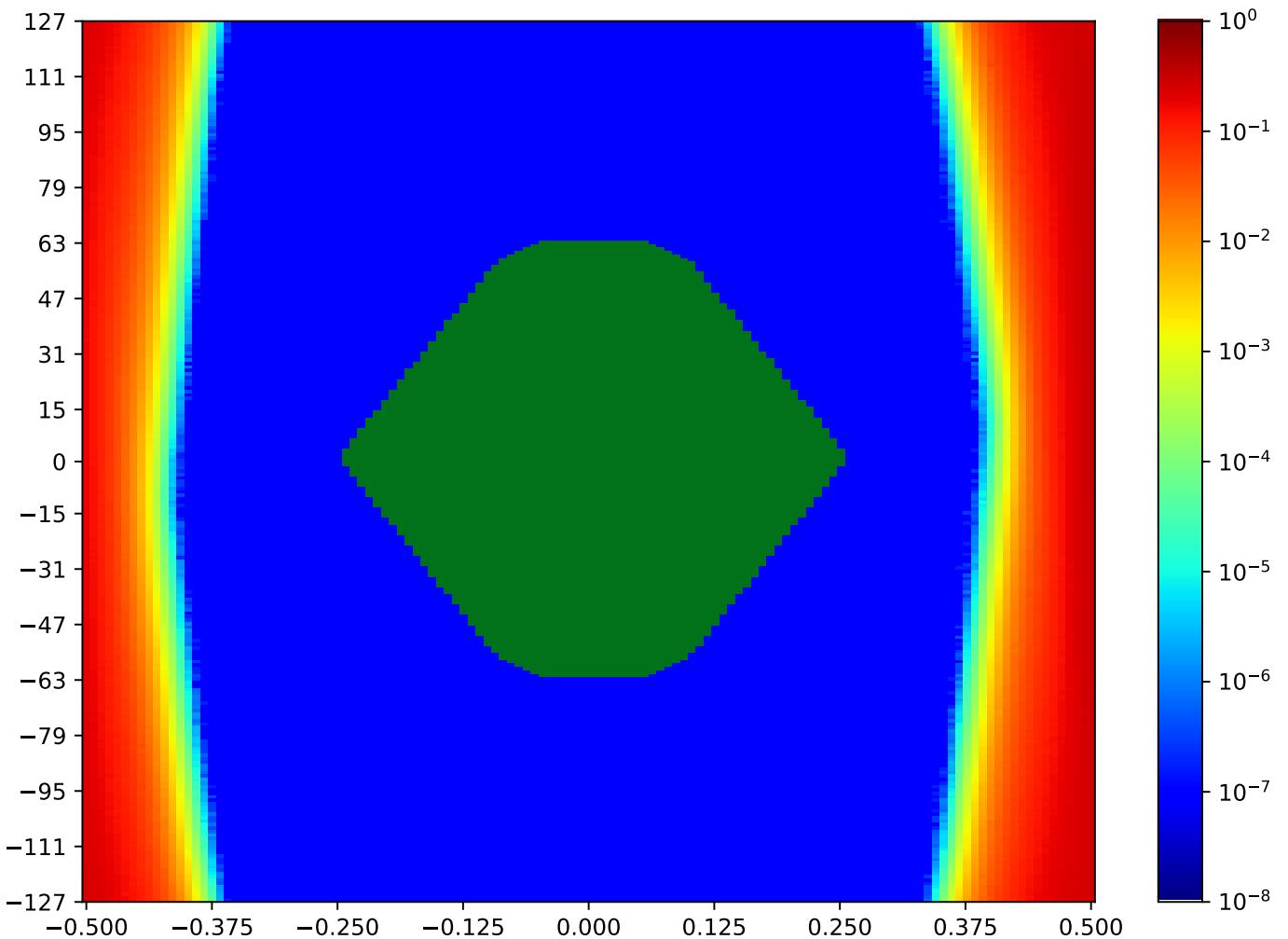


Figure 4.206: MSP_A_FPGA-TX2-04-RX11-04-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.6 MSP_A_FPGA-TX2-05-RX11-05-MSP_C_FPGA

Table 4.191: MSP_A_FPGA-TX2-05-RX11-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:06:52		2018-Sep-28 10:08:07	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24180	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

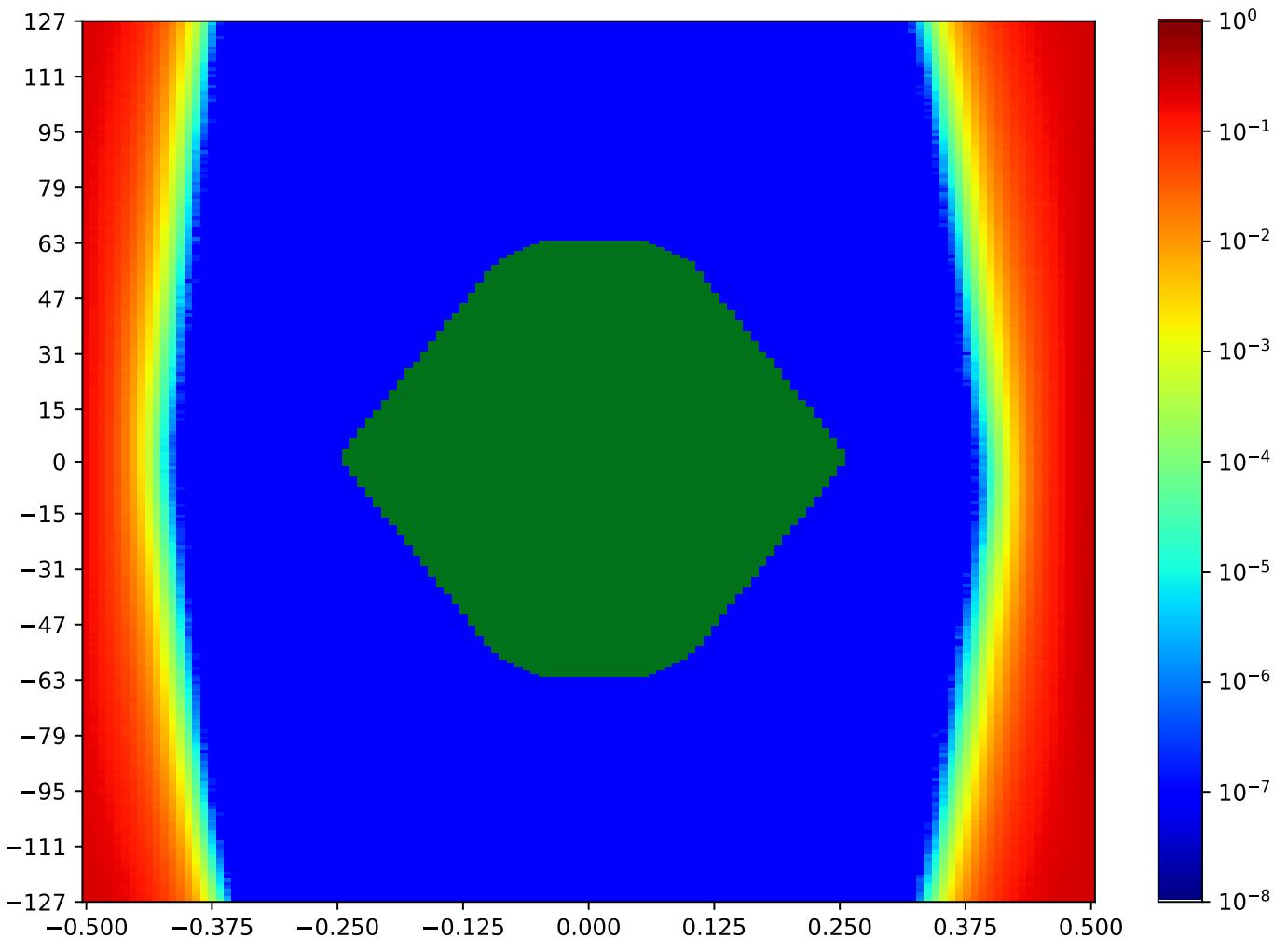


Figure 4.207: MSP_A_FPGA-TX2-05-RX11-05-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.7 MSP_A_FPGA-TX2-06-RX11-06-MSP_C_FPGA

Table 4.192: MSP_A_FPGA-TX2-06-RX11-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:18:11		2018-Sep-28 10:19:27	
Reset RX	OA	HO		VO	VO (%)
true	24557	104		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

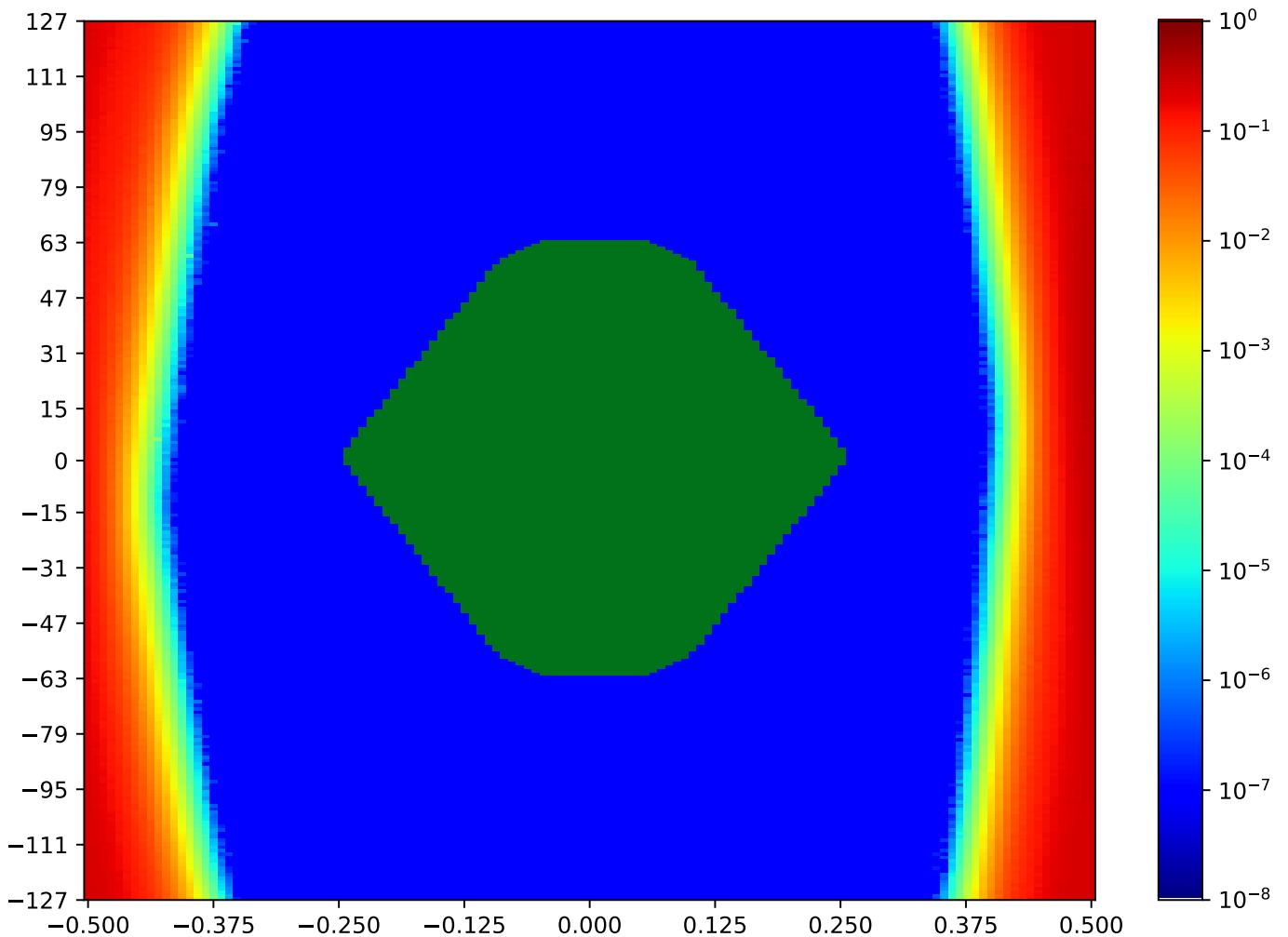


Figure 4.208: MSP_A_FPGA-TX2-06-RX11-06-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.8 MSP_A_FPGA-TX2-07-RX11-07-MSP_C_FPGA

Table 4.193: MSP_A_FPGA-TX2-07-RX11-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:09:22		2018-Sep-28 10:10:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24604	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

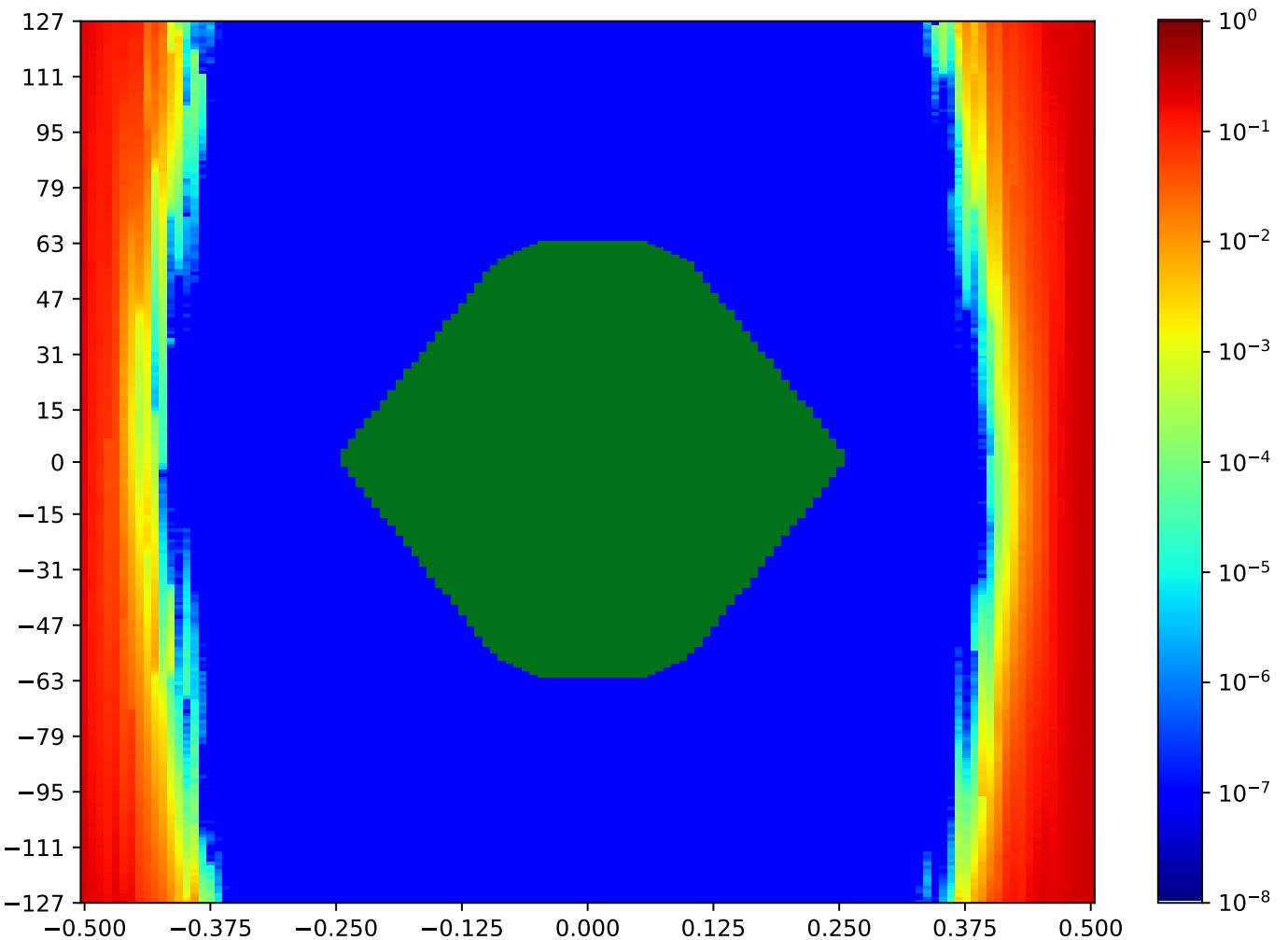


Figure 4.209: MSP_A_FPGA-TX2-07-RX11-07-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.9 MSP_A_FPGA-TX2-08-RX11-08-MSP_C_FPGA

Table 4.194: MSP_A_FPGA-TX2-08-RX11-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:16:55		2018-Sep-28 10:18:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	23572	99	76.74%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

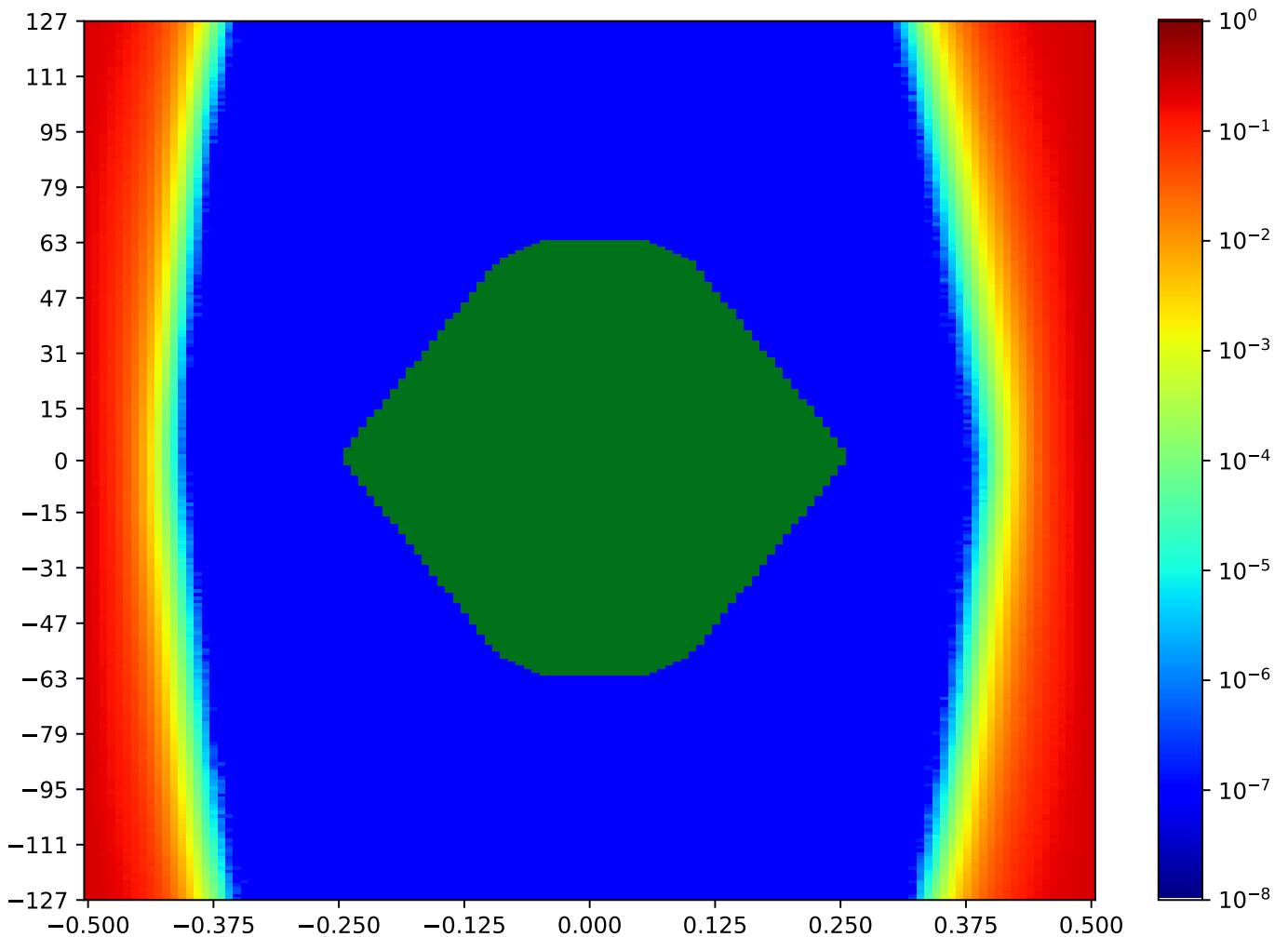


Figure 4.210: MSP_A_FPGA-TX2-08-RX11-08-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.10 MSP_A_FPGA-TX2-09-RX11-09-MSP_C_FPGA

Table 4.195: MSP_A_FPGA-TX2-09-RX11-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:10:38		2018-Sep-28 10:11:53	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24031	101		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

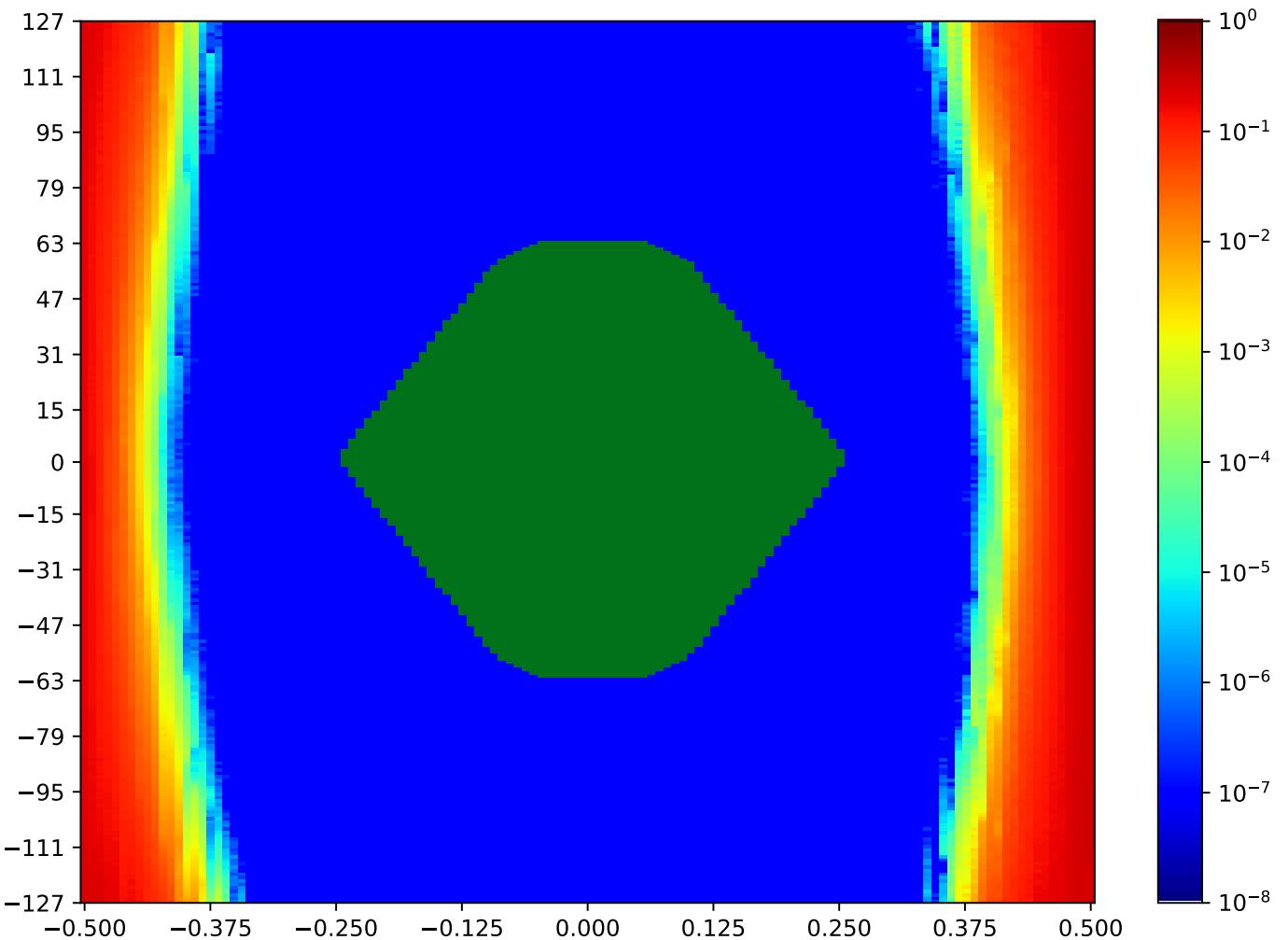


Figure 4.211: MSP_A_FPGA-TX2-09-RX11-09-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.11 MSP_A_FPGA-TX2-10-RX11-10-MSP_C_FPGA

Table 4.196: MSP_A_FPGA-TX2-10-RX11-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:14:24		2018-Sep-28 10:15:40	
Reset RX	OA	HO		VO	VO (%)
true	24495	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

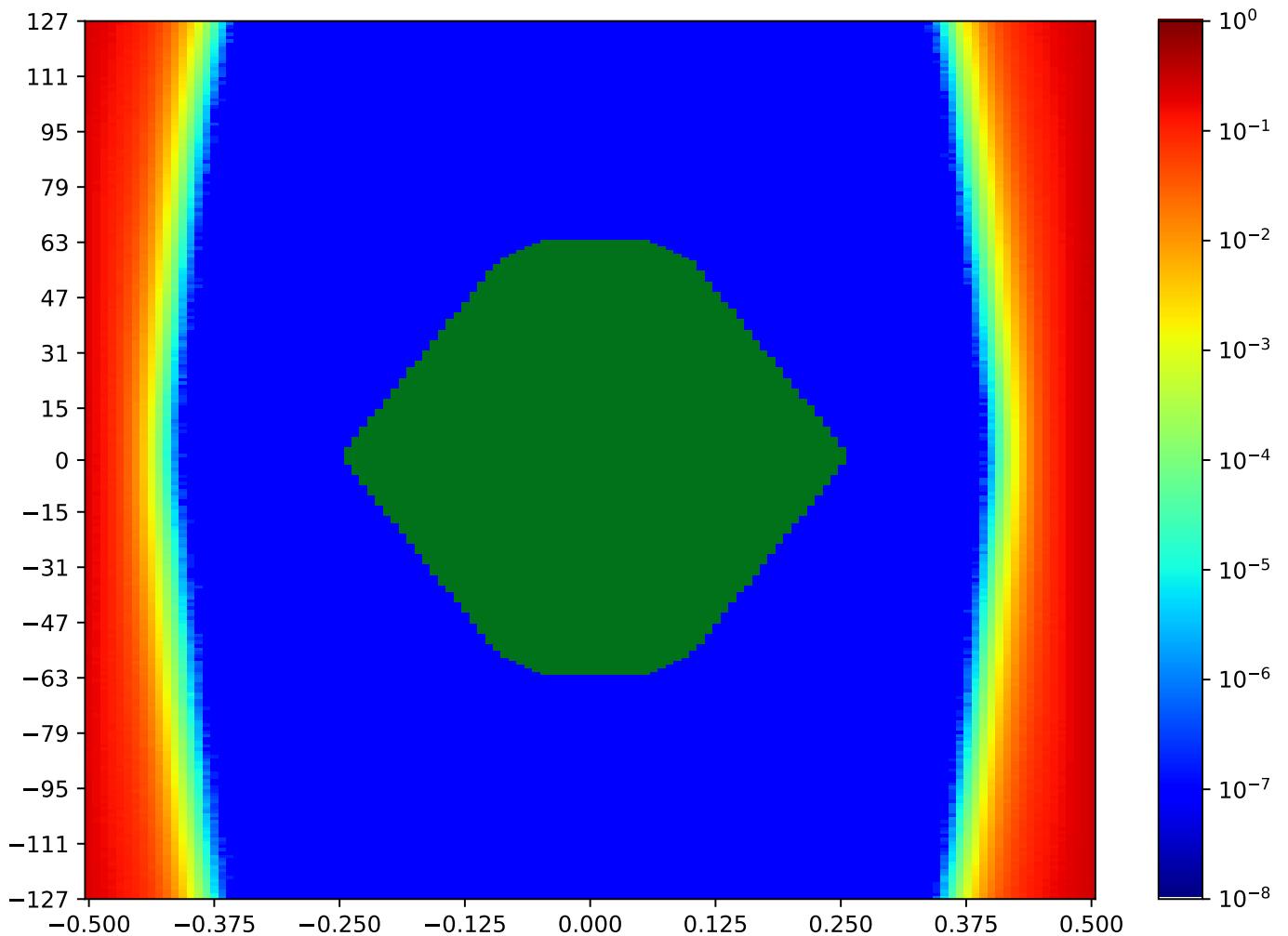


Figure 4.212: MSP_A_FPGA-TX2-10-RX11-10-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.16.12 MSP_A_FPGA-TX2-11-RX11-11-MSP_C_FPGA

Table 4.197: MSP_A_FPGA-TX2-11-RX11-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:13:09		2018-Sep-28 10:14:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24908	105	80.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

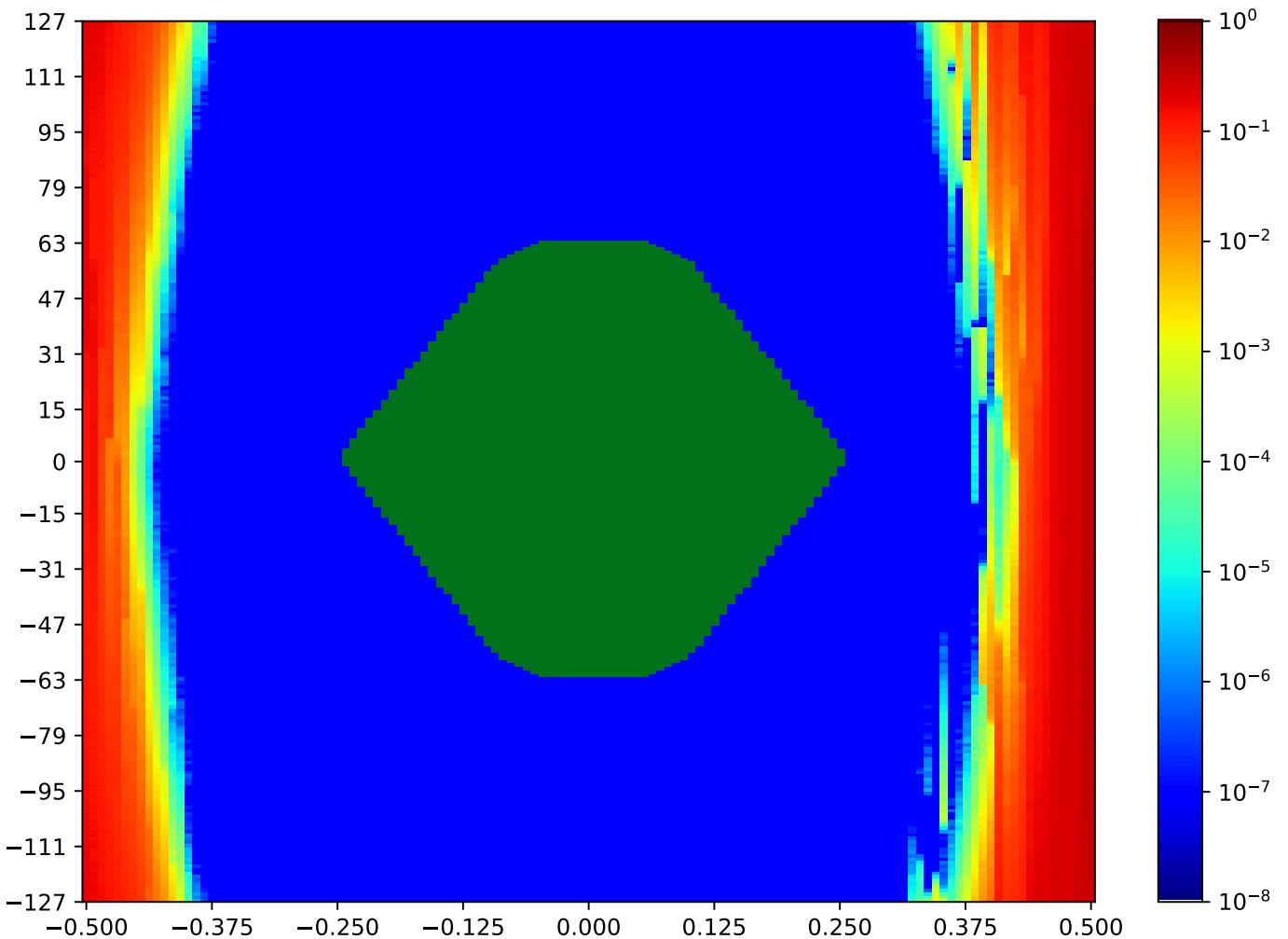


Figure 4.213: MSP_A_FPGA-TX2-11-RX11-11-MSP_C_FPGA

Call back to summary Figure 4.201. Sibling eye diagrams: V2-12.8.

4.17 MSP_C TX3 MSP_A RX1 Minipod Loopback

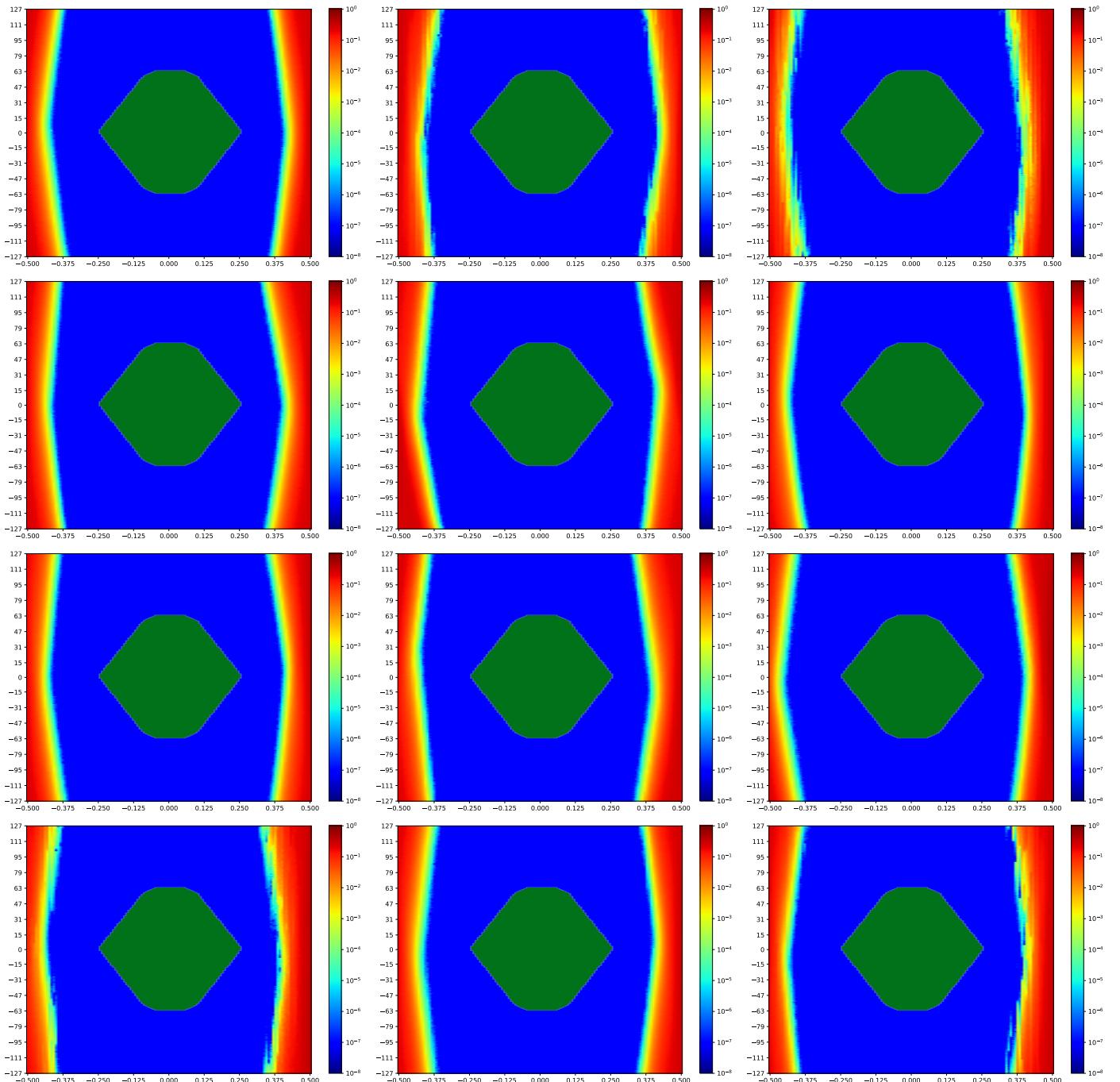


Figure 4.214: MSP_C TX3 MSP_A RX1 Minipod Loopback

A cross-reference to Figure 4.214. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.227.

4.17.1 MSP_C_FPGA-TX3-00-RX1-00-MSP_A_FPGA

Table 4.198: MSP_C_FPGA-TX3-00-RX1-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:23:13		2018-Sep-28 10:24:28	
Reset RX	OA	HO		VO	VO (%)
true	24574	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

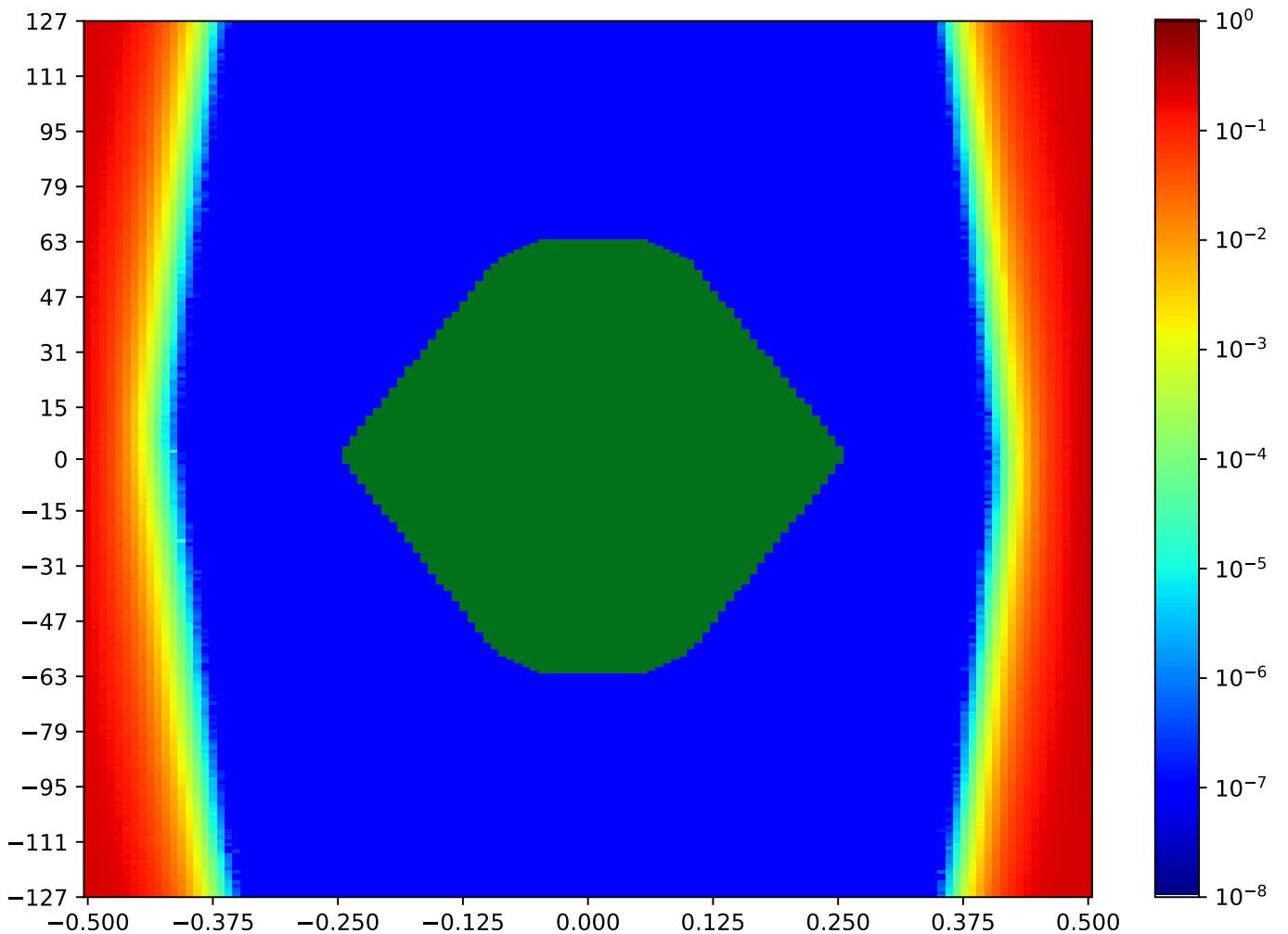


Figure 4.215: MSP_C_FPGA-TX3-00-RX1-00-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.2 MSP_C_FPGA-TX3-01-RX1-01-MSP_A_FPGA

Table 4.199: MSP_C_FPGA-TX3-01-RX1-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:25:44		2018-Sep-28 10:26:59	
Reset RX	OA	HO		VO	VO (%)
true	24529	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

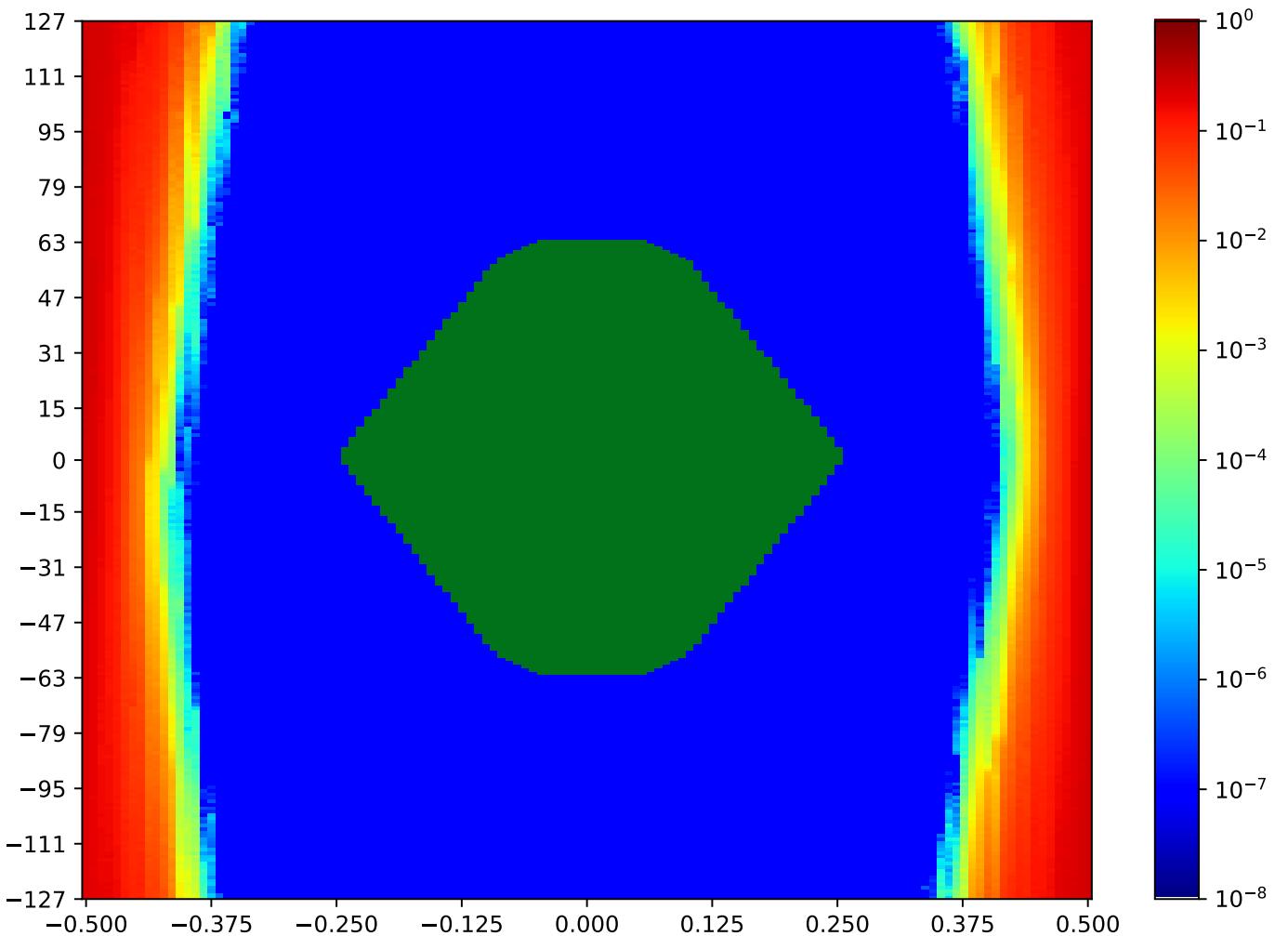


Figure 4.216: MSP_C_FPGA-TX3-01-RX1-01-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.3 MSP_C_FPGA-TX3-02-RX1-02-MSP_A_FPGA

Table 4.200: MSP_C_FPGA-TX3-02-RX1-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:26:59		2018-Sep-28 10:28:15	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24395	103		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

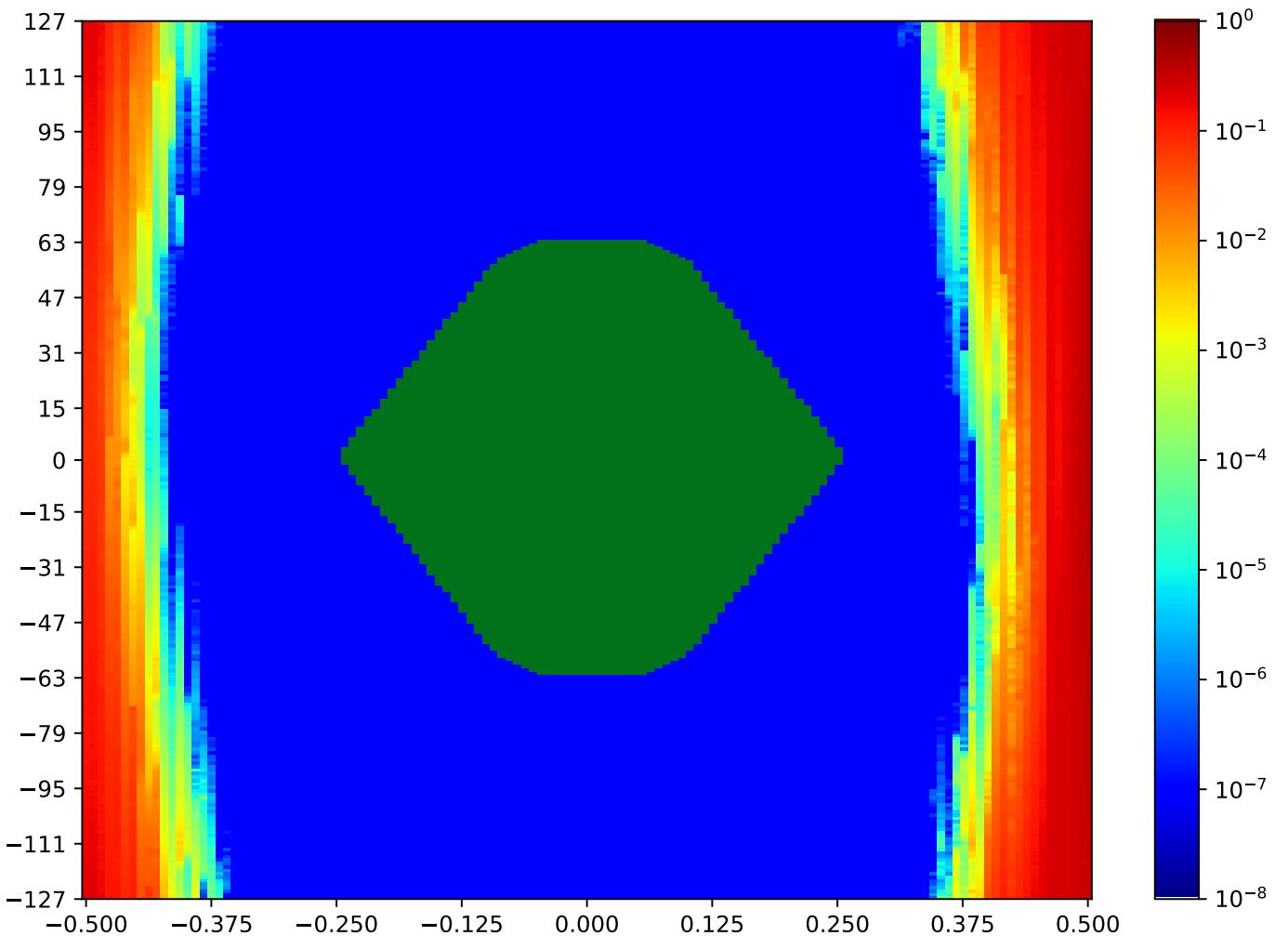


Figure 4.217: MSP_C_FPGA-TX3-02-RX1-02-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.4 MSP_C_FPGA-TX3-03-RX1-03-MSP_A_FPGA

Table 4.201: MSP_C_FPGA-TX3-03-RX1-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:20:42		2018-Sep-28 10:21:57	
Reset RX	OA	HO		VO	VO (%)
true	24159	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

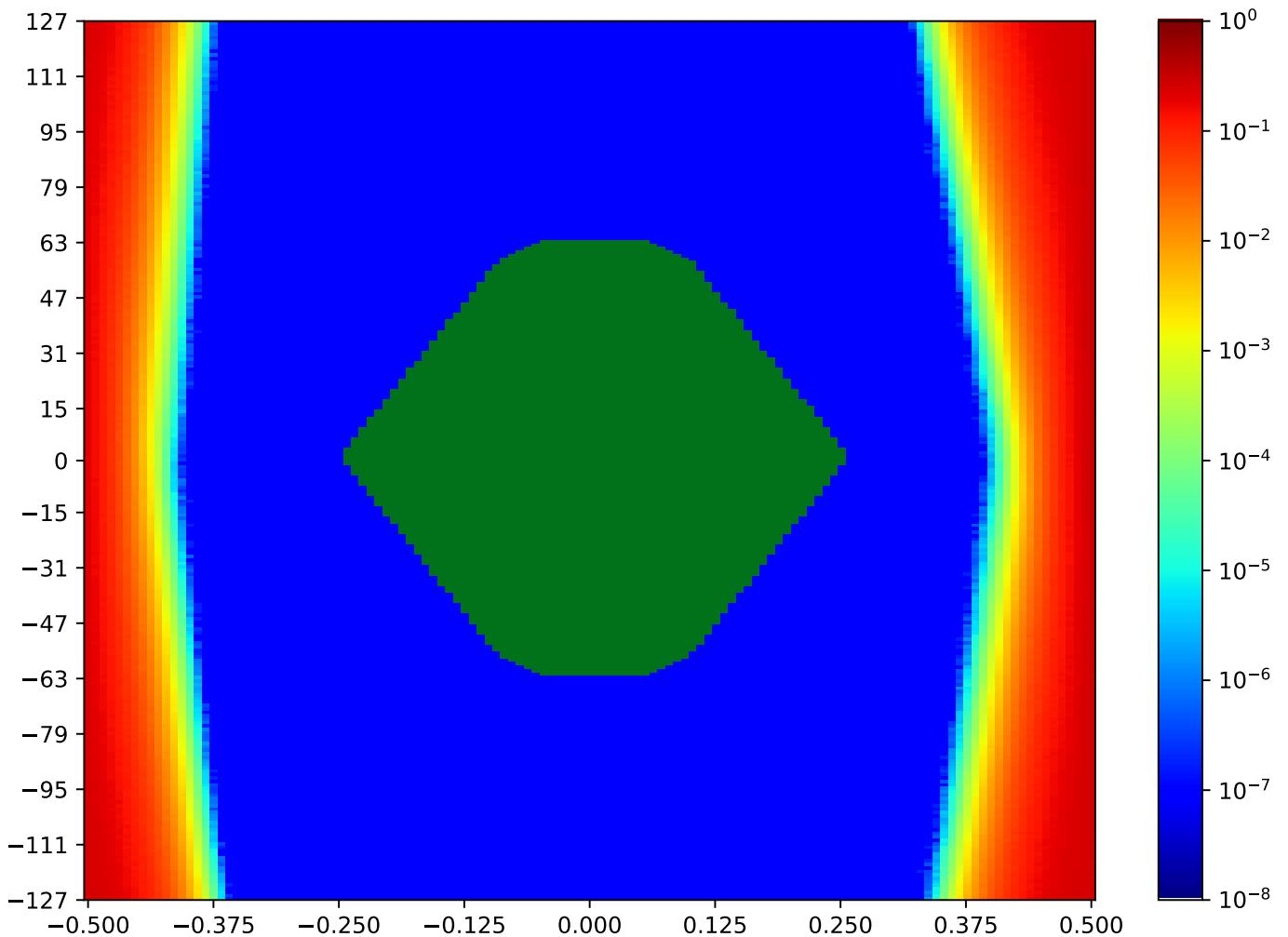


Figure 4.218: MSP_C_FPGA-TX3-03-RX1-03-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.5 MSP_C_FPGA-TX3-04-RX1-04-MSP_A_FPGA

Table 4.202: MSP_C_FPGA-TX3-04-RX1-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:30:46		2018-Sep-28 10:32:01	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24225	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

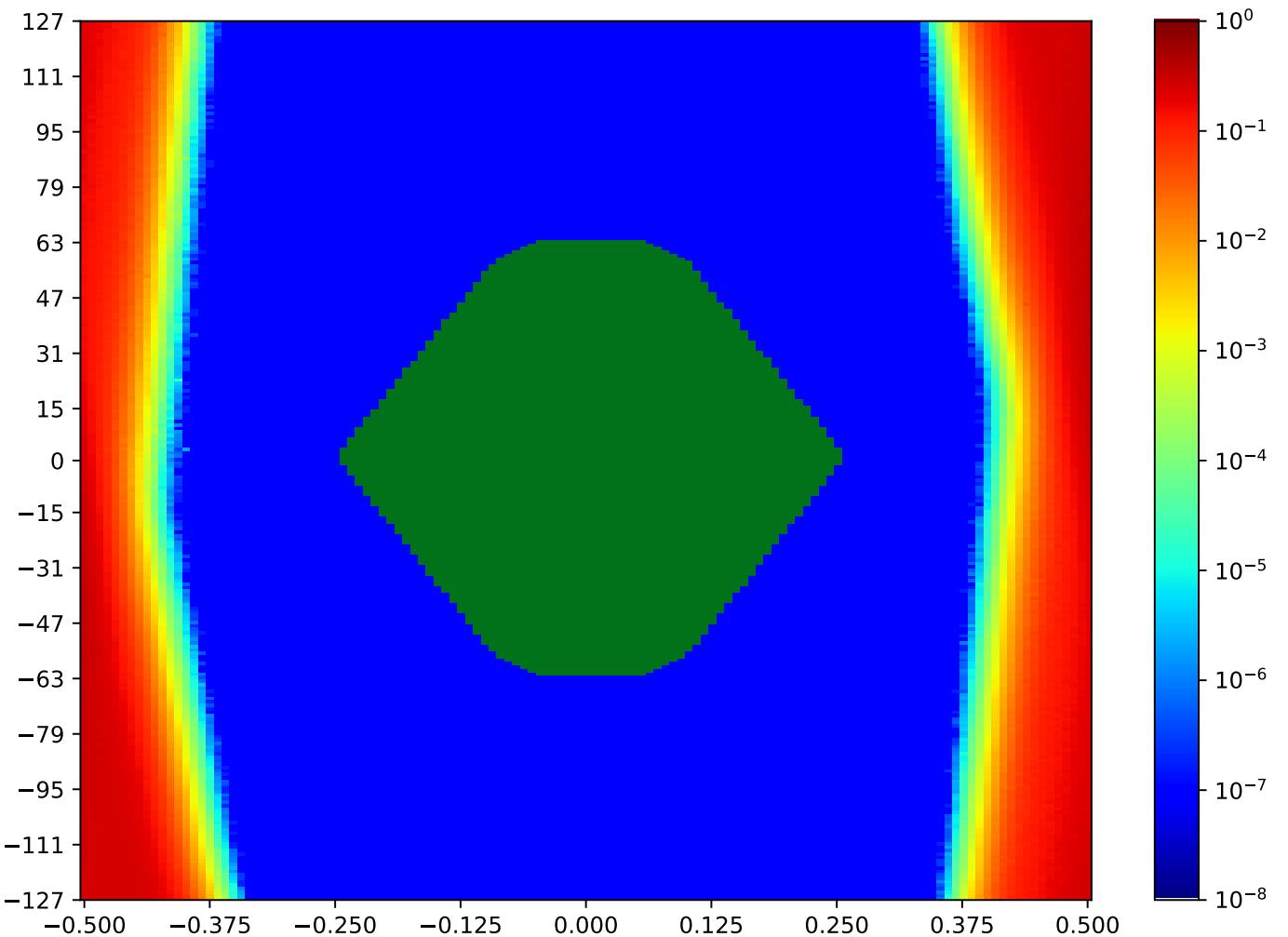


Figure 4.219: MSP_C_FPGA-TX3-04-RX1-04-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.6 MSP_C_FPGA-TX3-05-RX1-05-MSP_A_FPGA

Table 4.203: MSP_C_FPGA-TX3-05-RX1-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:19:27		2018-Sep-28 10:20:42	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24715	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

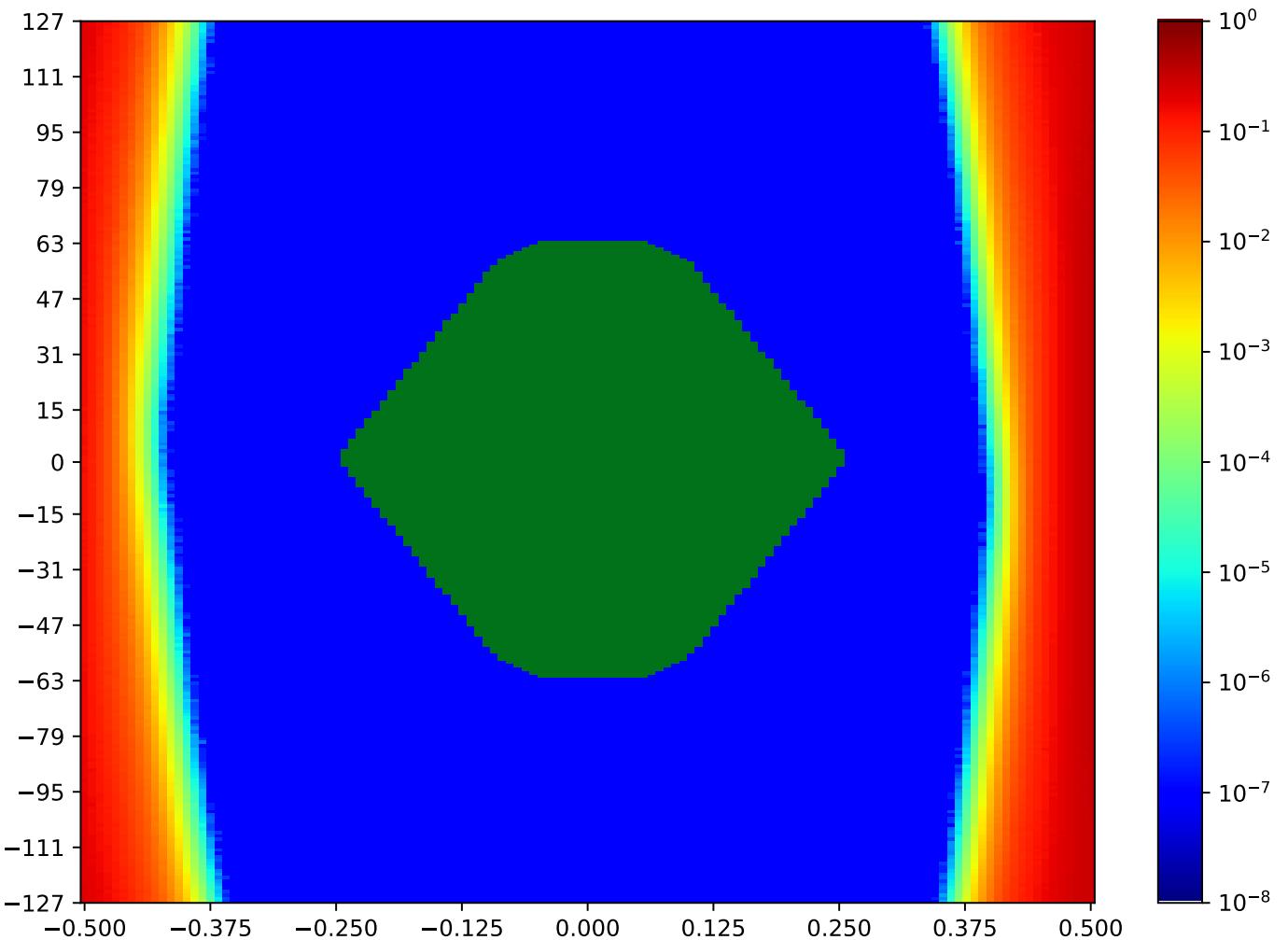


Figure 4.220: MSP_C_FPGA-TX3-05-RX1-05-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.7 MSP_C_FPGA-TX3-06-RX1-06-MSP_A_FPGA

Table 4.204: MSP_C_FPGA-TX3-06-RX1-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:33:17		2018-Sep-28 10:34:32	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24653	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

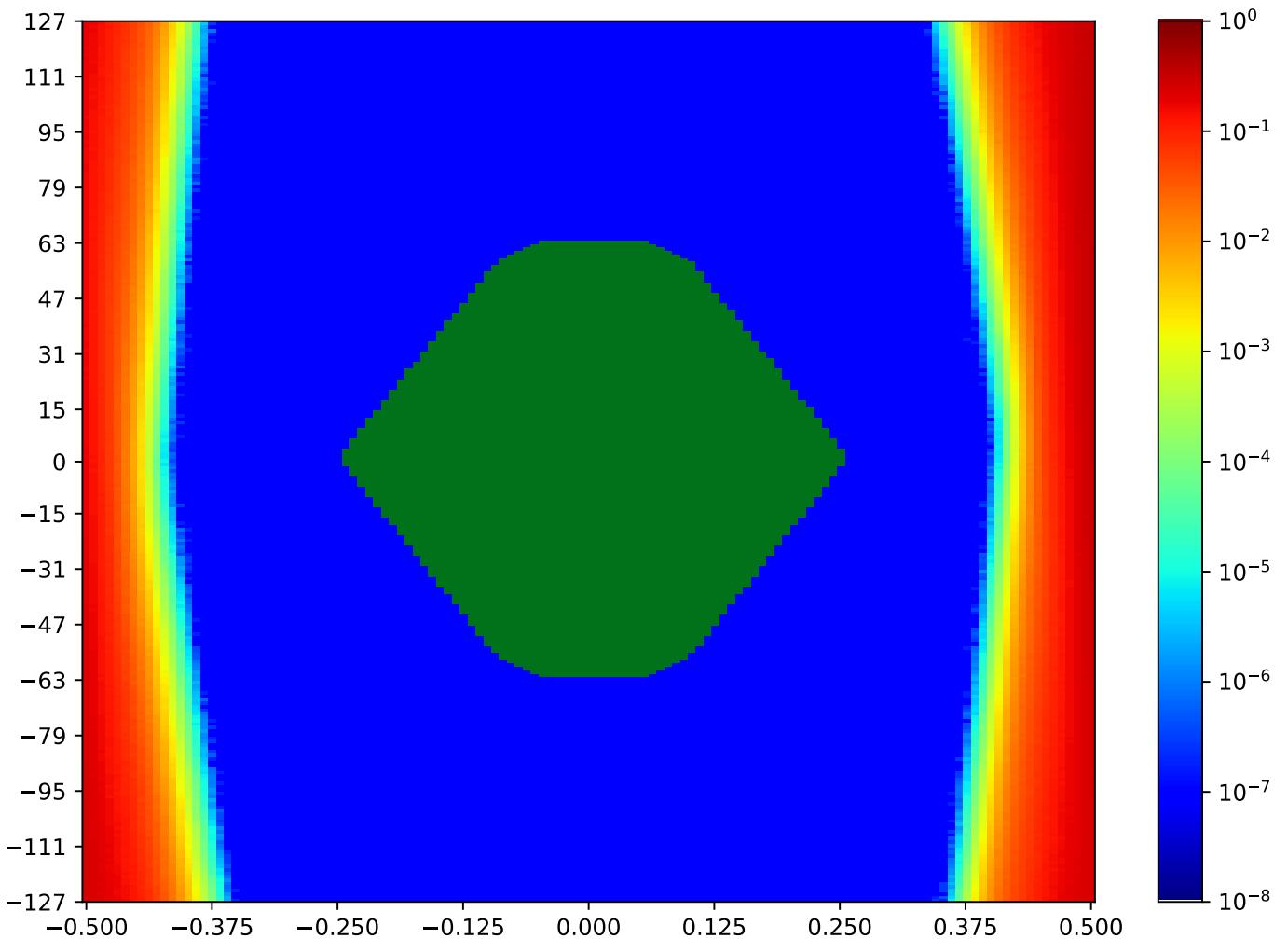


Figure 4.221: MSP_C_FPGA-TX3-06-RX1-06-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.8 MSP_C_FPGA-TX3-07-RX1-07-MSP_A_FPGA

Table 4.205: MSP_C_FPGA-TX3-07-RX1-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:21:58		2018-Sep-28 10:23:13	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24053	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

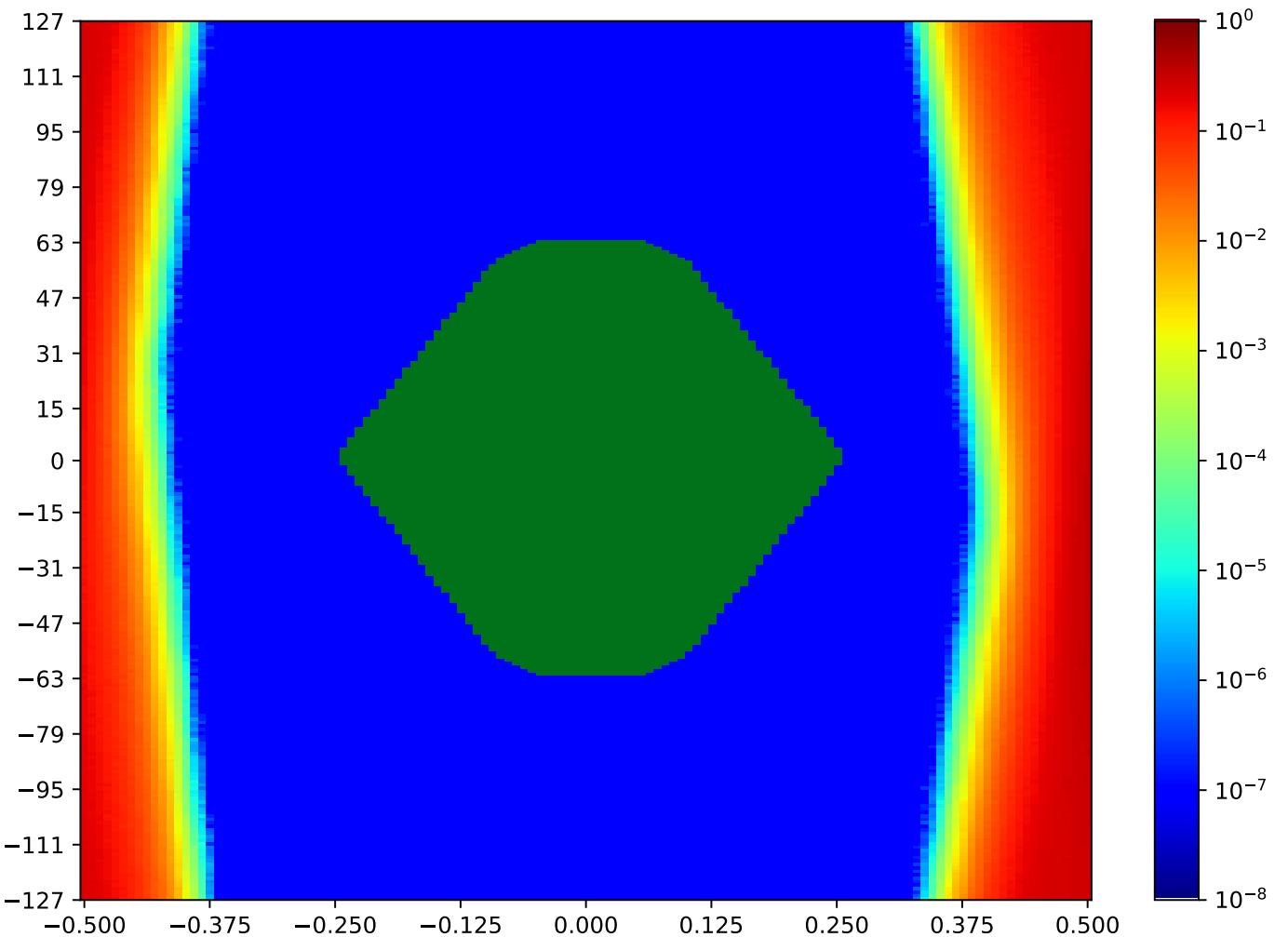


Figure 4.222: MSP_C_FPGA-TX3-07-RX1-07-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.9 MSP_C_FPGA-TX3-08-RX1-08-MSP_A_FPGA

Table 4.206: MSP_C_FPGA-TX3-08-RX1-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:32:01		2018-Sep-28 10:33:17	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	25012	104		80.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

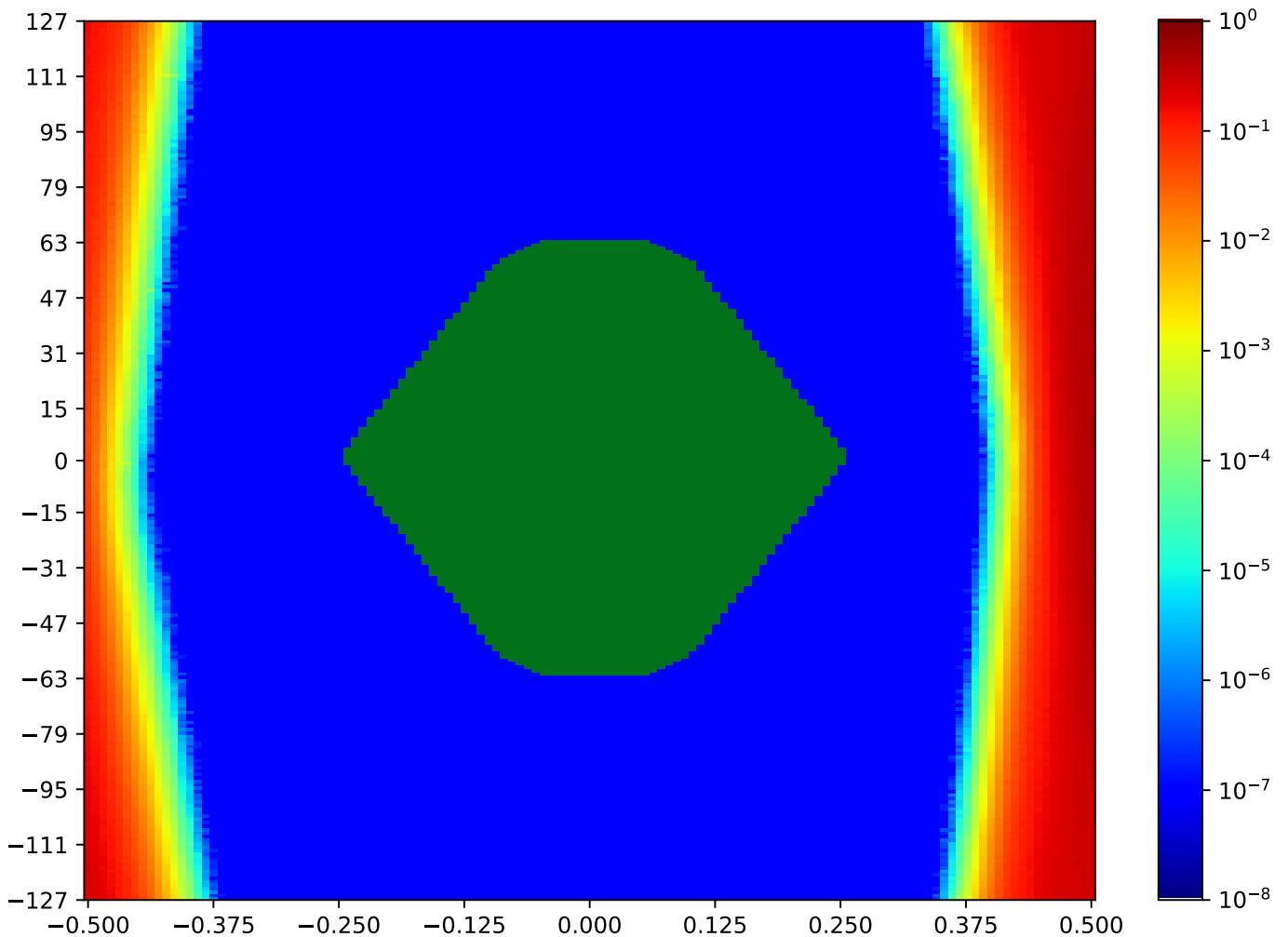


Figure 4.223: MSP_C_FPGA-TX3-08-RX1-08-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.10 MSP_C_FPGA-TX3-09-RX1-09-MSP_A_FPGA

Table 4.207: MSP_C_FPGA-TX3-09-RX1-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:24:29		2018-Sep-28 10:25:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24458	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

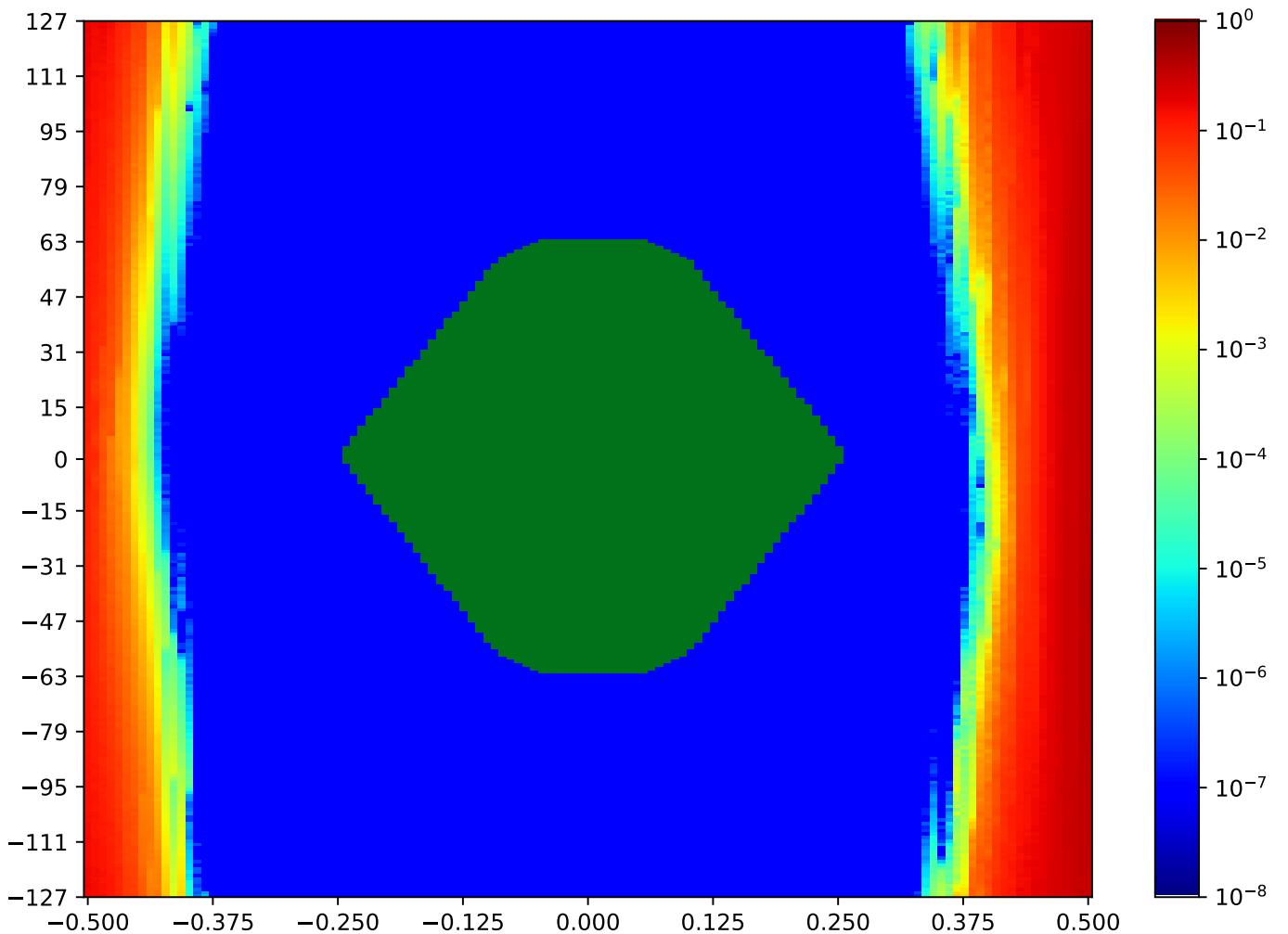


Figure 4.224: MSP_C_FPGA-TX3-09-RX1-09-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.11 MSP_C_FPGA-TX3-10-RX1-10-MSP_A_FPGA

Table 4.208: MSP_C_FPGA-TX3-10-RX1-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:29:31		2018-Sep-28 10:30:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24199	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

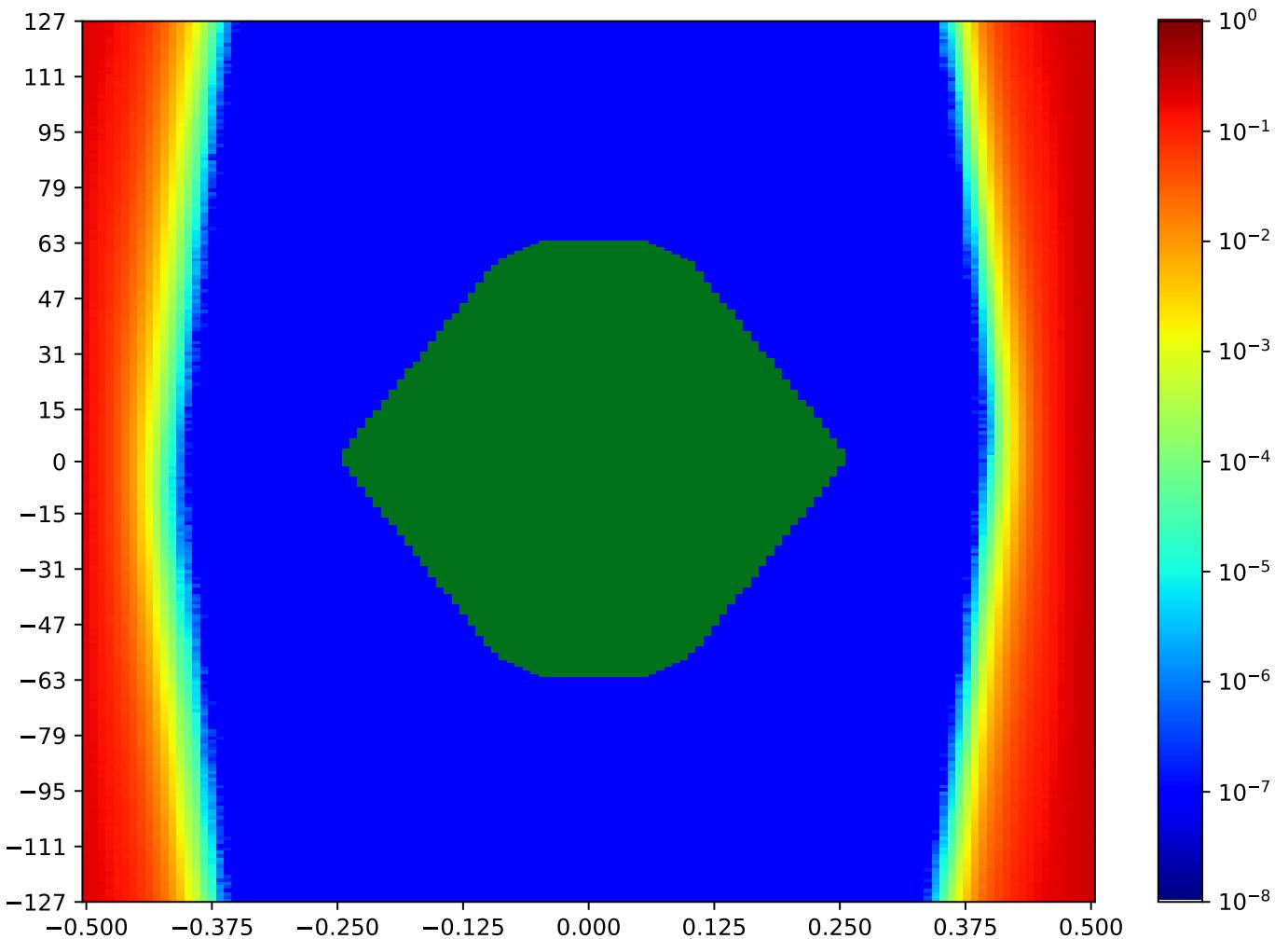


Figure 4.225: MSP_C_FPGA-TX3-10-RX1-10-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.17.12 MSP_C_FPGA-TX3-11-RX1-11-MSP_A_FPGA

Table 4.209: MSP_C_FPGA-TX3-11-RX1-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:28:15		2018-Sep-28 10:29:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24805	103	79.84%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

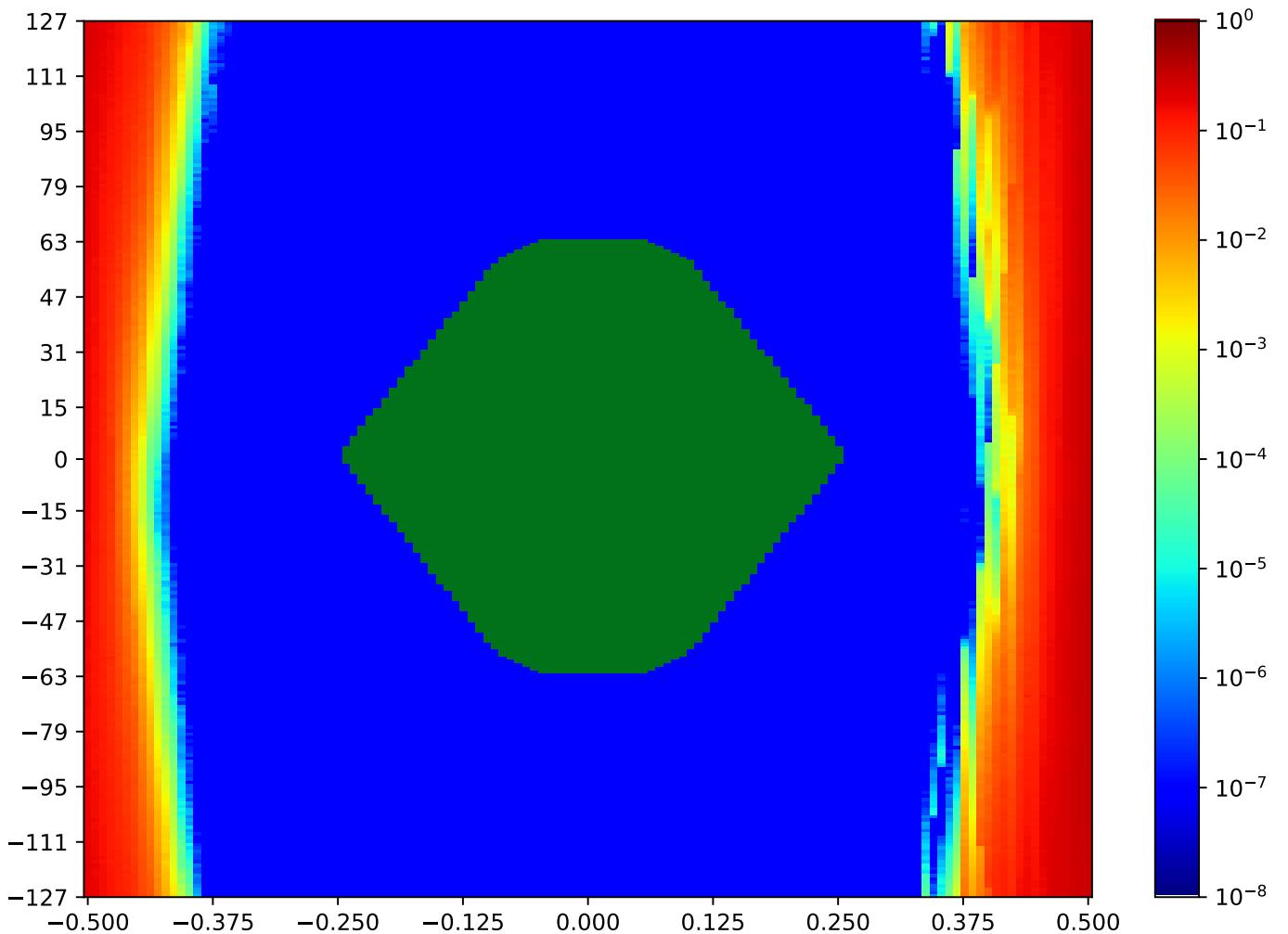


Figure 4.226: MSP_C_FPGA-TX3-11-RX1-11-MSP_A_FPGA

Call back to summary Figure 4.214. Sibling eye diagrams: V2-12.8.

4.18 MSP_C TX4 MSP_A RX2 Minipod Loopback

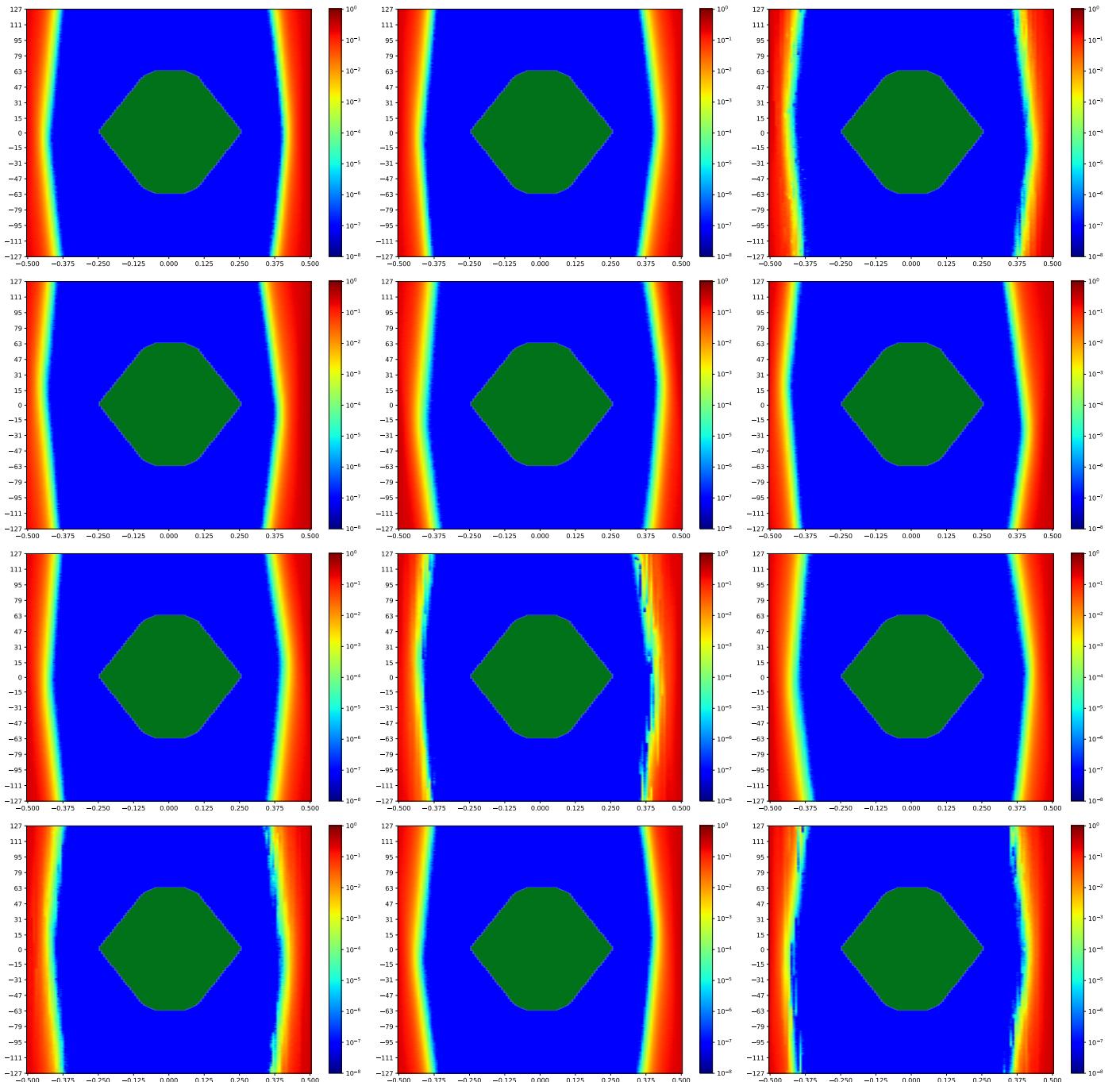


Figure 4.227: MSP_C TX4 MSP_A RX2 Minipod Loopback

A cross-reference to Figure 4.227. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.240.

4.18.1 MSP_C_FPGA-TX4-00-RX2-00-MSP_A_FPGA

Table 4.210: MSP_C_FPGA-TX4-00-RX2-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:38:19		2018-Sep-28 10:39:34	
Reset RX	OA	HO		VO	VO (%)
true	24909	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

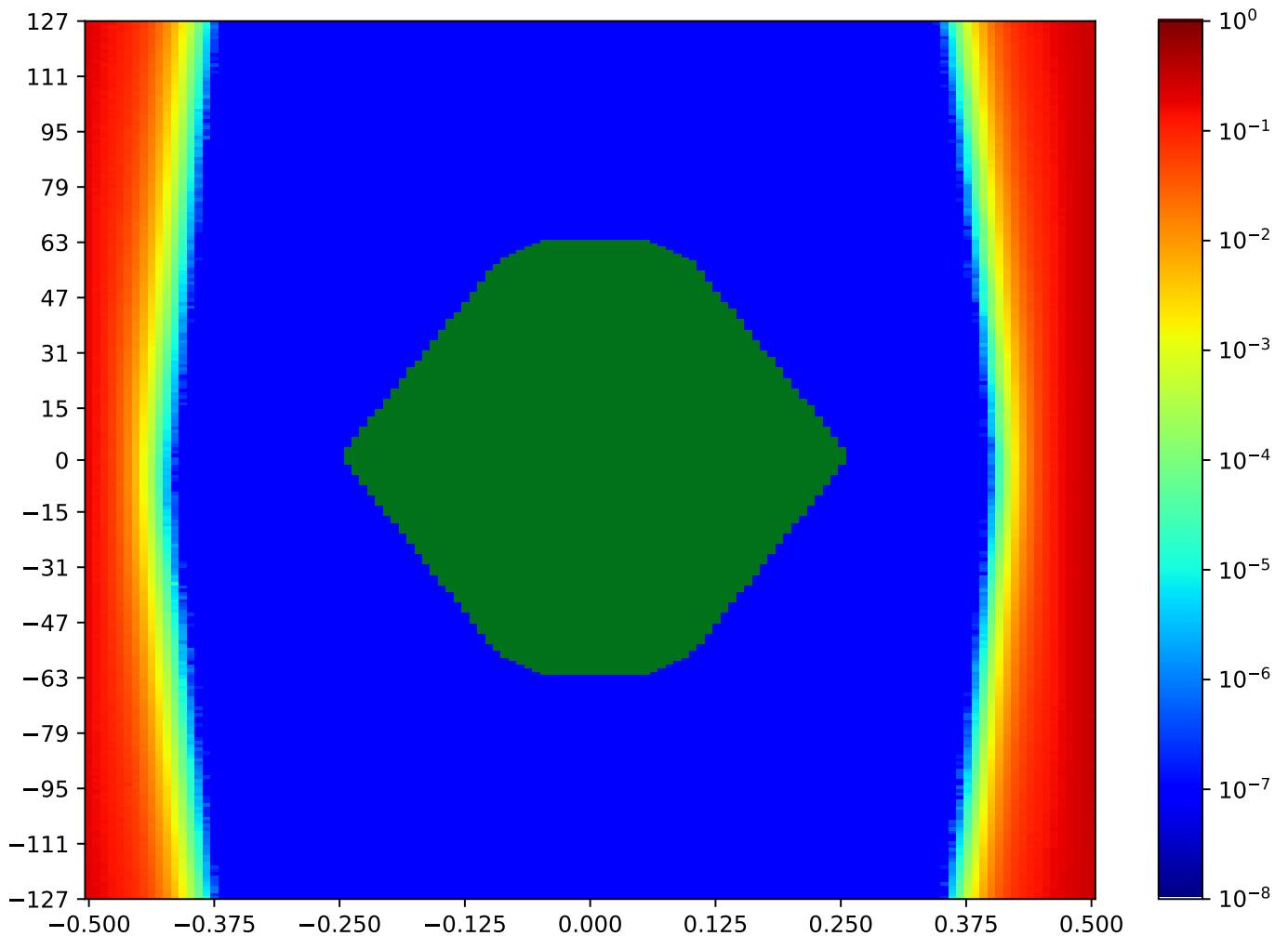


Figure 4.228: MSP_C_FPGA-TX4-00-RX2-00-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.2 MSP_C_FPGA-TX4-01-RX2-01-MSP_A_FPGA

Table 4.211: MSP_C_FPGA-TX4-01-RX2-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:35:48		2018-Sep-28 10:37:03	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24556	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

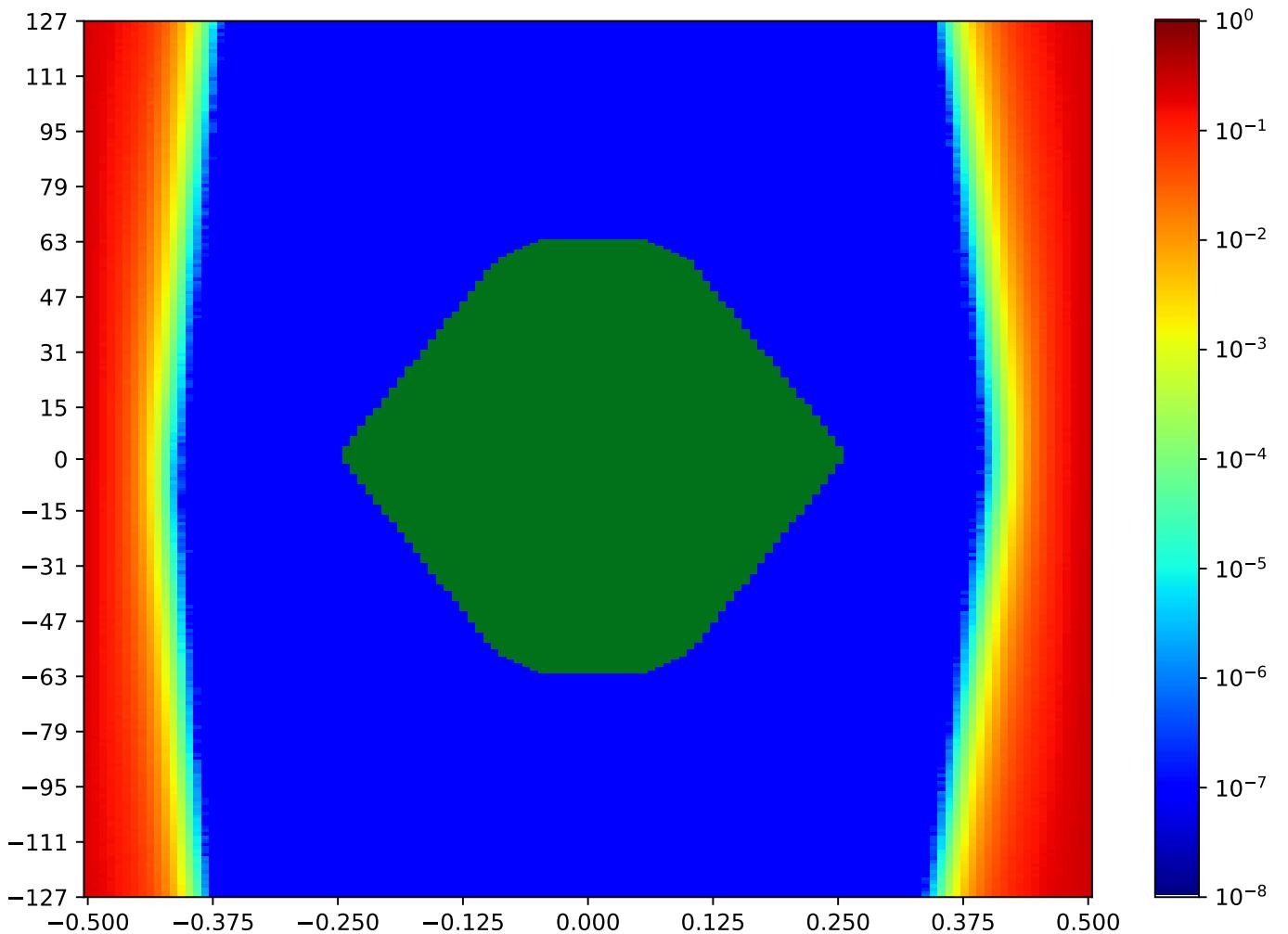


Figure 4.229: MSP_C_FPGA-TX4-01-RX2-01-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.3 MSP_C_FPGA-TX4-02-RX2-02-MSP_A_FPGA

Table 4.212: MSP_C_FPGA-TX4-02-RX2-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:42:06		2018-Sep-28 10:43:21	
Reset RX	OA	HO		VO	VO (%)
true	24823	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

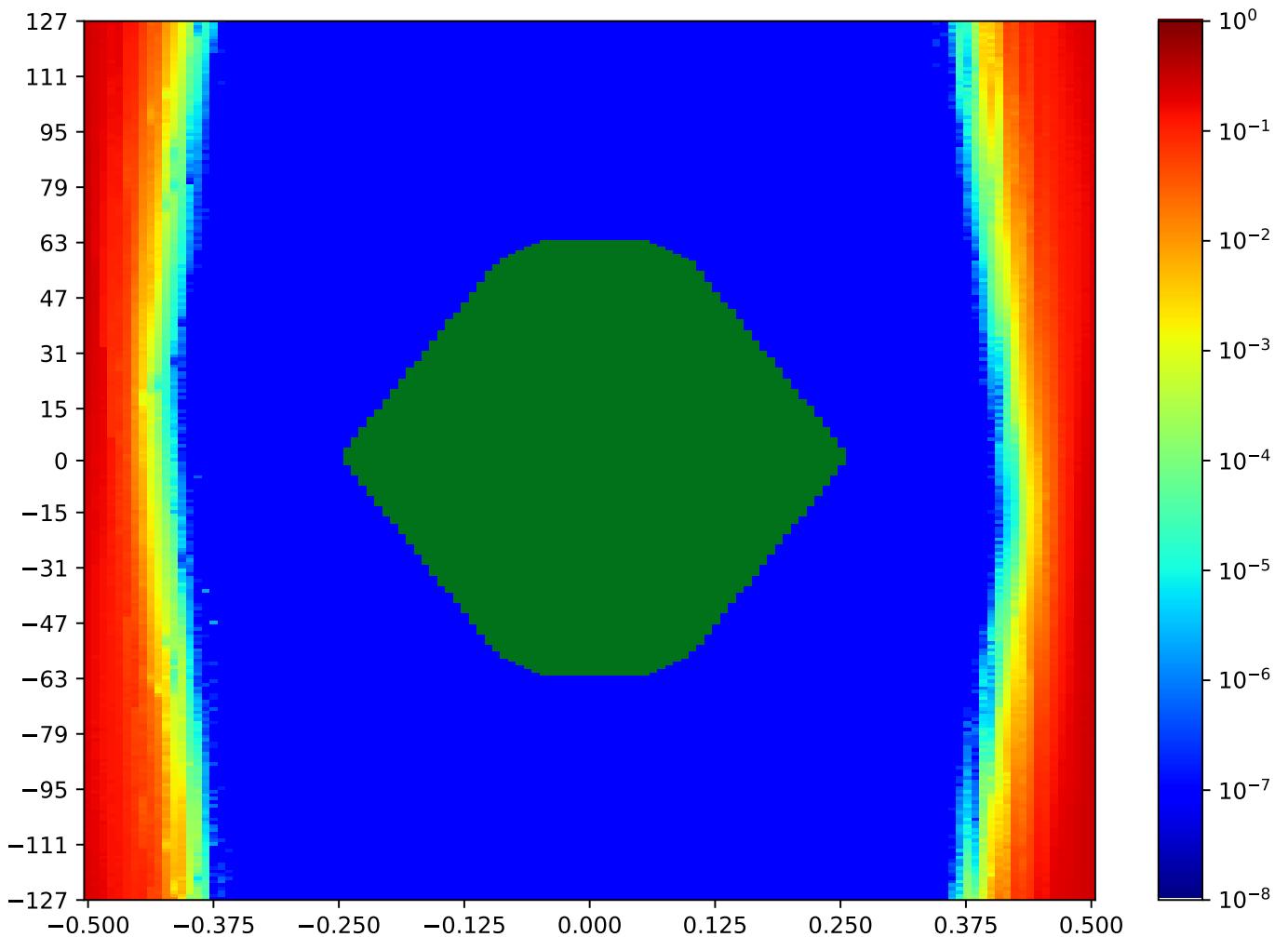


Figure 4.230: MSP_C_FPGA-TX4-02-RX2-02-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.4 MSP_C_FPGA-TX4-03-RX2-03-MSP_A_FPGA

Table 4.213: MSP_C_FPGA-TX4-03-RX2-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:34:33		2018-Sep-28 10:35:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24318	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

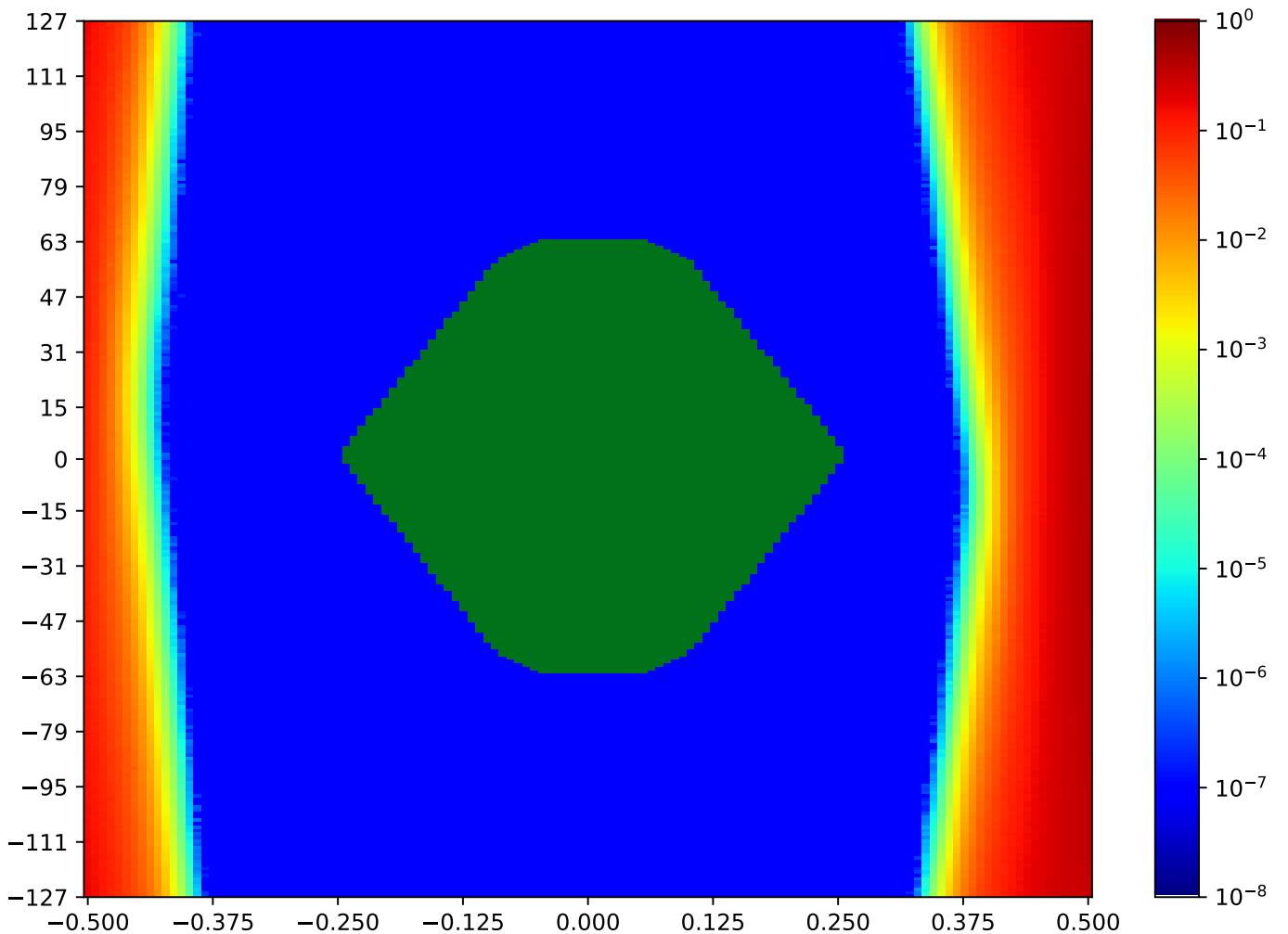


Figure 4.231: MSP_C_FPGA-TX4-03-RX2-03-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.5 MSP_C_FPGA-TX4-04-RX2-04-MSP_A_FPGA

Table 4.214: MSP_C_FPGA-TX4-04-RX2-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:45:52		2018-Sep-28 10:47:07	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24440	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

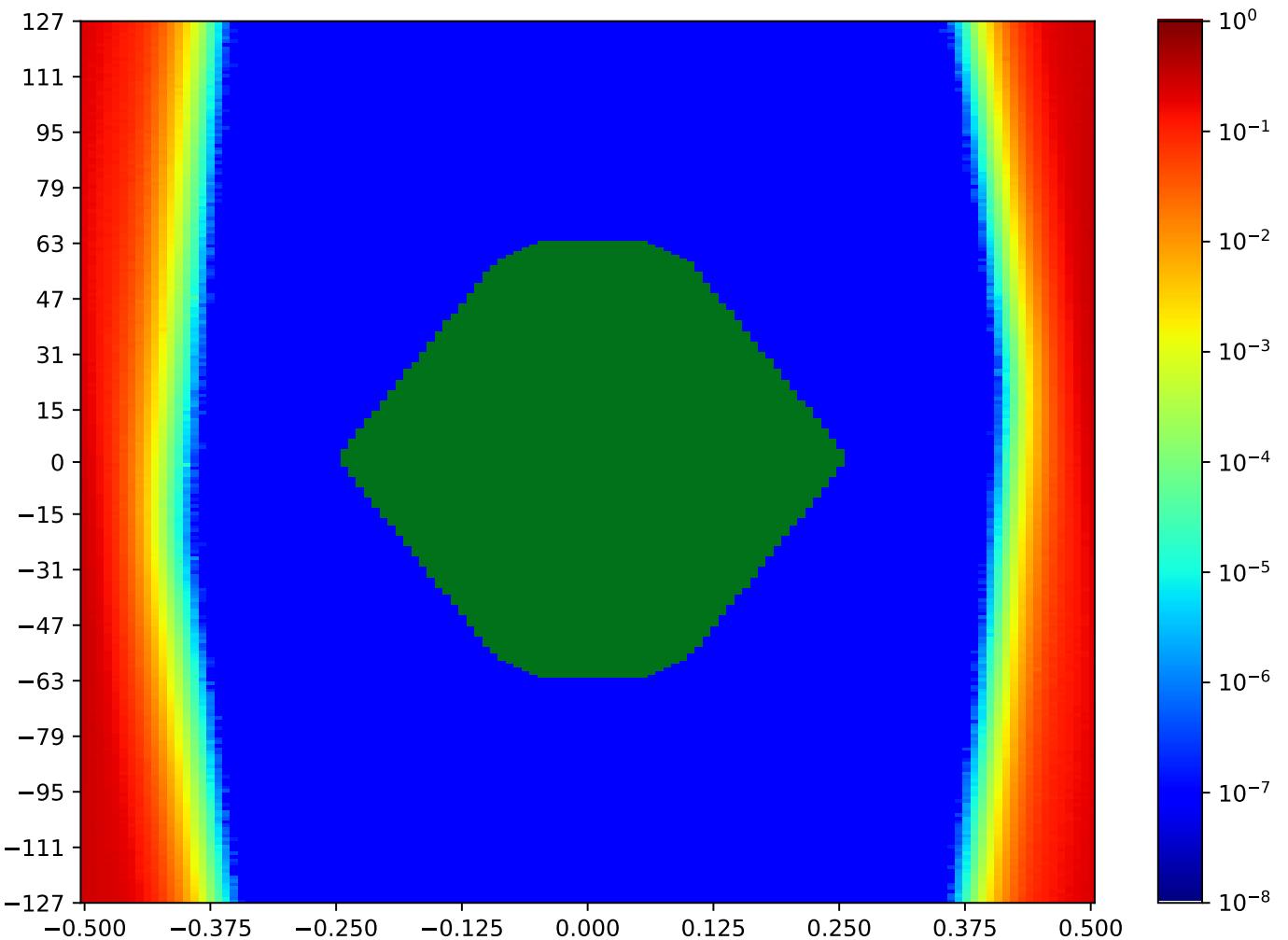


Figure 4.232: MSP_C_FPGA-TX4-04-RX2-04-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.6 MSP_C_FPGA-TX4-05-RX2-05-MSP_A_FPGA

Table 4.215: MSP_C_FPGA-TX4-05-RX2-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:37:03		2018-Sep-28 10:38:19	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24614	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

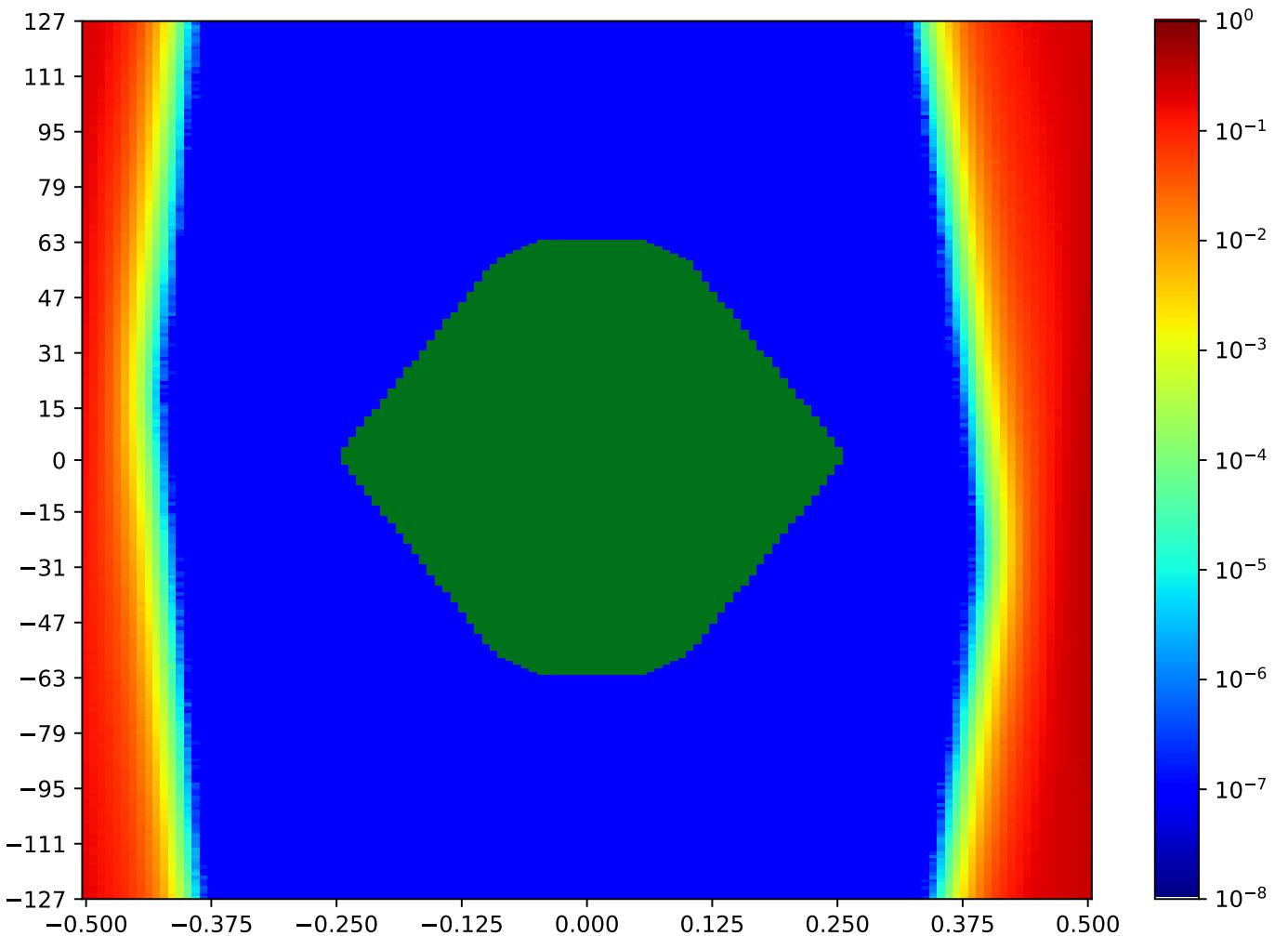


Figure 4.233: MSP_C_FPGA-TX4-05-RX2-05-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.7 MSP_C_FPGA-TX4-06-RX2-06-MSP_A_FPGA

Table 4.216: MSP_C_FPGA-TX4-06-RX2-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:48:23		2018-Sep-28 10:49:38	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24329	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

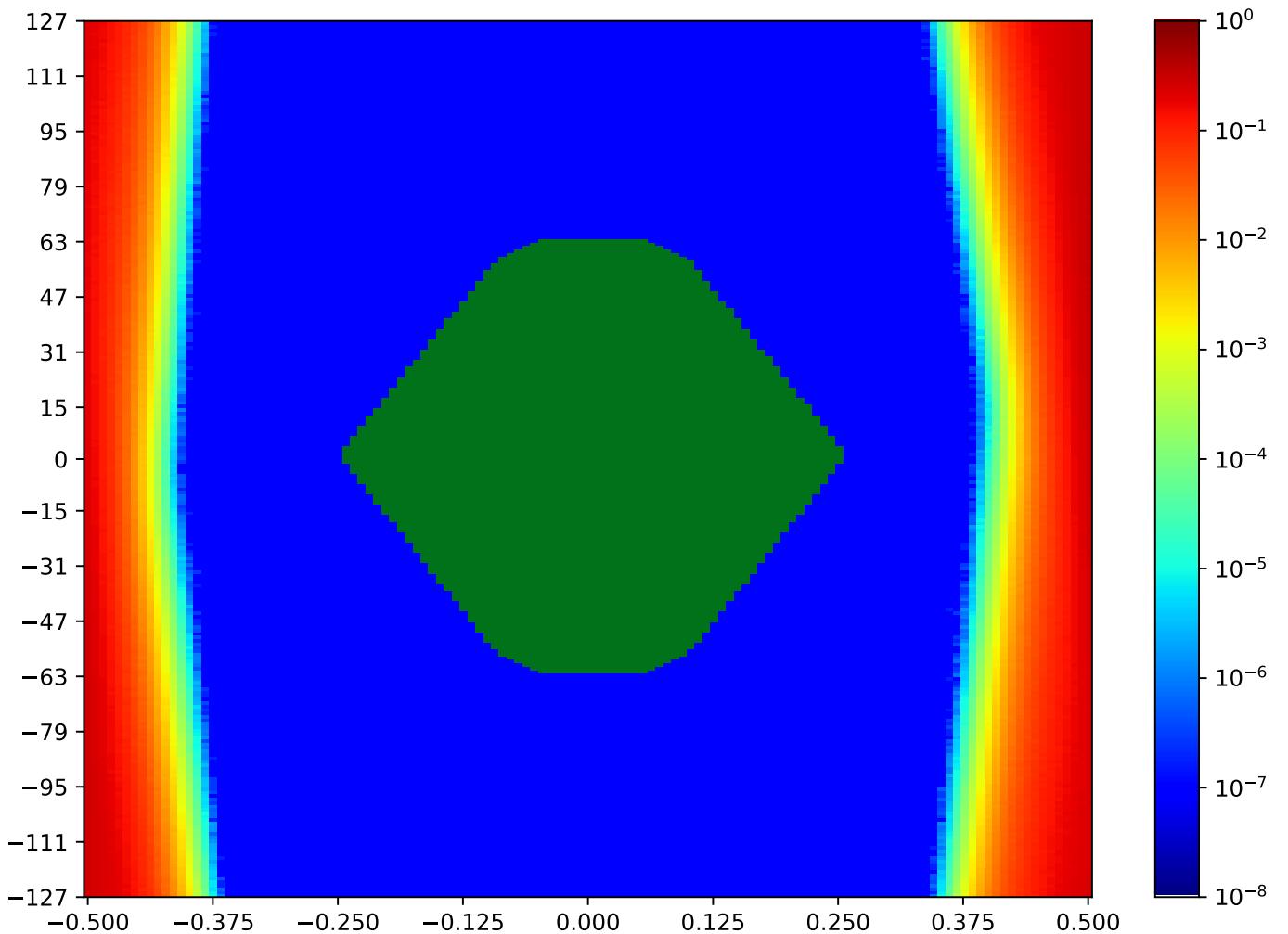


Figure 4.234: MSP_C_FPGA-TX4-06-RX2-06-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.8 MSP_C_FPGA-TX4-07-RX2-07-MSP_A_FPGA

Table 4.217: MSP_C_FPGA-TX4-07-RX2-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:39:35		2018-Sep-28 10:40:50	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24464	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

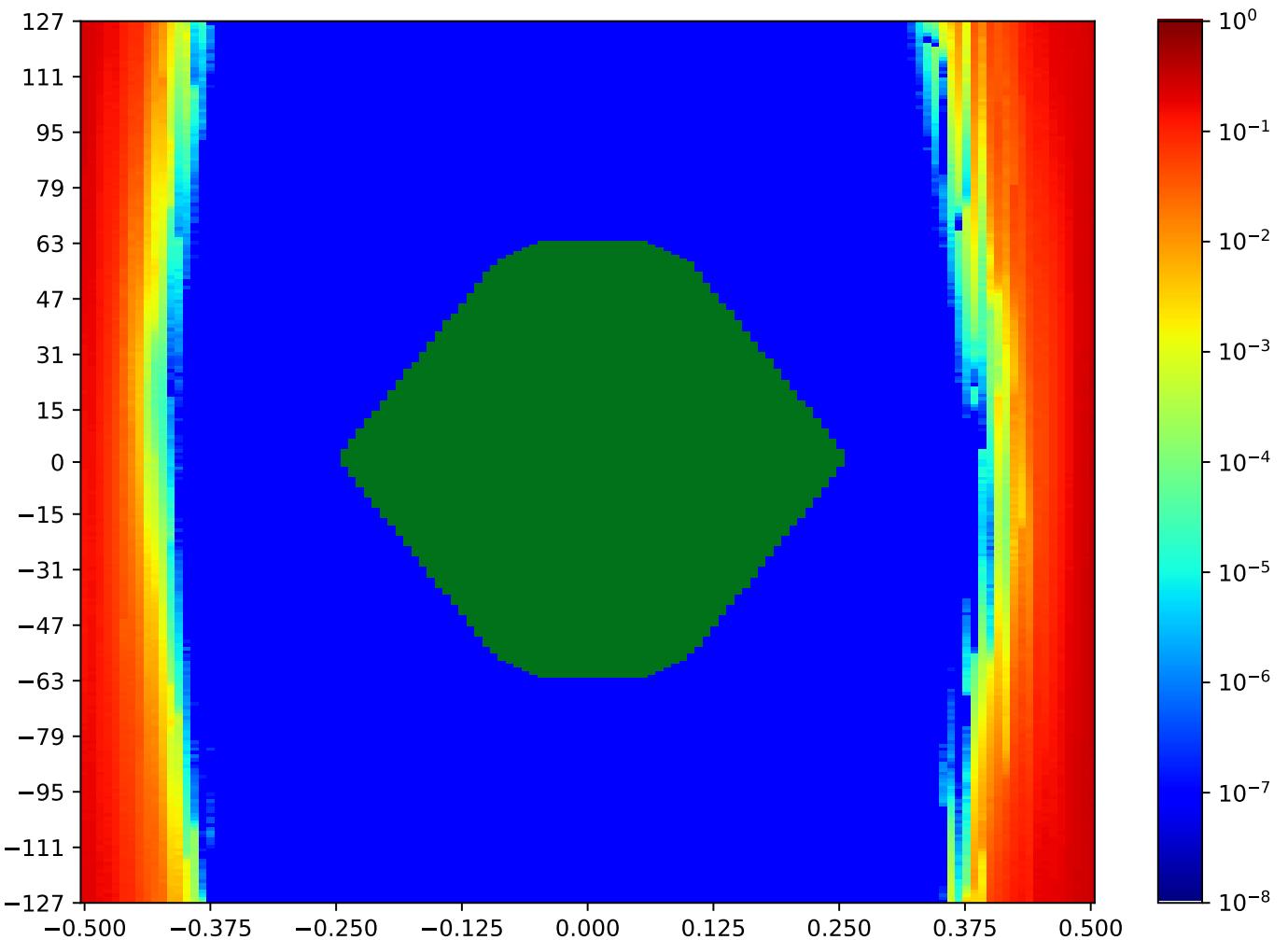


Figure 4.235: MSP_C_FPGA-TX4-07-RX2-07-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.9 MSP_C_FPGA-TX4-08-RX2-08-MSP_A_FPGA

Table 4.218: MSP_C_FPGA-TX4-08-RX2-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:47:07		2018-Sep-28 10:48:23	
Reset RX	OA	HO		VO	VO (%)
true	23939	100		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

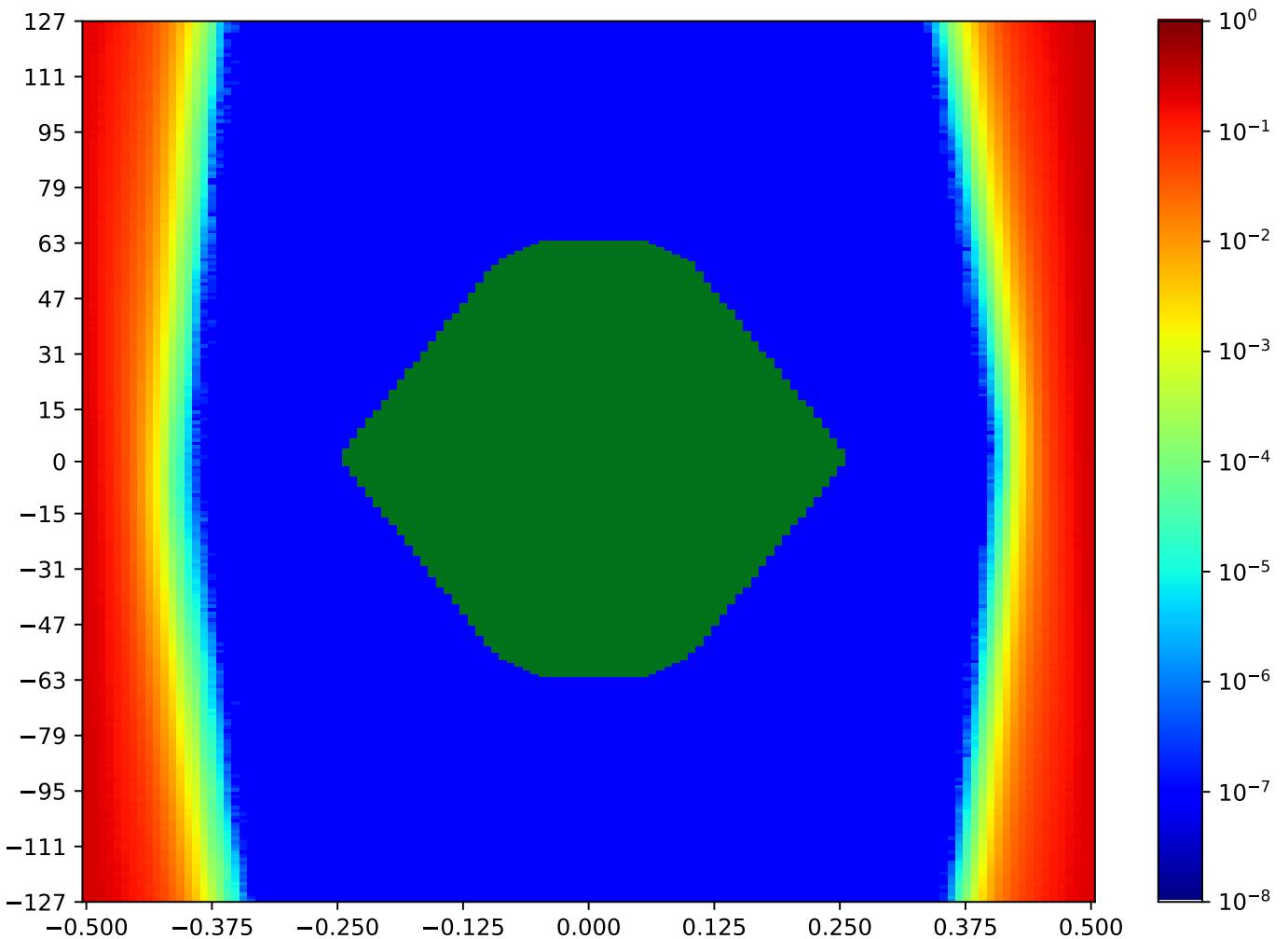


Figure 4.236: MSP_C_FPGA-TX4-08-RX2-08-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.10 MSP_C_FPGA-TX4-09-RX2-09-MSP_A_FPGA

Table 4.219: MSP_C_FPGA-TX4-09-RX2-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:40:50		2018-Sep-28 10:42:06	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24250	102	79.07%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

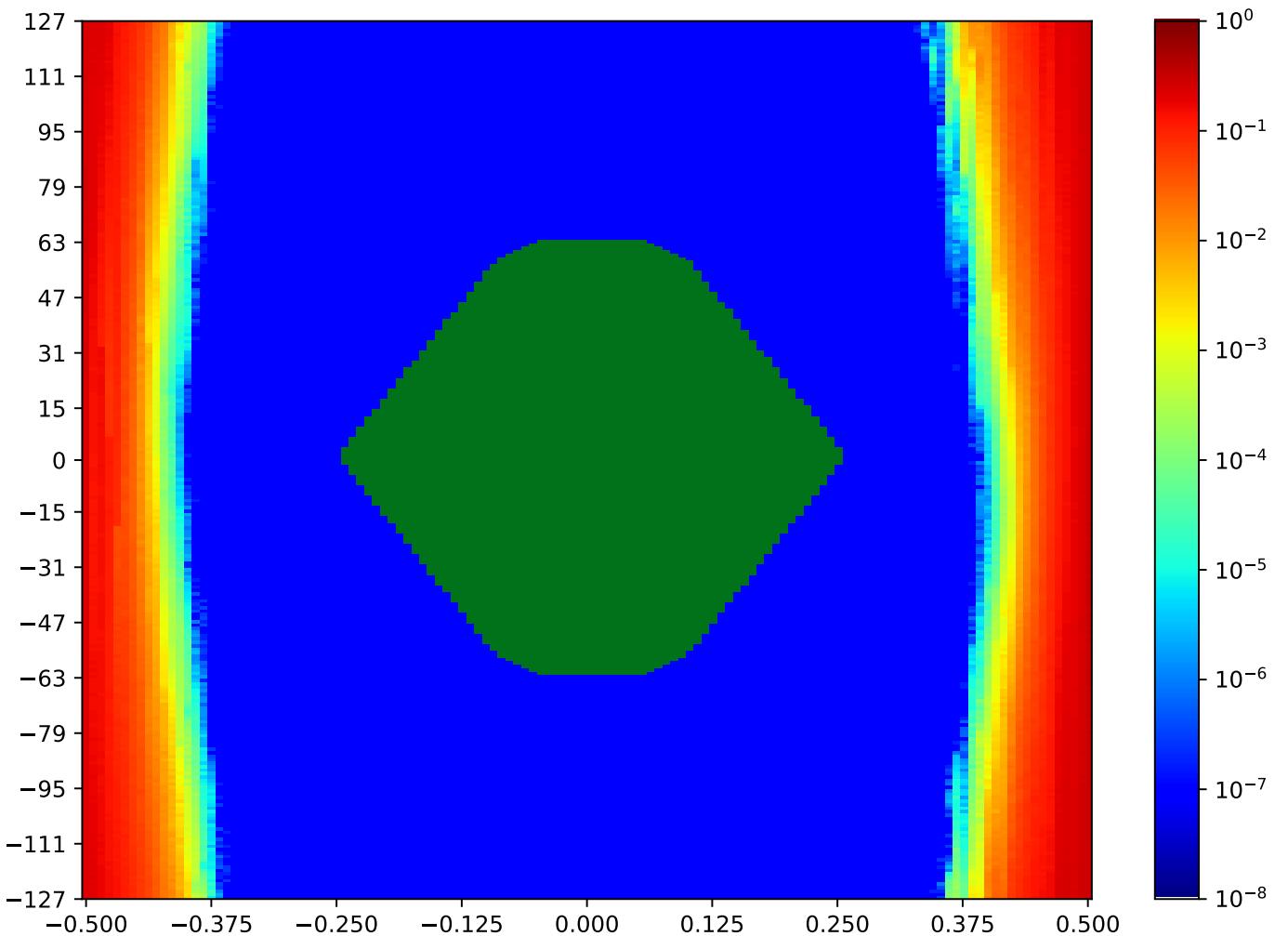


Figure 4.237: MSP_C_FPGA-TX4-09-RX2-09-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.11 MSP_C_FPGA-TX4-10-RX2-10-MSP_A_FPGA

Table 4.220: MSP_C_FPGA-TX4-10-RX2-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:44:37		2018-Sep-28 10:45:52	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24455	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

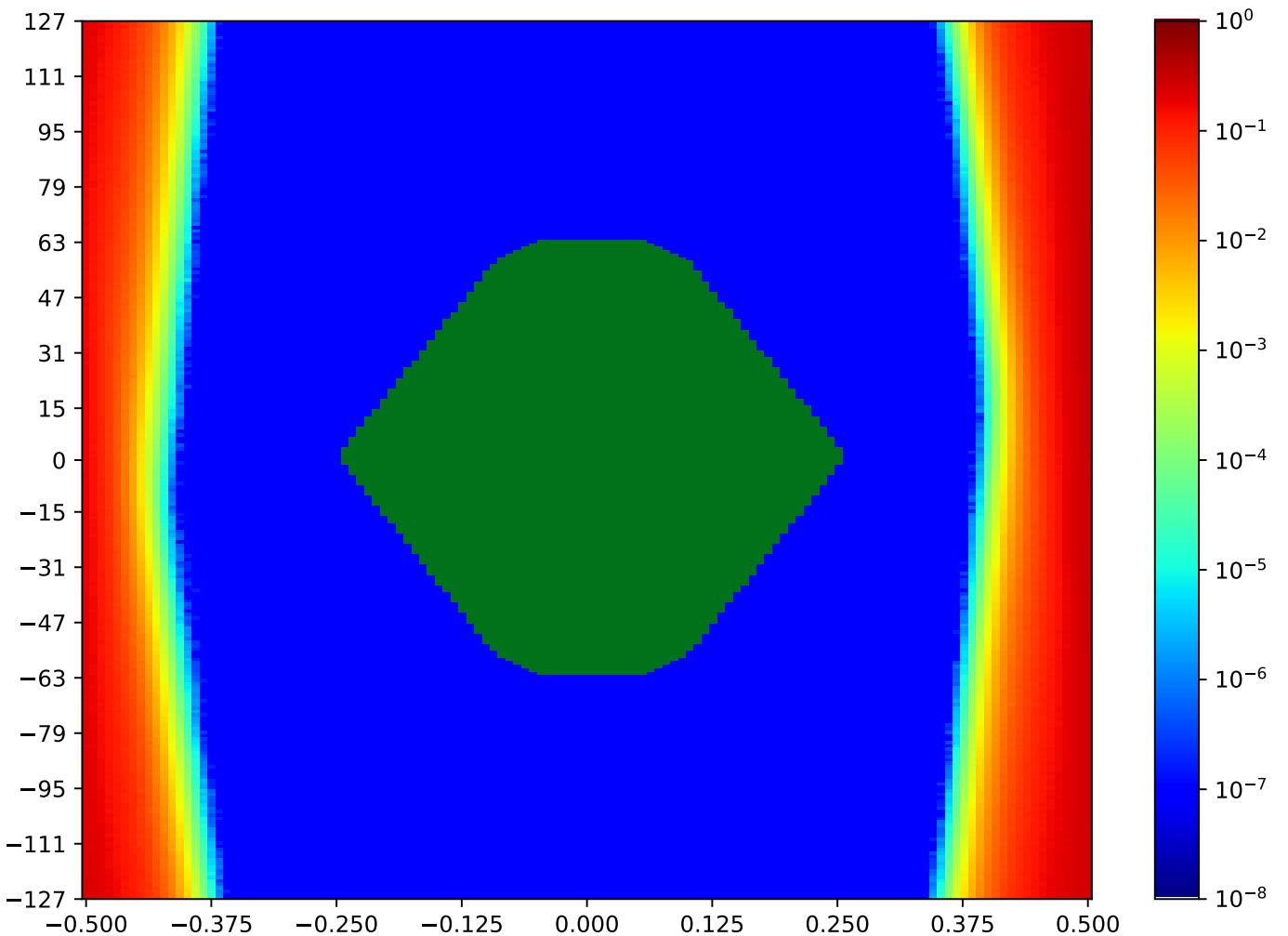


Figure 4.238: MSP_C_FPGA-TX4-10-RX2-10-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.18.12 MSP_C_FPGA-TX4-11-RX2-11-MSP_A_FPGA

Table 4.221: MSP_C_FPGA-TX4-11-RX2-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-28 10:43:22		2018-Sep-28 10:44:36	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24499	102		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

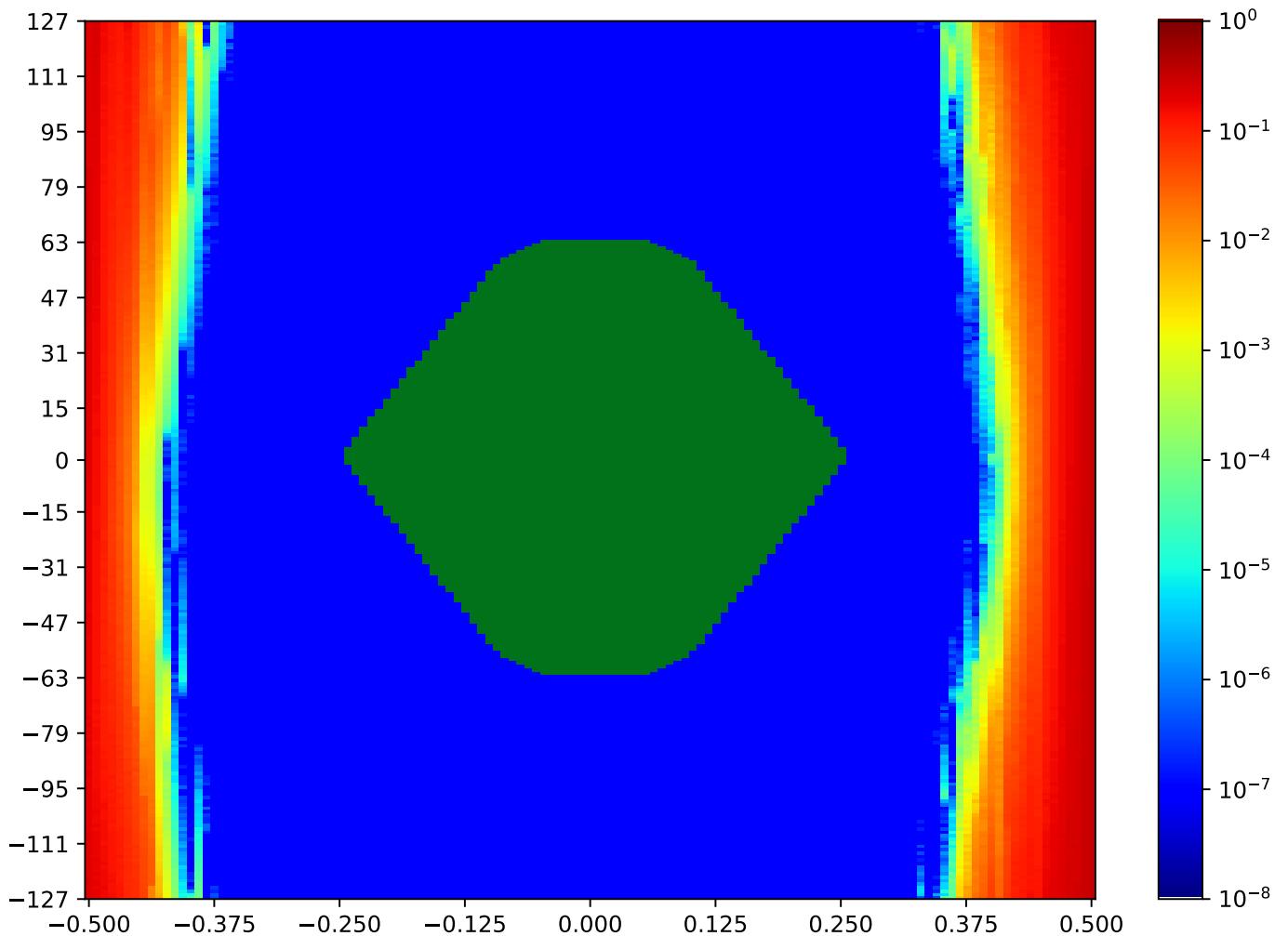


Figure 4.239: MSP_C_FPGA-TX4-11-RX2-11-MSP_A_FPGA

Call back to summary Figure 4.227. Sibling eye diagrams: V2-12.8.

4.19 MSP_A TX1 MSP_C RX12 Minipod Loopback

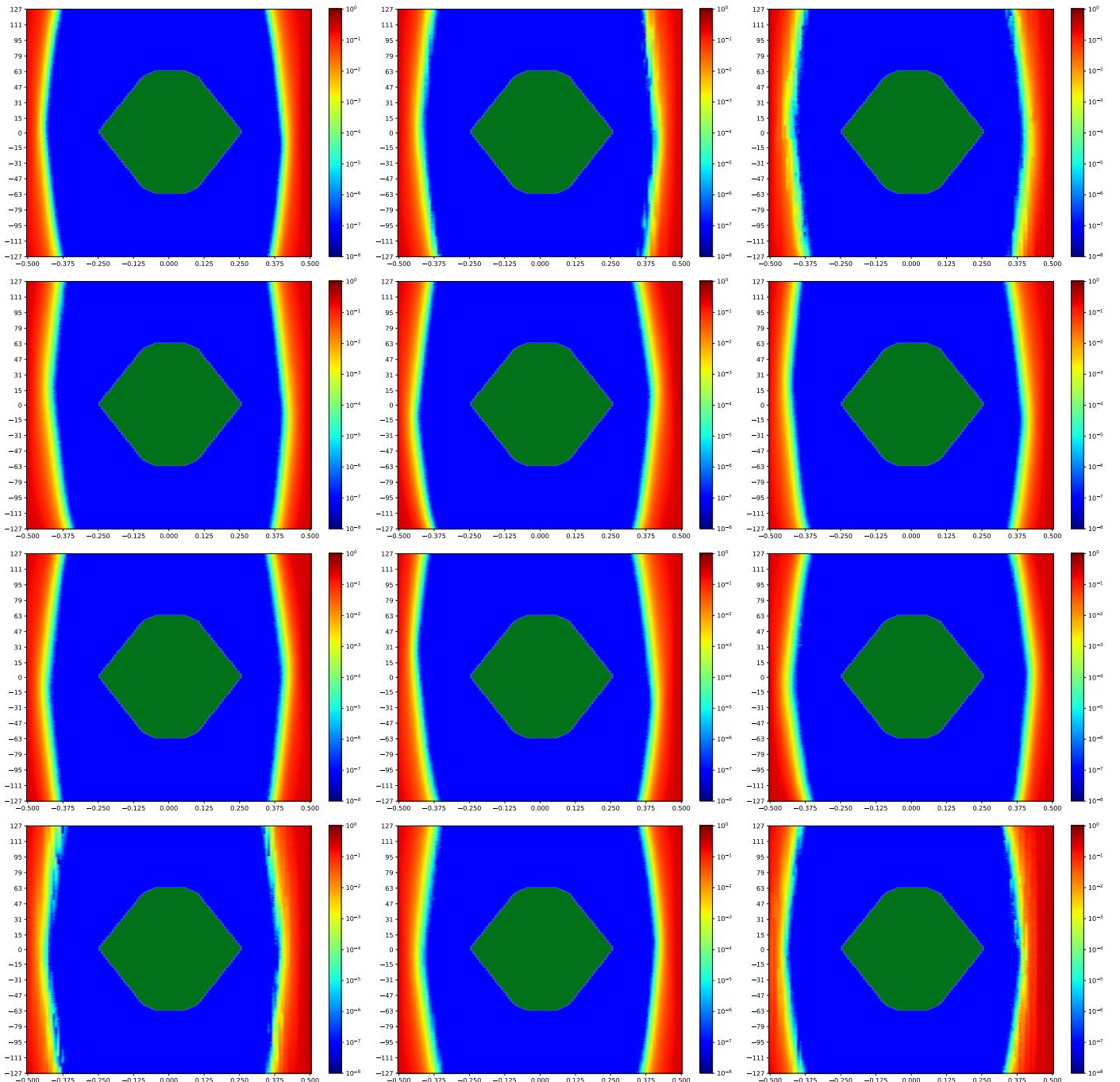


Figure 4.240: MSP_A TX1 MSP_C RX12 Minipod Loopback

A cross-reference to Figure 4.240. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.253.

4.19.1 MSP_A_FPGA-TX1-00-RX12-00-MSP_C_FPGA

Table 4.222: MSP_A_FPGA-TX1-00-RX12-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:13:00		2018-Sep-27 18:14:14	
Reset RX	OA	HO		VO	VO (%)
true	25145	104		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

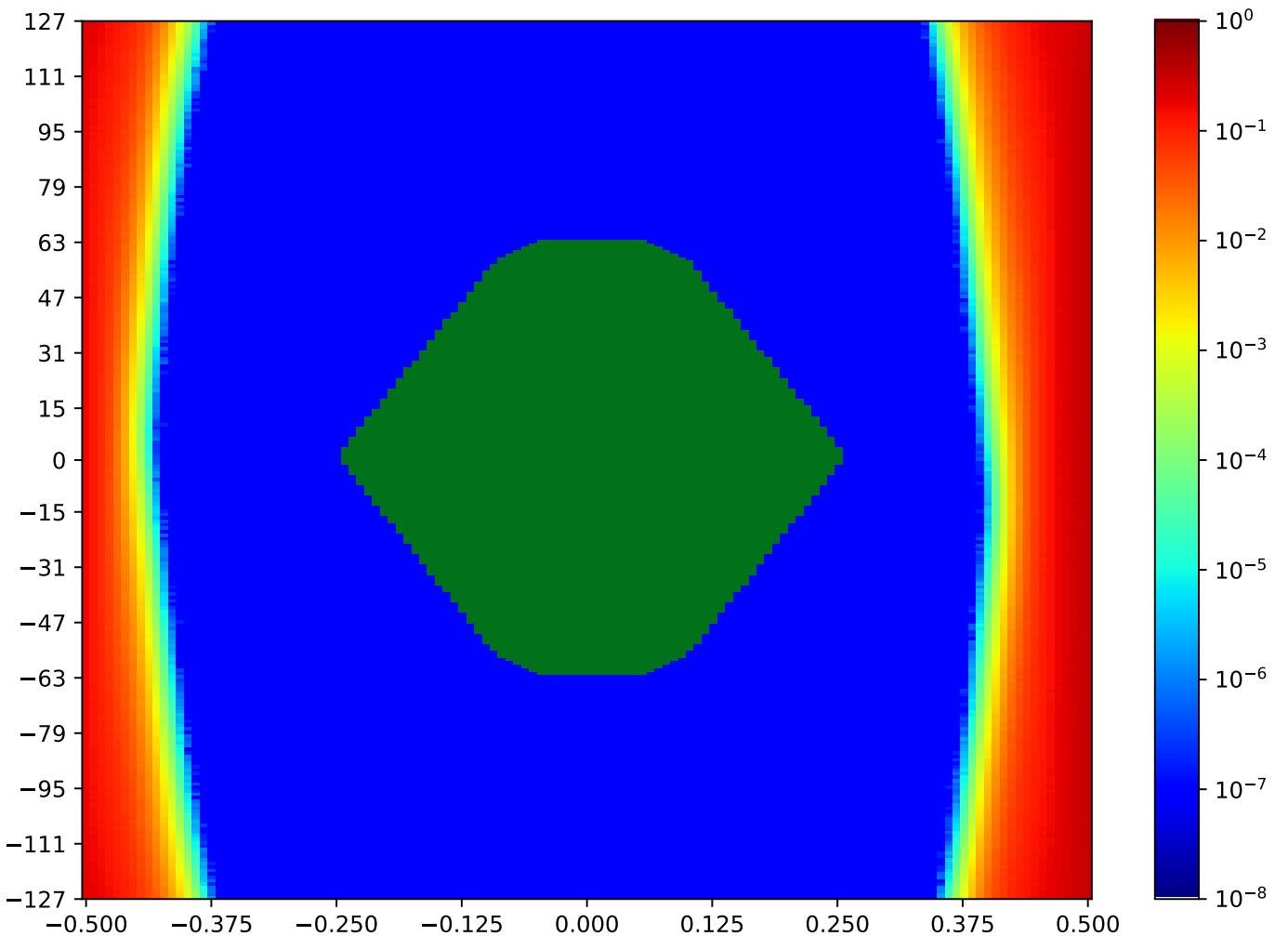


Figure 4.241: MSP_A_FPGA-TX1-00-RX12-00-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.2 MSP_A_FPGA-TX1-01-RX12-01-MSP_C_FPGA

Table 4.223: MSP_A_FPGA-TX1-01-RX12-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:15:28		2018-Sep-27 18:16:42	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24604	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

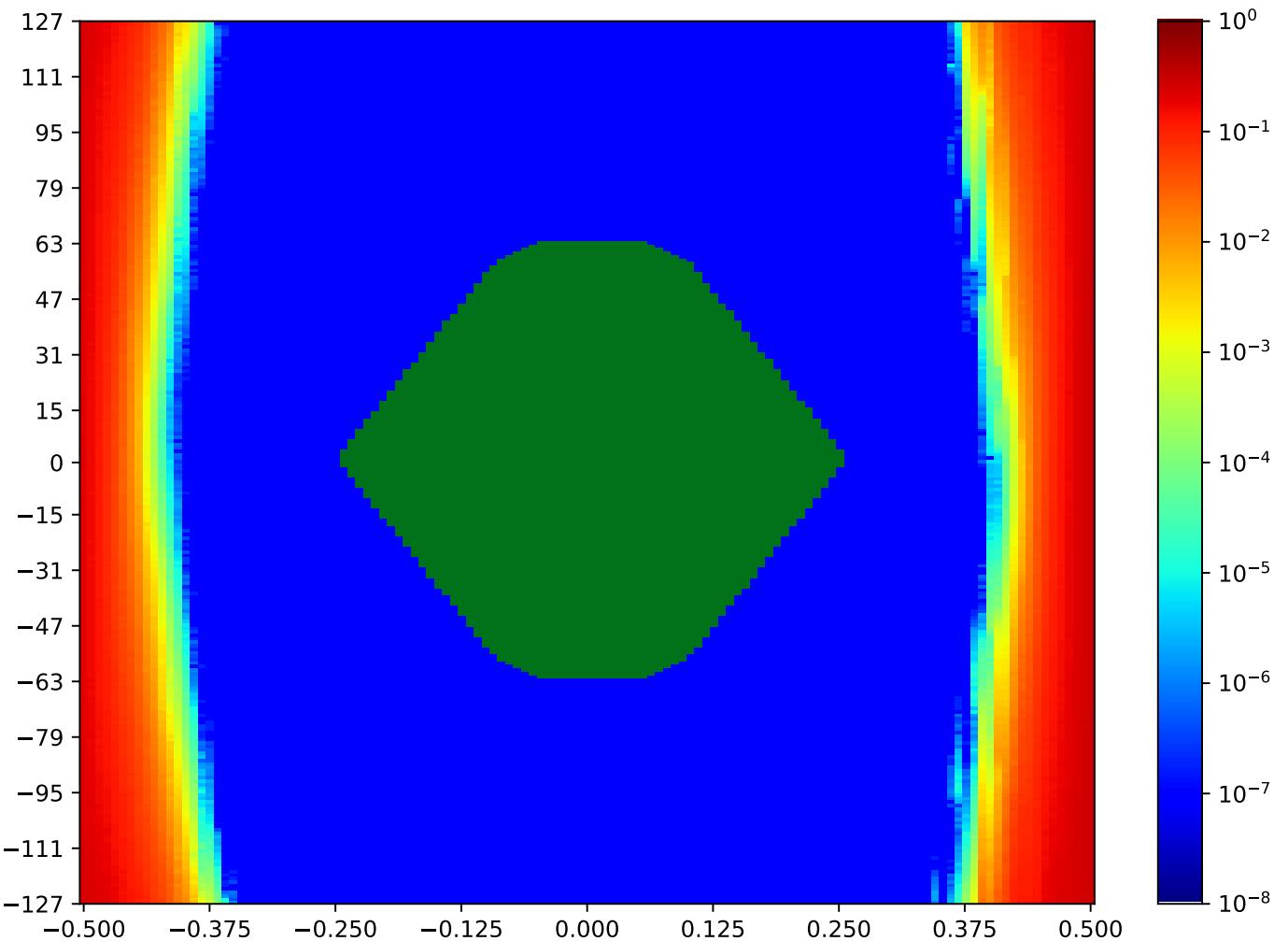


Figure 4.242: MSP_A_FPGA-TX1-01-RX12-01-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.3 MSP_A_FPGA-TX1-02-RX12-02-MSP_C_FPGA

Table 4.224: MSP_A_FPGA-TX1-02-RX12-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:16:42		2018-Sep-27 18:17:57	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24237	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

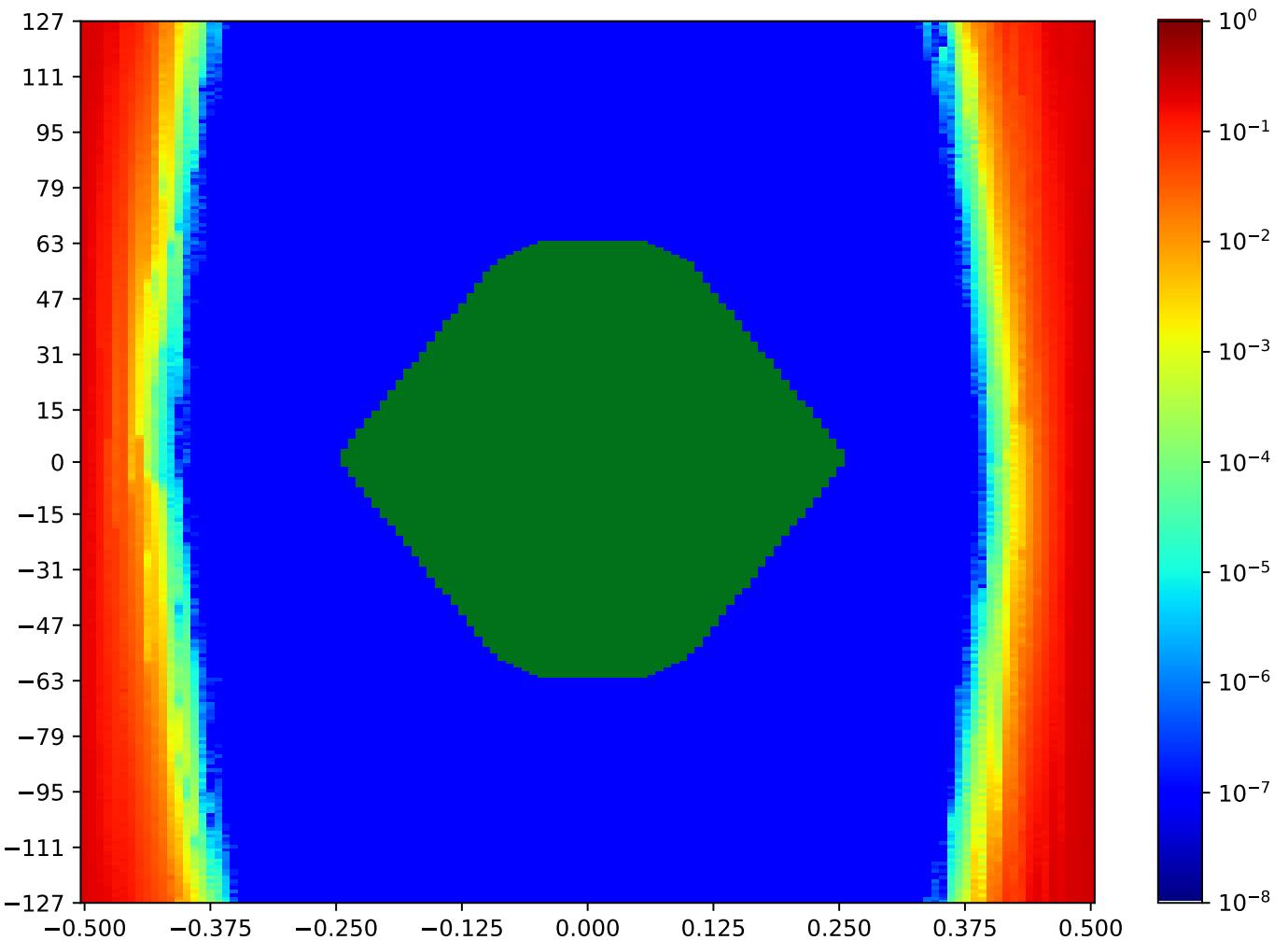


Figure 4.243: MSP_A_FPGA-TX1-02-RX12-02-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.4 MSP_A_FPGA-TX1-03-RX12-03-MSP_C_FPGA

Table 4.225: MSP_A_FPGA-TX1-03-RX12-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:10:30		2018-Sep-27 18:11:45	
Reset RX	OA	HO		VO	VO (%)
true	24299	100		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

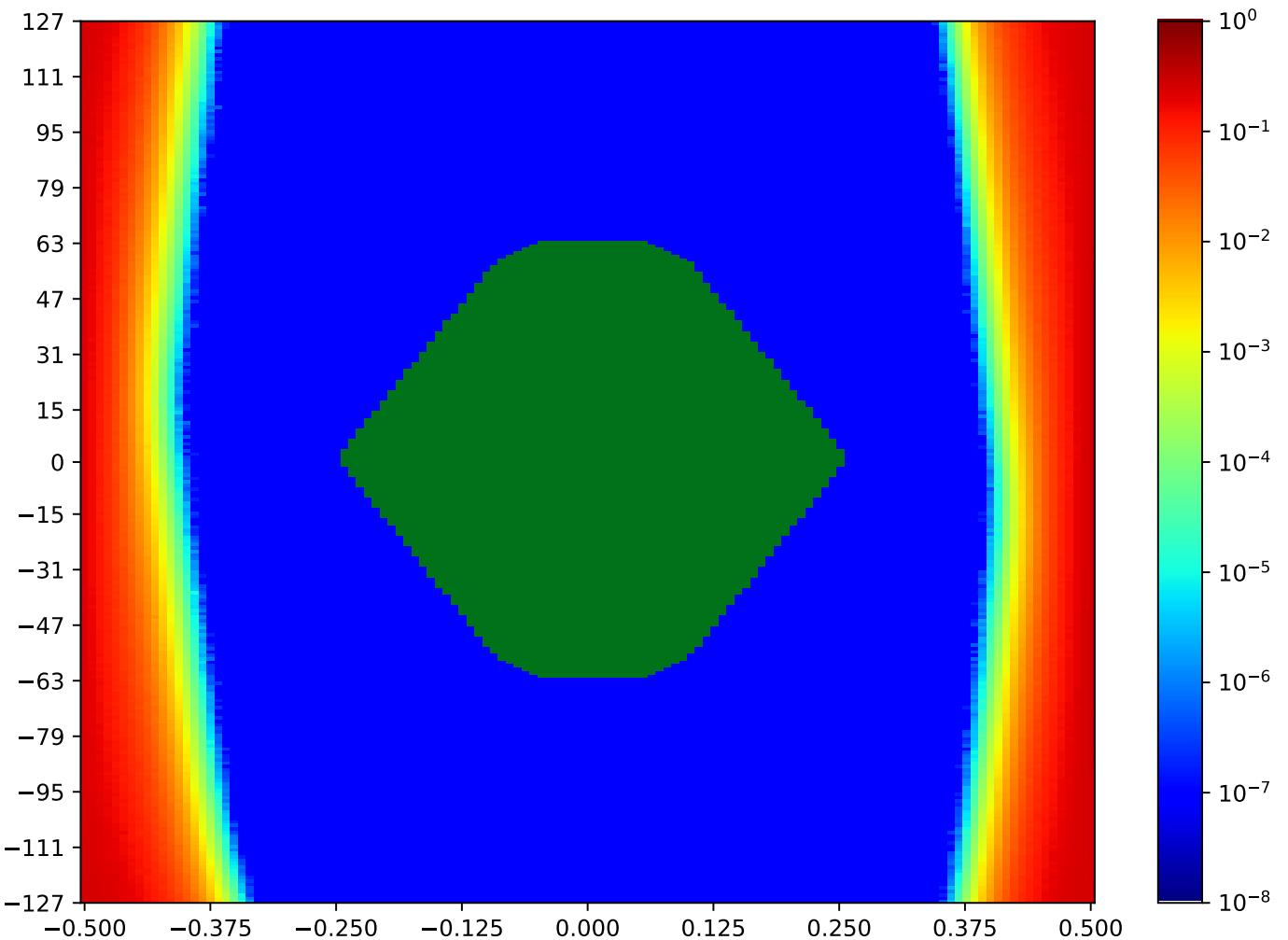


Figure 4.244: MSP_A_FPGA-TX1-03-RX12-03-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.5 MSP_A_FPGA-TX1-04-RX12-04-MSP_C_FPGA

Table 4.226: MSP_A_FPGA-TX1-04-RX12-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:20:26		2018-Sep-27 18:21:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24397	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

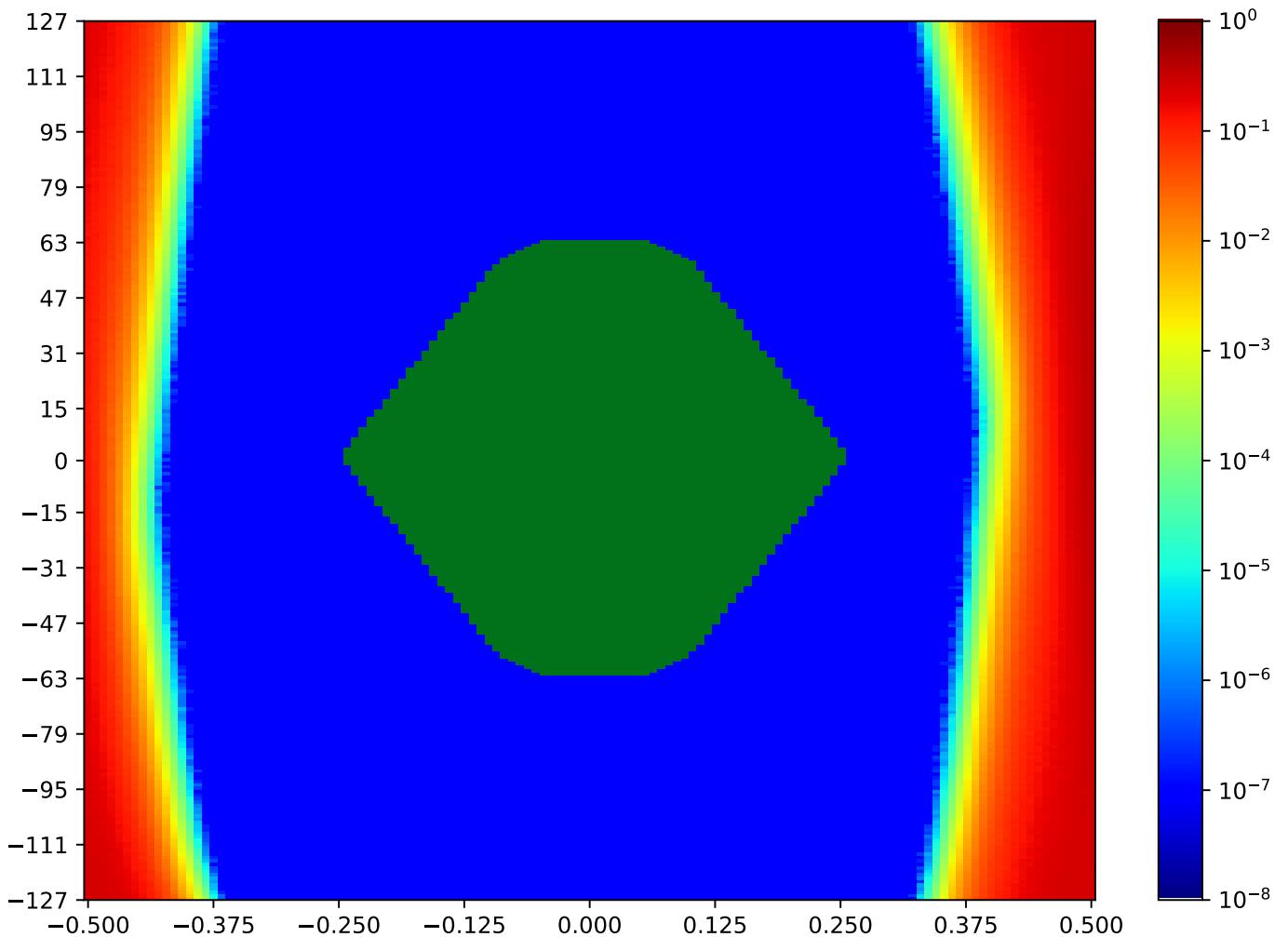


Figure 4.245: MSP_A_FPGA-TX1-04-RX12-04-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.6 MSP_A_FPGA-TX1-05-RX12-05-MSP_C_FPGA

Table 4.227: MSP_A_FPGA-TX1-05-RX12-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:09:16		2018-Sep-27 18:10:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24449	100	77.52%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

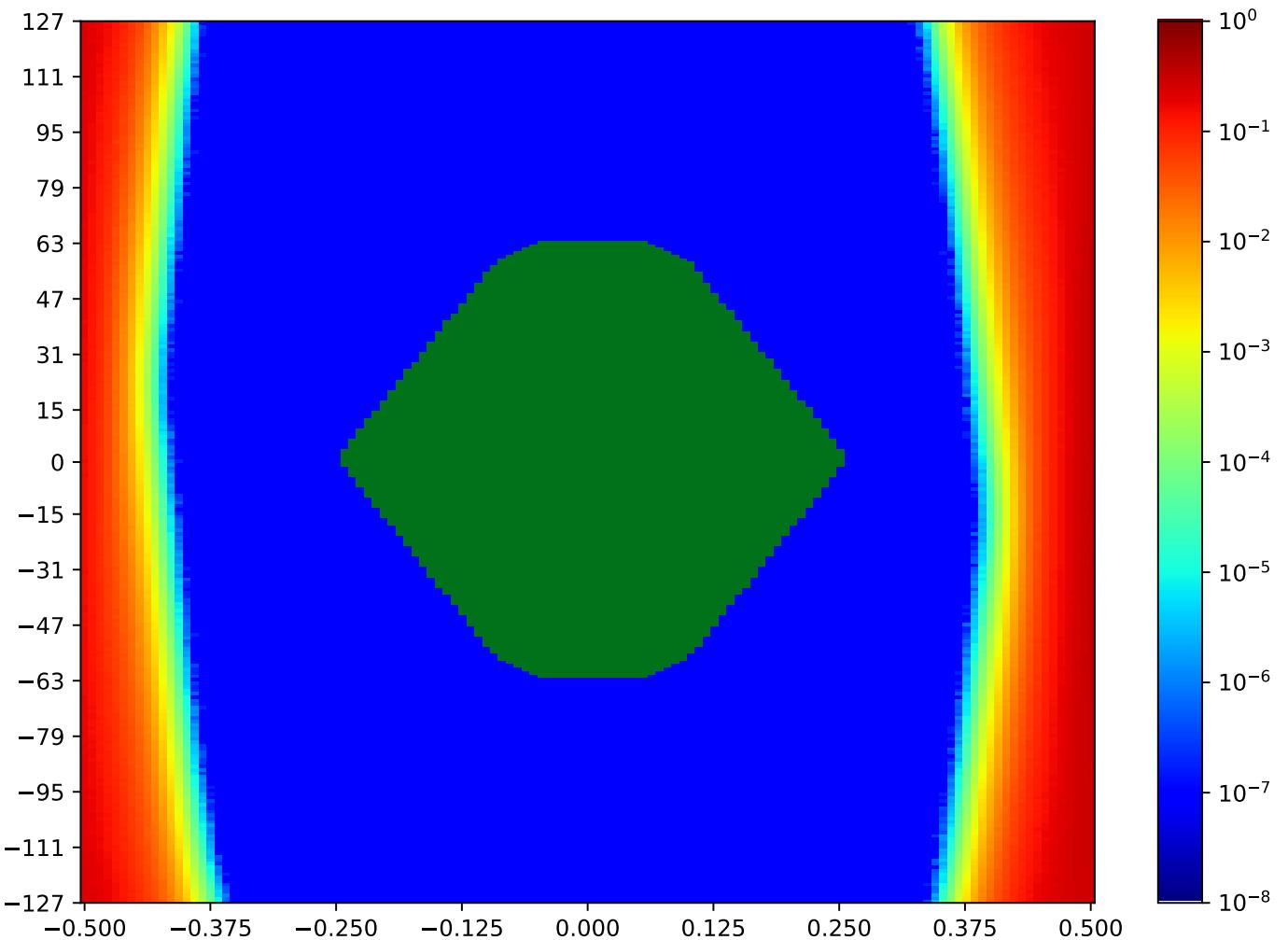


Figure 4.246: MSP_A_FPGA-TX1-05-RX12-05-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.7 MSP_A_FPGA-TX1-06-RX12-06-MSP_C_FPGA

Table 4.228: MSP_A_FPGA-TX1-06-RX12-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:22:54		2018-Sep-27 18:24:09	
Reset RX	OA	HO		VO	VO (%)
true	24598	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

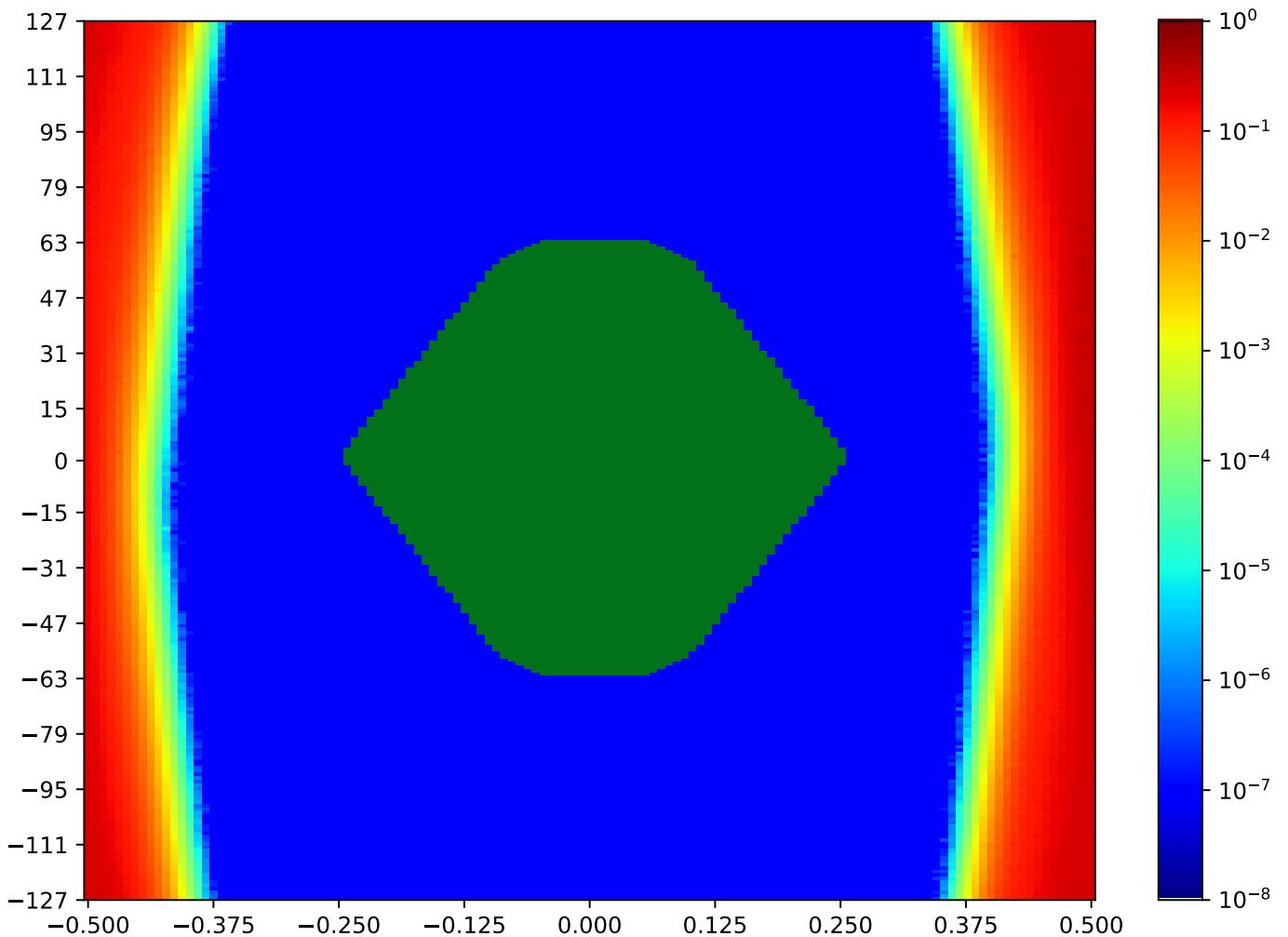


Figure 4.247: MSP_A_FPGA-TX1-06-RX12-06-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.8 MSP_A_FPGA-TX1-07-RX12-07-MSP_C_FPGA

Table 4.229: MSP_A_FPGA-TX1-07-RX12-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:11:45		2018-Sep-27 18:13:00	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24659	100	77.52%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

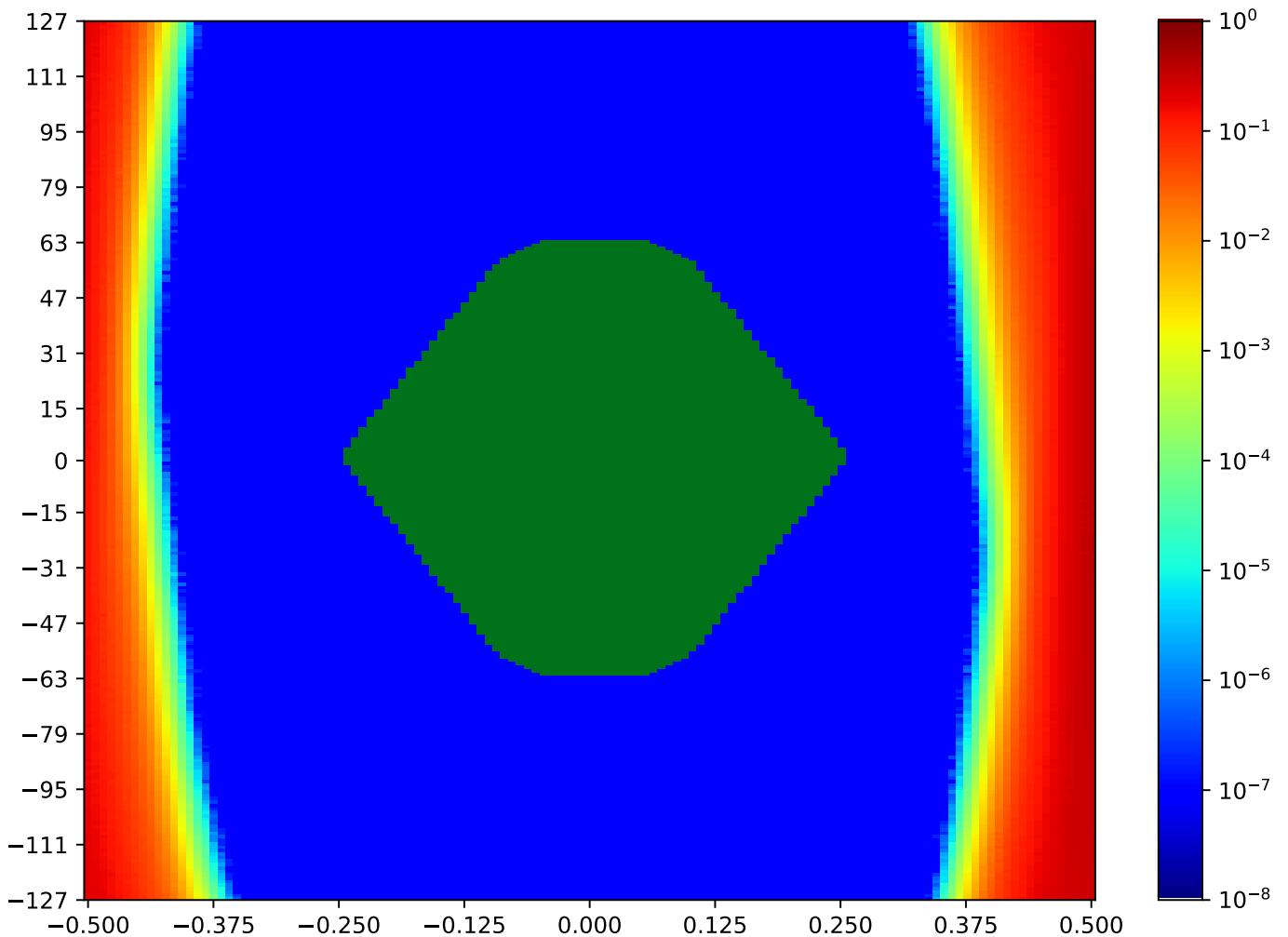


Figure 4.248: MSP_A_FPGA-TX1-07-RX12-07-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.9 MSP_A_FPGA-TX1-08-RX12-08-MSP_C_FPGA

Table 4.230: MSP_A_FPGA-TX1-08-RX12-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:21:40		2018-Sep-27 18:22:54	
Reset RX	OA	HO		VO	VO (%)
true	24531	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

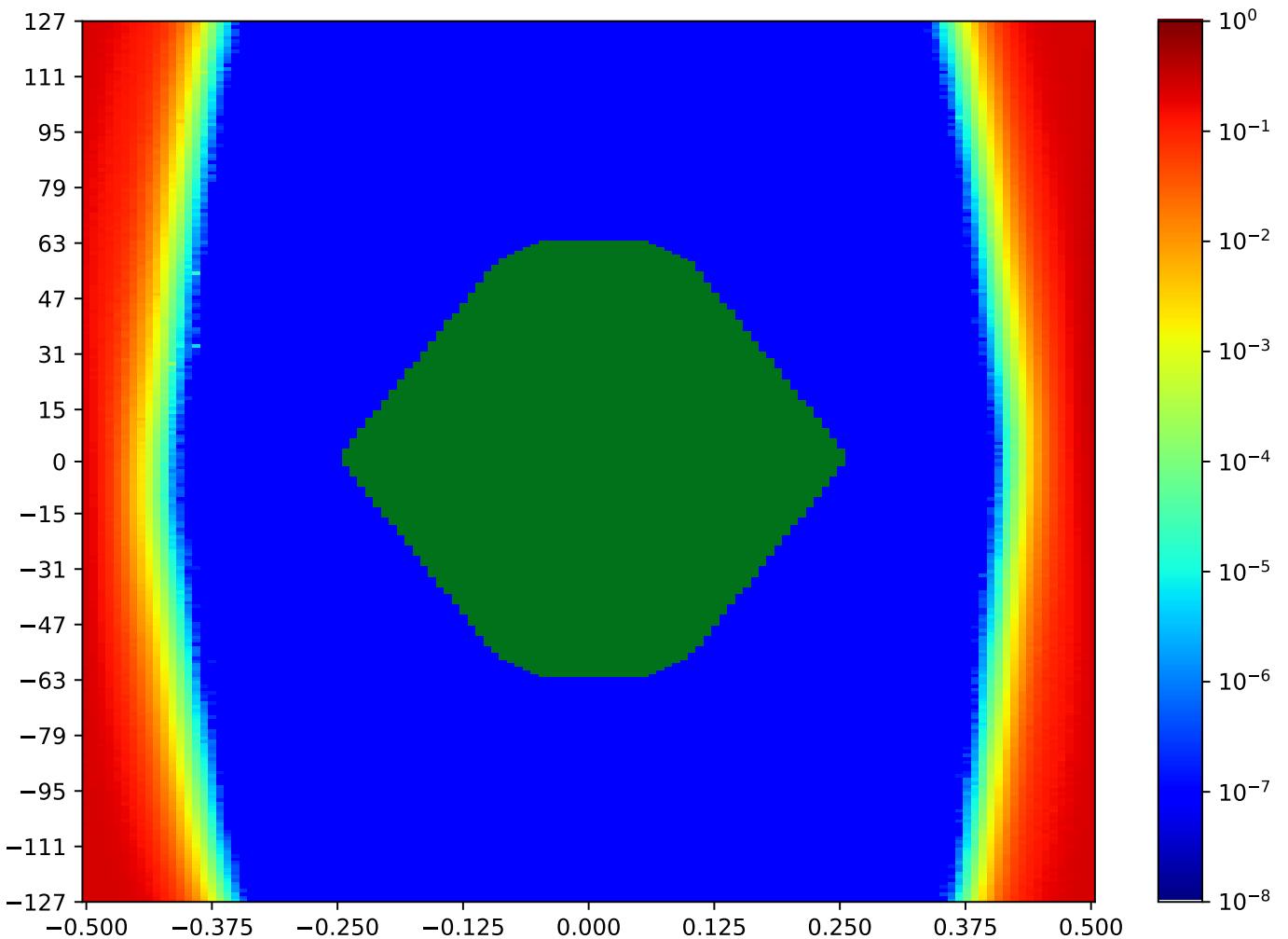


Figure 4.249: MSP_A_FPGA-TX1-08-RX12-08-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.10 MSP_A_FPGA-TX1-09-RX12-09-MSP_C_FPGA

Table 4.231: MSP_A_FPGA-TX1-09-RX12-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:14:14		2018-Sep-27 18:15:28	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24327	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

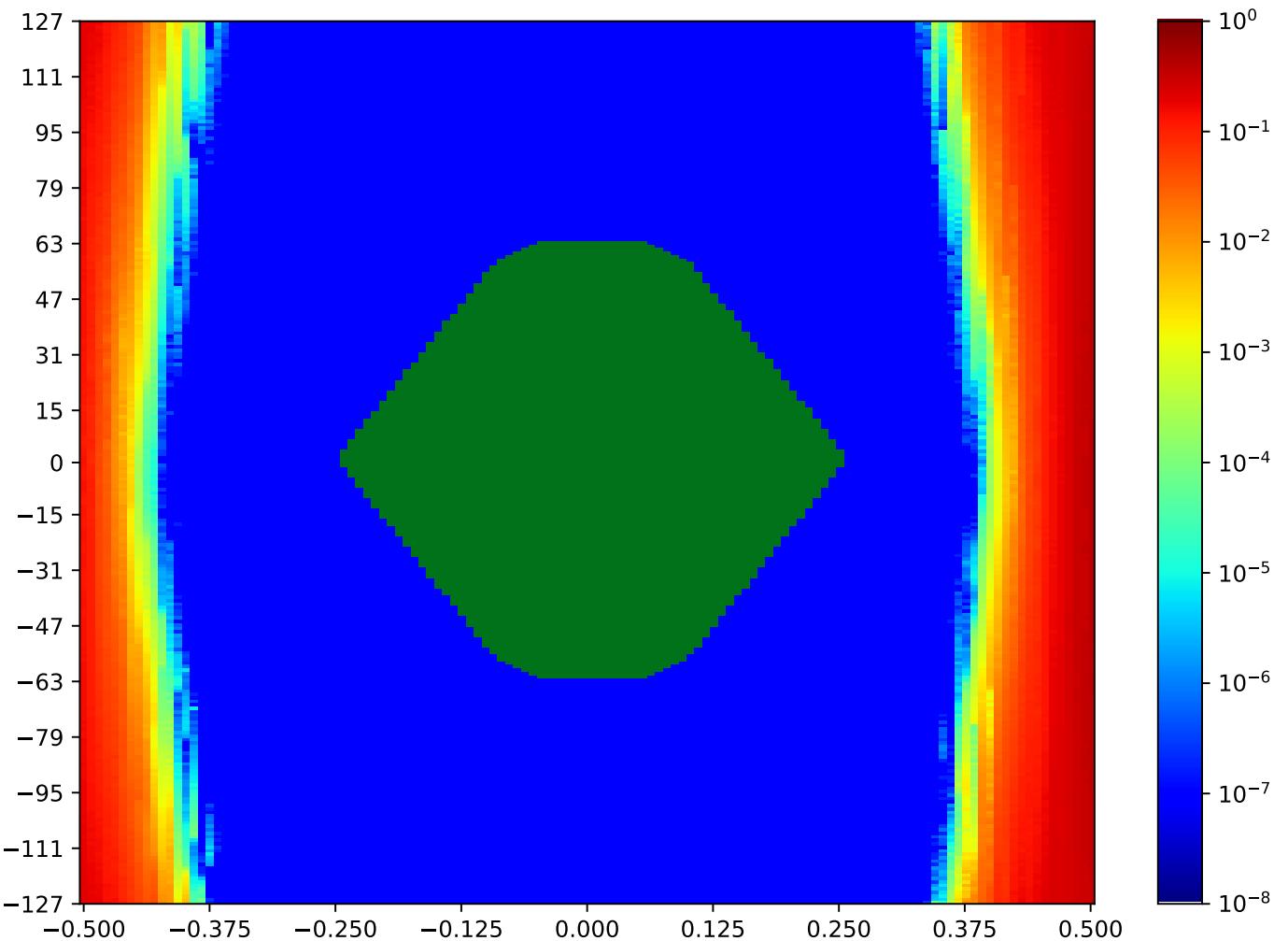


Figure 4.250: MSP_A_FPGA-TX1-09-RX12-09-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.11 MSP_A_FPGA-TX1-10-RX12-10-MSP_C_FPGA

Table 4.232: MSP_A_FPGA-TX1-10-RX12-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:19:12		2018-Sep-27 18:20:26	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24307	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

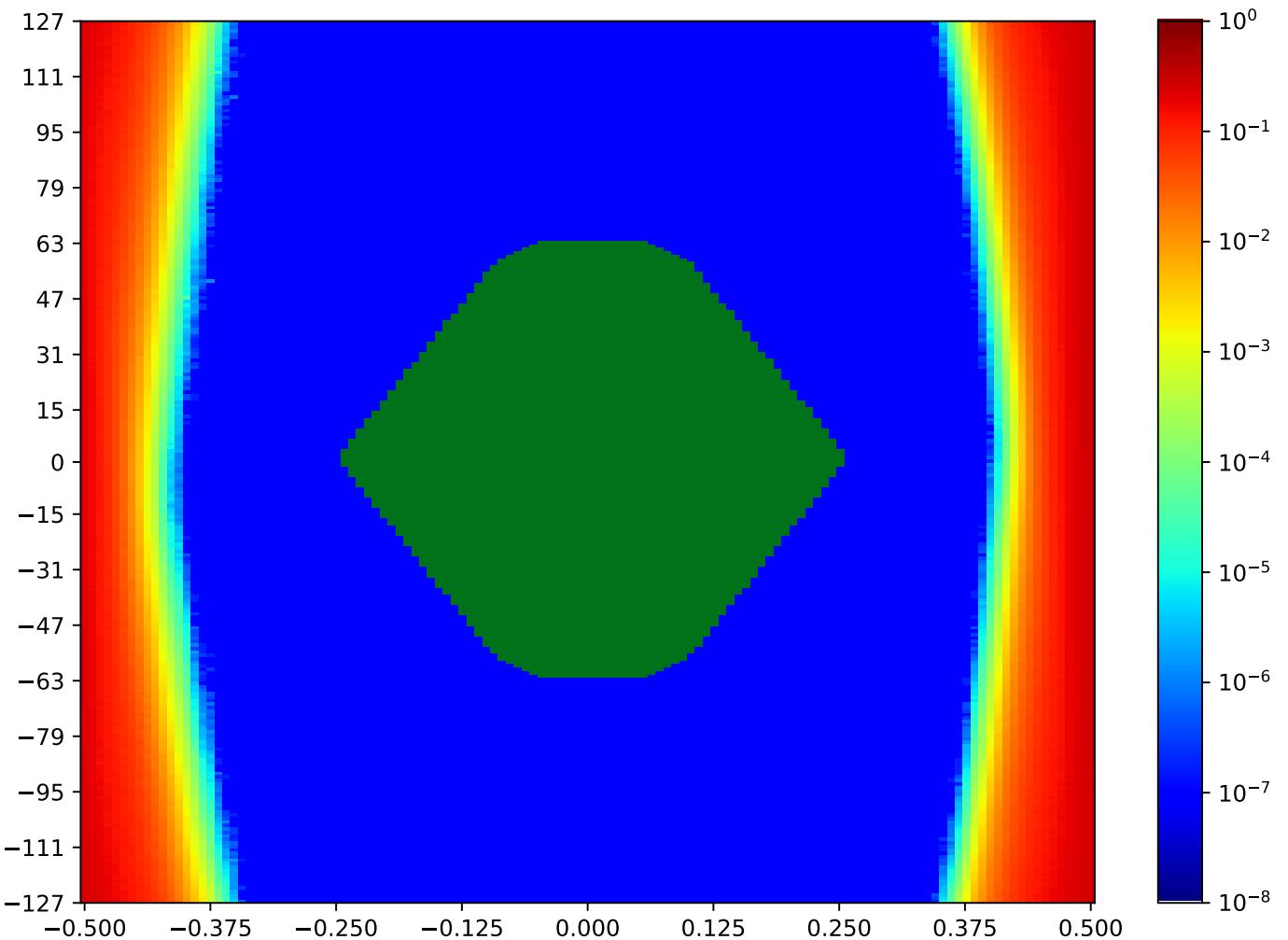


Figure 4.251: MSP_A_FPGA-TX1-10-RX12-10-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.19.12 MSP_A_FPGA-TX1-11-RX12-11-MSP_C_FPGA

Table 4.233: MSP_A_FPGA-TX1-11-RX12-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:17:57		2018-Sep-27 18:19:12	
Reset RX	OA	HO		VO	VO (%)
true	24559	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

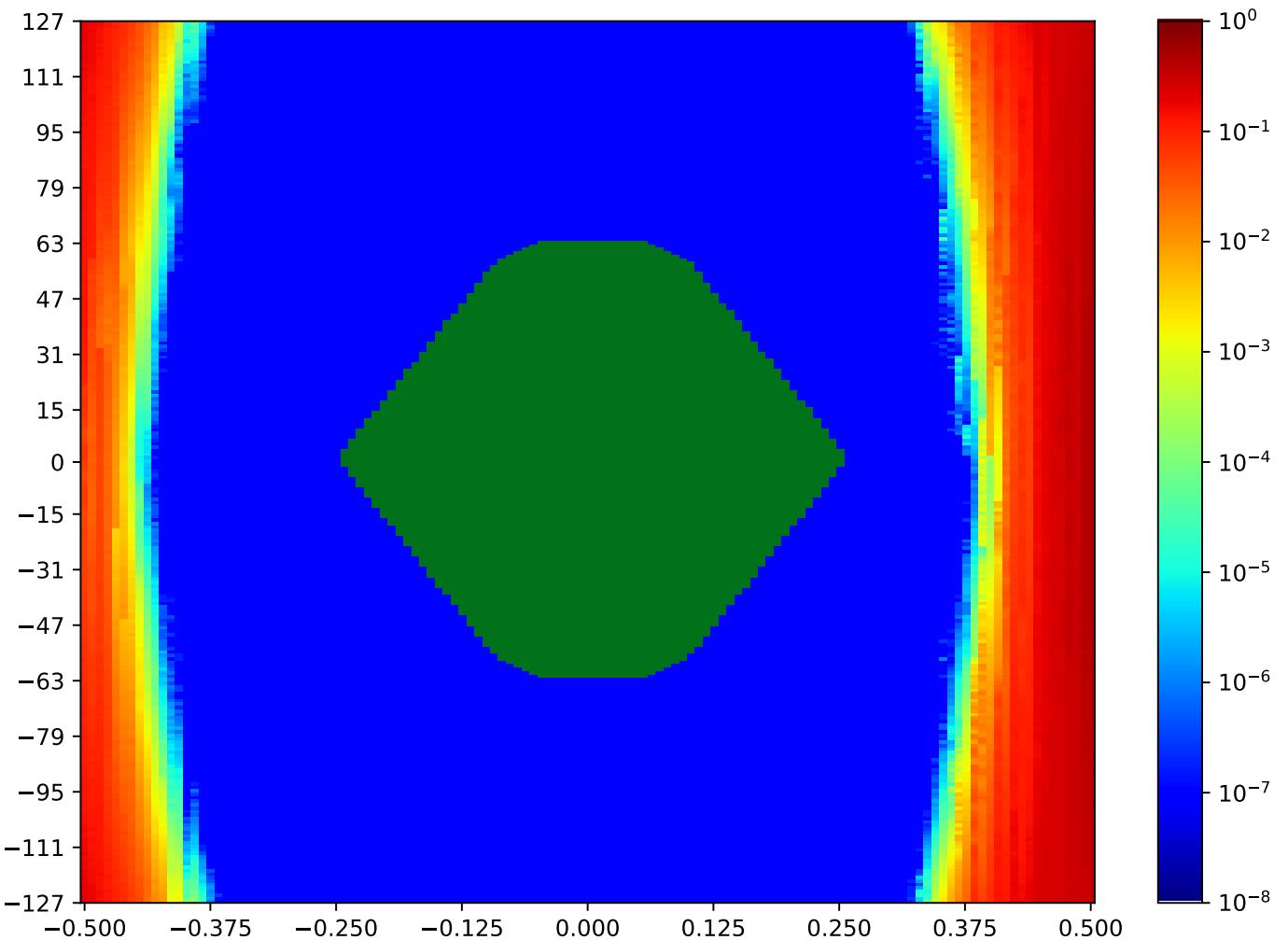


Figure 4.252: MSP_A_FPGA-TX1-11-RX12-11-MSP_C_FPGA

Call back to summary Figure 4.240. Sibling eye diagrams: V2-12.8.

4.20 MSP_A TX2 MSP_C RX13 Minipod Loopback

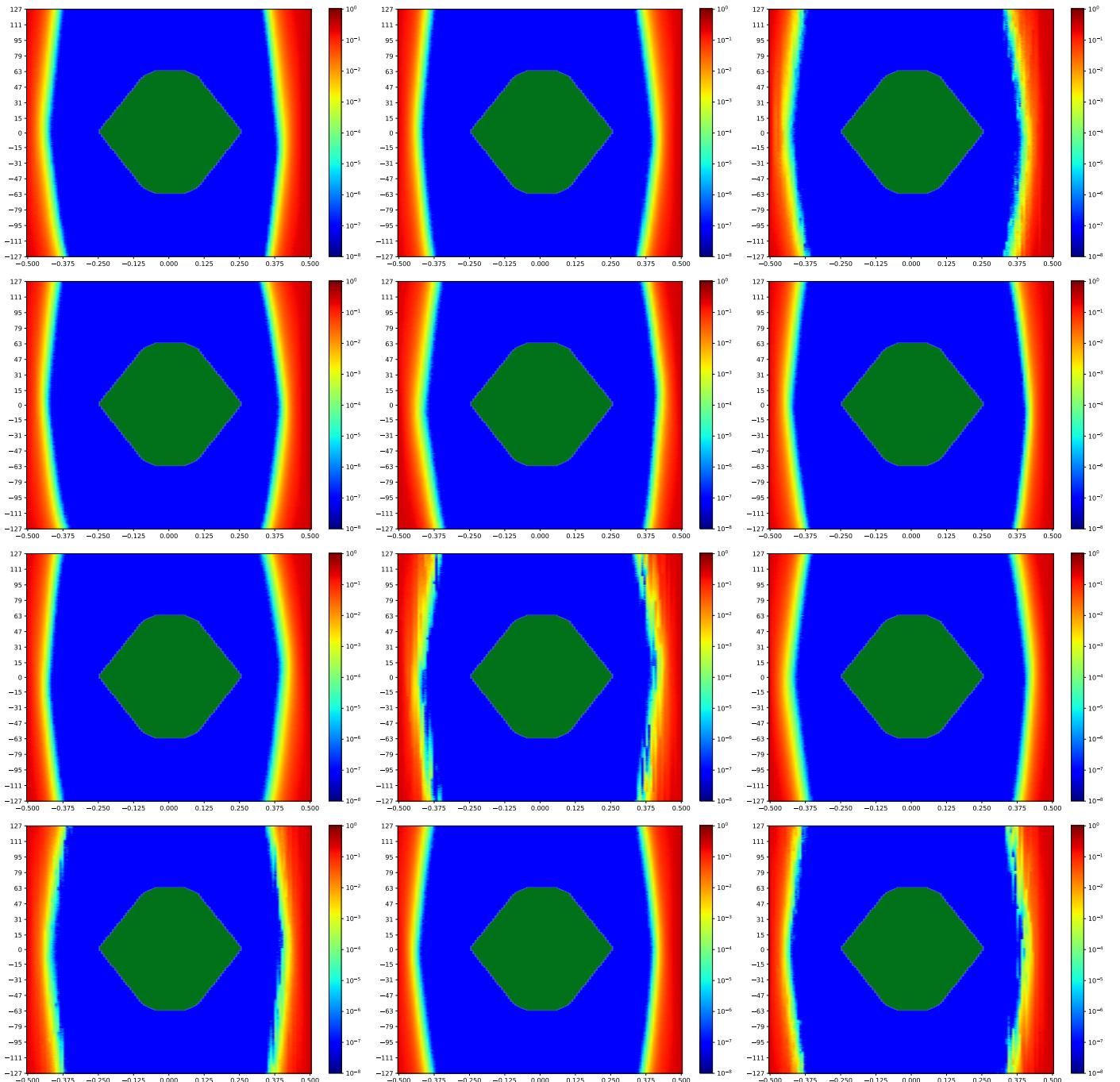


Figure 4.253: MSP_A TX2 MSP_C RX13 Minipod Loopback

A cross-reference to Figure 4.253. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.266.

4.20.1 MSP_A_FPGA-TX2-00-RX13-00-MSP_C_FPGA

Table 4.234: MSP_A_FPGA-TX2-00-RX13-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:27:52		2018-Sep-27 18:29:06	
Reset RX	OA	HO		VO	VO (%)
true	24229	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

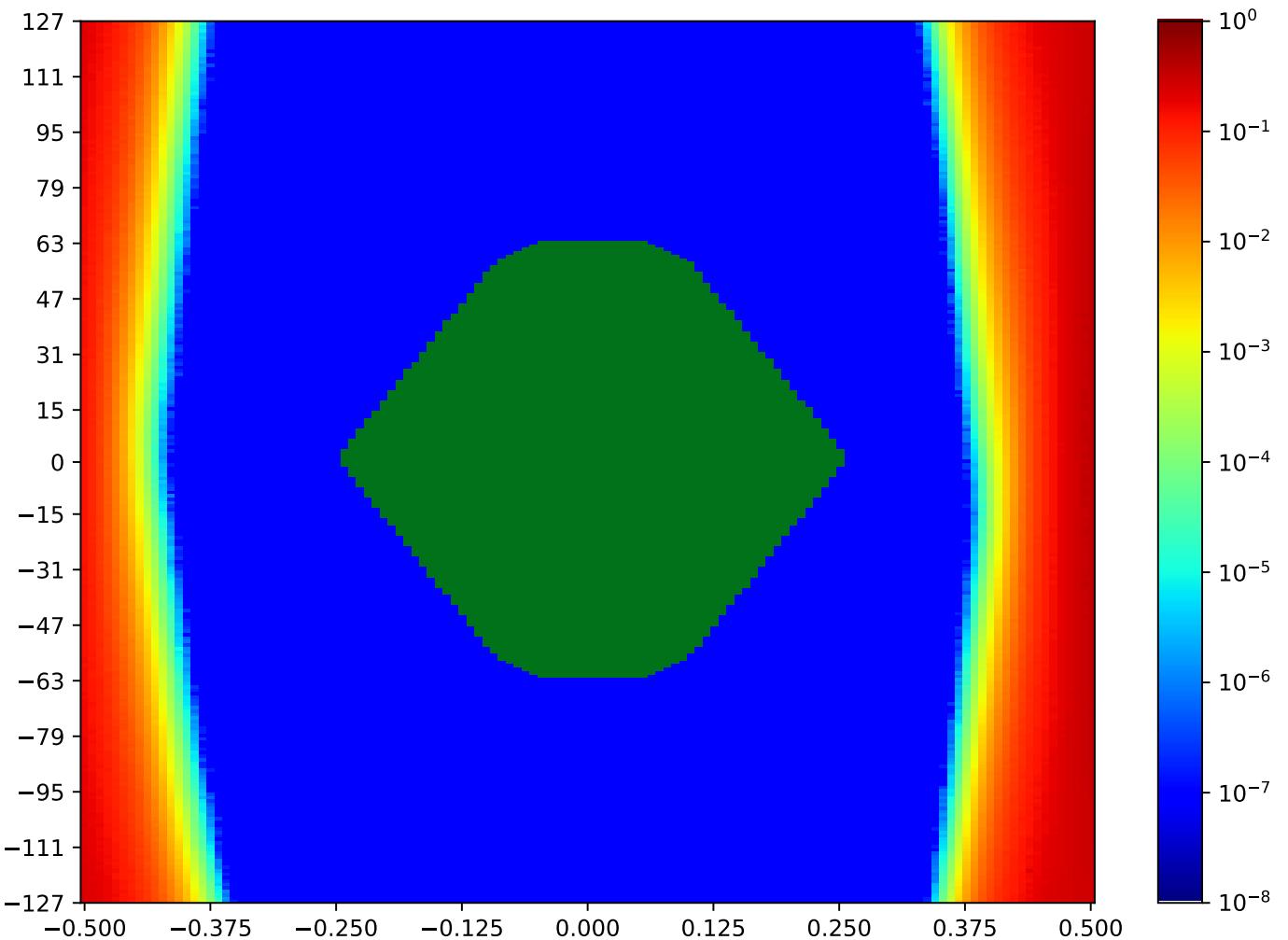


Figure 4.254: MSP_A_FPGA-TX2-00-RX13-00-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.2 MSP_A_FPGA-TX2-01-RX13-01-MSP_C_FPGA

Table 4.235: MSP_A_FPGA-TX2-01-RX13-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:25:23		2018-Sep-27 18:26:37	
Reset RX	OA	HO		VO	VO (%)
true	24499	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

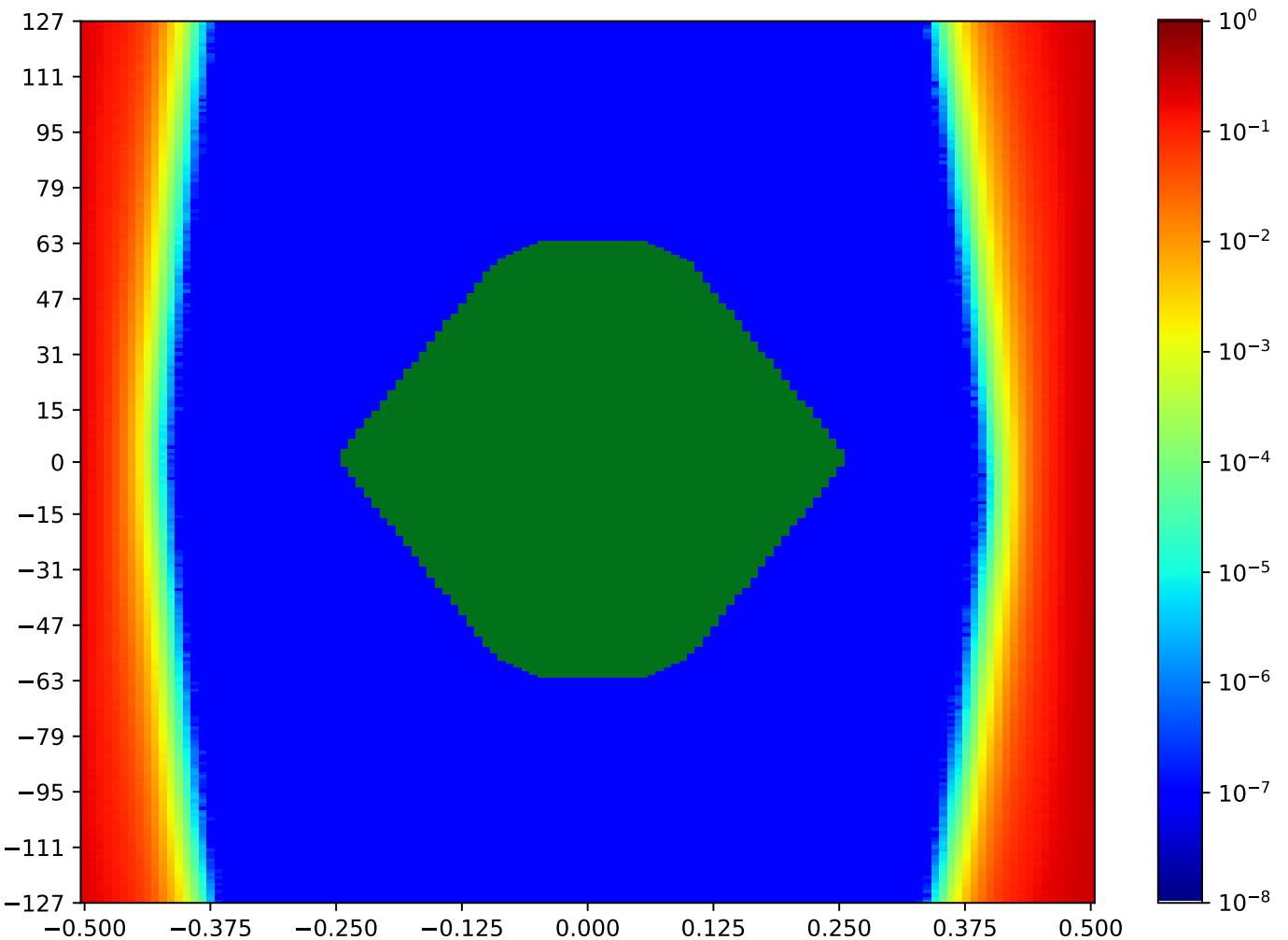


Figure 4.255: MSP_A_FPGA-TX2-01-RX13-01-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.3 MSP_A_FPGA-TX2-02-RX13-02-MSP_C_FPGA

Table 4.236: MSP_A_FPGA-TX2-02-RX13-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:31:36		2018-Sep-27 18:32:51	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24079	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

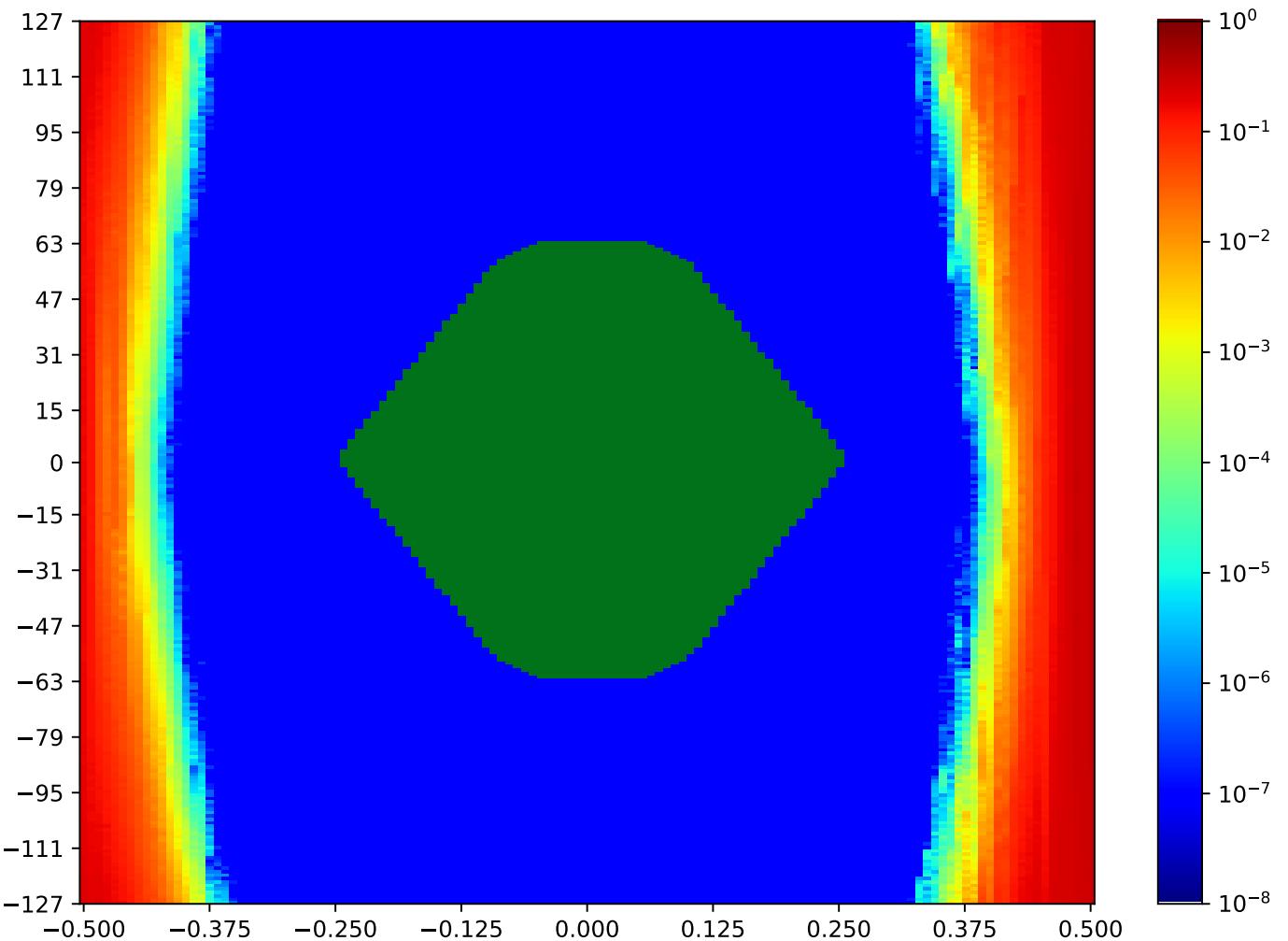


Figure 4.256: MSP_A_FPGA-TX2-02-RX13-02-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.4 MSP_A_FPGA-TX2-03-RX13-03-MSP_C_FPGA

Table 4.237: MSP_A_FPGA-TX2-03-RX13-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:24:09		2018-Sep-27 18:25:23	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24318	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

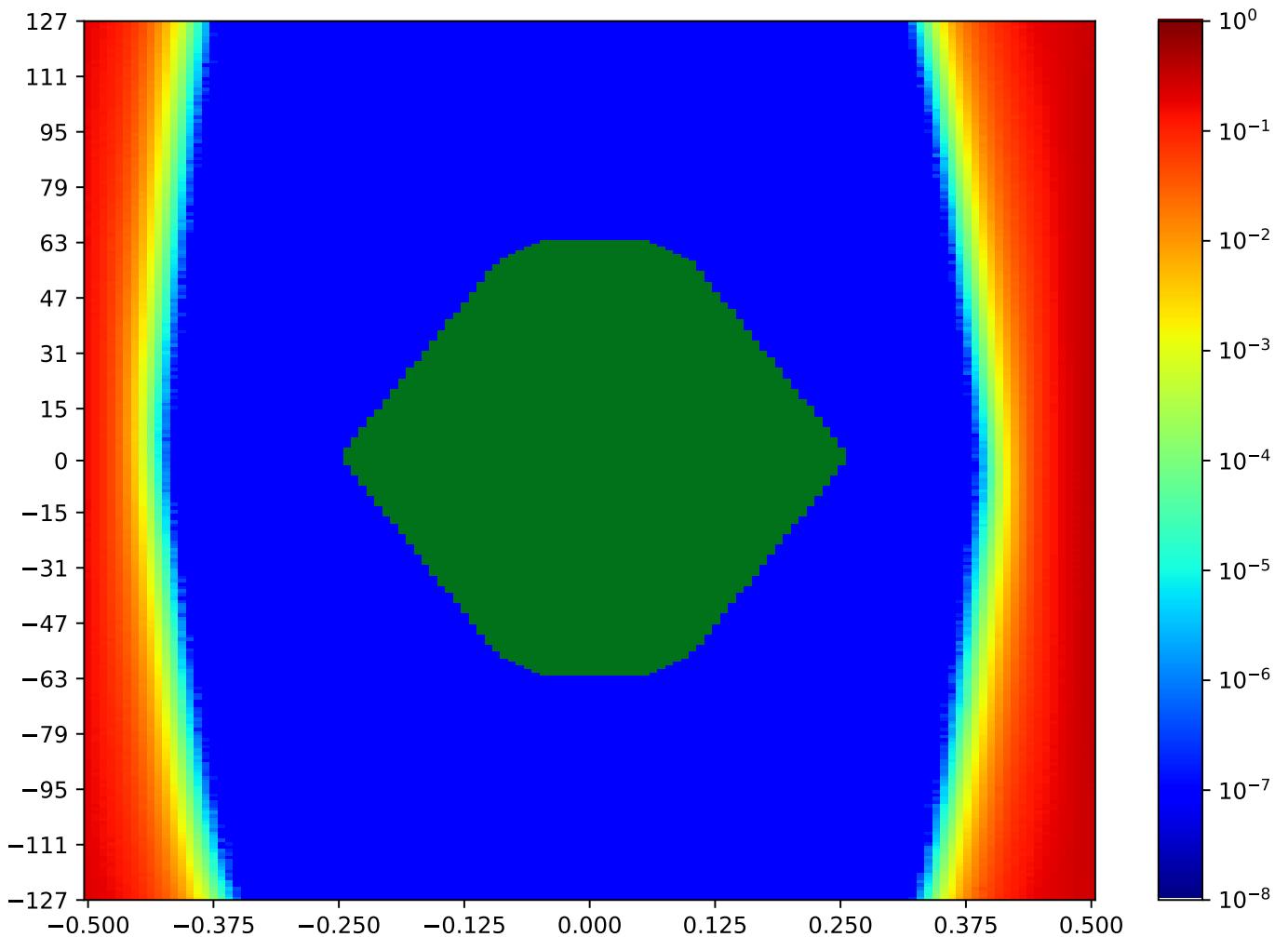


Figure 4.257: MSP_A_FPGA-TX2-03-RX13-03-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.5 MSP_A_FPGA-TX2-04-RX13-04-MSP_C_FPGA

Table 4.238: MSP_A_FPGA-TX2-04-RX13-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:35:22		2018-Sep-27 18:36:38	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24343	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

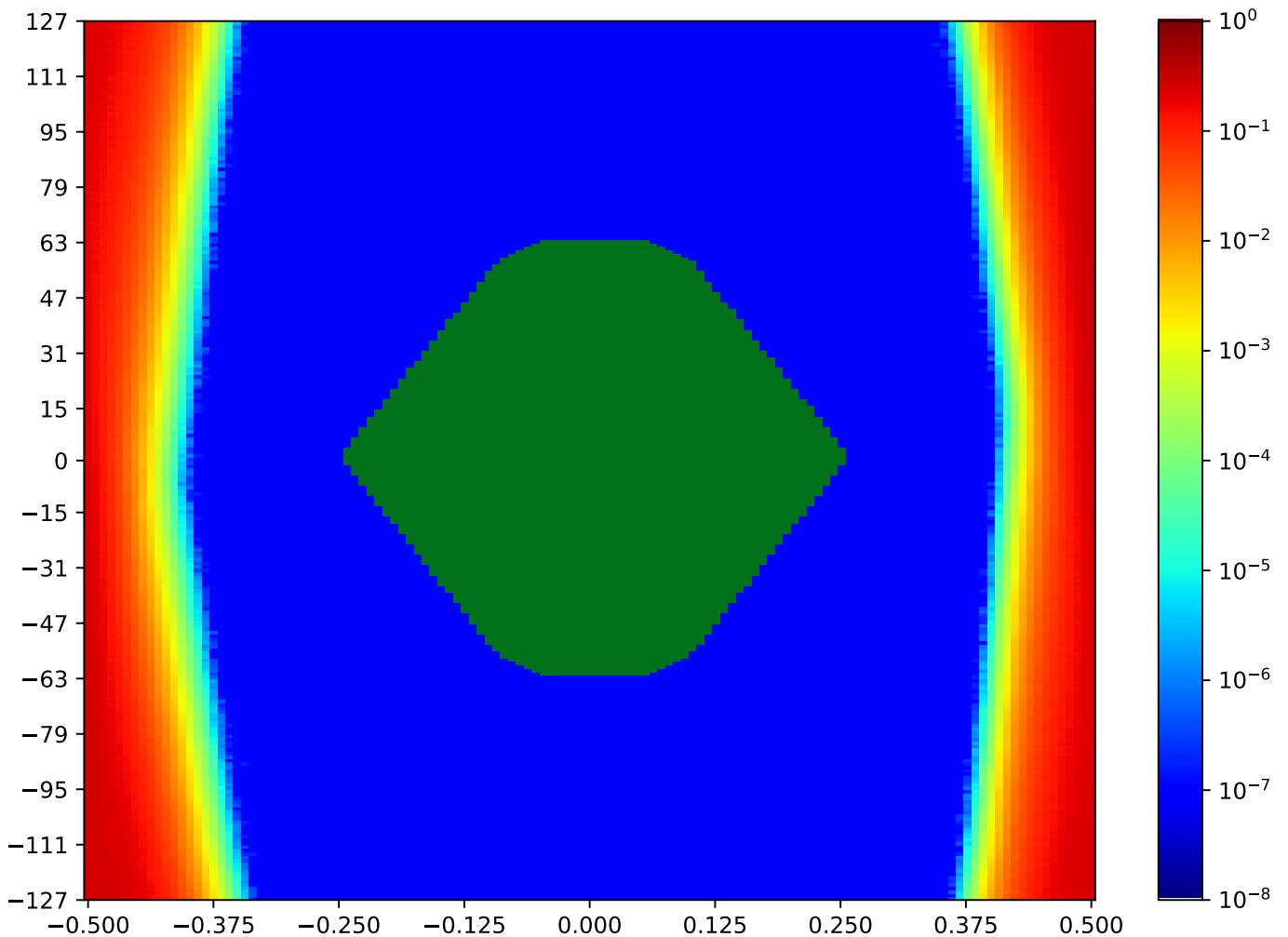


Figure 4.258: MSP_A_FPGA-TX2-04-RX13-04-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.6 MSP_A_FPGA-TX2-05-RX13-05-MSP_C_FPGA

Table 4.239: MSP_A_FPGA-TX2-05-RX13-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:26:37		2018-Sep-27 18:27:52	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24836	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

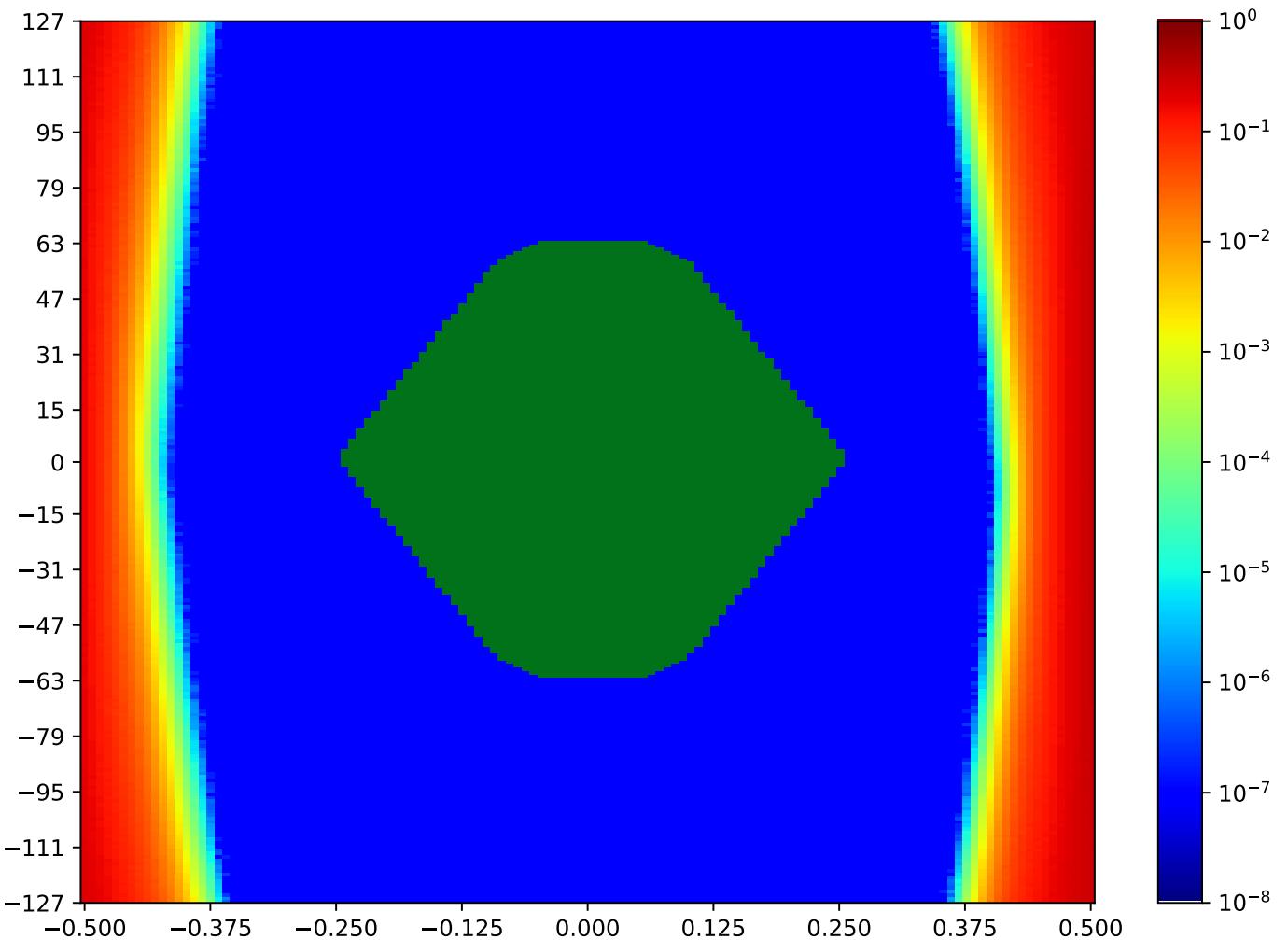


Figure 4.259: MSP_A_FPGA-TX2-05-RX13-05-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.7 MSP_A_FPGA-TX2-06-RX13-06-MSP_C_FPGA

Table 4.240: MSP_A_FPGA-TX2-06-RX13-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:37:54		2018-Sep-27 18:39:10	
Reset RX	OA	HO		VO	VO (%)
true	24387	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

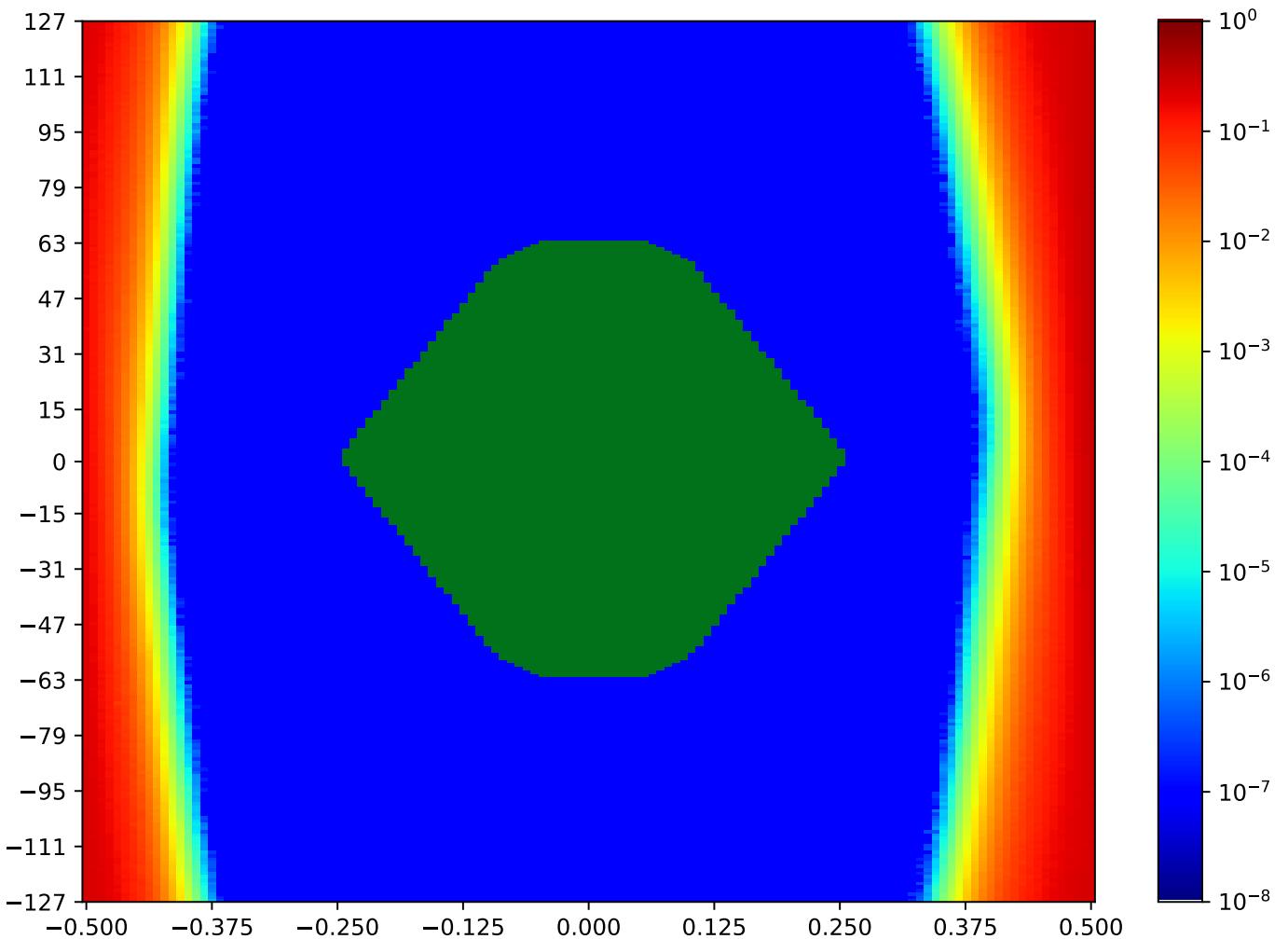


Figure 4.260: MSP_A_FPGA-TX2-06-RX13-06-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.8 MSP_A_FPGA-TX2-07-RX13-07-MSP_C_FPGA

Table 4.241: MSP_A_FPGA-TX2-07-RX13-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:29:06		2018-Sep-27 18:30:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24119	101	78.29%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

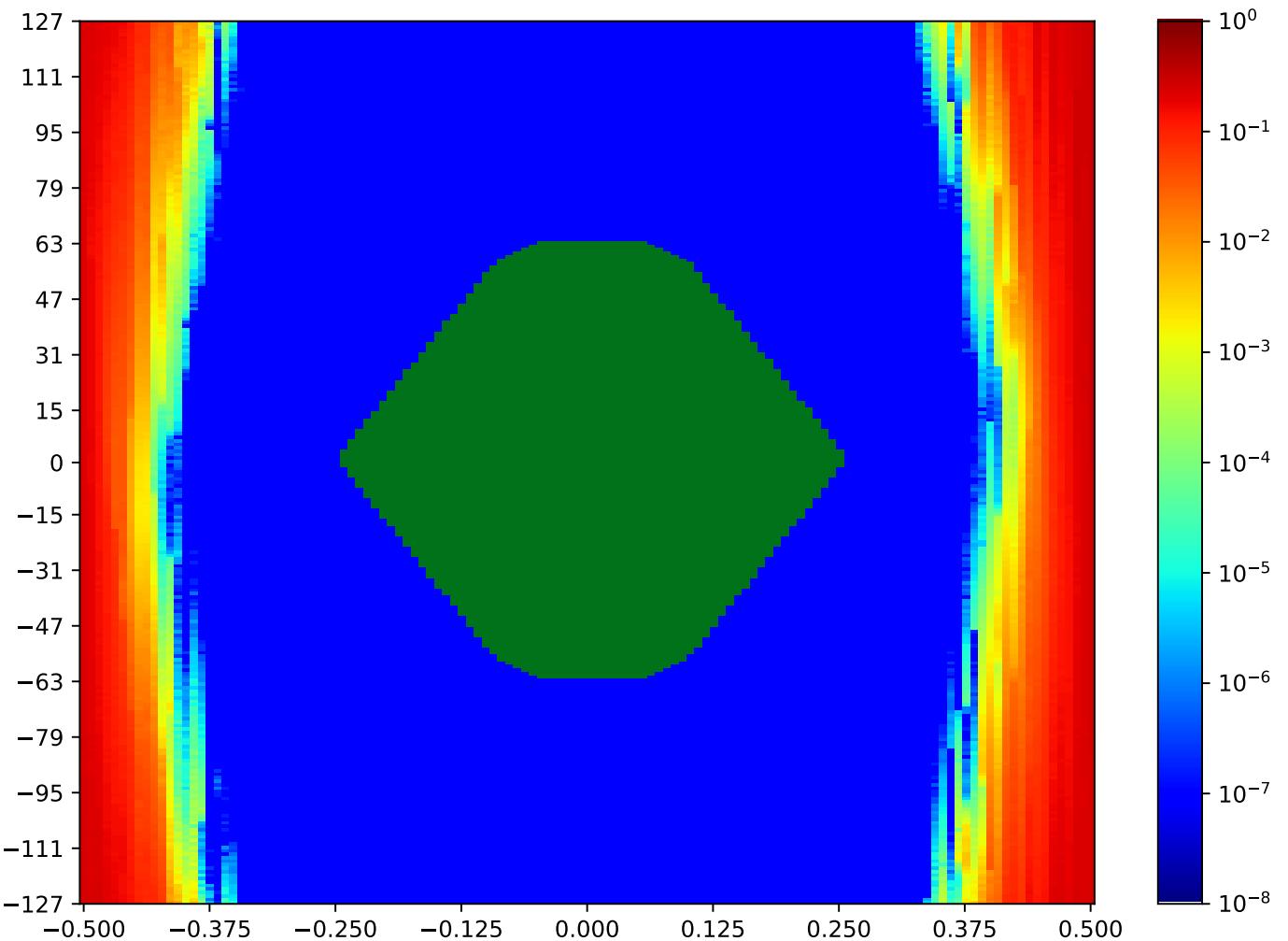


Figure 4.261: MSP_A_FPGA-TX2-07-RX13-07-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.9 MSP_A_FPGA-TX2-08-RX13-08-MSP_C_FPGA

Table 4.242: MSP_A_FPGA-TX2-08-RX13-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:36:38		2018-Sep-27 18:37:54	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24442	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

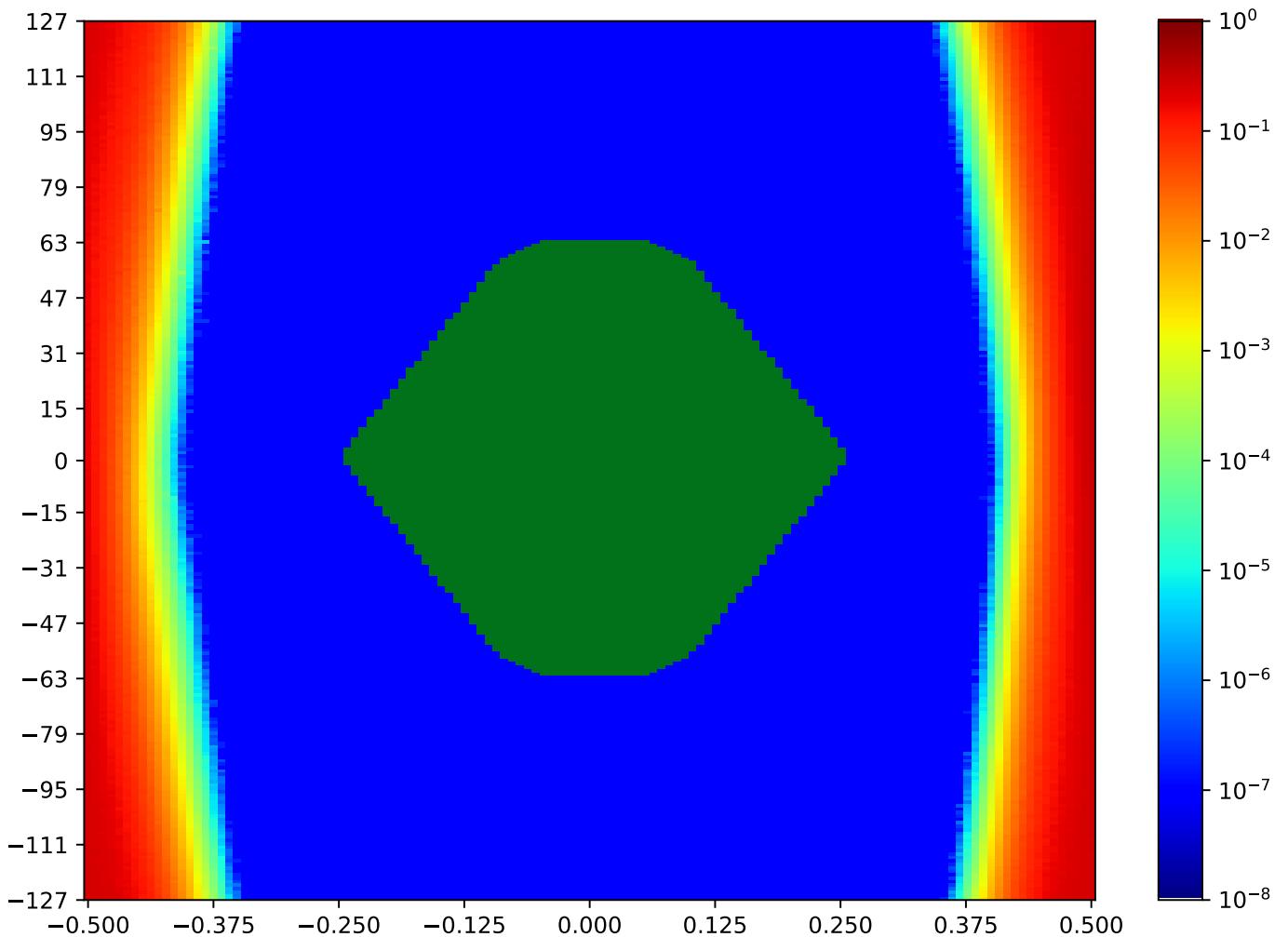


Figure 4.262: MSP_A_FPGA-TX2-08-RX13-08-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.10 MSP_A_FPGA-TX2-09-RX13-09-MSP_C_FPGA

Table 4.243: MSP_A_FPGA-TX2-09-RX13-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:30:21		2018-Sep-27 18:31:36	
Reset RX	OA	HO		VO	VO (%)
true	24293	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

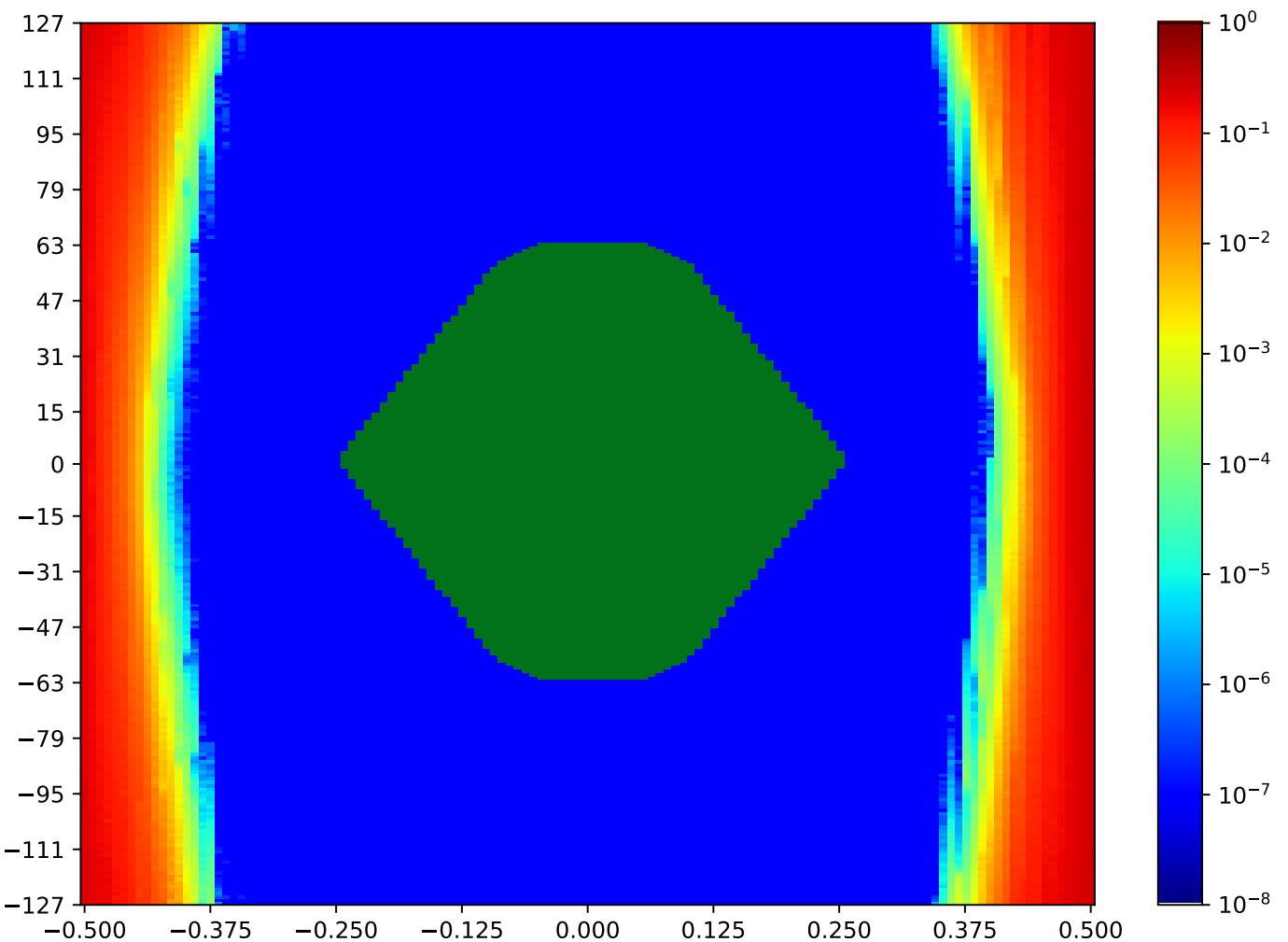


Figure 4.263: MSP_A_FPGA-TX2-09-RX13-09-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.11 MSP_A_FPGA-TX2-10-RX13-10-MSP_C_FPGA

Table 4.244: MSP_A_FPGA-TX2-10-RX13-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:34:07		2018-Sep-27 18:35:22	
Reset RX	OA	HO		VO	VO (%)
true	24791	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

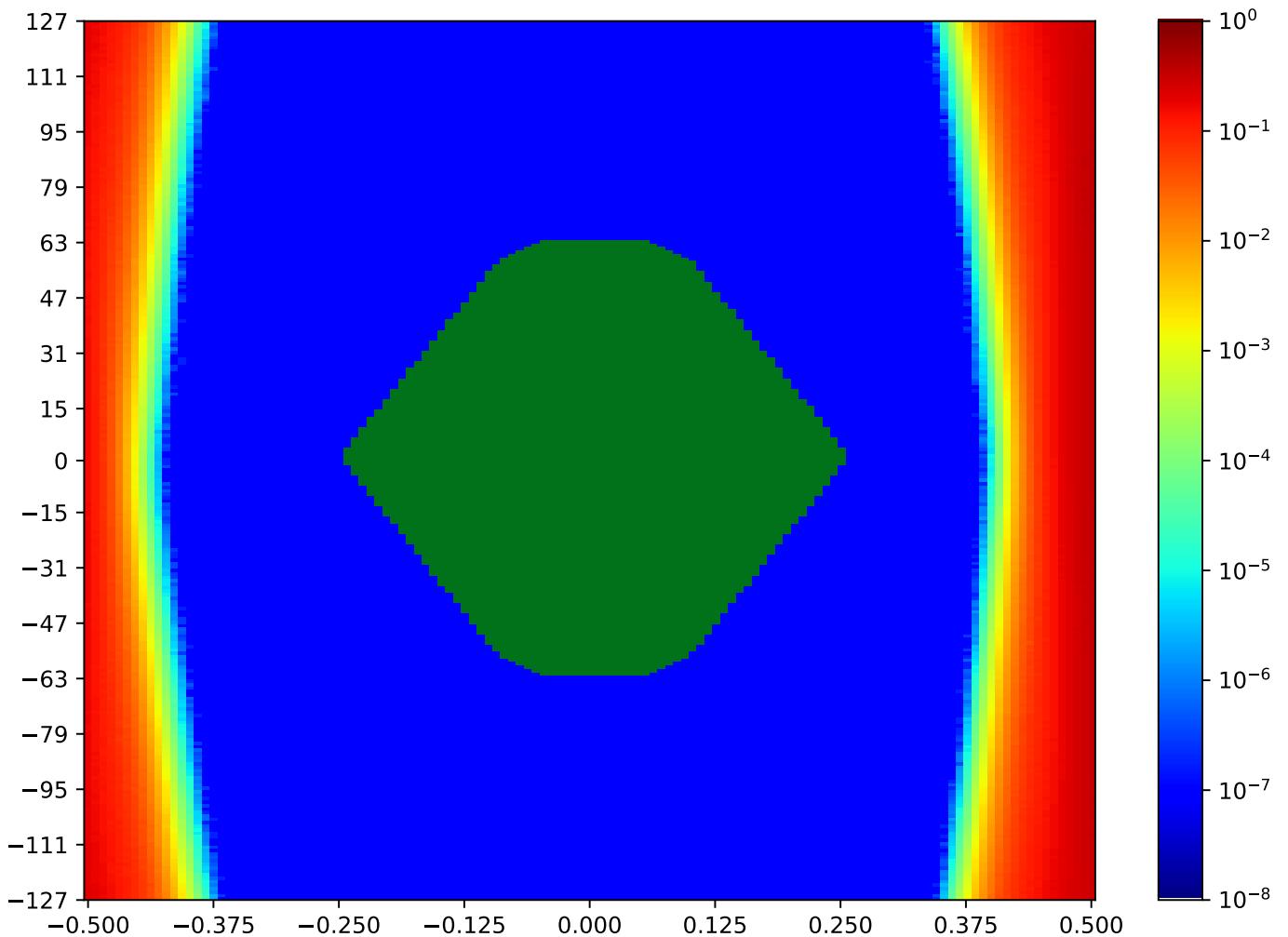


Figure 4.264: MSP_A_FPGA-TX2-10-RX13-10-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.20.12 MSP_A_FPGA-TX2-11-RX13-11-MSP_C_FPGA

Table 4.245: MSP_A_FPGA-TX2-11-RX13-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:32:51		2018-Sep-27 18:34:07	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24492	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

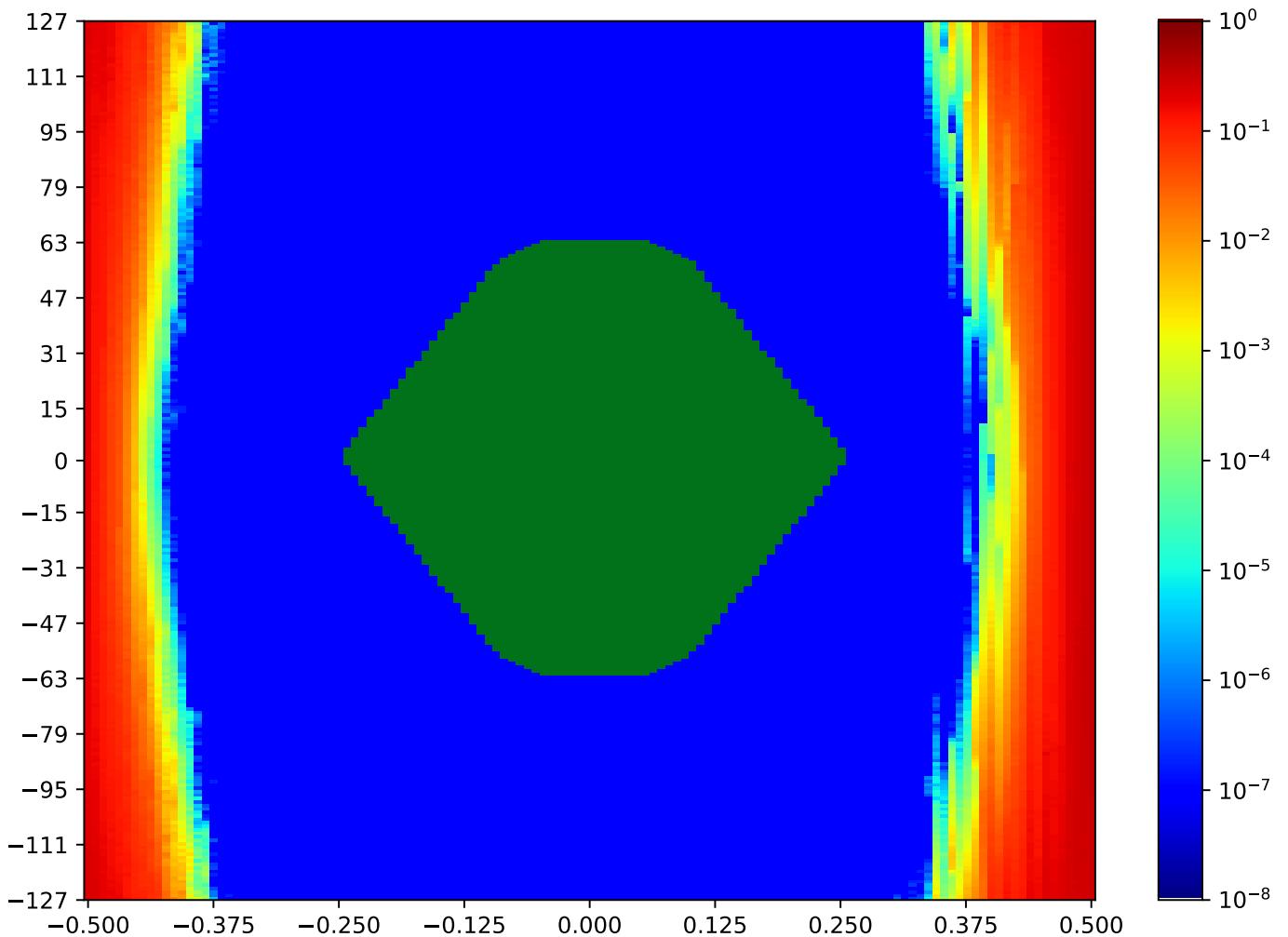


Figure 4.265: MSP_A_FPGA-TX2-11-RX13-11-MSP_C_FPGA

Call back to summary Figure 4.253. Sibling eye diagrams: V2-12.8.

4.21 MSP_C TX3 MSP_A RX3 Minipod Loopback

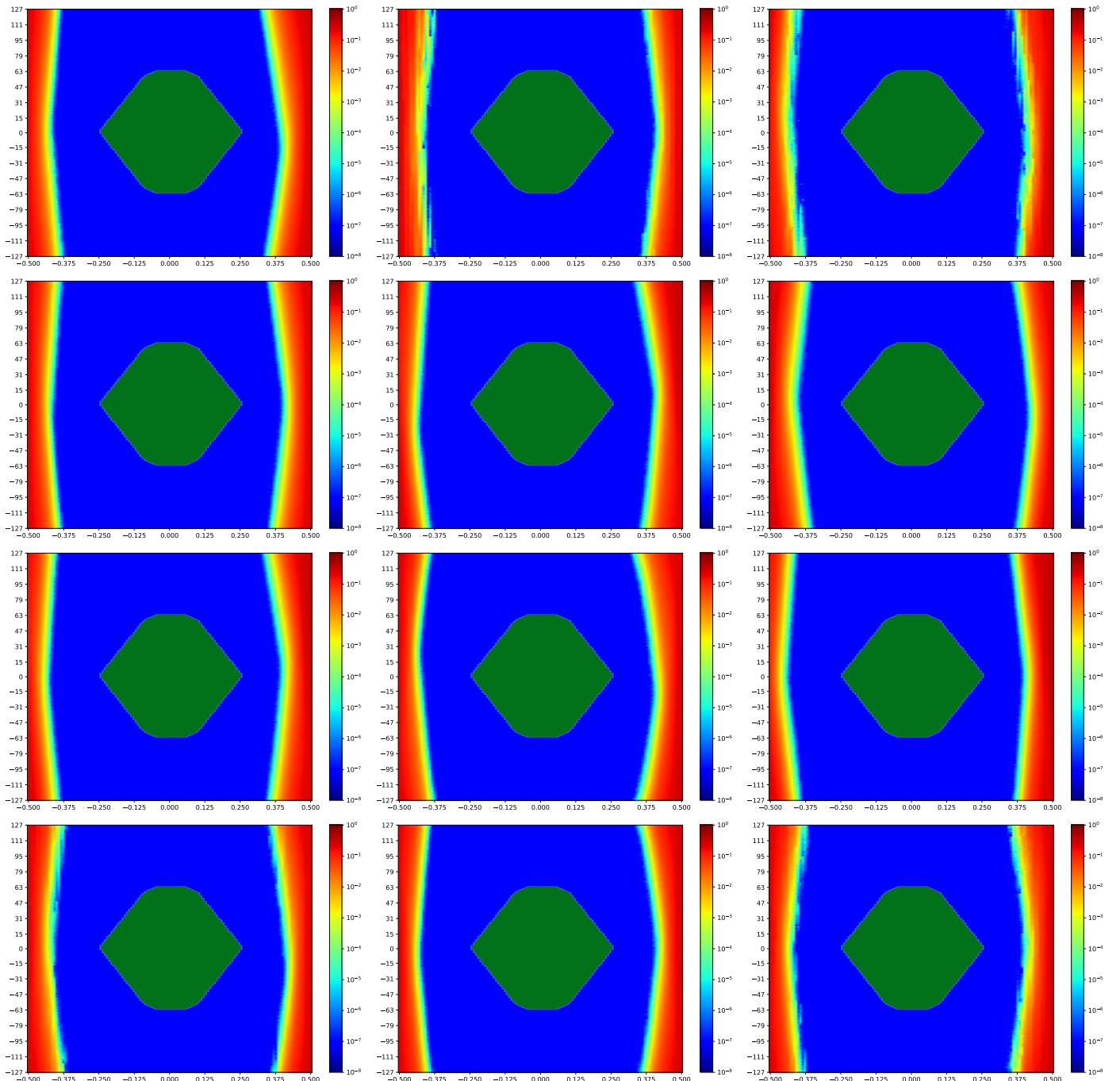


Figure 4.266: MSP_C TX3 MSP_A RX3 Minipod Loopback

A cross-reference to Figure 4.266. Sibling eye diagrams: V2-12.8.

Next summary Figure 4.279.

4.21.1 MSP_C_FPGA-TX3-00-RX3-00-MSP_A_FPGA

Table 4.246: MSP_C_FPGA-TX3-00-RX3-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:42:57		2018-Sep-27 18:44:12	
Reset RX	OA	HO		VO	VO (%)
true	24086	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

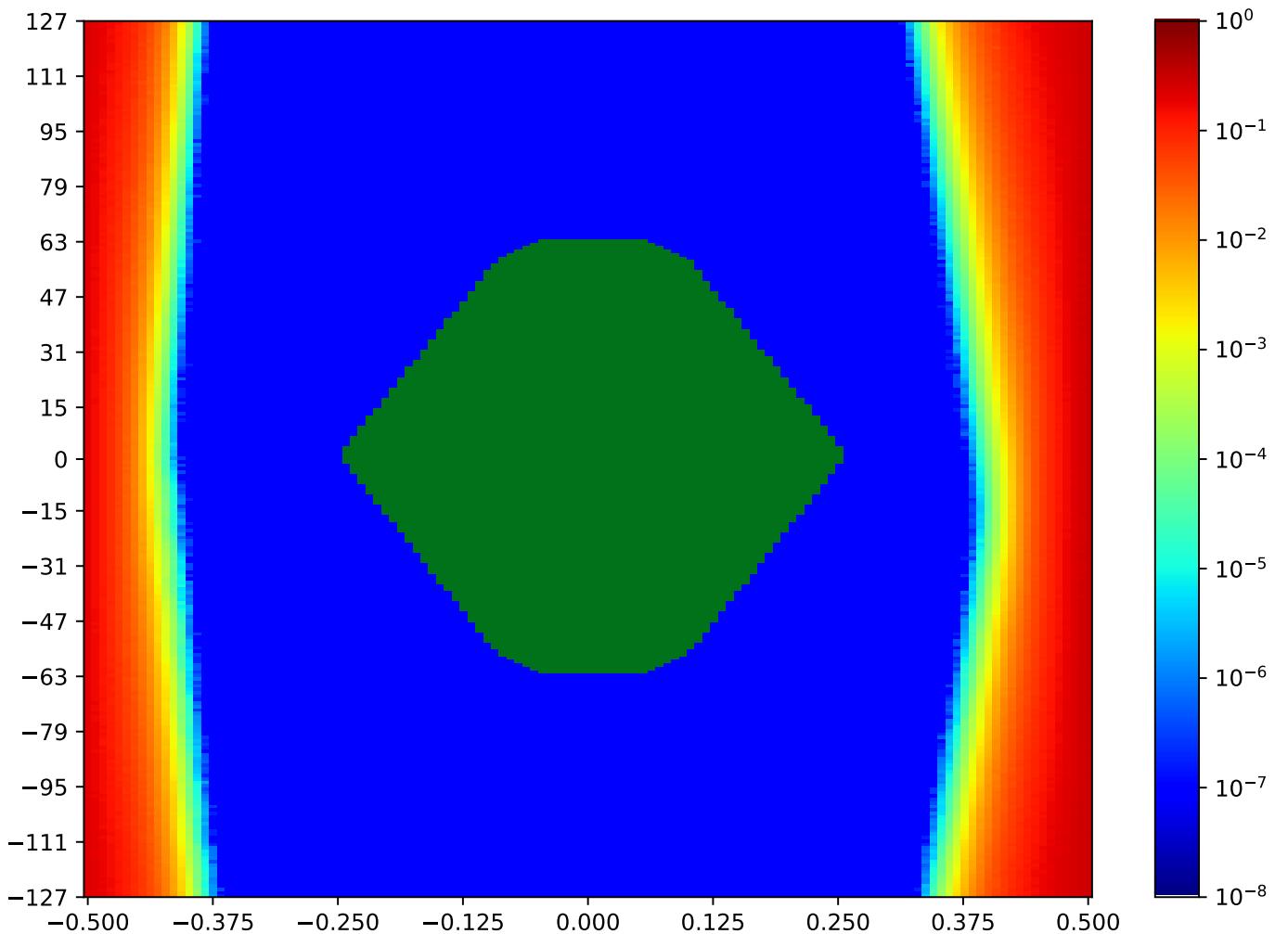


Figure 4.267: MSP_C_FPGA-TX3-00-RX3-00-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.2 MSP_C_FPGA-TX3-01-RX3-01-MSP_A_FPGA

Table 4.247: MSP_C_FPGA-TX3-01-RX3-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:45:28		2018-Sep-27 18:46:44	
Reset RX	OA	HO		VO	VO (%)
true	24805	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

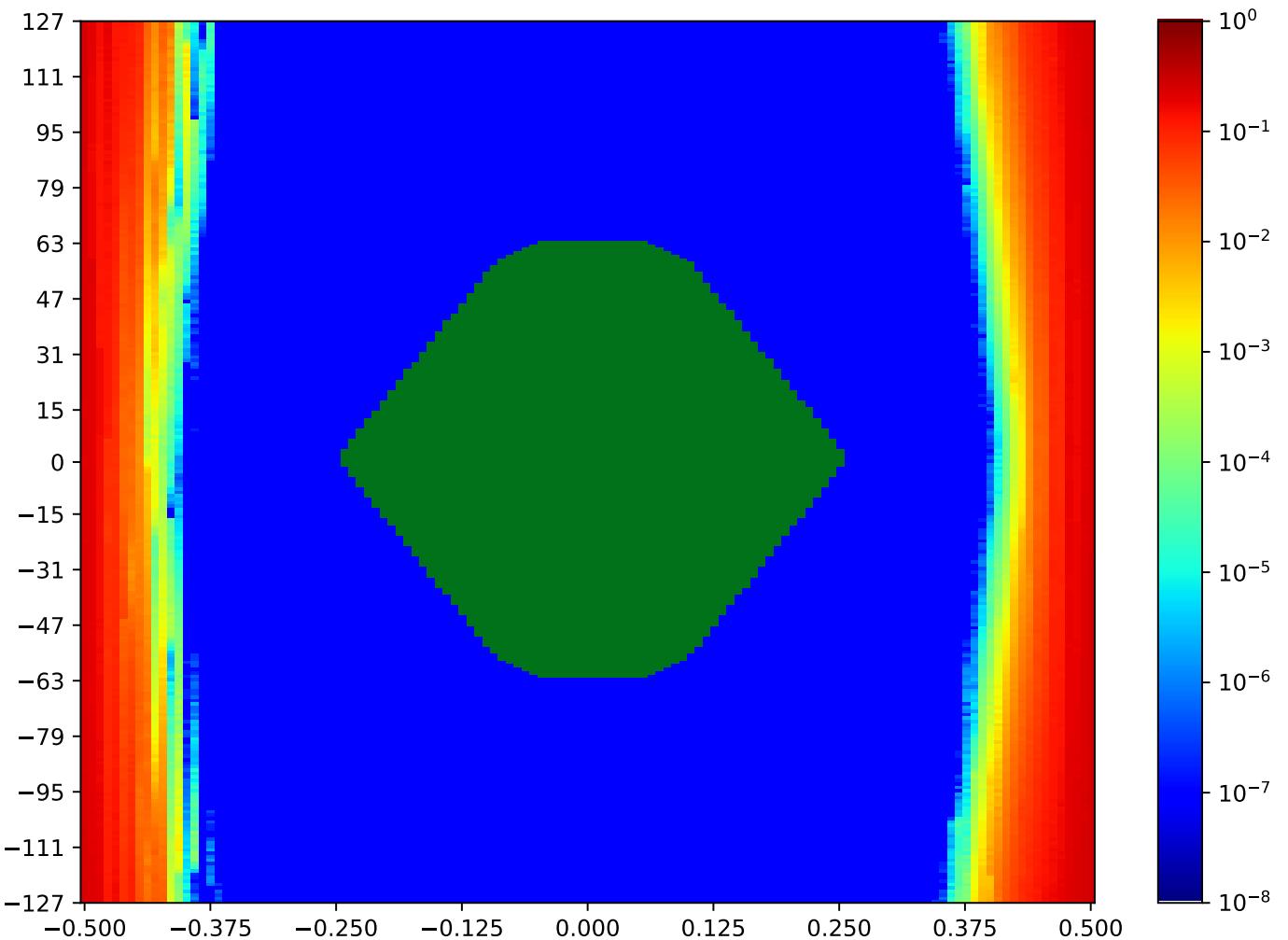


Figure 4.268: MSP_C_FPGA-TX3-01-RX3-01-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.3 MSP_C_FPGA-TX3-02-RX3-02-MSP_A_FPGA

Table 4.248: MSP_C_FPGA-TX3-02-RX3-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:46:44		2018-Sep-27 18:48:00	
Reset RX	OA	HO		VO	VO (%)
true	24798	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

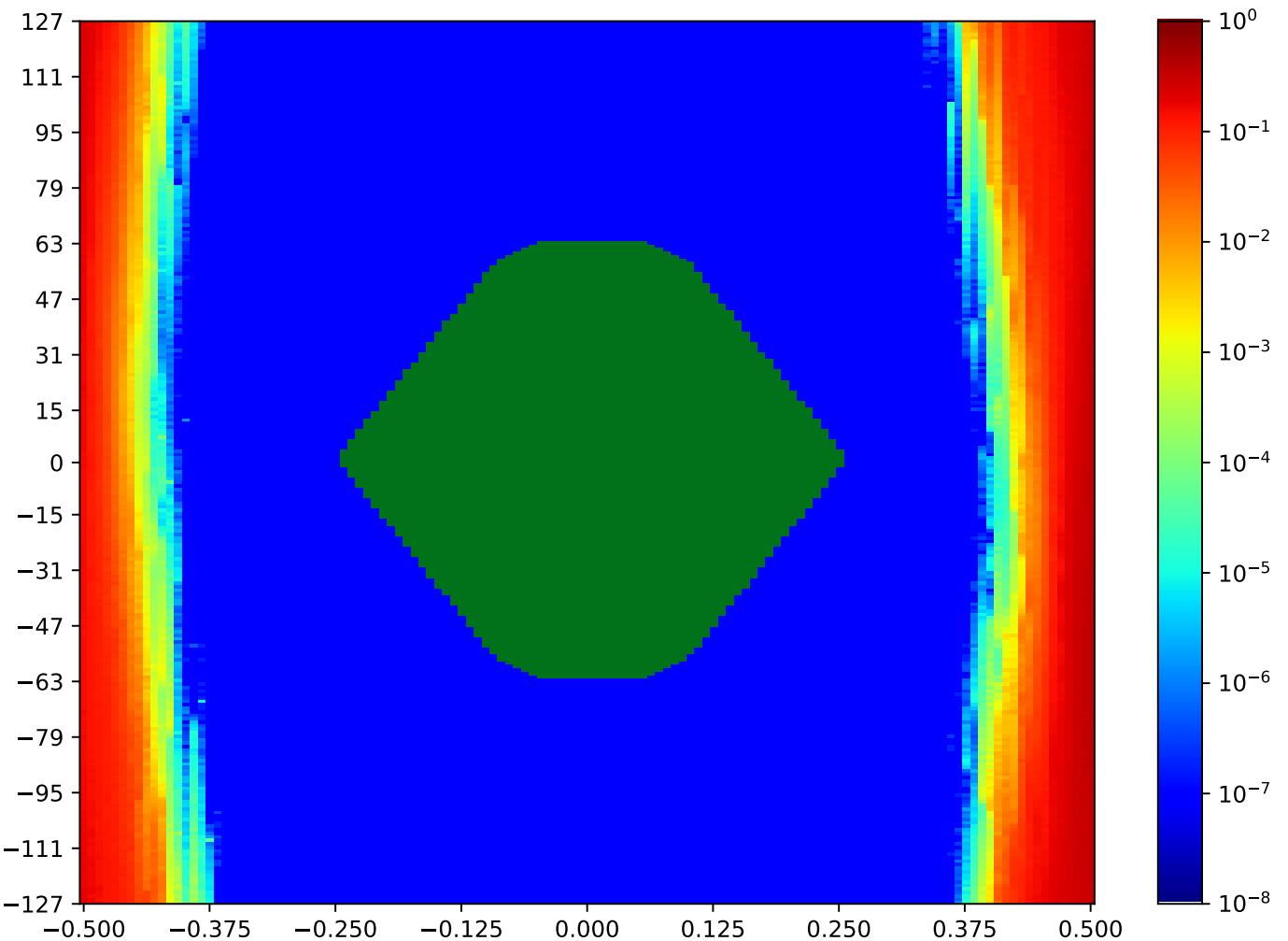


Figure 4.269: MSP_C_FPGA-TX3-02-RX3-02-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.4 MSP_C_FPGA-TX3-03-RX3-03-MSP_A_FPGA

Table 4.249: MSP_C_FPGA-TX3-03-RX3-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:40:26		2018-Sep-27 18:41:41	
Reset RX	OA	HO		VO	VO (%)
true	24632	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

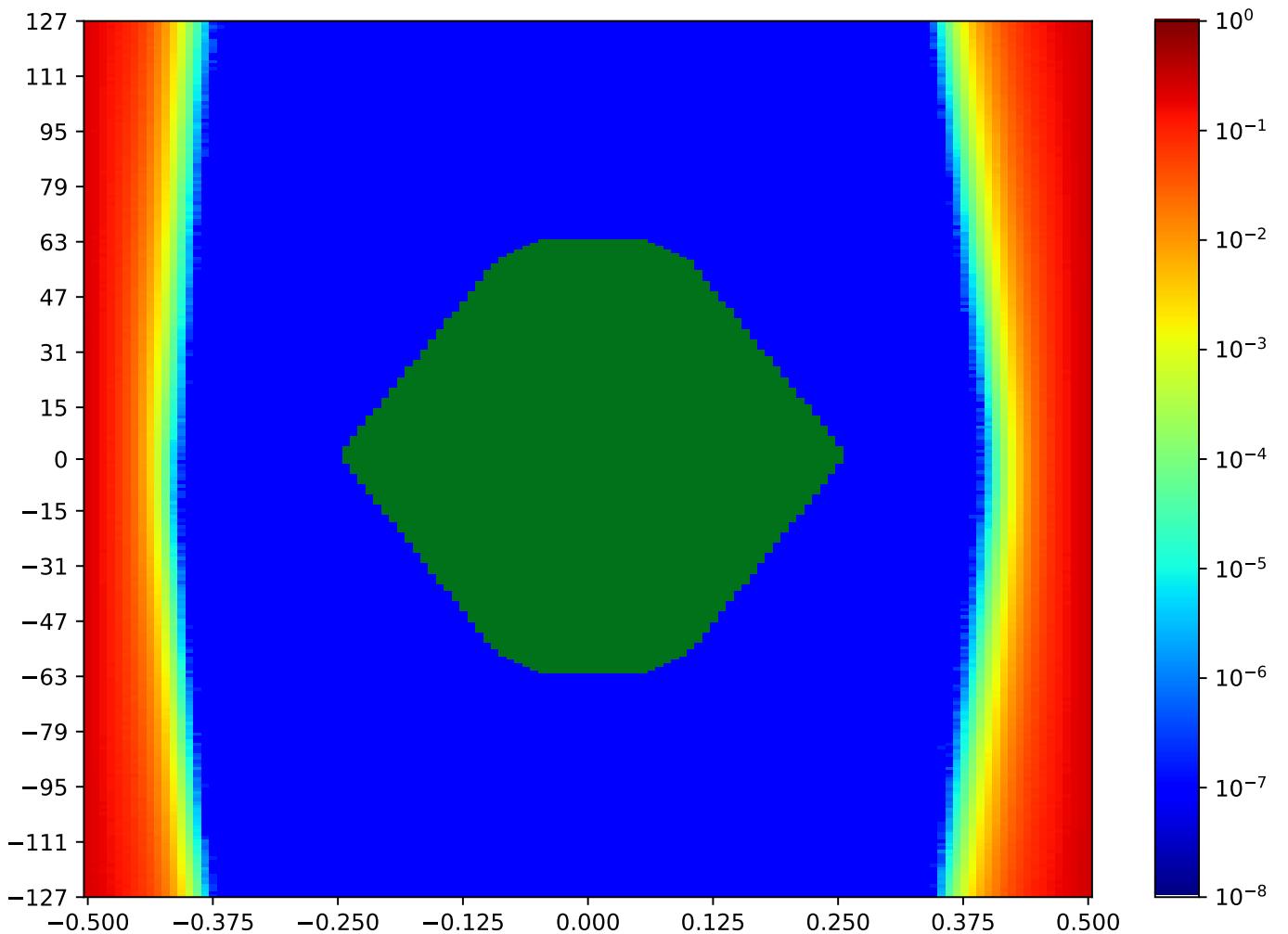


Figure 4.270: MSP_C_FPGA-TX3-03-RX3-03-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.5 MSP_C_FPGA-TX3-04-RX3-04-MSP_A_FPGA

Table 4.250: MSP_C_FPGA-TX3-04-RX3-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:50:31		2018-Sep-27 18:51:47	
Reset RX	OA	HO		VO	VO (%)
true	24885	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

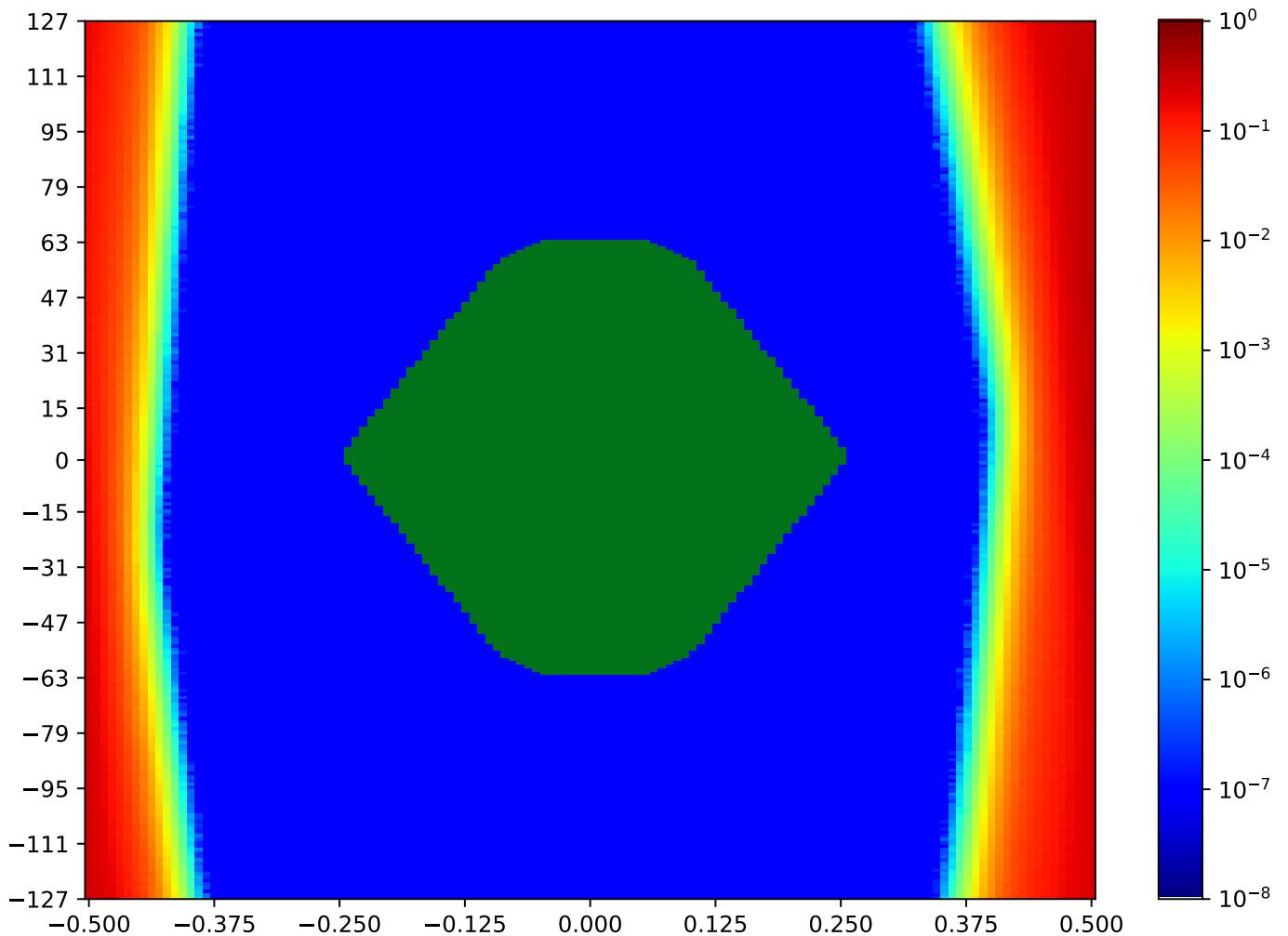


Figure 4.271: MSP_C_FPGA-TX3-04-RX3-04-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.6 MSP_C_FPGA-TX3-05-RX3-05-MSP_A_FPGA

Table 4.251: MSP_C_FPGA-TX3-05-RX3-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:39:10		2018-Sep-27 18:40:25	
Reset RX	OA	HO		VO	VO (%)
true	24364	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

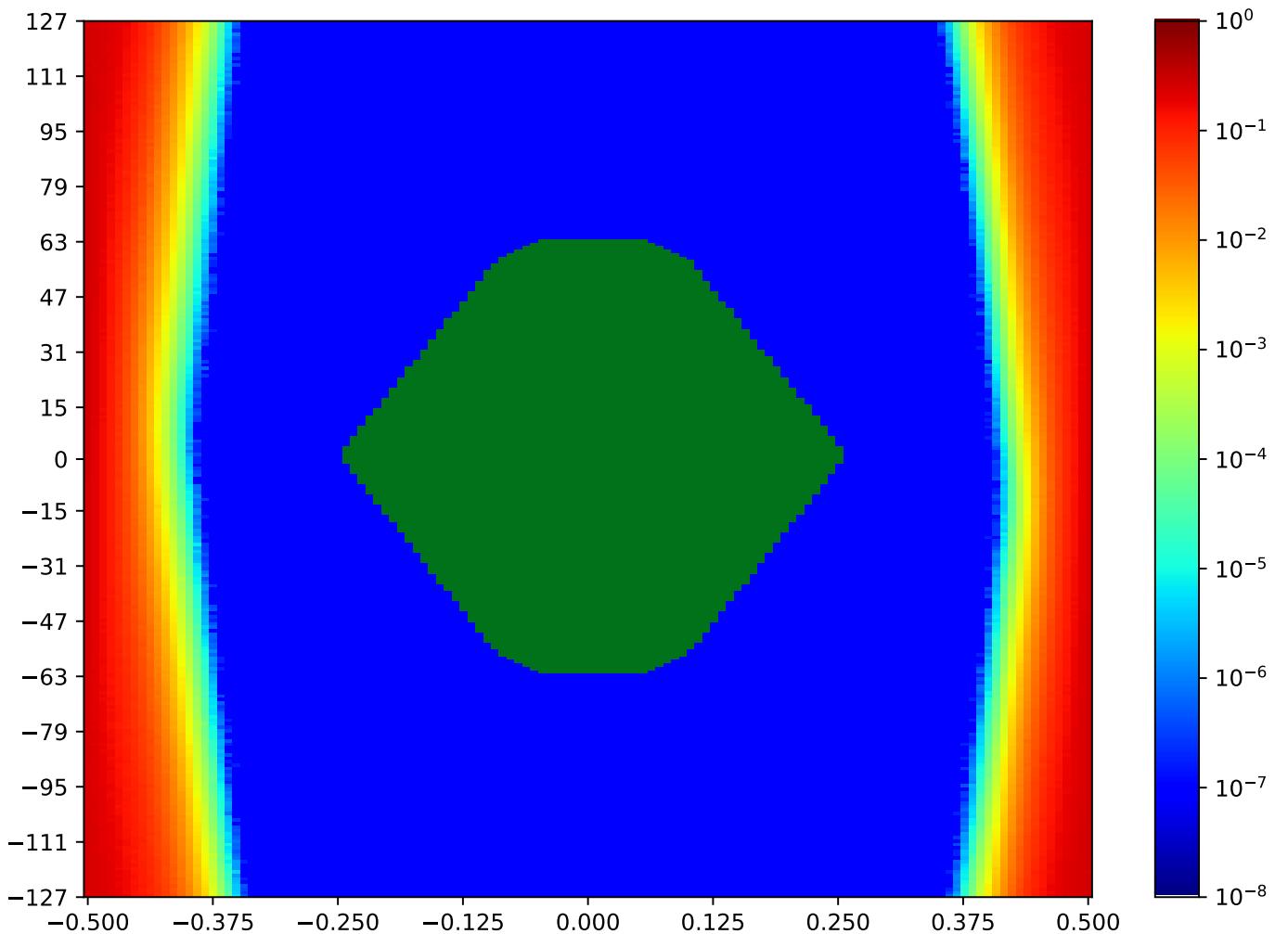


Figure 4.272: MSP_C_FPGA-TX3-05-RX3-05-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.7 MSP_C_FPGA-TX3-06-RX3-06-MSP_A_FPGA

Table 4.252: MSP_C_FPGA-TX3-06-RX3-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:53:03		2018-Sep-27 18:54:18	
Reset RX	OA	HO		VO	VO (%)
true	24675	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

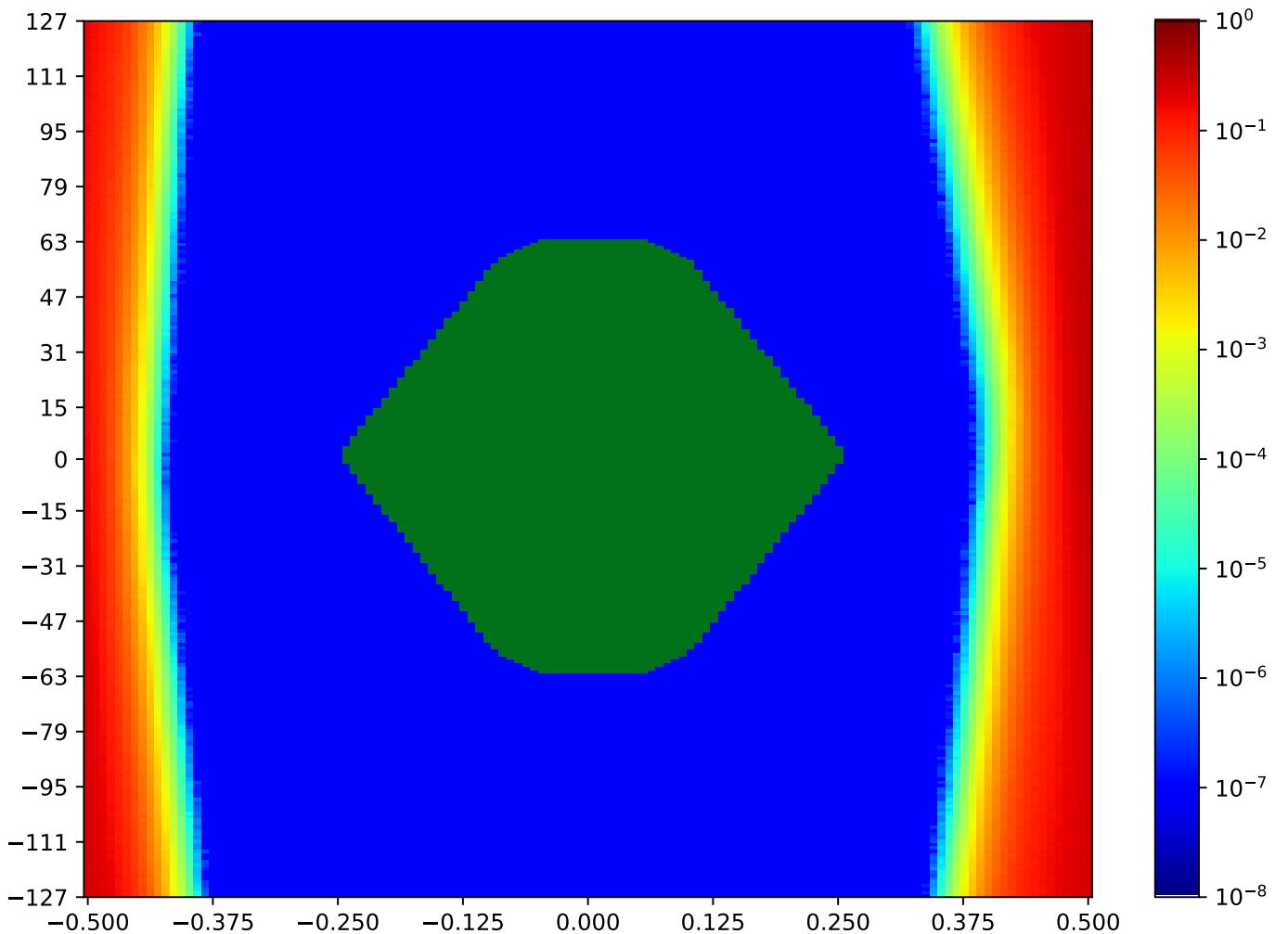


Figure 4.273: MSP_C_FPGA-TX3-06-RX3-06-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.8 MSP_C_FPGA-TX3-07-RX3-07-MSP_A_FPGA

Table 4.253: MSP_C_FPGA-TX3-07-RX3-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:41:41		2018-Sep-27 18:42:57	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24620	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

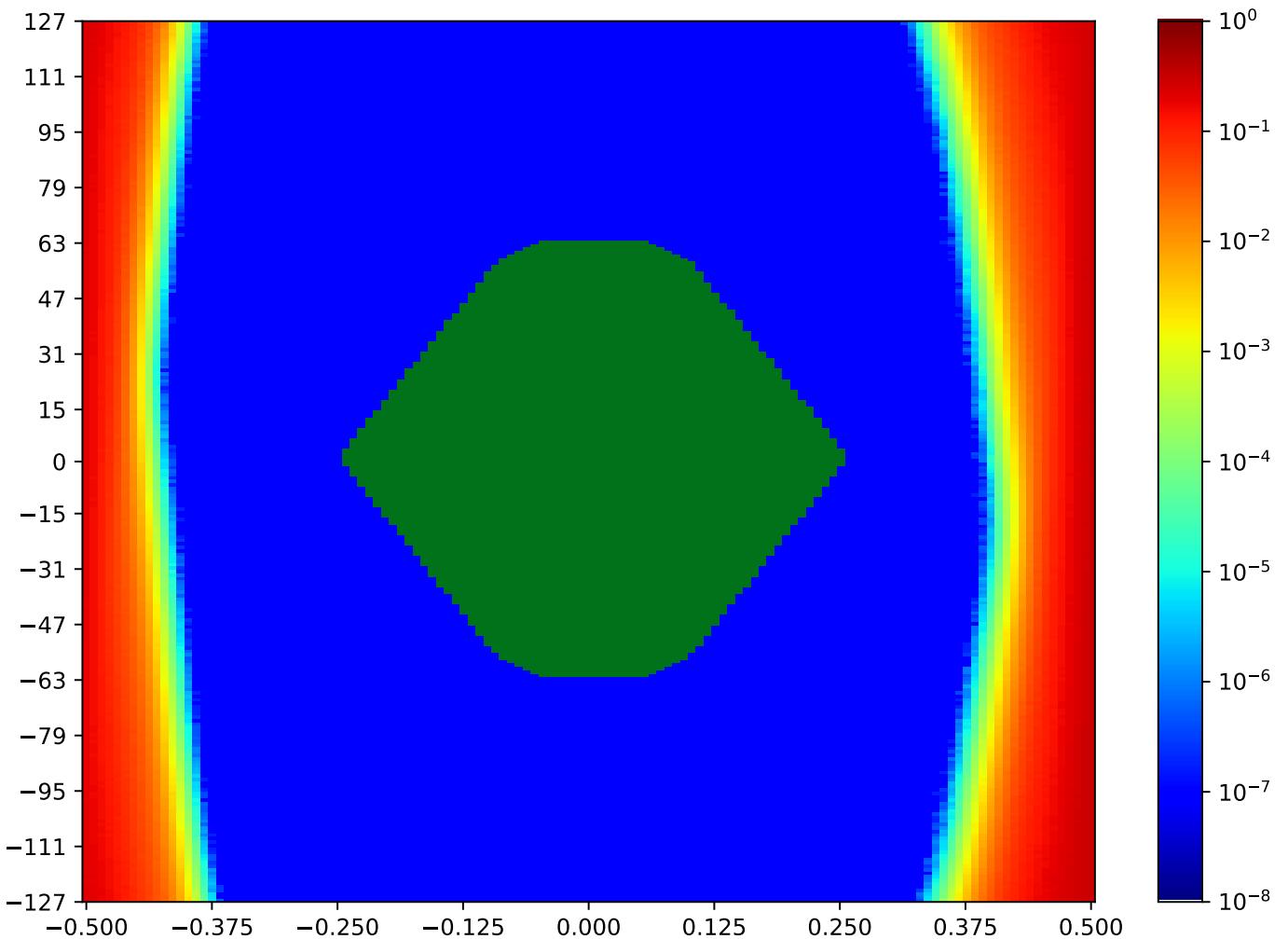


Figure 4.274: MSP_C_FPGA-TX3-07-RX3-07-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.9 MSP_C_FPGA-TX3-08-RX3-08-MSP_A_FPGA

Table 4.254: MSP_C_FPGA-TX3-08-RX3-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:51:47		2018-Sep-27 18:53:03	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	25242	103		79.84%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

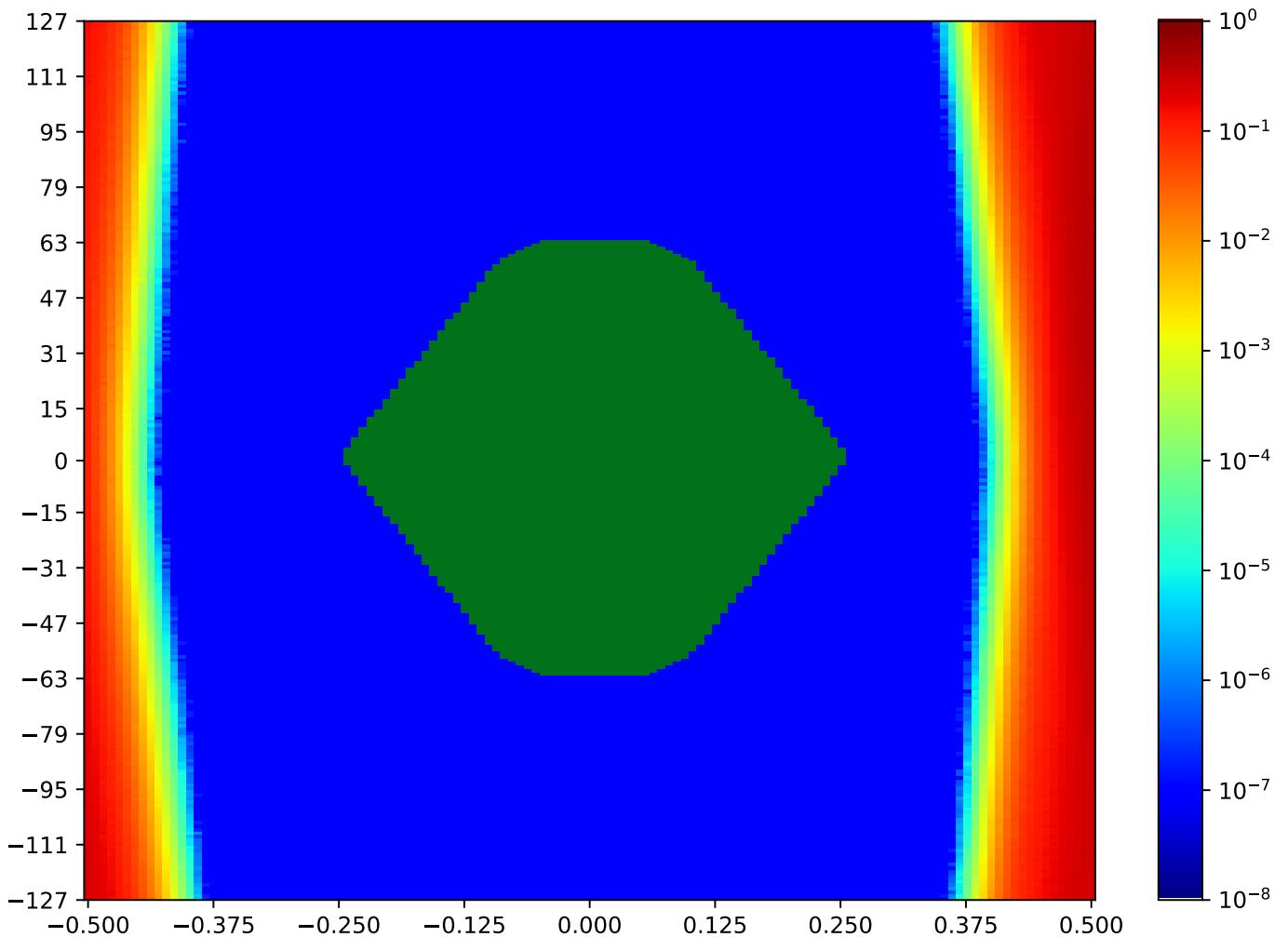


Figure 4.275: MSP_C_FPGA-TX3-08-RX3-08-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.10 MSP_C_FPGA-TX3-09-RX3-09-MSP_A_FPGA

Table 4.255: MSP_C_FPGA-TX3-09-RX3-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:44:12		2018-Sep-27 18:45:28	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24701	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

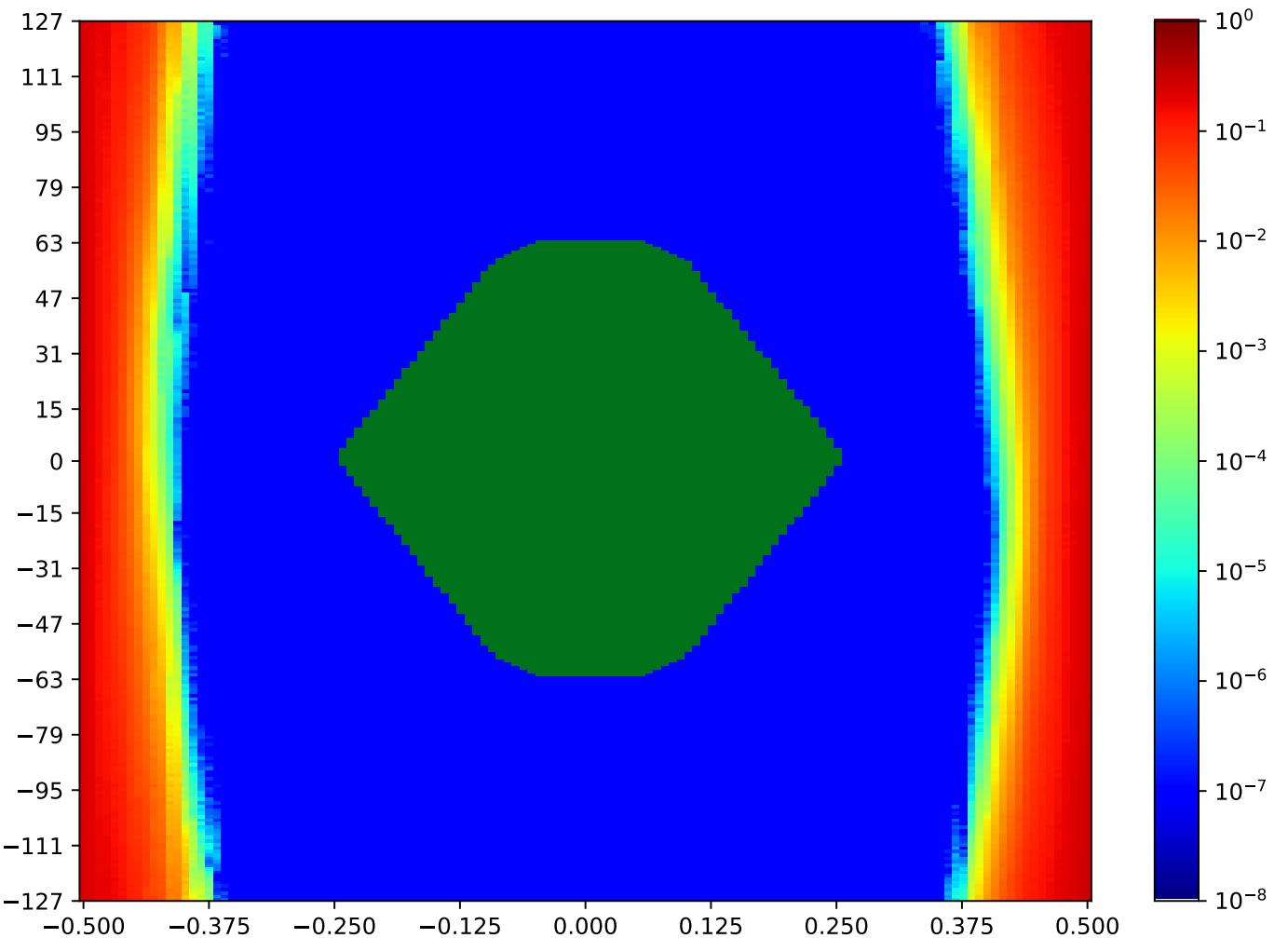


Figure 4.276: MSP_C_FPGA-TX3-09-RX3-09-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.11 MSP_C_FPGA-TX3-10-RX3-10-MSP_A_FPGA

Table 4.256: MSP_C_FPGA-TX3-10-RX3-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:49:15		2018-Sep-27 18:50:31	
Reset RX	OA	HO		VO	VO (%)
true	25075	104		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

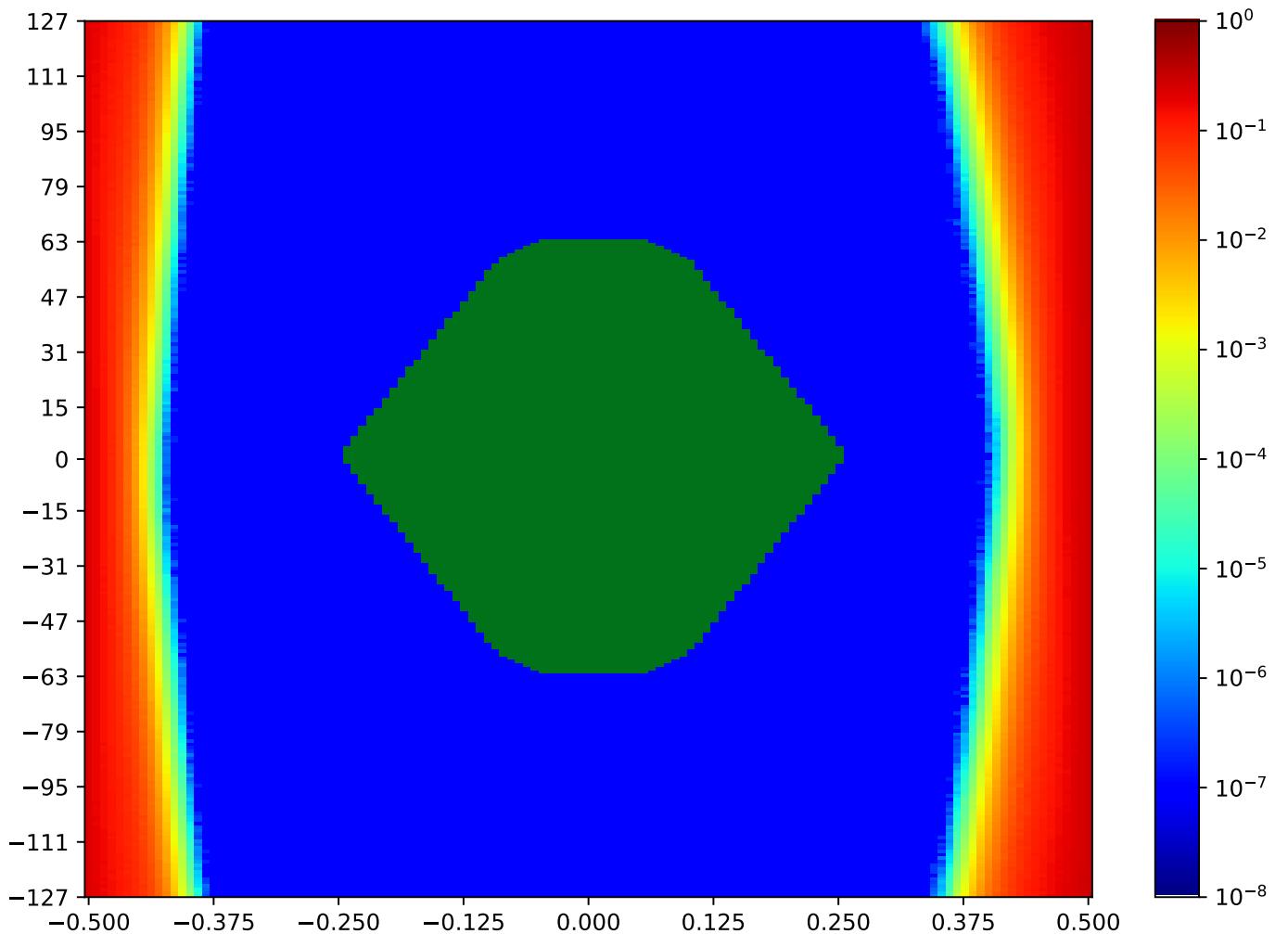


Figure 4.277: MSP_C_FPGA-TX3-10-RX3-10-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.21.12 MSP_C_FPGA-TX3-11-RX3-11-MSP_A_FPGA

Table 4.257: MSP_C_FPGA-TX3-11-RX3-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:48:00		2018-Sep-27 18:49:15	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24416	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

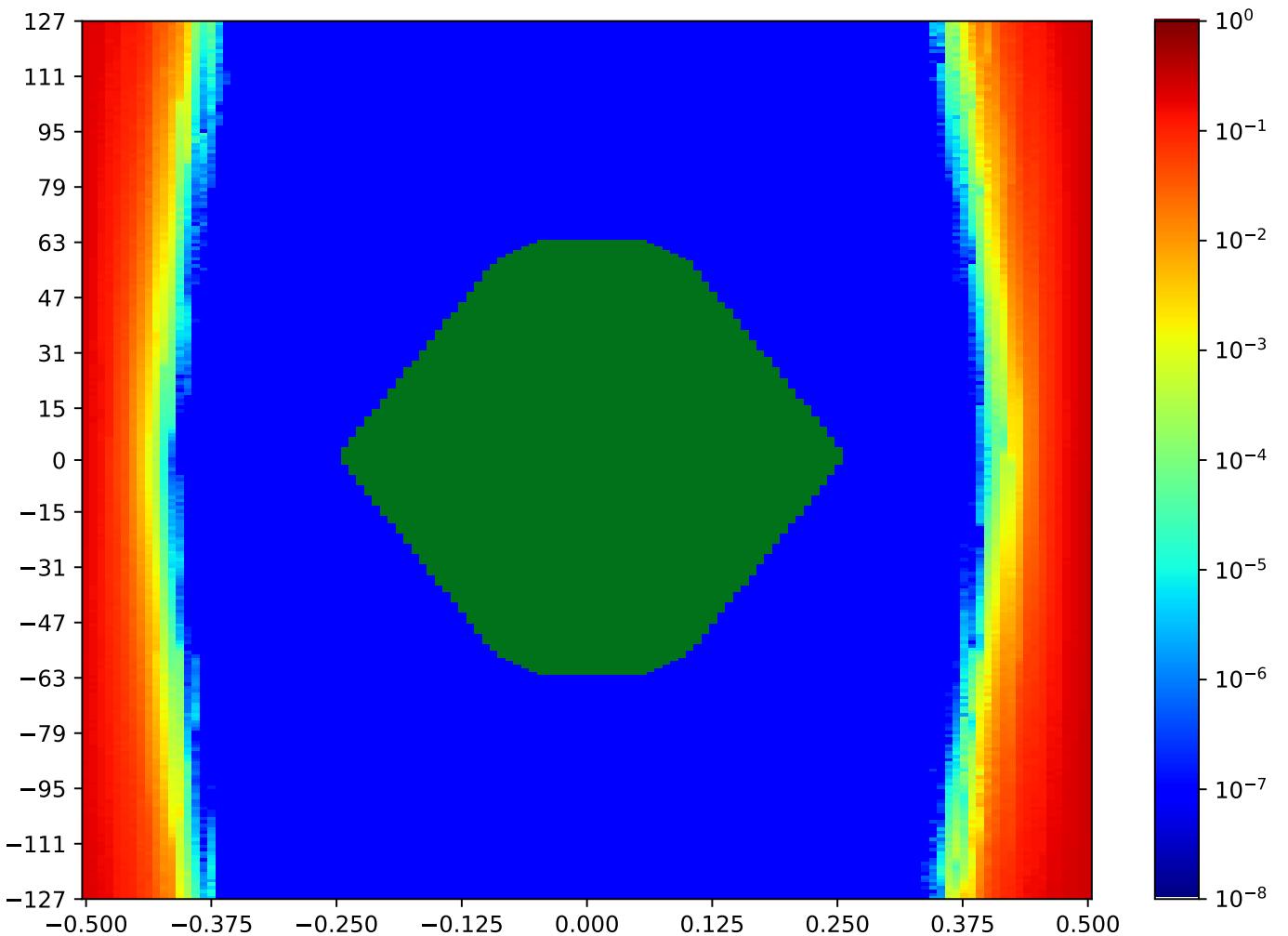


Figure 4.278: MSP_C_FPGA-TX3-11-RX3-11-MSP_A_FPGA

Call back to summary Figure 4.266. Sibling eye diagrams: V2-12.8.

4.22 MSP_C TX4 MSP_A RX4 Minipod Loopback

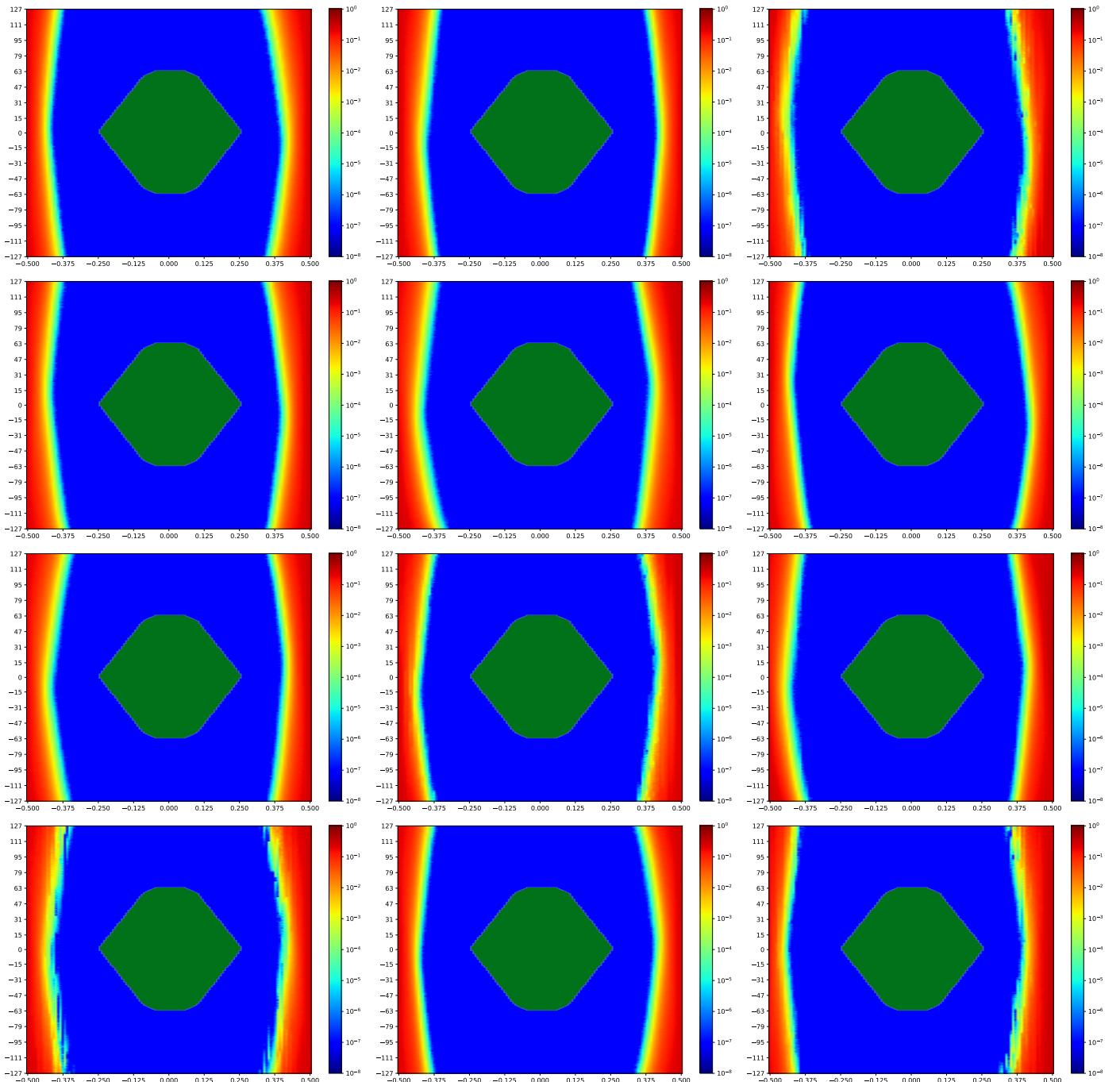


Figure 4.279: MSP_C TX4 MSP_A RX4 Minipod Loopback

A cross-reference to Figure 4.279. Sibling eye diagrams: V2-12.8.

Next summary Figure 5.1.

4.22.1 MSP_C_FPGA-TX4-00-RX4-00-MSP_A_FPGA

Table 4.258: MSP_C_FPGA-TX4-00-RX4-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:58:05		2018-Sep-27 18:59:21	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24288	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

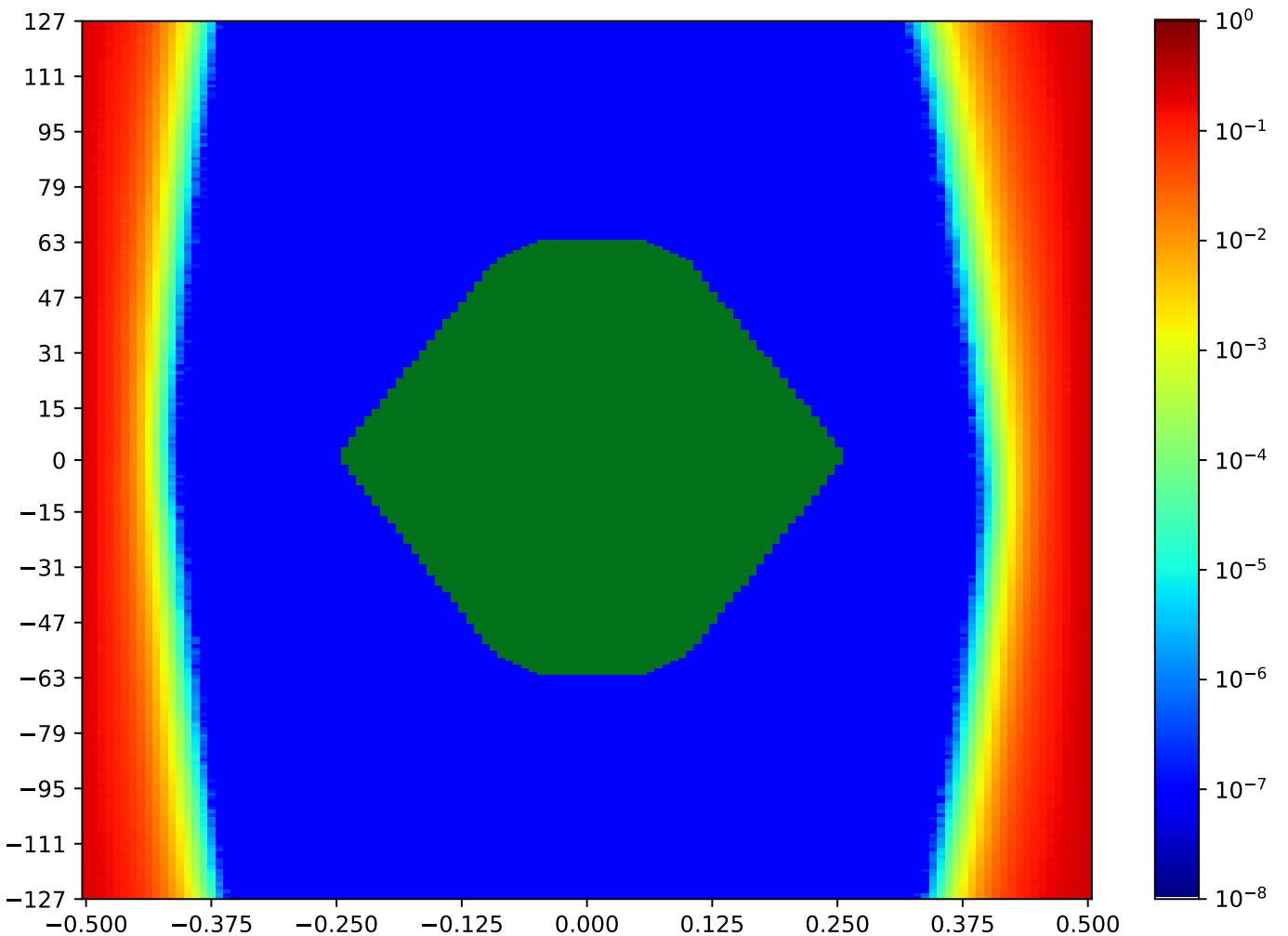


Figure 4.280: MSP_C_FPGA-TX4-00-RX4-00-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.2 MSP_C_FPGA-TX4-01-RX4-01-MSP_A_FPGA

Table 4.259: MSP_C_FPGA-TX4-01-RX4-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:55:34		2018-Sep-27 18:56:49	
Reset RX	OA	HO		VO	VO (%)
true	24585	101		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

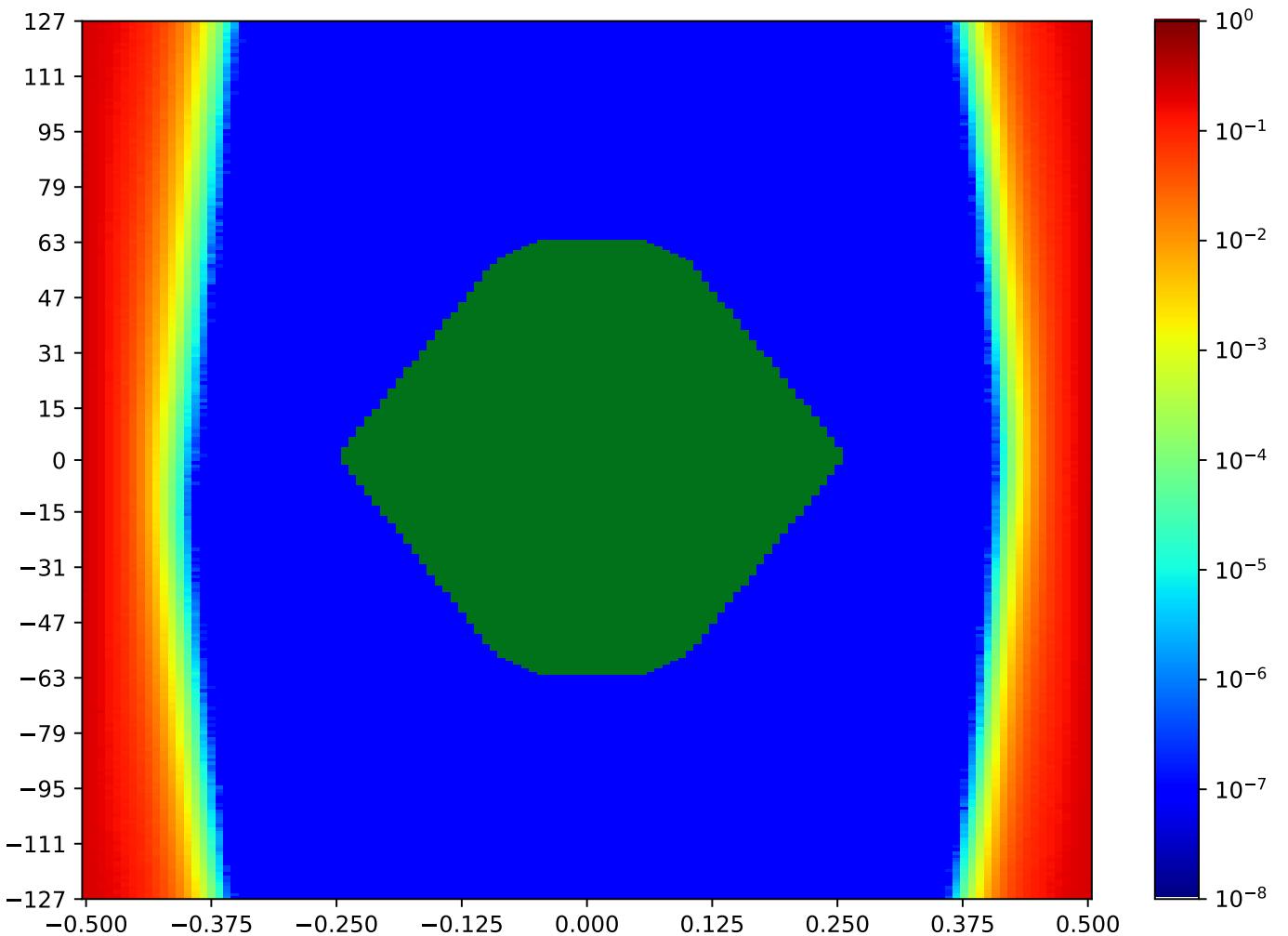


Figure 4.281: MSP_C_FPGA-TX4-01-RX4-01-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.3 MSP_C_FPGA-TX4-02-RX4-02-MSP_A_FPGA

Table 4.260: MSP_C_FPGA-TX4-02-RX4-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:01:51		2018-Sep-27 19:03:07	
Reset RX	OA	HO		VO	VO (%)
true	24527	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

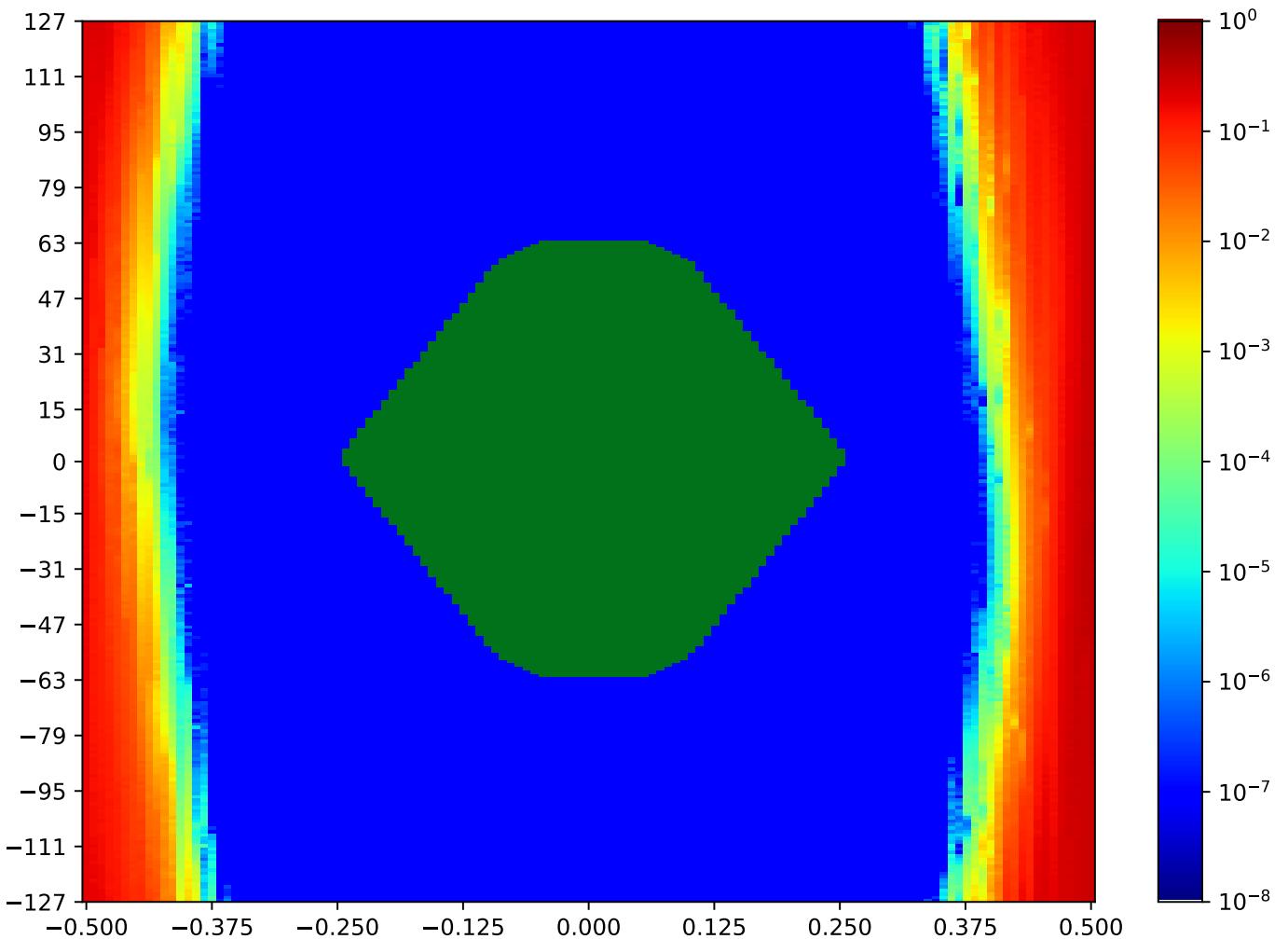


Figure 4.282: MSP_C_FPGA-TX4-02-RX4-02-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.4 MSP_C_FPGA-TX4-03-RX4-03-MSP_A_FPGA

Table 4.261: MSP_C_FPGA-TX4-03-RX4-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:54:18		2018-Sep-27 18:55:34	
Reset RX	OA	HO		VO	VO (%)
true	24128	100		77.52%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

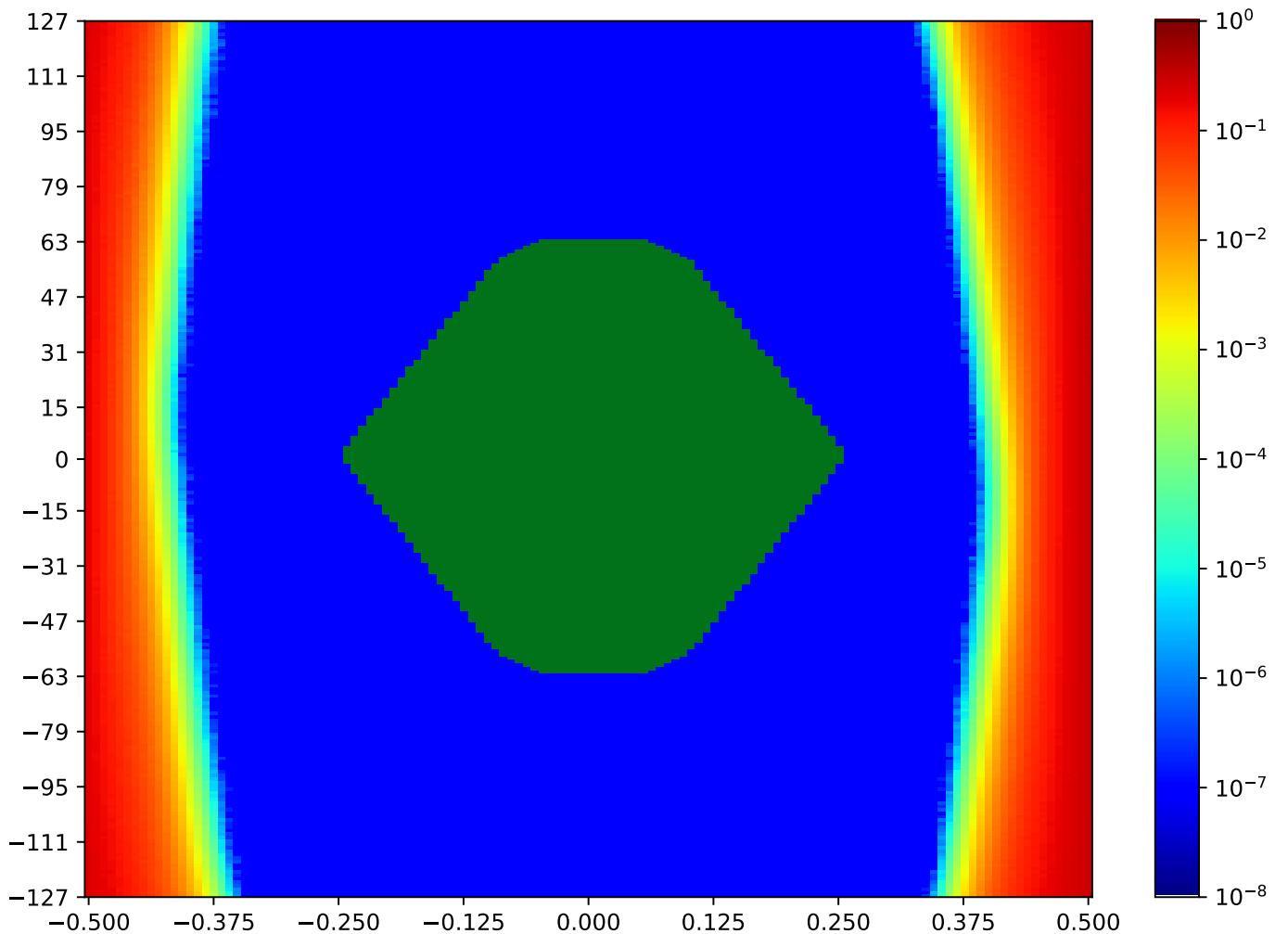


Figure 4.283: MSP_C_FPGA-TX4-03-RX4-03-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.5 MSP_C_FPGA-TX4-04-RX4-04-MSP_A_FPGA

Table 4.262: MSP_C_FPGA-TX4-04-RX4-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:05:38		2018-Sep-27 19:06:53	
Reset RX	OA	HO		VO	VO (%)
true	23389	99		76.74%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

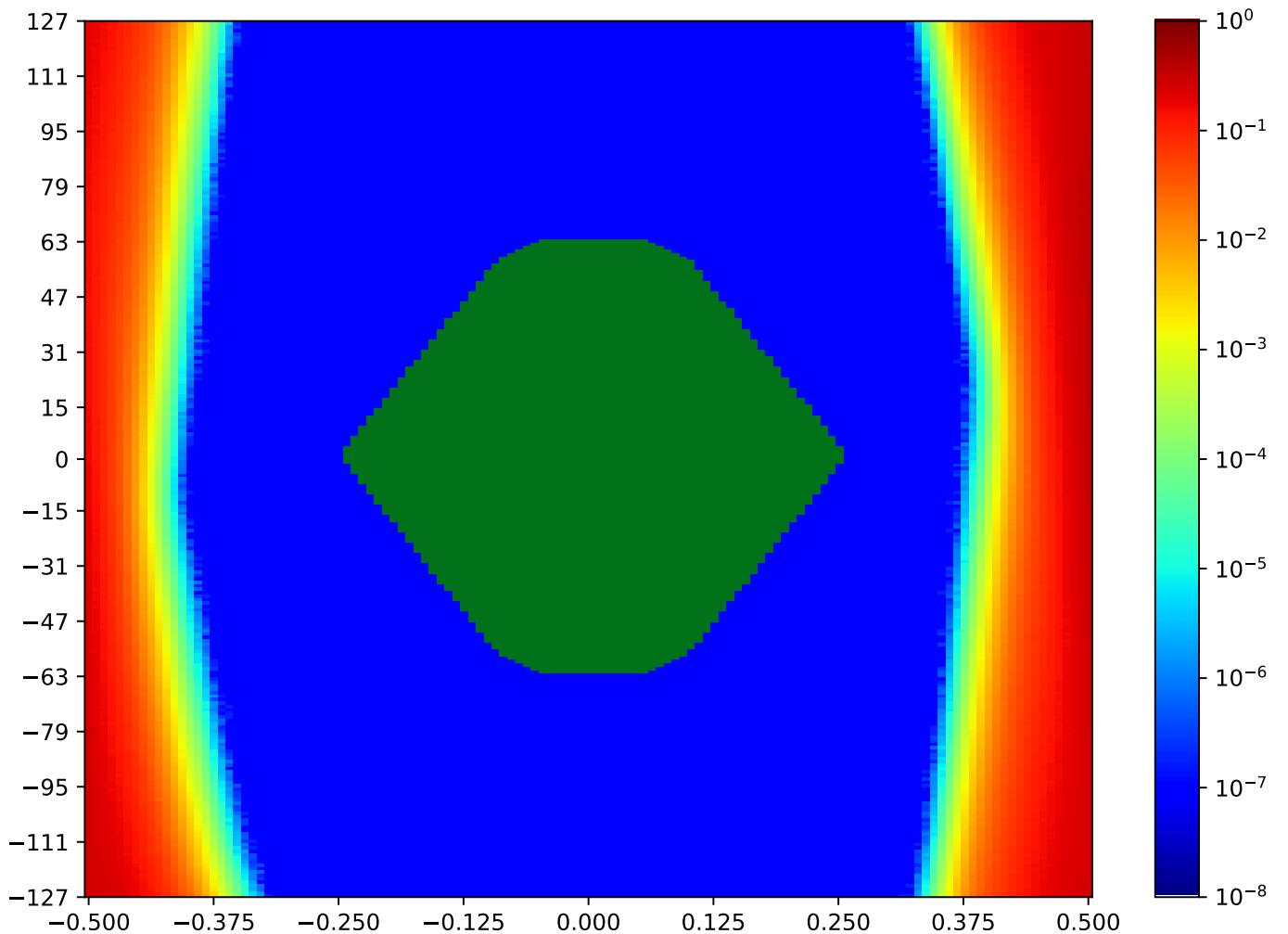


Figure 4.284: MSP_C_FPGA-TX4-04-RX4-04-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.6 MSP_C_FPGA-TX4-05-RX4-05-MSP_A_FPGA

Table 4.263: MSP_C_FPGA-TX4-05-RX4-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:56:49		2018-Sep-27 18:58:05	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24784	102		79.07%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

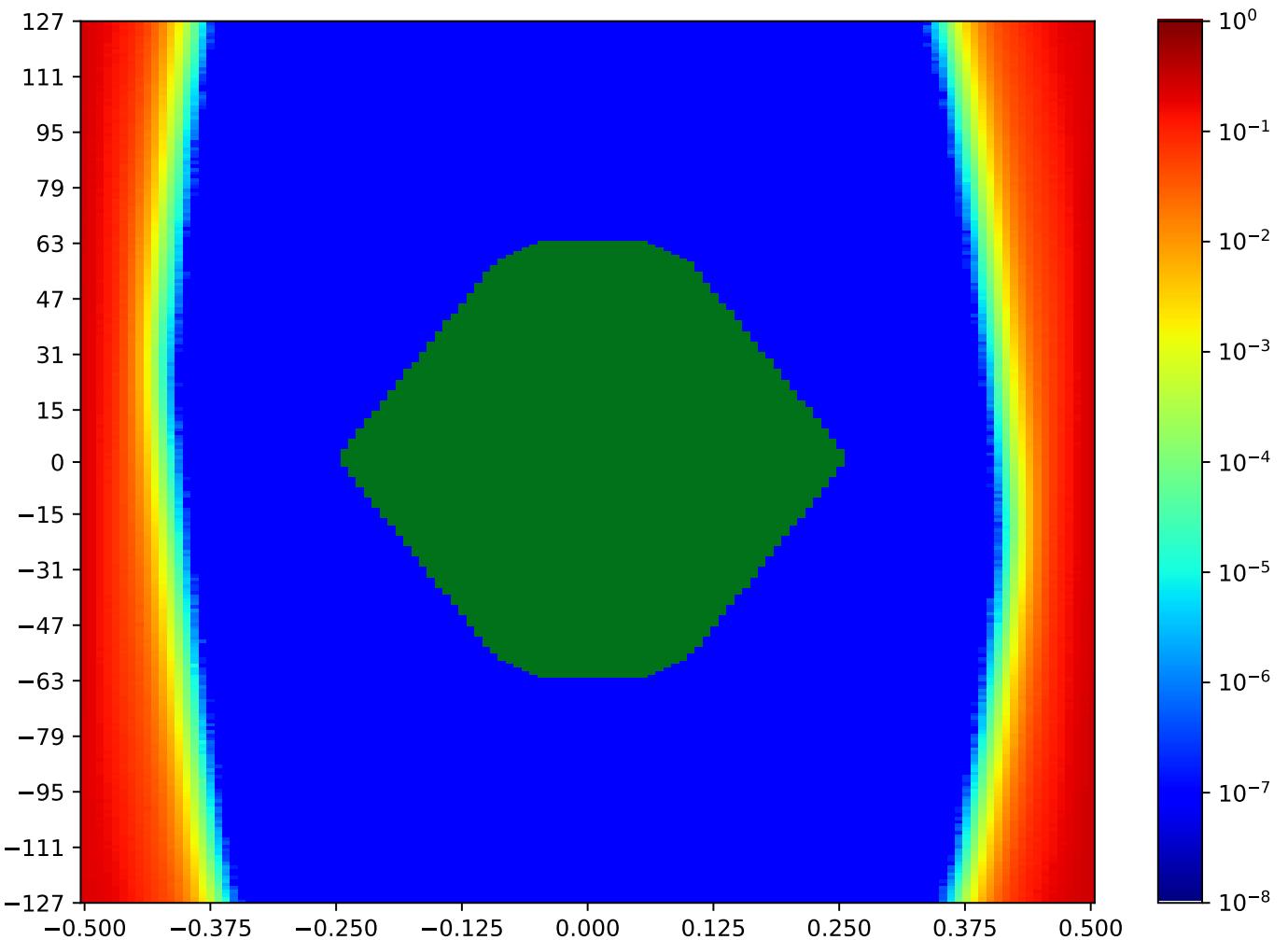


Figure 4.285: MSP_C_FPGA-TX4-05-RX4-05-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.7 MSP_C_FPGA-TX4-06-RX4-06-MSP_A_FPGA

Table 4.264: MSP_C_FPGA-TX4-06-RX4-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:08:08		2018-Sep-27 19:09:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	24107	100	77.52%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

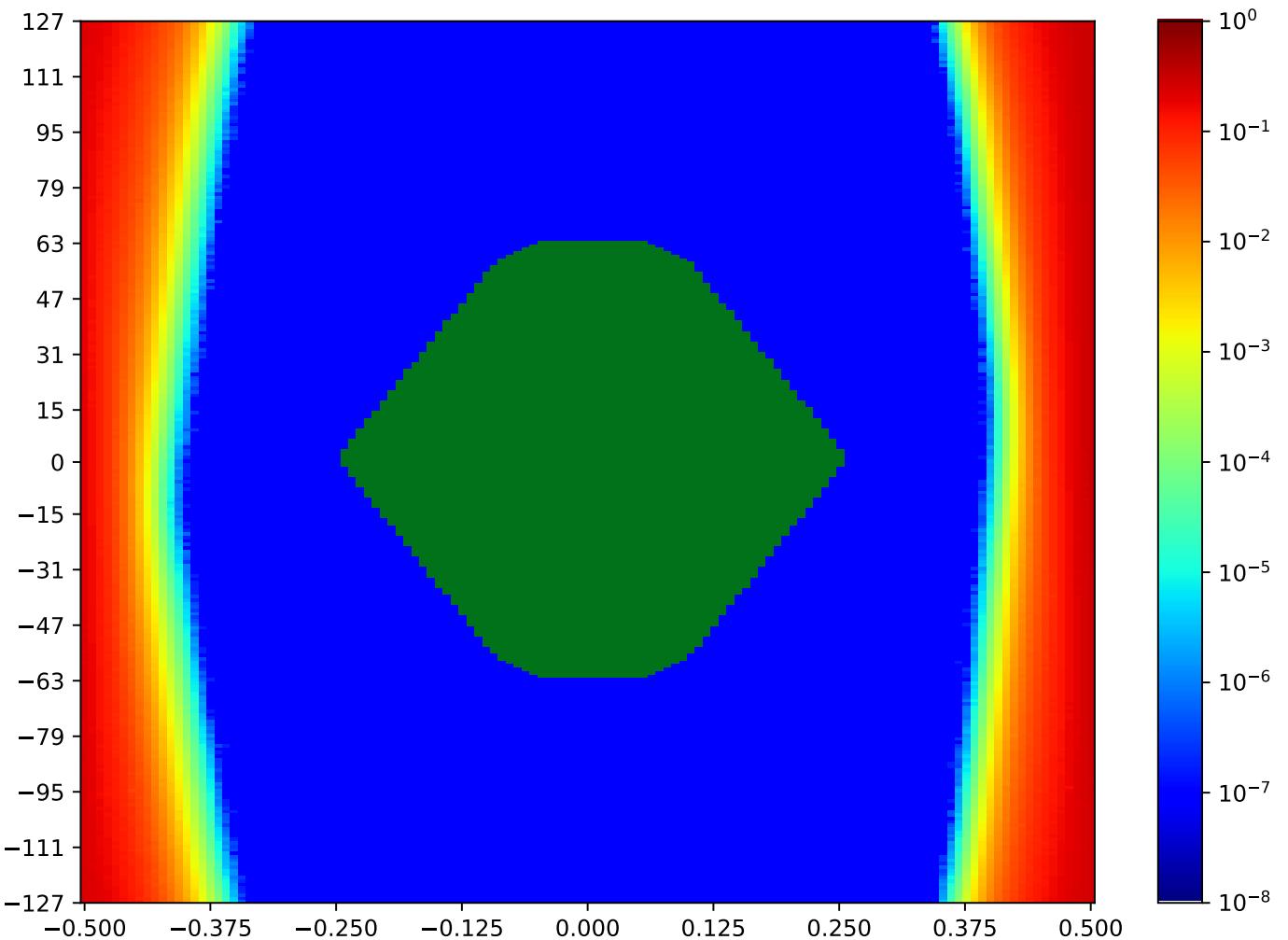


Figure 4.286: MSP_C_FPGA-TX4-06-RX4-06-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.8 MSP_C_FPGA-TX4-07-RX4-07-MSP_A_FPGA

Table 4.265: MSP_C_FPGA-TX4-07-RX4-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 18:59:21		2018-Sep-27 19:00:36	
Reset RX	OA	HO		VO	VO (%)
true	24772	102		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

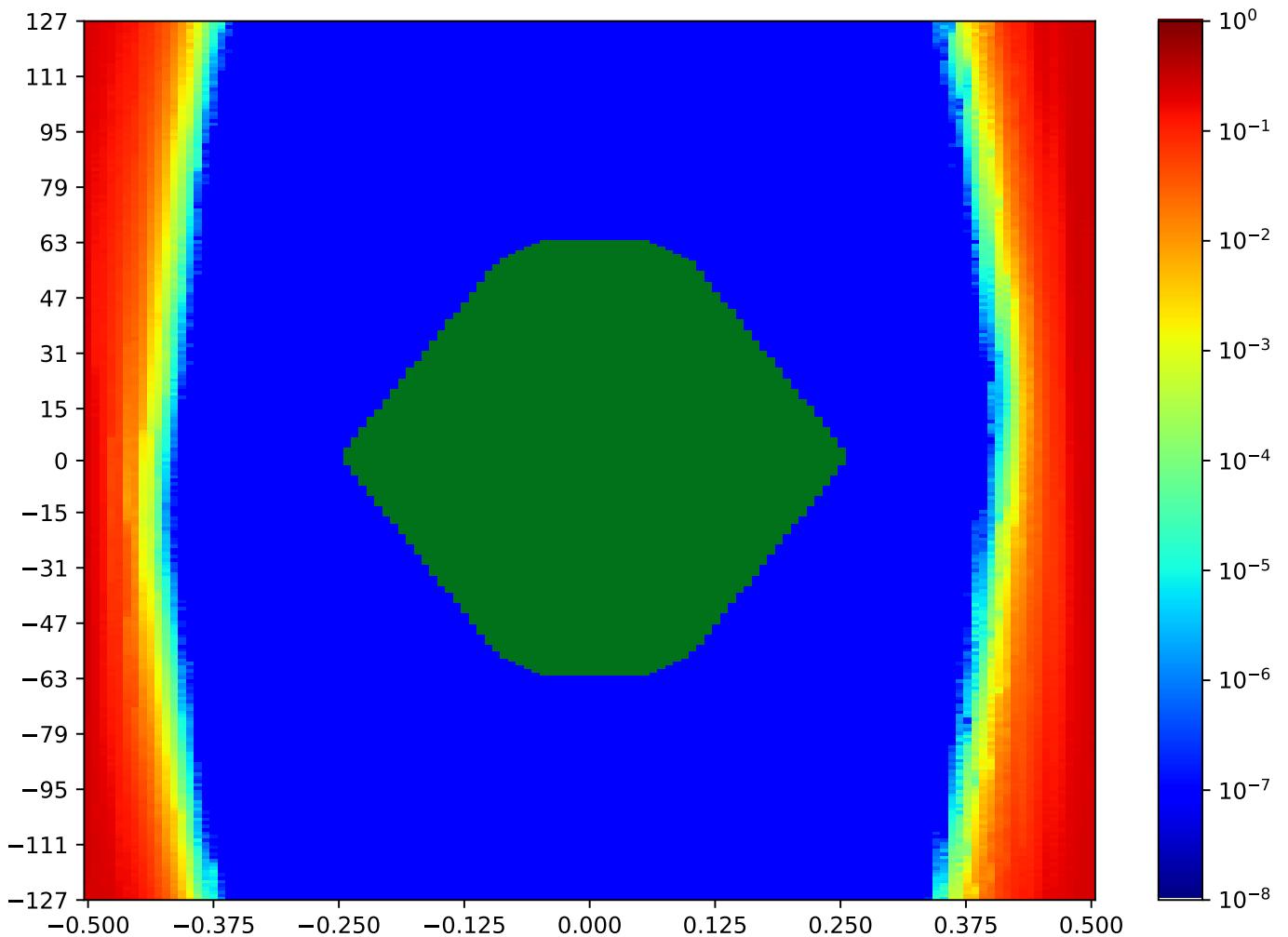


Figure 4.287: MSP_C_FPGA-TX4-07-RX4-07-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.9 MSP_C_FPGA-TX4-08-RX4-08-MSP_A_FPGA

Table 4.266: MSP_C_FPGA-TX4-08-RX4-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:06:53		2018-Sep-27 19:08:08	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	24423	101		78.29%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

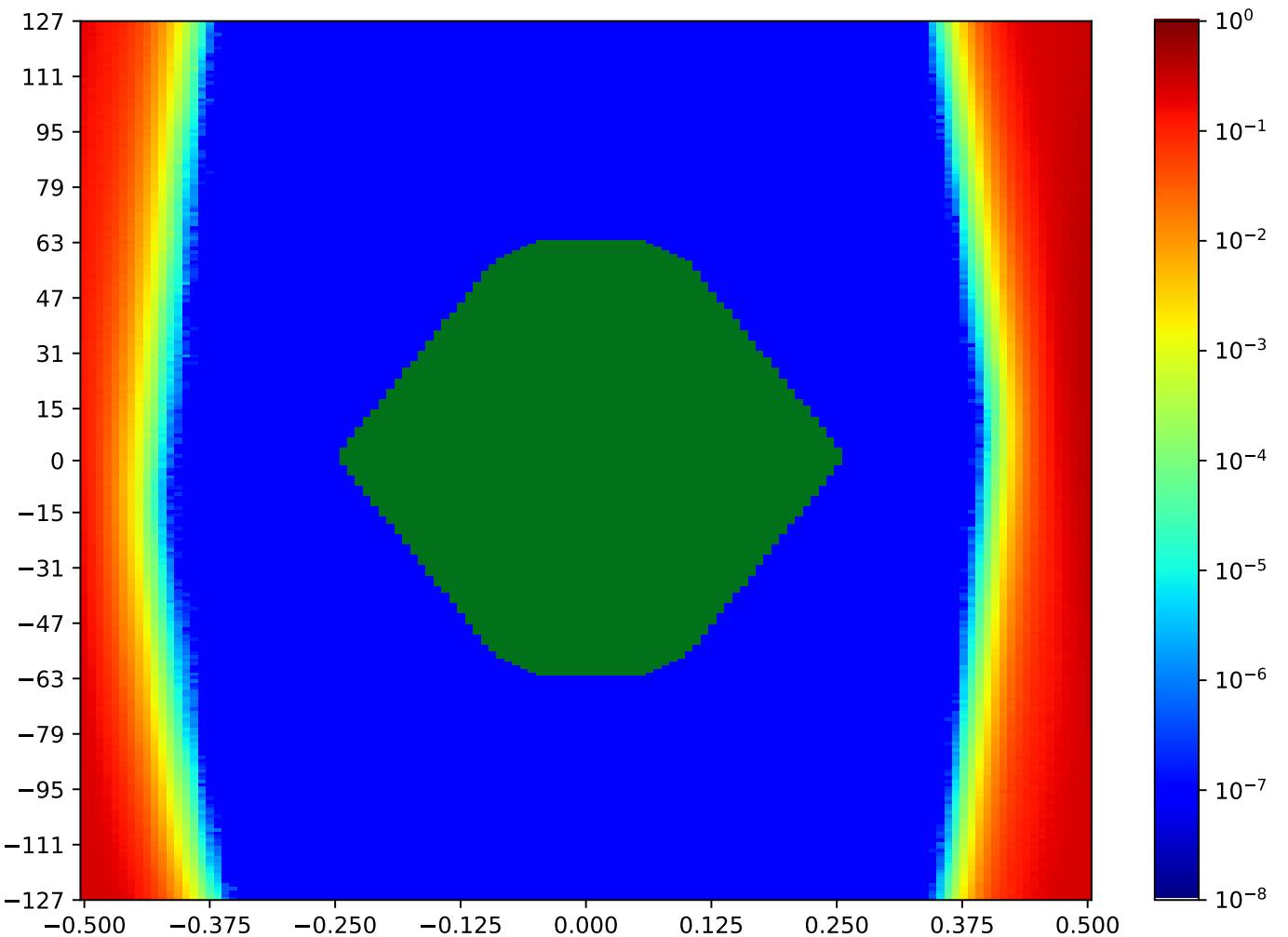


Figure 4.288: MSP_C_FPGA-TX4-08-RX4-08-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.10 MSP_C_FPGA-TX4-09-RX4-09-MSP_A_FPGA

Table 4.267: MSP_C_FPGA-TX4-09-RX4-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:00:37		2018-Sep-27 19:01:51	
Reset RX	OA	HO		VO	VO (%)
true	23984	100		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

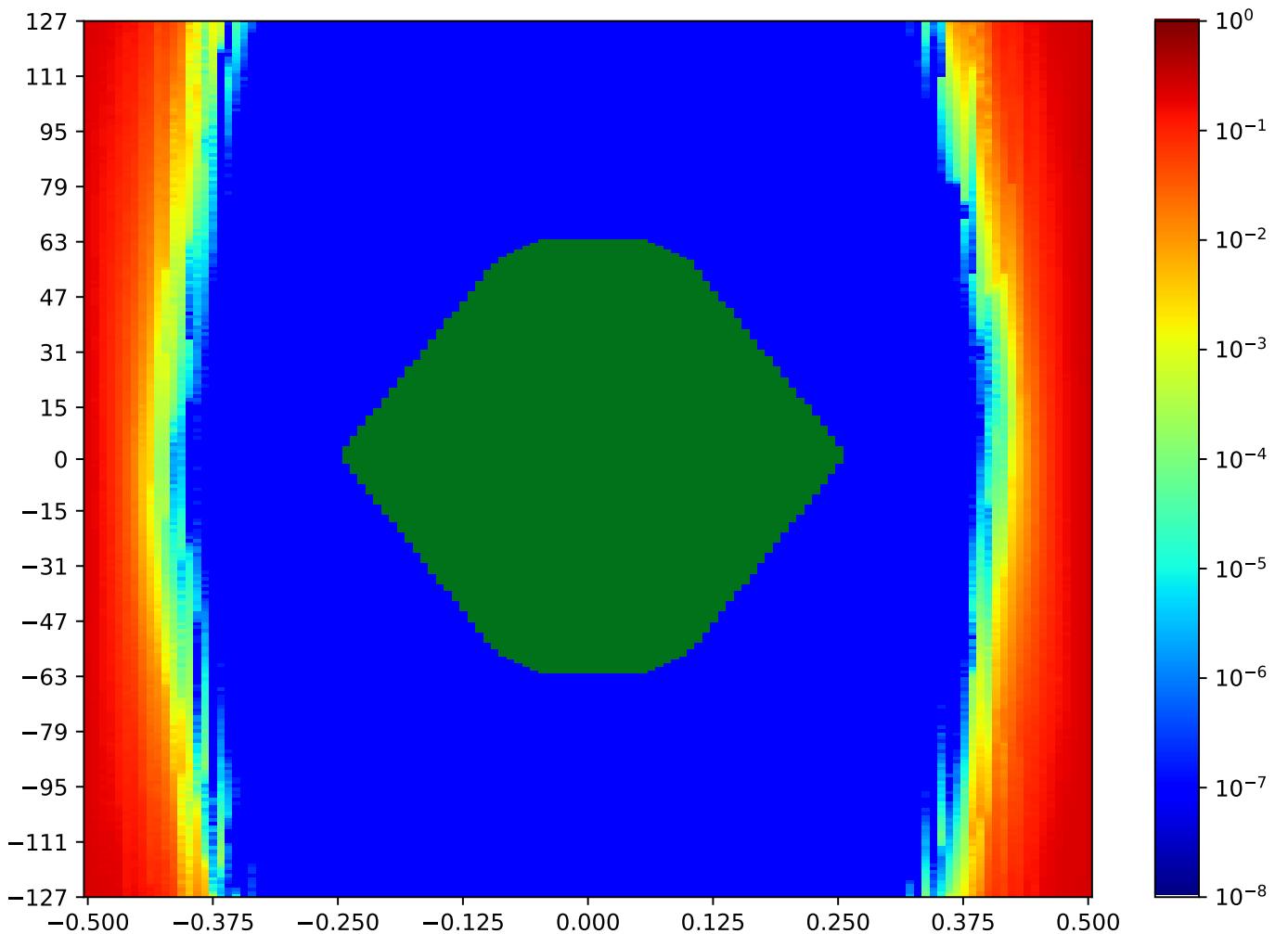


Figure 4.289: MSP_C_FPGA-TX4-09-RX4-09-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.11 MSP_C_FPGA-TX4-10-RX4-10-MSP_A_FPGA

Table 4.268: MSP_C_FPGA-TX4-10-RX4-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:04:22		2018-Sep-27 19:05:38	
Reset RX	OA	HO		VO	VO (%)
true	24618	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

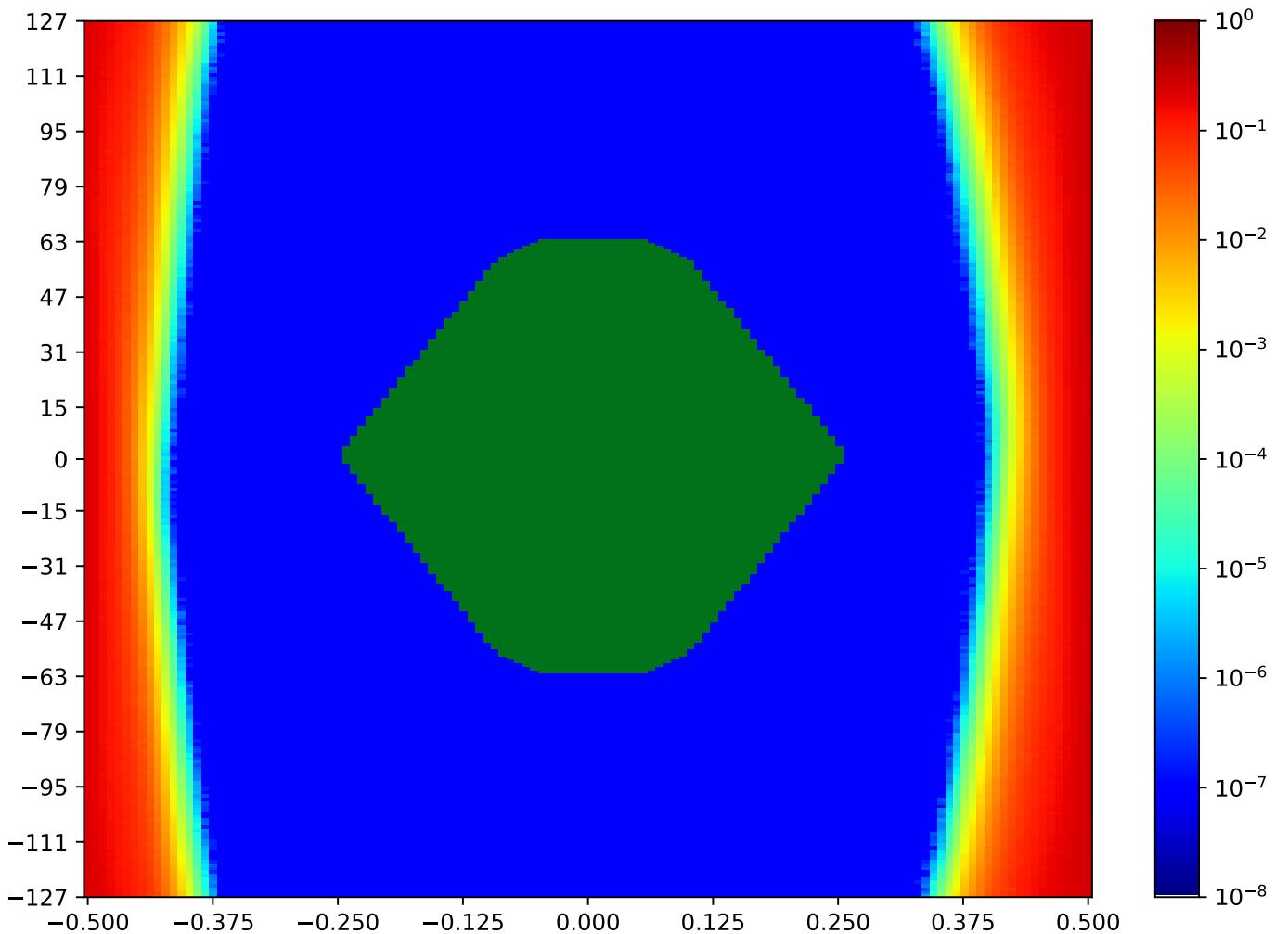


Figure 4.290: MSP_C_FPGA-TX4-10-RX4-10-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

4.22.12 MSP_C_FPGA-TX4-11-RX4-11-MSP_A_FPGA

Table 4.269: MSP_C_FPGA-TX4-11-RX4-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 19:03:07		2018-Sep-27 19:04:22	
Reset RX	OA	HO		VO	VO (%)
true	24829	103		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

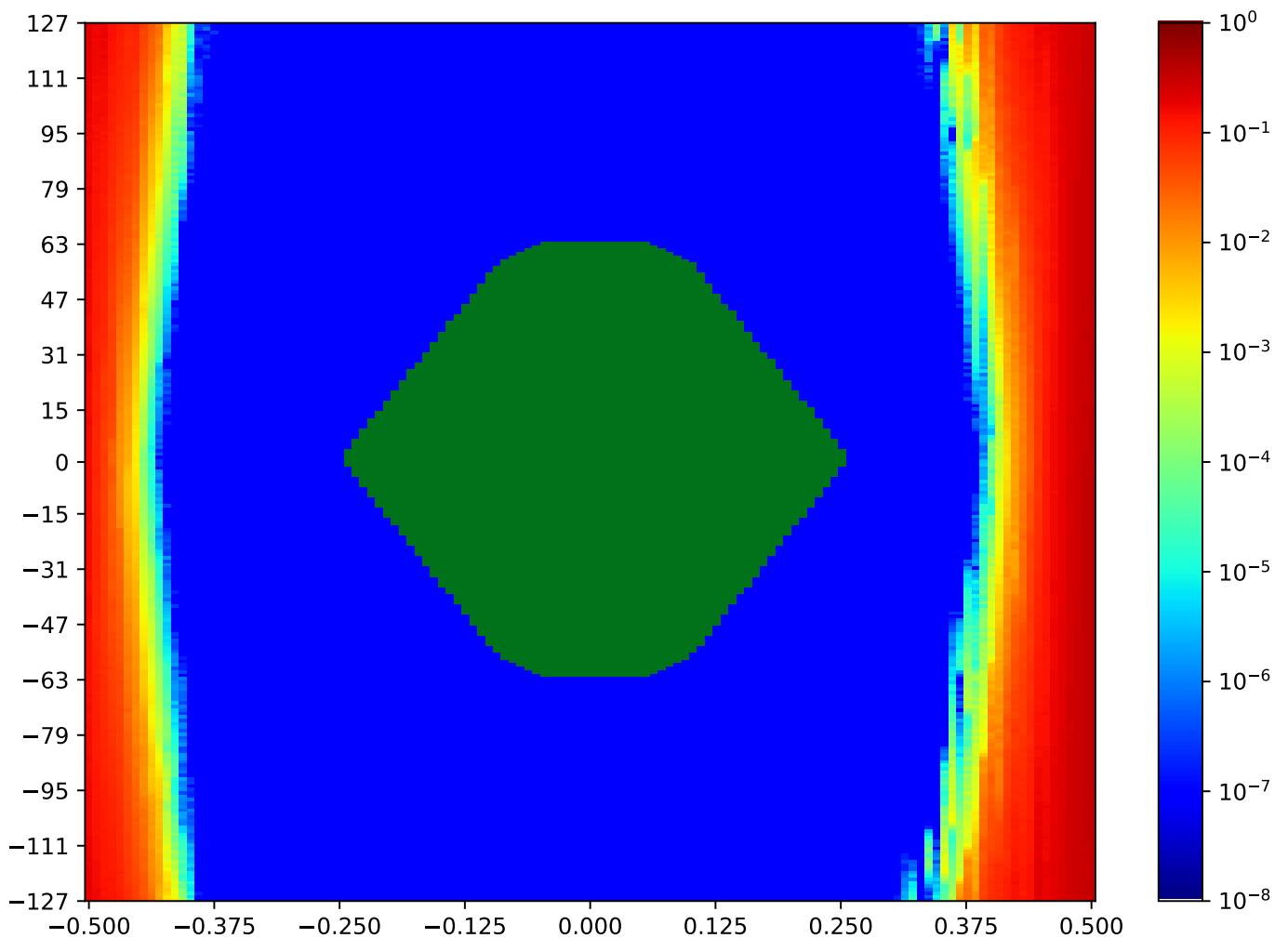


Figure 4.291: MSP_C_FPGA-TX4-11-RX4-11-MSP_A_FPGA

Call back to summary Figure 4.279. Sibling eye diagrams: V2-12.8.

Chapter 5

MUCTPI V2 12.8 Gbps

5.1 MSP_A TX1 MSP_C RX15 Minipod Loopback

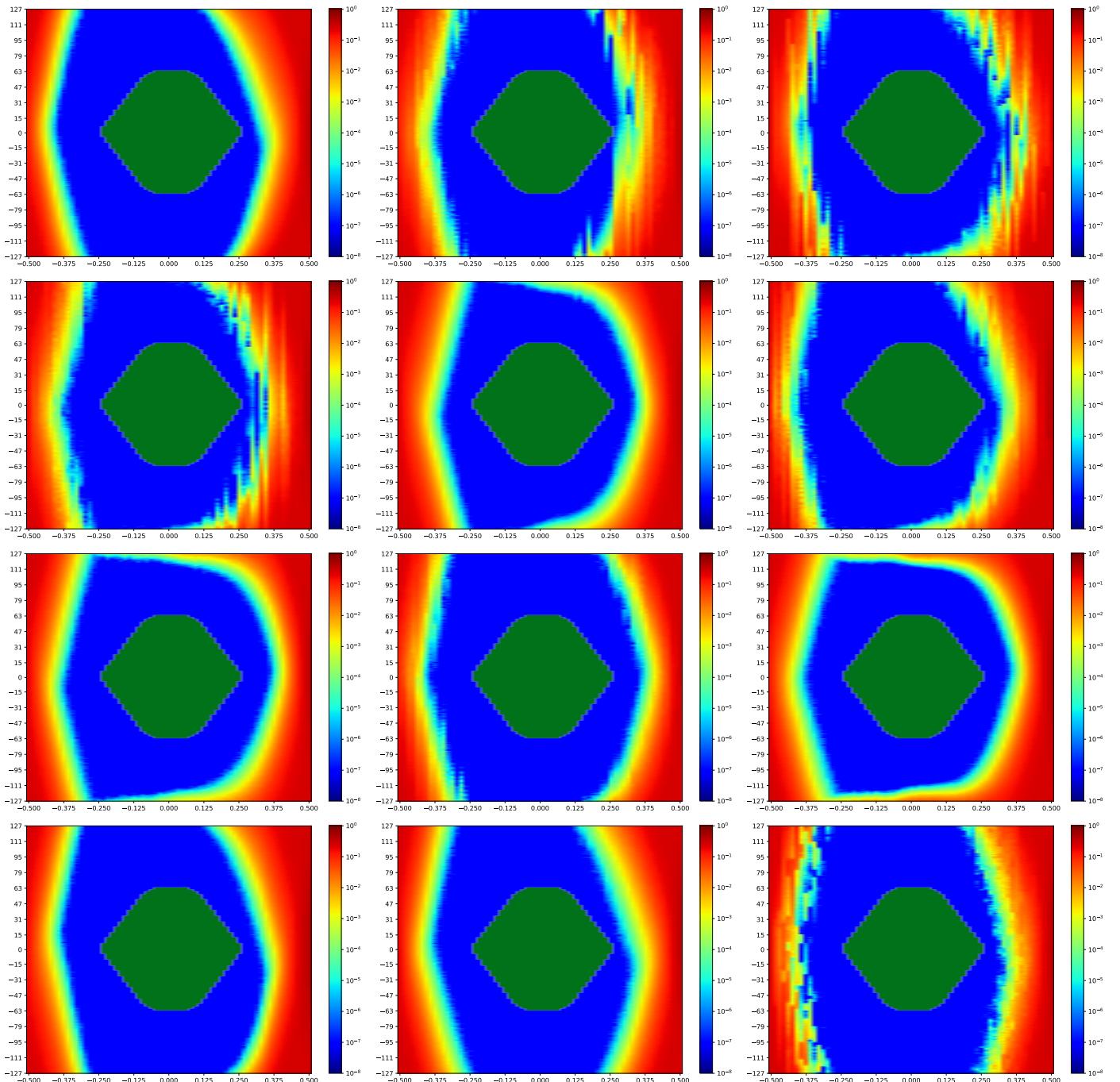


Figure 5.1: MSP_A TX1 MSP_C RX15 Minipod Loopback

A cross-reference to Figure 5.1. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.14.

5.1.1 MSP_A_FPGA-TX1-00-RX15-00-MSP_C_FPGA

Table 5.1: MSP_A_FPGA-TX1-00-RX15-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:45:40		2018-Sep-27 16:46:00	
Reset RX	OA	HO		VO	VO (%)
true	9522	44		67.69%	254 99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

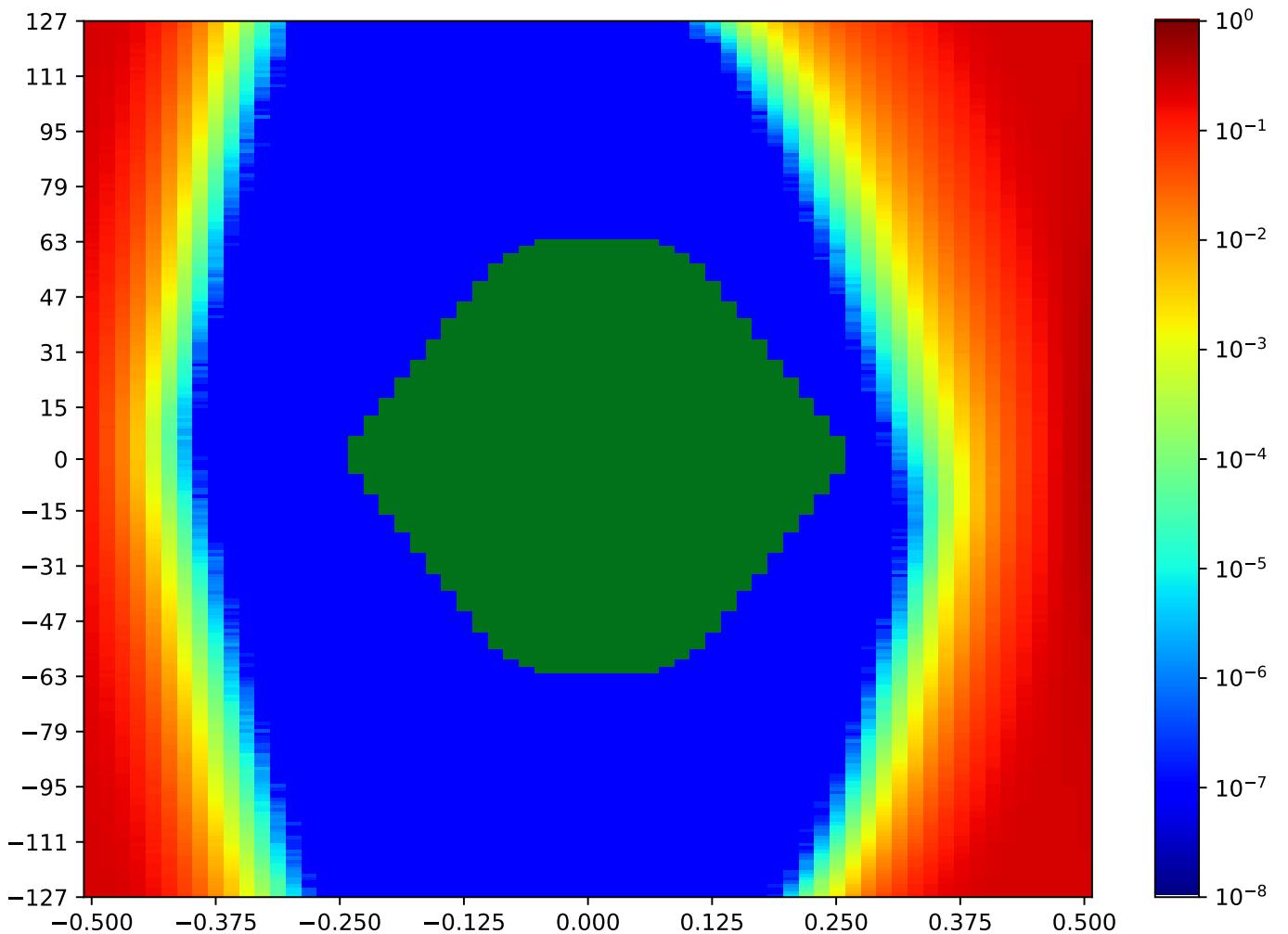


Figure 5.2: MSP_A_FPGA-TX1-00-RX15-00-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.2 MSP_A_FPGA-TX1-01-RX15-01-MSP_C_FPGA

Table 5.2: MSP_A_FPGA-TX1-01-RX15-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:46:21		2018-Sep-27 16:46:42	
Reset RX	OA	HO		VO	VO (%)
true	8715	39		60.00%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

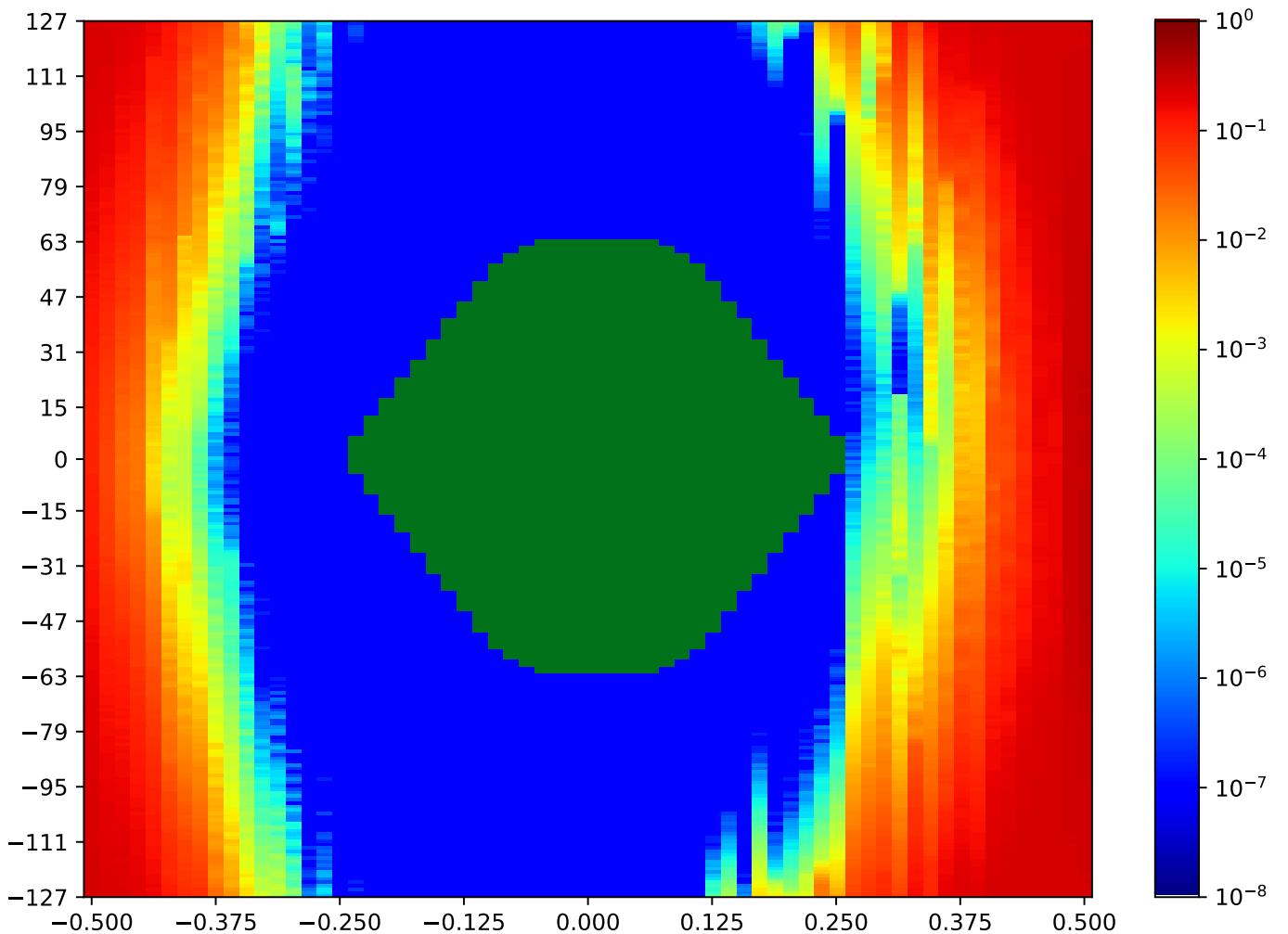


Figure 5.3: MSP_A_FPGA-TX1-01-RX15-01-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.3 MSP_A_FPGA-TX1-02-RX15-02-MSP_C_FPGA

Table 5.3: MSP_A_FPGA-TX1-02-RX15-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:46:42		2018-Sep-27 16:47:02	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8889	45		67.69%	248 97.25%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

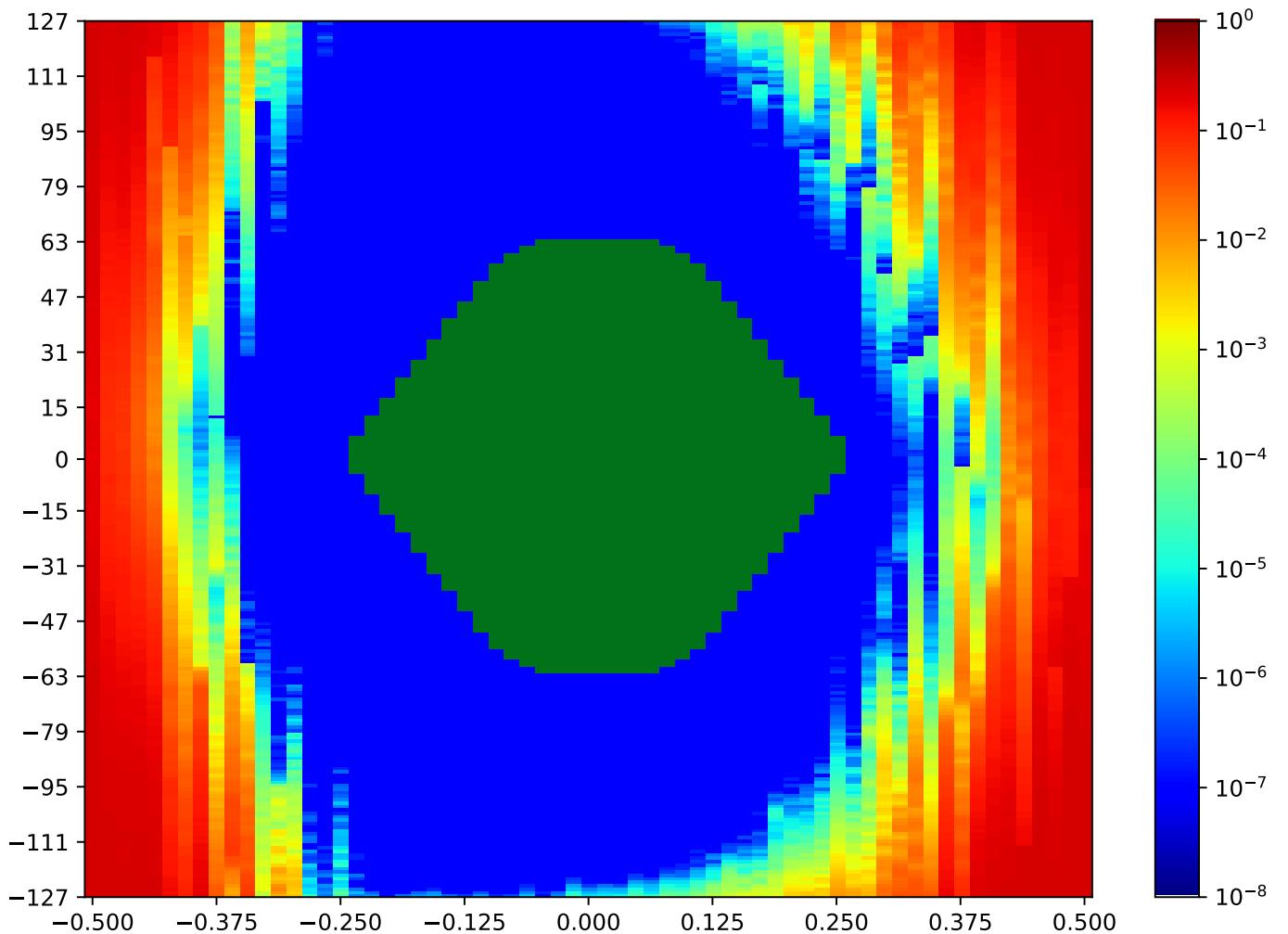


Figure 5.4: MSP_A_FPGA-TX1-02-RX15-02-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.4 MSP_A_FPGA-TX1-03-RX15-03-MSP_C_FPGA

Table 5.4: MSP_A_FPGA-TX1-03-RX15-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:45:00		2018-Sep-27 16:45:20	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8455	43		64.62%	250 96.08%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

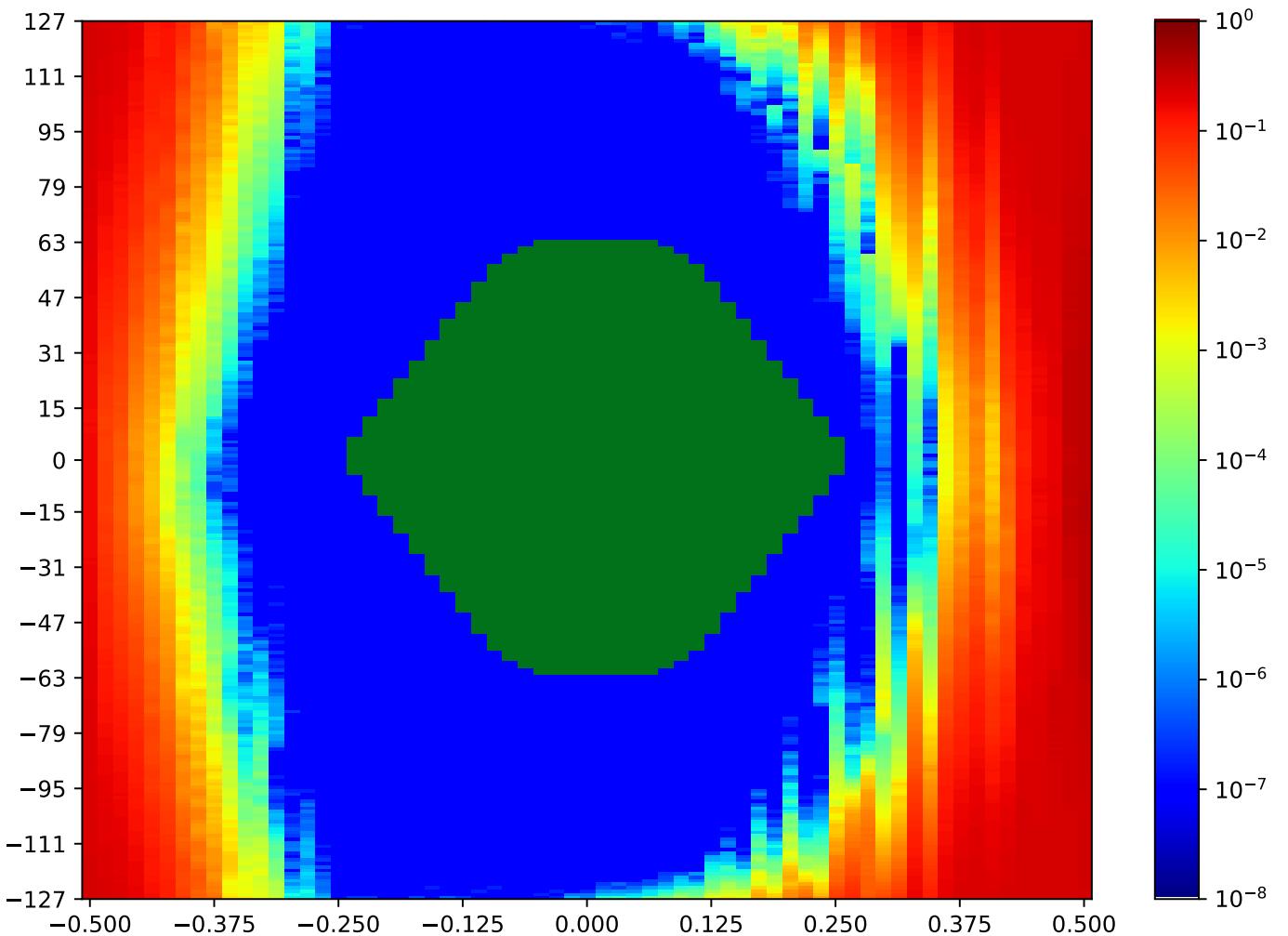


Figure 5.5: MSP_A_FPGA-TX1-03-RX15-03-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.5 MSP_A_FPGA-TX1-04-RX15-04-MSP_C_FPGA

Table 5.5: MSP_A_FPGA-TX1-04-RX15-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:50:17		2018-Sep-27 16:50:42	
Reset RX	OA	HO		VO	VO (%)
true	8054	42		233	91.37%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

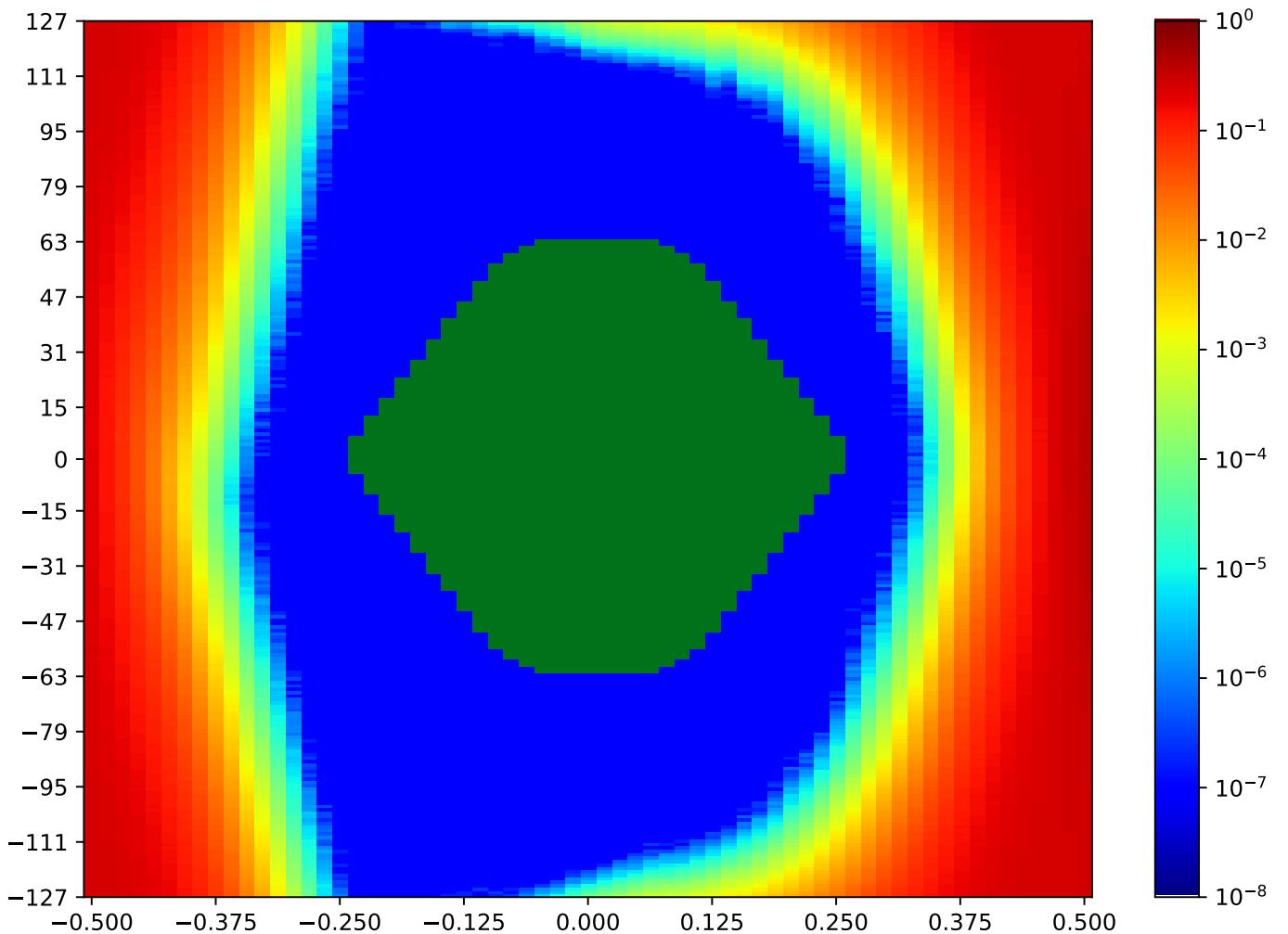


Figure 5.6: MSP_A_FPGA-TX1-04-RX15-04-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.6 MSP_A_FPGA-TX1-05-RX15-05-MSP_C_FPGA

Table 5.6: MSP_A_FPGA-TX1-05-RX15-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:44:40		2018-Sep-27 16:45:00	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8797	45		67.69%	248 97.25%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

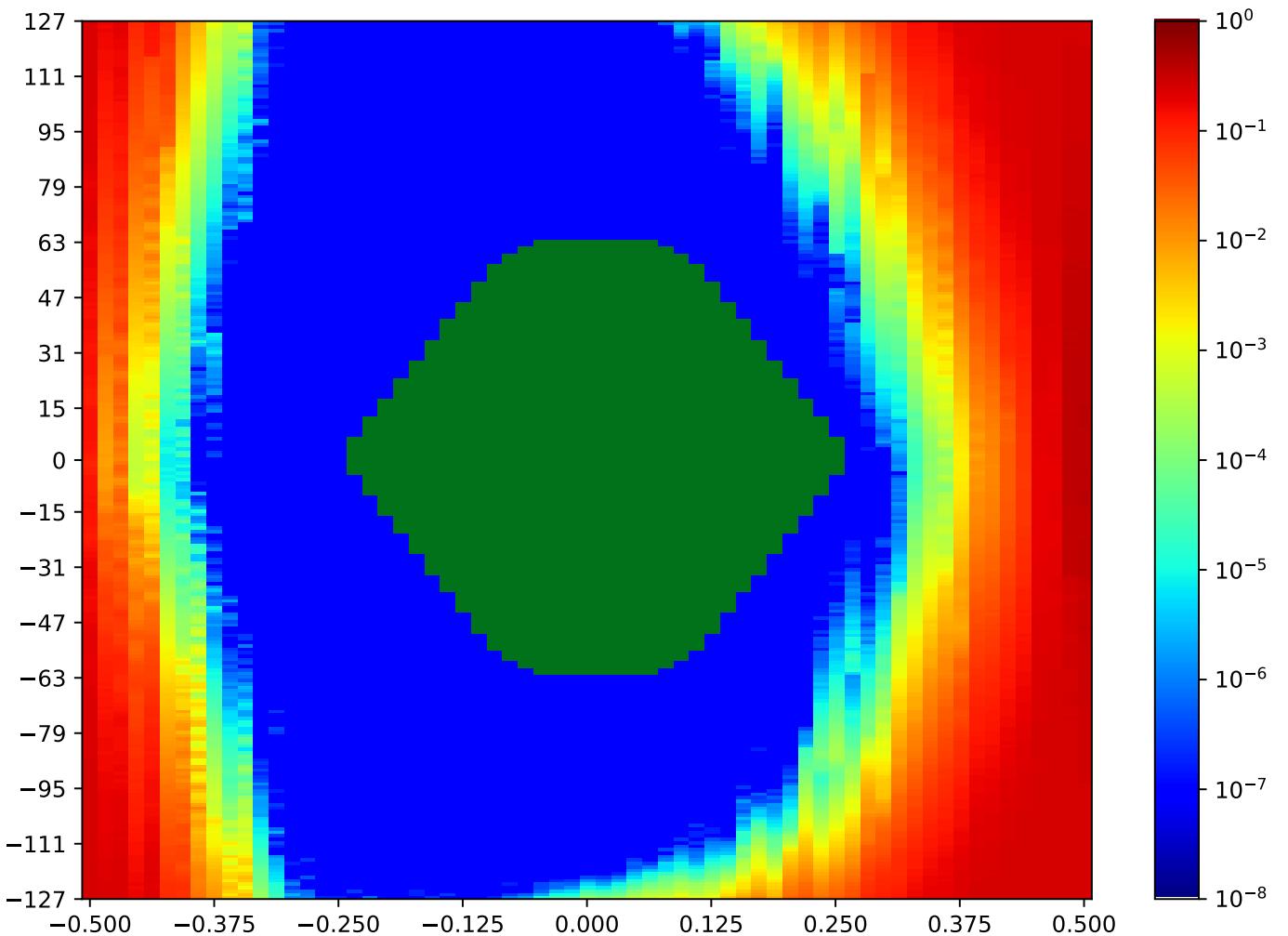


Figure 5.7: MSP_A_FPGA-TX1-05-RX15-05-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.7 MSP_A_FPGA-TX1-06-RX15-06-MSP_C_FPGA

Table 5.7: MSP_A_FPGA-TX1-06-RX15-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:52:20		2018-Sep-27 16:54:00	
Reset RX	OA	HO		VO	VO (%)
true	8657	45		230	90.20%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

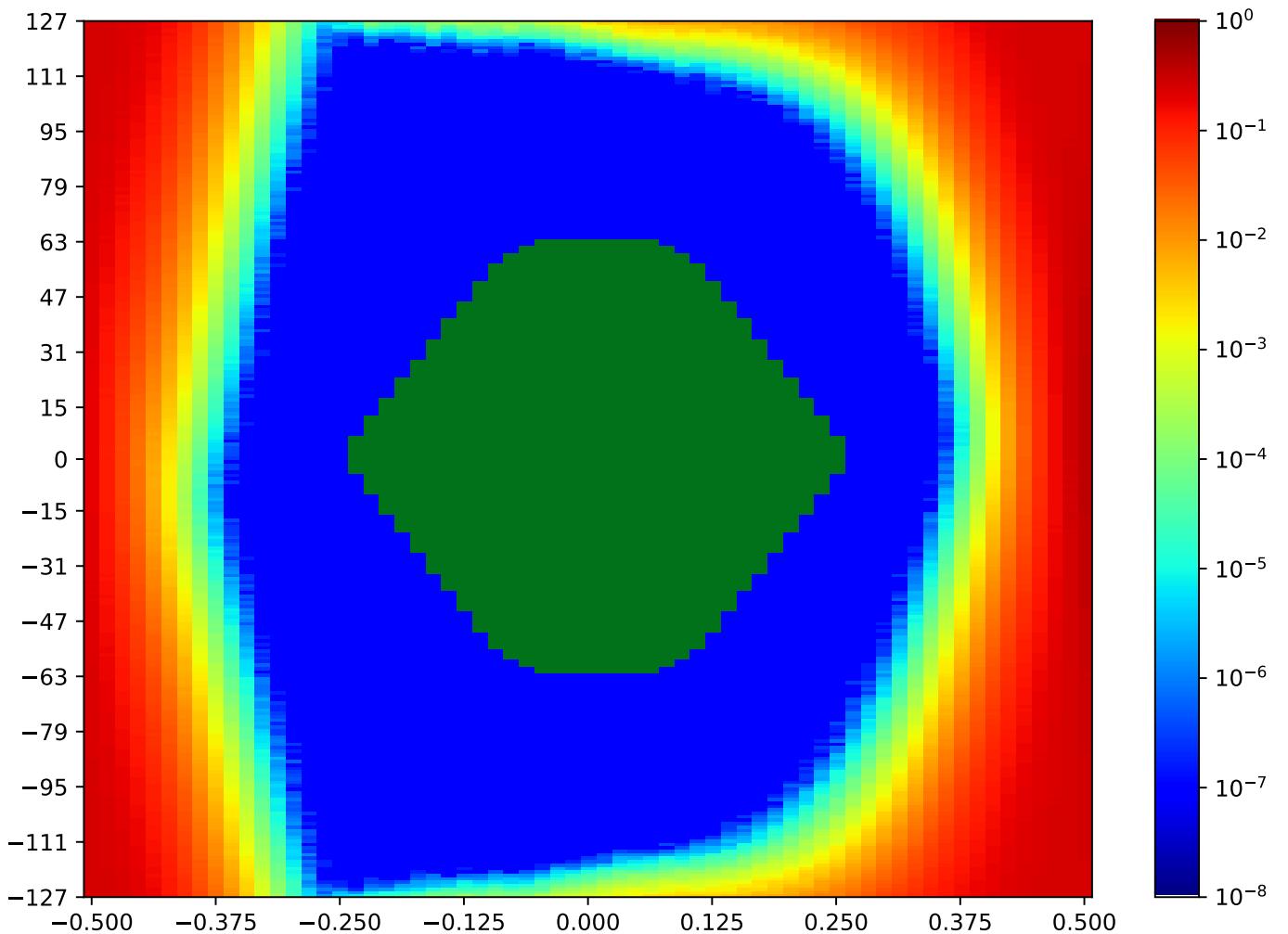


Figure 5.8: MSP_A_FPGA-TX1-06-RX15-06-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.8 MSP_A_FPGA-TX1-07-RX15-07-MSP_C_FPGA

Table 5.8: MSP_A_FPGA-TX1-07-RX15-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:45:20		2018-Sep-27 16:45:40	
Reset RX	OA	HO		VO	VO (%)
true	9890	47		72.31%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

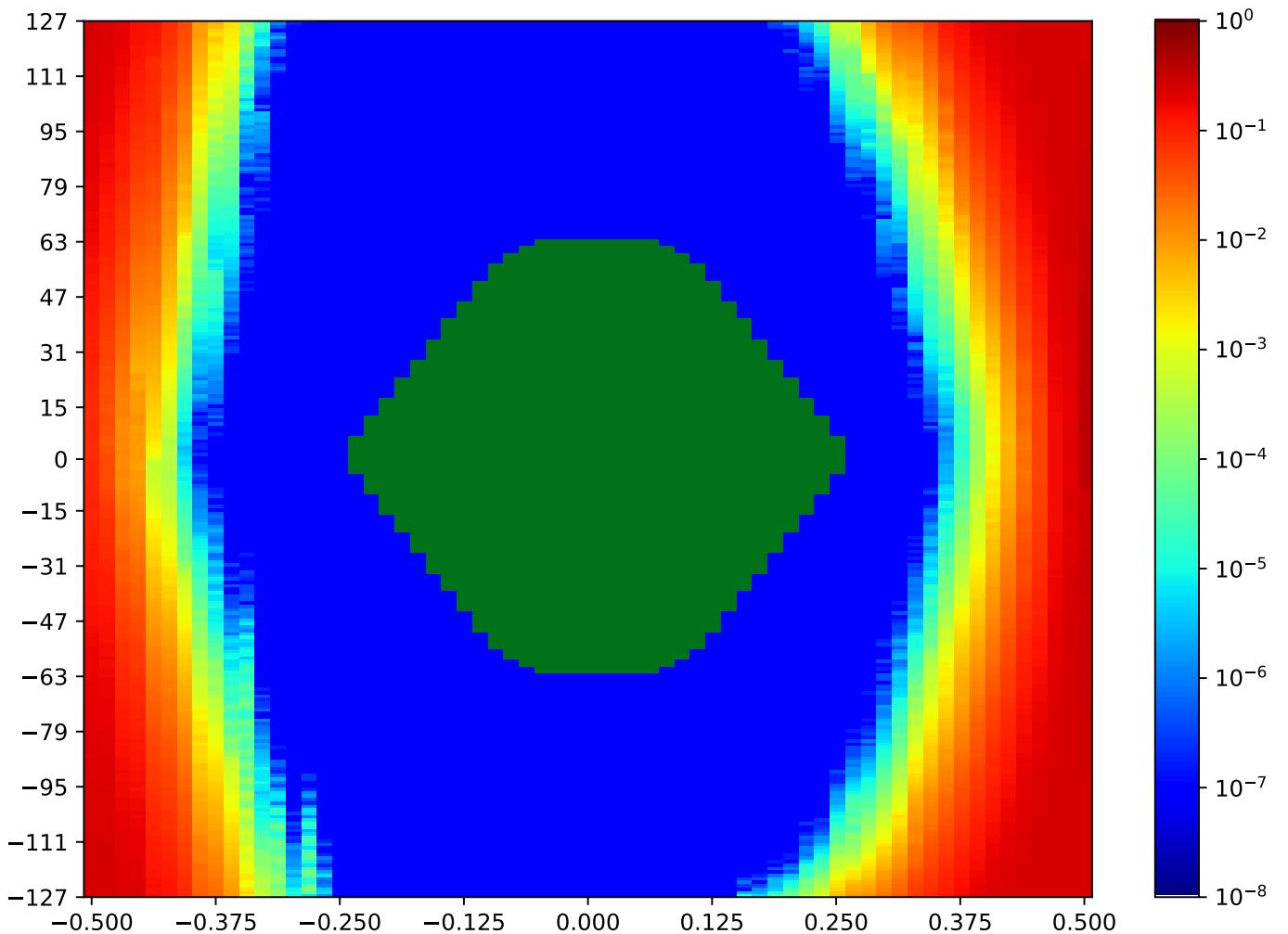


Figure 5.9: MSP_A_FPGA-TX1-07-RX15-07-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.9 MSP_A_FPGA-TX1-08-RX15-08-MSP_C_FPGA

Table 5.9: MSP_A_FPGA-TX1-08-RX15-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:50:42		2018-Sep-27 16:52:20	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8269	45		69.23%	223 87.06%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

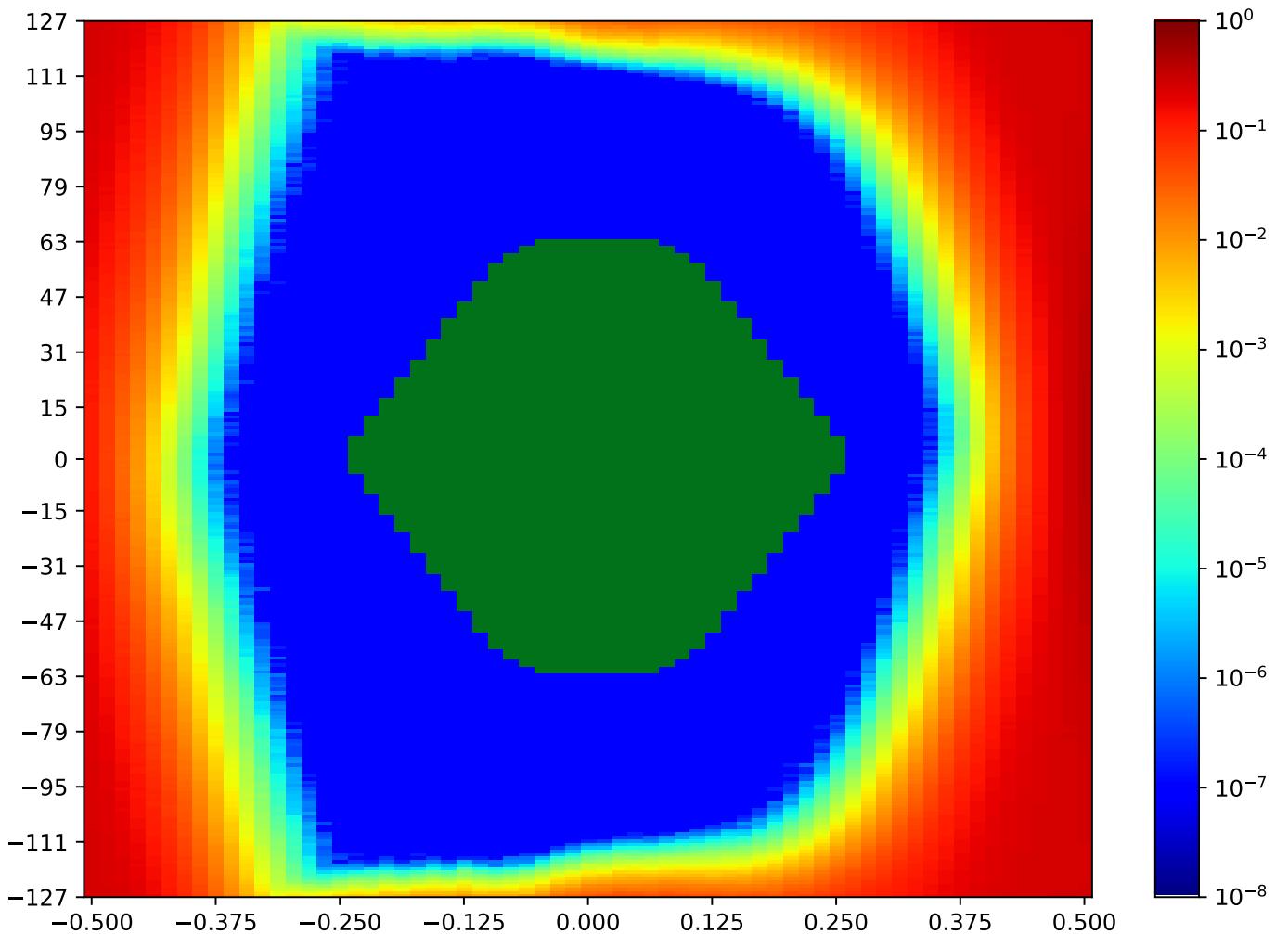


Figure 5.10: MSP_A_FPGA-TX1-08-RX15-08-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.10 MSP_A_FPGA-TX1-09-RX15-09-MSP_C_FPGA

Table 5.10: MSP_A_FPGA-TX1-09-RX15-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:46:01		2018-Sep-27 16:46:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9565	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

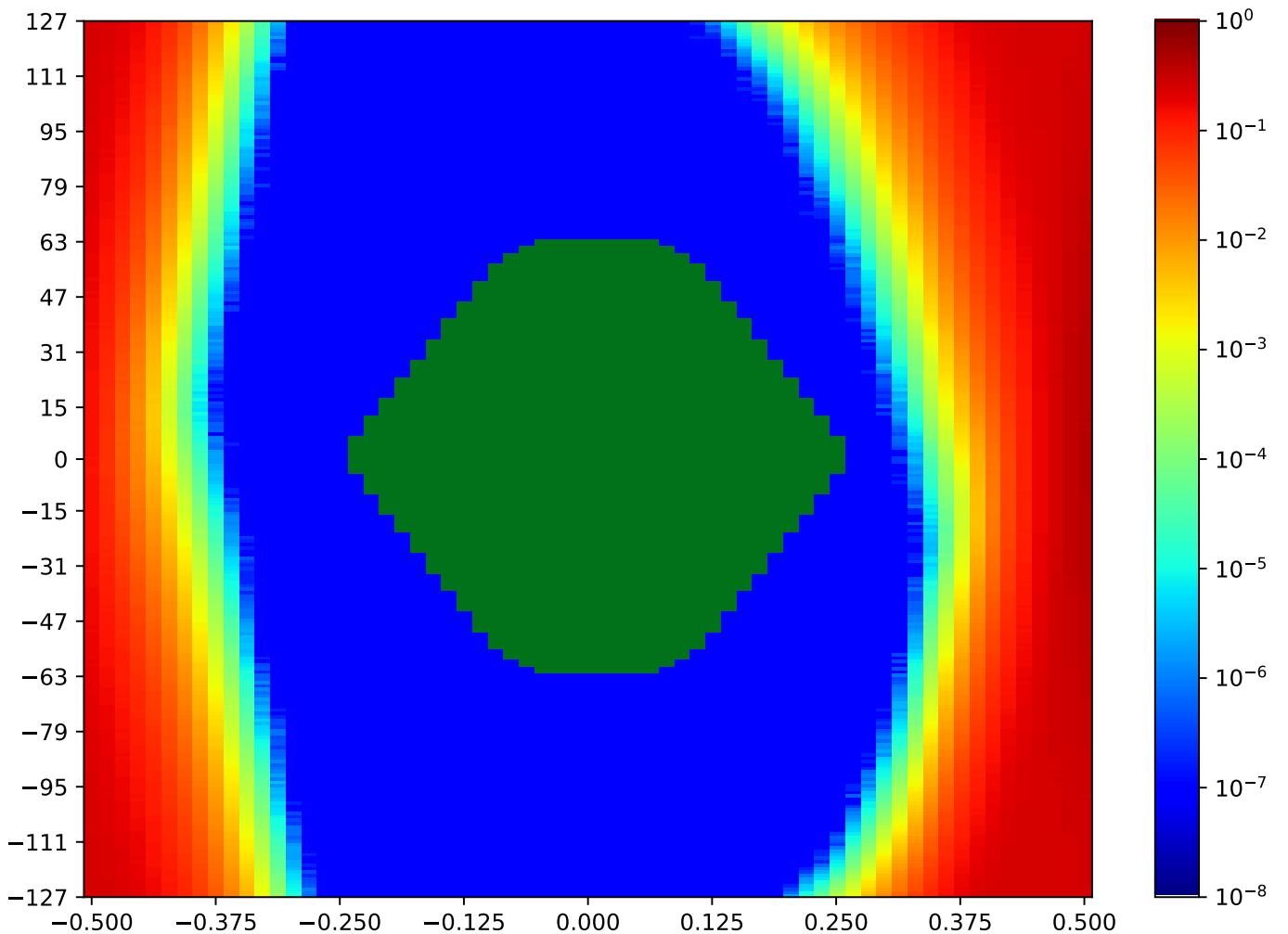


Figure 5.11: MSP_A_FPGA-TX1-09-RX15-09-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.11 MSP_A_FPGA-TX1-10-RX15-10-MSP_C_FPGA

Table 5.11: MSP_A_FPGA-TX1-10-RX15-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:48:38		2018-Sep-27 16:50:17	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8860	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

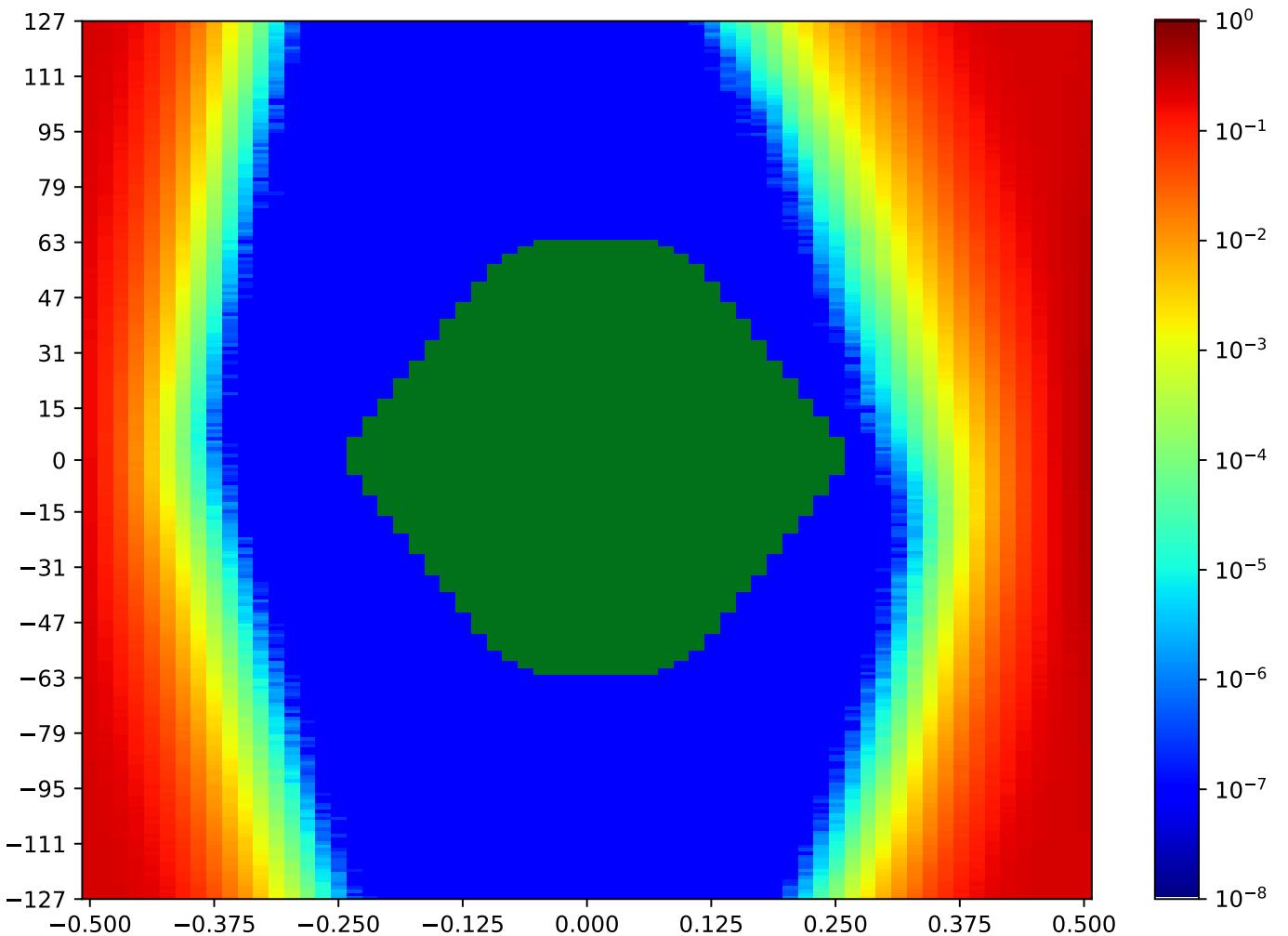


Figure 5.12: MSP_A_FPGA-TX1-10-RX15-10-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.1.12 MSP_A_FPGA-TX1-11-RX15-11-MSP_C_FPGA

Table 5.12: MSP_A_FPGA-TX1-11-RX15-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:47:02		2018-Sep-27 16:48:38	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9683	45		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

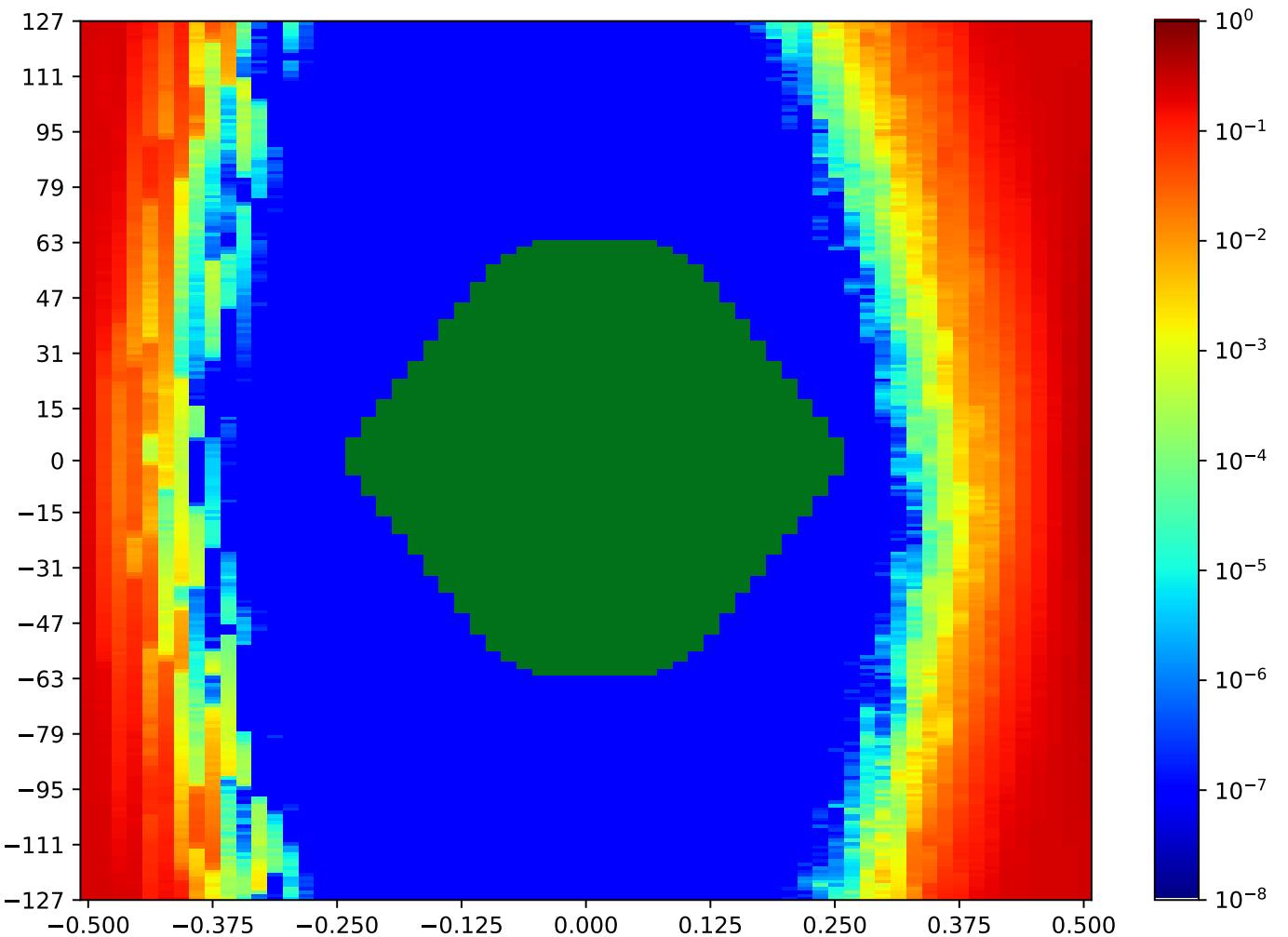


Figure 5.13: MSP_A_FPGA-TX1-11-RX15-11-MSP_C_FPGA

Call back to summary Figure 5.1. Sibling eye diagrams: V2-6.4.

5.2 MSP_A TX2 MSP_C RX16 Minipod Loopback

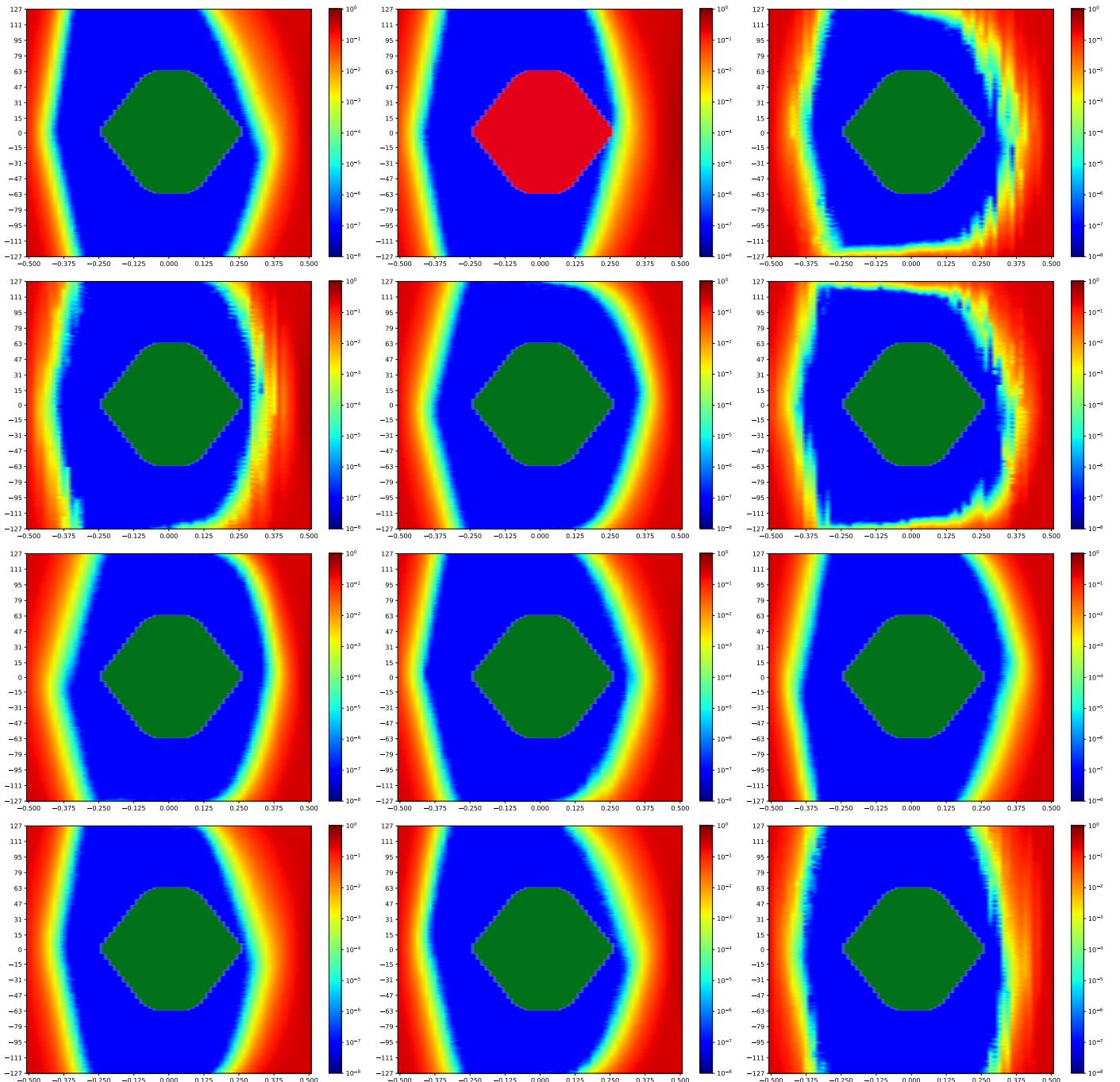


Figure 5.14: MSP_A TX2 MSP_C RX16 Minipod Loopback

A cross-reference to Figure 5.14. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.27.

5.2.1 MSP_A_FPGA-TX2-00-RX16-00-MSP_C_FPGA

Table 5.13: MSP_A_FPGA-TX2-00-RX16-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:55:00		2018-Sep-27 16:55:20	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9494	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

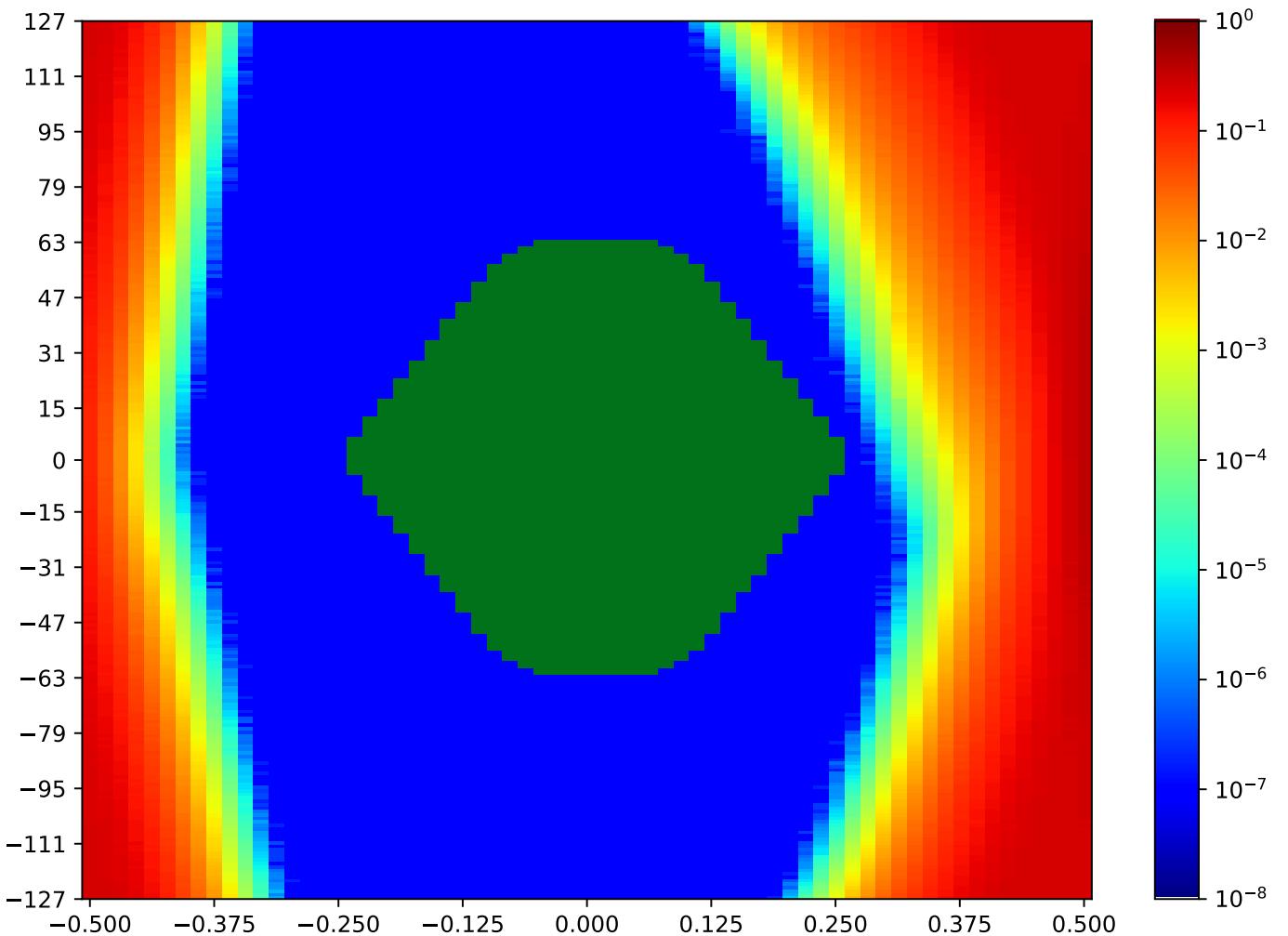


Figure 5.15: MSP_A_FPGA-TX2-00-RX16-00-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.2 MSP_A_FPGA-TX2-01-RX16-01-MSP_C_FPGA

Table 5.14: MSP_A_FPGA-TX2-01-RX16-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:54:20		2018-Sep-27 16:54:40	
Reset RX	OA	HO		VO	VO (%)
true	9026	41		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

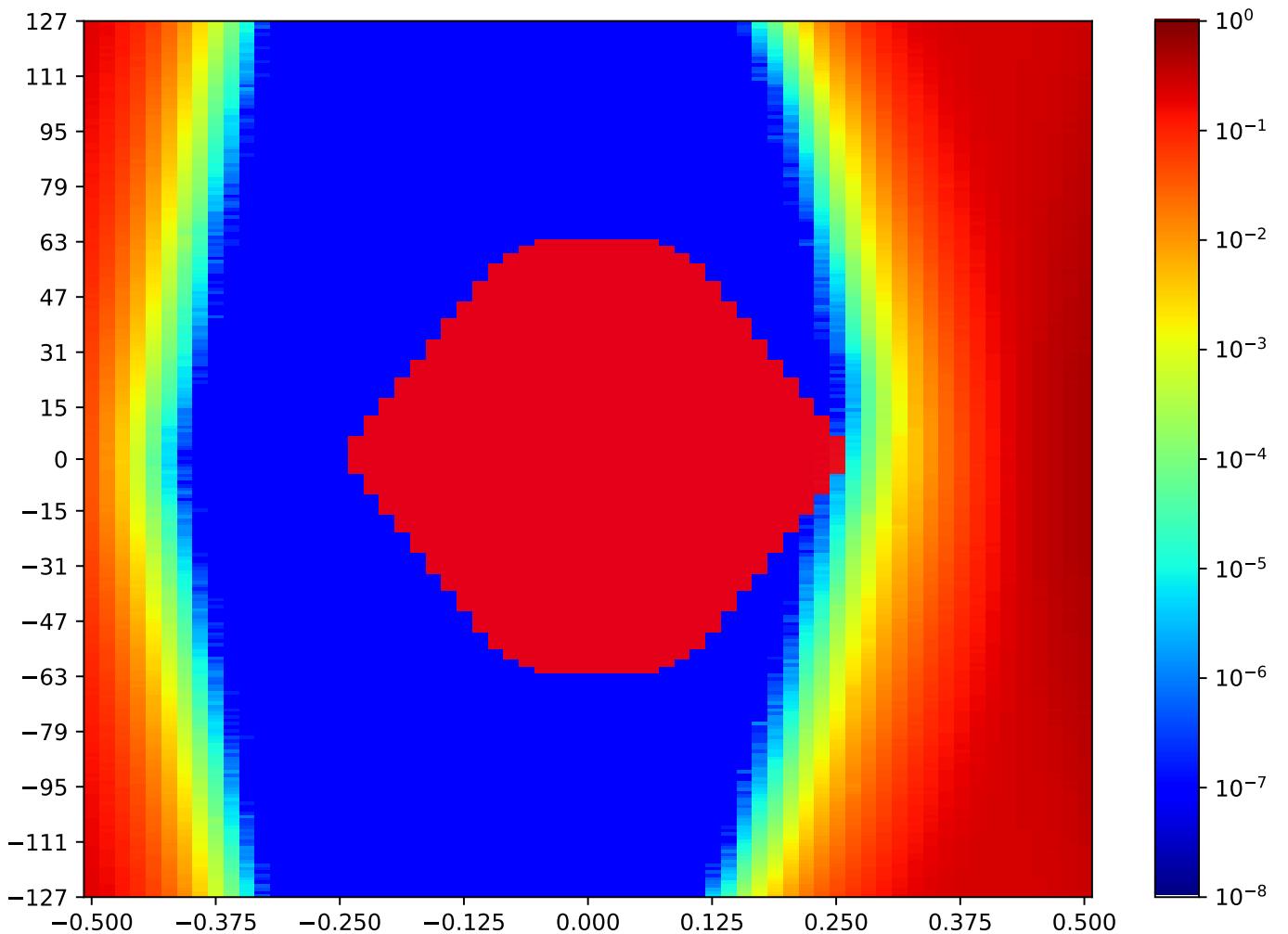


Figure 5.16: MSP_A_FPGA-TX2-01-RX16-01-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.3 MSP_A_FPGA-TX2-02-RX16-02-MSP_C_FPGA

Table 5.15: MSP_A_FPGA-TX2-02-RX16-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:56:06		2018-Sep-27 16:56:26	
Reset RX	OA	HO		VO	VO (%)
true	8198	42		229	89.41%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

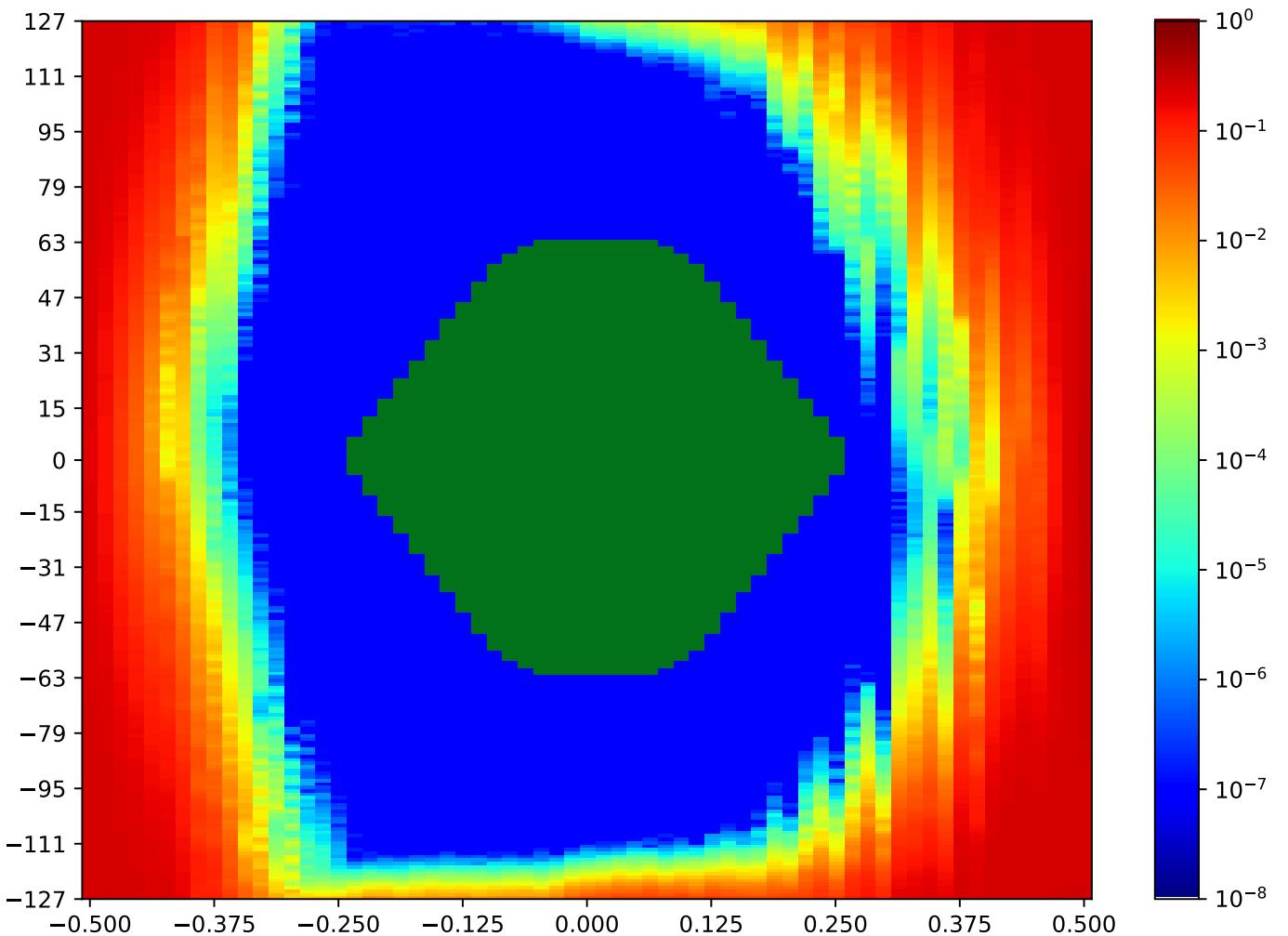


Figure 5.17: MSP_A_FPGA-TX2-02-RX16-02-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.4 MSP_A_FPGA-TX2-03-RX16-03-MSP_C_FPGA

Table 5.16: MSP_A_FPGA-TX2-03-RX16-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:54:00		2018-Sep-27 16:54:20	
Reset RX	OA	HO		VO	VO (%)
true	9223	43		66.15%	253 98.04%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

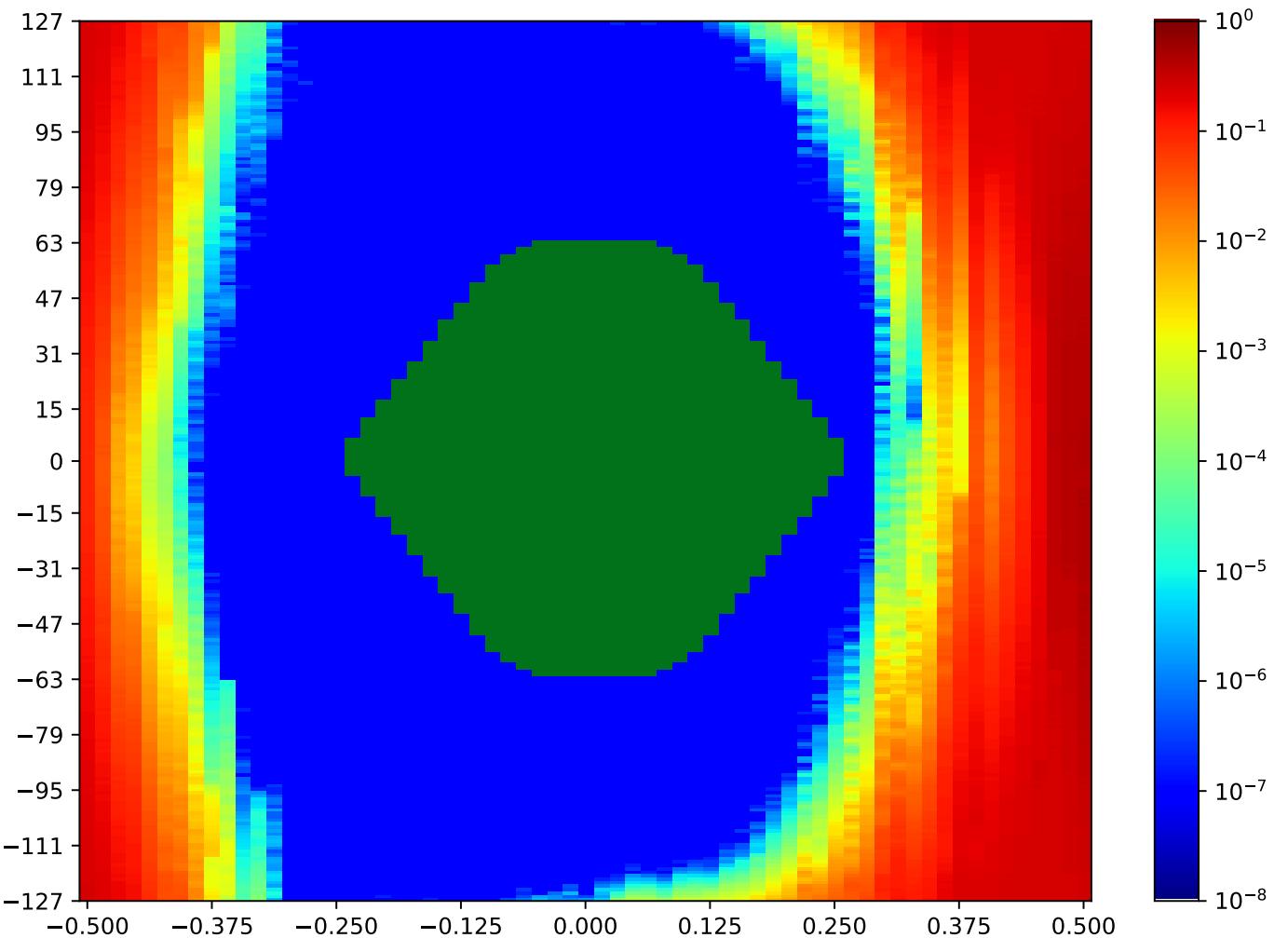


Figure 5.18: MSP_A_FPGA-TX2-03-RX16-03-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.5 MSP_A_FPGA-TX2-04-RX16-04-MSP_C_FPGA

Table 5.17: MSP_A_FPGA-TX2-04-RX16-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:57:07		2018-Sep-27 16:57:27	
Reset RX	OA	HO		VO	VO (%)
true	9086	44		251	96.86%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

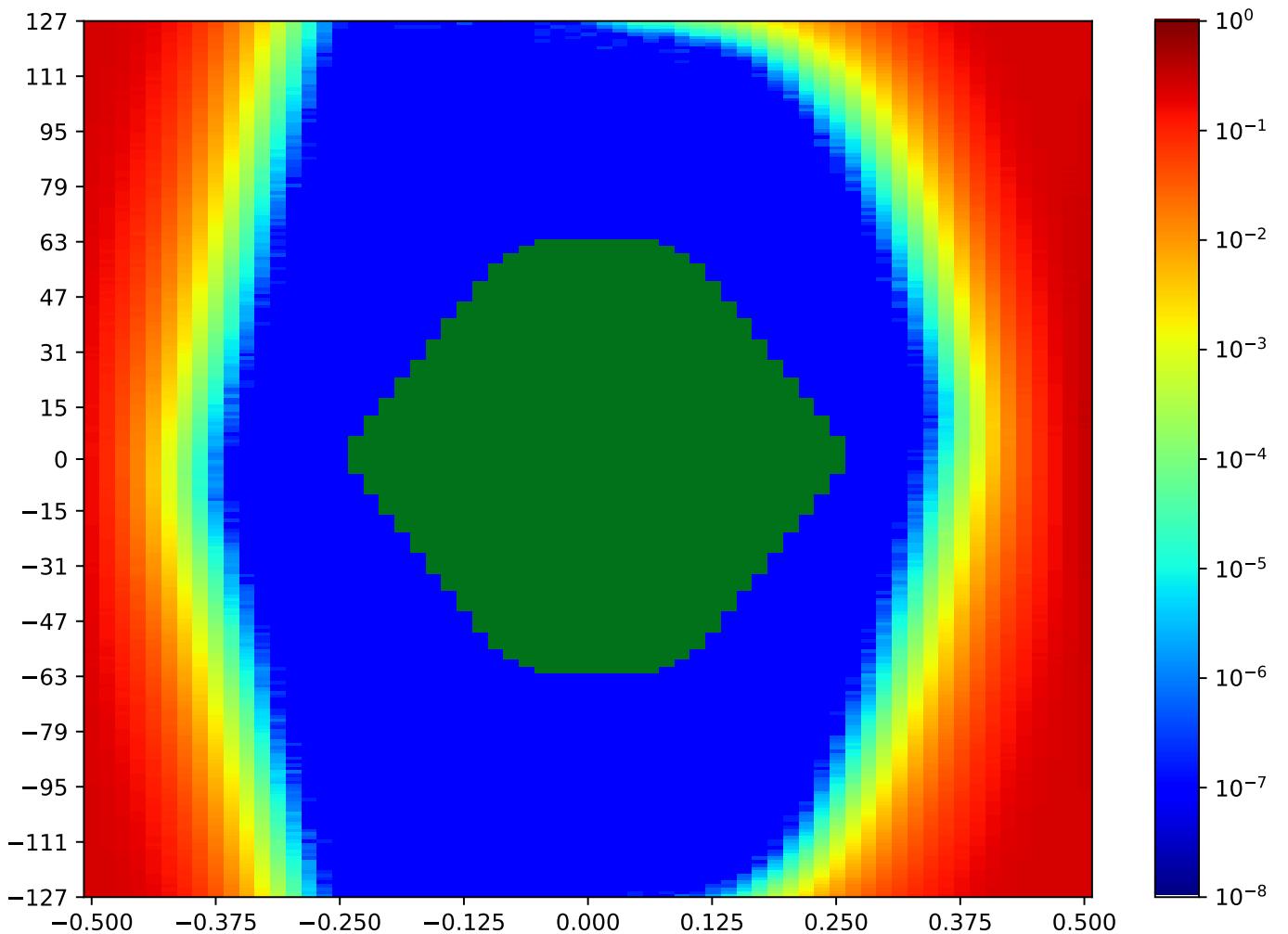


Figure 5.19: MSP_A_FPGA-TX2-04-RX16-04-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.6 MSP_A_FPGA-TX2-05-RX16-05-MSP_C_FPGA

Table 5.18: MSP_A_FPGA-TX2-05-RX16-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:54:40		2018-Sep-27 16:55:00	
Reset RX	OA	HO		VO	VO (%)
true	8556	44		67.69%	226 87.45%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

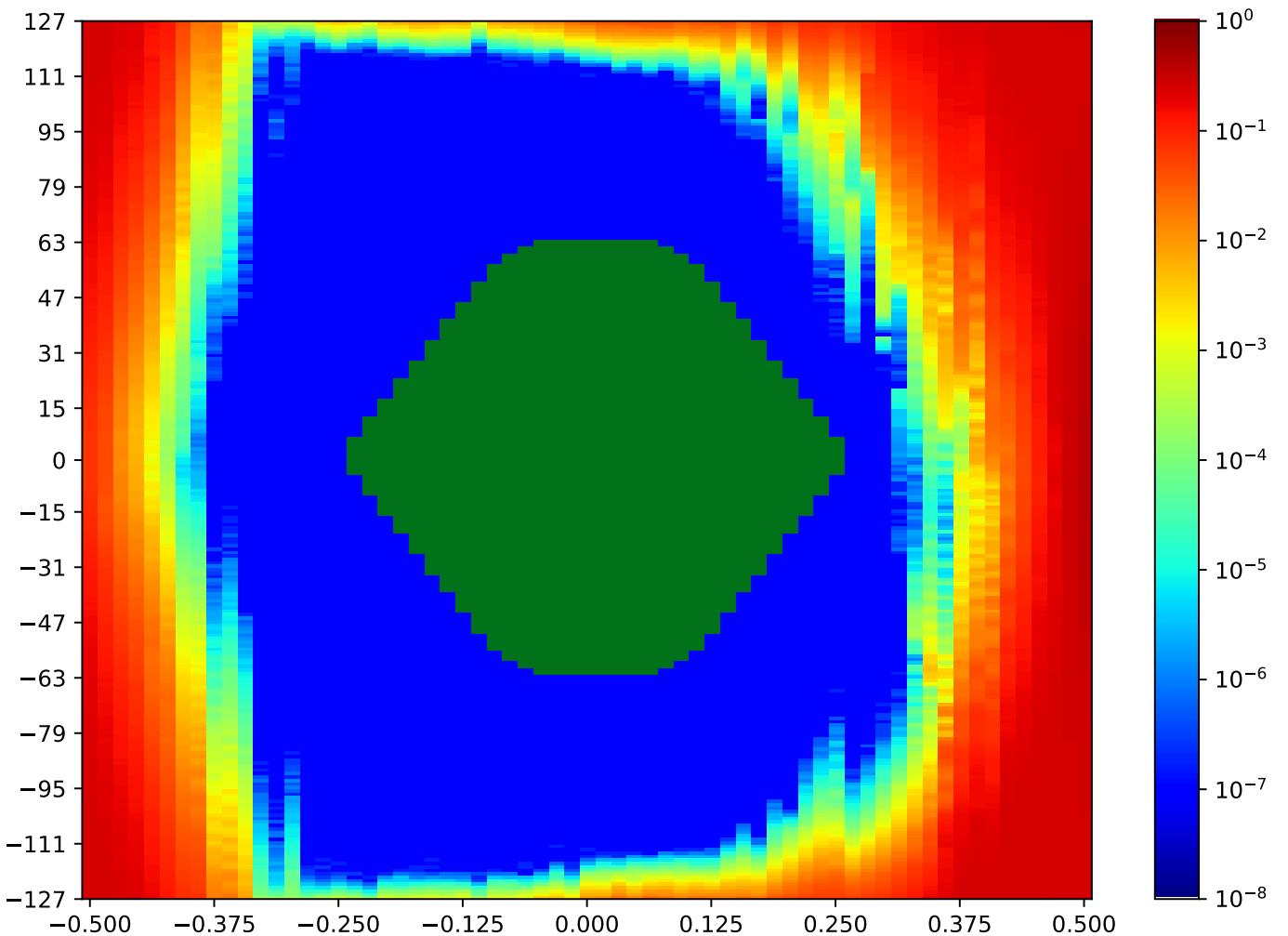


Figure 5.20: MSP_A_FPGA-TX2-05-RX16-05-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.7 MSP_A_FPGA-TX2-06-RX16-06-MSP_C_FPGA

Table 5.19: MSP_A_FPGA-TX2-06-RX16-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:57:48		2018-Sep-27 16:58:08	
Reset RX	OA	HO		VO	VO (%)
true	8993	43		66.15%	253 98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

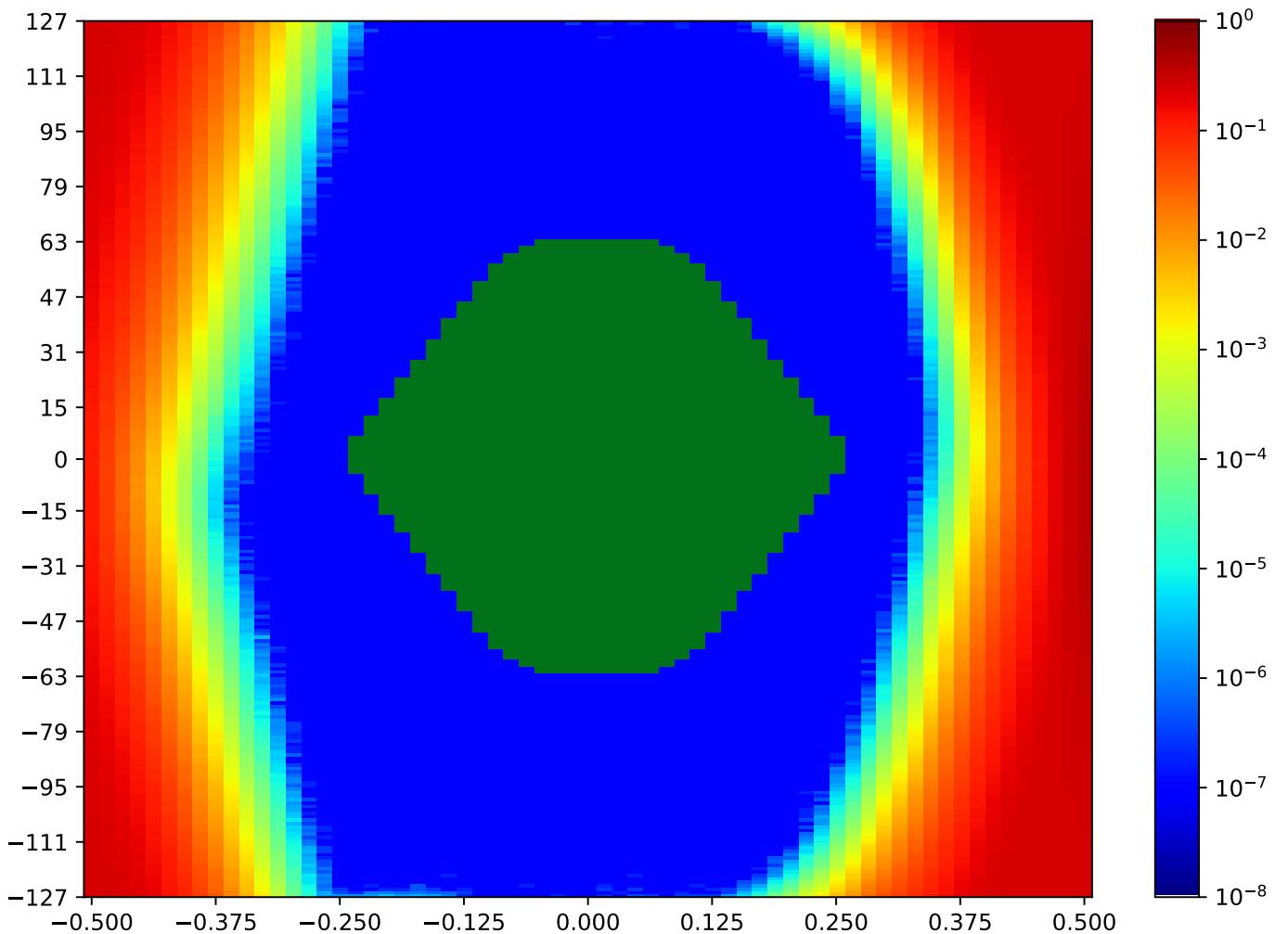


Figure 5.21: MSP_A_FPGA-TX2-06-RX16-06-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.8 MSP_A_FPGA-TX2-07-RX16-07-MSP_C_FPGA

Table 5.20: MSP_A_FPGA-TX2-07-RX16-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:55:20		2018-Sep-27 16:55:41	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9291	45		69.23%	254 99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

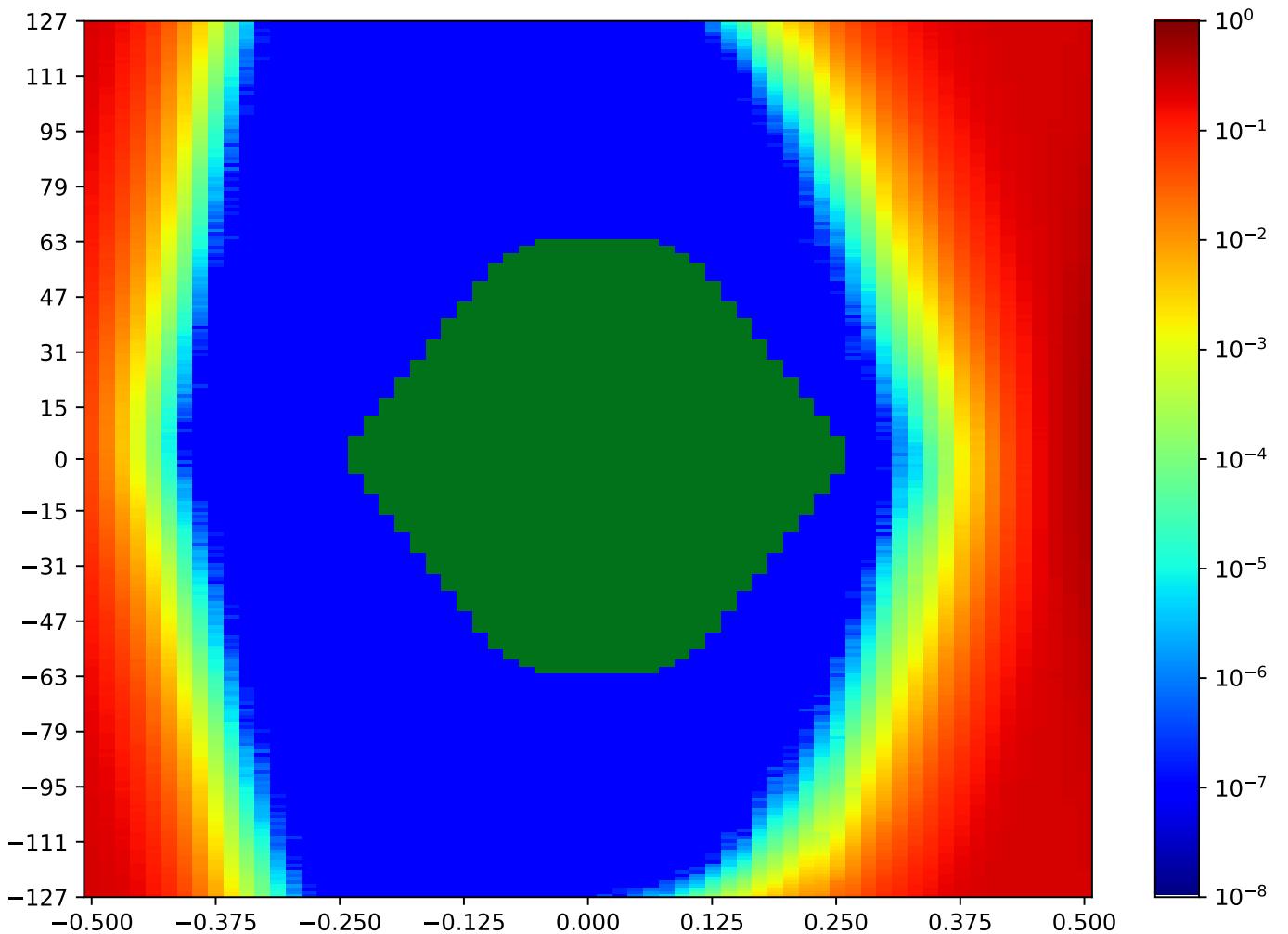


Figure 5.22: MSP_A_FPGA-TX2-07-RX16-07-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.9 MSP_A_FPGA-TX2-08-RX16-08-MSP_C_FPGA

Table 5.21: MSP_A_FPGA-TX2-08-RX16-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:57:27		2018-Sep-27 16:57:48	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9615	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

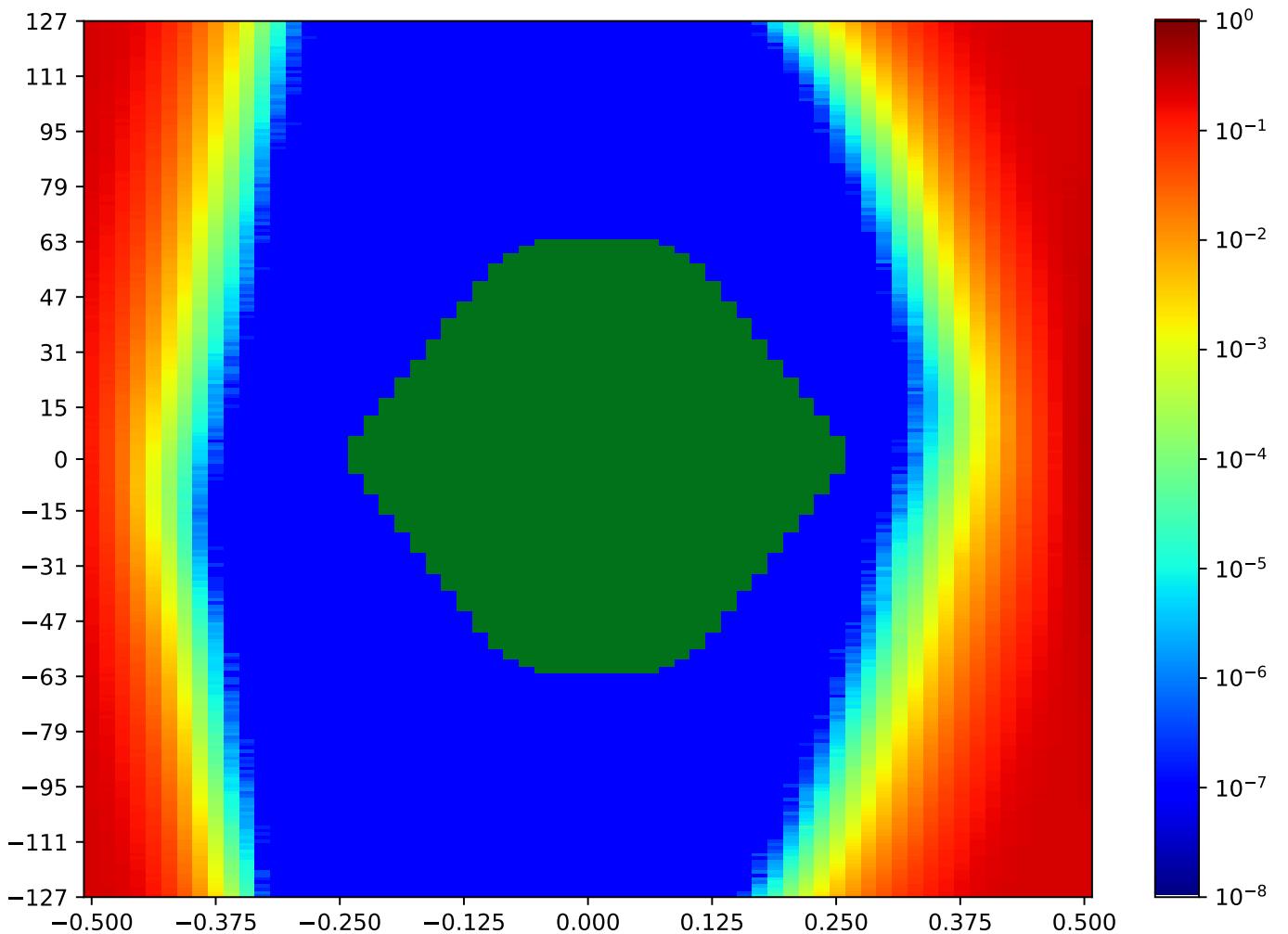


Figure 5.23: MSP_A_FPGA-TX2-08-RX16-08-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.10 MSP_A_FPGA-TX2-09-RX16-09-MSP_C_FPGA

Table 5.22: MSP_A_FPGA-TX2-09-RX16-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:55:41		2018-Sep-27 16:56:06	
Reset RX	OA	HO		VO	VO (%)
true	8601	39		250	97.65%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

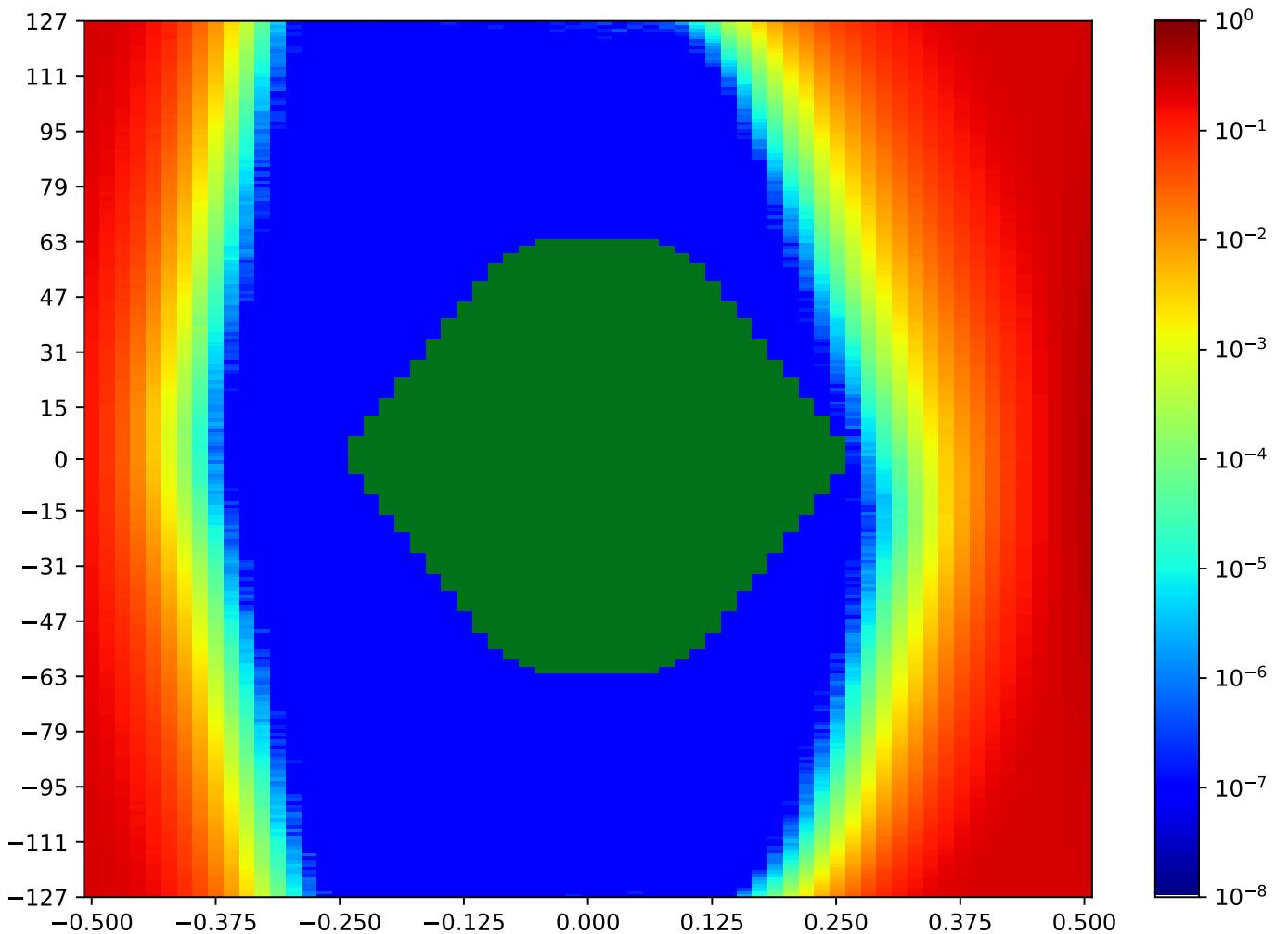


Figure 5.24: MSP_A_FPGA-TX2-09-RX16-09-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.11 MSP_A_FPGA-TX2-10-RX16-10-MSP_C_FPGA

Table 5.23: MSP_A_FPGA-TX2-10-RX16-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:56:47		2018-Sep-27 16:57:07	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8768	42		64.62%	254 98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

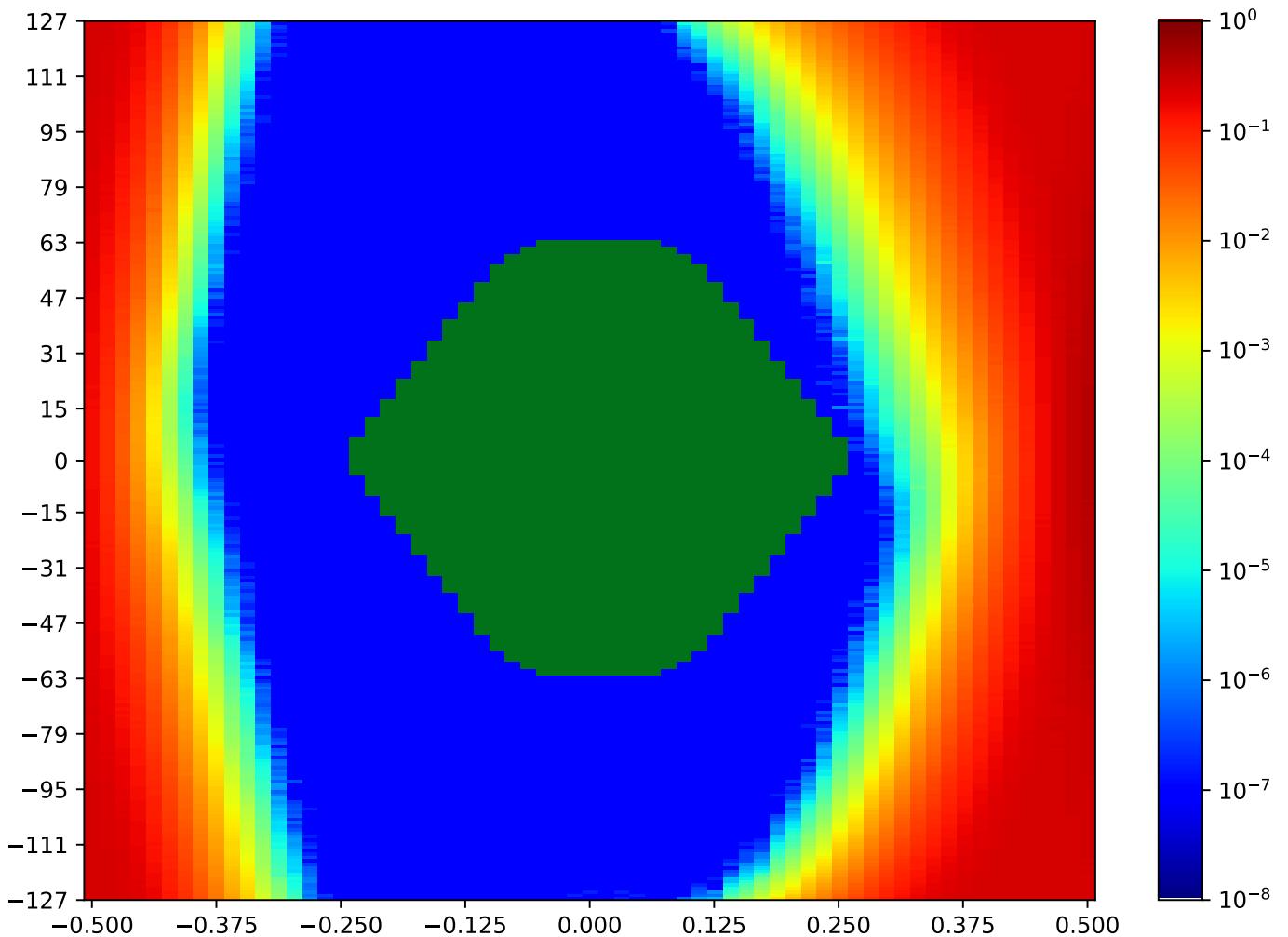


Figure 5.25: MSP_A_FPGA-TX2-10-RX16-10-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.2.12 MSP_A_FPGA-TX2-11-RX16-11-MSP_C_FPGA

Table 5.24: MSP_A_FPGA-TX2-11-RX16-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:56:26		2018-Sep-27 16:56:46	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9908	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

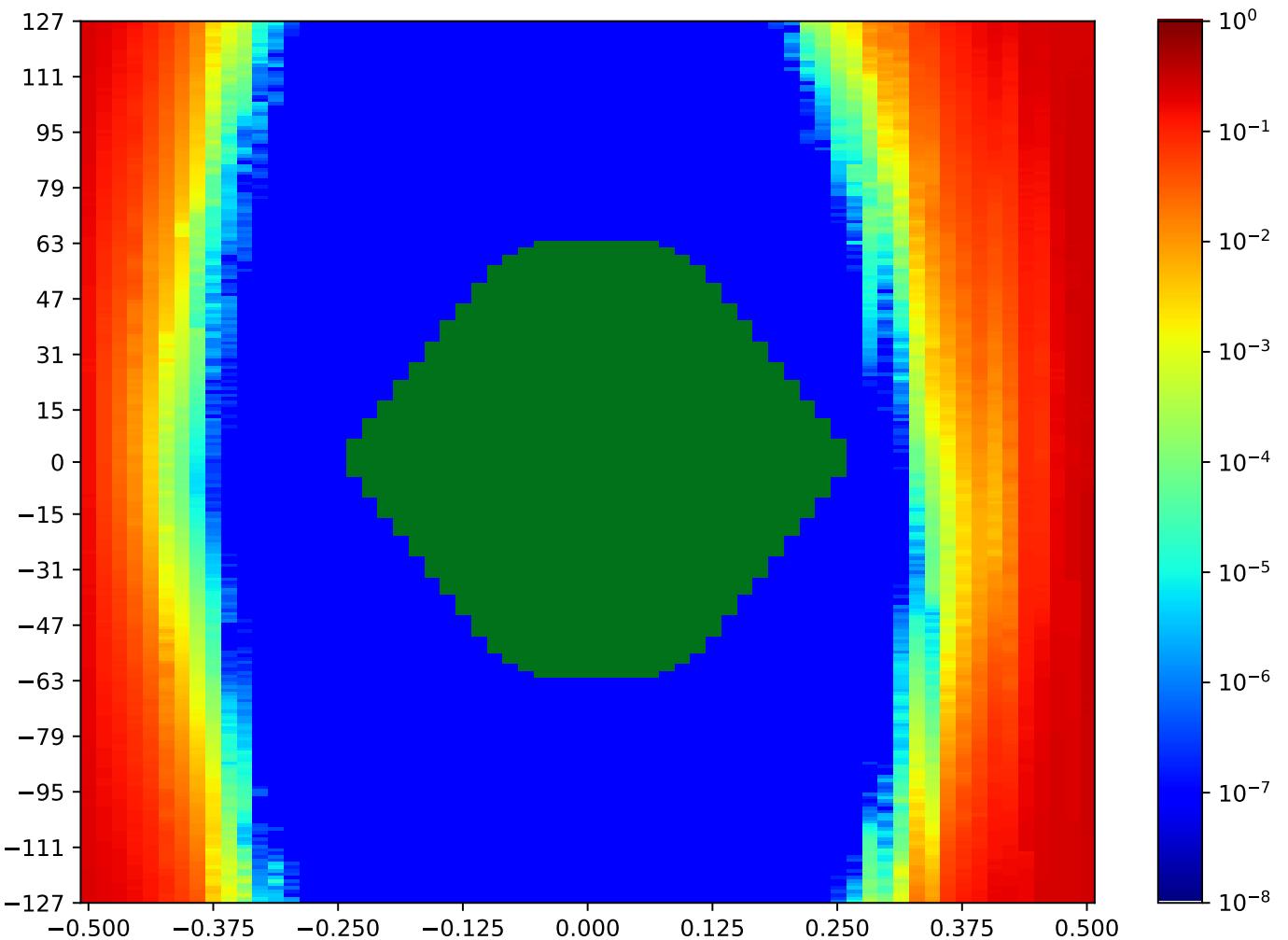


Figure 5.26: MSP_A_FPGA-TX2-11-RX16-11-MSP_C_FPGA

Call back to summary Figure 5.14. Sibling eye diagrams: V2-6.4.

5.3 MSP_C TX3 MSP_A RX6 Minipod Loopback

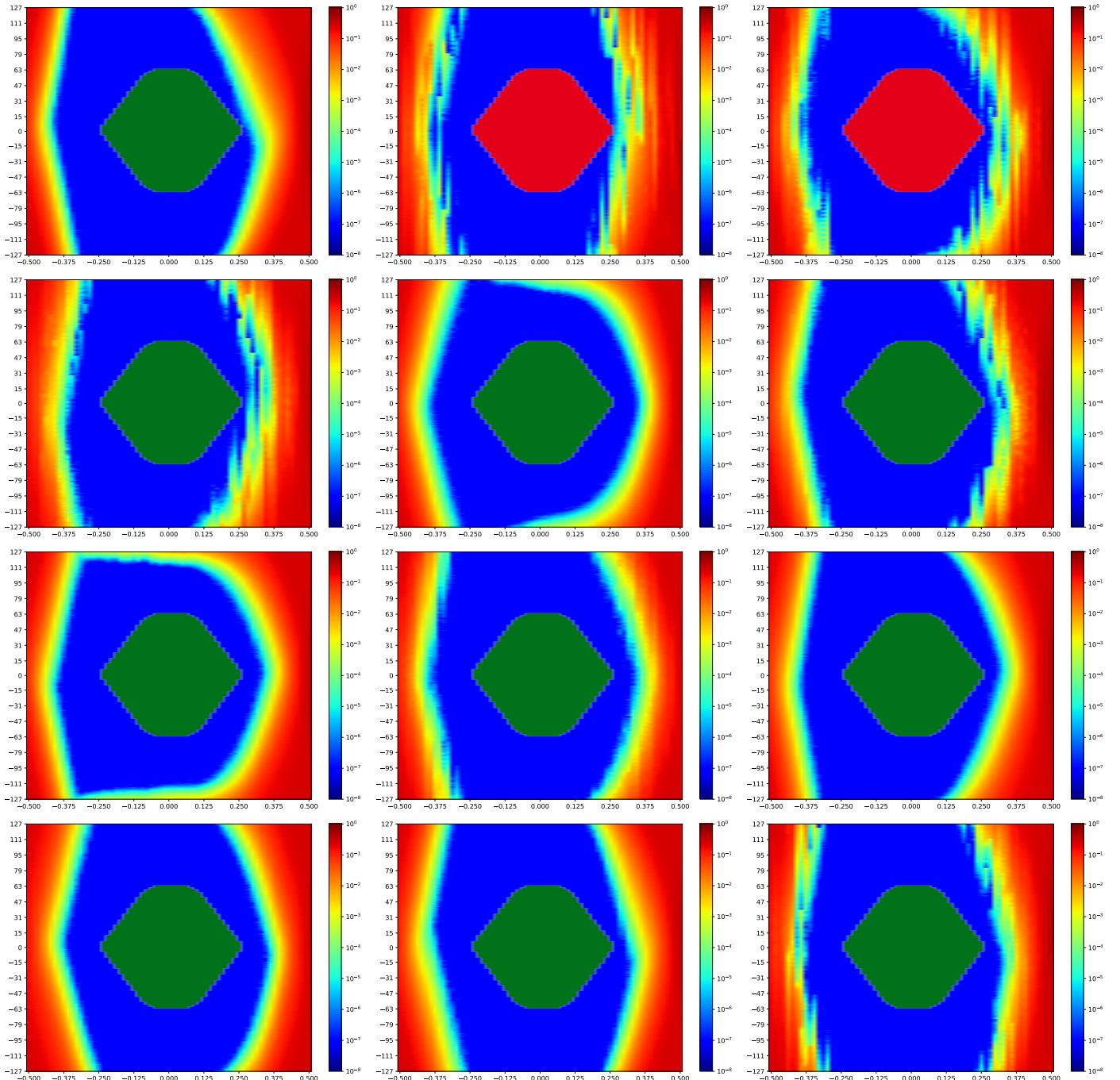


Figure 5.27: MSP_C TX3 MSP_A RX6 Minipod Loopback

A cross-reference to Figure 5.27. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.40.

5.3.1 MSP_C_FPGA-TX3-00-RX6-00-MSP_A_FPGA

Table 5.25: MSP_C_FPGA-TX3-00-RX6-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:59:09		2018-Sep-27 16:59:30	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9281	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

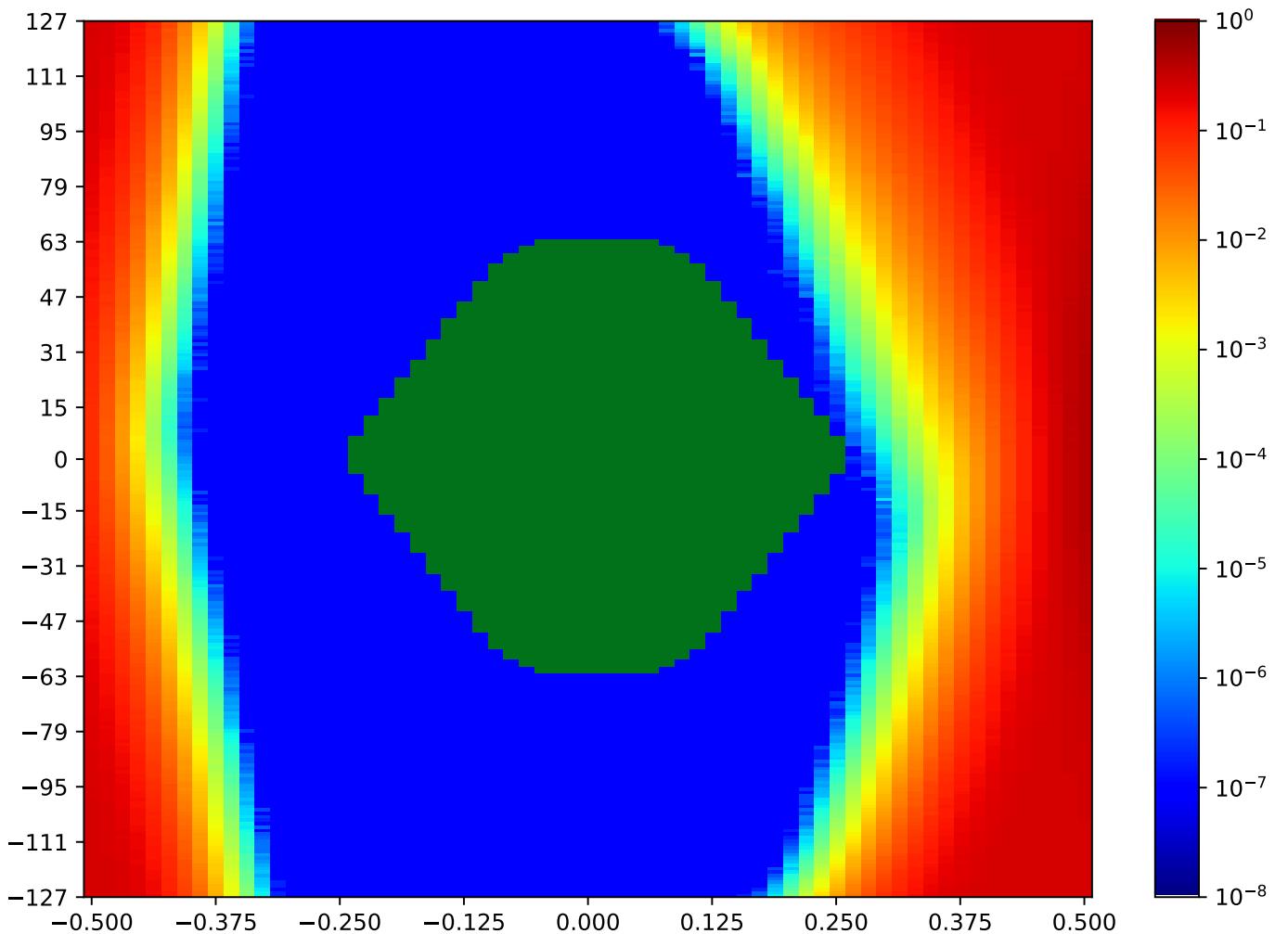


Figure 5.28: MSP_C_FPGA-TX3-00-RX6-00-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.2 MSP_C_FPGA-TX3-01-RX6-01-MSP_A_FPGA

Table 5.26: MSP_C_FPGA-TX3-01-RX6-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:59:51		2018-Sep-27 17:00:11	
Reset RX	OA	HO		VO	VO (%)
true	8746	39		60.00%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

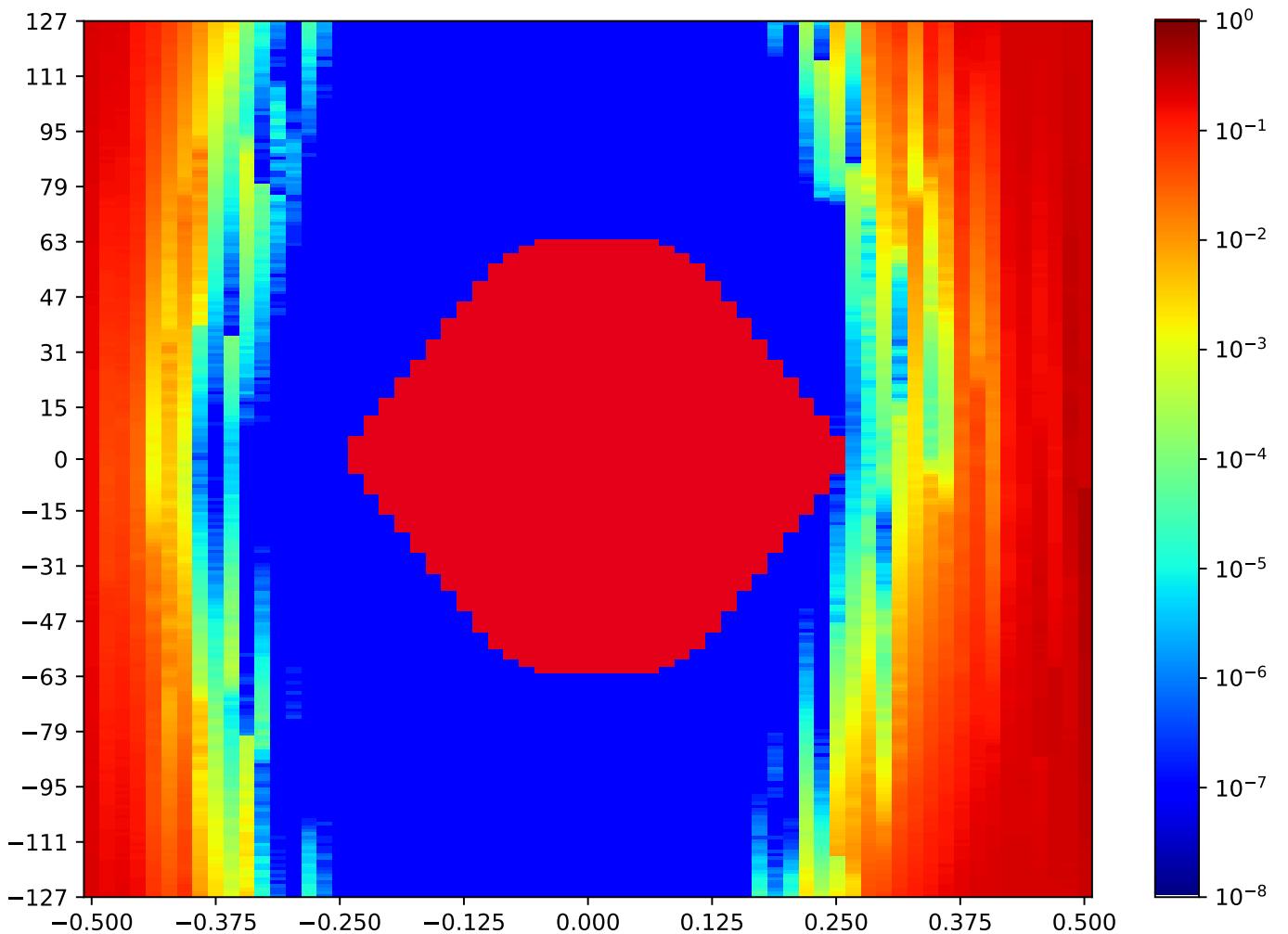


Figure 5.29: MSP_C_FPGA-TX3-01-RX6-01-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.3 MSP_C_FPGA-TX3-02-RX6-02-MSP_A_FPGA

Table 5.27: MSP_C_FPGA-TX3-02-RX6-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:00:12		2018-Sep-27 17:00:32	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8417	40		60.00%	254 99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

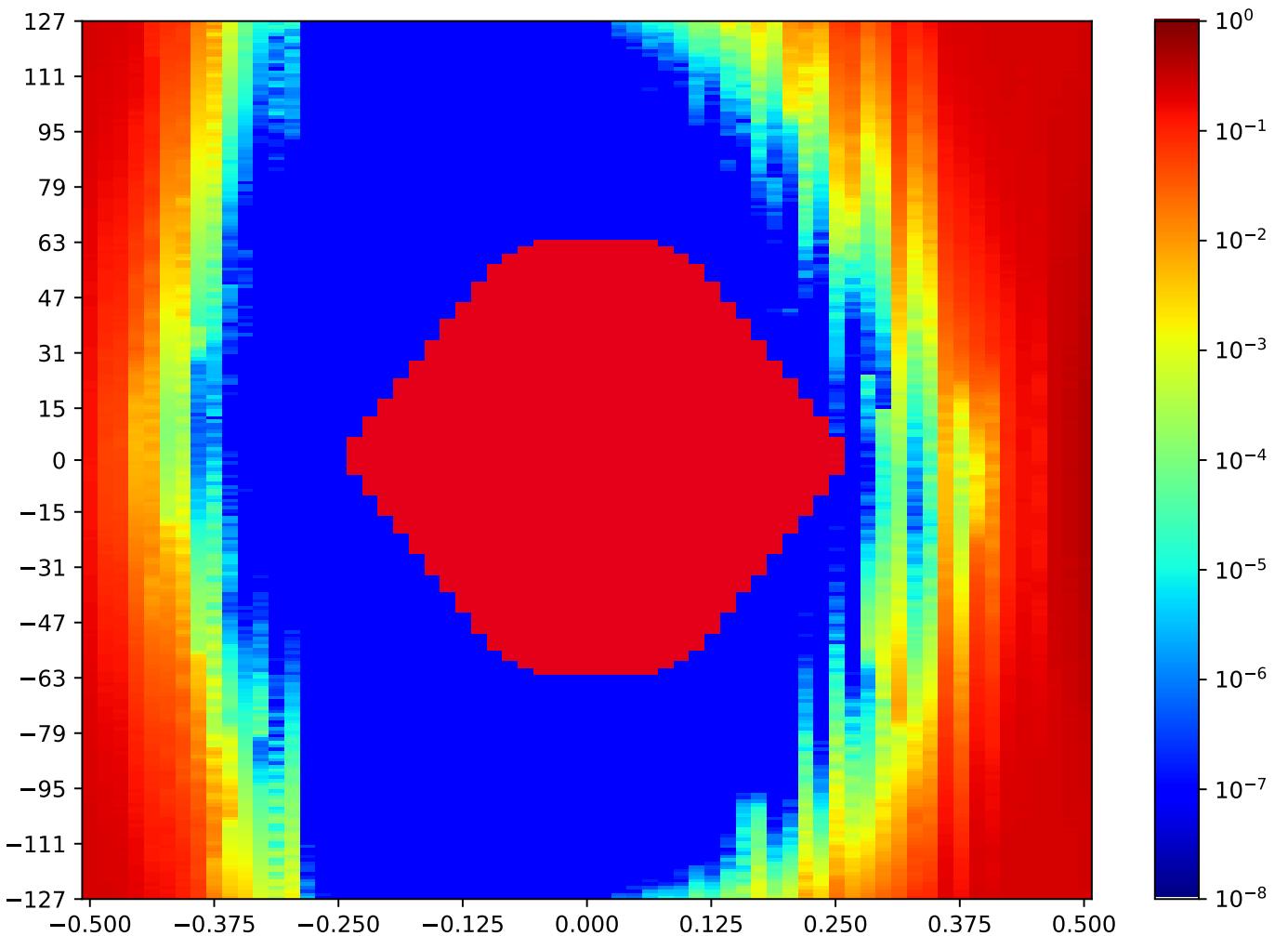


Figure 5.30: MSP_C_FPGA-TX3-02-RX6-02-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.4 MSP_C_FPGA-TX3-03-RX6-03-MSP_A_FPGA

Table 5.28: MSP_C_FPGA-TX3-03-RX6-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:58:29		2018-Sep-27 16:58:49	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8619	39		60.00%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

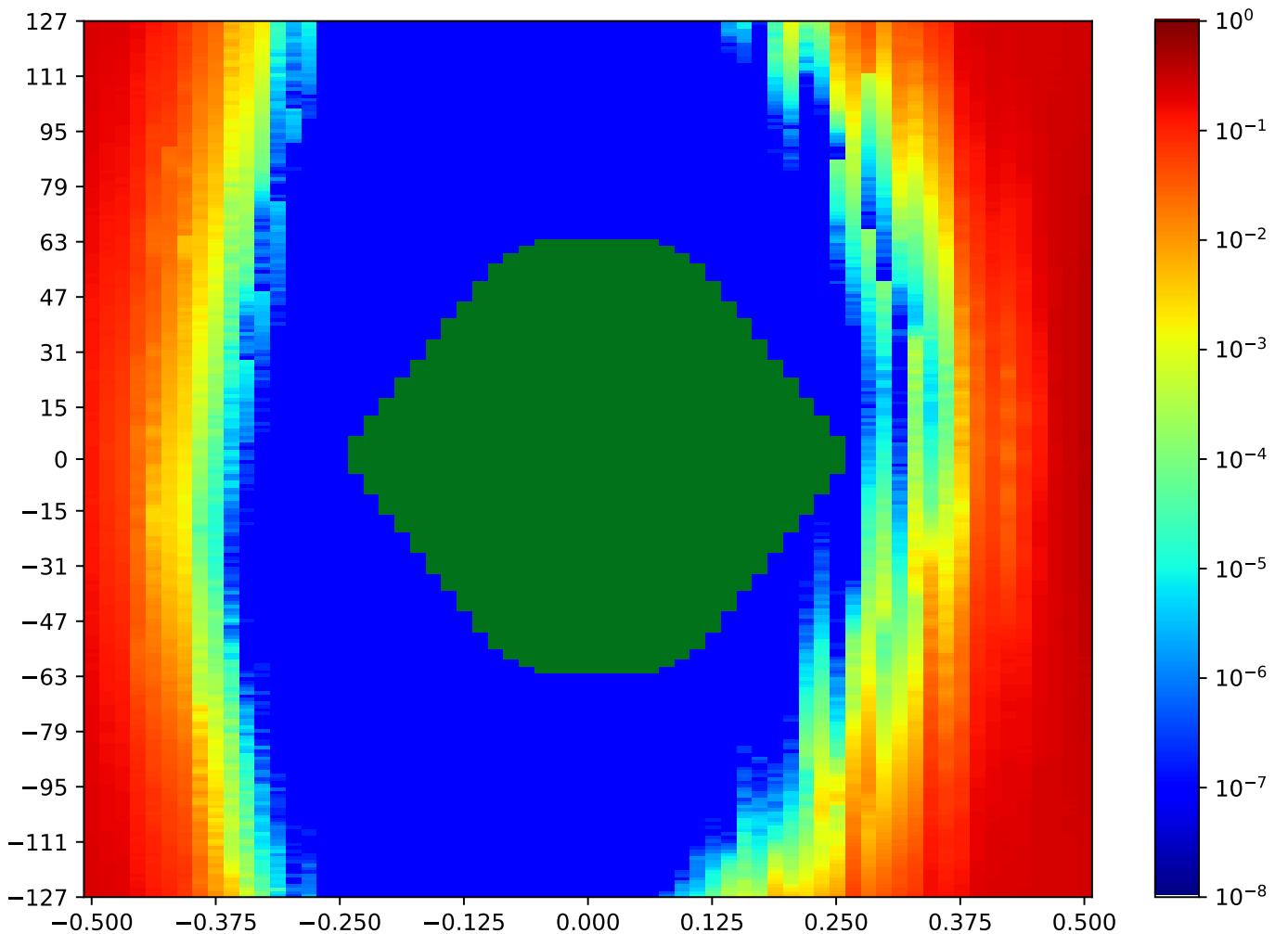


Figure 5.31: MSP_C_FPGA-TX3-03-RX6-03-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.5 MSP_C_FPGA-TX3-04-RX6-04-MSP_A_FPGA

Table 5.29: MSP_C_FPGA-TX3-04-RX6-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:01:13		2018-Sep-27 17:01:37	
Reset RX	OA	HO		VO	VO (%)
true	8603	45		229	88.63%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

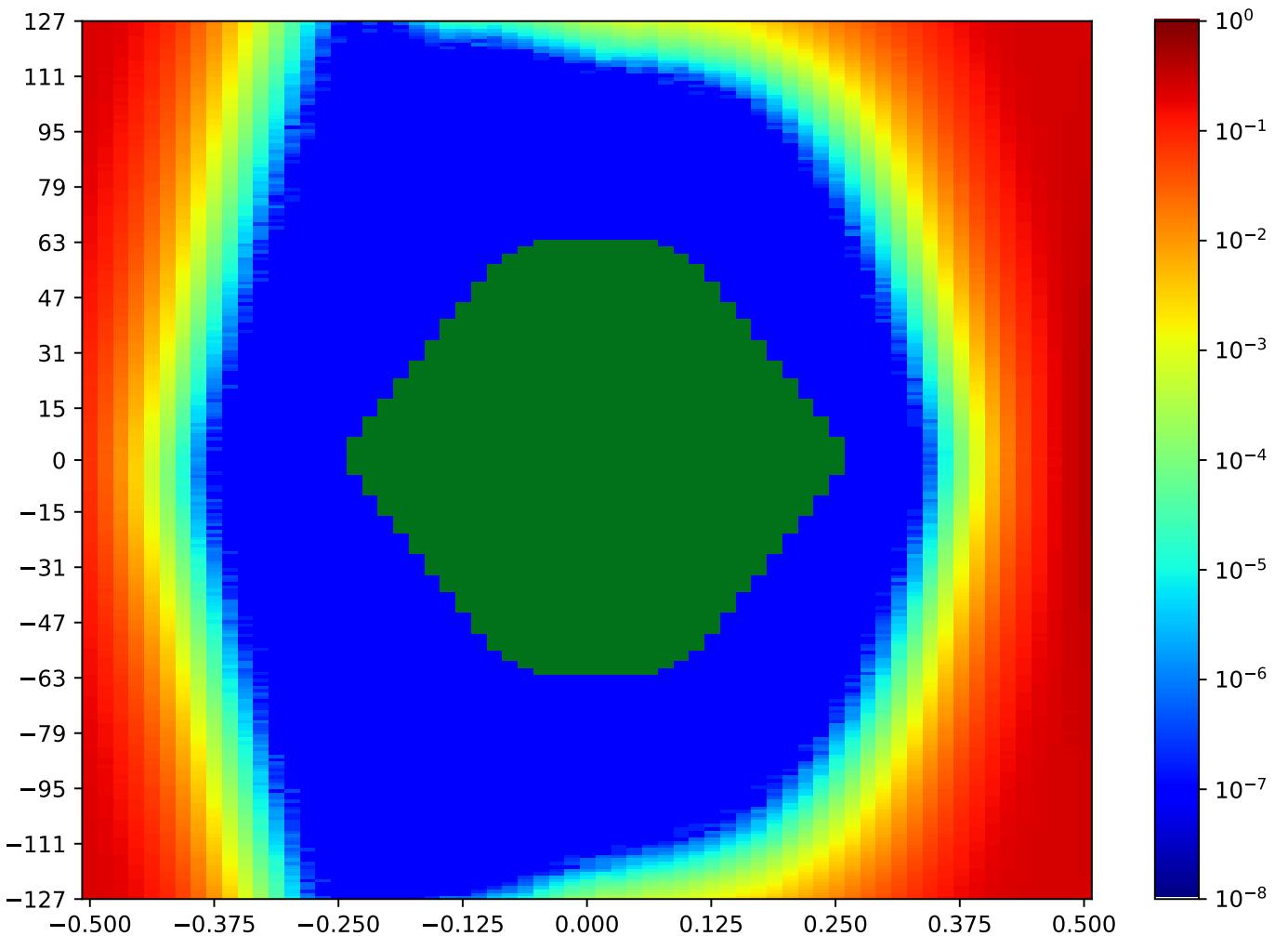


Figure 5.32: MSP_C_FPGA-TX3-04-RX6-04-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.6 MSP_C_FPGA-TX3-05-RX6-05-MSP_A_FPGA

Table 5.30: MSP_C_FPGA-TX3-05-RX6-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:58:09		2018-Sep-27 16:58:29	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9072	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

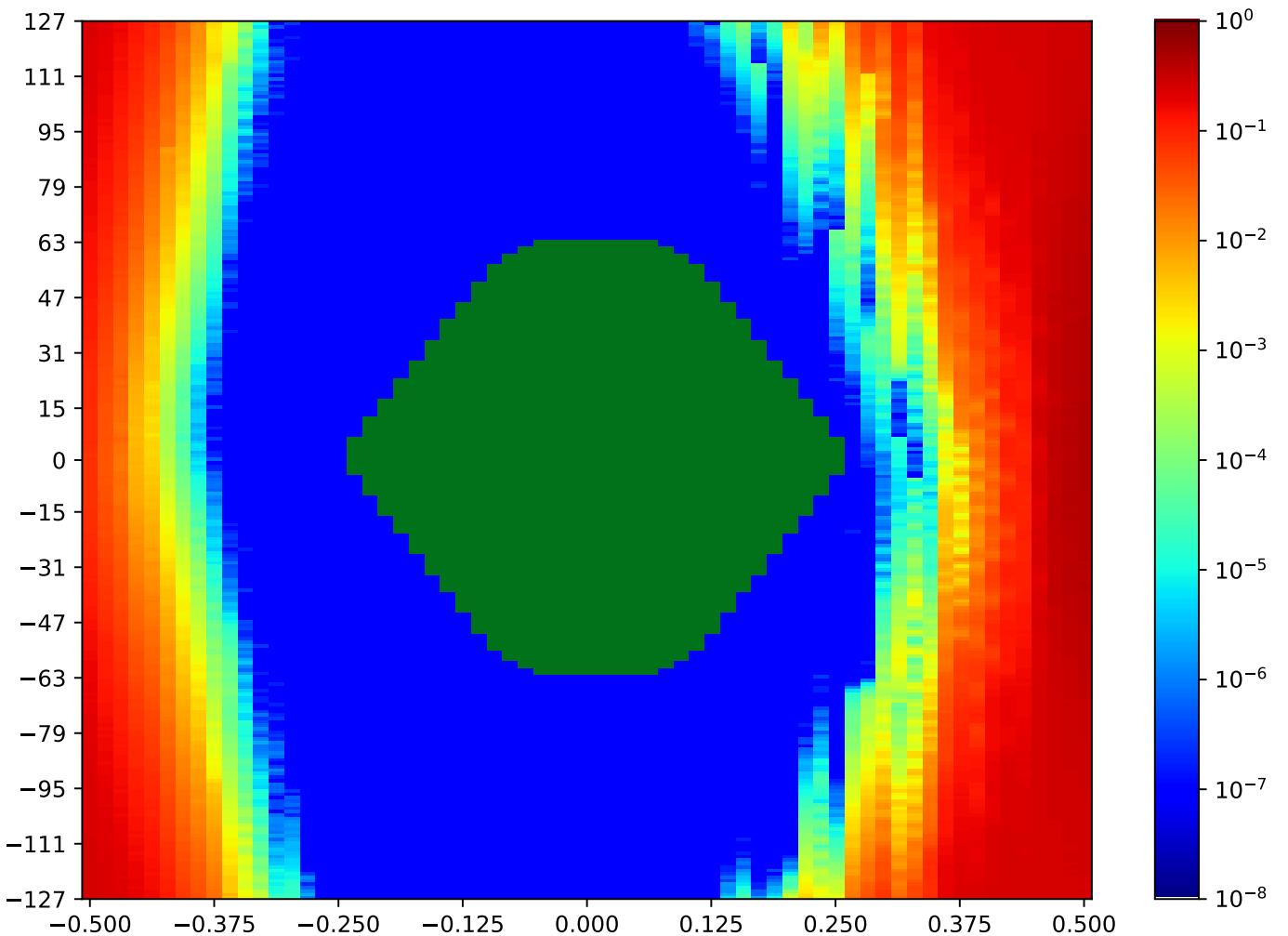


Figure 5.33: MSP_C_FPGA-TX3-05-RX6-05-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.7 MSP_C_FPGA-TX3-06-RX6-06-MSP_A_FPGA

Table 5.31: MSP_C_FPGA-TX3-06-RX6-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:01:58		2018-Sep-27 17:02:18	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8482	45		69.23%	221 86.67%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

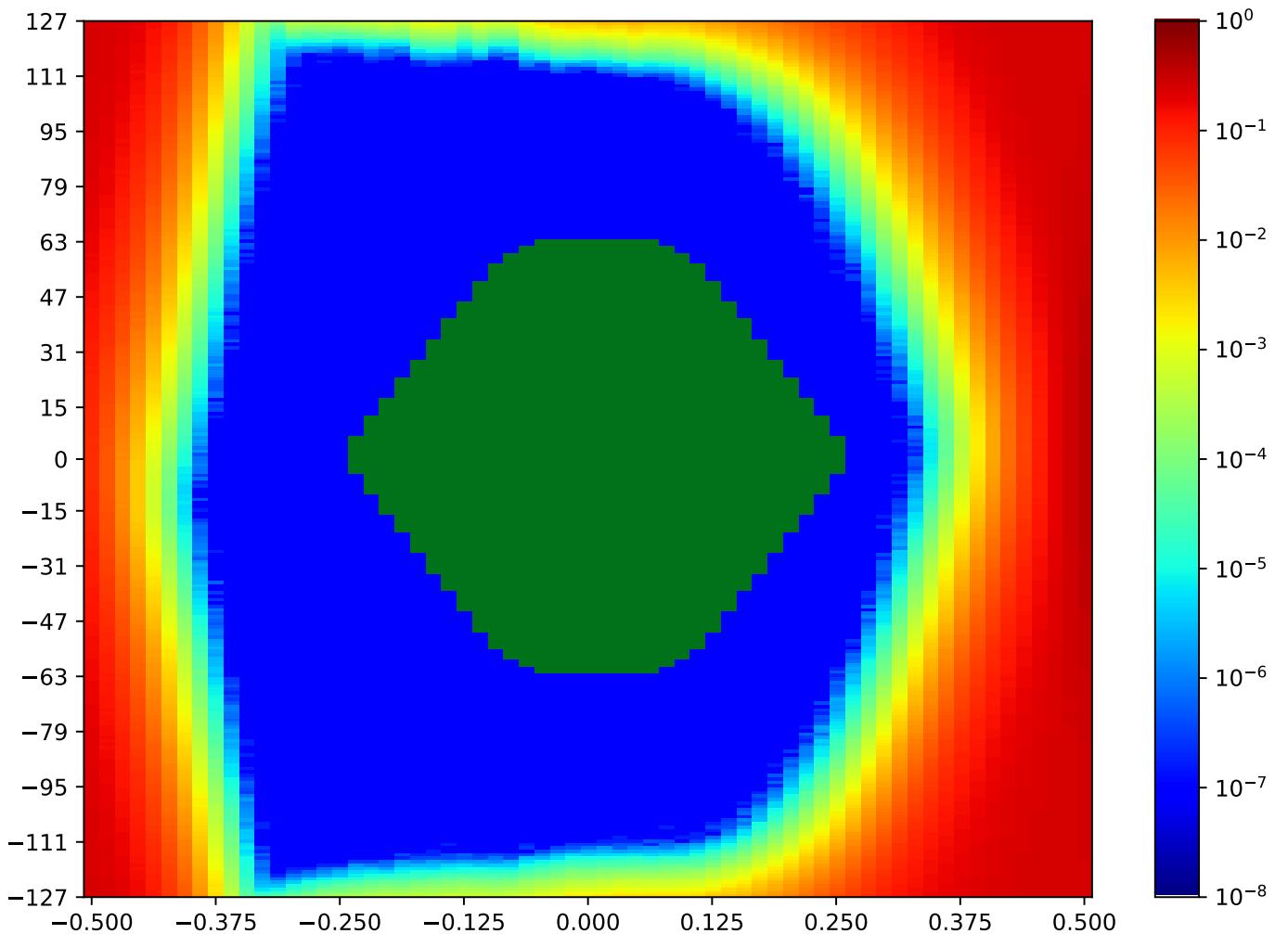


Figure 5.34: MSP_C_FPGA-TX3-06-RX6-06-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.8 MSP_C_FPGA-TX3-07-RX6-07-MSP_A_FPGA

Table 5.32: MSP_C_FPGA-TX3-07-RX6-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:58:49		2018-Sep-27 16:59:09	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9524	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

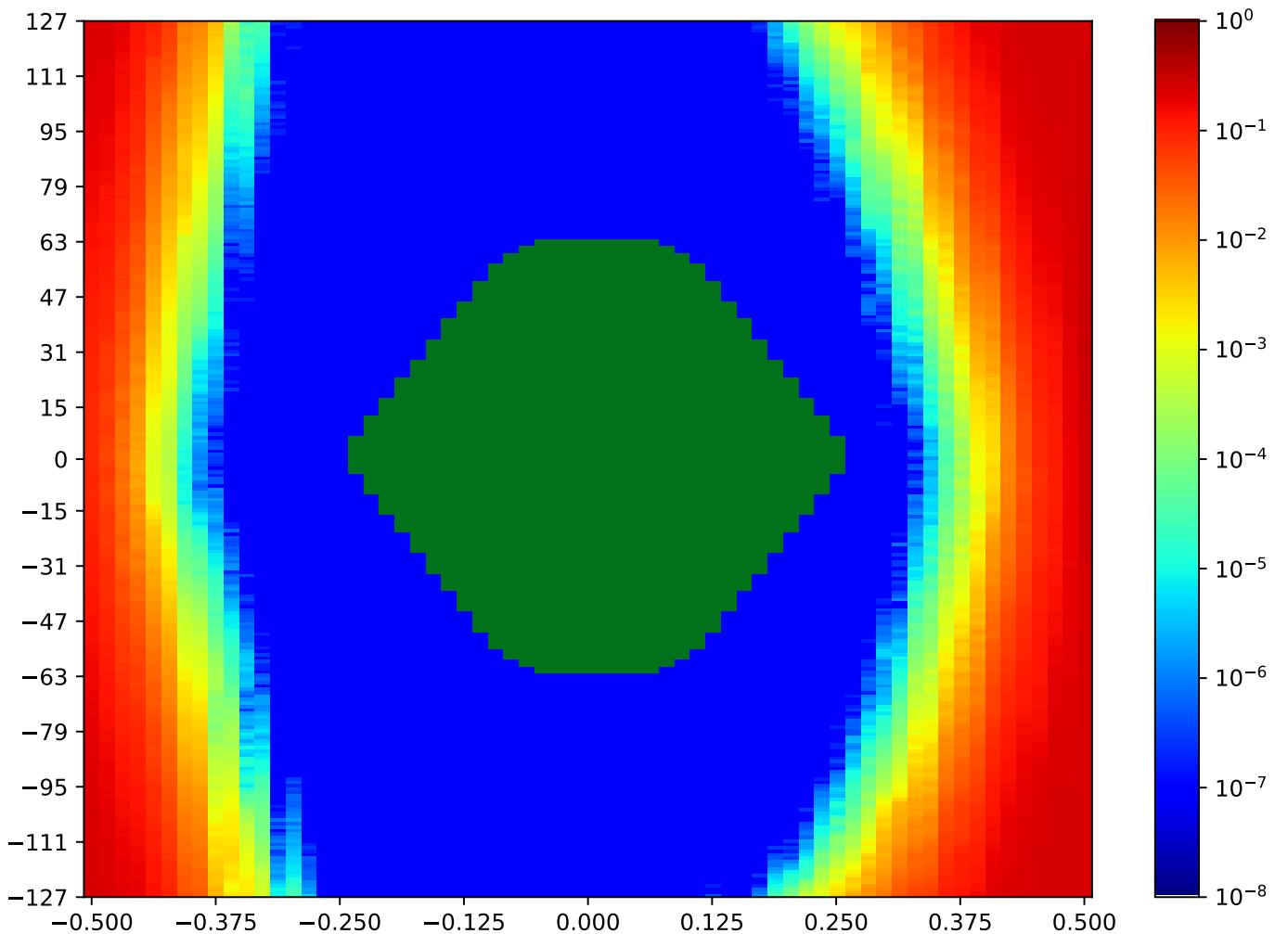


Figure 5.35: MSP_C_FPGA-TX3-07-RX6-07-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.9 MSP_C_FPGA-TX3-08-RX6-08-MSP_A_FPGA

Table 5.33: MSP_C_FPGA-TX3-08-RX6-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:01:37		2018-Sep-27 17:01:58	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9207	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

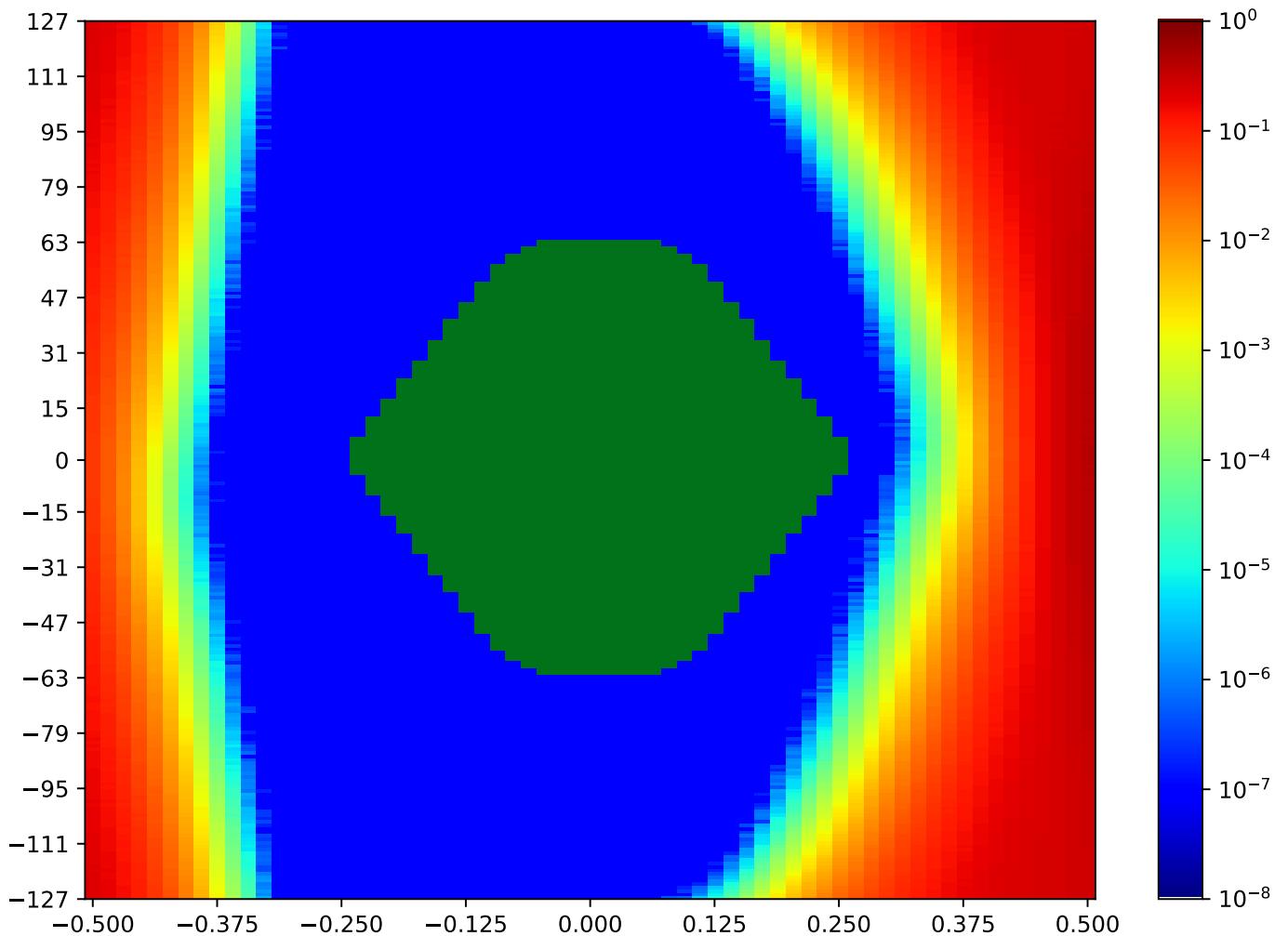


Figure 5.36: MSP_C_FPGA-TX3-08-RX6-08-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.10 MSP_C_FPGA-TX3-09-RX6-09-MSP_A_FPGA

Table 5.34: MSP_C_FPGA-TX3-09-RX6-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:59:30		2018-Sep-27 16:59:51	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9424	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

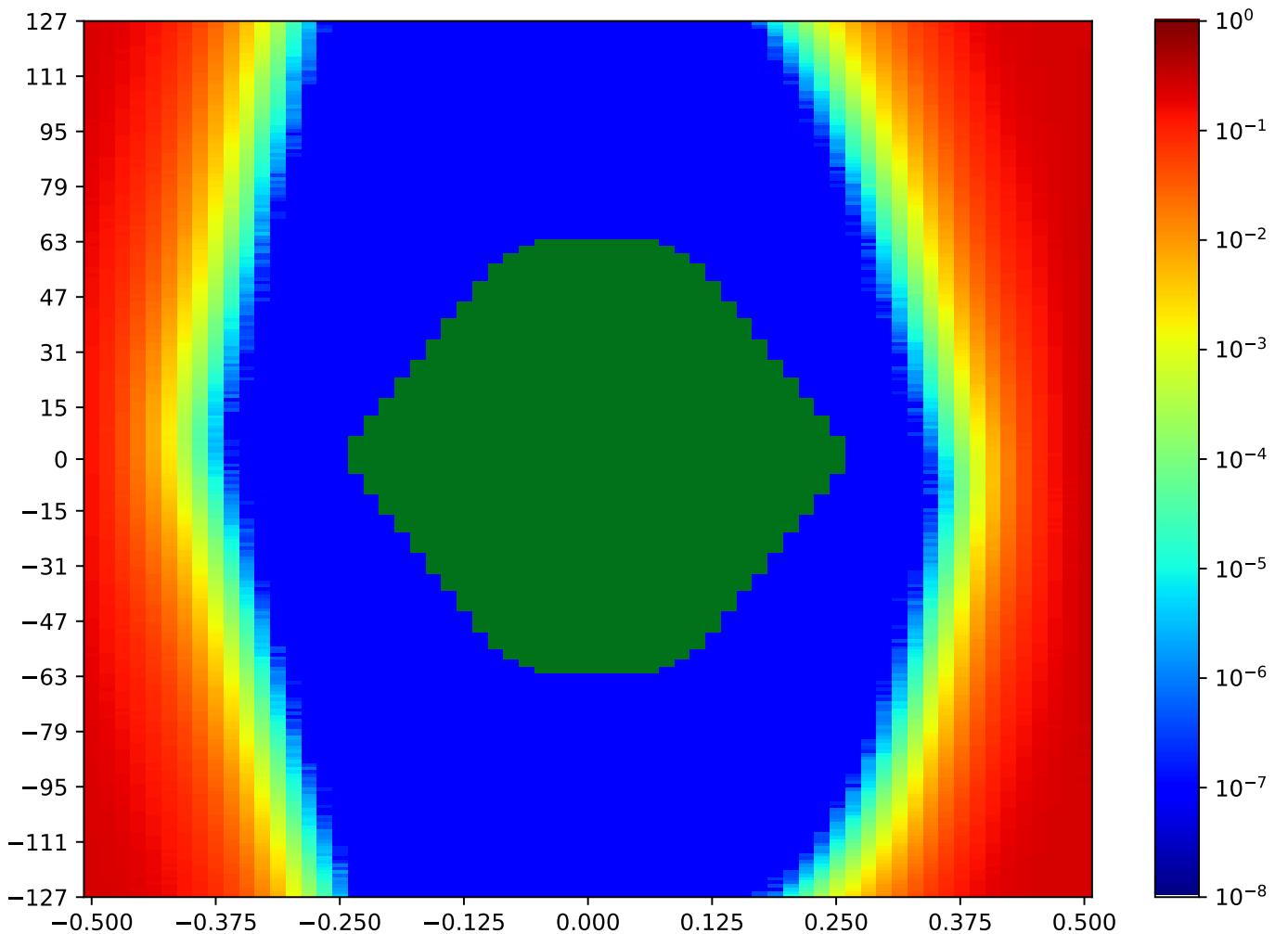


Figure 5.37: MSP_C_FPGA-TX3-09-RX6-09-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.11 MSP_C_FPGA-TX3-10-RX6-10-MSP_A_FPGA

Table 5.35: MSP_C_FPGA-TX3-10-RX6-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:00:52		2018-Sep-27 17:01:13	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9248	42		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

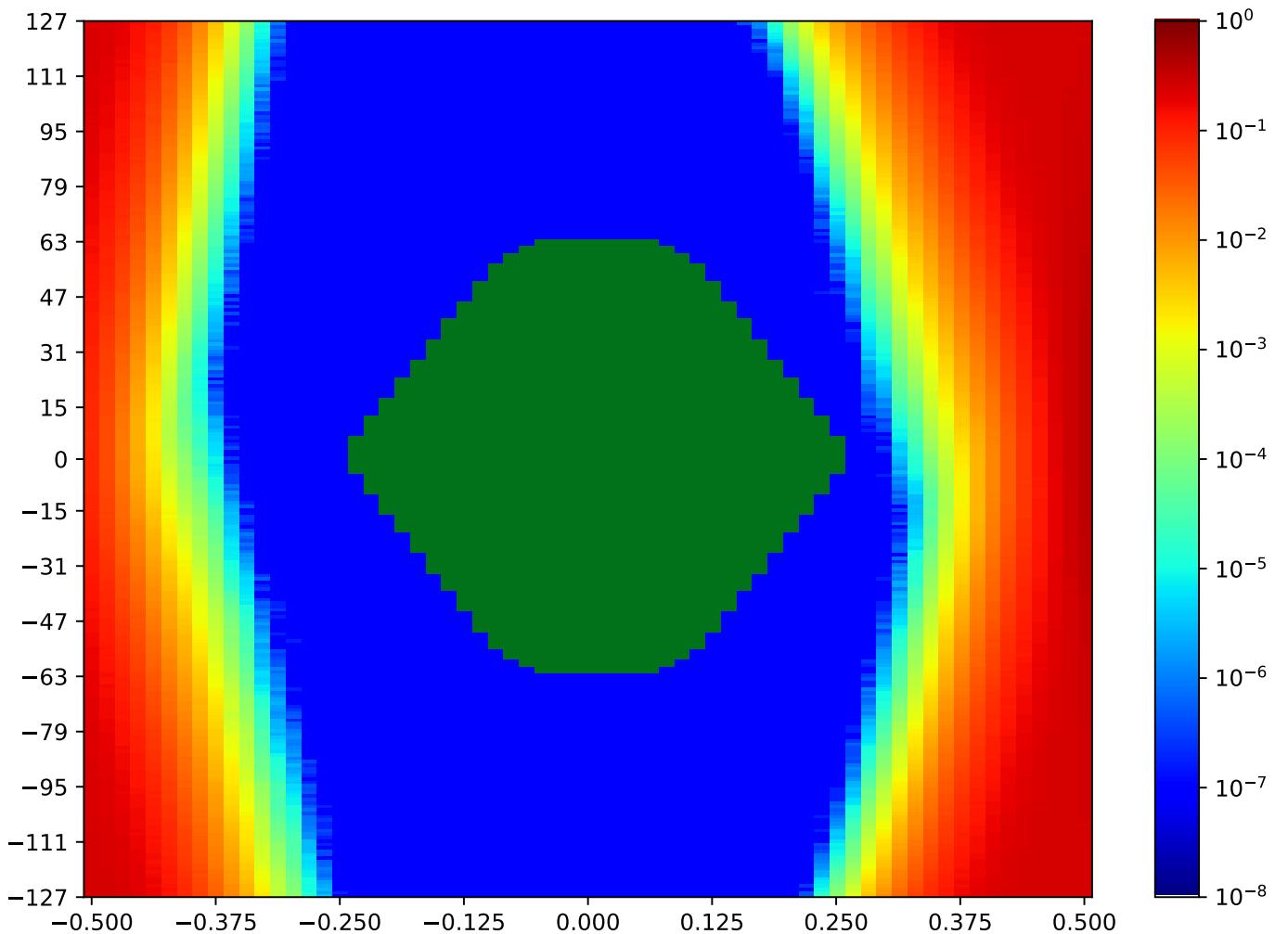


Figure 5.38: MSP_C_FPGA-TX3-10-RX6-10-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.3.12 MSP_C_FPGA-TX3-11-RX6-11-MSP_A_FPGA

Table 5.36: MSP_C_FPGA-TX3-11-RX6-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:00:32		2018-Sep-27 17:00:52	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9712	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

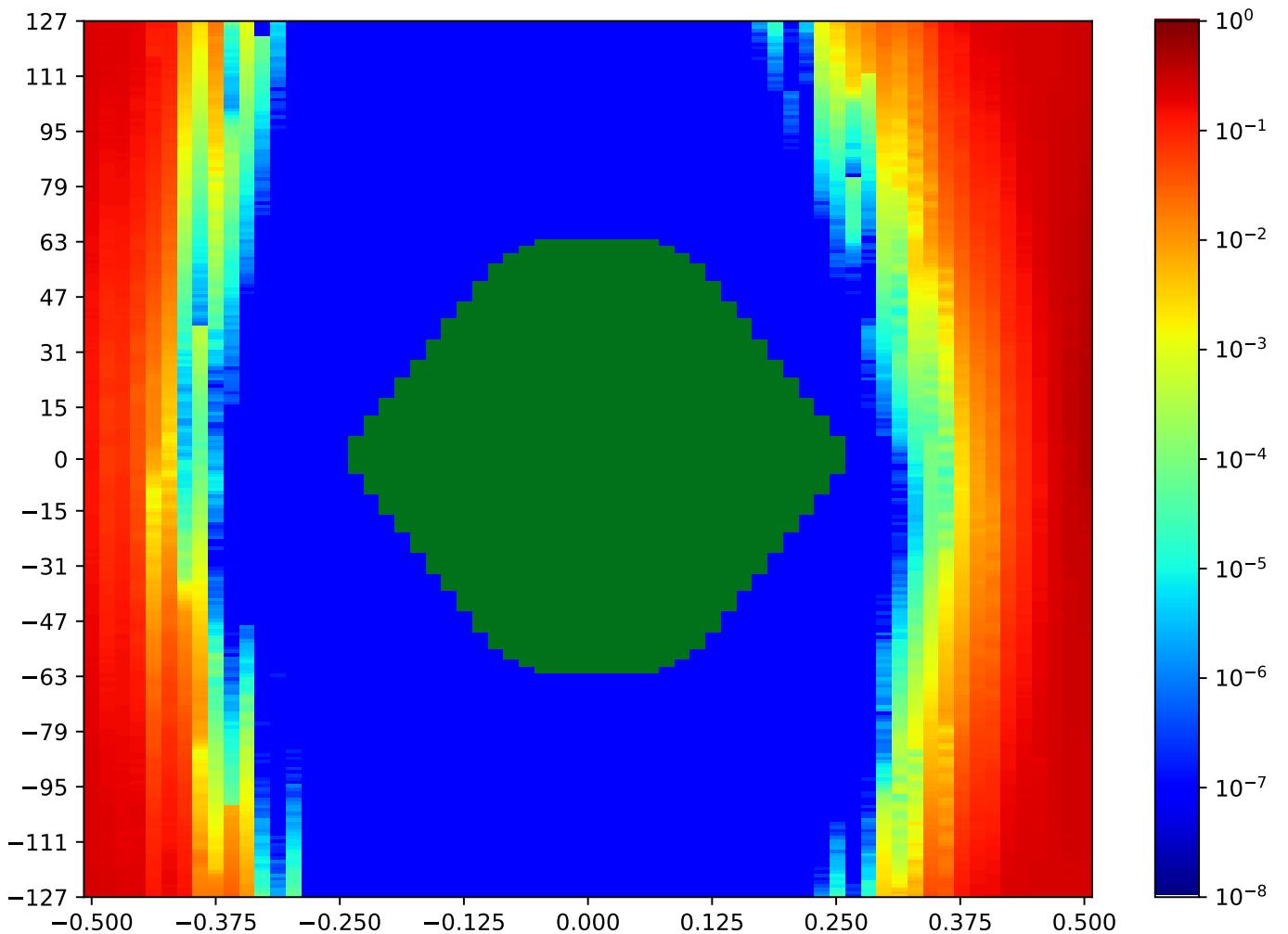


Figure 5.39: MSP_C_FPGA-TX3-11-RX6-11-MSP_A_FPGA

Call back to summary Figure 5.27. Sibling eye diagrams: V2-6.4.

5.4 MSP_C TX4 MSP_A RX7 Minipod Loopback

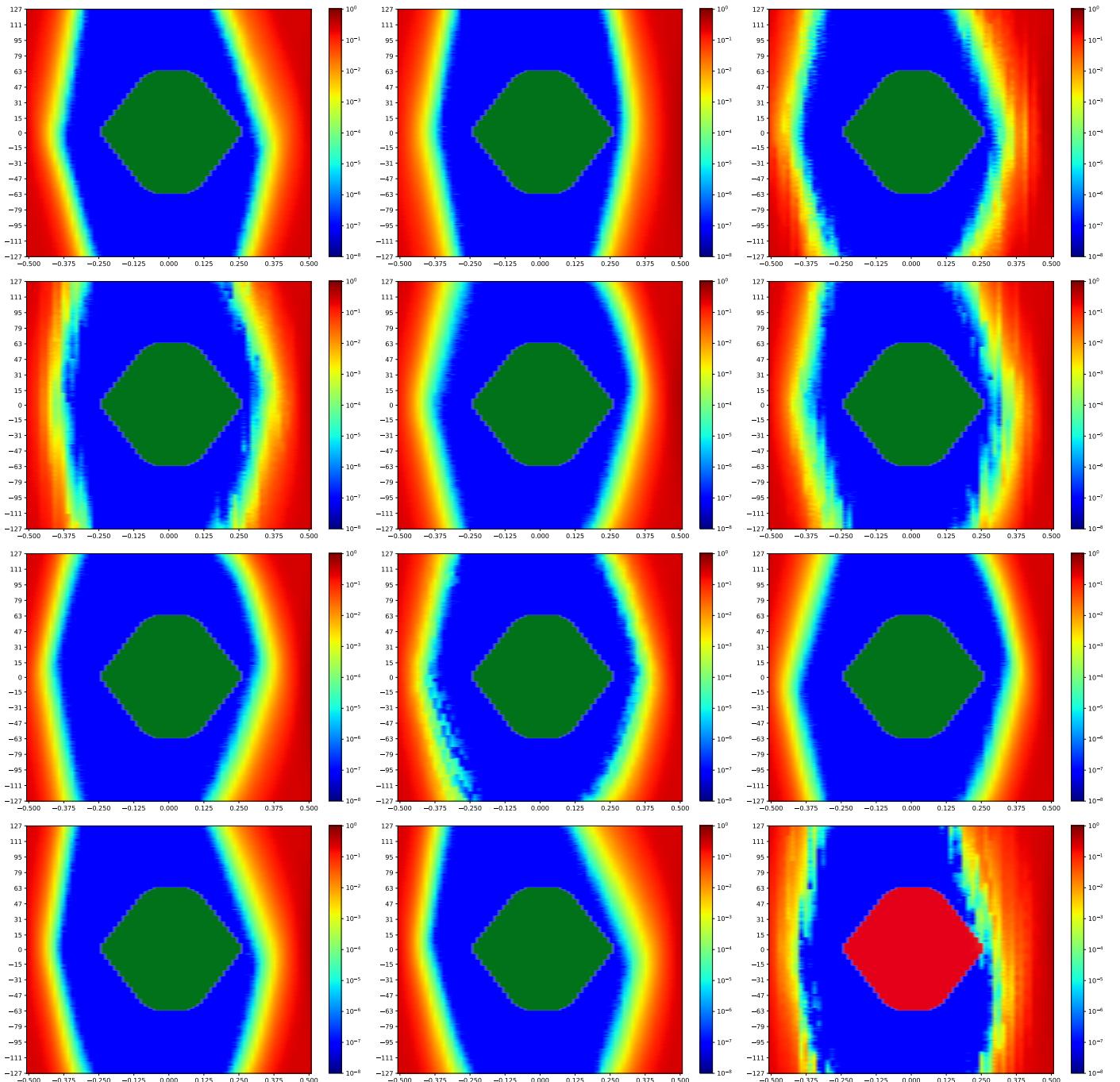


Figure 5.40: MSP_C TX4 MSP_A RX7 Minipod Loopback

A cross-reference to Figure 5.40. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.53.

5.4.1 MSP_C_FPGA-TX4-00-RX7-00-MSP_A_FPGA

Table 5.37: MSP_C_FPGA-TX4-00-RX7-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:03:19		2018-Sep-27 17:03:39	
Reset RX	OA	HO		VO	VO (%)
true	9052	40		61.54%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

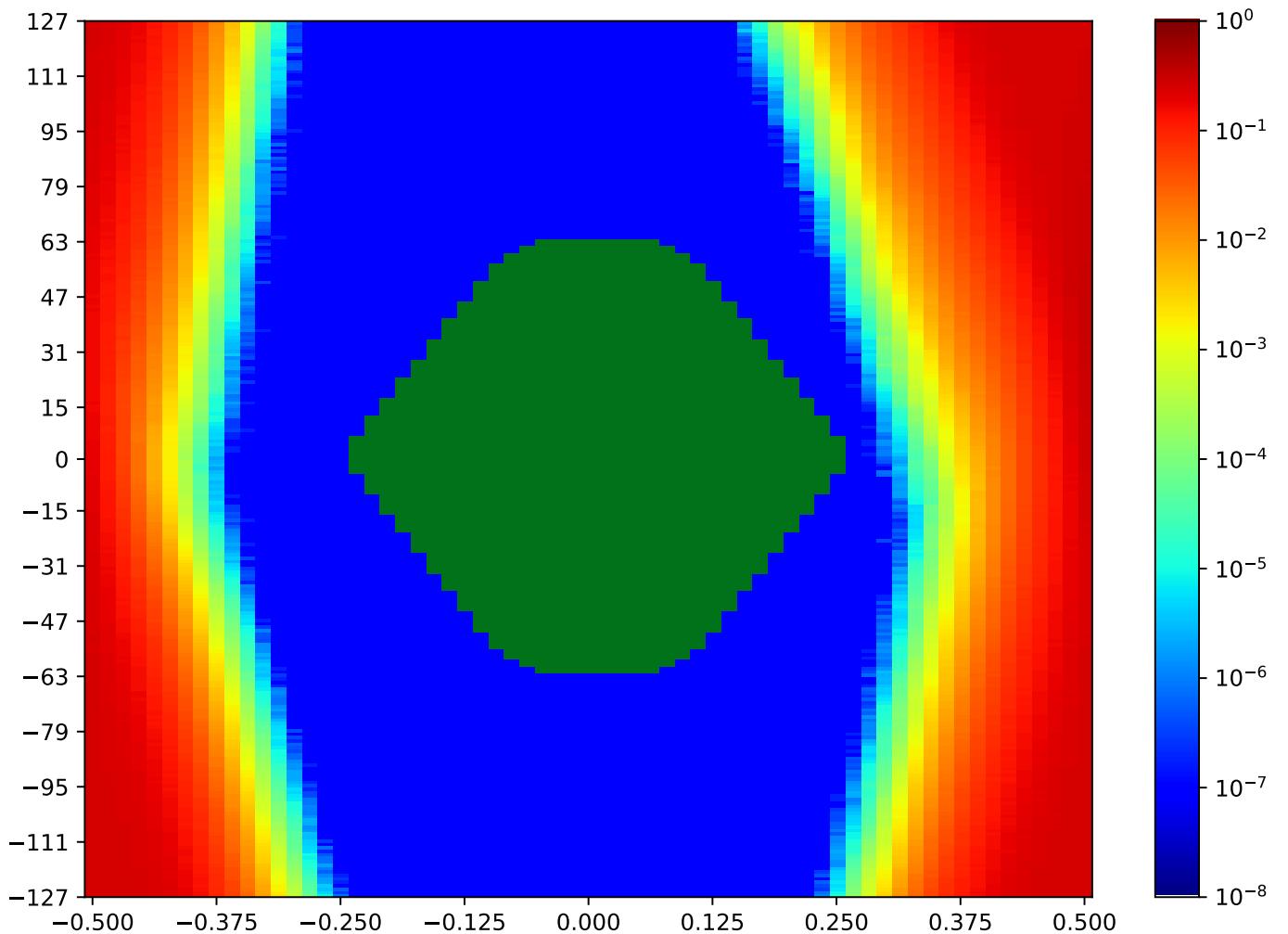


Figure 5.41: MSP_C_FPGA-TX4-00-RX7-00-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.2 MSP_C_FPGA-TX4-01-RX7-01-MSP_A_FPGA

Table 5.38: MSP_C_FPGA-TX4-01-RX7-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:02:38		2018-Sep-27 17:02:59	
Reset RX	OA	HO		VO	VO (%)
true	8861	39		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

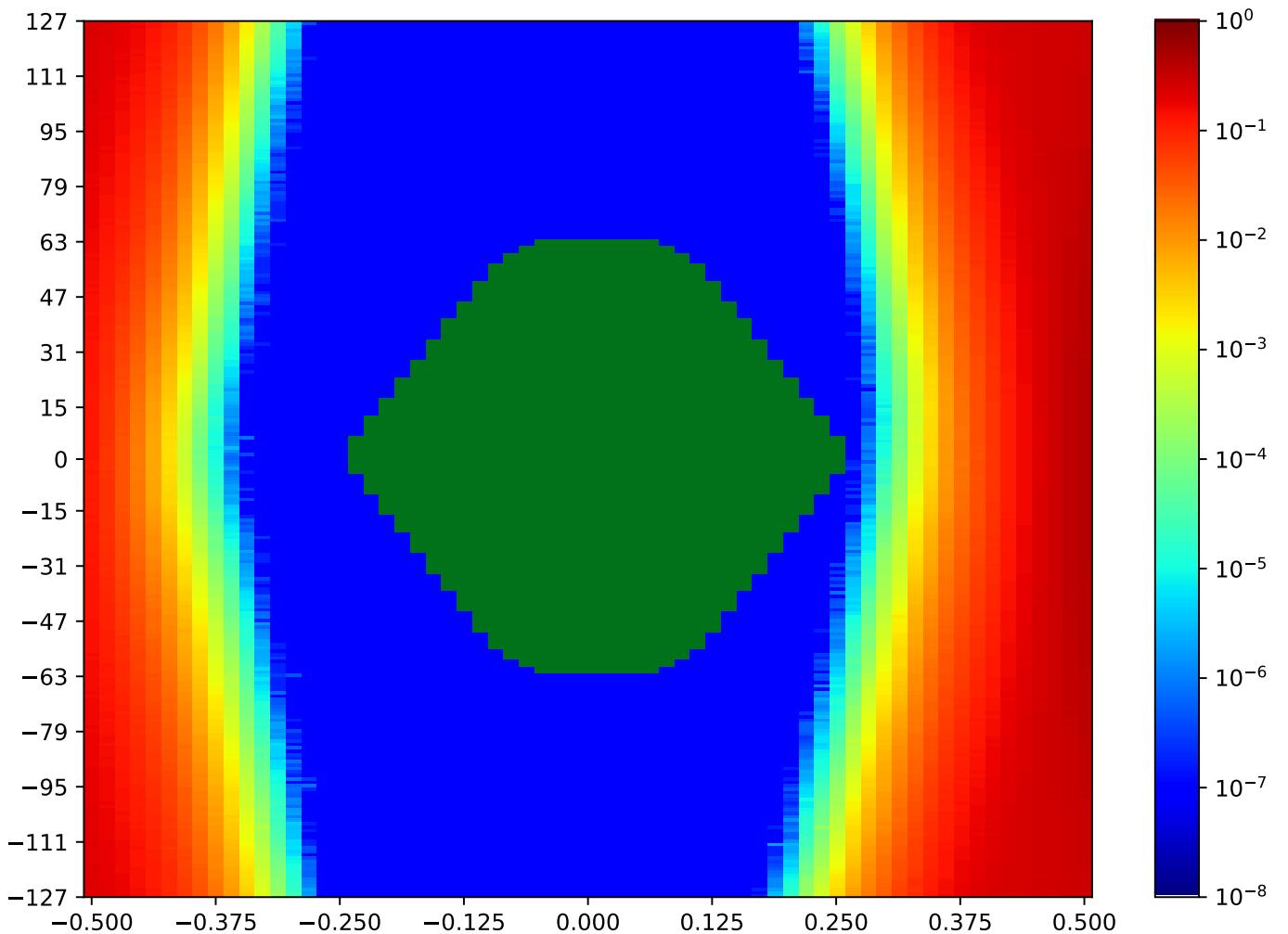


Figure 5.42: MSP_C_FPGA-TX4-01-RX7-01-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.3 MSP_C_FPGA-TX4-02-RX7-02-MSP_A_FPGA

Table 5.39: MSP_C_FPGA-TX4-02-RX7-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:04:20		2018-Sep-27 17:04:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8557	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

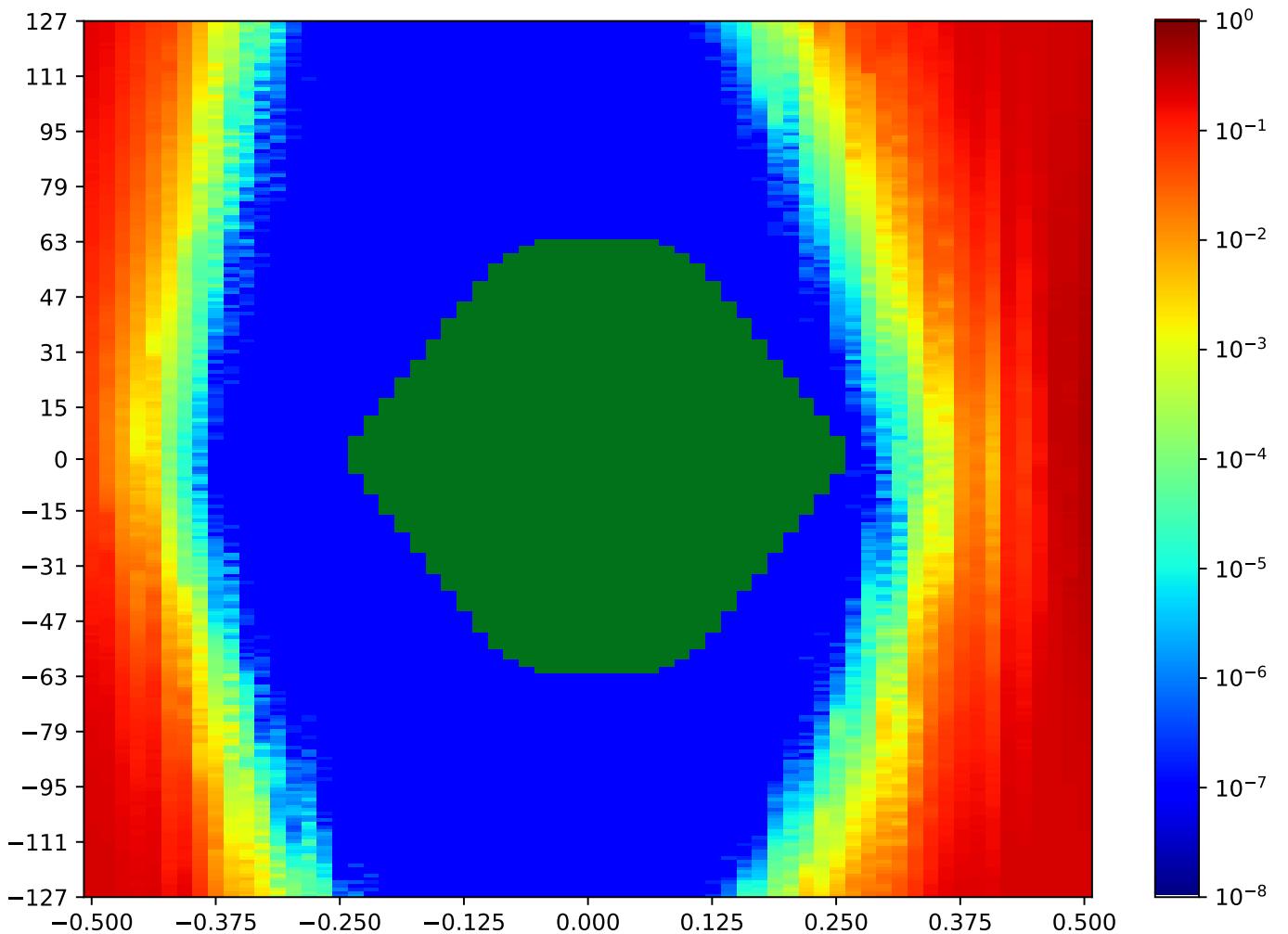


Figure 5.43: MSP_C_FPGA-TX4-02-RX7-02-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.4 MSP_C_FPGA-TX4-03-RX7-03-MSP_A_FPGA

Table 5.40: MSP_C_FPGA-TX4-03-RX7-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:02:18		2018-Sep-27 17:02:38	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8776	40		61.54%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

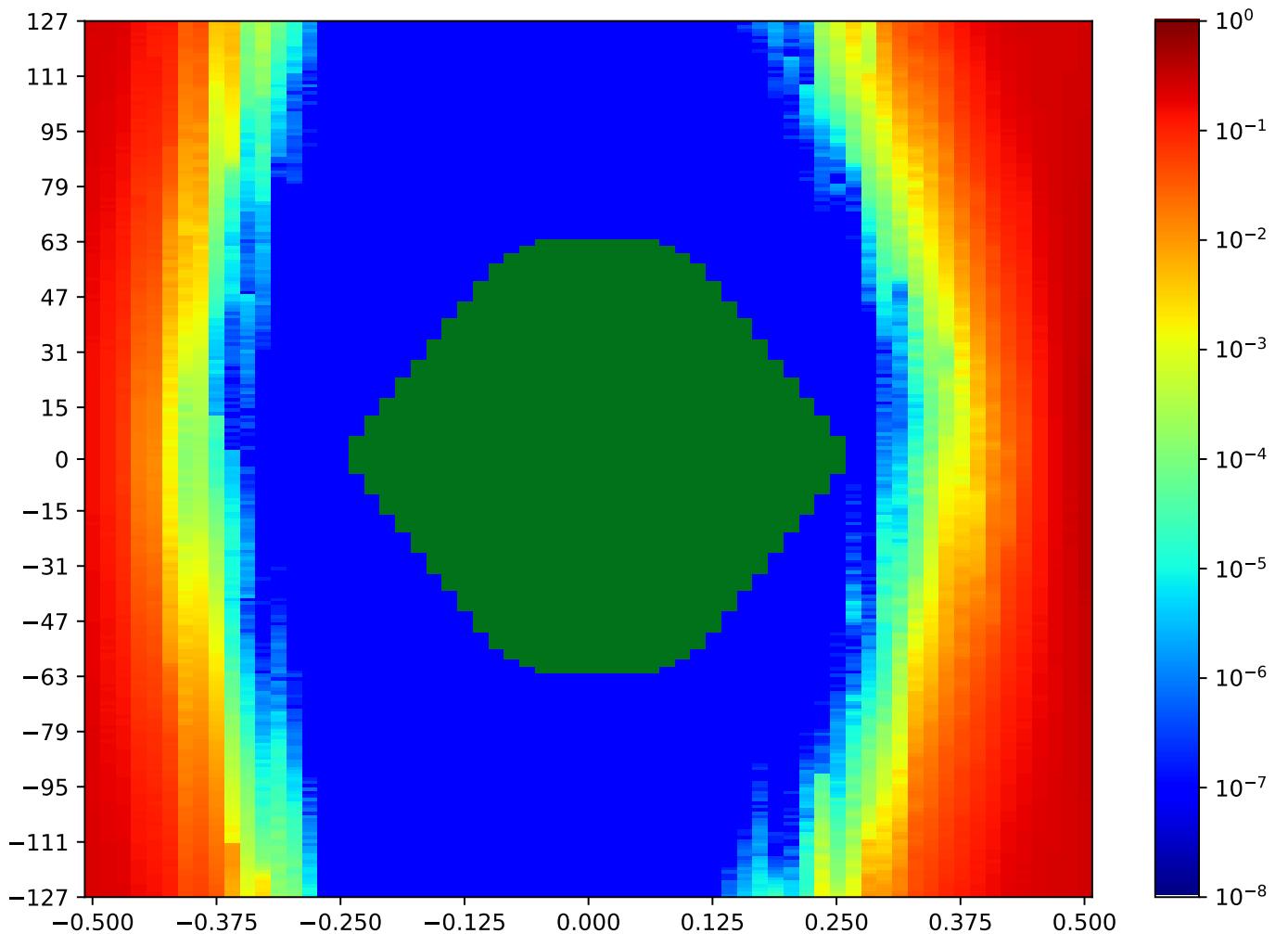


Figure 5.44: MSP_C_FPGA-TX4-03-RX7-03-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.5 MSP_C_FPGA-TX4-04-RX7-04-MSP_A_FPGA

Table 5.41: MSP_C_FPGA-TX4-04-RX7-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:05:21		2018-Sep-27 17:05:45	
Reset RX	OA	HO		VO	VO (%)
true	8511	40		61.54%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

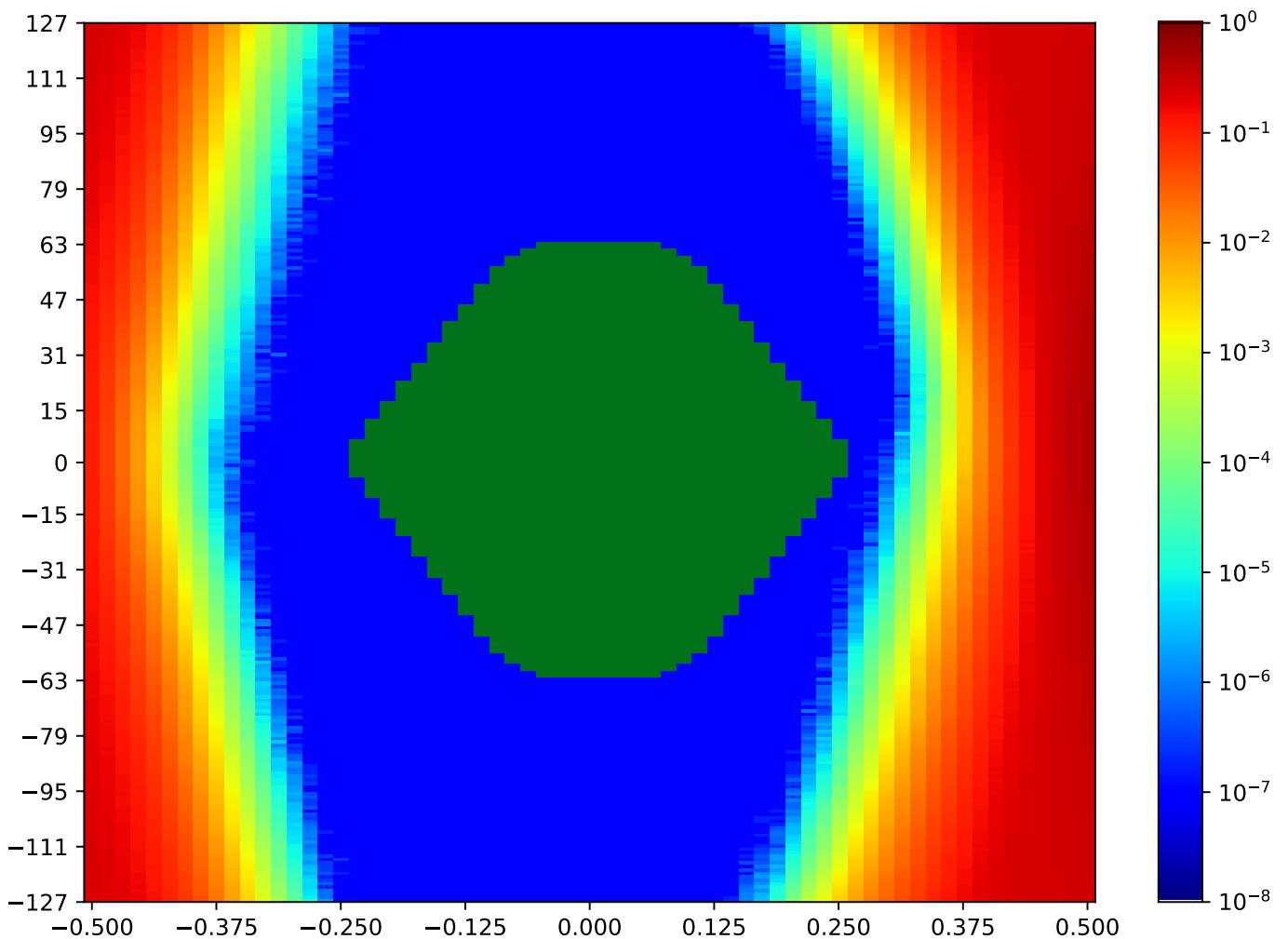


Figure 5.45: MSP_C_FPGA-TX4-04-RX7-04-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.6 MSP_C_FPGA-TX4-05-RX7-05-MSP_A_FPGA

Table 5.42: MSP_C_FPGA-TX4-05-RX7-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:02:59		2018-Sep-27 17:03:19	
Reset RX	OA	HO		VO	VO (%)
true	7992	37		56.92%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

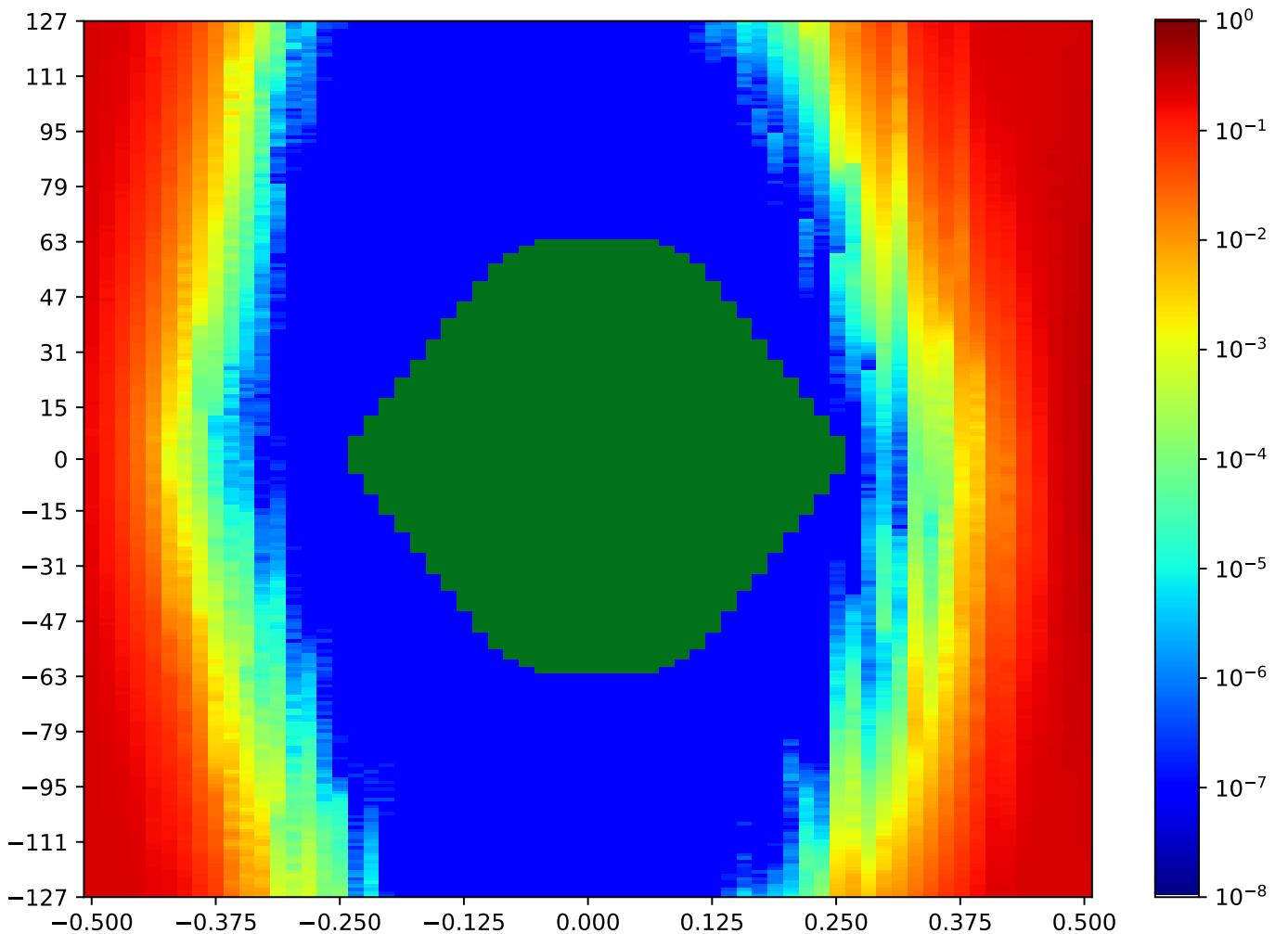


Figure 5.46: MSP_C_FPGA-TX4-05-RX7-05-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.7 MSP_C_FPGA-TX4-06-RX7-06-MSP_A_FPGA

Table 5.43: MSP_C_FPGA-TX4-06-RX7-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:06:05		2018-Sep-27 17:06:30	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9053	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

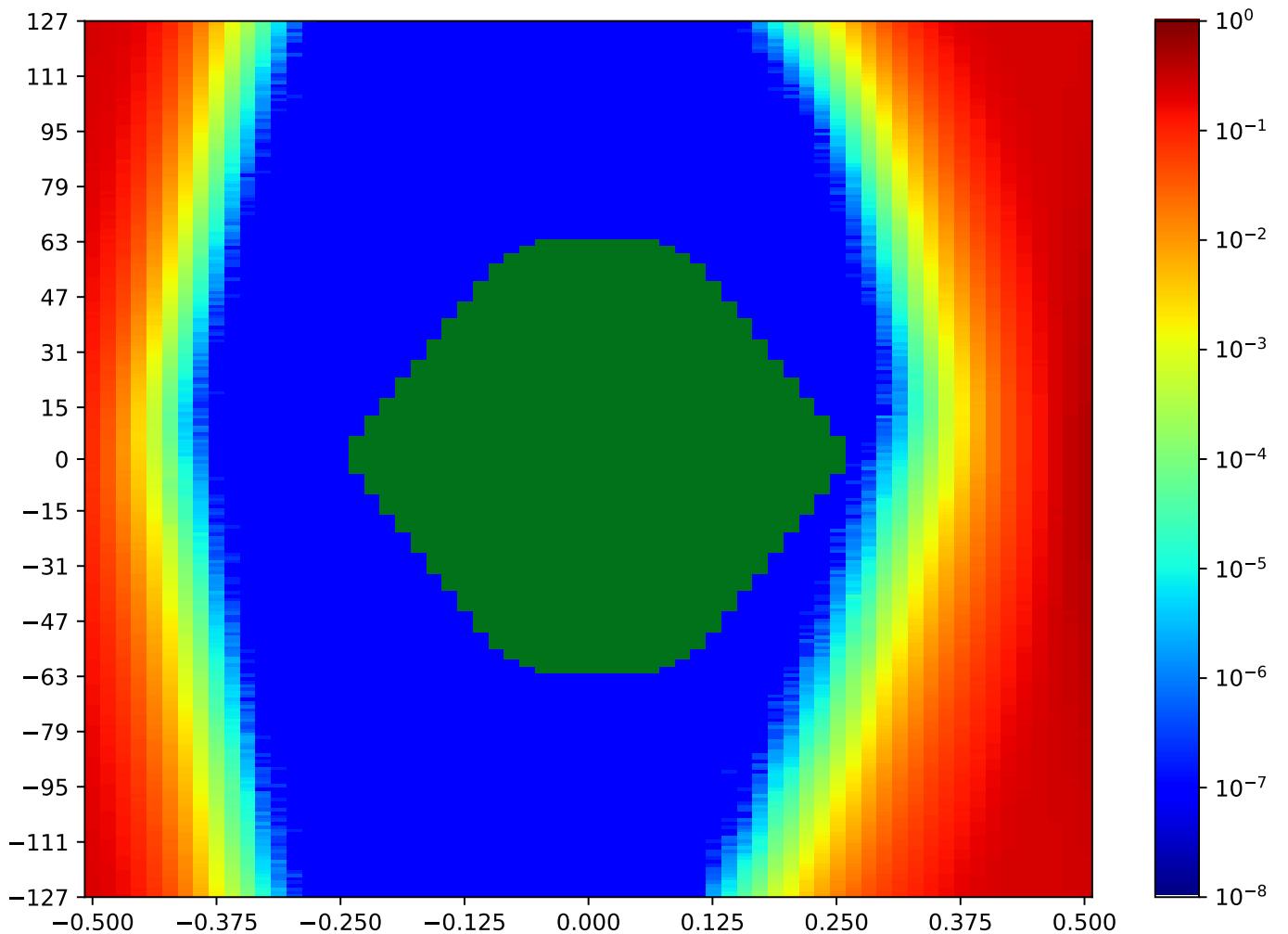


Figure 5.47: MSP_C_FPGA-TX4-06-RX7-06-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.8 MSP_C_FPGA-TX4-07-RX7-07-MSP_A_FPGA

Table 5.44: MSP_C_FPGA-TX4-07-RX7-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:03:40		2018-Sep-27 17:04:00	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9053	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

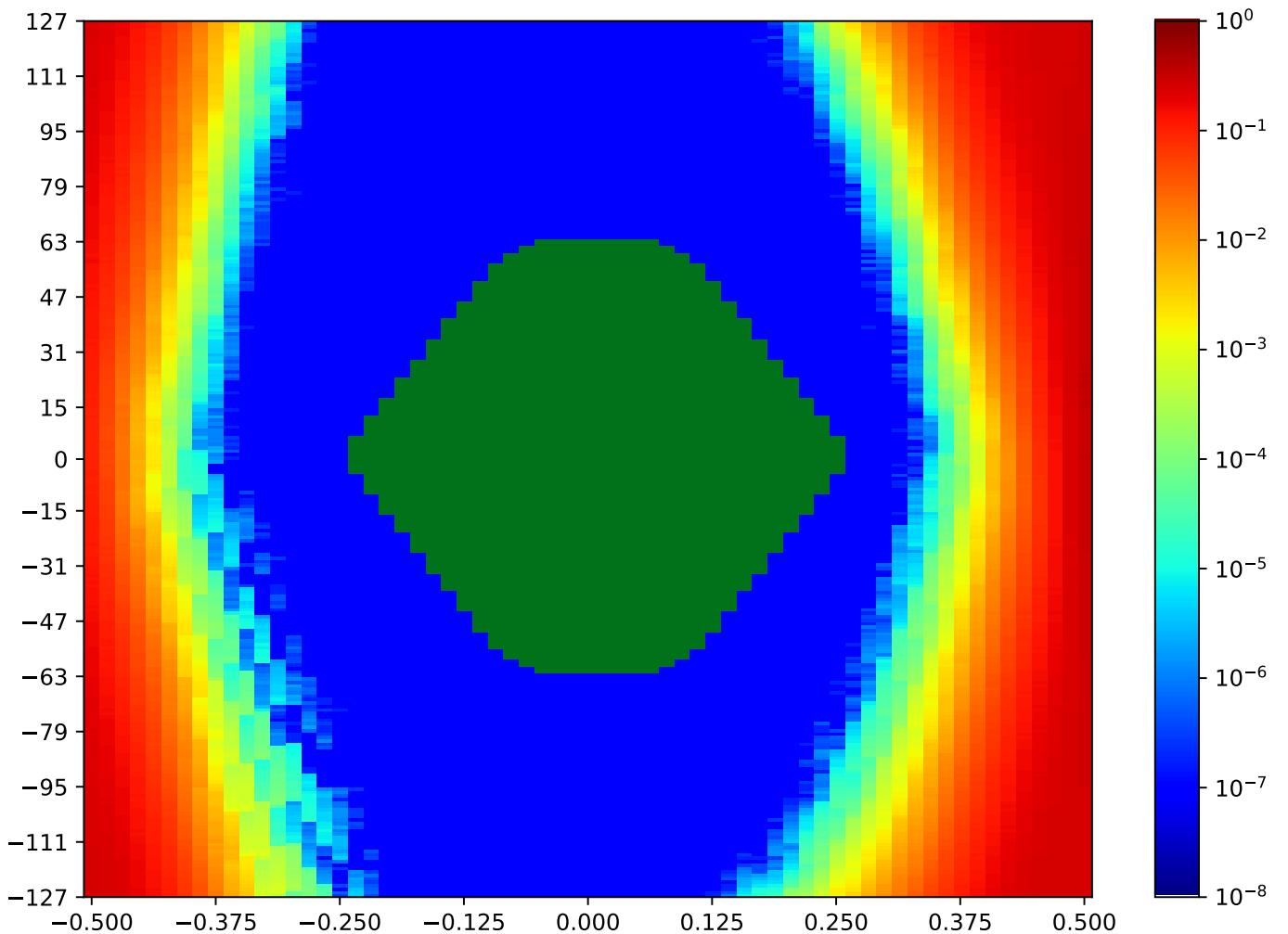


Figure 5.48: MSP_C_FPGA-TX4-07-RX7-07-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.9 MSP_C_FPGA-TX4-08-RX7-08-MSP_A_FPGA

Table 5.45: MSP_C_FPGA-TX4-08-RX7-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:05:45		2018-Sep-27 17:06:05	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9389	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

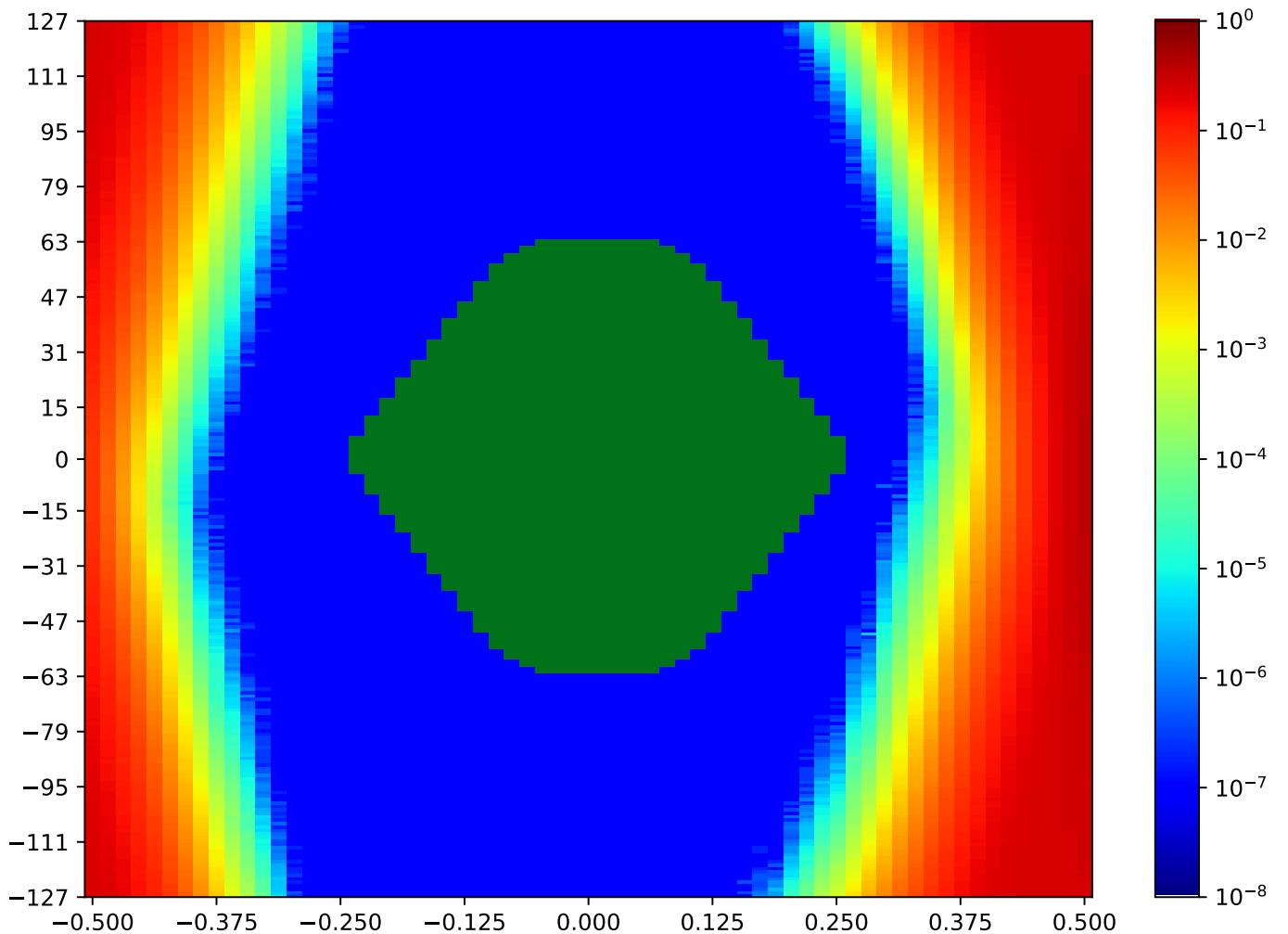


Figure 5.49: MSP_C_FPGA-TX4-08-RX7-08-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.10 MSP_C_FPGA-TX4-09-RX7-09-MSP_A_FPGA

Table 5.46: MSP_C_FPGA-TX4-09-RX7-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:04:00		2018-Sep-27 17:04:20	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9187	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

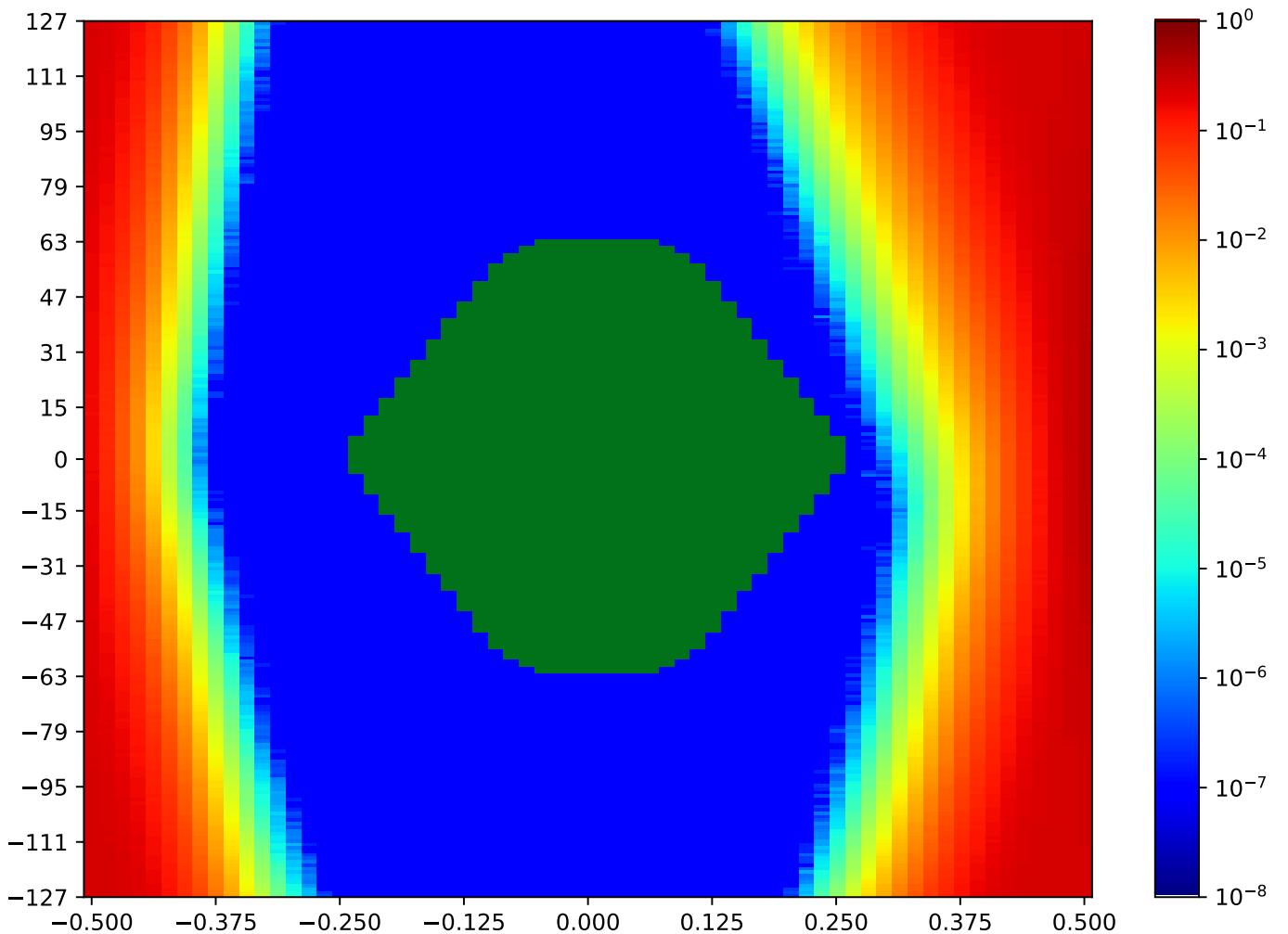


Figure 5.50: MSP_C_FPGA-TX4-09-RX7-09-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.11 MSP_C_FPGA-TX4-10-RX7-10-MSP_A_FPGA

Table 5.47: MSP_C_FPGA-TX4-10-RX7-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:05:01		2018-Sep-27 17:05:21	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8629	40		61.54%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

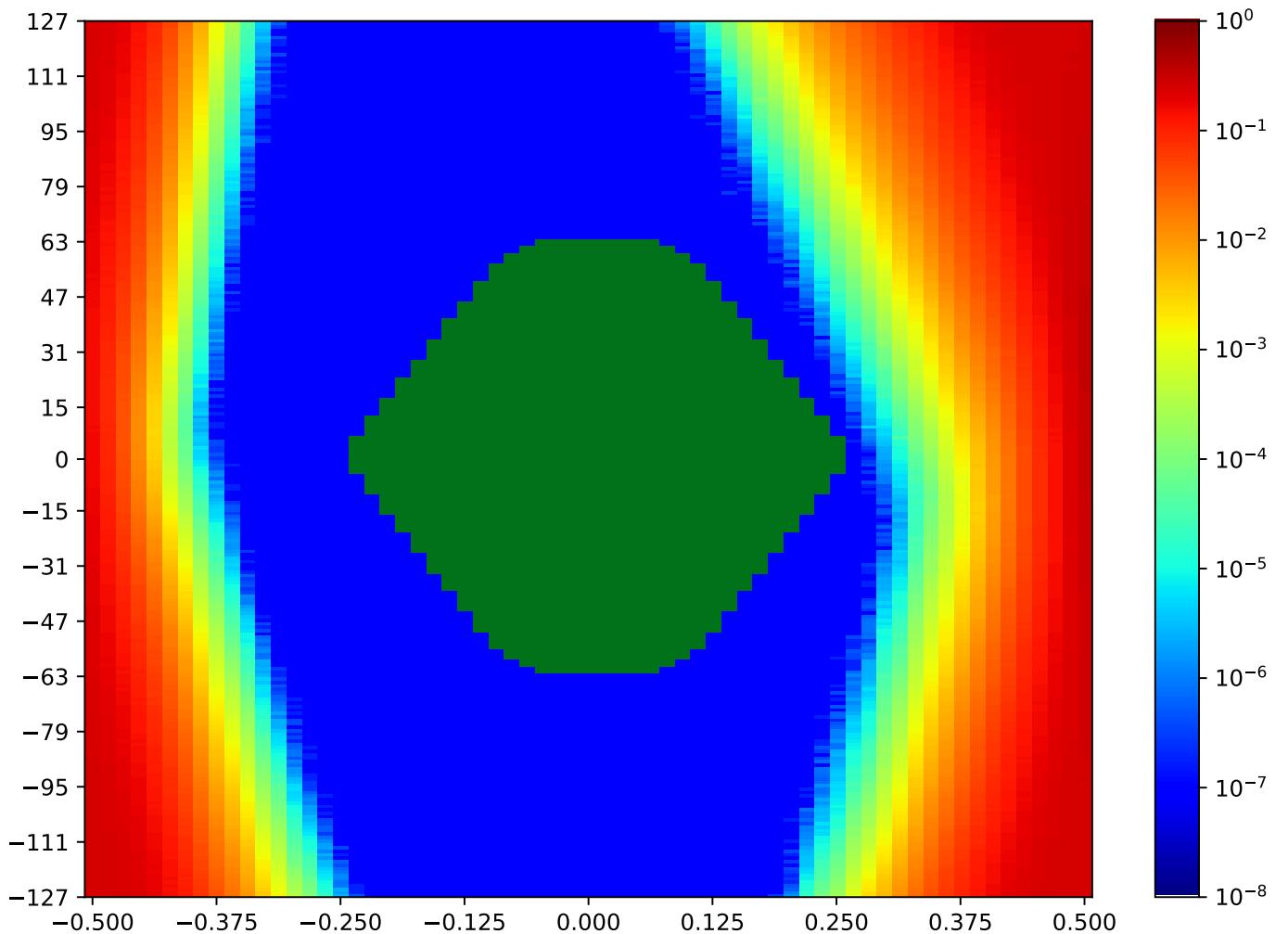


Figure 5.51: MSP_C_FPGA-TX4-10-RX7-10-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.4.12 MSP_C_FPGA-TX4-11-RX7-11-MSP_A_FPGA

Table 5.48: MSP_C_FPGA-TX4-11-RX7-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:04:41		2018-Sep-27 17:05:01	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8902	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x00009 SVN: 16356	

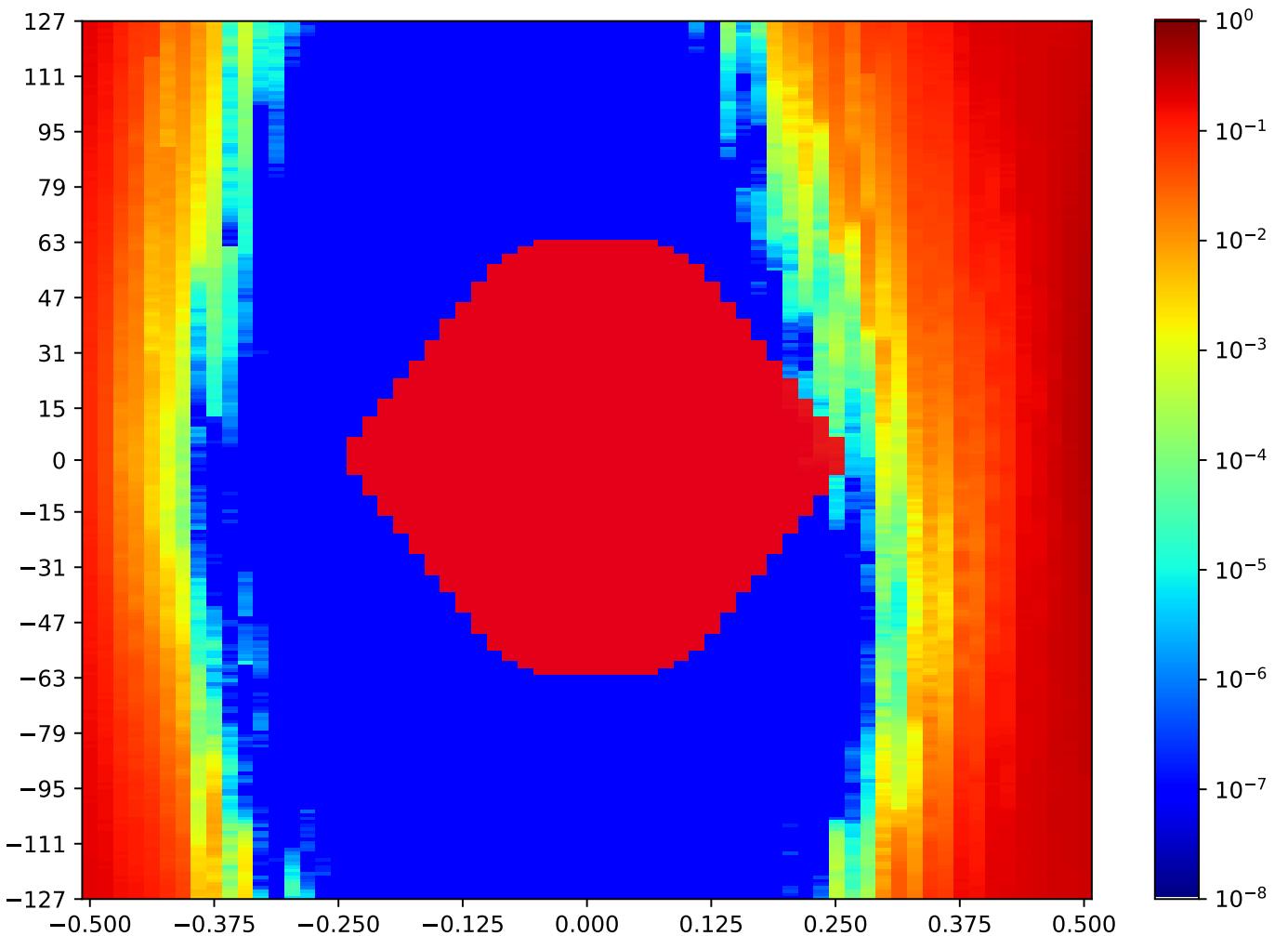


Figure 5.52: MSP_C_FPGA-TX4-11-RX7-11-MSP_A_FPGA

Call back to summary Figure 5.40. Sibling eye diagrams: V2-6.4.

5.5 Partial TRP TX5 MSP_A RX5 Minipod Loopback

A cross-reference to Figure 5.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

Next summary Figure 5.62.

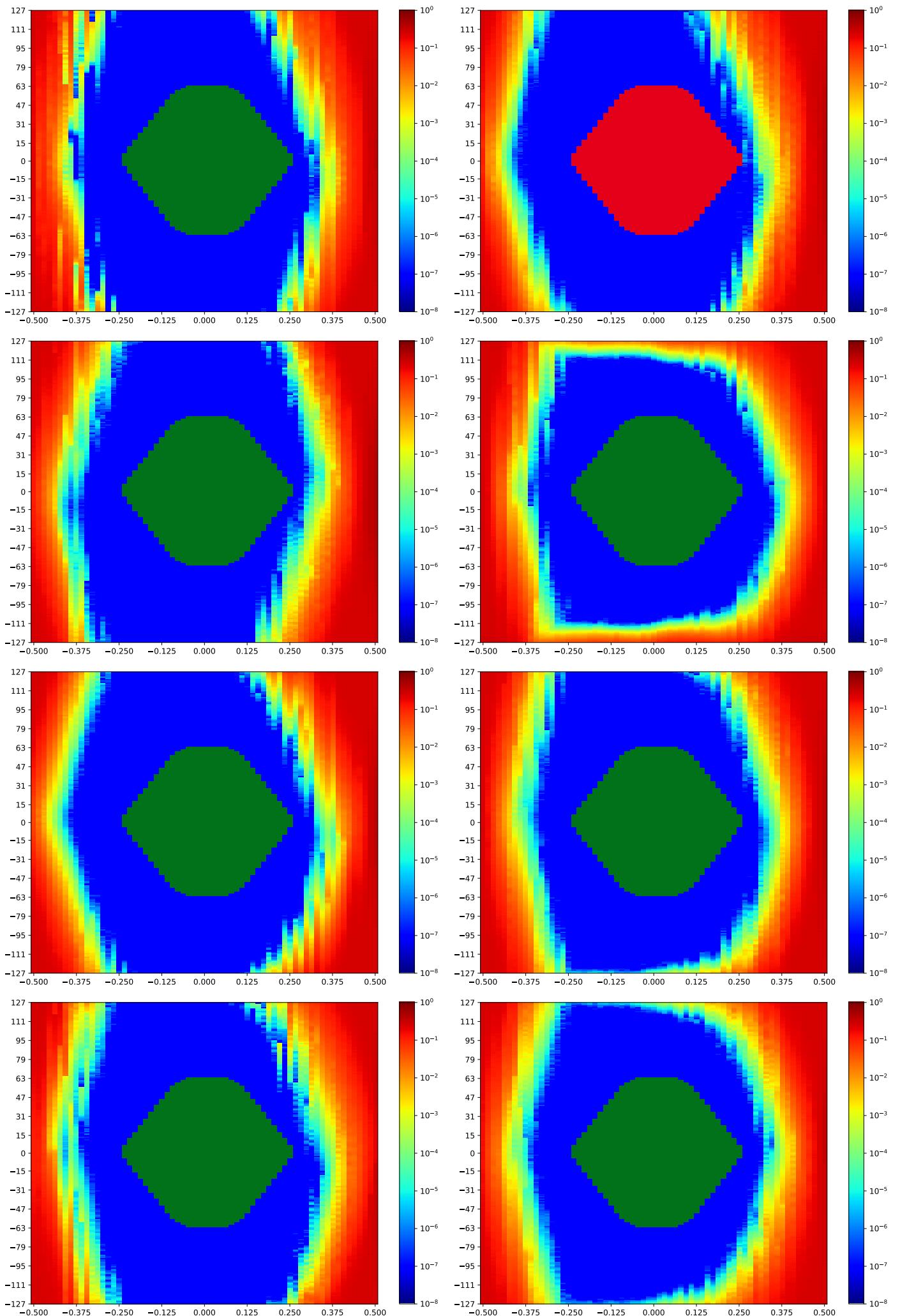


Figure 5.53: Partial TRP TX5 MSP_A RX5 Minipod Loopback
963

5.5.1 TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

Table 5.49: TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:07:31		2018-Sep-27 17:07:51	
Reset RX	OA	HO		VO	VO (%)
true	9257	44		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

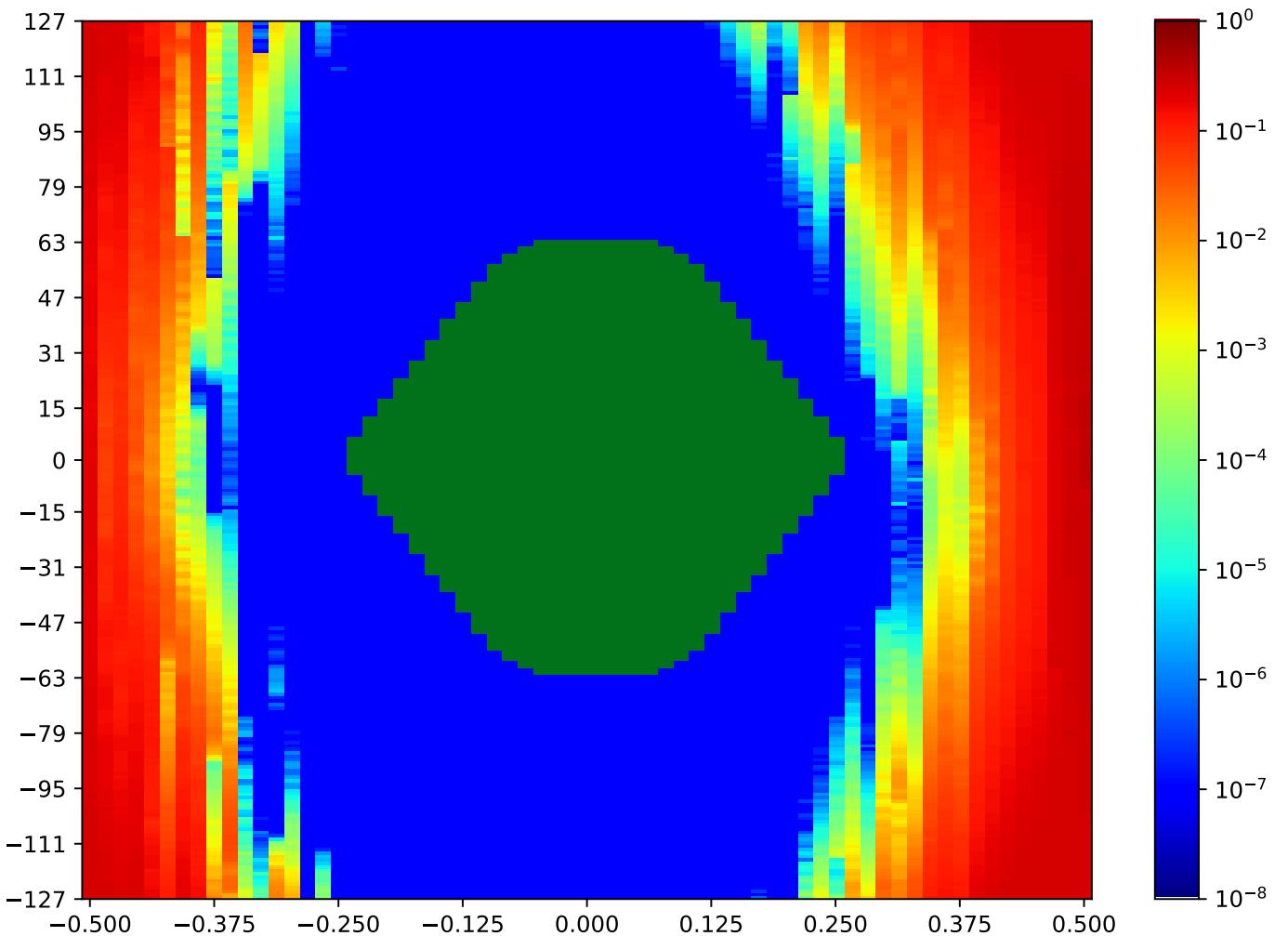


Figure 5.54: TRP_FPGA-TX5-00-RX5-00-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.5.2 TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

Table 5.50: TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:06:50		2018-Sep-27 17:07:11	
Reset RX	OA	HO		VO	VO (%)
true	8865	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

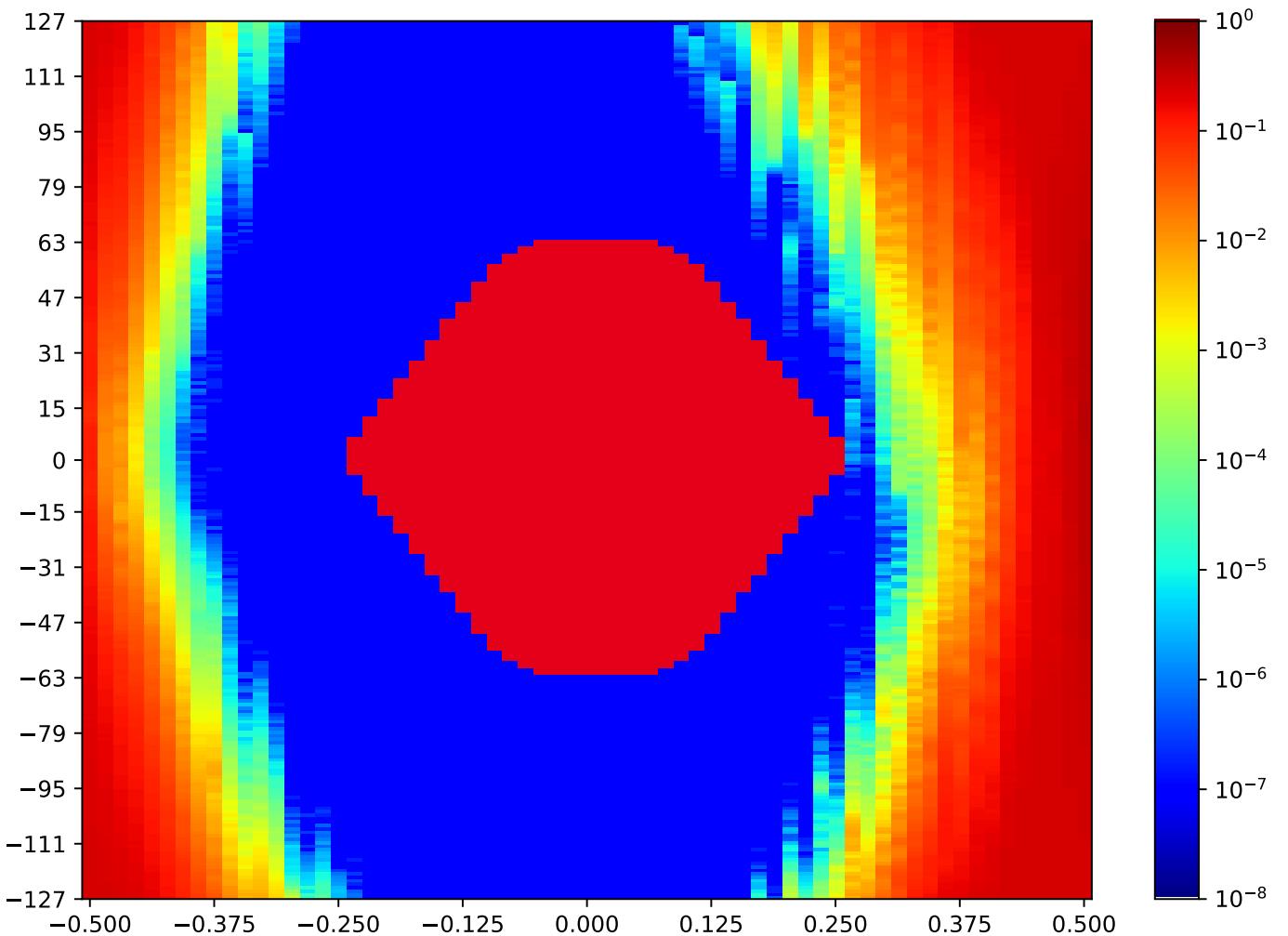


Figure 5.55: TRP_FPGA-TX5-01-RX5-01-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.5.3 TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

Table 5.51: TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:08:12		2018-Sep-27 17:08:32	
Reset RX	OA	HO		VO	VO (%)
true	8728	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

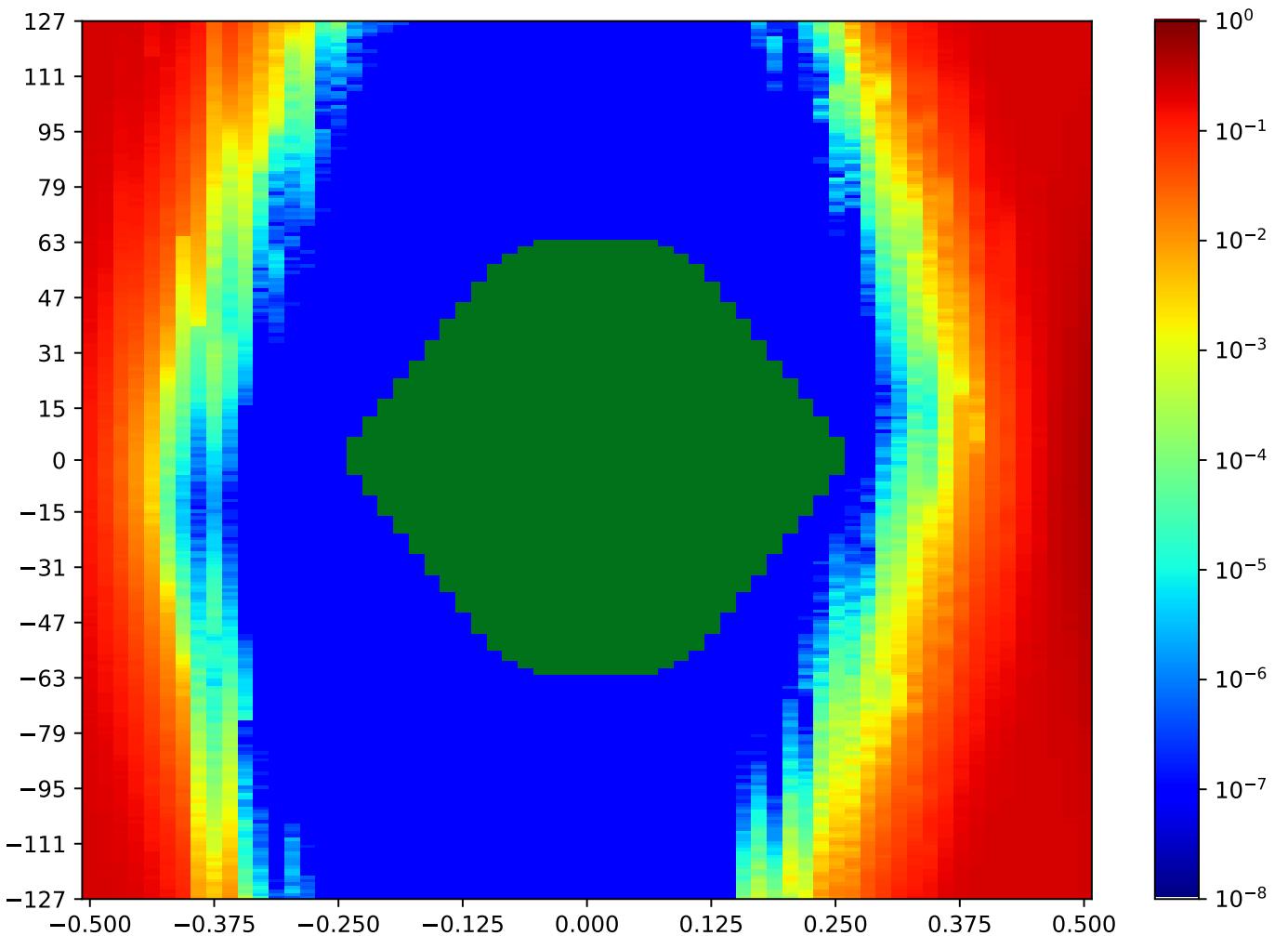


Figure 5.56: TRP_FPGA-TX5-02-RX5-02-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.5.4 TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

Table 5.52: TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:07:11		2018-Sep-27 17:07:31	
Reset RX	OA	HO		VO	VO (%)
true	7758	43		66.15%	218 85.49%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

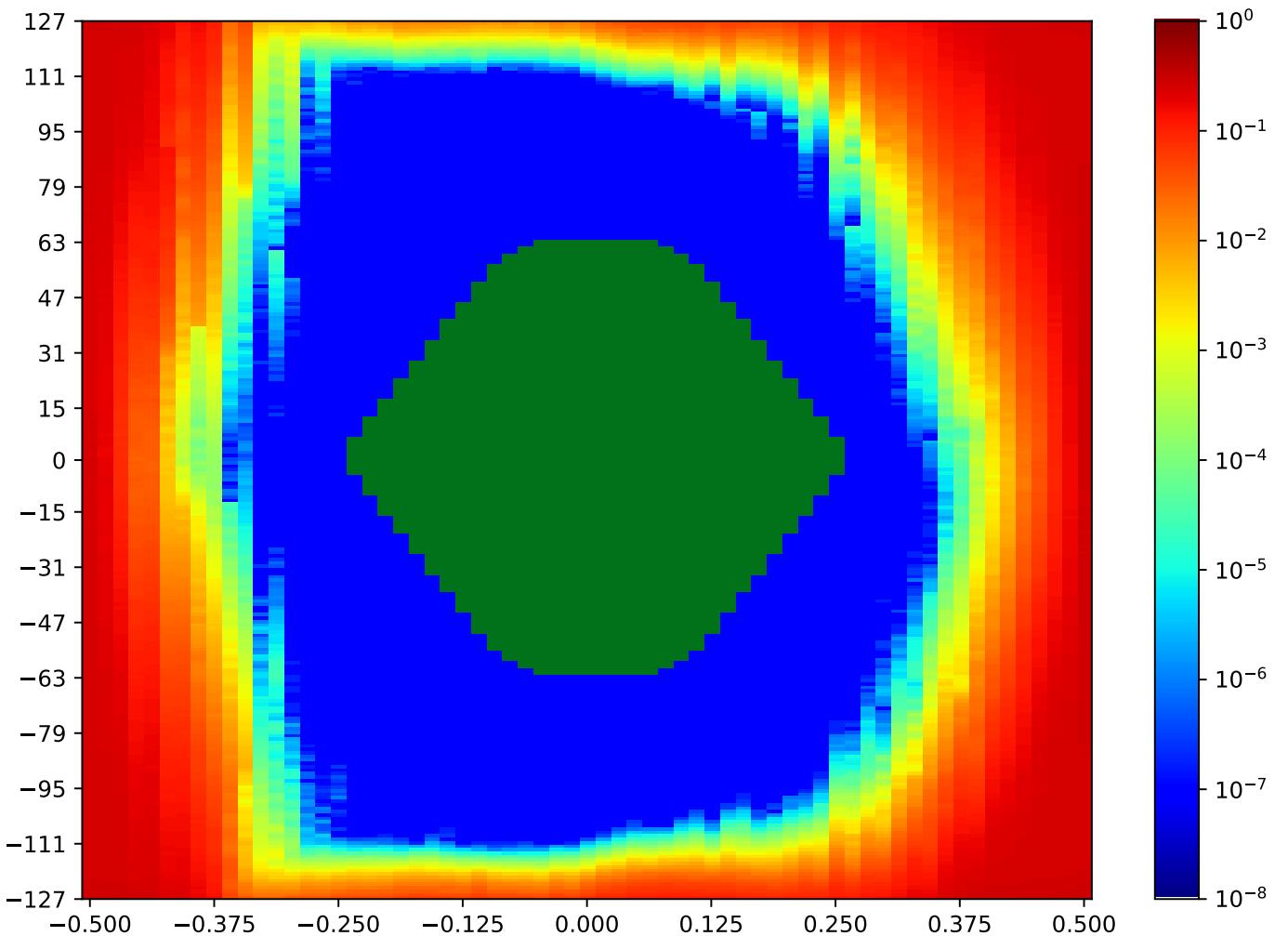


Figure 5.57: TRP_FPGA-TX5-03-RX5-03-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.5.5 TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

Table 5.53: TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:08:53		2018-Sep-27 17:09:13	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9135	45		69.23%	253 99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

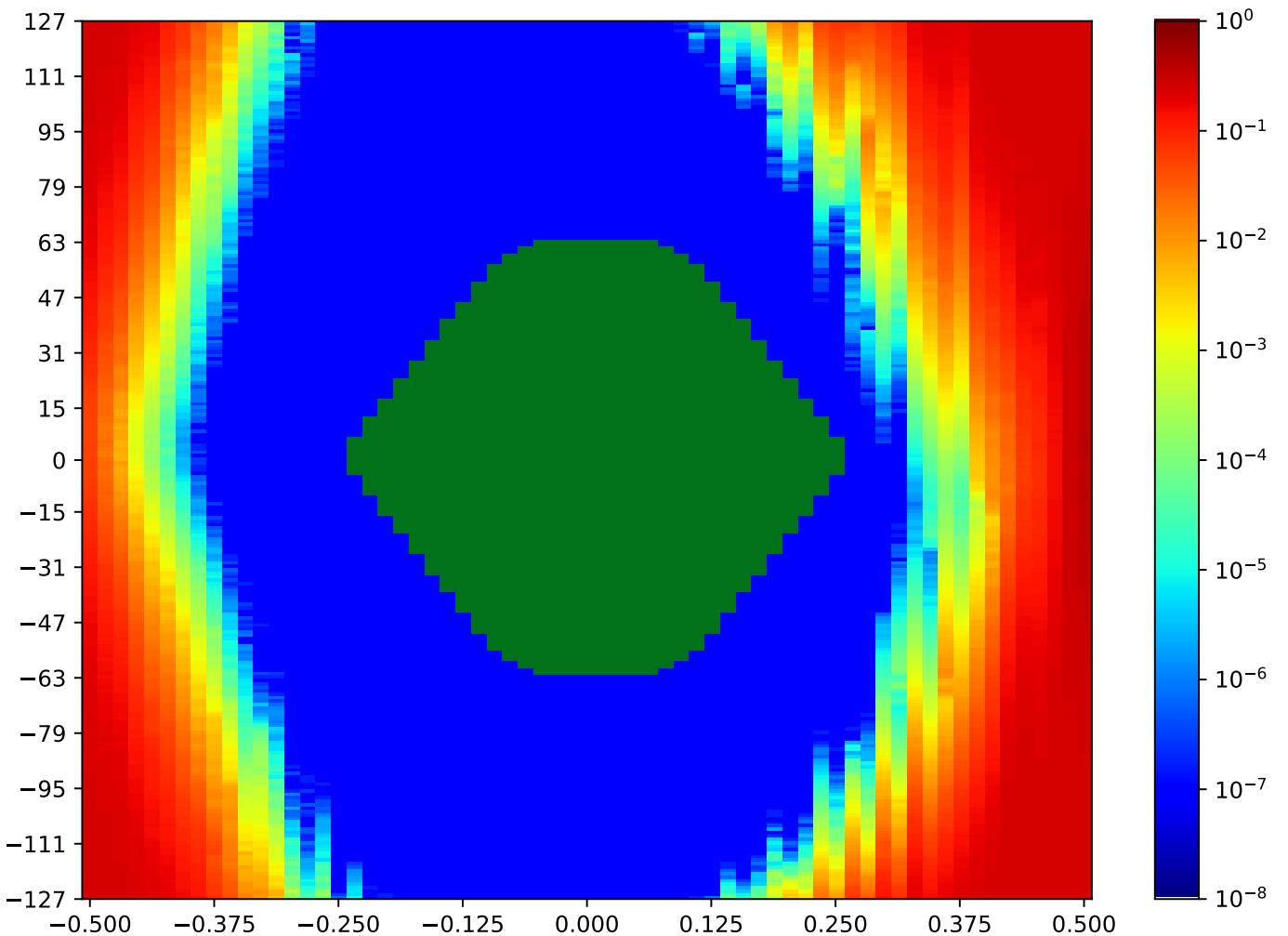


Figure 5.58: TRP_FPGA-TX5-04-RX5-04-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.5.6 TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

Table 5.54: TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:06:30		2018-Sep-27 17:06:50	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8394	40		61.54%	248 96.86%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

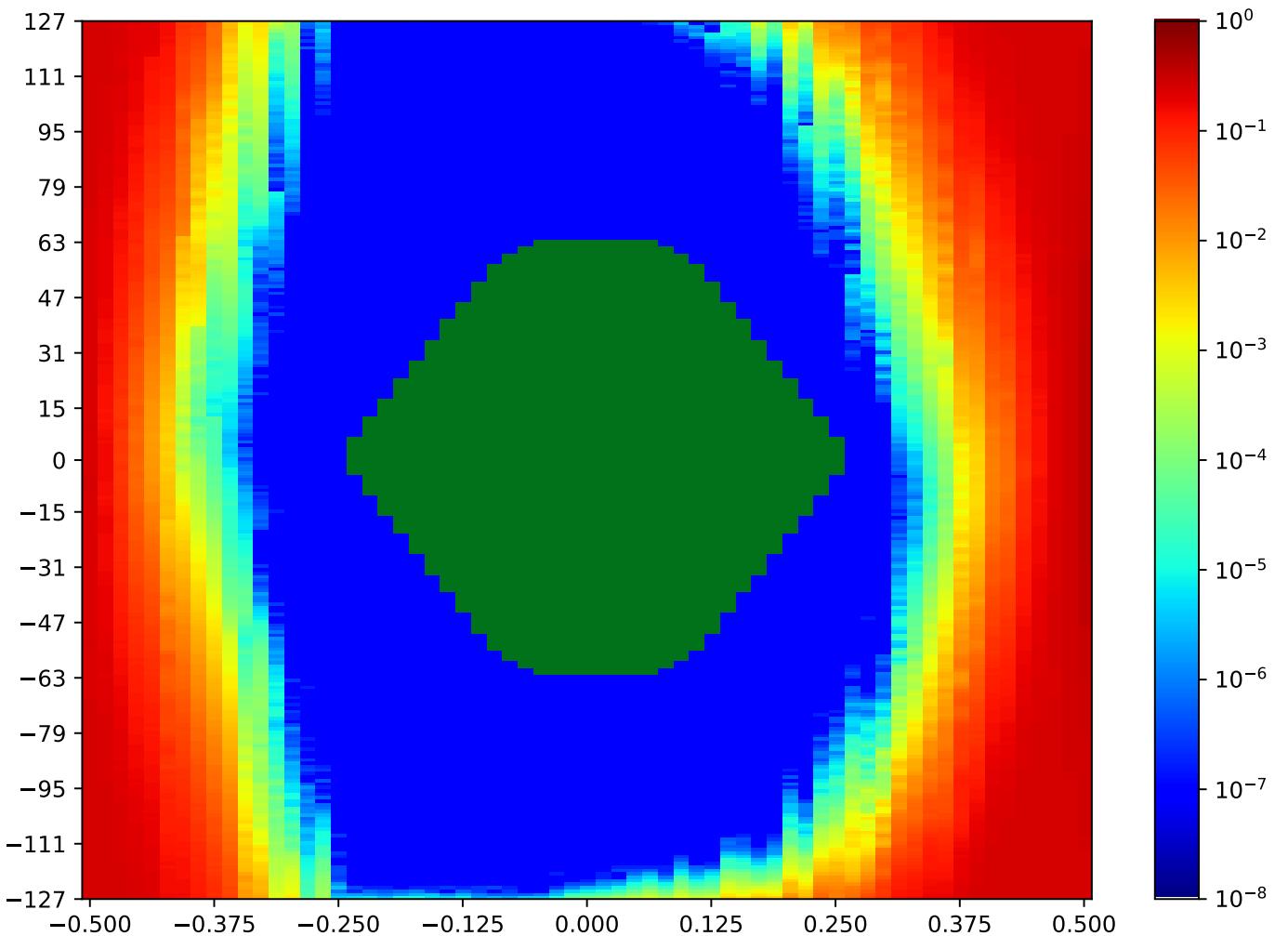


Figure 5.59: TRP_FPGA-TX5-05-RX5-05-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.5.7 TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

Table 5.55: TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:07:51		2018-Sep-27 17:08:12	
Reset RX	OA	HO		VO	VO (%)
true	9004	42		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

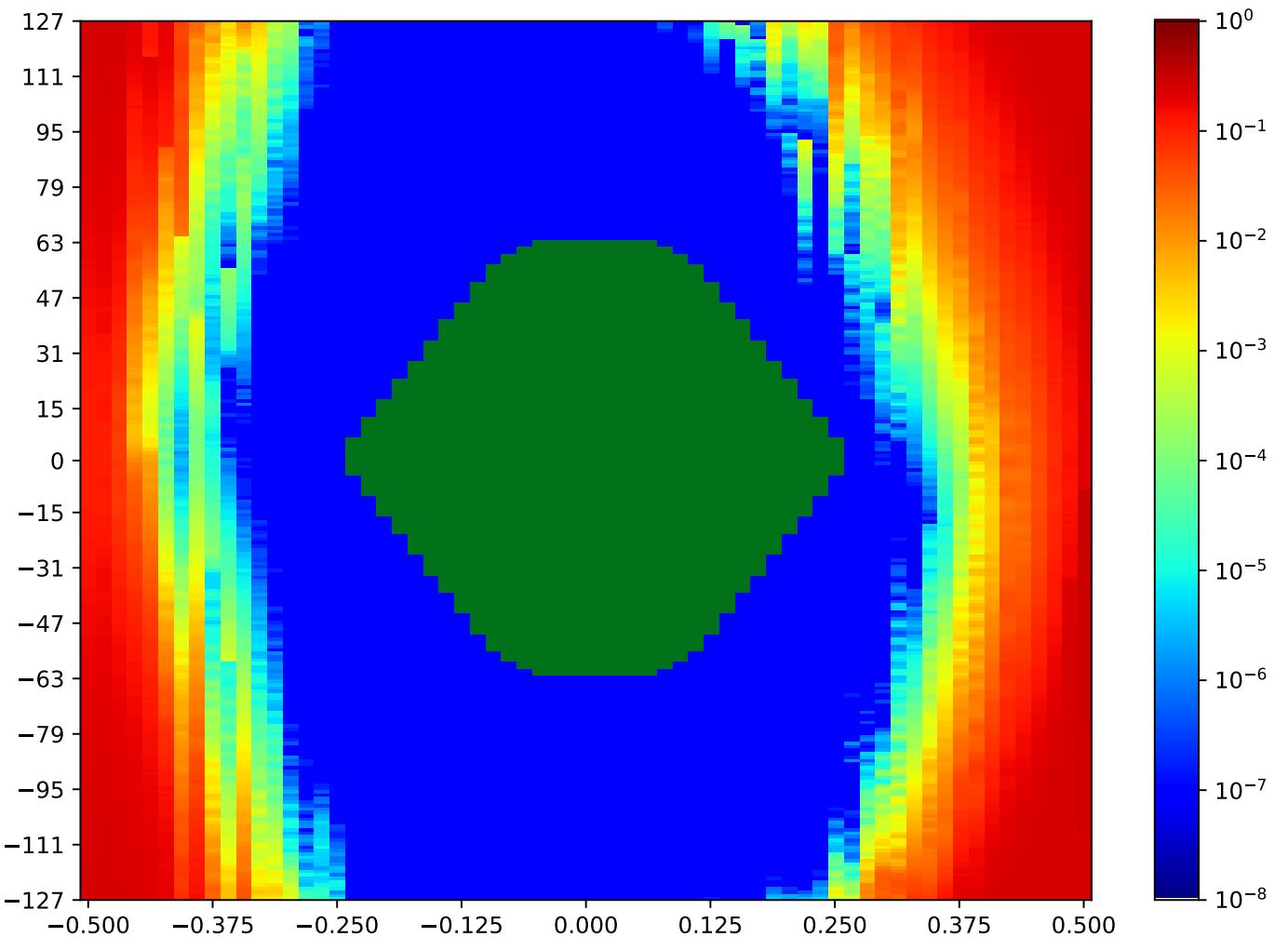


Figure 5.60: TRP_FPGA-TX5-06-RX5-06-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.5.8 TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

Table 5.56: TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 17:08:32		2018-Sep-27 17:08:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8189	42	64.62%	237	92.55%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

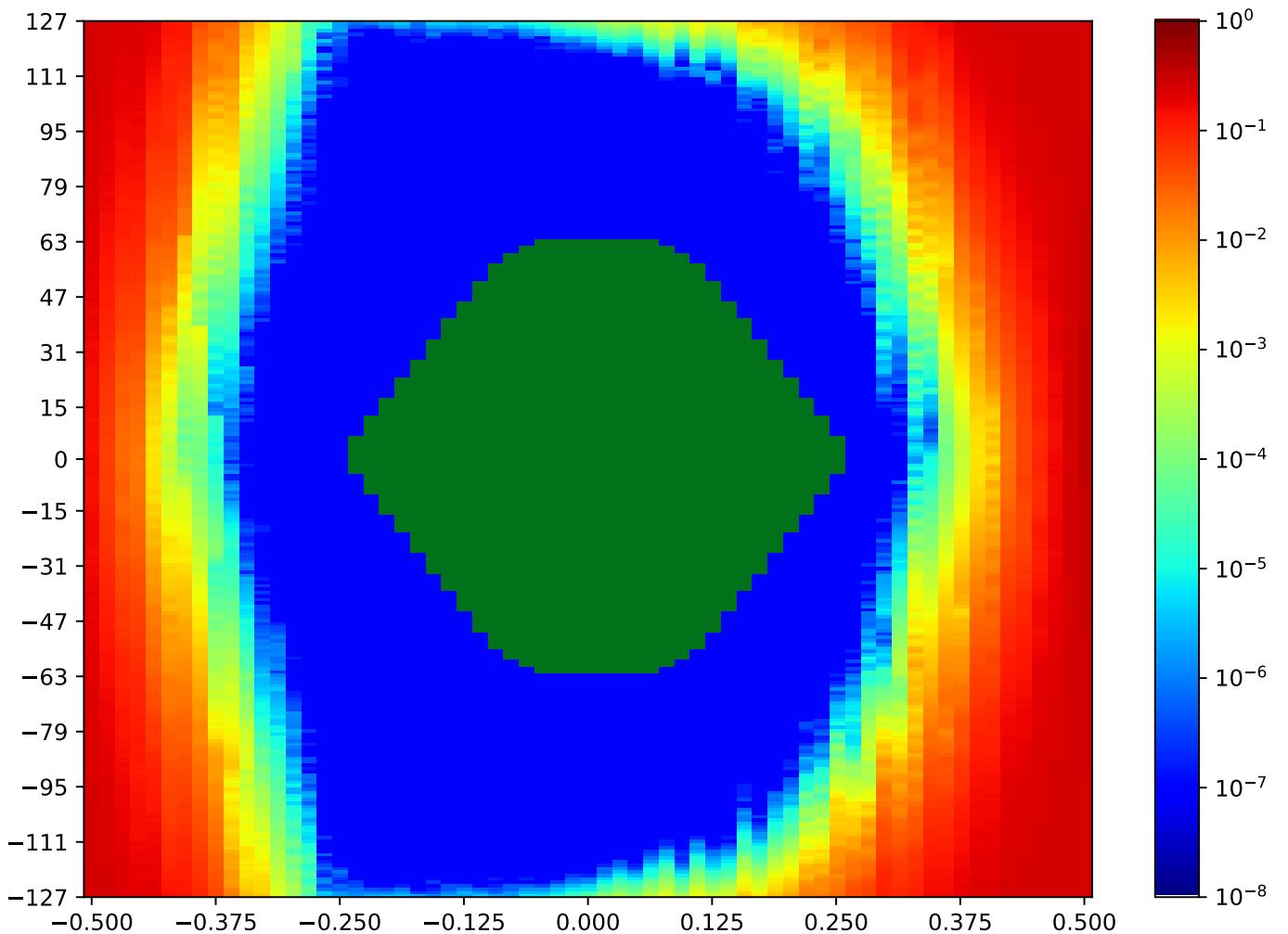


Figure 5.61: TRP_FPGA-TX5-07-RX5-07-MSP_A_FPGA

Call back to summary Figure 5.53. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.6 TRP J1 QSFP Loopback

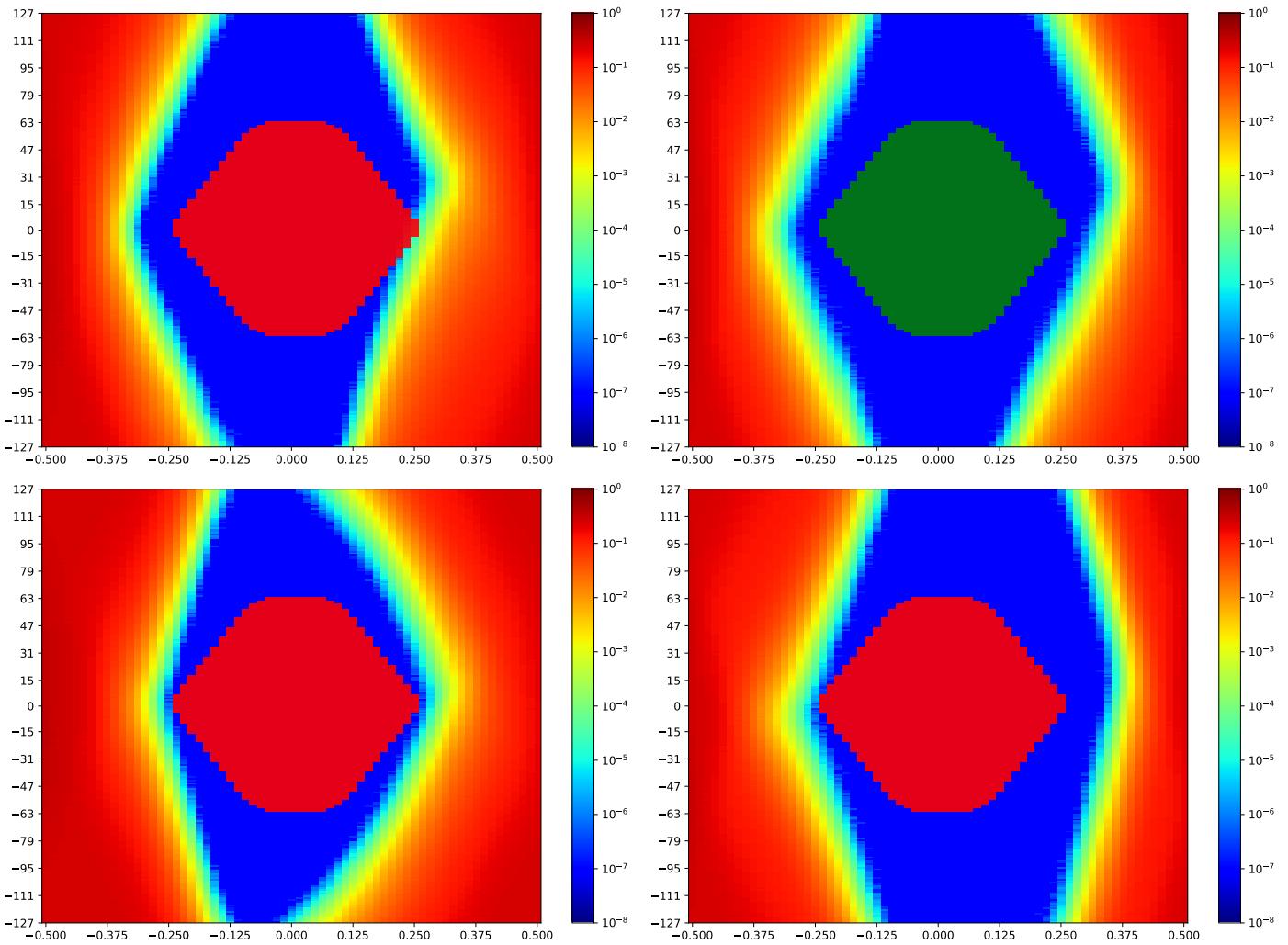


Figure 5.62: TRP J1 QSFP Loopback

A cross-reference to Figure 5.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.
Next summary Figure 5.67.

5.6.1 TRP_FPGA-J1-00–J1-00-TRP_FPGA

Table 5.57: TRP_FPGA-J1-00–J1-00-TRP_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:09:13			2018-Sep-27 17:09:33	
Reset RX	OA	HO	HO (%)		VO	VO (%)
true	6320	34	52.31%		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

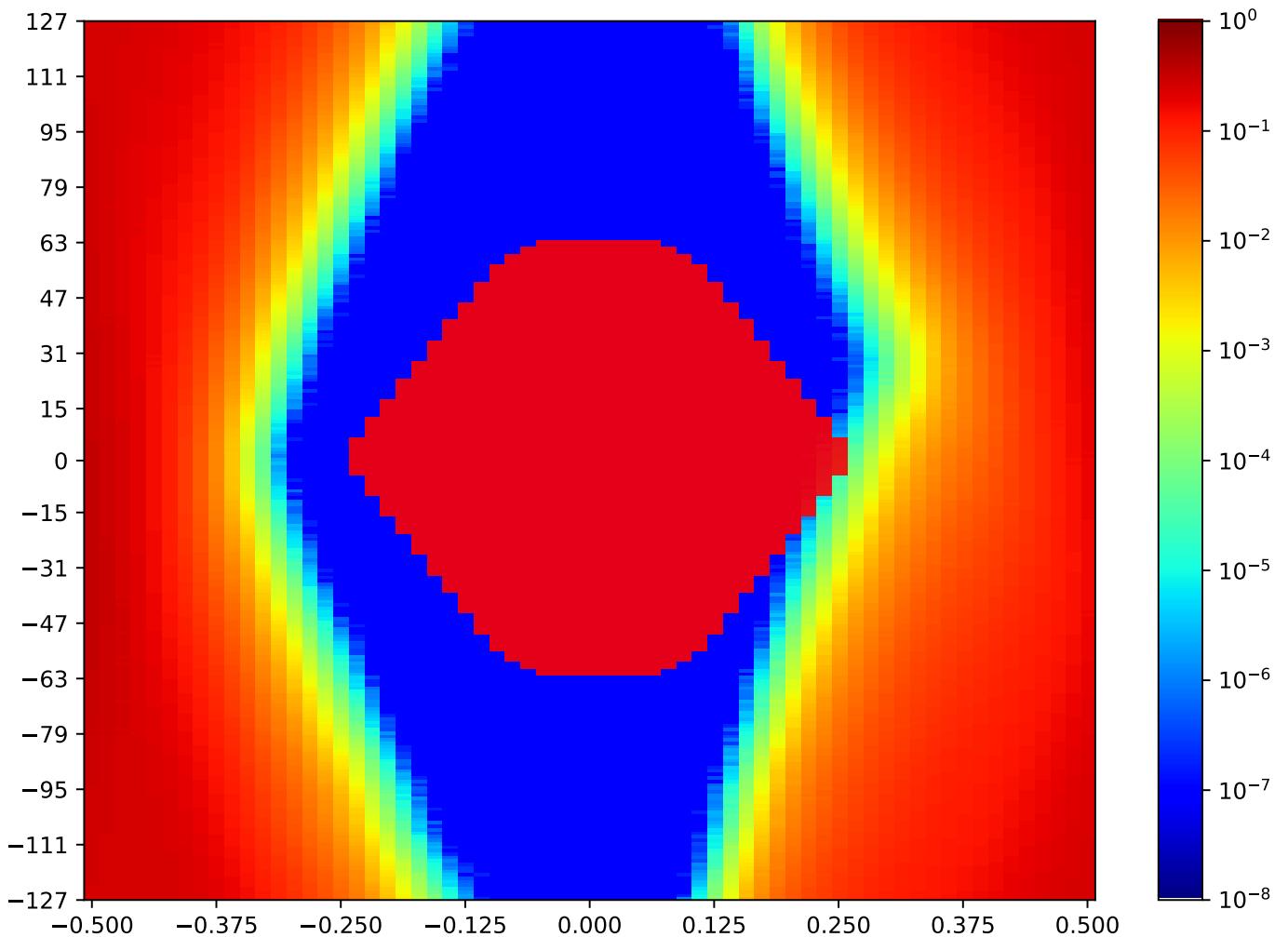


Figure 5.63: TRP_FPGA-J1-00–J1-00-TRP_FPGA

Call back to summary Figure 5.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.6.2 TRP_FPGA-J1-01–J1-01-TRP_FPGA

Table 5.58: TRP_FPGA-J1-01–J1-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:09:33		2018-Sep-27 17:09:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6746	36	55.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

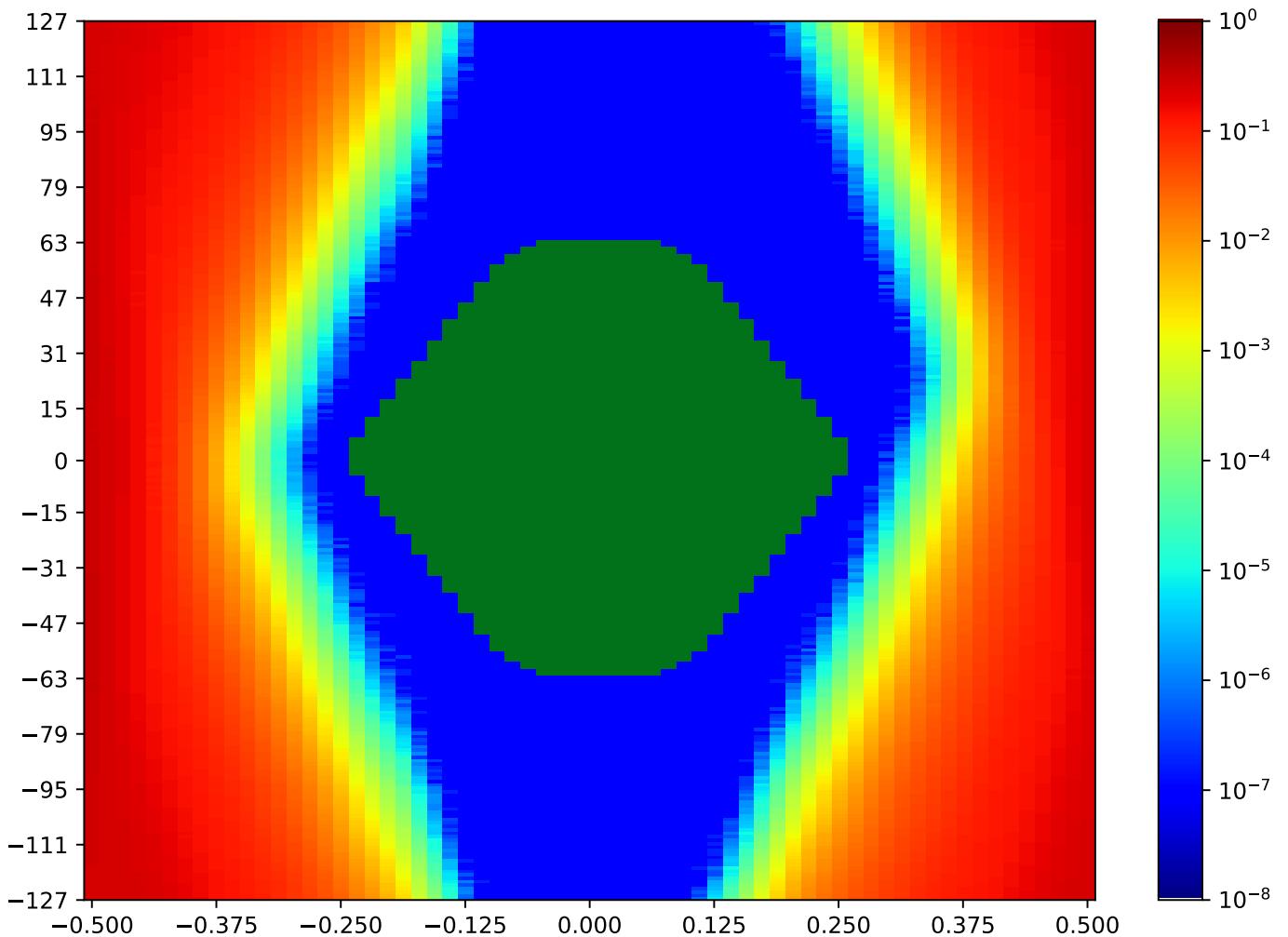


Figure 5.64: TRP_FPGA-J1-01–J1-01-TRP_FPGA

Call back to summary Figure 5.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.6.3 TRP_FPGA-J1-02–J1-02-TRP_FPGA

Table 5.59: TRP_FPGA-J1-02–J1-02-TRP_FPGA

SW Version	GT Type	Date and Time Started			Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:09:54			2018-Sep-27 17:10:15	
Reset RX	OA	HO	HO (%)	VO	VO (%)	
true	5311	31	47.69%	243	94.12%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info		
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0		

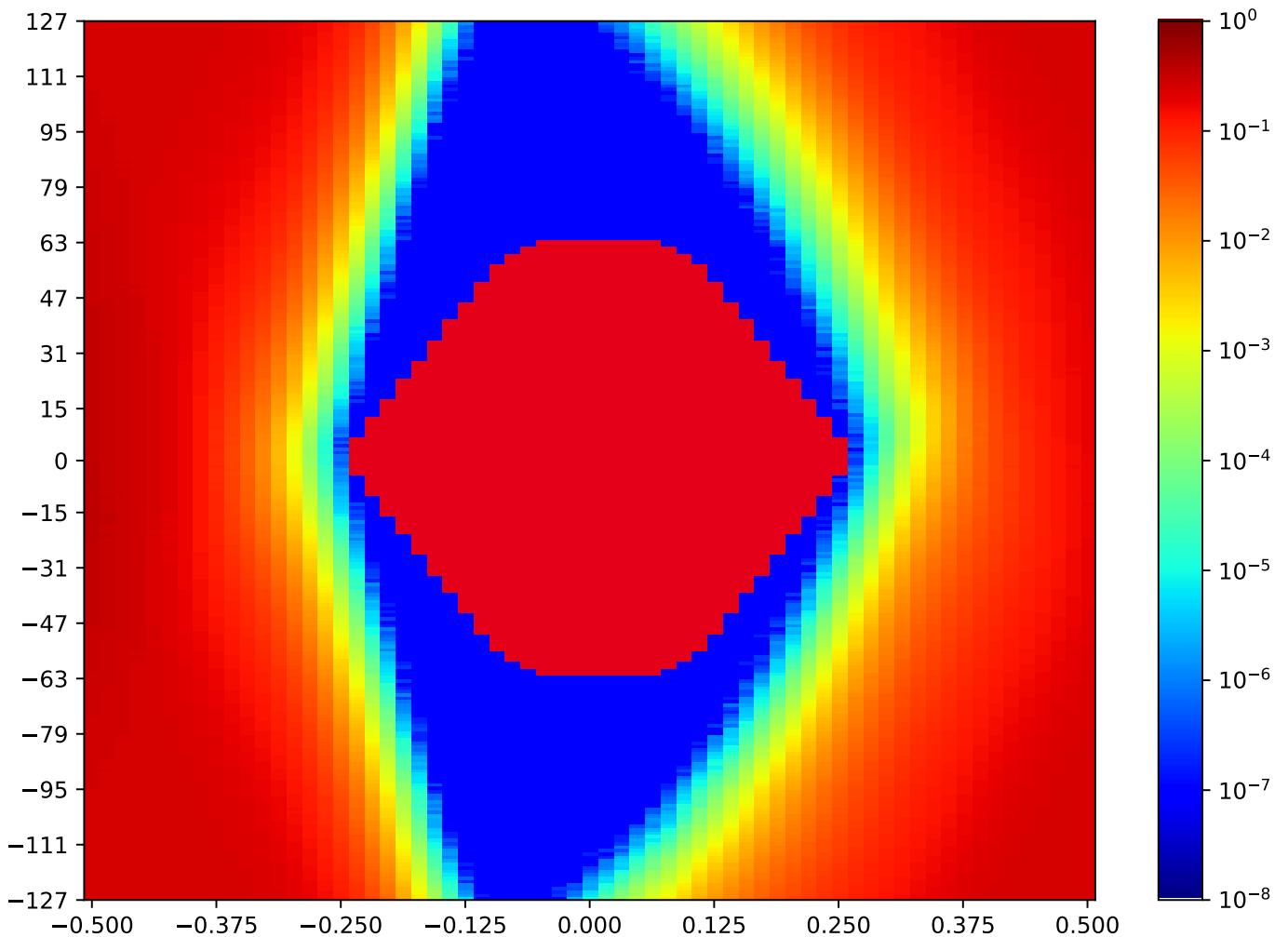


Figure 5.65: TRP_FPGA-J1-02–J1-02-TRP_FPGA

Call back to summary Figure 5.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.6.4 TRP_FPGA-J1-03–J1-03-TRP_FPGA

Table 5.60: TRP_FPGA-J1-03–J1-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:10:15		2018-Sep-27 17:10:35	
Reset RX	OA	HO		HO (%)	
true	7264	36		55.38%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

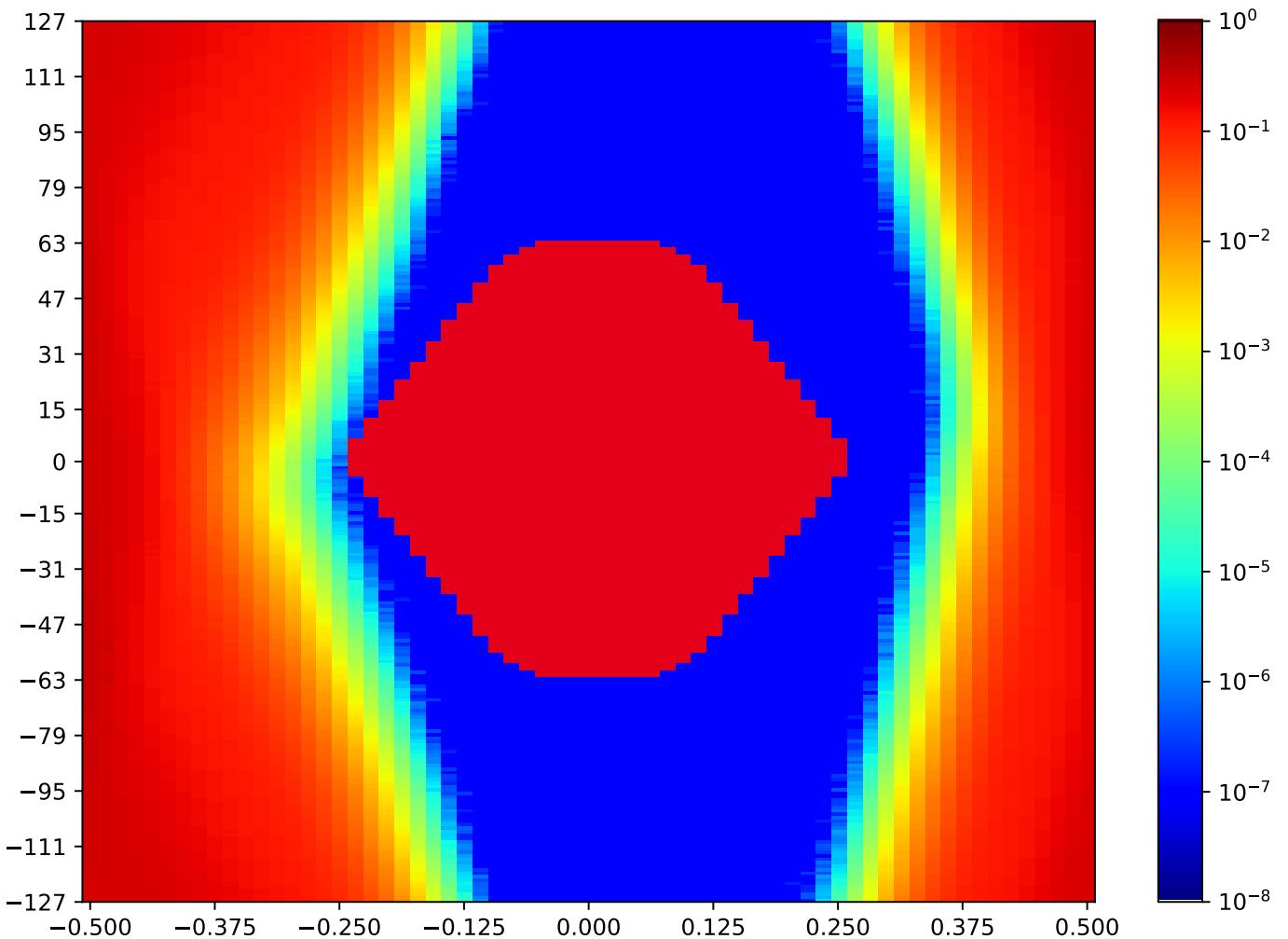


Figure 5.66: TRP_FPGA-J1-03–J1-03-TRP_FPGA

Call back to summary Figure 5.62. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.7 TRP J3 SFP Loopback

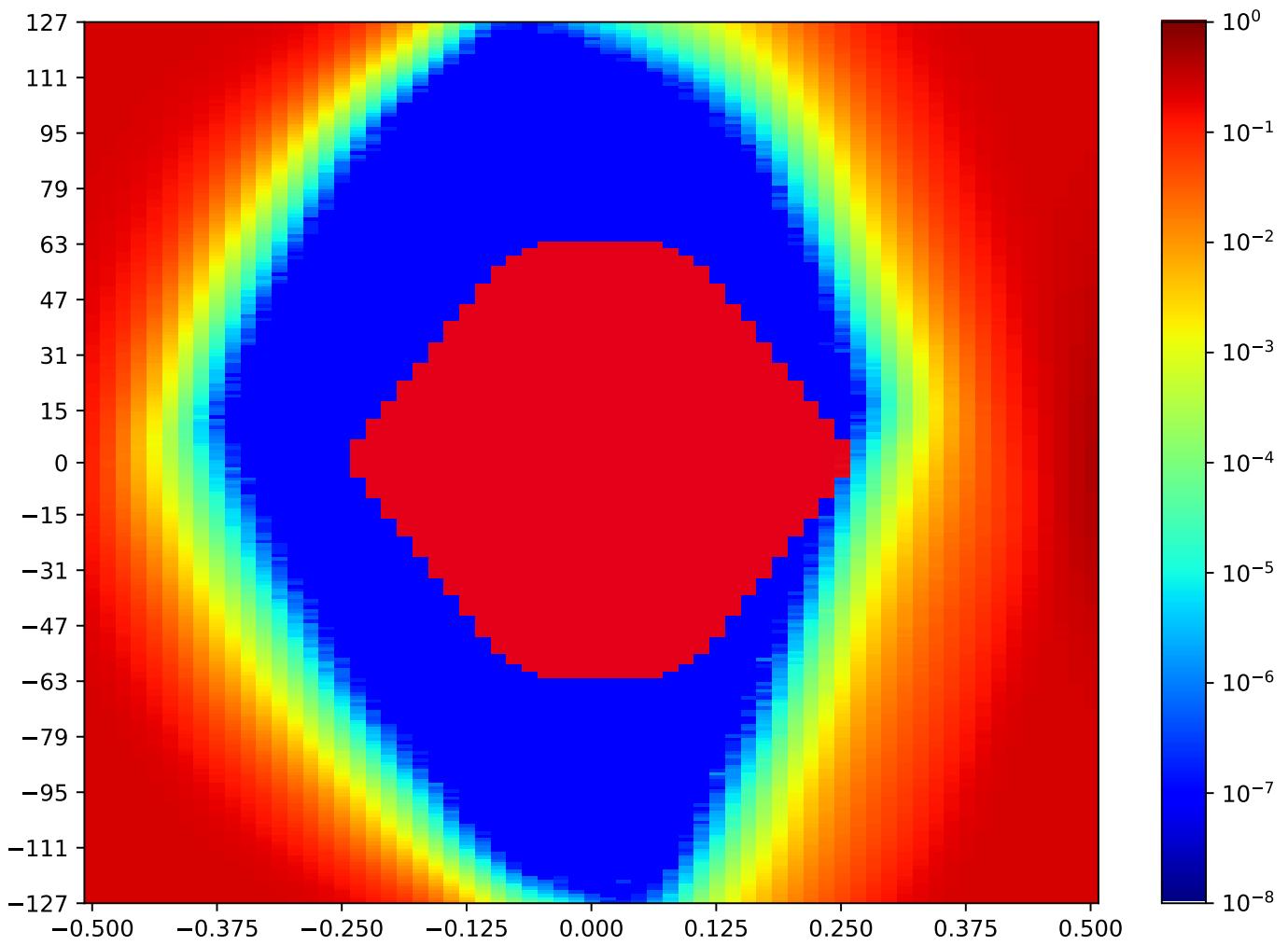


Figure 5.67: TRP J3 SFP Loopback

A cross-reference to Figure 5.67. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.
Next summary Figure 5.69.

5.7.1 TRP_FPGA-J3-00–J3-00-TRP_FPGA

Table 5.61: TRP_FPGA-J3-00–J3-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:10:36		2018-Sep-27 17:10:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	6571	36	55.38%	243	94.90%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

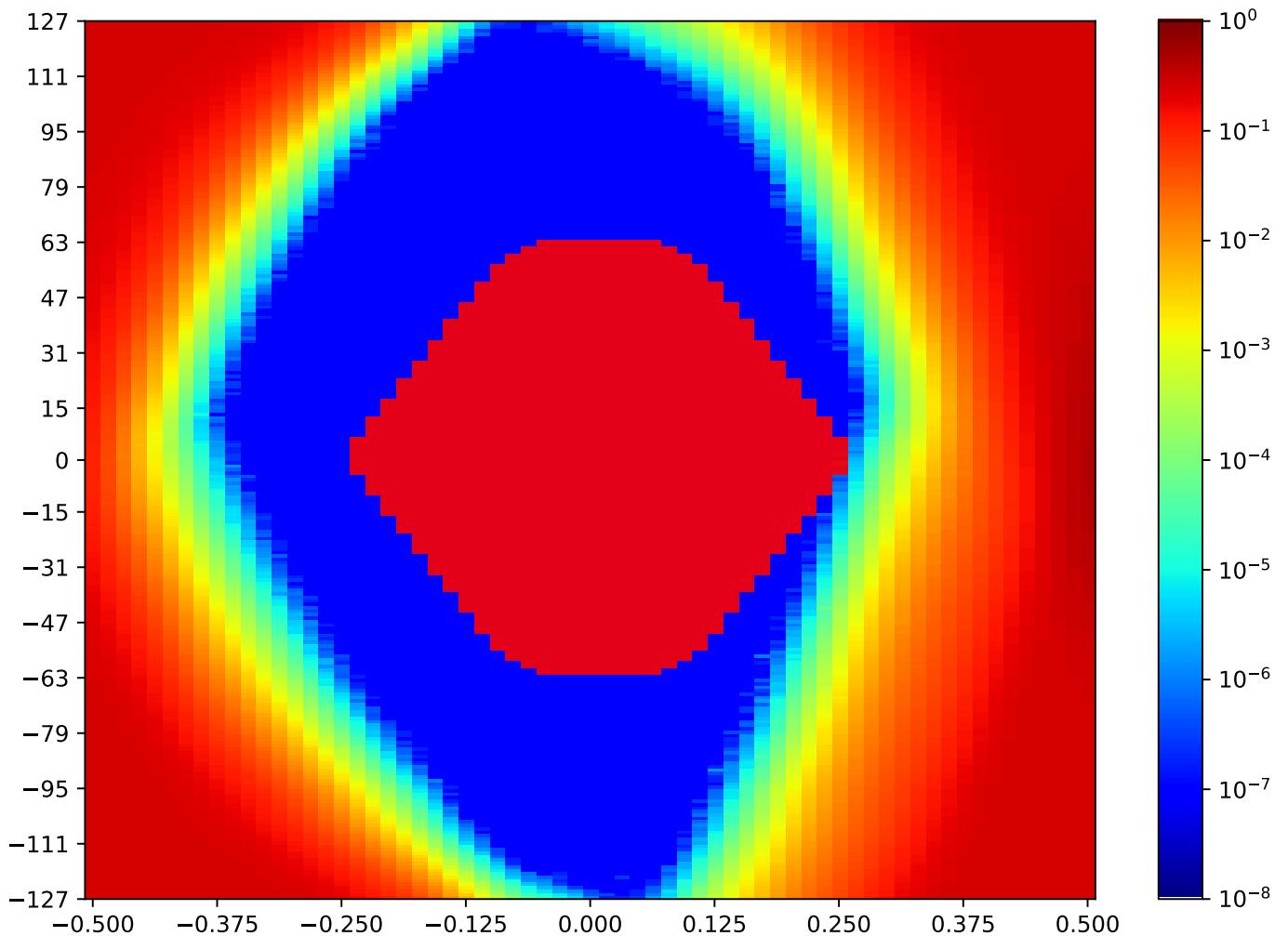


Figure 5.68: TRP_FPGA-J3-00–J3-00-TRP_FPGA

Call back to summary Figure 5.67. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8 MSP_A TRP On board links

A cross-reference to Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.
Next summary Figure 5.98.

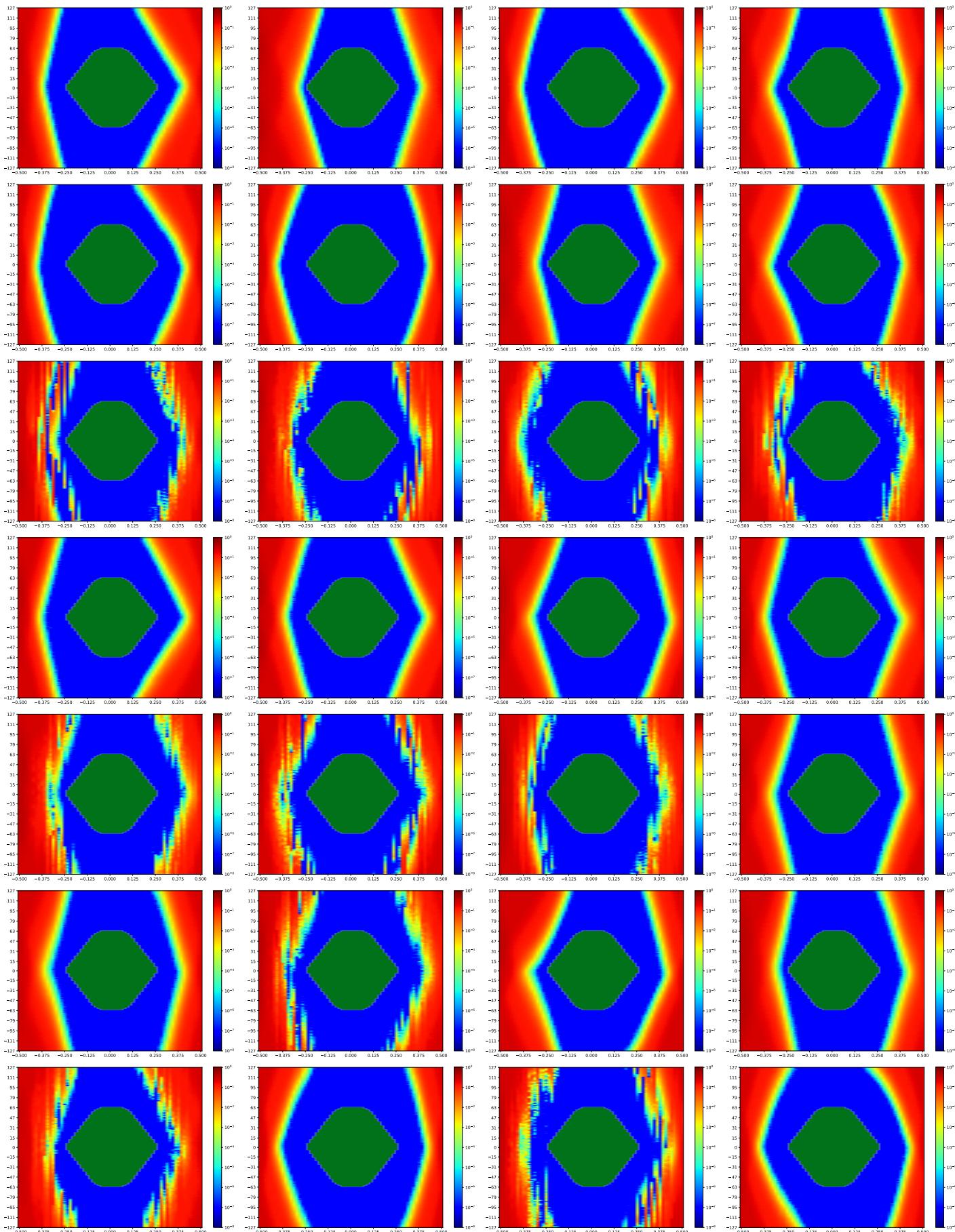


Figure 5.69: MSP_A TRP On board links

5.8.1 MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

Table 5.62: MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:10:56		2018-Sep-27 17:11:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8740	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

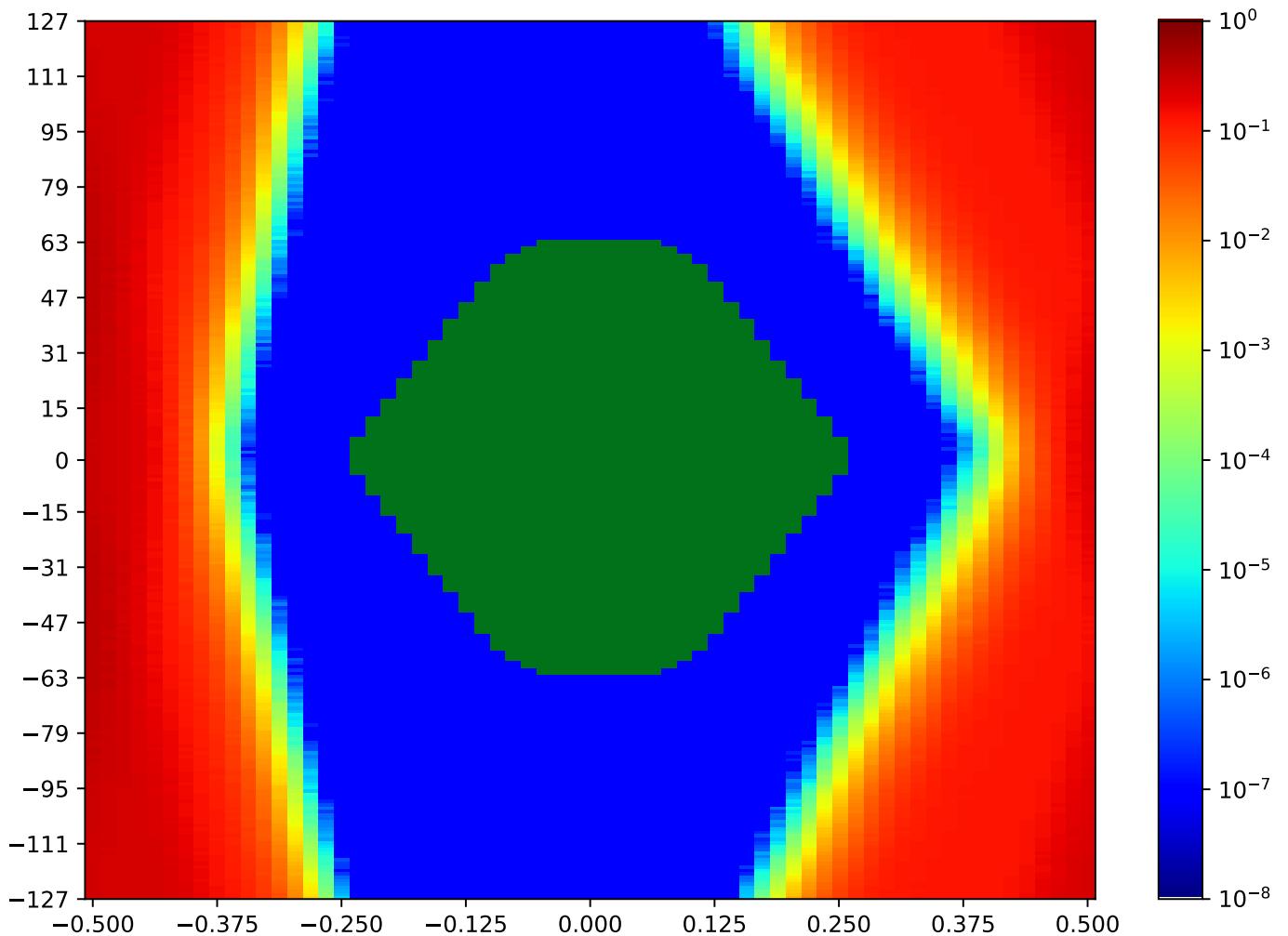


Figure 5.70: MSP_A_FPGA-IC39-00-IC4-00-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.2 MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

Table 5.63: MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:11:16		2018-Sep-27 17:11:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7753	38	58.46%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

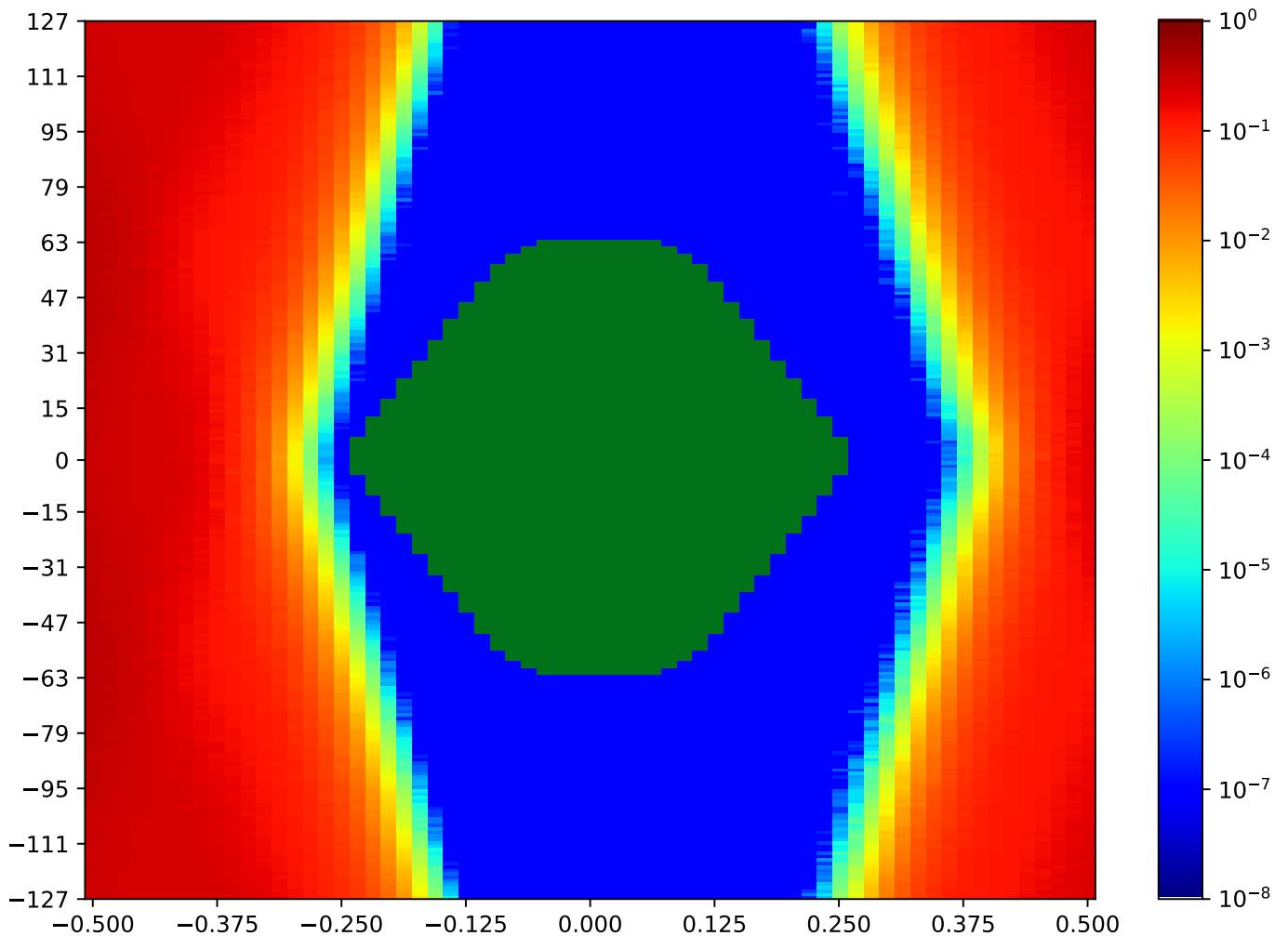


Figure 5.71: MSP_A_FPGA-IC39-01-IC4-01-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.3 MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

Table 5.64: MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:11:37		2018-Sep-27 17:11:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9522	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

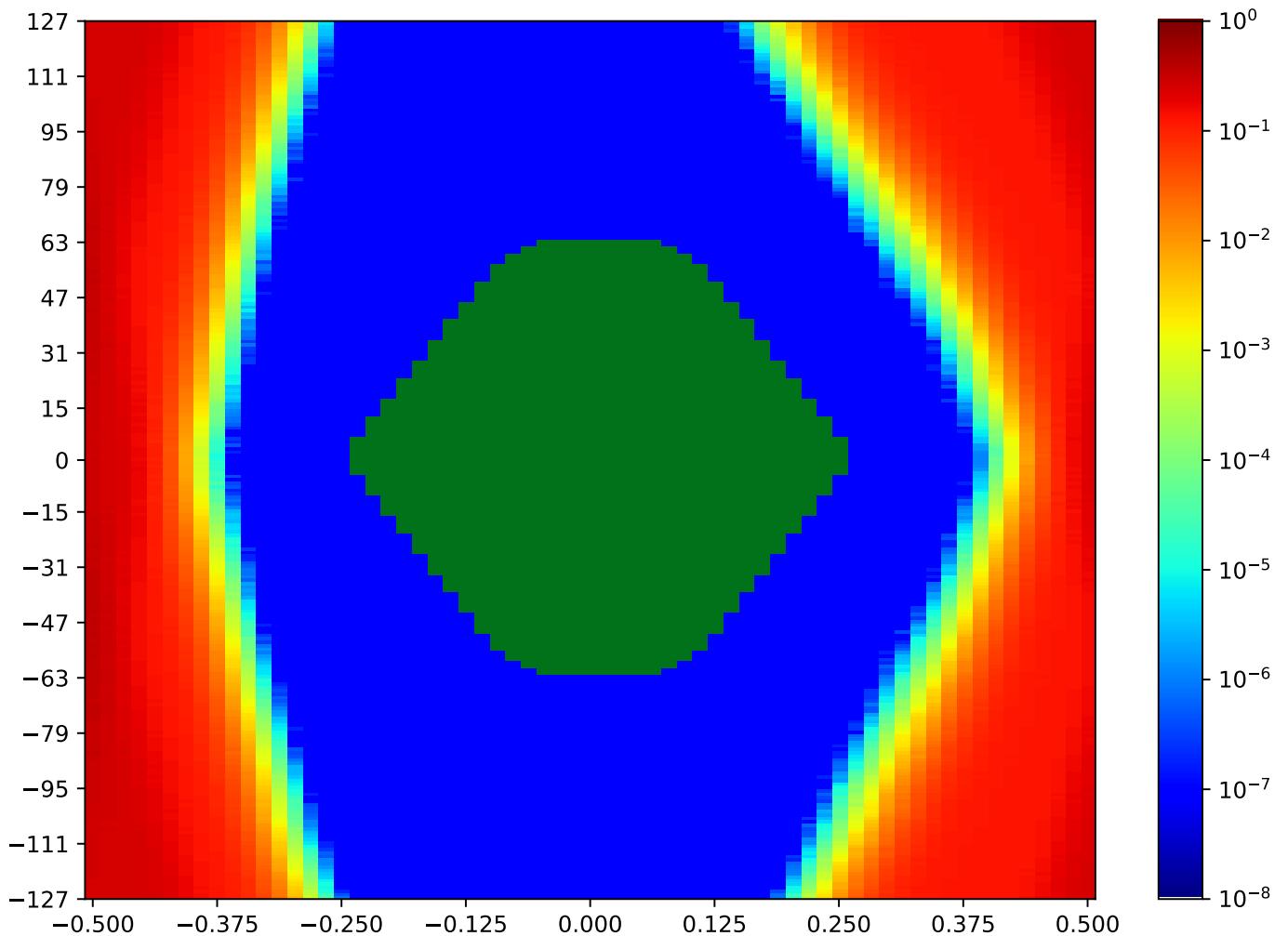


Figure 5.72: MSP_A_FPGA-IC39-02-IC4-02-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.4 MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

Table 5.65: MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:11:57		2018-Sep-27 17:12:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8692	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

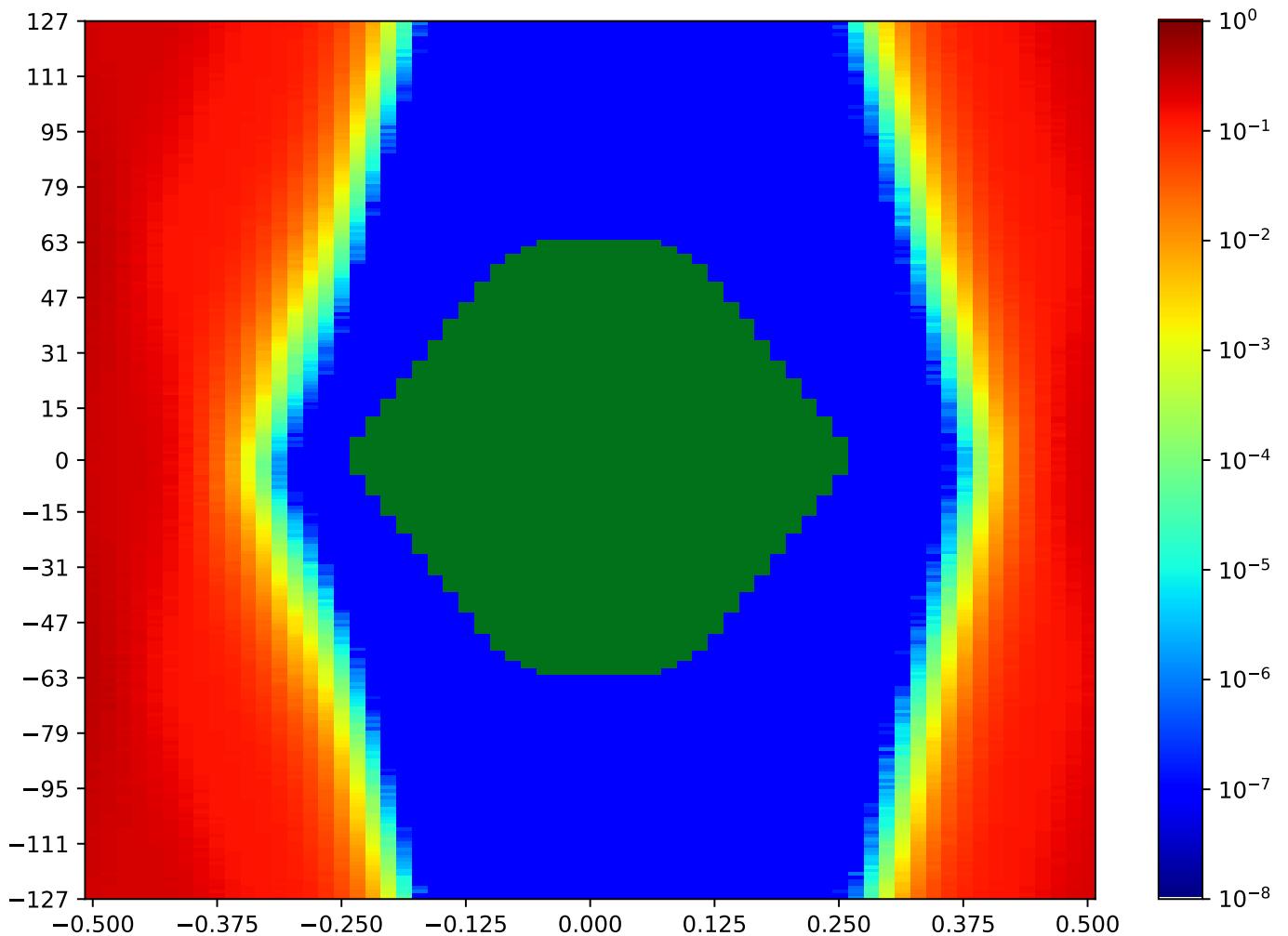


Figure 5.73: MSP_A_FPGA-IC39-03-IC4-03-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.5 MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

Table 5.66: MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:12:18		2018-Sep-27 17:12:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9918	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

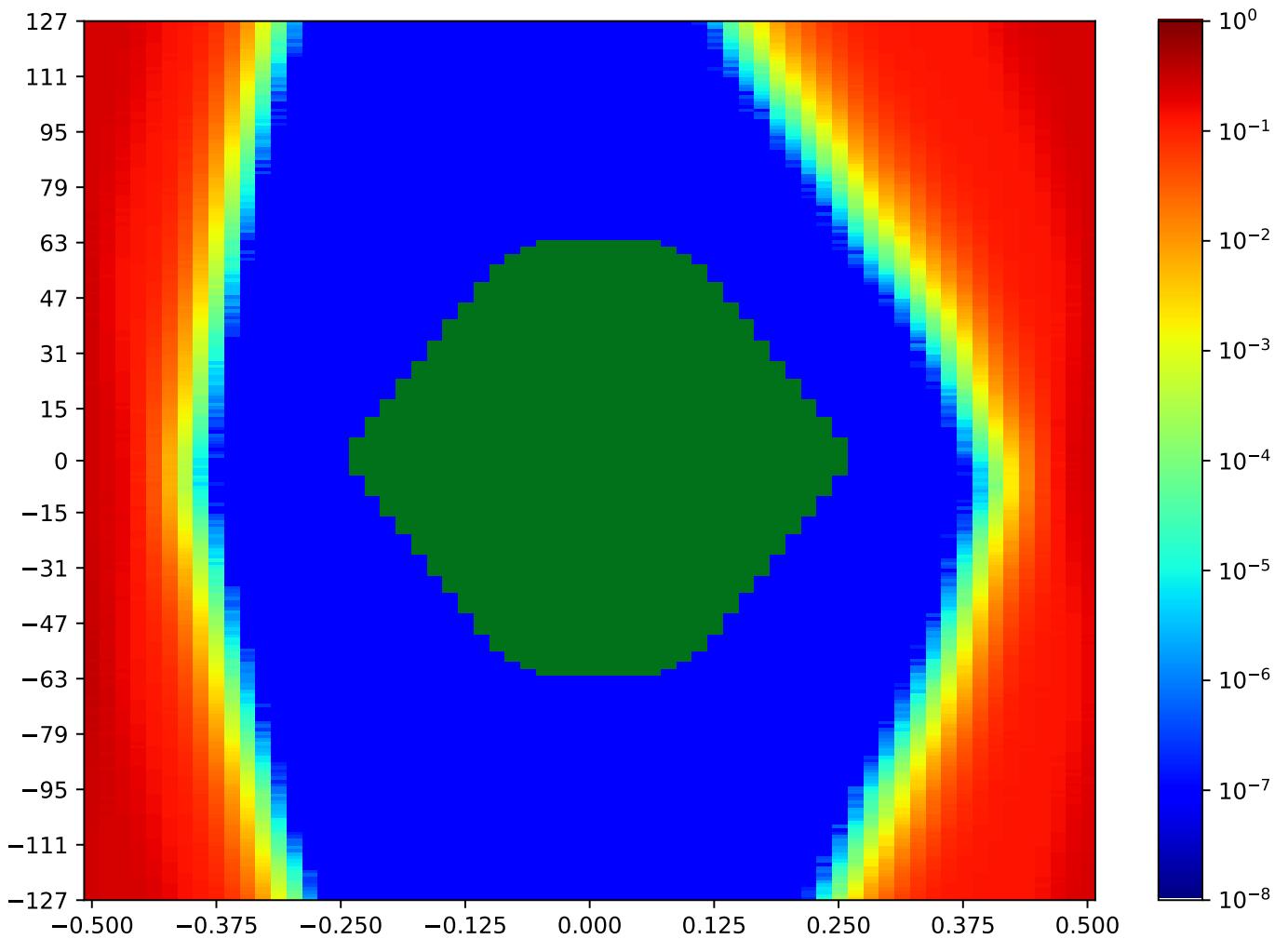


Figure 5.74: MSP_A_FPGA-IC39-04-IC4-04-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.6 MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

Table 5.67: MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:12:38		2018-Sep-27 17:12:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10795	50	76.92%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

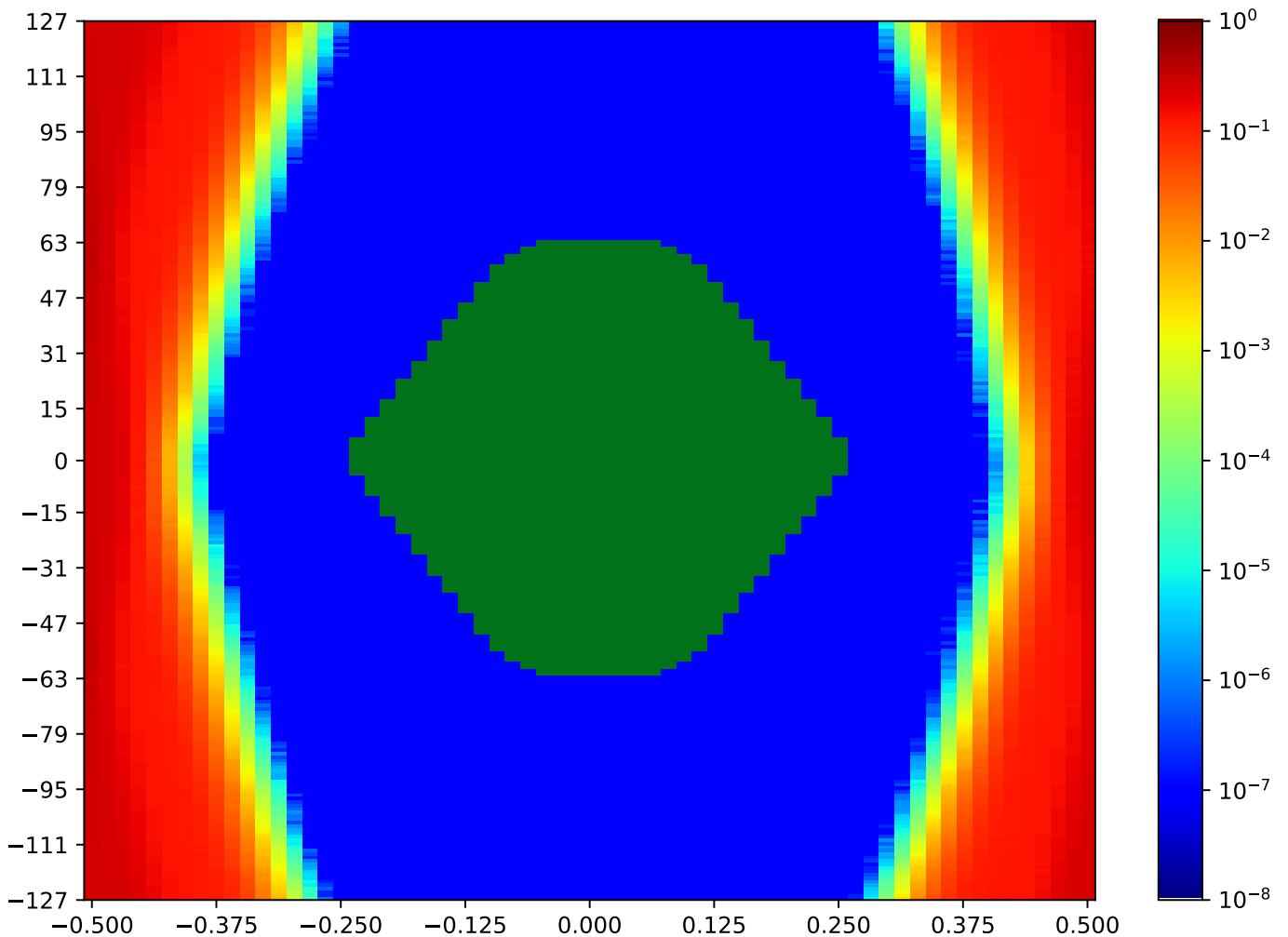


Figure 5.75: MSP_A_FPGA-IC39-05-IC4-05-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.7 MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

Table 5.68: MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:12:58		2018-Sep-27 17:13:18	
Reset RX	OA	HO		VO	VO (%)
true	7801	39		60.00%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

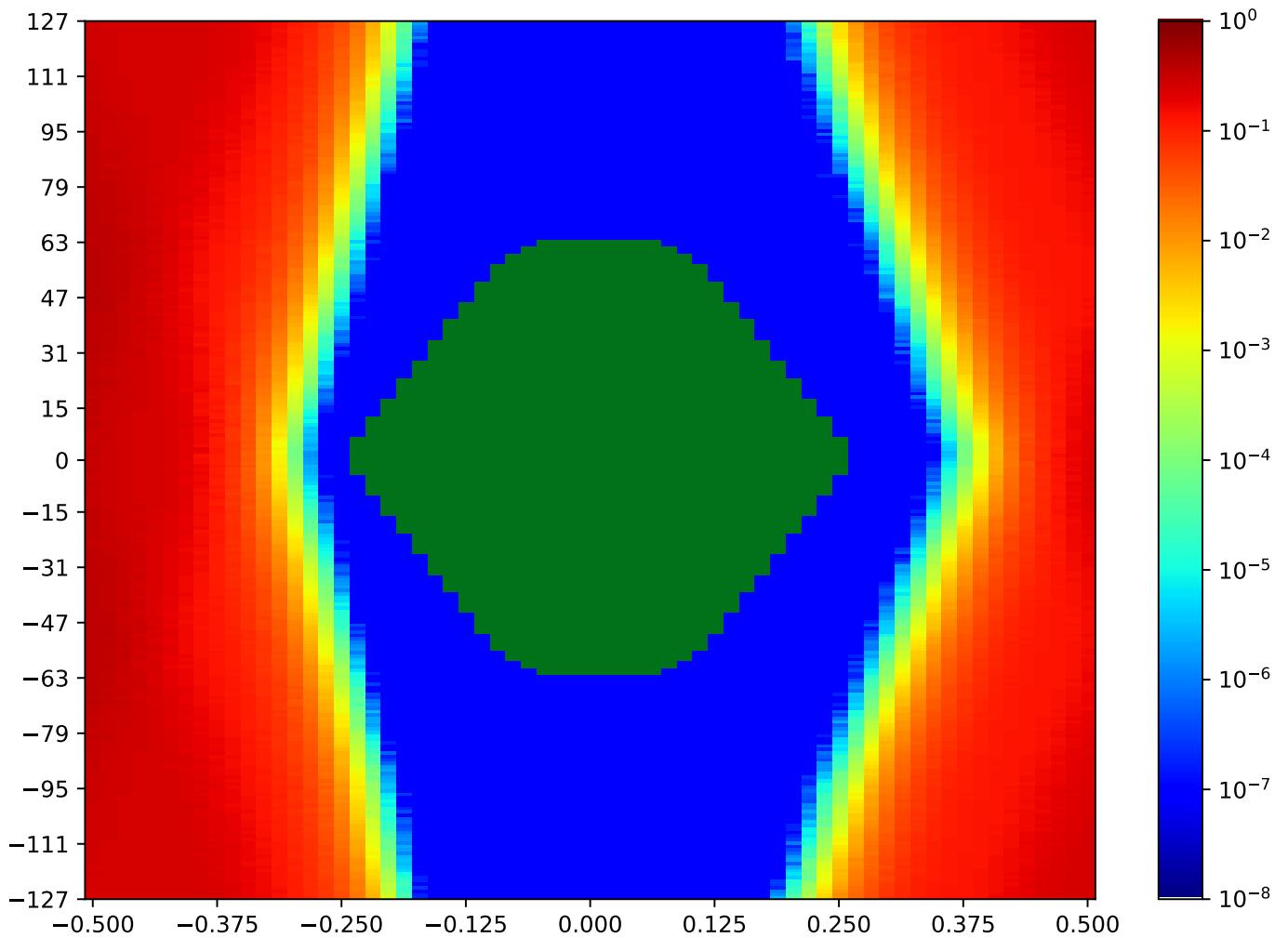


Figure 5.76: MSP_A_FPGA-IC39-06-IC4-06-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.8 MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

Table 5.69: MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:13:19		2018-Sep-27 17:13:39	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8450	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

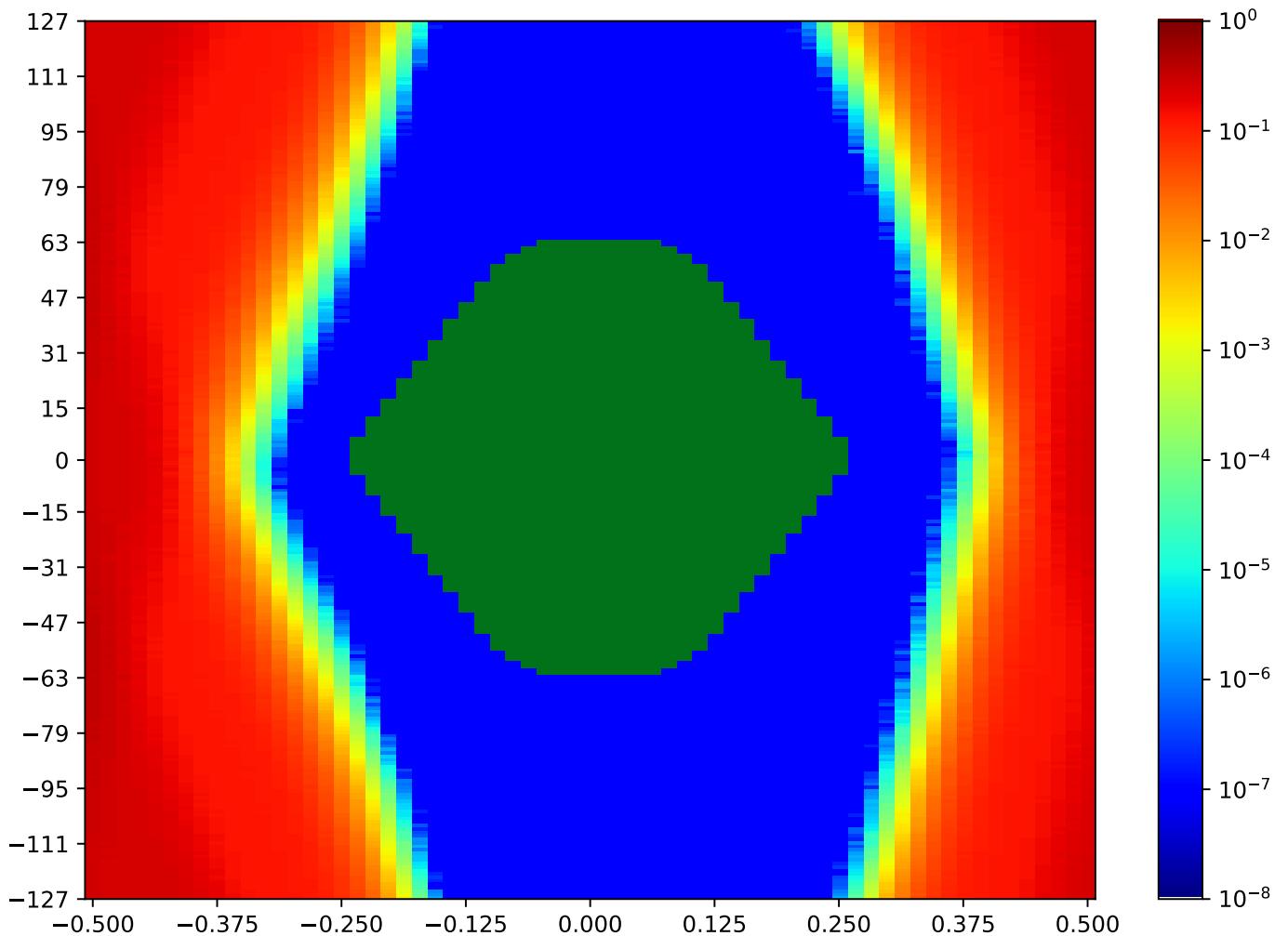


Figure 5.77: MSP_A_FPGA-IC39-07-IC4-07-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.9 MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

Table 5.70: MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:13:39		2018-Sep-27 17:13:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8995	46	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

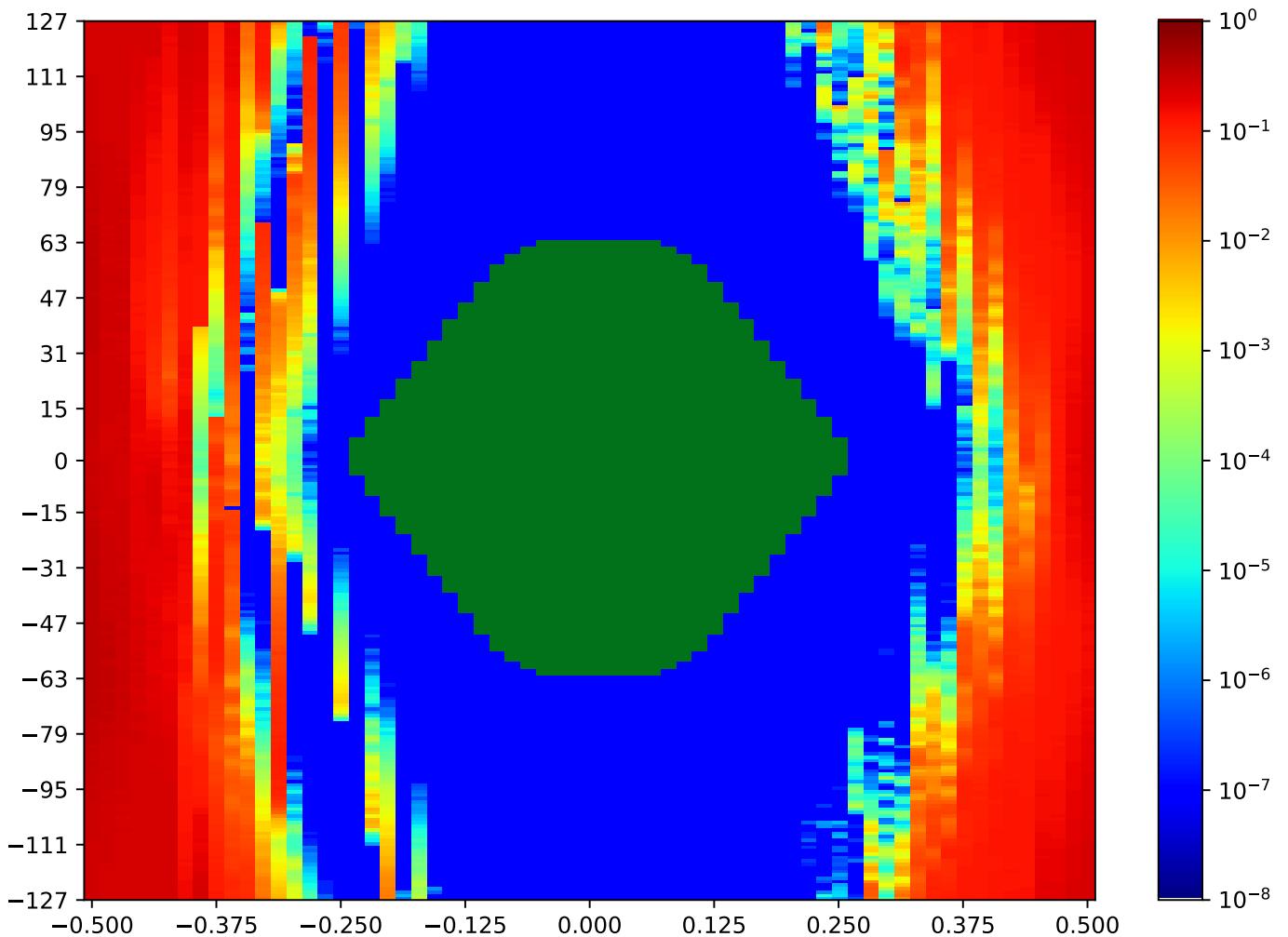


Figure 5.78: MSP_A_FPGA-IC39-08-IC4-08-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.10 MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

Table 5.71: MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:13:59		2018-Sep-27 17:14:20	
Reset RX	OA	HO		HO (%)	
true	8705	45		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

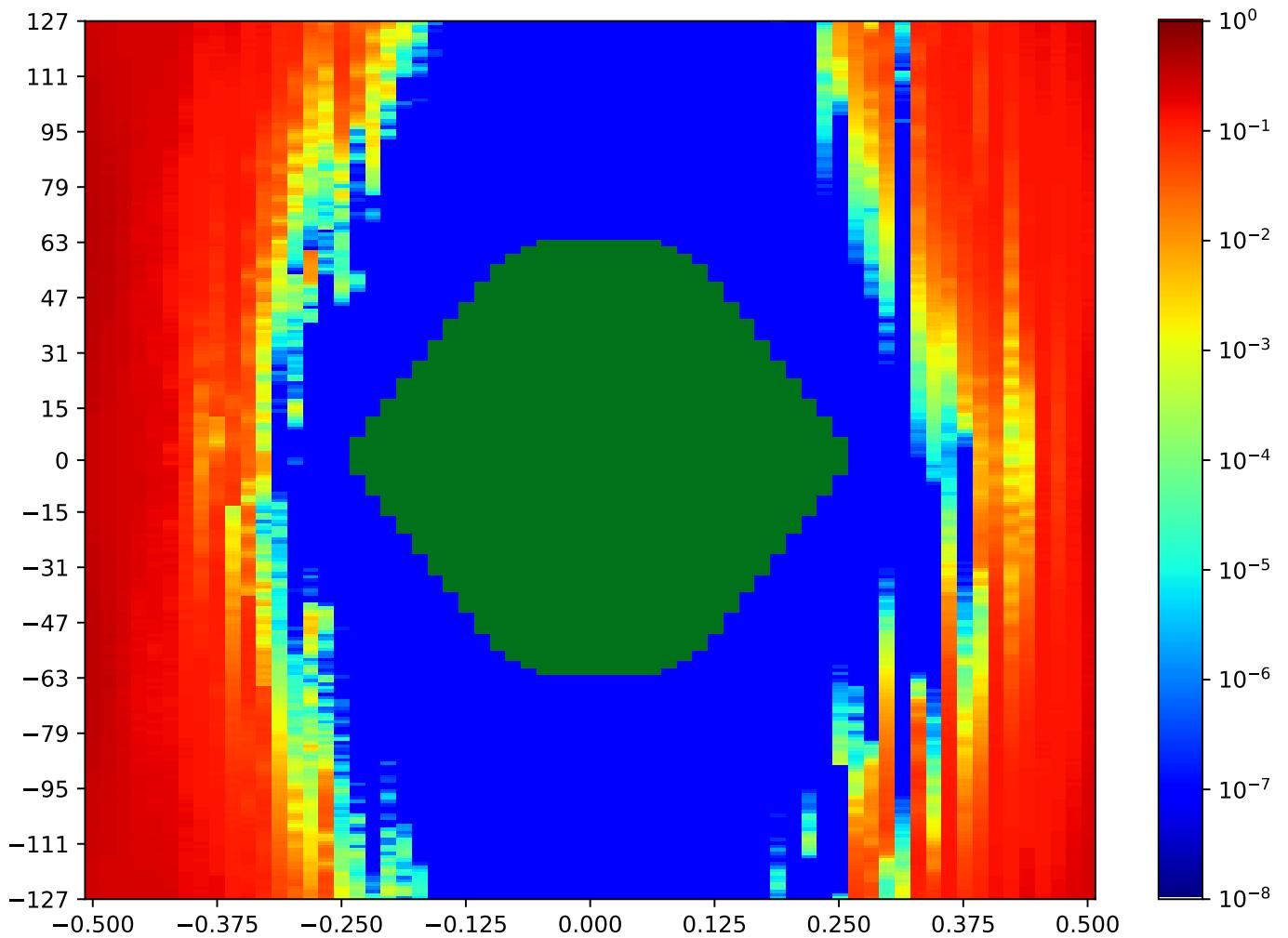


Figure 5.79: MSP_A_FPGA-IC39-09-IC4-09-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.11 MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

Table 5.72: MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:14:20		2018-Sep-27 17:14:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9208	46	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

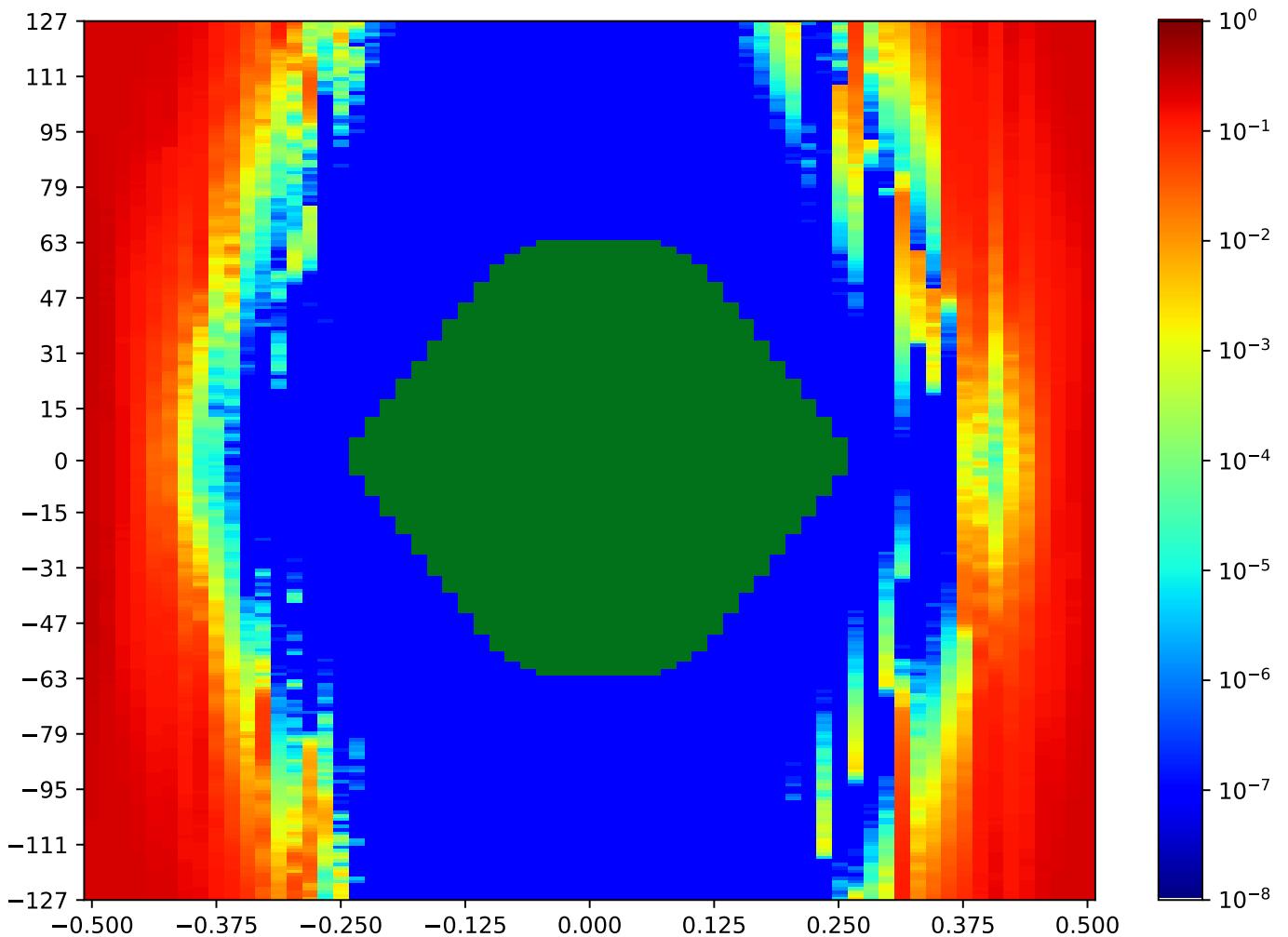


Figure 5.80: MSP_A_FPGA-IC39-10-IC4-10-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.12 MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

Table 5.73: MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:14:40		2018-Sep-27 17:15:00	
Reset RX	OA	HO		HO (%)	
true	8410	40		61.54%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

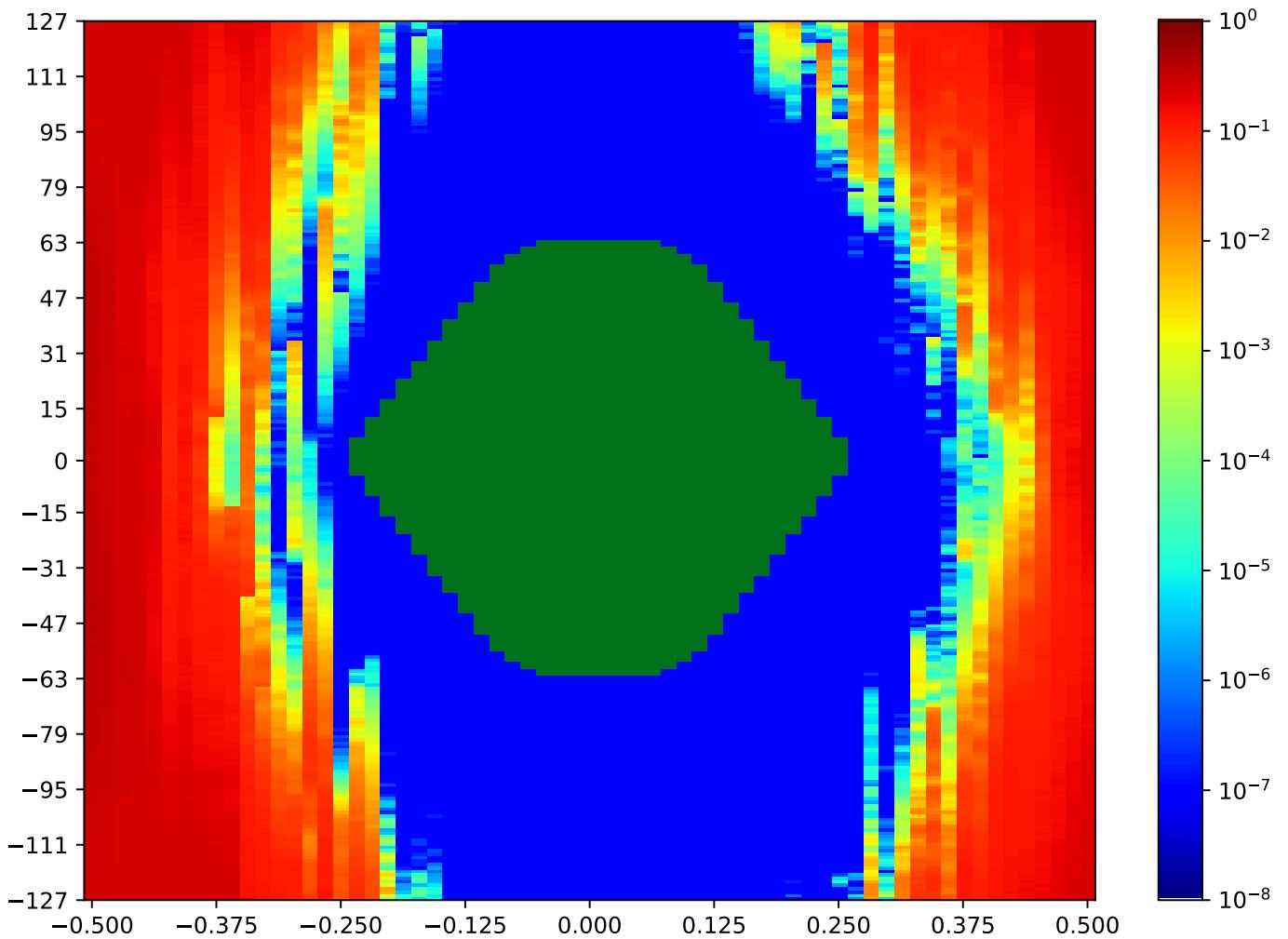


Figure 5.81: MSP_A_FPGA-IC39-11-IC4-11-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.13 MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

Table 5.74: MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:15:01		2018-Sep-27 17:15:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9039	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

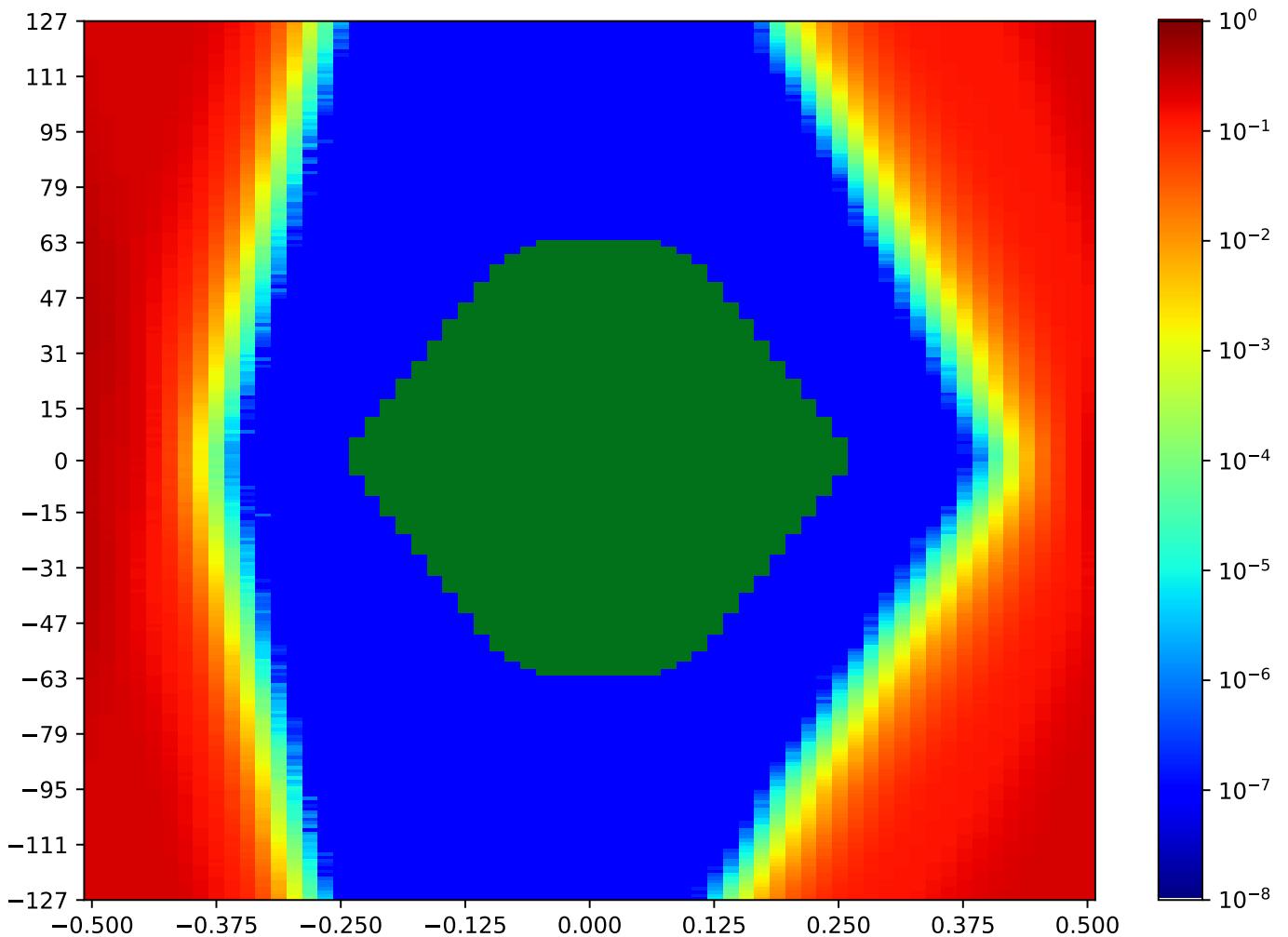


Figure 5.82: MSP_A_FPGA-IC39-12-IC4-12-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.14 MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

Table 5.75: MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:15:22		2018-Sep-27 17:15:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8903	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

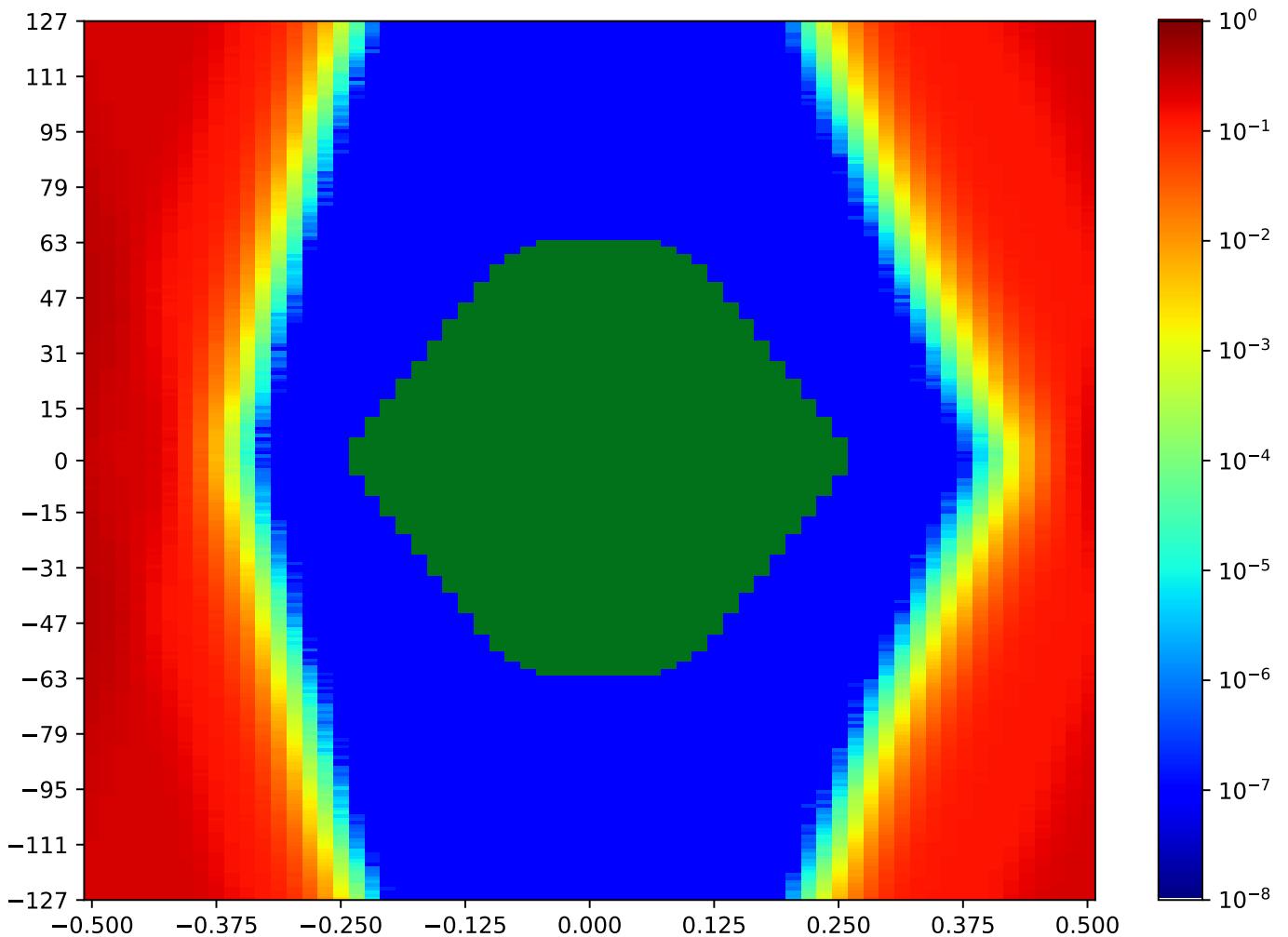


Figure 5.83: MSP_A_FPGA-IC39-13-IC4-13-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.15 MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

Table 5.76: MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:15:42		2018-Sep-27 17:16:02	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9036	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

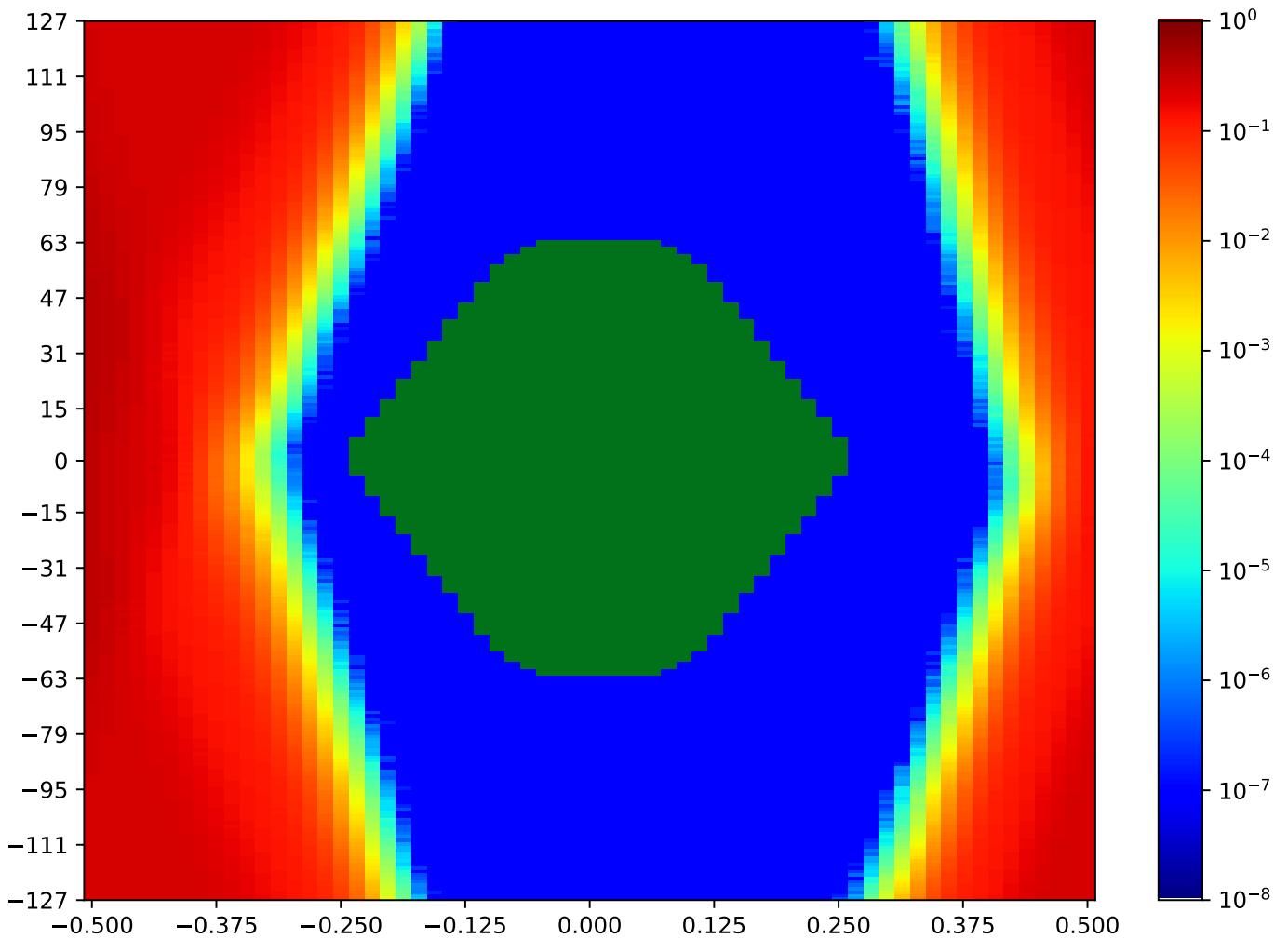


Figure 5.84: MSP_A_FPGA-IC39-14-IC4-14-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.16 MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

Table 5.77: MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:16:02		2018-Sep-27 17:16:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8508	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

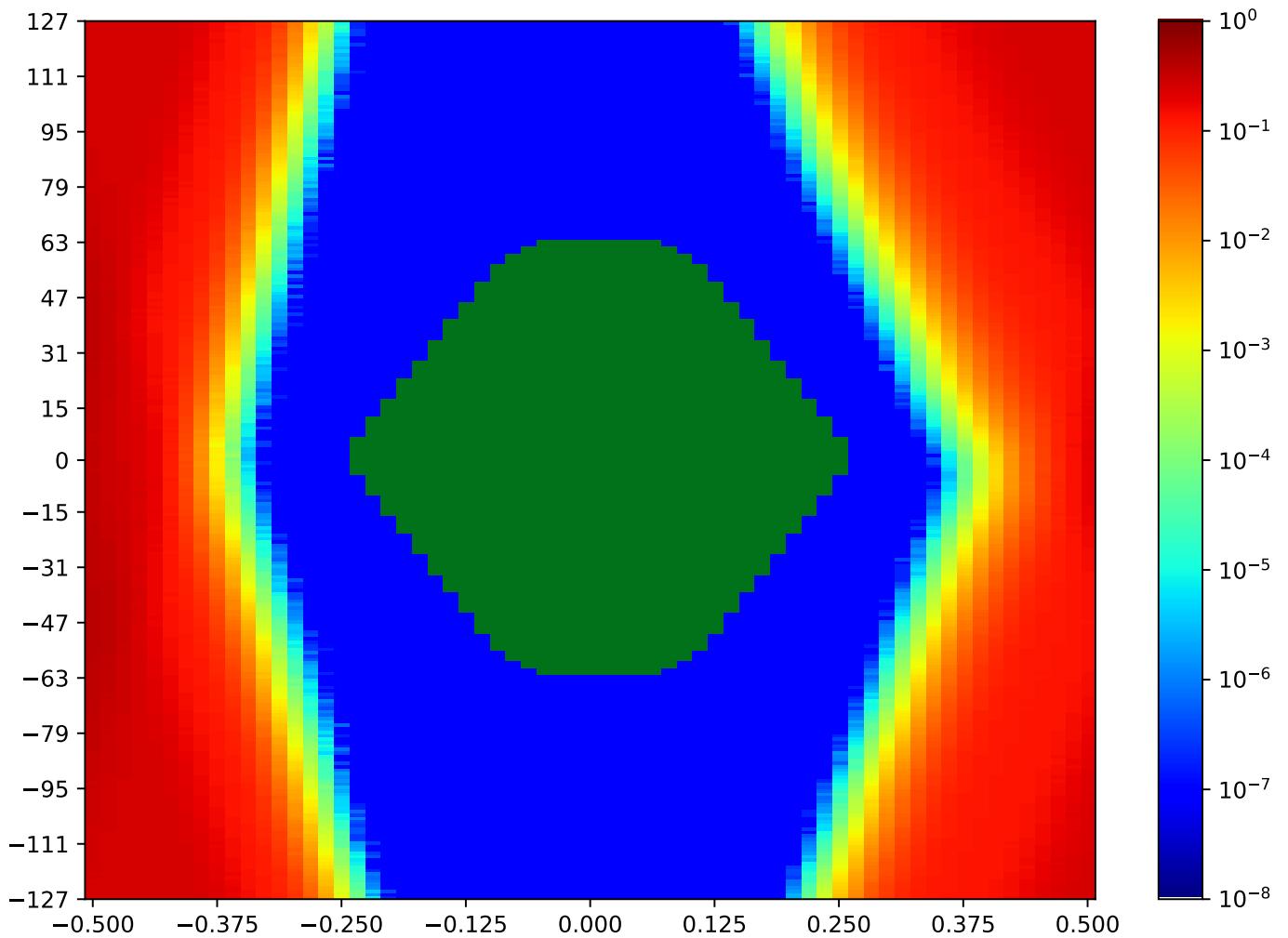


Figure 5.85: MSP_A_FPGA-IC39-15-IC4-15-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.17 MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

Table 5.78: MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:16:23		2018-Sep-27 17:16:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8676	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

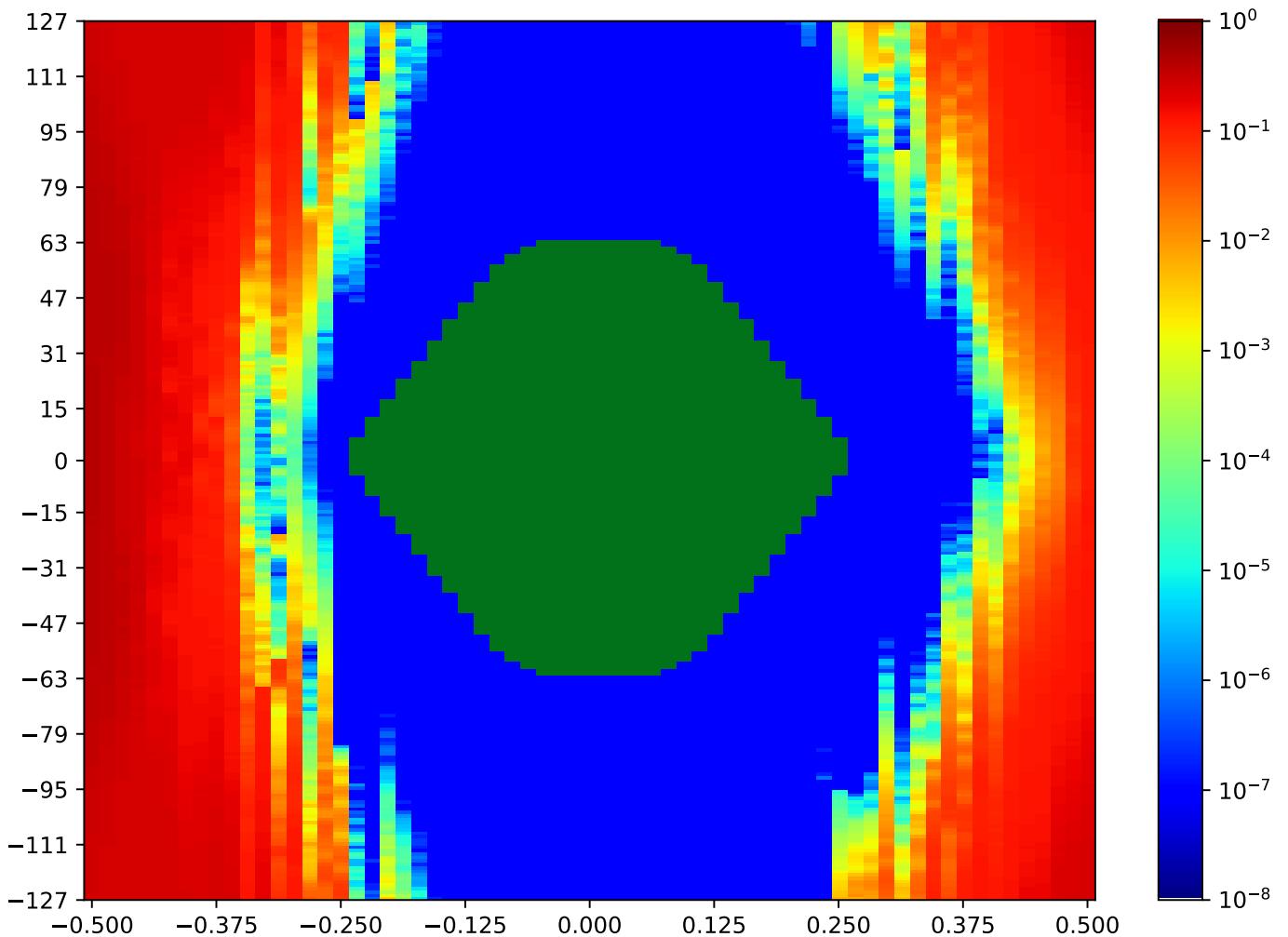


Figure 5.86: MSP_A_FPGA-IC39-16-IC4-16-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.18 MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

Table 5.79: MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:16:43		2018-Sep-27 17:17:03	
Reset RX	OA	HO		HO (%)	
true	9027	49		72.31%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

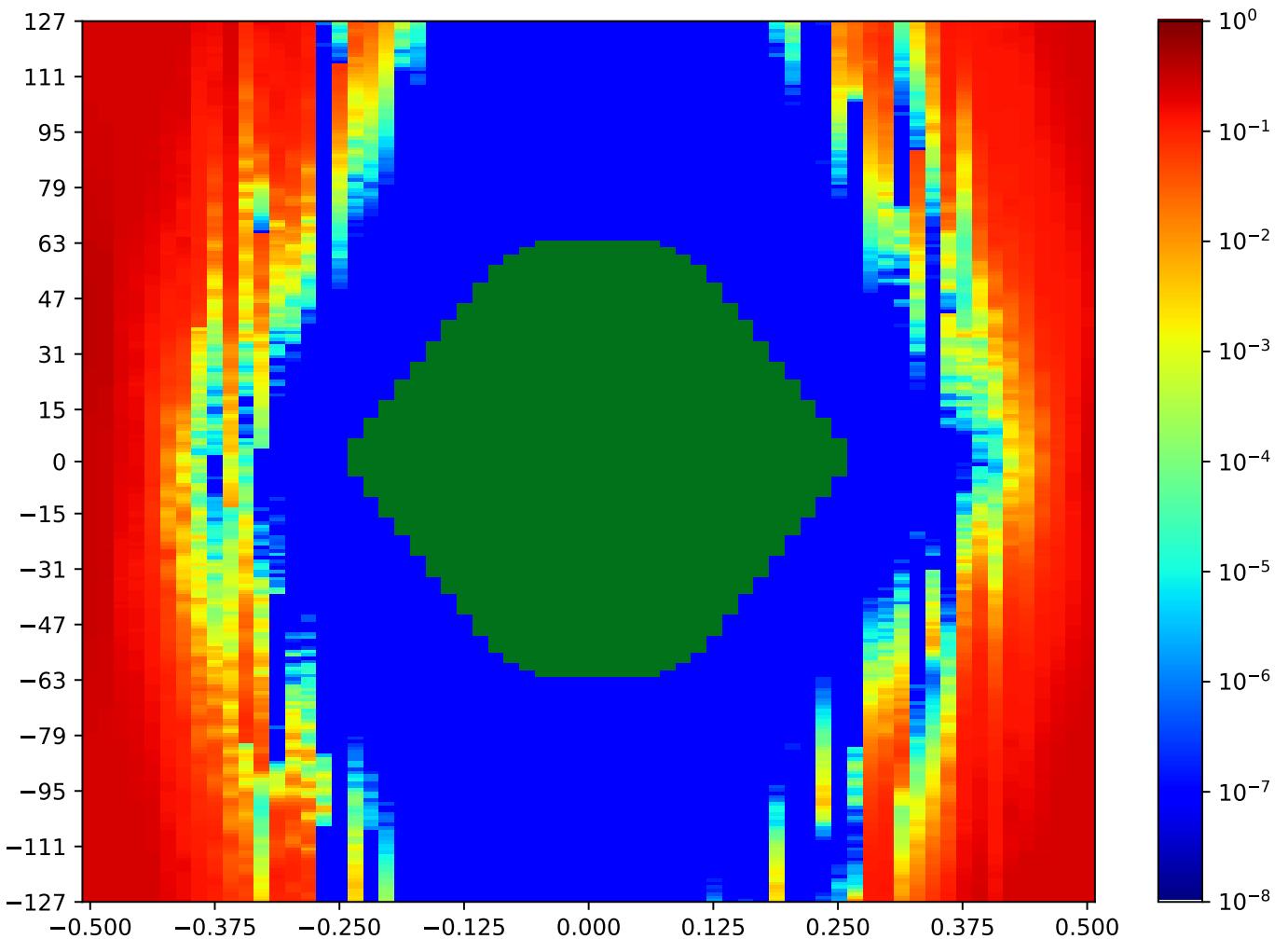


Figure 5.87: MSP_A_FPGA-IC39-17-IC4-17-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.19 MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

Table 5.80: MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:17:03		2018-Sep-27 17:17:24	
Reset RX	OA	HO		HO (%)	
true	8980	44		67.69%	
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

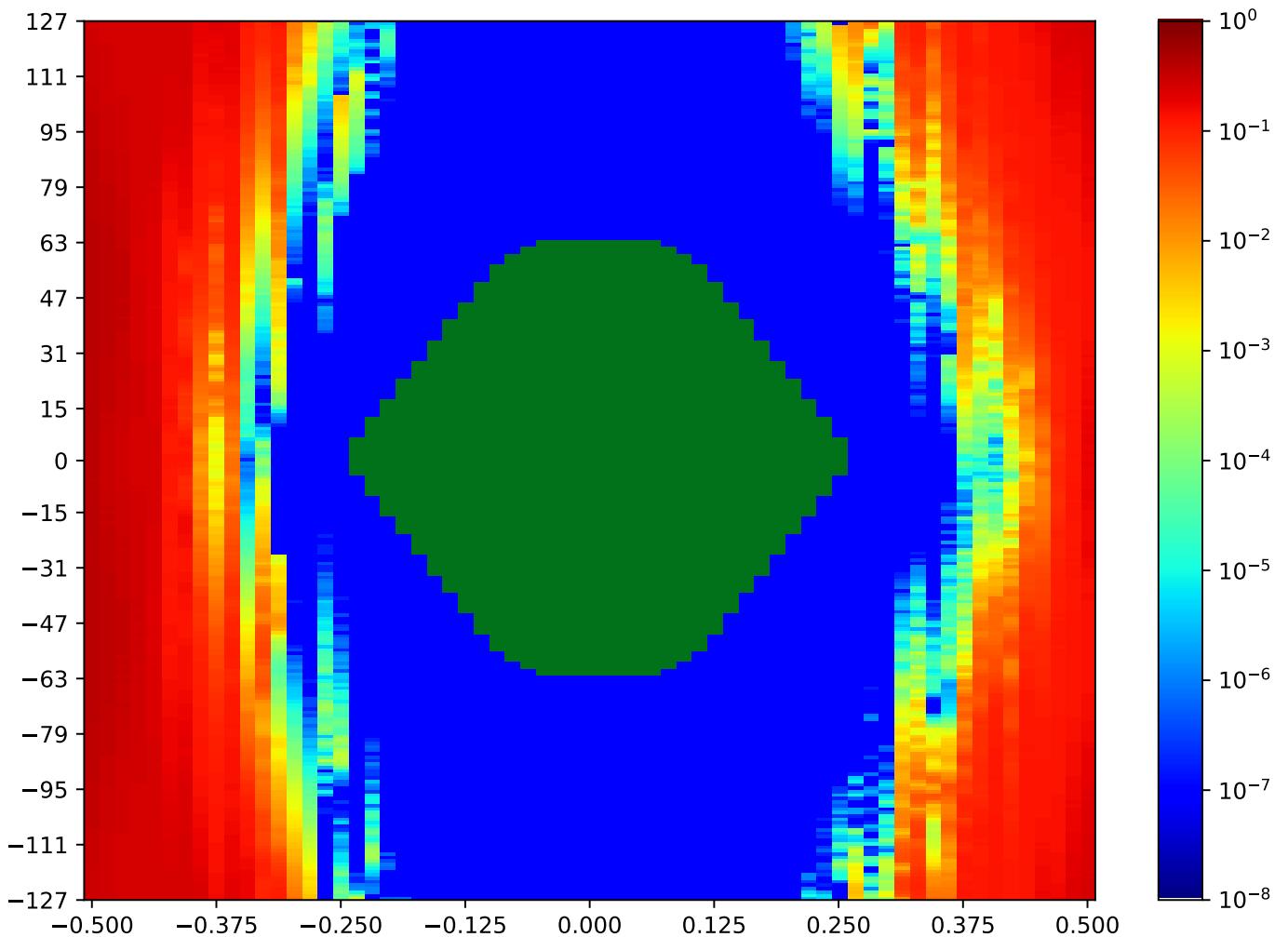


Figure 5.88: MSP_A_FPGA-IC39-18-IC4-18-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.20 MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

Table 5.81: MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:17:24		2018-Sep-27 17:17:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8608	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

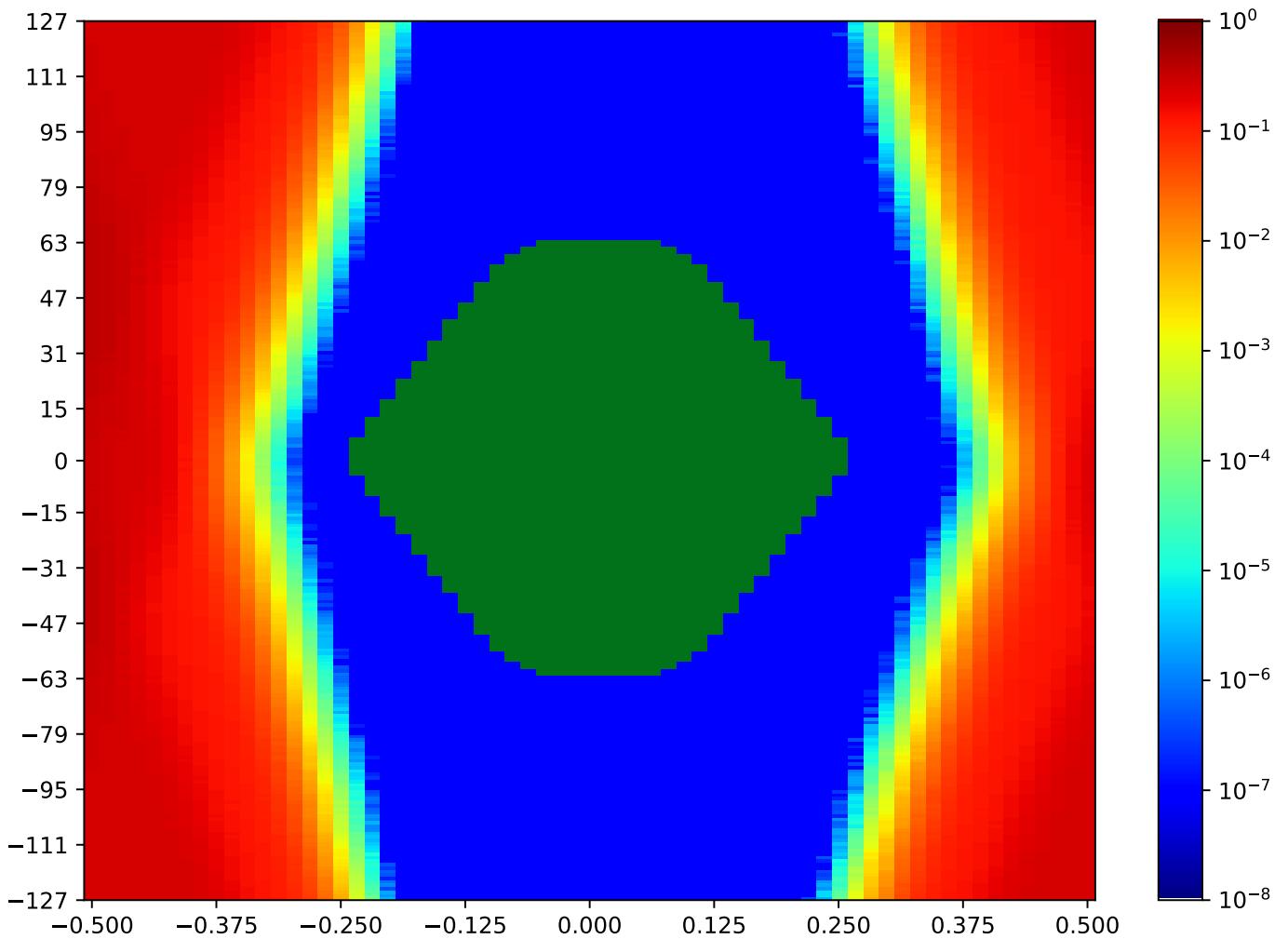


Figure 5.89: MSP_A_FPGA-IC39-19-IC4-19-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.21 MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

Table 5.82: MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:17:44		2018-Sep-27 17:18:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8900	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

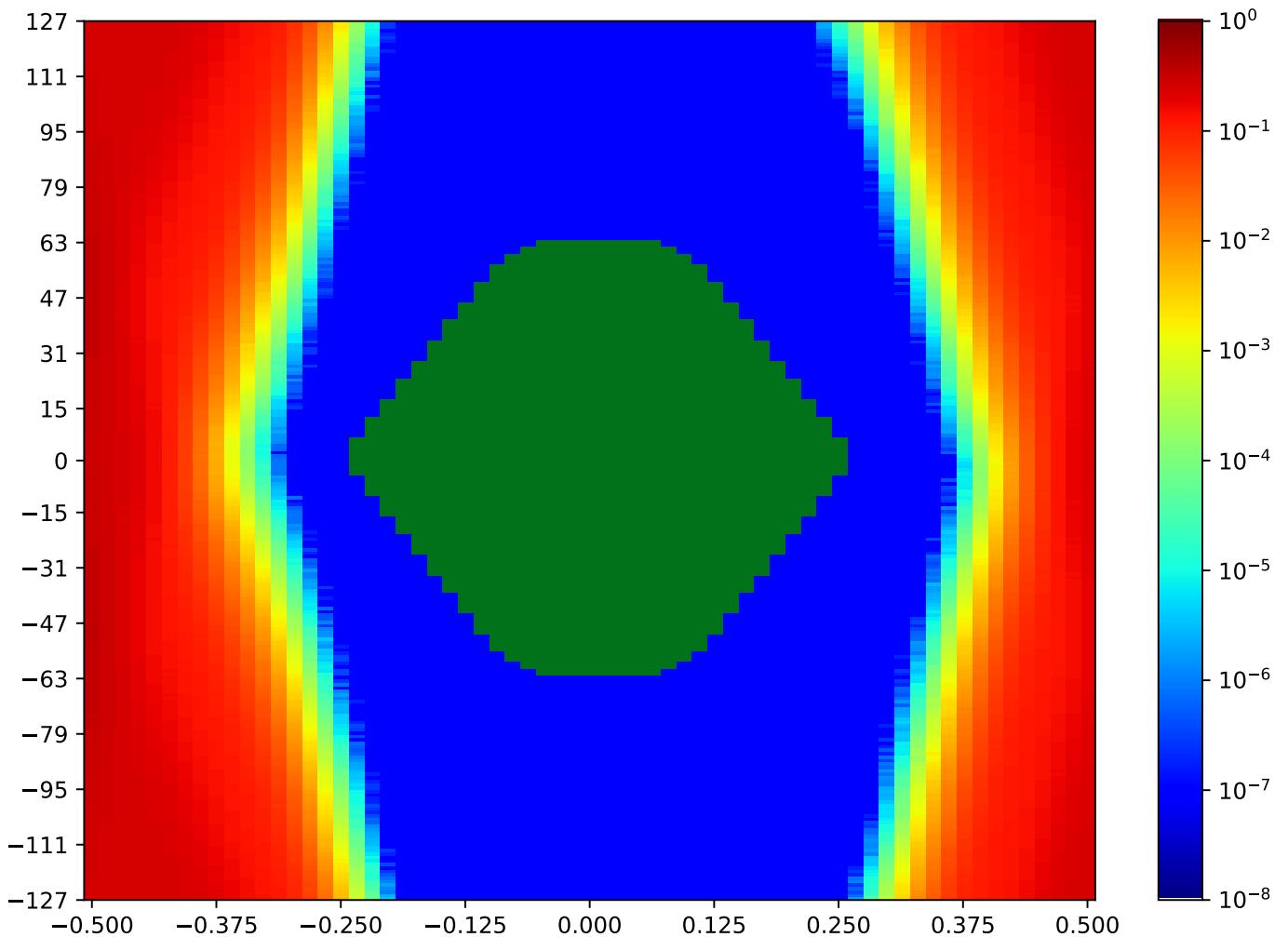


Figure 5.90: MSP_A_FPGA-IC39-20-IC4-20-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.22 MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

Table 5.83: MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:18:04		2018-Sep-27 17:18:25	
Reset RX	OA	HO		HO (%)	
true	8933	48		70.77%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

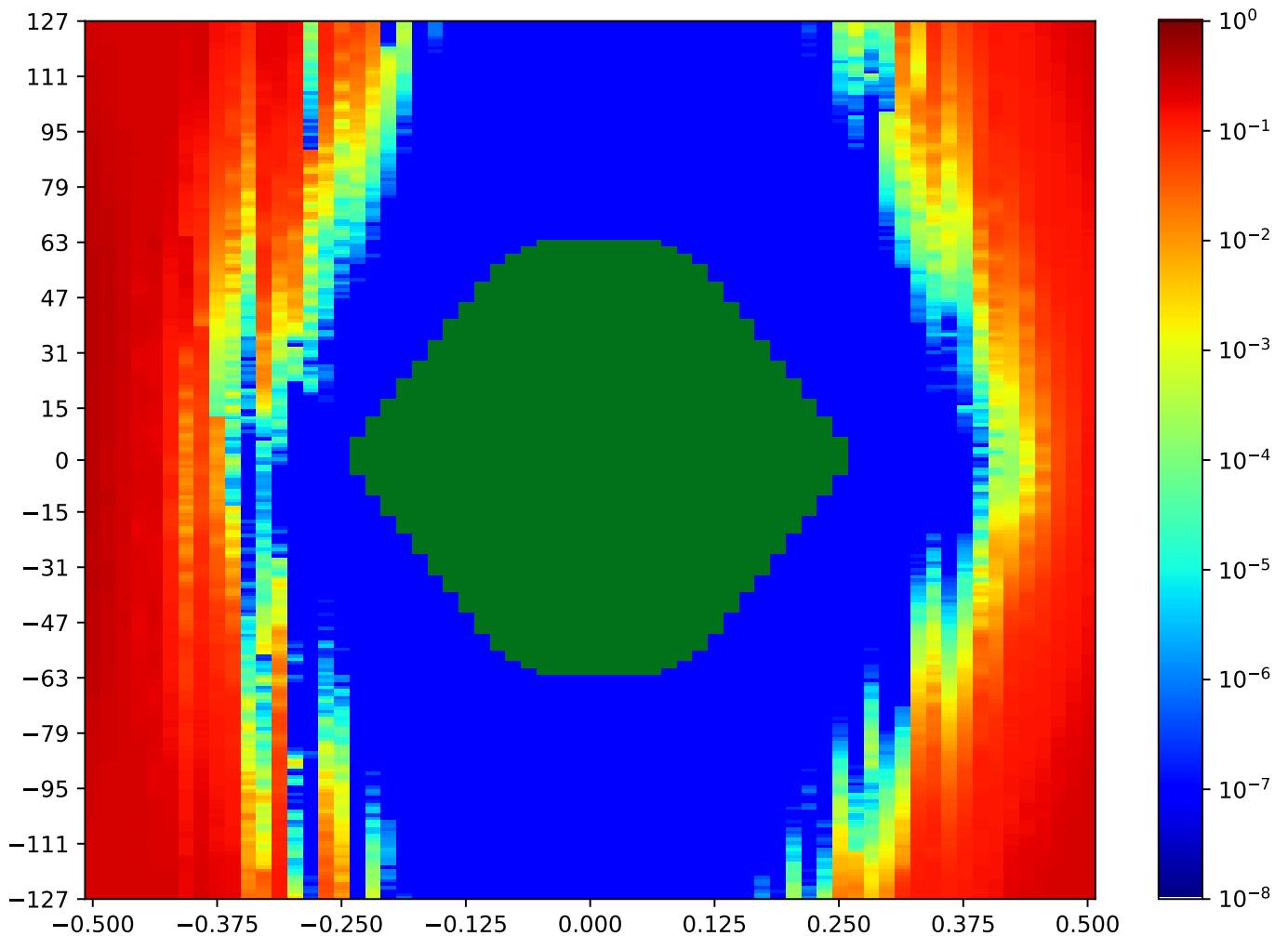


Figure 5.91: MSP_A_FPGA-IC39-21-IC4-21-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.23 MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

Table 5.84: MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:18:25		2018-Sep-27 17:18:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8248	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

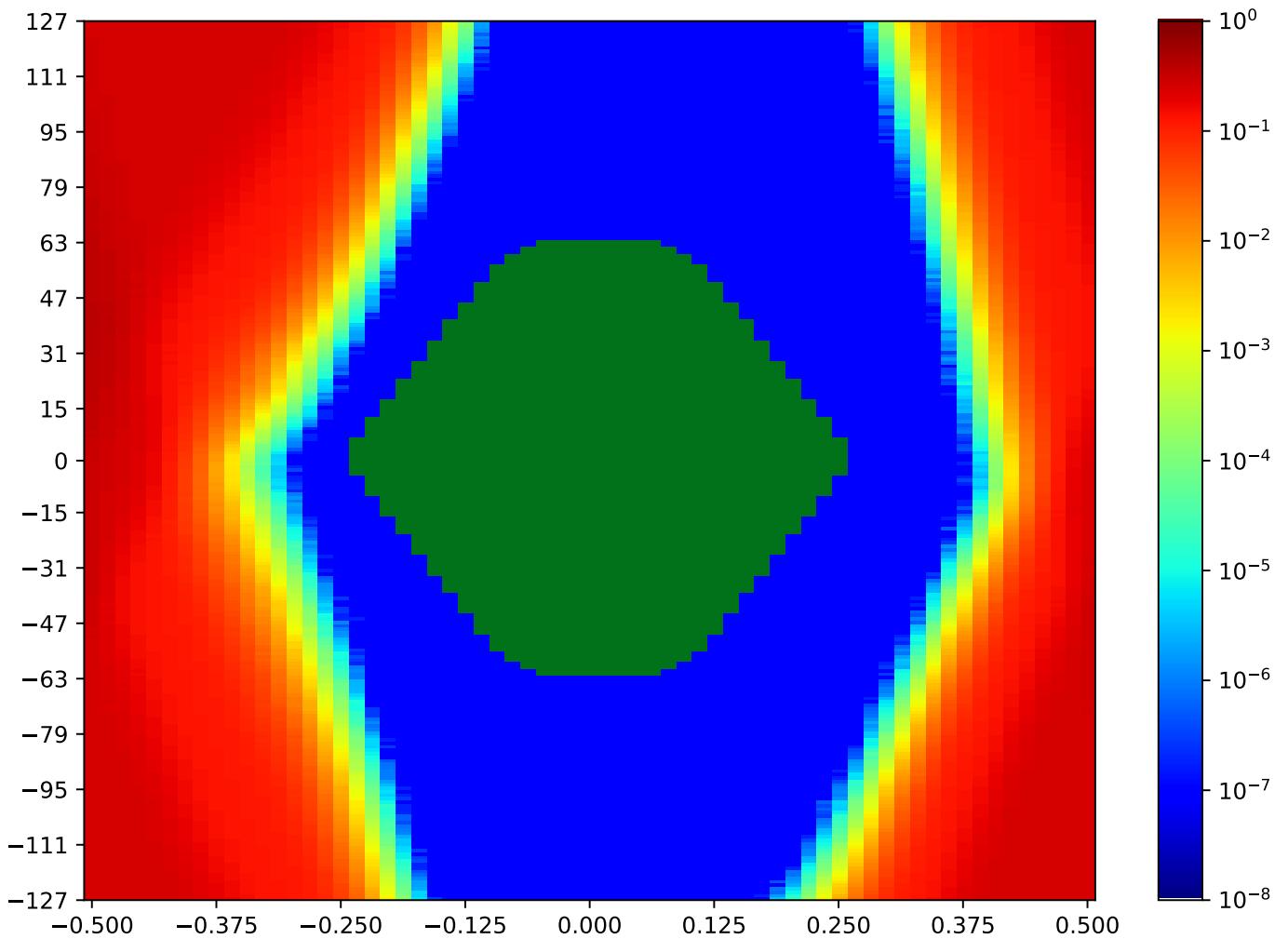


Figure 5.92: MSP_A_FPGA-IC39-22-IC4-22-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.24 MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

Table 5.85: MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:18:45		2018-Sep-27 17:19:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8629	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

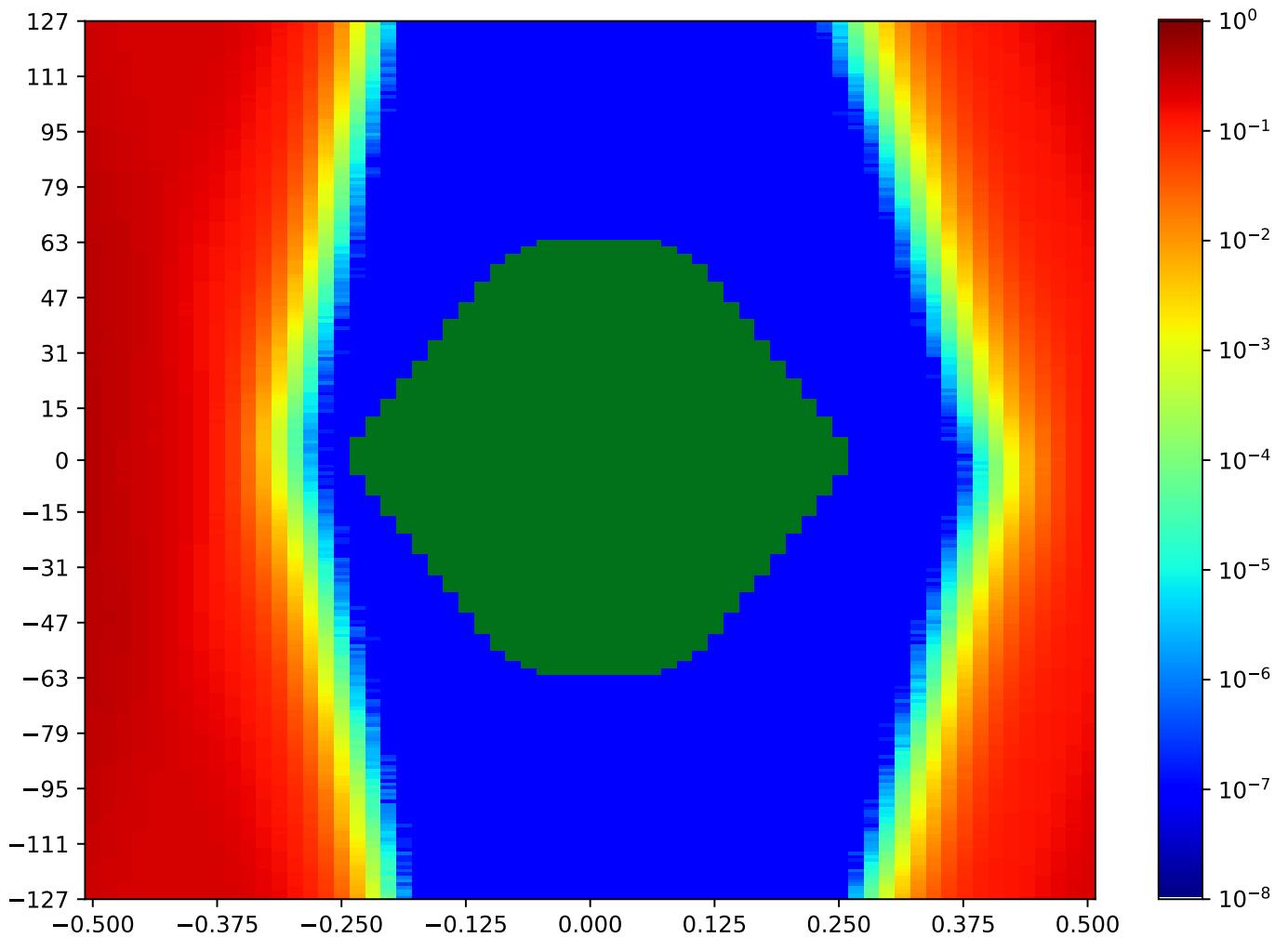


Figure 5.93: MSP_A_FPGA-IC39-23-IC4-23-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.25 MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

Table 5.86: MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:19:06		2018-Sep-27 17:19:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8082	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

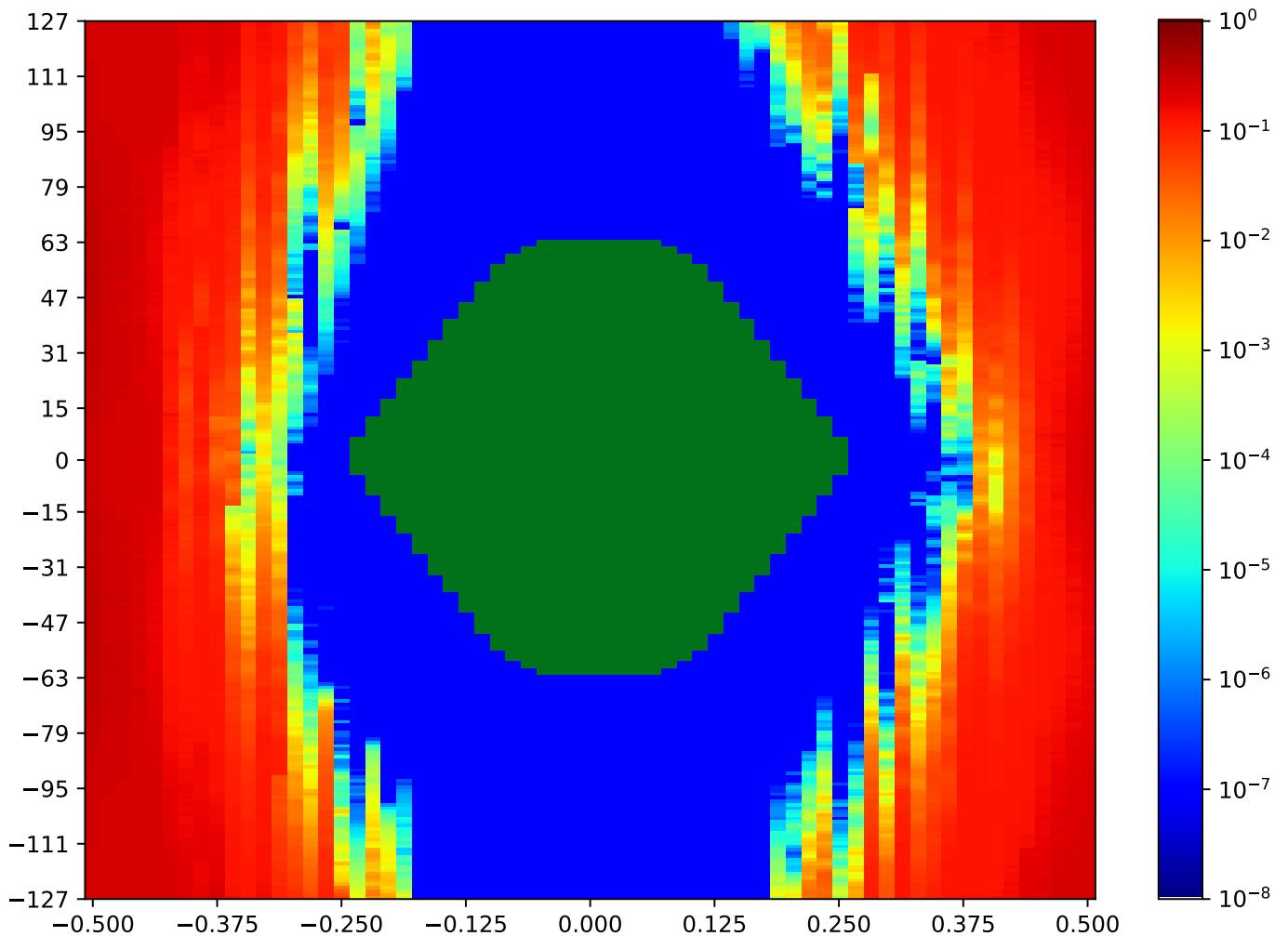


Figure 5.94: MSP_A_FPGA-IC39-24-IC4-24-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.26 MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

Table 5.87: MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:19:26		2018-Sep-27 17:19:46	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10222	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

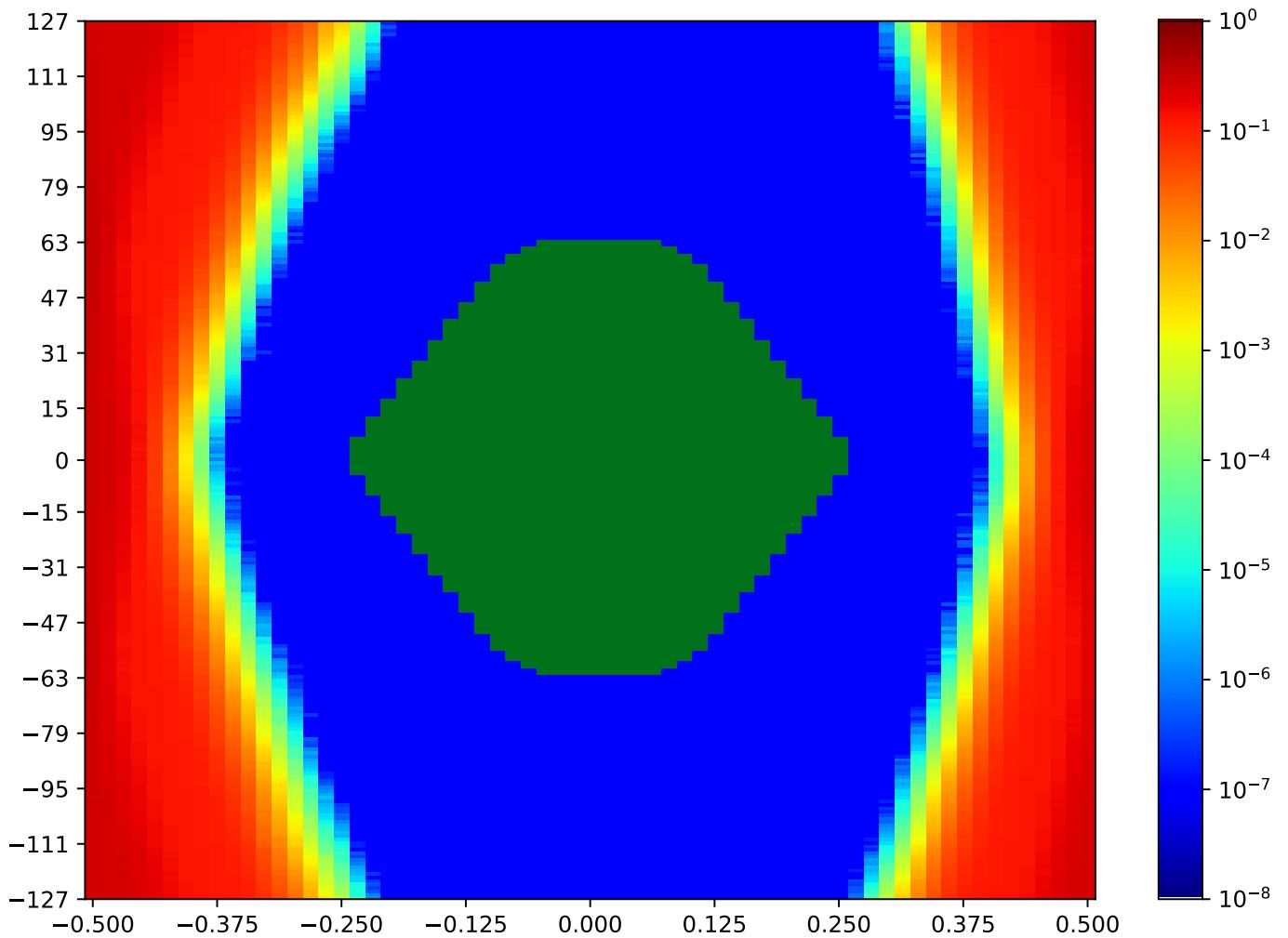


Figure 5.95: MSP_A_FPGA-IC39-25-IC4-25-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.27 MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

Table 5.88: MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:19:46		2018-Sep-27 17:20:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9305	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

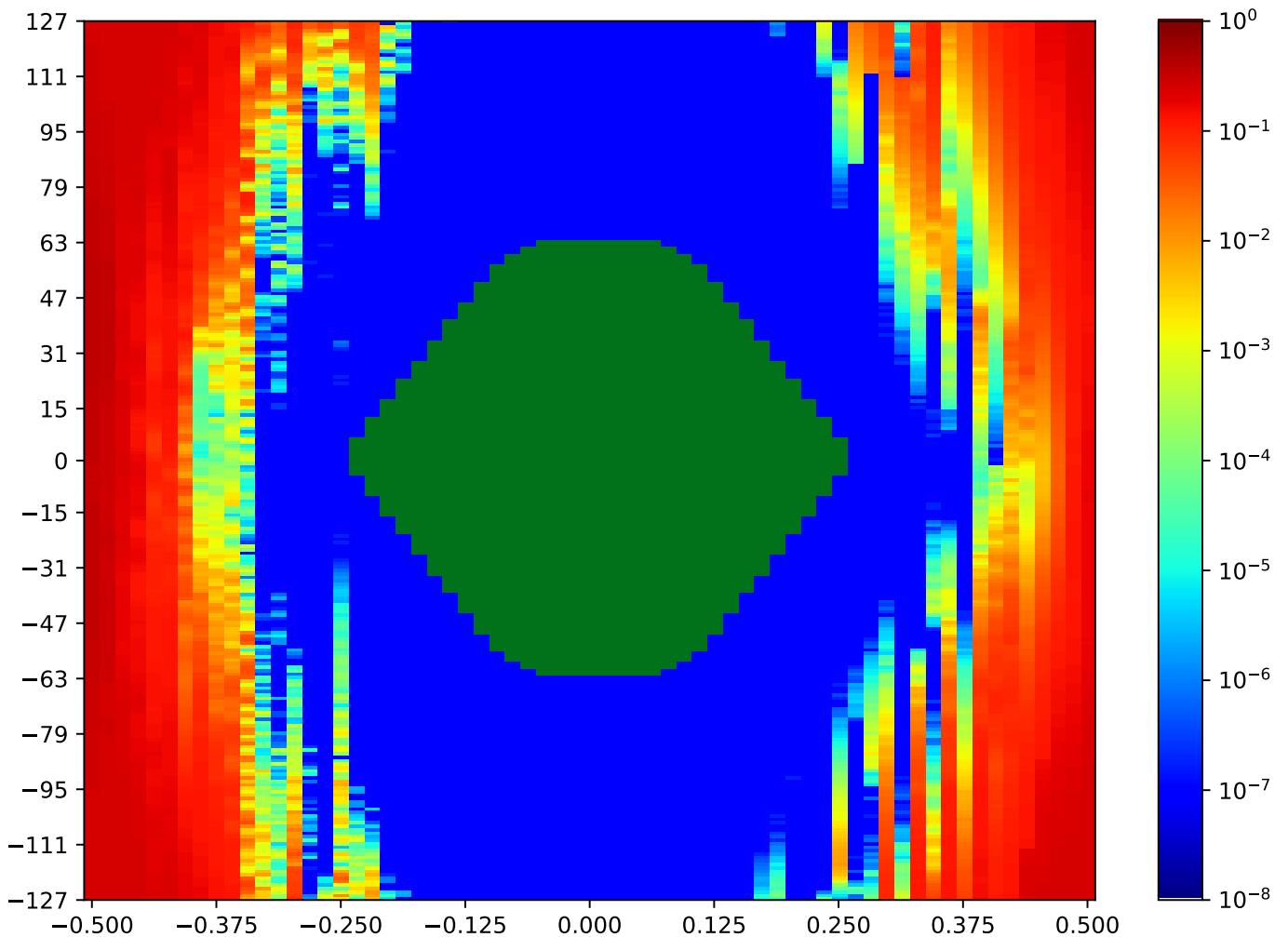


Figure 5.96: MSP_A_FPGA-IC39-26-IC4-26-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.8.28 MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

Table 5.89: MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTH	2018-Sep-27 17:20:07		2018-Sep-27 17:20:28	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9768	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0xC002 SVN: 0	

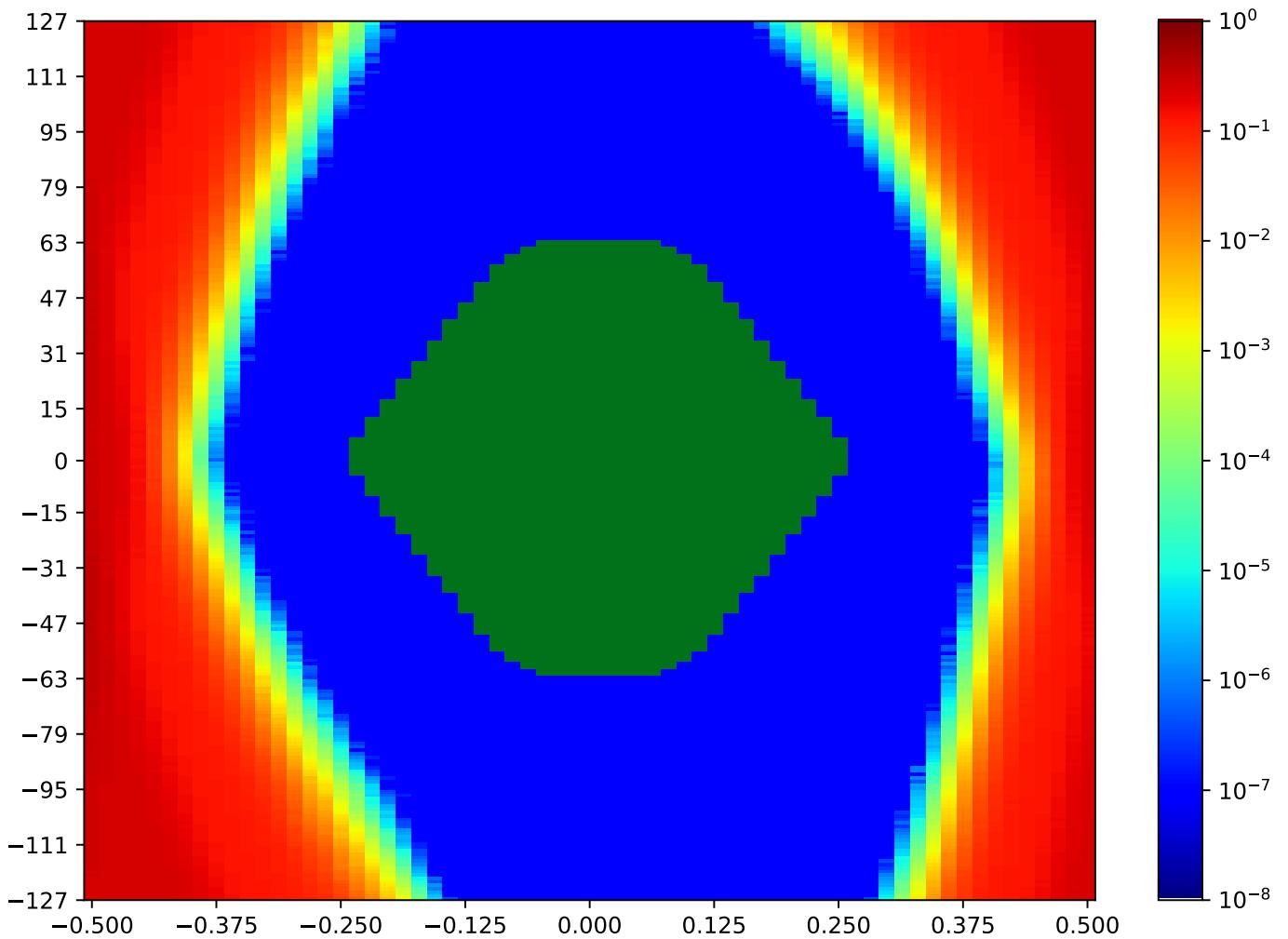


Figure 5.97: MSP_A_FPGA-IC39-27-IC4-27-TRP_FPGA

Call back to summary Figure 5.69. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9 MSP_C TRP On board links

A cross-reference to Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.
Next summary Figure 5.127.

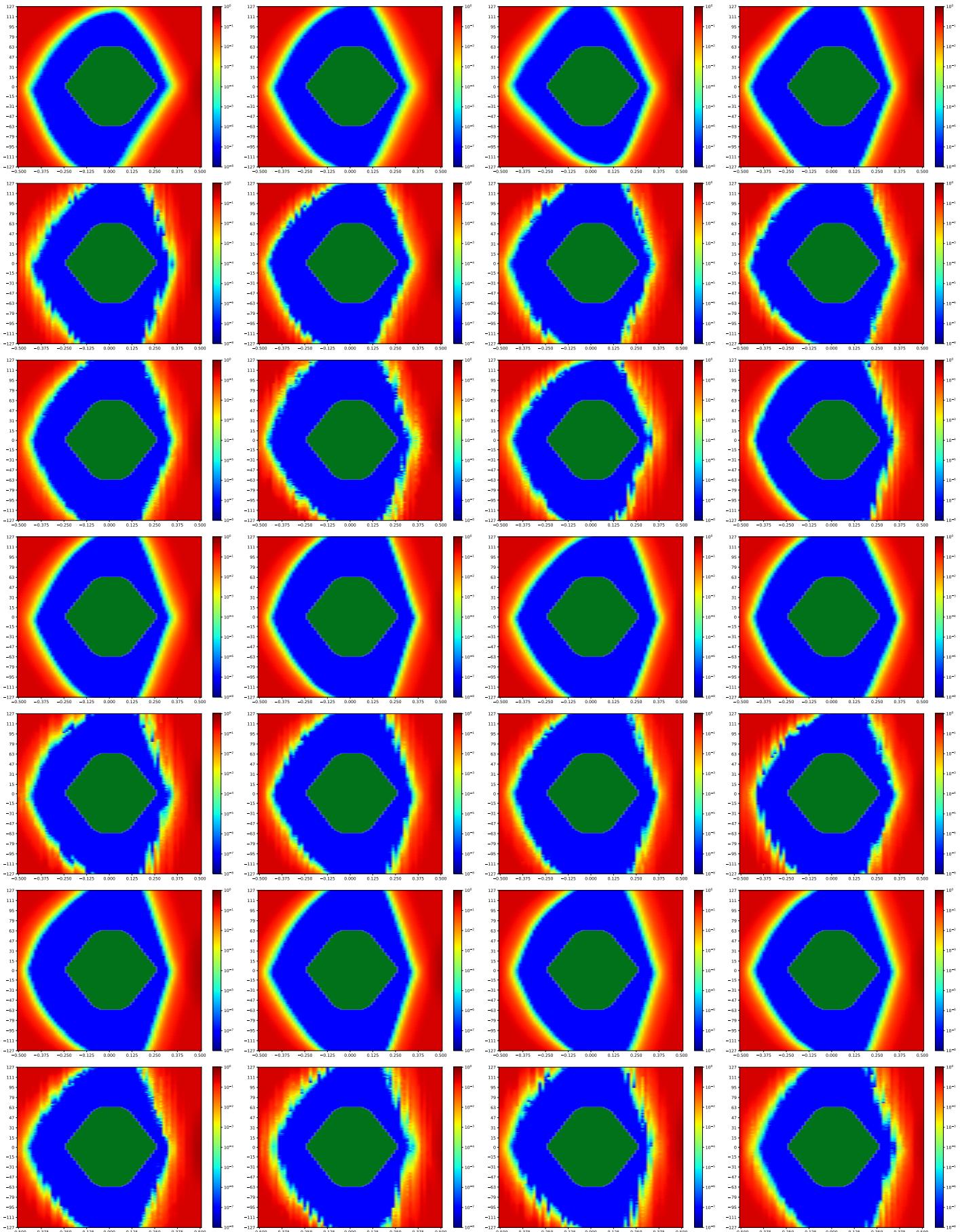


Figure 5.98: MSP_C TRP On board links

5.9.1 MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

Table 5.90: MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:20:28		2018-Sep-27 17:20:48	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7289	45	69.23%	243	94.90%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

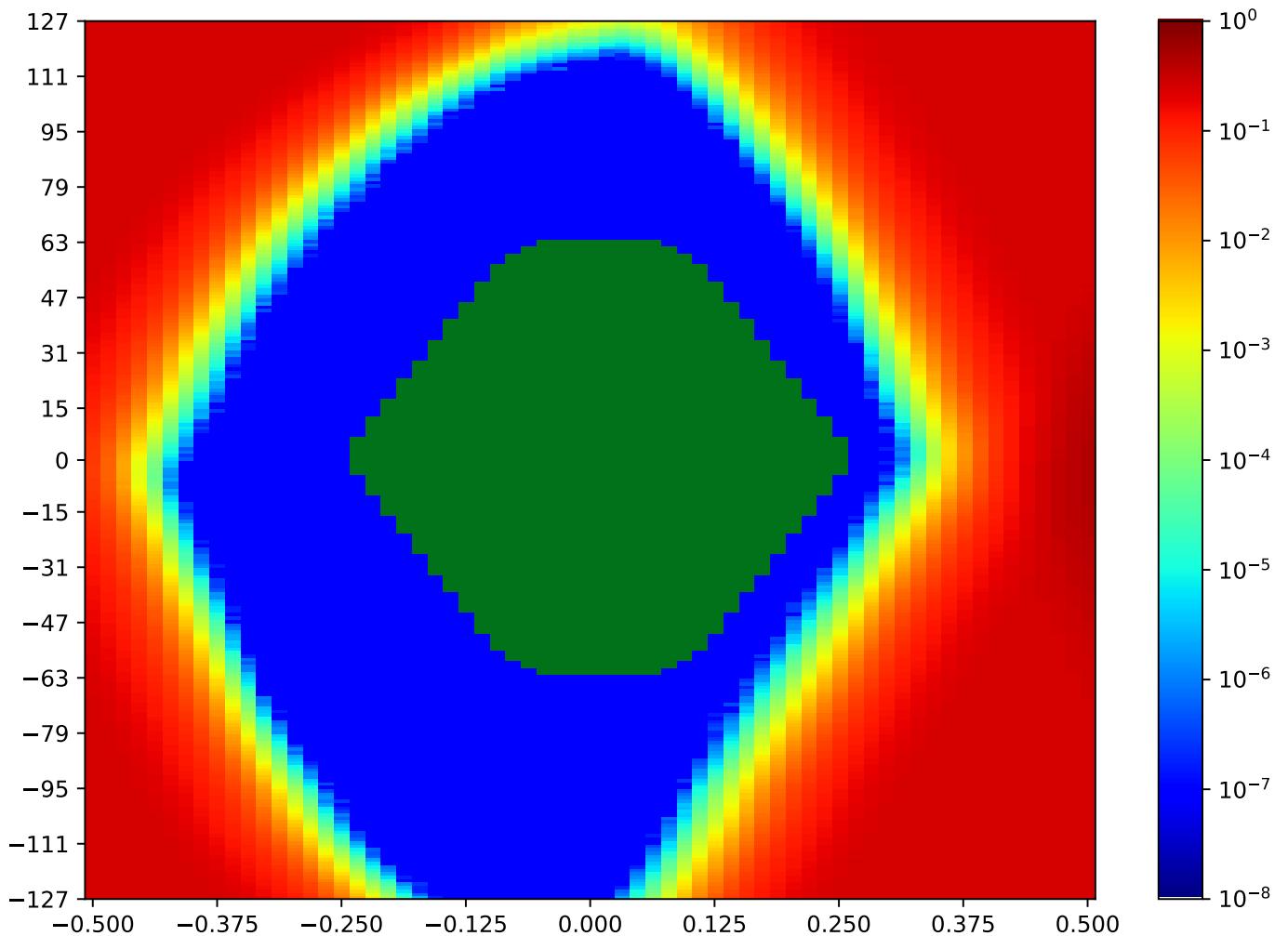


Figure 5.99: MSP_C_FPGA-IC39-00-IC15-00-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.2 MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

Table 5.91: MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:20:48		2018-Sep-27 17:21:08	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7647	45	69.23%	253	99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

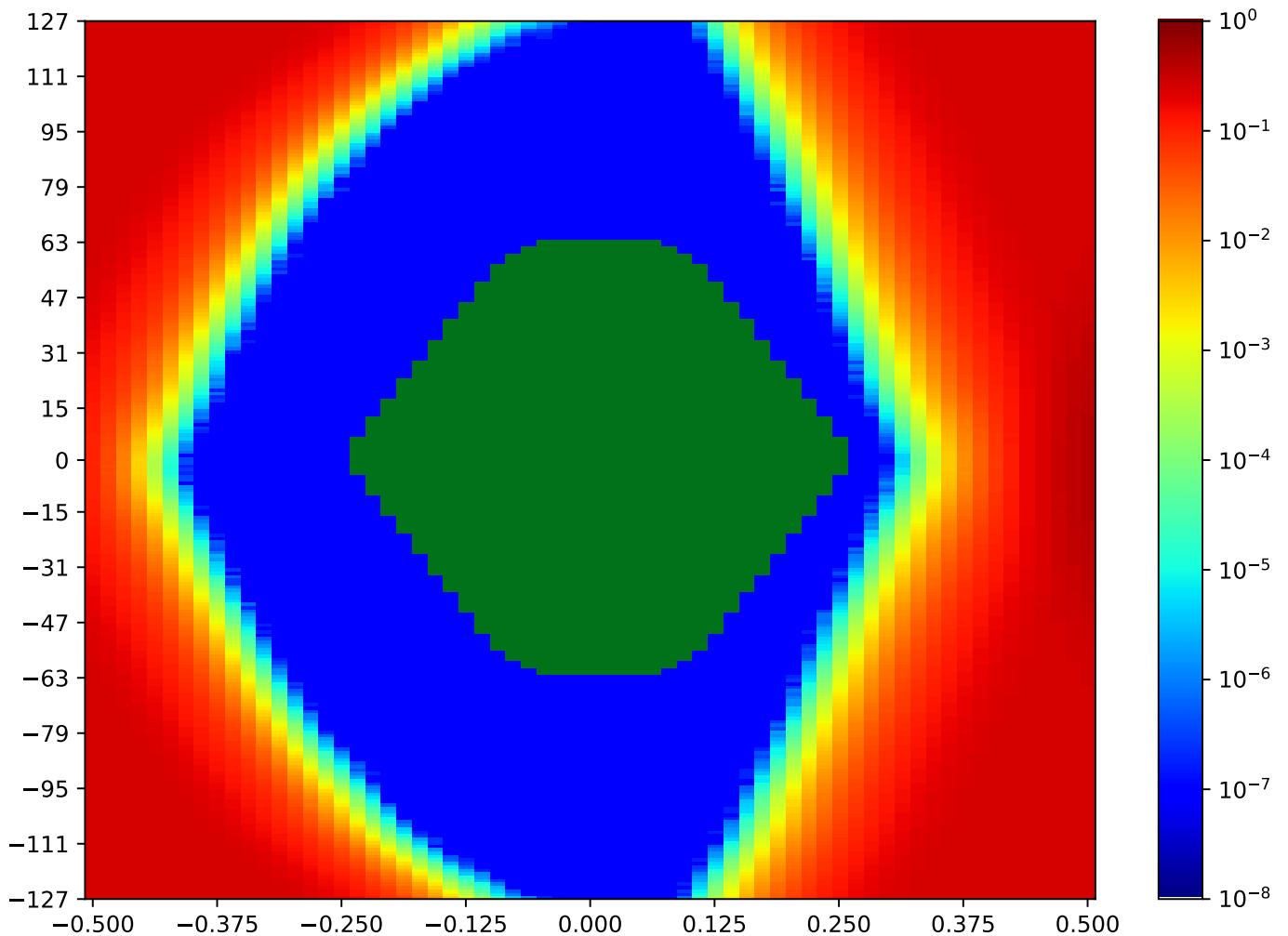


Figure 5.100: MSP_C_FPGA-IC39-01-IC15-01-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.3 MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

Table 5.92: MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:21:08		2018-Sep-27 17:21:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7237	44	67.69%	244	95.29%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

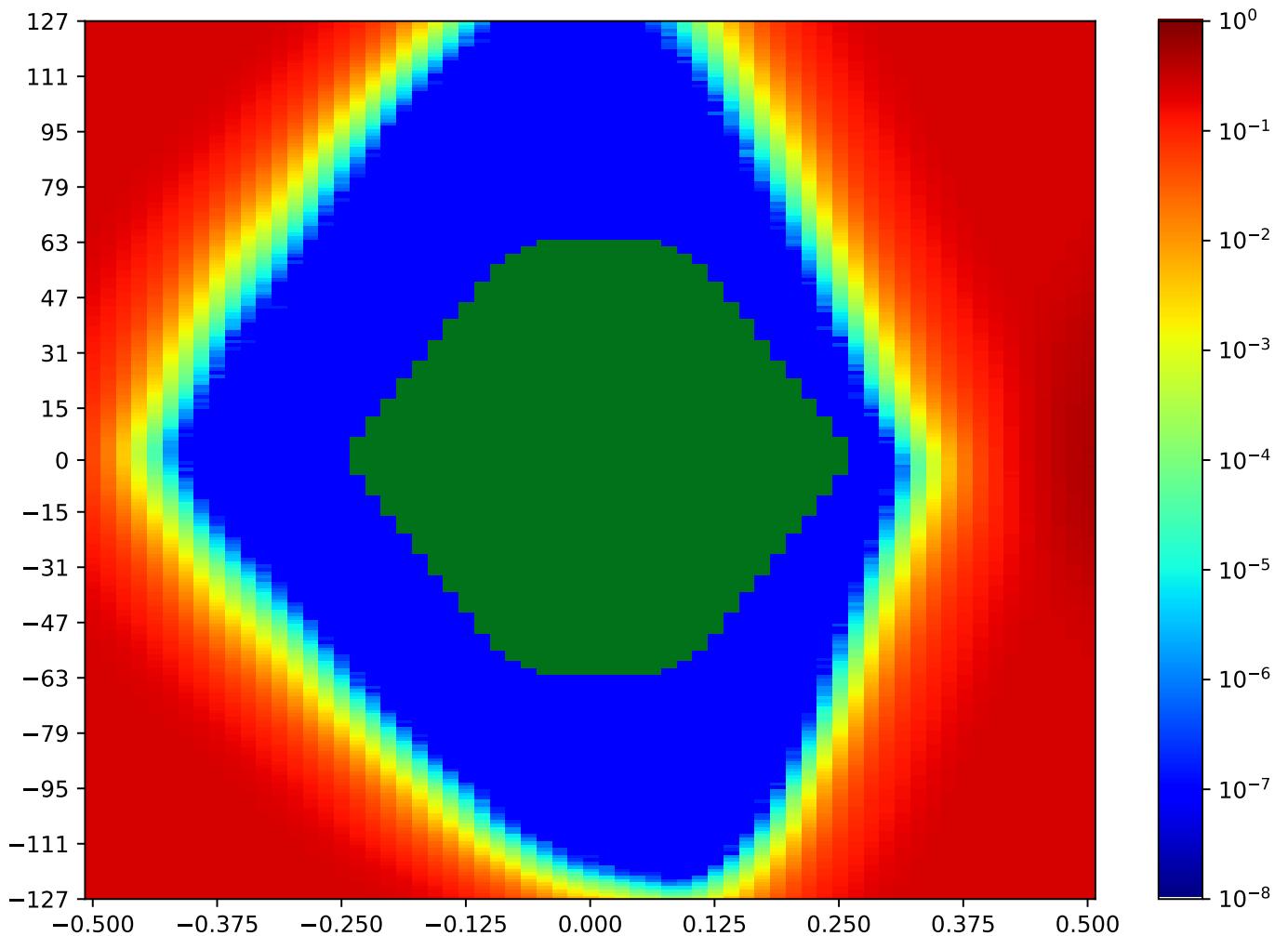


Figure 5.101: MSP_C_FPGA-IC39-02-IC15-02-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.4 MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

Table 5.93: MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:21:29		2018-Sep-27 17:21:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8569	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

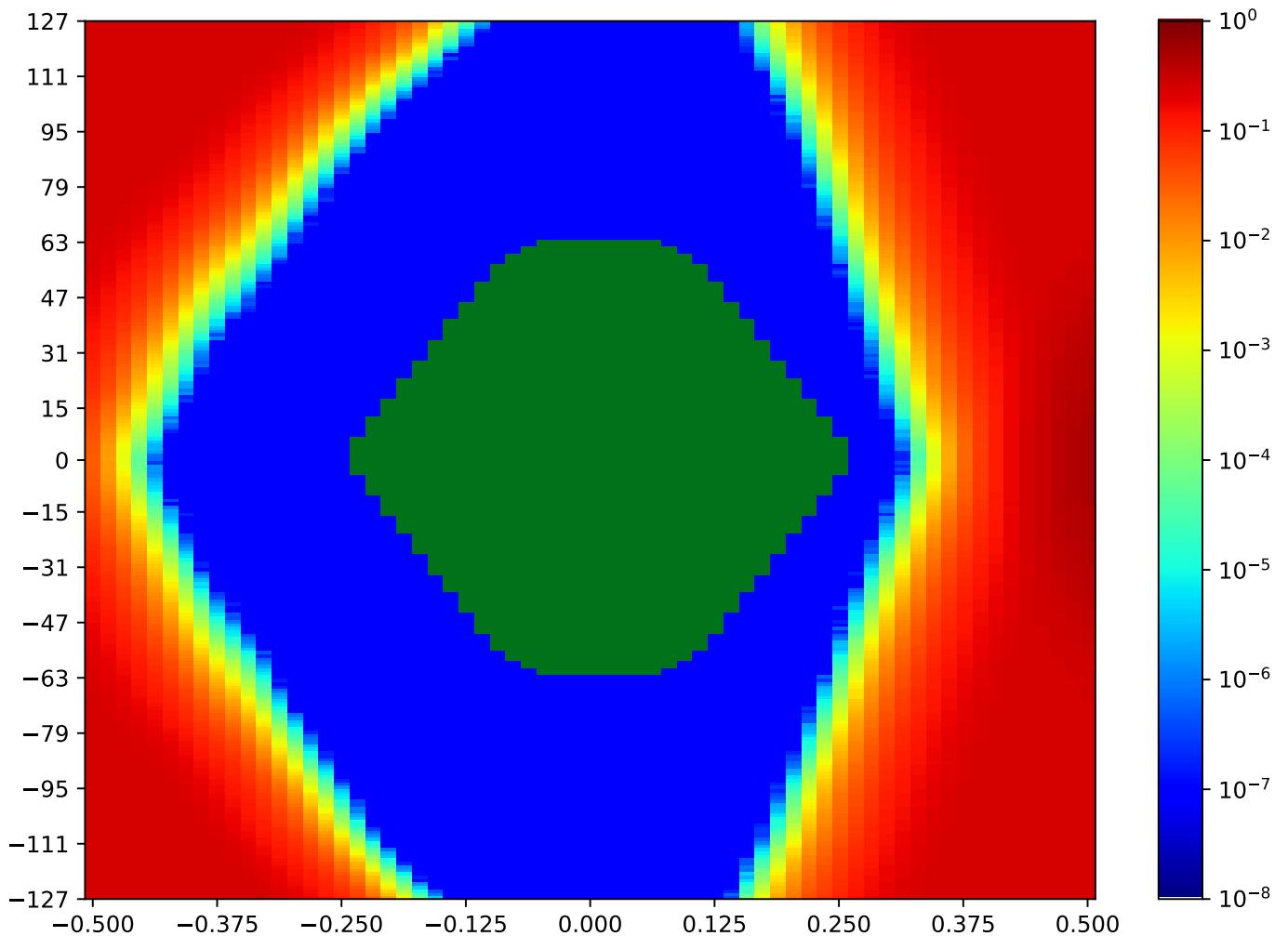


Figure 5.102: MSP_C_FPGA-IC39-03-IC15-03-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.5 MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

Table 5.94: MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:21:50		2018-Sep-27 17:22:10	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8625	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

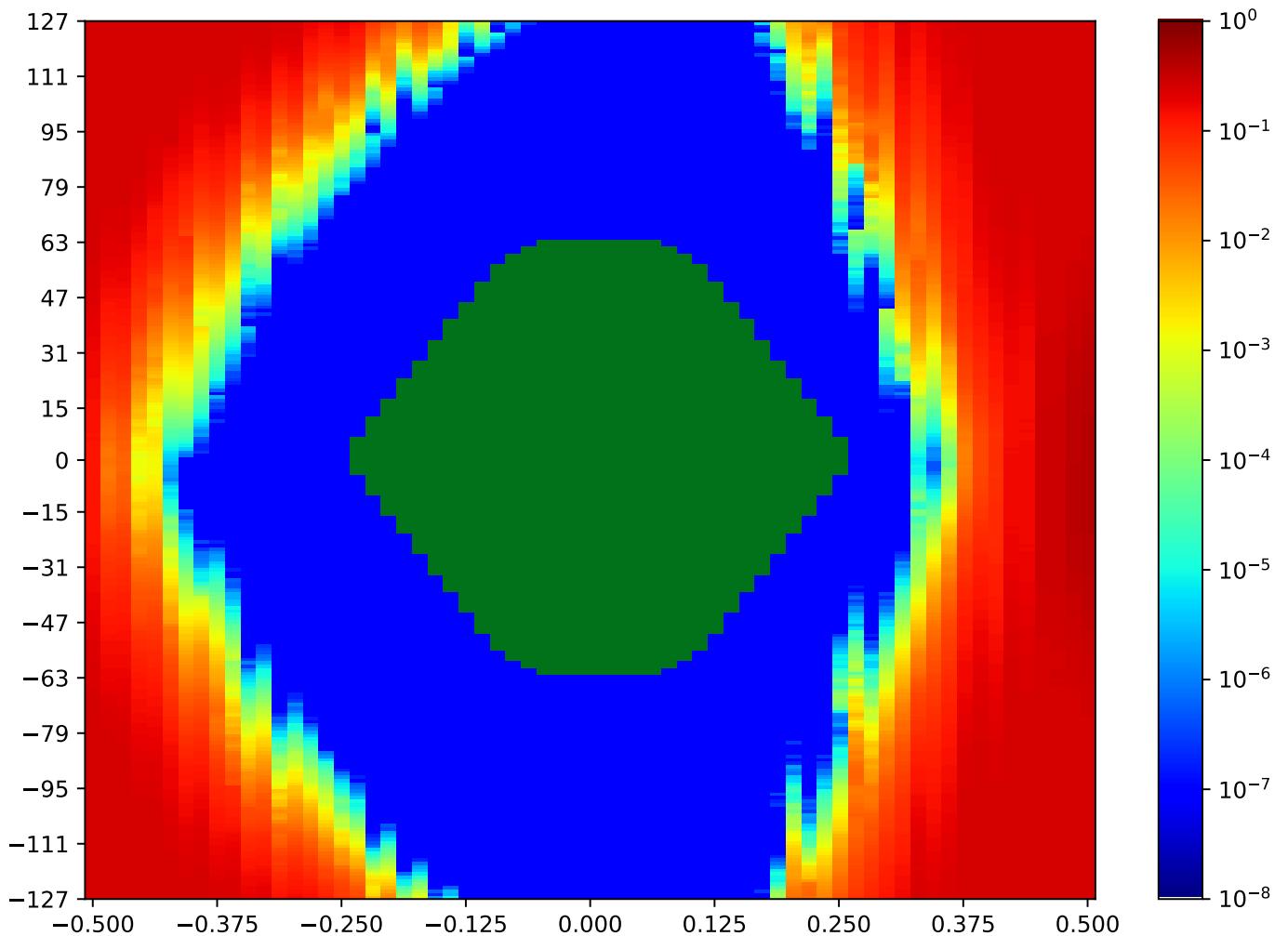


Figure 5.103: MSP_C_FPGA-IC39-04-IC15-04-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.6 MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

Table 5.95: MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:22:10		2018-Sep-27 17:22:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8721	48	73.85%	254	98.43%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

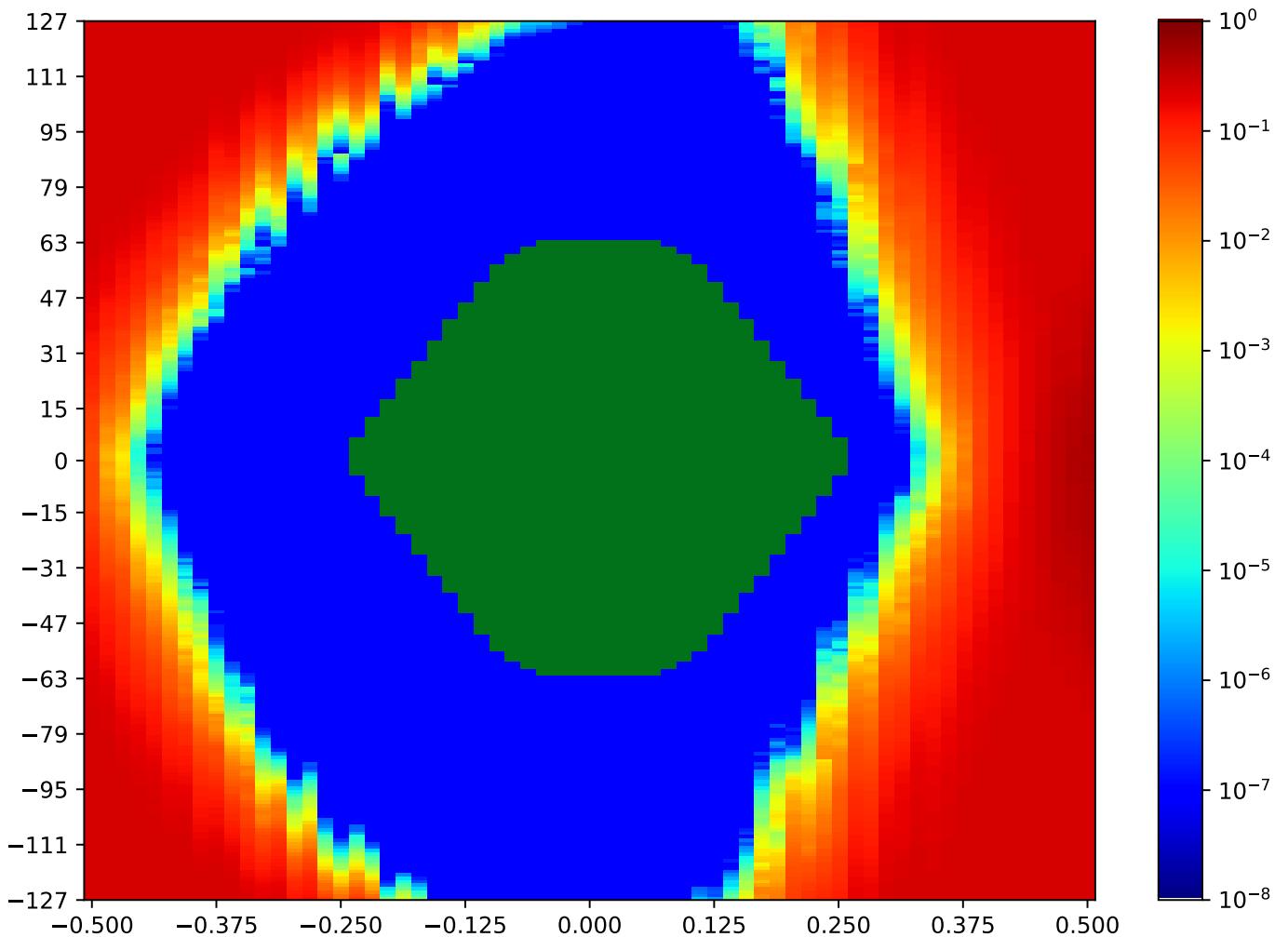


Figure 5.104: MSP_C_FPGA-IC39-05-IC15-05-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.7 MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

Table 5.96: MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:22:31		2018-Sep-27 17:22:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8872	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

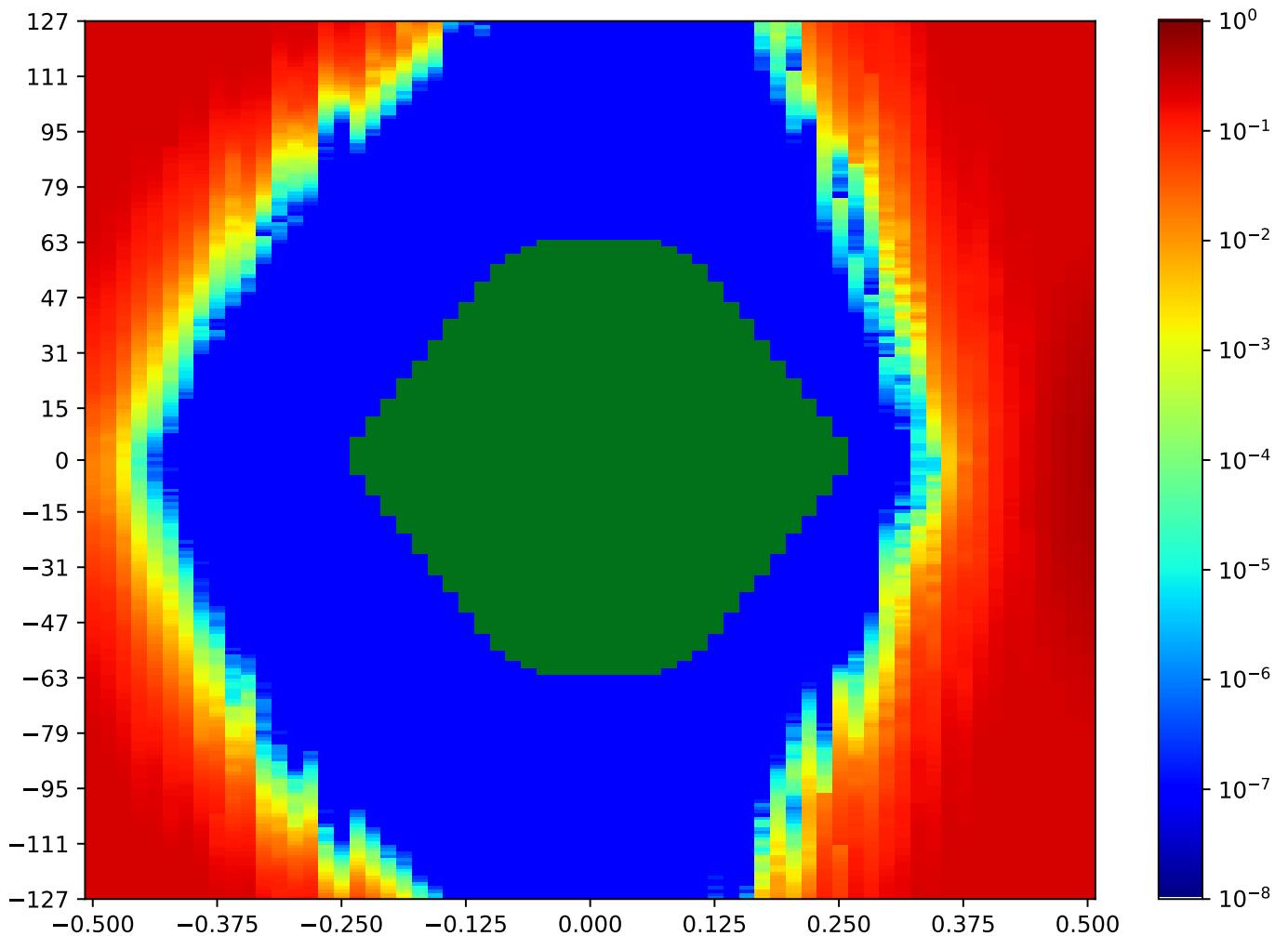


Figure 5.105: MSP_C_FPGA-IC39-06-IC15-06-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.8 MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

Table 5.97: MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:22:51		2018-Sep-27 17:23:11	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9100	49	75.38%	254	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

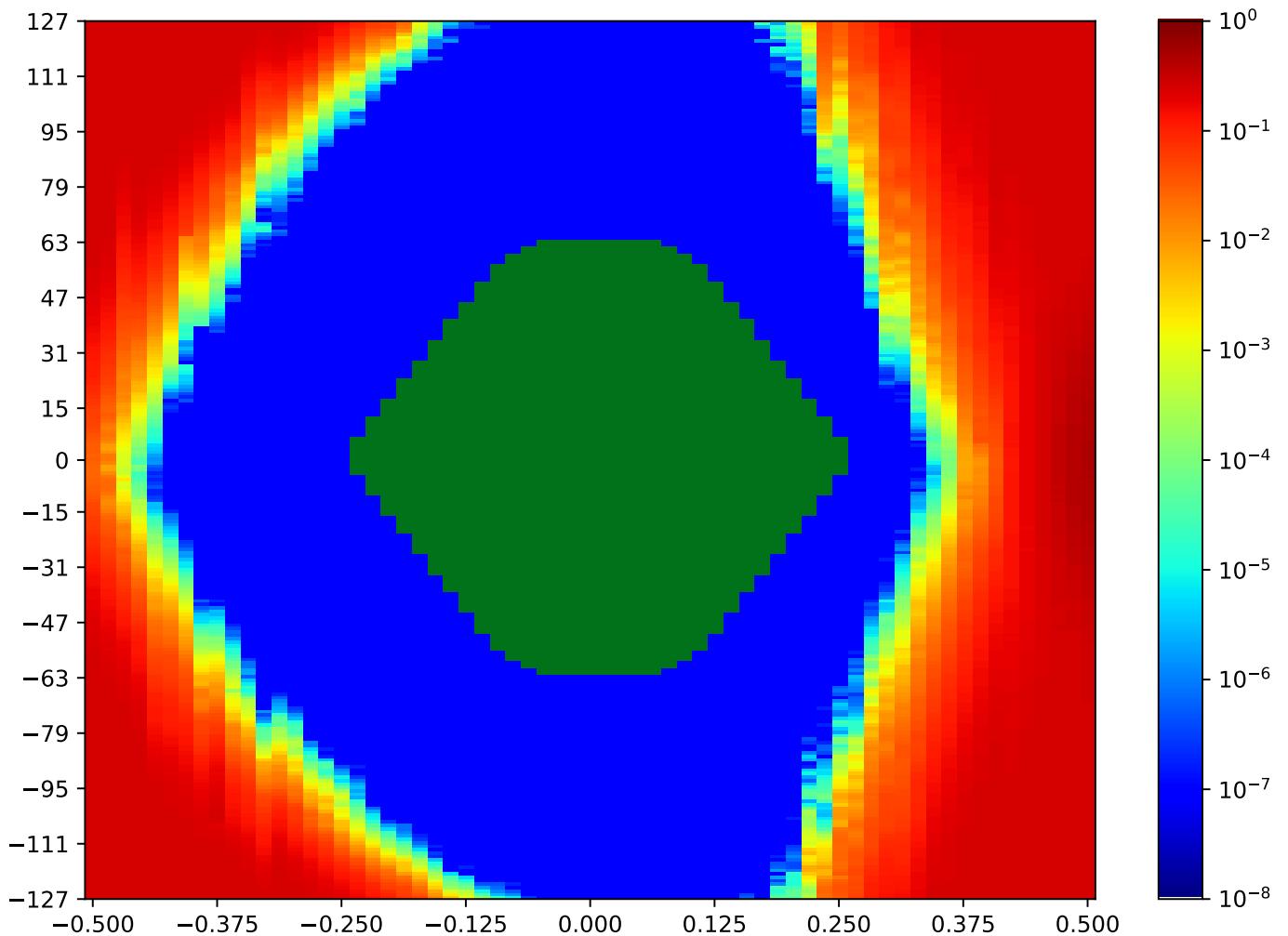


Figure 5.106: MSP_C_FPGA-IC39-07-IC15-07-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.9 MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

Table 5.98: MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:23:11		2018-Sep-27 17:23:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8875	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

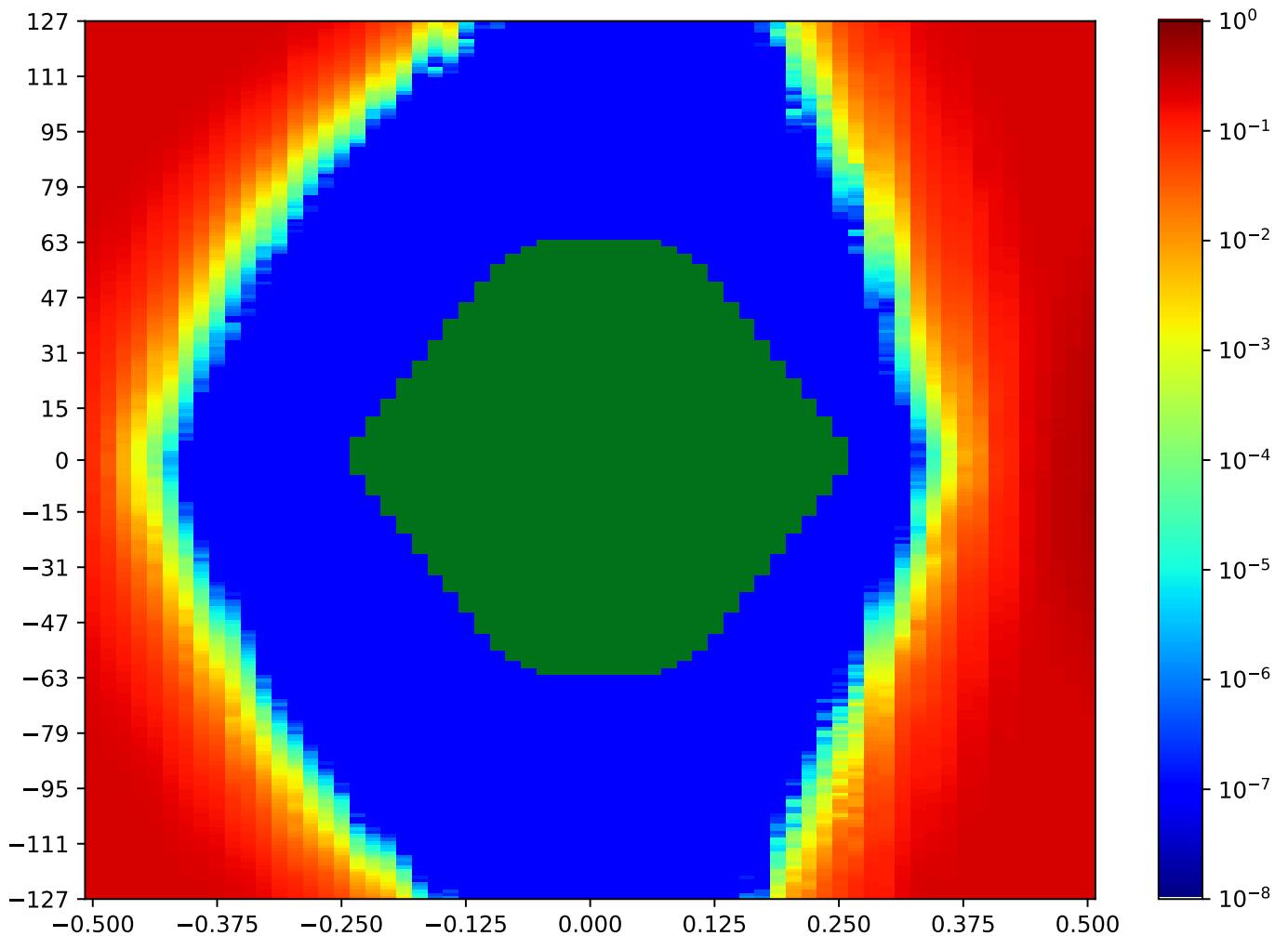


Figure 5.107: MSP_C_FPGA-IC39-08-IC15-08-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.10 MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

Table 5.99: MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:23:32		2018-Sep-27 17:23:52	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9068	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

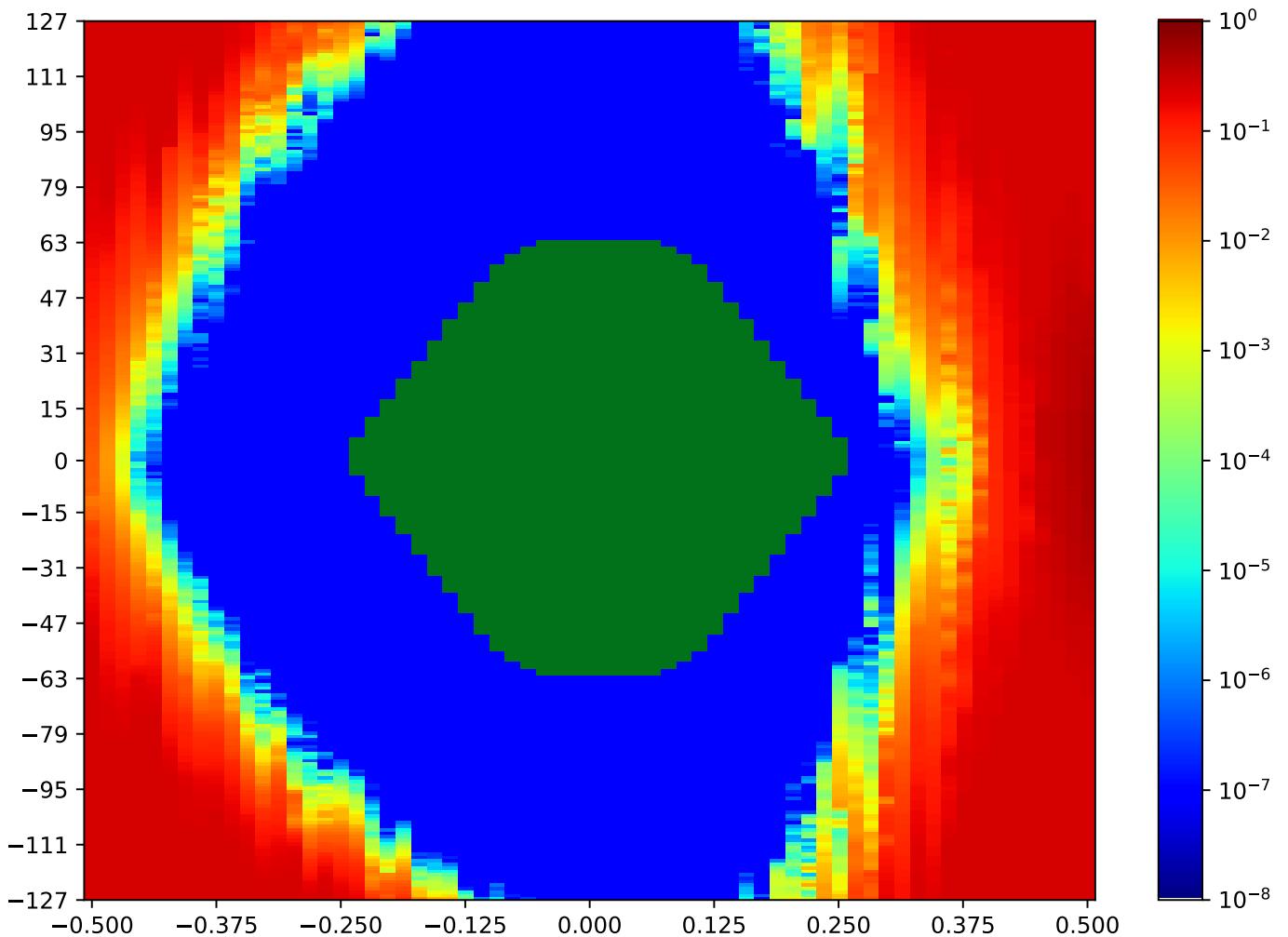


Figure 5.108: MSP_C_FPGA-IC39-09-IC15-09-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.11 MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

Table 5.100: MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:23:52		2018-Sep-27 17:24:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8236	49	73.85%	252	98.43%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

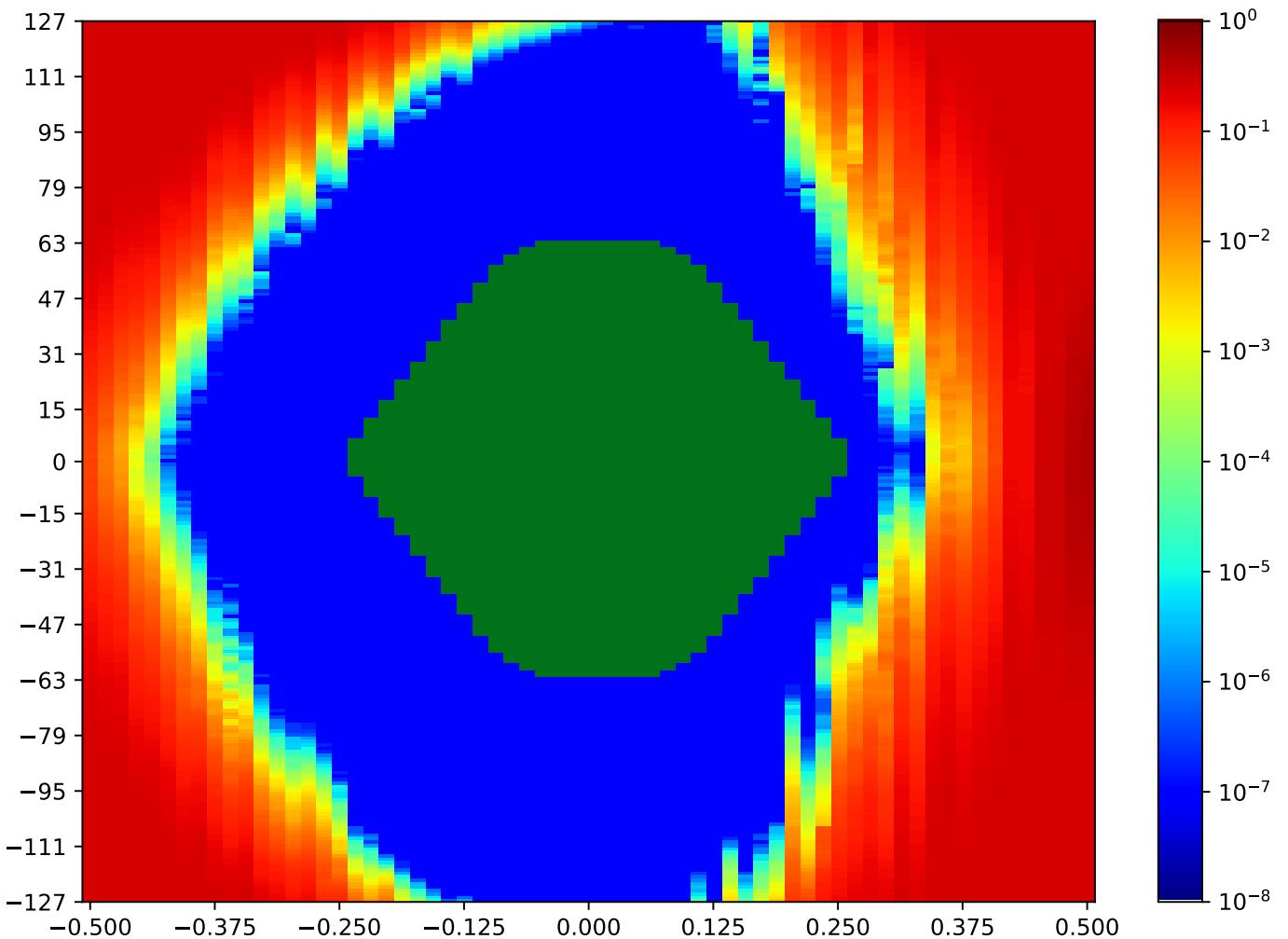


Figure 5.109: MSP_C_FPGA-IC39-10-IC15-10-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.12 MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

Table 5.101: MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:24:12		2018-Sep-27 17:24:33	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8975	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

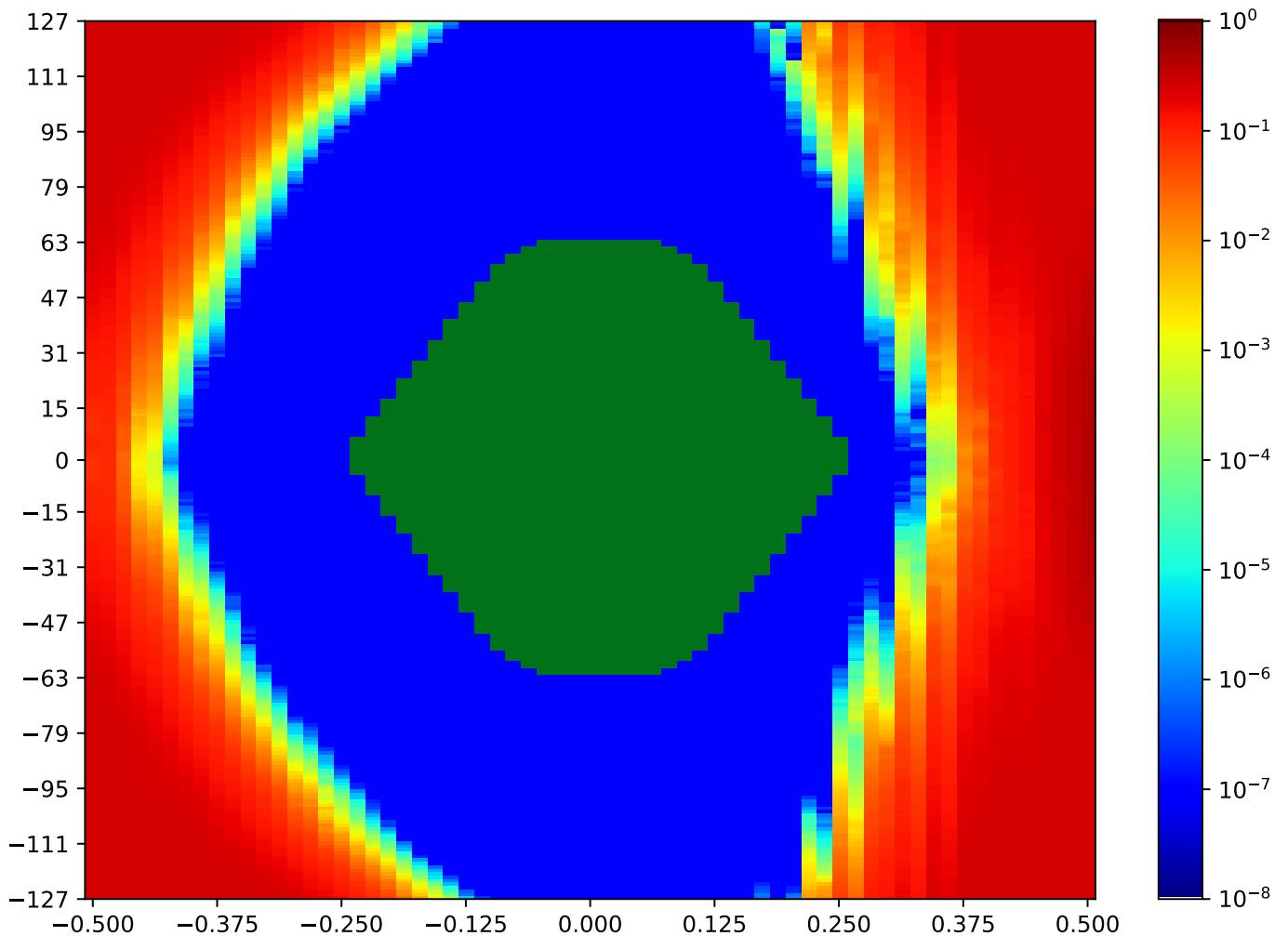


Figure 5.110: MSP_C_FPGA-IC39-11-IC15-11-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.13 MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

Table 5.102: MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:24:33		2018-Sep-27 17:24:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8256	45	69.23%	254	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

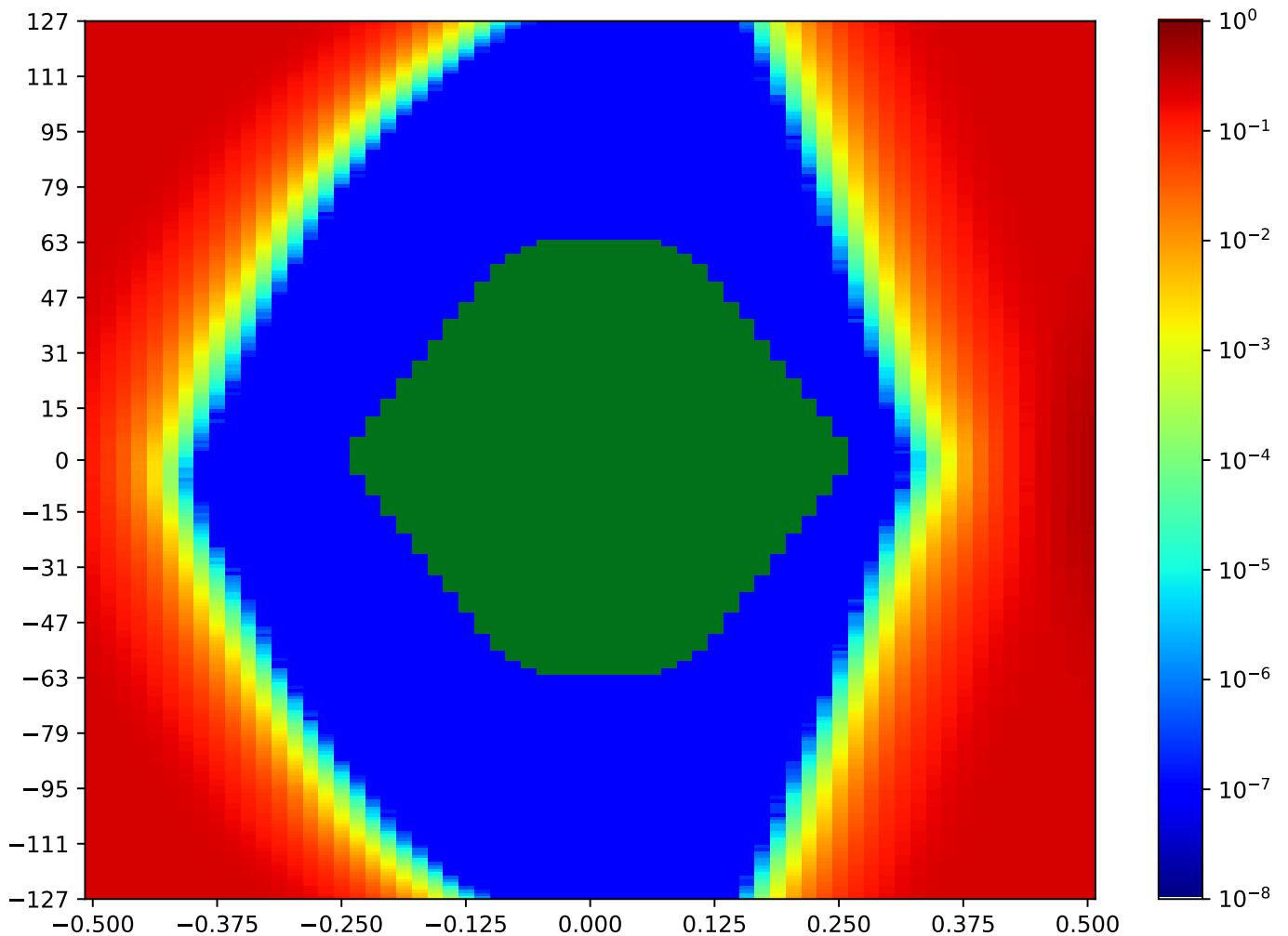


Figure 5.111: MSP_C_FPGA-IC39-12-IC15-12-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.14 MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

Table 5.103: MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:24:53		2018-Sep-27 17:25:13	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9190	48	73.85%	255	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

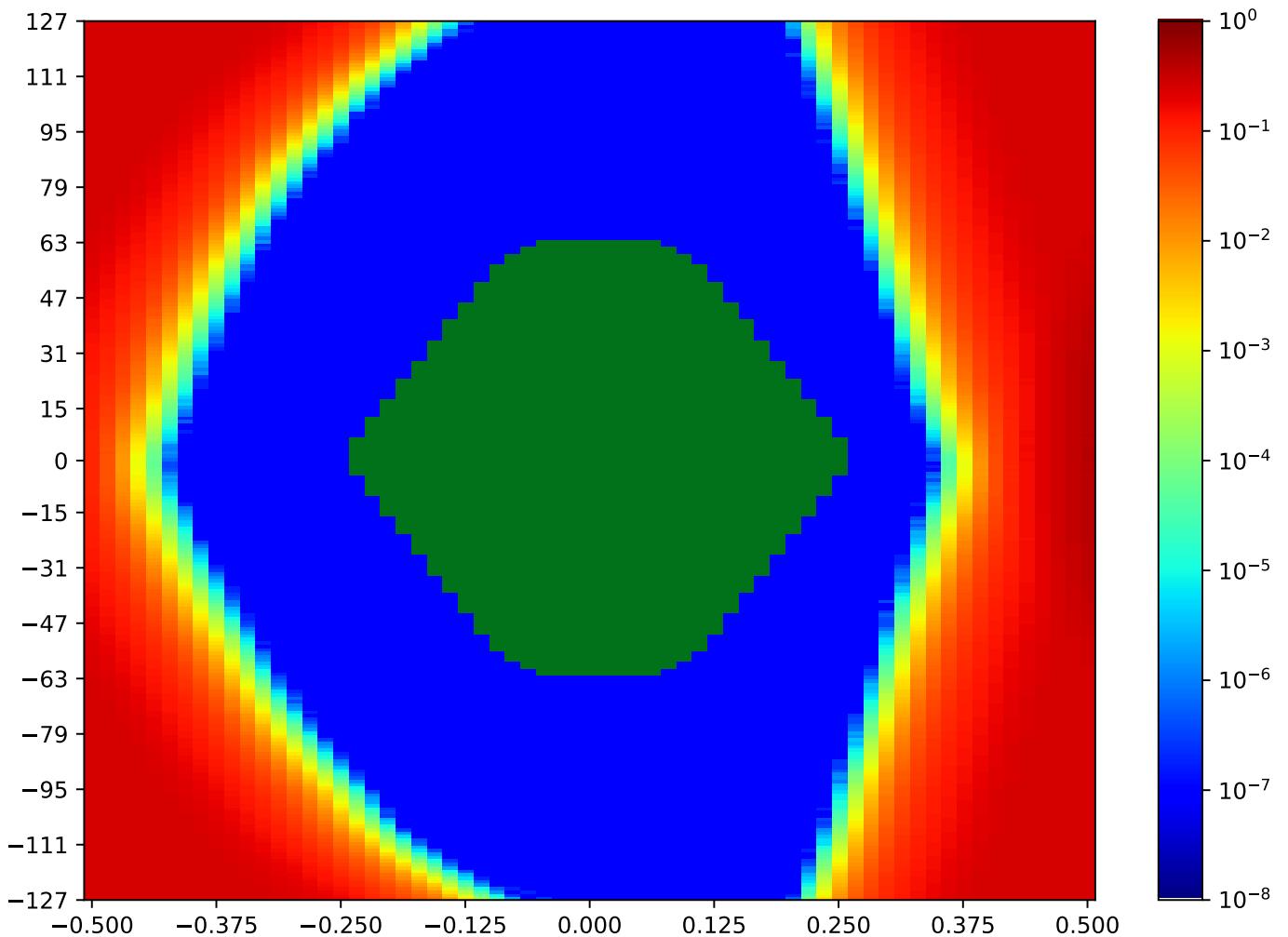


Figure 5.112: MSP_C_FPGA-IC39-13-IC15-13-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.15 MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

Table 5.104: MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:25:14		2018-Sep-27 17:25:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8838	48	73.85%	252	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

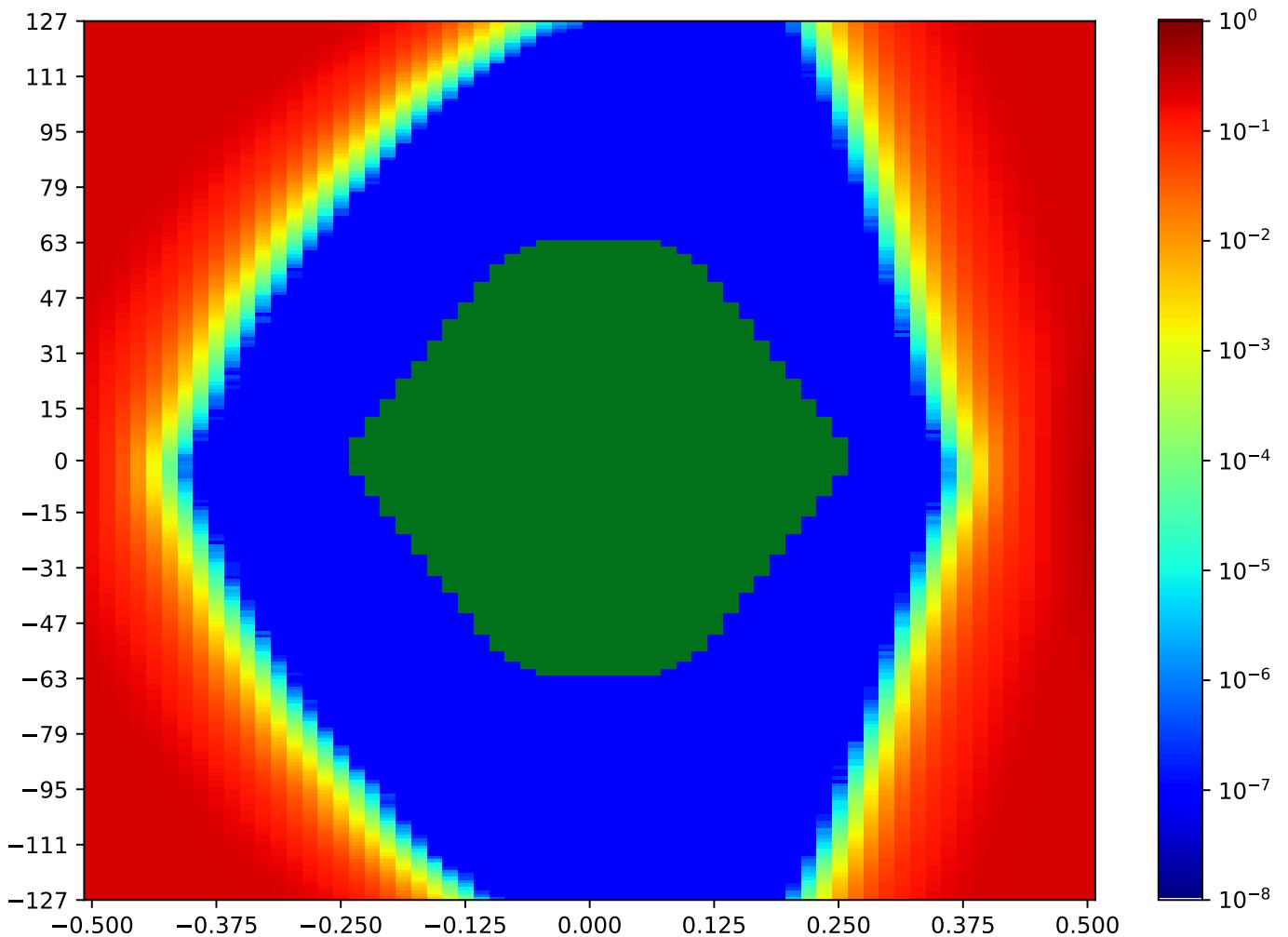


Figure 5.113: MSP_C_FPGA-IC39-14-IC15-14-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.16 MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

Table 5.105: MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:25:34		2018-Sep-27 17:25:54	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9126	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

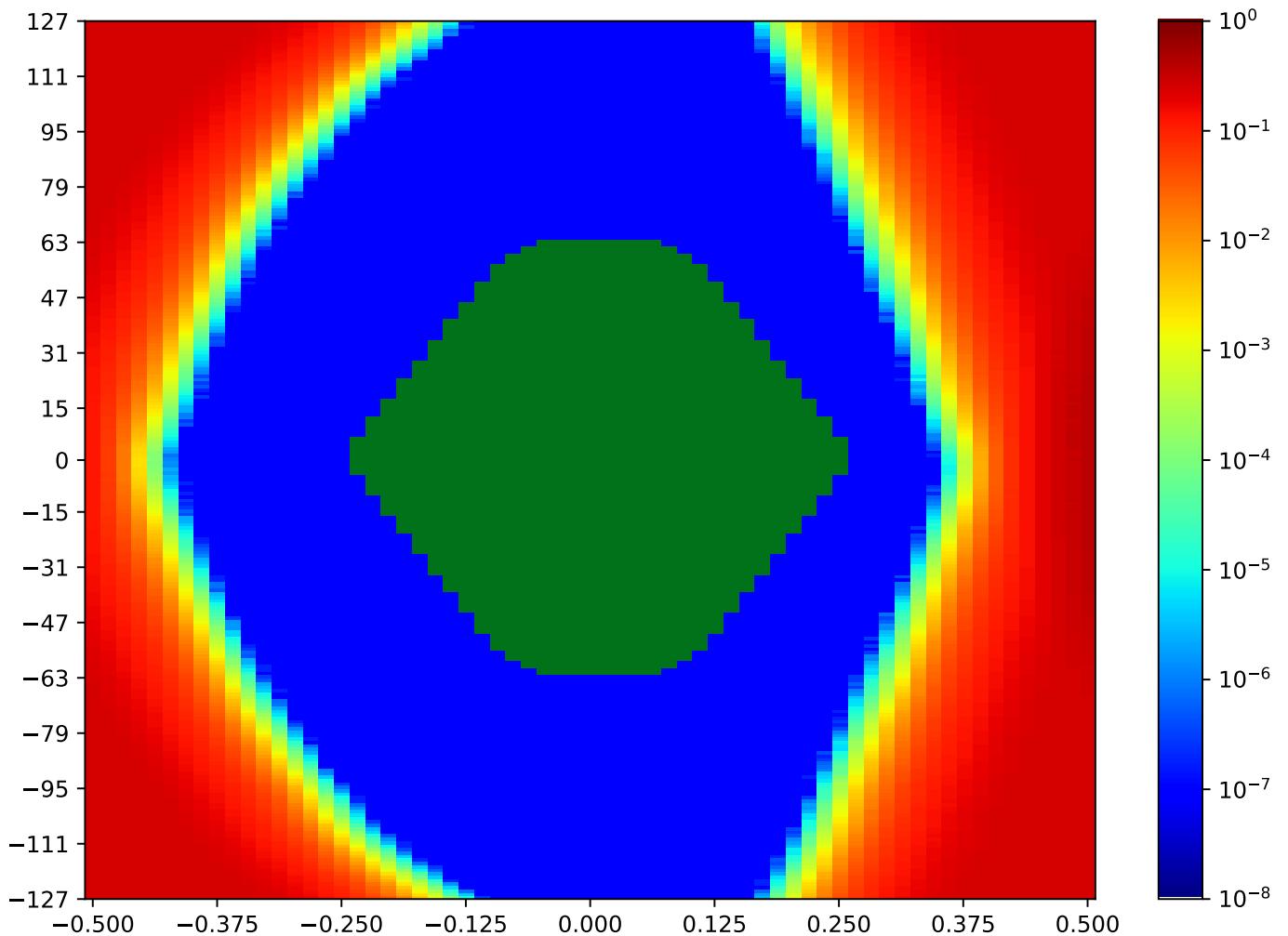


Figure 5.114: MSP_C_FPGA-IC39-15-IC15-15-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.17 MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

Table 5.106: MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:25:54		2018-Sep-27 17:26:14	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8641	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

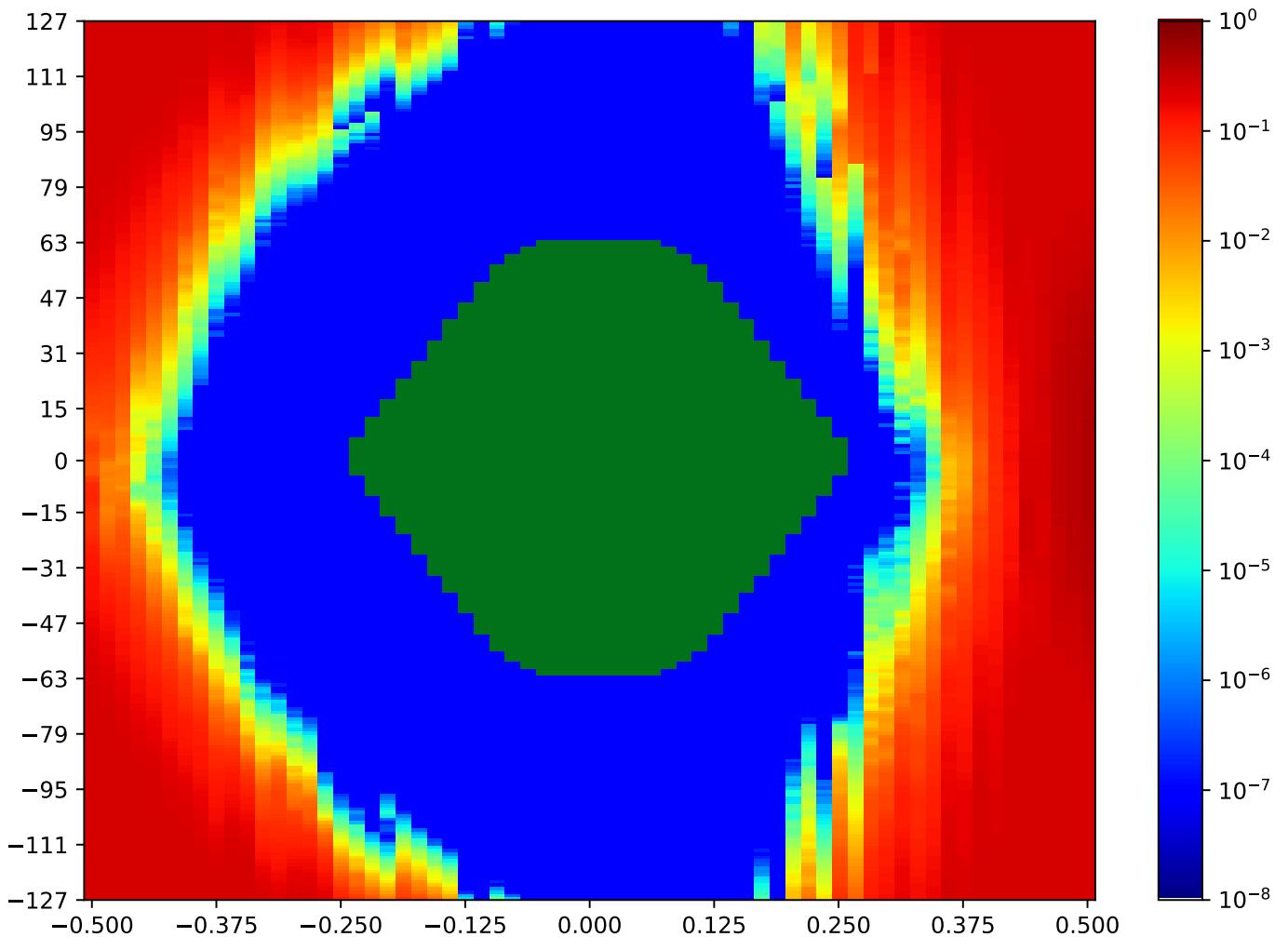


Figure 5.115: MSP_C_FPGA-IC39-16-IC15-16-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.18 MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

Table 5.107: MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:26:15		2018-Sep-27 17:26:35	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8913	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

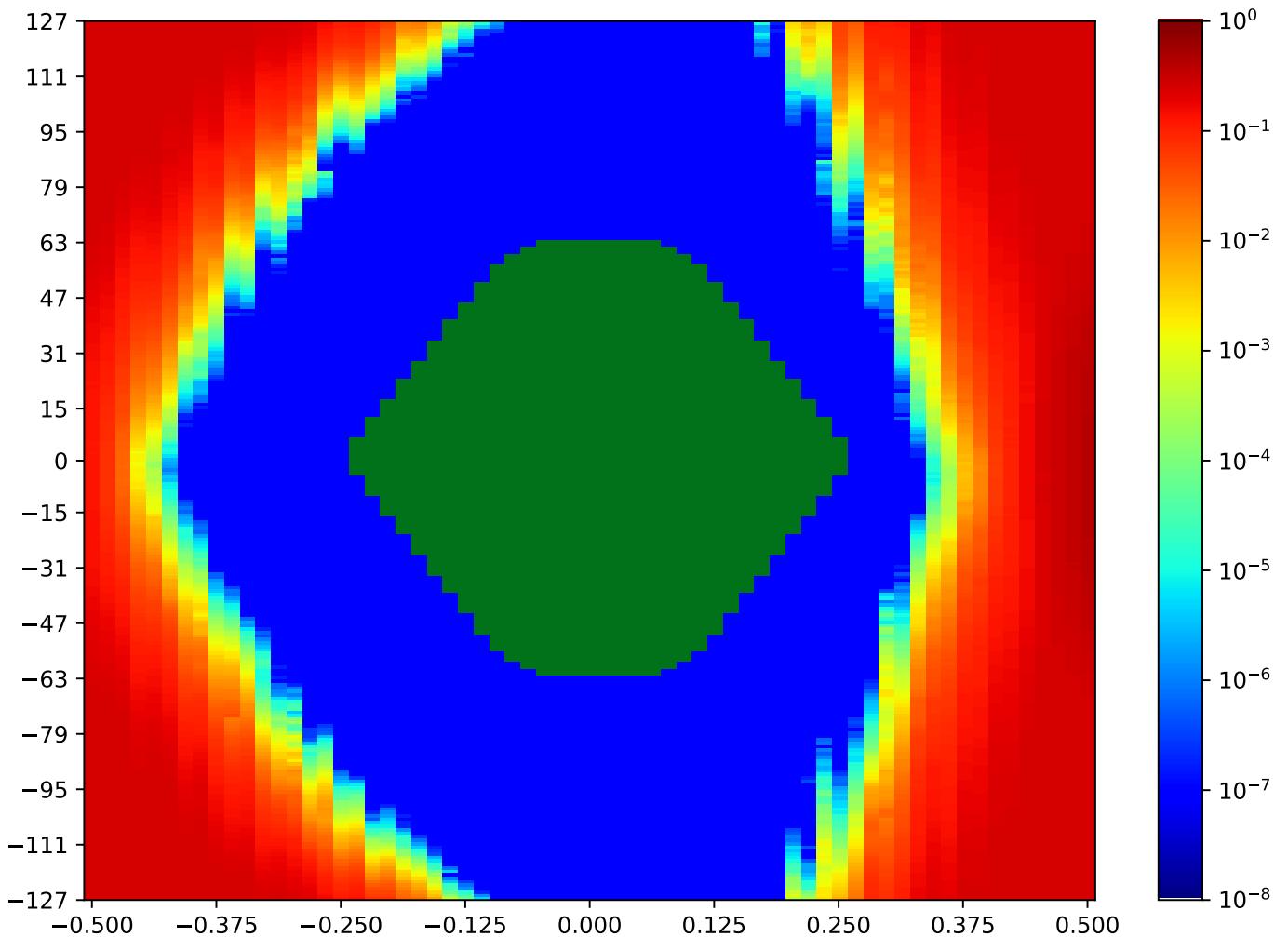


Figure 5.116: MSP_C_FPGA-IC39-17-IC15-17-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.19 MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

Table 5.108: MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:26:35		2018-Sep-27 17:26:55	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9327	49	75.38%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

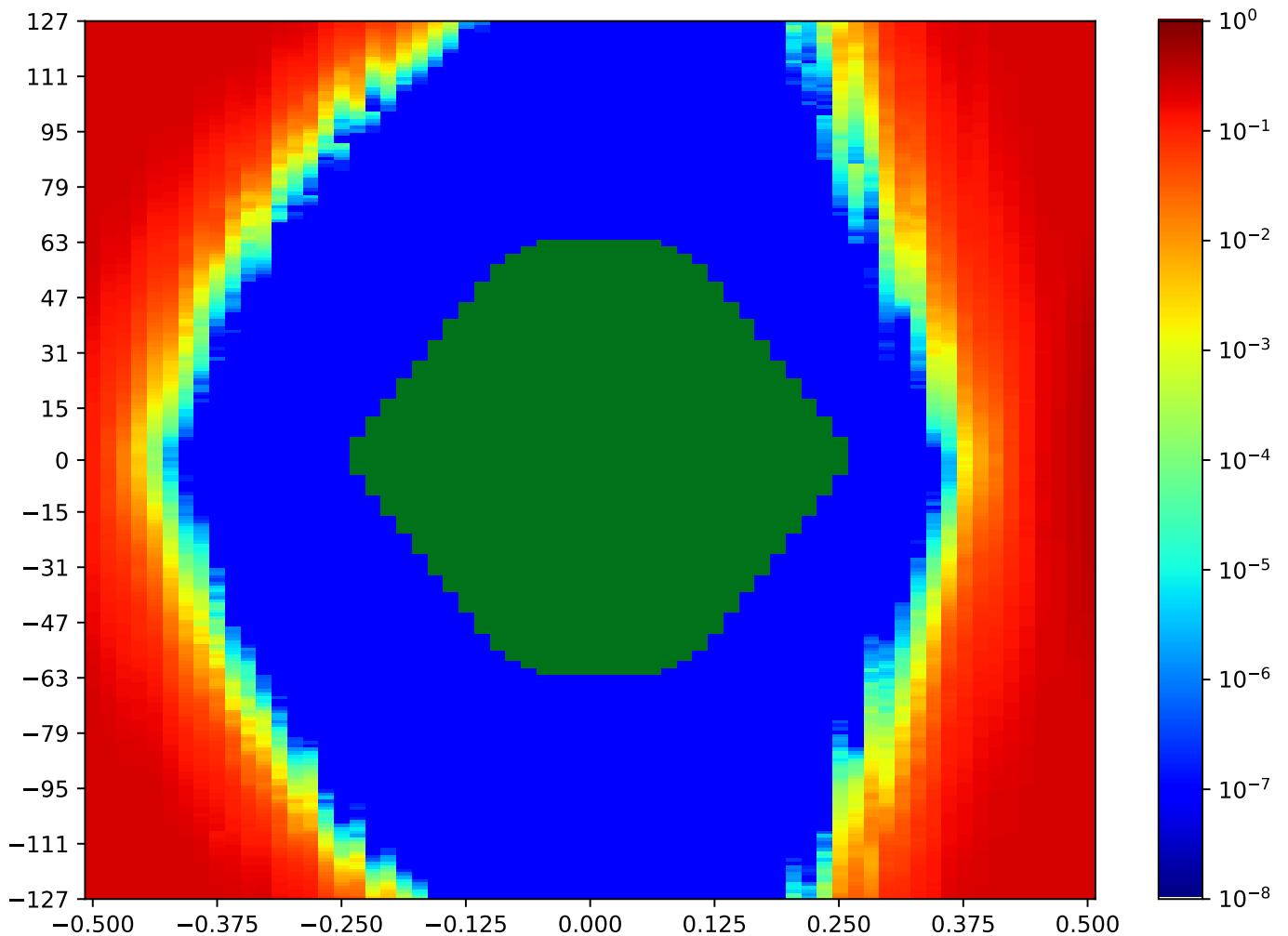


Figure 5.117: MSP_C_FPGA-IC39-18-IC15-18-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.20 MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

Table 5.109: MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:26:55		2018-Sep-27 17:27:16	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8853	48	73.85%	252	98.43%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

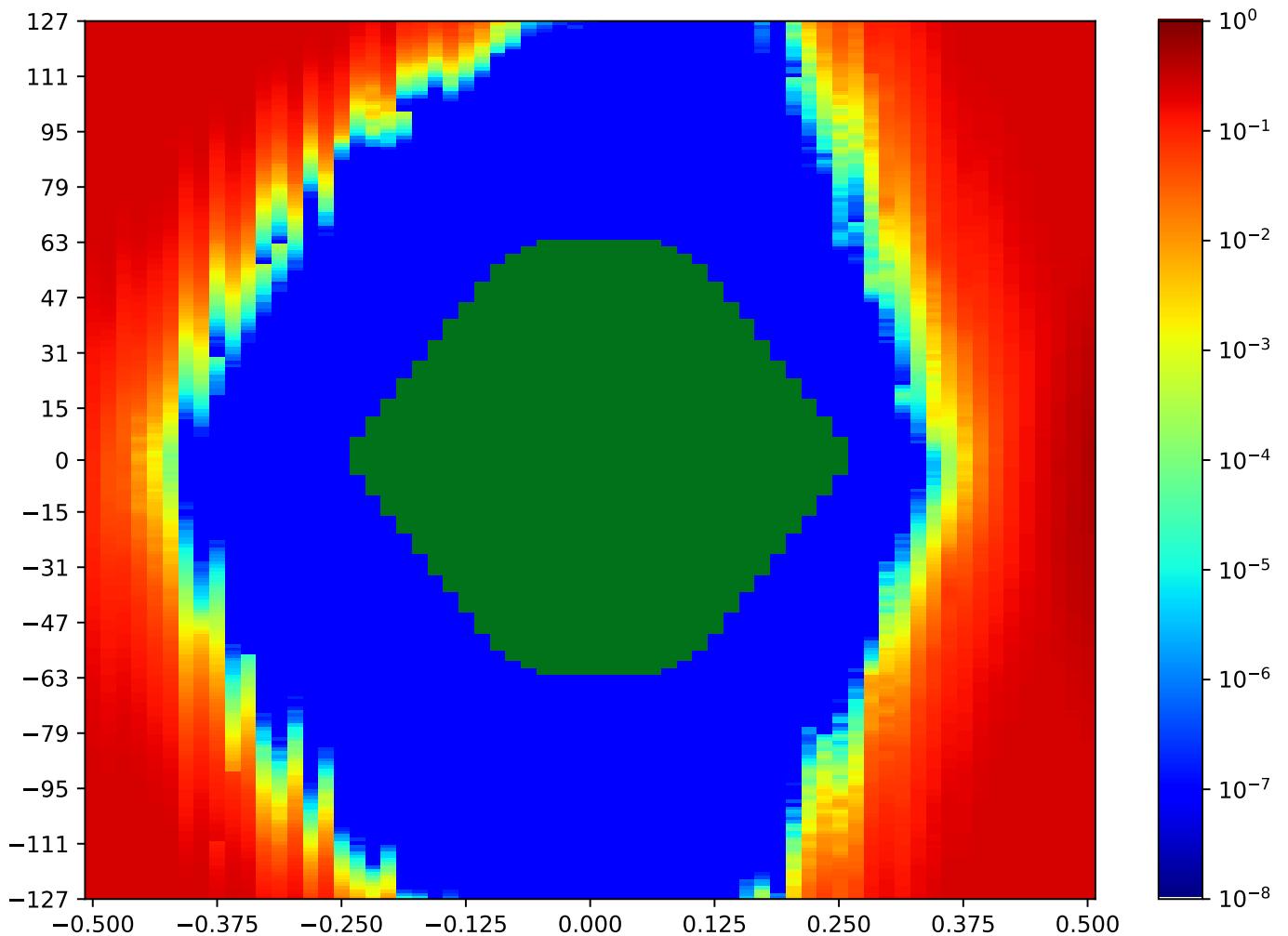


Figure 5.118: MSP_C_FPGA-IC39-19-IC15-19-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.21 MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

Table 5.110: MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:27:16		2018-Sep-27 17:27:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9158	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

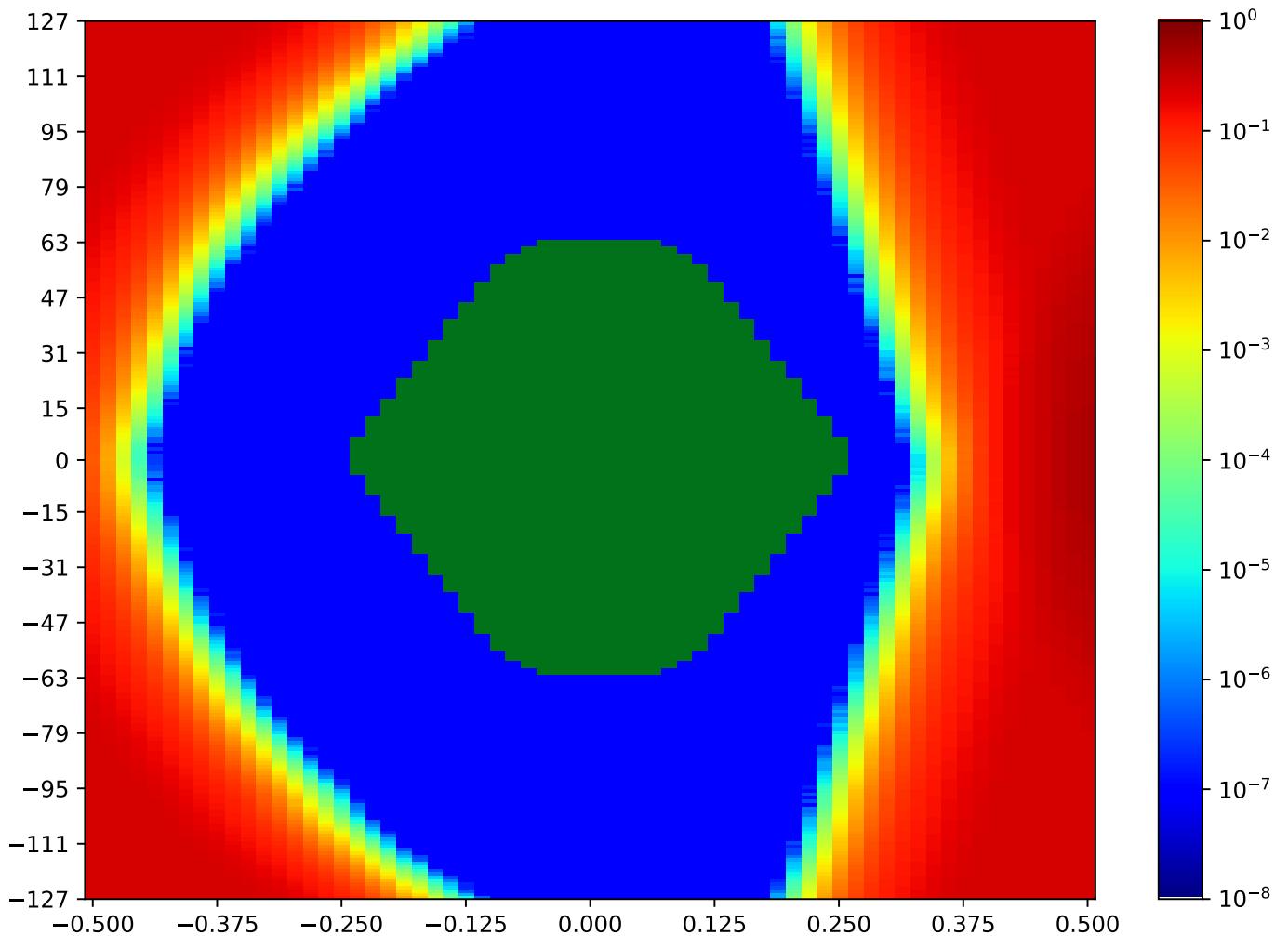


Figure 5.119: MSP_C_FPGA-IC39-20-IC15-20-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.22 MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

Table 5.111: MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:27:36		2018-Sep-27 17:27:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9076	48	73.85%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

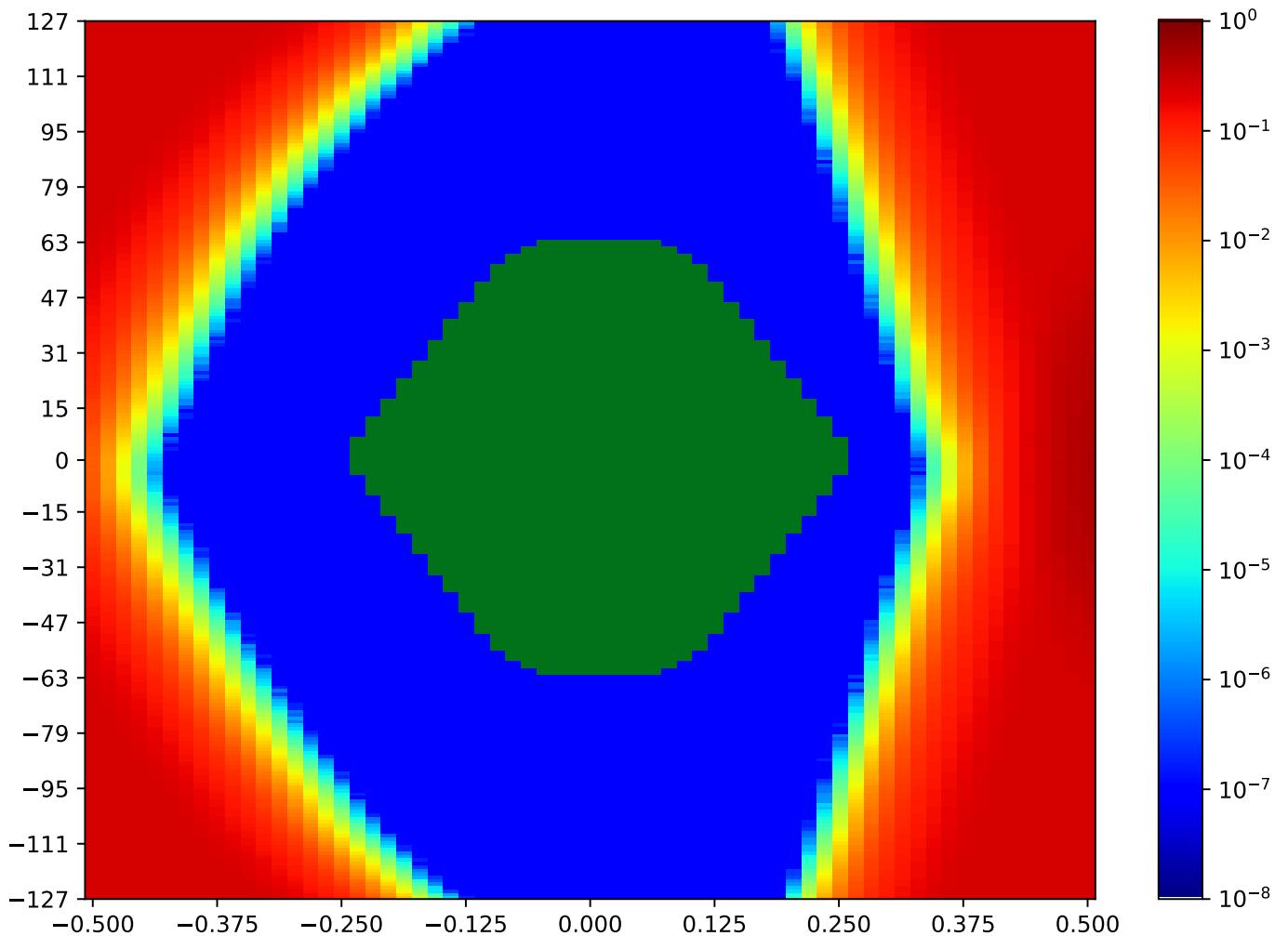


Figure 5.120: MSP_C_FPGA-IC39-21-IC15-21-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.23 MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

Table 5.112: MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:27:57		2018-Sep-27 17:28:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8855	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

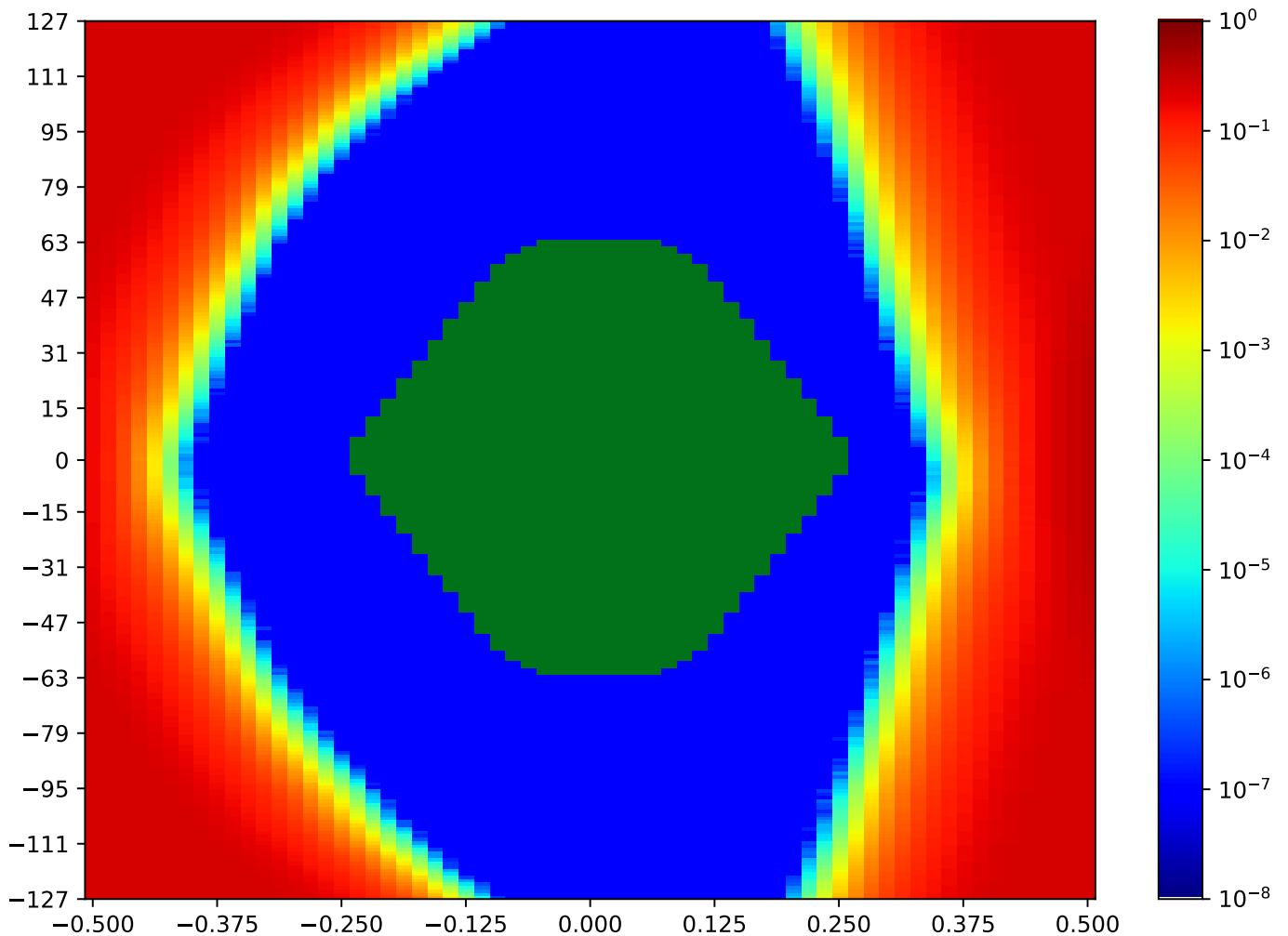


Figure 5.121: MSP_C_FPGA-IC39-22-IC15-22-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.24 MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

Table 5.113: MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:28:17		2018-Sep-27 17:28:37	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8634	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

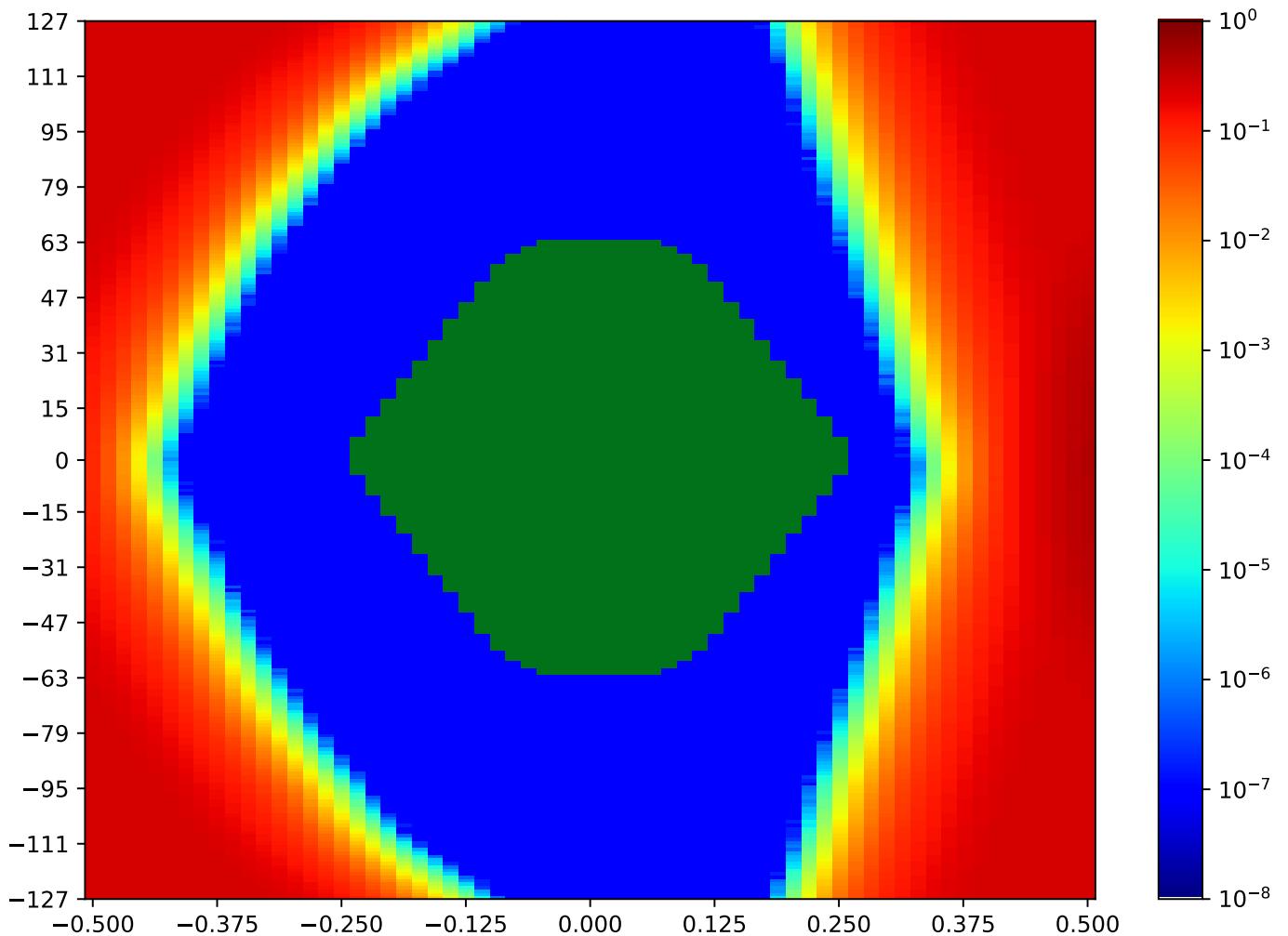


Figure 5.122: MSP_C_FPGA-IC39-23-IC15-23-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.25 MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

Table 5.114: MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:28:37		2018-Sep-27 17:28:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8699	48	73.85%	254	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

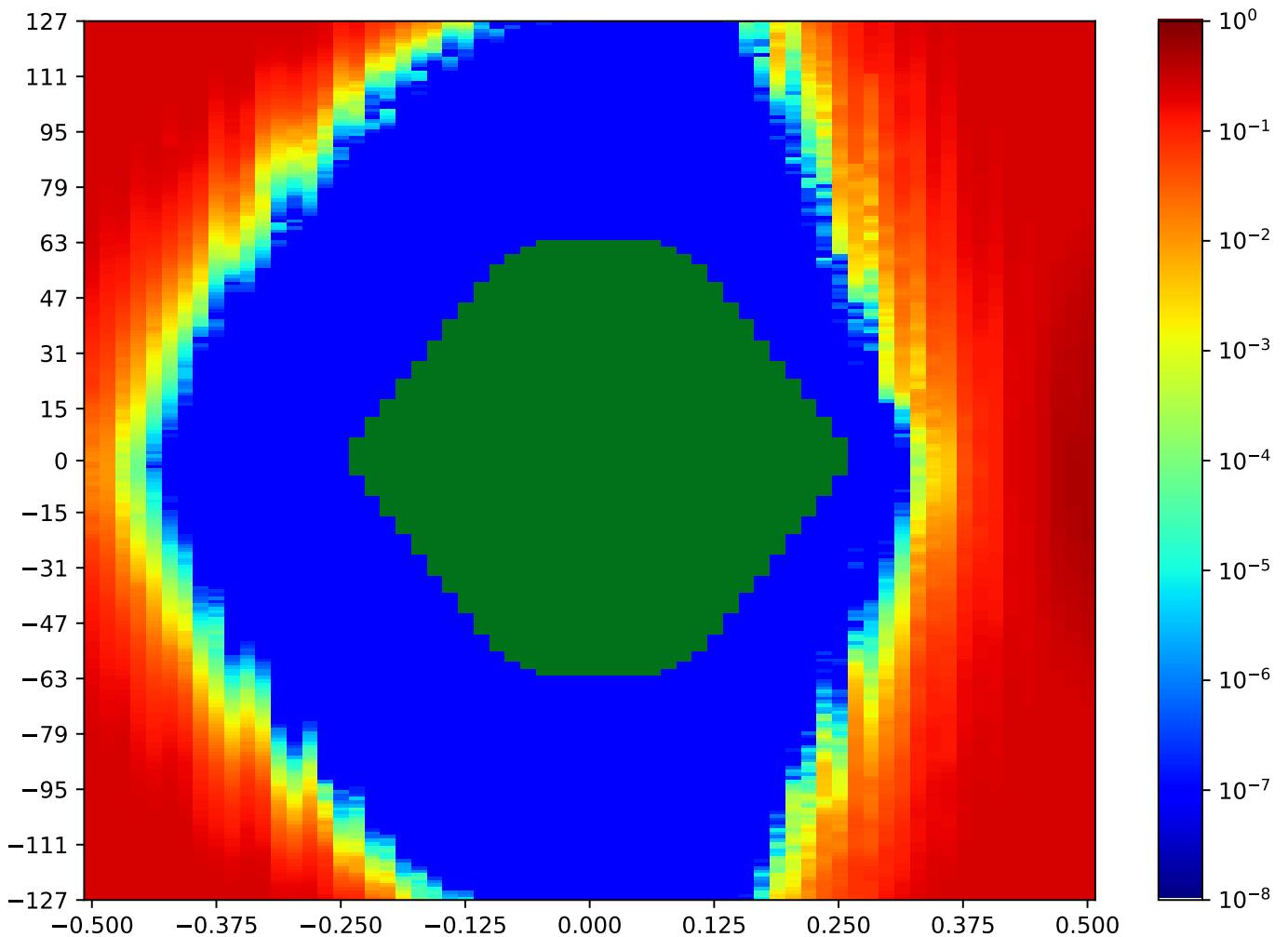


Figure 5.123: MSP_C_FPGA-IC39-24-IC15-24-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.26 MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

Table 5.115: MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:28:58		2018-Sep-27 17:29:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8557	45	69.23%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

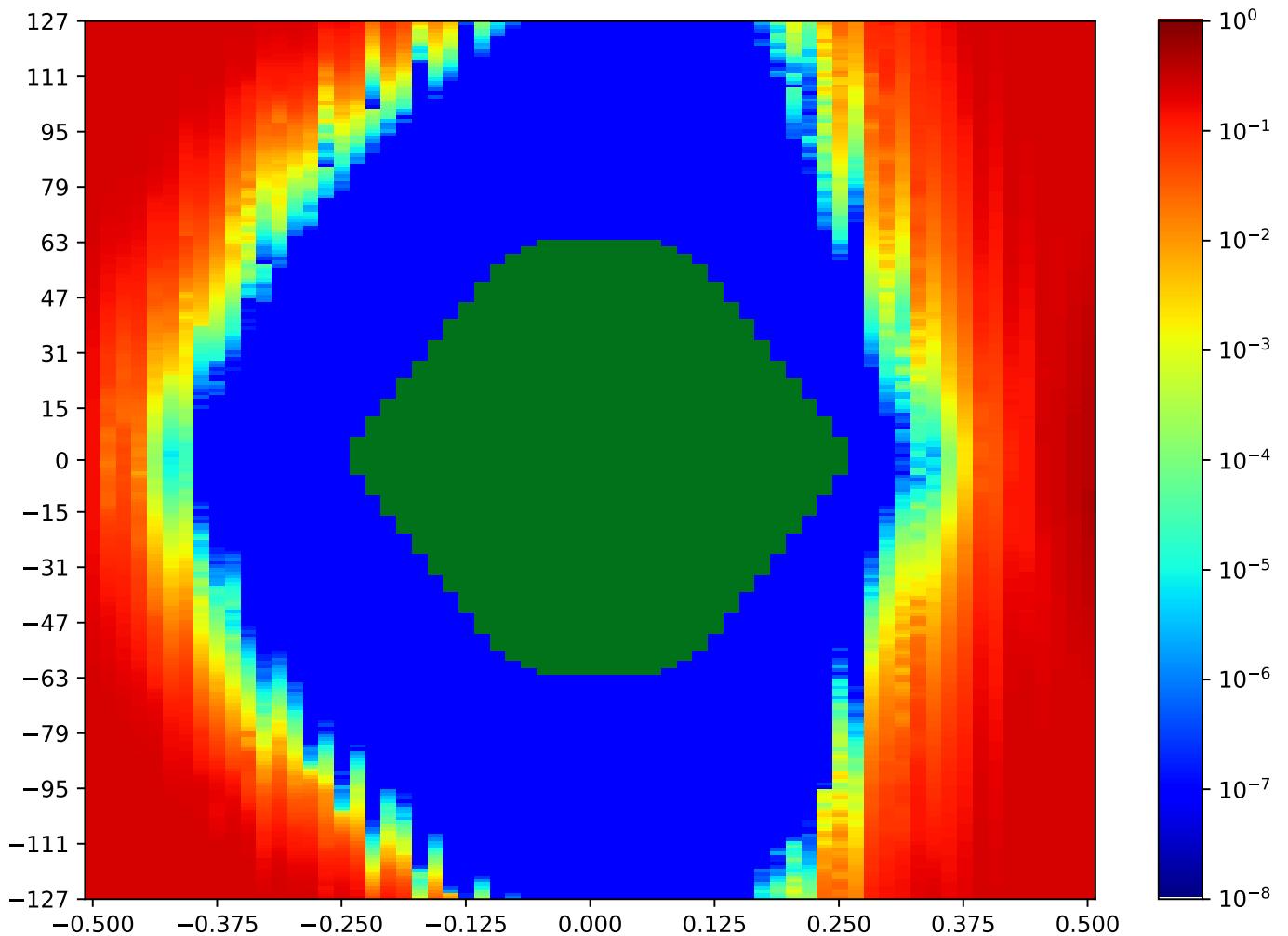


Figure 5.124: MSP_C_FPGA-IC39-25-IC15-25-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.27 MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

Table 5.116: MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:29:18		2018-Sep-27 17:29:38	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8924	47	72.31%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

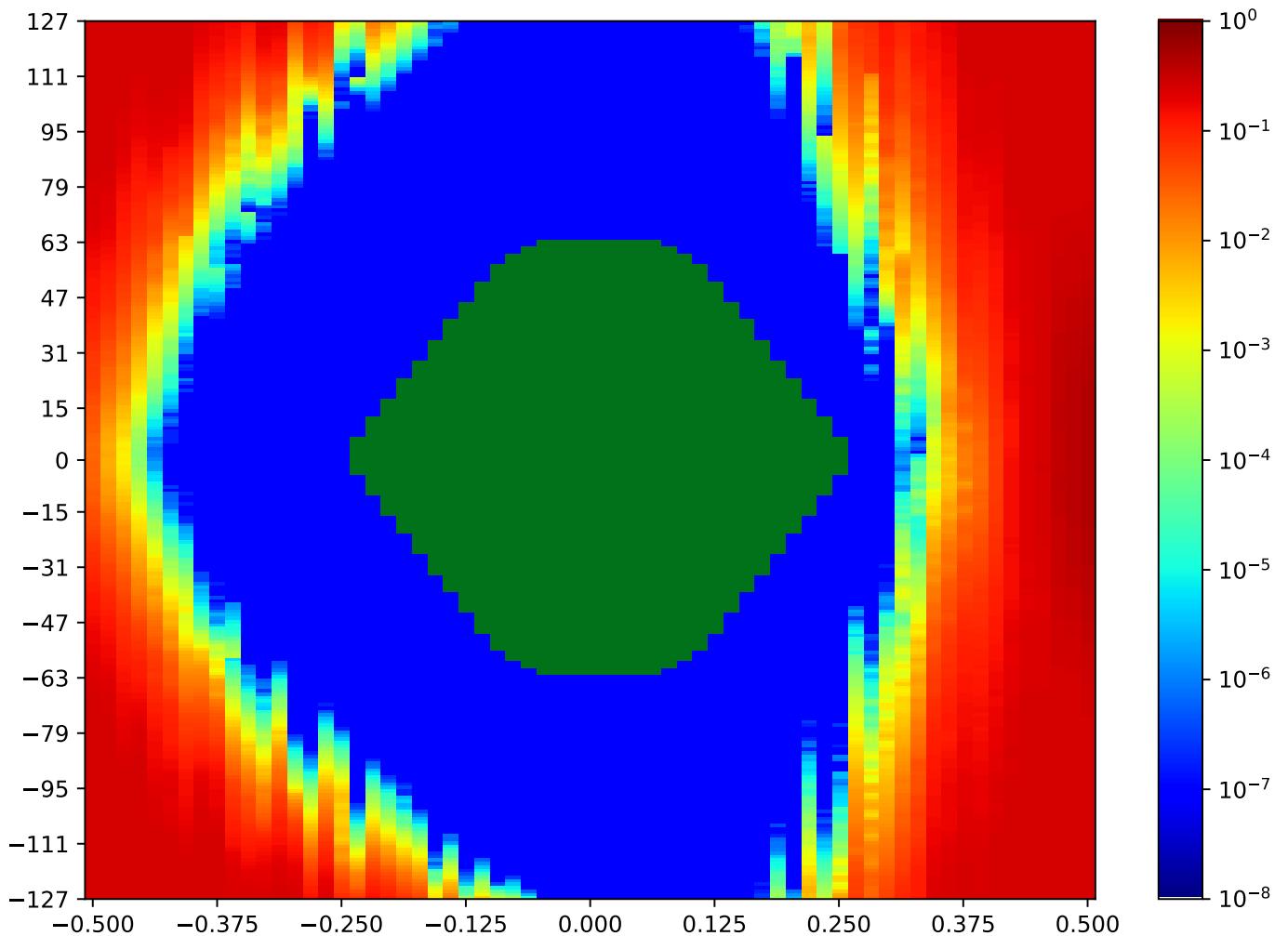


Figure 5.125: MSP_C_FPGA-IC39-26-IC15-26-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.9.28 MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

Table 5.117: MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale GTY	2018-Sep-27 17:29:38		2018-Sep-27 17:29:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8770	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x4002 SVN: 0	

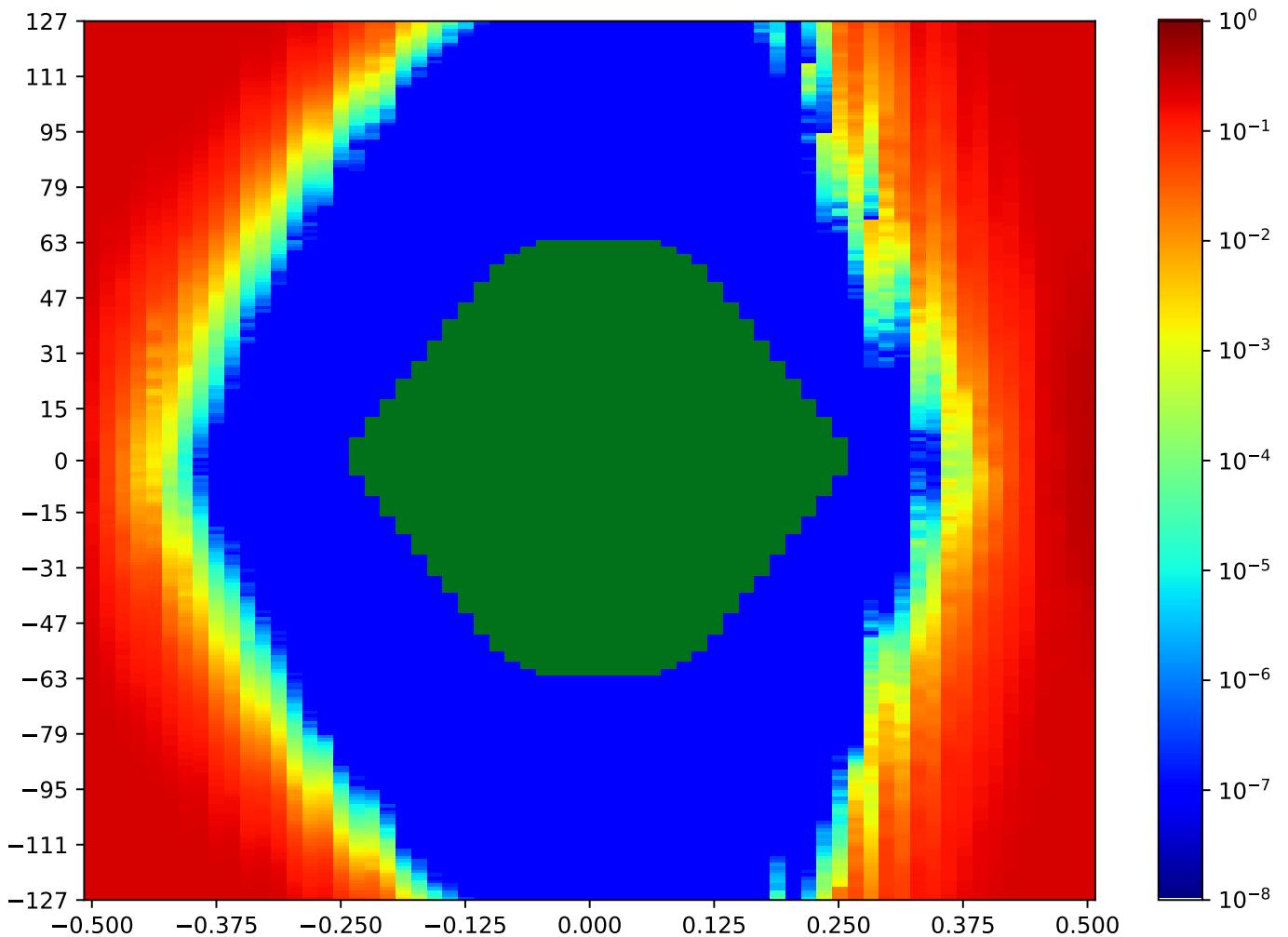


Figure 5.126: MSP_C_FPGA-IC39-27-IC15-27-TRP_FPGA

Call back to summary Figure 5.98. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.10 MSP_A TX1 MSP_C RX17 Minipod Loopback

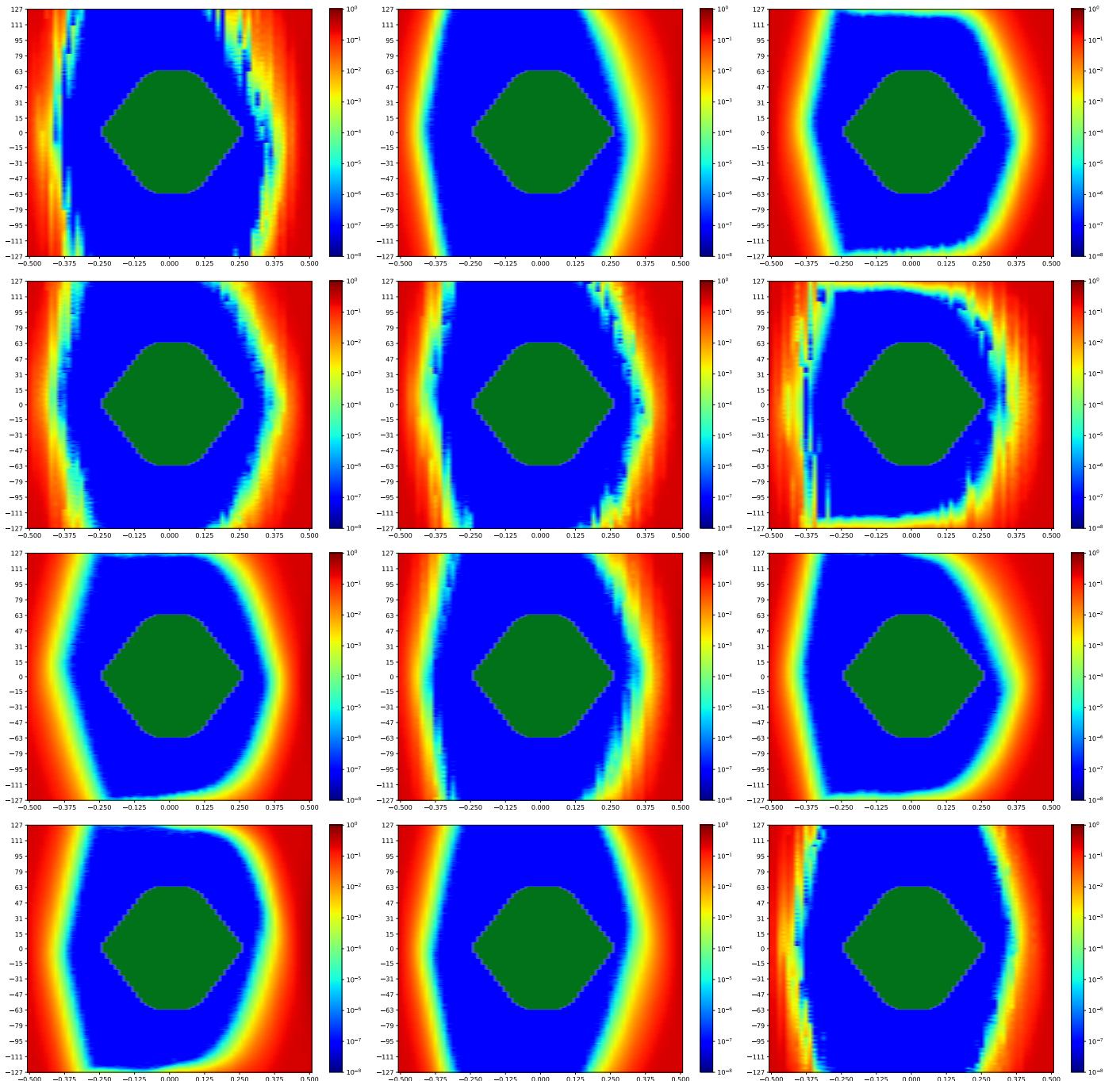


Figure 5.127: MSP_A TX1 MSP_C RX17 Minipod Loopback

A cross-reference to Figure 5.127. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.140.

5.10.1 MSP_A_FPGA-TX1-00-RX17-00-MSP_C_FPGA

Table 5.118: MSP_A_FPGA-TX1-00-RX17-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:12:42		2018-Sep-27 16:13:02	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9954	45		69.23%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

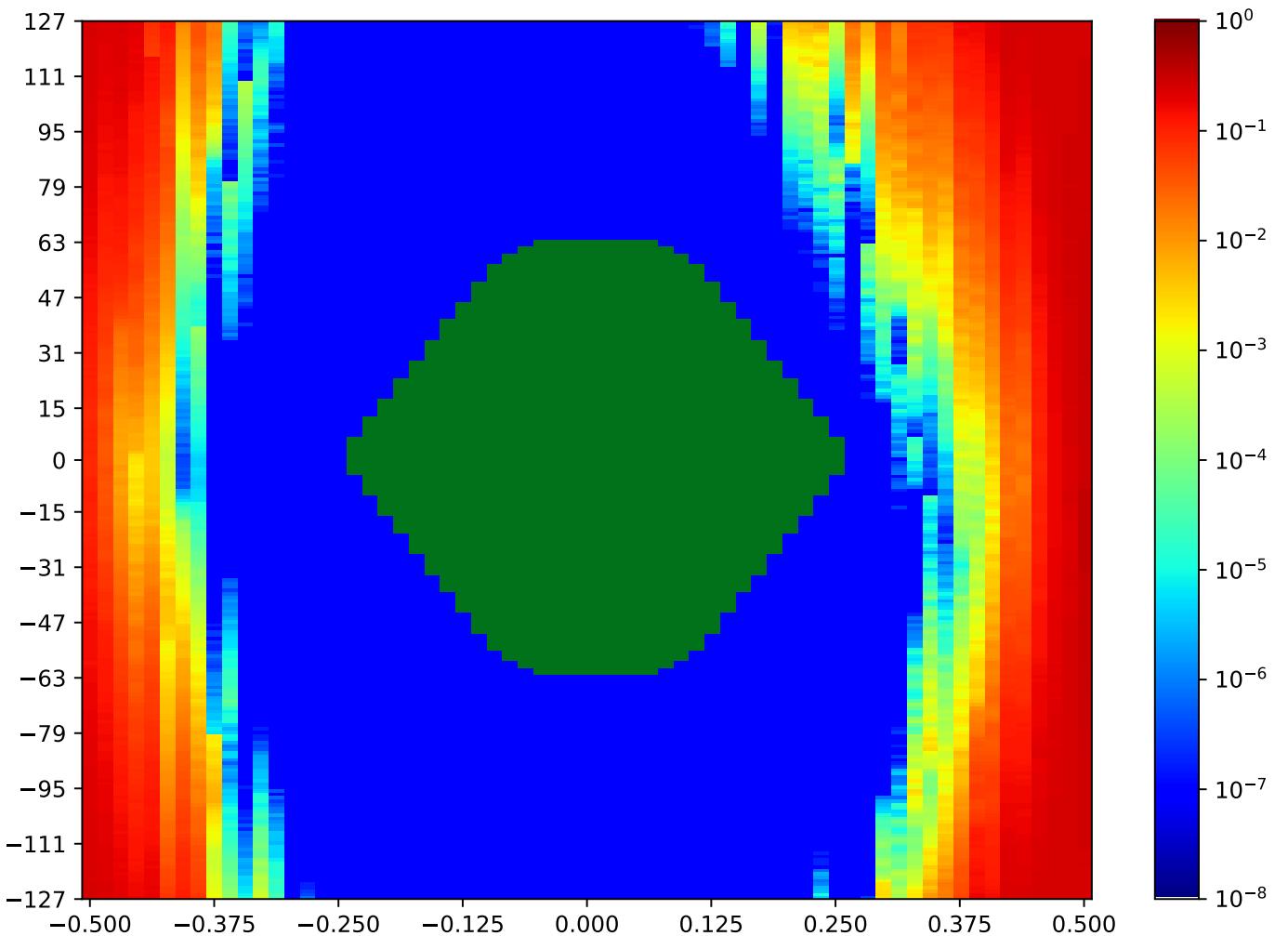


Figure 5.128: MSP_A_FPGA-TX1-00-RX17-00-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.2 MSP_A_FPGA-TX1-01-RX17-01-MSP_C_FPGA

Table 5.119: MSP_A_FPGA-TX1-01-RX17-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:13:23		2018-Sep-27 16:13:44	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9345	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

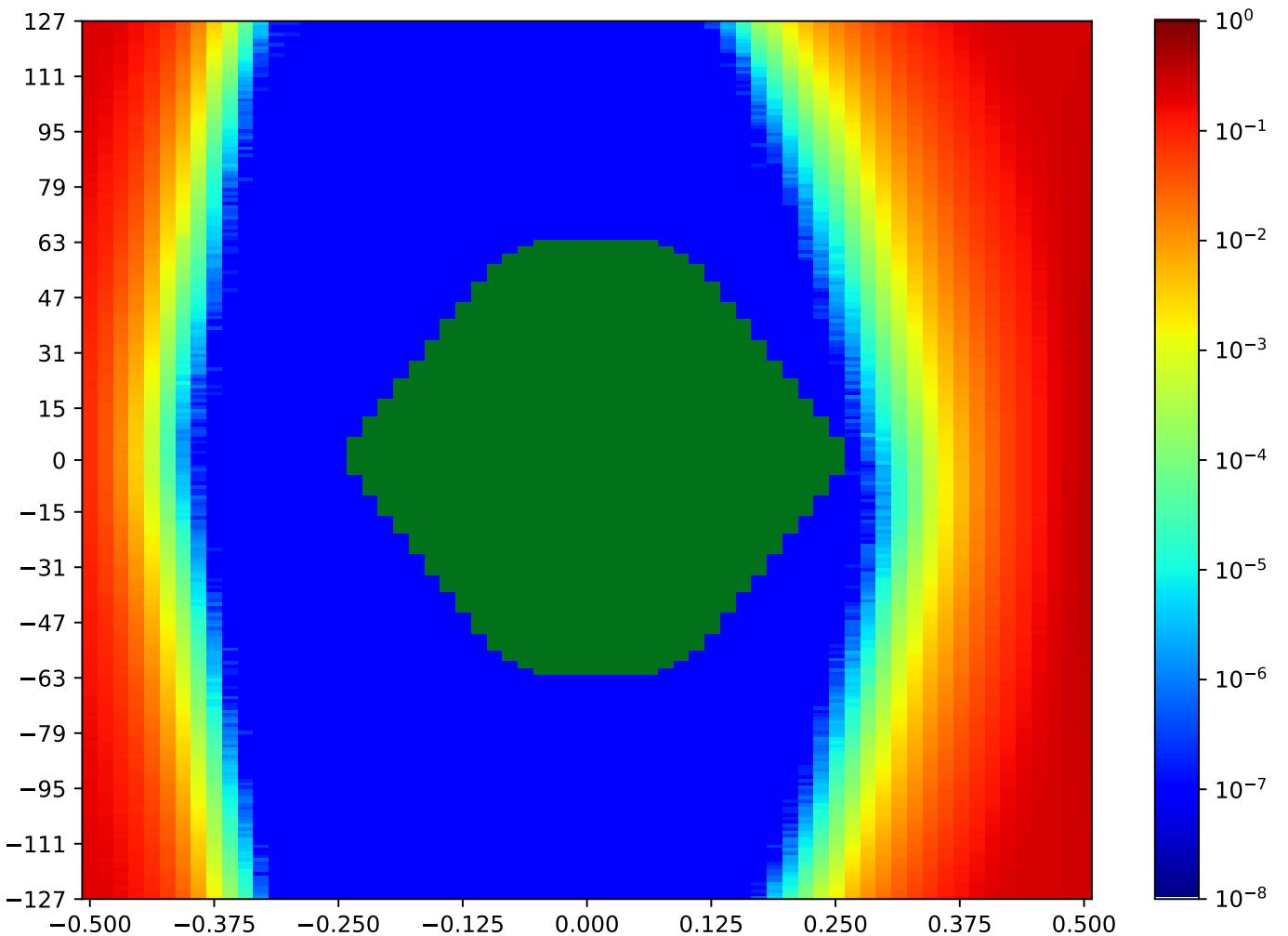


Figure 5.129: MSP_A_FPGA-TX1-01-RX17-01-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.3 MSP_A_FPGA-TX1-02-RX17-02-MSP_C_FPGA

Table 5.120: MSP_A_FPGA-TX1-02-RX17-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:13:44		2018-Sep-27 16:14:04	
Reset RX	OA	HO		VO	VO (%)
true	8325	43		66.15%	236 92.16%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

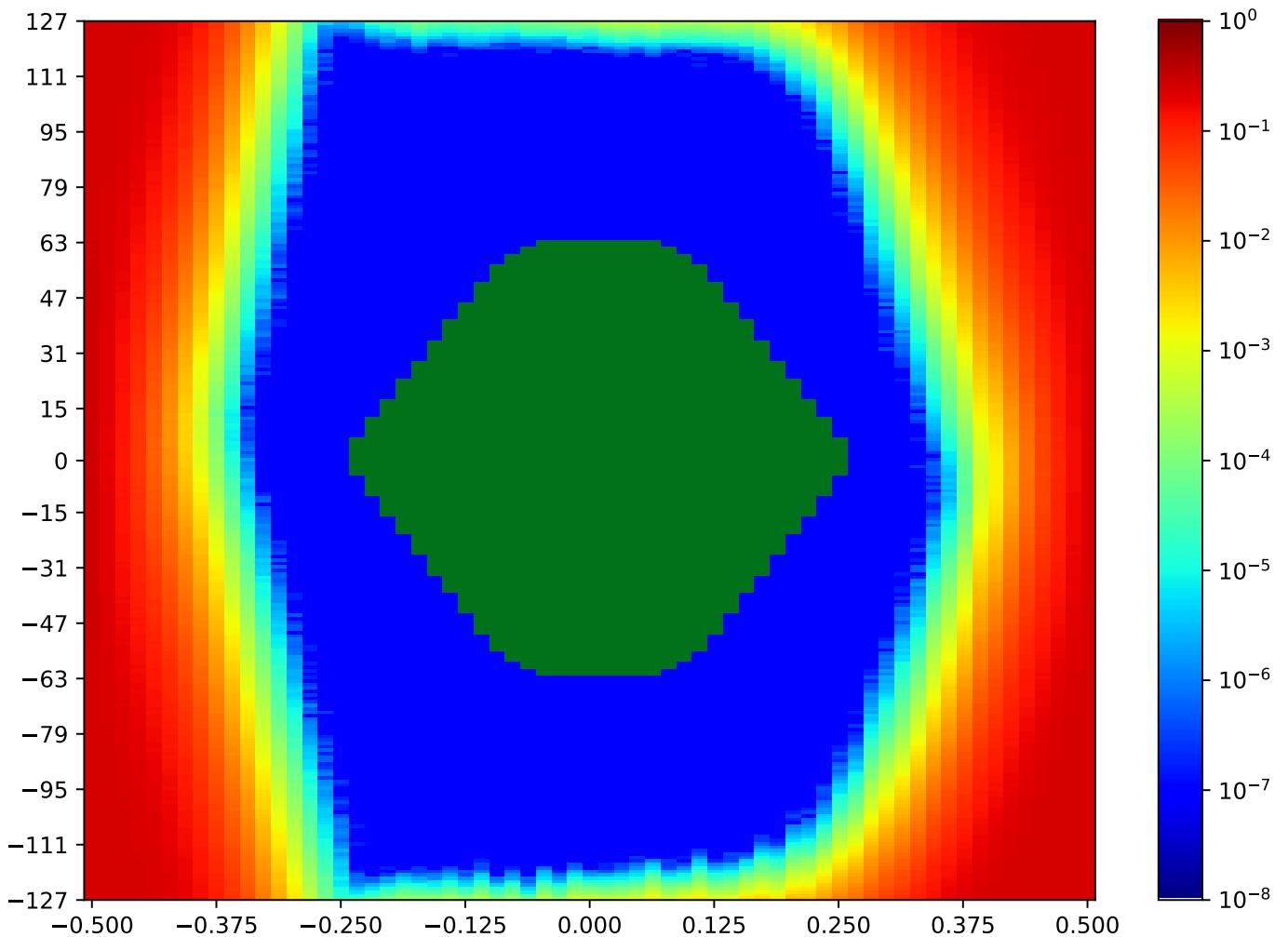


Figure 5.130: MSP_A_FPGA-TX1-02-RX17-02-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.4 MSP_A_FPGA-TX1-03-RX17-03-MSP_C_FPGA

Table 5.121: MSP_A_FPGA-TX1-03-RX17-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:12:02		2018-Sep-27 16:12:22	
Reset RX	OA	HO		VO	VO (%)
true	9204	45		69.23%	255 99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

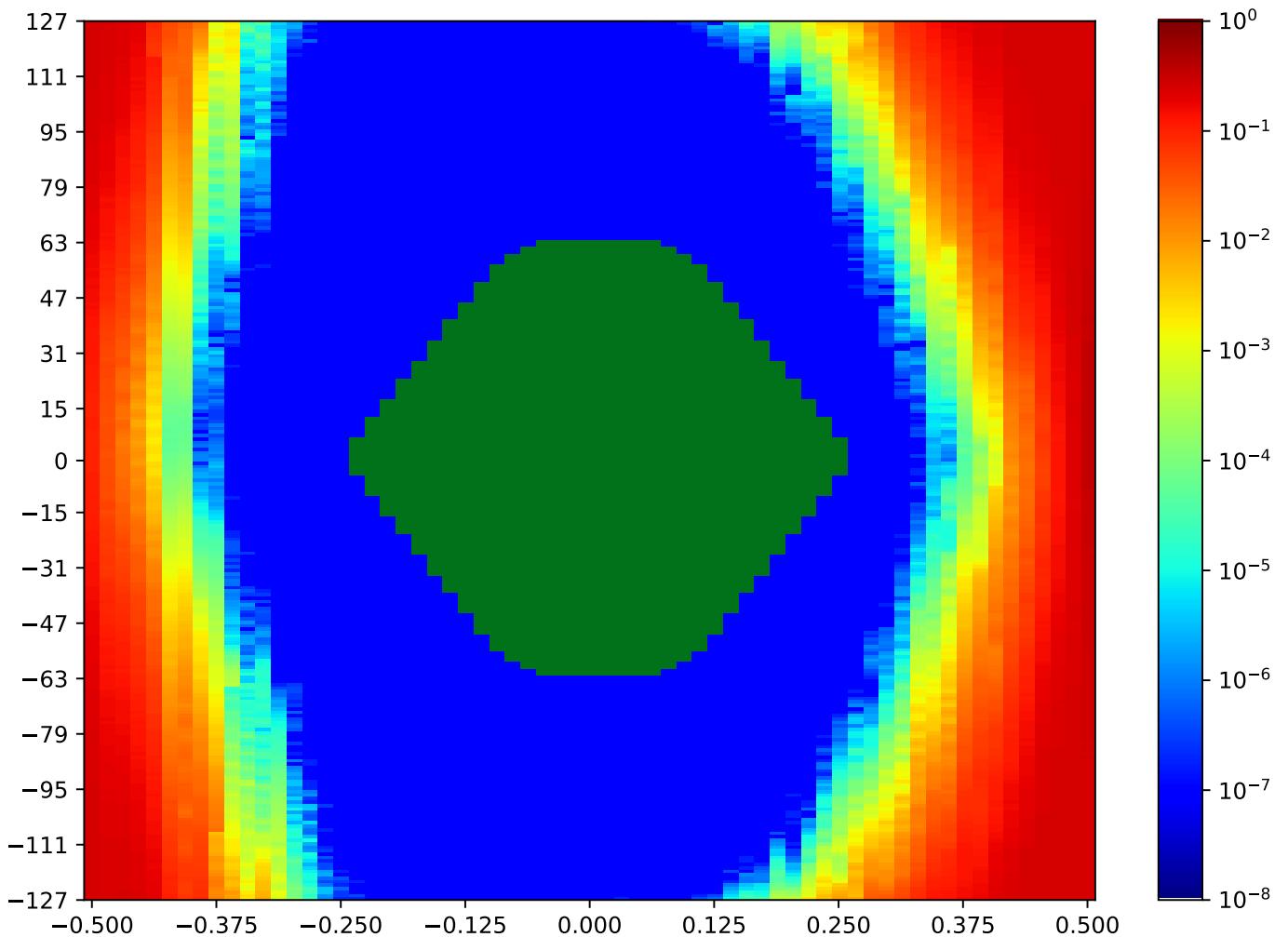


Figure 5.131: MSP_A_FPGA-TX1-03-RX17-03-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.5 MSP_A_FPGA-TX1-04-RX17-04-MSP_C_FPGA

Table 5.122: MSP_A_FPGA-TX1-04-RX17-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:14:45		2018-Sep-27 16:15:05	
Reset RX	OA	HO		VO	VO (%)
true	9245	44		67.69%	254 99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

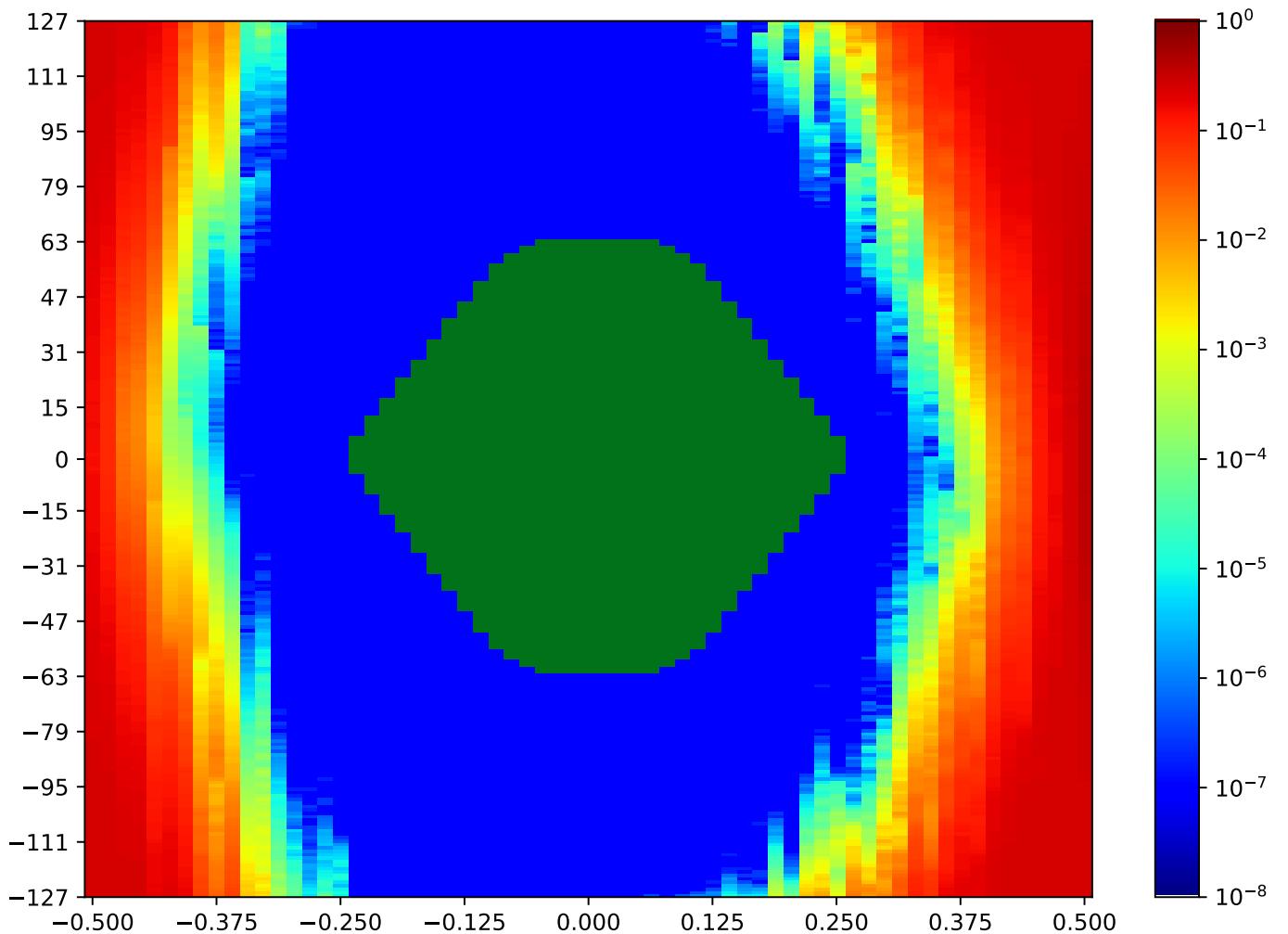


Figure 5.132: MSP_A_FPGA-TX1-04-RX17-04-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.6 MSP_A_FPGA-TX1-05-RX17-05-MSP_C_FPGA

Table 5.123: MSP_A_FPGA-TX1-05-RX17-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:11:42		2018-Sep-27 16:12:02	
Reset RX	OA	HO		VO	VO (%)
true	7778	42		63.08%	221 86.67%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

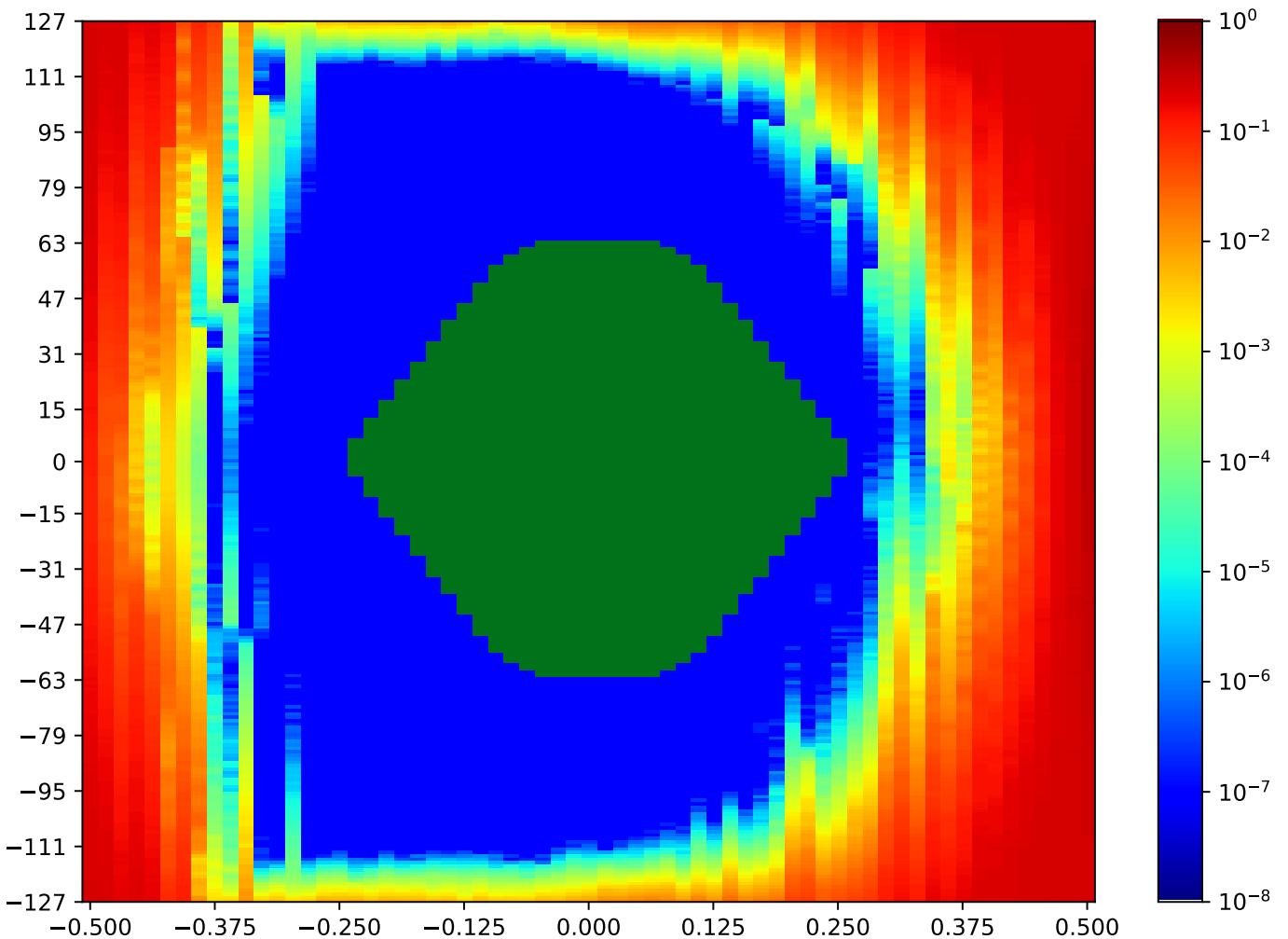


Figure 5.133: MSP_A_FPGA-TX1-05-RX17-05-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.7 MSP_A_FPGA-TX1-06-RX17-06-MSP_C_FPGA

Table 5.124: MSP_A_FPGA-TX1-06-RX17-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:15:26		2018-Sep-27 16:15:53	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8250	43	66.15%	239	93.33%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

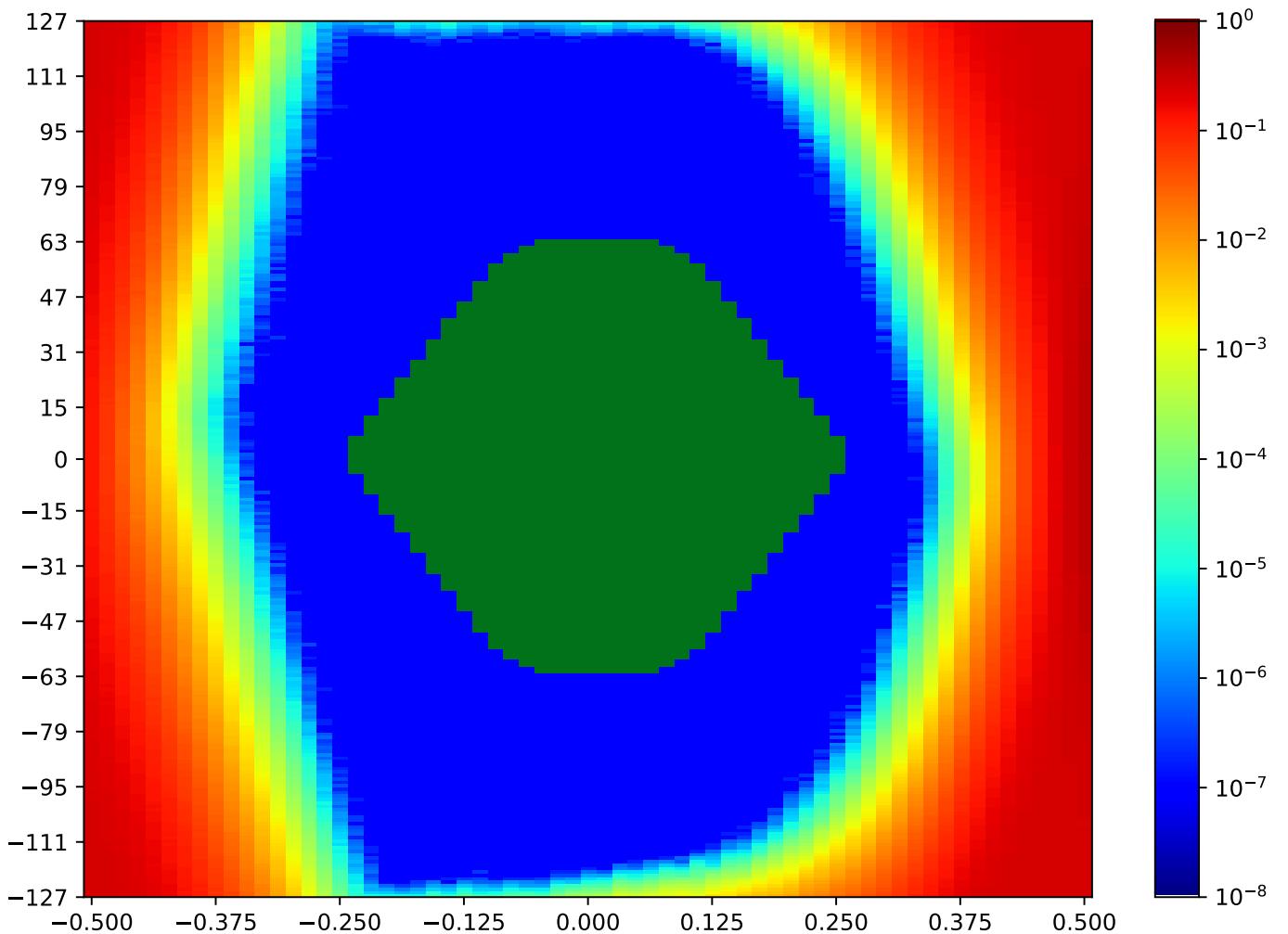


Figure 5.134: MSP_A_FPGA-TX1-06-RX17-06-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.8 MSP_A_FPGA-TX1-07-RX17-07-MSP_C_FPGA

Table 5.125: MSP_A_FPGA-TX1-07-RX17-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:12:22		2018-Sep-27 16:12:42	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9363	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

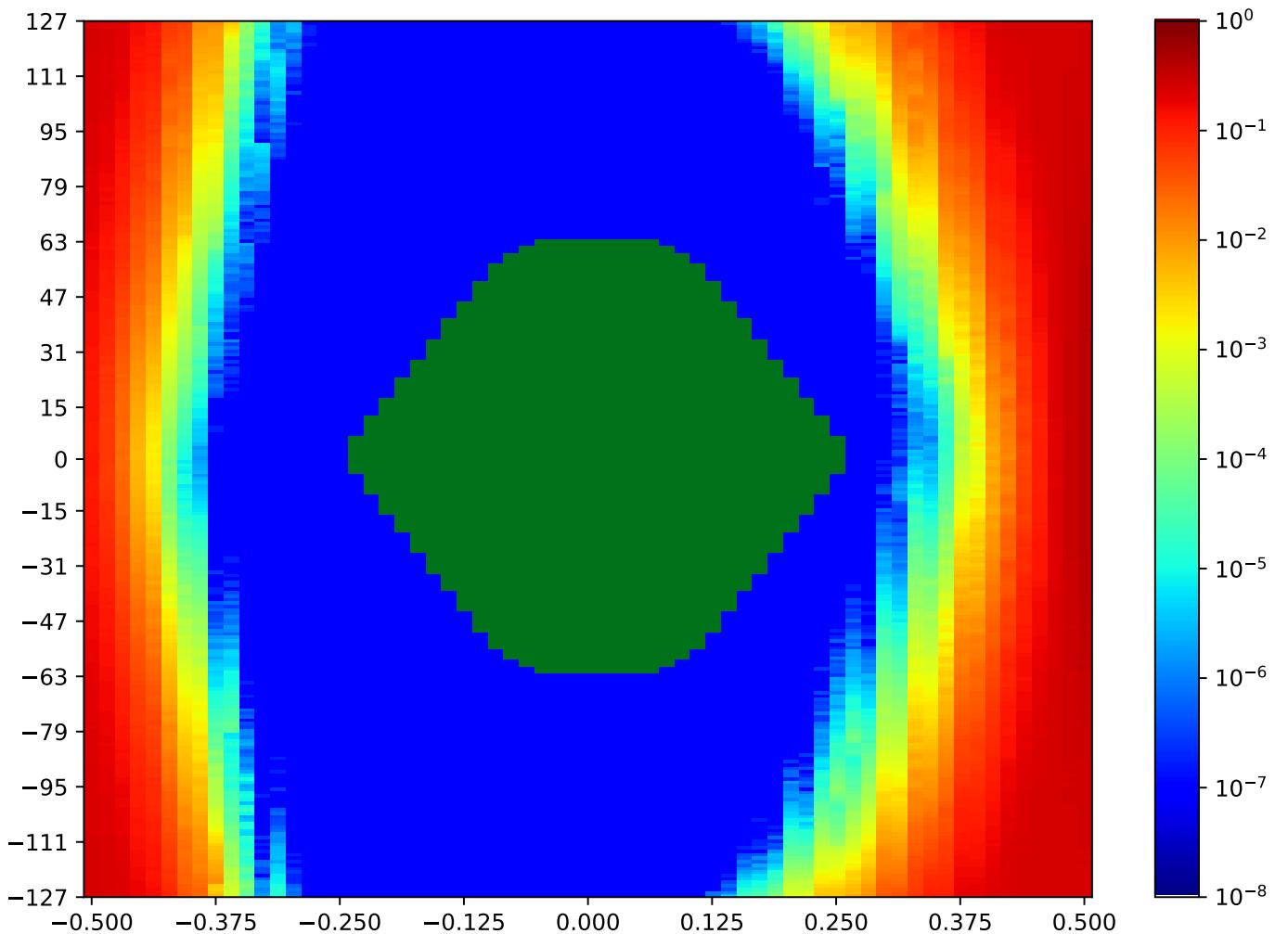


Figure 5.135: MSP_A_FPGA-TX1-07-RX17-07-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.9 MSP_A_FPGA-TX1-08-RX17-08-MSP_C_FPGA

Table 5.126: MSP_A_FPGA-TX1-08-RX17-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:15:05		2018-Sep-27 16:15:26	
Reset RX	OA	HO		VO	VO (%)
true	8329	42		237	92.16%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

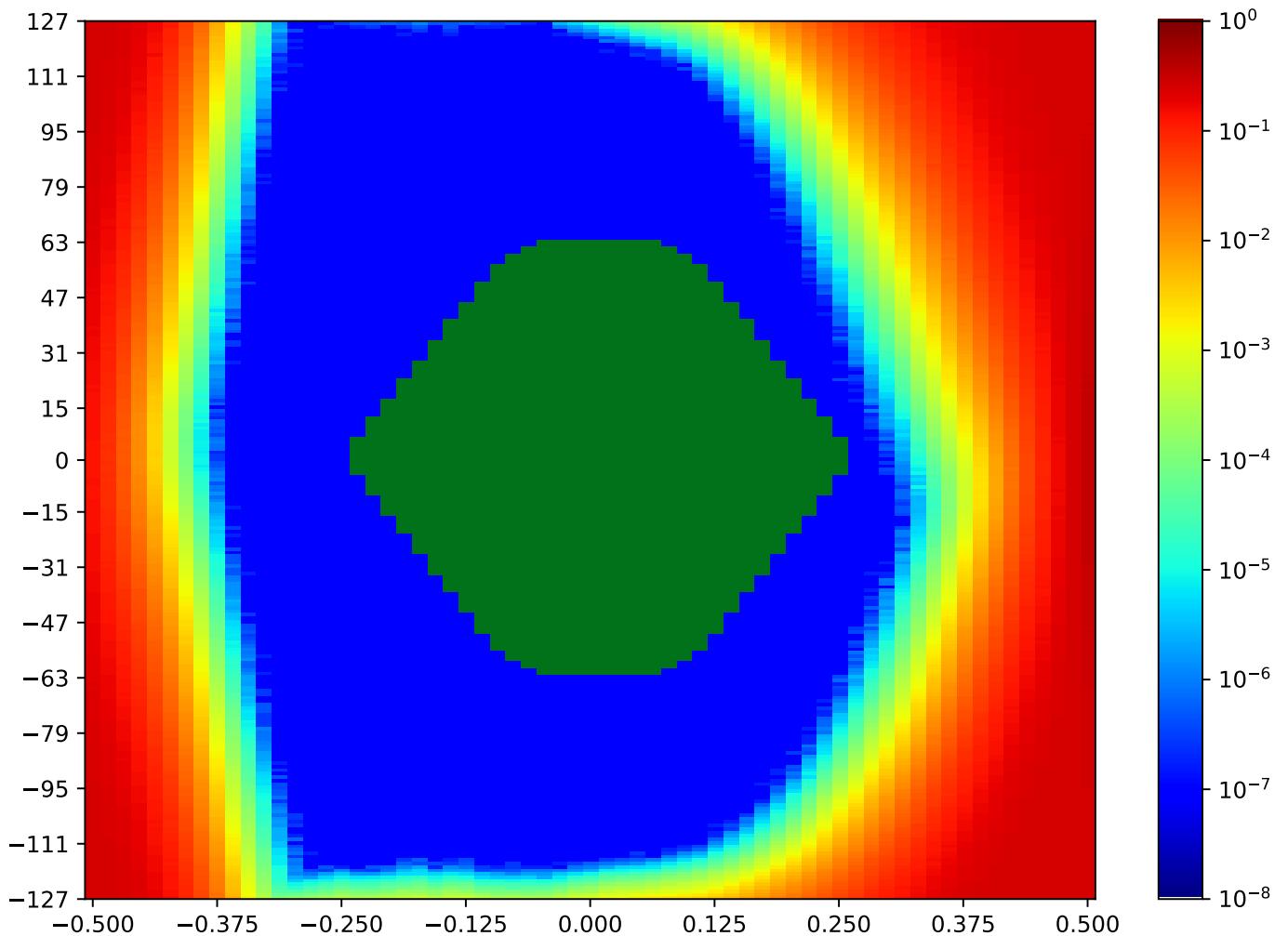


Figure 5.136: MSP_A_FPGA-TX1-08-RX17-08-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.10 MSP_A_FPGA-TX1-09-RX17-09-MSP_C_FPGA

Table 5.127: MSP_A_FPGA-TX1-09-RX17-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:13:03		2018-Sep-27 16:13:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8261	41	63.08%	234	90.98%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

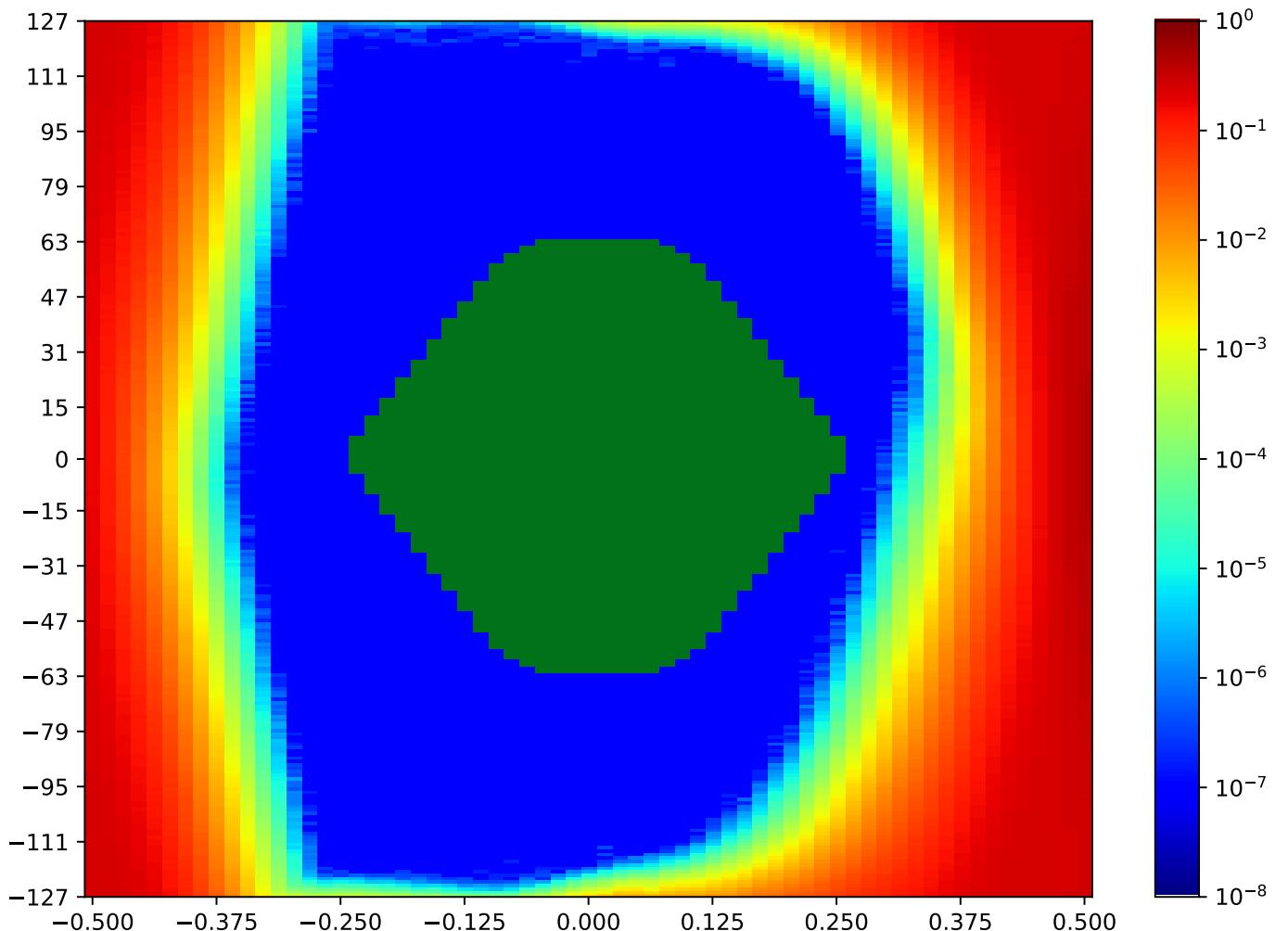


Figure 5.137: MSP_A_FPGA-TX1-09-RX17-09-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.11 MSP_A_FPGA-TX1-10-RX17-10-MSP_C_FPGA

Table 5.128: MSP_A_FPGA-TX1-10-RX17-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:14:24		2018-Sep-27 16:14:45	
Reset RX	OA	HO		VO	VO (%)
true	9219	41		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

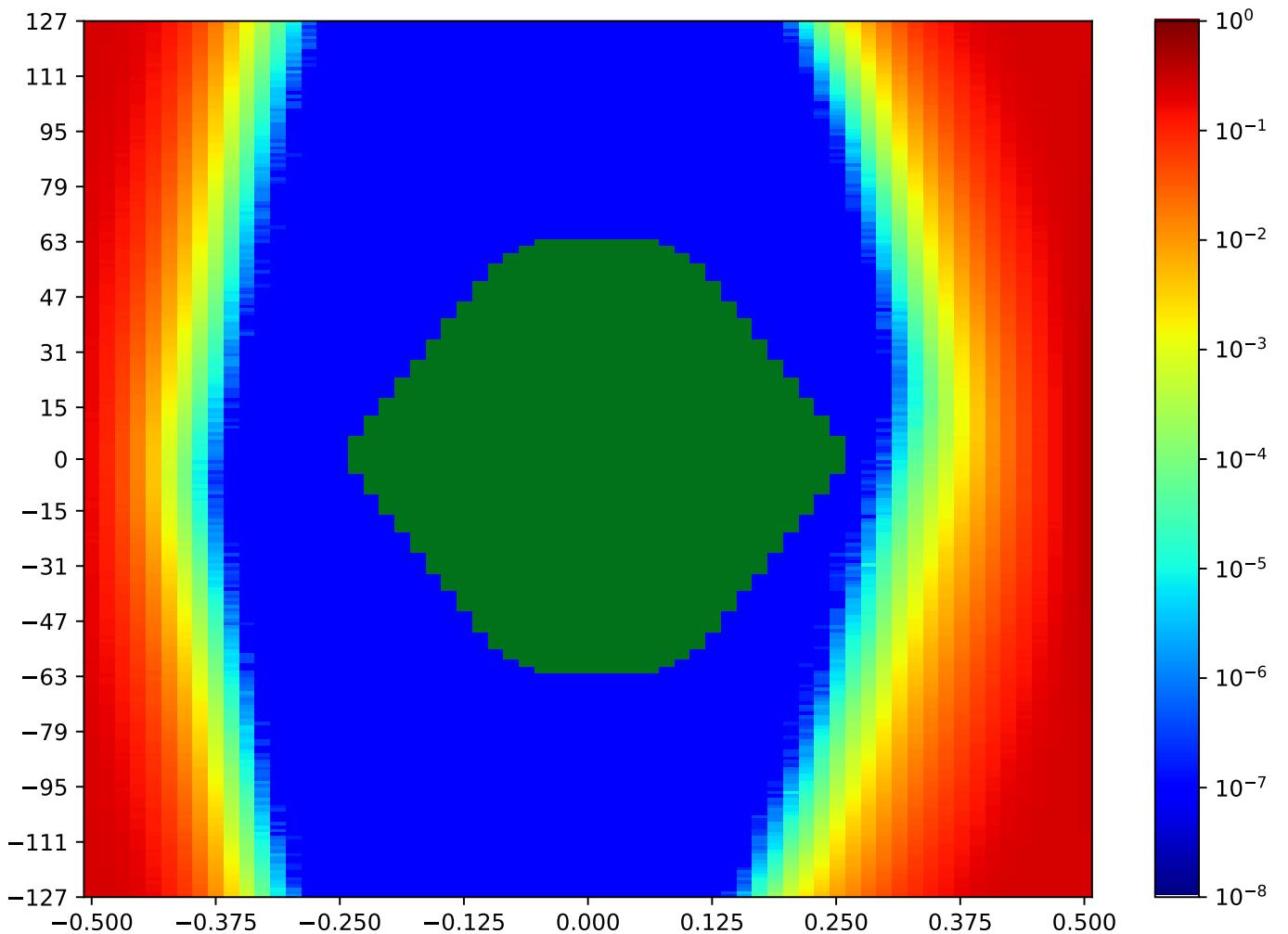


Figure 5.138: MSP_A_FPGA-TX1-10-RX17-10-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.10.12 MSP_A_FPGA-TX1-11-RX17-11-MSP_C_FPGA

Table 5.129: MSP_A_FPGA-TX1-11-RX17-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:14:04		2018-Sep-27 16:14:24	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	10245	45		69.23%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

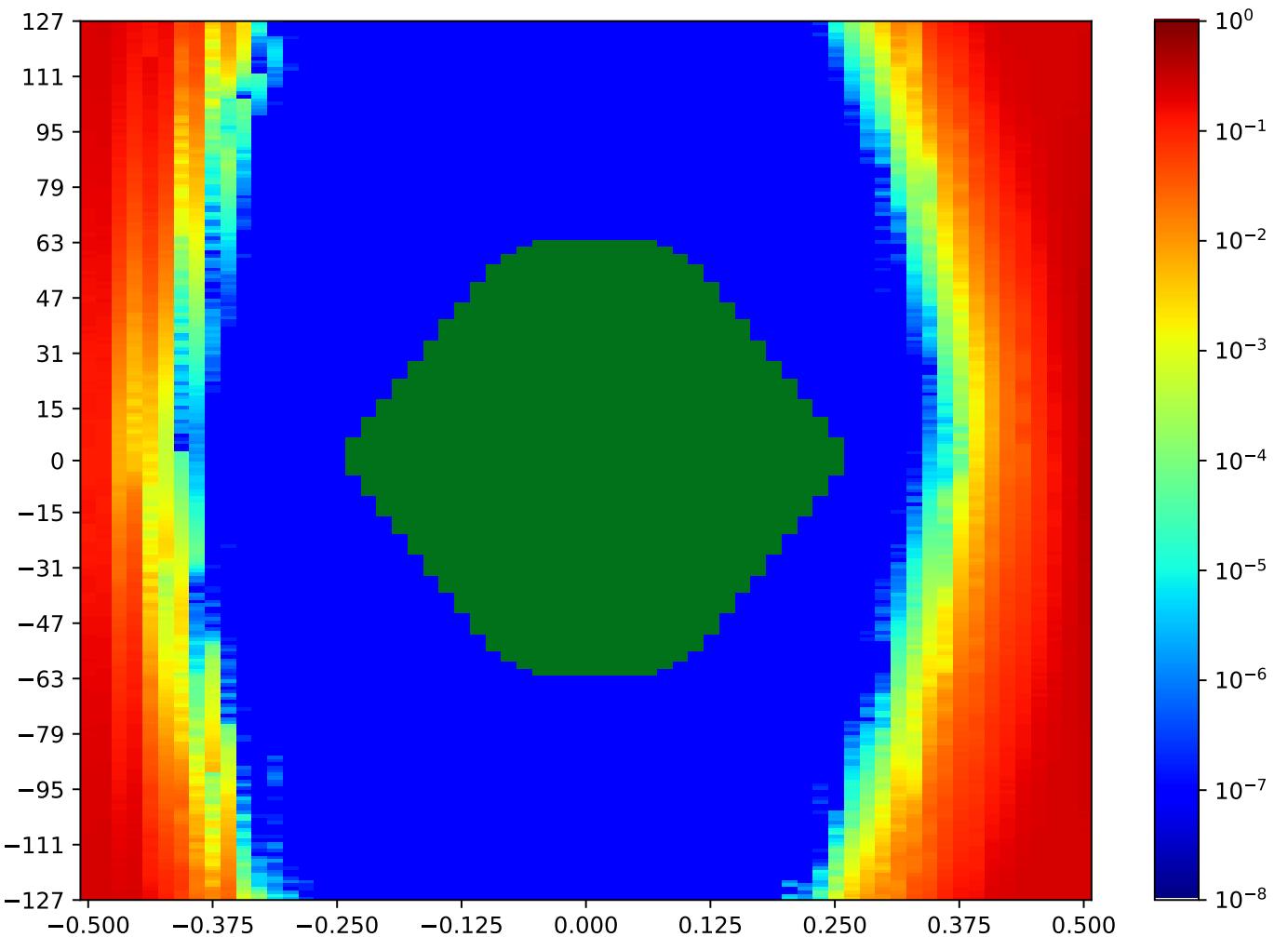


Figure 5.139: MSP_A_FPGA-TX1-11-RX17-11-MSP_C_FPGA

Call back to summary Figure 5.127. Sibling eye diagrams: V2-6.4.

5.11 MSP_A TX2 MSP_C RX18 Minipod Loopback

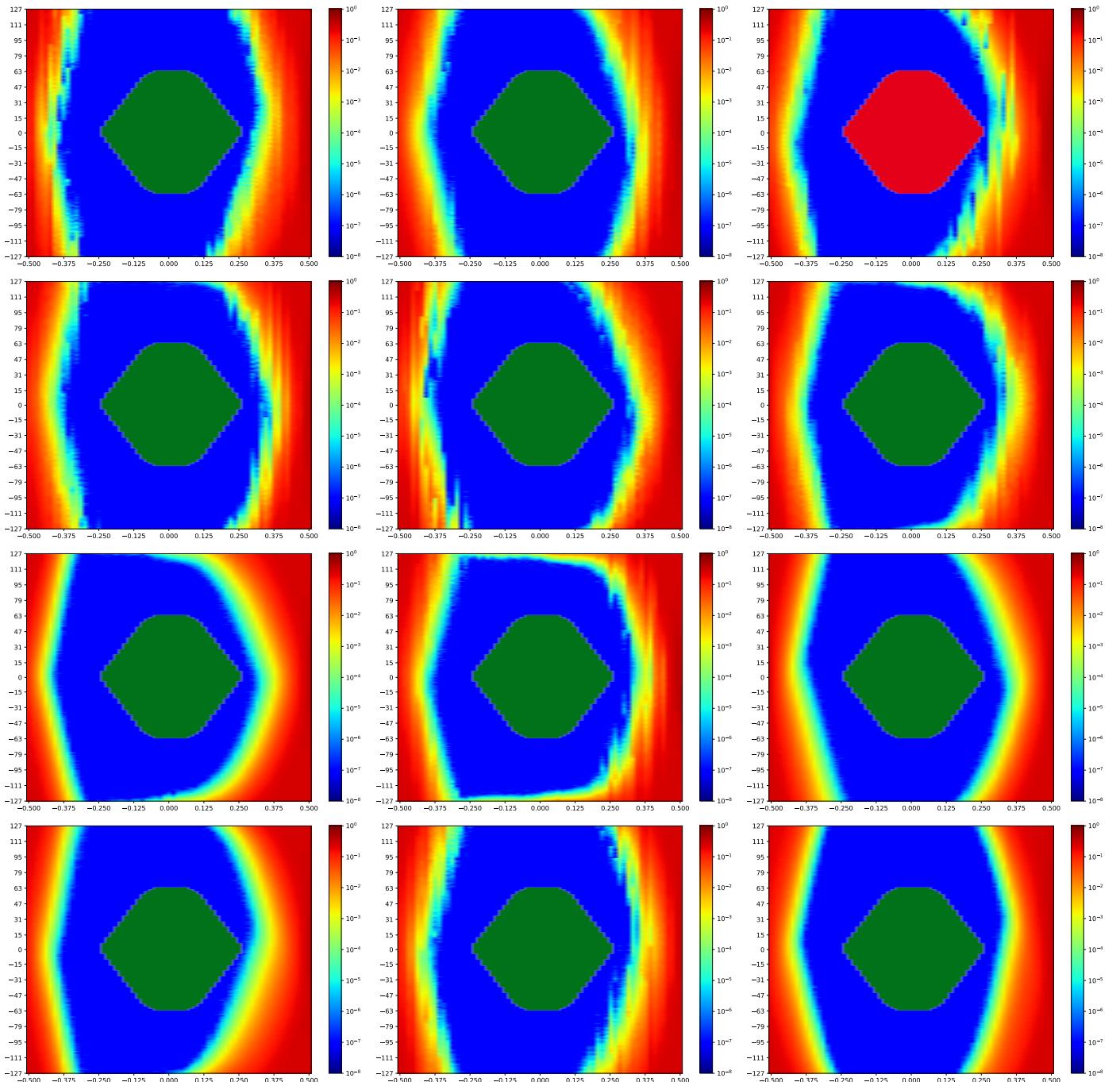


Figure 5.140: MSP_A TX2 MSP_C RX18 Minipod Loopback

A cross-reference to Figure 5.140. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.153.

5.11.1 MSP_A_FPGA-TX2-00-RX18-00-MSP_C_FPGA

Table 5.130: MSP_A_FPGA-TX2-00-RX18-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:16:55		2018-Sep-27 16:17:16	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9366	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

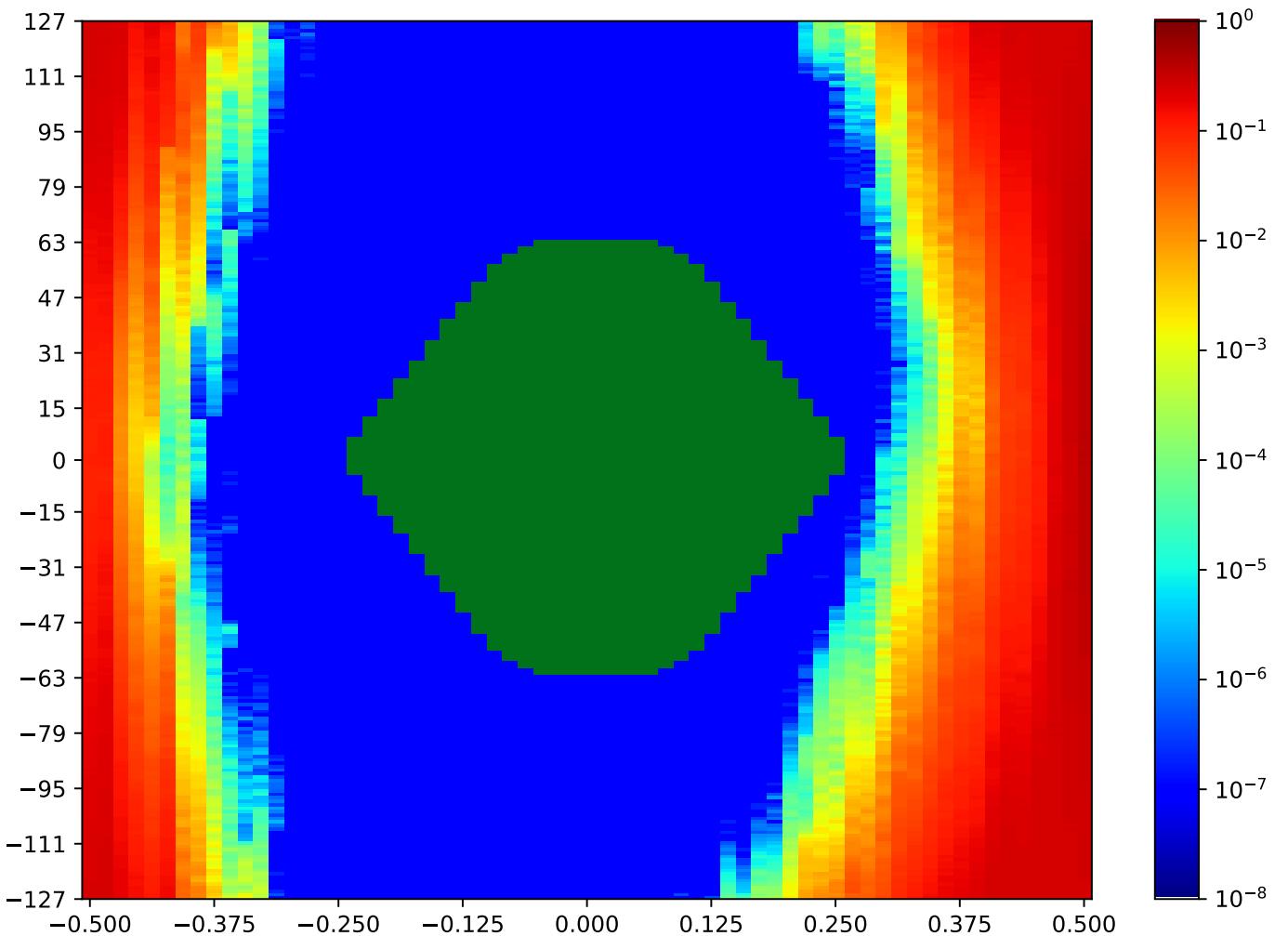


Figure 5.141: MSP_A_FPGA-TX2-00-RX18-00-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.2 MSP_A_FPGA-TX2-01-RX18-01-MSP_C_FPGA

Table 5.131: MSP_A_FPGA-TX2-01-RX18-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:16:14		2018-Sep-27 16:16:34	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9040	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

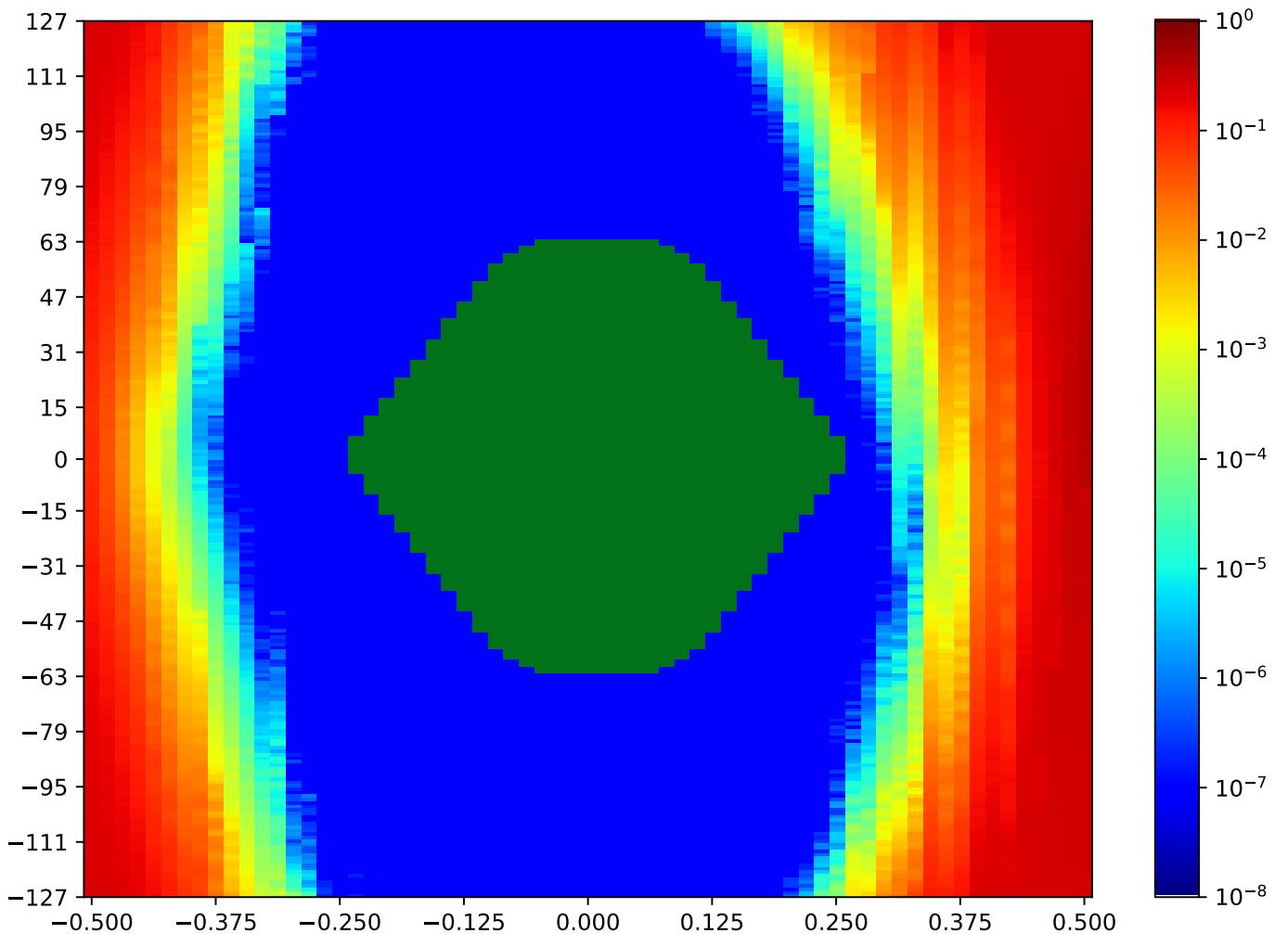


Figure 5.142: MSP_A_FPGA-TX2-01-RX18-01-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.3 MSP_A_FPGA-TX2-02-RX18-02-MSP_C_FPGA

Table 5.132: MSP_A_FPGA-TX2-02-RX18-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:17:57		2018-Sep-27 16:18:17	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8723	41	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

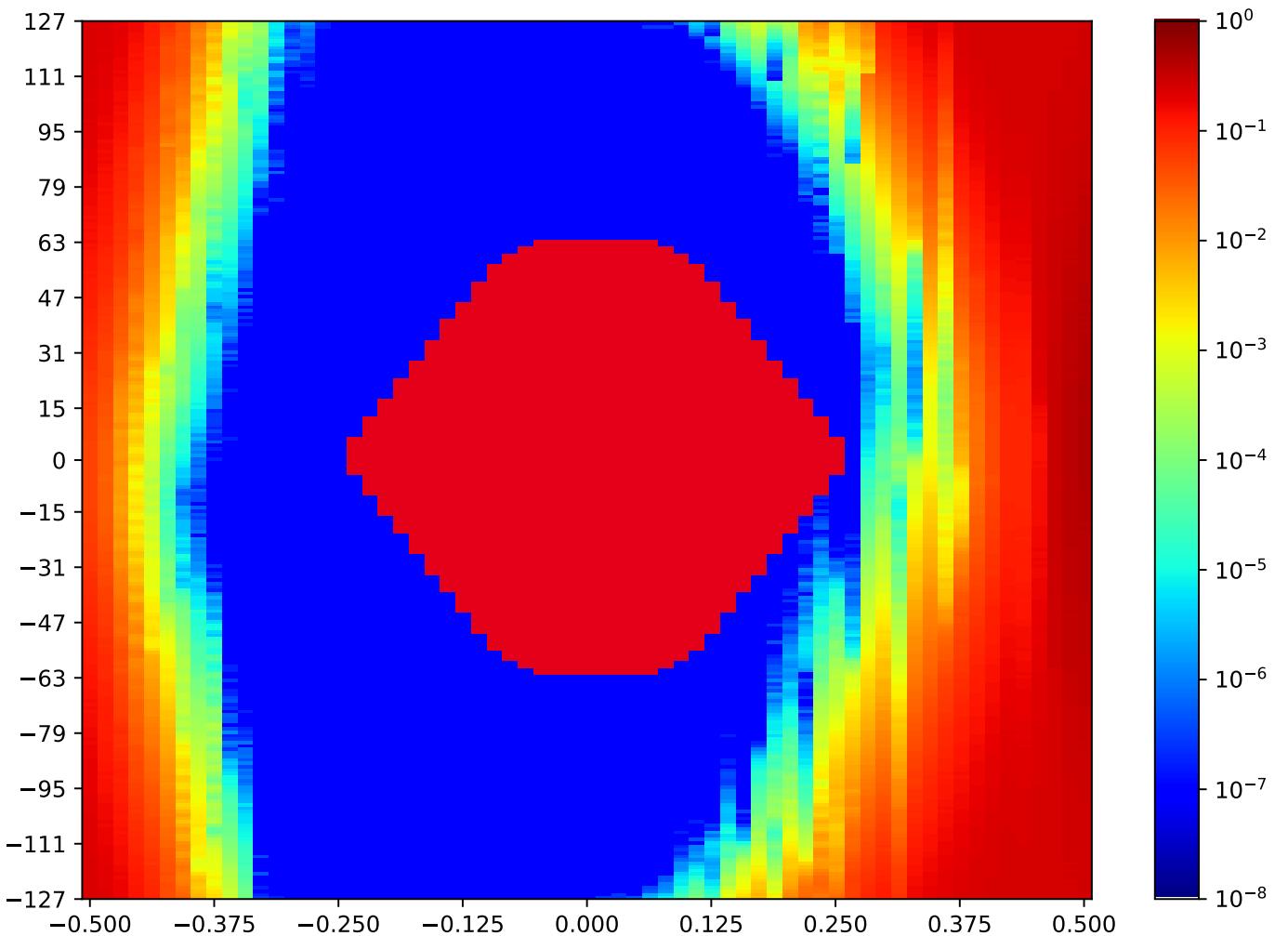


Figure 5.143: MSP_A_FPGA-TX2-02-RX18-02-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.4 MSP_A_FPGA-TX2-03-RX18-03-MSP_C_FPGA

Table 5.133: MSP_A_FPGA-TX2-03-RX18-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:15:53		2018-Sep-27 16:16:13	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9314	43		66.15%	252 96.47%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

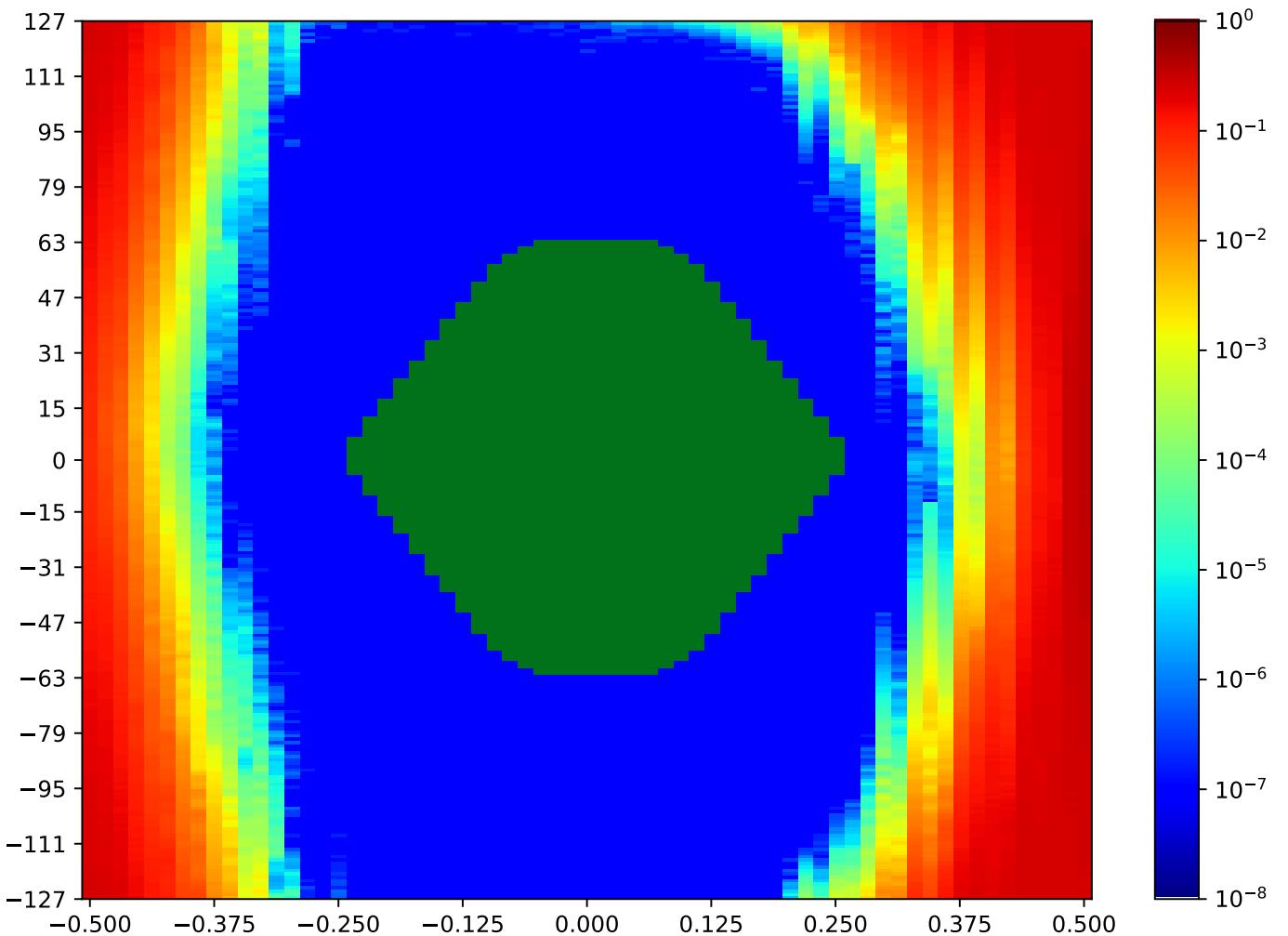


Figure 5.144: MSP_A_FPGA-TX2-03-RX18-03-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.5 MSP_A_FPGA-TX2-04-RX18-04-MSP_C_FPGA

Table 5.134: MSP_A_FPGA-TX2-04-RX18-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:18:58		2018-Sep-27 16:19:18	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9059	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

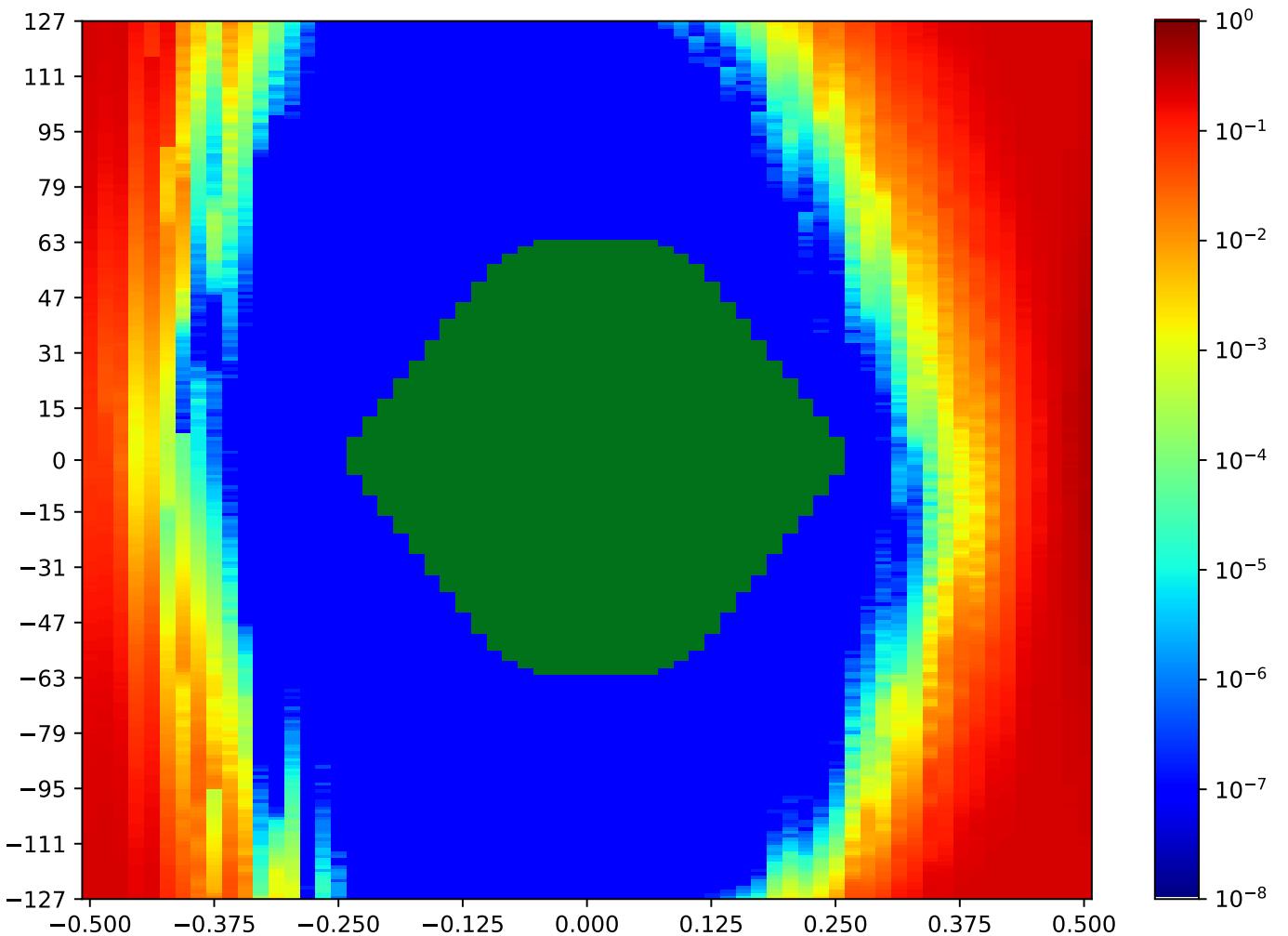


Figure 5.145: MSP_A_FPGA-TX2-04-RX18-04-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.6 MSP_A_FPGA-TX2-05-RX18-05-MSP_C_FPGA

Table 5.135: MSP_A_FPGA-TX2-05-RX18-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:16:34		2018-Sep-27 16:16:55	
Reset RX	OA	HO		VO	VO (%)
true	8330	42		240	93.33%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

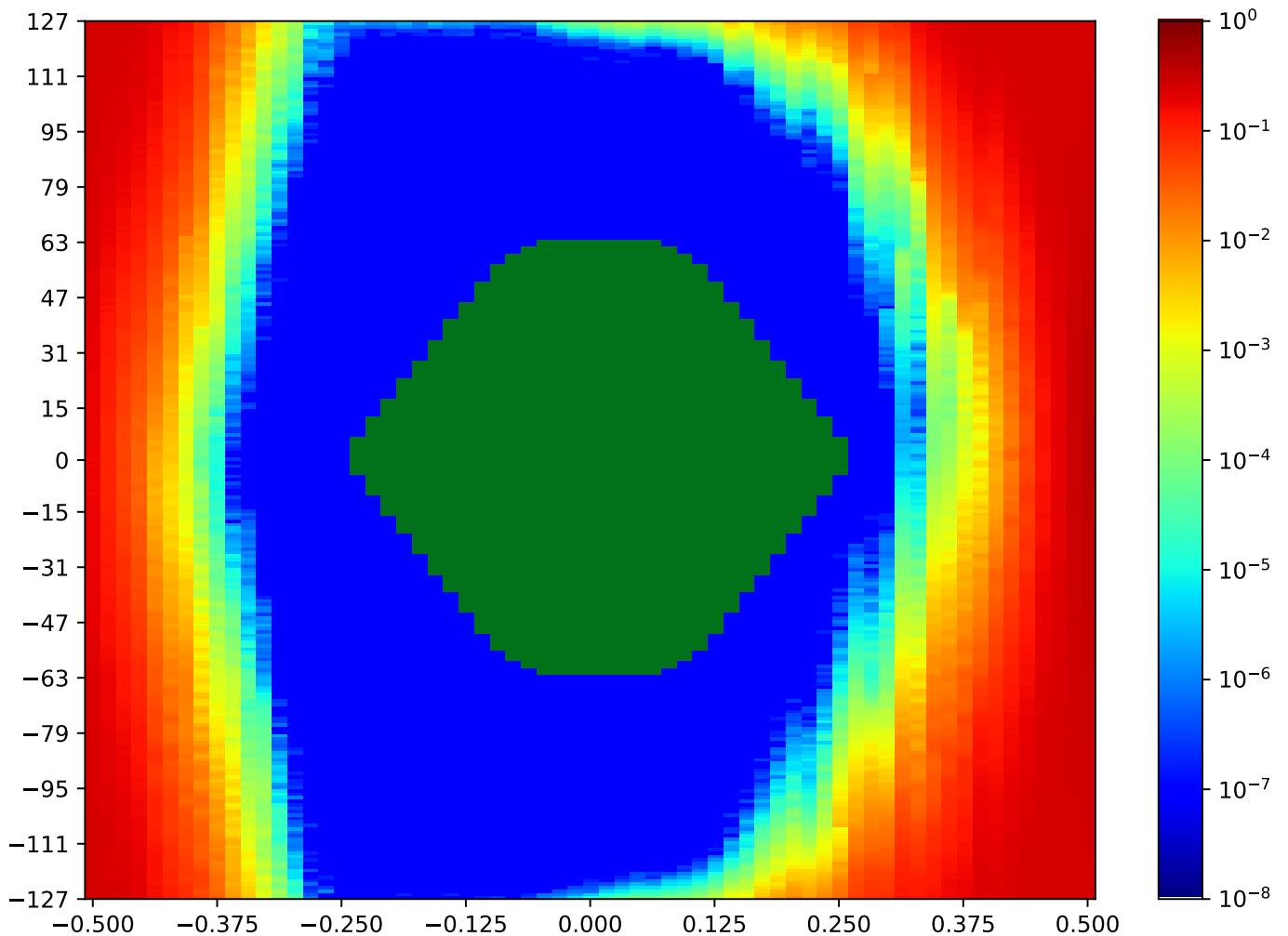


Figure 5.146: MSP_A_FPGA-TX2-05-RX18-05-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.7 MSP_A_FPGA-TX2-06-RX18-06-MSP_C_FPGA

Table 5.136: MSP_A_FPGA-TX2-06-RX18-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:19:39		2018-Sep-27 16:19:59	
Reset RX	OA	HO		VO	VO (%)
true	8648	42		64.62%	234 91.37%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

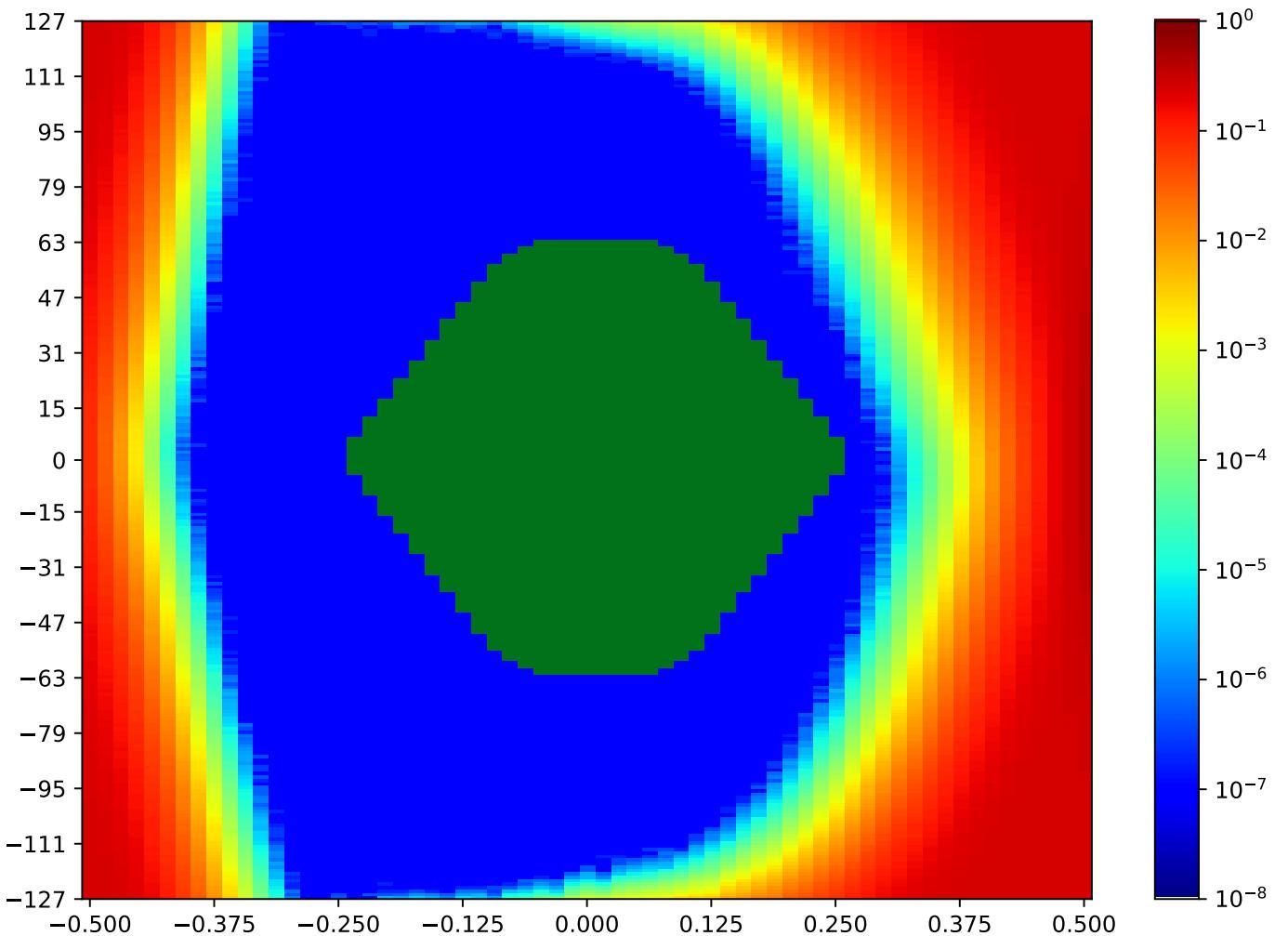


Figure 5.147: MSP_A_FPGA-TX2-06-RX18-06-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.8 MSP_A_FPGA-TX2-07-RX18-07-MSP_C_FPGA

Table 5.137: MSP_A_FPGA-TX2-07-RX18-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:17:16		2018-Sep-27 16:17:36	
Reset RX	OA	HO		VO	VO (%)
true	8583	44		233	89.80%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

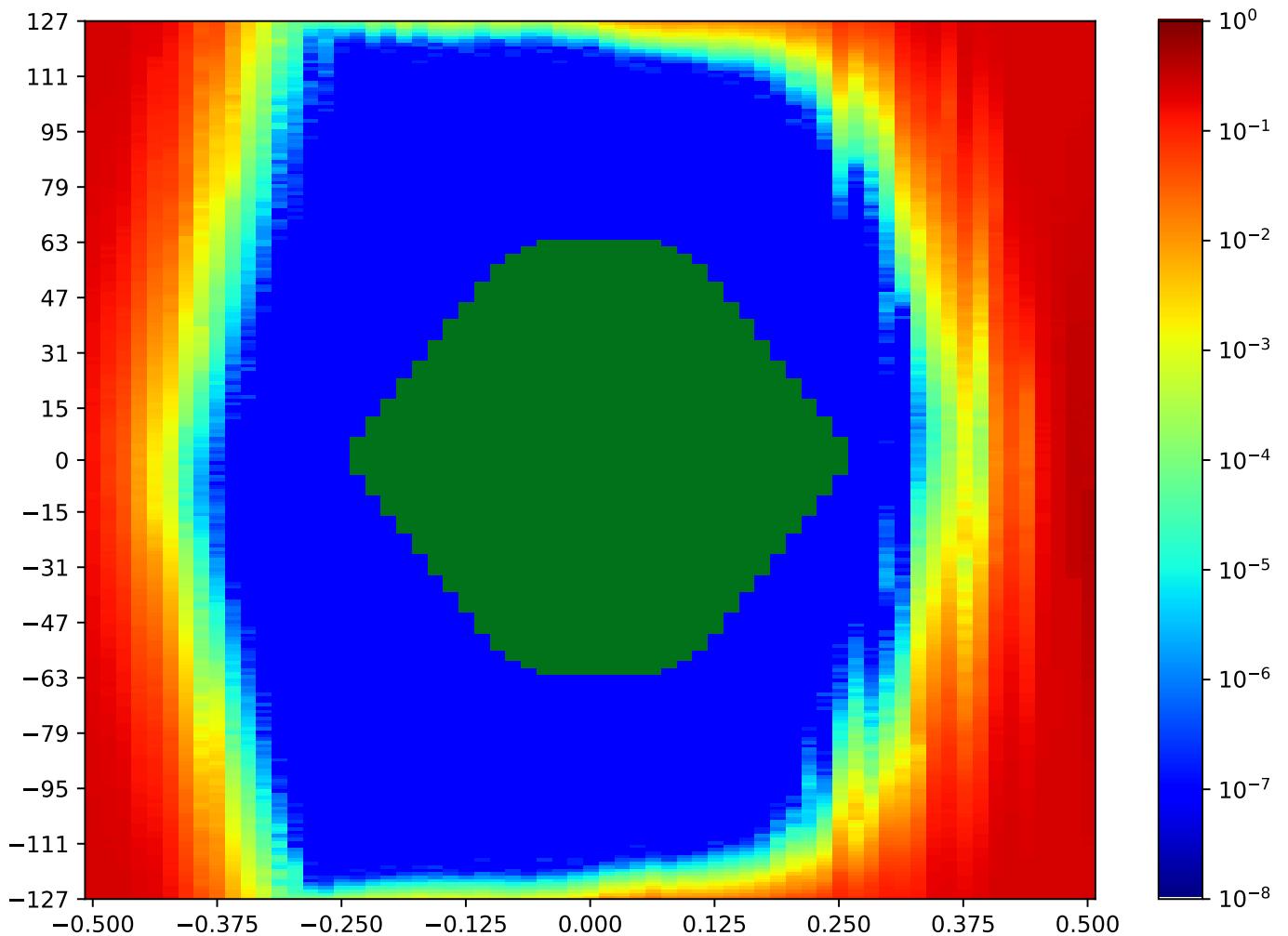


Figure 5.148: MSP_A_FPGA-TX2-07-RX18-07-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.9 MSP_A_FPGA-TX2-08-RX18-08-MSP_C_FPGA

Table 5.138: MSP_A_FPGA-TX2-08-RX18-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:19:19		2018-Sep-27 16:19:39	
Reset RX	OA	HO		VO	VO (%)
true	8829	43		255	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

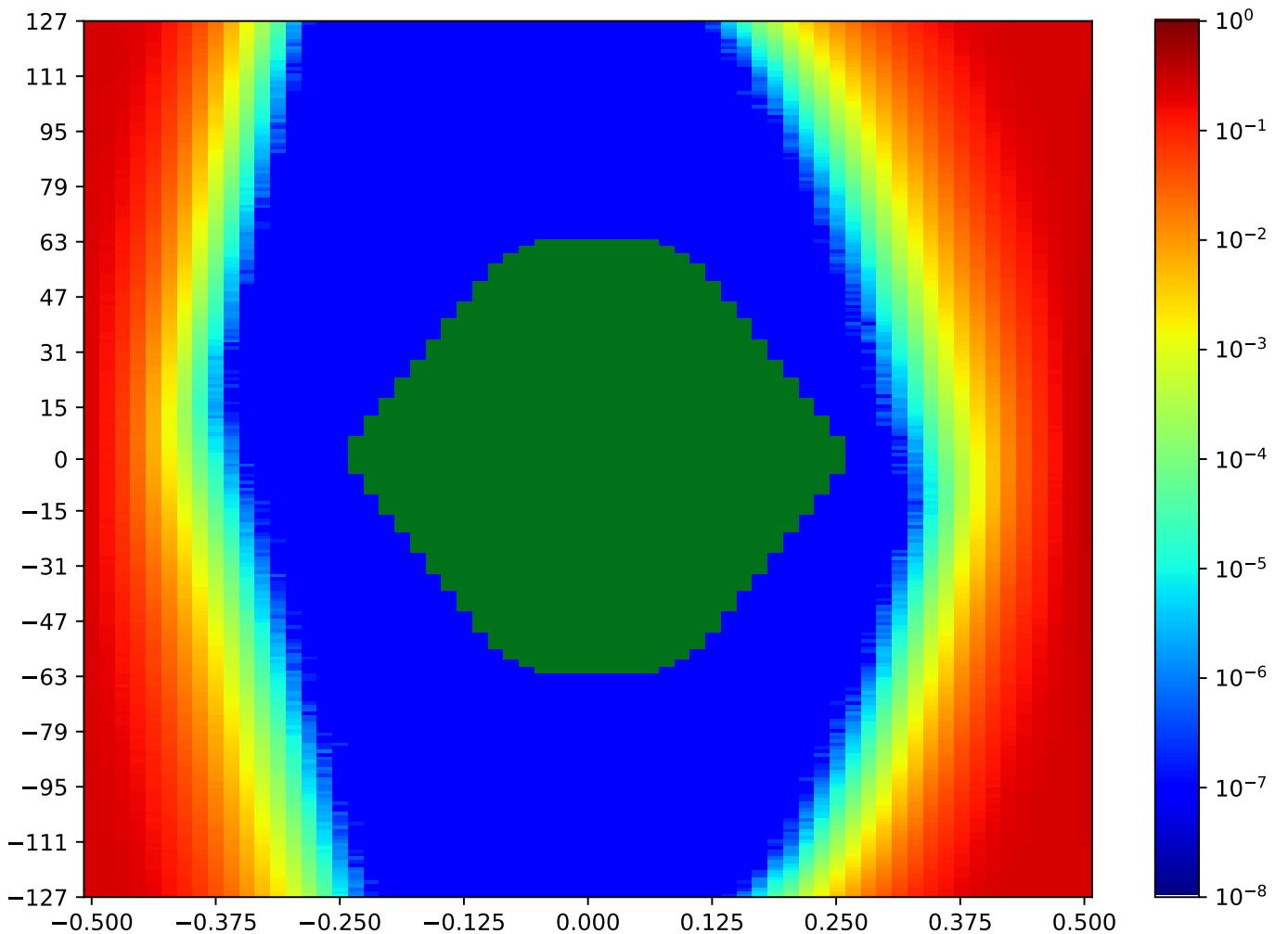


Figure 5.149: MSP_A_FPGA-TX2-08-RX18-08-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.10 MSP_A_FPGA-TX2-09-RX18-09-MSP_C_FPGA

Table 5.139: MSP_A_FPGA-TX2-09-RX18-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:17:36		2018-Sep-27 16:17:56	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8664	40	61.54%	247	96.86%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

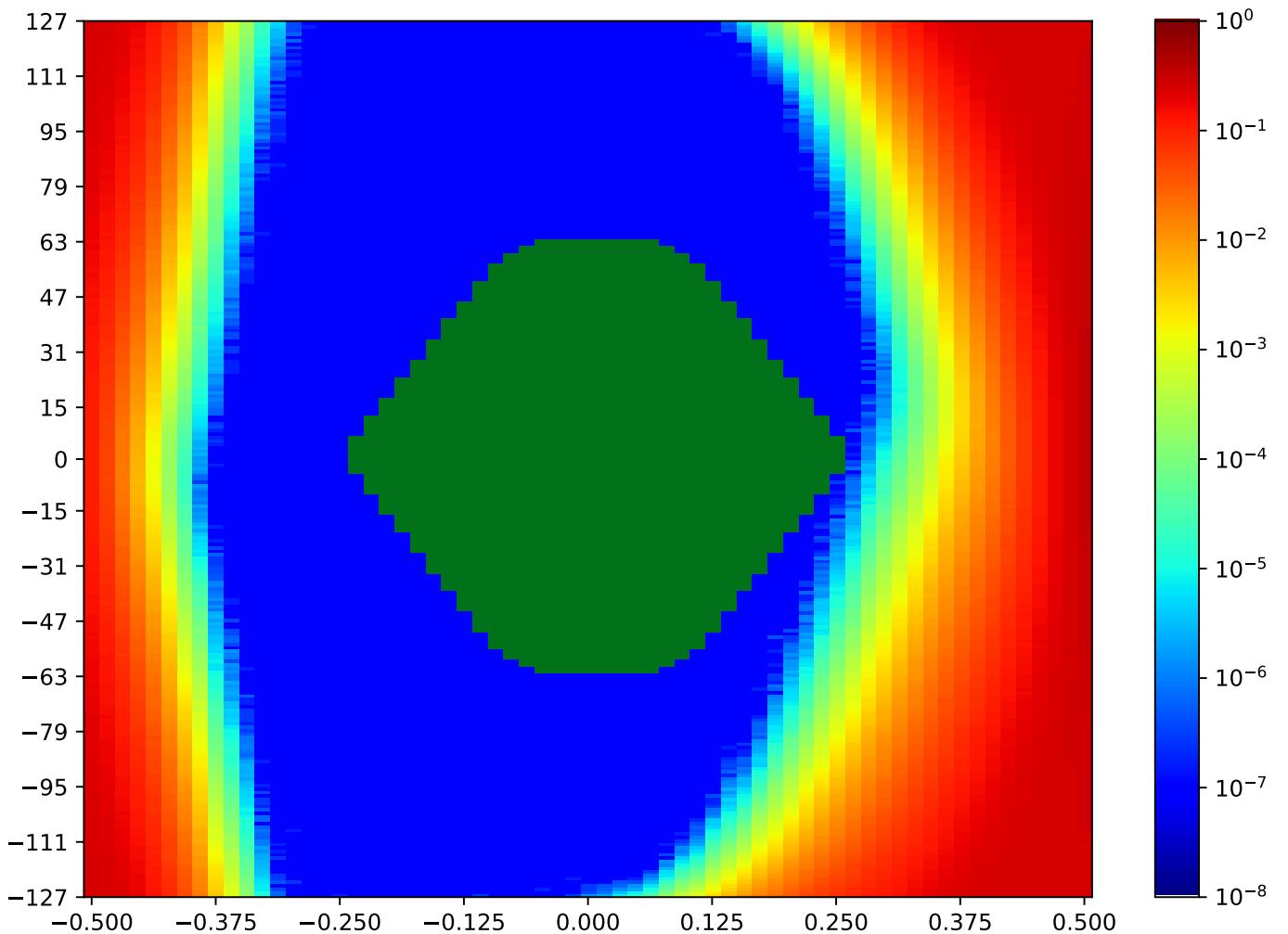


Figure 5.150: MSP_A_FPGA-TX2-09-RX18-09-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.11 MSP_A_FPGA-TX2-10-RX18-10-MSP_C_FPGA

Table 5.140: MSP_A_FPGA-TX2-10-RX18-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:18:37		2018-Sep-27 16:18:57	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9239	43	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

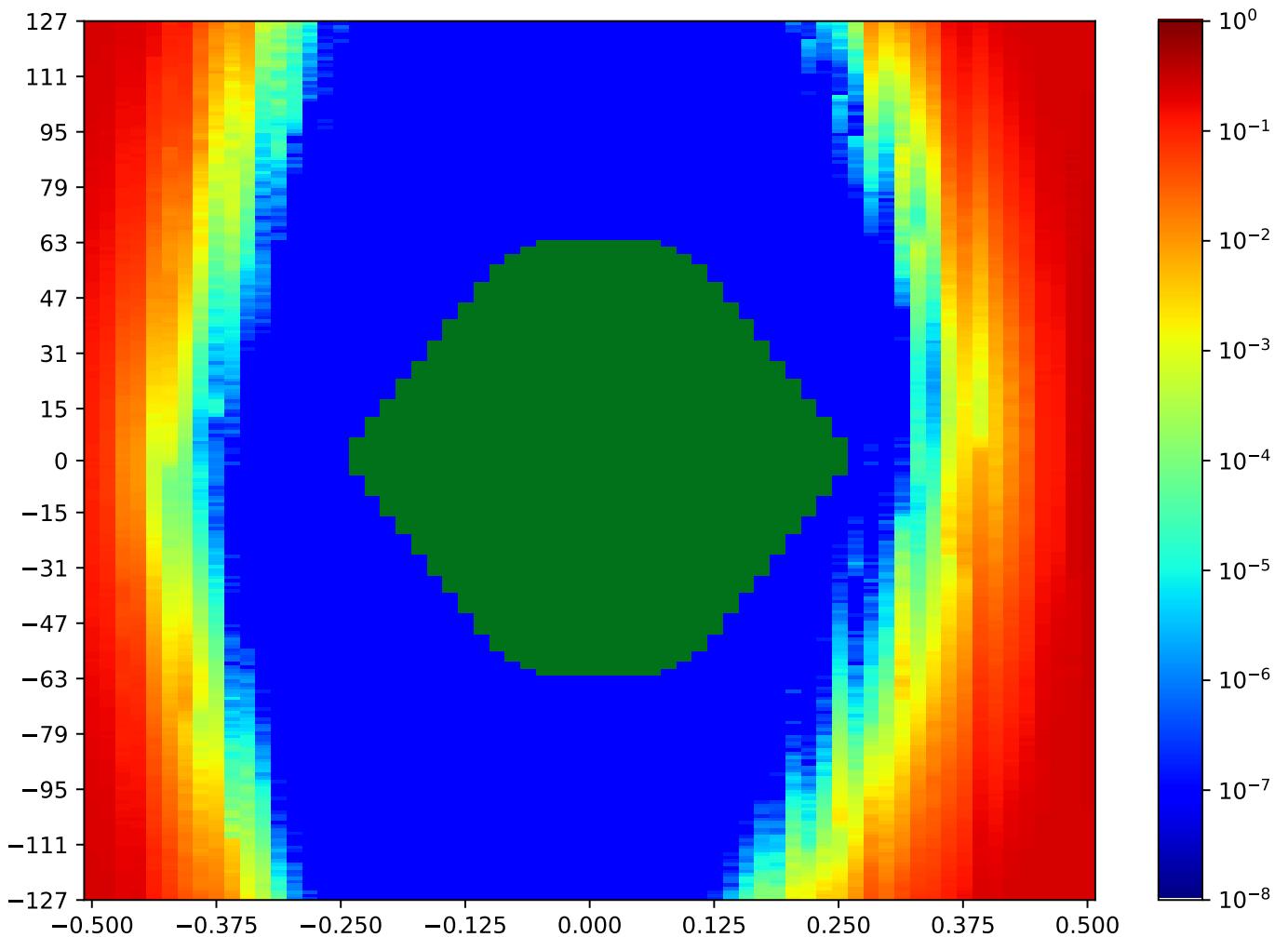


Figure 5.151: MSP_A_FPGA-TX2-10-RX18-10-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.11.12 MSP_A_FPGA-TX2-11-RX18-11-MSP_C_FPGA

Table 5.141: MSP_A_FPGA-TX2-11-RX18-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:18:17		2018-Sep-27 16:18:37	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9537	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

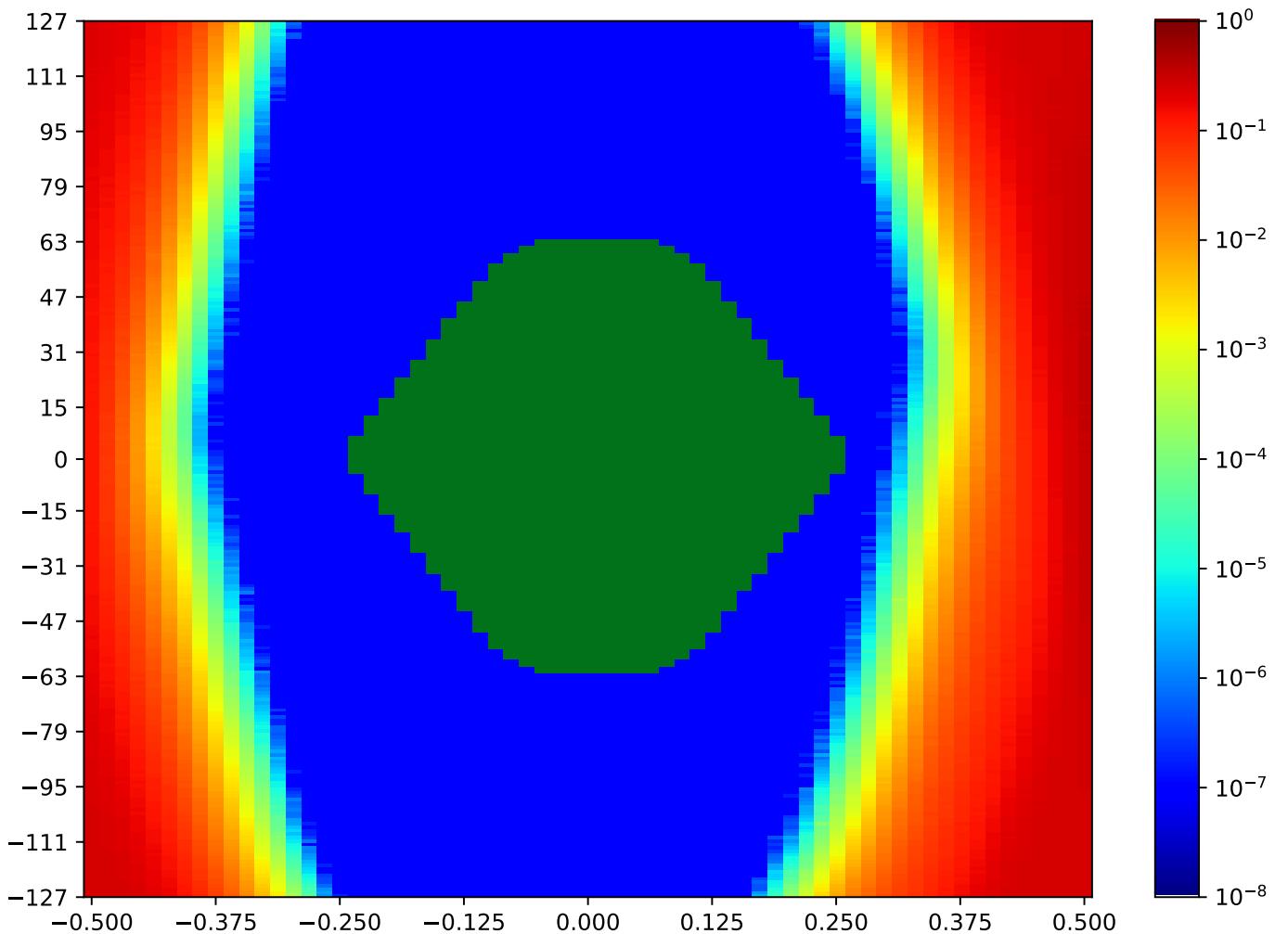


Figure 5.152: MSP_A_FPGA-TX2-11-RX18-11-MSP_C_FPGA

Call back to summary Figure 5.140. Sibling eye diagrams: V2-6.4.

5.12 MSP_C TX3 MSP_A RX8 Minipod Loopback

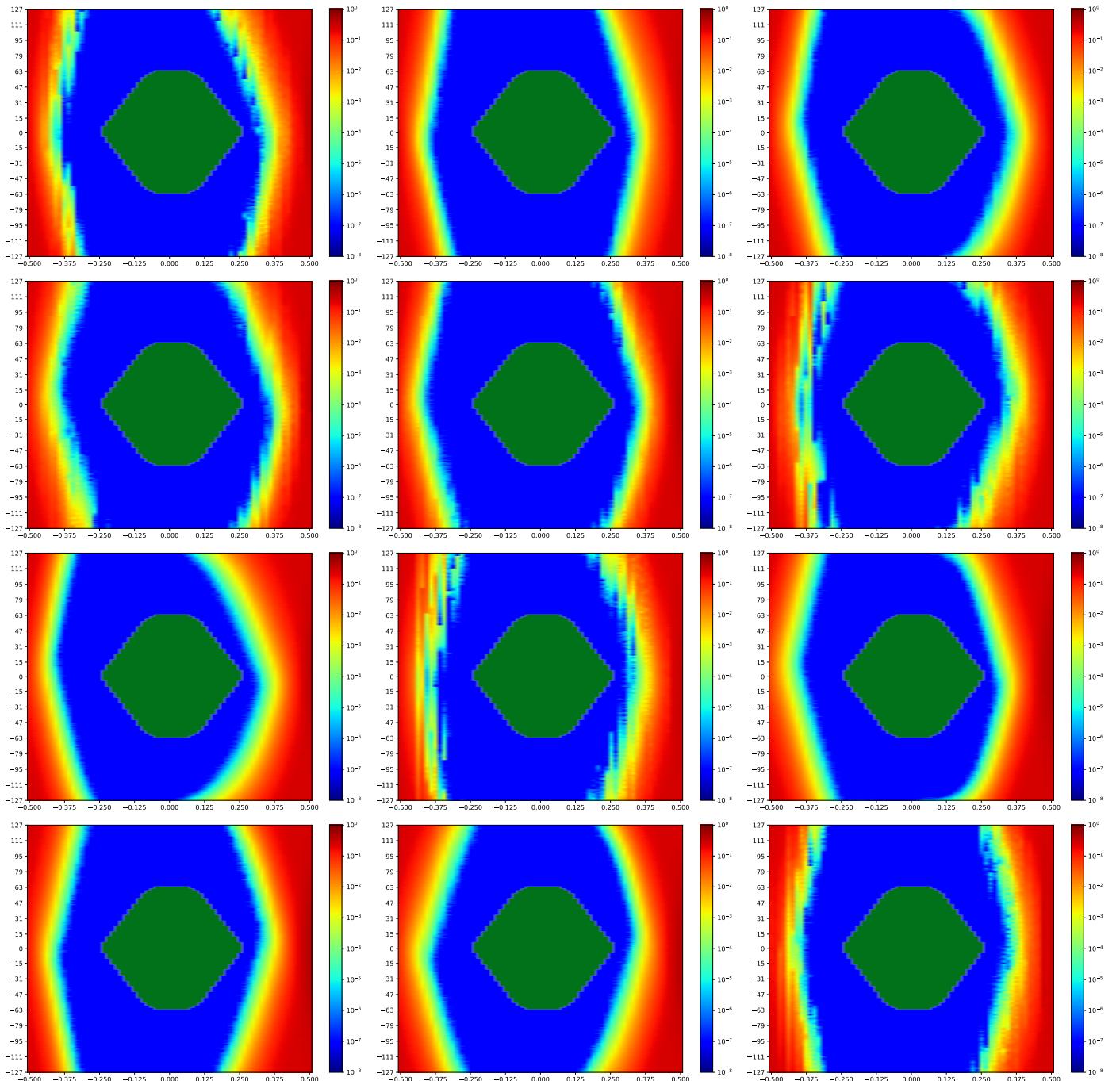


Figure 5.153: MSP_C TX3 MSP_A RX8 Minipod Loopback

A cross-reference to Figure 5.153. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.166.

5.12.1 MSP_C_FPGA-TX3-00-RX8-00-MSP_A_FPGA

Table 5.142: MSP_C_FPGA-TX3-00-RX8-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:21:02		2018-Sep-27 16:21:22	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9533	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

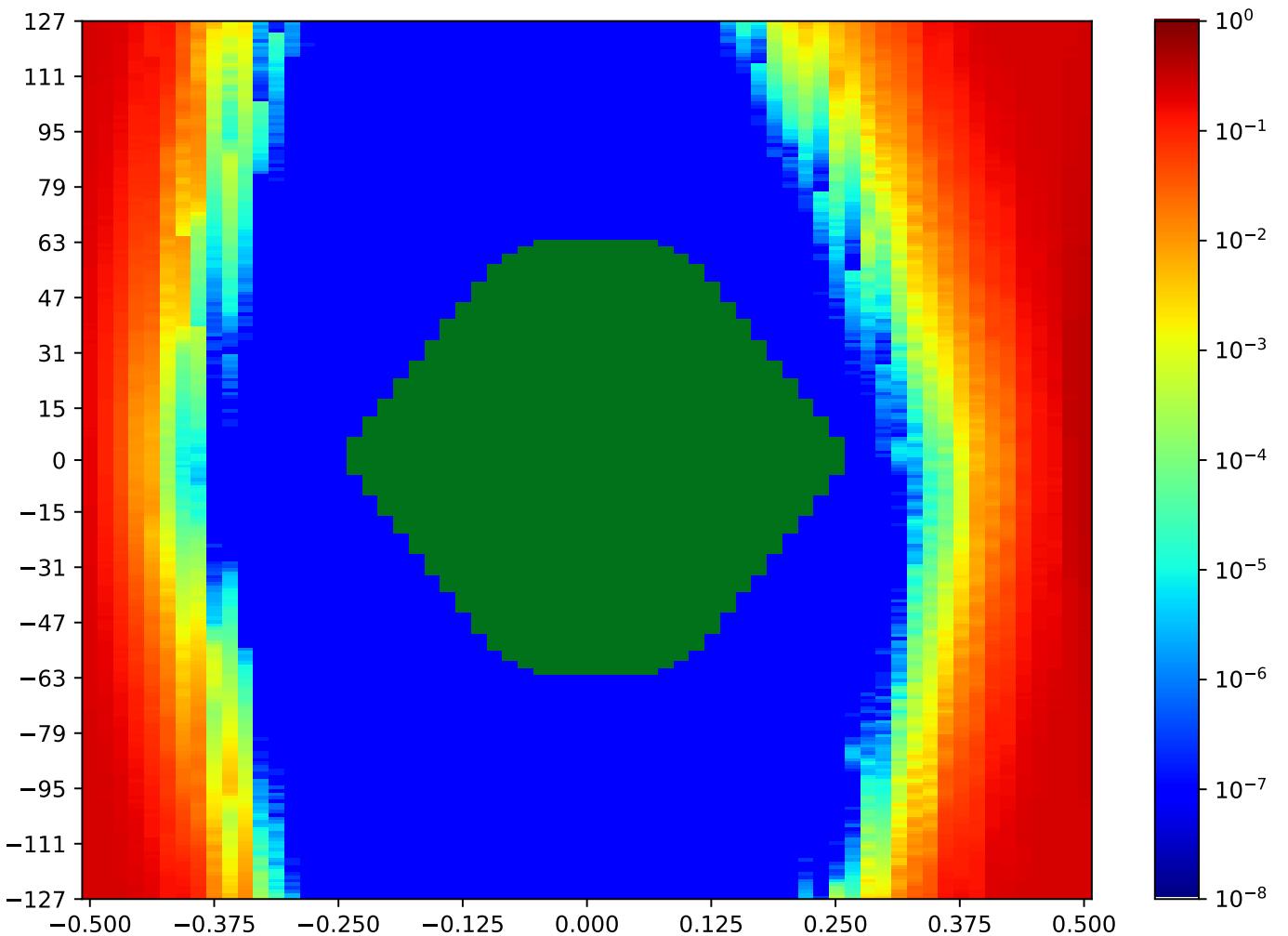


Figure 5.154: MSP_C_FPGA-TX3-00-RX8-00-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.2 MSP_C_FPGA-TX3-01-RX8-01-MSP_A_FPGA

Table 5.143: MSP_C_FPGA-TX3-01-RX8-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:21:43		2018-Sep-27 16:22:03	
Reset RX	OA	HO		VO	VO (%)
true	9705	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

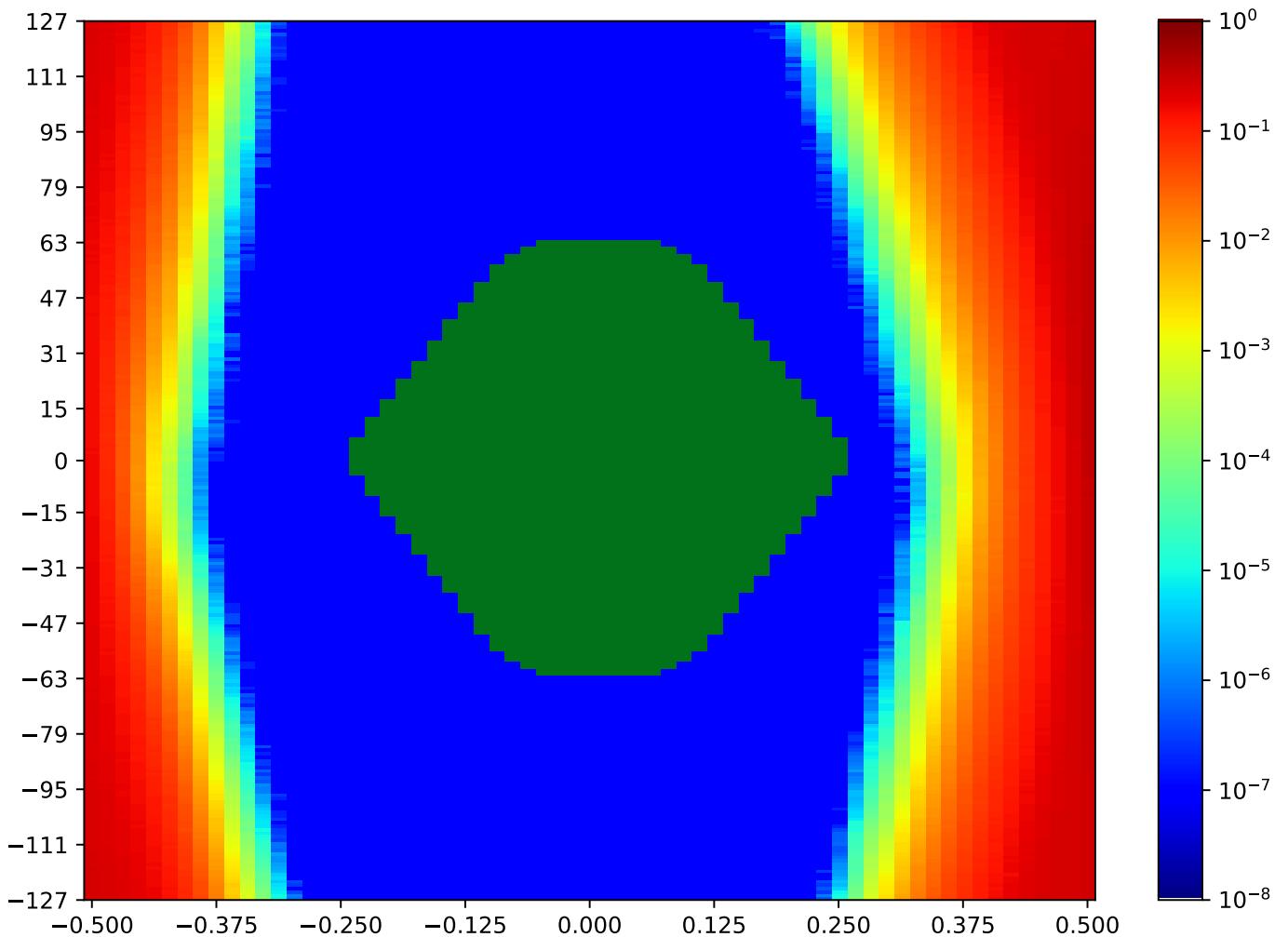


Figure 5.155: MSP_C_FPGA-TX3-01-RX8-01-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.3 MSP_C_FPGA-TX3-02-RX8-02-MSP_A_FPGA

Table 5.144: MSP_C_FPGA-TX3-02-RX8-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:22:03		2018-Sep-27 16:22:24	
Reset RX	OA	HO		VO	VO (%)
true	9390	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

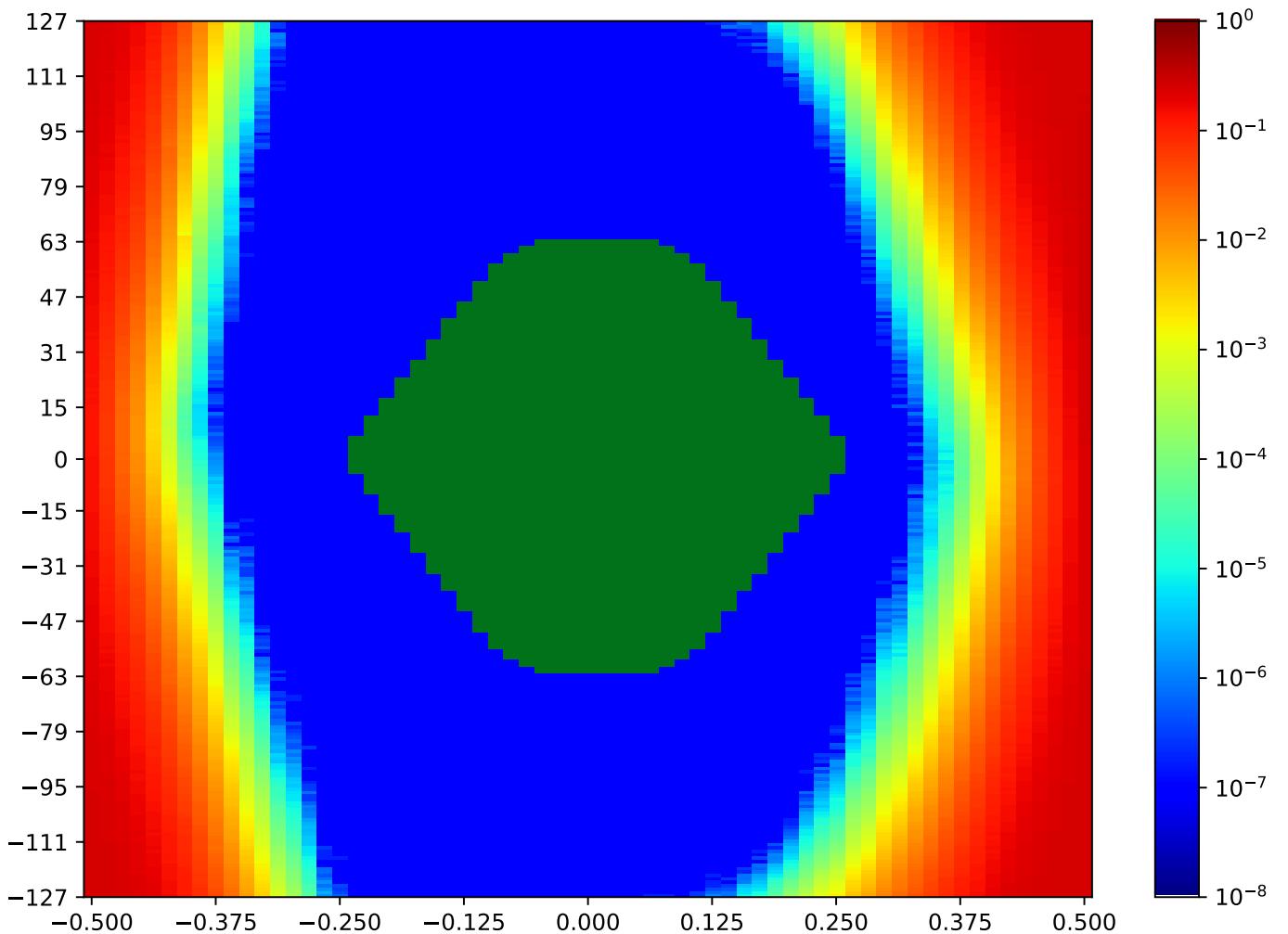


Figure 5.156: MSP_C_FPGA-TX3-02-RX8-02-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.4 MSP_C_FPGA-TX3-03-RX8-03-MSP_A_FPGA

Table 5.145: MSP_C_FPGA-TX3-03-RX8-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:20:20		2018-Sep-27 16:20:41	
Reset RX	OA	HO		VO	VO (%)
true	9465	44		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

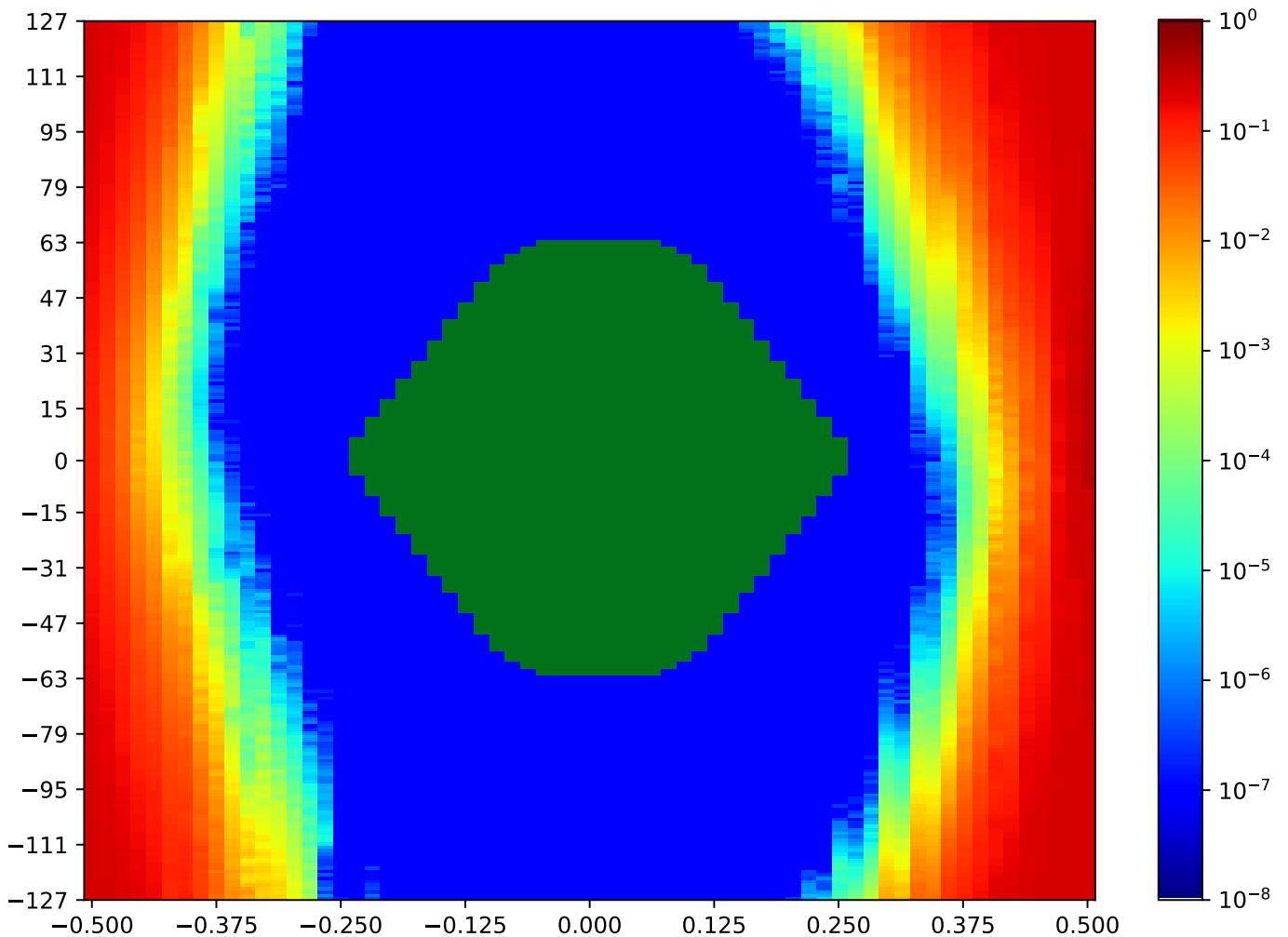


Figure 5.157: MSP_C_FPGA-TX3-03-RX8-03-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.5 MSP_C_FPGA-TX3-04-RX8-04-MSP_A_FPGA

Table 5.146: MSP_C_FPGA-TX3-04-RX8-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:23:05		2018-Sep-27 16:23:25	
Reset RX	OA	HO		VO	VO (%)
true	9853	46		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

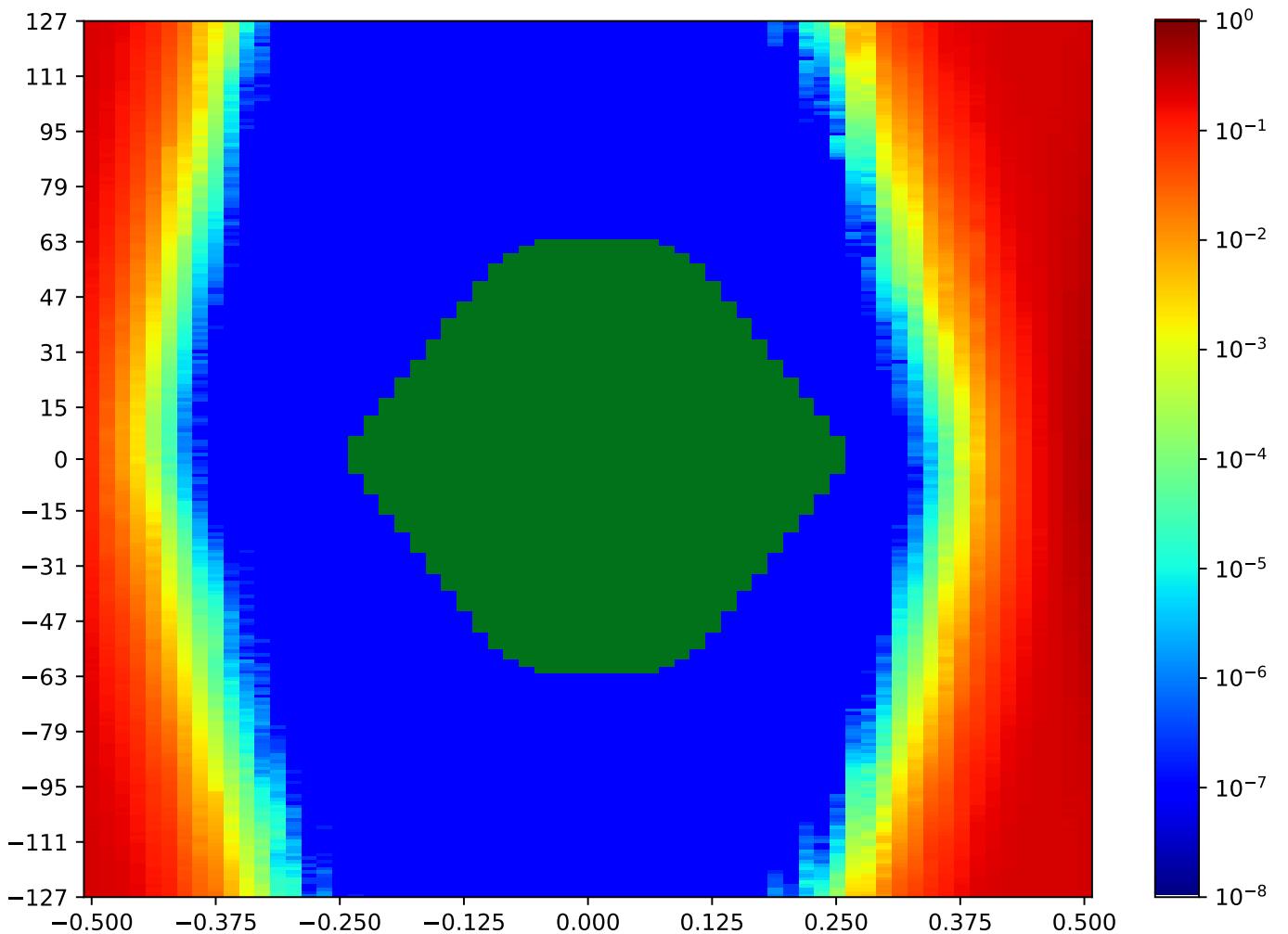


Figure 5.158: MSP_C_FPGA-TX3-04-RX8-04-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.6 MSP_C_FPGA-TX3-05-RX8-05-MSP_A_FPGA

Table 5.147: MSP_C_FPGA-TX3-05-RX8-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:20:00		2018-Sep-27 16:20:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8887	43	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

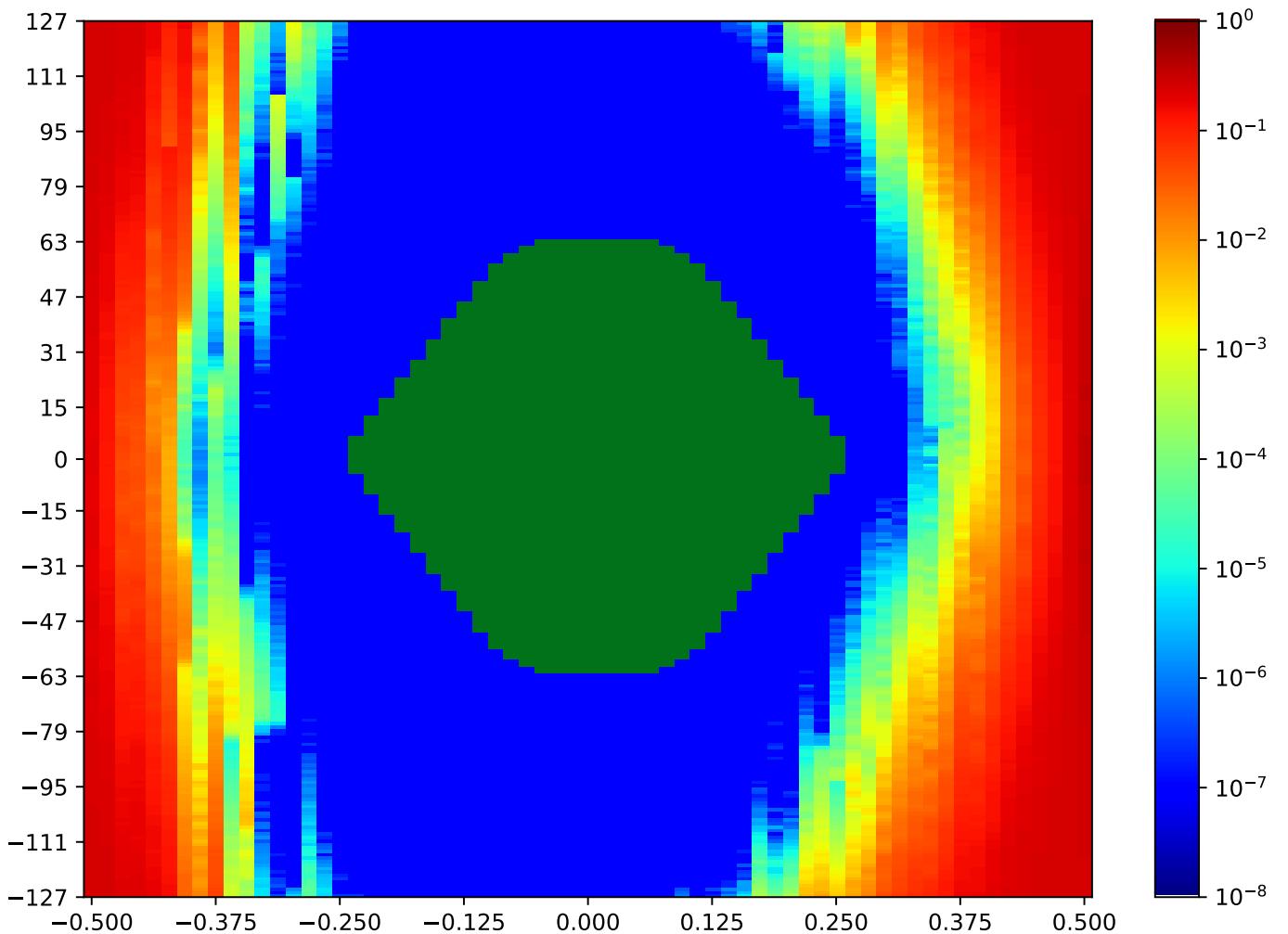


Figure 5.159: MSP_C_FPGA-TX3-05-RX8-05-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.7 MSP_C_FPGA-TX3-06-RX8-06-MSP_A_FPGA

Table 5.148: MSP_C_FPGA-TX3-06-RX8-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:23:46		2018-Sep-27 16:24:10	
Reset RX	OA	HO		VO	VO (%)
true	8742	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

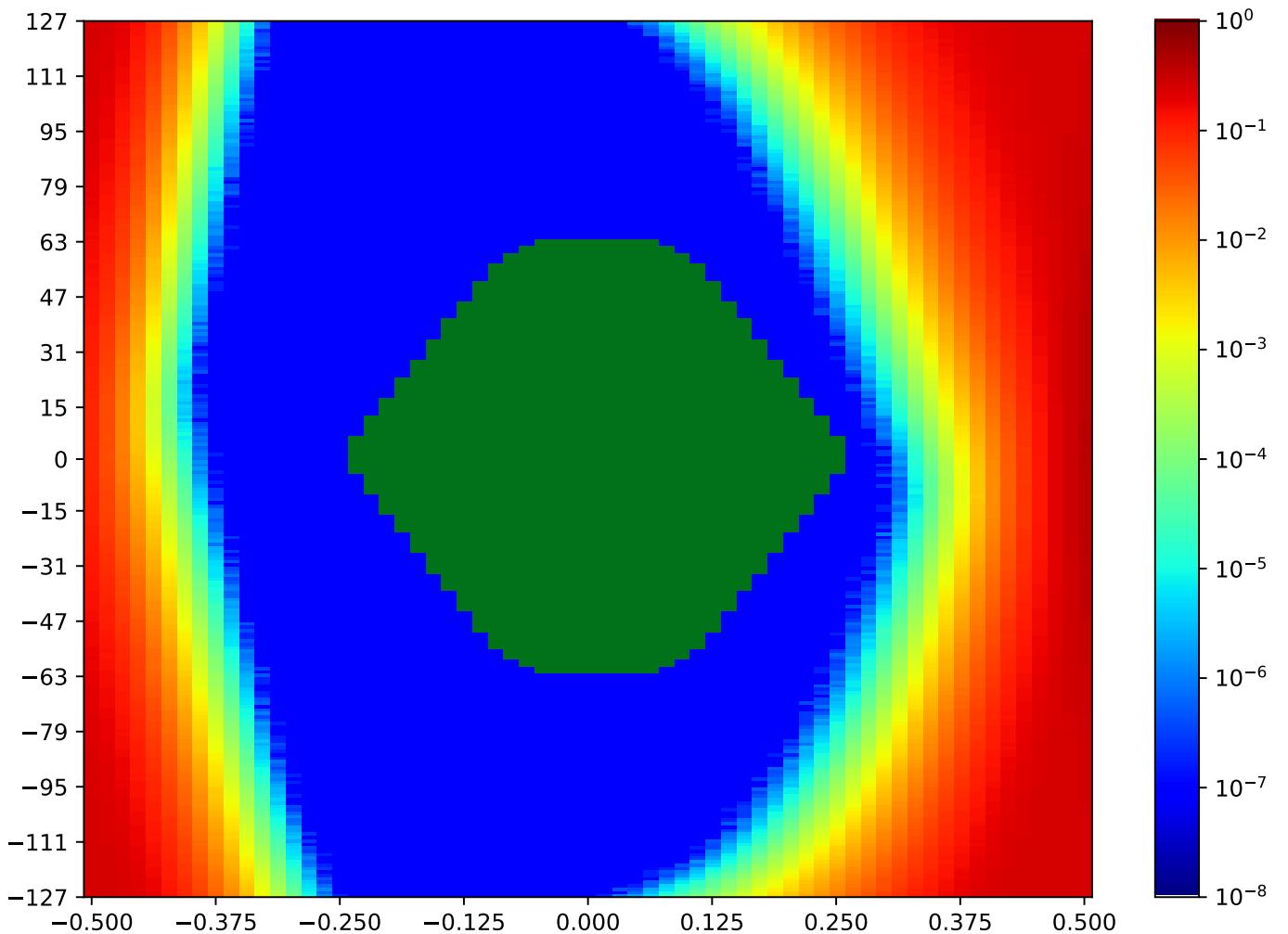


Figure 5.160: MSP_C_FPGA-TX3-06-RX8-06-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.8 MSP_C_FPGA-TX3-07-RX8-07-MSP_A_FPGA

Table 5.149: MSP_C_FPGA-TX3-07-RX8-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:20:41		2018-Sep-27 16:21:01	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9221	42		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

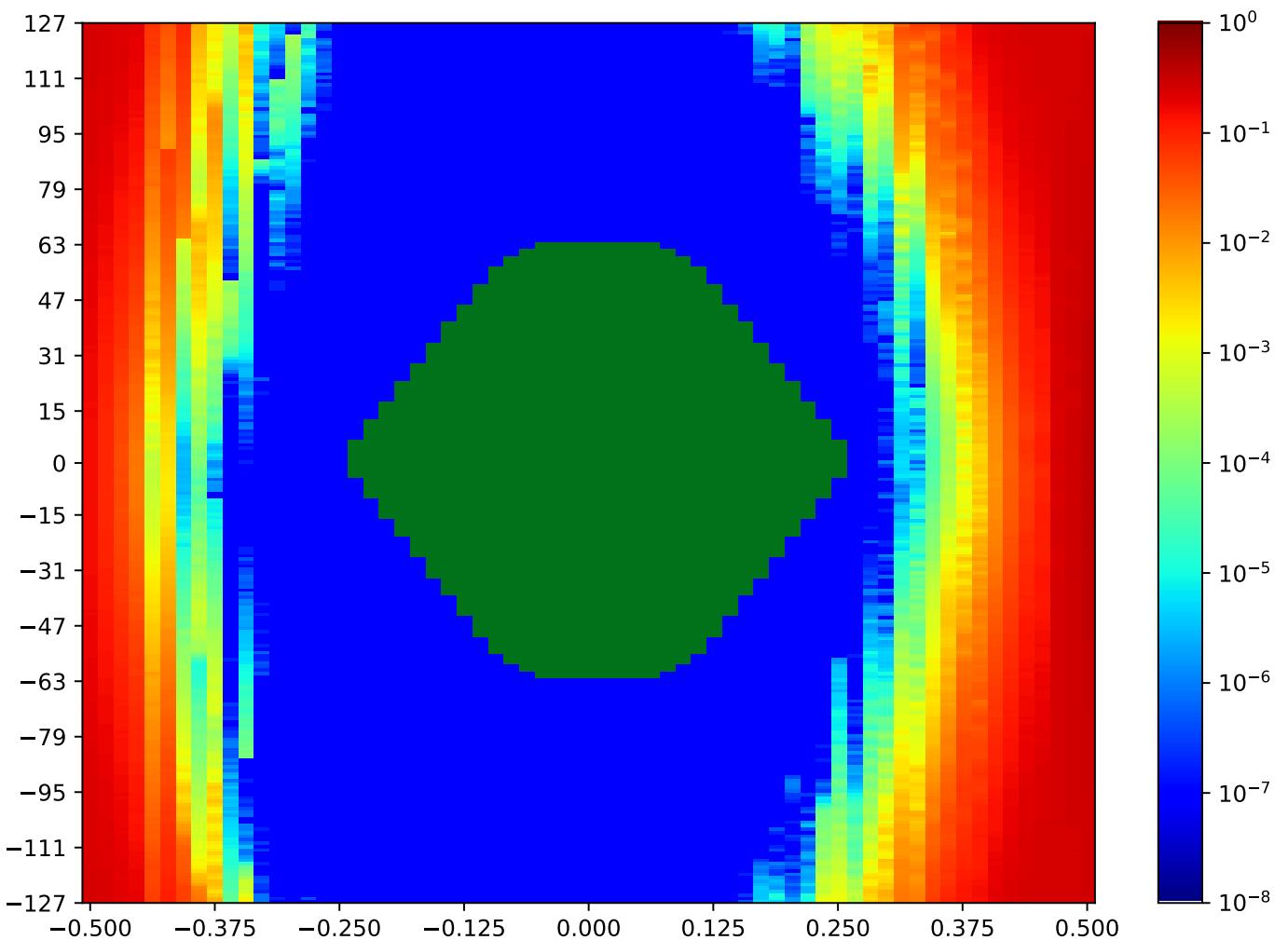


Figure 5.161: MSP_C_FPGA-TX3-07-RX8-07-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.9 MSP_C_FPGA-TX3-08-RX8-08-MSP_A_FPGA

Table 5.150: MSP_C_FPGA-TX3-08-RX8-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:23:26		2018-Sep-27 16:23:46	
Reset RX	OA	HO		VO	VO (%)
true	8798	40		253	99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

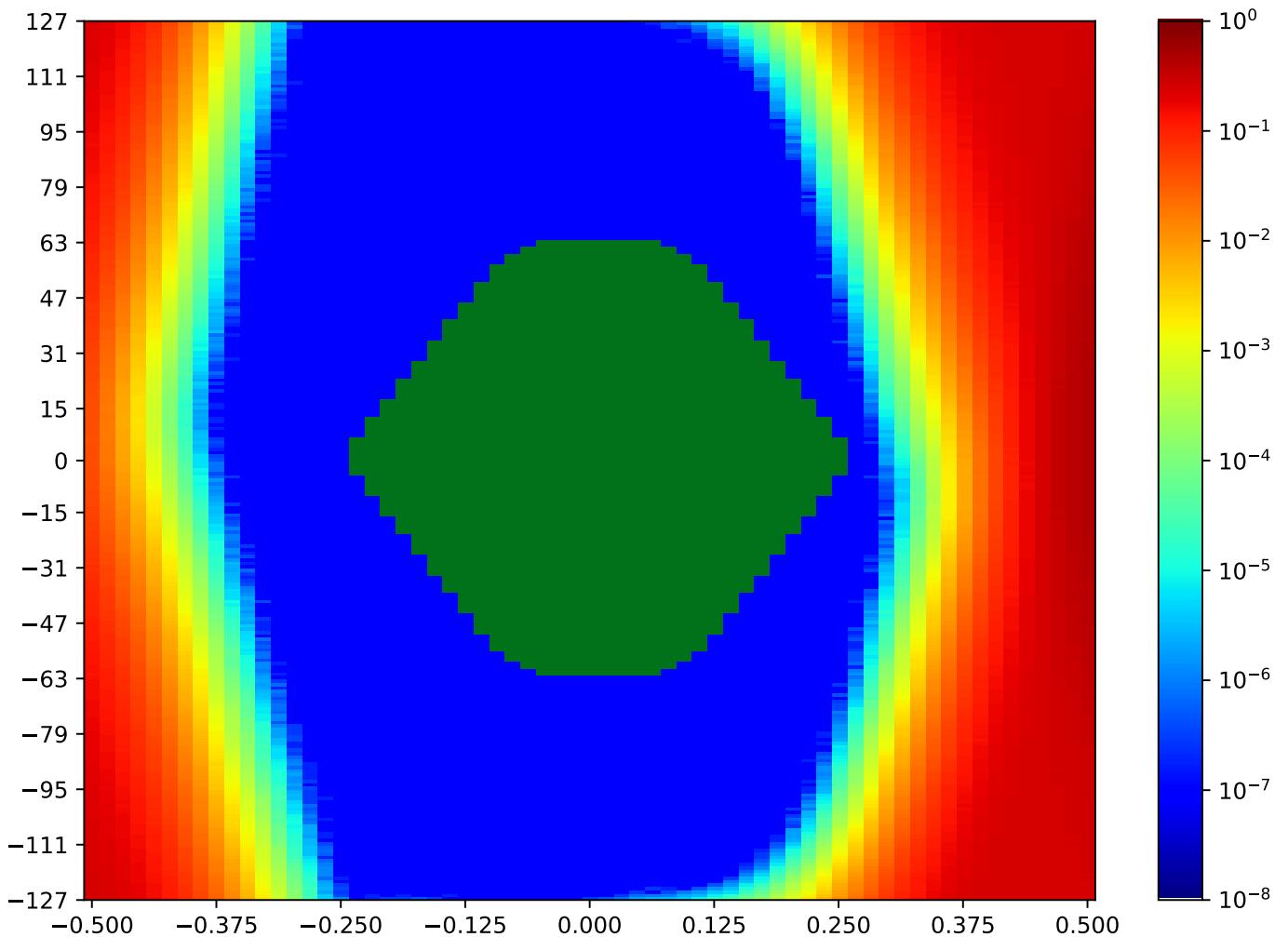


Figure 5.162: MSP_C_FPGA-TX3-08-RX8-08-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.10 MSP_C_FPGA-TX3-09-RX8-09-MSP_A_FPGA

Table 5.151: MSP_C_FPGA-TX3-09-RX8-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:21:22		2018-Sep-27 16:21:42	
Reset RX	OA	HO		VO	VO (%)
true	9421	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

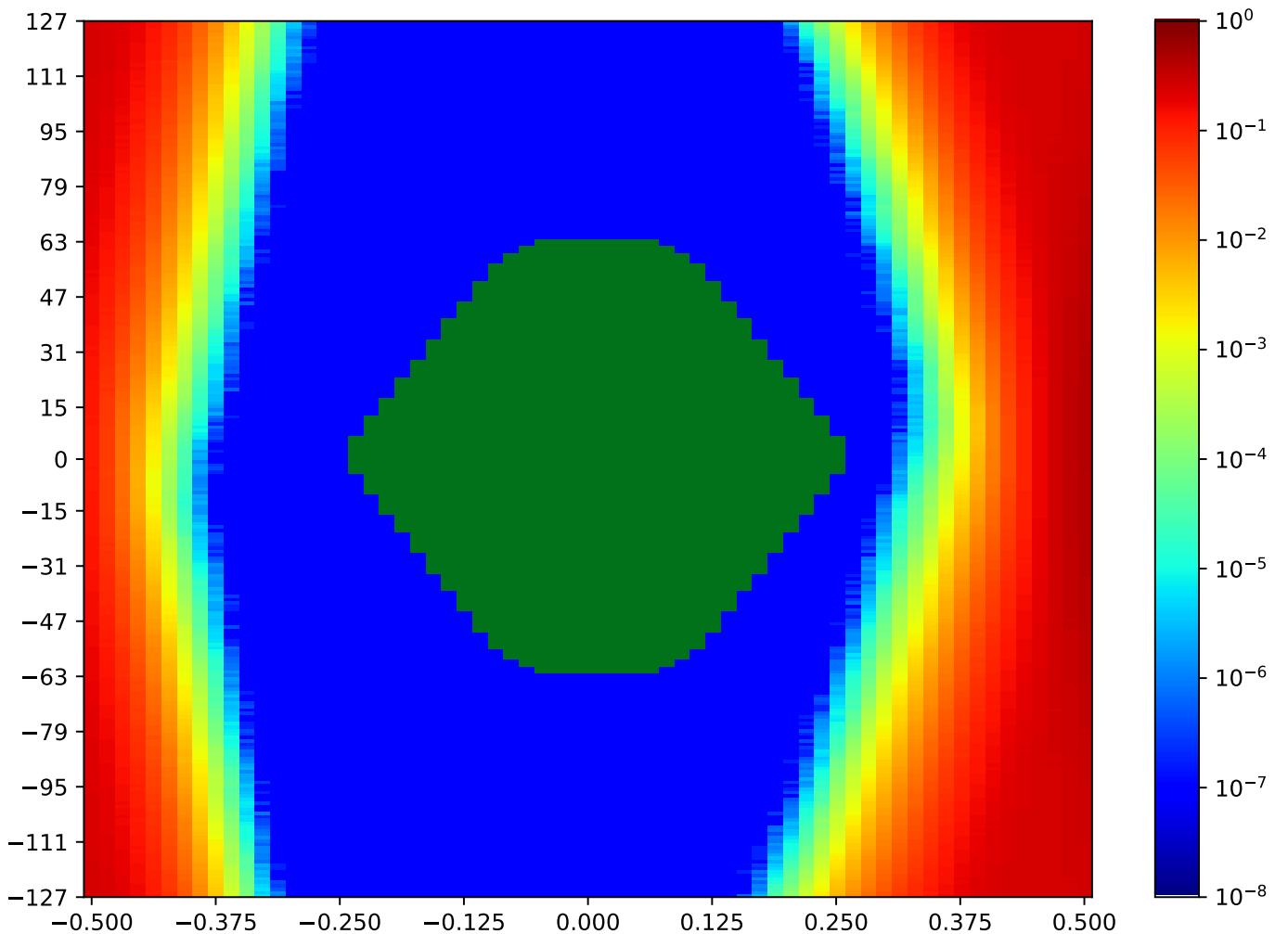


Figure 5.163: MSP_C_FPGA-TX3-09-RX8-09-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.11 MSP_C_FPGA-TX3-10-RX8-10-MSP_A_FPGA

Table 5.152: MSP_C_FPGA-TX3-10-RX8-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:22:45		2018-Sep-27 16:23:05	
Reset RX	OA	HO		VO	VO (%)
true	8925	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

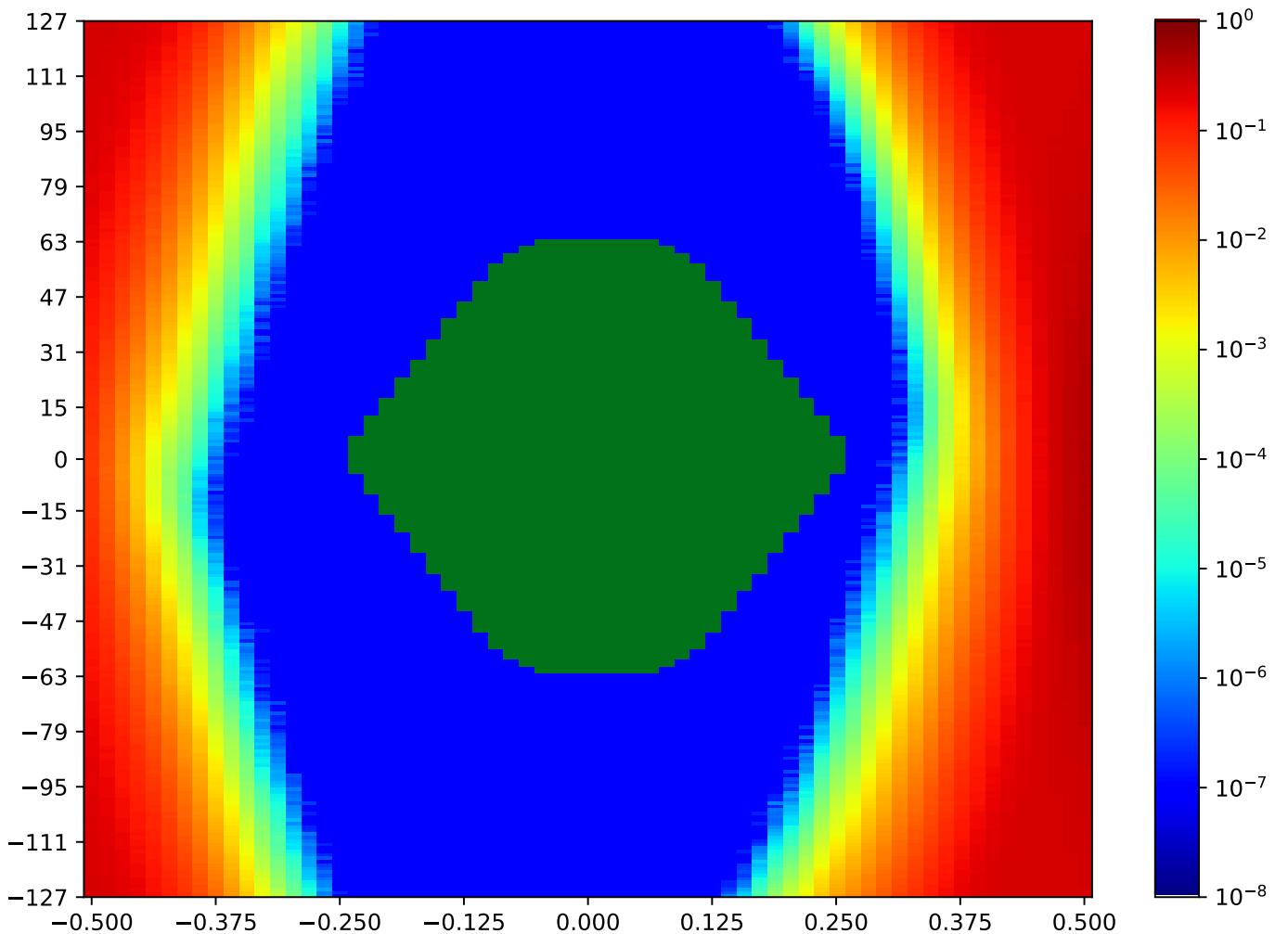


Figure 5.164: MSP_C_FPGA-TX3-10-RX8-10-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.12.12 MSP_C_FPGA-TX3-11-RX8-11-MSP_A_FPGA

Table 5.153: MSP_C_FPGA-TX3-11-RX8-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:22:24		2018-Sep-27 16:22:44	
Reset RX	OA	HO		VO	VO (%)
true	9980	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

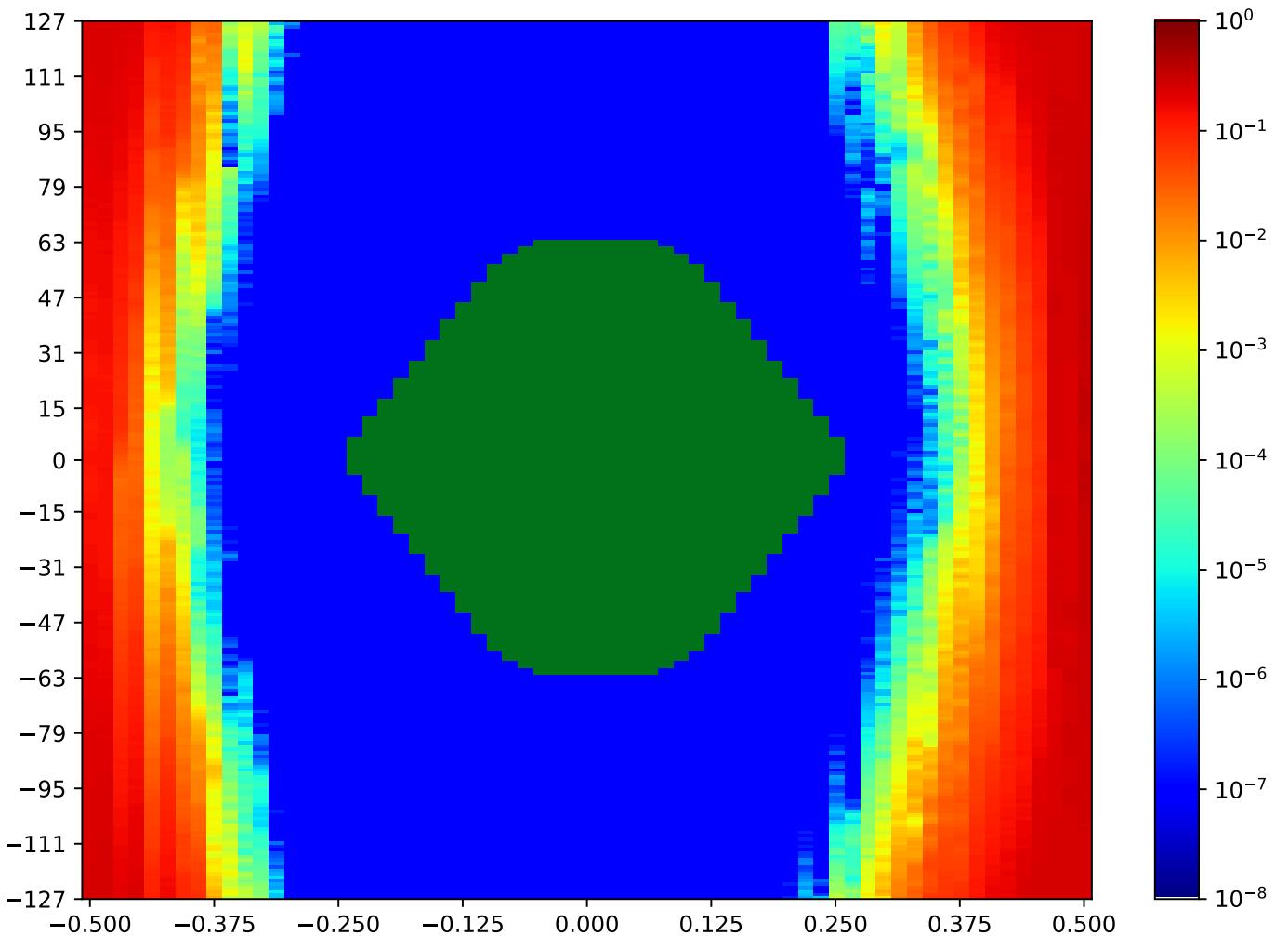


Figure 5.165: MSP_C_FPGA-TX3-11-RX8-11-MSP_A_FPGA

Call back to summary Figure 5.153. Sibling eye diagrams: V2-6.4.

5.13 MSP_C TX4 MSP_A RX9 Minipod Loopback

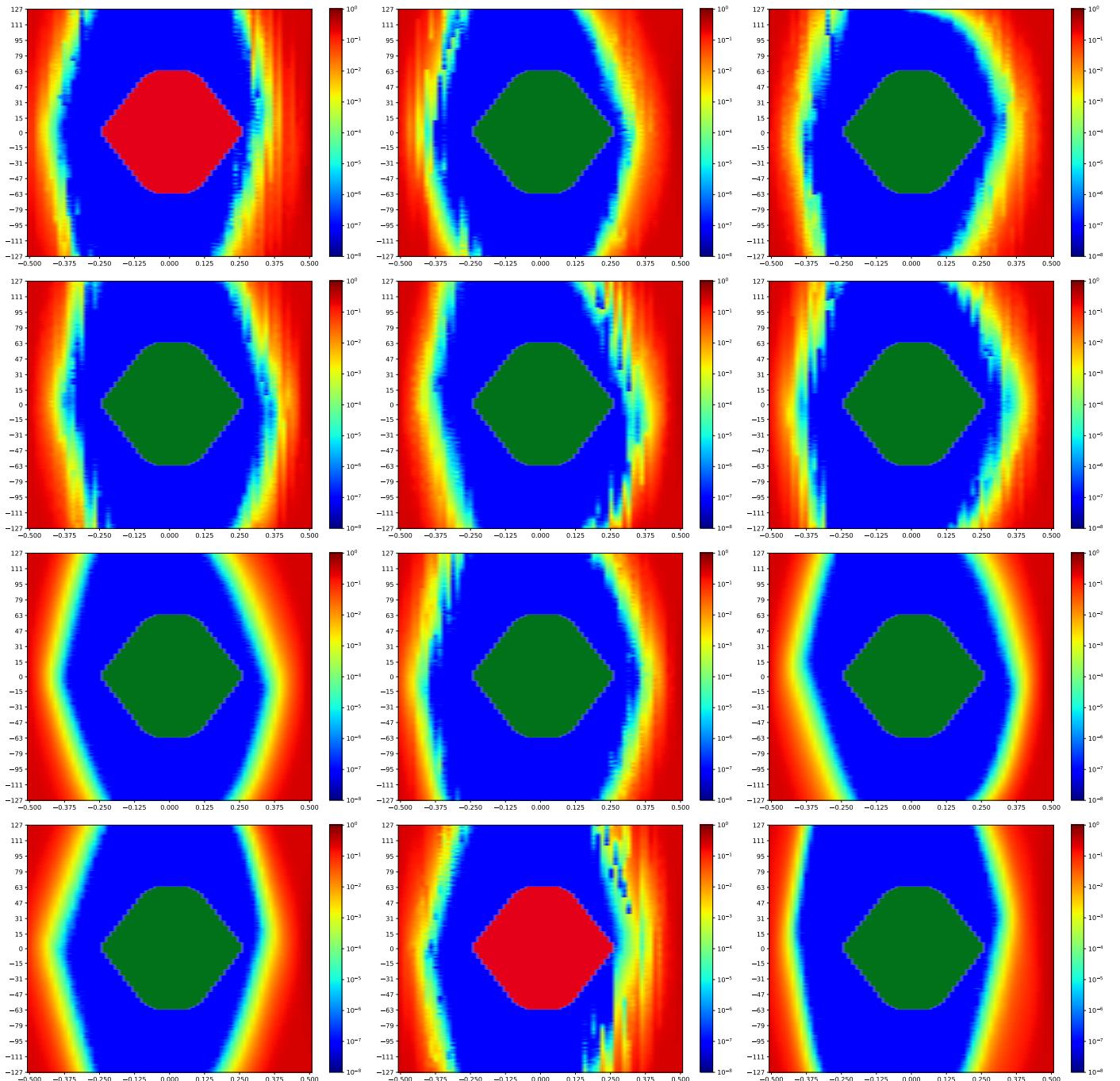


Figure 5.166: MSP_C TX4 MSP_A RX9 Minipod Loopback

A cross-reference to Figure 5.166. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.179.

5.13.1 MSP_C_FPGA-TX4-00-RX9-00-MSP_A_FPGA

Table 5.154: MSP_C_FPGA-TX4-00-RX9-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:25:12		2018-Sep-27 16:25:37	
Reset RX	OA	HO		VO	VO (%)
true	9339	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

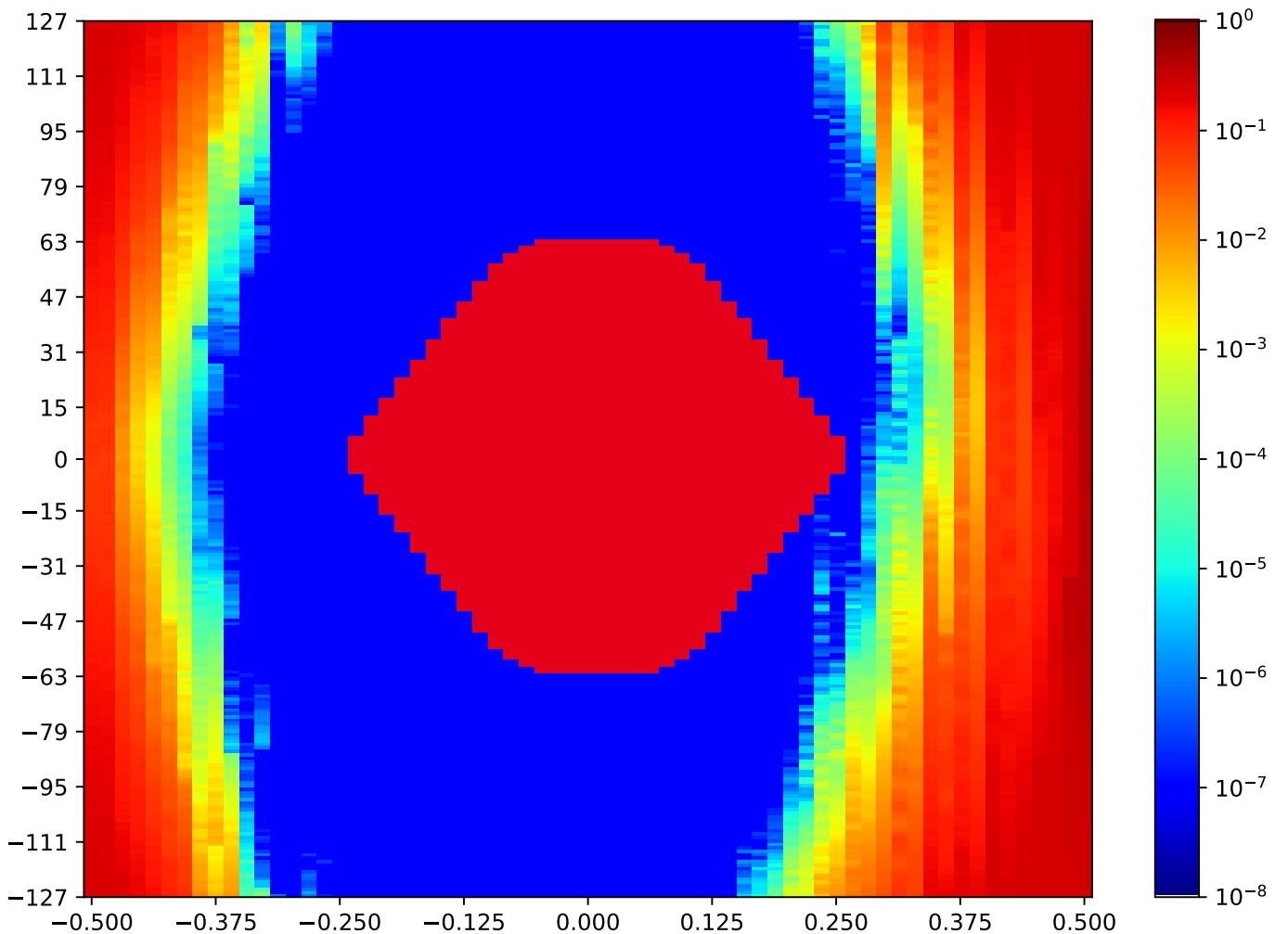


Figure 5.167: MSP_C_FPGA-TX4-00-RX9-00-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.2 MSP_C_FPGA-TX4-01-RX9-01-MSP_A_FPGA

Table 5.155: MSP_C_FPGA-TX4-01-RX9-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:24:30		2018-Sep-27 16:24:51	
Reset RX	OA	HO		VO	VO (%)
true	8470	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

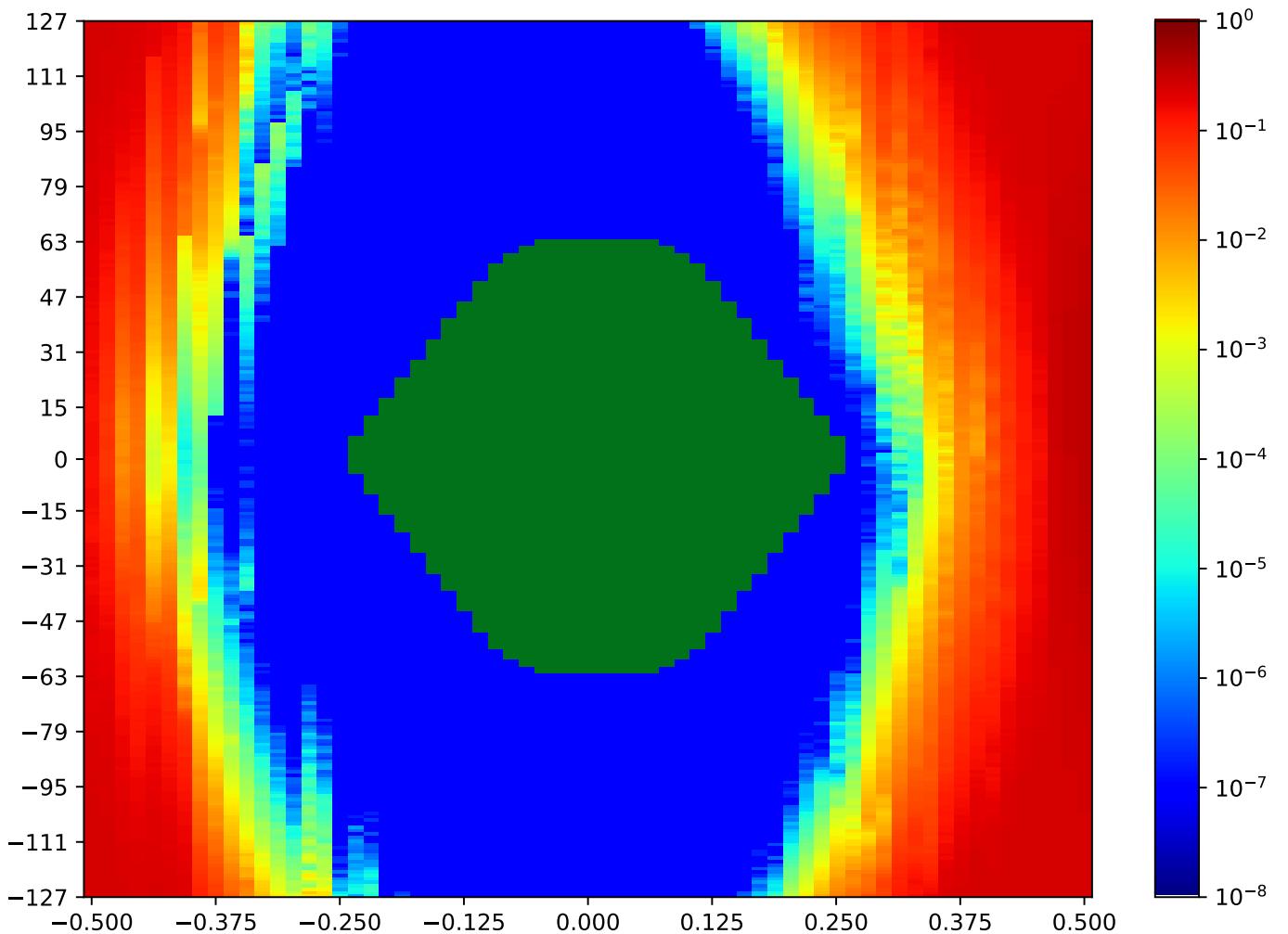


Figure 5.168: MSP_C_FPGA-TX4-01-RX9-01-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.3 MSP_C_FPGA-TX4-02-RX9-02-MSP_A_FPGA

Table 5.156: MSP_C_FPGA-TX4-02-RX9-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:26:18		2018-Sep-27 16:26:39	
Reset RX	OA	HO		VO	VO (%)
true	8330	41		248	96.86%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

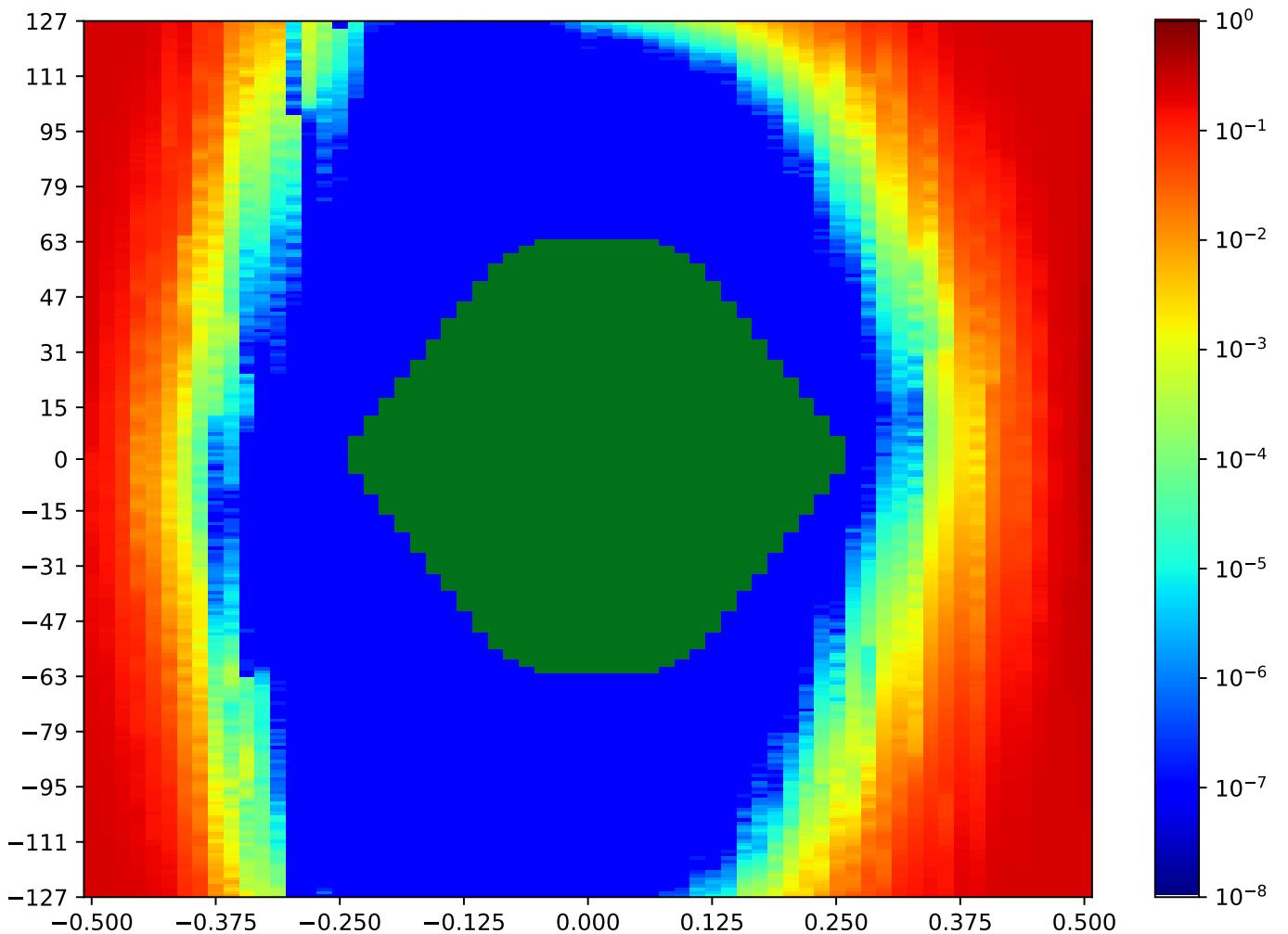


Figure 5.169: MSP_C_FPGA-TX4-02-RX9-02-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.4 MSP_C_FPGA-TX4-03-RX9-03-MSP_A_FPGA

Table 5.157: MSP_C_FPGA-TX4-03-RX9-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:24:10		2018-Sep-27 16:24:30	
Reset RX	OA	HO		VO	VO (%)
true	9080	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

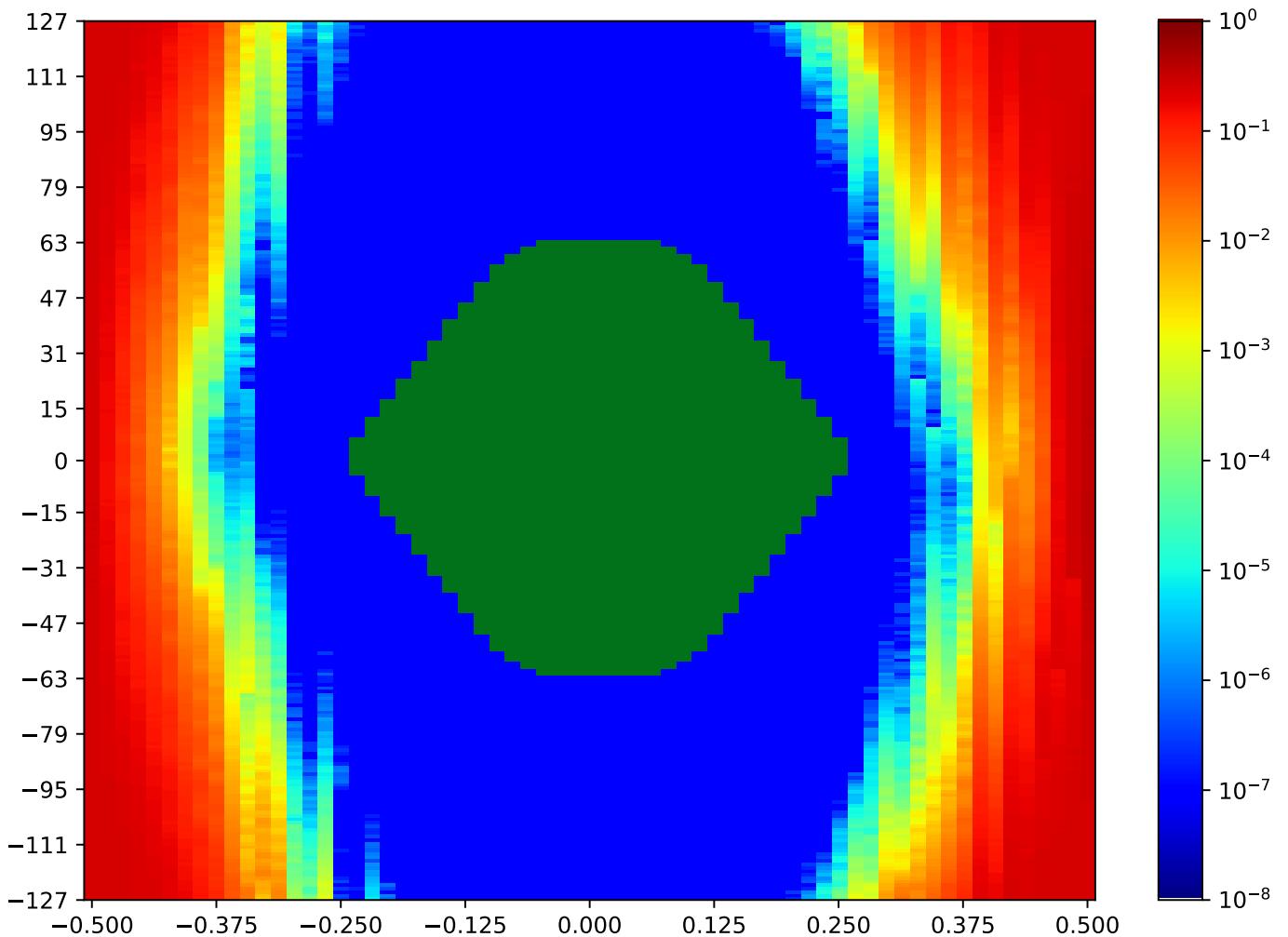


Figure 5.170: MSP_C_FPGA-TX4-03-RX9-03-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.5 MSP_C_FPGA-TX4-04-RX9-04-MSP_A_FPGA

Table 5.158: MSP_C_FPGA-TX4-04-RX9-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:27:20		2018-Sep-27 16:27:40	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8626	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

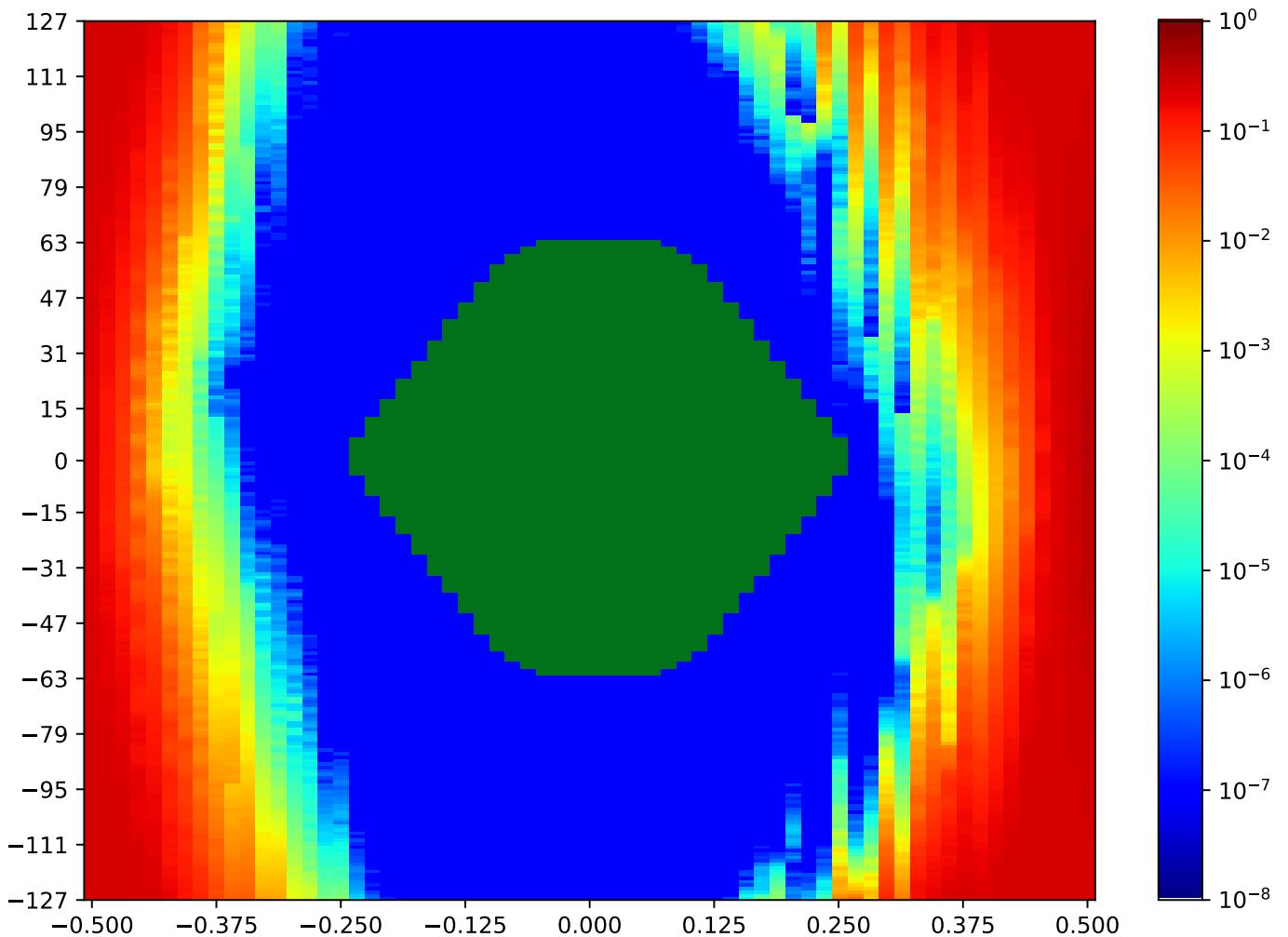


Figure 5.171: MSP_C_FPGA-TX4-04-RX9-04-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.6 MSP_C_FPGA-TX4-05-RX9-05-MSP_A_FPGA

Table 5.159: MSP_C_FPGA-TX4-05-RX9-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:24:51		2018-Sep-27 16:25:11	
Reset RX	OA	HO		VO	VO (%)
true	8840	43		64.62%	254 99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

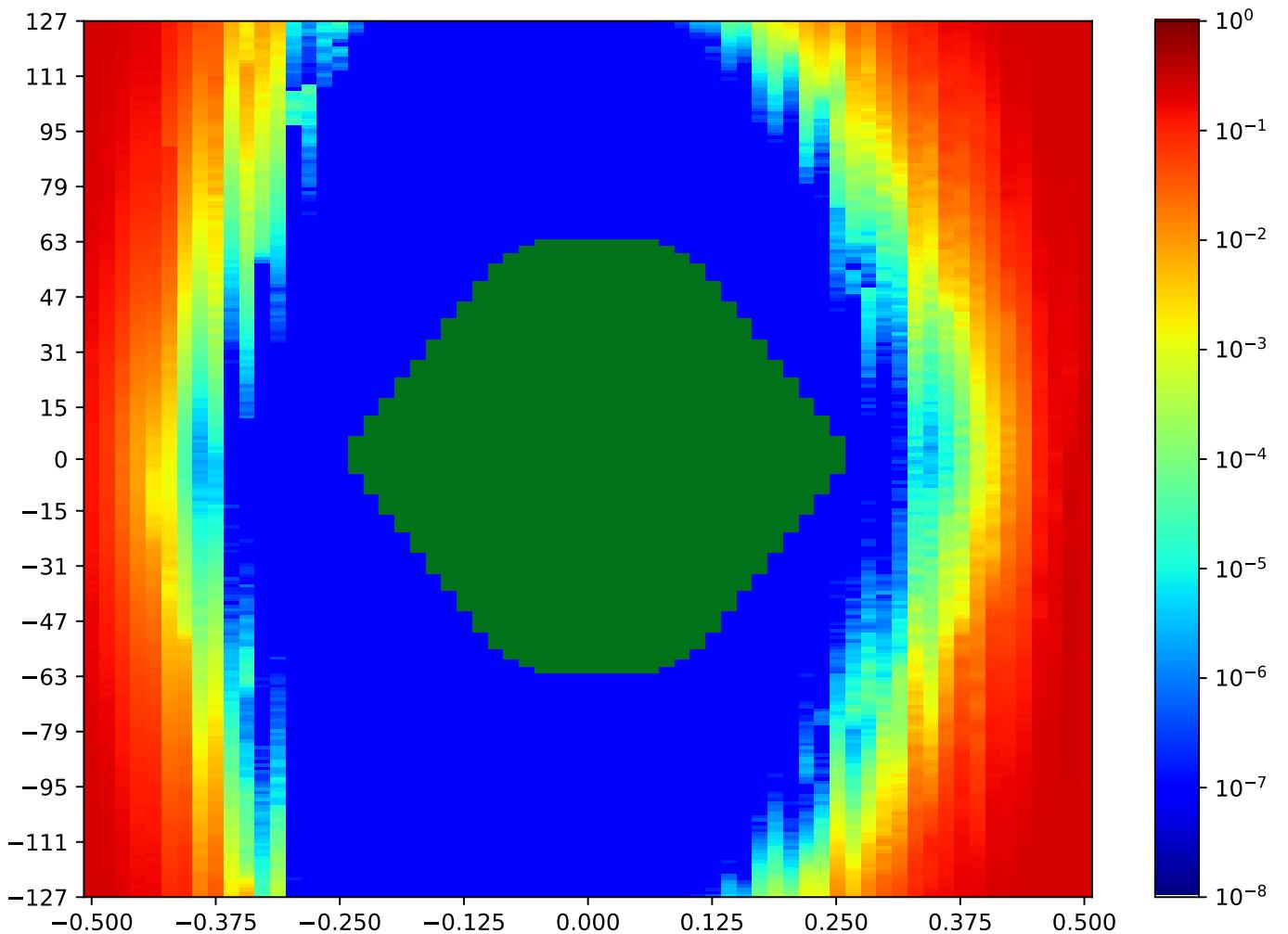


Figure 5.172: MSP_C_FPGA-TX4-05-RX9-05-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.7 MSP_C_FPGA-TX4-06-RX9-06-MSP_A_FPGA

Table 5.160: MSP_C_FPGA-TX4-06-RX9-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:28:01		2018-Sep-27 16:28:22	
Reset RX	OA	HO		VO	VO (%)
true	8832	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

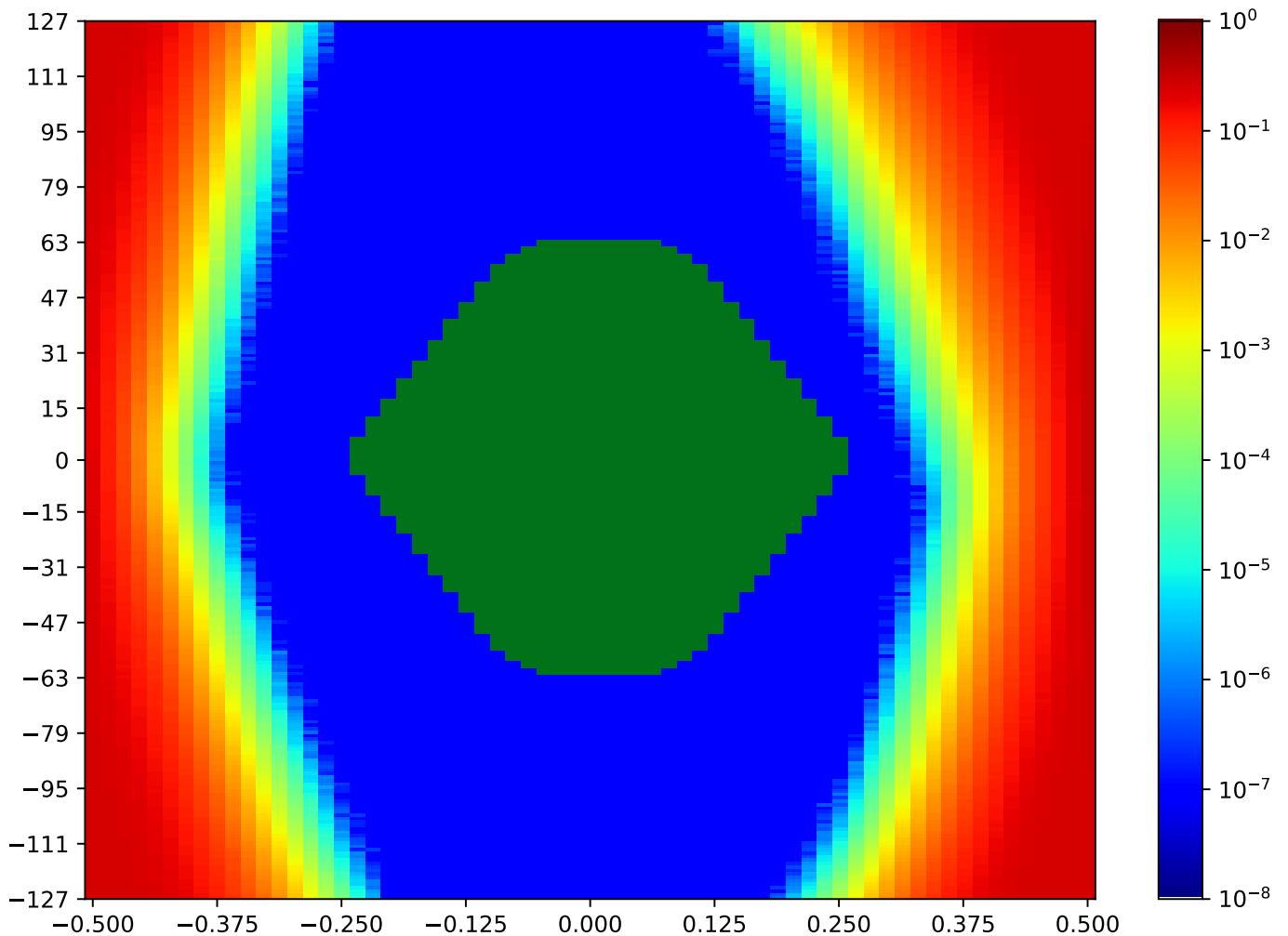


Figure 5.173: MSP_C_FPGA-TX4-06-RX9-06-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.8 MSP_C_FPGA-TX4-07-RX9-07-MSP_A_FPGA

Table 5.161: MSP_C_FPGA-TX4-07-RX9-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:25:38		2018-Sep-27 16:25:58	
Reset RX	OA	HO		VO	VO (%)
true	9755	47		70.77%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

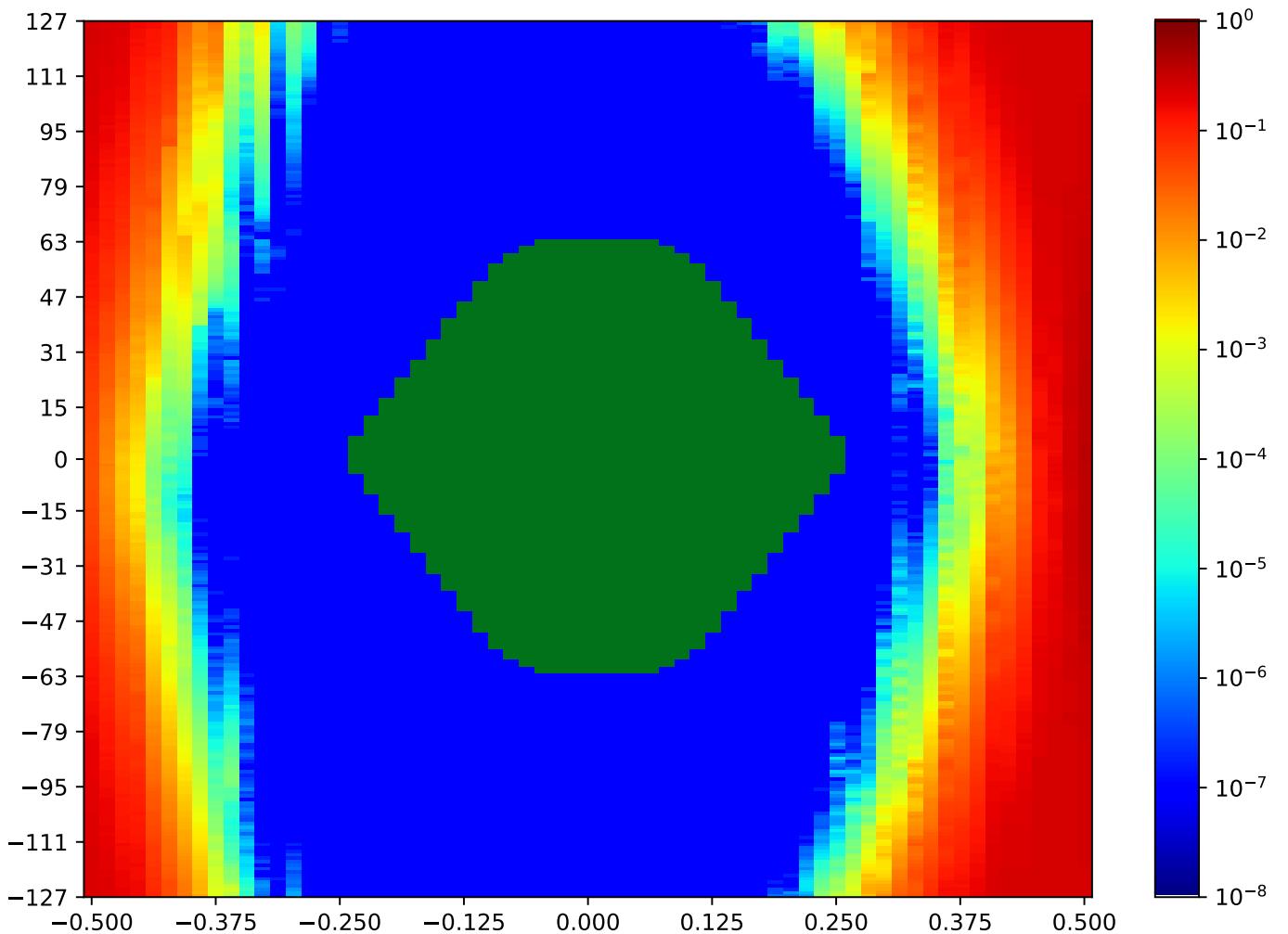


Figure 5.174: MSP_C_FPGA-TX4-07-RX9-07-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.9 MSP_C_FPGA-TX4-08-RX9-08-MSP_A_FPGA

Table 5.162: MSP_C_FPGA-TX4-08-RX9-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:27:40		2018-Sep-27 16:28:01	
Reset RX	OA	HO		VO	VO (%)
true	9128	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

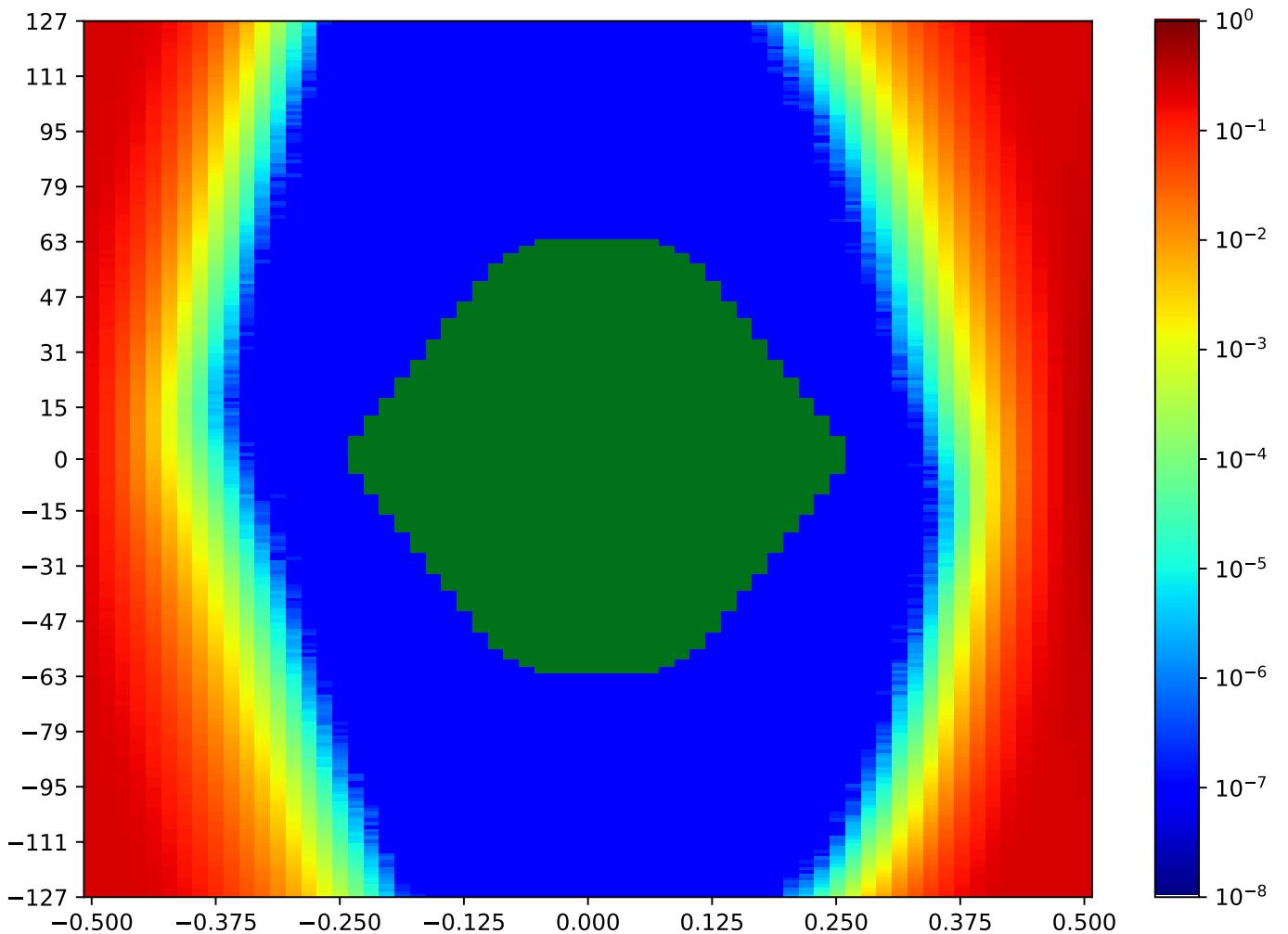


Figure 5.175: MSP_C_FPGA-TX4-08-RX9-08-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.10 MSP_C_FPGA-TX4-09-RX9-09-MSP_A_FPGA

Table 5.163: MSP_C_FPGA-TX4-09-RX9-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:25:58		2018-Sep-27 16:26:18	
Reset RX	OA	HO		VO	VO (%)
true	8896	40		61.54%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

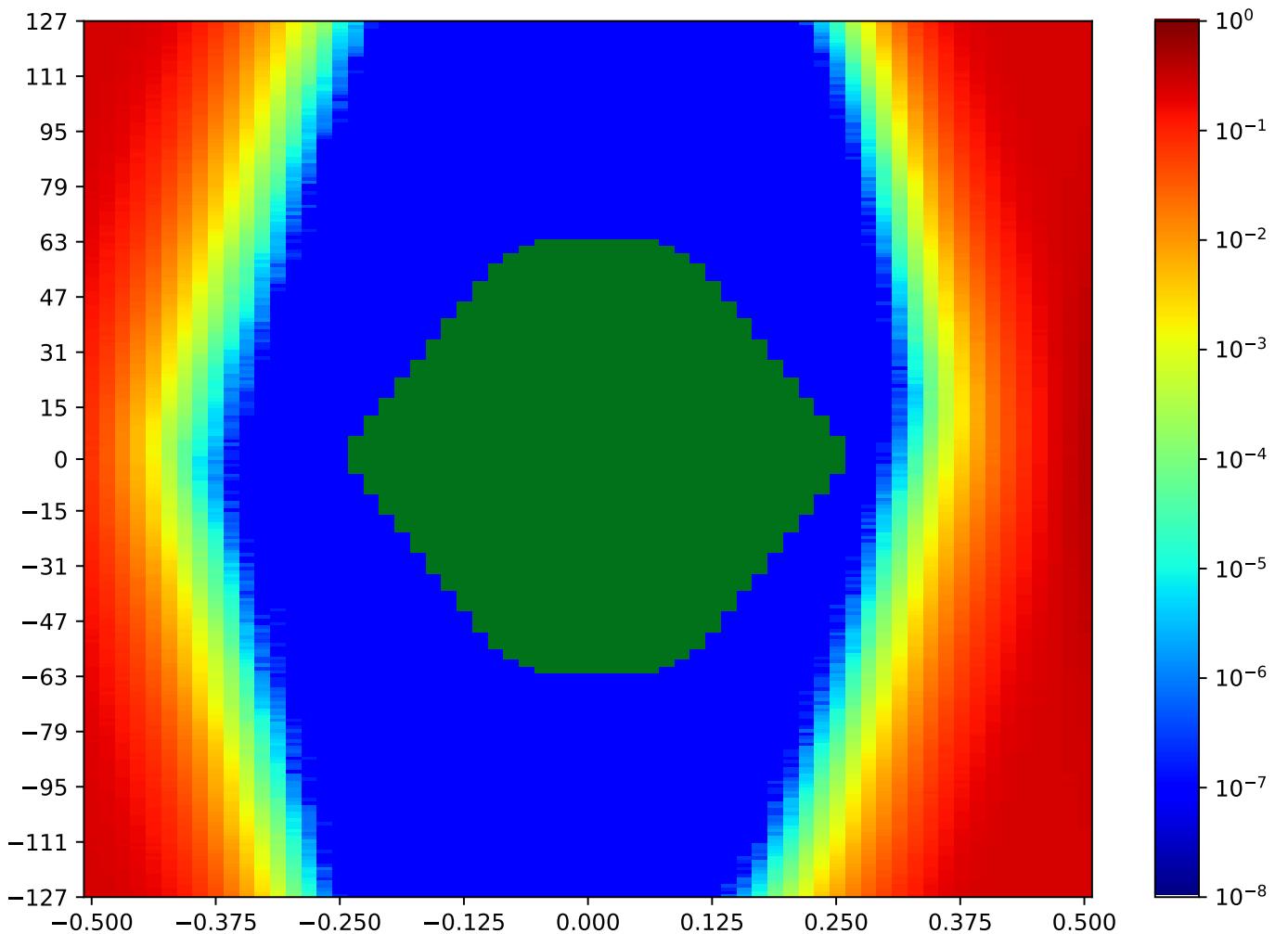


Figure 5.176: MSP_C_FPGA-TX4-09-RX9-09-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.11 MSP_C_FPGA-TX4-10-RX9-10-MSP_A_FPGA

Table 5.164: MSP_C_FPGA-TX4-10-RX9-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:27:00		2018-Sep-27 16:27:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8668	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

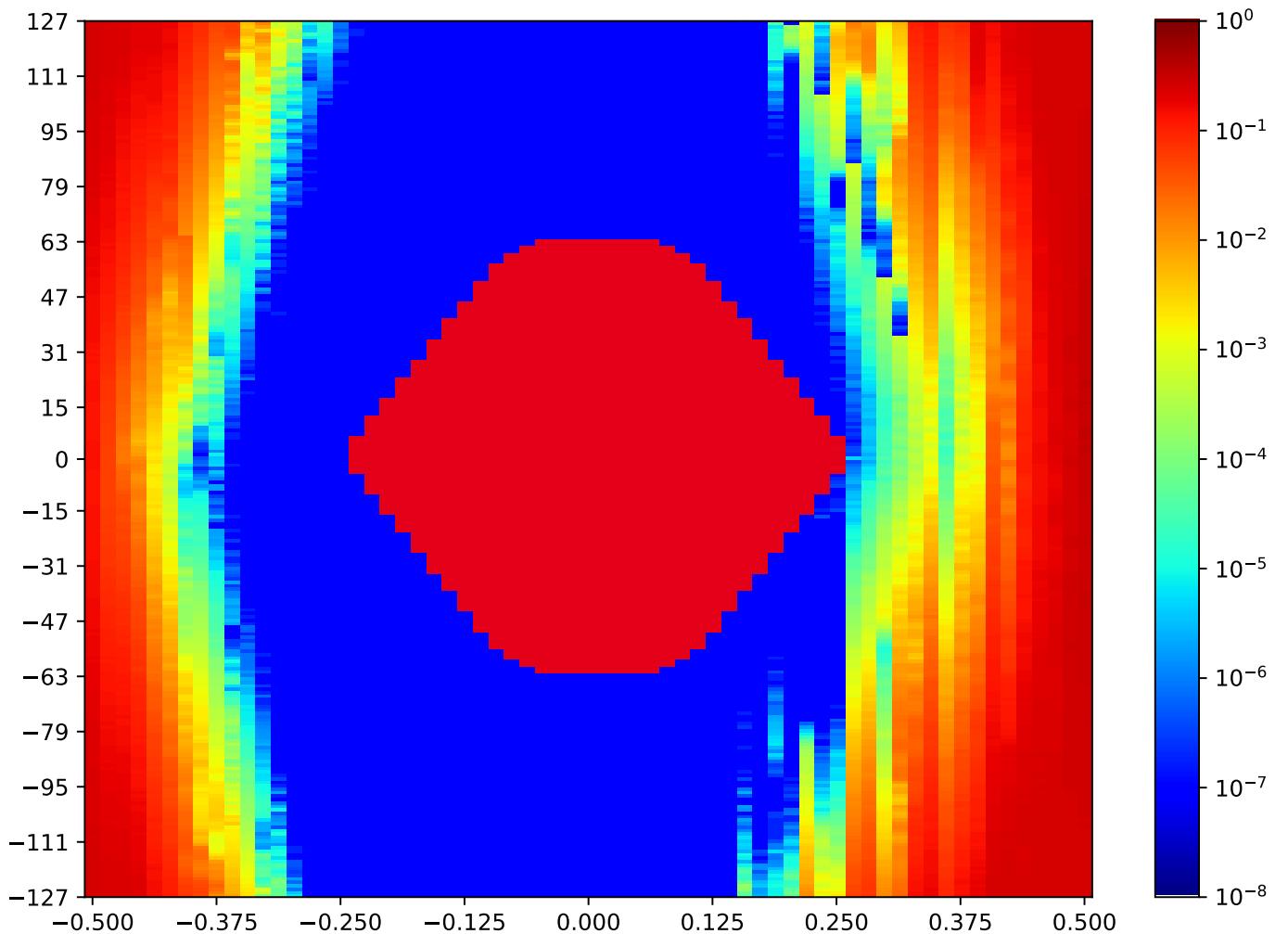


Figure 5.177: MSP_C_FPGA-TX4-10-RX9-10-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.13.12 MSP_C_FPGA-TX4-11-RX9-11-MSP_A_FPGA

Table 5.165: MSP_C_FPGA-TX4-11-RX9-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:26:39		2018-Sep-27 16:26:59	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9855	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

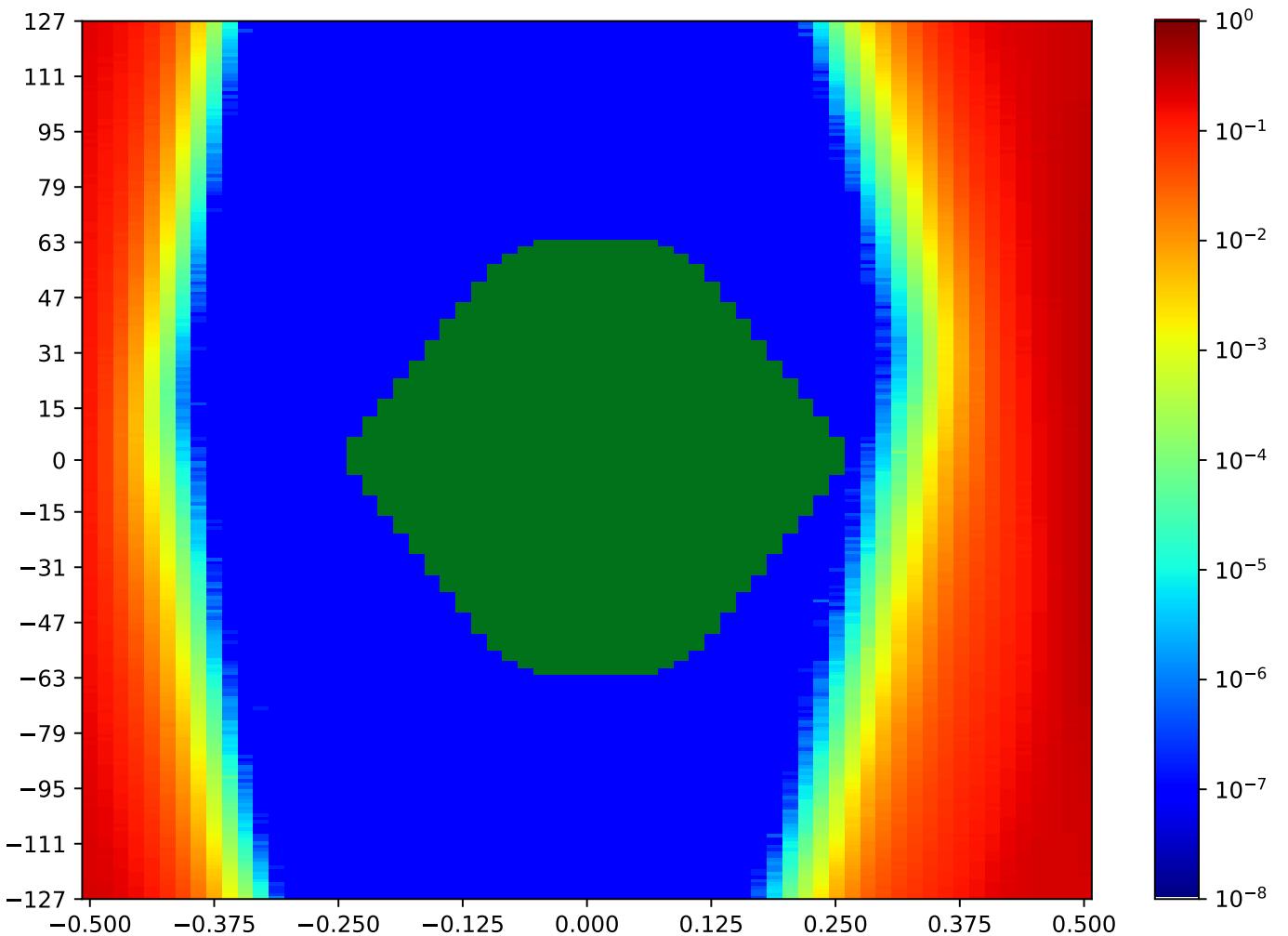


Figure 5.178: MSP_C_FPGA-TX4-11-RX9-11-MSP_A_FPGA

Call back to summary Figure 5.166. Sibling eye diagrams: V2-6.4.

5.14 Partial TRP TX5 MSP_C RX14 Minipod Loopback

A cross-reference to Figure 5.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.
Next summary Figure 5.188.

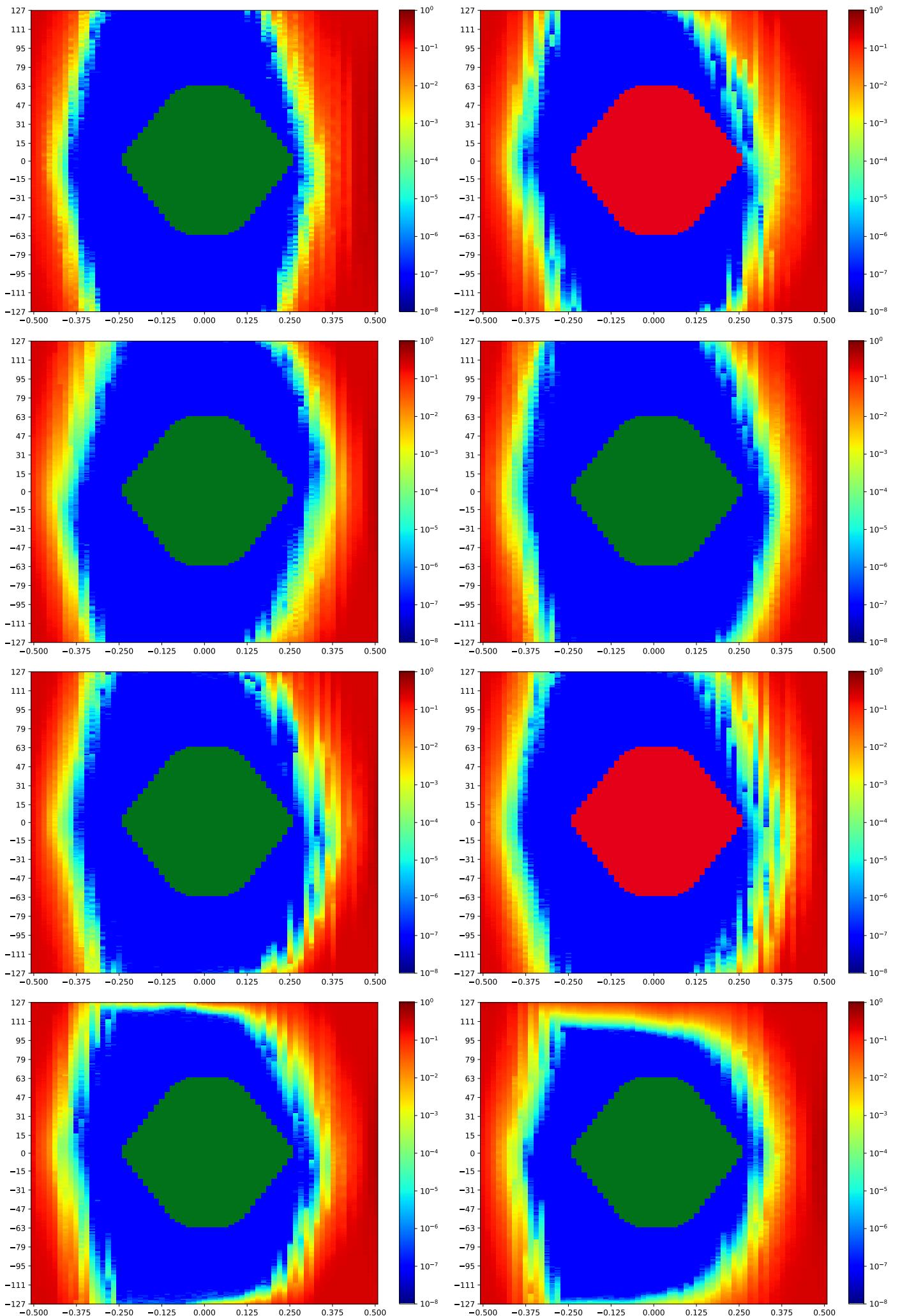


Figure 5.179: Partial TRP TX5 MSP_C RX14 Minipod Loopback
1092

5.14.1 TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

Table 5.166: TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:29:23		2018-Sep-27 16:29:44	
Reset RX	OA	HO		VO	VO (%)
true	9168	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

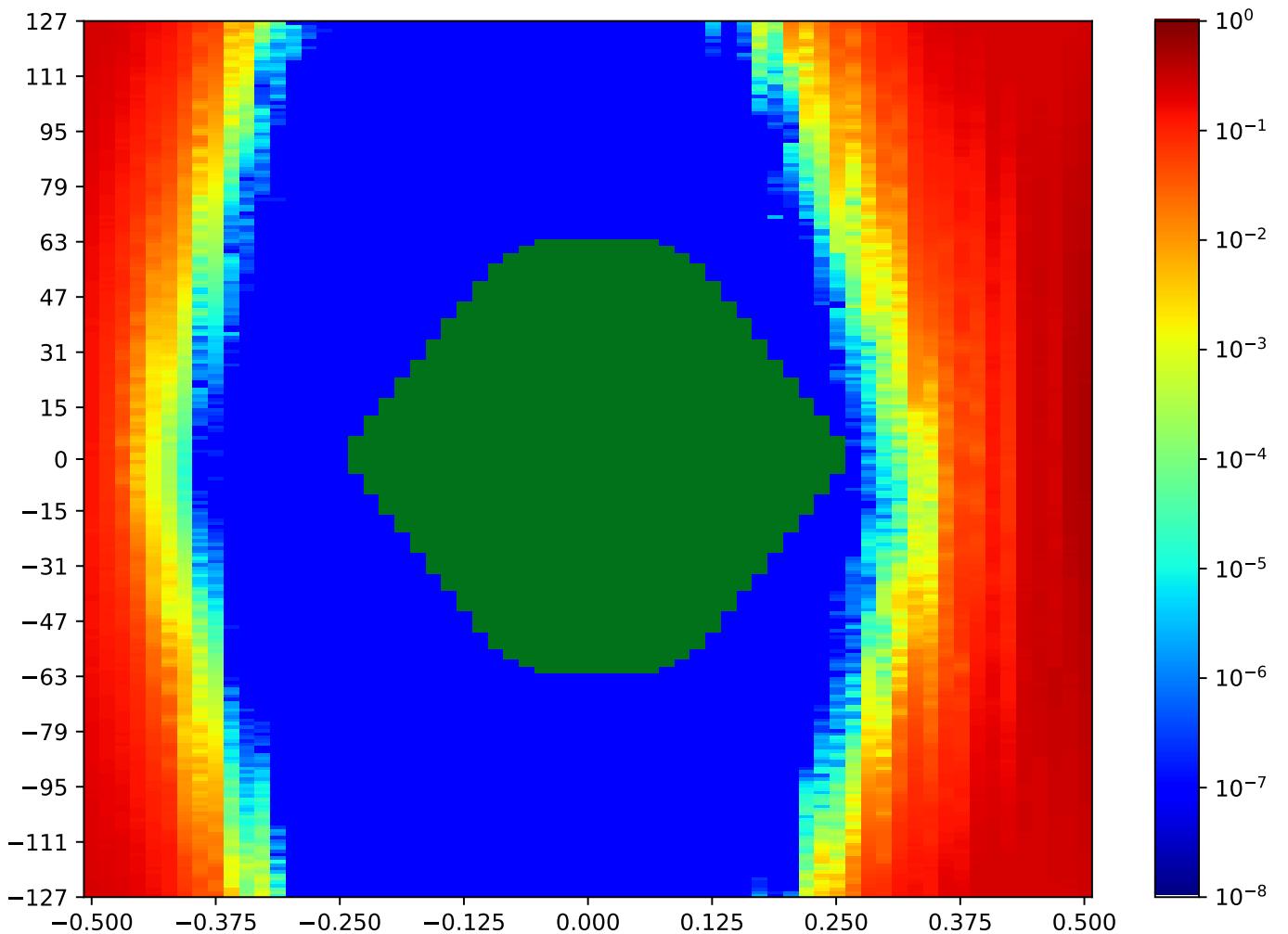


Figure 5.180: TRP_FPGA-TX5-00-RX14-00-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.14.2 TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

Table 5.167: TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:28:43		2018-Sep-27 16:29:03	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8044	37	56.92%	255	99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

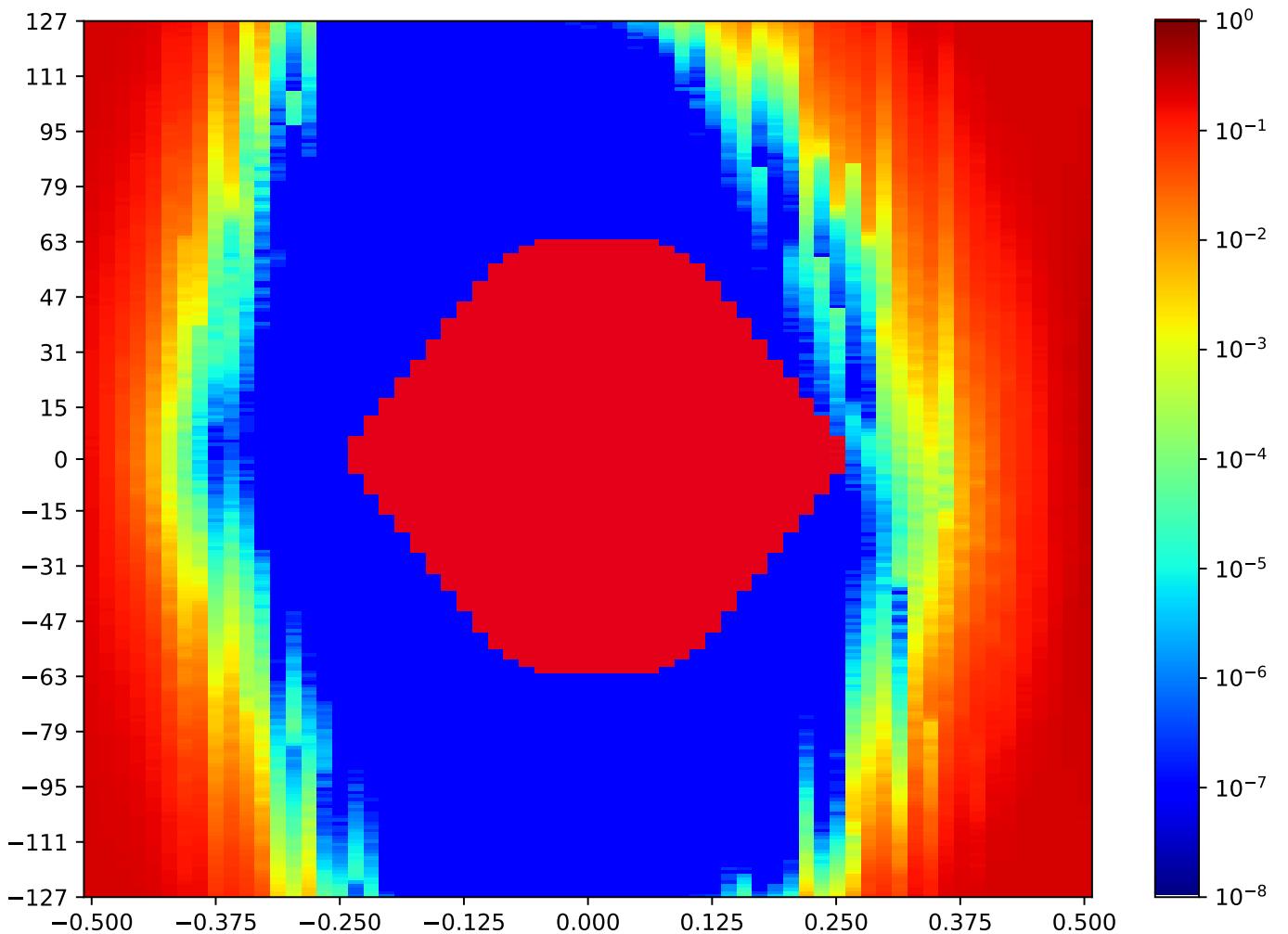


Figure 5.181: TRP_FPGA-TX5-01-RX14-01-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.14.3 TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

Table 5.168: TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:30:04		2018-Sep-27 16:30:25	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8999	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

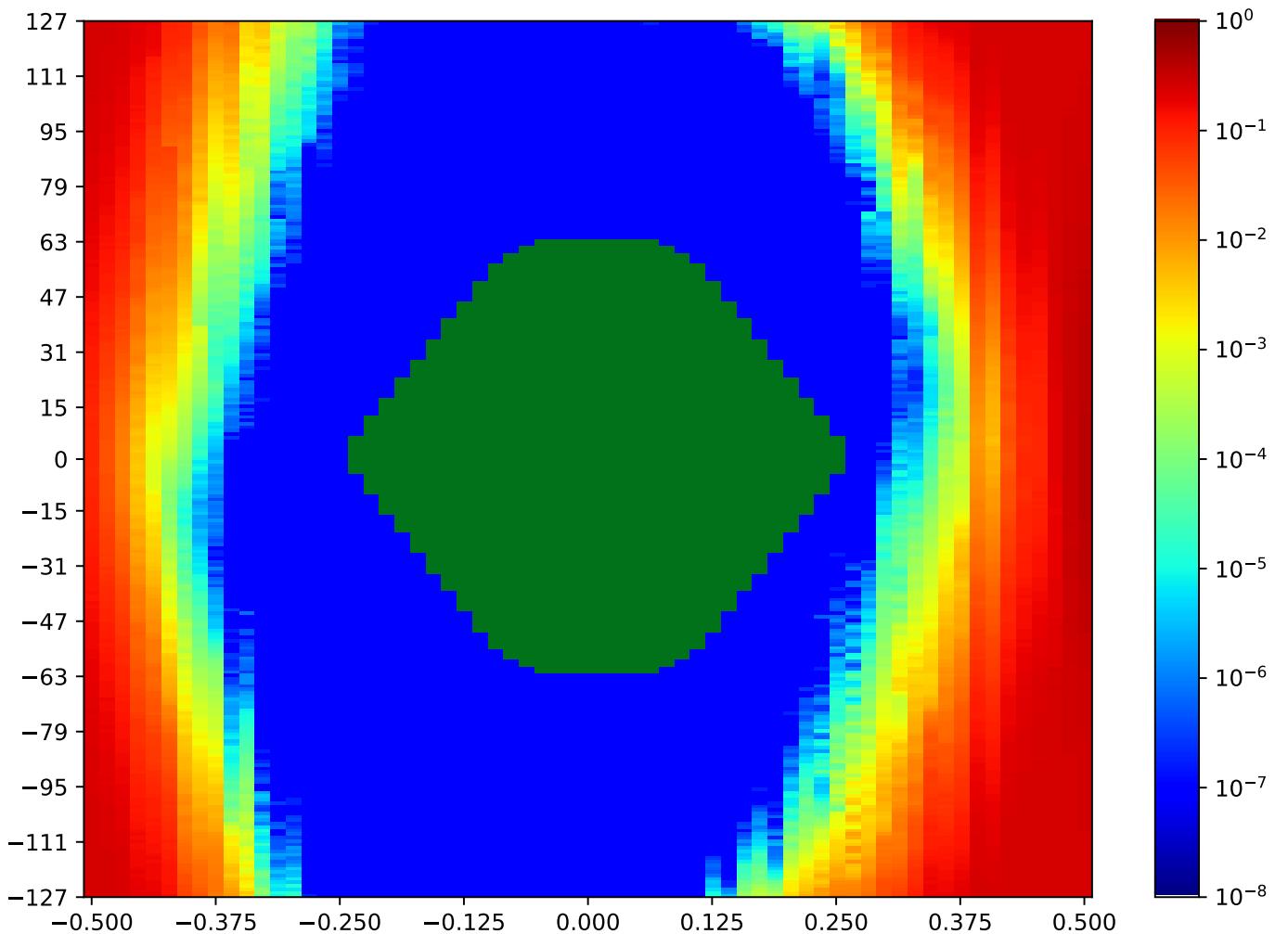


Figure 5.182: TRP_FPGA-TX5-02-RX14-02-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.14.4 TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

Table 5.169: TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:29:03		2018-Sep-27 16:29:23	
Reset RX	OA	HO		VO	VO (%)
true	9217	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

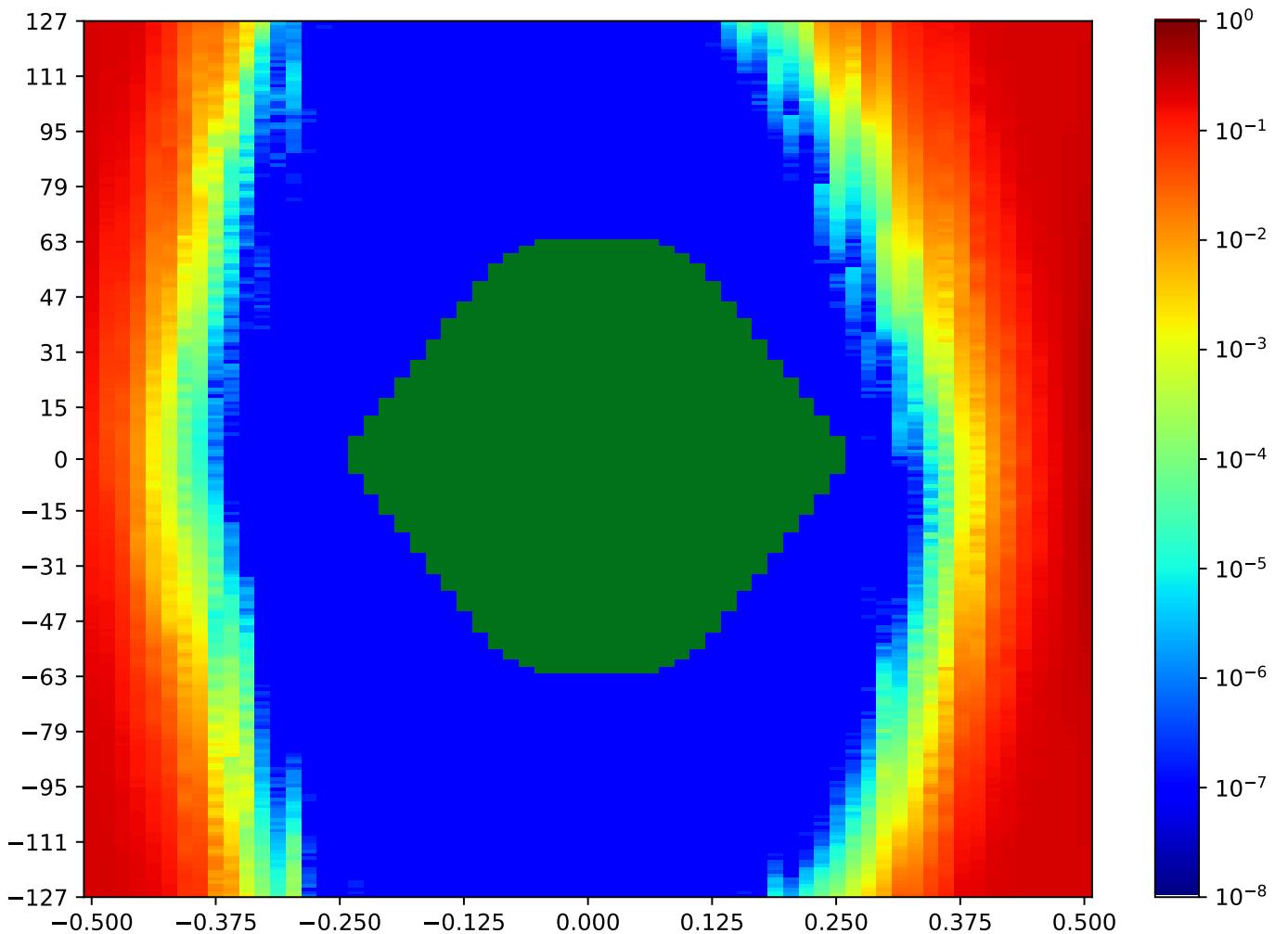


Figure 5.183: TRP_FPGA-TX5-03-RX14-03-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.14.5 TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

Table 5.170: TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:30:45		2018-Sep-27 16:31:05	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8631	41	61.54%	248	97.25%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

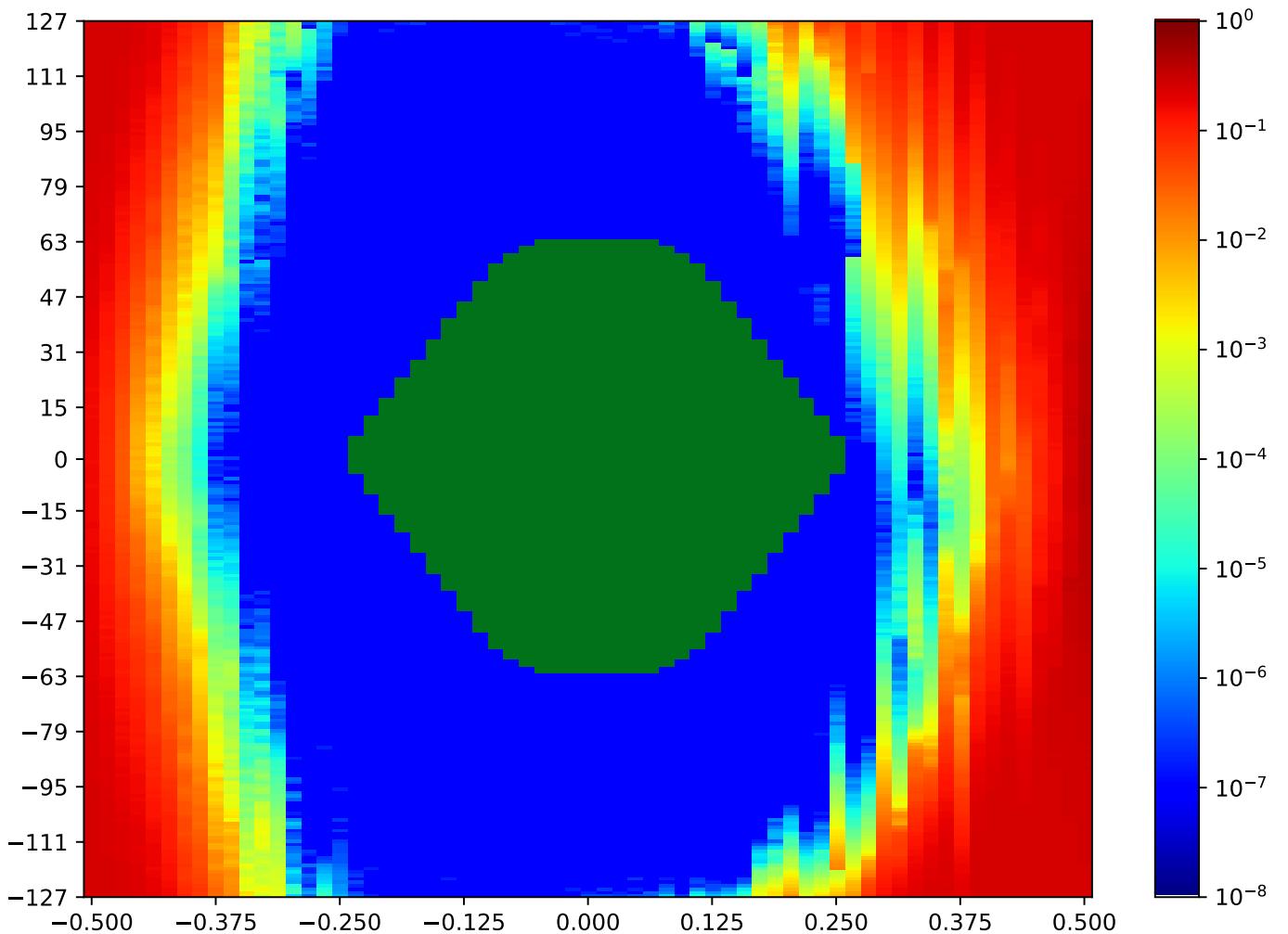


Figure 5.184: TRP_FPGA-TX5-04-RX14-04-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.14.6 TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

Table 5.171: TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:28:22		2018-Sep-27 16:28:43	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8697	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

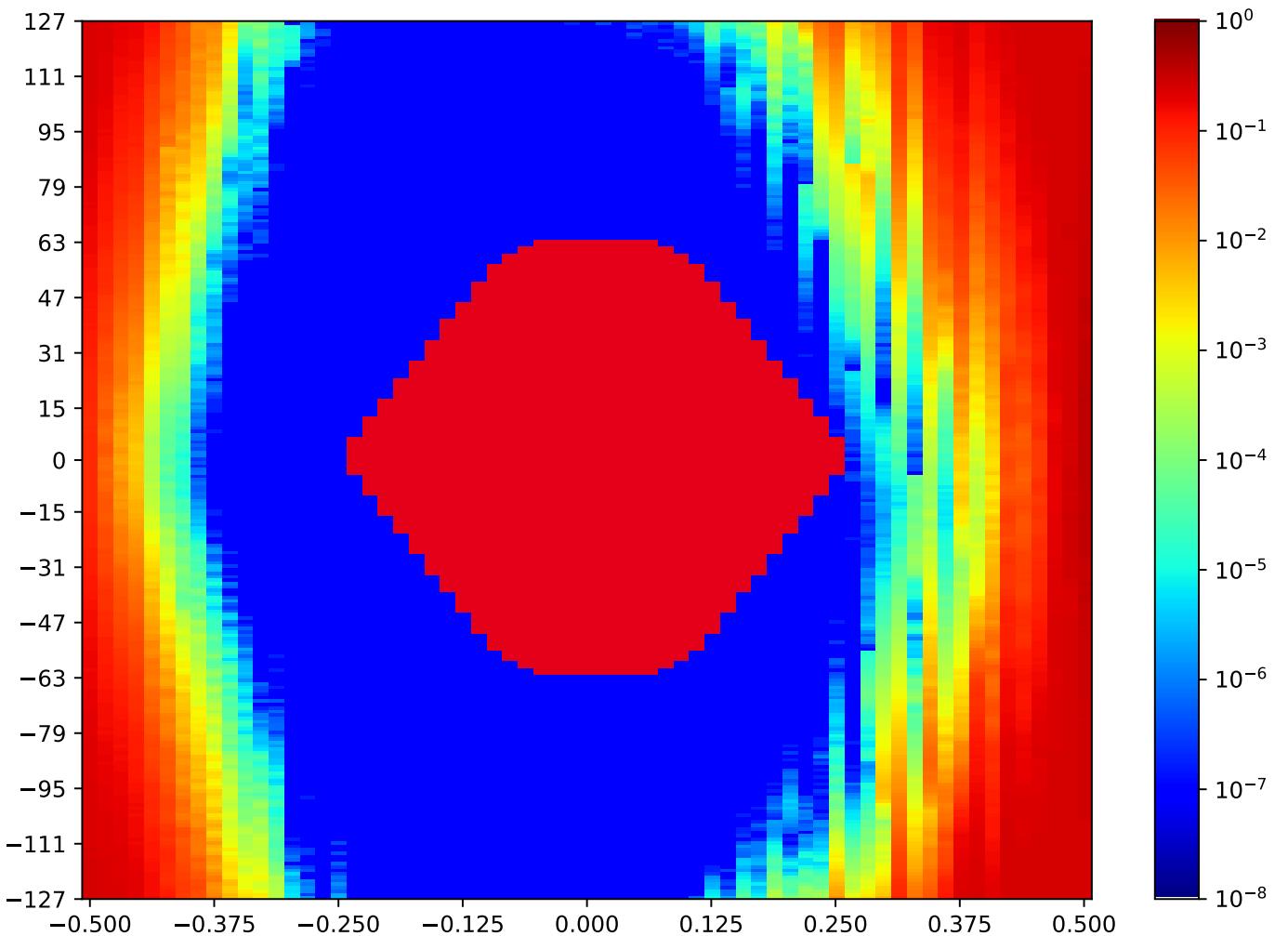


Figure 5.185: TRP_FPGA-TX5-05-RX14-05-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.14.7 TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

Table 5.172: TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:29:44		2018-Sep-27 16:30:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	7847	42	63.08%	229	89.80%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

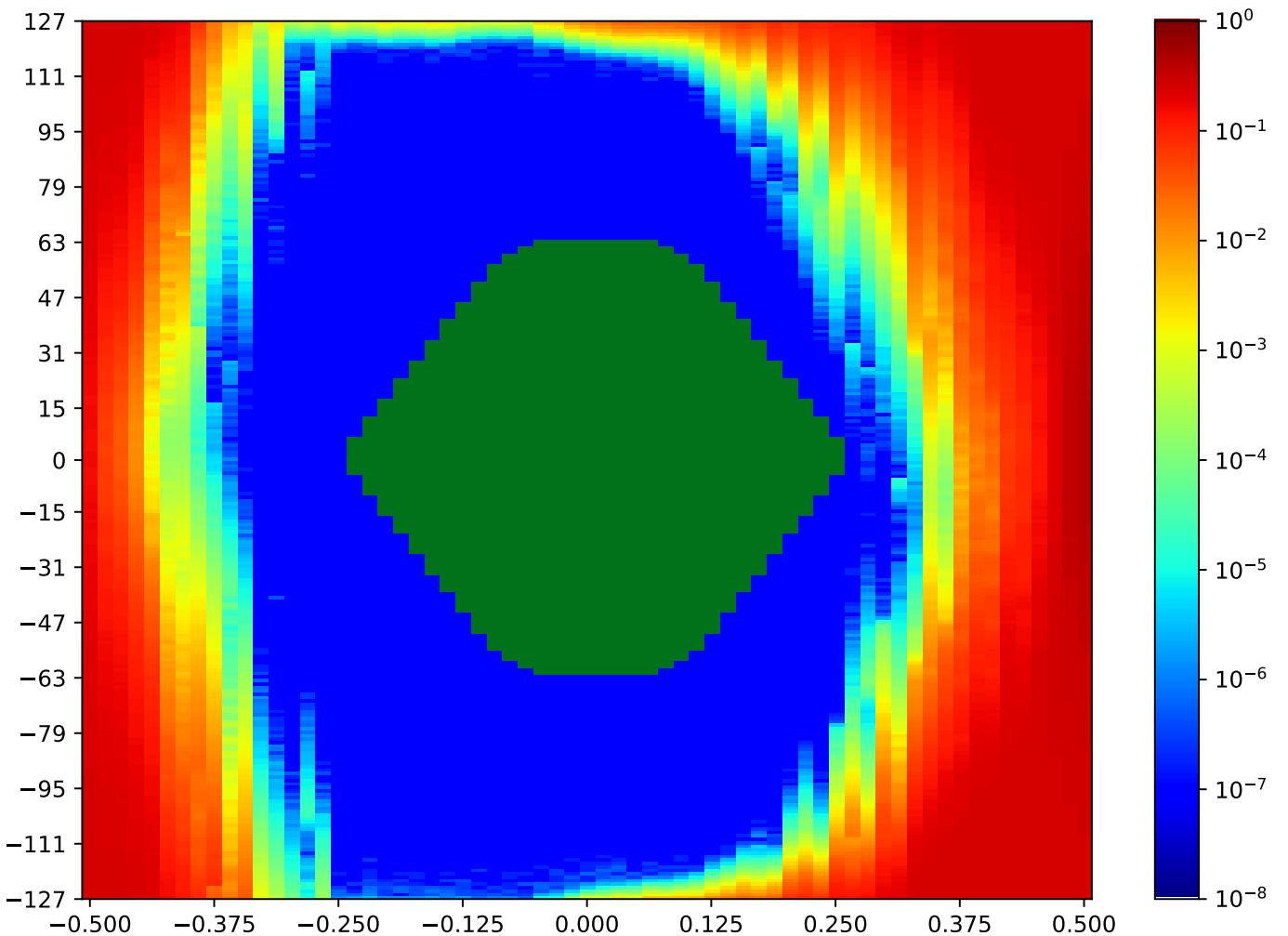


Figure 5.186: TRP_FPGA-TX5-06-RX14-06-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.14.8 TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

Table 5.173: TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 16:30:25		2018-Sep-27 16:30:45	
Reset RX	OA	HO		VO	VO (%)
true	7261	40		61.54%	215 84.31%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

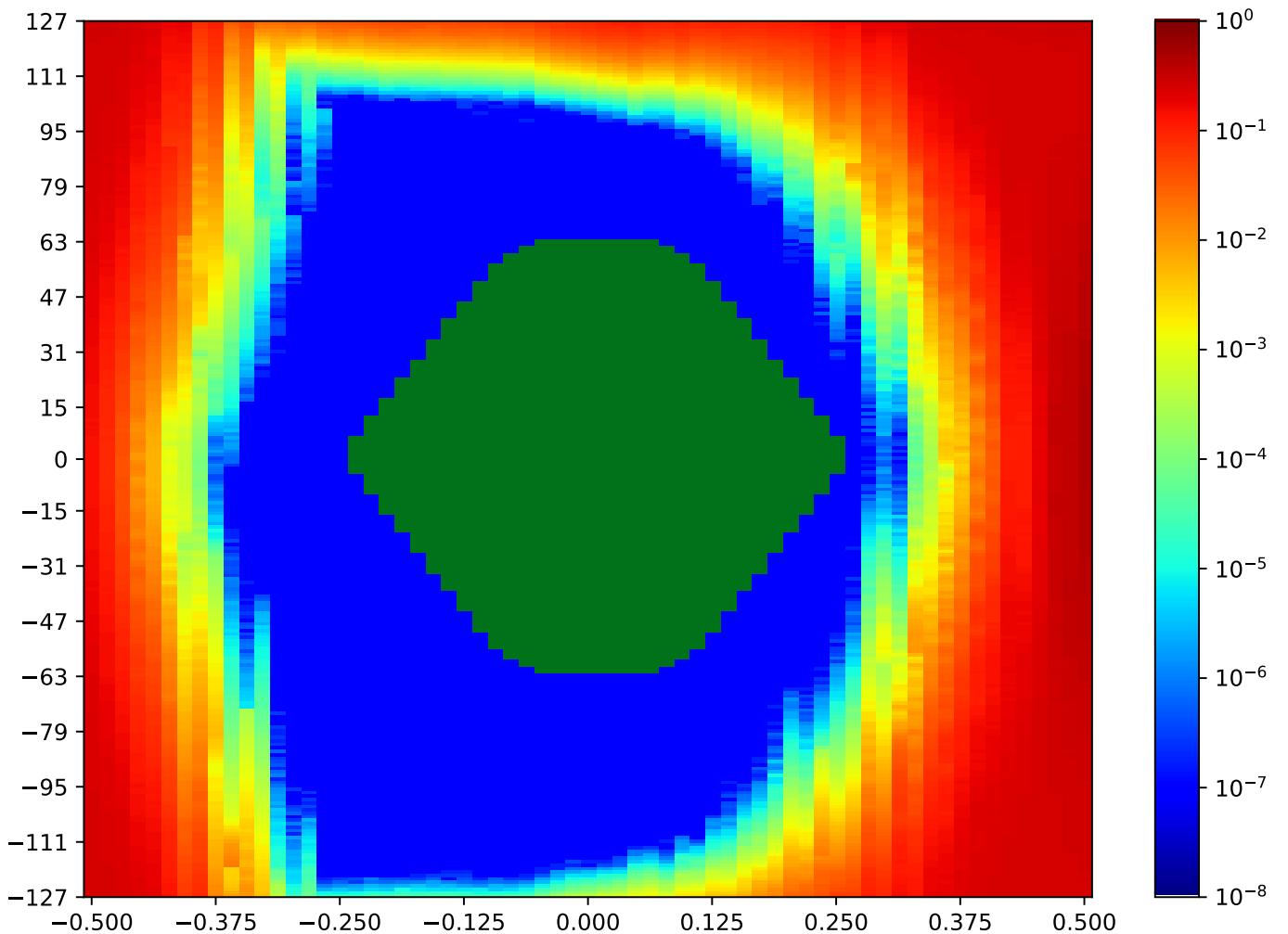


Figure 5.187: TRP_FPGA-TX5-07-RX14-07-MSP_C_FPGA

Call back to summary Figure 5.179. Sibling eye diagrams: V1-6.4, V1-12.8, V2-6.4.

5.15 MSP_A TX1 MSP_C RX10 Minipod Loopback

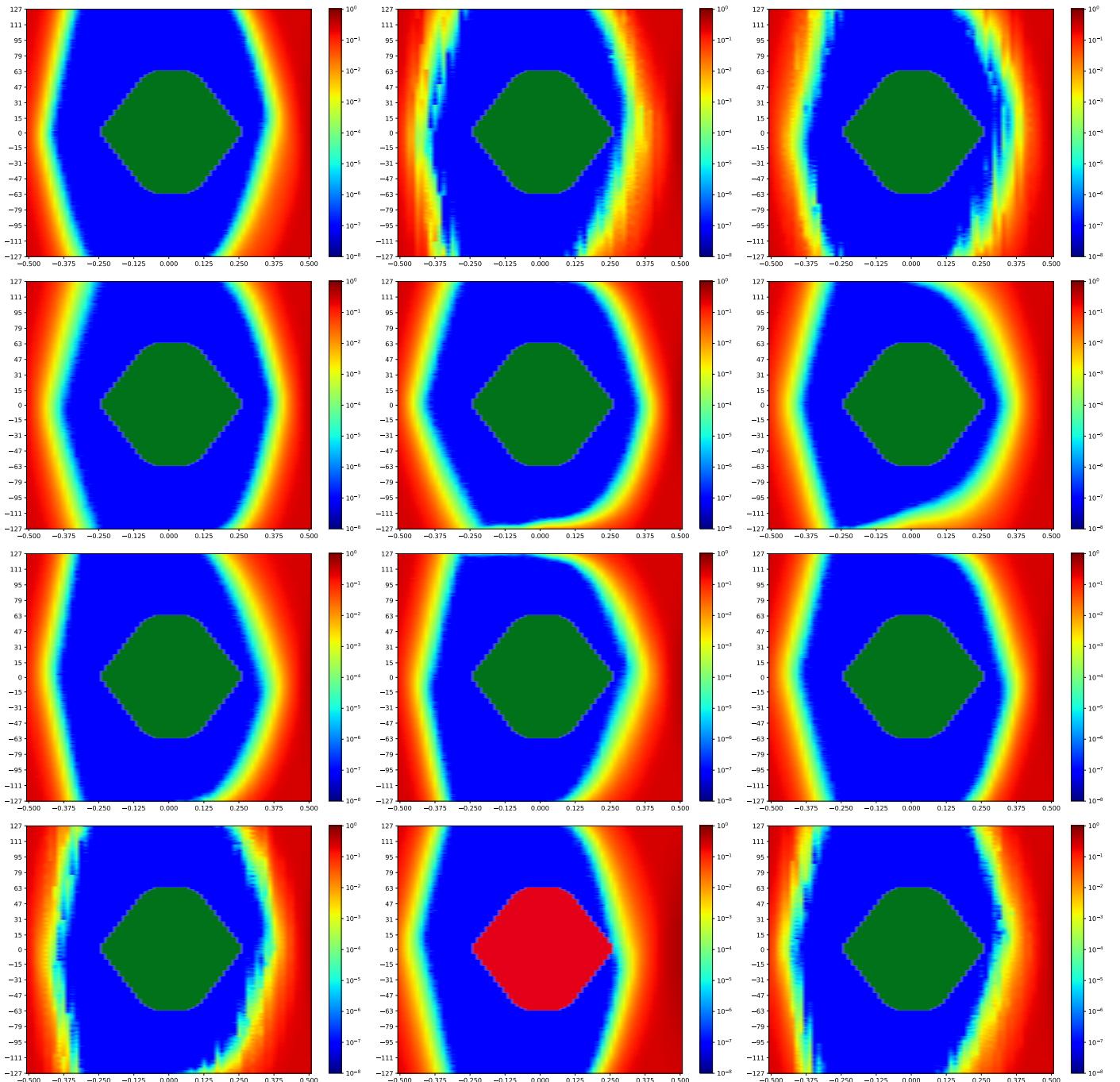


Figure 5.188: MSP_A TX1 MSP_C RX10 Minipod Loopback

A cross-reference to Figure 5.188. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.201.

5.15.1 MSP_A_FPGA-TX1-00-RX10-00-MSP_C_FPGA

Table 5.174: MSP_A_FPGA-TX1-00-RX10-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:44:03		2018-Sep-27 15:44:23	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9981	46	70.77%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

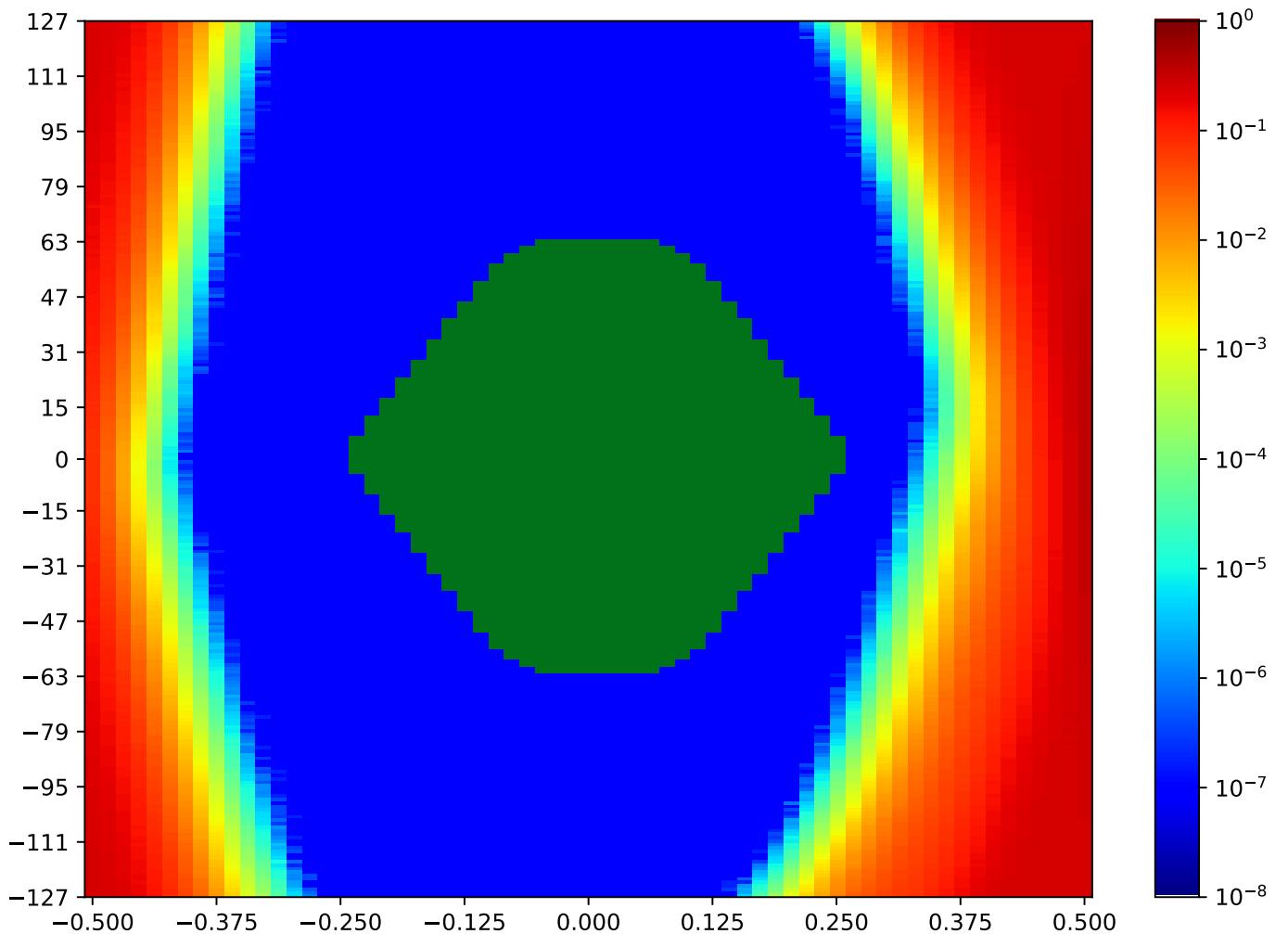


Figure 5.189: MSP_A_FPGA-TX1-00-RX10-00-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.2 MSP_A_FPGA-TX1-01-RX10-01-MSP_C_FPGA

Table 5.175: MSP_A_FPGA-TX1-01-RX10-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:44:44		2018-Sep-27 15:45:04	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8863	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

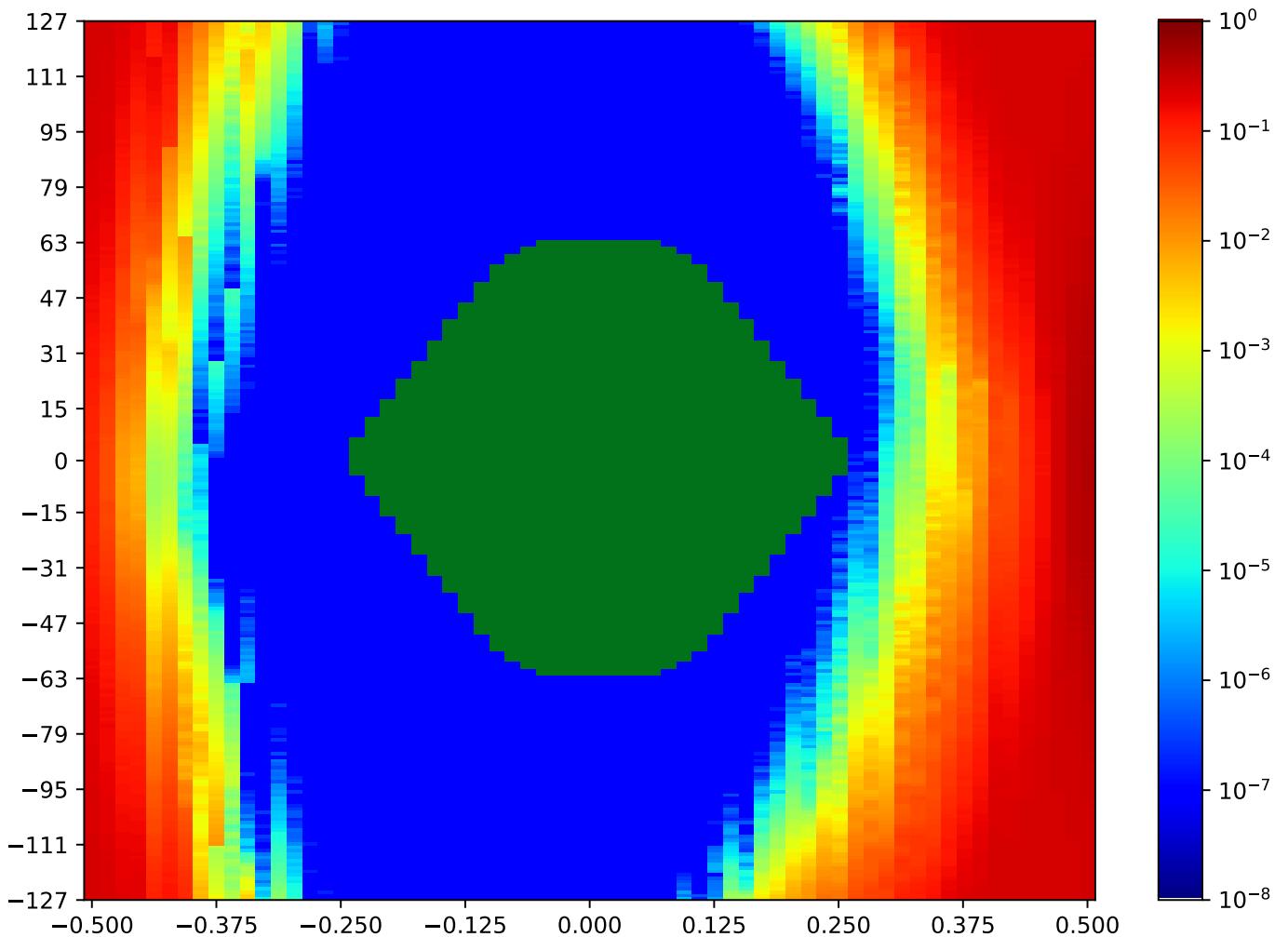


Figure 5.190: MSP_A_FPGA-TX1-01-RX10-01-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.3 MSP_A_FPGA-TX1-02-RX10-02-MSP_C_FPGA

Table 5.176: MSP_A_FPGA-TX1-02-RX10-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:45:04		2018-Sep-27 15:45:24	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8913	43	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

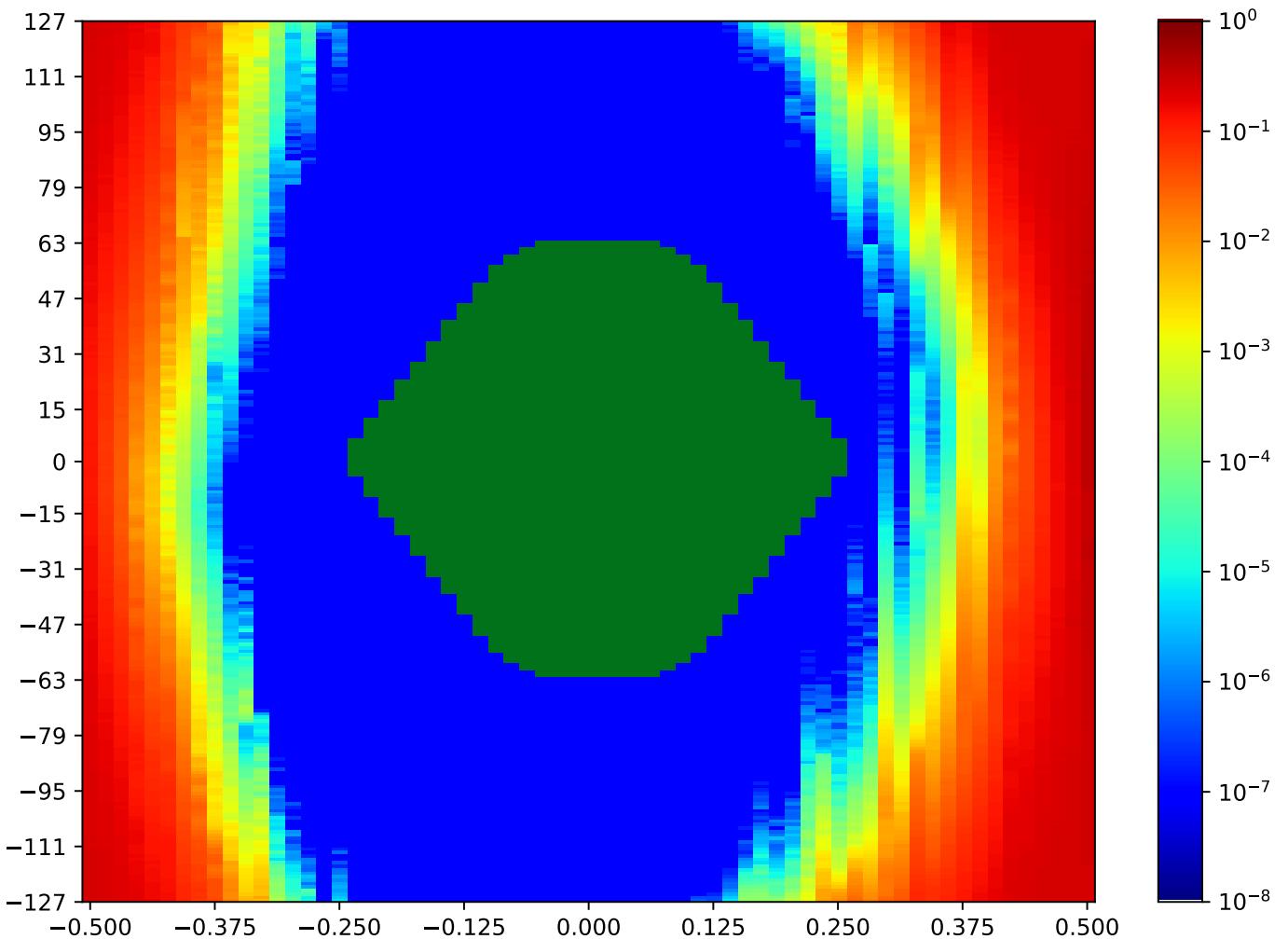


Figure 5.191: MSP_A_FPGA-TX1-02-RX10-02-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.4 MSP_A_FPGA-TX1-03-RX10-03-MSP_C_FPGA

Table 5.177: MSP_A_FPGA-TX1-03-RX10-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:43:23		2018-Sep-27 15:43:43	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9420	46		69.23%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

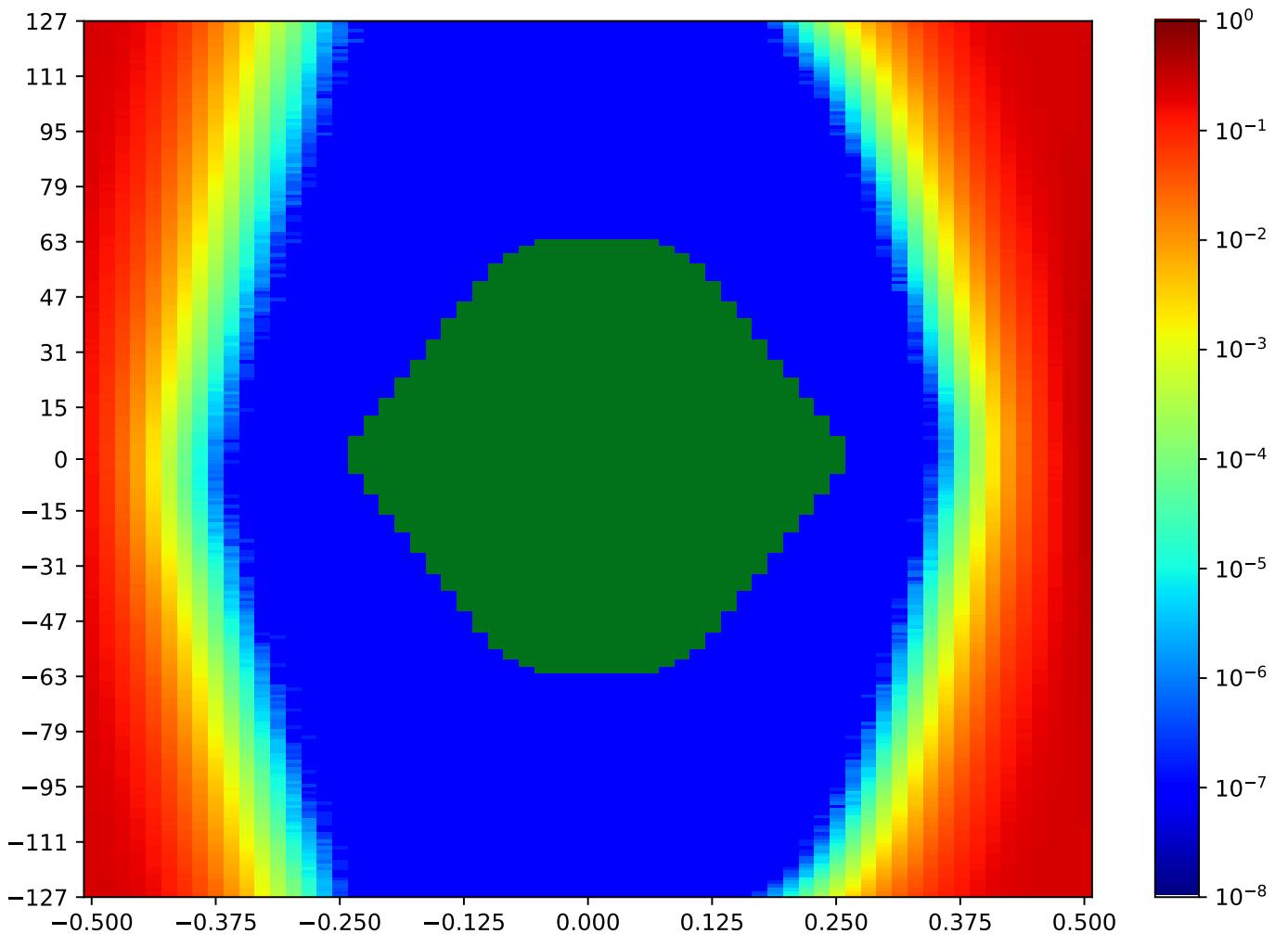


Figure 5.192: MSP_A_FPGA-TX1-03-RX10-03-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.5 MSP_A_FPGA-TX1-04-RX10-04-MSP_C_FPGA

Table 5.178: MSP_A_FPGA-TX1-04-RX10-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:46:10		2018-Sep-27 15:46:30	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8789	46	70.77%	242	94.90%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

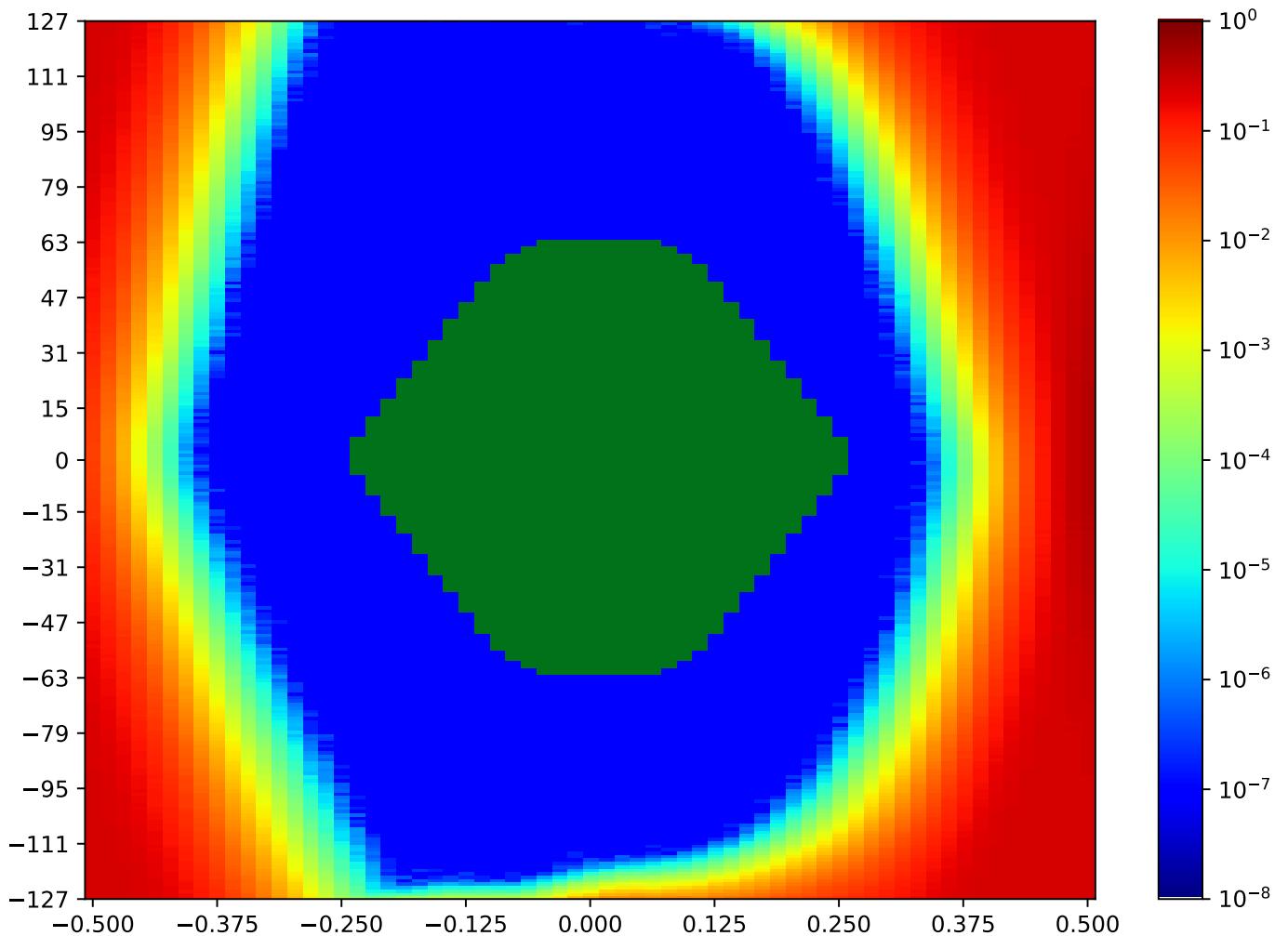


Figure 5.193: MSP_A_FPGA-TX1-04-RX10-04-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.6 MSP_A_FPGA-TX1-05-RX10-05-MSP_C_FPGA

Table 5.179: MSP_A_FPGA-TX1-05-RX10-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:43:03		2018-Sep-27 15:43:23	
Reset RX	OA	HO		VO	VO (%)
true	7893	43		66.15%	223 87.45%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

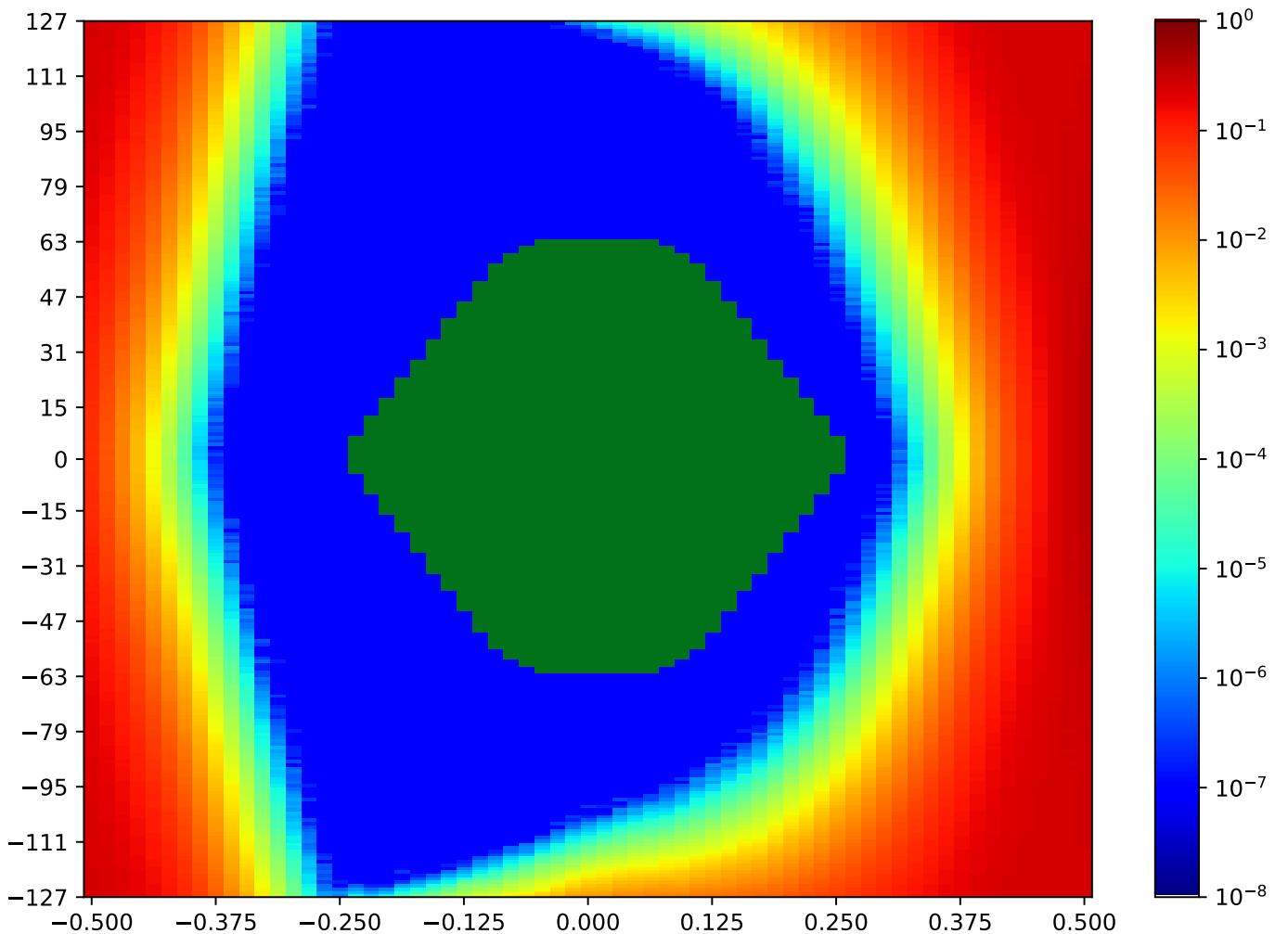


Figure 5.194: MSP_A_FPGA-TX1-05-RX10-05-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.7 MSP_A_FPGA-TX1-06-RX10-06-MSP_C_FPGA

Table 5.180: MSP_A_FPGA-TX1-06-RX10-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:46:56		2018-Sep-27 15:47:16	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9290	43		66.15%	255 99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

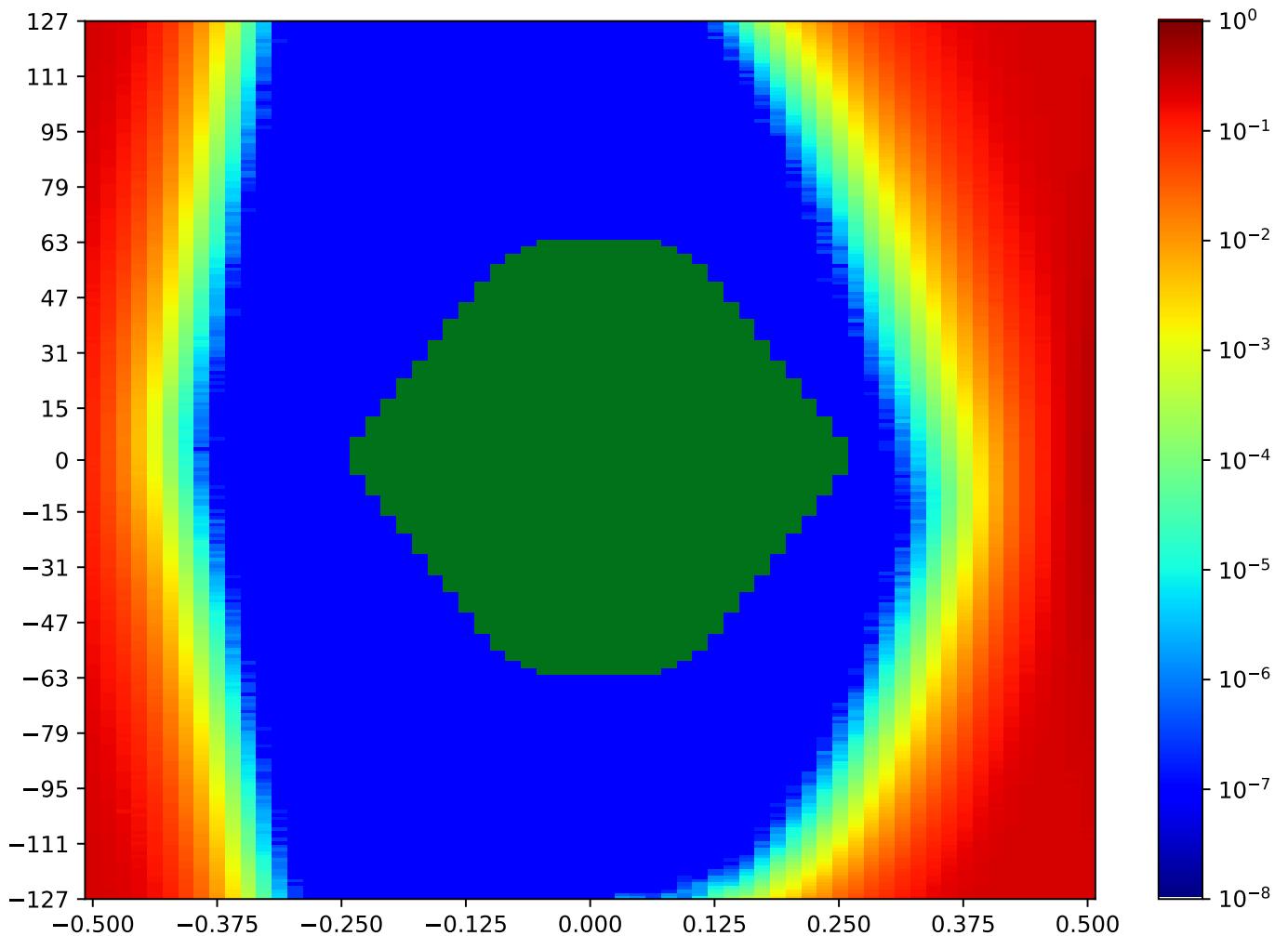


Figure 5.195: MSP_A_FPGA-TX1-06-RX10-06-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.8 MSP_A_FPGA-TX1-07-RX10-07-MSP_C_FPGA

Table 5.181: MSP_A_FPGA-TX1-07-RX10-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:43:43		2018-Sep-27 15:44:03	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8418	40		61.54%	248 96.47%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

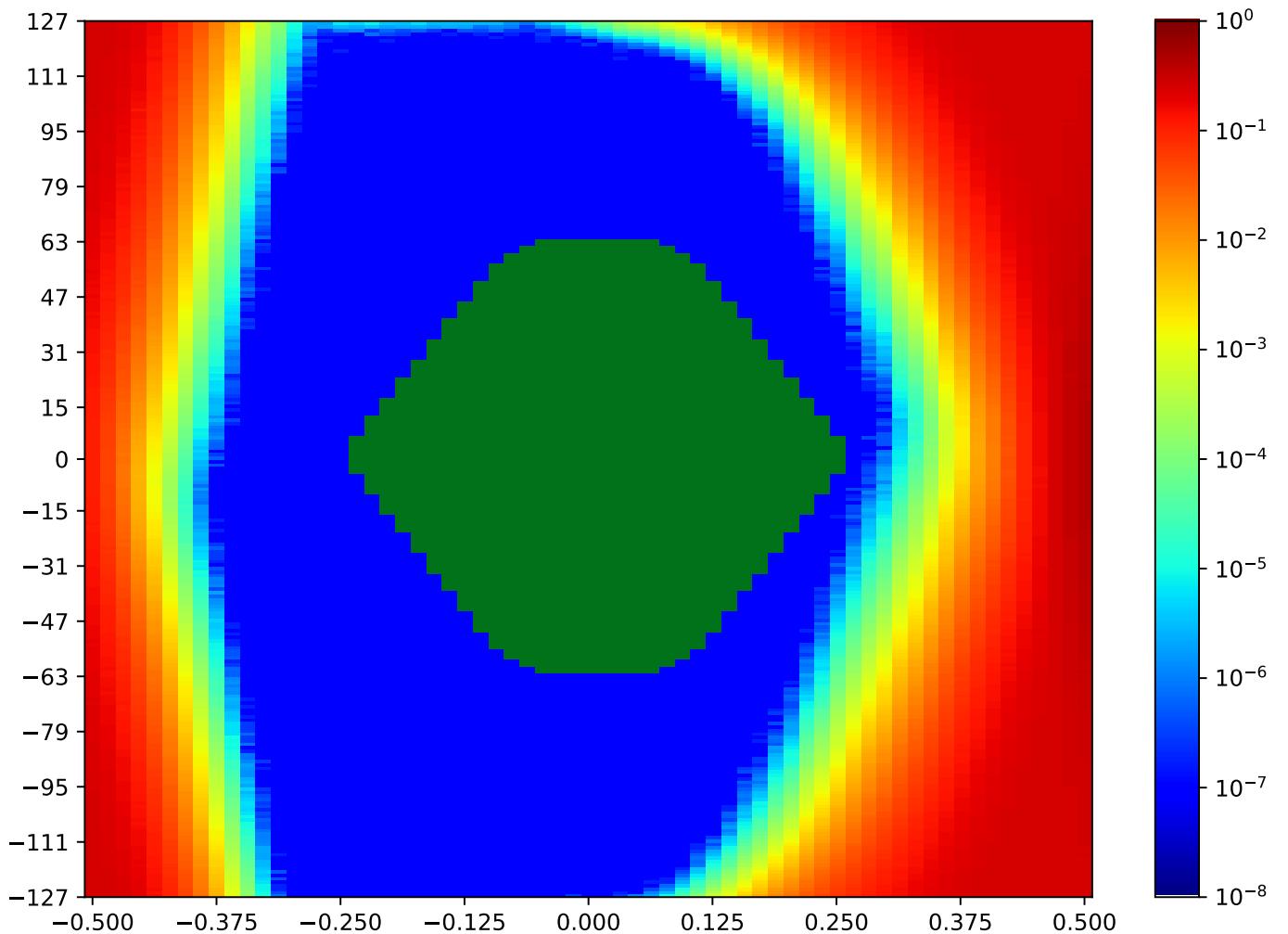


Figure 5.196: MSP_A_FPGA-TX1-07-RX10-07-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.9 MSP_A_FPGA-TX1-08-RX10-08-MSP_C_FPGA

Table 5.182: MSP_A_FPGA-TX1-08-RX10-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:46:30		2018-Sep-27 15:46:56	
Reset RX	OA	HO		VO	VO (%)
true	9223	43		66.15%	255 99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

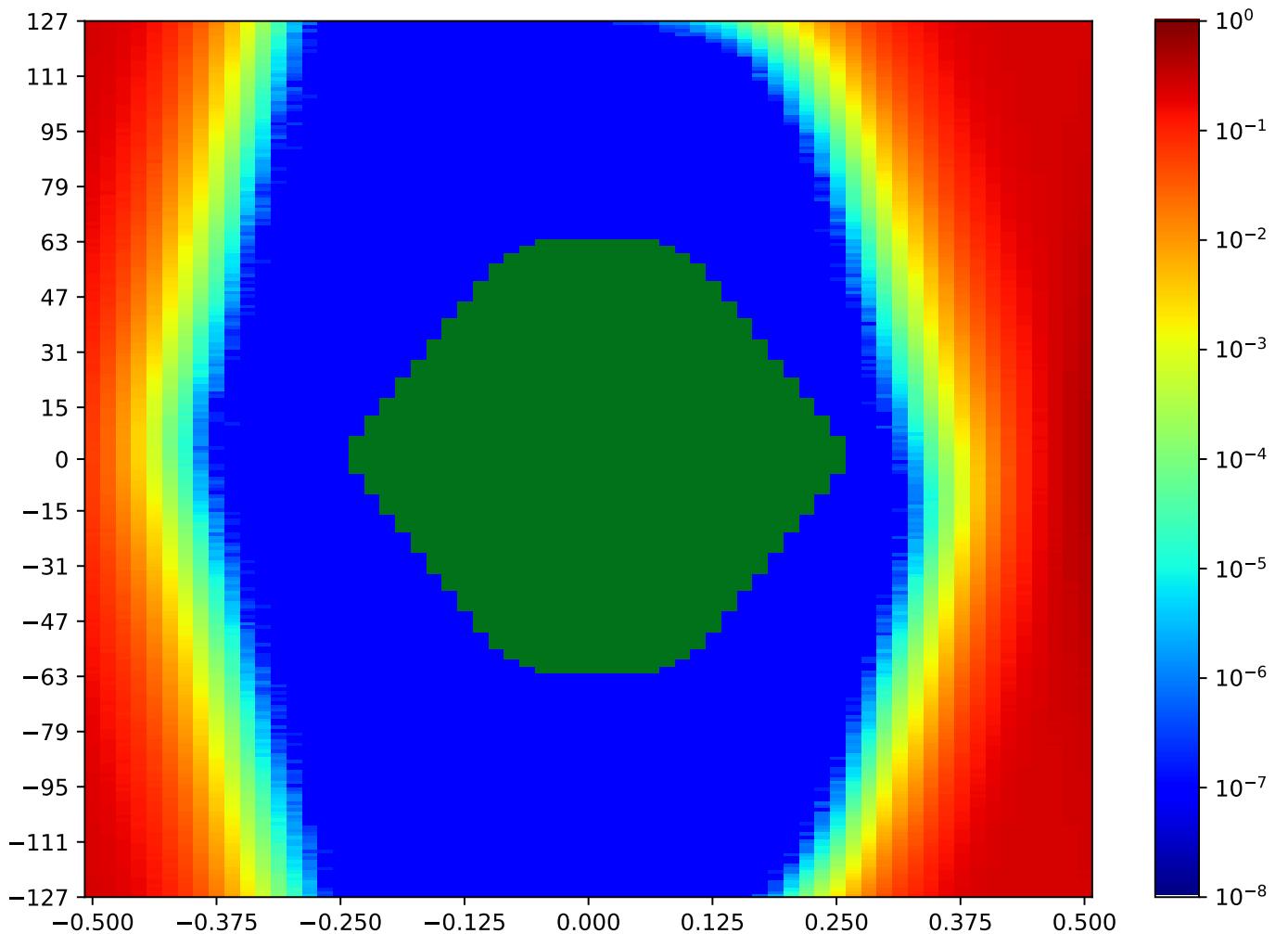


Figure 5.197: MSP_A_FPGA-TX1-08-RX10-08-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.10 MSP_A_FPGA-TX1-09-RX10-09-MSP_C_FPGA

Table 5.183: MSP_A_FPGA-TX1-09-RX10-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:44:23		2018-Sep-27 15:44:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9412	43	66.15%	254	99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

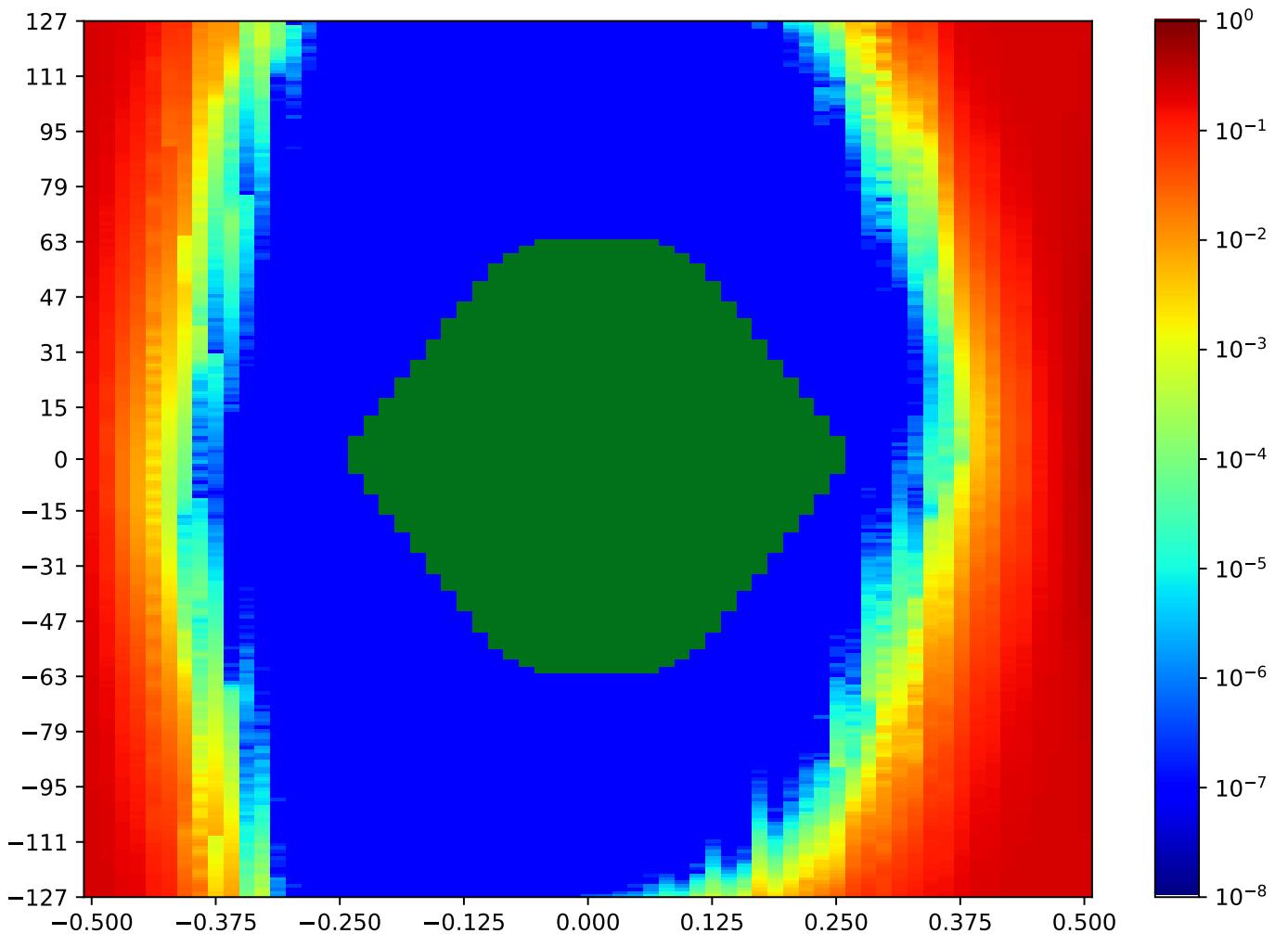


Figure 5.198: MSP_A_FPGA-TX1-09-RX10-09-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.11 MSP_A_FPGA-TX1-10-RX10-10-MSP_C_FPGA

Table 5.184: MSP_A_FPGA-TX1-10-RX10-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:45:44		2018-Sep-27 15:46:09	
Reset RX	OA	HO		VO	VO (%)
true	9030	40		61.54%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

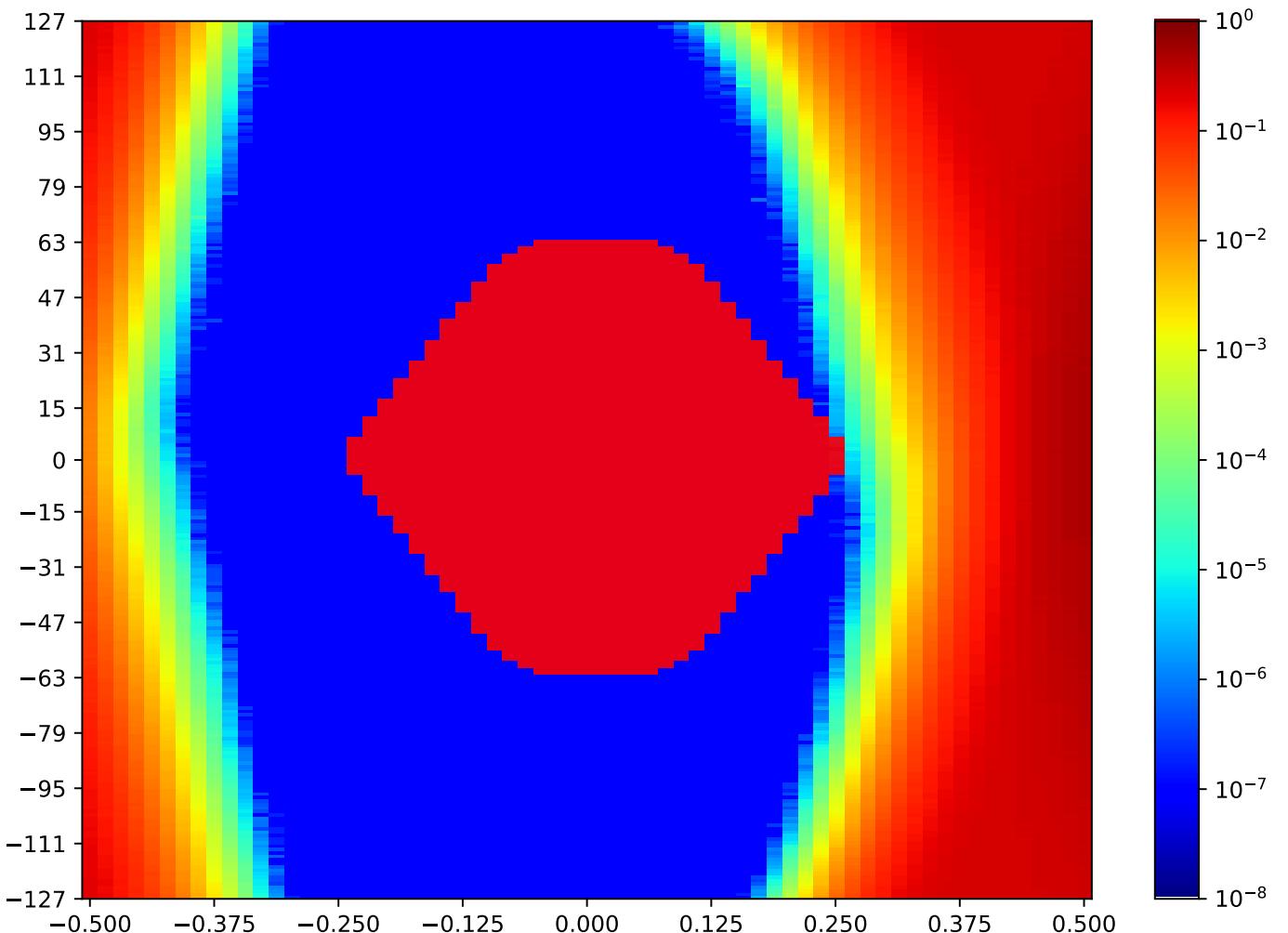


Figure 5.199: MSP_A_FPGA-TX1-10-RX10-10-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.15.12 MSP_A_FPGA-TX1-11-RX10-11-MSP_C_FPGA

Table 5.185: MSP_A_FPGA-TX1-11-RX10-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:45:24		2018-Sep-27 15:45:44	
Reset RX	OA	HO		VO	VO (%)
true	9437	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

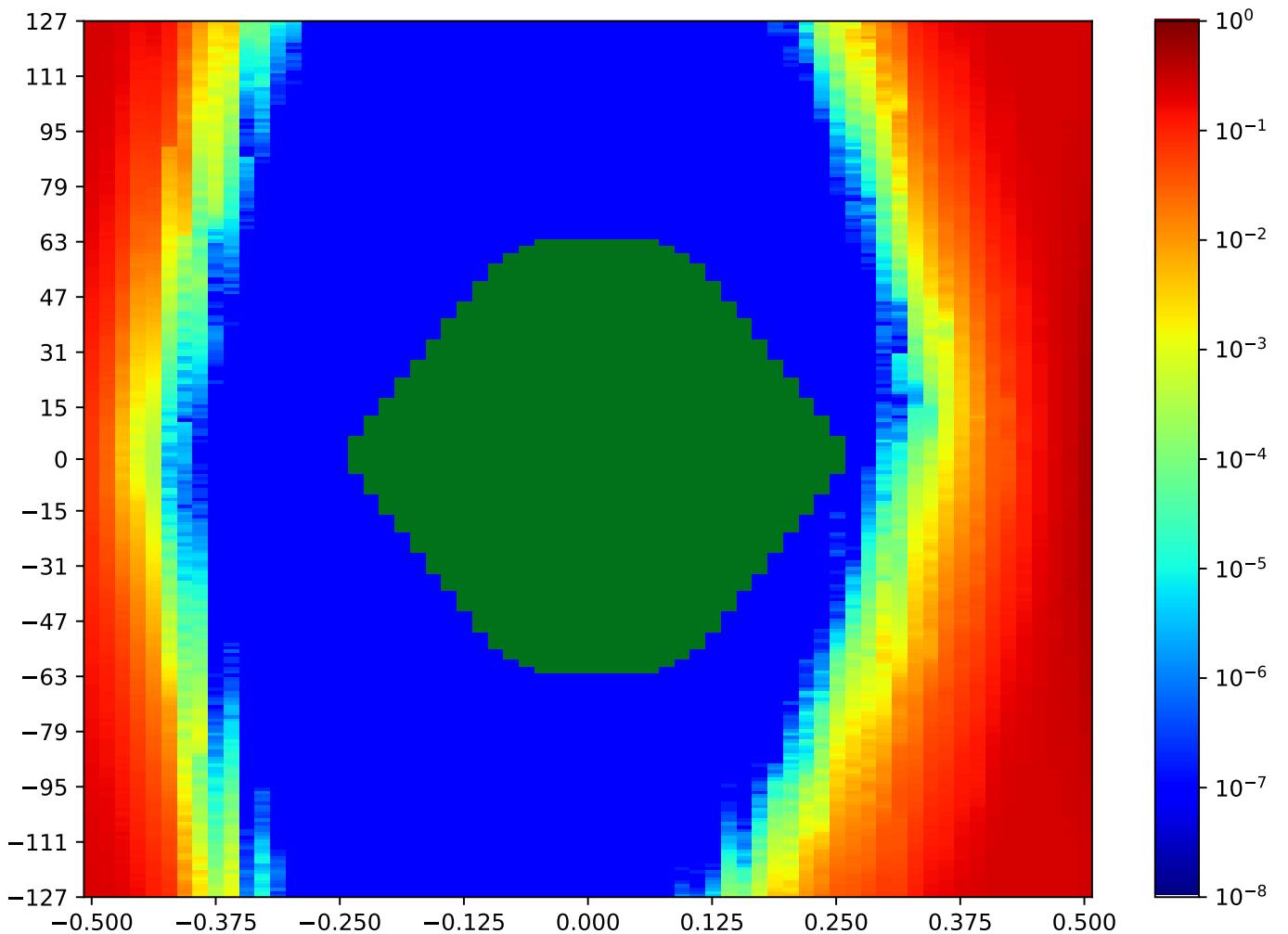


Figure 5.200: MSP_A_FPGA-TX1-11-RX10-11-MSP_C_FPGA

Call back to summary Figure 5.188. Sibling eye diagrams: V2-6.4.

5.16 MSP_A TX2 MSP_C RX11 Minipod Loopback

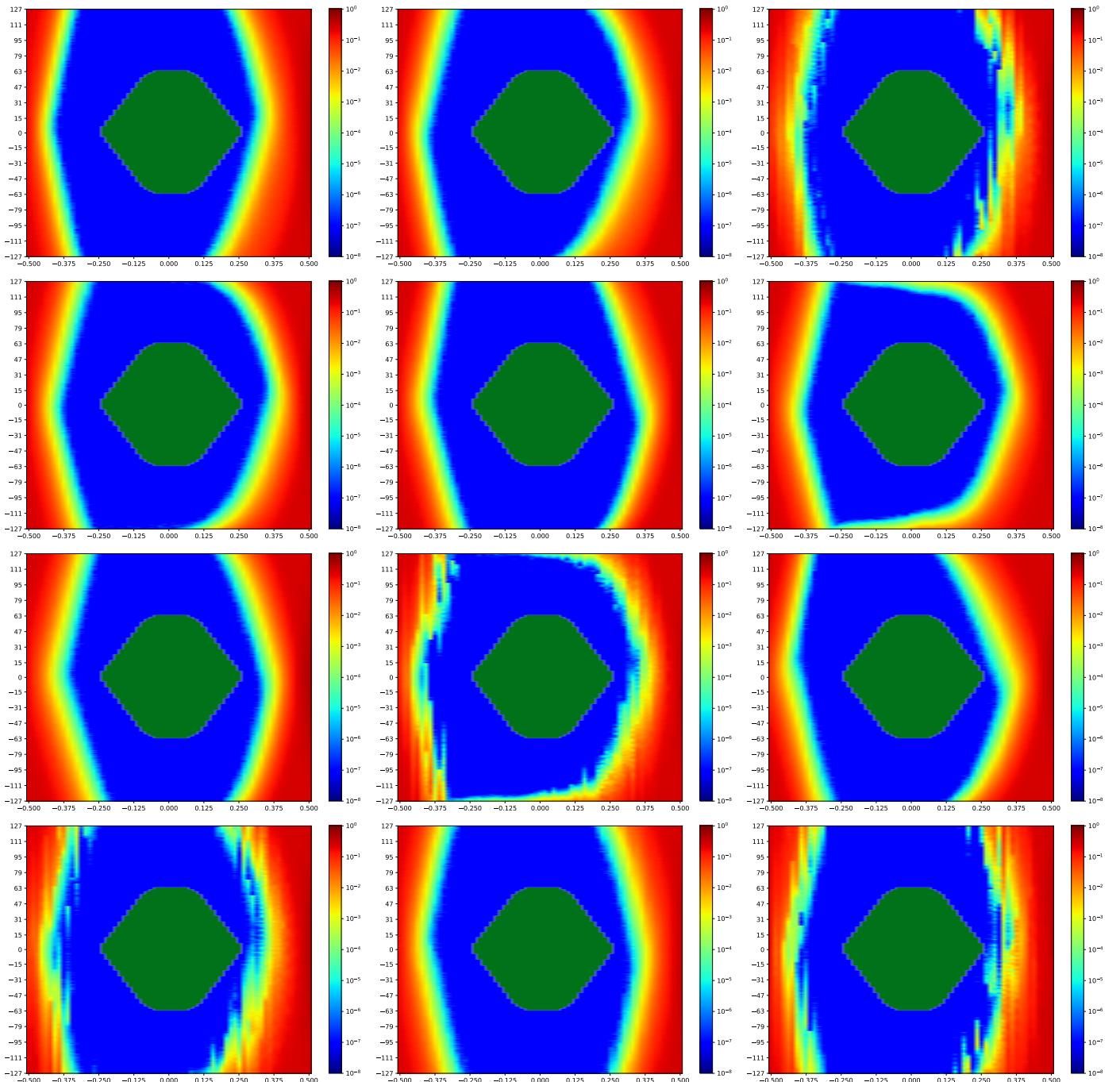


Figure 5.201: MSP_A TX2 MSP_C RX11 Minipod Loopback

A cross-reference to Figure 5.201. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.214.

5.16.1 MSP_A_FPGA-TX2-00-RX11-00-MSP_C_FPGA

Table 5.186: MSP_A_FPGA-TX2-00-RX11-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:48:16		2018-Sep-27 15:48:37	
Reset RX	OA	HO		VO	VO (%)
true	9408	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

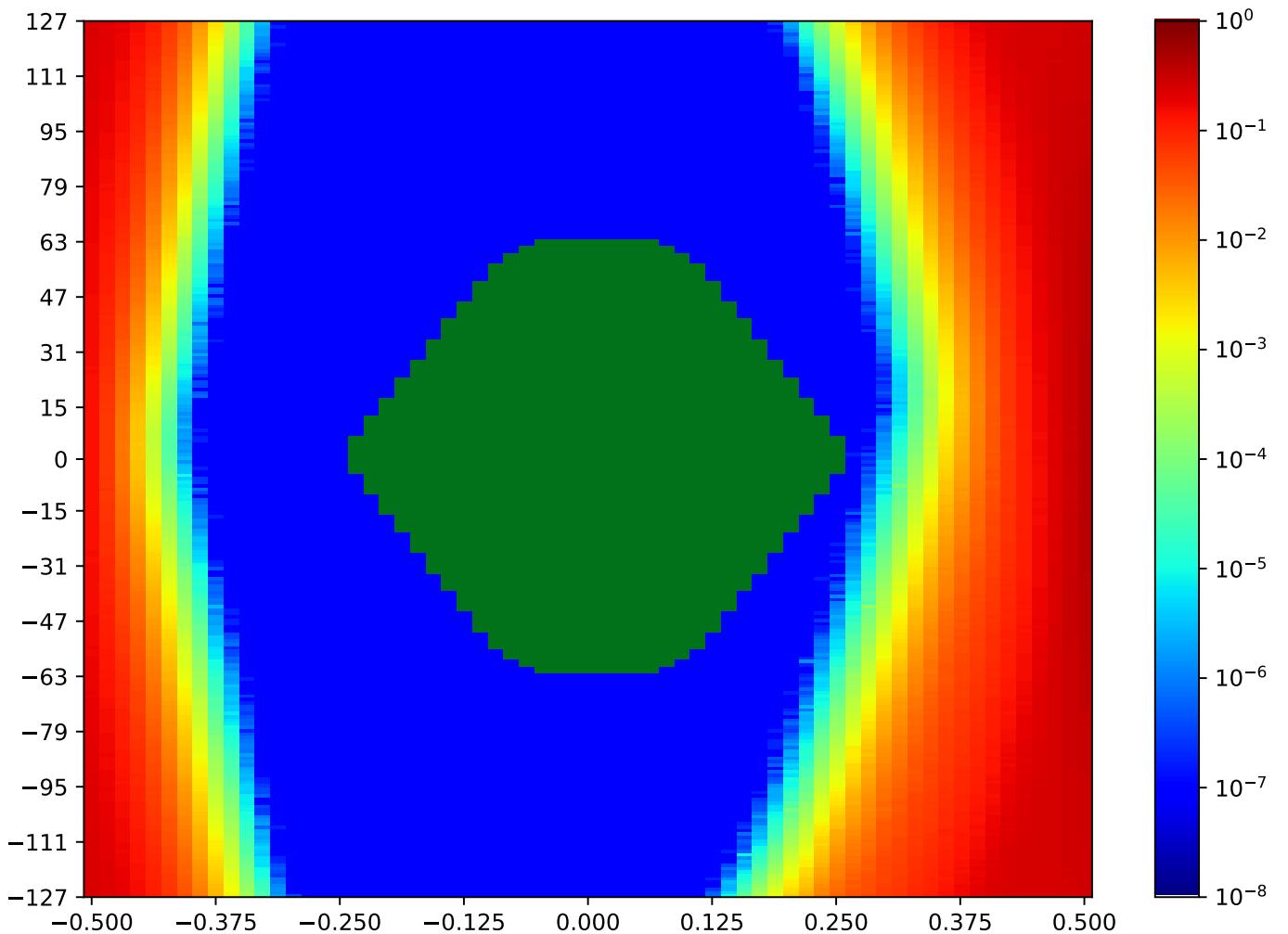


Figure 5.202: MSP_A_FPGA-TX2-00-RX11-00-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.2 MSP_A_FPGA-TX2-01-RX11-01-MSP_C_FPGA

Table 5.187: MSP_A_FPGA-TX2-01-RX11-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:47:36		2018-Sep-27 15:47:56	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8888	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

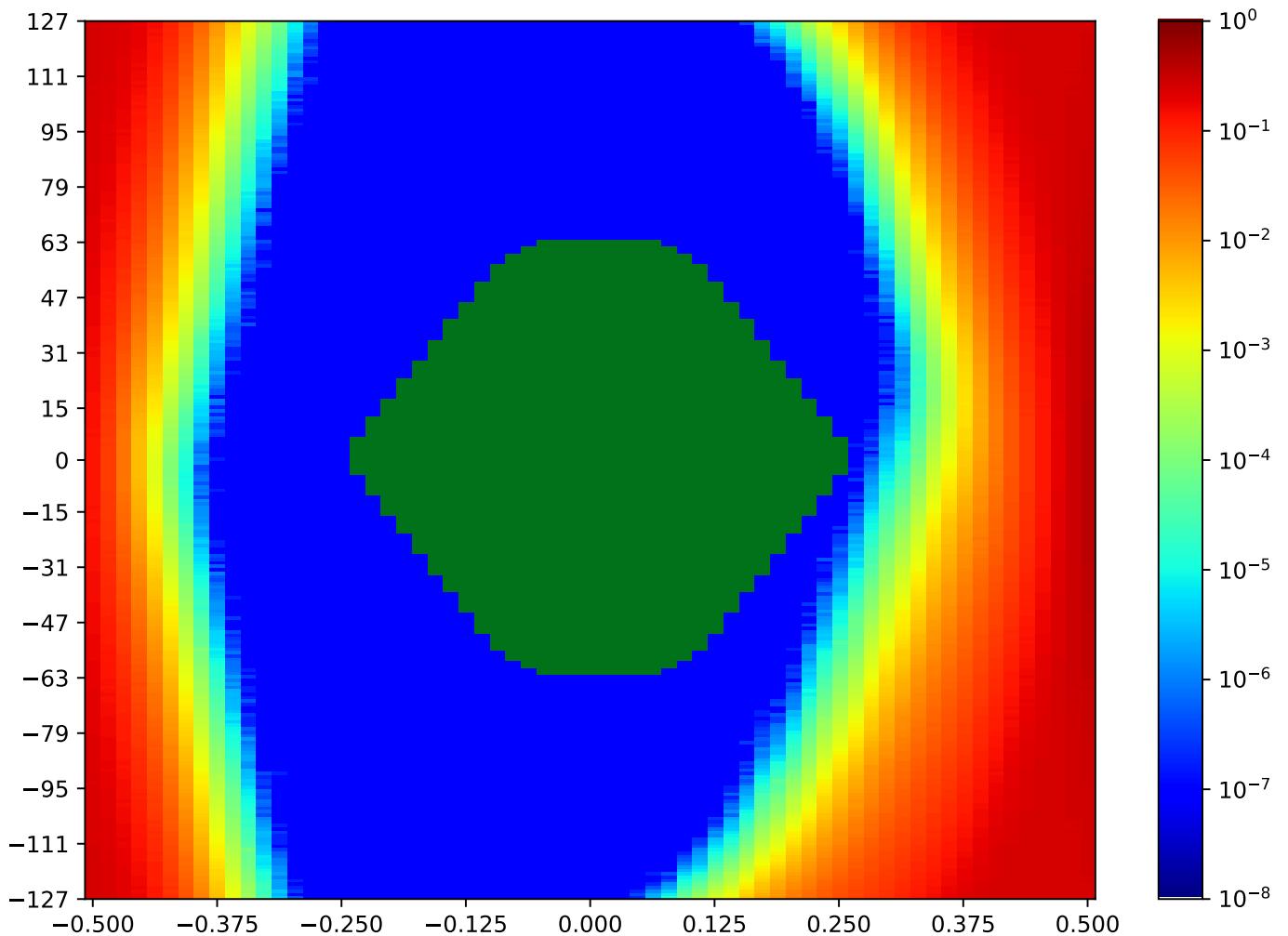


Figure 5.203: MSP_A_FPGA-TX2-01-RX11-01-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.3 MSP_A_FPGA-TX2-02-RX11-02-MSP_C_FPGA

Table 5.188: MSP_A_FPGA-TX2-02-RX11-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:49:18		2018-Sep-27 15:49:38	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9223	42		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

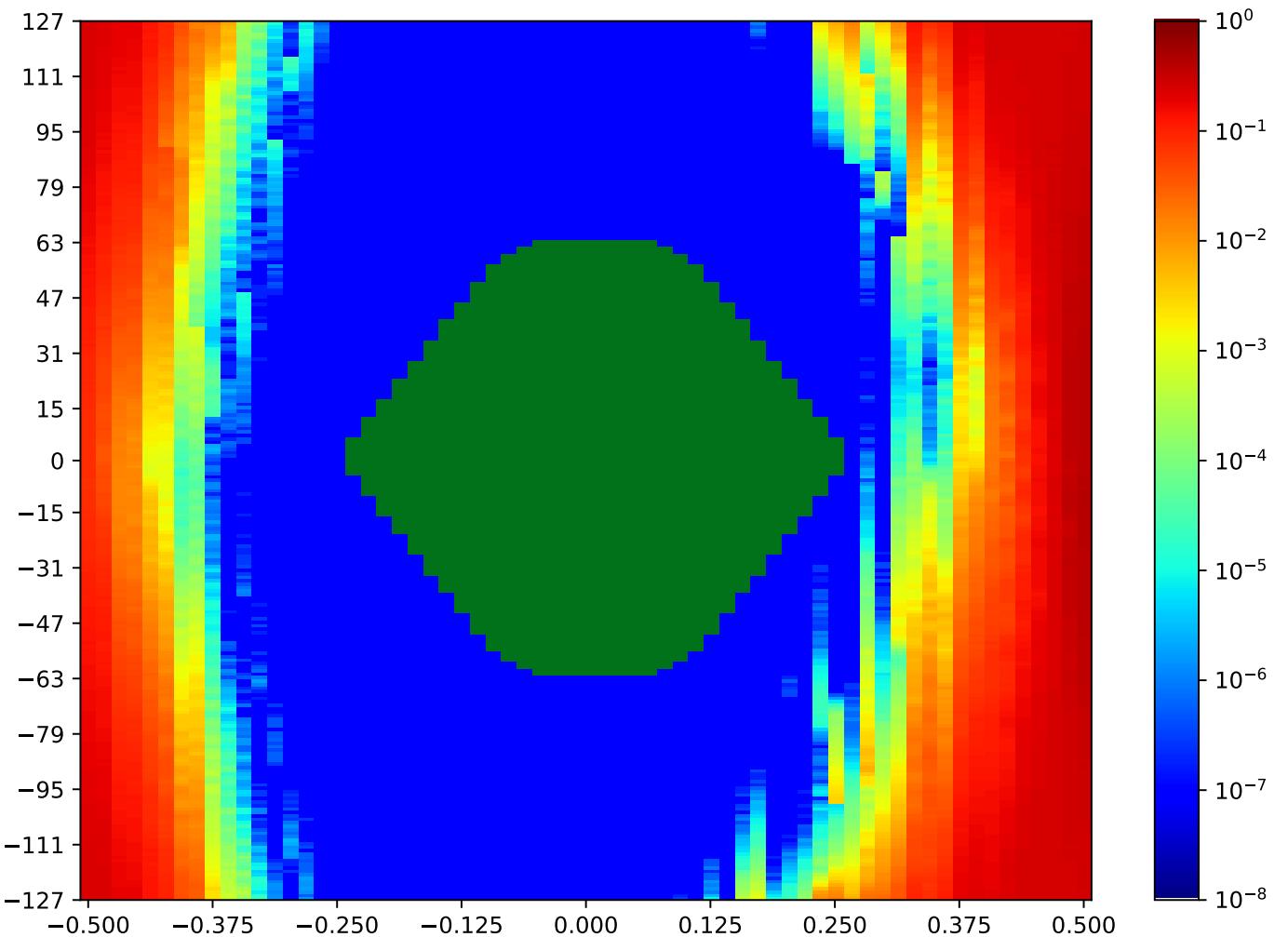


Figure 5.204: MSP_A_FPGA-TX2-02-RX11-02-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.4 MSP_A_FPGA-TX2-03-RX11-03-MSP_C_FPGA

Table 5.189: MSP_A_FPGA-TX2-03-RX11-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:47:16		2018-Sep-27 15:47:36	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9034	43	66.15%	248	96.47%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

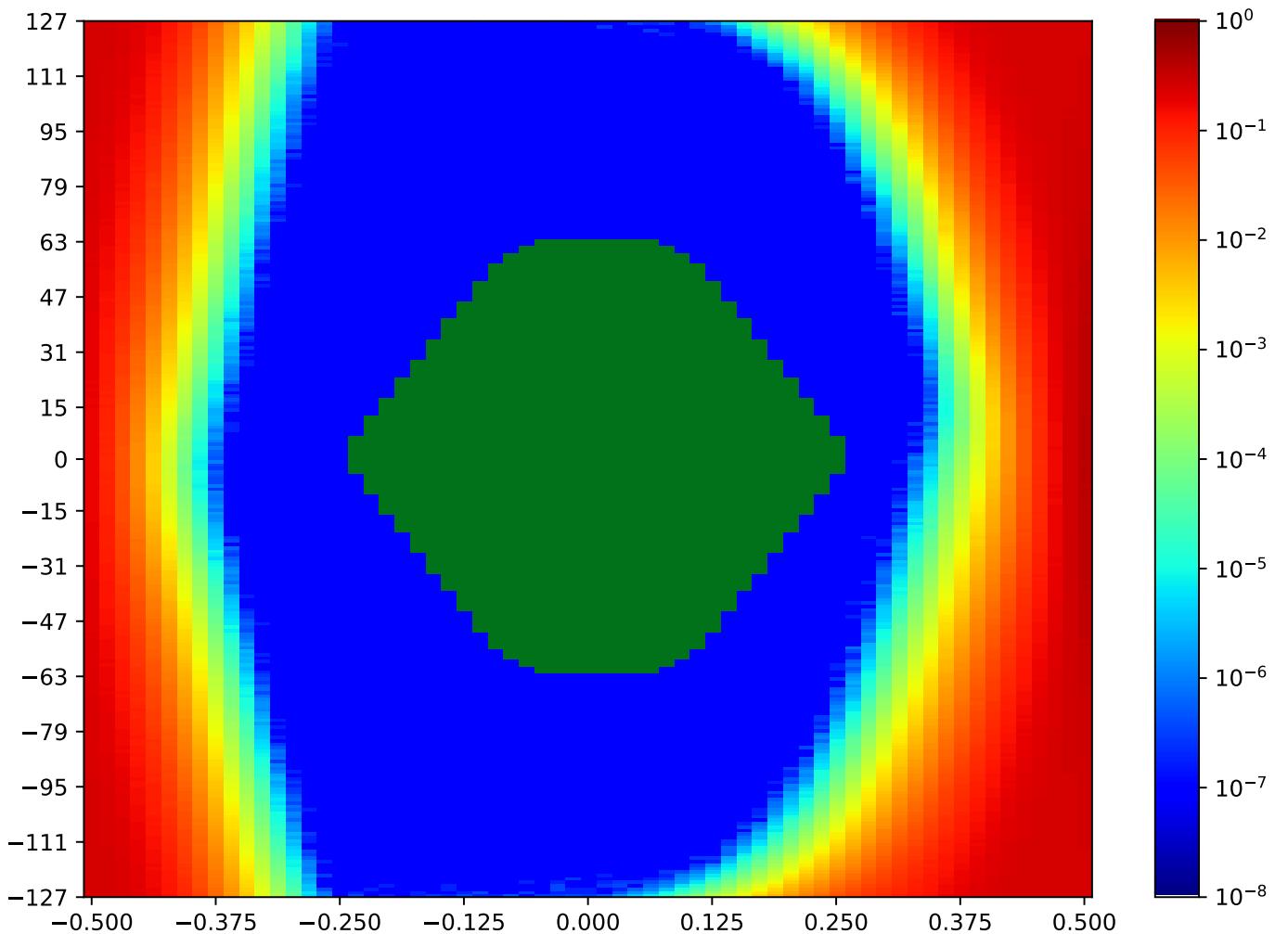


Figure 5.205: MSP_A_FPGA-TX2-03-RX11-03-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.5 MSP_A_FPGA-TX2-04-RX11-04-MSP_C_FPGA

Table 5.190: MSP_A_FPGA-TX2-04-RX11-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:50:19		2018-Sep-27 15:50:39	
Reset RX	OA	HO		VO	VO (%)
true	9427	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

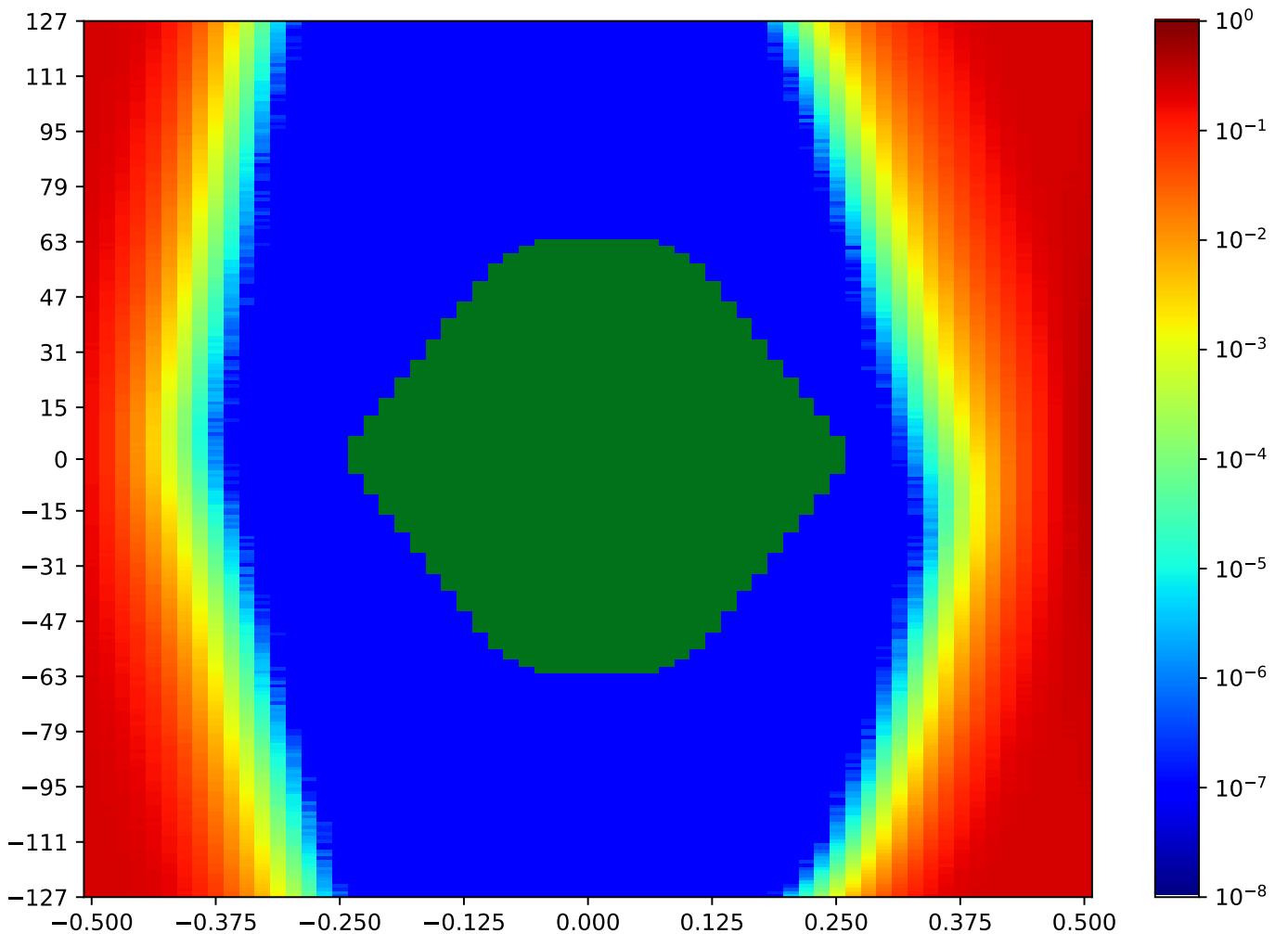


Figure 5.206: MSP_A_FPGA-TX2-04-RX11-04-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.6 MSP_A_FPGA-TX2-05-RX11-05-MSP_C_FPGA

Table 5.191: MSP_A_FPGA-TX2-05-RX11-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:47:56		2018-Sep-27 15:48:16	
Reset RX	OA	HO		VO	VO (%)
true	7961	42		223	87.45%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

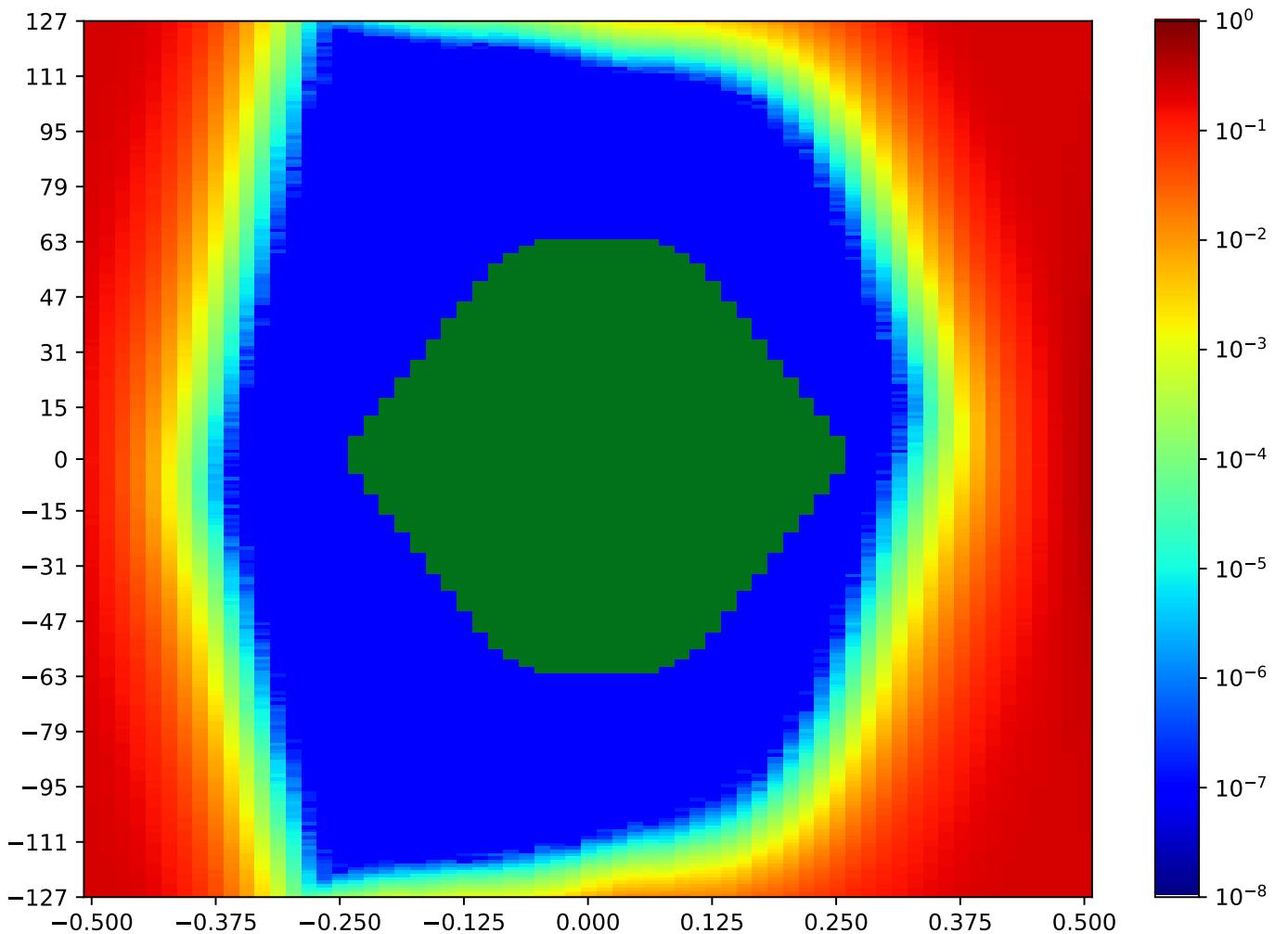


Figure 5.207: MSP_A_FPGA-TX2-05-RX11-05-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.7 MSP_A_FPGA-TX2-06-RX11-06-MSP_C_FPGA

Table 5.192: MSP_A_FPGA-TX2-06-RX11-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:50:59		2018-Sep-27 15:51:20	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8654	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

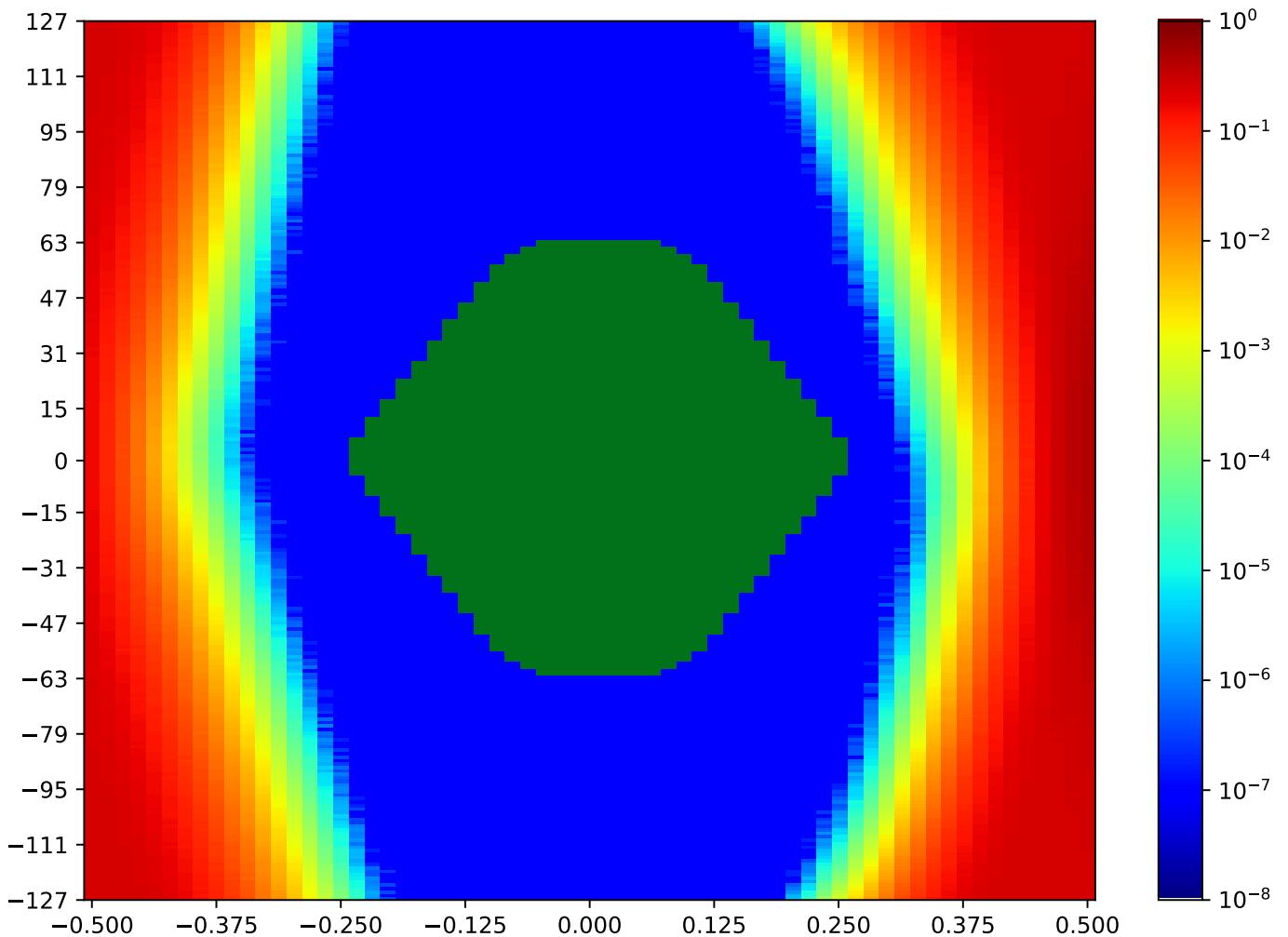


Figure 5.208: MSP_A_FPGA-TX2-06-RX11-06-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.8 MSP_A_FPGA-TX2-07-RX11-07-MSP_C_FPGA

Table 5.193: MSP_A_FPGA-TX2-07-RX11-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:48:37		2018-Sep-27 15:48:57	
Reset RX	OA	HO		VO	VO (%)
true	9041	45		237	92.94%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x00009 SVN: 16356	

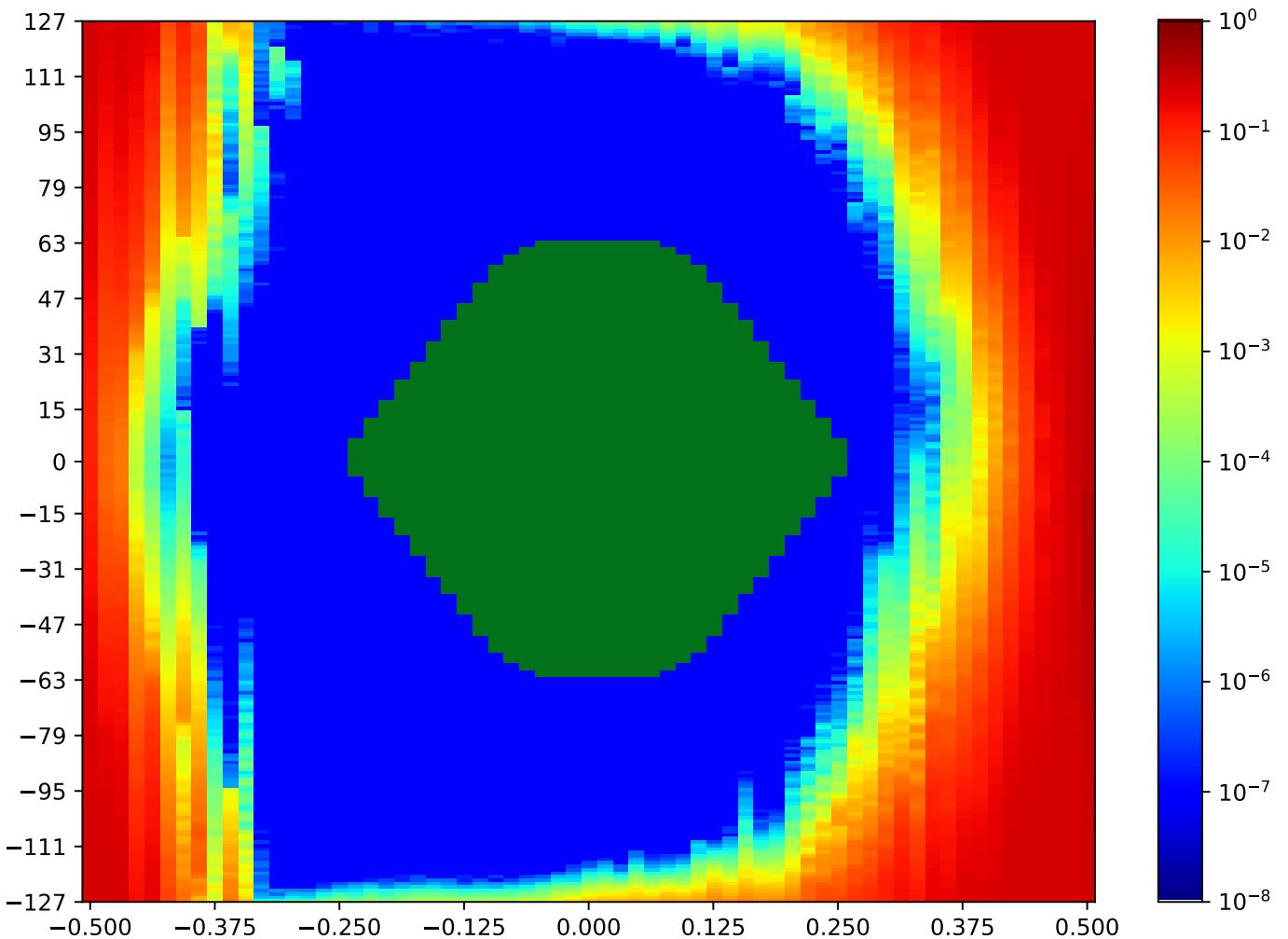


Figure 5.209: MSP_A_FPGA-TX2-07-RX11-07-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.9 MSP_A_FPGA-TX2-08-RX11-08-MSP_C_FPGA

Table 5.194: MSP_A_FPGA-TX2-08-RX11-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:50:39		2018-Sep-27 15:50:59	
Reset RX	OA	HO		VO	VO (%)
true	8876	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

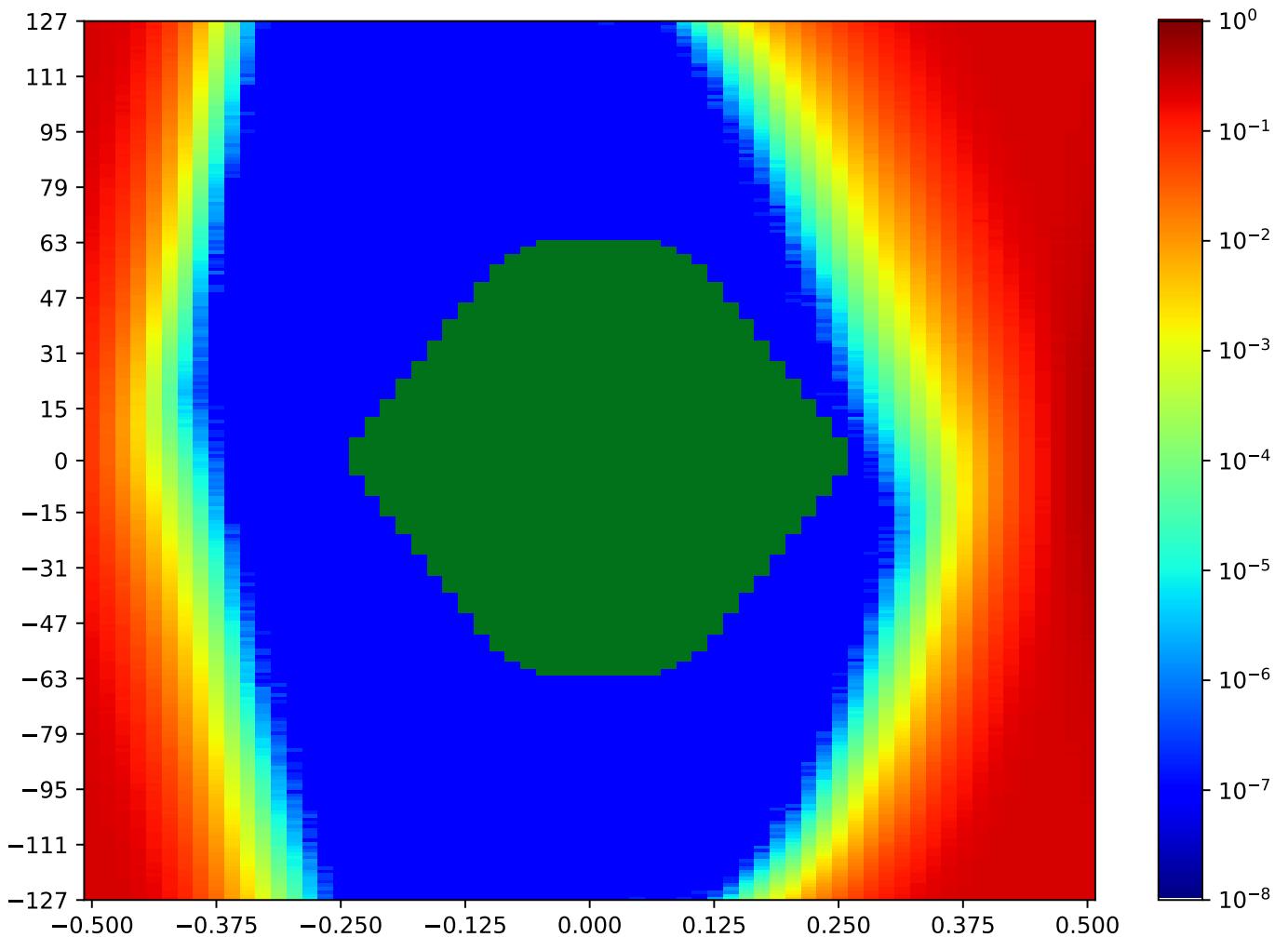


Figure 5.210: MSP_A_FPGA-TX2-08-RX11-08-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.10 MSP_A_FPGA-TX2-09-RX11-09-MSP_C_FPGA

Table 5.195: MSP_A_FPGA-TX2-09-RX11-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:48:57		2018-Sep-27 15:49:18	
Reset RX	OA	HO		VO	VO (%)
true	9019	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

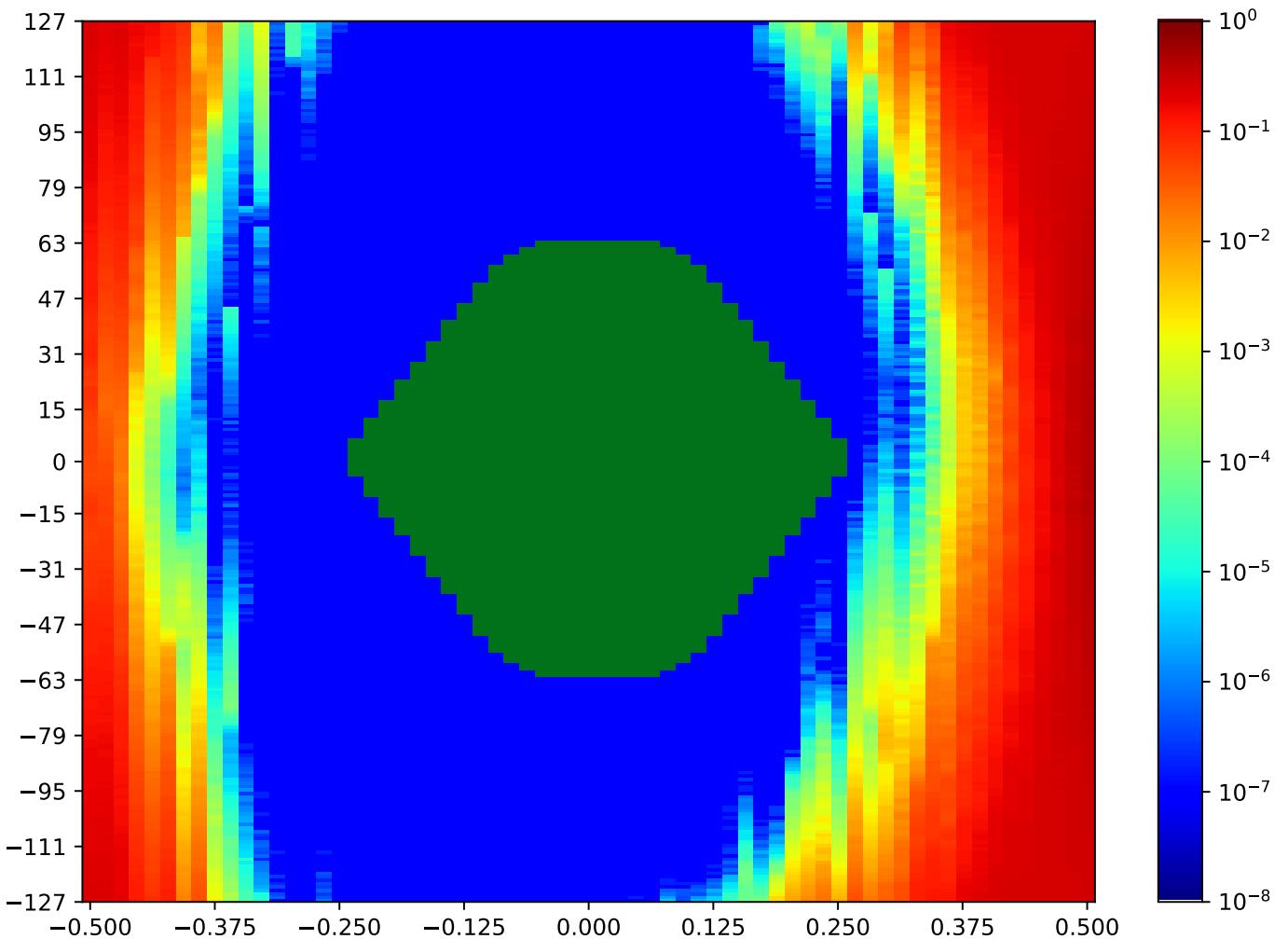


Figure 5.211: MSP_A_FPGA-TX2-09-RX11-09-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.11 MSP_A_FPGA-TX2-10-RX11-10-MSP_C_FPGA

Table 5.196: MSP_A_FPGA-TX2-10-RX11-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:49:58		2018-Sep-27 15:50:18	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9415	42	64.62%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

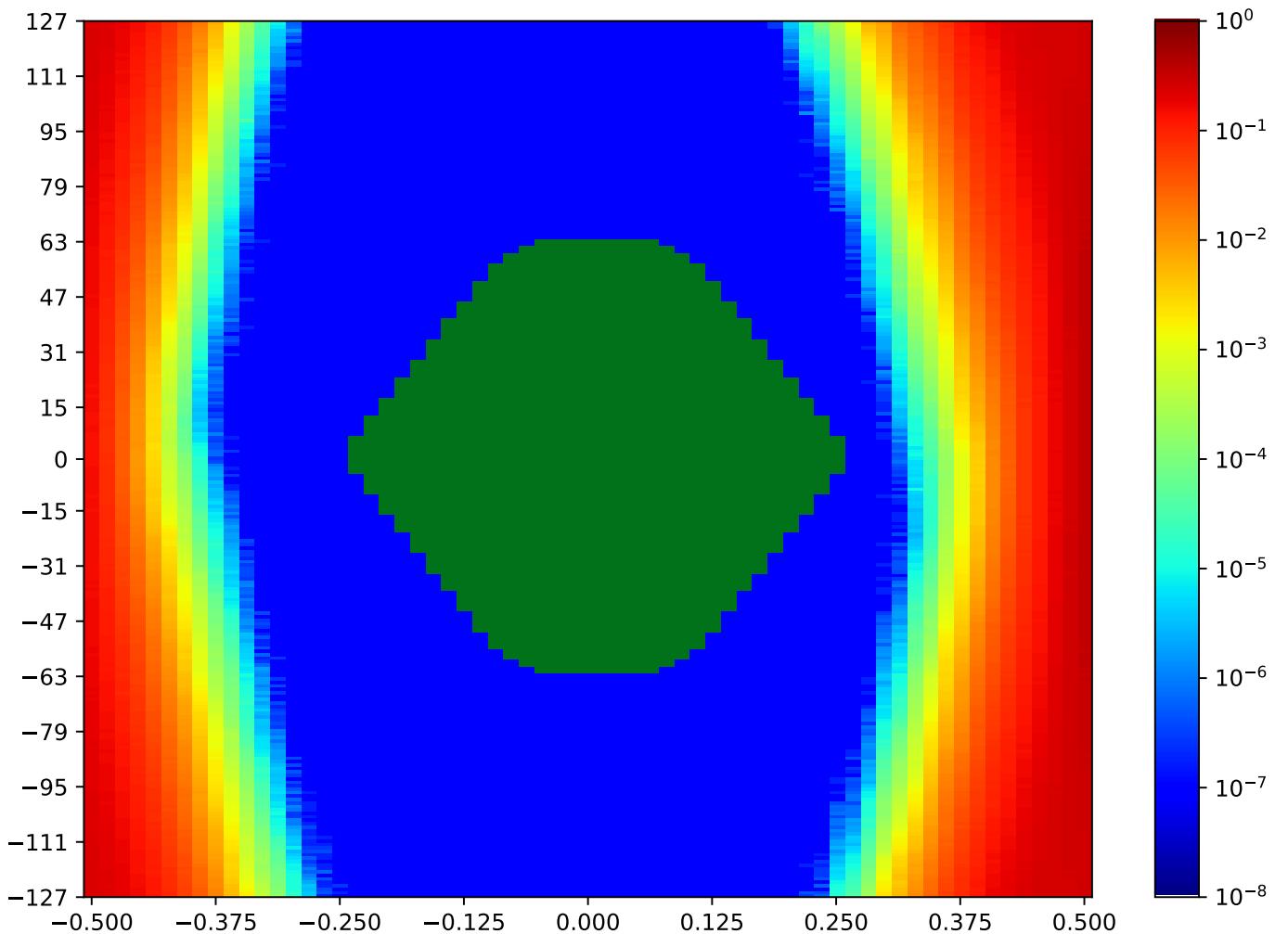


Figure 5.212: MSP_A_FPGA-TX2-10-RX11-10-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.16.12 MSP_A_FPGA-TX2-11-RX11-11-MSP_C_FPGA

Table 5.197: MSP_A_FPGA-TX2-11-RX11-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:49:38		2018-Sep-27 15:49:58	
Reset RX	OA	HO		VO	VO (%)
true	9626	40		61.54%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

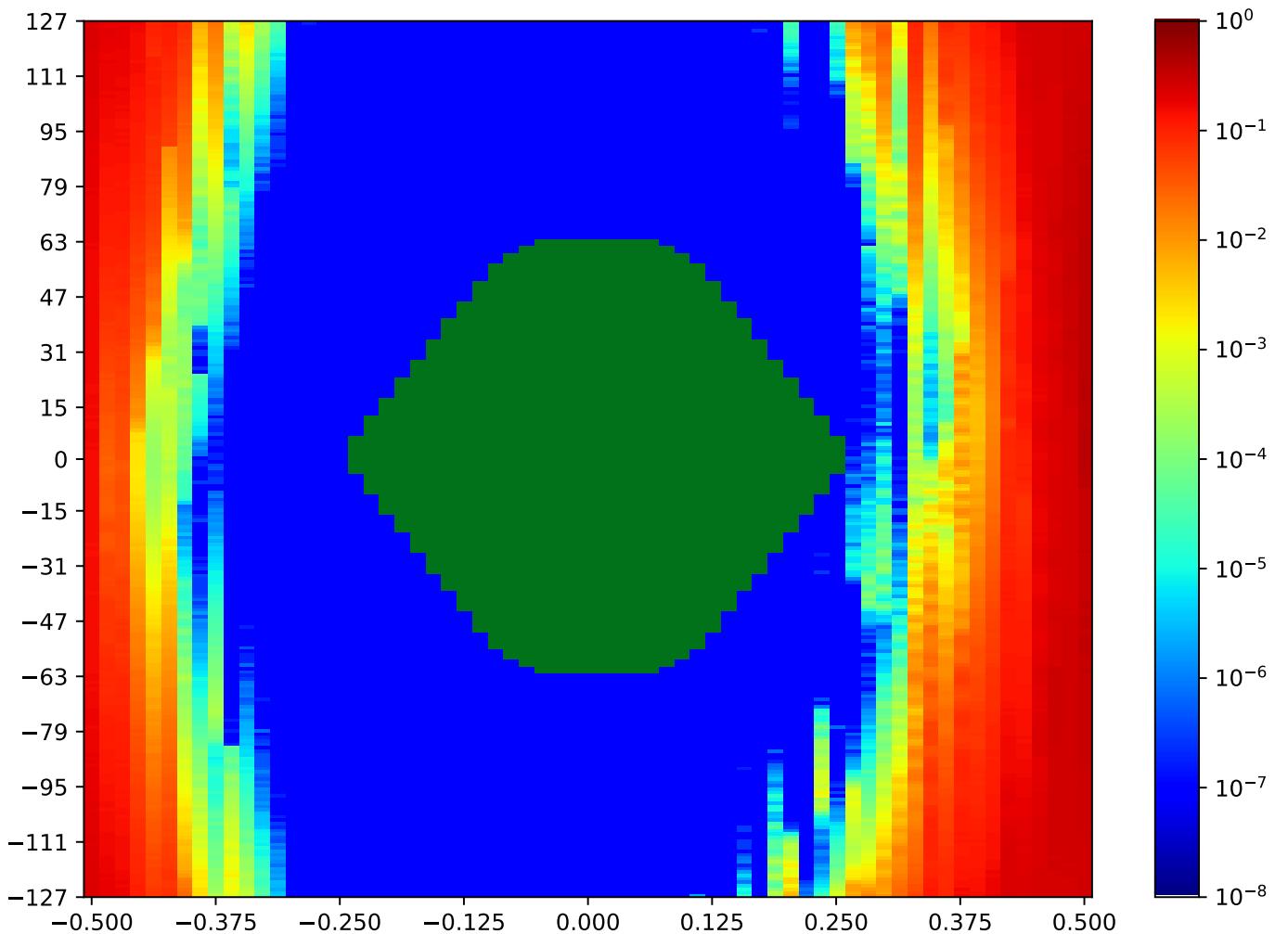


Figure 5.213: MSP_A_FPGA-TX2-11-RX11-11-MSP_C_FPGA

Call back to summary Figure 5.201. Sibling eye diagrams: V2-6.4.

5.17 MSP_C TX3 MSP_A RX1 Minipod Loopback

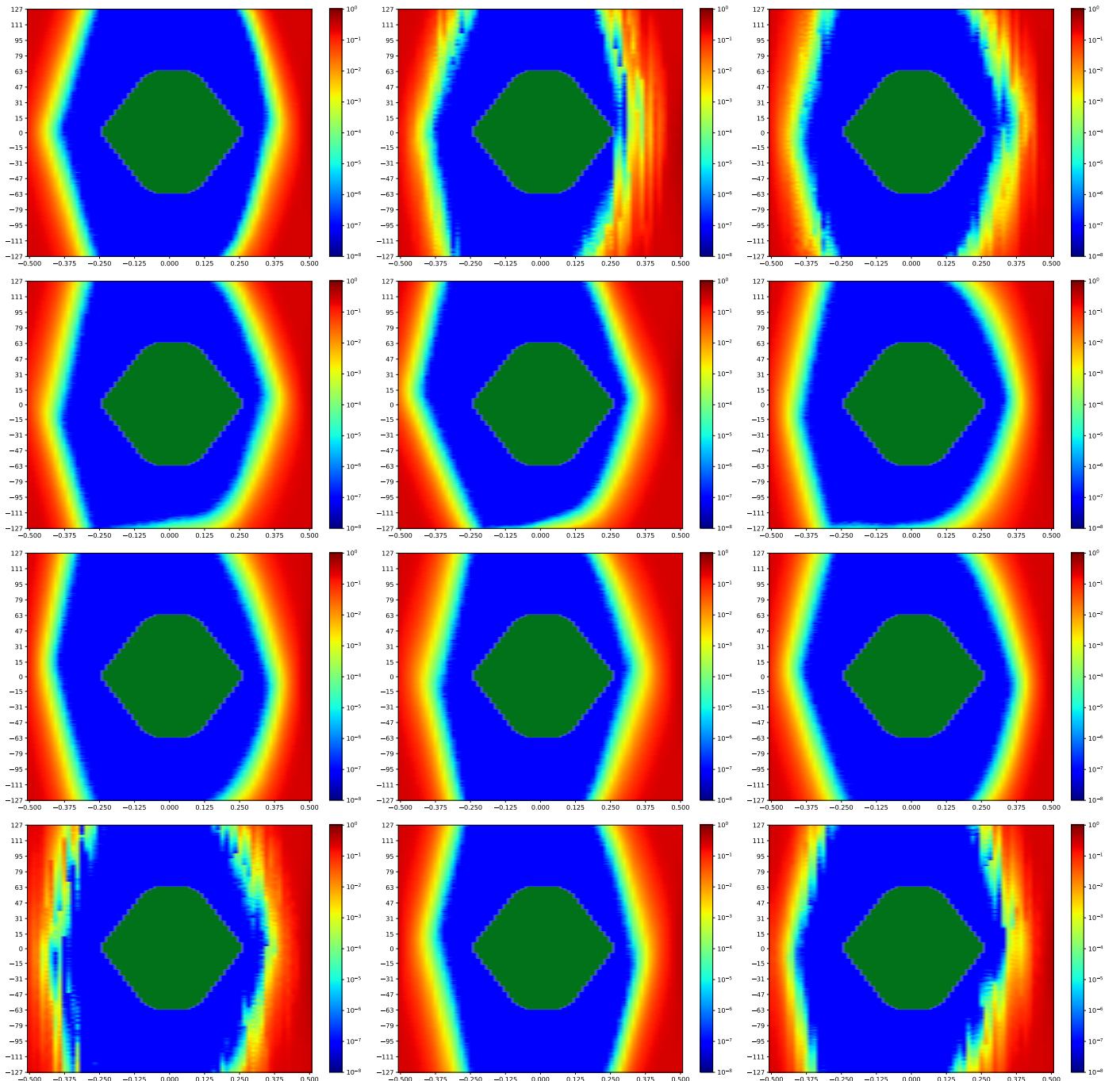


Figure 5.214: MSP_C TX3 MSP_A RX1 Minipod Loopback

A cross-reference to Figure 5.214. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.227.

5.17.1 MSP_C_FPGA-TX3-00-RX1-00-MSP_A_FPGA

Table 5.198: MSP_C_FPGA-TX3-00-RX1-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:52:21		2018-Sep-27 15:52:41	
Reset RX	OA	HO		VO	VO (%)
true	9646	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

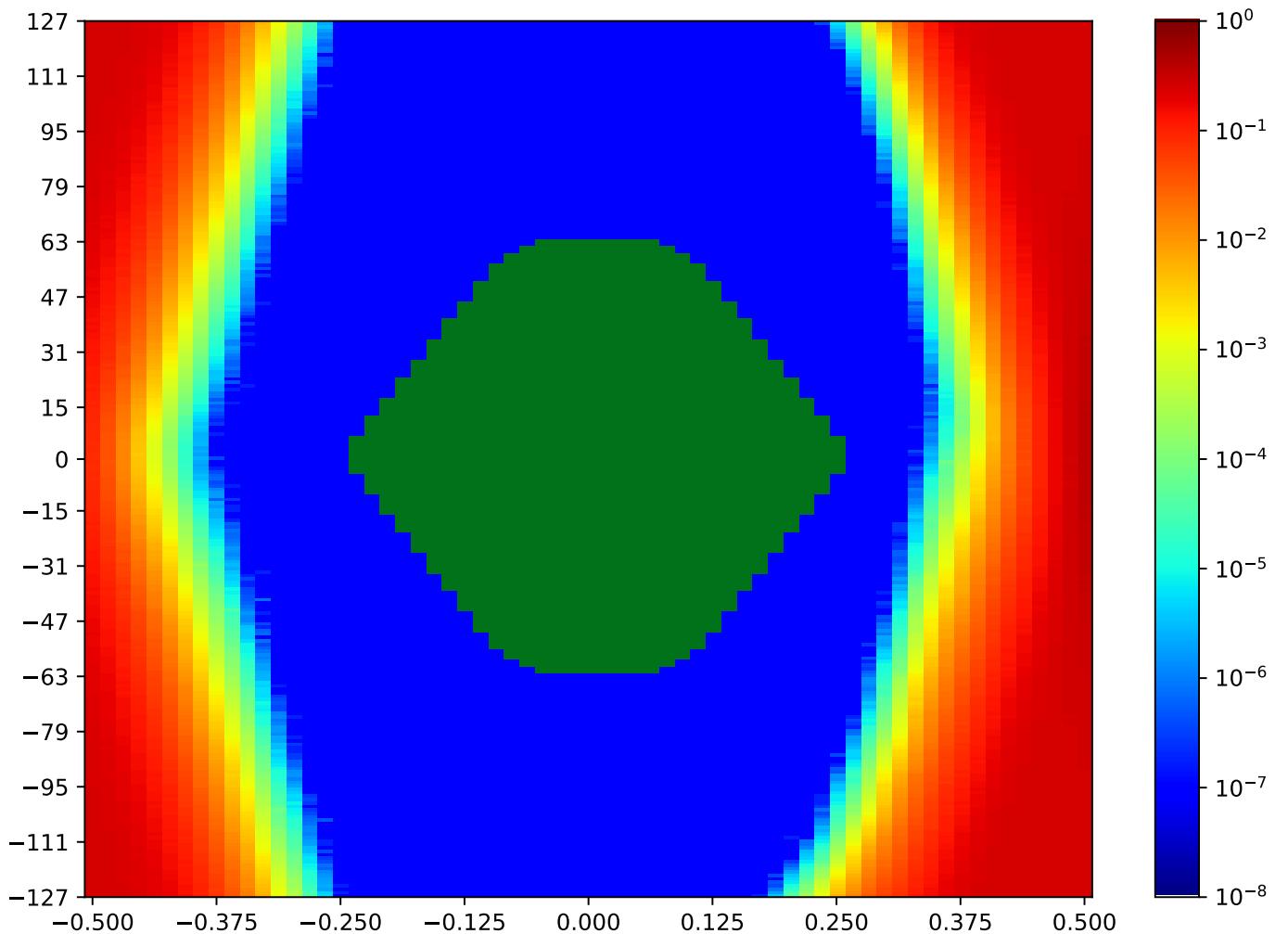


Figure 5.215: MSP_C_FPGA-TX3-00-RX1-00-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.2 MSP_C_FPGA-TX3-01-RX1-01-MSP_A_FPGA

Table 5.199: MSP_C_FPGA-TX3-01-RX1-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:53:02		2018-Sep-27 15:53:22	
Reset RX	OA	HO		VO	VO (%)
true	8697	43		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

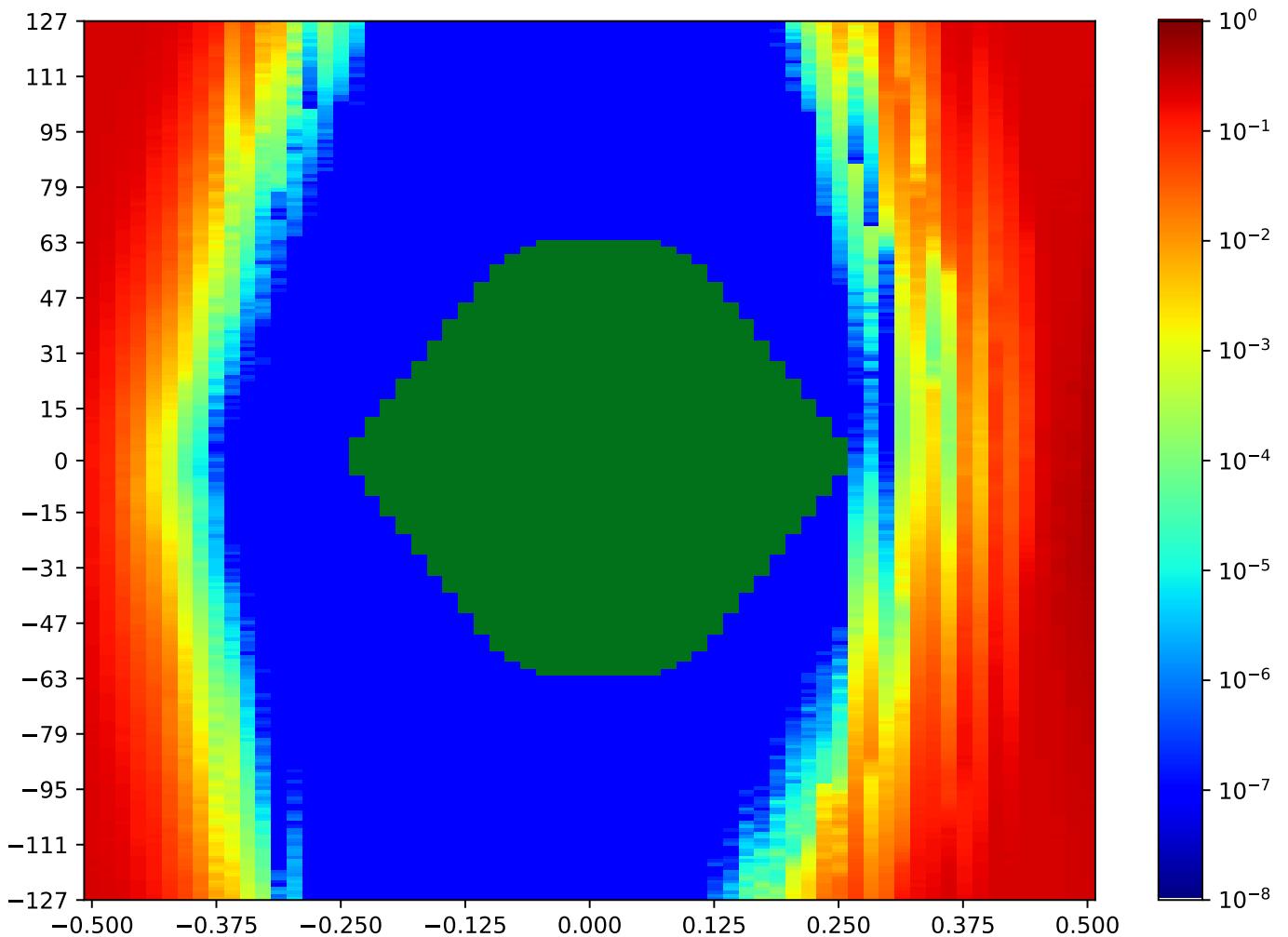


Figure 5.216: MSP_C_FPGA-TX3-01-RX1-01-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.3 MSP_C_FPGA-TX3-02-RX1-02-MSP_A_FPGA

Table 5.200: MSP_C_FPGA-TX3-02-RX1-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:53:22		2018-Sep-27 15:53:43	
Reset RX	OA	HO		VO	VO (%)
true	9028	42		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

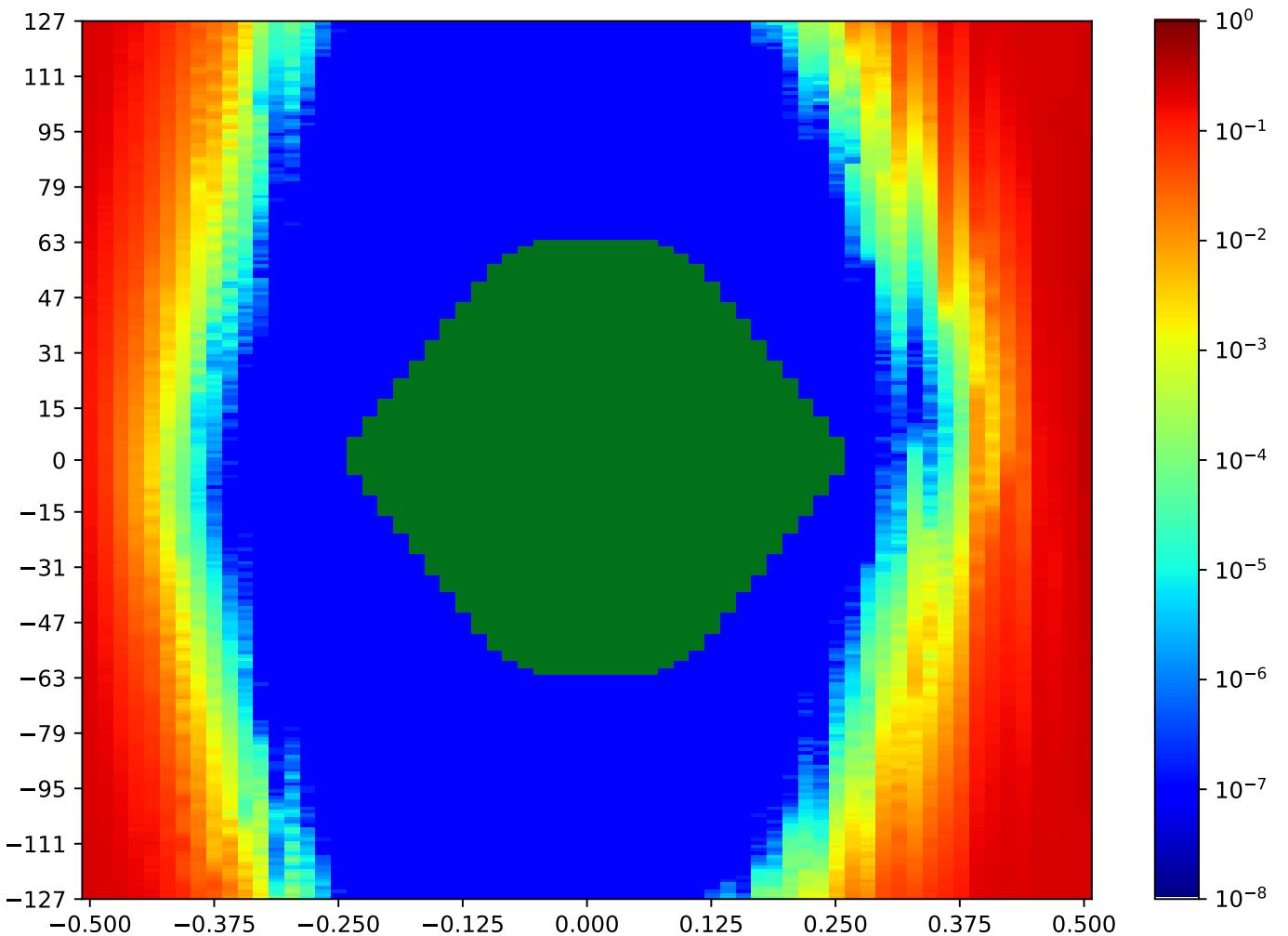


Figure 5.217: MSP_C_FPGA-TX3-02-RX1-02-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.4 MSP_C_FPGA-TX3-03-RX1-03-MSP_A_FPGA

Table 5.201: MSP_C_FPGA-TX3-03-RX1-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:51:40		2018-Sep-27 15:52:00	
Reset RX	OA	HO		VO	VO (%)
true	8699	43		66.15%	239 93.73%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

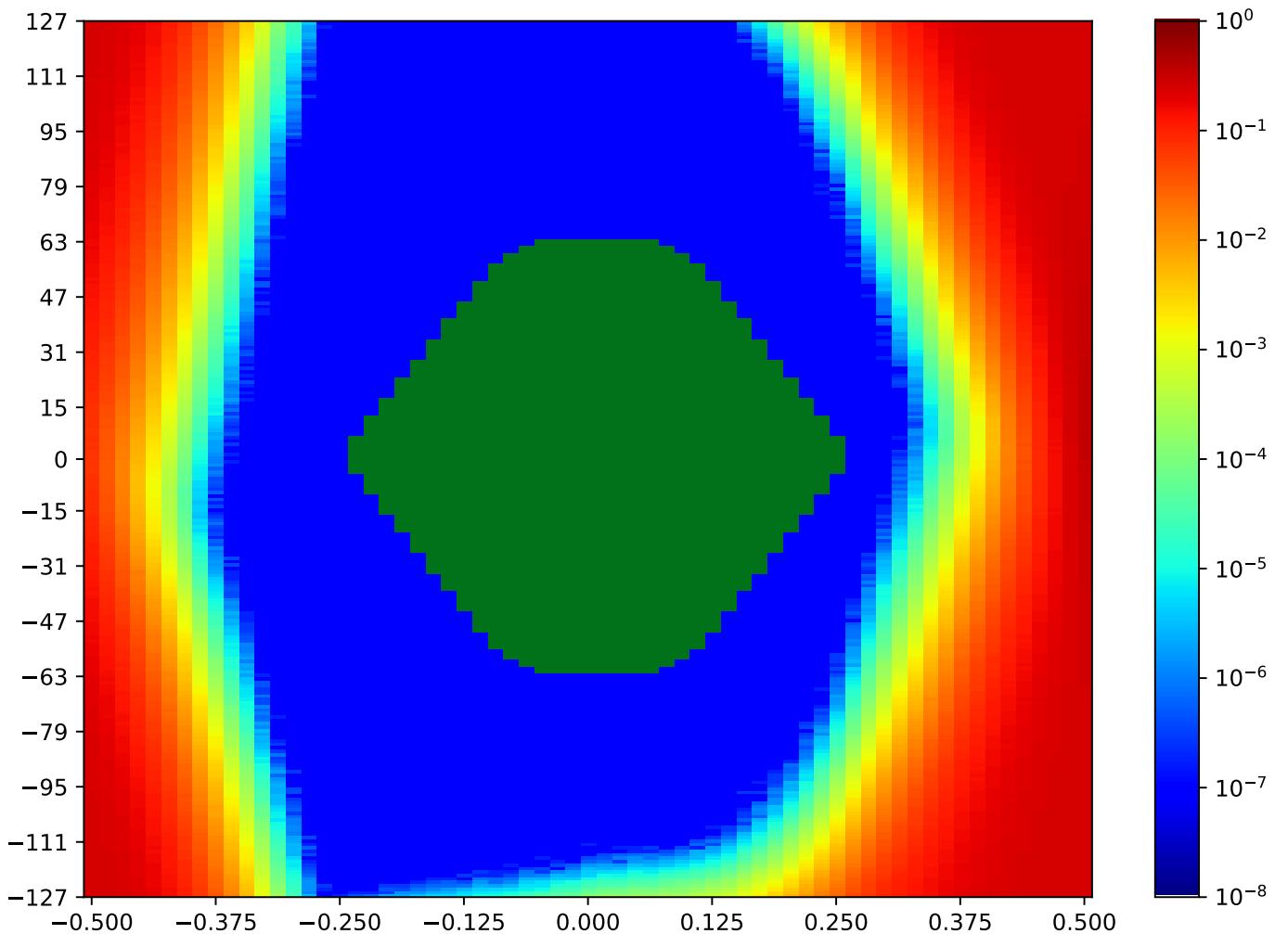


Figure 5.218: MSP_C_FPGA-TX3-03-RX1-03-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.5 MSP_C_FPGA-TX3-04-RX1-04-MSP_A_FPGA

Table 5.202: MSP_C_FPGA-TX3-04-RX1-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:54:24		2018-Sep-27 15:54:45	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8587	43	66.15%	245	95.69%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

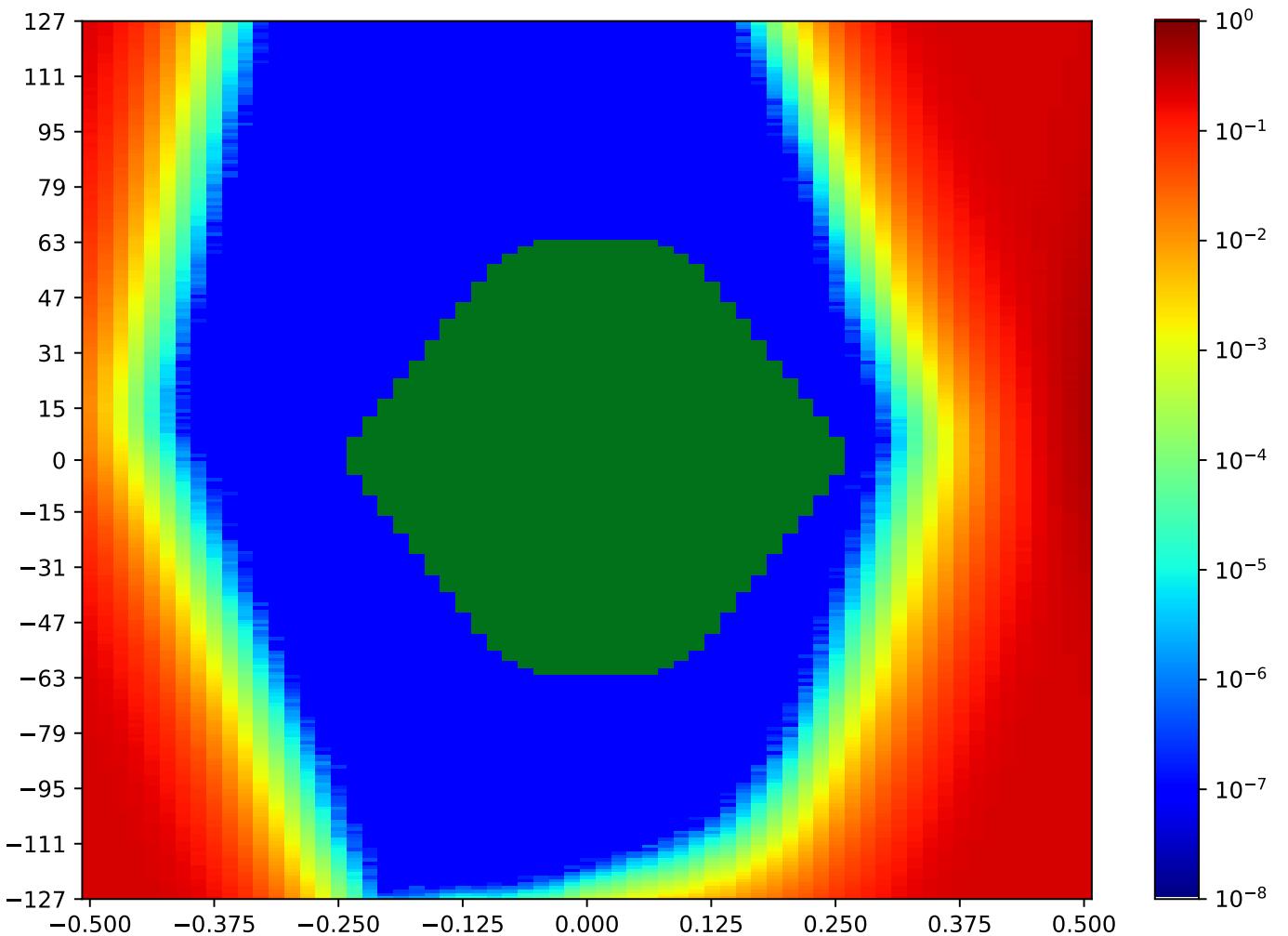


Figure 5.219: MSP_C_FPGA-TX3-04-RX1-04-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.6 MSP_C_FPGA-TX3-05-RX1-05-MSP_A_FPGA

Table 5.203: MSP_C_FPGA-TX3-05-RX1-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:51:20		2018-Sep-27 15:51:40	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8781	44		67.69%	245 95.69%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

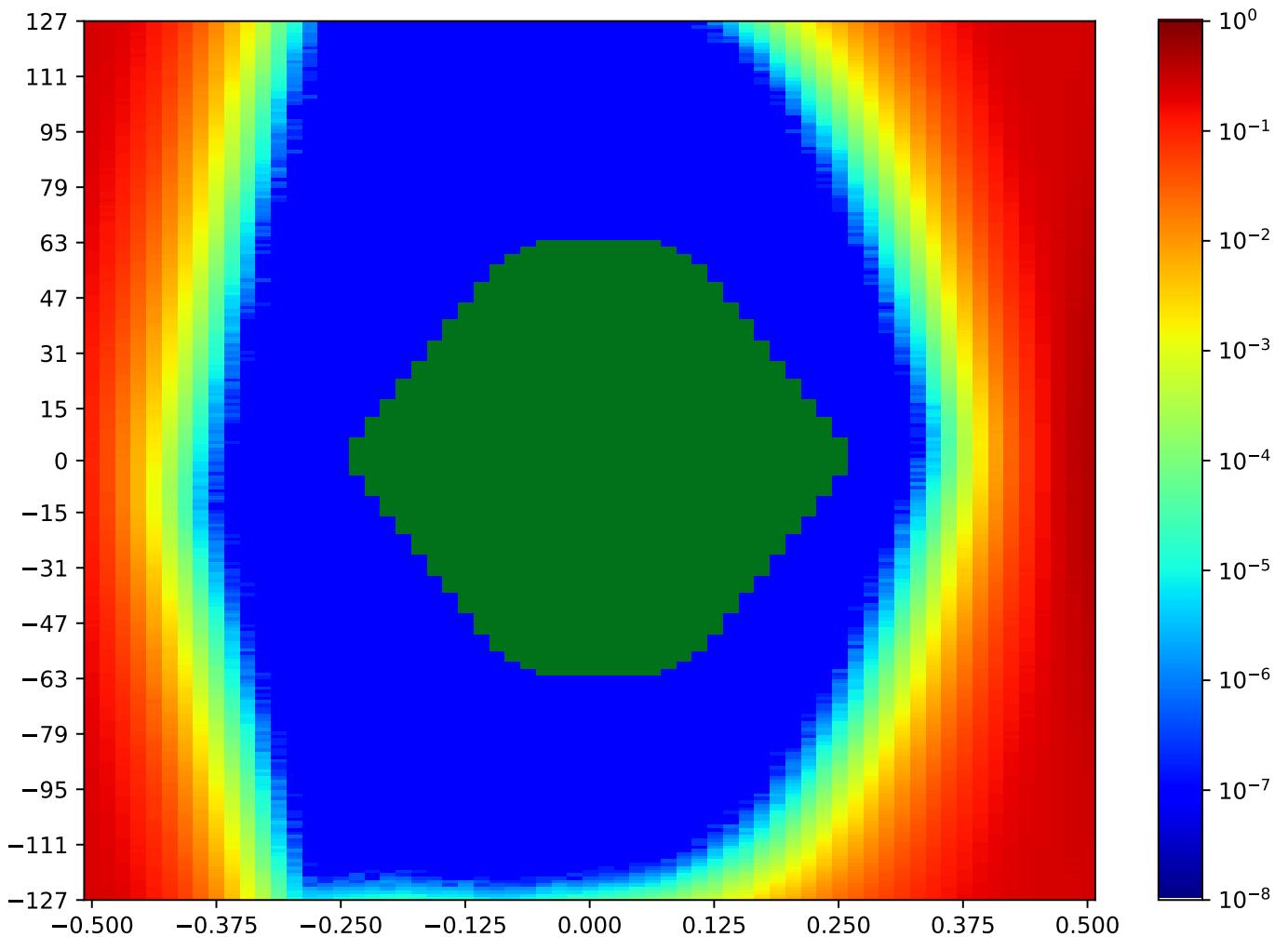


Figure 5.220: MSP_C_FPGA-TX3-05-RX1-05-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.7 MSP_C_FPGA-TX3-06-RX1-06-MSP_A_FPGA

Table 5.204: MSP_C_FPGA-TX3-06-RX1-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:55:05		2018-Sep-27 15:55:26	
Reset RX	OA	HO		VO	VO (%)
true	9711	45		69.23%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

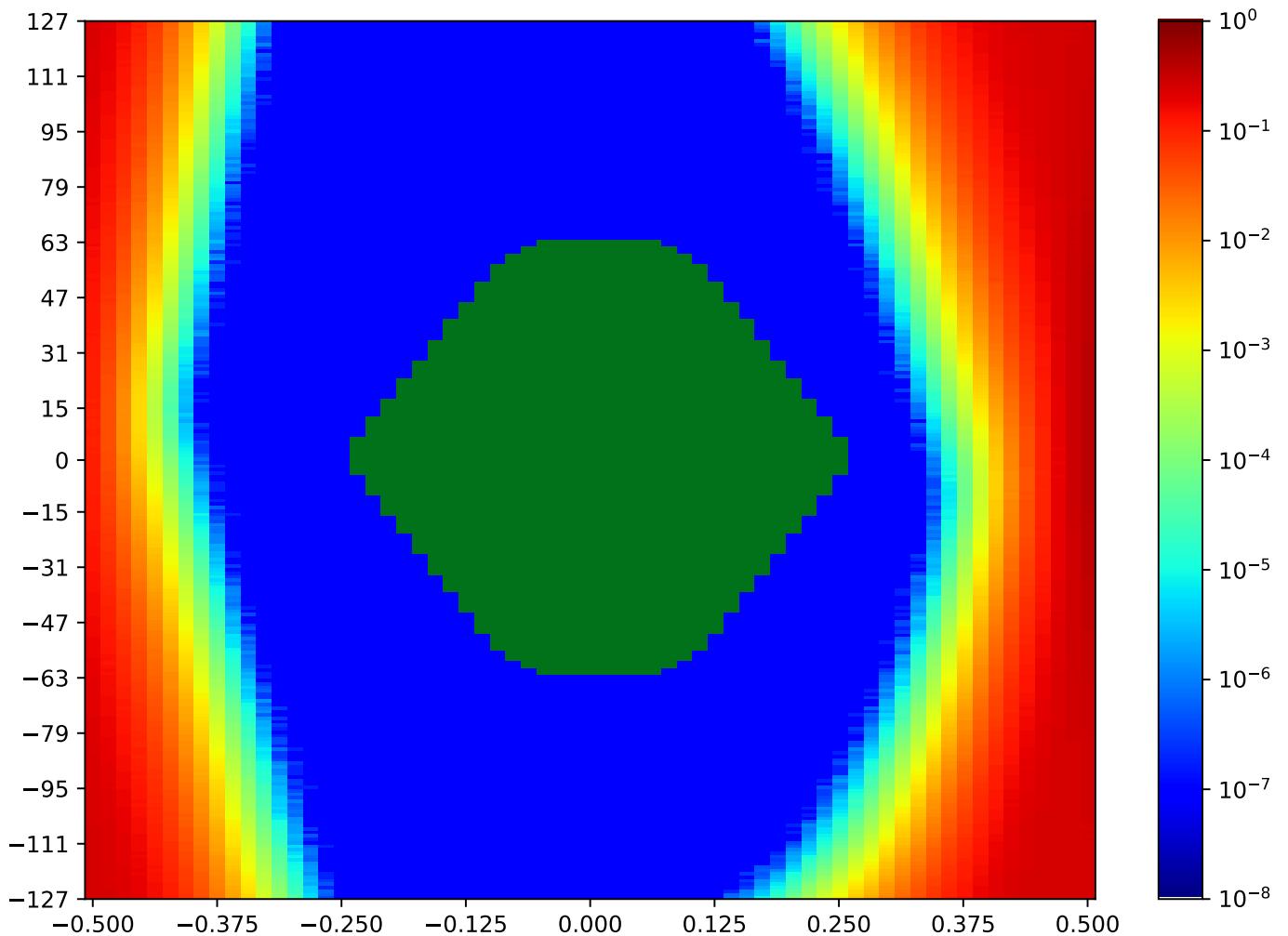


Figure 5.221: MSP_C_FPGA-TX3-06-RX1-06-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.8 MSP_C_FPGA-TX3-07-RX1-07-MSP_A_FPGA

Table 5.205: MSP_C_FPGA-TX3-07-RX1-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:52:01		2018-Sep-27 15:52:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8413	39	60.00%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

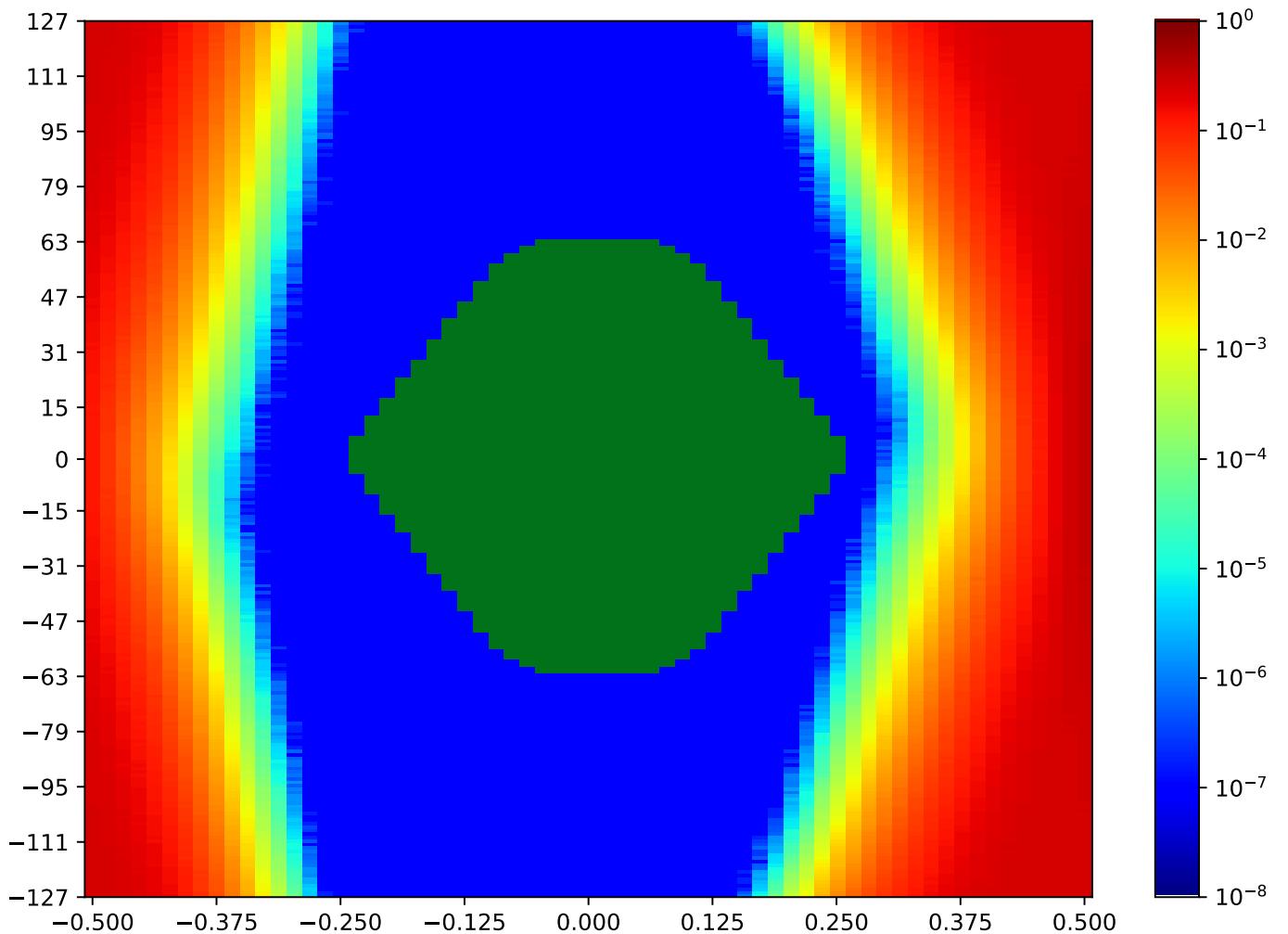


Figure 5.222: MSP_C_FPGA-TX3-07-RX1-07-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.9 MSP_C_FPGA-TX3-08-RX1-08-MSP_A_FPGA

Table 5.206: MSP_C_FPGA-TX3-08-RX1-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:54:45		2018-Sep-27 15:55:05	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9405	45		69.23%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

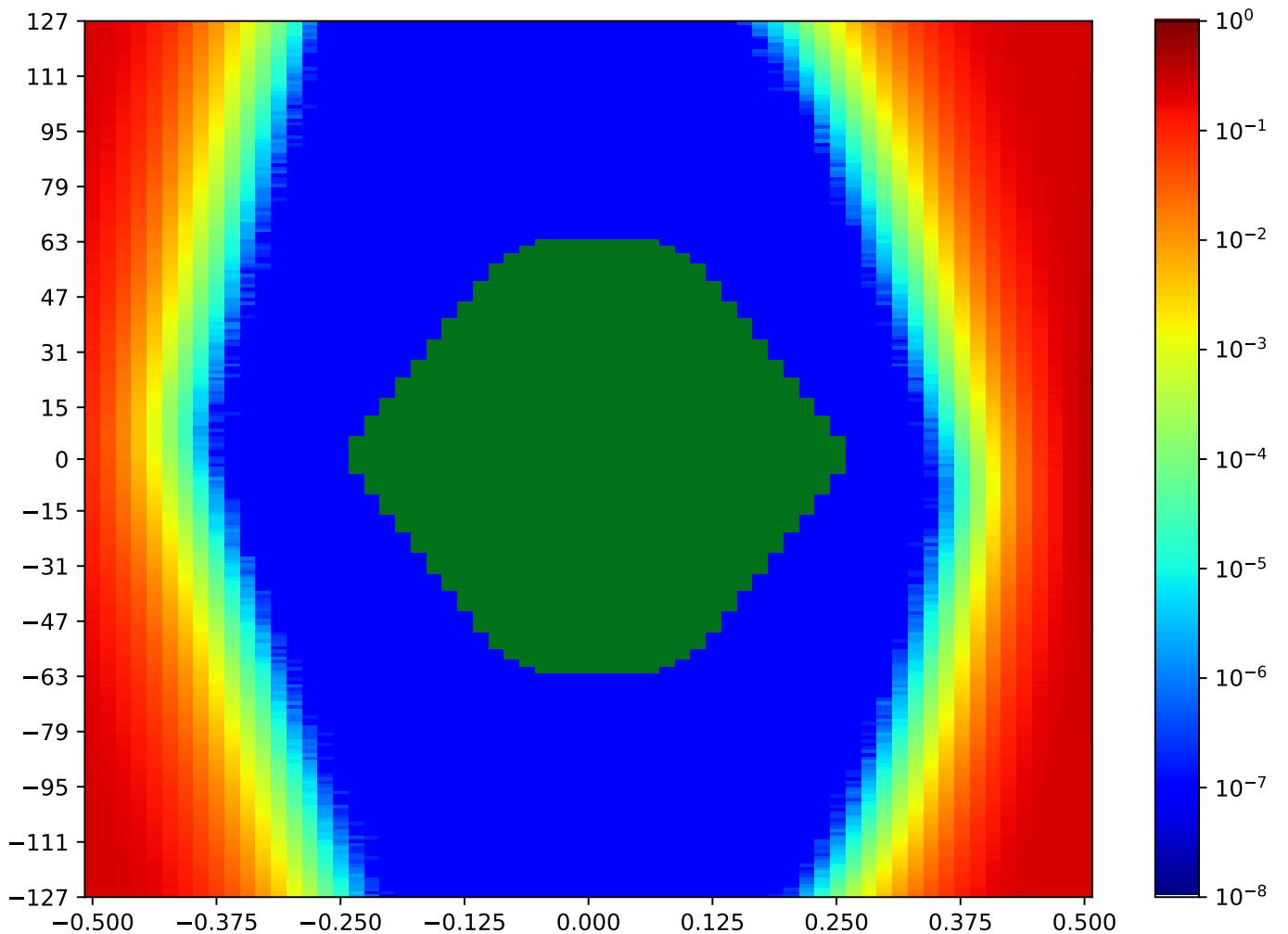


Figure 5.223: MSP_C_FPGA-TX3-08-RX1-08-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.10 MSP_C_FPGA-TX3-09-RX1-09-MSP_A_FPGA

Table 5.207: MSP_C_FPGA-TX3-09-RX1-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:52:42		2018-Sep-27 15:53:02	
Reset RX	OA	HO		VO	VO (%)
true	9412	45		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

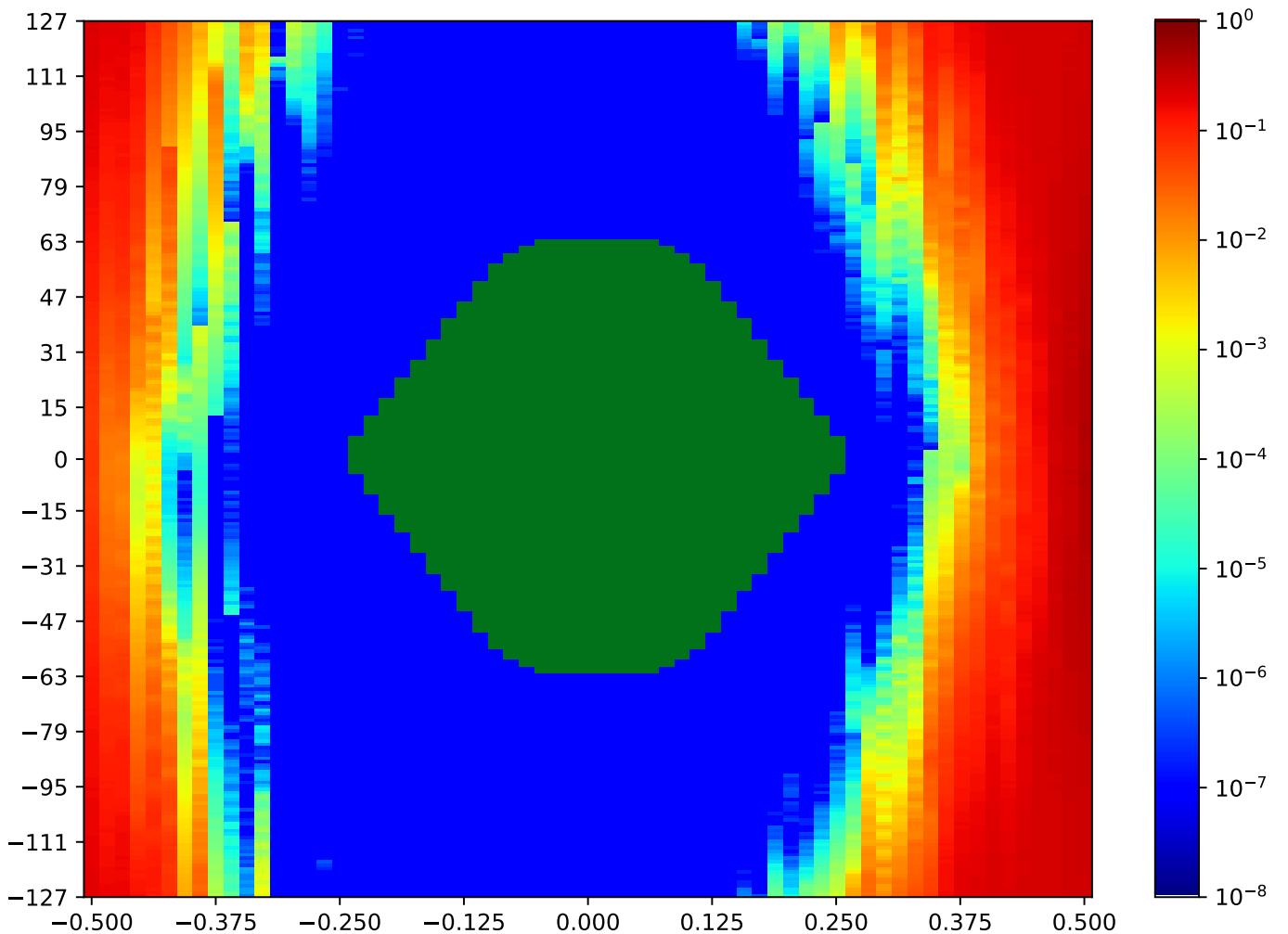


Figure 5.224: MSP_C_FPGA-TX3-09-RX1-09-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.11 MSP_C_FPGA-TX3-10-RX1-10-MSP_A_FPGA

Table 5.208: MSP_C_FPGA-TX3-10-RX1-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:54:04		2018-Sep-27 15:54:24	
Reset RX	OA	HO		VO	VO (%)
true	9140	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

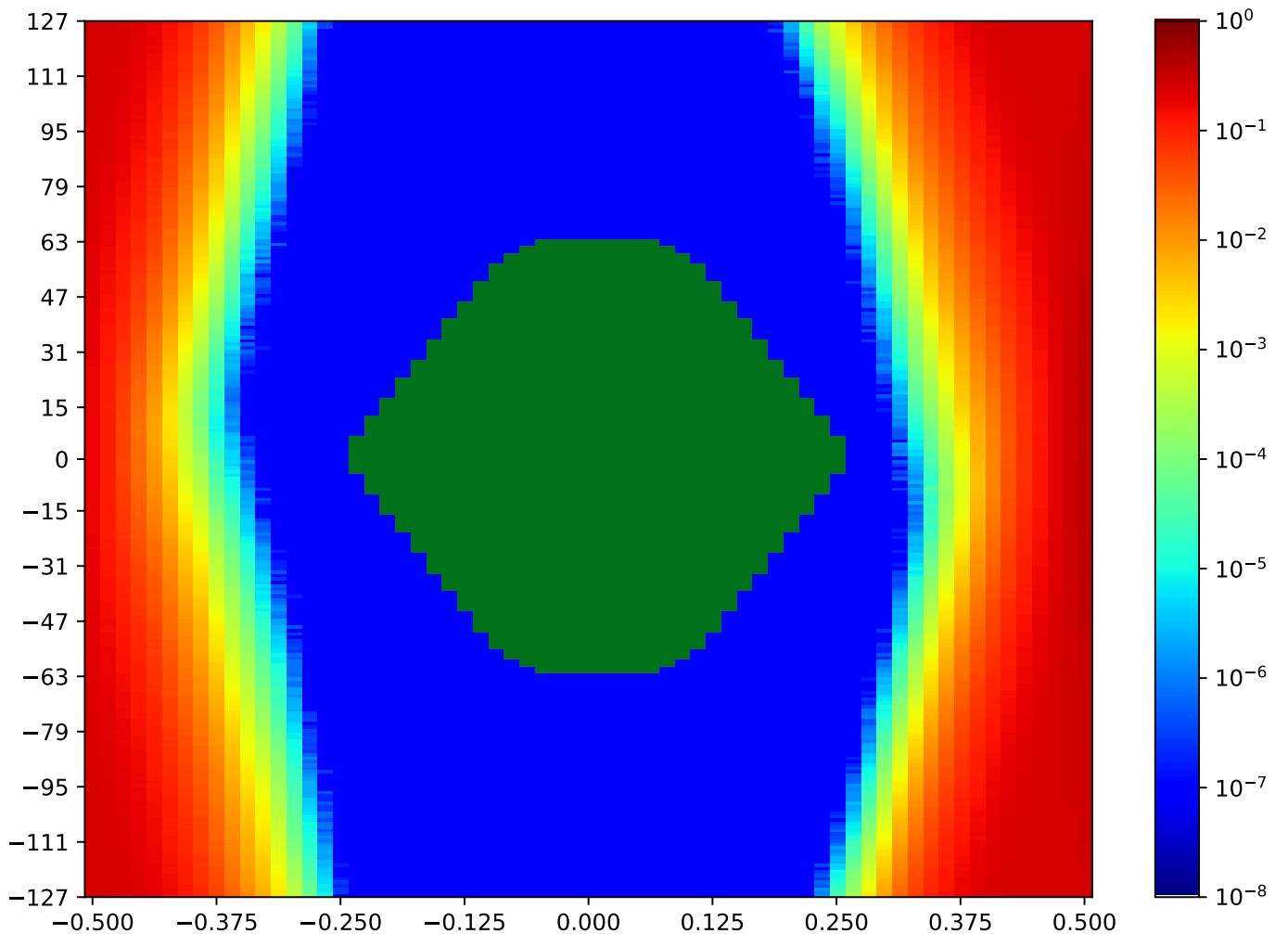


Figure 5.225: MSP_C_FPGA-TX3-10-RX1-10-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.17.12 MSP_C_FPGA-TX3-11-RX1-11-MSP_A_FPGA

Table 5.209: MSP_C_FPGA-TX3-11-RX1-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:53:43		2018-Sep-27 15:54:04	
Reset RX	OA	HO		VO	VO (%)
true	9606	45		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

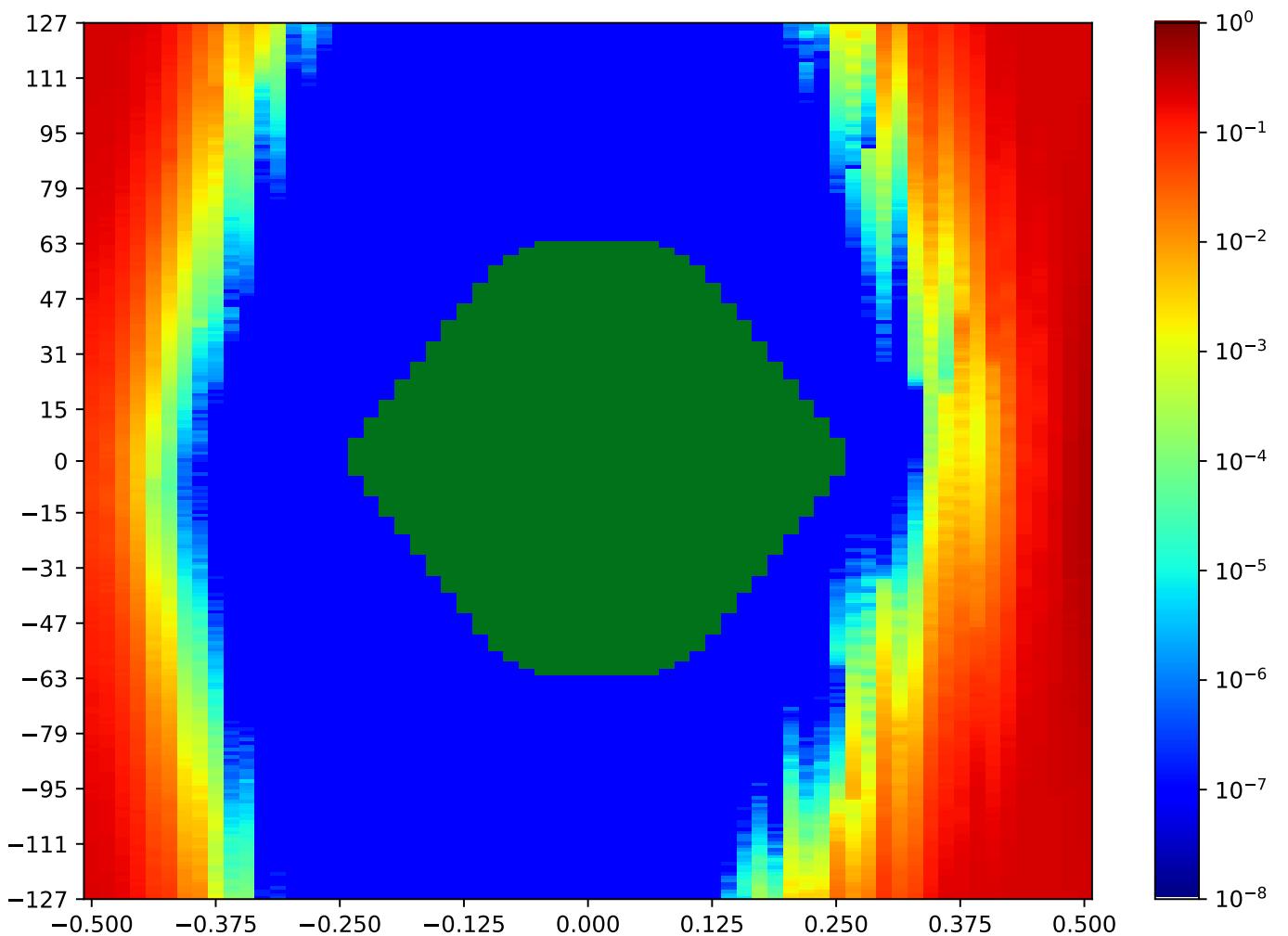


Figure 5.226: MSP_C_FPGA-TX3-11-RX1-11-MSP_A_FPGA

Call back to summary Figure 5.214. Sibling eye diagrams: V2-6.4.

5.18 MSP_C TX4 MSP_A RX2 Minipod Loopback

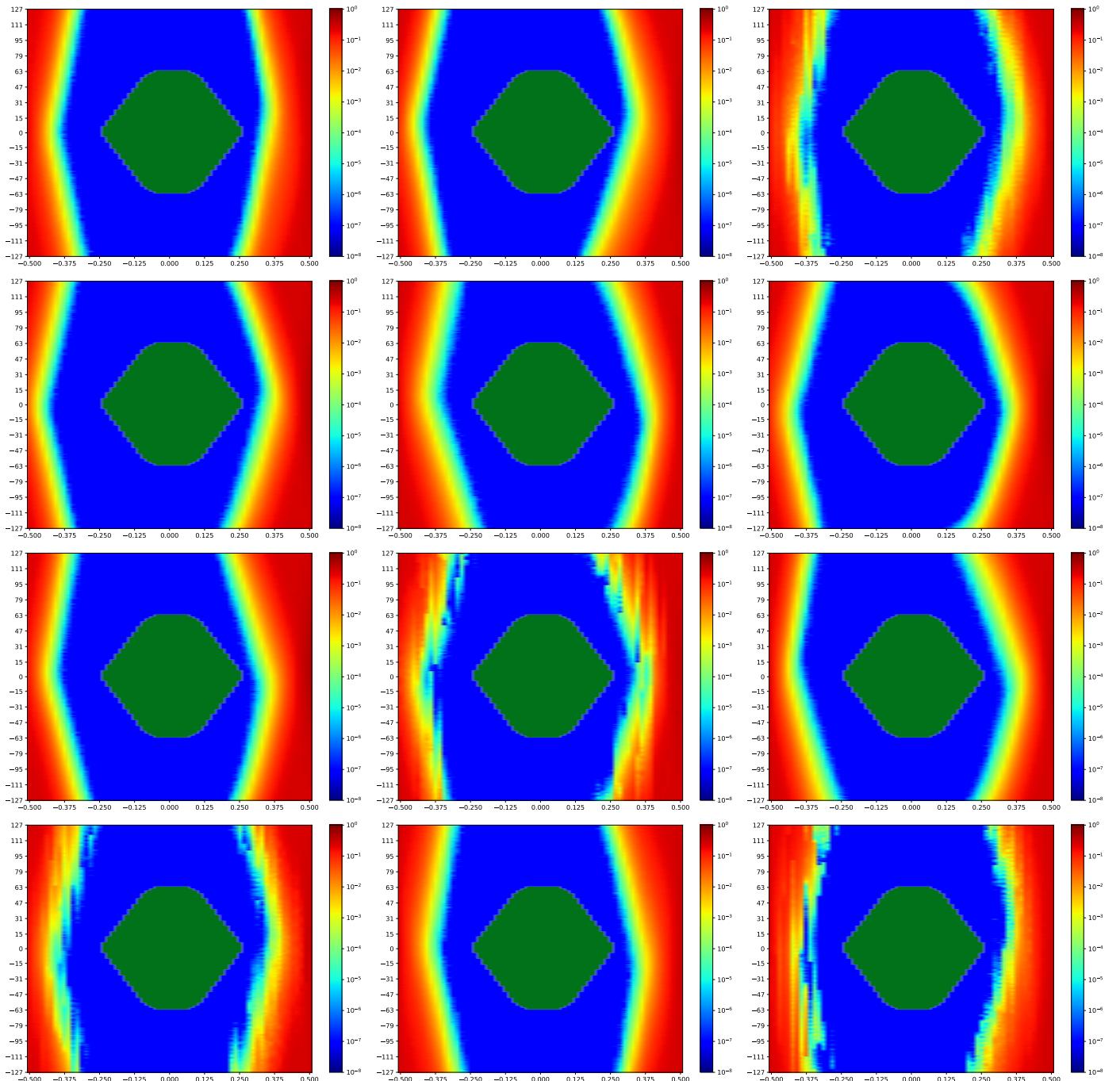


Figure 5.227: MSP_C TX4 MSP_A RX2 Minipod Loopback

A cross-reference to Figure 5.227. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.240.

5.18.1 MSP_C_FPGA-TX4-00-RX2-00-MSP_A_FPGA

Table 5.210: MSP_C_FPGA-TX4-00-RX2-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:56:27		2018-Sep-27 15:56:48	
Reset RX	OA	HO		VO	VO (%)
true	9794	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

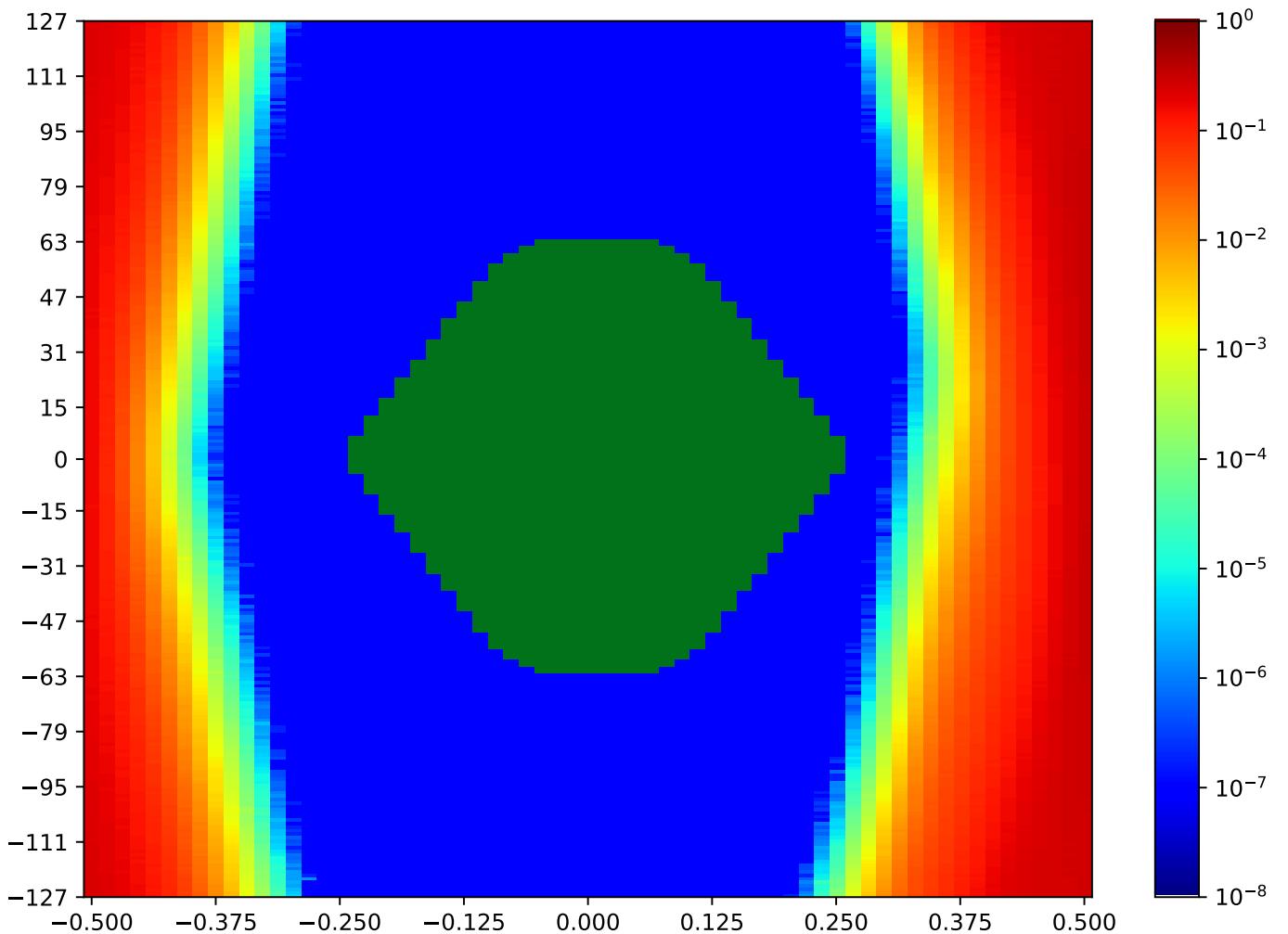


Figure 5.228: MSP_C_FPGA-TX4-00-RX2-00-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.2 MSP_C_FPGA-TX4-01-RX2-01-MSP_A_FPGA

Table 5.211: MSP_C_FPGA-TX4-01-RX2-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:55:46		2018-Sep-27 15:56:06	
Reset RX	OA	HO		VO	VO (%)
true	9510	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

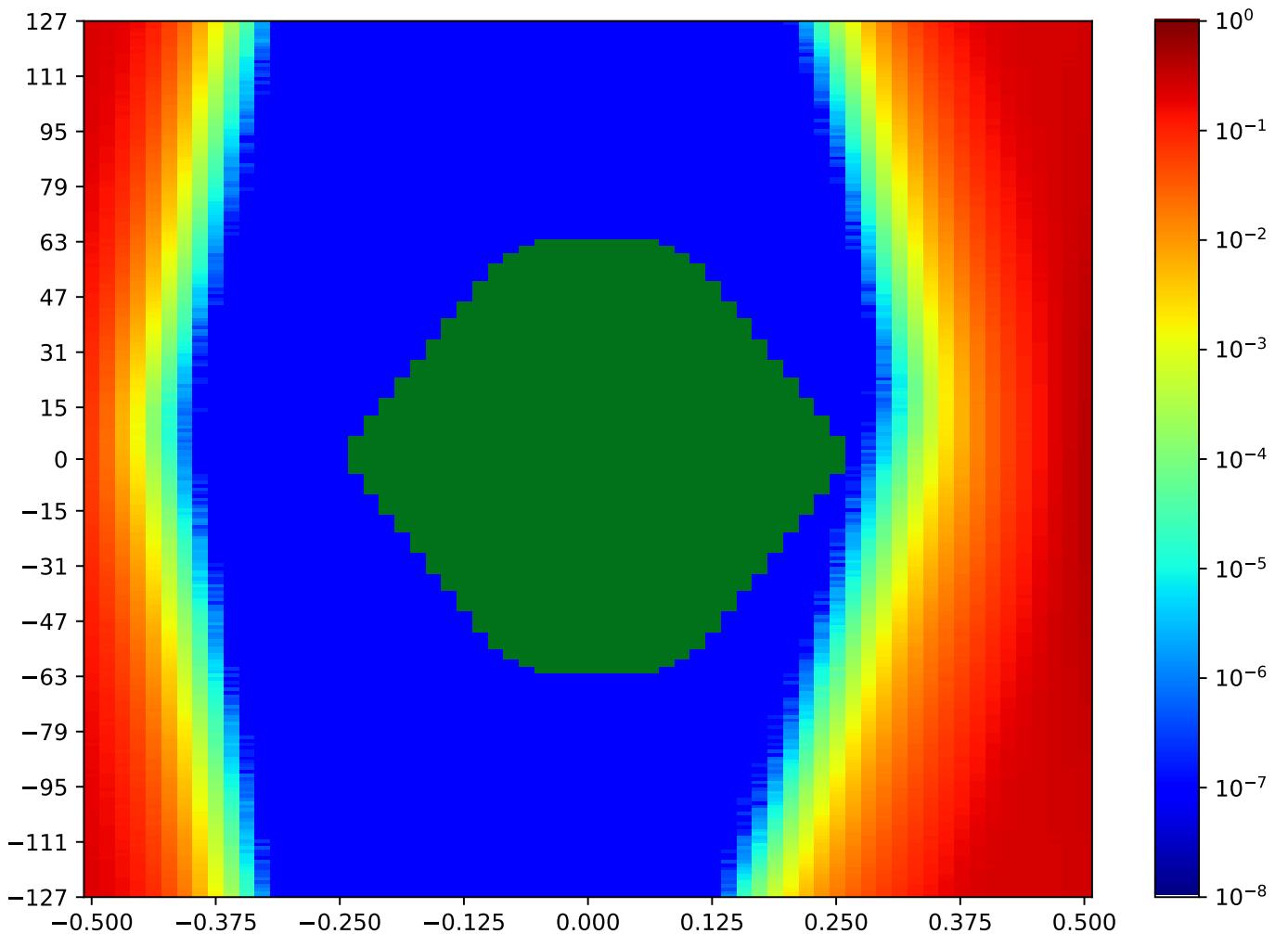


Figure 5.229: MSP_C_FPGA-TX4-01-RX2-01-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.3 MSP_C_FPGA-TX4-02-RX2-02-MSP_A_FPGA

Table 5.212: MSP_C_FPGA-TX4-02-RX2-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:57:29		2018-Sep-27 15:57:49	
Reset RX	OA	HO		VO	VO (%)
true	9230	42		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

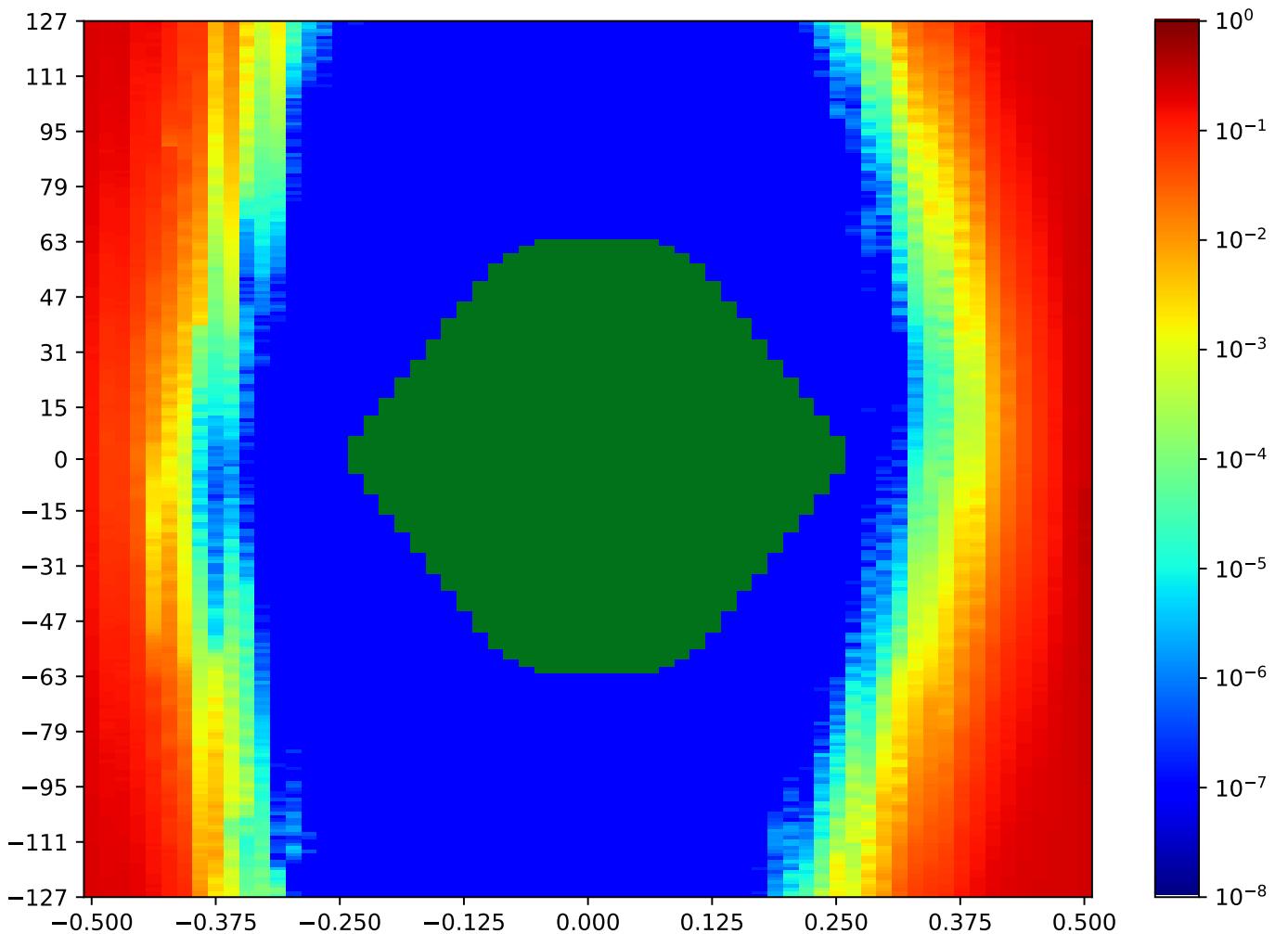


Figure 5.230: MSP_C_FPGA-TX4-02-RX2-02-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.4 MSP_C_FPGA-TX4-03-RX2-03-MSP_A_FPGA

Table 5.213: MSP_C_FPGA-TX4-03-RX2-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:55:26		2018-Sep-27 15:55:46	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9979	45		69.23%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

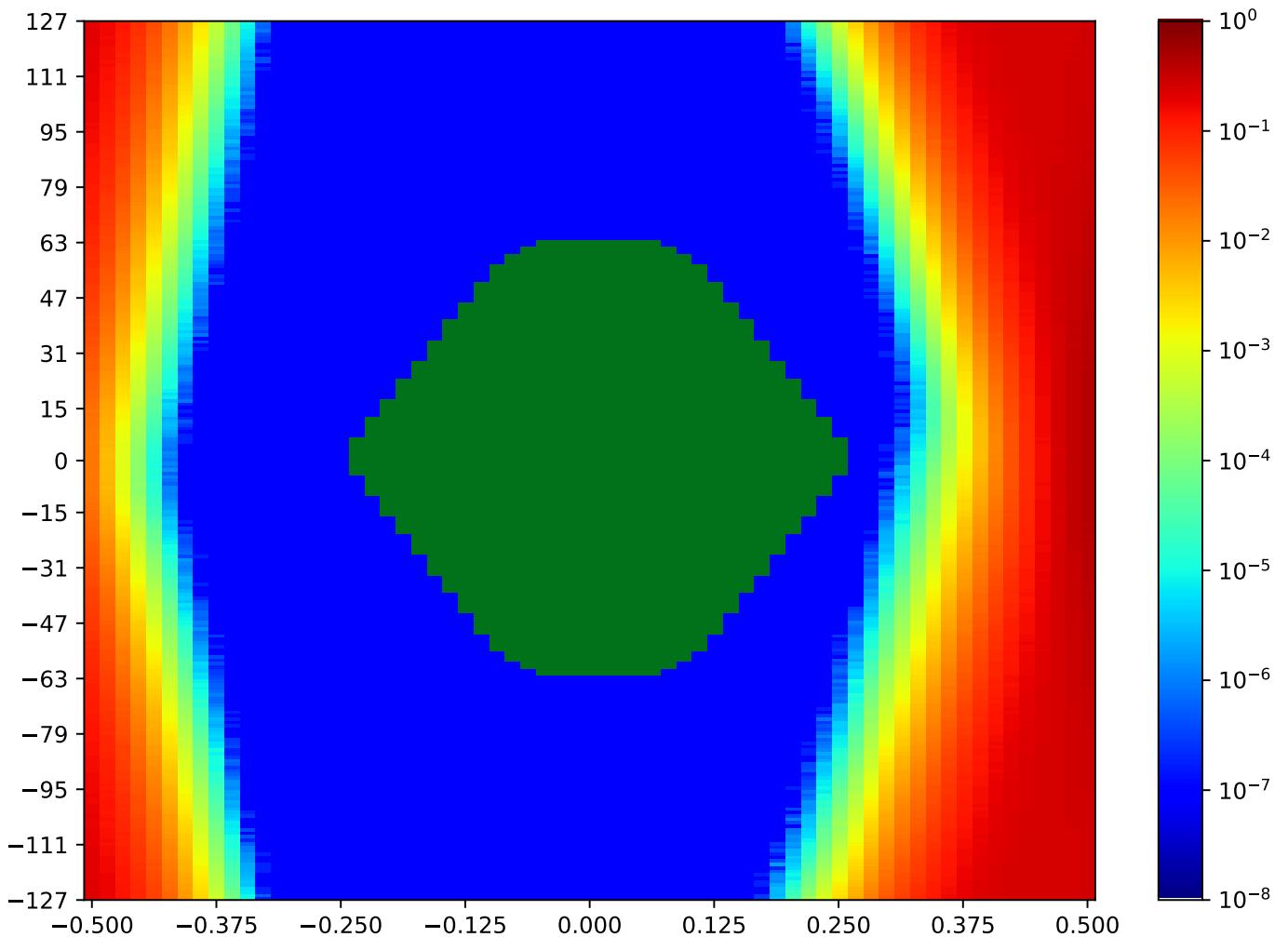


Figure 5.231: MSP_C_FPGA-TX4-03-RX2-03-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.5 MSP_C_FPGA-TX4-04-RX2-04-MSP_A_FPGA

Table 5.214: MSP_C_FPGA-TX4-04-RX2-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:58:31		2018-Sep-27 15:58:51	
Reset RX	OA	HO		VO	VO (%)
true	8997	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

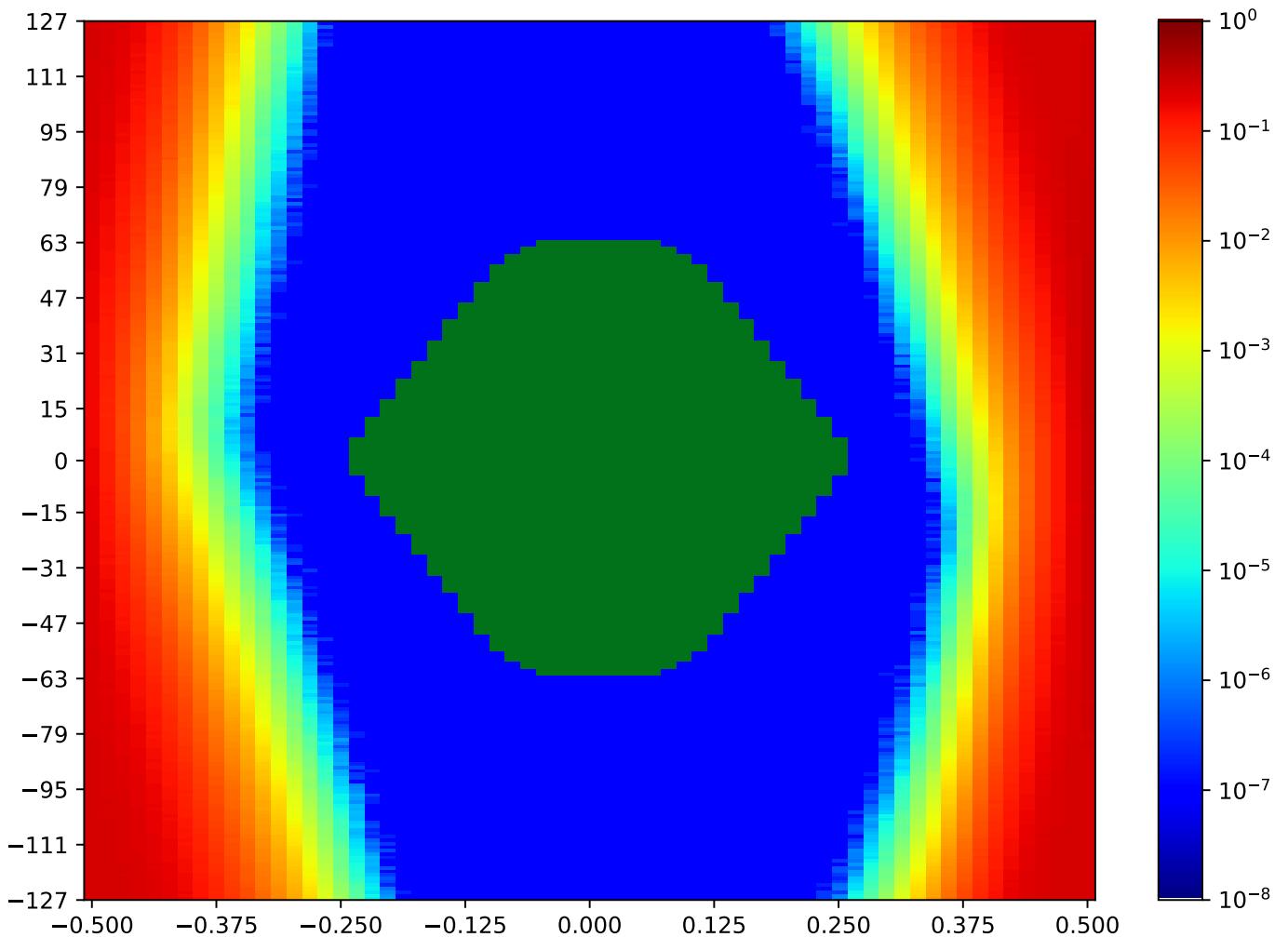


Figure 5.232: MSP_C_FPGA-TX4-04-RX2-04-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.6 MSP_C_FPGA-TX4-05-RX2-05-MSP_A_FPGA

Table 5.215: MSP_C_FPGA-TX4-05-RX2-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:56:07		2018-Sep-27 15:56:27	
Reset RX	OA	HO		VO	VO (%)
true	9196	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

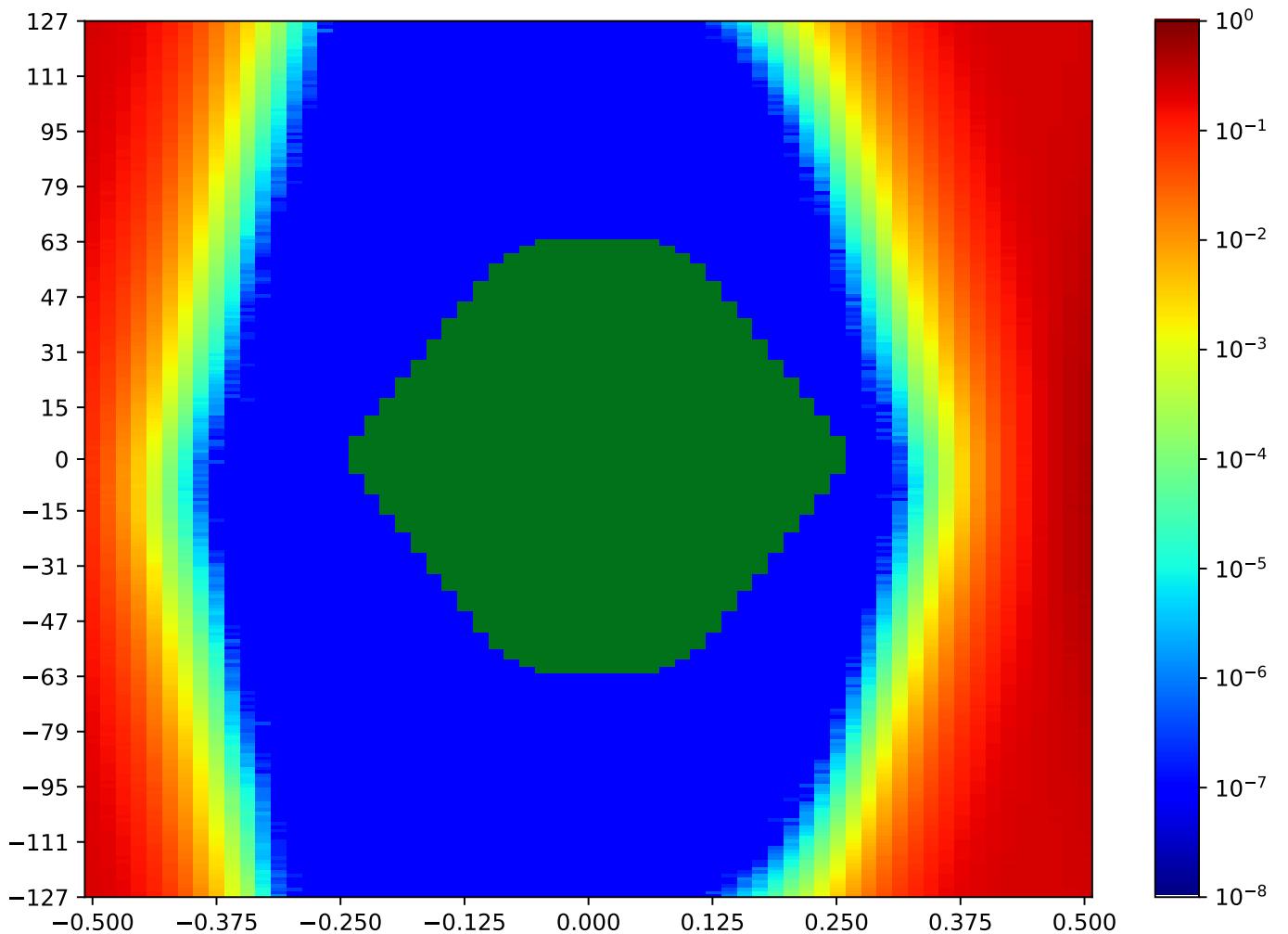


Figure 5.233: MSP_C_FPGA-TX4-05-RX2-05-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.7 MSP_C_FPGA-TX4-06-RX2-06-MSP_A_FPGA

Table 5.216: MSP_C_FPGA-TX4-06-RX2-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:59:12		2018-Sep-27 15:59:32	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9232	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

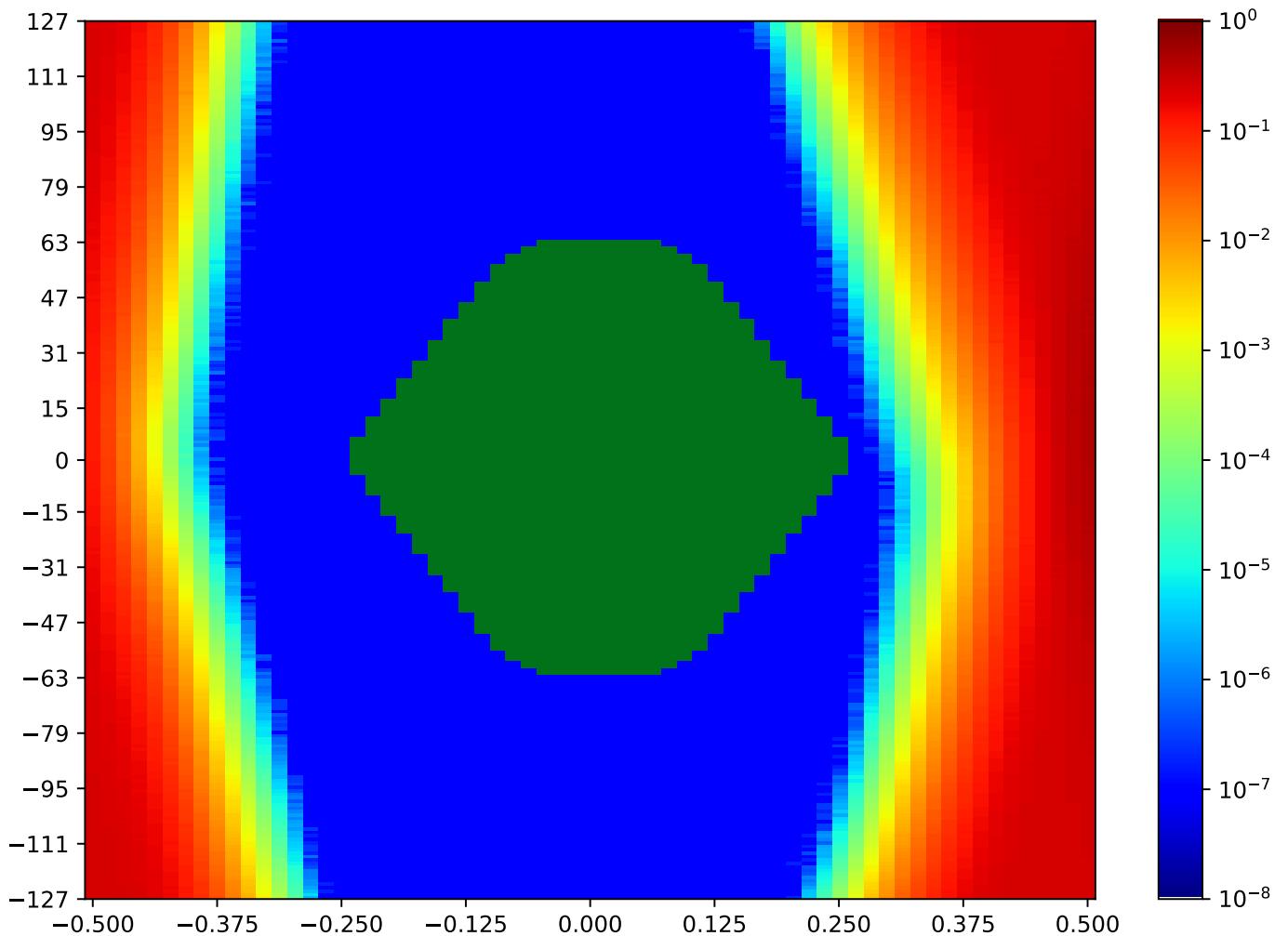


Figure 5.234: MSP_C_FPGA-TX4-06-RX2-06-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.8 MSP_C_FPGA-TX4-07-RX2-07-MSP_A_FPGA

Table 5.217: MSP_C_FPGA-TX4-07-RX2-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:56:48		2018-Sep-27 15:57:09	
Reset RX	OA	HO		VO	VO (%)
true	9307	44		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

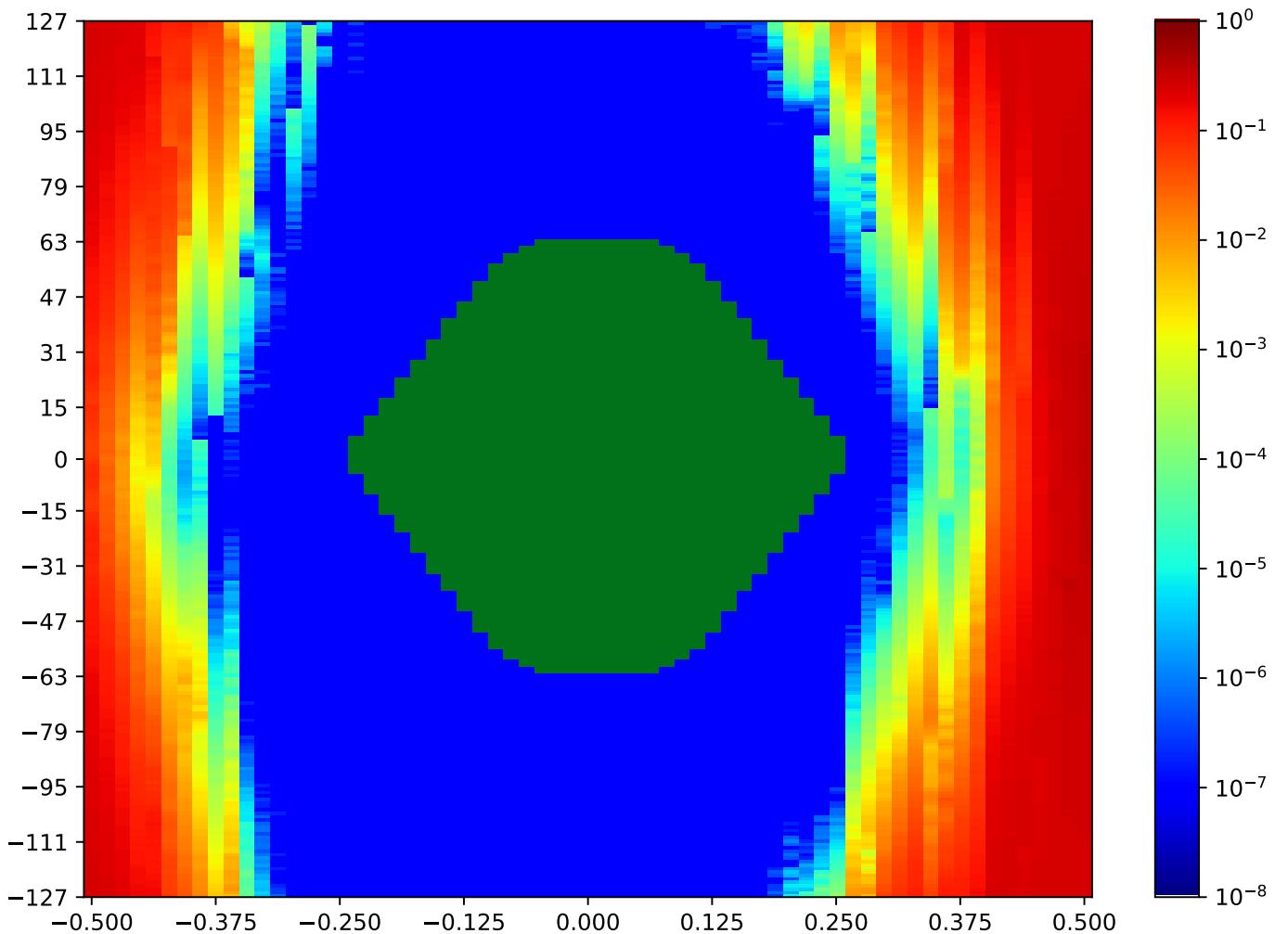


Figure 5.235: MSP_C_FPGA-TX4-07-RX2-07-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.9 MSP_C_FPGA-TX4-08-RX2-08-MSP_A_FPGA

Table 5.218: MSP_C_FPGA-TX4-08-RX2-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:58:51		2018-Sep-27 15:59:11	
Reset RX	OA	HO		VO	VO (%)
true	9211	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

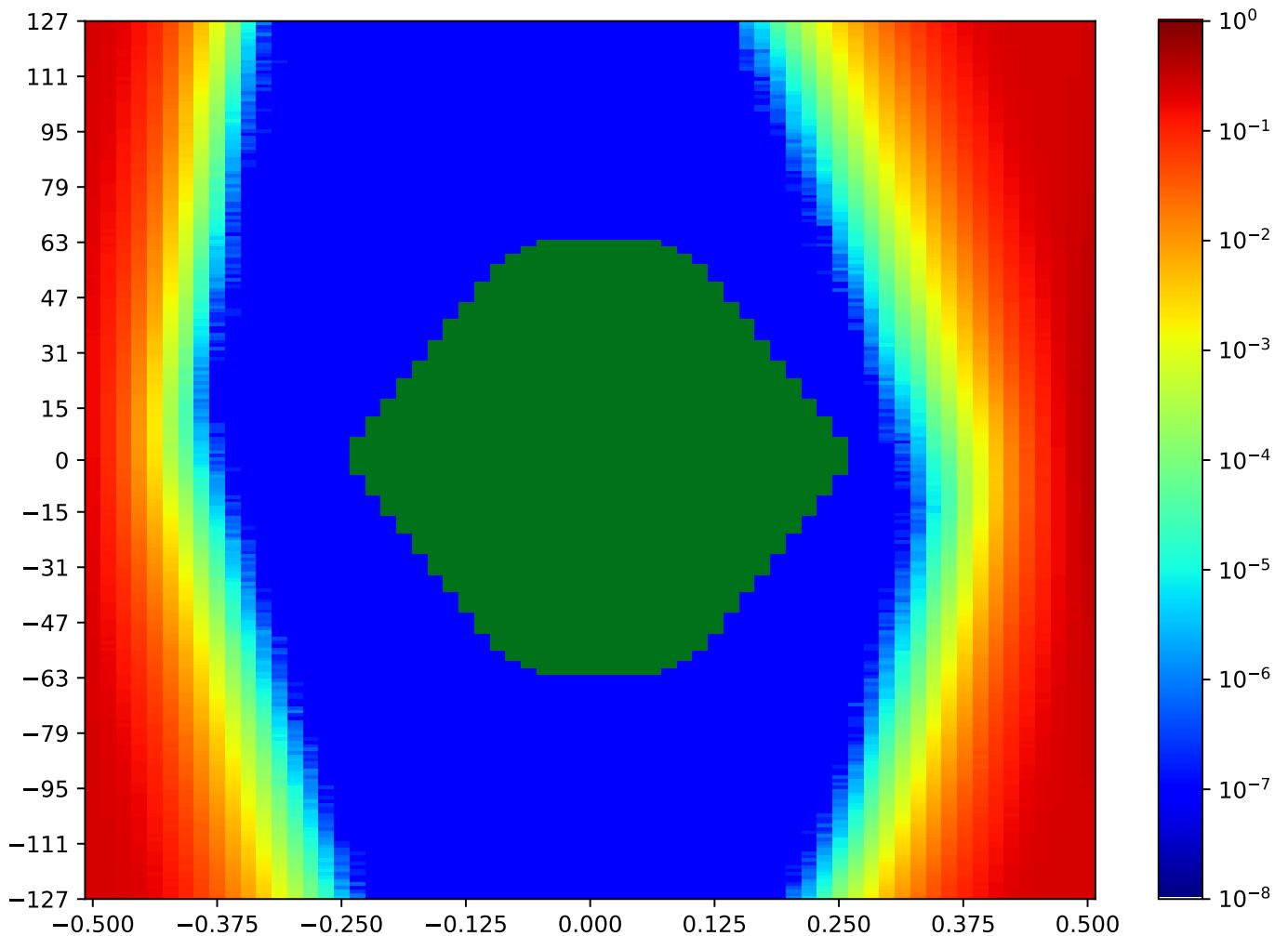


Figure 5.236: MSP_C_FPGA-TX4-08-RX2-08-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.10 MSP_C_FPGA-TX4-09-RX2-09-MSP_A_FPGA

Table 5.219: MSP_C_FPGA-TX4-09-RX2-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:57:09		2018-Sep-27 15:57:29	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9500	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

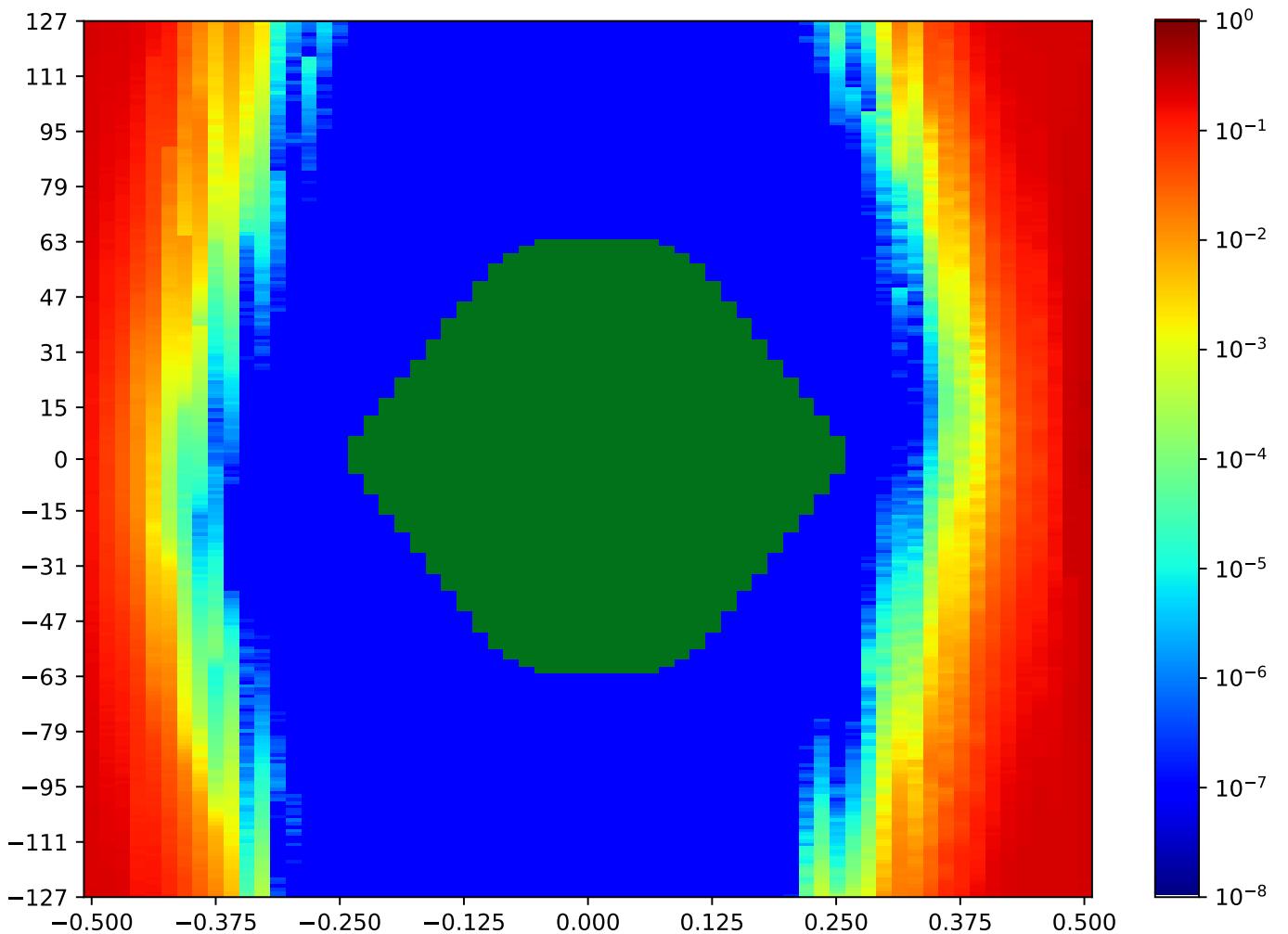


Figure 5.237: MSP_C_FPGA-TX4-09-RX2-09-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.11 MSP_C_FPGA-TX4-10-RX2-10-MSP_A_FPGA

Table 5.220: MSP_C_FPGA-TX4-10-RX2-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:58:10		2018-Sep-27 15:58:31	
Reset RX	OA	HO		VO	VO (%)
true	9294	40		61.54%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

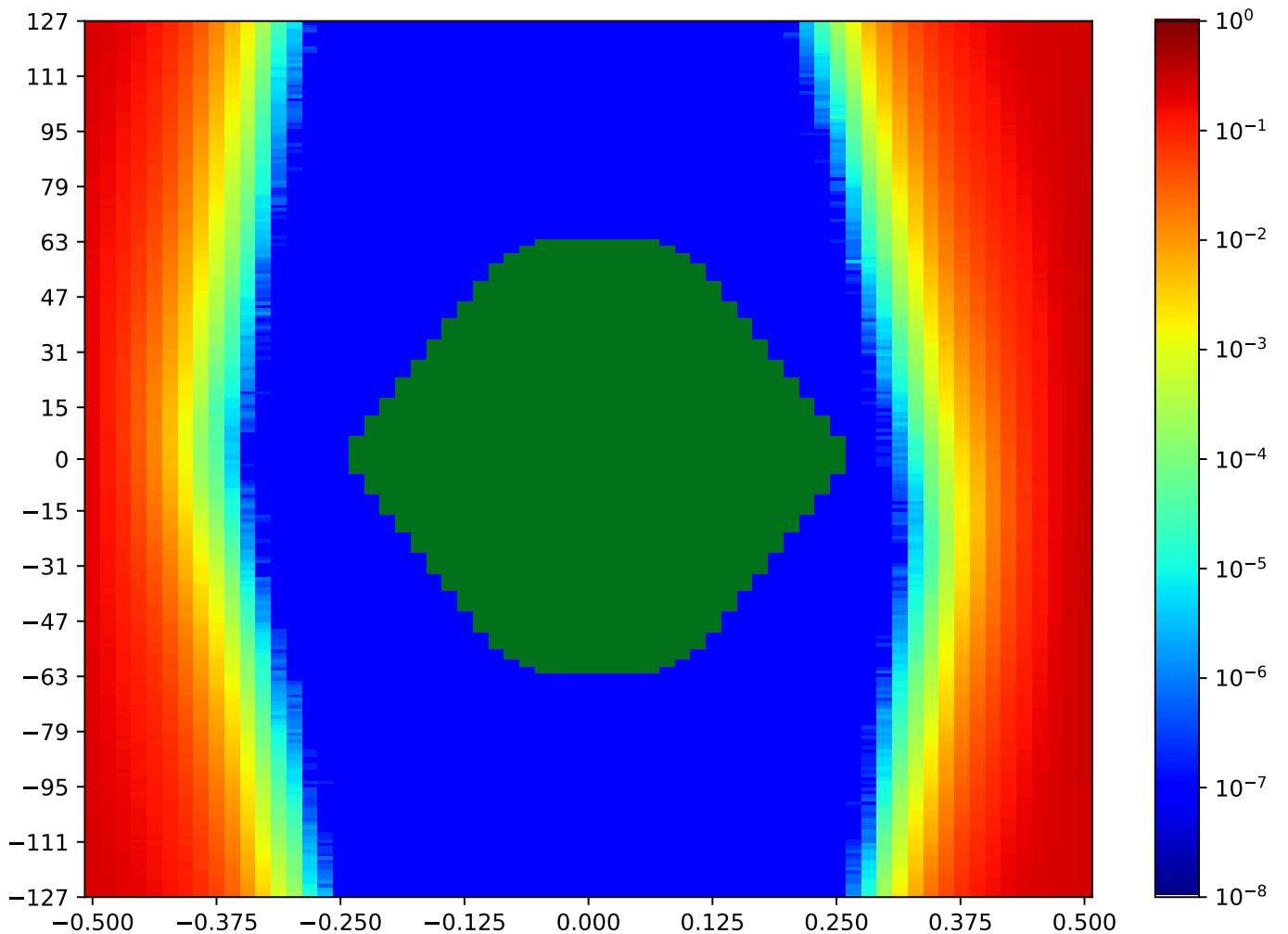


Figure 5.238: MSP_C_FPGA-TX4-10-RX2-10-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.18.12 MSP_C_FPGA-TX4-11-RX2-11-MSP_A_FPGA

Table 5.221: MSP_C_FPGA-TX4-11-RX2-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:57:50		2018-Sep-27 15:58:10	
Reset RX	OA	HO		VO	VO (%)
true	9660	43		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

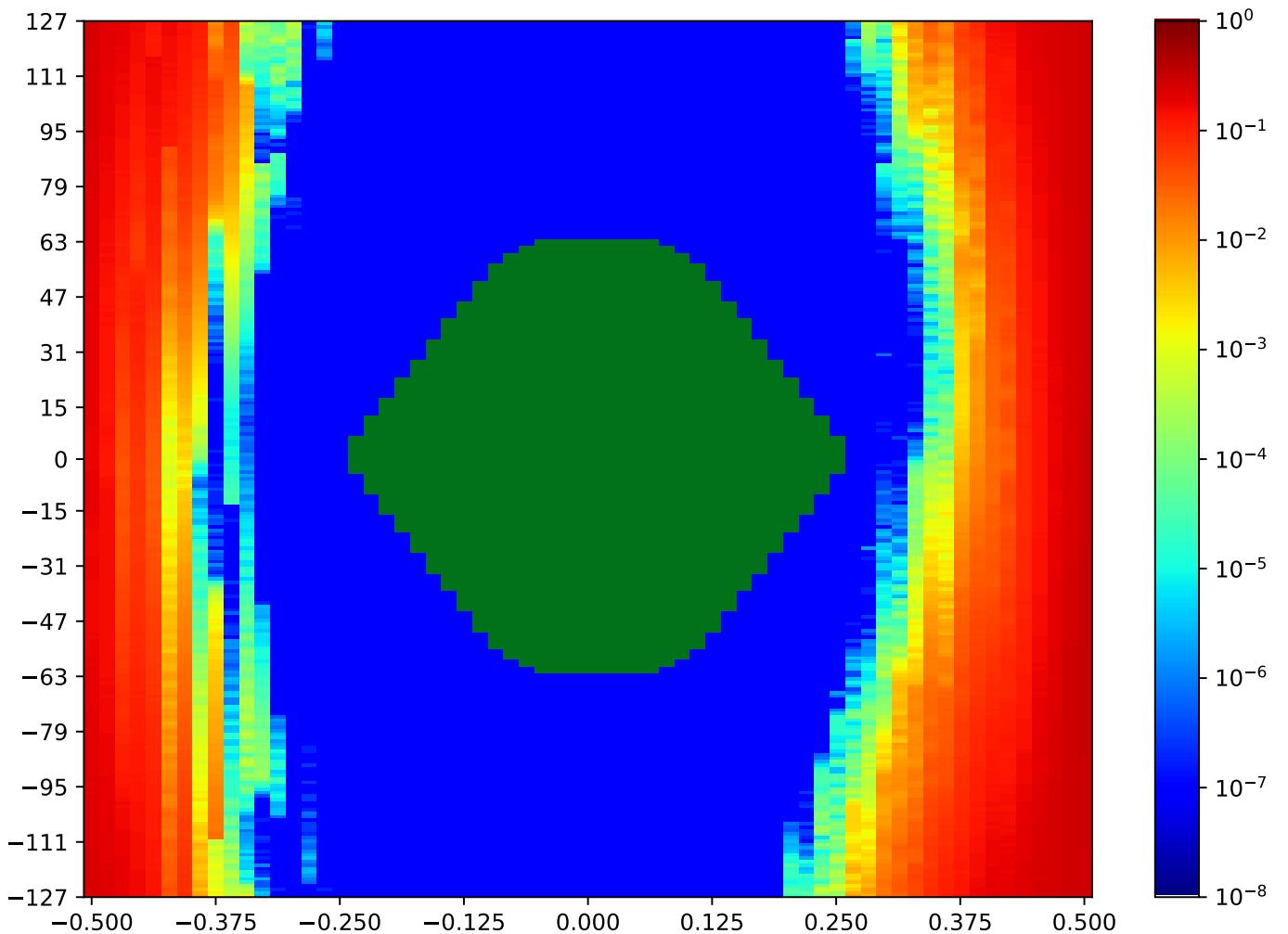


Figure 5.239: MSP_C_FPGA-TX4-11-RX2-11-MSP_A_FPGA

Call back to summary Figure 5.227. Sibling eye diagrams: V2-6.4.

5.19 MSP_A TX1 MSP_C RX12 Minipod Loopback

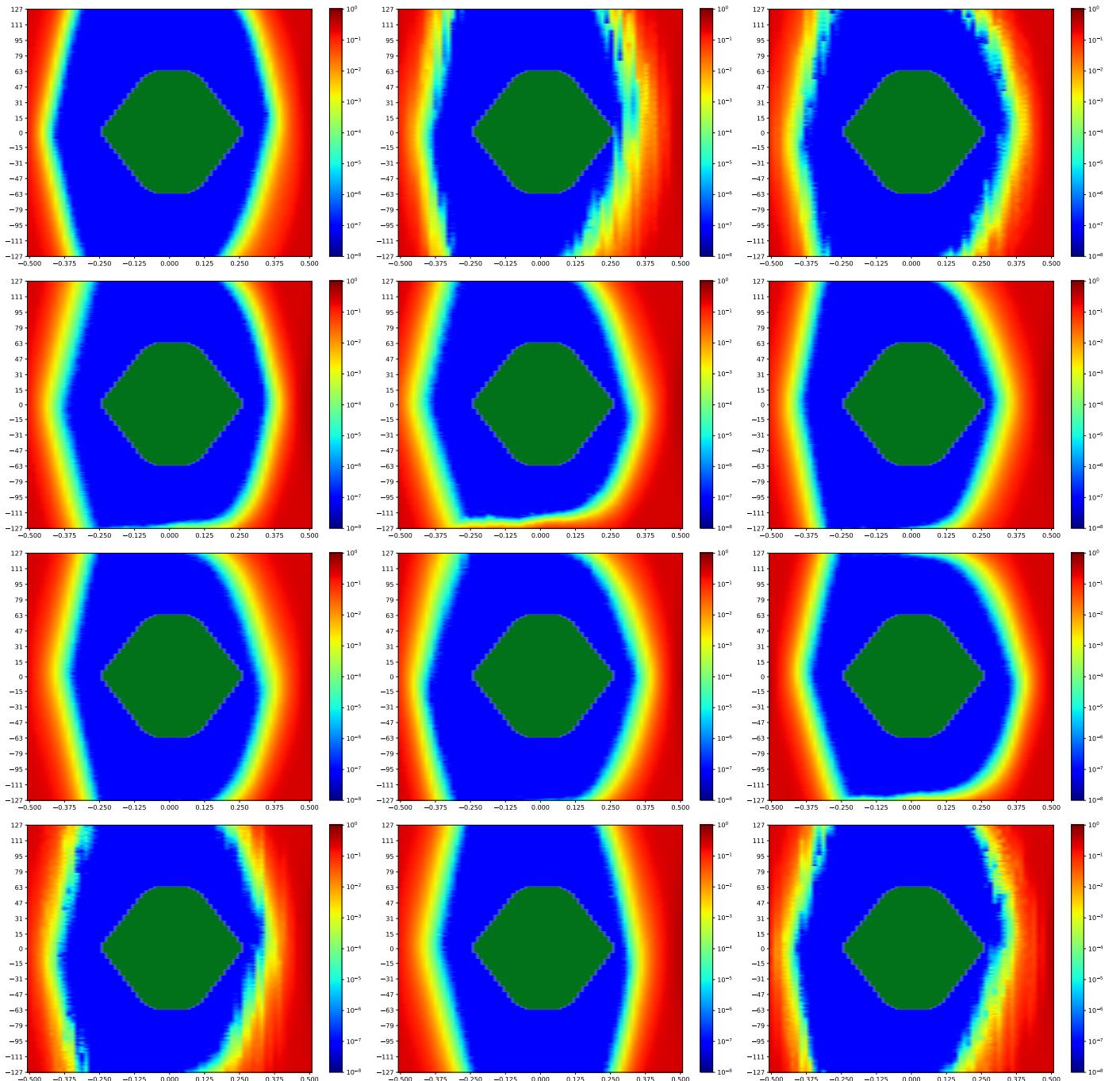


Figure 5.240: MSP_A TX1 MSP_C RX12 Minipod Loopback

A cross-reference to Figure 5.240. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.253.

5.19.1 MSP_A_FPGA-TX1-00-RX12-00-MSP_C_FPGA

Table 5.222: MSP_A_FPGA-TX1-00-RX12-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:23:29		2018-Sep-27 15:23:49	
Reset RX	OA	HO		VO	VO (%)
true	10244	46		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

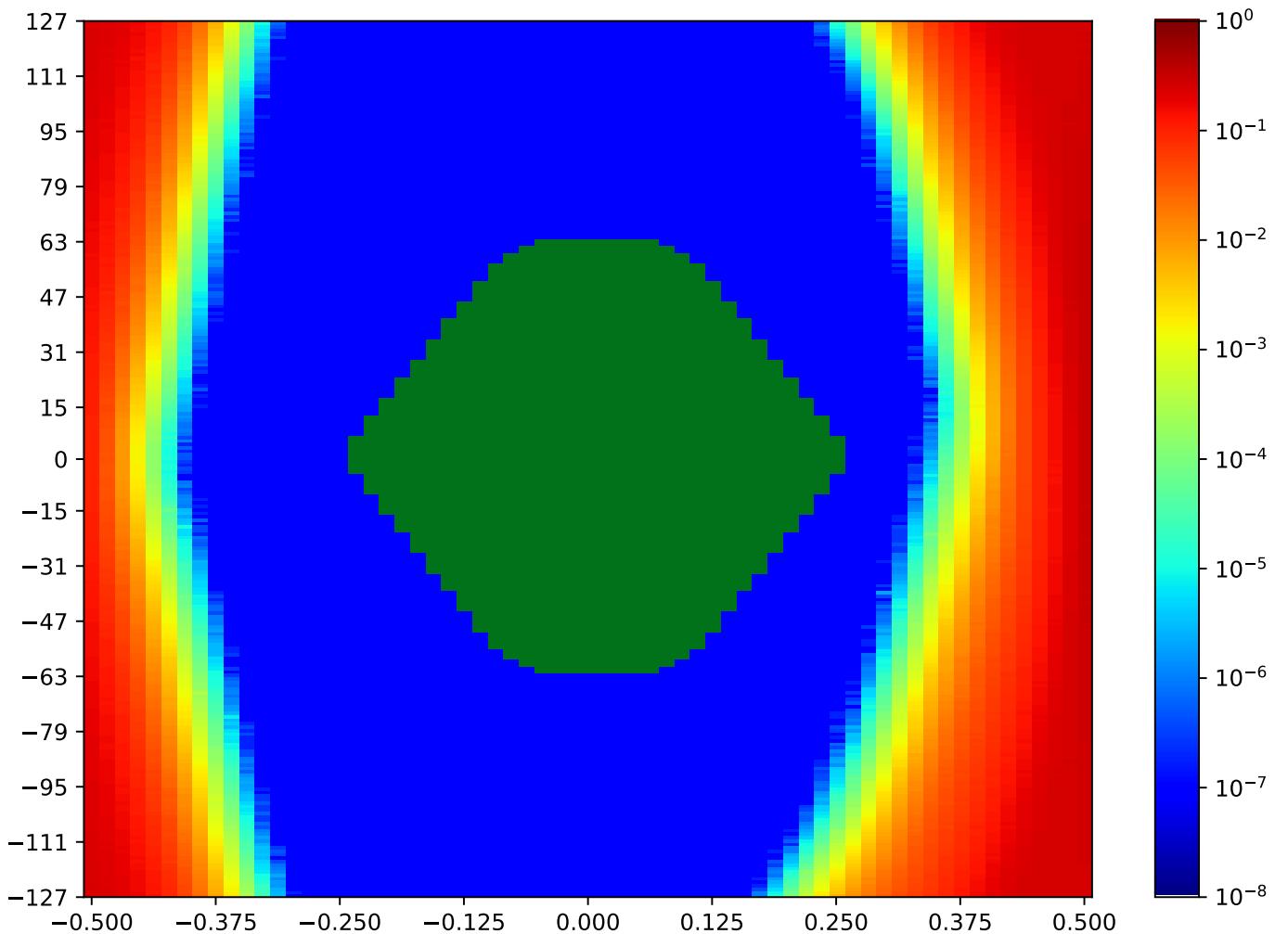


Figure 5.241: MSP_A_FPGA-TX1-00-RX12-00-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.2 MSP_A_FPGA-TX1-01-RX12-01-MSP_C_FPGA

Table 5.223: MSP_A_FPGA-TX1-01-RX12-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:24:10		2018-Sep-27 15:24:30	
Reset RX	OA	HO		VO	VO (%)
true	8915	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

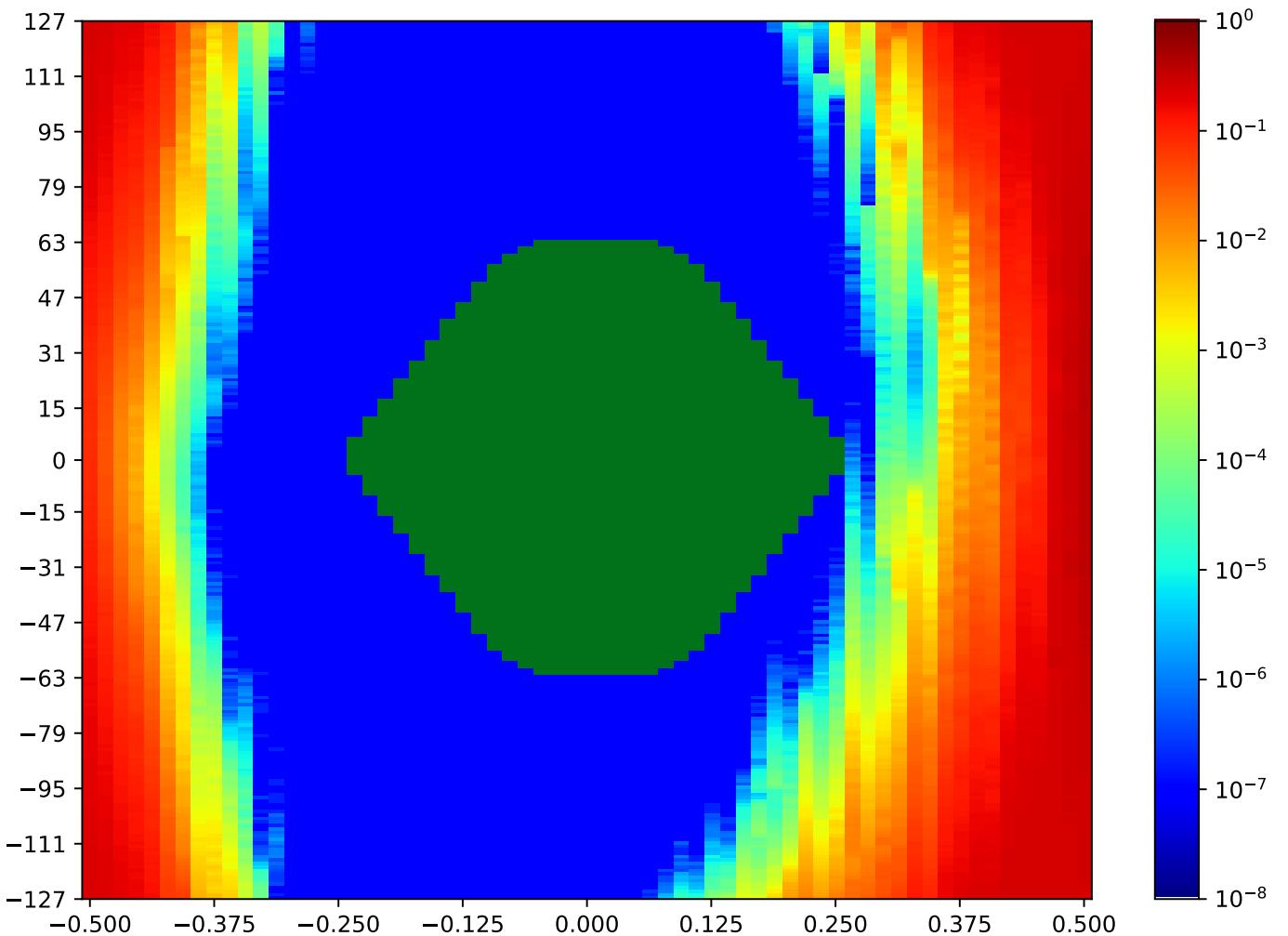


Figure 5.242: MSP_A_FPGA-TX1-01-RX12-01-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.3 MSP_A_FPGA-TX1-02-RX12-02-MSP_C_FPGA

Table 5.224: MSP_A_FPGA-TX1-02-RX12-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:24:30		2018-Sep-27 15:24:51	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9255	43	64.62%	254	99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

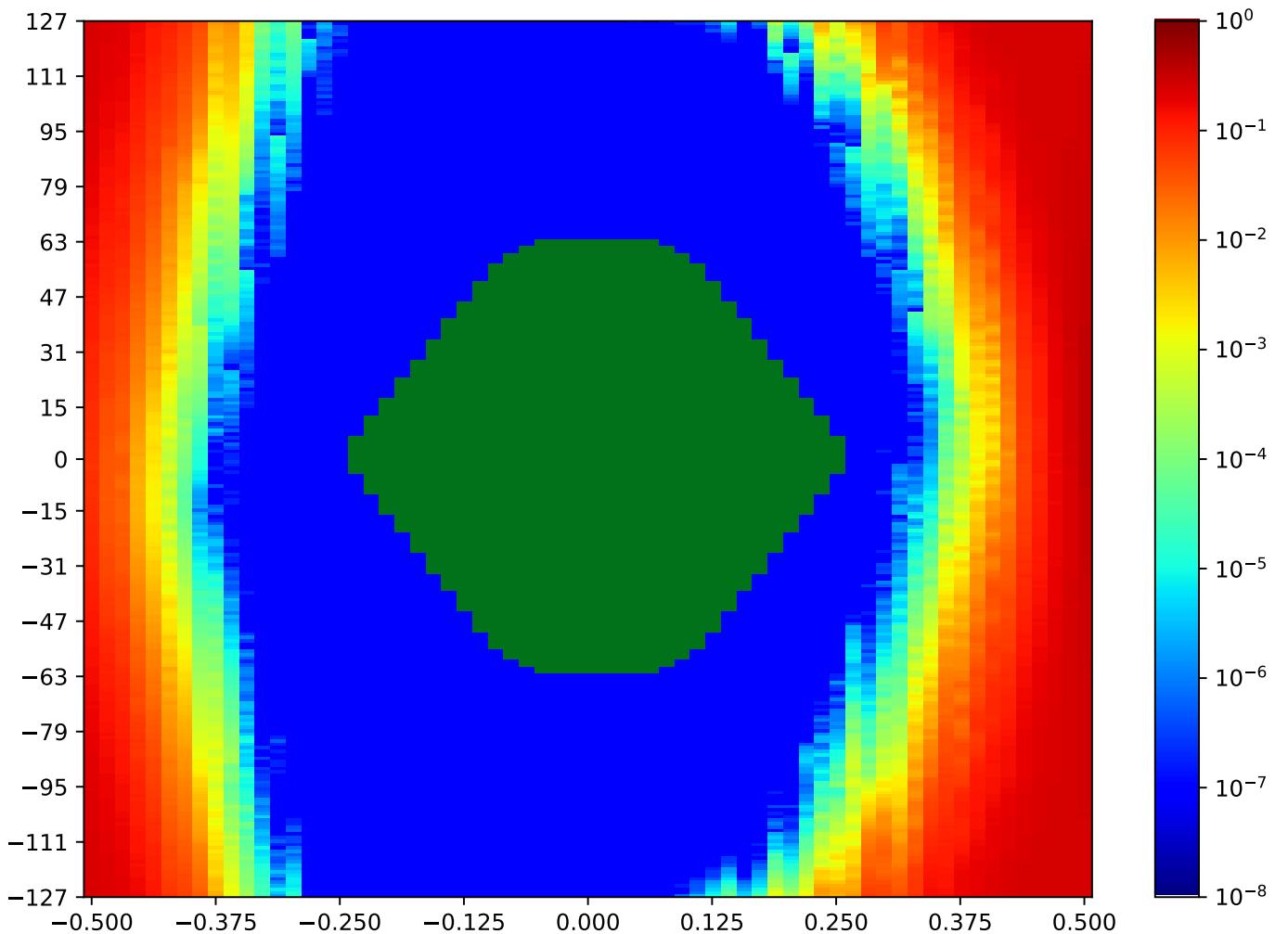


Figure 5.243: MSP_A_FPGA-TX1-02-RX12-02-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.4 MSP_A_FPGA-TX1-03-RX12-03-MSP_C_FPGA

Table 5.225: MSP_A_FPGA-TX1-03-RX12-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:22:48		2018-Sep-27 15:23:09	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9079	44		67.69%	246 95.69%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

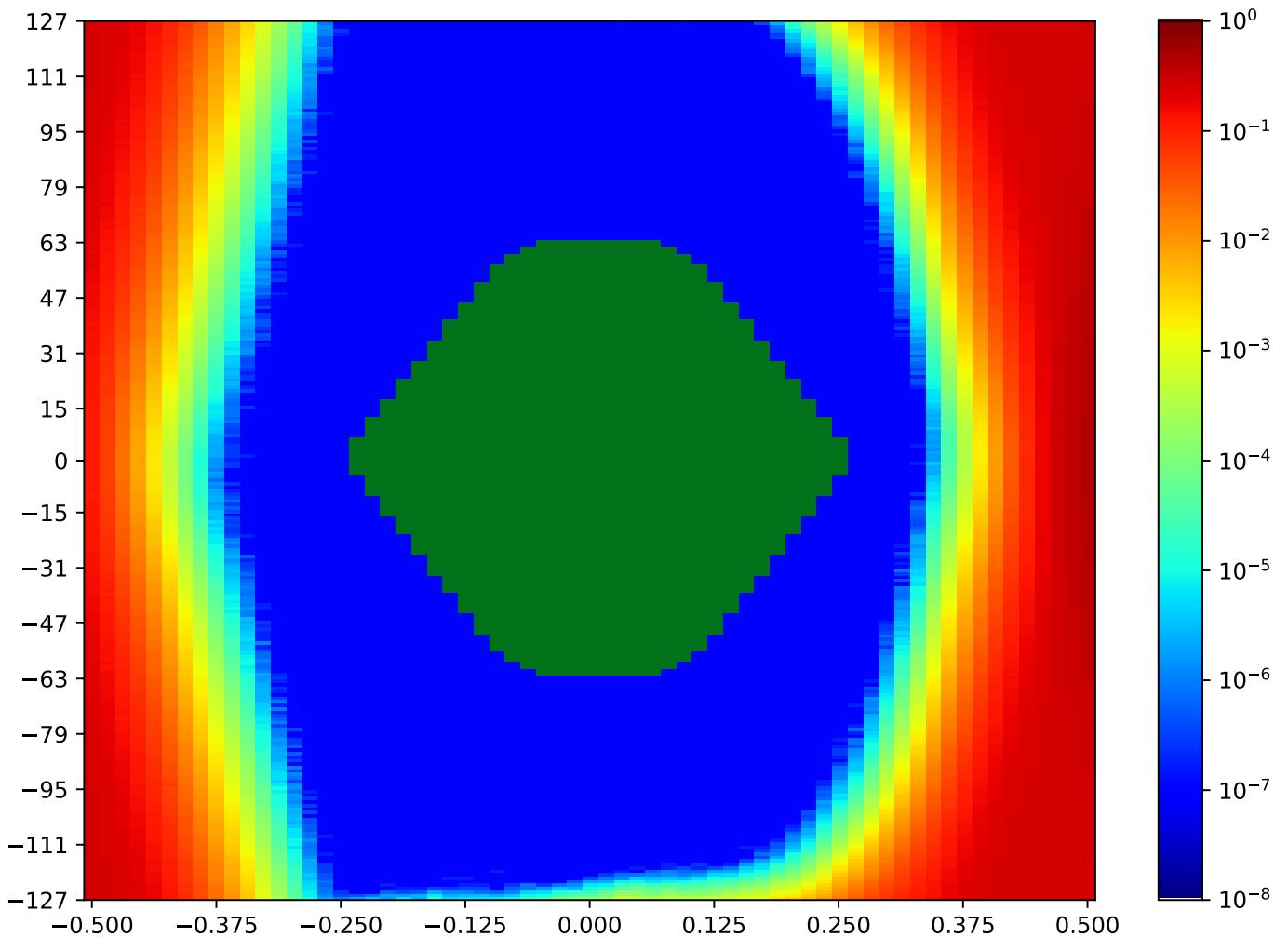


Figure 5.244: MSP_A_FPGA-TX1-03-RX12-03-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.5 MSP_A_FPGA-TX1-04-RX12-04-MSP_C_FPGA

Table 5.226: MSP_A_FPGA-TX1-04-RX12-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:25:31		2018-Sep-27 15:25:52	
Reset RX	OA	HO		VO	VO (%)
true	8343	41		63.08%	237 92.94%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

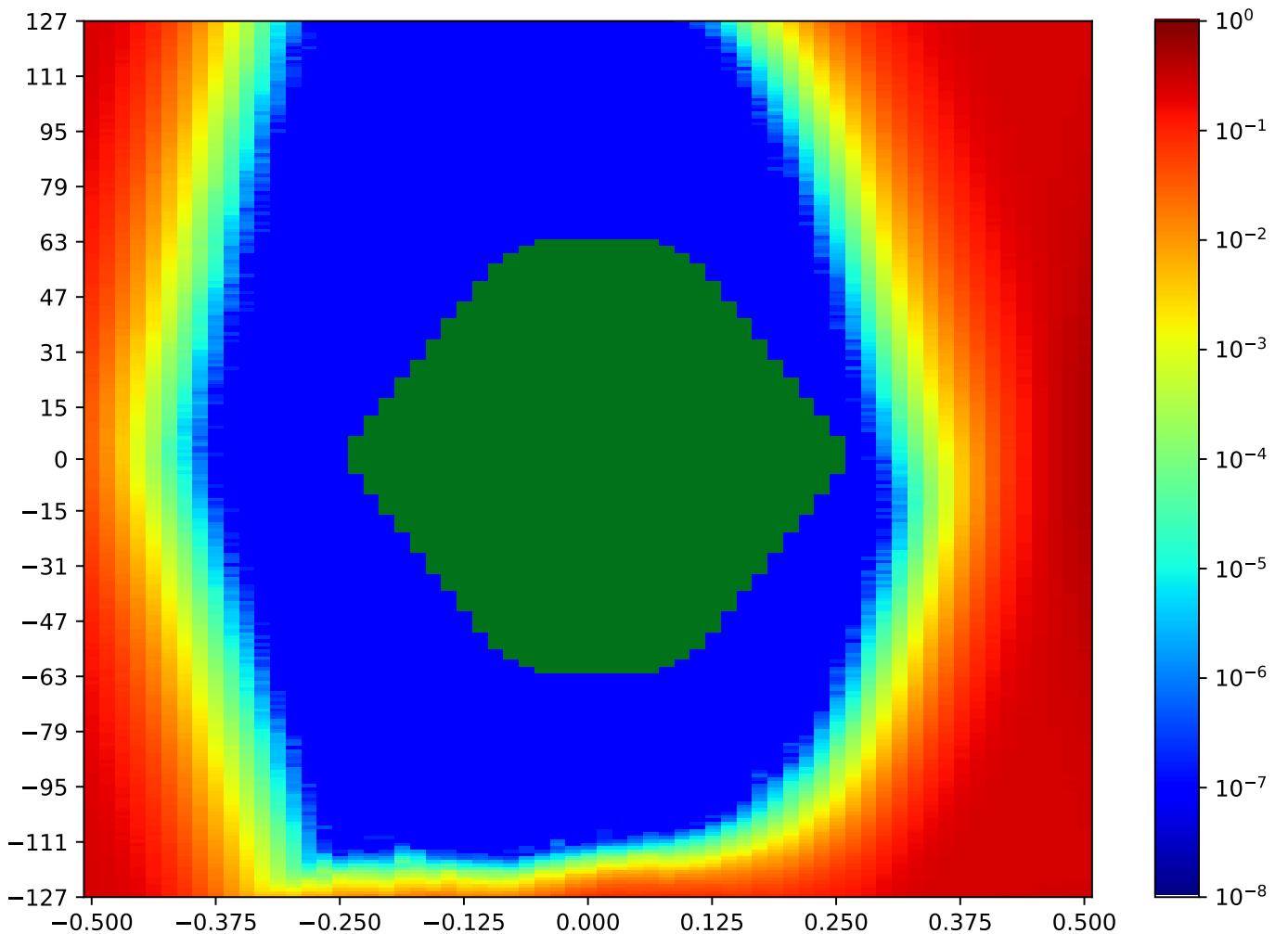


Figure 5.245: MSP_A_FPGA-TX1-04-RX12-04-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.6 MSP_A_FPGA-TX1-05-RX12-05-MSP_C_FPGA

Table 5.227: MSP_A_FPGA-TX1-05-RX12-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:22:28		2018-Sep-27 15:22:48	
Reset RX	OA	HO		VO	VO (%)
true	8608	41		252	98.04%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

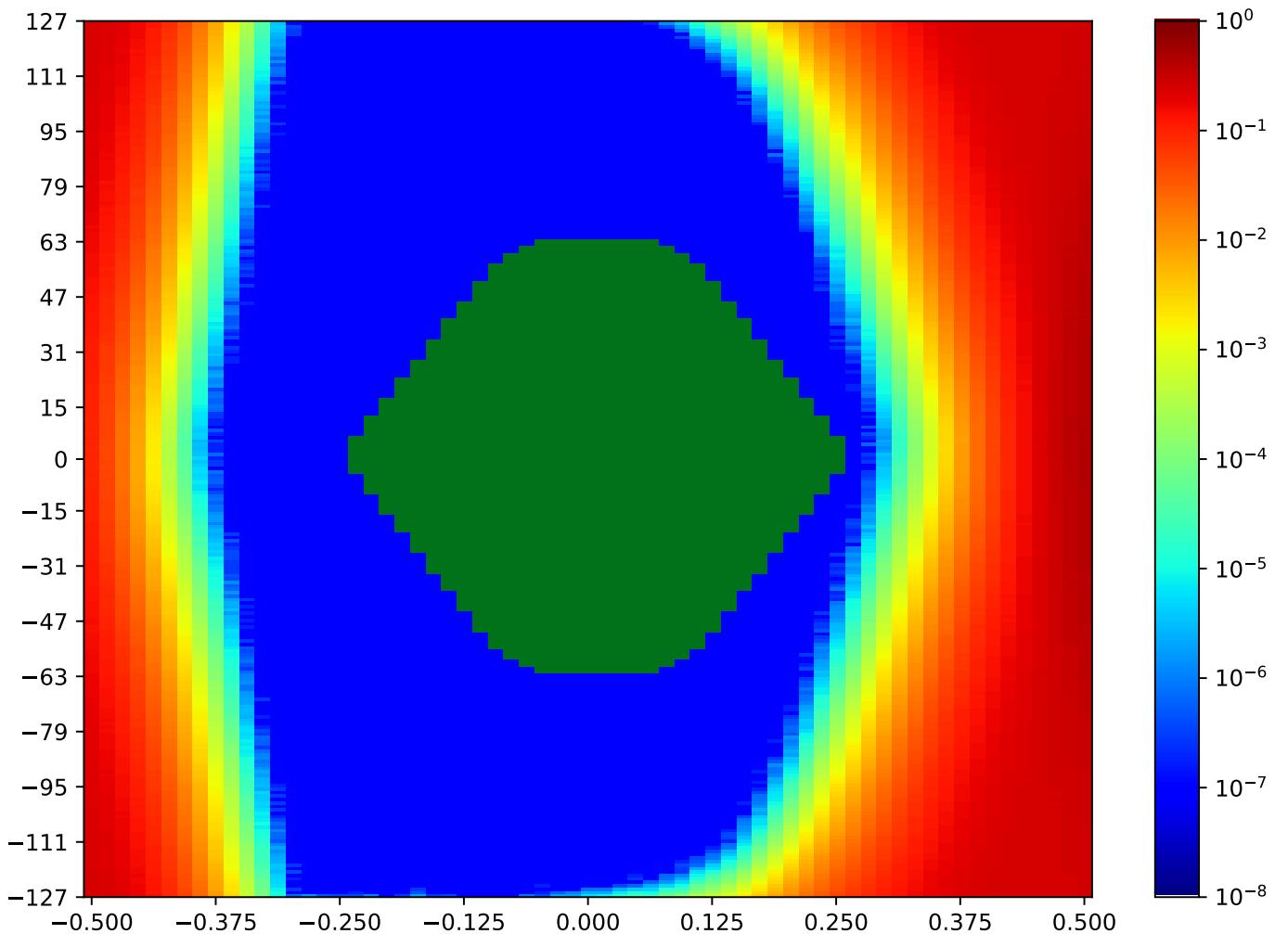


Figure 5.246: MSP_A_FPGA-TX1-05-RX12-05-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.7 MSP_A_FPGA-TX1-06-RX12-06-MSP_C_FPGA

Table 5.228: MSP_A_FPGA-TX1-06-RX12-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:26:12		2018-Sep-27 15:26:32	
Reset RX	OA	HO		VO	VO (%)
true	8452	41		63.08%	255 99.22%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

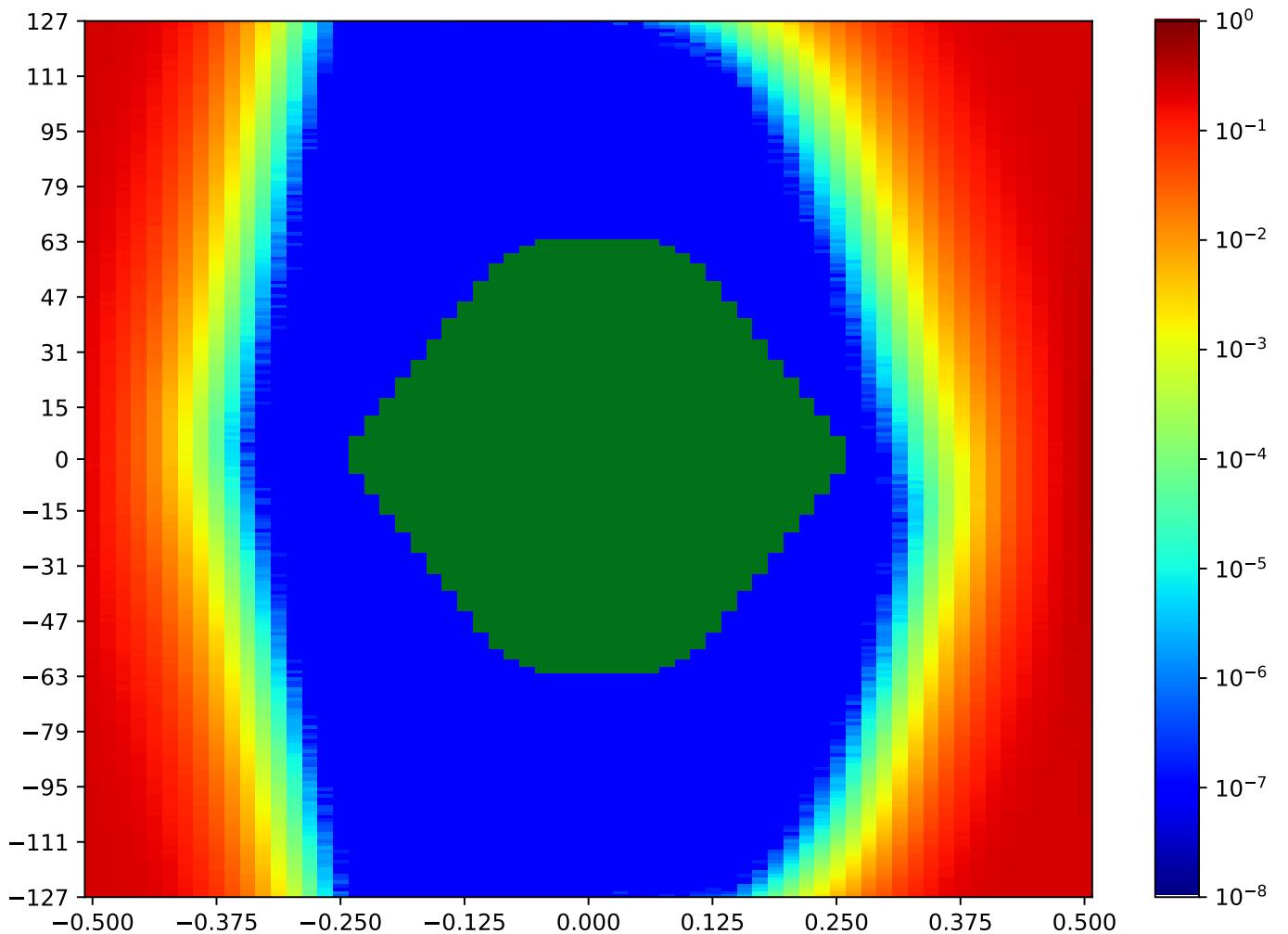


Figure 5.247: MSP_A_FPGA-TX1-06-RX12-06-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.8 MSP_A_FPGA-TX1-07-RX12-07-MSP_C_FPGA

Table 5.229: MSP_A_FPGA-TX1-07-RX12-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:23:09		2018-Sep-27 15:23:29	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9216	44	67.69%	252	98.43%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

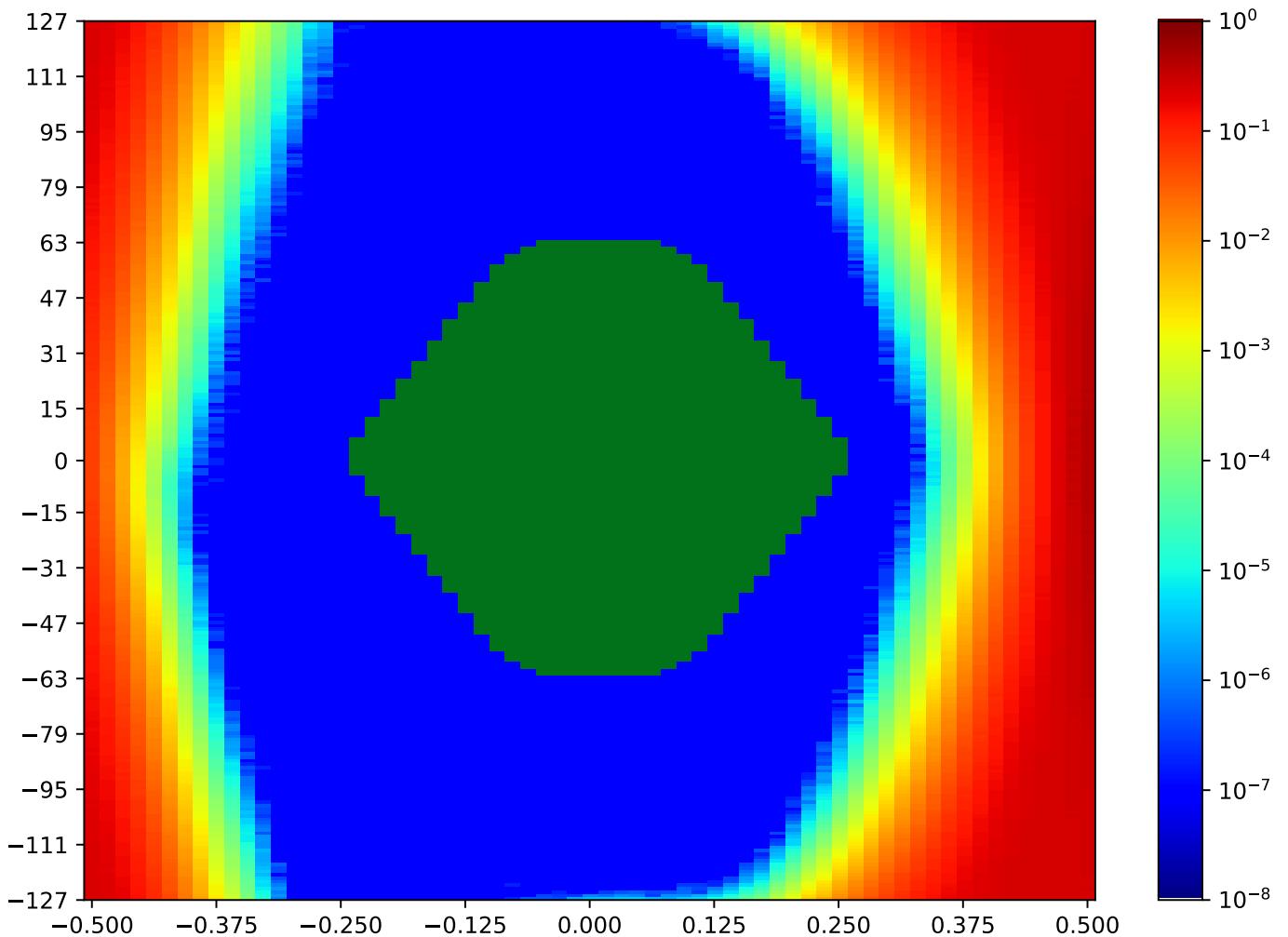


Figure 5.248: MSP_A_FPGA-TX1-07-RX12-07-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.9 MSP_A_FPGA-TX1-08-RX12-08-MSP_C_FPGA

Table 5.230: MSP_A_FPGA-TX1-08-RX12-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:25:52		2018-Sep-27 15:26:12	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8483	43	66.15%	239	93.33%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

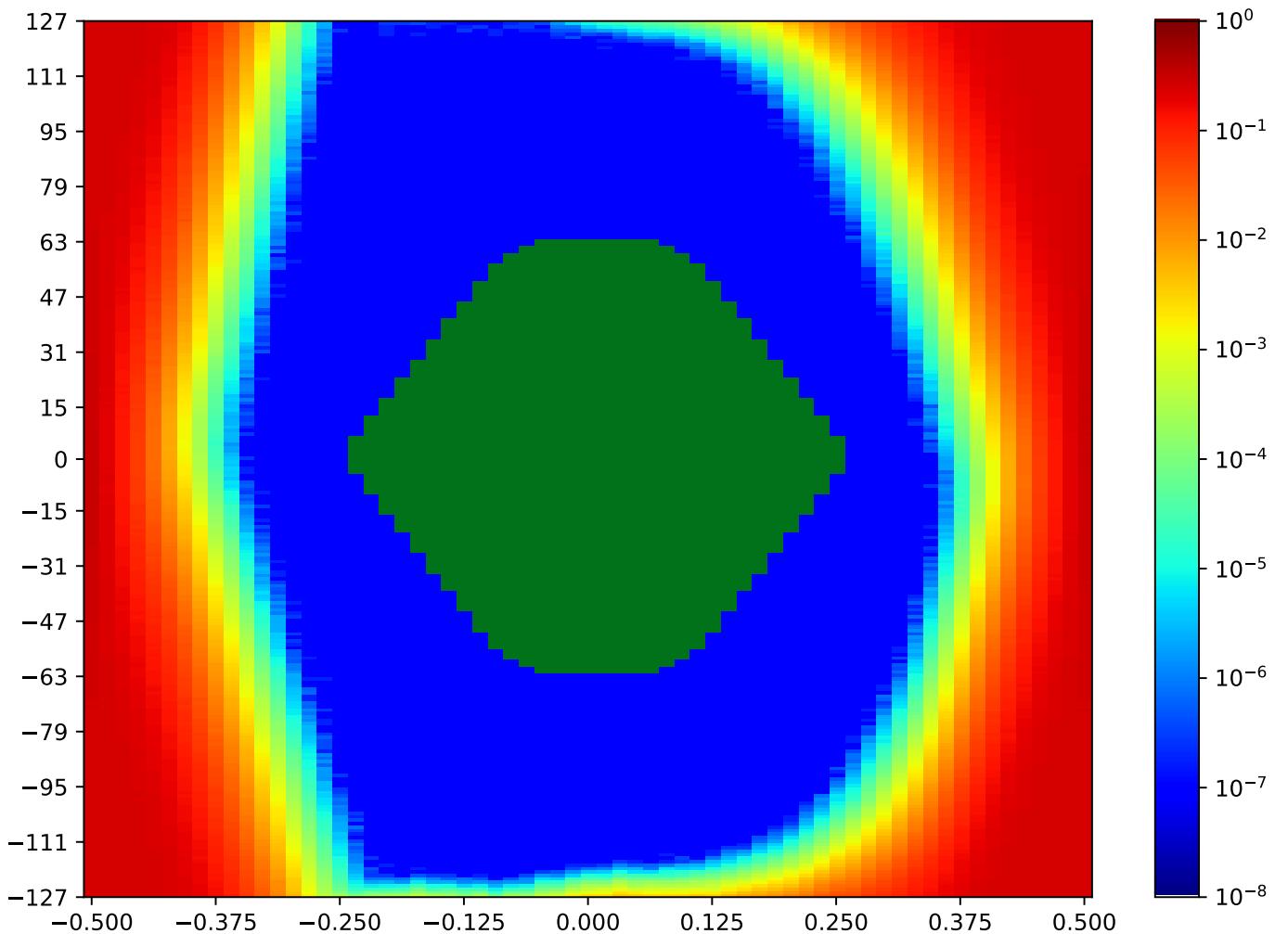


Figure 5.249: MSP_A_FPGA-TX1-08-RX12-08-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.10 MSP_A_FPGA-TX1-09-RX12-09-MSP_C_FPGA

Table 5.231: MSP_A_FPGA-TX1-09-RX12-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:23:50		2018-Sep-27 15:24:10	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9024	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

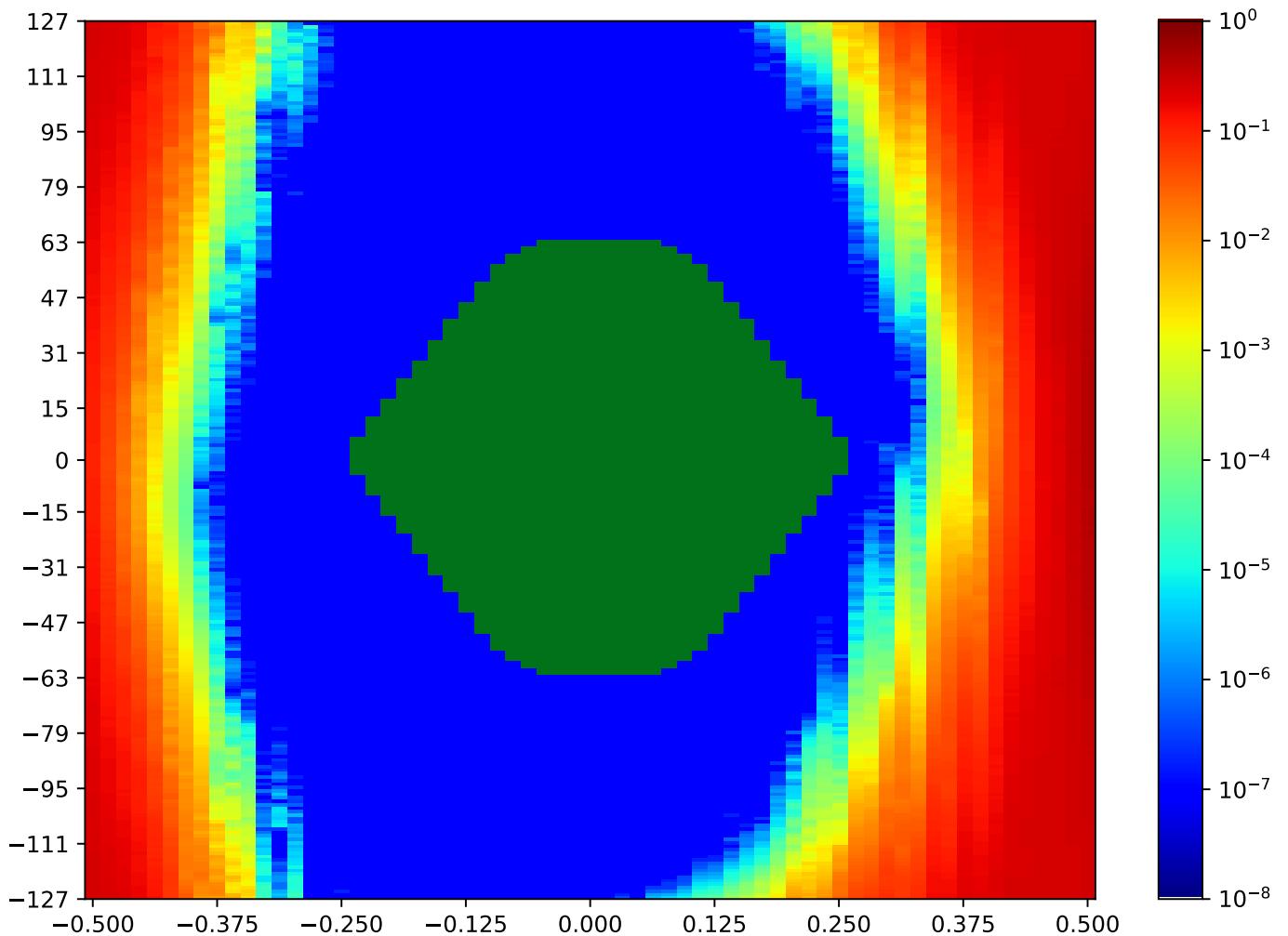


Figure 5.250: MSP_A_FPGA-TX1-09-RX12-09-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.11 MSP_A_FPGA-TX1-10-RX12-10-MSP_C_FPGA

Table 5.232: MSP_A_FPGA-TX1-10-RX12-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:25:11		2018-Sep-27 15:25:31	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8855	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

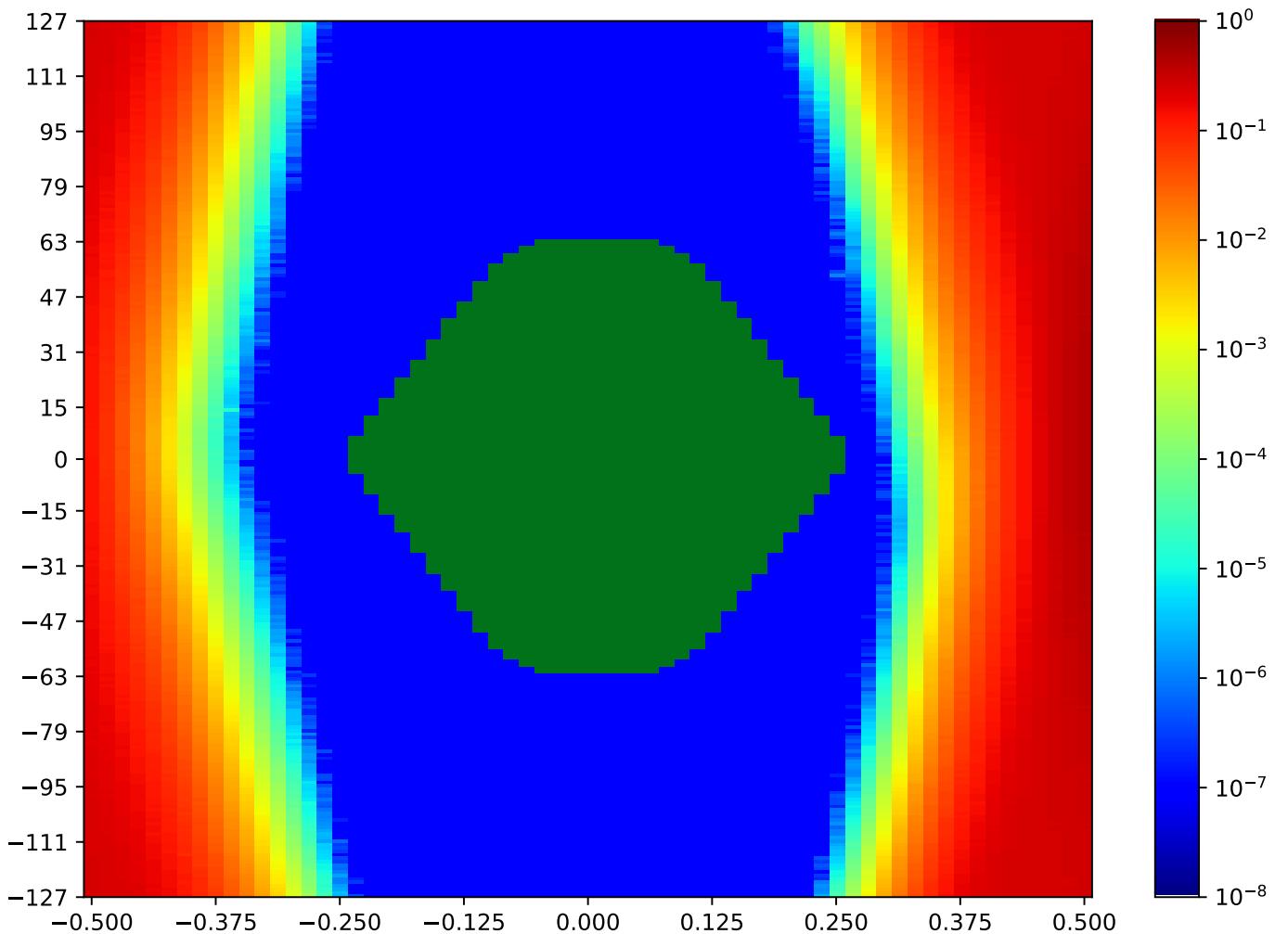


Figure 5.251: MSP_A_FPGA-TX1-10-RX12-10-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.19.12 MSP_A_FPGA-TX1-11-RX12-11-MSP_C_FPGA

Table 5.233: MSP_A_FPGA-TX1-11-RX12-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:24:51		2018-Sep-27 15:25:11	
Reset RX	OA	HO		VO	VO (%)
true	9552	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

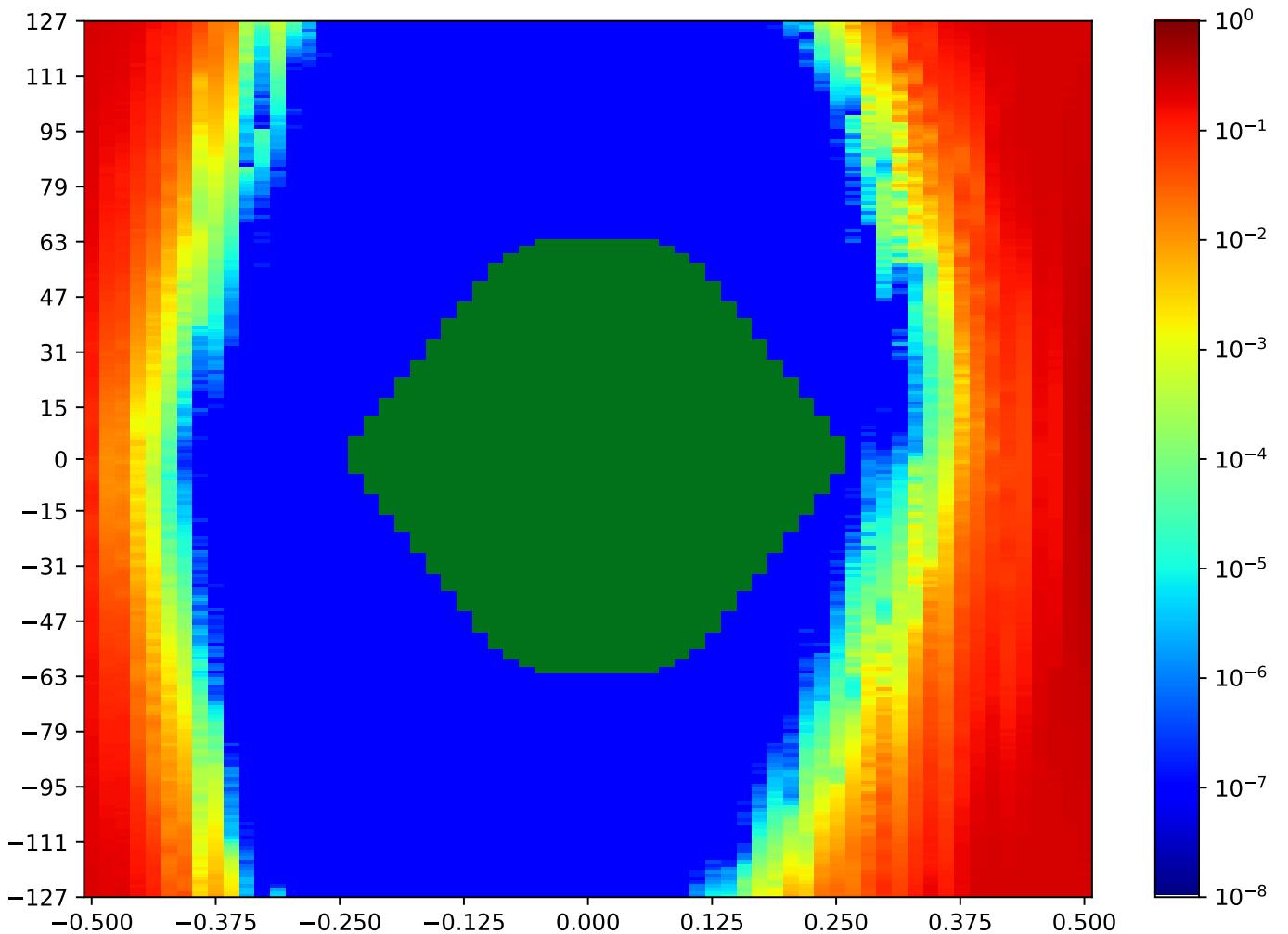


Figure 5.252: MSP_A_FPGA-TX1-11-RX12-11-MSP_C_FPGA

Call back to summary Figure 5.240. Sibling eye diagrams: V2-6.4.

5.20 MSP_A TX2 MSP_C RX13 Minipod Loopback

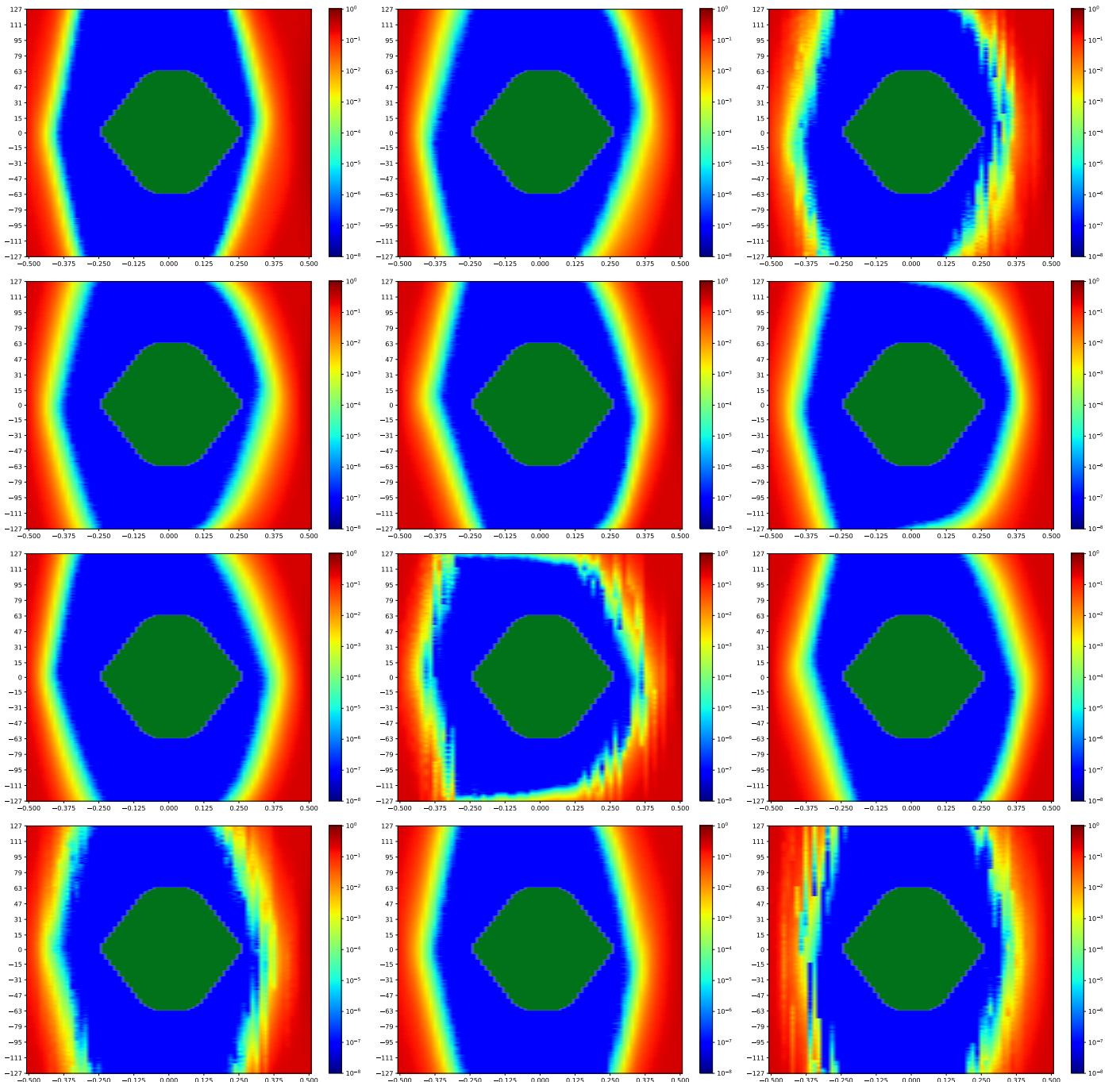


Figure 5.253: MSP_A TX2 MSP_C RX13 Minipod Loopback

A cross-reference to Figure 5.253. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.266.

5.20.1 MSP_A_FPGA-TX2-00-RX13-00-MSP_C_FPGA

Table 5.234: MSP_A_FPGA-TX2-00-RX13-00-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:27:33		2018-Sep-27 15:27:57	
Reset RX	OA	HO		VO	VO (%)
true	9351	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

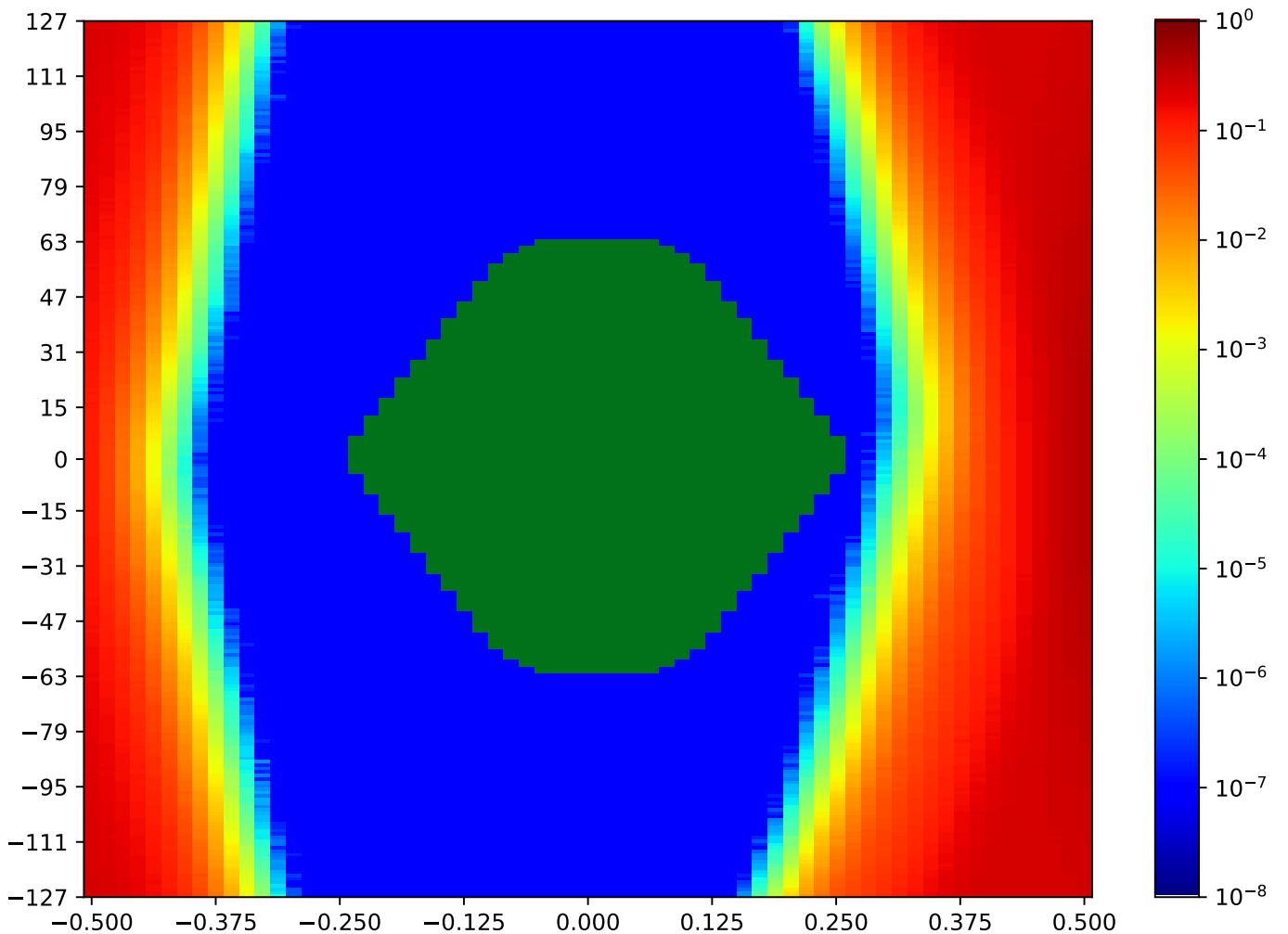


Figure 5.254: MSP_A_FPGA-TX2-00-RX13-00-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.2 MSP_A_FPGA-TX2-01-RX13-01-MSP_C_FPGA

Table 5.235: MSP_A_FPGA-TX2-01-RX13-01-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:26:52		2018-Sep-27 15:27:12	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9206	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

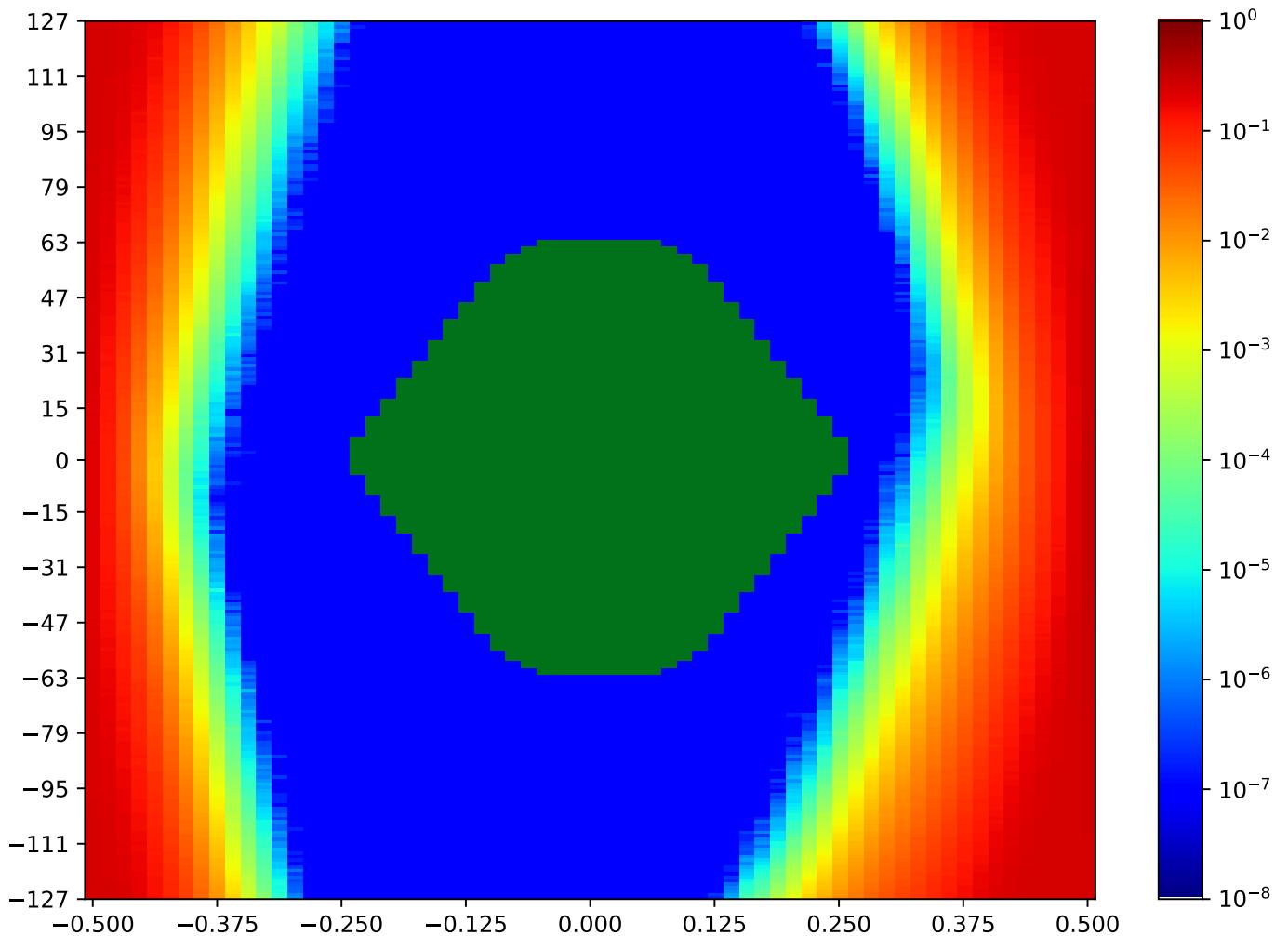


Figure 5.255: MSP_A_FPGA-TX2-01-RX13-01-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.3 MSP_A_FPGA-TX2-02-RX13-02-MSP_C_FPGA

Table 5.236: MSP_A_FPGA-TX2-02-RX13-02-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:28:38		2018-Sep-27 15:28:58	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8846	42	64.62%	254	99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

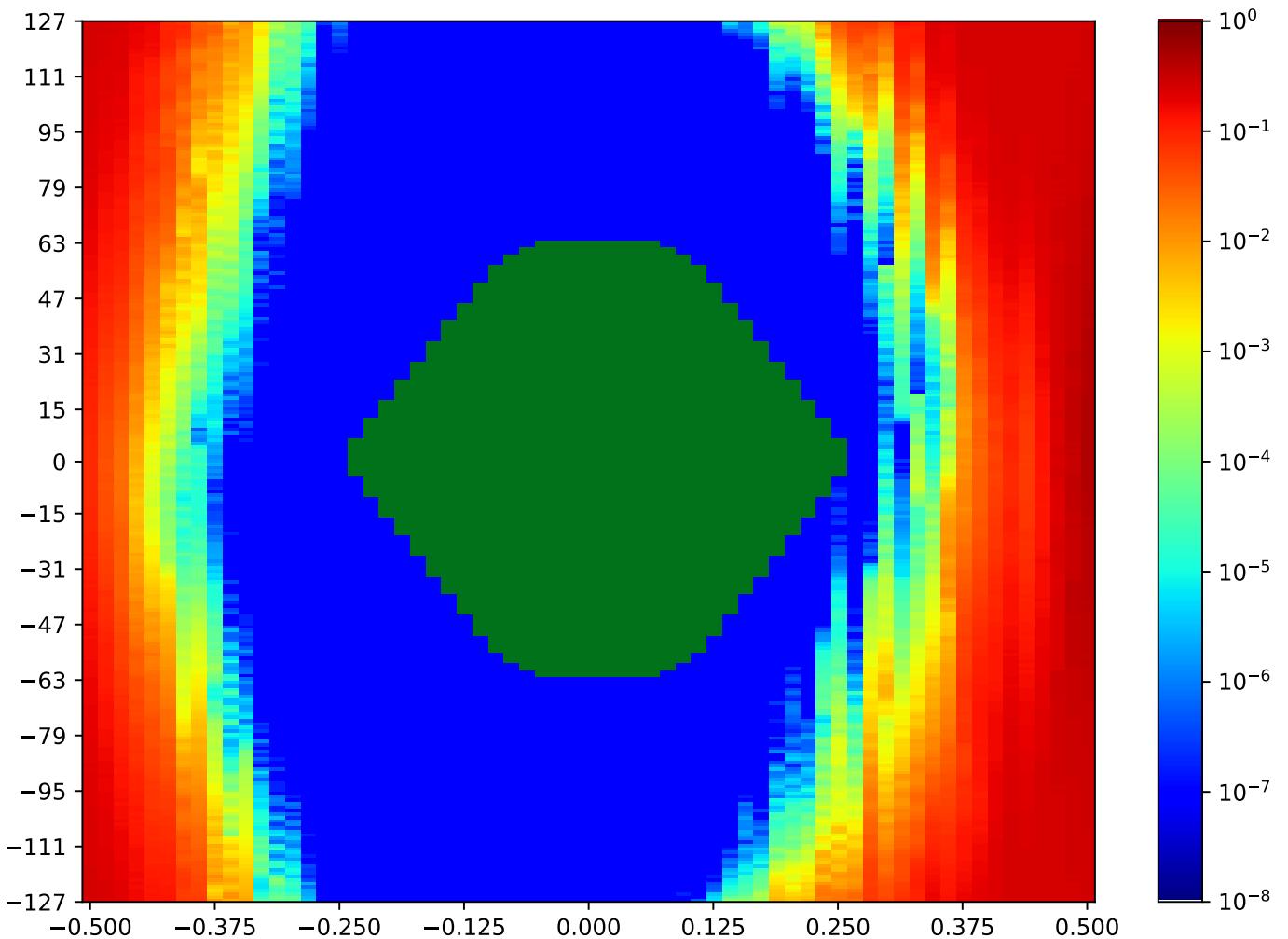


Figure 5.256: MSP_A_FPGA-TX2-02-RX13-02-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.4 MSP_A_FPGA-TX2-03-RX13-03-MSP_C_FPGA

Table 5.237: MSP_A_FPGA-TX2-03-RX13-03-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:26:32		2018-Sep-27 15:26:52	
Reset RX	OA	HO		VO	VO (%)
true	8676	40		61.54%	255 99.61%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

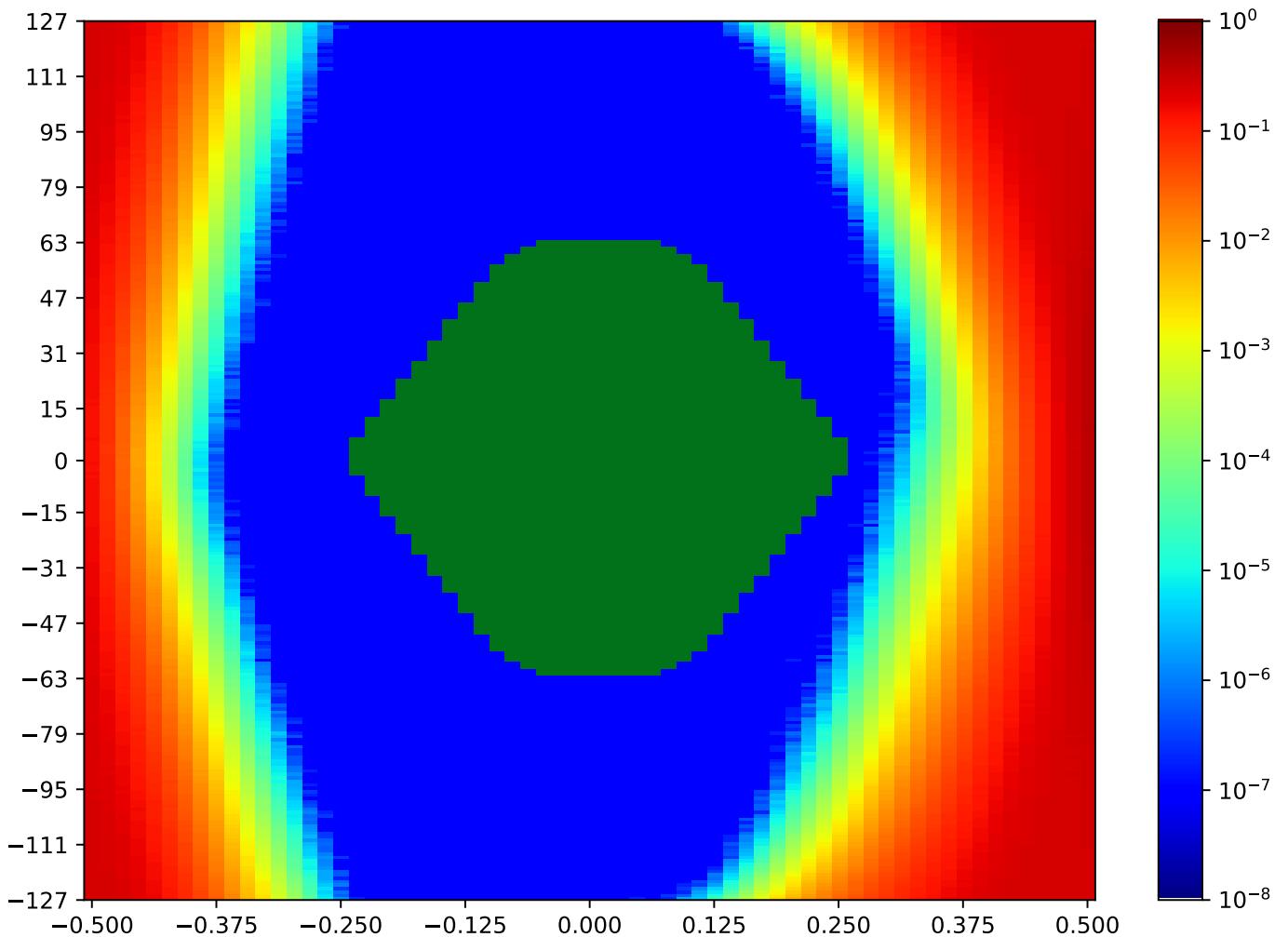


Figure 5.257: MSP_A_FPGA-TX2-03-RX13-03-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.5 MSP_A_FPGA-TX2-04-RX13-04-MSP_C_FPGA

Table 5.238: MSP_A_FPGA-TX2-04-RX13-04-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:29:39		2018-Sep-27 15:30:00	
Reset RX	OA	HO		VO	VO (%)
true	8660	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

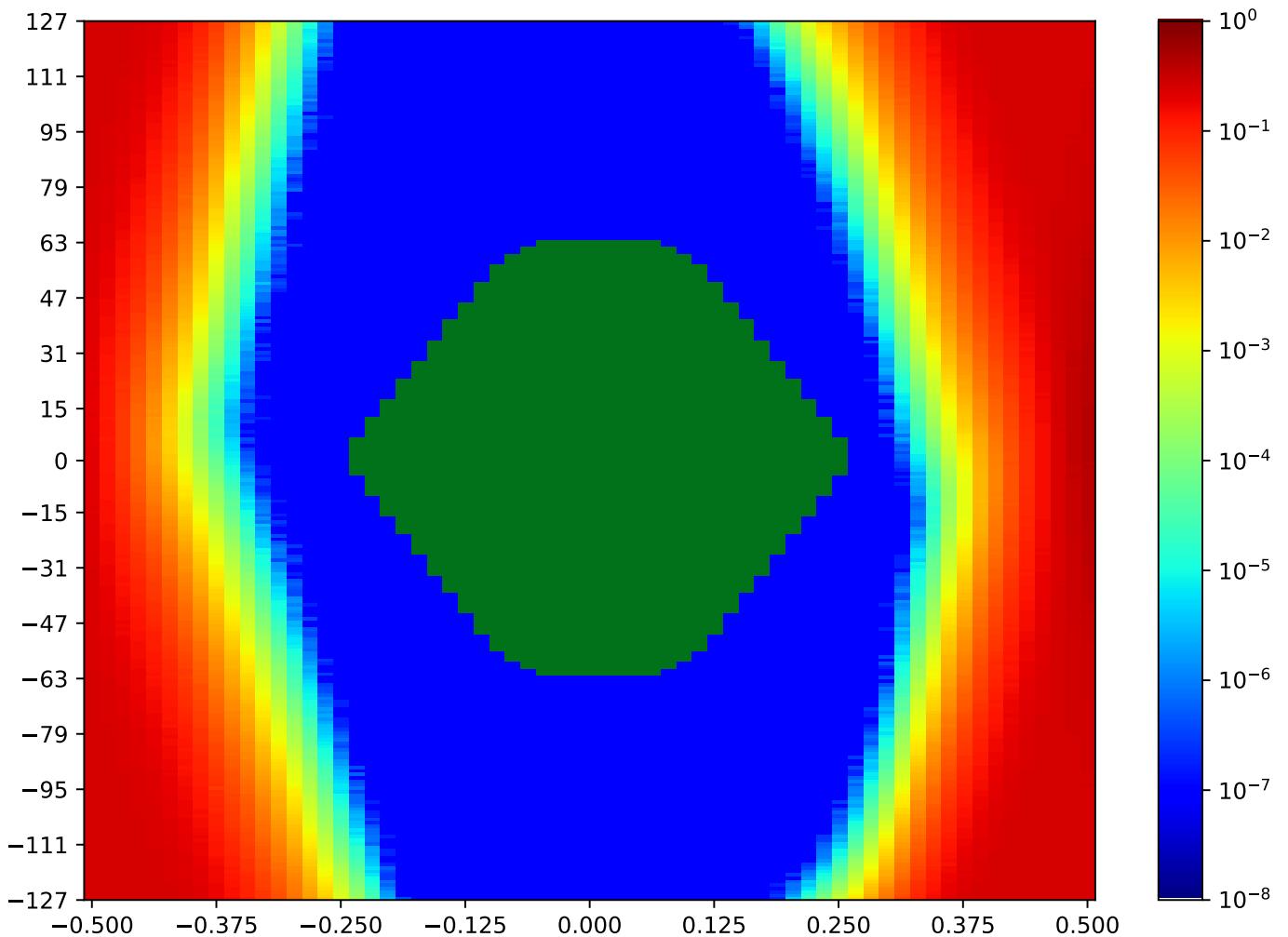


Figure 5.258: MSP_A_FPGA-TX2-04-RX13-04-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.6 MSP_A_FPGA-TX2-05-RX13-05-MSP_C_FPGA

Table 5.239: MSP_A_FPGA-TX2-05-RX13-05-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:27:12		2018-Sep-27 15:27:33	
Reset RX	OA	HO		VO	VO (%)
true	8866	43		66.15%	243 94.90%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

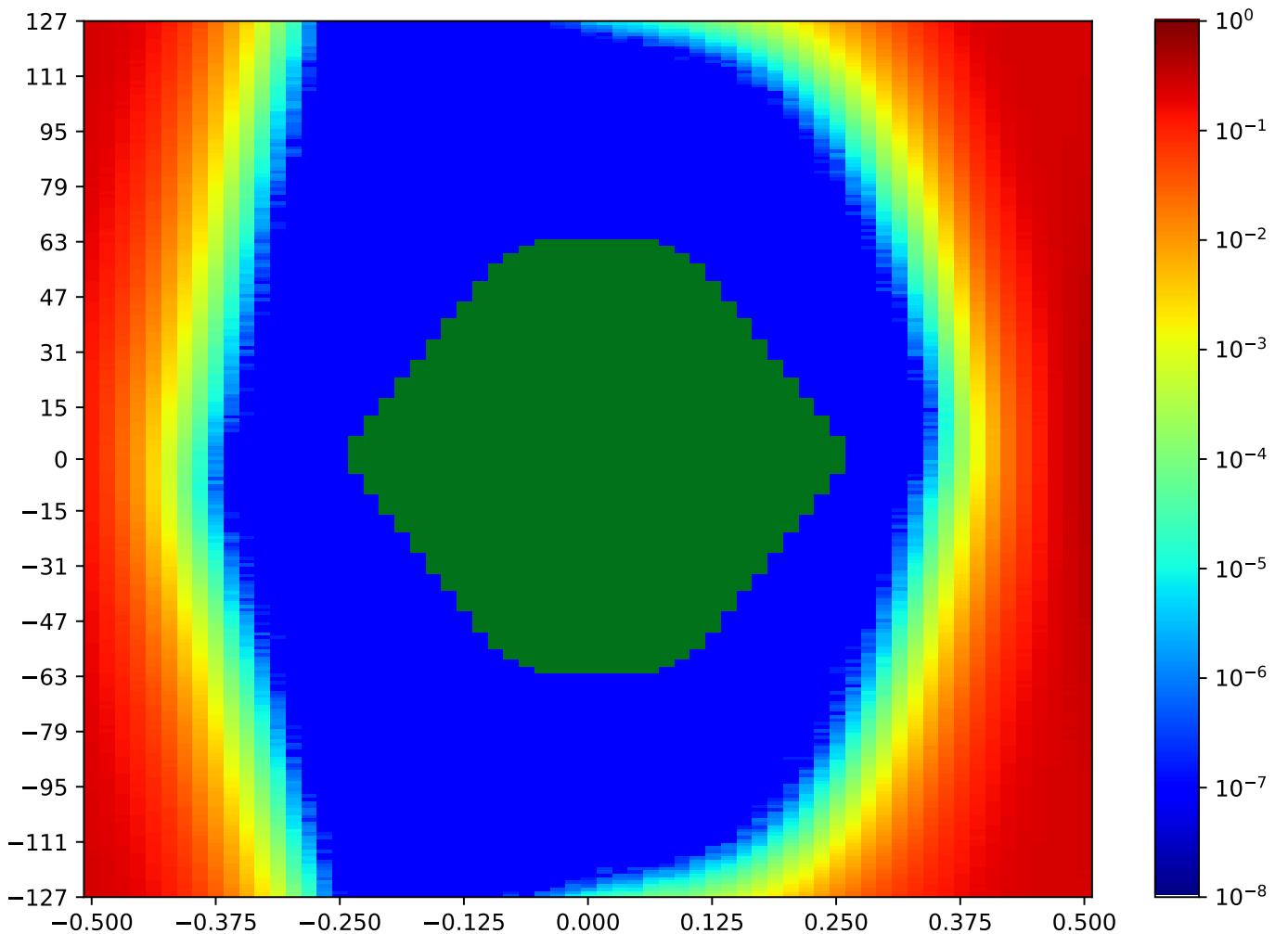


Figure 5.259: MSP_A_FPGA-TX2-05-RX13-05-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.7 MSP_A_FPGA-TX2-06-RX13-06-MSP_C_FPGA

Table 5.240: MSP_A_FPGA-TX2-06-RX13-06-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:30:20		2018-Sep-27 15:30:41	
Reset RX	OA	HO		VO	VO (%)
true	9455	45		69.23%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

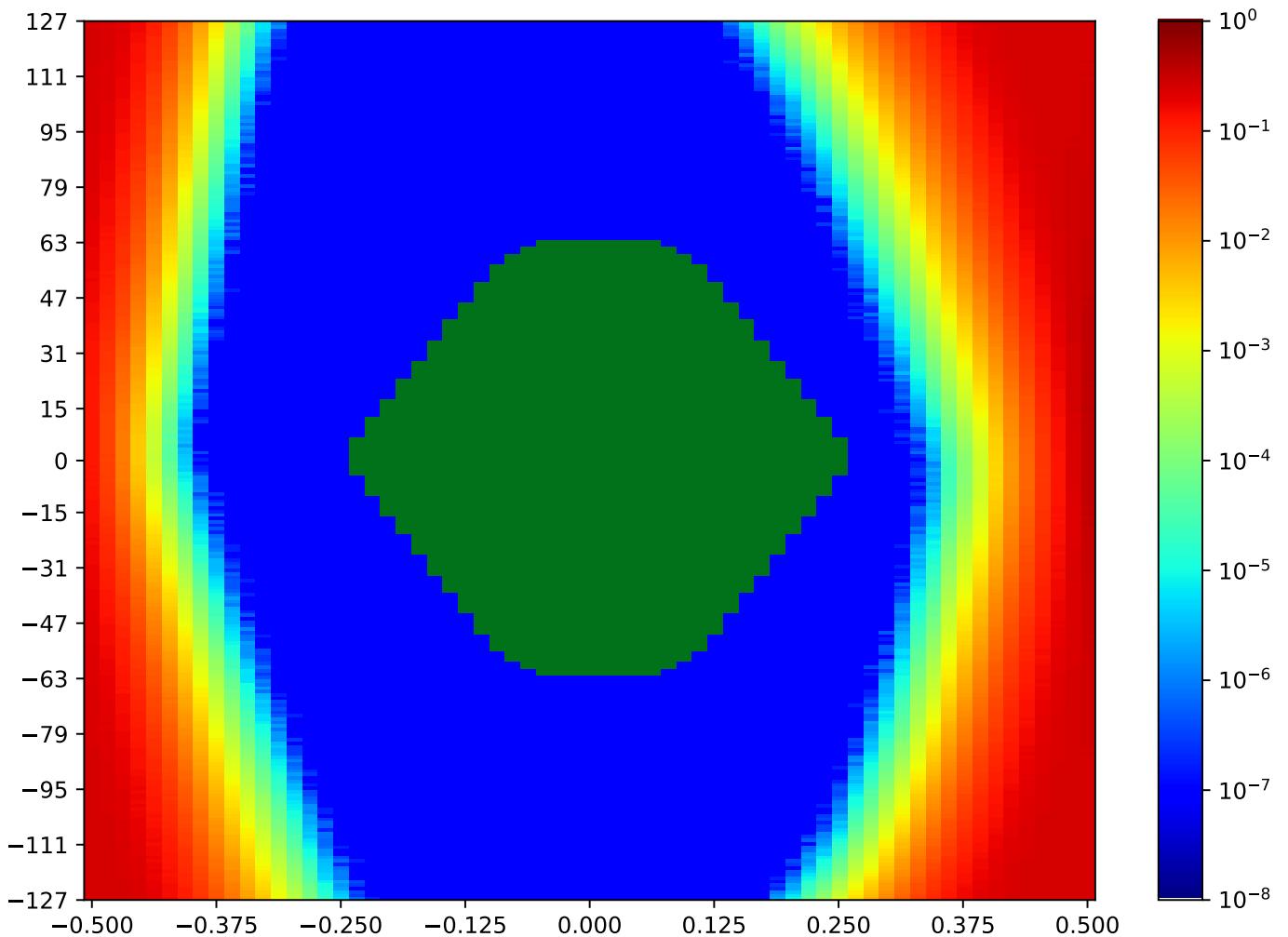


Figure 5.260: MSP_A_FPGA-TX2-06-RX13-06-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.8 MSP_A_FPGA-TX2-07-RX13-07-MSP_C_FPGA

Table 5.241: MSP_A_FPGA-TX2-07-RX13-07-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:27:57		2018-Sep-27 15:28:17	
Reset RX	OA	HO		VO	VO (%)
true	8364	42		230	90.20%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

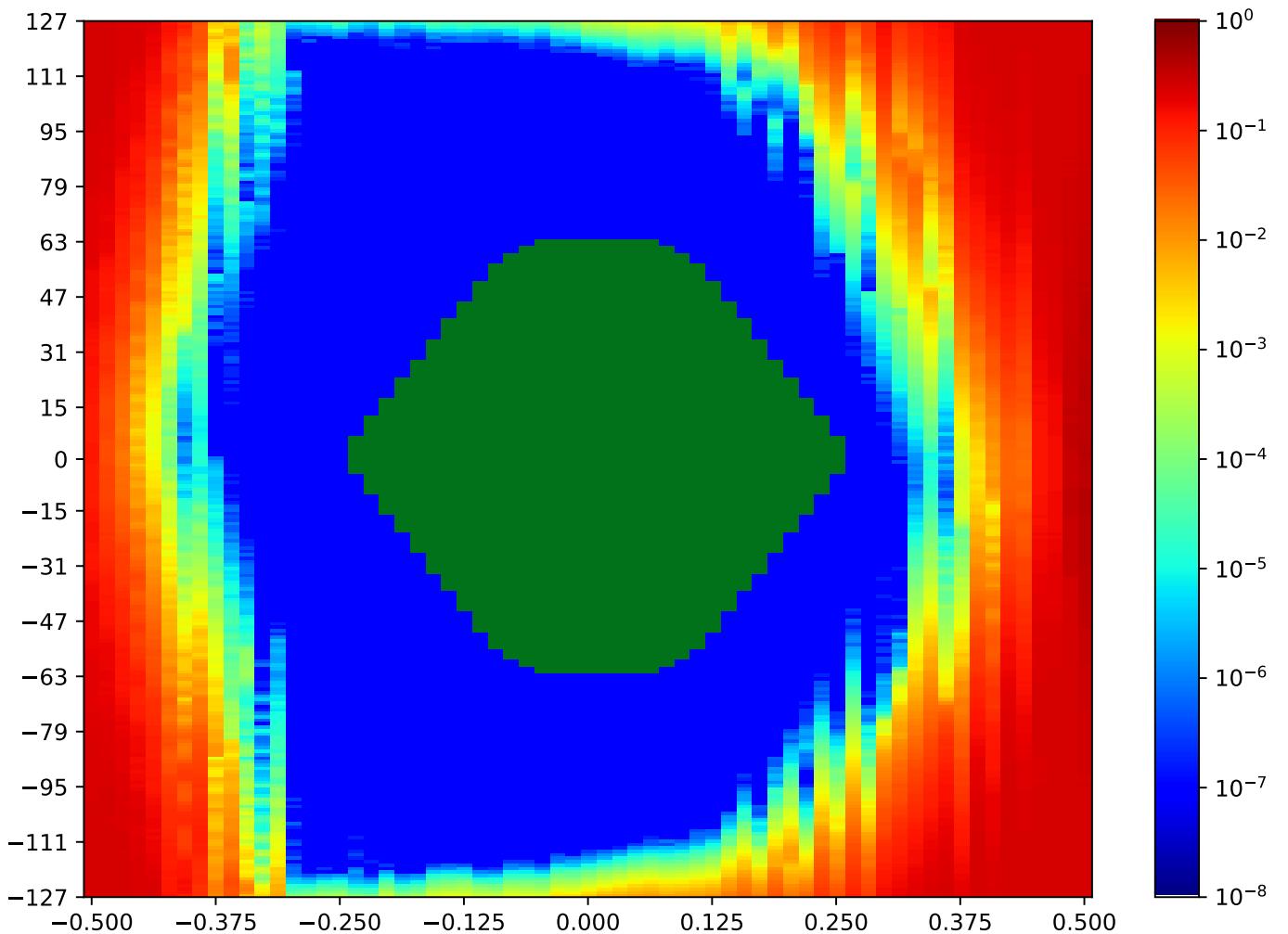


Figure 5.261: MSP_A_FPGA-TX2-07-RX13-07-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.9 MSP_A_FPGA-TX2-08-RX13-08-MSP_C_FPGA

Table 5.242: MSP_A_FPGA-TX2-08-RX13-08-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:30:00		2018-Sep-27 15:30:20	
Reset RX	OA	HO		VO	VO (%)
true	9051	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

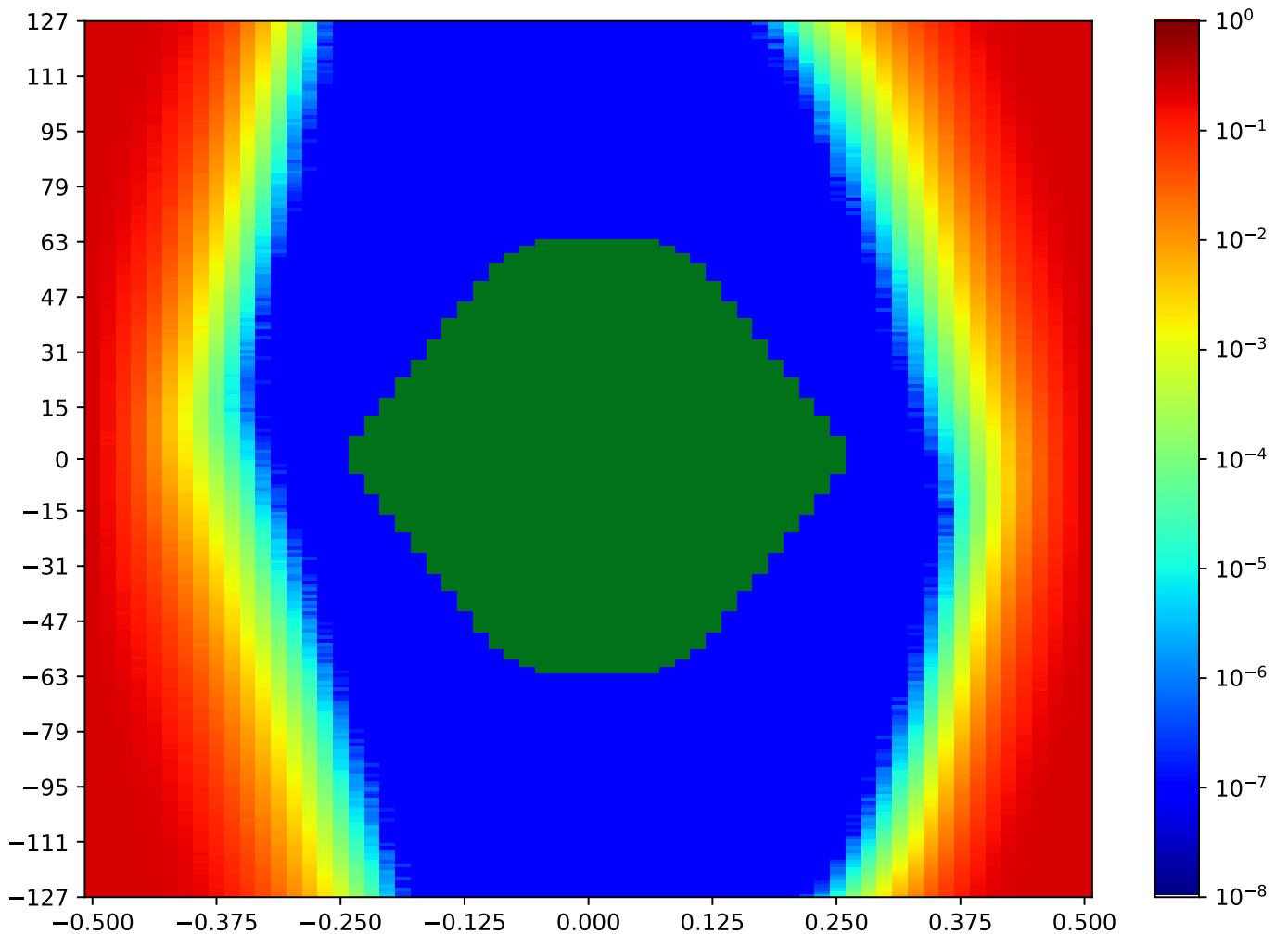


Figure 5.262: MSP_A_FPGA-TX2-08-RX13-08-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.10 MSP_A_FPGA-TX2-09-RX13-09-MSP_C_FPGA

Table 5.243: MSP_A_FPGA-TX2-09-RX13-09-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:28:17		2018-Sep-27 15:28:38	
Reset RX	OA	HO		VO	VO (%)
true	8994	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

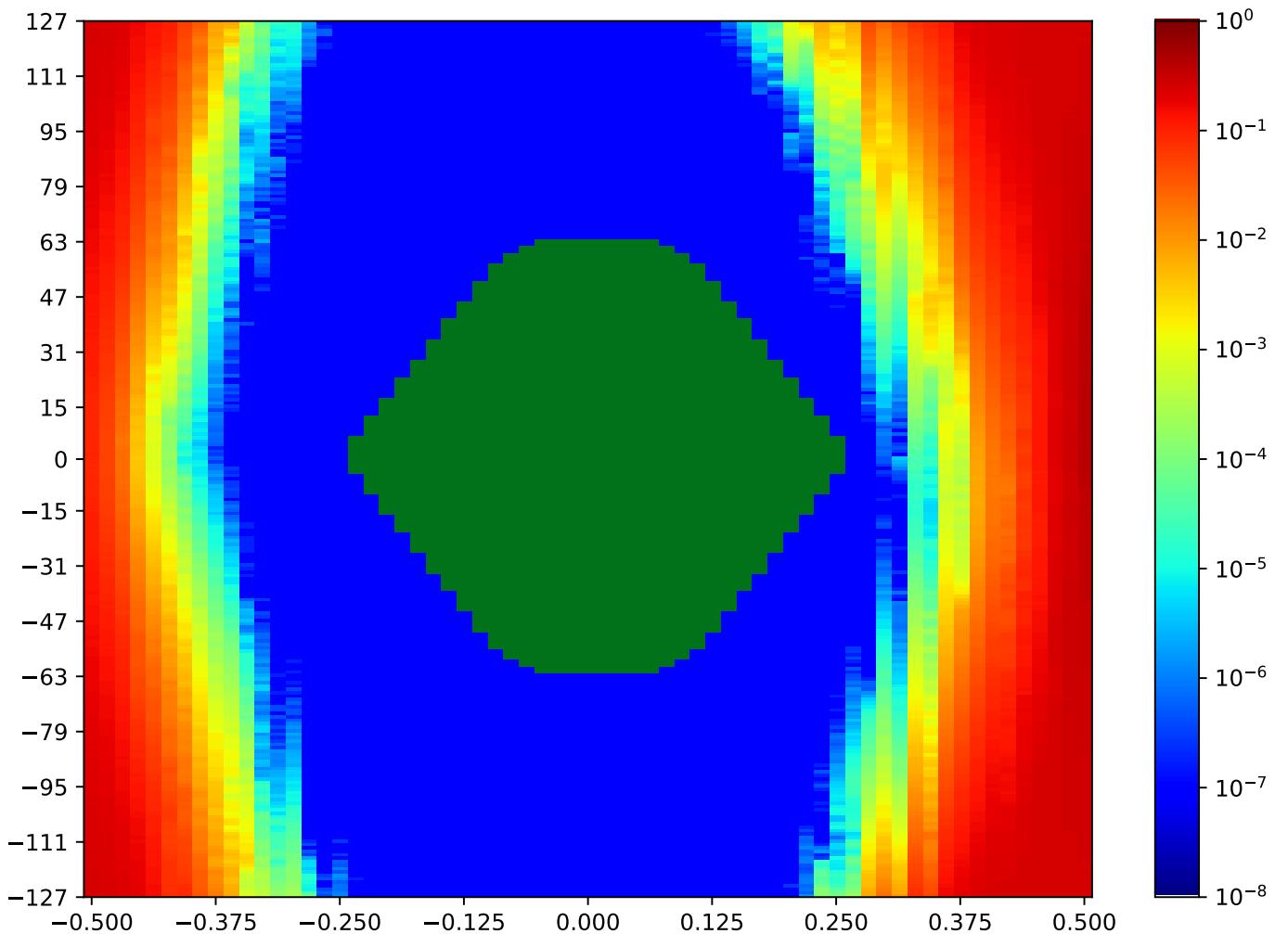


Figure 5.263: MSP_A_FPGA-TX2-09-RX13-09-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.11 MSP_A_FPGA-TX2-10-RX13-10-MSP_C_FPGA

Table 5.244: MSP_A_FPGA-TX2-10-RX13-10-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:29:19		2018-Sep-27 15:29:39	
Reset RX	OA	HO		VO	VO (%)
true	9244	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

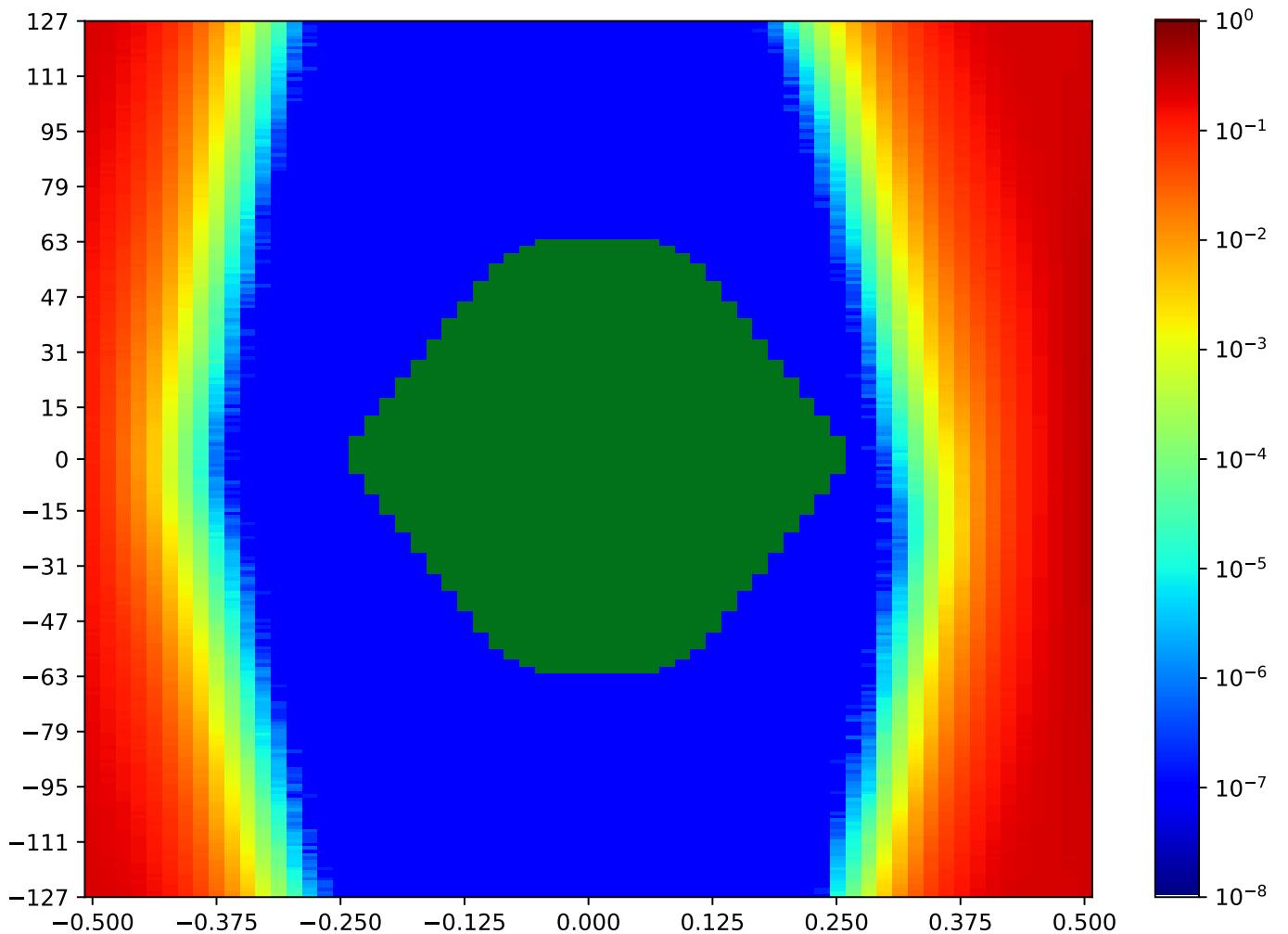


Figure 5.264: MSP_A_FPGA-TX2-10-RX13-10-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.20.12 MSP_A_FPGA-TX2-11-RX13-11-MSP_C_FPGA

Table 5.245: MSP_A_FPGA-TX2-11-RX13-11-MSP_C_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:28:58		2018-Sep-27 15:29:18	
Reset RX	OA	HO		VO	VO (%)
true	9173	41		61.54%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

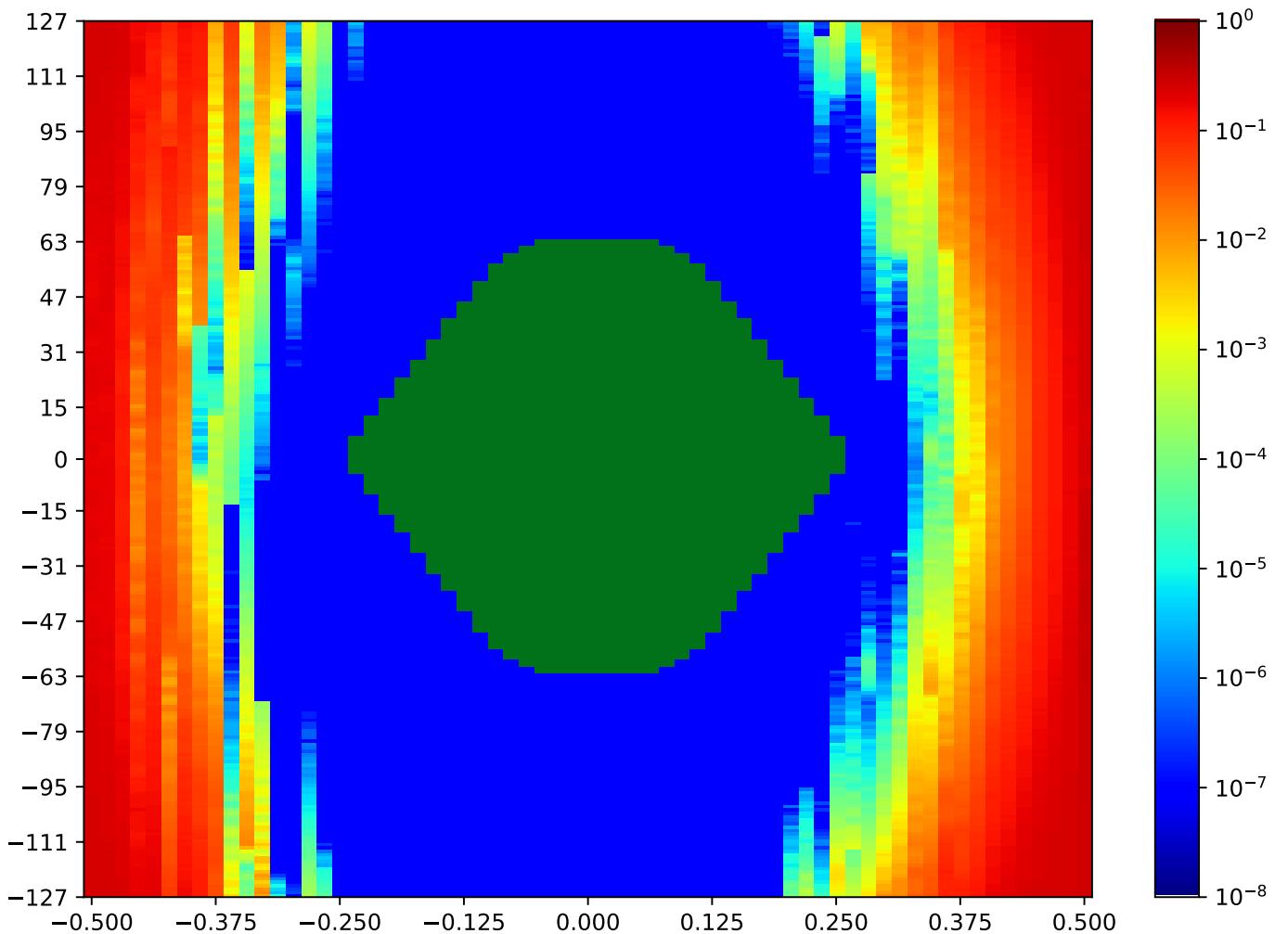


Figure 5.265: MSP_A_FPGA-TX2-11-RX13-11-MSP_C_FPGA

Call back to summary Figure 5.253. Sibling eye diagrams: V2-6.4.

5.21 MSP_C TX3 MSP_A RX3 Minipod Loopback

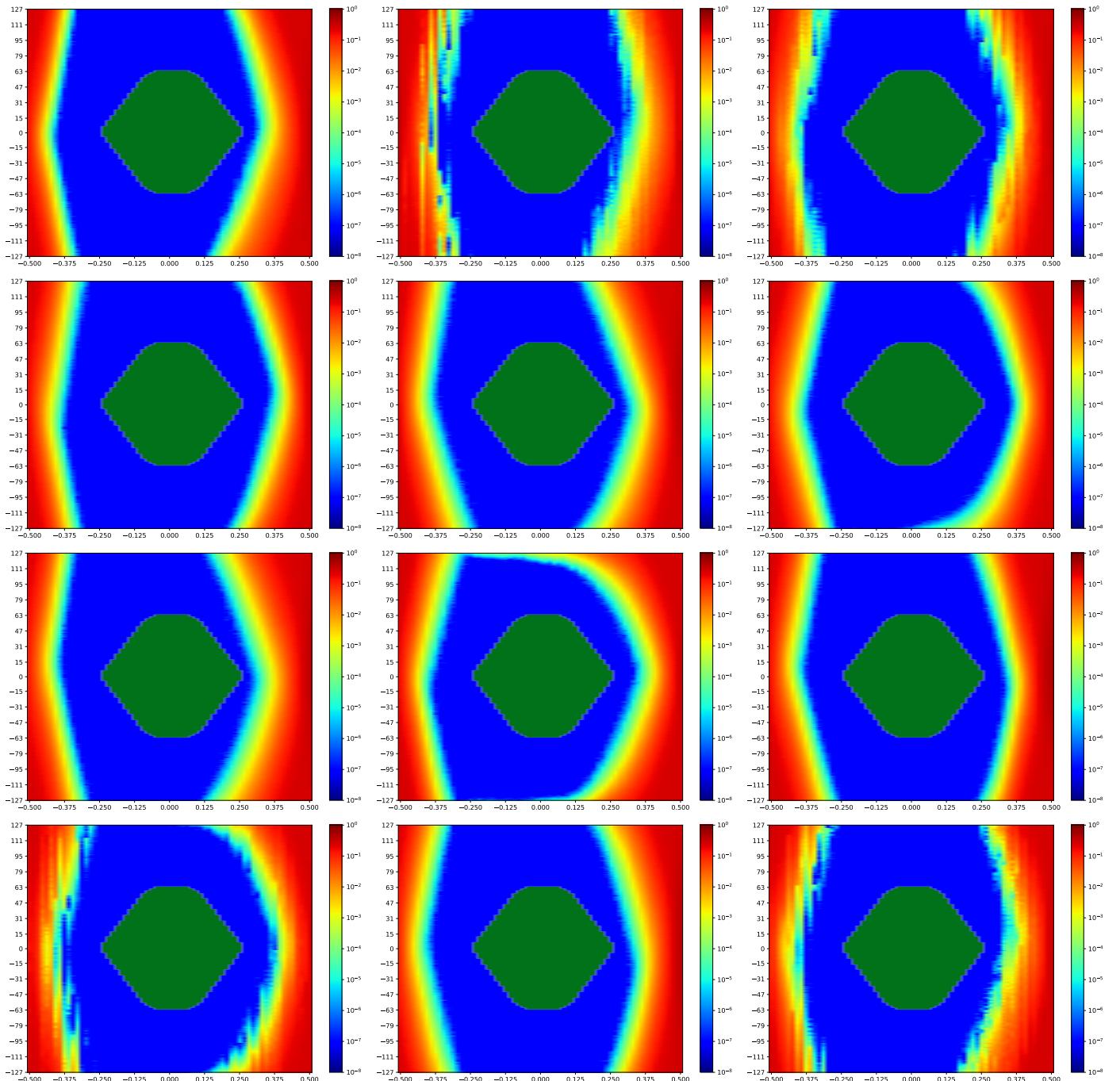


Figure 5.266: MSP_C TX3 MSP_A RX3 Minipod Loopback

A cross-reference to Figure 5.266. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.279.

5.21.1 MSP_C_FPGA-TX3-00-RX3-00-MSP_A_FPGA

Table 5.246: MSP_C_FPGA-TX3-00-RX3-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:31:41		2018-Sep-27 15:32:01	
Reset RX	OA	HO		VO	VO (%)
true	9610	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

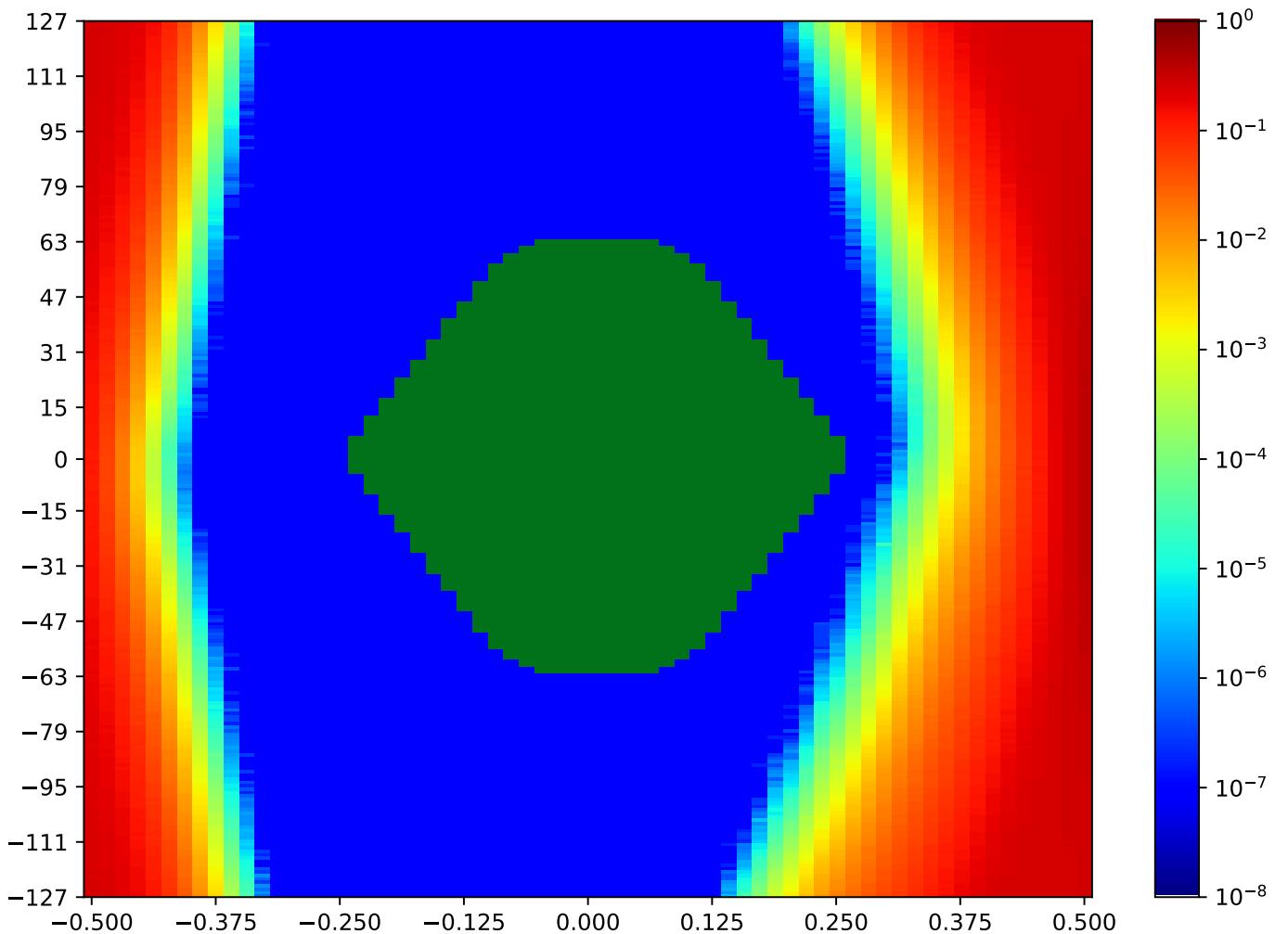


Figure 5.267: MSP_C_FPGA-TX3-00-RX3-00-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.2 MSP_C_FPGA-TX3-01-RX3-01-MSP_A_FPGA

Table 5.247: MSP_C_FPGA-TX3-01-RX3-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:32:22		2018-Sep-27 15:32:42	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8940	40	61.54%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

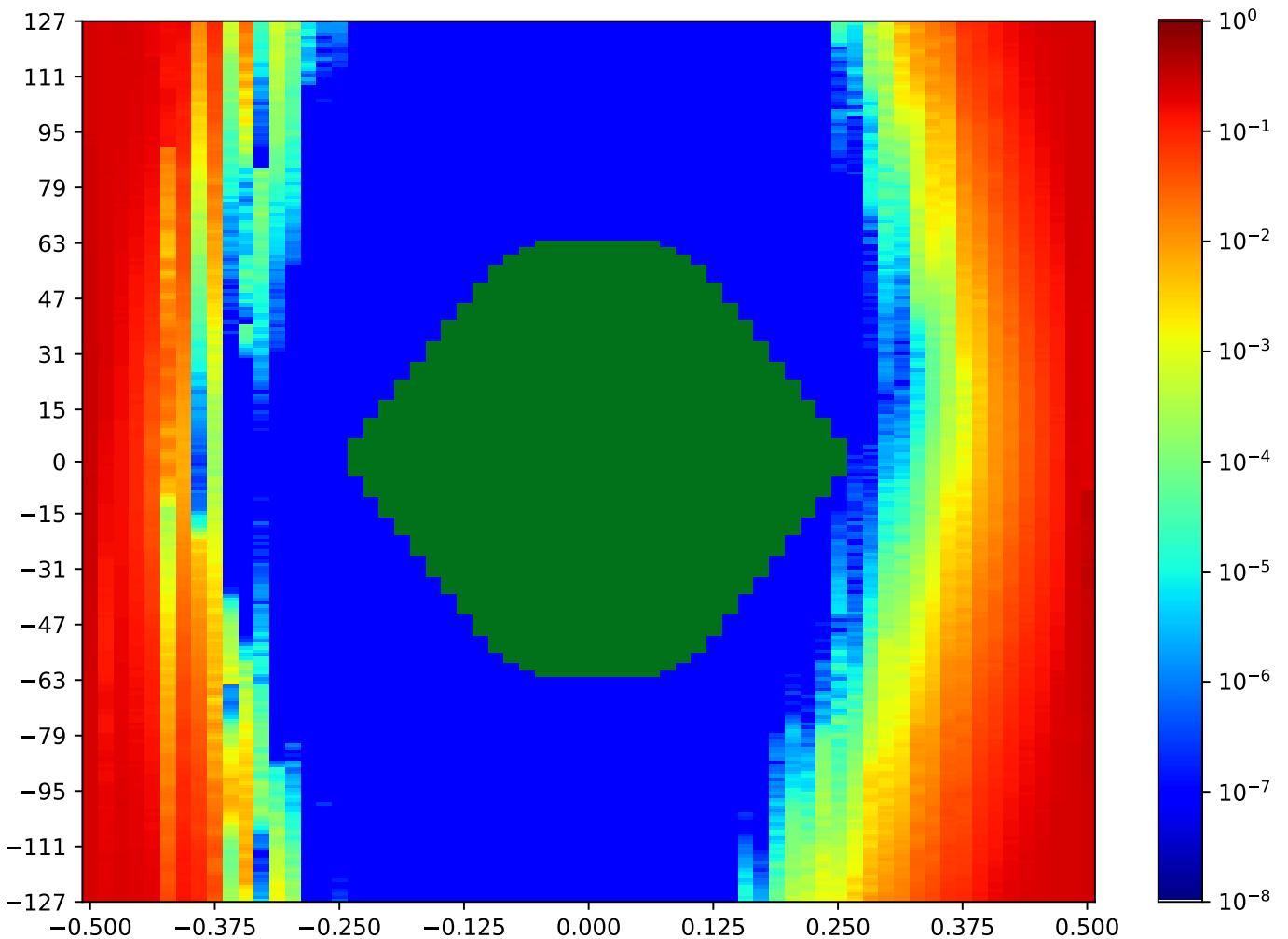


Figure 5.268: MSP_C_FPGA-TX3-01-RX3-01-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.3 MSP_C_FPGA-TX3-02-RX3-02-MSP_A_FPGA

Table 5.248: MSP_C_FPGA-TX3-02-RX3-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:32:43		2018-Sep-27 15:33:03	
Reset RX	OA	HO		VO	VO (%)
true	9453	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

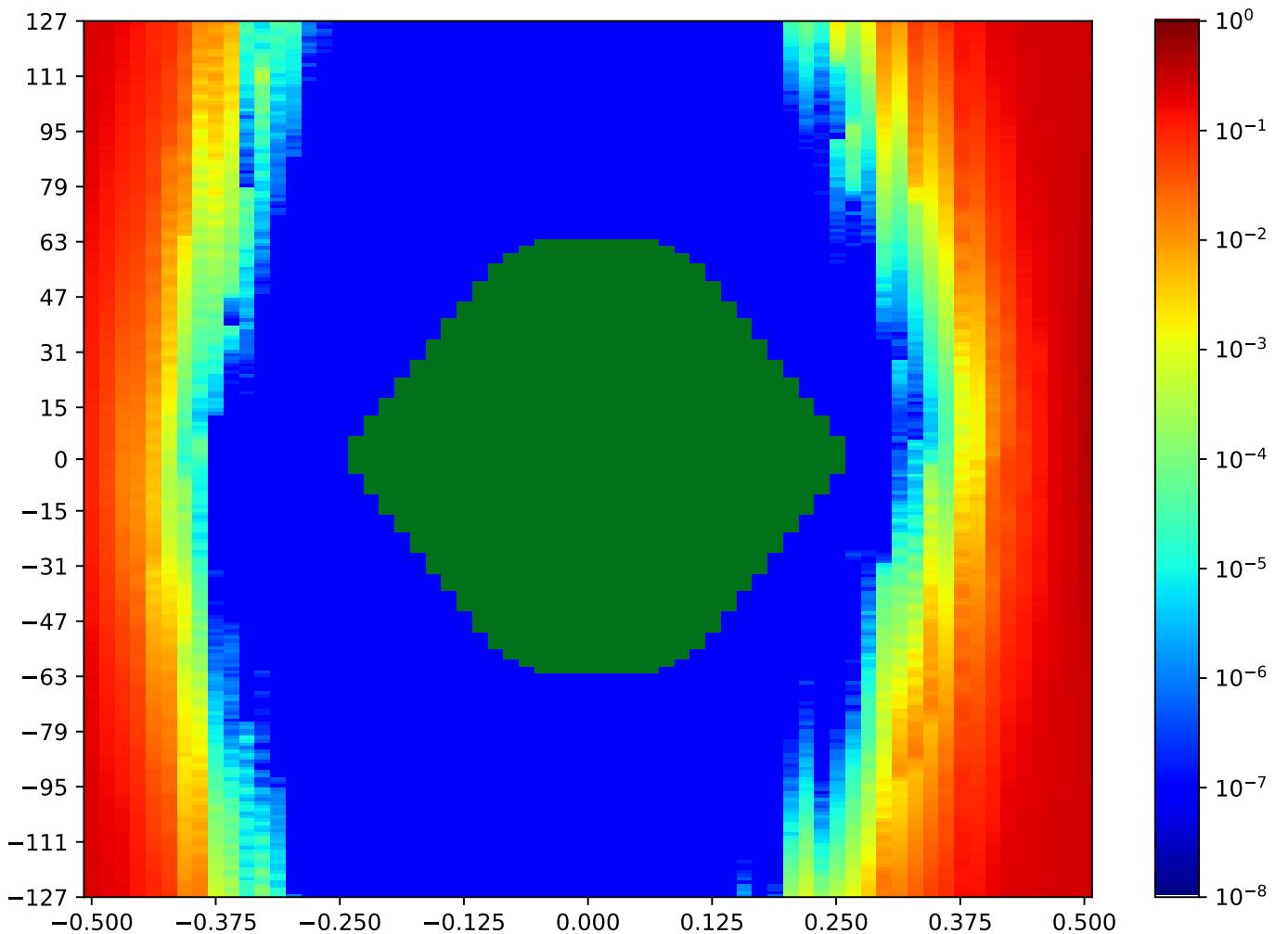


Figure 5.269: MSP_C_FPGA-TX3-02-RX3-02-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.4 MSP_C_FPGA-TX3-03-RX3-03-MSP_A_FPGA

Table 5.249: MSP_C_FPGA-TX3-03-RX3-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:31:01		2018-Sep-27 15:31:21	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	10030	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

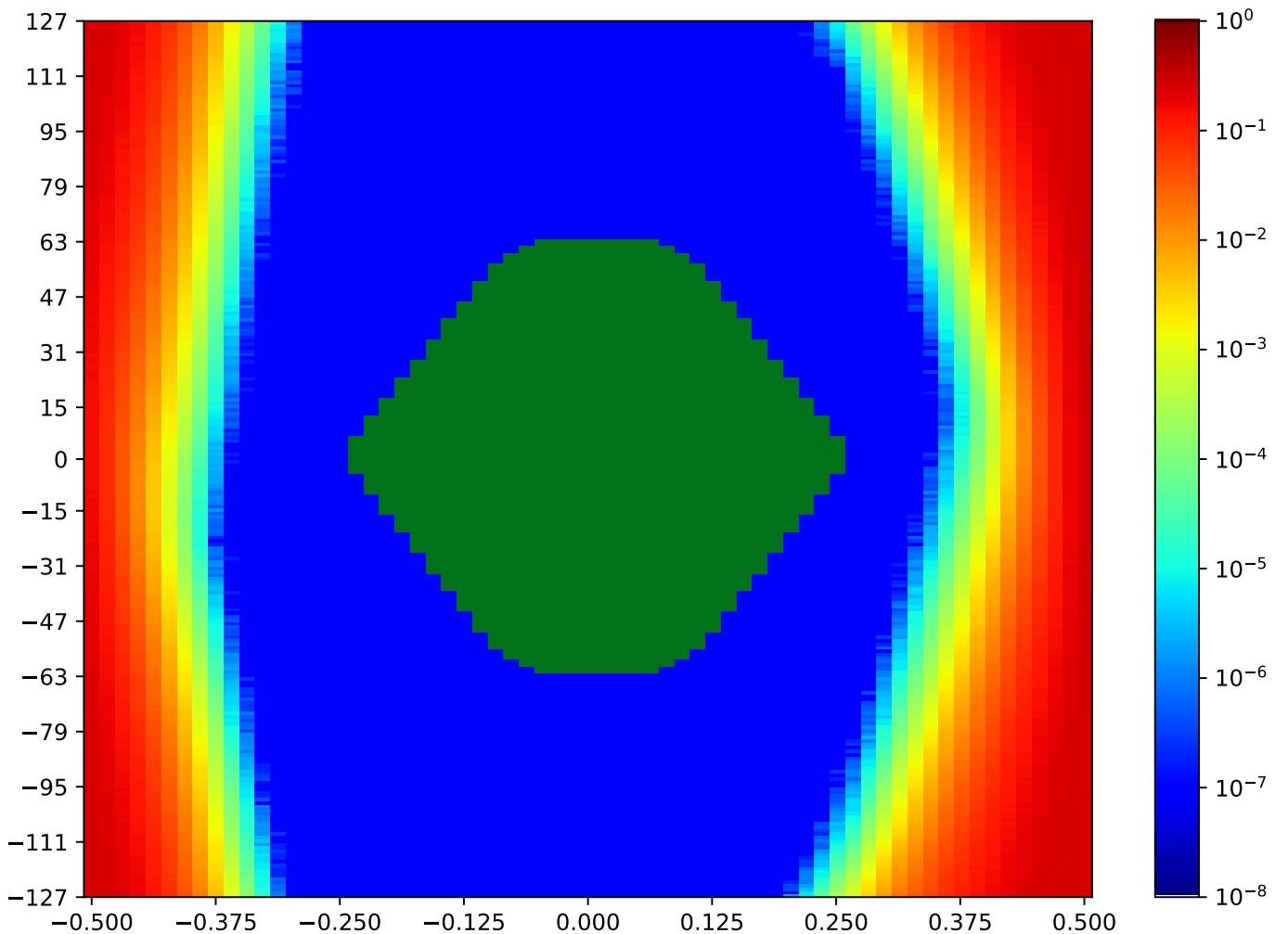


Figure 5.270: MSP_C_FPGA-TX3-03-RX3-03-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.5 MSP_C_FPGA-TX3-04-RX3-04-MSP_A_FPGA

Table 5.250: MSP_C_FPGA-TX3-04-RX3-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:33:44		2018-Sep-27 15:34:05	
Reset RX	OA	HO		VO	VO (%)
true	8495	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

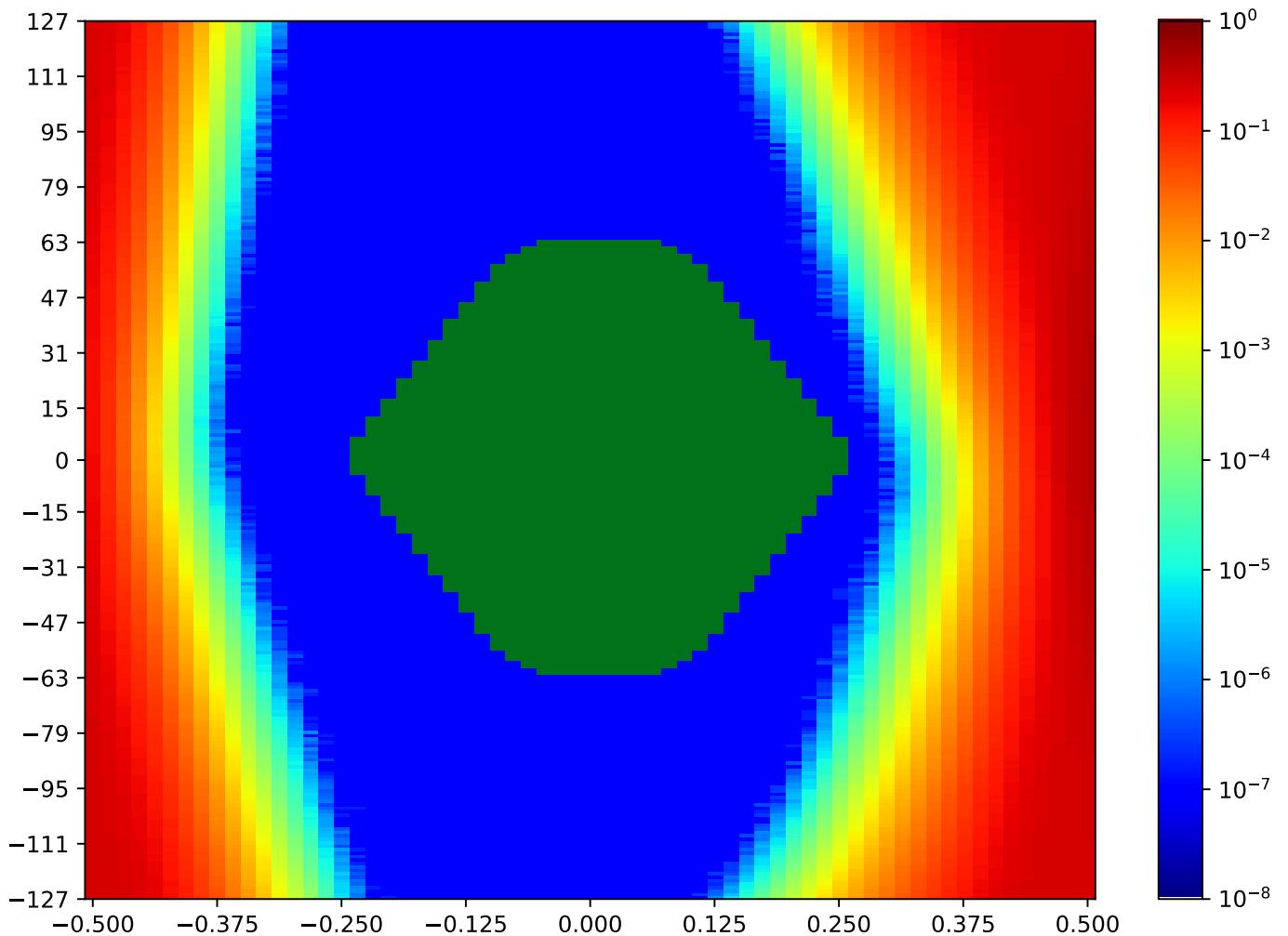


Figure 5.271: MSP_C_FPGA-TX3-04-RX3-04-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.6 MSP_C_FPGA-TX3-05-RX3-05-MSP_A_FPGA

Table 5.251: MSP_C_FPGA-TX3-05-RX3-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:30:41		2018-Sep-27 15:31:01	
Reset RX	OA	HO		VO	VO (%)
true	9208	45		252	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

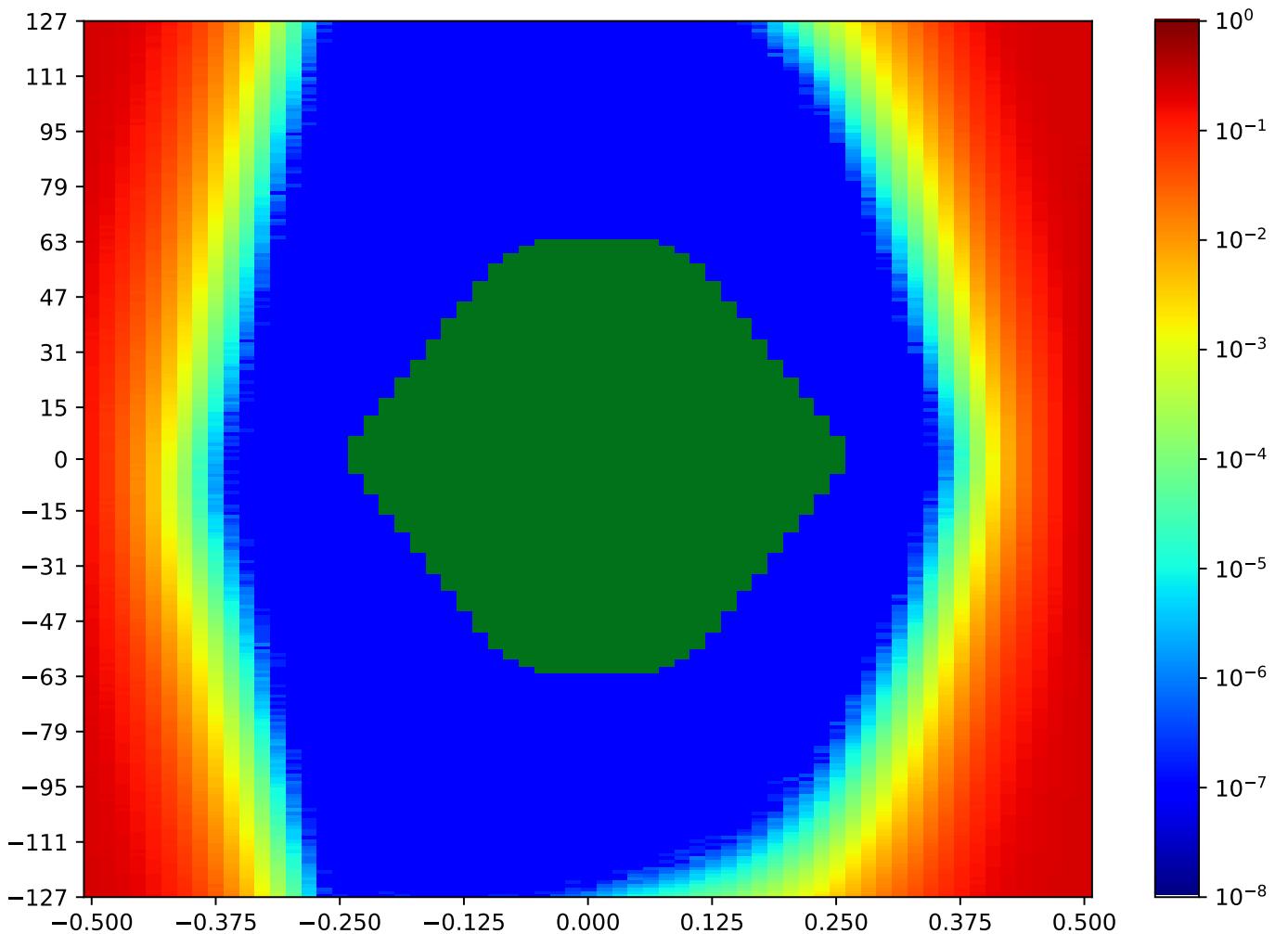


Figure 5.272: MSP_C_FPGA-TX3-05-RX3-05-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.7 MSP_C_FPGA-TX3-06-RX3-06-MSP_A_FPGA

Table 5.252: MSP_C_FPGA-TX3-06-RX3-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:34:26		2018-Sep-27 15:34:47	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8850	41	63.08%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

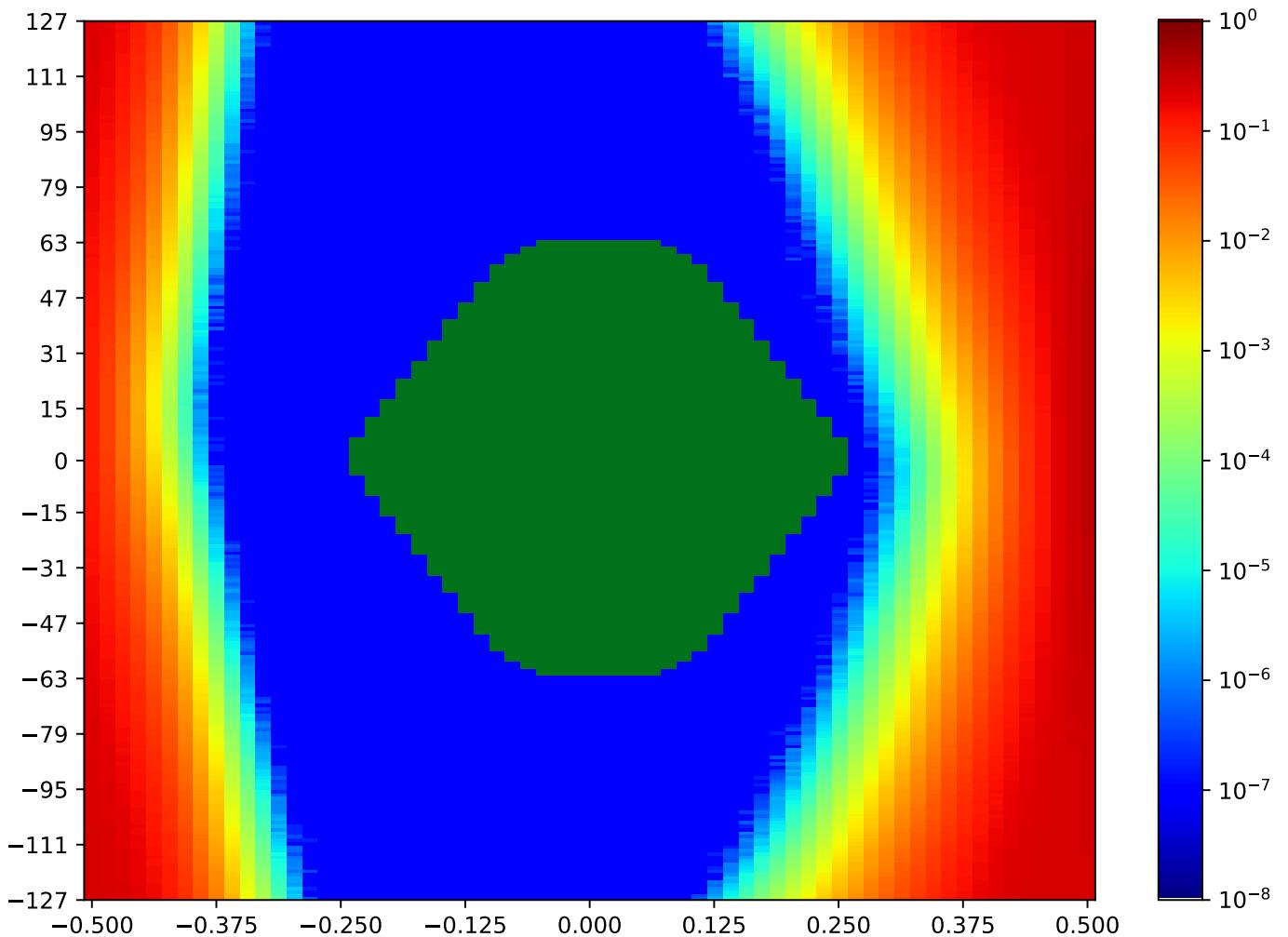


Figure 5.273: MSP_C_FPGA-TX3-06-RX3-06-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.8 MSP_C_FPGA-TX3-07-RX3-07-MSP_A_FPGA

Table 5.253: MSP_C_FPGA-TX3-07-RX3-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:31:21		2018-Sep-27 15:31:41	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8582	43	66.15%	235	92.16%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

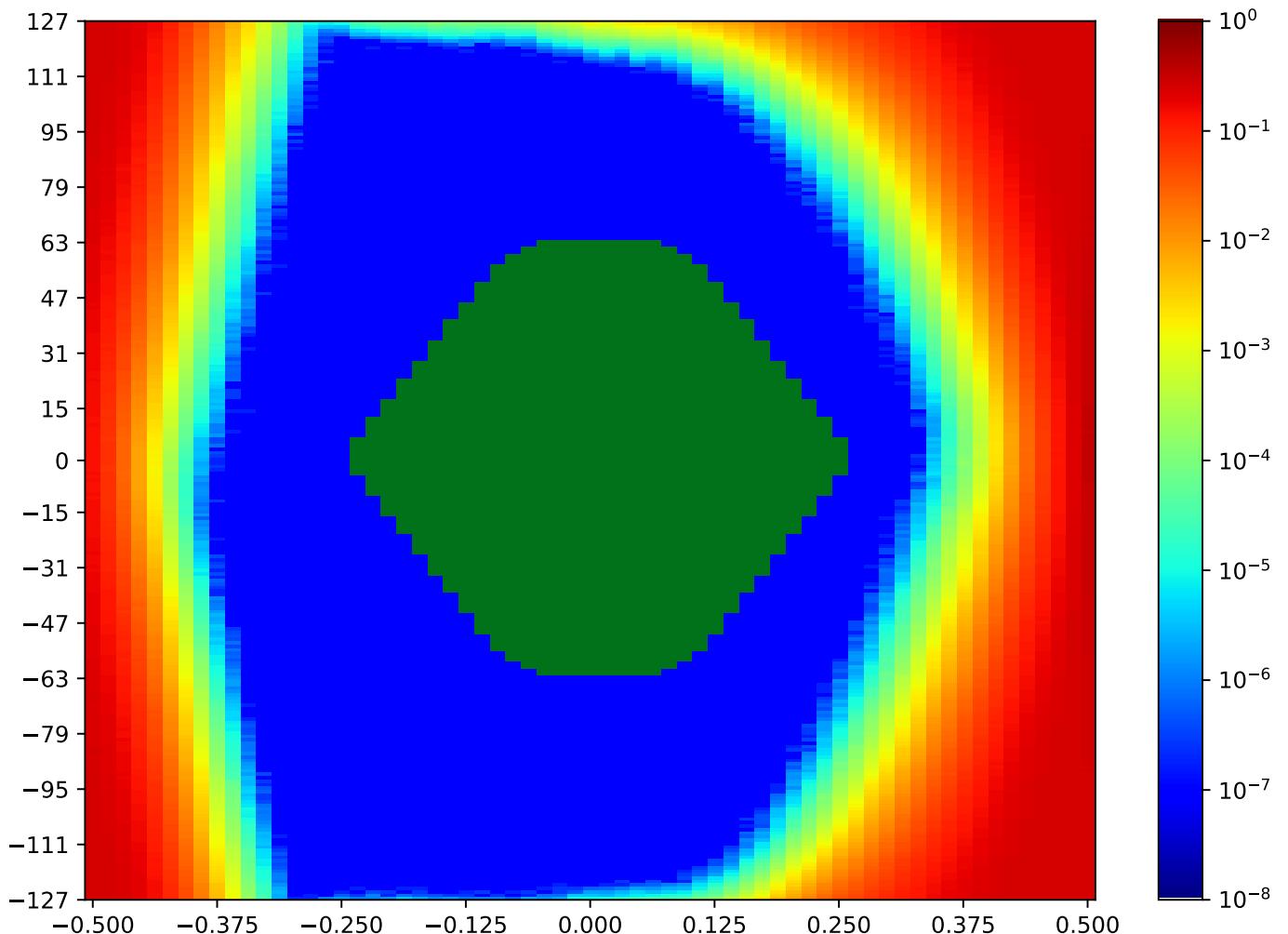


Figure 5.274: MSP_C_FPGA-TX3-07-RX3-07-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.9 MSP_C_FPGA-TX3-08-RX3-08-MSP_A_FPGA

Table 5.254: MSP_C_FPGA-TX3-08-RX3-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:34:05		2018-Sep-27 15:34:26	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9739	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

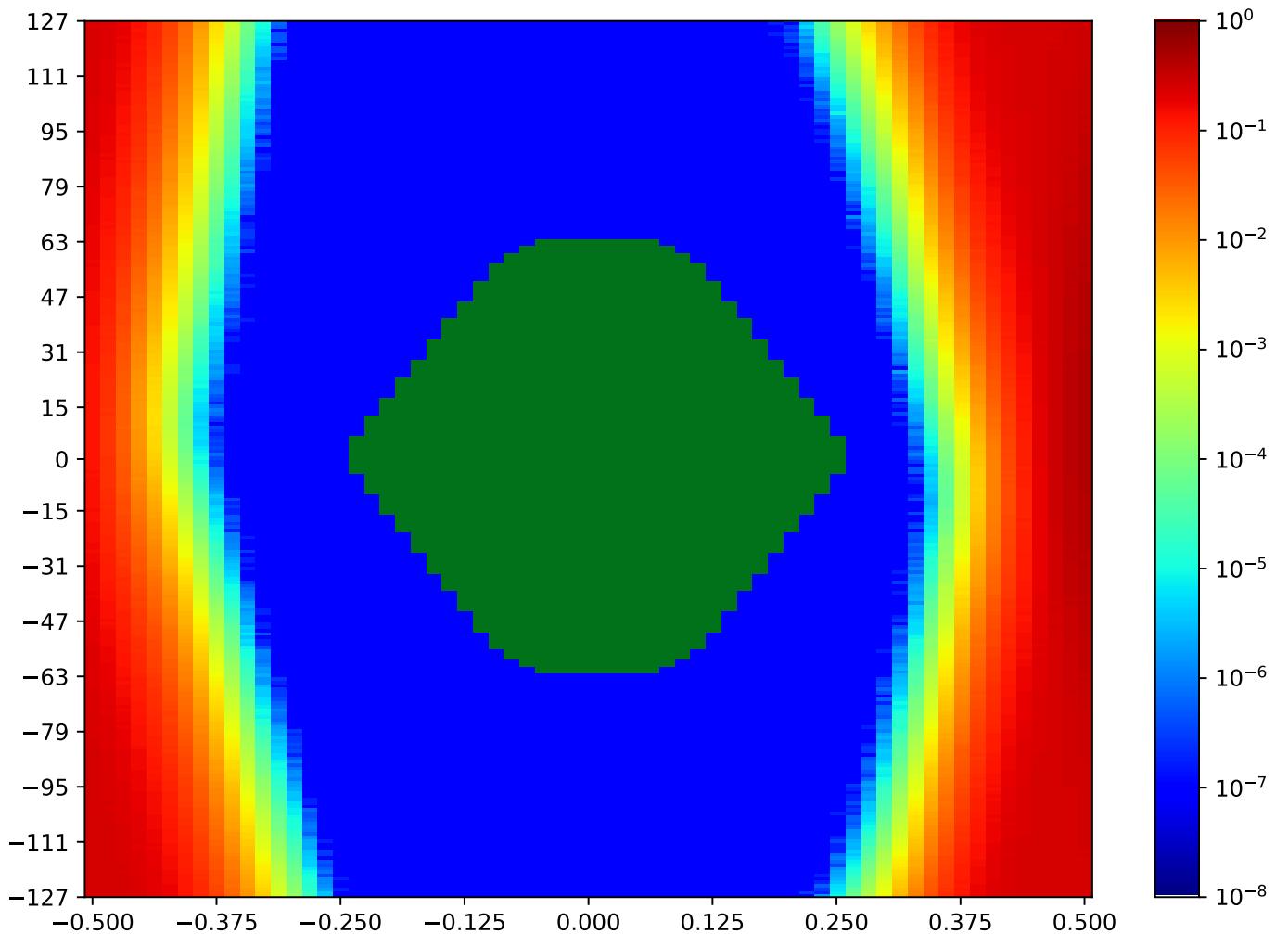


Figure 5.275: MSP_C_FPGA-TX3-08-RX3-08-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.10 MSP_C_FPGA-TX3-09-RX3-09-MSP_A_FPGA

Table 5.255: MSP_C_FPGA-TX3-09-RX3-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:32:02		2018-Sep-27 15:32:22	
Reset RX	OA	HO		VO	VO (%)
true	9600	47		70.77%	252 98.43%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

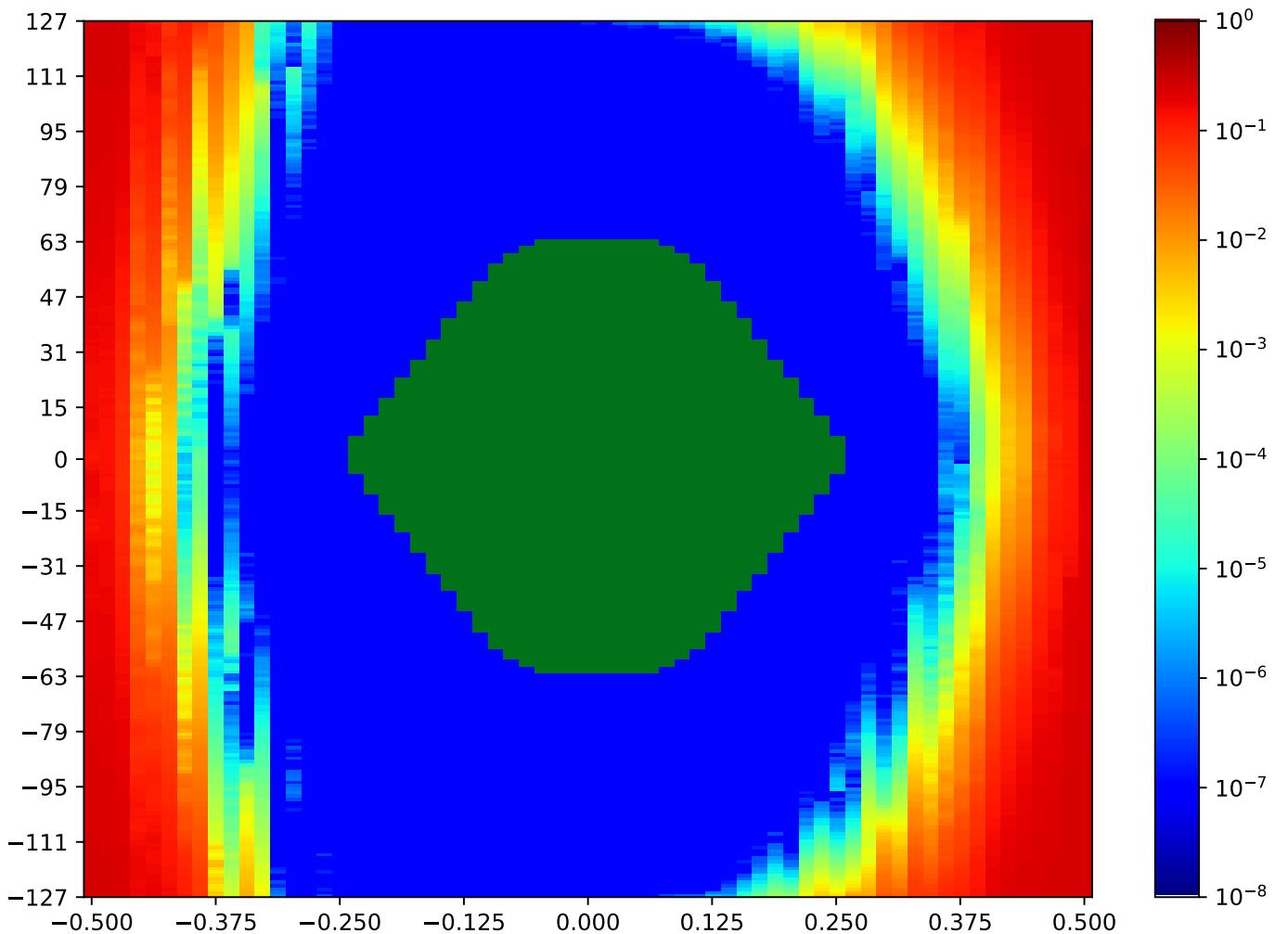


Figure 5.276: MSP_C_FPGA-TX3-09-RX3-09-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.11 MSP_C_FPGA-TX3-10-RX3-10-MSP_A_FPGA

Table 5.256: MSP_C_FPGA-TX3-10-RX3-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:33:24		2018-Sep-27 15:33:44	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9688	43	66.15%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

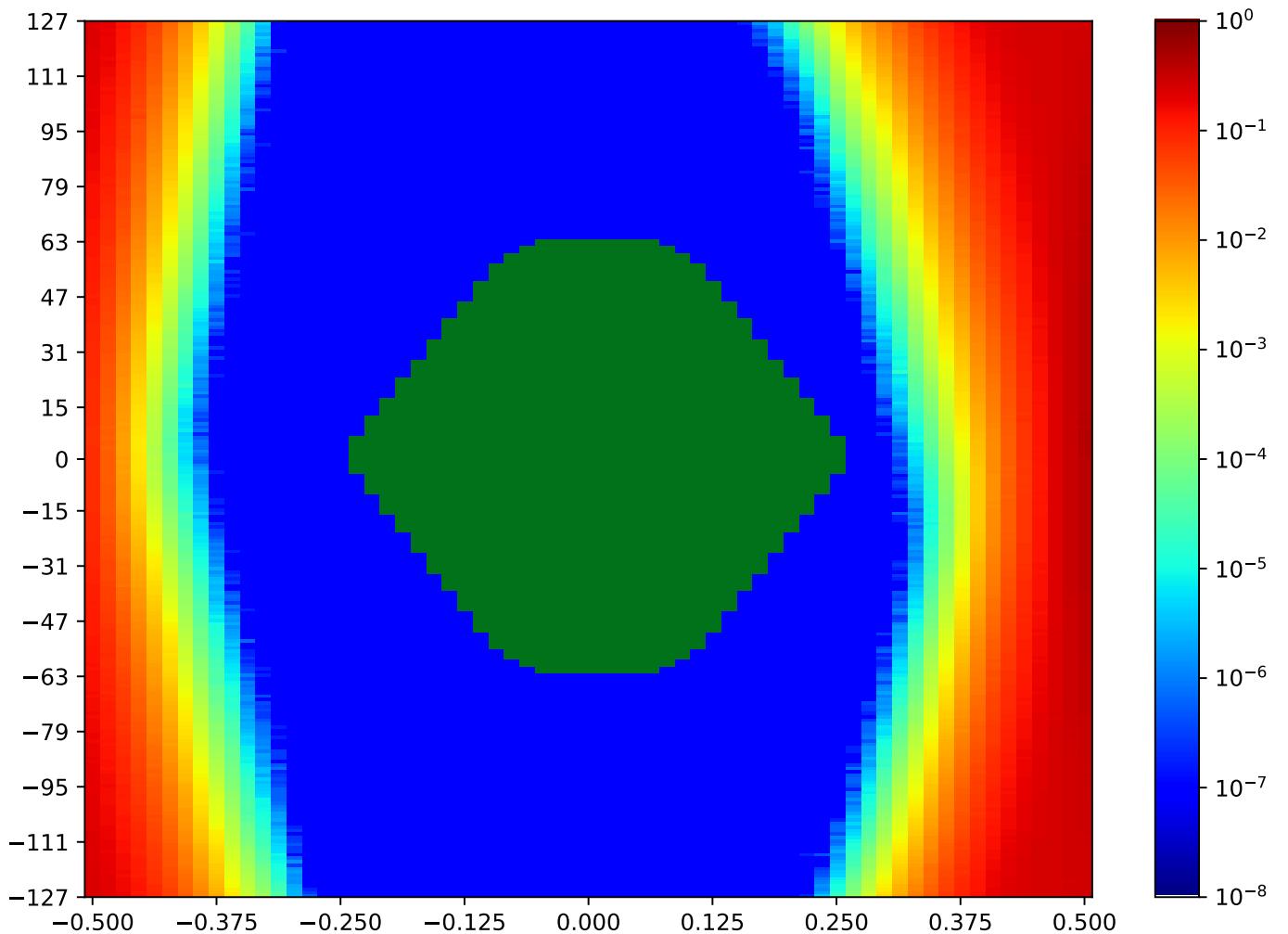


Figure 5.277: MSP_C_FPGA-TX3-10-RX3-10-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.21.12 MSP_C_FPGA-TX3-11-RX3-11-MSP_A_FPGA

Table 5.257: MSP_C_FPGA-TX3-11-RX3-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:33:03		2018-Sep-27 15:33:23	
Reset RX	OA	HO		VO	VO (%)
true	9702	45		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

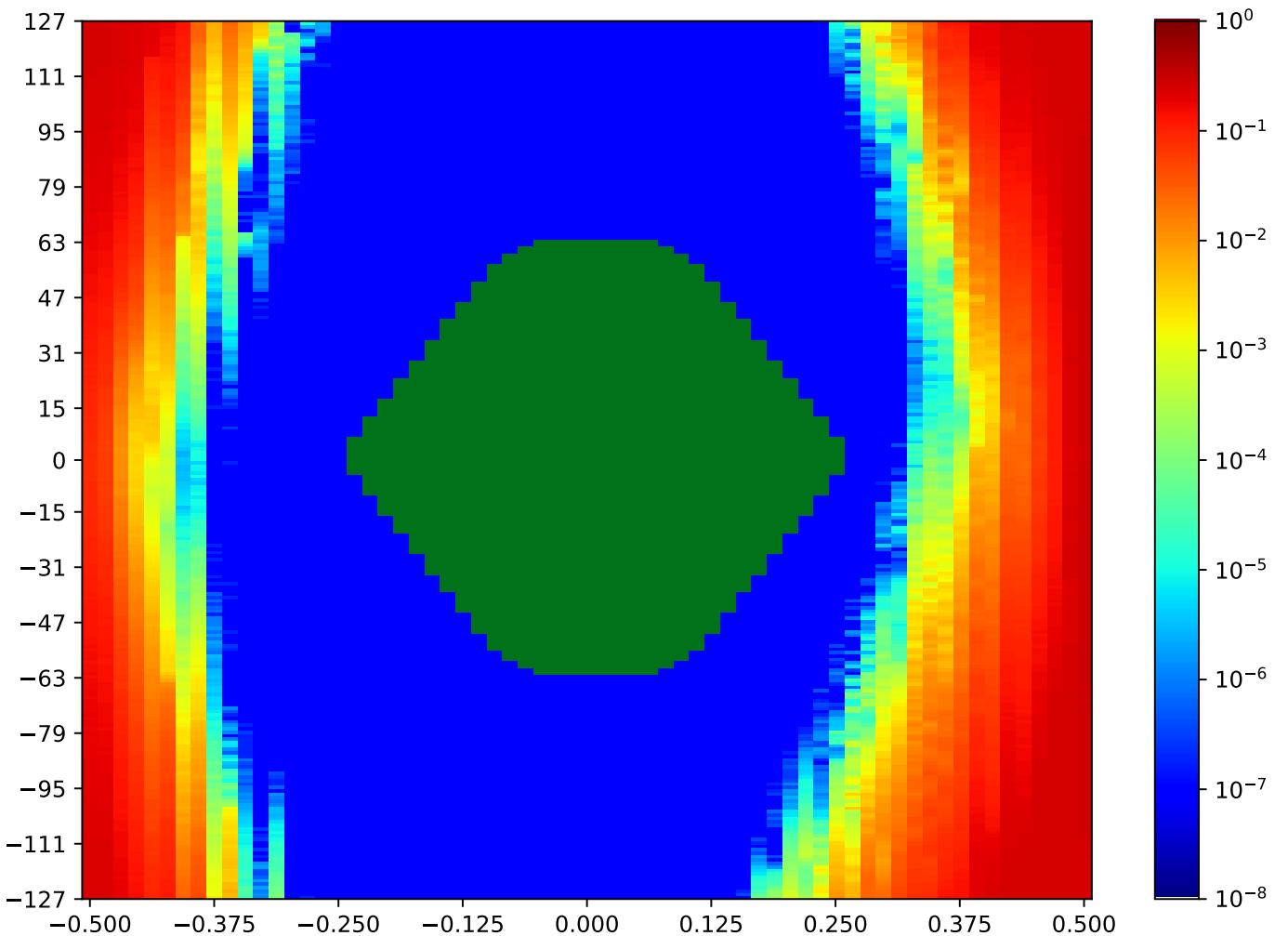


Figure 5.278: MSP_C_FPGA-TX3-11-RX3-11-MSP_A_FPGA

Call back to summary Figure 5.266. Sibling eye diagrams: V2-6.4.

5.22 MSP_C TX4 MSP_A RX4 Minipod Loopback

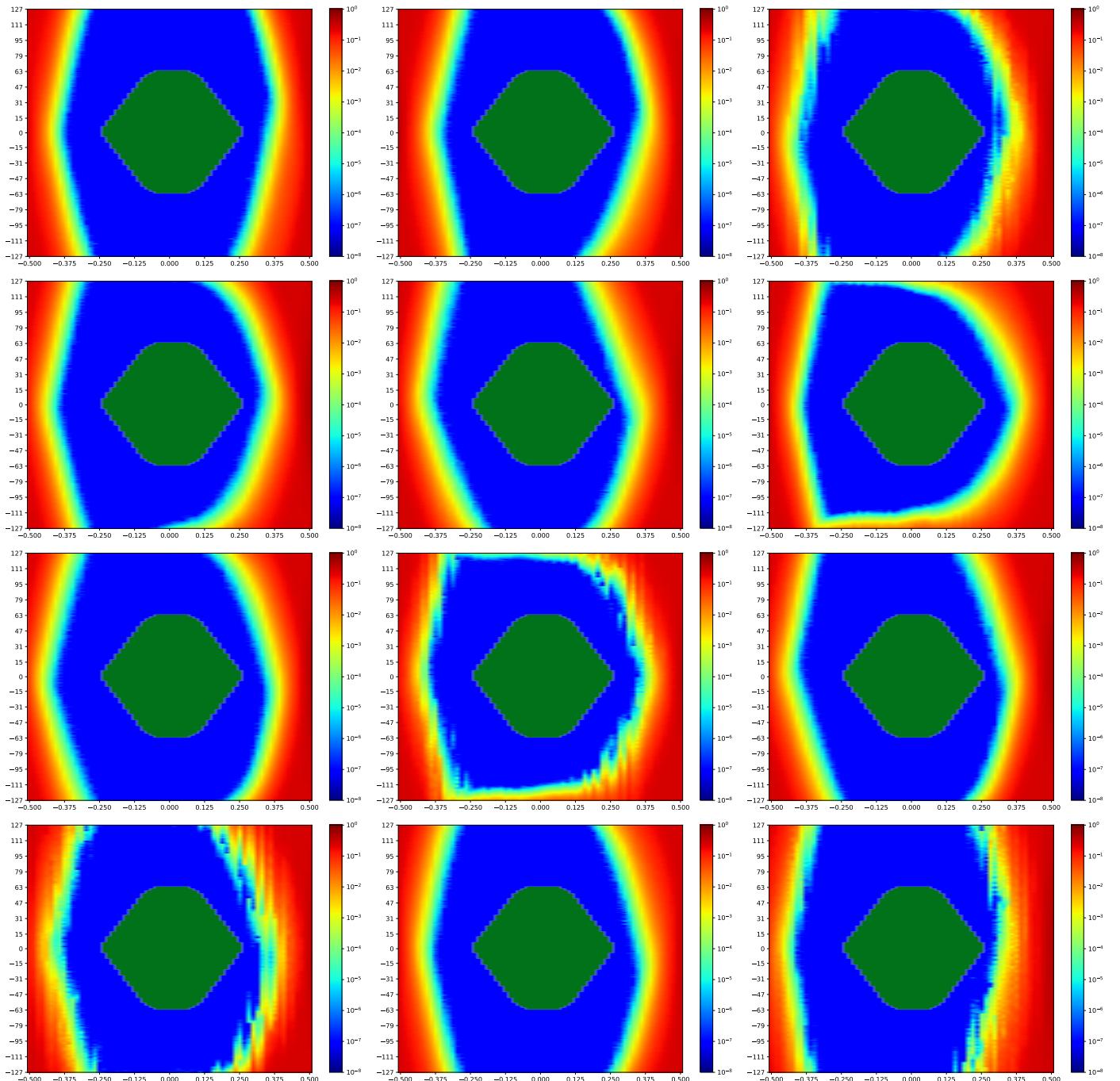


Figure 5.279: MSP_C TX4 MSP_A RX4 Minipod Loopback

A cross-reference to Figure 5.279. Sibling eye diagrams: V2-6.4.

Next summary Figure 5.279.

5.22.1 MSP_C_FPGA-TX4-00-RX4-00-MSP_A_FPGA

Table 5.258: MSP_C_FPGA-TX4-00-RX4-00-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:35:48		2018-Sep-27 15:36:08	
Reset RX	OA	HO		VO	VO (%)
true	9885	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

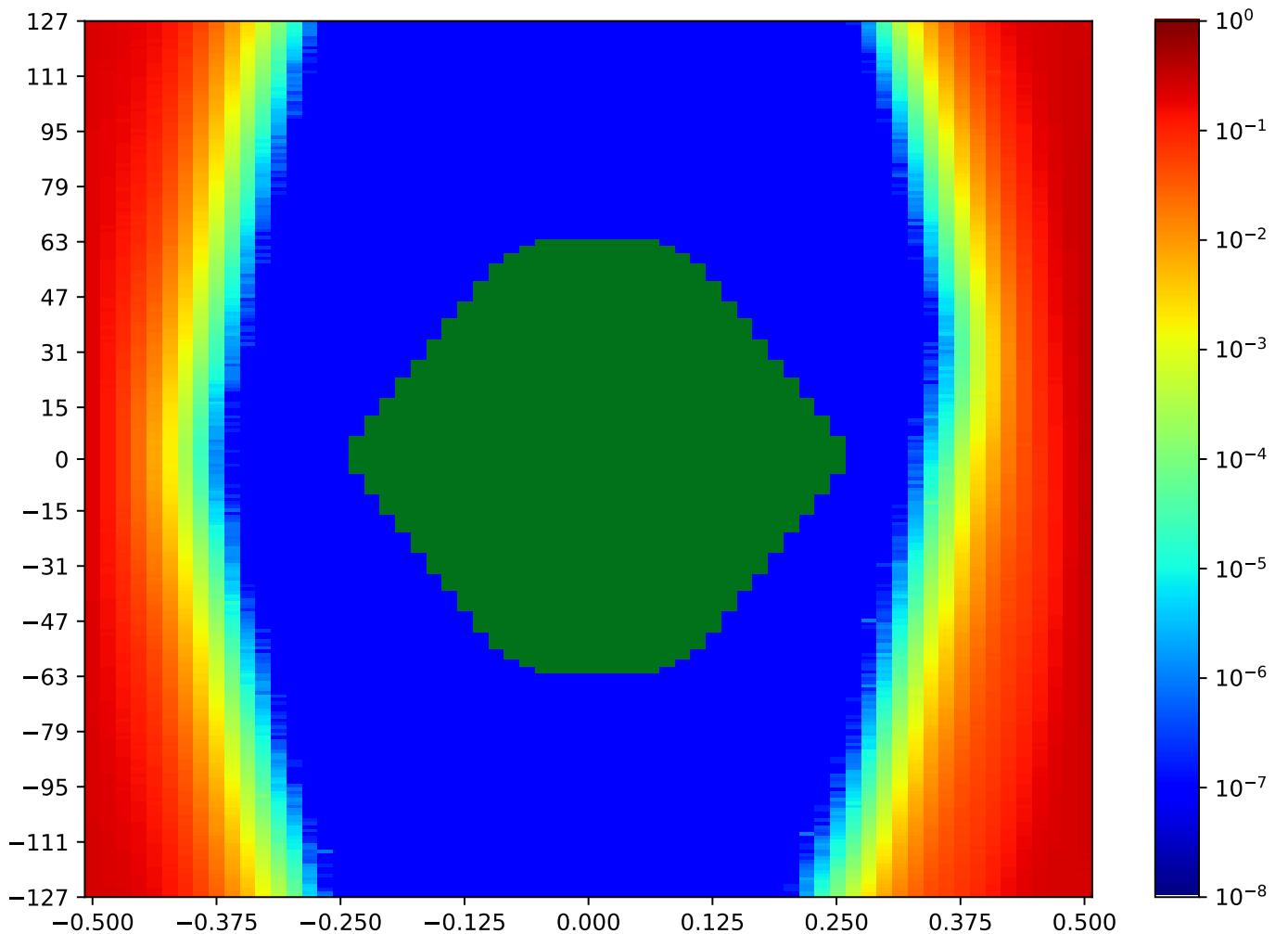


Figure 5.280: MSP_C_FPGA-TX4-00-RX4-00-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.2 MSP_C_FPGA-TX4-01-RX4-01-MSP_A_FPGA

Table 5.259: MSP_C_FPGA-TX4-01-RX4-01-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:35:07		2018-Sep-27 15:35:27	
Reset RX	OA	HO		VO	VO (%)
true	8818	41		63.08%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

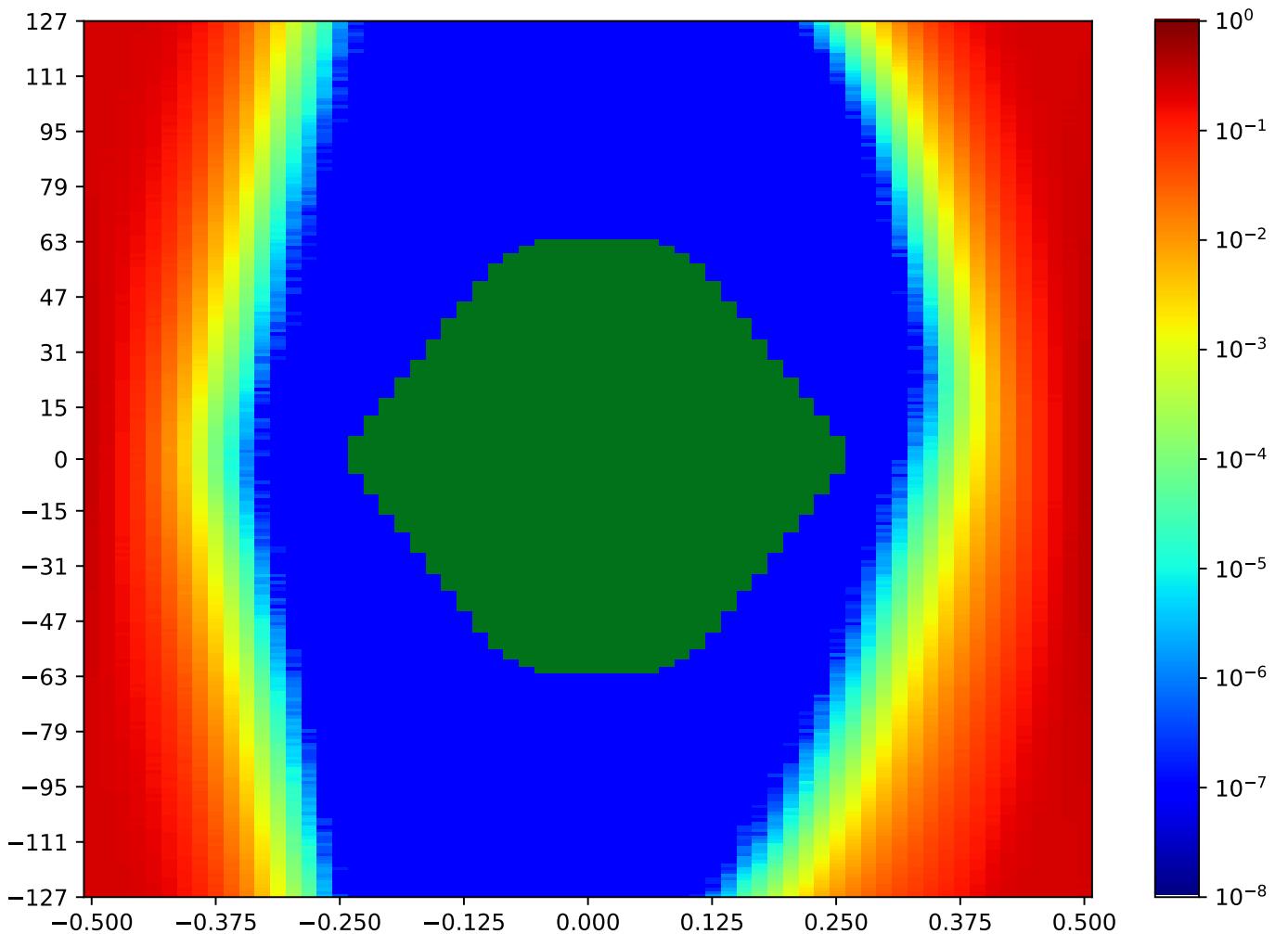


Figure 5.281: MSP_C_FPGA-TX4-01-RX4-01-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.3 MSP_C_FPGA-TX4-02-RX4-02-MSP_A_FPGA

Table 5.260: MSP_C_FPGA-TX4-02-RX4-02-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:36:49		2018-Sep-27 15:37:09	
Reset RX	OA	HO		VO	VO (%)
true	8839	40		61.54%	251 98.04%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

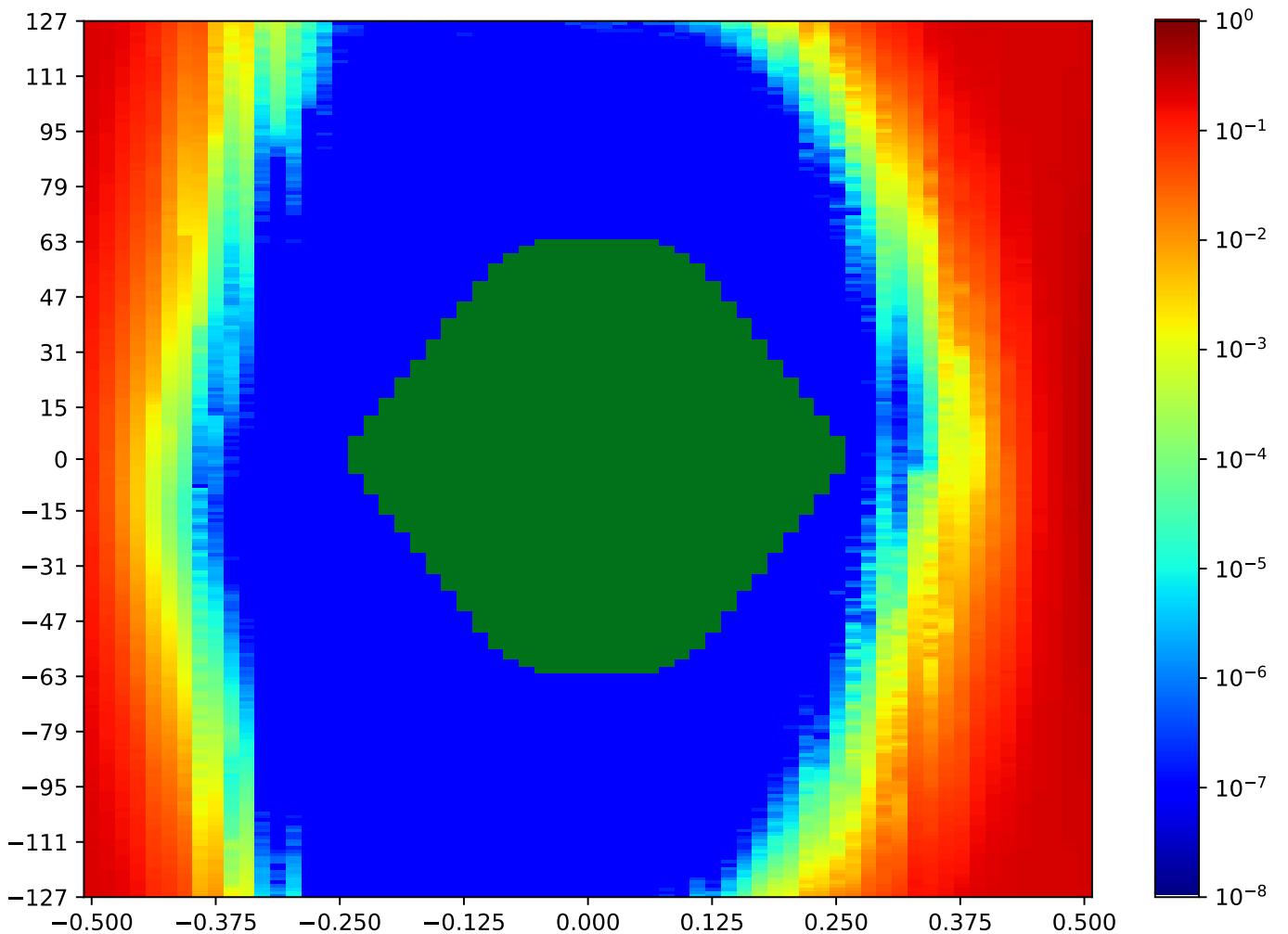


Figure 5.282: MSP_C_FPGA-TX4-02-RX4-02-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.4 MSP_C_FPGA-TX4-03-RX4-03-MSP_A_FPGA

Table 5.261: MSP_C_FPGA-TX4-03-RX4-03-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:34:47		2018-Sep-27 15:35:07	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	8899	43	66.15%	247	96.08%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

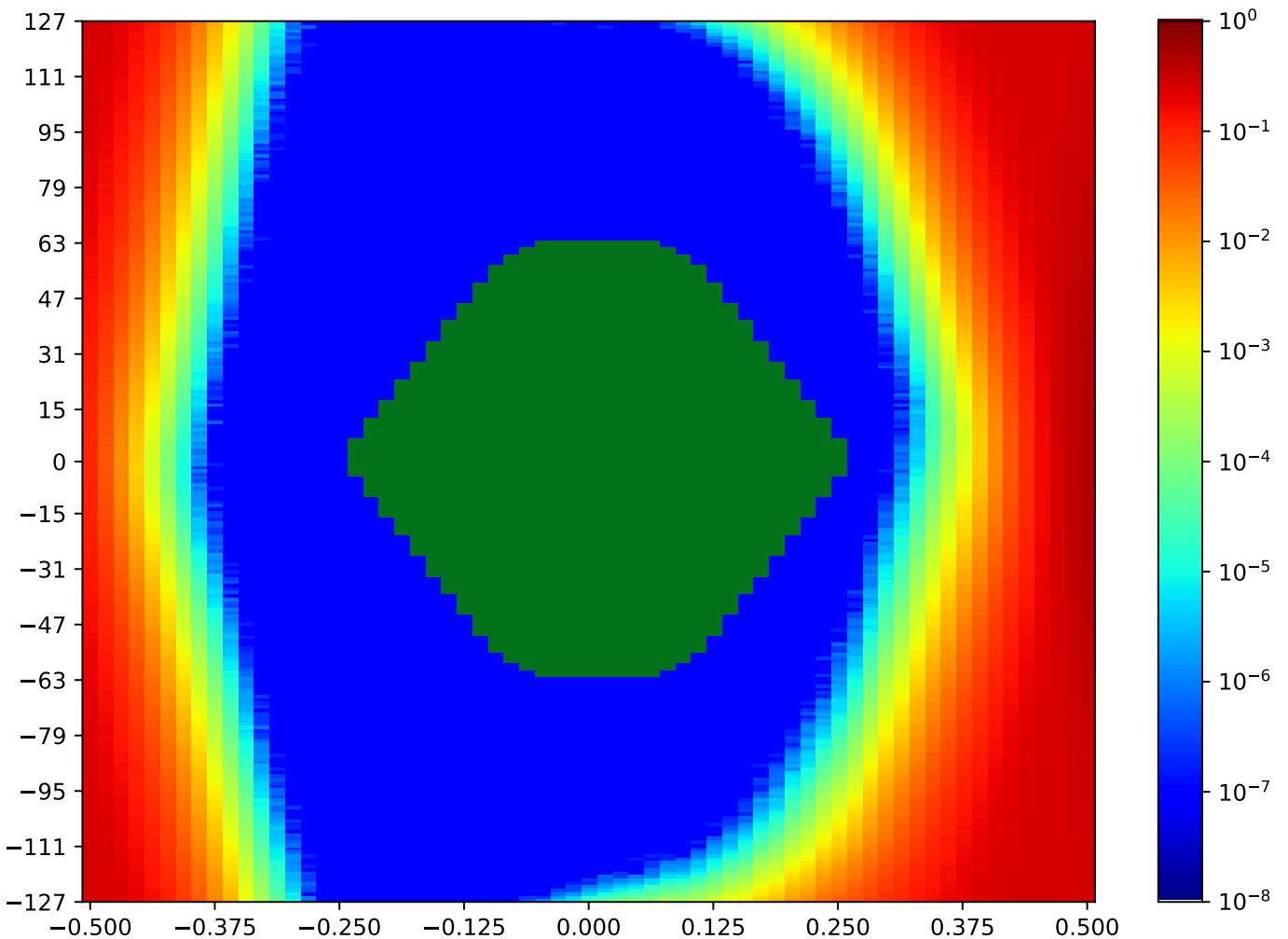


Figure 5.283: MSP_C_FPGA-TX4-03-RX4-03-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.5 MSP_C_FPGA-TX4-04-RX4-04-MSP_A_FPGA

Table 5.262: MSP_C_FPGA-TX4-04-RX4-04-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:37:50		2018-Sep-27 15:38:15	
Reset RX	OA	HO		VO	VO (%)
true	8215	40		255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

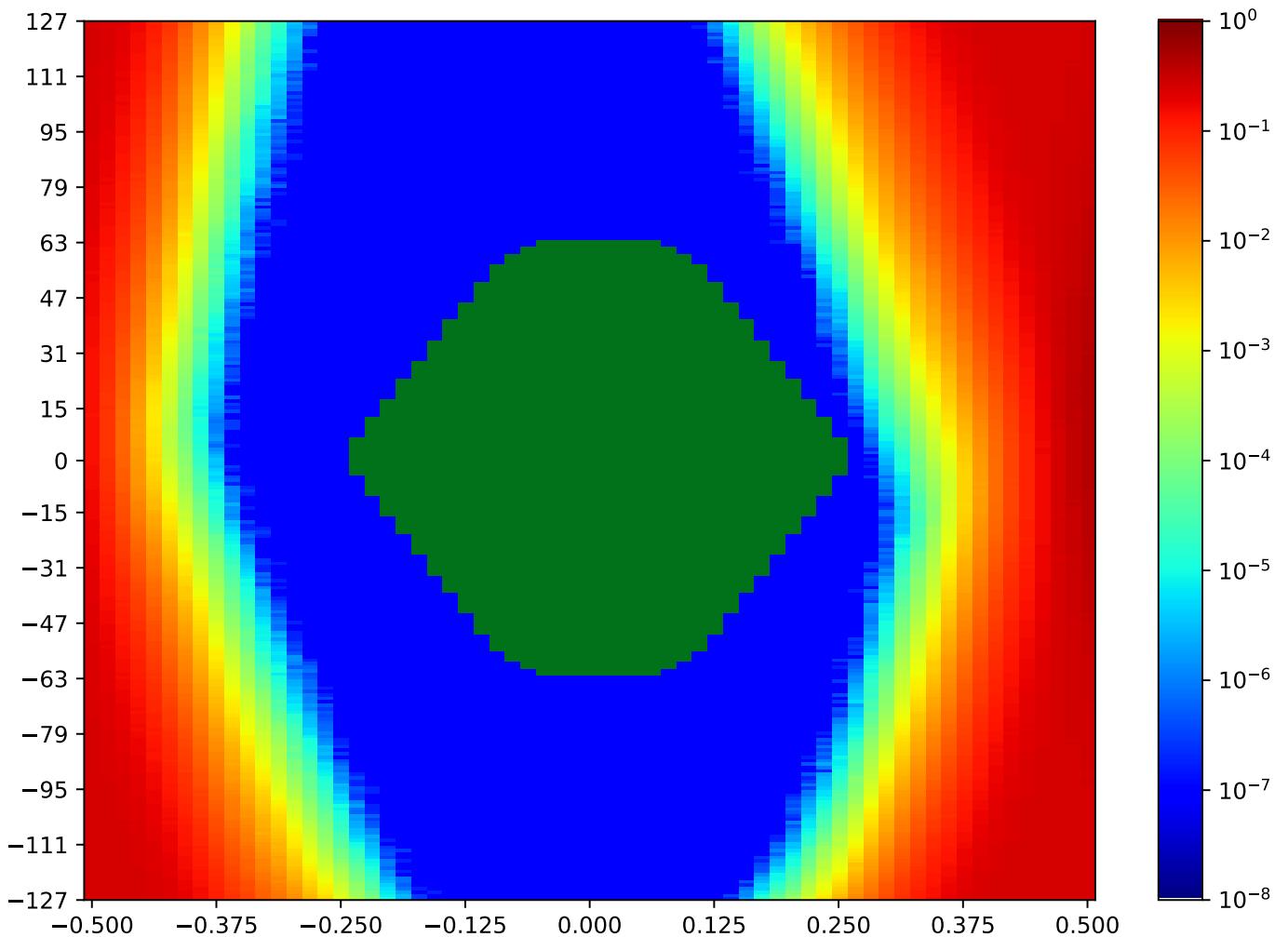


Figure 5.284: MSP_C_FPGA-TX4-04-RX4-04-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.6 MSP_C_FPGA-TX4-05-RX4-05-MSP_A_FPGA

Table 5.263: MSP_C_FPGA-TX4-05-RX4-05-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:35:27		2018-Sep-27 15:35:48	
Reset RX	OA	HO		VO	VO (%)
true	7947	44		218	85.49%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

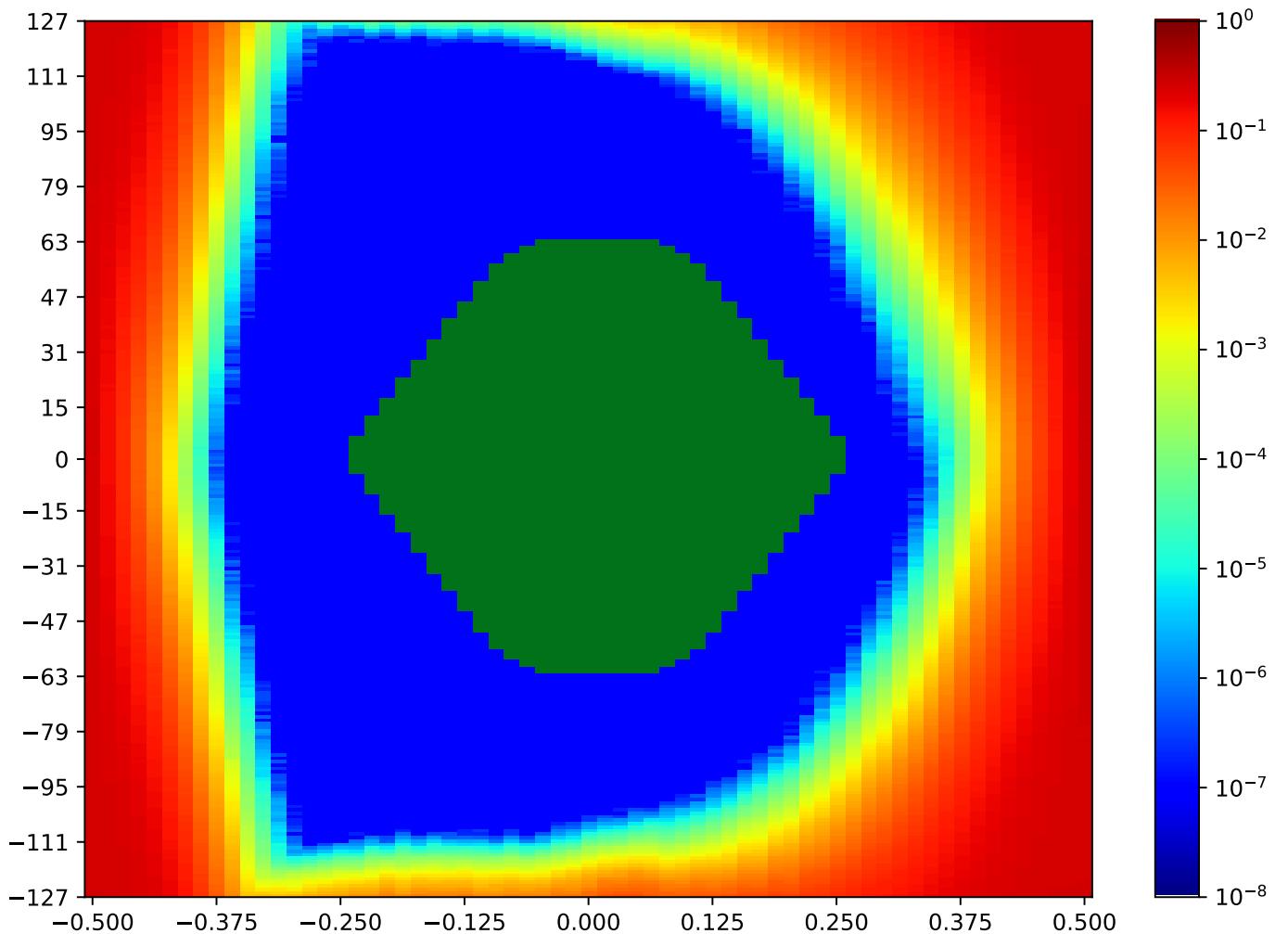


Figure 5.285: MSP_C_FPGA-TX4-05-RX4-05-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.7 MSP_C_FPGA-TX4-06-RX4-06-MSP_A_FPGA

Table 5.264: MSP_C_FPGA-TX4-06-RX4-06-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:38:35		2018-Sep-27 15:38:56	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	9563	44		67.69%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

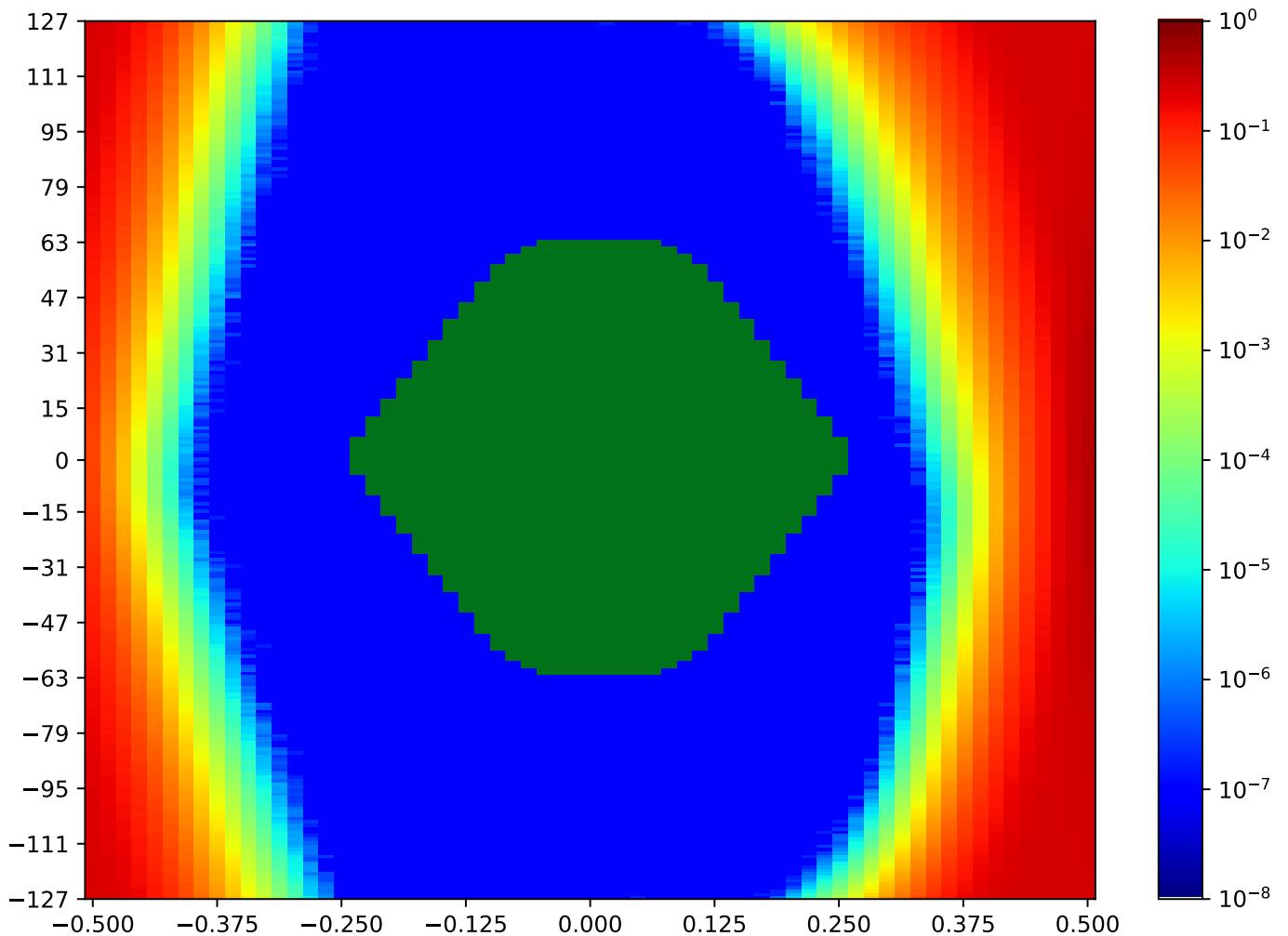


Figure 5.286: MSP_C_FPGA-TX4-06-RX4-06-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.8 MSP_C_FPGA-TX4-07-RX4-07-MSP_A_FPGA

Table 5.265: MSP_C_FPGA-TX4-07-RX4-07-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:36:08		2018-Sep-27 15:36:29	
Reset RX	OA	HO		HO (%)	VO VO (%)
true	8466	47		72.31%	226 88.63%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

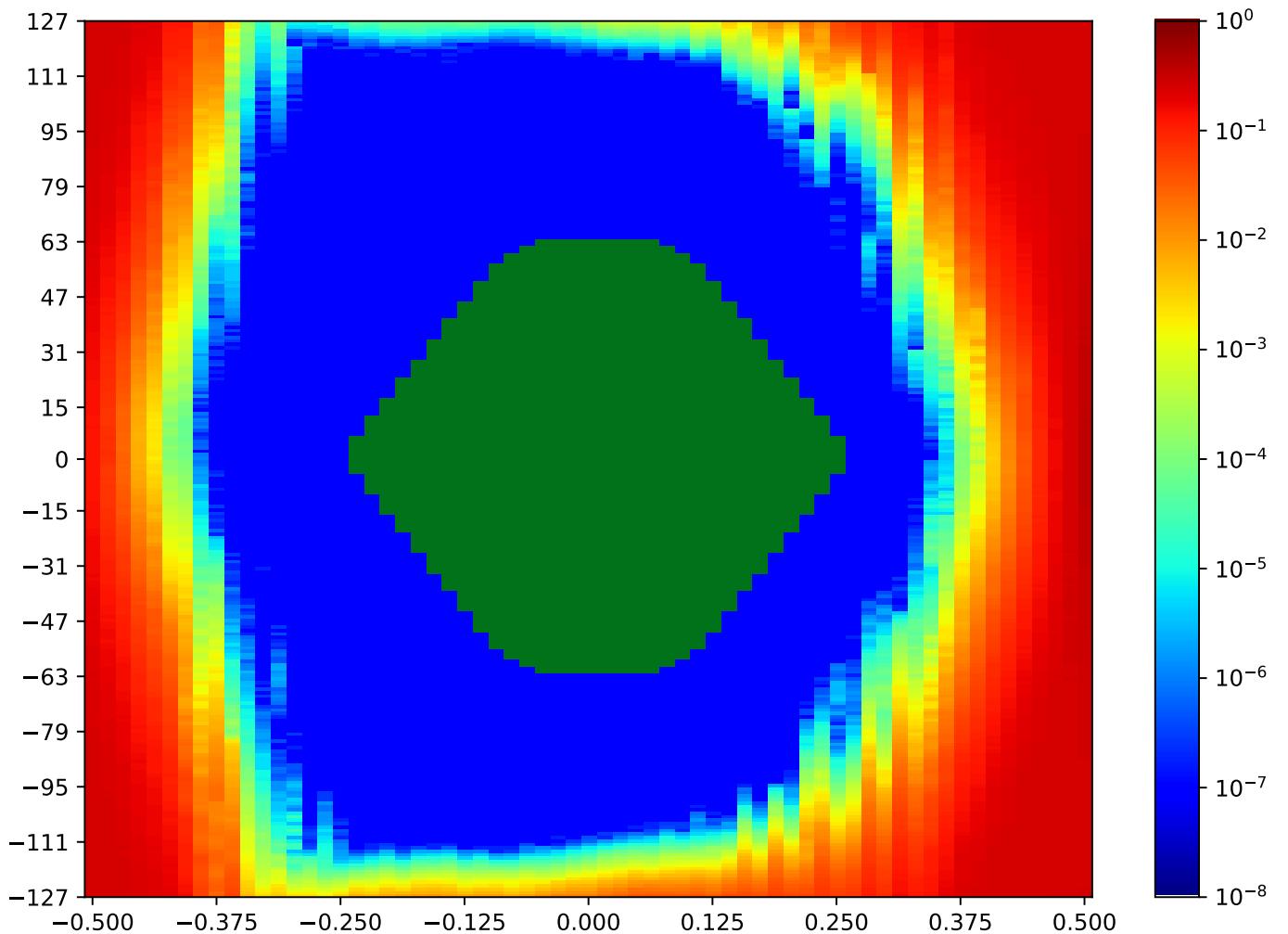


Figure 5.287: MSP_C_FPGA-TX4-07-RX4-07-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.9 MSP_C_FPGA-TX4-08-RX4-08-MSP_A_FPGA

Table 5.266: MSP_C_FPGA-TX4-08-RX4-08-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:38:15		2018-Sep-27 15:38:35	
Reset RX	OA	HO		VO	VO (%)
true	9231	42		64.62%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

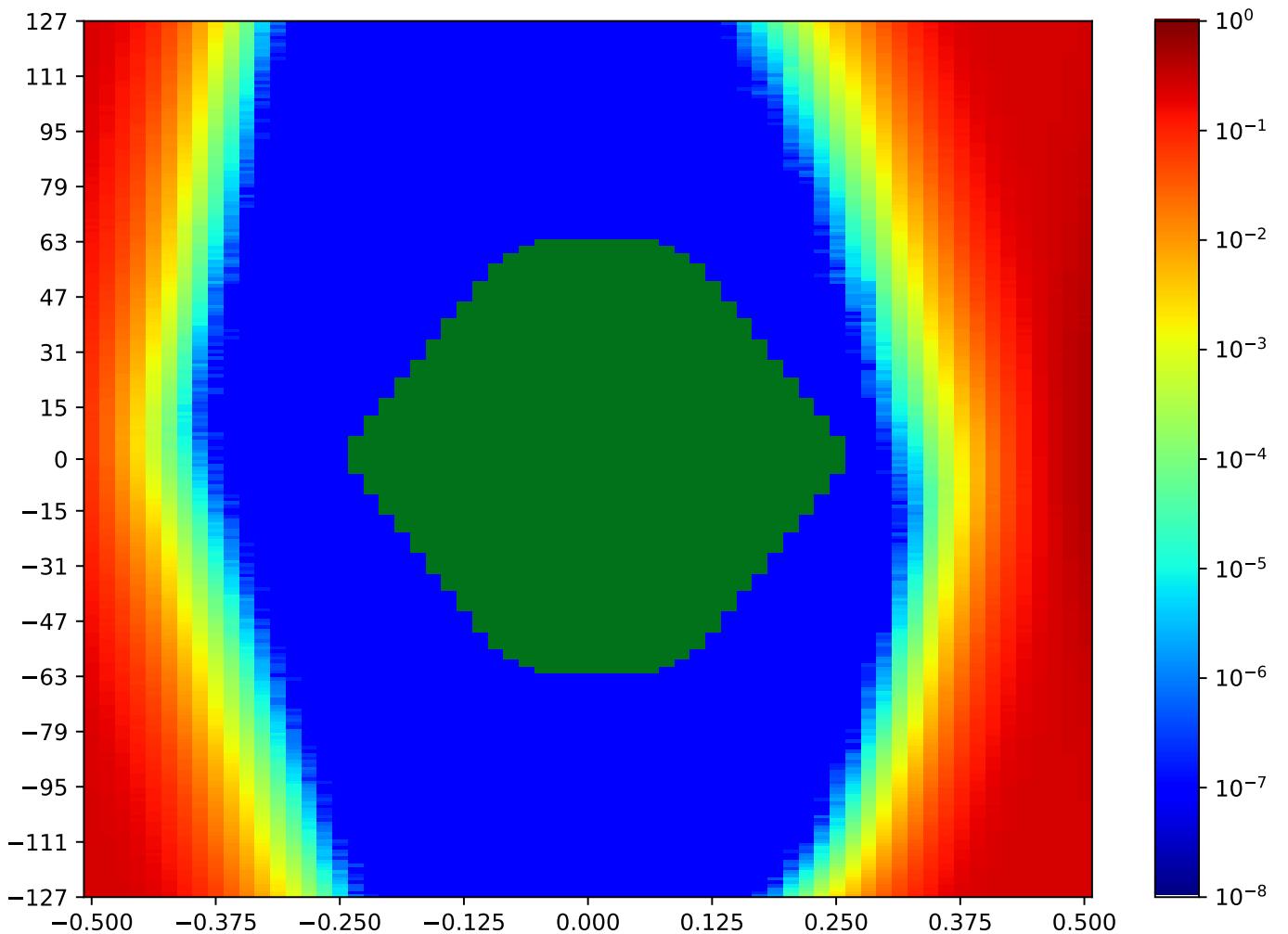


Figure 5.288: MSP_C_FPGA-TX4-08-RX4-08-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.10 MSP_C_FPGA-TX4-09-RX4-09-MSP_A_FPGA

Table 5.267: MSP_C_FPGA-TX4-09-RX4-09-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:36:29		2018-Sep-27 15:36:49	
Reset RX	OA	HO		VO	VO (%)
true	9022	44		252	98.82%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

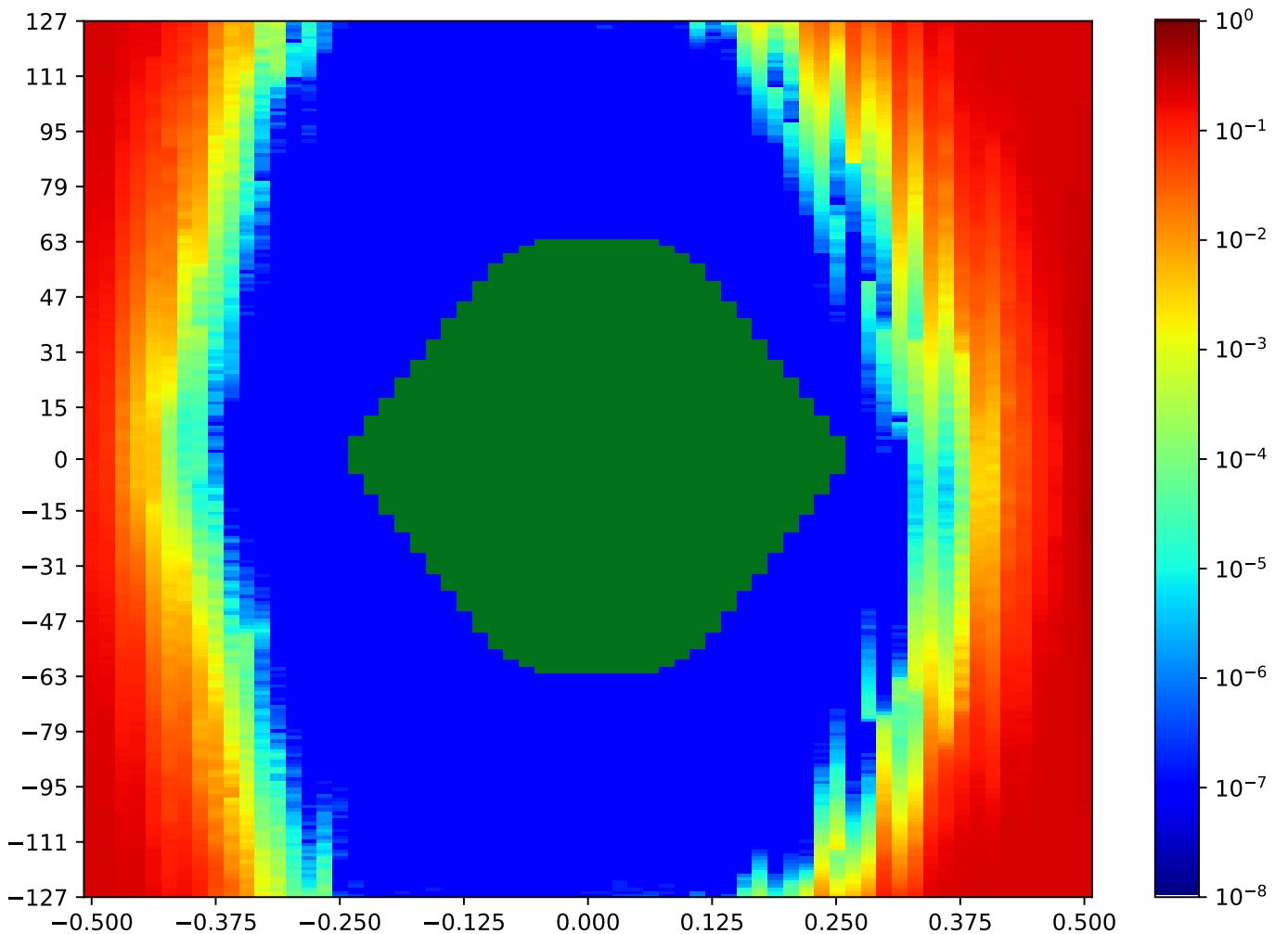


Figure 5.289: MSP_C_FPGA-TX4-09-RX4-09-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.11 MSP_C_FPGA-TX4-10-RX4-10-MSP_A_FPGA

Table 5.268: MSP_C_FPGA-TX4-10-RX4-10-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:37:30		2018-Sep-27 15:37:50	
Reset RX	OA	HO	HO (%)	VO	VO (%)
true	9613	44	67.69%	255	100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

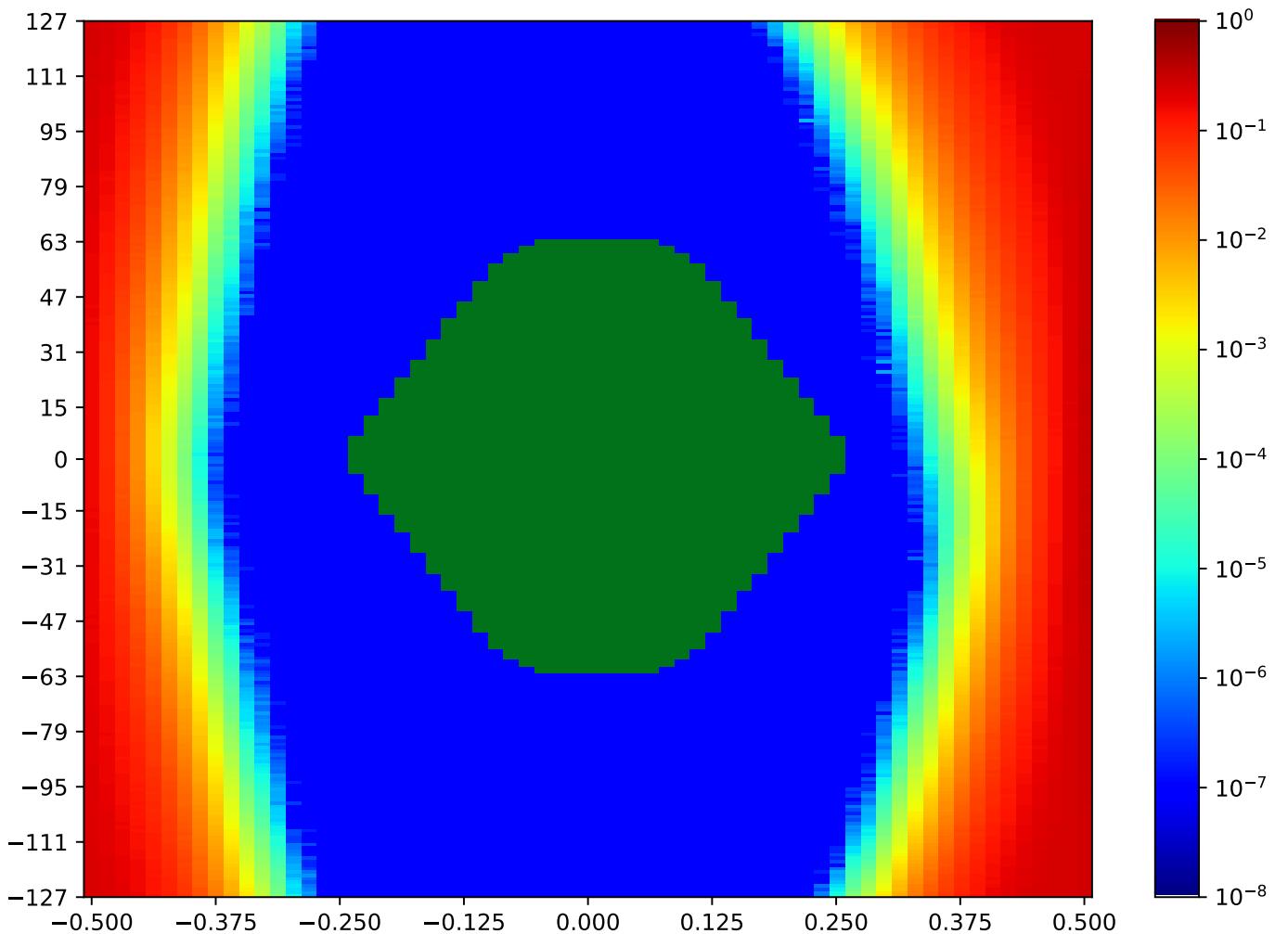


Figure 5.290: MSP_C_FPGA-TX4-10-RX4-10-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.

5.22.12 MSP_C_FPGA-TX4-11-RX4-11-MSP_A_FPGA

Table 5.269: MSP_C_FPGA-TX4-11-RX4-11-MSP_A_FPGA

SW Version	GT Type	Date and Time Started		Date and Time Ended	
2017.4	UltraScale+ GTY	2018-Sep-27 15:37:09		2018-Sep-27 15:37:29	
Reset RX	OA	HO		VO	VO (%)
true	9763	43		66.15%	255 100.00%
Dwell Type	Dwell BER	Horizontal Increment	Vertical Increment	Misc Info	
BER	1e-7	1	1	ELF Version: 0x0009 SVN: 16356	

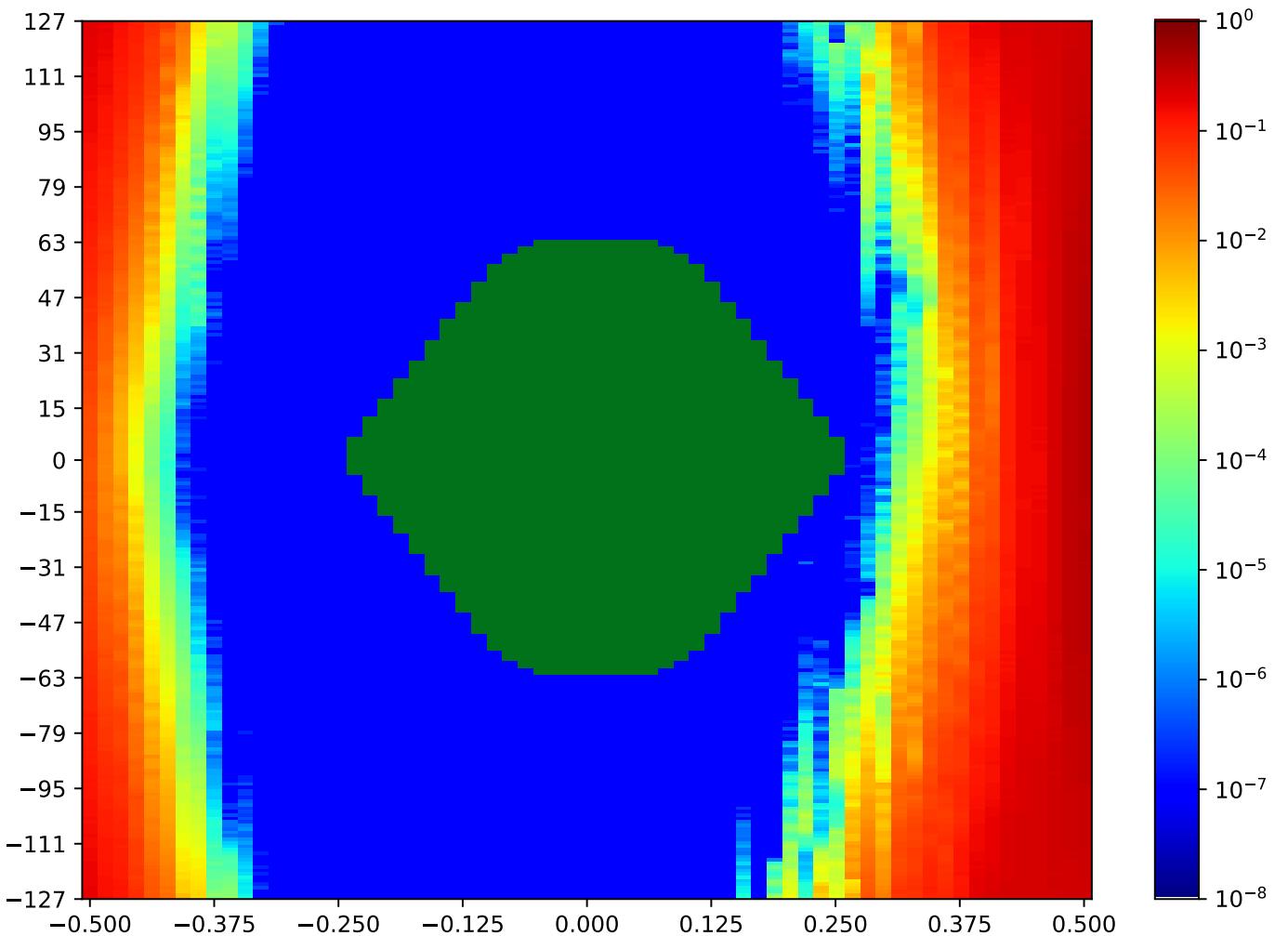


Figure 5.291: MSP_C_FPGA-TX4-11-RX4-11-MSP_A_FPGA

Call back to summary Figure 5.279. Sibling eye diagrams: V2-6.4.