Assignment 3

Due Date: 02/04/2021, 11:59 PM

Question 1: Consider following two scenarios of two silicon based P-N junction diodes, both diodes of identical area, at room temperature.

Diode 1: $N_D = 9 \times 10^{19}/cm^3$, $N_A = 1 \times 10^{15}/cm^3$

Diode 2: $N_D = 2 \times 10^{16}/cm^3$, $N_A = 5 \times 10^{17}/cm^3$

Calculate the ratio of Depletion Capacitance of Diode 1 to Depletion Capacitance of Diode 2 at zero bias (that is, when there is no external voltage applied across the diode). [10 Marks]

Question 2: With reference to IC Fabrication Technology, briefly explain following terms. [15 Marks]

(a) Positive Photoresist (b) Negative Photoresist (c) Ion Implantation (d) Mention three places where Multi-level Interconnects and/or Metallization are used (e) Anisotropic Etching

Question 3: Consider a MOS system with the following parameters.

Substrate Doping Concentration: $N_A = 3 \times 10^{16}\ cm^{-3}$

Poly-silicon Gate Doping Concentration: $N_D = 7 \times 10^{20}\ cm^{-3}$

Oxide Thickness: $T_{ox} = 250\ ^oA$

Oxide charge Density: $N_{ox} = 4 \times 10^{10}\ cm^{-2}$

(a) Calculate the threshold voltage at $V_{SB} = 0$.

(b) If you want to increase above calculated threshold voltage by 0.1 V using additional ion implantation, calculate how many additional atoms will be needed. Which type of dopant will you use?

[30 Marks]