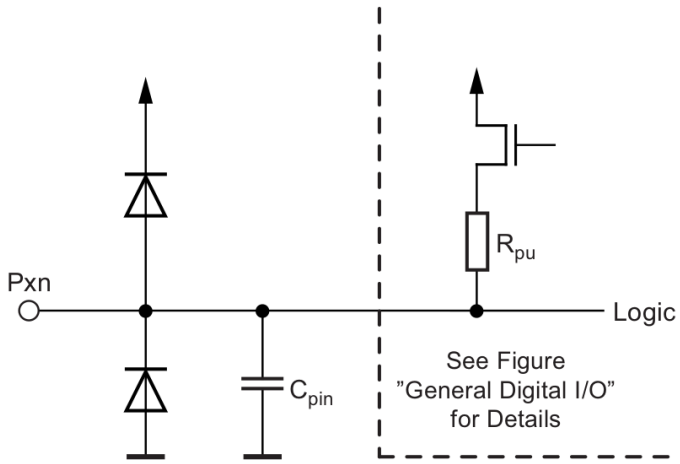
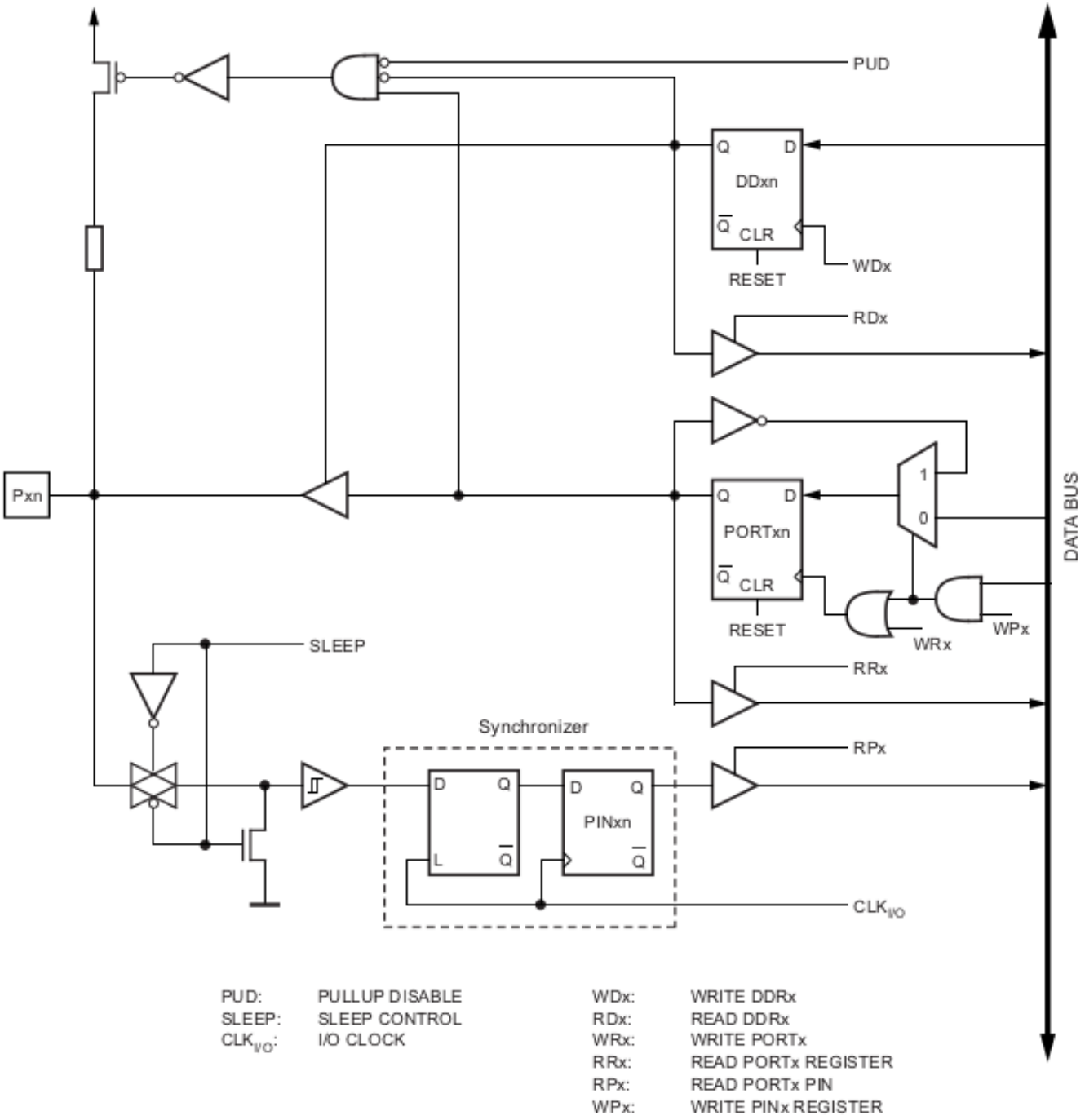
1 Introduction

- The directin/drive value/pull-up register of one port pin can be changed without changing the directin/drive value/pull-up register of any other pin - true *read-modify-write*.
- Each output buffer has symmetrical drive characteristics with both high sink and source capability.
- All I/Opins have protection diode to both V_{CC} and Ground.



- Three I/O memory address locations are allocated for each port, one each for the data register – **PORTx**, data direction register – **DDRx**, and the port input pins – **PINx**.
- Most pins are multiplexed with alternative functions.
- Generally, after reset, the port pins are tri-stated.
- Disbaling the ***PUD*** bit in **MCUCR** register disables the pull-up function of all pins.
- Unconnected pins should not float and must be connected to internal pull-up or external pull-up/pull-down registor.

2 General Digital I/O



2.1 DDR Registers

- It is used to select the direction of a pin.
- DDxn == 1 −− > Pin n of Port x is configured as output.
- DDxn == 0 −− > Pin n of Port x is configured as input.

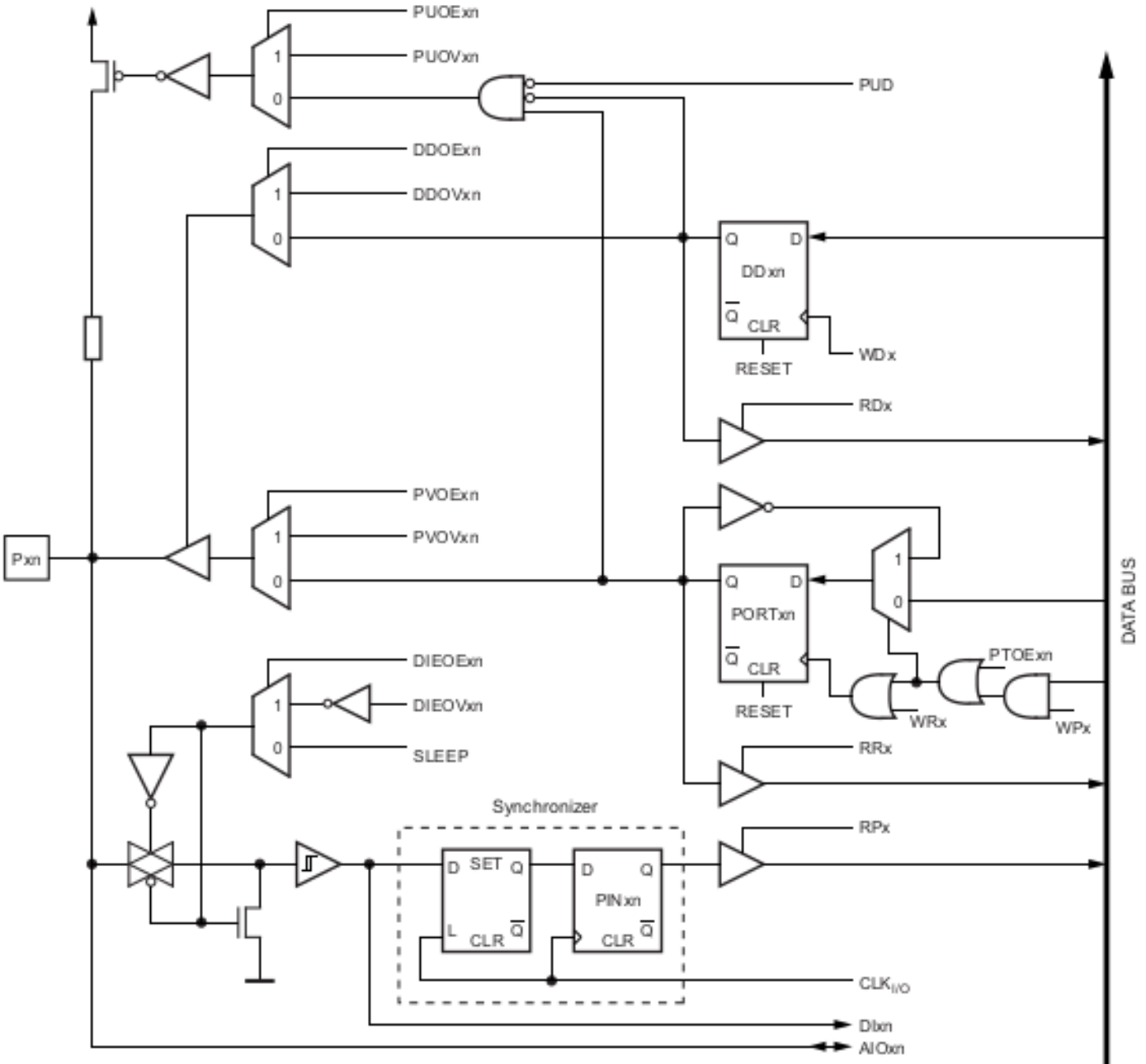
2.2 PORT registers

- If the pin is configured as Output - Drive the pin.
  - PORTxn == 1 −− > Pin n of Port x is driven to logic HIGH.
  - PORTxn == 0 −− > Pin n of Port x is driven to logic LOW.
- If the pin is configured as Input - configure pull-up resistor.
  - PORTxn == 1 −− > Pin n of Port x has pull-up resistor activaed.
  - PORTxn == 0 −− > Pin n of Port x has pull-up resistor deactivaed.

2.3 PIN Registers

- It is used to read the status of a pin.
- Writing 1 to a PINxn makes the Pin n of Port x toggle.

3 Alternate Port Functions



PUOExn:	Pxn PULL-UP OVERRIDE ENABLE	PUD:	PULL-UP DISABLE
PUOVxn:	Pxn PULL-UP OVERRIDE VALUE	WDx:	WRITE DDRx
DDOExn:	Pxn DATA DIRECTION OVERRIDE ENABLE	RDx:	READ DDRx
DDOVxn:	Pxn DATA DIRECTION OVERRIDE VALUE	RRx:	READ PORTx REGISTER
PVOExn:	Pxn PORT VALUE OVERRIDE ENABLE	WRx:	WRITE PORTx
PVOVxn:	Pxn PORT VALUE OVERRIDE VALUE	RPx:	READ PORTx PIN
DIEOExn:	Pxn DIGITAL INPUT ENABLE OVERRIDE ENABLE	WPx:	WRITE PINx
DIEOVxn:	Pxn DIGITAL INPUT ENABLE OVERRIDE VALUE	$CLK_{I/O}$	I/O CLOCK
SLEEP:	SLEEP CONTROL	DIxn:	DIGITAL INPUT PIN n ON PORTx
PTOExn:	Pxn, PORT TOGGLE OVERRIDE ENABLE	AIOxn:	ANALOG INPUT/OUTPUT PIN n ON PORTx

Signal Name	Full Name	Description
PUOE	Pull-up override enable	If this signal is set, the pull-up enable is controlled by the PUOV signal. If this signal is cleared, the pull-up is enabled when {DDxn, PORTxn, PUD} = 0b010.
PUOV	Pull-up override value	If PUOE is set, the pull-up is enabled/disabled when PUOV is set/cleared, regardless of the setting of the DDxn, PORTxn, and PUD register bits.
DDOE	Data direction override enable	If this signal is set, the output driver enable is controlled by the DDOV signal. If this signal is cleared, the output driver is enabled by the DDxn register bit.
DDOV	Data direction override value	If DDOE is set, the output driver is enabled/disabled when DDOV is set/cleared, regardless of the setting of the DDxn register bit.
PVOE	Port value override enable	If this signal is set and the output driver is enabled, the port value is controlled by the PVOV signal. If PVOE is cleared, and the output driver is enabled, the port value is controlled by the PORTxn register bit.
PVOV	Port value override value	If PVOE is set, the port value is set to PVOV, regardless of the setting of the PORTxn register bit.
PTOE	Port toggle override enable	If PTOE is set, the PORTxn register bit is inverted.
DIEOE	Digital input enable override enable	If this bit is set, the digital input enable is controlled by the DIEOV signal. If this signal is cleared, the digital input enable is determined by MCU state (normal mode, sleep mode).
DIEOV	Digital input enable override value	If DIEOE is set, the digital input is enabled/disabled when DIEOV is set/cleared, regardless of the MCU state (normal mode, sleep mode).
DI	Digital input	This is the digital input to alternate functions. In the figure, the signal is connected to the output of the schmitt trigger but before the synchronizer. Unless the digital input is used as a clock source, the module with the alternate function will use its own synchronizer.
AIO	Analog input/output	This is the analog input/output to/from alternate functions. The signal is connected directly to the pad, and can be used bi-directionally.