

ATmega328P Timer/Counter 1

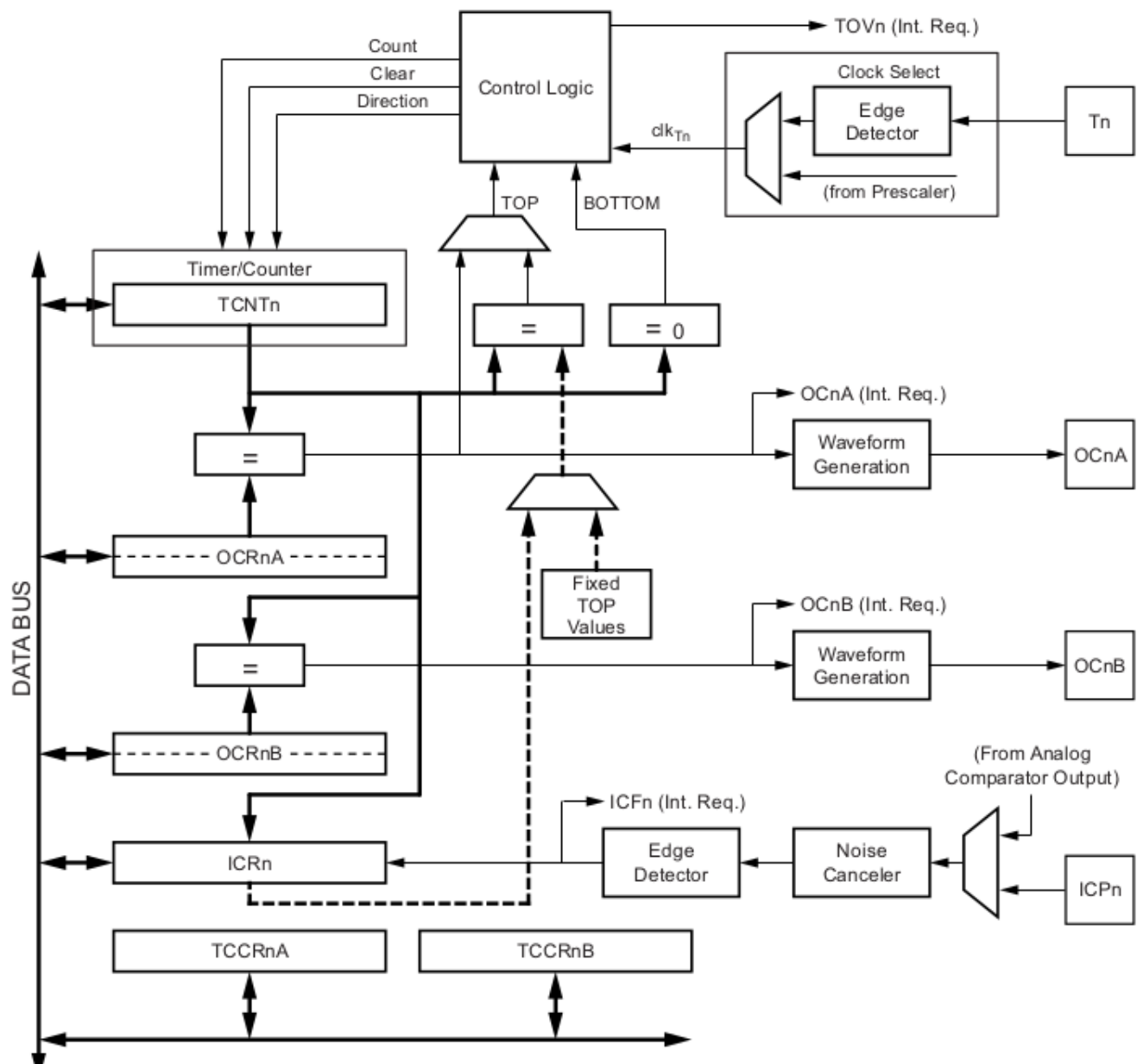
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1 Features

- General purpose 16-bit PWM/Counter module.
- Two independent output compare units and One input capture unit
- Variable PWM.
- Four independent interrupt sources (TOV1, OCF0A, OCF1B and ICF1).
- Clear timer on compare match (auto reload)

2 Block Diagram



3 Terminologies and Registers

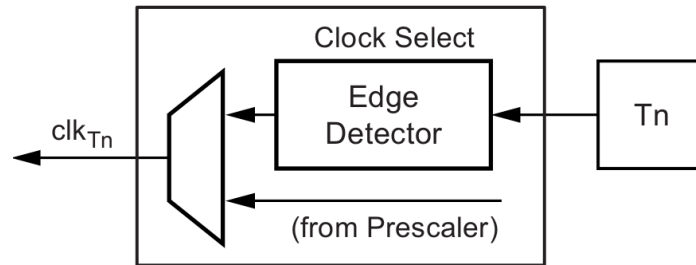
Parameter	Description	Register - 16 bit	Name
BOTTOM	counter reaches 0x0000	TCN10	Timer/Counter1 count value
MAX	counter reaches 0xFFFF	TCCR1A	Timer/Counter1 Control Register A
TOP	counter reaches highest value (depends on mode of operation can be 0xFF, 0x1FF, 0x3FF, OCR1A, ICR1)	TCCR1B	Timer/Counter1 Control Register B
		OCBR1A	Output compare register A
		OCBR1B	Output compare register B
		TIFR1	Timer Interrupt Flag Register
		TIMSK1	Timer interrupt Mask Register
		ICR1	Input Capture Register

Note:

- The **CNT1**, **OCR1A/B**, **ICR1** are 16-bit registers that can be accessed by the CPU via the 8-bit data bus.
- For 16-bit write, the high byte must be written before the low byte.
- For 16-bit read, the low byte must be read before the high byte.

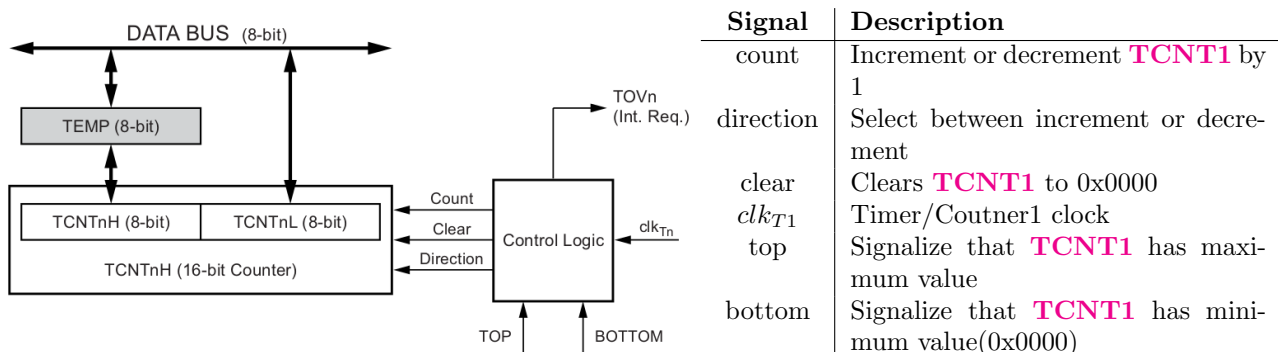
4 Timer/Counter1 Units

4.1 Clock Source/Select Unit



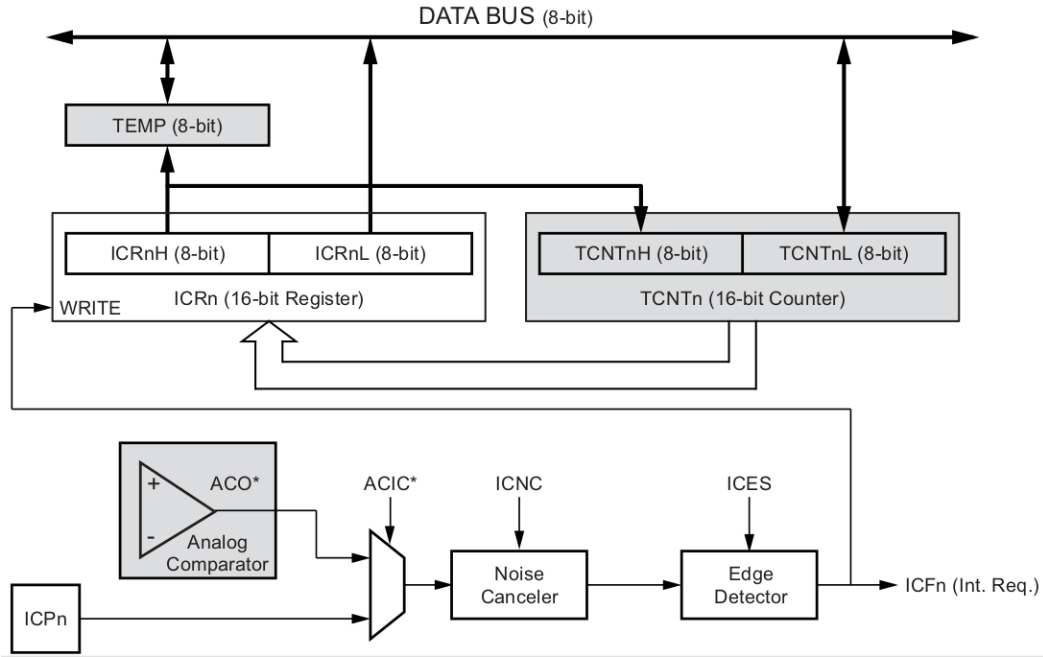
- The source for the Timer/Counter0 can be external or internal.
- External clock source is from **T1** pin.
- While Internal Clock source can be clocked via a prescaler.
- The output of this unit is the timer clock (clk_{T1}).
- It uses **CS1[2:0]** bits in **TCCR1B** register to select the source.

4.2 Counter Unit



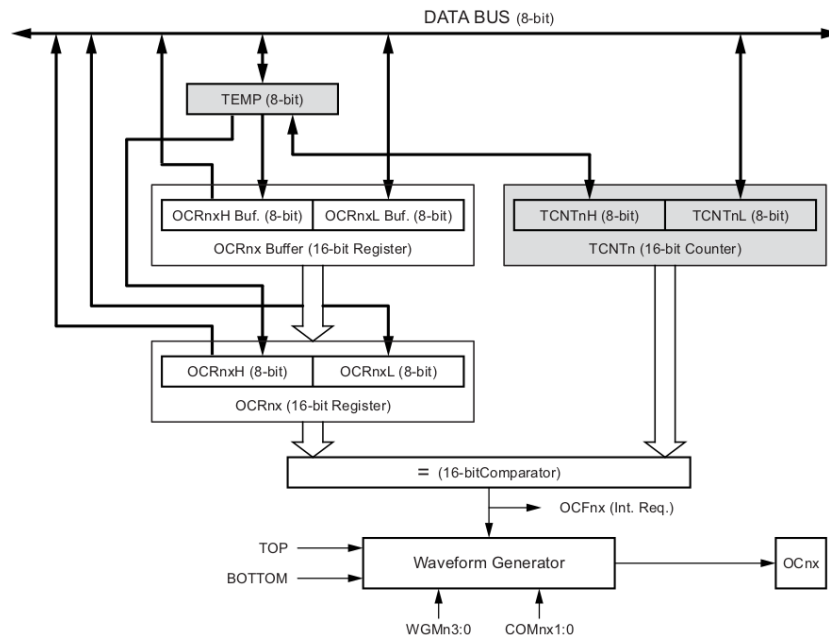
- The main part of the 16-bit Timer/Counter is the programmable bi-directional counter.
- Counter high (**TCNT1H**) containing the upper eight bits of the counter, and counter low (**TCNT1L**) containing the lower eight bits.
- Depending the mode of operation the counter is cleared, incremented, or decremented at each timer clock (clk_{T1}).
- Counting sequence is determined by **WGM1[3:0]** bits of **TCCR1A** -Timer/Counter1 Control register A and **TCCR1B** - Timer/Counter1 Control register B.
- The Timer/Counter1 Overflow flag (**TOV1**) is set and can generate interrupt according to the mode.

4.3 Input Capture Unit



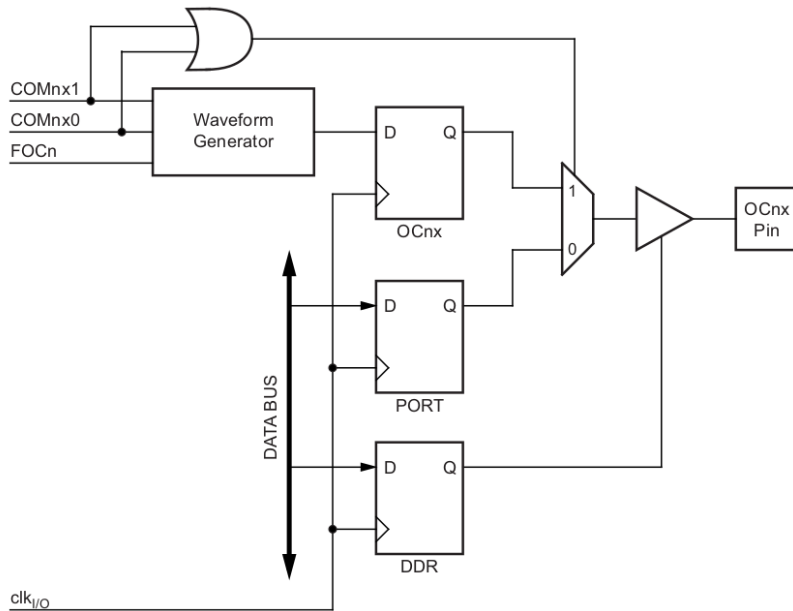
- Can capture external events and give them time-stamp indicating time of occurrence.
- External signal can be from **ICP1** pin or analog-comparator unit.
- Usage : calculate frequency, duty-cycle, log of the signal
- When a change of the logic level (an event) occurs on the input capture pin (**ICP1**), or on the analog comparator output (**ACO**), and this change confirms to the setting of the edge detector, a capture will be triggered.
- When a capture is triggered, the 16-bit value of the counter (**TCNT1**) is written to the input capture register (**ICR1**).
- The input capture flag (**ICF1**) is set at the same system clock as the **TCNT1** value is copied into **ICR1** register.
- If enabled (**ICIE1** = 1), the input capture flag generates an input capture interrupt.
- **ICF1** flag is automatically cleared when the interrupt is executed and by writing on to it.
- An input capture can be triggered by software by controlling the port of the **ICP1** pin.

4.4 Output Compare Unit



- 16-bit comparator continuously compares **TCNT1** with both **OCR1A** and **OCR1B**.
- When **TCNT1** equals **OCR1A** or **OCR1B**, the comparator signals a match which will set the output compare flag at the next timer clock cycle.
- If interrupts are enabled, then output compare interrupt is generated.
- The waveform generator uses the match signal to generate an output according to operating mode set by the **WGM1[3:0]** bits and compare output mode **COM0x[1:0]** bits.

4.5 Compare Match Output Unit



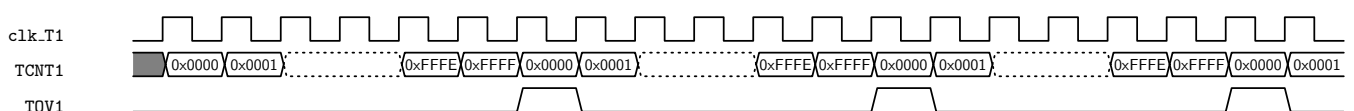
- This unit is used for changing the state of **OC1A** and **OC1B** pins by configuring the **COM1x[1:0]** bits.
- But, general I/O port function is overridden by DDR register.

5 Modes of Operation

- The mode of operation can be defined by combination of waveform generation mode (**WGM1[3:0]**) and compare output mode(**COM1[1:0]**) bits.
- The waveform generation mode (**WGM1[3:0]**) bits affect the counting sequence.
- For non-PWM mode, **COM1[1:0]** bits control if the output should be set, cleared or toggled at a compare match.
- For PWM mode, **COM1[1:0]** bits control if the PWM generated should be inverted or non-inverted.

5.1 Normal Mode - Non-PWM Mode

- **WGM1[3:0]** — > 000.
- Counter counts up and no counter clear.
- Overruns TOP(0xFFFF) and restarts from BOTTOM(0x0000).
- **TOV1** Flag is only set when overrun.
- We have to clear **TOV1** flag inorder to have next running.
- But, if we use interrupt we don't need to clear it as interrupt automatically clear the **TOV1** flag.
- The input capture unit can be used to capture events at **ICP1** pin or **ACO** pin.
- The timing can be seen below.



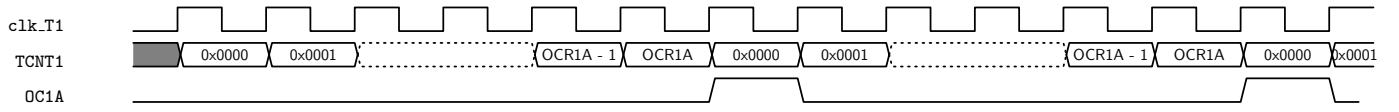
5.2 Clear Timer on Compare Match(CTC) Mode - Non-PWM Mode

- **WGM1[3:0]** -- > 0100 or 1100.
 - Counter value clears when **TCNT1** reaches **OCR1A** if **WGM1[3:0]** is 0100.
 - Counter value clears when **TCNT1** reaches **ICR1** if **WGM1[3:0]** is 1100.
- Interrupt can be generated each time **TCNT1** reaches **OCR1A** register value by **OCF1A** flag.
- Interrupt can be generated each time **TCNT1** reaches **ICR1** register value by **ICF1** flag.
- When **COM1A[1:0]** == 01, the **OC1A** pin output can be set to toggle its match between **TCNT1** and **OCR1A** or **ICR1** register to generate waveform.
- The frequency of the waveform its

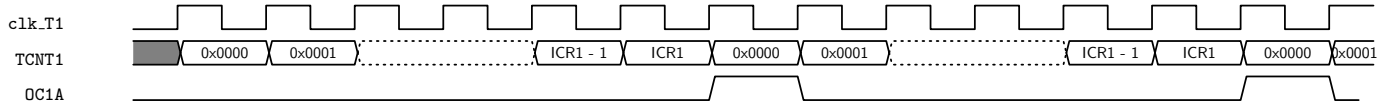
$$f_{OC1A} = \frac{f_{clkT1}}{2*N*(1+OCR1A)}$$

- Here N is prescalar factor and can be (1, 8, 64, 256, or 1024).

5.2.1 WGM1[3:0] == 0100



5.2.2 WGM1[3:0] == 1100

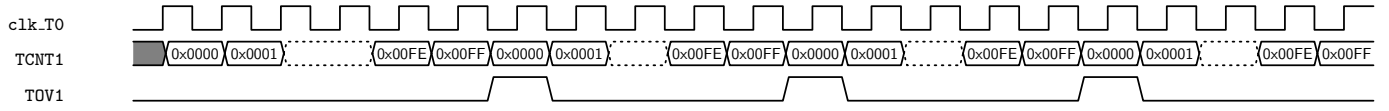


5.3 Fast PWM Mode

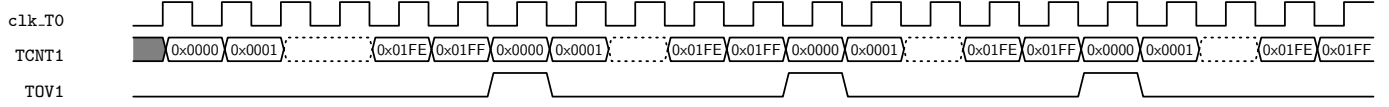
- **WGM1[3:0]** -- > 0101 or 0110 or 0111 or 1110 or 1111.
- Power Regulation, Rectification, DAC applications.
- Single slope operations causing high frequency PWM waveform.
- Counter starts from BOTTOM to TOP and then restarts from BOTTOM.
- TOP is defined by
 - TOP == 0x00FF if **WGM1[3:0]** -- > 0101
 - TOP == 0x01FF if **WGM1[3:0]** -- > 0110
 - TOP == 0x03FF if **WGM1[3:0]** -- > 0111
 - TOP == **ICR1** if **WGM1[3:0]** -- > 1110
 - TOP == **OCR1A** if **WGM1[3:0]** -- > 1111
- When **COM1A[1:0]** == 01, the **OC1A** pin output can be set to toggle its match between **TCNT1** and TOP to generate waveform.
 - The above is possible only when **WGM12** bit is set.
 - And only on **OC1A** pin and not on **OC1B** pin.
- In Inverting Compare Mode **COM1A[1:0]** == 10 , the **OC1A** or **OC1B** pins is made 1 on compare match between **TCNT1** and TOP and made 0 on reaching BOTTOM.
- In Non-Inverting Compare Mode **COM1A[1:0]** == 11 , the **OC1A** or **OC1B** pins is made 0 on compare match between **TCNT1** and TOP and 1 made on reaching BOTTOM.
- The Timer/Counter overflow flag (**TOV1**) is set each time the counter reaches TOP.
- The PWM frequency is given by

$$f_{OC1xPWM} = \frac{f_{clkT1}}{N*(1+TOP)}$$

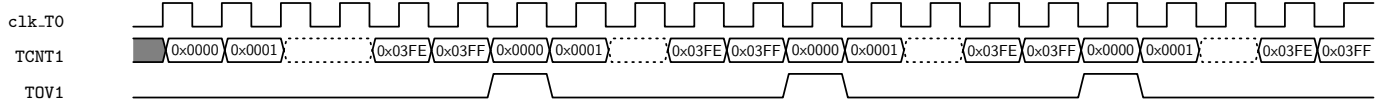
5.3.1 WGM1[3:0] == 0101



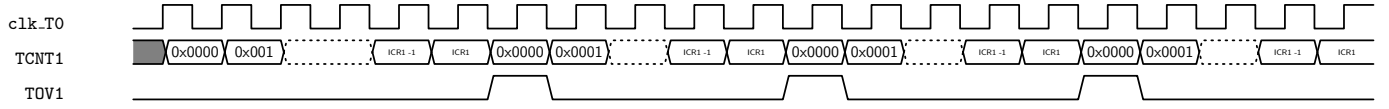
5.3.2 WGM1[3:0] == 0110



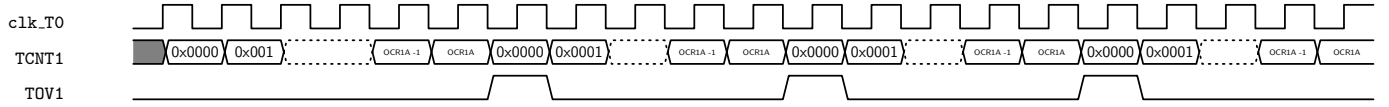
5.3.3 WGM1[3:0] == 0111



5.3.4 WGM1[3:0] == 1110



5.3.5 WGM1[3:0] == 1111

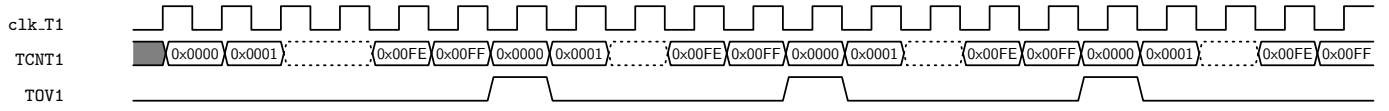


5.4 Phase Correct PWM Mode

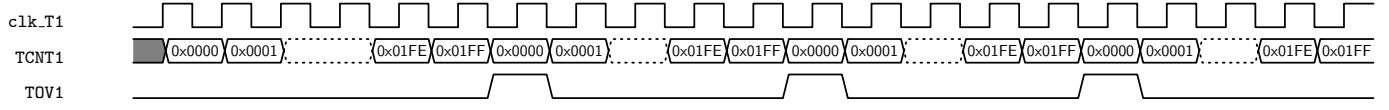
- **WGM1[3:0]** -- > 0001 or 0010 or 0011 or 1010 or 1011.
- High resolution phase correct PWM.
- Motor control due to symmetric features
- Dual slope operations causing lower frequency PWM waveform.
- Counter starts from BOTTOM to TOP and then from TOP to BOTTOM.
- TOP is defined by
 - TOP == 0x00FF if **WGM1[3:0]** -- > 0001
 - TOP == 0x01FF if **WGM1[3:0]** -- > 0010
 - TOP == 0x03FF if **WGM1[3:0]** -- > 0011
 - TOP == **ICR1** if **WGM1[3:0]** -- > 1010
 - TOP == **OCR1A** if **WGM1[3:0]** -- > 1011
- When **COM1A[1:0]** == 01, the **OC1A** pin output can be set to toggle its match between **TCNT1** and TOP to generate waveform.
 - The above is possible only when **WGM12** bit is set.
 - And only on **OC1A** pin and not on **OC1B** pin.
- In Inverting Compare Mode **COM1A[1:0]** == 10, the **OC1A** or **OC1B** pins is made 1 on compare match between **TCNT1** and TOP and made 0 on reaching BOTTOM.
- In Non-Inverting Compare Mode **COM1A[1:0]** == 11, the **OC1A** or **OC1B** pins is made 0 on compare match between **TCNT1** and TOP and 1 made on reaching BOTTOM.
- The Timer/Counter overflow flag (**TOV1**) is set each time the counter reaches BOTTOM..
- The PWM frequency is given by

$$f_{OC1xPWM} = \frac{f_{clkT1}}{2*N*TOP}$$

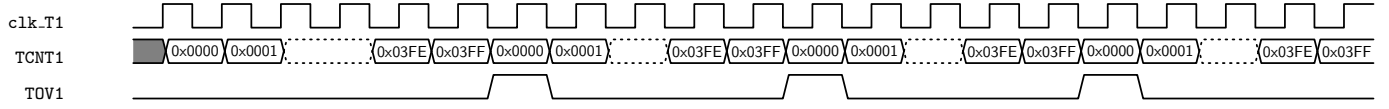
5.4.1 WGM1[3:0] == 0001



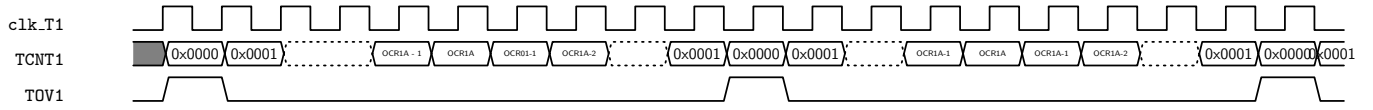
5.4.2 WGM1[3:0] == 0010



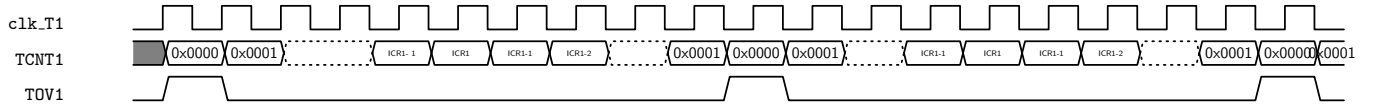
5.4.3 WGM1[3:0] == 0011



5.4.4 WGM[2:0] == 1010



5.4.5 WGM[2:0] == 1011



5.5 Phase and Frequency Corrected PWM Mode

- **WGM1[3:0]** == > 1000 or 1001.
- High resolution and Phase corrected PWM.
- Dual-Slope.
- Counter counts from BOTTOM to TOP and then from TOP to BOTTOM.
 - TOP == **OCR1A** if **WGM1[3:0]** == > 1001
 - TOP == **ICR1** if **WGM1[3:0]** == > 1000
- In Inverting Compare Mode **COM1x[1:0]** == 10 the **OC0x** pins is made 1 on compare match between **TCNT1** and TOP when upcounting and made 0 on compare match between **TCNT1** and TOP when downcounting.
- In Non-Inverting Compare Mode **COM1x[1:0]** == 11, the **OC0x** pins is made 0 on compare match between **TCNT1** and TOP when upcounting AND made 1 on compare match between **TCNT1** and TOP when downcounting.
- The Timer/Counter overflow flag (**TOV1**) is set each time the counter reaches BOTTOM.
- The interrupt flag can be used to generate an interrupt each time the counter reaches the BOTTOM value.
- The PWM frequency is given by

$$f_{OC1xPWM} = \frac{f_{clkT1}}{2*N*TOP}$$

6 Register Description

TCCR1A – Timer/Counter 1 Control Register A

7	6	5	4	3	2	1	0
COM1A1	COM1A0	COM1B1	COM1B0	-	-	WGM11	WGM10

<i>COM1x[1:0]</i>	Non-PWM modes	Fast PWM	Phase Corrected PWM & Phase and Frequency Corrected PWM
00	No output @ <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> pin	No output @ <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> pin	No output @ <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> pin
01	Toggle No output @ <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> pin on compare Match.	When <i>WGM[3:0]</i> == 1110 or 1111, Toggle <i>OC1A</i> pin on compare match	When <i>WGM[3:0]</i> == 1110 or 1111, Toggle <i>OC1A</i> pin on compare match.
10	Clear <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> pin on compare Match.	Clear <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> on compare match and set <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> at BOTTOM	Clear <i>PD5 - OC0B</i> on compare match when up-counting and set <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> on compare match when down-counting.
11	Set <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> pin on compare Match.	Set <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> on compare match and clear <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> at BOTTOM	Set <i>PD5 - OC0B</i> on compare match when up-counting and clear <i>PB1 - OC1A</i> or <i>PB2 - OC1B</i> on compare match when down-counting.