50.002 COMPUTATION STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

Problem Set 5

1 Warm Up – Flip Flops

Consider the following diagram of a simple sequential circuit:

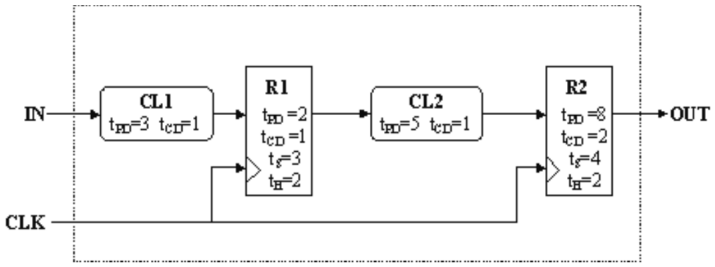


Figure 1

The components labeled CL1 and CL2 are combinational; R1 and R2 are edge triggered flip flops. Timing parameters for each component are as noted. Answer both questions below:

1. Write the timing specifications (tS, tH, tCD, tPD, tCLK) for the system as a whole using the timing specifications for the internal components that are given in the figure.

   Solution:
   t_H and t_S is for IN, t_{CD} and t_{PD} is for CLK. Below are the proposed values:

$$t_S = t_{S.R1} + t_{PD.CL1} = 3 + 3 = 6 \quad (1)$$
$$t_H = t_{H.R1} - t_{CD.CL1} = 2 - 1 = 1 \quad (2)$$
$$t_{CD} = t_{CD.R2} = 2 \quad (3)$$
$$t_{PD} = t_{PD.R2} = 8 \quad (4)$$
$$t_{CLK} \geq t_{PD.R1} + t_{PD.CL2} + t_{S.R2} = 2 + 5 + 4 = 11 \quad (5)$$

2. Suppose you had available a faster version of CL2 having a propagation delay of 3 and a contamination delay of zero. Could you substitute the faster CL2 for the one shown in the diagram? Explain.

   Solution:
   No we can't. The contamination delay for R1 is 1, while the contamination delay for CL2 is 0. After CLK change, R2 input holds for 1s, but t_H required is 2s.

2 Warm Up – Analyzing Timing Plot

Consider the following unusual D-latch configuration:

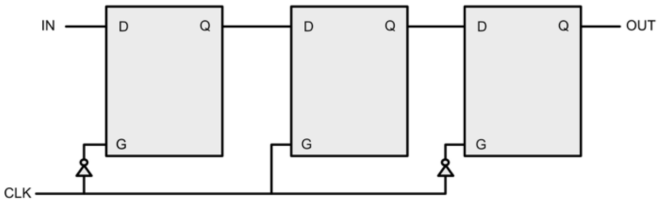


Figure 2

Now we feed it the following input signal and CLK signal. Which of the following signal plots represent the output of this device made out of 3 D-latches? Assume that the jagged edges means unknown value and that the contents of each latch in the beginning is unknown.

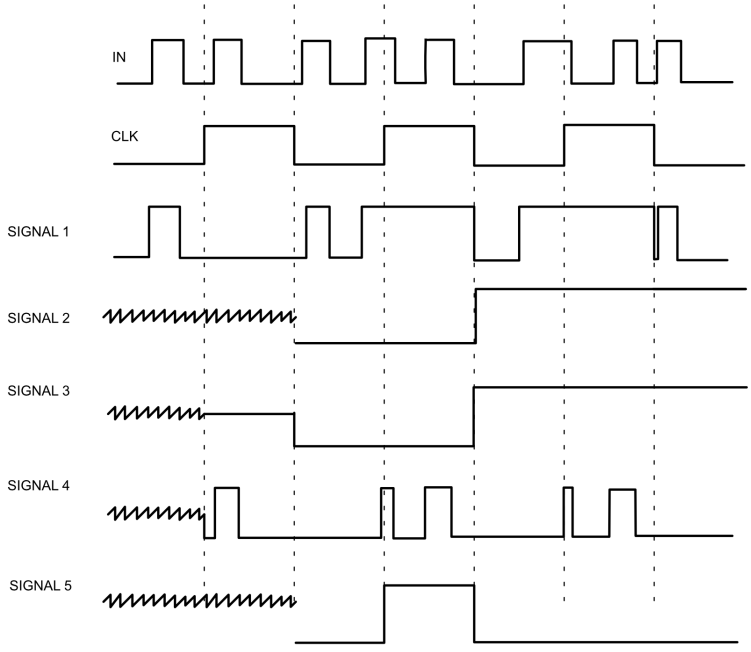


Figure 3

Solution:
SIGNAL 2 is the output of the device since there's two *unknown* outputs (it takes two half-clock cycles for the input to be propagated to the output). Signal 5, although it has "invalid" values for two clock cycles isn't the answer because since it is an odd-numbered DFFs, it only **changes output** at **falling** edge, as opposed to rising edge in a normal Register with two DFFs.

3 Warm Up – Simple Timing Computation

Consider the following circuit, and **notice the feedback loop**:

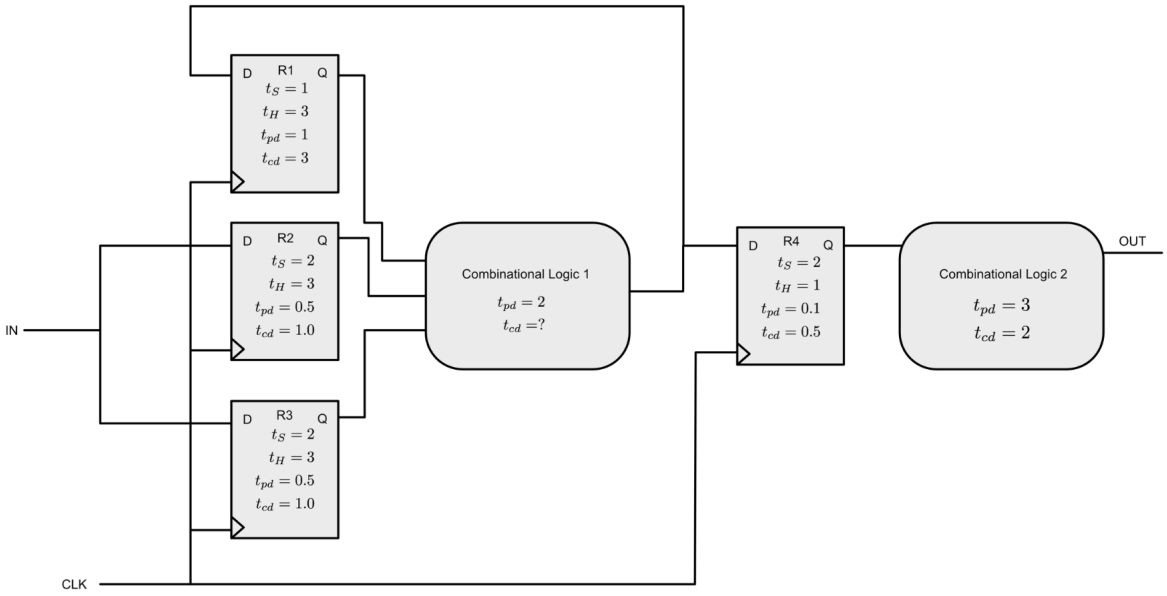


Figure 4

Setup time, hold time, propagation delay, and contamination delay (all in nanoseconds) of each component is as written above. Lets now analyse its timing constraints:

(a) What is the minimum contamination delay (tcd) of Combinational Logic 1 such that the sequential circuit may still function properly?
Solution:
The combinational logic unit 1 (CL1) is responsible for the hold times of R4 and R1. Since R1's tHold is larger than R4, we should consider that to compute min tcd for CL1. The thold of R1 can be satisfied using the tcd of CL1 plus the min tcd of either R1, R2, or R3. Hence, minimum acceptable tcd of CL1 is thold R1 - tcd R2 = 3 - 1 = 2ns.

(b) Write down the minimum CLK period for the sequential circuit to function properly.
Solution:
The clock period must be big enough for signals to propagate from the upstream registers on the left to any downstream registers R1 or R4. The longest path is formed by the tpd of R1 + tpd CL1 + tSetup R4 = 1 + 2 + 2 = 5ns.

(c) Write down the minimum hold time (tH) for the IN signal to the system.
Solution:
The input must satisfy the thold of both R2 and R3, which is 3ns.

(d) Write down the minimum propagation time of the sequential logic circuit.
Solution:
The propagation time of the circuit is counted from R4 onwards since it is the last register in the circuit, hence it tpd R4 + tpd CL2 = 3.1ns.

4 Metastable State Analysis

Consider the following D-latch device and its VTC plot:

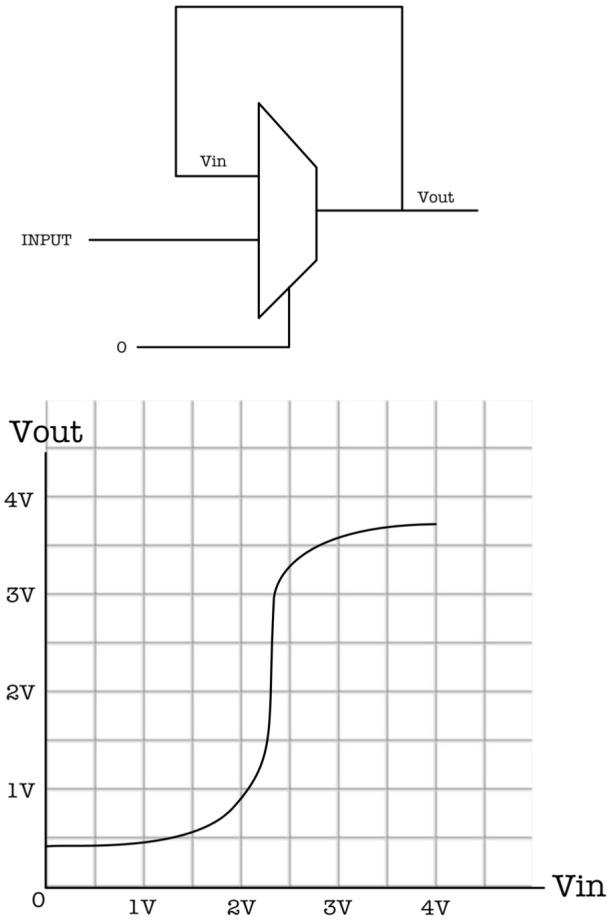


Figure 5

We are given the following specification about the multiplexer's valid operating voltage ranges: $V_{IL} = 1V, V_{OL} = 0.5V, V_{IH} = 3V, VOH = 3.5V$. The noise margin is $0.5V$ and we can assume that the device obeys the **static discipline**.

(a) Which voltage value approximately, has the highest probability for the device to be in the metastable state?
Solution:
We plot the line Vout == Vin and find the intersection with the VTC curve to be approximately at 2.35V. This is the Vin value that has the highest probability for the device to stay in metastable state.

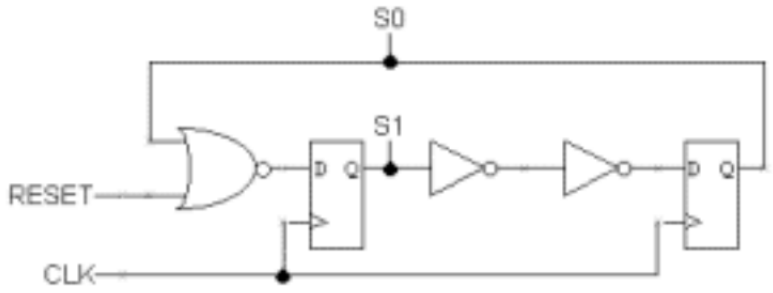
(b) Compare $V_{IN} = 0.9V$ vs $V_{IN} = 3V$. Which input voltage will most likely cause the device stay in the metastable state?

Solution:
Both input voltage values are **valid** inputs. Therefore the device will **always produce valid output voltages** since it obeys the static discipline. We can say that both values are equally unlikely to stay in the metastable state.

(c) Compare $V_{IN} = 2.1V$ vs $V_{IN} = 2.5V$. Which input voltage will most likely cause the device stay in the metastable state?
Solution:
Both input voltage values are *invalid* inputs. From the graph, we can deduce that $V_{IN} = 2.1V$ results in $V_{OUT} = 1V$, while $V_{IN} = 2.5V$ results in $V_{OUT} = 3.3V$. Taking $2.35V$ as the most likely voltage value for the device to stay in the metastable state, 3.3V is nearer to 2.35V as opposed to 1V. Hence, we can deduce that $V_{IN} = 2.5V$ is more likely to cause the device to stay in the metastable state.

5 Another Combinational Circuit

The following circuit diagram implements a sequential circuit with two state bits, S0 and S1:



inverter: t_{CD}=1ns, t_{PD}=2ns
nor2: t_{CD}=1.5ns, t_{PD}=2ns
D register: t_{CD}=0ns, t_{PD}=2ns, t_H=1ns, t_S=3ns

Figure 6

Answer the following questions:

1. What is the smallest clock period for which the circuit still operates correctly?
   Solution:
   There are two contraints to check:

$$t_{PD.REG} + t_{PD.INV} + t_{PD.INV} + t_{S.REG} \leq t_{CLK} \quad (6)$$

$$t_{PD.REG} + t_{PD.NOR2} + t_{S.REG} \leq t_{CLK} \quad (7)$$

   The first constraint requires $t_{CLK} \geq$ 9ns.

2. A sharp-eyed student suggests optimizing the circuit by removing the pair of inverters and connecting the Q output of the left register directly to the D input of the right register. If the clock period could be adjusted appropriately, would the optimized circuit operate correctly? If yes, explain the adjustment to the clock period that would be needed

   Solution:
   No, the circuit won't operate correctly since $t_{CD.REG} < t_{HOLD.REG}$, i.e., the output of the left register doesn't meet the required hold time when connected directly to the input of the right register.

3. When the RESET signal is set to "1" for several cycles, what values are S0 and S1 set to?
   Solution:
   S0 = 0, S1 = 0.

4. Assuming the RESET signal has been set to ”0” and will stay that way, what is the state following S0=1 and S1=1?
   Solution:
   S0 = 1, S1 = 0.

6 Advanced Timing Computation

Take a look at the following State Machine circuitry:

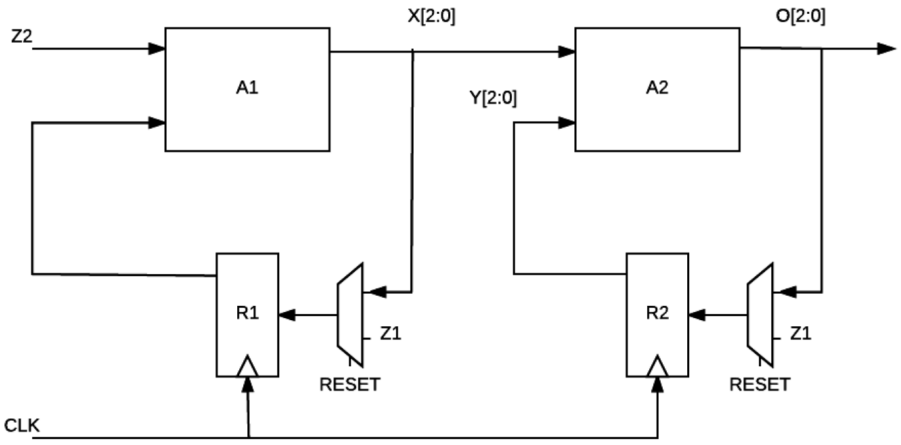


Figure 7

The device A2 has the following schematic:

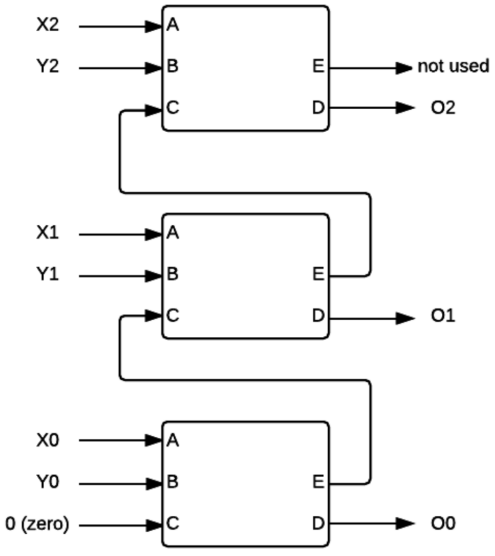


Figure 8

Basically, it is made out of this device we call A000R with **tcd = 1ns, and tpd = 3ns** with the followings chematic

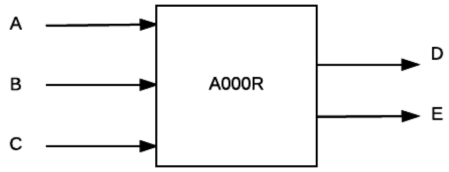


Figure 9

The truth table for A000R is as follows:

A	B	C	D	E
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1

The timing specifications for other devices in the state machine is:

- The Mux has the following time specification: **tcd = 1ns, and tpd = 2ns.**
- The Registers has the following time specification: **tcd = 2ns, tpd = 5ns, ts = 2ns, th = 2ns.**

Both A1 and A2 are combinational logic that contains A000R only. Unfortunately, the design for A1 is missing. We only know that A1 uses only A000R to compute the output and the next state function **and that A1 has the same tpd as A2**. The other information that we have is that the output of A1, X[2:0], is a sequence of decimal, [1, 2, 3, ...] in the binary form, i.e. [001, 010, 011, ...].

Answer the following questions:

(a) What is the number of bits that the constant Z1 should have?
Solution:
Since one of the inputs to the muxes are 3-bits, this hardware is implemented using three 2-input mux. Z1 is essentially **three bits**, connected to each of the three copies of 2-input muxes.

(b) What is the minimum number of bits that the constant Z2 should have?
Solution:
1 bit. The number of bits of each input to a combinational logic device such as A1 are independent / does not depend on other inputs.

(c) What is the decimal value of Z1?
Solution:
Since X[2:0] produces an increasing sequence from decimal value of 1,2,3,4, etc, we can easily guess that the the decimal value of Z1 should be 0, such that when there's a RESET, the output of the register R1 is zero.

(d) What is the decimal value of Z2?
Solution:
Z2 is 1. Same reason applies: since the sequence X[2:0] produced by A1 is increasing by 1, the input to A1 should be 1 such that at every cycle, theres an addition of 1 to be produced at X.

(e) What is the tpd of A2 in nanosecond?
Solution:

The tpd of A000R is 3ns, hence the tpd of A2 is 9ns since it is made out of three A000R in series.

(f) What is the minimum clock period in nanosecond?
Solution:
The *longest* path that the CLK has to satisfy is R1 - A1 - A2 - Z1 - R2. Hence we need to consider the tpd of all devices in its path (except R2) plus the tsetup of R2: $5 + 9 + 9 + 2 + 2 = 27$ns.

(g) What is the minimum Tcd of A1 in nanosecond?
Solution:
The tcd of A1 has to be big enough so as to satisfy the thold of R1. Thold requirement of R1 is 2 ns, and the tcd of the mux is 1 ns. Therefore min tcd of A1 is $2 - 1 = 1$ns.

(h) What is the Tcd of A2 in nanosecond?
Solution:
The tcd of A2 is basically the tcd of a single A000R (1ns) since thats the shortest path from input to output.

(i) When RESET is 1 for several cycles, what is the value of X[2:0]?
Solution:
When RESET is HIGH, the output of R1 will be 0b000. Hence the value of X[2:0] is 0b001.

(j) When outputing the X sequence [1, 2, 3, ...], what is the value of RESET?
Solution:

RESET is LOW (0) to enable the addition of the *previous* value of X to form the new value of X in the next CLK cycle.

(k) Suppose that at time t = 0, RESET signal is changed from 1 to 0, and X becomes 0b001. From then on, RESET remains 0.

(a) What is the decimal value of O[2:0] at time $t = 0$?
Solution:
X is 0b001 and Y is 0b000 at $t = 0$. Using the truth table of A000R and the schematic of A1, we can deduce that O[2:0] at $t = 0$ is 1.

(b) What is the decimal value of O[2:0] at time $t = 1$?
Solution:
X is 0b010 and Y is 0b001 at $t = 1$. Using the truth table of A000R and the schematic of A1, we can deduce that O[2:0] at $t = 1$ is 3.

(c) What is the decimal value of O[2:0] at time $t = 3$?
Solution:
X is 0b011 and Y is 0b011 at $t = 1$. Using the truth table of A000R and the schematic of A1, we can deduce that O[2:0] at $t = 2$ is 2.

7 Hardware Implementation of another state machine

Consider the schematic of a machine before that is able to **Detects a sequence of three or more consecutive 1's, and output: 1 after three or more consecutive 1's, or 0 otherwise.**

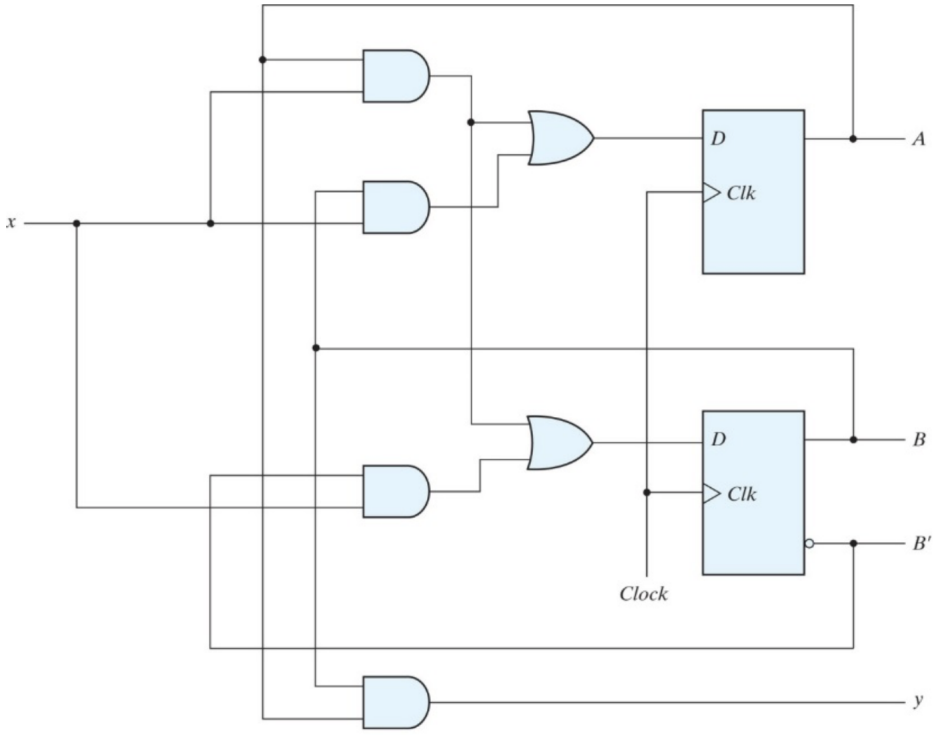


Figure 10

Lets analyse the circuit by answering the questions below:

(a) If the circuit has an initial state of AB=00, and the input at t=0 is x=0, what is the next state?
Solution:
AB = 00

(b) If the initial state is AB=00 and the input at t=0 is x=1, what is the next state?
Solution:
AB = 01

(c) If the current state is AB=01, and the input is x=1, what is the next state?
Solution:
AB = 10

(d) If the current state is AB=10, and the input is x=1, what is the next state?
Solution:
AB = 11

(e) If the current state is AB=11, and the input is x=1, what is the next state?
Solution:
AB = 11

(f) If the current state is AB=11, and the input is x=0, what is the next state?
Solution:
AB = 00

(g) What are the state(s) that can go to state AB=00 as its next state?
Solution:
All combinations, i.e: AB=00, or 01, or 10, or 11.

(h) What is the output y when the current state is AB = 11 and the current input is x = 0?
Solution:
y=1

(i) The propagation delays for all the combinational logic gates and the flip-flops are 2 ns. The clock frequency is 100 MHz. **What is the worst case delay** in nanosecond for the next states at A and B to appear (i.e. for A and B to be valid) after the input x is changed to be a valid input. **Assume that the initial states of both dff are given**.
Solution:
From the frequency, we can compute the period of the clock to be 10ns. For the worst case delay, we need to consider the scenario that input x is propagated up to input of the register and *just missed the CLK rise*. It takes 4 ns to propagate through the AND and OR gates, and another 10 ns to wait for another CLK rise. Finally, it takes 2 ns to propagate through the register to produce A or B. Hence the worst case delay is $4+10+2=16$ns.

(j) The propagation delays for all the combinational logic gates and the flip-flops are 2 ns. The dffs have thold and tsetup of 1ns each. If the clock frequency is not given, *what is the maximum clock frequency* that we can have for this device?
Solution:
The CLK period has to satisfy the feedback path, that is the tpd of the dff, the tpd of AND gate, the tpd of OR gate, and the tsetup of the register. This adds up to $2+2+2+1=9$ns. Hence the maximum frequency is $1/(9*10^{-9}) = 111111111.11Hz = 111.11Mhz$.

(k) What is the next output sequence from $t=1$ to $t=16$ of the circuit with the following input (fed from left to right): 1101 1111 1110 0010 at $t=0$ to $t=15$ (assuming the initial states of both flip flops are 0)?
Solution:
We would have to trace this one by one, or deduce from the *functionality* of the device given, that is to detect three consecutive 1's and output 0 afterwards. Given that the initial flip-flop state is 0, that makes $B'=1$. The output sequence is 0000 0010 0000 0000 from $t=1$ to $t=16$.