50.002 COMPUTATIONAL STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

Problem Set 2

1 VTC Plot

The behavior of a 1-input 1-output device is measured by hooking a voltage source to its input and measuring the voltage at the output for several different input voltages, resulting in the following VTC plot,

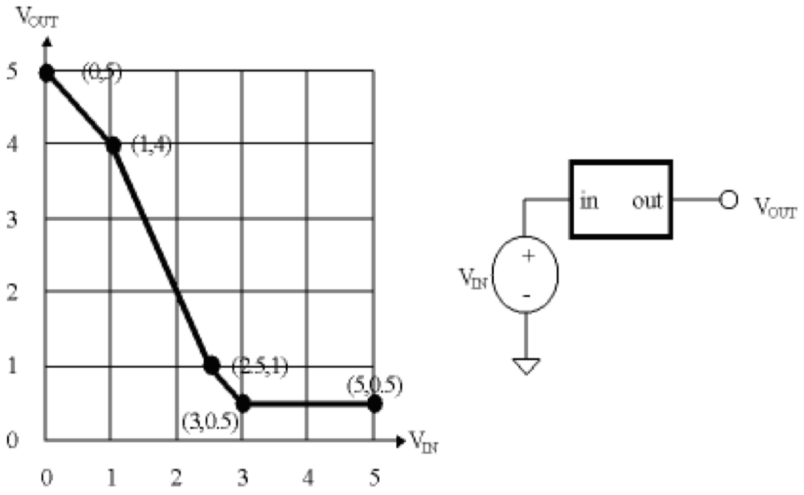

Figure 1

We're interested in whether this device can serve as a legal combinational device that obeys the **static discipline**. For this device, obeying the static discipline means that,

$$\text{If } V_{IN} \leq V_{IL} \text{ then } V_{OUT} \geq V_{OH}\text{, and if } V_{IN} \geq V_{IH} \text{ then } V_{OUT} \leq V_{OL} \quad (1)$$

When answering the questions below, assume that all voltages are constrained to be in the range of 0V to 5V,

1. Can one choose a V_{OL} of 0V for this device? Explain.

2. What's the smallest V_{OL} one can choose and still the device obey the static discipline?

3. Assuming that we want to have 0.5V noise margins for both "0" and "1" values, what are the appropriate voltage levels for V_{OL}, V_{IL}, V_{IH}, and V_{OH} so that the device obeys the static discipline? *Hint: there are many choices. Just choose the one that obeys the static discipline and the NM constraint*.

4. What device is this called?

2 Inverter Madness

1. The following graph plots the VTC for a device with one input and one output. Can this device be used as a combinational device in logic family with 0.75 noise margins?

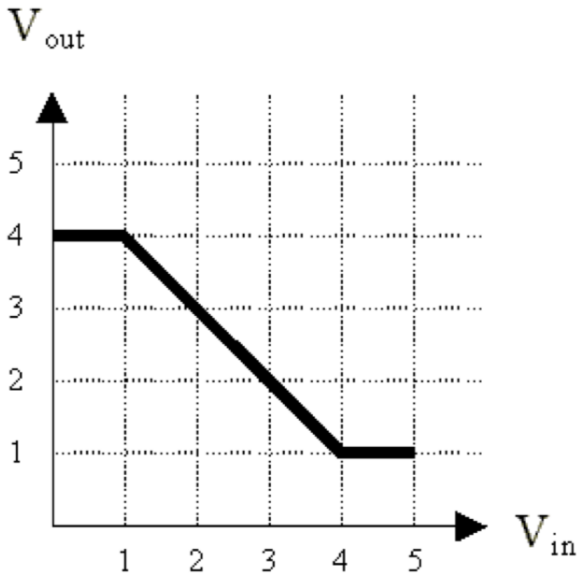

Figure 2

2. You are designing a new logic family and trying to decide on values of the four parameters: V_{OL}, V_{IL}, V_{IH}, and V_{OH} that lead to non-zero noise margins for various possible inverter designs. Four proposed inverter designs exhibit the VTC shown in the diagrams below. For each design, either specify four suitable values of V_{OL}, V_{IL}, V_{IH}, and V_{OH} or explain why no values can obey the static discipline.
   Hint: you may want to start by choosing NM to be 0.5V for ease of calculation.

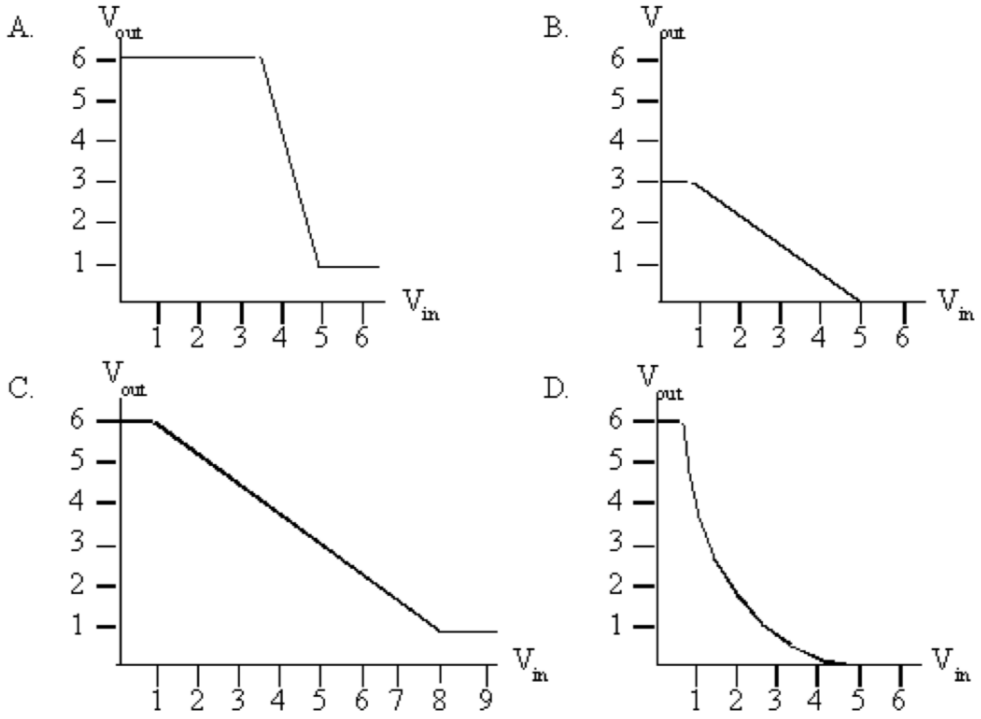

Figure 3

3 Static Discipline

1. Consider a combinational *buffer* with one input and one output. Suppose we set its input to some voltage V_{IN}, wait for the device to reach a steady state, then measure the voltage on its output V_{OUT} and find out $V_{OUT} < V_{OL}$. What can we say about V_{IN}?

2. Now consider an inverter. Suppose we set its input to some voltage V_{IN}, wait for the device to reach a steady state, then measure the voltage on its output V_{OUT}, and find $V_{OUT} > V_{OH}$. What can we say about V_{IN}?

4 VTC Analysis

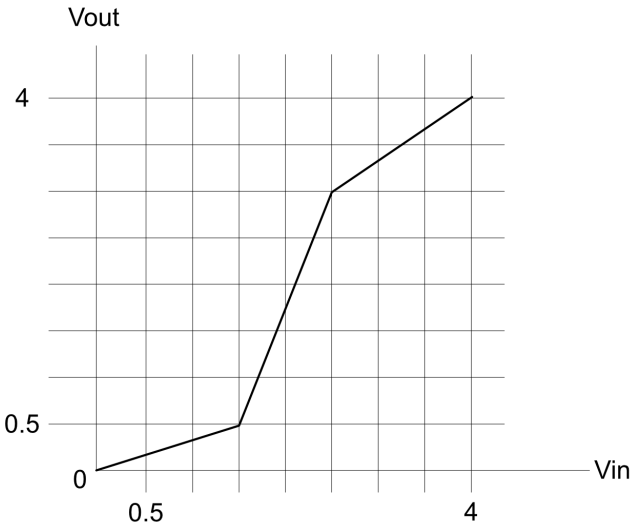

Figure 4: VTC Plot

Which of the following specification(s) does not obey the static discipline? Select all that apply.

1. $V_{IL} = 0.4V, V_{IH} = 3.1V, V_{OL} = 0.2V, V_{OH} = 4.2V$
2. $V_{IL} = 0.5V, V_{IH} = 3V, V_{OL} = 0.3V, V_{OH} = 4V$
3. $V_{IL} = 0.2V, V_{IH} = 3V, V_{OL} = 0.4V, V_{OH} = 4.2V$
4. $V_{IL} = 0.5V, V_{IH} = 4V, V_{OL} = 0V, V_{OH} = 3.5V$
5. $V_{IL} = 0.5V, V_{IH} = 3.5V, V_{OL} = 0V, V_{OH} = 4V$