50.002 COMPUTATION STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

Problem Set 5

1 Flip Flops

Consider the following diagram of a simple sequential circuit:

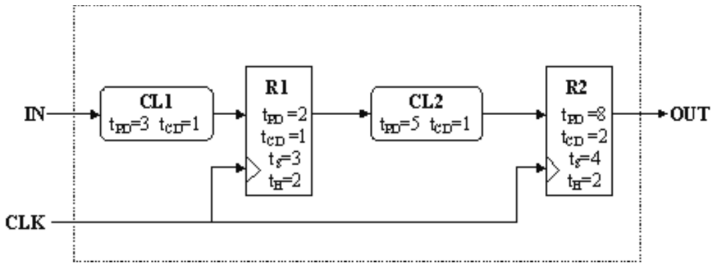

Figure 1

The components labeled CL1 and CL2 are combinational; R1 and R2 are edge triggered flip flops. Timing parameters for each component are as noted. Answer both questions below:

1. Write the timing specifications (tS, tH, tCD, tPD, tCLK) for the system as a whole using the timing specifications for the internal components that are given in the figure.

   Solution:
   t_H and t_S is for IN, t_{CD} and t_{PD} is for CLK. Below are the proposed values:

$$t_S = t_{S.R1} + t_{PD.CL1} = 3 + 3 = 6 \tag{1}$$
$$t_H = t_{H.R1} - t_{CD.CL1} = 2 - 1 = 1 \tag{2}$$
$$t_{CD} = t_{CD.R2} = 2 \tag{3}$$
$$t_{PD} = t_{PD.R2} = 8 \tag{4}$$
$$t_{CLK} \geq t_{PD.R1} + t_{PD.CL2} + t_{S.R2} = 2 + 5 + 4 = 11 \tag{5}$$

2. Suppose you had available a faster version of CL2 having a propagation delay of 3 and a contamination delay of zero. Could you substitute the faster CL2 for the one shown in the diagram? Explain.

   Solution:
   No we can't. The contamination delay for R1 is 1, while the contamination delay for CL2 is 0. After CLK change, R2 input holds for 1s, but t_H required is 2s.

2 Another Combinational Circuit

The following circuit diagram implements a sequential circuit with two state bits, S0 and S1:

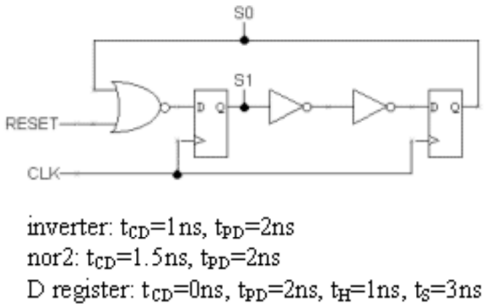

Figure 2

Answer the following questions:

1. What is the smallest clock period for which the circuit still operates correctly?
   Solution:
   There are two contraints to check:

$$t_{PD.REG} + t_{PD.INV} + t_{PD.INV} + t_{S.REG} \leq t_{CLK} \quad (6)$$

$$t_{PD.REG} + t_{PD.NOR2} + t_{S.REG} \leq t_{CLK} \quad (7)$$

   The first constraint requires $t_{CLK} \geq$ 9ns.

2. A sharp-eyed student suggests optimizing the circuit by removing the pair of inverters and connecting the Q output of the left register directly to the D input of the right register. If the clock period could be adjusted appropriately, would the optimized circuit operate correctly? If yes, explain the adjustment to the clock period that would be needed

   Solution:
   No, the circuit won't operate correctly since $t_{CD.REG} < t_{HOLD.REG}$, i.e., the output of the left register doesn't meet the required hold time when connected directly to the input of the right register.

3. When the RESET signal is set to ”1” for several cycles, what values are S0 and S1 set to?
   Solution:
   S0 = 0, S1 = 0.

4. Assuming the RESET signal has been set to ”0” and will stay that way, what is the state following S0=1 and S1=1?
   Solution:
   S0 = 1, S1 = 0.

5. Now suppose there is skew in the CLK signal such that the rising edge of CLK always arrives at the left register exactly 1ns before it arrives at the right register. What is the smallest clock period for which the circuit still operates correctly?

   Solution:
   Fortunately the skew doesn't introduce any hold time problems with the input to the right register. t_{CLK} can now be as small as 8ns (both paths between registers fit exactly).