50.002 COMPUTATIONAL STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

Problem Set 3

1 Warm Up – Combinational Logic Timing

Consider the following combinational logic. Each logic gate has the same propagation delay, $t_{pd} = 2ns, t_{cd} = 1ns$. Compute the overall propagation delay and contamination delay for the circuit.

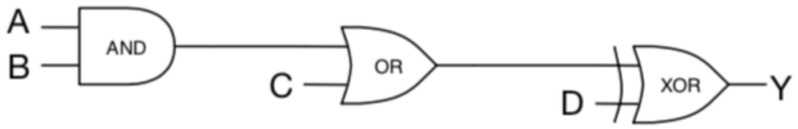

Figure 1

Solution:
Overal $t_{pd} = 6ns$ (counting paths from the AND gate, OR gate, and XOR gate). Overall $t_{cd} = 1ns$ (counting the shortest path from XOR gate only).

2 Warm Up – Tracing CMOS Circuit

Draw the truth table for the following CMOS circuitry:

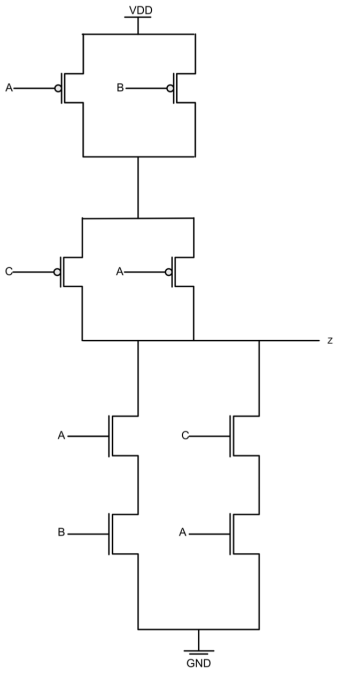

Figure 2

Solution:

A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Table 1

3 Full Adder Timing Analysis

Refer to the FA circuitry below, Compute the t_{pd} and t_{cd} of the full adder above.

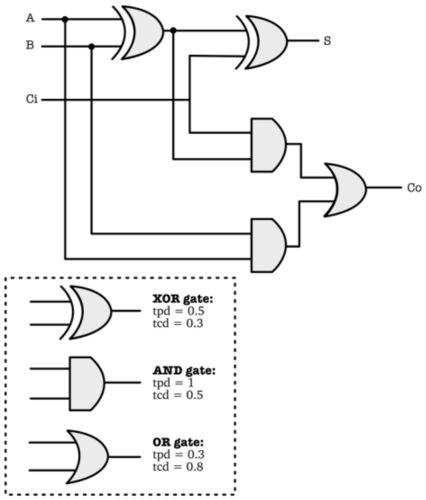

Figure 3

If we were to put several of these FAs to form an 8-bit ripple-carry adder as shown, **compute the t_{pd} and t_{cd} of an 8-bit ripple-carry adder made of 8 of these FA circuits**. In the figure, C_0 is assumed to be grounded for this particular instance, so this sample device can only add two numbers and not subtract them. *However, is the computation of t_{pd} and t_{cd} of an 8-bit ripple carry adder usage specific?*.

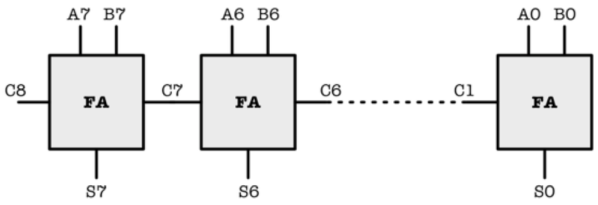

Figure 4

Solution:
t_{pd} is 1.8 and the t_{cd} is 0.3 for the FA. For the 8-bit ripple-carry adder, we do not have an input C_0 as it is grounded. However the t_{cd} is *still* 0.3 as the specification of contamination delay is not usage specific. Its t_{pd} is eight times bigger than a single FA, $t_{pd} = 14.4$.

However if the question is asking for the t_{cd} of **this** particular device with no C_0 at all (and not 8-bit ripple carry adder), then the answer is **0.6ns** since there's no C_0.

4 Combinational Construction Rules

In lecture, we learned two basic principles regarding the class of combinational devices. The first allows us to build a combinational device from, e.g., electronic components. A combinational device is a circuit element that has:

1. one or more digital inputs
2. one or more digital outputs
3. a functional specification that details the value of each output for every possible combination of valid input values
4. a timing specification consisting (at minimum) of an upper bound t_{pd} on the required time for the device to compute the specified output values from an arbitrary set of stable, valid input values.

while the second allows us to construct complex combinational devices from acyclic circuits containing simpler ones. A set of interconnected elements is a combinational device if:

1. each circuit element is combinational
2. every input is connected to exactly one output or to some vast supply of 0's and 1's
3. the circuit contains no directed cycles

In this problem, we ask you to think carefully about why these rules work - in particular, why an acyclic circuit of combinational devices, constructed according to the second principle, is itself a combinational device as defined by the first. You may assume for the following that every input and output is a logical 0 or 1. Consider the following 2-input acyclic circuit whose two components, A and B, are each combinational devices:

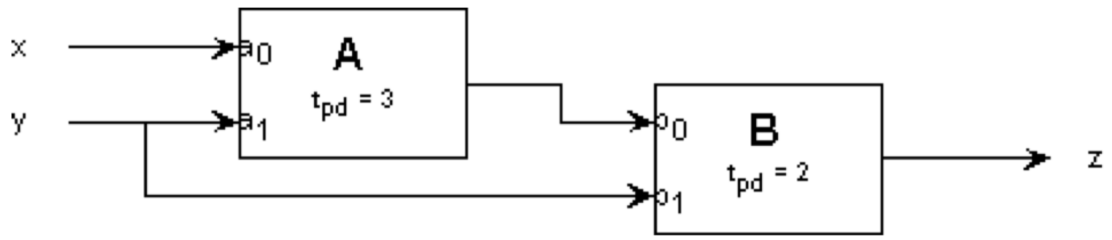

Figure 5

The propagation delay - the upper bound on the output settling time - for each device is specified in nanoseconds. The functional specifications for each component are given as truth tables detailing output values for each combination of inputs:
Answer the following questions,

a_0	a_1	A_{a_0,a_1}	b_0	. b_1	$B_{b_0.b_1}$
0	0	1	0	0	0
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	1	1	1

Table 2

1. Give a truth table for the acyclic circuit, i.e. a table that specifies the value of z for each of the possible combinations of input values on x and y.

   Solution:

x	y	z
0	0	0
0	1	0
1	0	0
1	1	1

Table 3

2. Describe a general procedure by which a truth table can be computed for each output of an arbitrary acyclic circuit containing only combinational components. *Hint : construct a functional specification to each circuit node*.
   Solution:
   We can construct the truth table from left to right, i.e: solve the truth table for each component from the leftmost all the way to the rightmost one by one.

3. Specify a propagation delay (the upper bound required for each combinational device) for the circuit.

   Solution:
   The total propagation delay is $3 + 2 = 5$.

4. Describe a general procedure by which a propagation delay can be computed for an arbitrary acyclic circuit containing only combinational components. *Hint: add a timing specification to each circuit node*.

   Solution:
   One has to find the longest path from input to output to find the total propagation delay of the combinational circuit.

5. Do your general procedures for computing functional specifications and propagation delays work if the restriction to acyclic circuits is relaxed? Explain.

Solution:
No, the signal can propagate back in the circuit so using the longest path to calculate t_{pd} is not accurate.

5 CMOS Circuit Boolean Expression

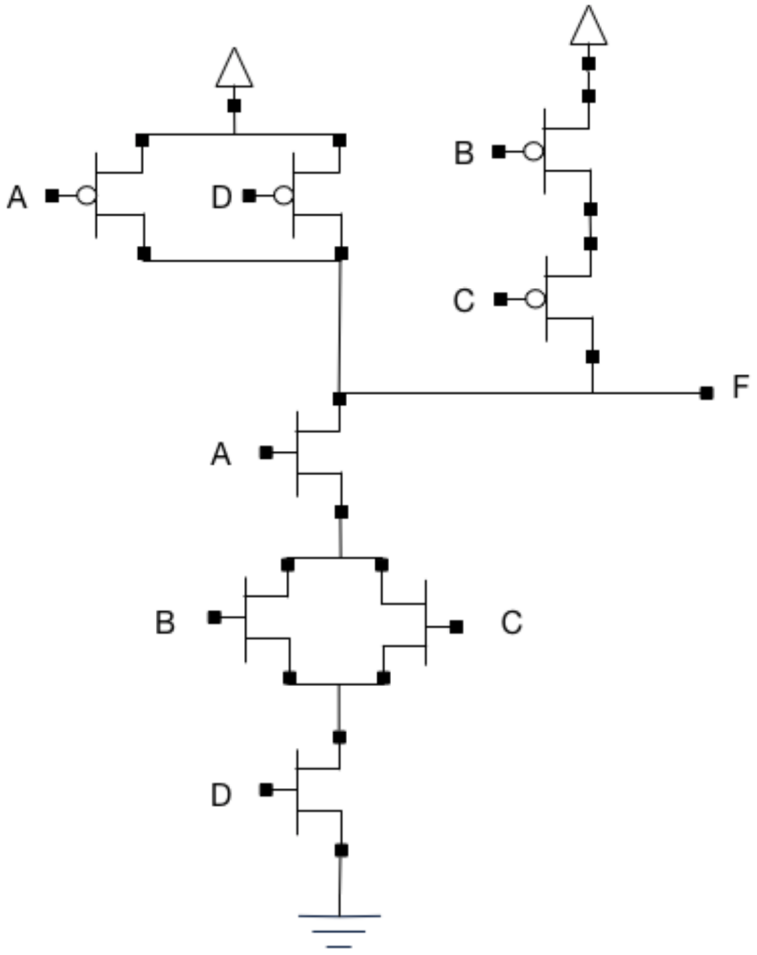

Figure 6

Draw the truth table of the CMOS circuit above. What is the boolean expression for the CMOS circuit shown?

Solution:
$F = \overline{A(B+C)D}$

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Table 4