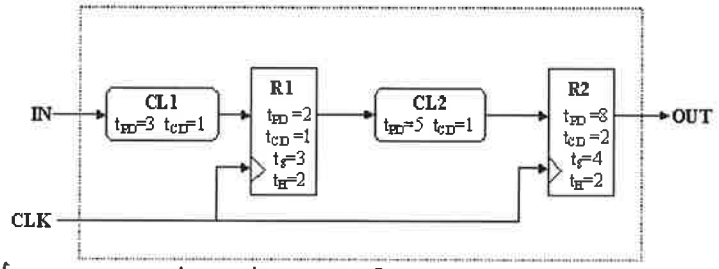
Problem 1. Consider the following diagram of a simple sequential circuit:



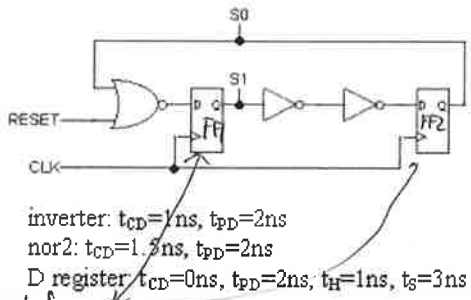
The components labeled CL1 and CL2 are combinational; R1 and R2 are edge-triggered flip flops. Timing parameters for each component are as noted.

A. Write the timing specifications (tS, tH, tCD, tPD, tCLK) for the system as a whole using the timing specifications for the internal components that are given in the figure.

B. Suppose you had available a faster version of CL2 having a propagation delay of 3 and a contamination delay of zero. Could you substitute the faster CL2 for the one shown in the diagram? Explain.

Not

Problem 2. The following circuit diagram implements a sequential circuit with two state bits, S0 and S1:



A. What is the smallest clock period for which the circuit still operates correctly?

B. A sharp-eyed student suggests optimizing the circuit by removing the pair of inverters and connecting the Q output of the left register directly to the D input of the right register. If the clock period could be adjusted appropriately, would the optimized circuit operate correctly? If yes, explain the adjustment to the clock period that would be needed.

C. When the RESET signal is set to "1" for several cycles, what values are S0 and S1 set to?

D. Assuming the RESET signal has been set to "0" and will stay that way, what is the state following S0=1 and S1=1?

E. Now suppose there is *skew* in the CLK signal such that the rising edge of CLK always arrives at the left register exactly 1ns before it arrives at the right register. What is the smallest clock period for which the circuit still operates correctly?

8ns