50.002 COMPUTATION STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

Problem Set 5

1 Warm Up – Flip Flops

Consider the following diagram of a simple sequential circuit:

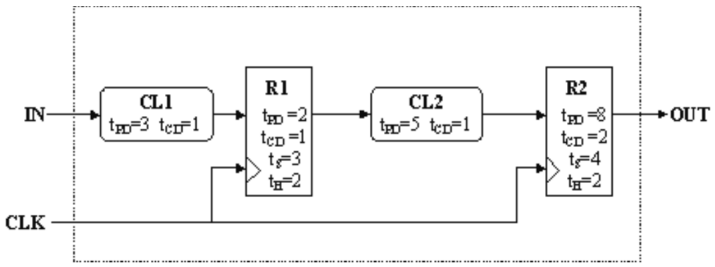


Figure 1

The components labeled CL1 and CL2 are combinational; R1 and R2 are edge triggered flip flops. Timing parameters for each component are as noted. Answer both questions below:

1. Write the timing specifications (tS, tH, tCD, tPD, tCLK) for the system as a whole using the timing specifications for the internal components that are given in the figure.

2. Suppose you had available a faster version of CL2 having a propagation delay of 3 and a contamination delay of zero. Could you substitute the faster CL2 for the one shown in the diagram? Explain.

2 Warm Up – Analyzing Timing Plot

Consider the following unusual D-latch configuration:

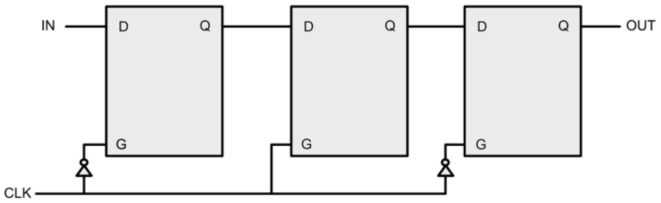


Figure 2

Now we feed it the following input signal and CLK signal. Which of the following signal plots represent the output of this device made out of 3 D-latches? Assume that the jagged edges means unknown value and that the contents of each latch in the beginning is unknown.

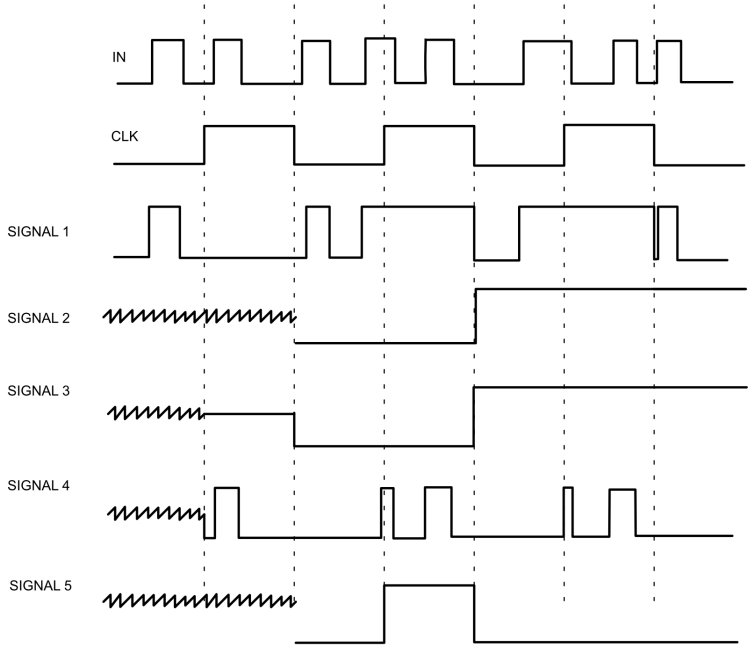


Figure 3

3 Warm Up – Simple Timing Computation

Consider the following circuit, and **notice the feedback loop**:

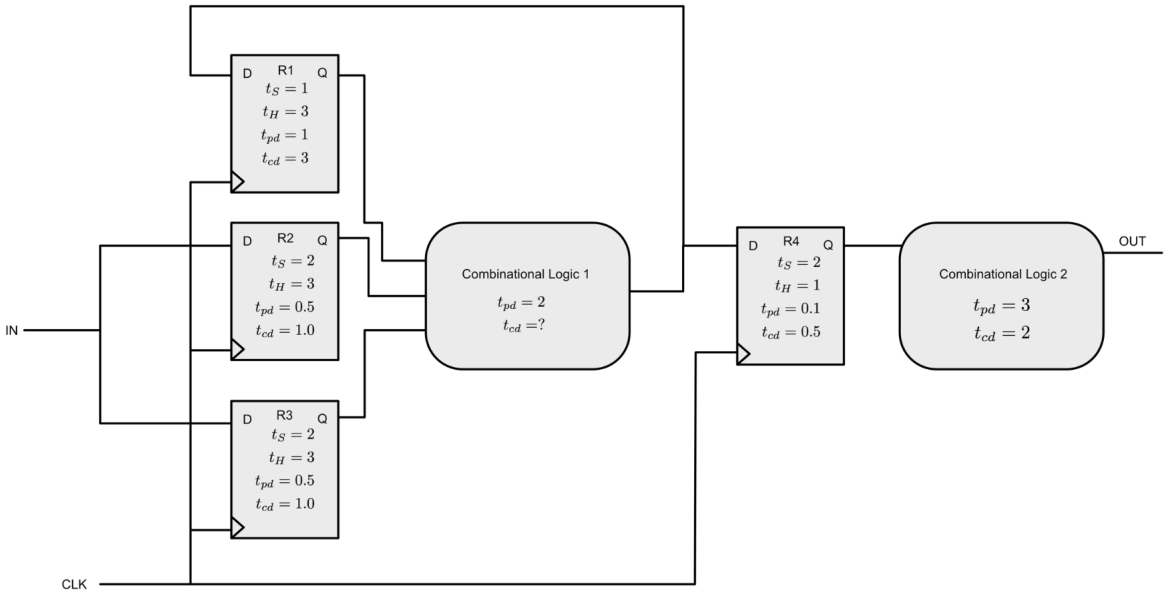


Figure 4

Setup time, hold time, propagation delay, and contamination delay (all in nanoseconds) of each component is as written above. Lets now analyse its timing constraints:

(a) What is the minimum contamination delay (tcd) of Combinational Logic 1 such that the sequential circuit may still function properly?

(b) Write down the minimum CLK period for the sequential circuit to function properly.

(c) Write down the minimum hold time (tH) for the IN signal to the system.

(d) Write down the minimum propagation time of the sequential logic circuit.

4 Metastable State Analysis

Consider the following D-latch device and its VTC plot:

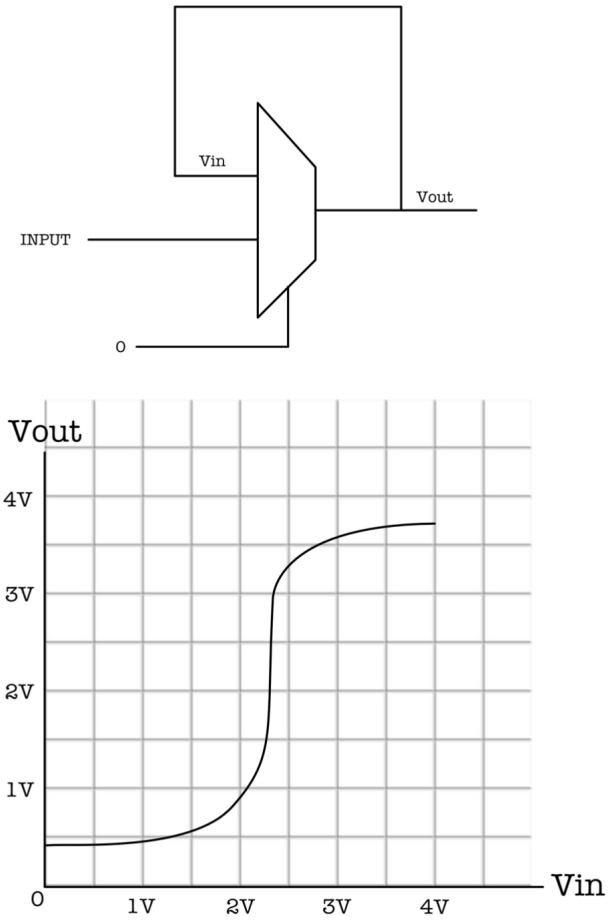


Figure 5

We are given the following specification about the multiplexer's valid operating voltage ranges: $V_{IL} = 1V, V_{OL} = 0.5V, V_{IH} = 3V, VOH = 3.5V$. The noise margin is $0.5V$ and we can assume that the device obeys the **static discipline**.

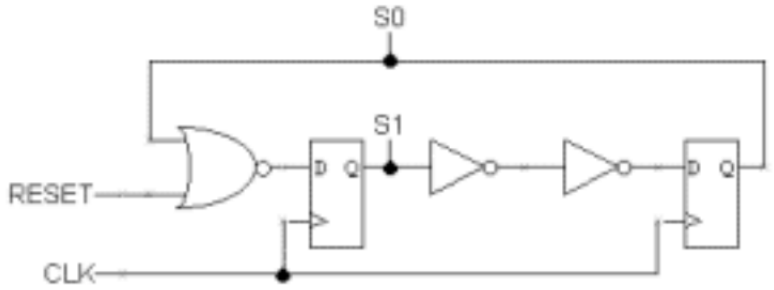
(a) Which voltage value approximately, has the highest probability for the device to be in the metastable state?

(b) Compare $V_{IN} = 0.9V$ vs $V_{IN} = 3V$. Which input voltage will most likely cause the device stay in the metastable state?

(c) Compare $V_{IN} = 2.1V$ vs $V_{IN} = 2.5V$. Which input voltage will most likely cause the device stay in the metastable state?

5 Another Combinational Circuit

The following circuit diagram implements a sequential circuit with two state bits, S0 and S1:



inverter: t_{CD}=1ns, t_{PD}=2ns
nor2: t_{CD}=1.5ns, t_{PD}=2ns
D register: t_{CD}=0ns, t_{PD}=2ns, t_H=1ns, t_S=3ns

Figure 6

Answer the following questions:

1. What is the smallest clock period for which the circuit still operates correctly?
2. A sharp-eyed student suggests optimizing the circuit by removing the pair of inverters and connecting the Q output of the left register directly to the D input of the right register. If the clock period could be adjusted appropriately, would the optimized circuit operate correctly? If yes, explain the adjustment to the clock period that would be needed
3. When the RESET signal is set to ”1” for several cycles, what values are S0 and S1 set to?
4. Assuming the RESET signal has been set to ”0” and will stay that way, what is the state following S0=1 and S1=1?

6 Advanced Timing Computation

Take a look at the following State Machine circuitry:

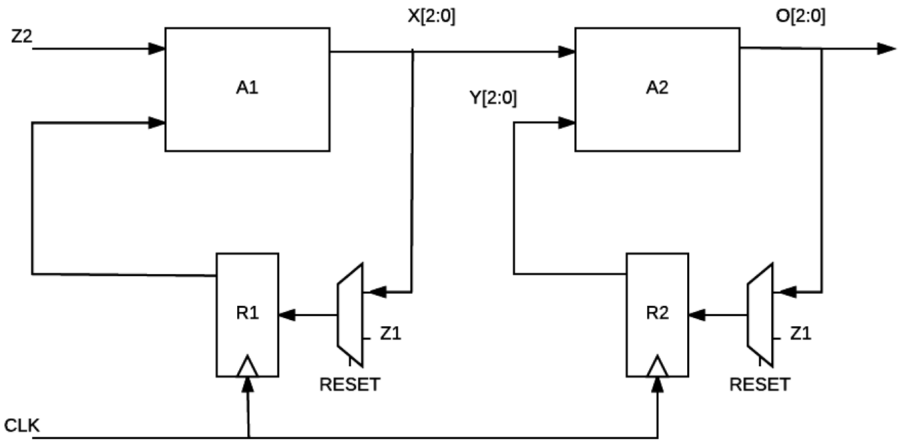


Figure 7

The device A2 has the following schematic:

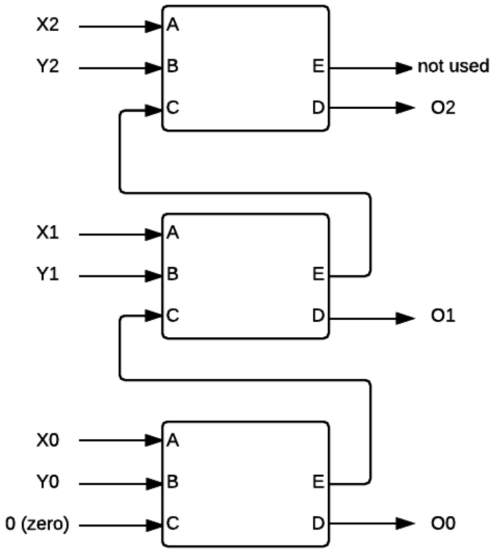


Figure 8

Basically, it is made out of this device we call A000R with **tcd = 1ns, and tpd = 3ns** with the followings chematic

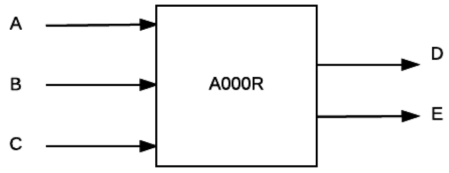


Figure 9

The truth table for A000R is as follows:

A	B	C	D	E
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1

The timing specifications for other devices in the state machine is:

- The Mux has the following time specification: **tcd = 1ns, and tpd = 2ns.**
- The Registers has the following time specification: **tcd = 2ns, tpd = 5ns, ts = 2ns, th = 2ns.**

Both A1 and A2 are combinational logic that contains A000R only. Unfortunately, the design for A1 is missing. We only know that A1 uses only A000R to compute the output and the next state function **and that A1 has the same tpd as A2**. The other information that we have is that the output of A1, X[2:0], is a sequence of decimal, [1, 2, 3, ...] in the binary form, i.e. [001, 010, 011, ...].

Answer the following questions:

(a) What is the number of bits that the constant Z1 should have?

(b) What is the minimum number of bits that the constant Z2 should have?

(c) What is the decimal value of Z1?

(d) What is the decimal value of Z2?

(e) What is the tpd of A2 in nanosecond?

(f) What is the minimum clock period in nanosecond?

(g) What is the minimum Tcd of A1 in nanosecond?

(h) What is the Tcd of A2 in nanosecond?

(i) When RESET is 1 for several cycles, what is the value of X[2:0]?

(j) When outputing the X sequence [1, 2, 3, ...], what is the value of RESET?

(k) Suppose that at time t = 0, RESET signal is changed from 1 to 0, and X becomes 0b001. From then on, RESET remains 0.

   (a) What is the decimal value of O[2:0] at time $t = 0$?

   (b) What is the decimal value of O[2:0] at time $t = 1$?

   (c) What is the decimal value of O[2:0] at time $t = 3$?

7 Hardware Implementation of another state machine

Consider the schematic of a machine before that is able to **Detects a sequence of three or more consecutive 1's, and output: 1 after three or more consecutive 1's, or 0 otherwise.**

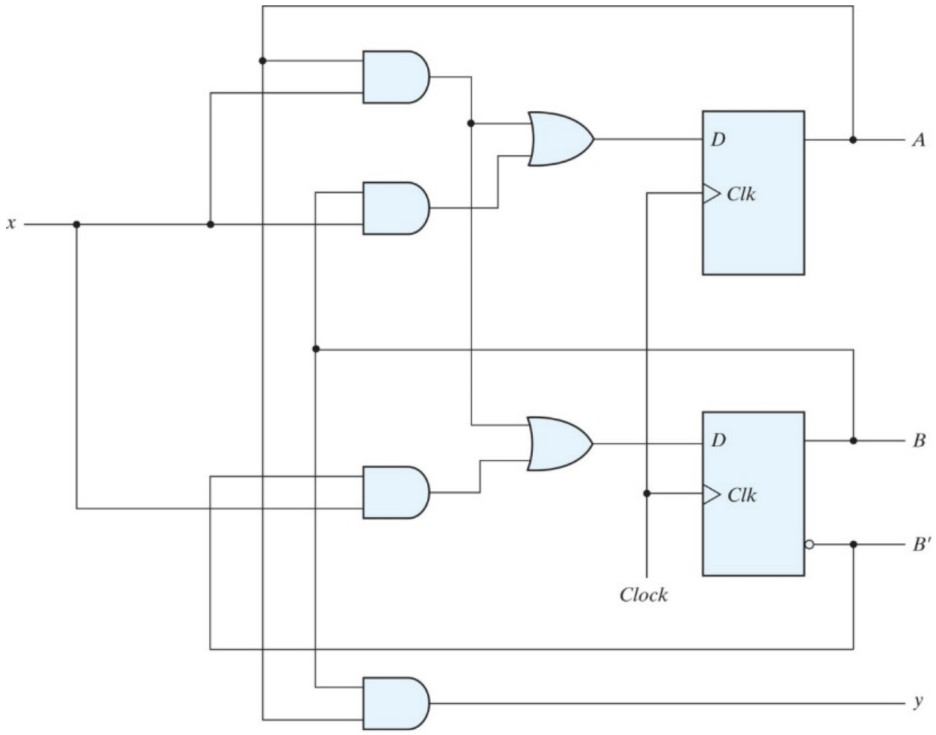


Figure 10

Lets analyse the circuit by answering the questions below:

(a) If the circuit has an initial state of AB=00, and the input at t=0 is x=0, what is the next state?

(b) If the initial state is AB=00 and the input at t=0 is x=1, what is the next state?

(c) If the current state is AB=01, and the input is x=1, what is the next state?

(d) If the current state is AB=10, and the input is x=1, what is the next state?

(e) If the current state is AB=11, and the input is x=1, what is the next state?

(f) If the current state is AB=11, and the input is x=0, what is the next state?

(g) What are the state(s) that can go to state AB=00 as its next state?

(h) What is the output y when the current state is AB = 11 and the current input is x = 0?

(i) The propagation delays for all the combinational logic gates and the flip-flops are 2 ns. The clock frequency is 100 MHz. **What is the worst case delay** in nanosecond for the next states at A and B to appear (i.e. for A and B to be valid) after the input x is changed to be a valid input. **Assume that the initial states of both dff are given**.

(j) The propagation delays for all the combinational logic gates and the flip-flops are 2 ns. The dffs have thold and tsetup of 1ns each. If the clock frequency is not given, *what is the maximum clock frequency* that we can have for this device?

(k) What is the next output sequence from $t = 1$ to $t = 16$ of the circuit with the following input (fed from left to right): 1101 1111 1110 0010 at $t = 0$ to $t = 15$ (assuming the initial states of both flip flops are 0)?