Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2020

Lab Number 4 – Two's Complement Adder/Subtractor

Due September 27, 2020, 11:59 PM

This exercise uses The BitBoard.

CSE 2441 **LABORATORY ASSIGNMENT 4** **FALL 2020**

TWO'S COMPLEMENT ADDER/SUBTRACTOR

(100 POINTS)

PURPOSE/OUTCOMES

To introduce you to circuits for adding and subtracting numbers in a two's complement number system. After completing this lab, you will have demonstrated an ability to design four-bit adders and subtractors, to capture and verify your designs using Quartus II, and to construct and test your designs on a BB/DE1.

BACKGROUND

In Lab 3, you designed, constructed, and tested full adders and a four-bit ripple-carry adder that used four full-adders as components as shown in Figure 1. In this lab you will design, construct, and test a two's complement adder/subtractor circuit as described below.

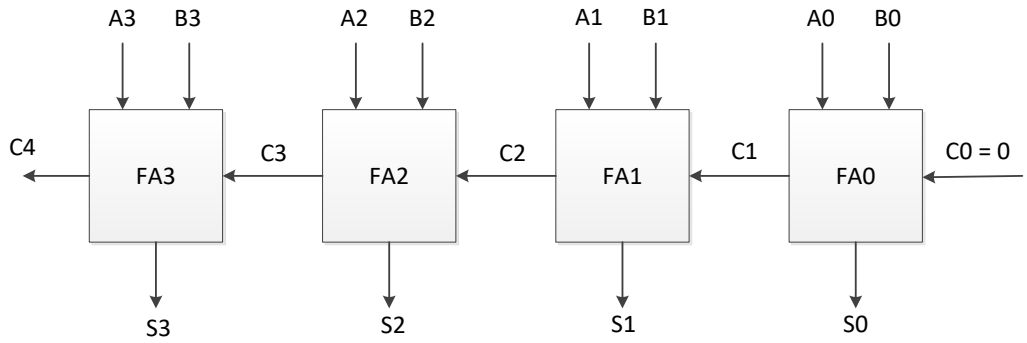

Figure 1 – Four-Bit Ripple-Carry Adder (A + B)

Recall that if *A* and *B* are binary numbers then $A - B = A + (-B) = A + [B]_2 = A + [B]_1 + 1$ where $[B]_2$ is the *2's* complement of *B and* $[B]_1$ is the 1's complement. Example, if *A = 0101* and *B = 0010*, then $A - B = 0101 + (-0010) = 0101 + [0010]_2 = 0101 + [0010]_1 + 1 = 0101 + 1101 + 1 = \cancel{1}0011$. The following modified four-bit ripple-carry adder performs all of this in hardware.

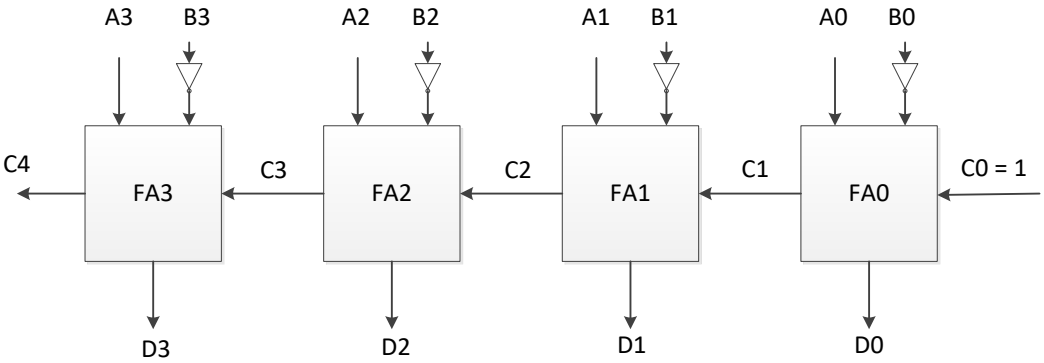

Figure 2 – Four-Bit Two's Complement Subtractor (A - B)

LAB REQUIREMENTS

1. Design a realization of a four-bit, two's-complement adder/subtractor corresponding to the block diagram in Figure 3. Your design should incorporate the ripple-carry adder that you designed and simulated in Lab 2 and constructed and tested in Lab 3.
2. Use Quartus II to capture and verify your design by simulating it's response to the test inputs given in step 5.
3. Create a symbol file for your design for use in a later lab assignment.

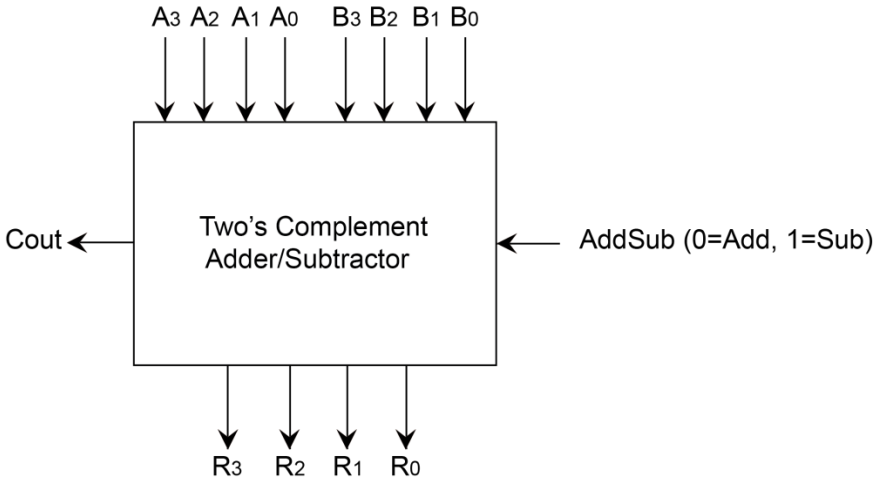

Figure 3 Two's Complement Adder/Subtractor

4. Construct your two's-complement adder/subtractor by modifying the ripple-carry adder you constructed in Lab 3. Use the following pin assignments.

   A3: SW7, *A2:* SW6, *A1*: SW5, *A0*: SW4
   B3: SW3, *B2*: SW2, *B1*: SW1, *B0*: SW0
   R3: LEDR3, *R2*: LEDR2, *R1*: LEDR1, *R0*: LEDR0
   C4: LEDR4
   C0: SW8

5. Test your adder/subtractor for the values of A and B in the following table.

A	***B***	***R = A + B***	***Cout(C4)***	***R = A - B***	***Cout(C4)***
0101	0001				
0111	0001				
0111	1111				
1001	1110				
1010	1110				
1101	1100				

REPORT REQUIREMENTS

1. Cover sheet (as shown on this assignment)
2. Lab purpose
3. Diagram of your adder/subtractor design
4. Simulation results (waveforms) showing the verification of your design
5. Symbol file input/output diagram
6. Picture of your constructed adder/subtractor circuit
7. Pictures of your tests for 0101 + 0001 and 1010 + 1110
8. Test results table