Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2020

Lab Number 5 – Programming the Altera DE1

100 Points

Due October 4, 2020, 11:59 PM

CSE 2441 LABORATORY NUMBER 5 FALL 2020

PROGRAMMING THE ALTERA DE1 DEVELOPMENT AND EDUCATION BOARD

(100 POINTS)

PURPOSE and OUTCOME: To give you experience using the basic features of the DE1 in FPGA mode and programming the on-board Cyclone II field programmable gate array (FPGA). Once you've successfully completed the exercises below, you will be able to implement and test basic digital logic circuits on the DE1.

BASIC DE1 FEATURES

The DE1 Development and Education Board is suitable for use in undergraduate teaching laboratories, yet it is powerful enough for prototyping of complex designs. An image of the DE1 is shown below in Figure 1. Features of the DE1 include the following.

- Cyclone II EP2C20F484C7 field programmable gate array
- Ten data switches (SW0-SW9)
- Four debounced pushbutton switches (KEY0-KEY3)
- Ten red LED displays (LEDR0-LEDR9)
- Eight green LED displays (LEDG0-LEDG7)
- Four 7-segment LED displays (HEX0-HEX3)
- RUN/PROG switch
- ON/OFF switch
- Power port
- USB/MIC/LINE-IN/LINE-OUT/VGA/RS-232/PS2/BNC I/O ports
- Two header blocks
- SD memory card slot
- SDRAM/SRAM/Flash on-board memory chips

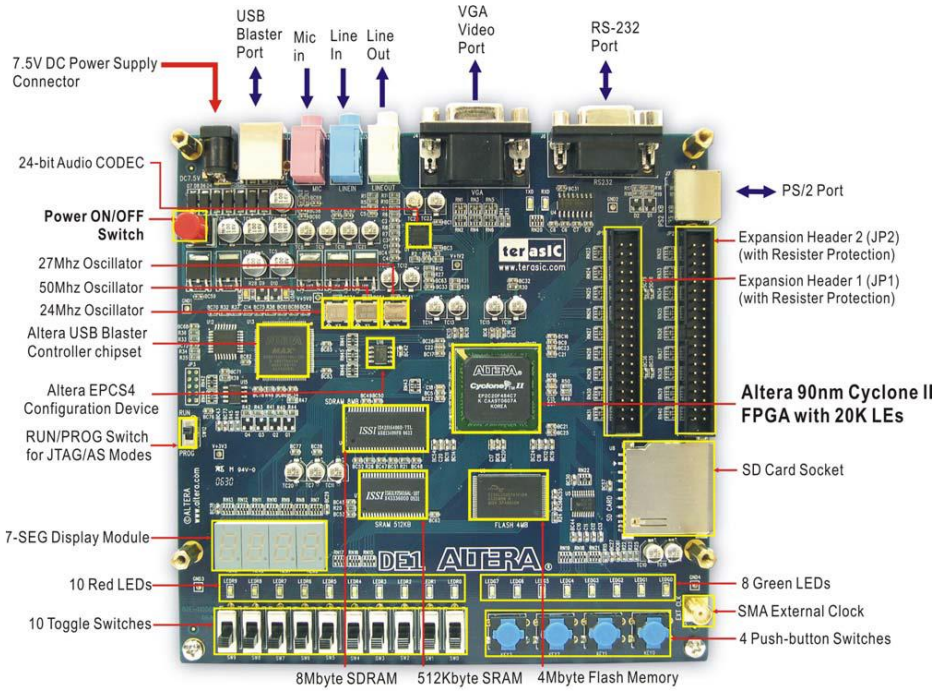


Figure 1. DE1 Layout.

BASIC OPERATION AND PROGRAMMING OF THE DE1

The DE1 is used in *BitBoard mode* as an input/output device for The BitBoard as you have done in previous labs. The DE1 can also be programmed to realize logic circuits with the on-board Cyclone II FPGA. This is referred to as the *FPGA mode*. In FPGA mode, the DE1 switches and LEDs serve as inputs and outputs for the circuit realized by the FPGA.

Programming an FPGA is the equivalent of interconnecting gates and flip flops with wires on a printed circuit board. But, as you will learn, much easier and faster. Programming the Cyclone II is done using tools provided in Quartus II and can be viewed as an extension of the design flow that you've been following in previous exercises. The programming process is outlined below and illustrated in Figure 2.

1. Capture, or enter, your circuit design using Quartus II. This can be a circuit diagram or HDL (VHDL or Verilog) code.
2. Compile your design.
3. Verify your design using the Quartus II simulator.
4. Assign the input/output nodes of your design to specific pins on the DE1. This can be done using the Quartus II Assignment Editor.
5. Recompile your design so that the pin assignments will be incorporated.
6. Program or "burn" the Cyclone II with your design using the Quartus II Programmer tool.
7. Test your design using the DE1 input switches and pushbuttons and output LEDs and seven-segment displays.

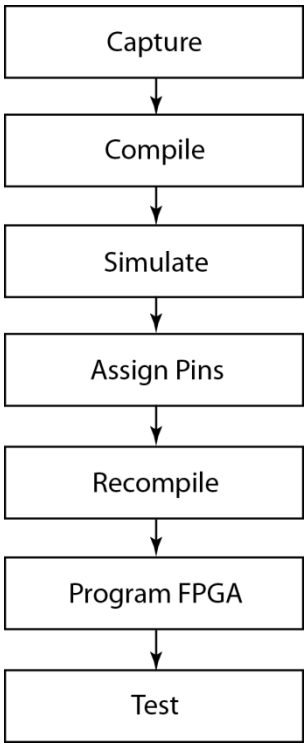


Figure 2. DE1 FPGA Programming Process.

USING THE DE1 – GUIDED TOUR

In this section, you will be guided through these steps for the circuit shown below in Figure 3. You may recognize this as the same circuit you captured in Laboratory Exercise 2 when learning to use Quartus II.

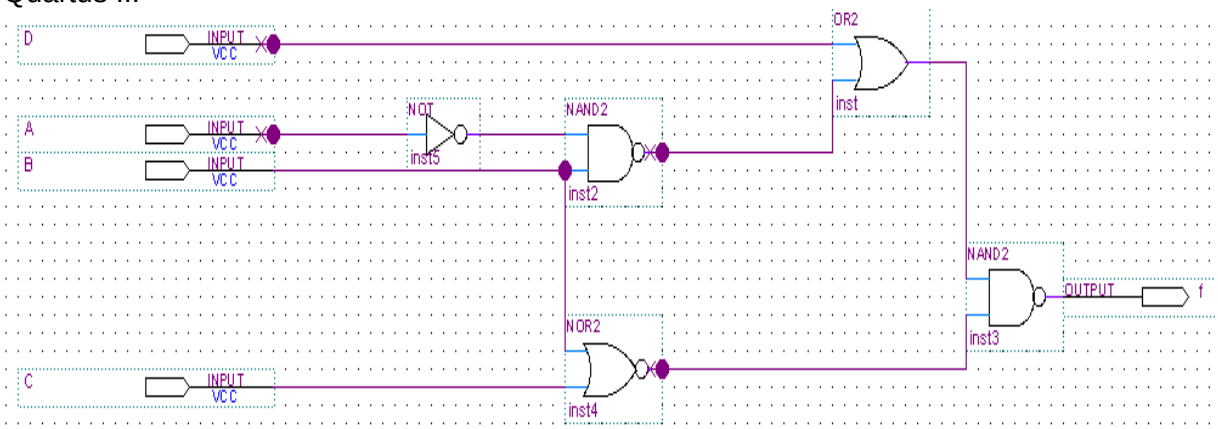


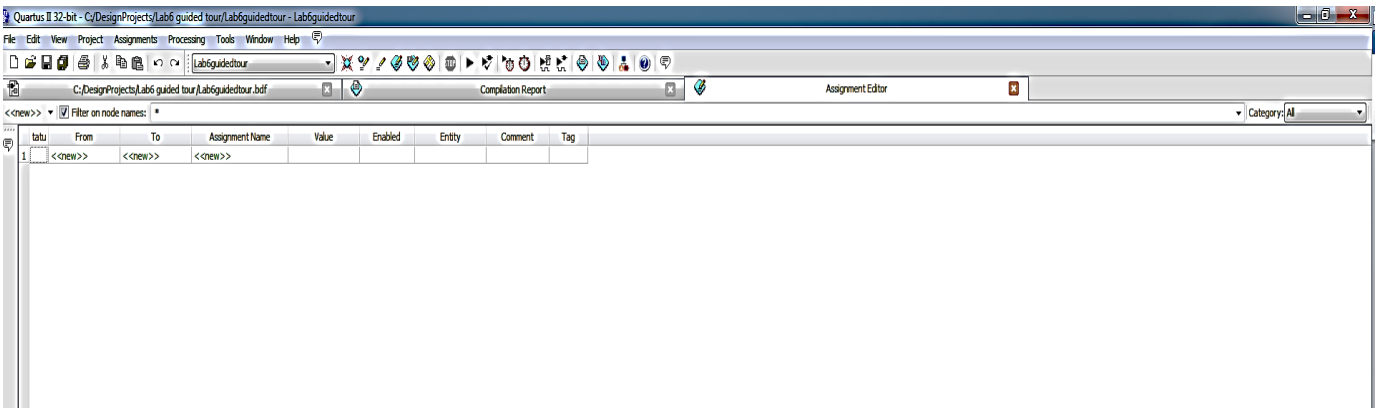
Figure 3. DE1 Guided Tour Exercise Schematic Diagram.

1. Capture the circuit schematic using Quartus II or reuse your .bdf file from lab 2. Make sure the Cyclone II family and EP2C20F484C7 device have been selected.
2. Compile your design.
3. Verify your design using the simulator.
4. The circuit inputs A,B,C,D and output f must be assigned to specific switches and LEDs on the DE-1 in order for the Programmer to properly make the connections to the Cyclone II FPGA device. Use the assignments below for this design. See the Appendix for the pin assignments for all of the DE-1 I/O switches and LEDs.

A (SW3) -> PIN_V12	Aout (LEDR3) -> PIN_Y19
B (SW2) -> PIN_M22	Bout (LEDR2) -> PIN_U19
C (SW1) -> PIN_L21	Cout (LEDR1) -> PIN_R19
D (SW0) -> PIN_L22	Dout (LEDR0) -> PIN_R20
f (LEDG0 -> PIN_U22	

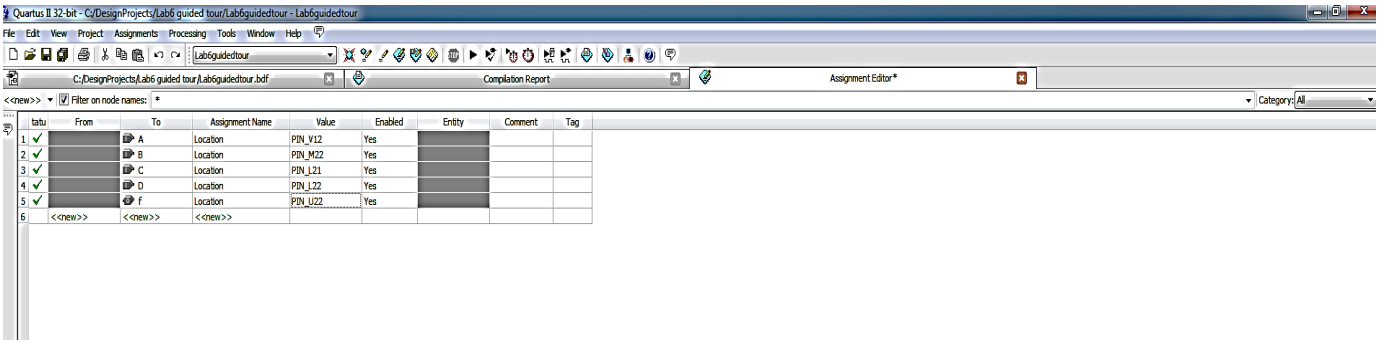
Use the Quartus II Assignments Editor to enter the assignments as illustrated below.

Select ***Assignments > Assignment Editor*** from the Quartus II memu which will take you to the following window.



All should be selected in the ***Category*** drop-down menu.

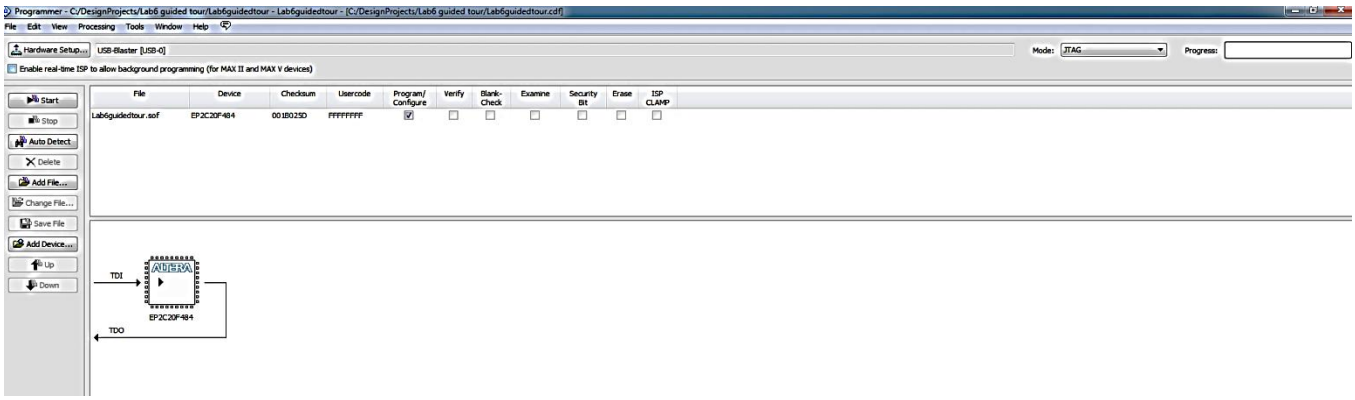
Now enter the pin assignments by filling the ***To, Assignment Value***, and ***Value*** columns. This will produce the following window. Save the assignment using ***File > Save***.



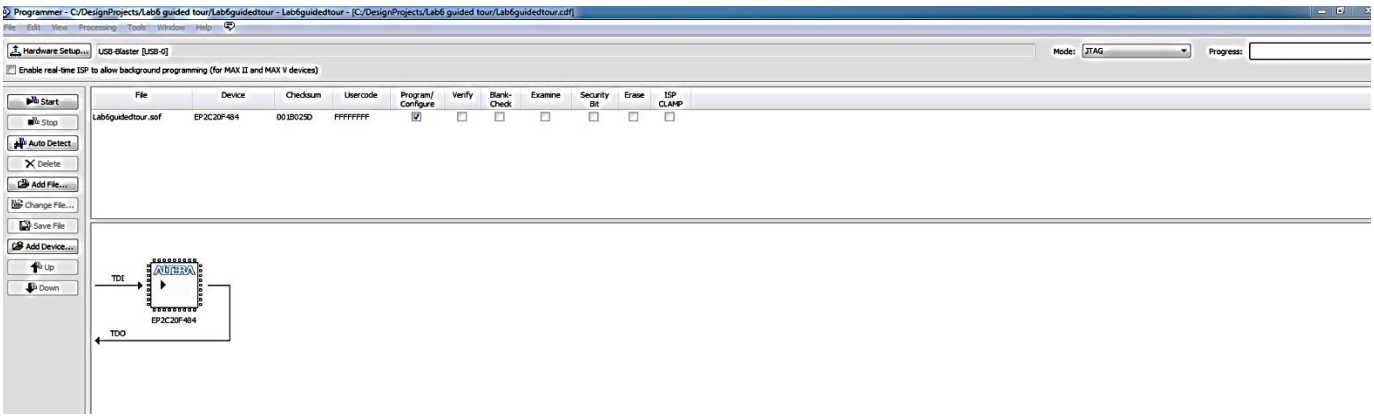
5. Recompile your design to incorporate the pin assignments.

6. Program the Cyclone II with your design using the Quartus II Programmer tool as illustrated below. JTAG programming will be used, so make sure the RUN/PROG switch on the DE1 is still in the RUN position.

Begin programming by selecting ***Tools > Programmer*** from the Quartus II menu. This will display the following window.



Select ***USB-Blaster*** in the ***Hardware Setup*** box if it's not already selected. Make sure ***JTAG*** is selected in the ***Mode*** box. The window should look like this.



Now click the ***Start*** button to begin programming. The box will display 100% (Successful) when done. Programming will only take a few seconds.

The Cyclone II FPGA on the DE1 is now programmed with the design and testing can begin.

7. Exaustively test your design on the DE-1 by successively entering the input patterns on SW3-SW0 and observing the responses on LEDG0.

A (SW3)	B (SW2)	C (SW1)	D (SW0)	f (LEDG0)
0 (down)	0 (down)	0 (down)	0 (down)	On/Off
0 (down)	0 (down)	0 (down)	1 (up)	On/Off
0 (down)	0 (down)	1 (up)	0 (down)	On/Off
0 (down)	0 (down)	1 (up)	1 (up)	On/Off
0 (down)	1 (up)	0 (down)	0 (down)	On/Off
0 (down)	1 (up)	0 (down)	1 (up)	On/Off
0 (down)	1 (up)	1 (up)	0 (down)	On/Off
0 (down)	1 (up)	1 (up)	1 (up)	On/Off
1 (up)	0 (down)	0 (down)	0 (down)	On/Off
1 (up)	0 (down)	0 (down)	1 (up)	On/Off
1 (up)	0 (down)	1 (up)	0 (down)	On/Off
1 (up)	0 (down)	1 (up)	1 (up)	On/Off
1 (up)	1 (up)	0 (down)	0 (down)	On/Off
1 (up)	1 (up)	0 (down)	1 (up)	On/Off
1 (up)	1 (up)	1 (up)	0 (down)	On/Off
1 (up)	1 (up)	1 (up)	1 (up)	On/Off

USING THE DE1 – DO-IT-YOURSELF EXERCISE

Implement and test the full-adder circuit that you designed previously on the DE1 following the steps from the guided tour. ***Employ exhaustive testing.*** Use the following DE1 pin assignments. See Figure 4 for the pin-outs.

A (SW2) -> PIN_M22
B (SW1) -> PIN_L21
C (SW0) -> PIN_L22
S (LEDG0) -> PIN_U22
Cout (LEDG1) -> PIN_U21

Aout (LEDR2) -> PIN_U19
Bout (LEDR1) -> PIN_R19
Cout (LERD0) -> PIN_R20

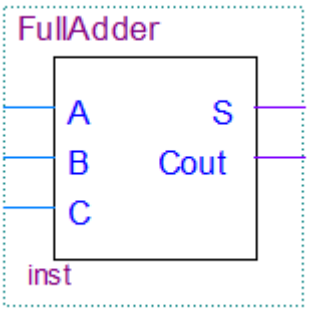


Figure 4. DE1 Do-It-Yourself Exercise Pin-Out Diagram.

IMPLEMENTING YOUR FOUR-BIT ADDER/SUBTRACTOR

Implement the Adder/Subtractor that you designed in Laboratories 3 and 4 on the DE1. Use the following DE1 pin assignments corresponding to the pin-out diagram in Figure 5.

AddSub (SW8) -> PIN_M1
A3 (SW7) -> PIN_M2
A2 (SW6) -> PIN_U11
A1 (SW5) -> PIN_U12
A0 (SW4) -> PIN_W12
B3 (SW3) -> PIN_V12
B2 (SW2) -> PIN_M22
B1 (SW1) -> PIN_ L21
B0 (SW0) -> PIN_L22

R3 (LEDG3) -> PIN_V21
R2 (LEDG2) -> PIN_V22
R1 (LEDG1) -> PIN_U21
R0 (LEDG0) -> PIN_U22

Cout (LEDG7) -> PIN_Y21

AddSubout (LEDR8) -> PIN_R18
A3out (LEDR7) -> PIN_U18
A2out (LEDR6) -> PIN_Y18
A1out (LEDR5) -> PIN_V19
A0out (LEDR4) -> PIN_T18
B3out (LEDR3) -> PIN_Y19
B2out (LEDR2) -> PIN_U19
B1out (LEDR1) -> PIN_R19
B0out (LEDR0) -> PIN_R20

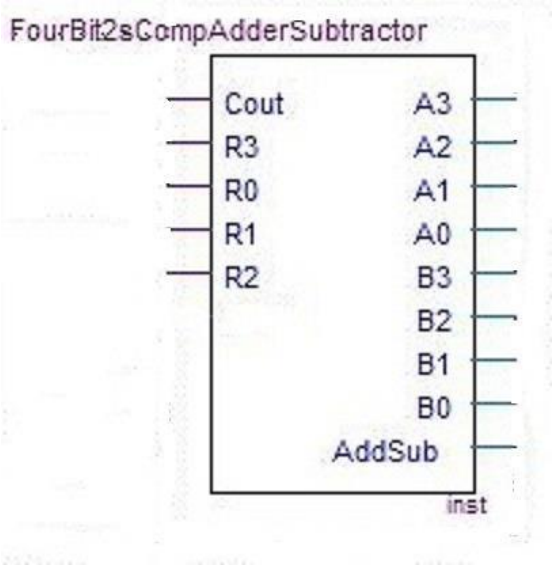


Figure 5. Four-Bit Adder/Subtractor Pin-Out Diagram

Test your implementation with the inputs given in the following table.

A	***B***	***R = A + B***	***Cout(C4)***	***R in Signed Decimal***	***R = A - B***	***Cout(C4)***	***R in Signed Decimal***
0101	0010						
0101	1110						
0101	0011						
0110	1010						
1011	1110						
1101	1010						
1011	0000						
1010	1110						

Mark any overflow results.

REPORT REQUIREMENTS

1. Cover sheet (as shown on this assignment)
2. Lab purpose
3. Screen shot of your *guided tour* circuit showing input and output pins.
4. Screen shot of your *guided tour* pin assignments.
5. Exhaustive test results table for your *guided tour* circuit.
6. Pictures of your *guided tour* test inputs/outputs for *ABCD* = 0101 and *ABCD* = 1100
7. Screen shot of your *full adder* symbol showing input and output pins.
8. Screen shot of your *full adder* pin assignments.
9. Exhaustive test results table for your *full adder* circuit.
10. Pictures of your test inputs/outputs for *ABC* = 000, *ABC* = 010, *ABC* = 101, and *ABC* = 111
11. Screen shot of your *2's complement adder/subtractor* symbol showing input and output pins.
12. Screen shot of your *2's complement adder/subtractor* pin assignments.
13. Test results table for your *full adder* circuit. Identify overflows, if any.
14. Pictures of your test inputs/outputs for *0101 + 1110, 0101 – 1110, 1101 + 1010, 1101 - 1010*

APPENDIX – DE1 I/O Pin Assignments

Input Switches	*LED Outputs*	*Seven-Segment*
SW0 – PIN_L22	LEDR0 – PIN_R20	HEX0(0) – PIN_J2
SW1 – PIN_L21	LEDR1 – PIN_R19	HEX0(1) – PIN_J1
SW2 – PIN_M22	LEDR2 – PIN_U19	HEX0(2) – PIN_H2
SW3 – PIN_V12	LEDR3 – PIN_Y19	HEX0(3) – PIN_H1
SW4 – PIN_W12	LEDR4 – PIN_T18	HEX0(4) – PIN_F2
SW5 – PIN_U12	LEDR5 – PIN_V19	HEX0(5) – PIN_F1
SW6 – PIN_U11	LEDR6 – PIN_Y18	HEX0(6) – PIN_E2
SW7 – PIN_M2	LEDR7 – PIN_U18	
SW8 – PIN_M1	LEDR8 – PIN_R18	HEX1(0) – PIN_E1
SW9 – PIN_L2	LEDR9 – PIN_R17	HEX1(1) – PIN_H6
		HEX1(2) – PIN_H5
KEY0 – PIN_R22	LEDG0 – PIN_U22	HEX1(3) – PIN_H4
KEY1 – PIN_R21	LEDG1 – PIN_U21	HEX1(4) – PIN_G3
KEY2 – PIN_T22	LEDG2 – PIN_V22	HEX1(5) – PIN_D2
KEY3 – PIN_T21	LEDG3 – PIN_V21	HEX1(6) – PIN_D1
	LEDG4 – PIN_W22	
	LEDG5 – PIN_W21	HEX2(0) – PIN_G5
	LEDG6 – PIN_Y22	HEX2(1) – PIN_G6
	LEDG7 – PIN_Y21	HEX2(2) – PIN_C2
		HEX2(3) – PIN_C1
		HEX2(4) – PIN_E3
		HEX2(5) – PIN_E4
		HEX2(6) – PIN_D3
		HEX3(0) – PIN_F4
		HEX3(1) – PIN_D5
		HEX3(2) – PIN_D6
		HEX3(3) – PIN_J4
		HEX3(4) – PIN_L8
		HEX3(5) – PIN_F3
		HEX3(6) – PIN_D4