Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2020

Laboratory 1 – Policies, Procedures, Resources, Basic Gates

Lab Report Due – September 6, 2020 by 11:59 PM

CSE 2441 **LABORATORY ASSIGNMENT 1** **FALL 2020**

Policies, Procedures, Resources, Basic Gates

PURPOSE: To introduce you to the digital logic lab policies and procedures and the equipment, tools, parts, and software that you'll be using during the semester.

LAB POLICIES and PROCEDURES

We are still living, working, and studying in unusual and difficult circumstances. Never-the-less we strive to provide you with a quality educational experience while keeping you healthy and safe. The following policies and procedures have been formulated with those objectives in mind. Please be mindful and respectful of these throughout the semester.

1. **Face coverings and social distancing – Masks must be worn at all times while working in the lab. It is recommended that you use MS Teams on your laptop, tablet, or smart phone to interact with your classmates or TA while in the lab.**
2. **Lab location –** ERB 127 is the primary lab facility for CSE 2441. However, the room capacity has been reduced to accommodate social distancing policies and guidelines. As such, ERB 126 will be used for overflow when necessary.
3. **Assignments –** Laboratory assignments and other documents will be placed, in advance, on Canvas. You have the responsibility for downloading and reading the relevant materials each week.
4. **Lab reports –** Lab reports must be submitted on Canvas by the due date in order to receive full credit.
5. **Late penalties –** Lab reports submitted late will be reduced by 20 points for each day late.
6. **Working at home –** You are expected to perform your lab work at home using resources provided in The BitBox lab kit and Quartus II Web-Edition, Version 13.0 sp1, installed on your laptop or home computer. You may download the software from Intel FPGA by clicking the link below and following directions. Be sure to download and install the Cyclone II devices while installing the software. http://fpgasoftware.intel.com/13.0sp1/?edition=web.
7. **Lab sessions –** Lab sessions should be used primarily to get help and/or pick up wire or other materials.
8. **Help sessions –** You are encouraged to use the virtual help sessions instead of coming to campus in order to minimize face-to-face contact. See the syllabus for days and times.
9. **Demonstrations of work –** Some assignments and the term project will require in-person, real-time virtual, or video demonstrations of your work.
10. **Lab grading –** Each lab assignment will be worth 100 points and will be averaged to compute your lab grade.
11. **Lab grade –** Your lab grade will count for 20% of your final course grade.
12. **Equipment problems –** Please report any faulty equipment or parts to the TA as soon as possible.

SAFETY/OPERATIONAL CONSIDERATIONS

1. General

- **Clean the surface of your workbench before beginning your work!**
- ERB 127 is shared by several computer engineering courses.
- Students can only be in the lab when a lab instructor, faculty member, or staff member is present.
- Food and drinks are not allowed in the lab at any time.
- Keep the lab neat and tidy at all times.
- Pick up loose wire or parts when leaving.
- Store backpacks and similar items in the bench pedestal so as not to create a trip hazard.
- Notify the lab instructor or faculty/staff member of any observed safety or operational issue.

2. Electrical hazards

- The 5-volt DC power used in this lab does not pose a danger. However, it is good practice to turn off power when wiring circuits. This provides you with extra protection and also protects the equipment and components.
- The 120-volt AC power used for computers and other equipment is a lethal voltage level, so please plug and unplug power cords with care. Never use equipment with a damaged power cord or plug.

3. Computers

- Do not install or uninstall any software on the lab computers without approval of the faculty or staff member in charge of the lab.
- Do not remove any hardware or cables from lab computers or monitors without approval of the faculty or staff member in charge of the lab.

4. Other lab equipment

- Do not use, handle, or move equipment that is not used in CSE 2441.
- Soldering is not done in CSE 2441. So please don't use the soldering equipment or tables.

LAB RESOURCES

1. **The BitBoard** – The BitBoard accommodates the assembly and implementation of small digital logic circuits. It consists of a solder-less breadboard that can be connected to a DE1 or similar device for power and input/output. See Figure 1. A BitBoard will be checked out to you for use during the semester. ***You will be required to return the BitBoard at the end of the semester.*** More details on The BitBoard can be found on page 4.

2. **Altera DE1 Development and Education Board** – The DE1 accommodates the implementation and test of small to complex digital logic circuits utilizing the Altera Cyclone II field programmable gate array (FPGA) and supporting devices. See Figure 2. The DE1 can also be used to provide power and I/O for The BitBoard. A DE1 will be checked out to you for the semester. ***You will be required to return the DE1 at the end of the semester.***

3. **Parts** – You will be provided a collection of commonly used integrated circuits (ICs) and jumper wire. ***You will be required to return the ICs at the end of the semester.*** Additional parts will be available in the lab as needed. Please see the ***Appendix*** for more details on IC nomenclature and package layout for some of the ICs available in the lab.

4. **Tools** – digital multimeters (DMMs), wire strippers, IC pullers, logic probes, etc. are available in the lab. DMMs are also included in the BitBox lab kit this semester and must be returned at the end of the semester.

5. **Lab PCs –** each lab bench is equipped with a Windows-based personal computer loaded with standard Windows and Office application software. A CAD software tool-set for analyzing and designing field programmable gate arrays (FPGAs) is also installed.

6. **Computer Login –** Login to the lab PCs using your UTA netID and password.

7. **CAD Software** – Intel FPGA (Altera) Quartus II (v13.0sp1) Web-Edition is installed on lab PCs in 126 and 127 ERB. You are ***expected*** to download the software from Intel FPGA to your own laptop or home PC. The web-edition is free. **DO NOT download versions later than v13.0sp1!!** Later versions are not compatible with the DE1 technology. Quartus is Intel FPGA's industry standard computer-aided-design (CAD) software for design capture, simulation, and implementation of digital logic circuits.

8. **Printer –** an HP M651 color laser printer is available in the lab for printing designs and simulation results. The printer is networked to lab machines but is not accessible remotely or wirelessly.

9. **File storage –** User files on the lab PCs are not saved from session to session, so you need to set up a directory on the J: drive, e.g., MyCSE2441Labs, or use a usb drive to store your design files for the semester.

10. **Lab stewardship** – the laboratory equipment, software, and facilities are here for your educational use and are maintained on a regular basis by the CSE Technical Staff. It is your responsibility to treat the equipment with care so that it is available the next time you or someone else needs it.

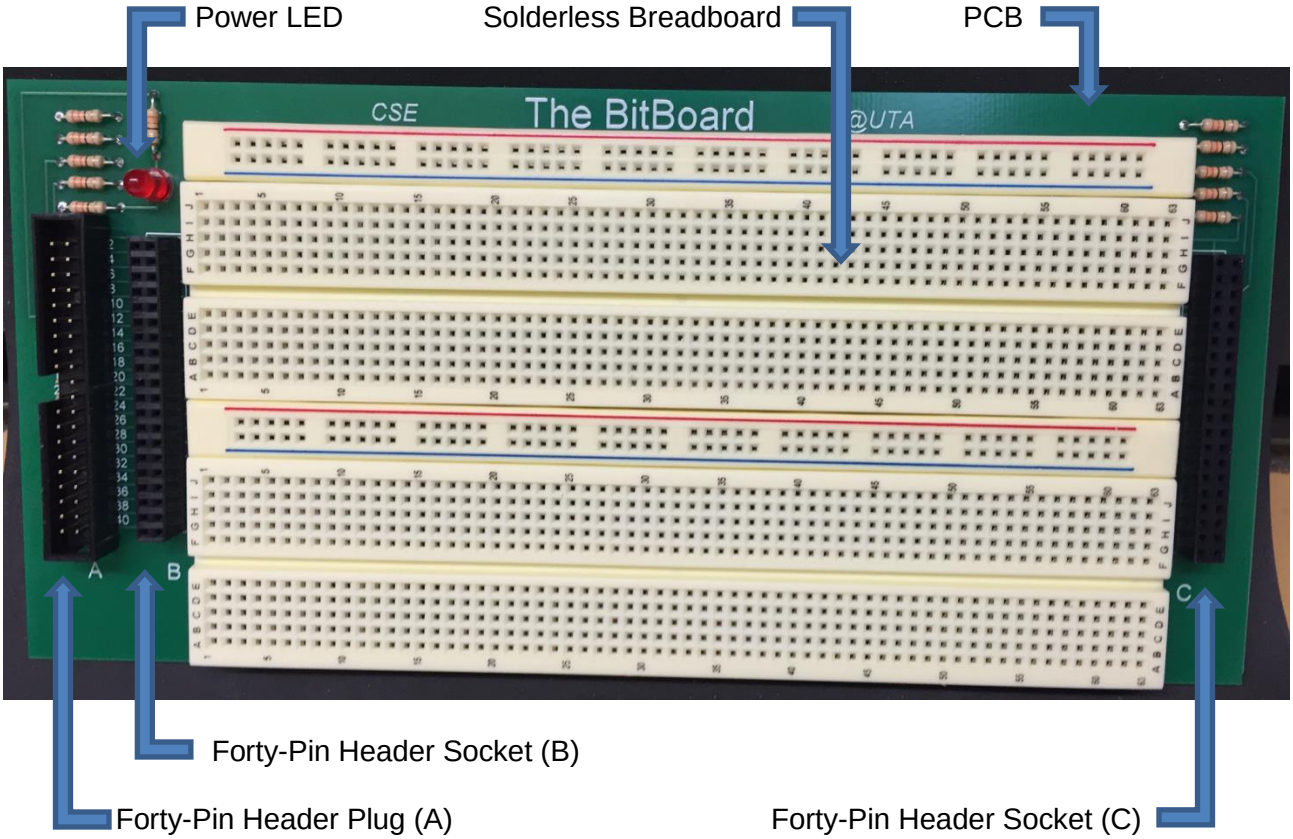


Figure 1 – The BitBoard Layout and Nomenclature.

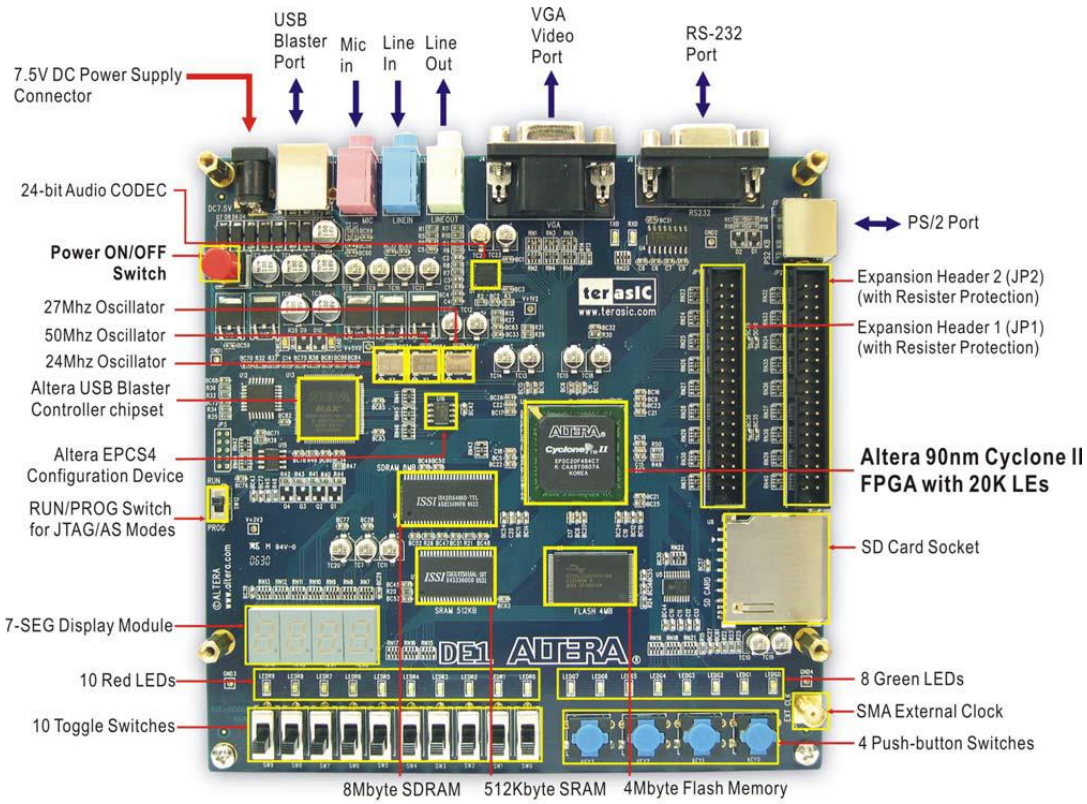


Figure 2. Layout of the DE1 Development and Education Board.

THE BITBOARD© USER'S GUIDE

The BitBoard© is a device that can be used for constructing, testing, and experimenting with small digital logic circuits. It consists of a solderless breadboard, three 40-pin connectors, and a printed circuit board (PCB). Corresponding pins of each connector are permanently interconnected by the PCB. Connector *A* is a 40-pin header plug that can be used to connect The BitBoard to other devices such as an Altera DE1. Connectors *B* and *C* are 40-pin header sockets that can be used to connect signals to the solderless breadboard using jumper wires. Figure 1 shows The BitBoard layout and nomenclature.

An Altera DE1 Development and Education Board, or similar device, can be used to conveniently provide power and input/output for The BitBoard via a ribbon cable connection as shown in Figure 3. DE1s used for this purpose are said to be operating in the *BitBoard mode* and will always enter the mode on power up. DE1s may also be operated in the *FPGA mode* as will be done later in the semester.

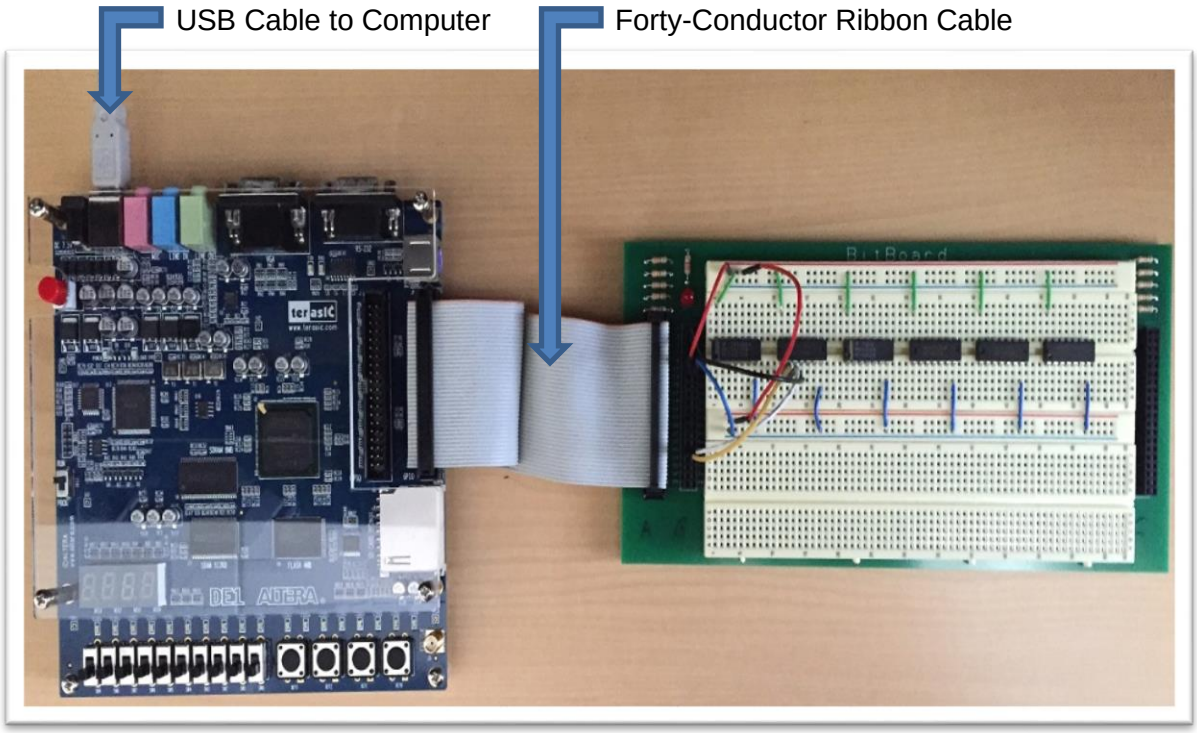


Figure 3 – DE1 Connected to The BitBoard.

Mapping of The BitBoard pins to DE1 switches, LEDs, and seven-segment displays is detailed in Figure 4. Note that some DE1 I/O devices are not accessible from The BitBoard due to pin limitations of the cable and connectors.

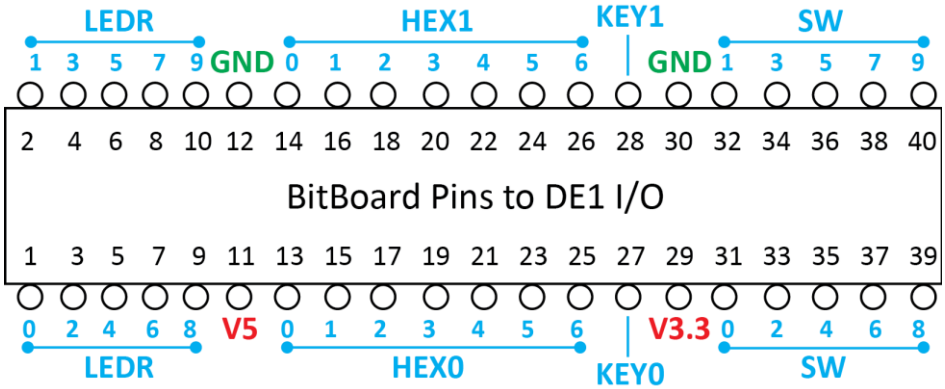


Figure 4 – Pin Mapping of The BitBoard to DE1.

USING SOLDERLESS BREADBOARDS

Solderless breadboards (SB) are used to build electrical and electronic circuits without the need to solder wires and/or make printed circuit boards for interconnecting circuit components. SBs are organized as rows and columns of connection points (CPs) as shown in Figure 5.

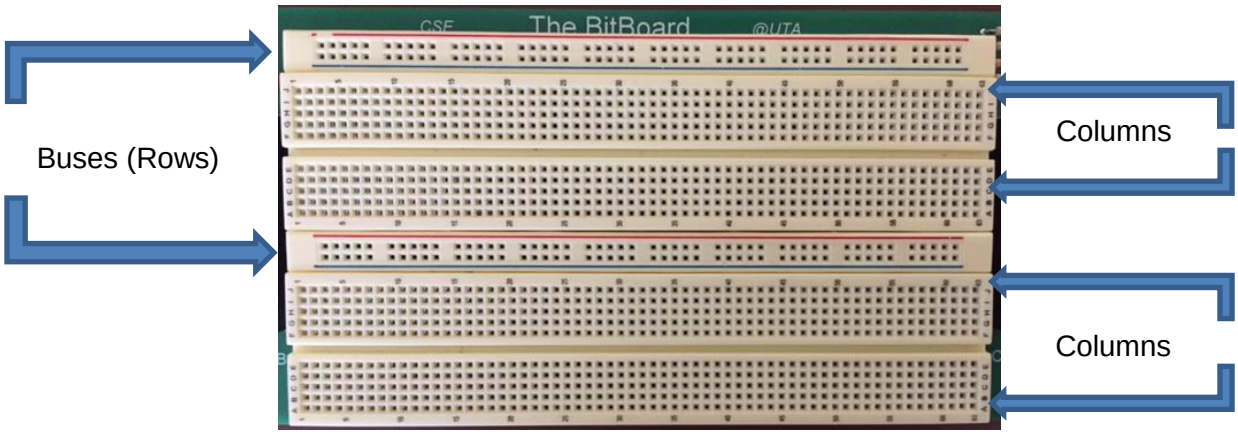


Figure 5 – Solderless Breadboard Organization.

Two horizontal rows of CPs are located at the top of the SB with one labeled red and the other blue. All CPs in one of these rows are electrically common (connected together). These horizontal rows are sometime called buses and can be conveniently used to supply power (red) and ground (blue) connections across the board. Another pair of buses is available about half-way down. Note that these four buses are independent, so the SB provides two red buses and two blue buses.
Each CP in a column in the BitBoard are connected and hence receive the same signal as shown in Figure 5. For Example, Column 1 gets same signal through A, B, C, D, E but not through F, G, H, I, J as it's separated by the gap.

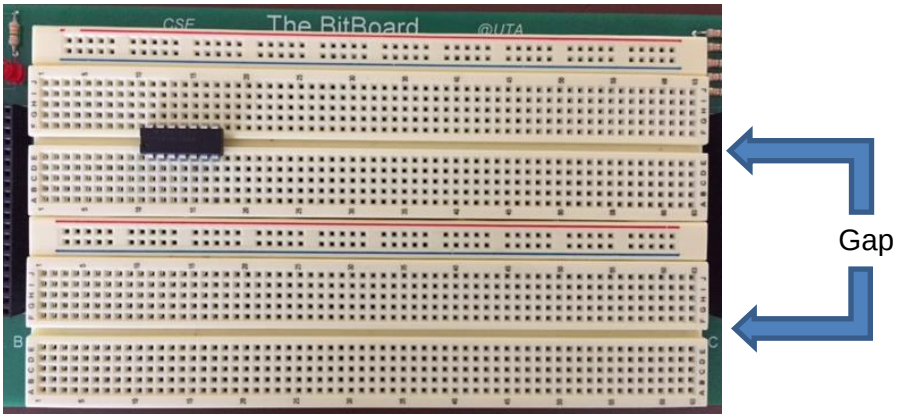


Figure 6 – Chips Placement

The gaps on the Bitboard are used to place the chips with one row of the pins on the top of the gap and the other row of pins below the gap just as shown in Figure 6.

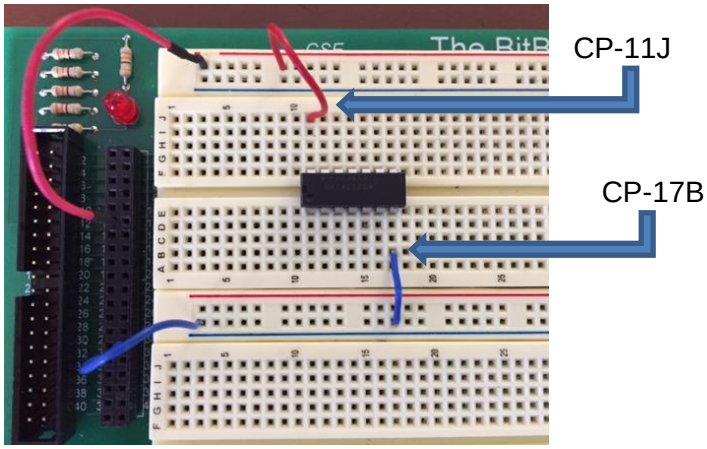


Figure 7 – Making Connections

The small pit on the chip is placed to the left of the image. As shown in Figure 7, the 14th pin (Vcc) is connected to 11F on the BitBoard and further connected to Bitboard Pin 11 using the red wires and the top red bus. The 7th pin (GND) of the chip is connected to 17E on the BitBoard which is further connected to Bitboard Pin 30 using the blue wires and the lower blue bus in Figure 7.

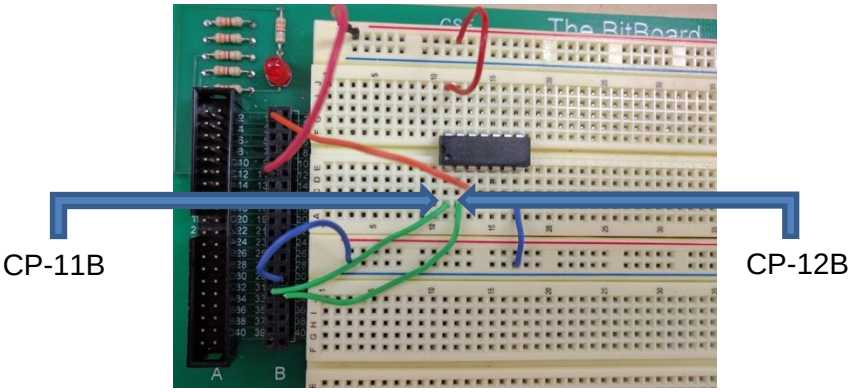


Figure 8 - Connecting Gates to Vcc, GND, and I/O.

The *green* wires in Figure 8 are the 2 inputs to a NAND gate where the 1st and 2nd pins of the IC are connected to 11E and 12E, respectively, which in turn are connected to the Bitboard Pin 31 and Pin 32 which are SW0 and SW1, respectively. The output pin is the 3rd pin of IC which is connected to 13E which is connected using the orange wire to Bitboard Pin 1 which is LEDR0.

DIGITAL MULTIMETER (DMM) USER'S GUIDE

Digital Multimeters (DMMs) can be used to measure voltage, current, resistance, and other characteristics of electrical circuits and devices. Figure 9 shows the DT-182 DMM that will be used in the CSE 2441 logic lab. Some of you may have a DT830D DMM in your kit. It works similarly to the DT-182. Manuals for both are posted under Reference Materials on Canvas.

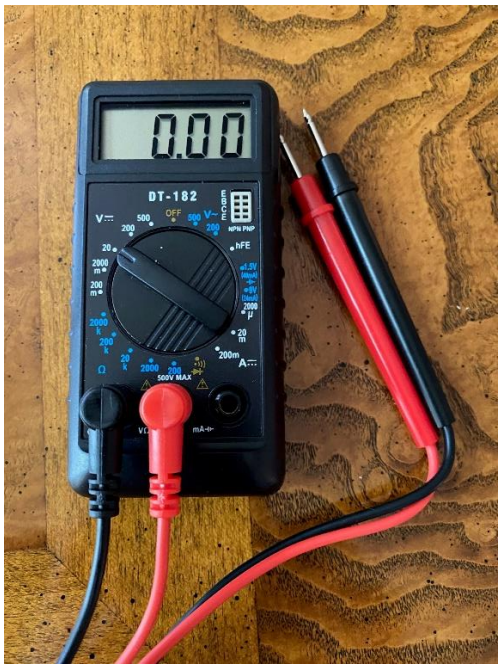


Figure 9 – DT-182 Digital Multimeter (DMM)

Measuring DC Voltage – First, select the smallest voltage range that is larger than the voltage to be measured. This is typically 20-volts for logic circuits and devices as shown above. Next, connect the *black test lead* to *ground* of the circuit or device to be measured. Connect the *red lead* to the terminal to be measured. The voltage of the terminal, relative to ground, will be shown on the DMM display.

Measuring AC Voltage – Select the appropriate range (500-volts or 200-volts)**.** Connect the test leads as described above. The voltage read will be RMS.

Measuring DC Current – Select the appropriate current range and connect the test leads as above. When measuring DC current, the red lead must be connected to the rightmost terminal..

Measuring Resistance – Select the appropriate range and connect the test leads as described previously.

The DMM can also be used to test diodes and transistors and as a square-wave generator. However, these features will not be described in this guide.

POWER OFF – Be sure to place the selector switch in the **OFF** position when not using the DMM in order to preserve battery life.

ASSIGNMENT

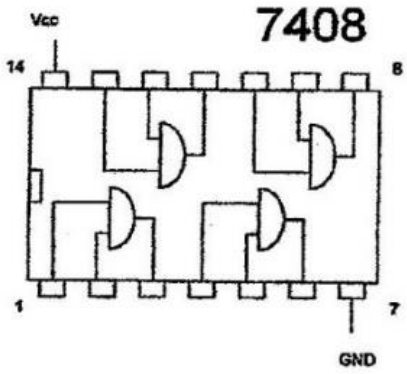
The purpose of this assignment is to familiarize you with the basic features of The BitBoard and the DE1. You will also study logical and electrical characteristics of basic logic gates (AND, OR, NOT, NAND, NOR, and XOR) by experimentally deriving their truth tables.

Use DE1 switch SW1 for input A, SW0 for input B and LEDR0 for output Y in your experiments. Here's how to use and interpret the switches and LEDs.

SW1 (Input A): UP = logic 1, DOWN = logic 0
SW0 (Input B): UP = logic 1, DOWN = logic 0
LEDR0 (Output Y): ON = logic 1, OFF = logic 0

Note that each IC chip contains multiple gates. However, for this exercise it's only necessary to use one gate per chip. Figure 8 shows a typical wiring layout for this experiment. Chip pinouts for this and other chips are shown in the Appendix.

1. **Experimentally derive the truth table of an AND gate**. An SN74xx08 2-Input Quad AND chip has been pre-inserted and pre-wired on your BitBoard as shown in Figure 8. The chip contains four 2-input AND gates. Hence, the nomenclature QUAD! You'll be using only one gate in this experiment (input pins 1 and 2, output pin 3). Refer to pinout diagram below.



1.1 Connect the DE1 to the BitBoard using the flat cable as shown in Figure 3.

1.2 Power on the DE1. The red LED on the BitBoard should light up.

1.3 Apply inputs (*A* and *B*) 00, 01, 10, and 11 to the AND gate and record the results (*Y*) in the following table.

***A* (SW1)**	***B* (SW0)**	***Y* (LEDR0)**	V_A	V_B	V_Y
0	0				
0	1				
1	0				
1	1				

1.4 Take pictures of your set up with AB=01 and AB=11.

1.5 What is the logic equation for *Y* in terms of *A* and *B*? Y = ?

1.6 Now use the DMM to read the voltages for inputs *A* and *B* and output *Y* and record your readings in the above table in columns V_A, V_B, and V_Y.

1.7 Use the DMM to read the voltages of *Vcc* (pin 14) and *GND* (pin 7). Record your results. Vcc = ? GND = ?

2. **Experimentally derive the truth table of an OR gate**. Replace the SN74xx08 chip with an SN74xx32 2-input Quad OR gate. Repeat the steps from 1 to complete the table and questions below. ***Note: the pinouts for the SN74xx08 and the SN74xx32 are the same, so no wiring has to be changed.***

***A* (SW1)**	***B* (SW0)**	***Y* (LEDR0)**	V_A	V_B	V_Y
0	0				
0	1				
1	0				
1	1				

3. **Experimentally derive the truth table of a NAND gate**. Replace the SN74xx32 chip with an SN74xx00 2-input Quad NAND gate. Repeat the steps from 1 to complete the table and questions below. *Again the pinouts are the same, so no wiring has to be changed.*

***A* (SW1)**	***B* (SW0)**	***Y* (LEDR0)**	V_A	V_B	V_Y
0	0				
0	1				
1	0				
1	1				

4. **Experimentally derive the truth table of an XOR gate**. Replace the SN74xx00 chip with an SN74xx86 2-input Quad XOR gate. Repeat the steps from 1 to complete the table and questions below. *Again the pinouts are the same, so no wiring has to be changed.*

***A* (SW1)**	***B* (SW0)**	***Y* (LEDR0)**	V_A	V_B	V_Y
0	0				
0	1				
1	0				
1	1				

5. **Experimentally derive the truth table of a NOR gate**. Replace the SN74xx86 chip with an SN74xx02 2-input Quad NOR gate. Repeat the steps from 1 to complete the table and questions below. ***Note: The pinouts have changed, so the wiring has to be changed. Please see the pinout diagram in the Appendix.***

***A* (SW1)**	***B* (SW0)**	***Y* (LEDR0)**	V_A	V_B	V_Y
0	0				
0	1				
1	0				
1	1				

6. **Experimentally derive the truth table of a NOT gate**. Replace the SN74xx02 chip with an SN74xx04 Hex Inverter. Repeat the steps from 1 to complete the table and questions below. ***Note:*** A ***NOT gate is a single-input device sometimes called an Inverter. So the pinouts have changed, and the wiring has to be changed. Please see the pinout diagram in the Appendix.***

A	***Y***	V_A	V_Y
0			
1			

Y = ?
Vcc = ?
GND = ?

LABORATORY REPORT REQUIREMENT (Due September 4, 2020, 11:59 PM, on Canvas)

1. Assignment number and name
2. Student name and ID
3. Student Email
4. Date and time submitted
5. Assignment purpose
6. Circuit diagrams
7. Truth tables with I/O voltages as experimentally observed
8. Vcc and GND voltages as experimentally observed
9. Logic equations for each gate studied
10. Photos with captions

APPENDIX

A (Very) Brief Introduction to Small, Medium, and Large Scale Digital Integrated Circuits

CSE 2441 Fall 2020

Introduction

Small scale (SSI), medium scale (MSI), and large scale (LSI) integrated circuits (ICs) have been a mainstay of digital logic circuit implementation for more than forty years. They are still in use for educational purposes and for small to medium sized industrial projects that will be constructed in small quantities or for special purpose applications. ICs are interconnected using wires or printed circuit boards in order to realize the desired functionality. Circuits constructed of SSI, MSI, and LSI ICs are generally referred to as *fixed logic* since the functions they realize cannot be changed without physically rebuilding the circuit. So design changes are difficult, expensive, or impossible.

The advent of very large scale integrated (VLSI) circuits led to the development of *programmable and customizable logic devices* which were introduced about twenty-five years ago and have grown in popularity because of their cost effectiveness, versatility, ease of design change, and the availability of computer-aided-design (CAD) software to support the design process. Programmable devices also enable the design and implementation of much larger and more complex systems. Currently, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), and microcontrollers are the most commonly used of these devices.

Integrated Circuit Technologies

Various electronic technologies have been employed to implement digital integrated circuits. Bi-polar transistor-transistor logic (TTL) and complementary metal oxide semiconductors (CMOS) have been the most dominate. The SSI and MSI devices you'll be using this semester are either TTL or TTL-compatible CMOS technology and the Cyclone II FPGA used in the DE1 is CMOS.

Typical voltage parameters for SSI and MSI logic devices are as follows.

Supply voltage (VCC) – 5 volts (4.75 to 5.25)
High-level input voltage – 2 volts minimum
Low-level input voltage – 0.8 volts maximum
High-level output voltage – 2.7 volts minimum
Low-level output voltage – 0.5 maximum

IC Packaging

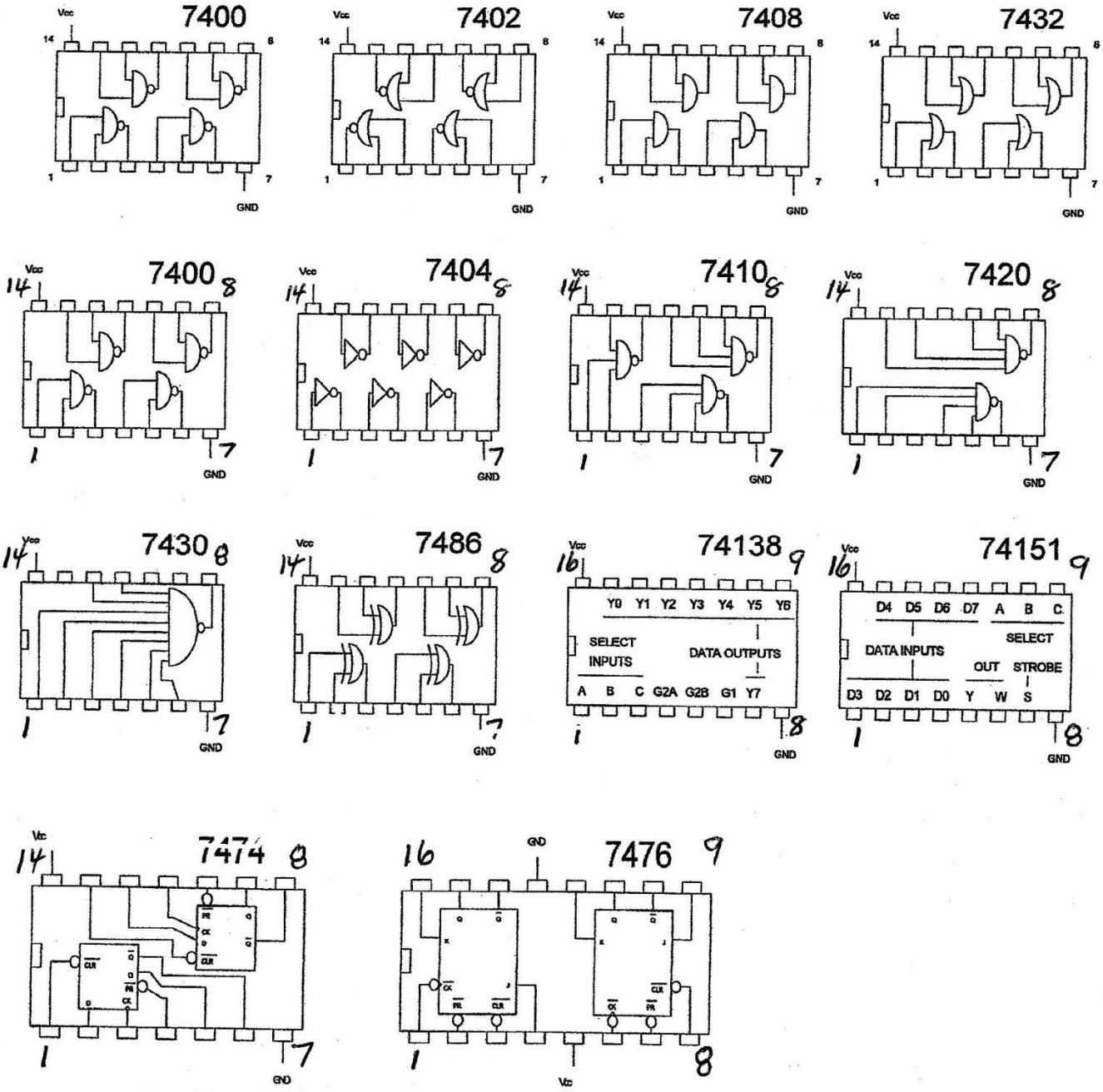
SSI and MSI devices generally employ dual in-line packaging (DIP) with 14, 16, or 18 pins. LSI and VLSI are generally found in square packages with pins on all four sides in numbers that reflect the complexity of the IC. The Cyclone II FPGA used in the DE1 is a 484-pin package.

Note how SSI and MSI integrated circuit (ICs) pins are numbered. One end of the IC is marked with a small indentation in its plastic case. The indentation is indicated by a small rectangle in the drawings below. The pins are numbered in the counter-clockwise direction starting in the corner below the indentation. An alternate marking for ICs is a small circular dot right next to pin 1. You may encounter either type of markings on the ICs used in this lab.

The numbers given to the ICs (7400, 7402, 7408 & 7432) are generic numbers. For the real ICs you will be using the part numbers have additional letters which vary from one manufacturer to another.

A typical IC might be marked SN7400, or SN74LS00, or SN74HC00. Many combinations exist, and often indicate special properties of an IC, but for the labs this semester you should be concerned only with the generic types.

Package Layout and Pin Outs of Commonly Used SSI and MSI Digital Integrated Circuits



REFERENCE SHEET