Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2020

Lab Number 11 – RAM Tester

Due November 16, 2020, 11:59 PM

Note: This lab is performed on the DE1 FPGA.

CSE 2441 **LABORATORY ASSIGNMENT 11** **FALL 2020**

RAM TESTER

(100 POINTS)

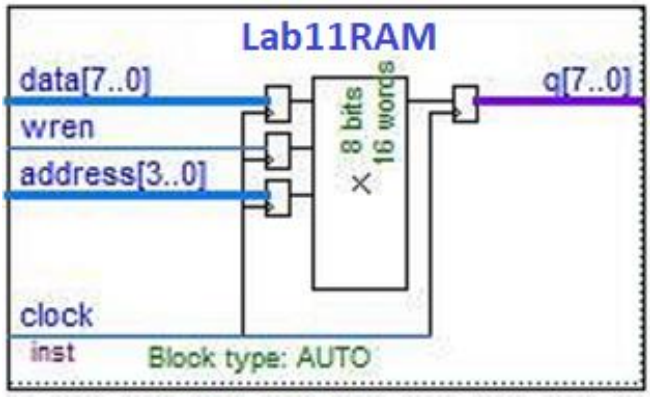
PURPOSE/OUTCOMES

To study the operation and interfacing of a basic random access memory (RAM). From this exercise, you will learn how to read from and write to a (RAM) using a simple test set up and procedure. You will also learn how to interconnect components using buses.

RANDOM ACCESS MEMORY (RAM) BACKGROUND

RAM is used in digital computers to store program instructions and data. A diagram of a Quartus II RAM model is shown below. The storage array is organized as 2^m, n-bit words. Each word is identified by a unique m-bit address. For Lab11RAM, m = 4 and n = 8. There are two basic RAM operations, READ and WRITE. READ means to read the contents of a specific word of the memory array and place the value in the Memory Data Output (MDO) register. The word to be read is selected by placing its address in the Memory Address Register (MAR). WRITE means to write the contents of the Memory Data Input (MDI) register in to the word of memory specified by the address stored in the MAR. There are two signals needed to control a RAM, *clock* and *wren*. A READ is specified by *clock* = 1 and *wren* = 0. WRITE is specified by *clock* = *wren* = 1. *clock* = 0 means no operation. This is summarized in the following table.

A series of steps is required for each READ or WRITE operation. These are typically called Memory Cycles and are detailed below for the Quartus II LAB11ram model.



clock	*wren*	*Operation*
0	0	Idle
0	1	Idle
1	0	READ
1	1	WRITE

READ Cycle

address bus ← Address
wren ← 0
clock ← 0-1 (posedge)
MAR ← address bus
clock ← 0-1 (posedge)
q ← (MemoryWord)

Note: *q and MDO are synomimous.

WRITE Cycle

address bus ← Address
wren ← 1
data bus ← DataIn
clock ← 0-1 (posedge)
MAR ← address bus
MDI ← data bus
clock ← 0-1 (posedge)
MemoryWord ← (MDI)
wren ← 0

RAM LAB EXERCISE

1. Capture the circuit shown on the next page with Quartus II and realize on the DE1. The Lab11RAM design files can be found on Canvas under Laboratory Exercises. Unzip the folder and add files *Lab11RAM.v* and *Lab11RAM.bsf* to your project. Refer to class notes for more details on Quartus II RAM modules.
2. Read and record the initial contents of each memory location.
3. Write all 0's in to the RAM and read them back out to verify that the writes actually worked.
4. Write all 1's in to the RAM and read them back out.
5. Write a 1-0-1-0-1-0-1-0 pattern in to even addresses of the memory and 0-1-0-1-0-1-0-1 in to odd address. Read them back out to verify that the writes worked.

OPERATING PROCEDURE

Read Operation

1. *Press and Release* Key0 to *Clear* the Address Generator – this places address 0x0 on the *address bus.*
2. *Press and Release* Key1 – this loads the address in to the *MAR* of the RAM.
3. *Press and Release* Key1 again – the *Press* loads the data read in to the *MDO* of the RAM and on to the *Dout* bus. The *Release* advances the Address Generator to the next address.
4. Repeat steps 2 and 3 as necessary to read the remaining RAM locations.

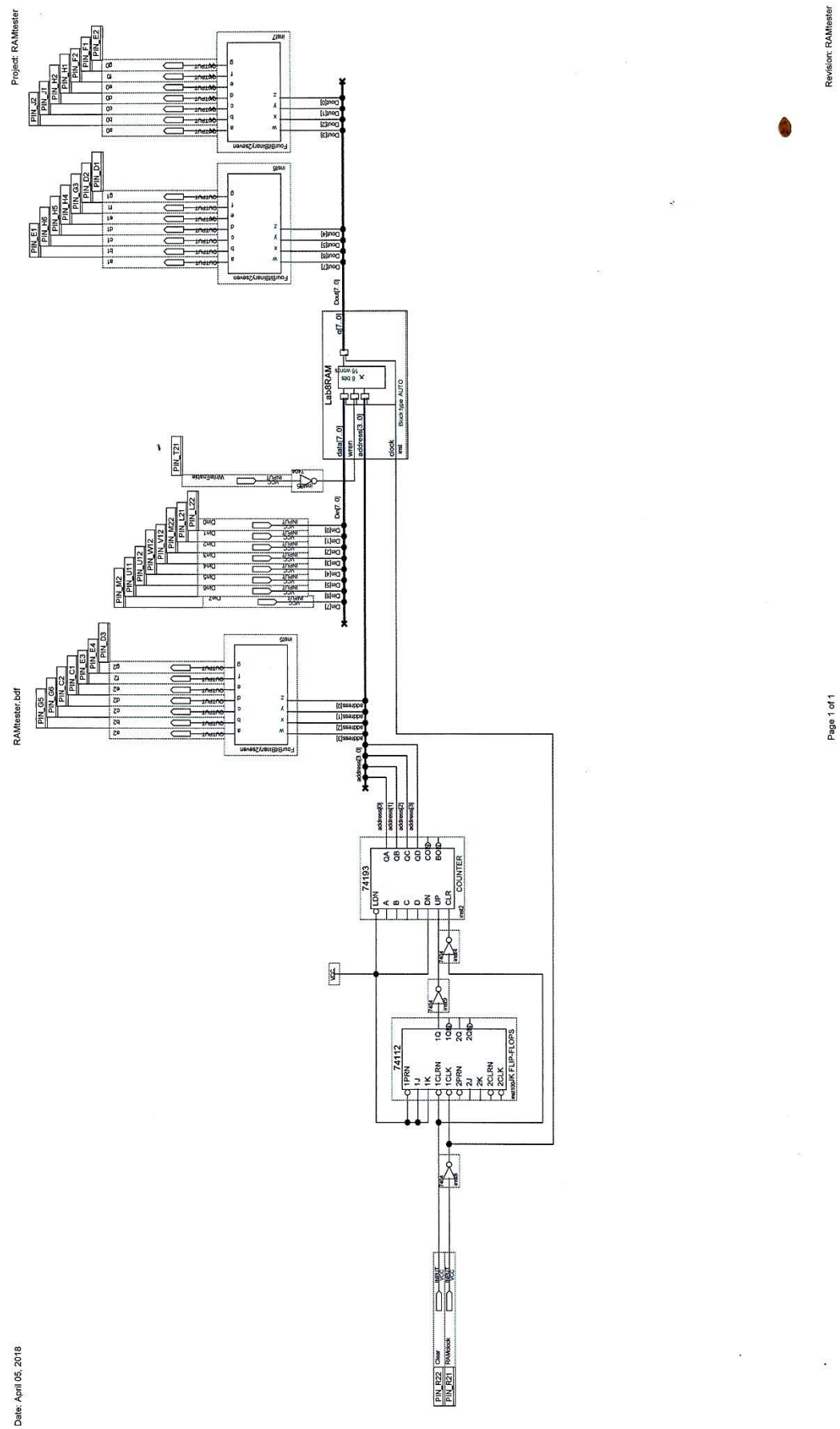
Write Operation

1. *Press and Release* Key0 to *Clear* the Address Generator – this places address 0x0 on the *address bus.*
2. Apply data to the *Din* bus using switches SW7 to SW0.
3. *Press and hold* Key3 to enable Write.
4. *Press and Release* Key1 twice while continuing to hold Key3. This will store the value on the *Din* bus in to the addressed RAM location. This will also advance the Address Generator to the next address.
5. Repeat steps 2, 3, and 4 as necessary to write the remaining RAM locations.

REPORT REQUIREMENTS

1. Cover sheet (as shown on this assignment)
2. Lab purpose
3. Schematic of your circuit (screen shot)
4. Record of the original RAM contents
5. Record of writing all 0's to, and reading from, RAM (*)
6. Record of writing all 1's to, and reading from, RAM (*)
7. Record of writing 1-0-1-0-1-0-1-0 and 0-1-0-1-0-1-0-1 to, and reading from, RAM (*)

* Document with photos or videos


Project: RAMtester
RAMtester.bdf
Revision: RAMtester
Date: April 05, 2018
Page 1 of 1
Lab8RAM
74193
74112
COUNTER
FLIP-FLOPS
PIN_R22
PIN_R21
Clear
RAMclock
writeEnable
PIN_T21