Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2020

Lab Number 6 – Seven-Segment Displays and Decoders

100 Points

(Due October 13, 2020, 11:59 PM)

This is a DE1 FPGA Lab.

CSE 2441 **LABORATORY SESSION 6** **FALL 2020**

SEVEN-SEGMENT DISPLAYS AND DECODERS

(100 POINTS)

PURPOSE and OUTCOME – The purpose of this assignment is to give you experience designing and realizing decoders for displaying binary and decimal numbers on the DE1's seven-segment displays. You will **design your decoders using Verilog** and realize the designs by programming the Cyclone II FPGA found on the DE1.

BACKGROUND

Seven-segment LEDs have been a widely used display device for many decades and continue to be used in myriad applications. A single seven-segment display, see Figure 1, can display decimal digits from *0 through 9* and can also be used to display hexadecimal digits using stylized letters *A, b, C, d, E*,and *F* to represent the digits *A through F*. Two-digit decimal numbers may be displayed by using two seven-segment devices, see Figure 2. Decoders are needed to convert binary numbers or BCD to seven-segment code or to a two-digit seven segment code.

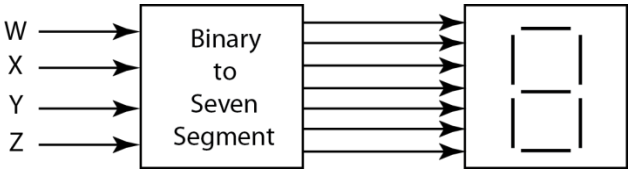

Figure 1

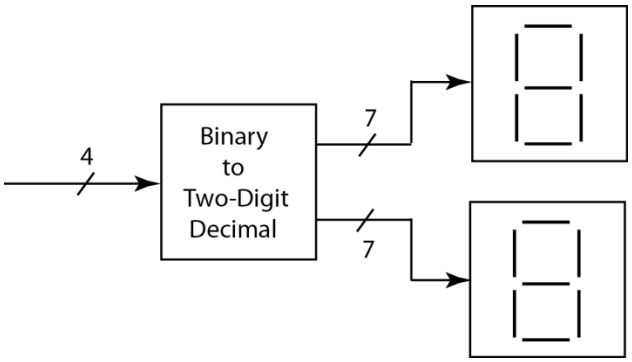

Figure 2

The DE1 seven-segment displays are ***active-low***, so please keep this in mind when designing your decoders. Also, the DE1 designers chose to name the displays *HEX3, HEX2, HEX1, and HEX0*, from left to right, and label the segments *0,1,2,3,4,5,6* clockwise from the top.

DESIGN ASSIGNMENT – Use Verilog for your decoder designs. Save your designs as symbol files for use later in the semester.

1. Design a decoder that converts 4-bit binary to seven-segment code for displaying on a single seven-segment display in hexadecimal.
2. Next, design a decoder that converts four-bit binary numbers to seven-segment codes for displaying in decimal on two seven-segment displays. The most significant digit should be blank when not needed.
3. Finally, design a decoder that converts 4-bit two's complement numbers to seven-segment codes for the decimal sign and magnitude of the number on two seven-segment displays. The sign should be displayed as "blank" for positive numbers and "-" for negative numbers.

LAB ASSIGNMENT

1. Realize your 4-bit binary to seven-segment decoder on the DE1 and demonstrate that it properly displays the binary codes 0000 through 1111 on HEX0. Use the following pin assignments.

   W → SW3 X → SW2 Y → SW1 Z → SW0
   a → HEX0(0) b → HEX0(1) c → HEX0(2) … f → HEX0(5) g → HEX0(6)

2. Realize your second 4-bit binary to seven-segment decoder on the DE1 and demonstrate that it properly displays the binary numbers 0000 through 1111 in decimal on HEX1 and HEX0. Use the following pin assignments.

   W → SW3 X → SW2 Y → SW1 Z → SW0
   a_1 → HEX1(0) b_1 → HEX1(1) c_1 → HEX1(2) … f_1 → HEX1(5) g_1 → HEX1(6)
   a_0 → HEX0(0) b_0 → HEX0(1) c_0 → HEX0(2) … f_0 → HEX0(5) g_0 → HEX0(6)

3. Realize your 4-bit two's complement to seven-segment decoder on the DE1 and demonstrate that it properly displays the decimal sign-magnitude of the numbers 0000 through 1111 on HEX1 and HEX0. Use the same pin assignments as in part 2.

REPORT REQUIREMENTS

1. Cover sheet (as shown on this assignment)
2. Lab purpose
3. Verilog code for your 4-bit binary to seven-segment decoder
4. Pictures of the above decoder and 7-segment displaying 0000, 0011, 0110, 1001, 1100, 1111
5. Verilog code for your 4-bit binary to two-digit seven-segment decoder
6. Pictures of the above decoder and two-digit, 7-segment displaying 0000, 0011, 0110, 1001, 1100, 1111
7. Verilog code for your 4-bit 2's-complement to sign-magnitude decoder
8. Pictures of the above decoder and 7-segment displaying 0000, 0011, 0110, 1001, 1100, 1111