Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2020

Lab Number 7 – A Basic Arithmetic Logic Unit (ALU)

100 Points

Due October 19, 2020, 11:59 PM

This is a DE1 FPGA Lab.

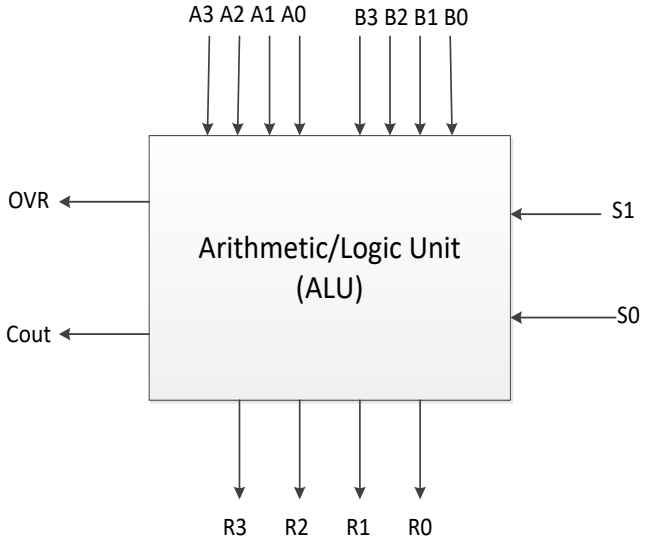
CSE 2441 **LABORATORY SESSION 7** **FALL 2020**

A BASIC ARITHMETIC LOGIC UNIT (ALU)

(100 POINTS)

PURPOSE/OUTCOMES: To design, implement (DE1 FPGA), and test a basic four-bit, four-function ALU. By successfully completing this laboratory, you will have demonstrated an ability to design and implement an ALU.

BACKGROUND: In this lab you will design a basic four-bit ALU that can perform addition, subtraction, logical AND, and logical XOR as illustrated in the diagram below. The operation to be performed is specified using control inputs S1 and S0 as defined in the table. A two's complement number system will be used to represent signed numbers. The adder/subtractor circuit that you designed in previous labs will be used as a component in the ALU. You will need to add the AND and XOR functions, OVR logic and control logic to the adder/subtractor to complete the ALU.



S1	*S0*	*Operation*
0	0	Add (A + B)
0	1	Subtract (A - B)
1	0	Logical AND (A·B)
1	1	Logical XOR (A ⊕ B)

DESIGN REQUIREMENT Design the ALU specified above. Capture and verify your design using Quartus II. Create a block symbol file for future use.

LAB REQUIREMENT Realize your design on the DE1. Record your results in the table below. Use the pin assignments given on the following page. **Also, display *R* as a signed decimal number on HEX1 and HEX0.**

A	*B*	*R = A + B*	*OVR*	*Cout(C4)*	*R = A - B*	*OVR*	*Cout(C4)*	*A·B*	*A ⊕ B*
0110	0001								
0110	0010								
0010	1001								
1101	1111								
1100	1001								
1010	1110								
0110	1111								
1001	0111								

DE1 Pin Assignments

B0 → SW0	B0out → LEDR0
B1 → SW1	B1out → LEDR1
B2 → SW2	B2out → LEDR2
B3 → SW3	B3out → LEDR3
A0 → SW4	A0out → LEDR4
A1 → SW5	A1out → LEDR5
A2 → SW6	A2out → LEDR6
A3 → SW7	A3out → LEDR7
S0 → SW8	S0out → LEDR8
S1 → SW9	S1out → LEDR9

R0 → LEDG0
R1 → LEDG1
R2 → LEDG2
R3 → LEDG3

Cout → LEDG4
OVR → LEDG5

REPORT REQUIREMENT

1. Cover sheet (as shown on this assignment)
2. Lab purpose
3. Screen shot of your ALU circuit design
4. Screen shot of your ALU block symbol file diagram
5. Your table of experimental test results
6. Pictures of your test results for 0110 +/- 0010, 0010 +/- 1001, 1010 +/- 1110, 1001 +/- 0111