Name: _____ ID# _____

Date Submitted: _____ Lab Section # _____

CSE 2441 – Introduction to Digital Logic Fall Semester 2020

Lab Number 12 – TRISC Processor Control Unit

Due November 30, 2020, 11:59 PM

Note: This lab is performed on the DE1 FPGA.

CSE 2441 **LABORATORY ASSIGNMENT 12** **FALL 2020**

TRISC PROCESSOR CONTROL UNIT

(100 POINTS)

PURPOSE/OUTCOMES

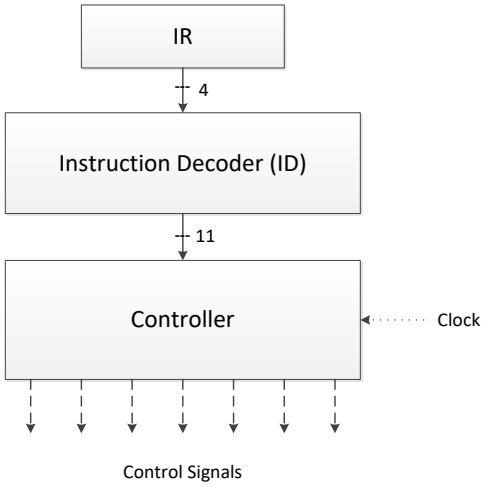
To design, implement on the DE1, and test a control unit for a subset (INC, CLR, JMP, LDA, STA, and ADD) of the Tiny Reduced Instruction Set Computer (TRISC) instruction set. By successfully completing this assignment, you will have demonstrated an ability to design a simple FSM-based controller.

BACKGROUND

You have been designing and implementing various components, e.g., ALU, PC, ACC, IR, and ID, for the Tiny Reduced Instruction Set Computer (TRISC) over the past several laboratory exercises. In this lab, you will design a FSM to fetch and execute the INC, CLR, JMP, LDA, STA, and ADD instructions. You will then integrate the FSM with the ID you designed in HW #8 to realize the TRISC control unit. Please refer to the class notes for more details on TRISC.

DESIGN REQUIREMENTS

1. Design a FSM controller for generating the sequence of control signals necessary to fetch and execute the INC, CLR, JMP, LDA, STA, and ADD instructions. Use Verilog for your design.
2. Integrate your ID design from HW #8 with the FSM controller to realize the TRISC control unit.



LAB REQUIREMENTS

1. Install your control unit (ID + FSM controller) on the DE1.
2. Use slide switches SW3, SW2, SW1, and SW0 to enter opcodes. Use Key1 for the SystemClock and Key0 for SystemReset.
3. Use the following assignments for displaying control signals.

   C0:LEDG0, C1:LEDG1, C2:LEDG2, C3:LEDG3, C4:LEDG4, C5:LEDG5, C7:LEDG6,

   C8:LEDG7, C9:LEDR0, C10:LEDR1, C11:LEDR2, C12:LEDR3, C13:LEDR4, C14:LEDR5
4. Demonstrate that your control unit generates the correct sequence of control signals for each of the six instructions – INC, CLR, JMP, LDA, STA, and ADD.

REPORT REQUIREMENTS

1. Cover sheet (as shown on this assignment)
2. Lab purpose
3. Instruction Decoder (ID) circuit diagram or Verilog code. (screen shot)
4. FSM controller Verilog code. (screen shot)
5. Control unit block diagram or Verilog code. (screen shot)
6. Records of control sequences produced for each instruction.
7. Visual evidence of #6. (photos or videos)