CE233(CAD), Lecture 2:

Introduction to PLDs

Mehdi Modarressi
Department of Electrical and Computer Engineering,
University of Tehran

World of integrated circuits

TTL Gates

Full-Custom Design

Standard Cell Design

User Programmable

SPLD

CPLD

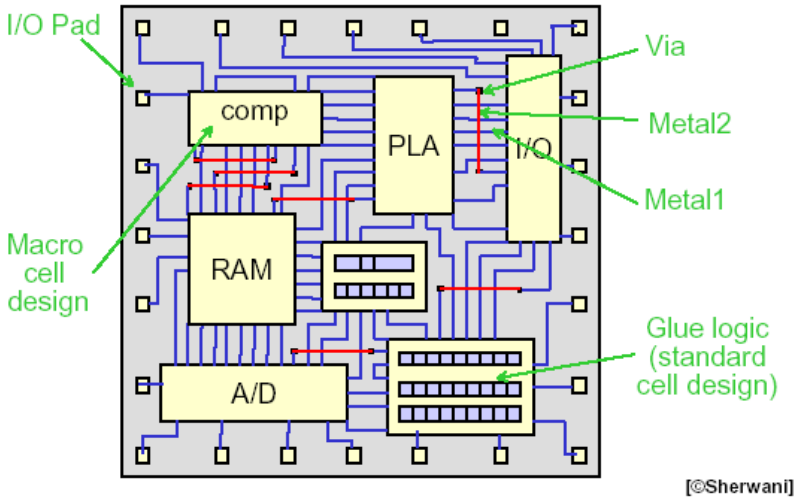
FPGA

Full-custom ICs

- General-purpose processors
  - Example: Intel and AMD microprocessors
- Application-specific processors
  - Example: Embedded processor of a digital camera
- Requires establishing a fabrication line
  - You will learn more about this in the VLSI Design course

Full-custom design

- Very efficient in terms of performance, but:
  - Long design and manufacturing cycles
  - Very expensive, sometimes several million dollars
  - Once manufactured, the logic can't simply be altered
    - large penalty if a bug is found

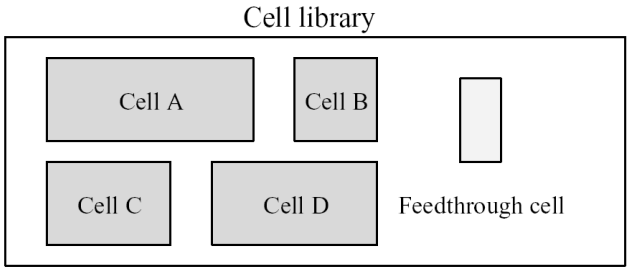


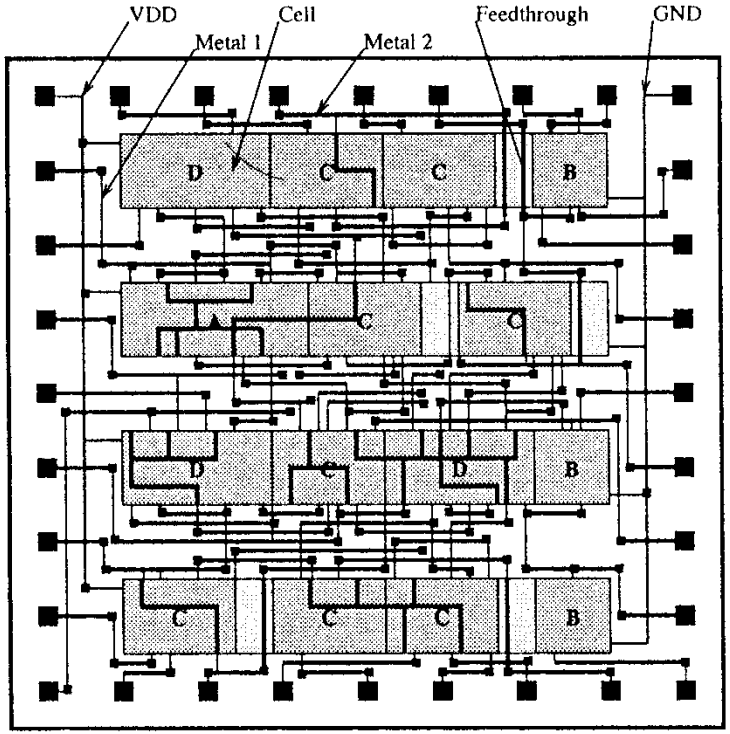
Full-custom design

- Requires establishing a fabrication (production) line
- Suitable for large volume production
- Example: General-purpose processors
  - Intel and AMD microprocessors

Standard-cell design

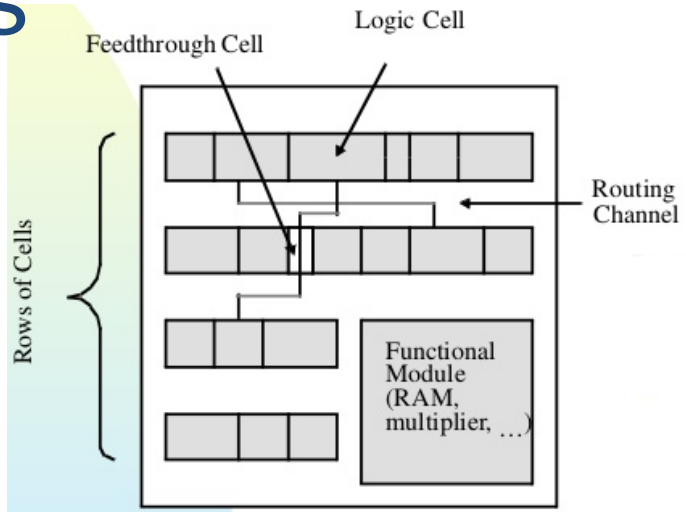
- Still needs fabrication line, but the logic are selected from a library



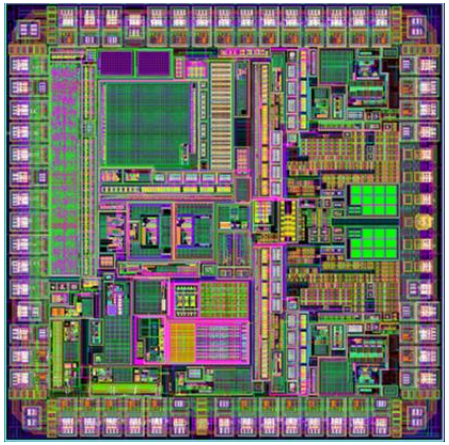


Semi-custom designs

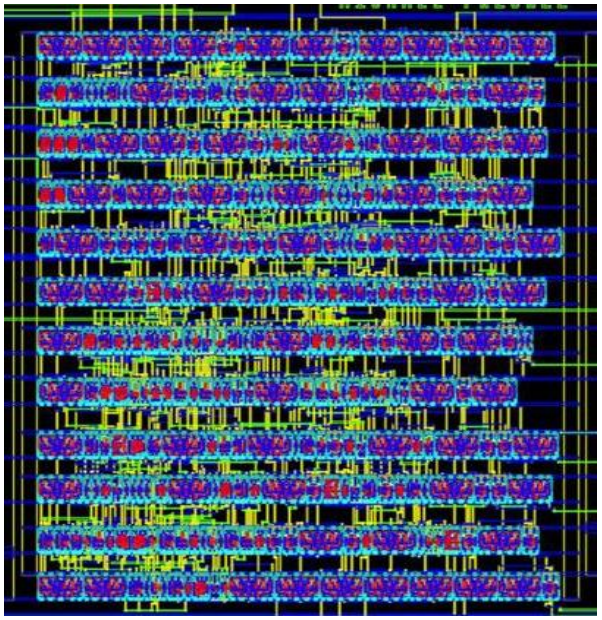
- Designers use standard libraries and pre-defined chip layouts to ease implementation
  - To reduce design time/effort



Full custom

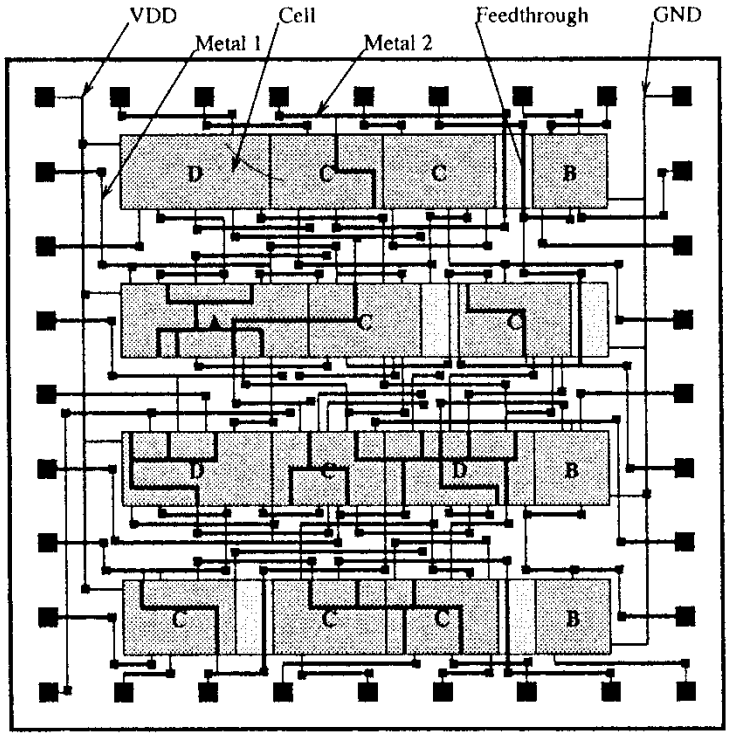


Standard cell

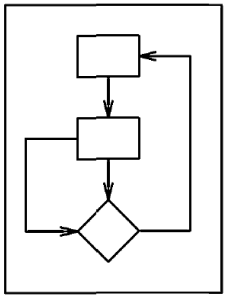


Standard-cell design

- Cell library
- Cell: a transistor level implementation of a function (e.g. mux, register, adder,…) in a rectangular shape of the same height
- Cells placed in rows and space between rows are used for routing



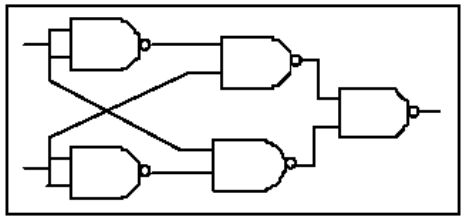
VLSI design process

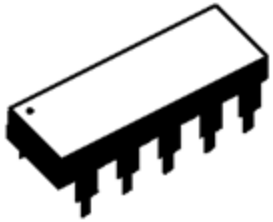


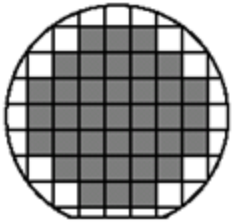
- System specification
- Functional design
- Logic design
- Circuit design
- Physical design
- Fabrication and packaging

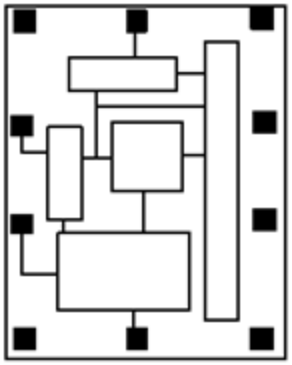
→ Test or verification after each step

x = (AB*CD)+(A+D)+(A(B+C))
Y=(A(B+C)+AC+D+A(BC+D))



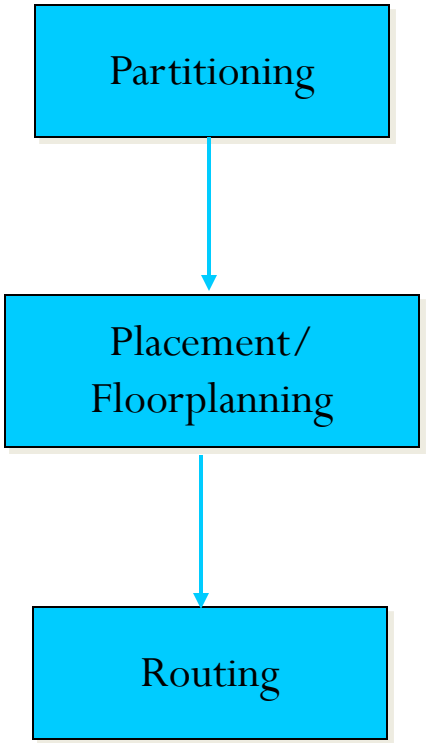


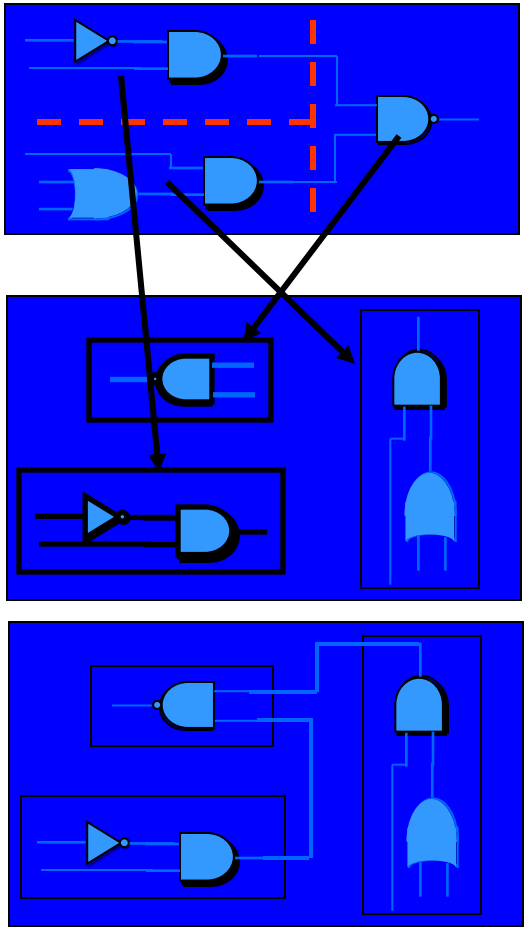




Picture Source: CEIT483 at Amirkabir U. ofTech., Lecture 2, by Dr Saheb-zamani, with modifications

Physical design in ASICs





Break the circuit up into smaller segments

Place the segments on the chip

Layout out the wire paths

Picture Source: CEIT483 at Amirkabir U. ofTech., Lecture 2, by Dr Saheb-zamani, with modifications

IC fabrication process

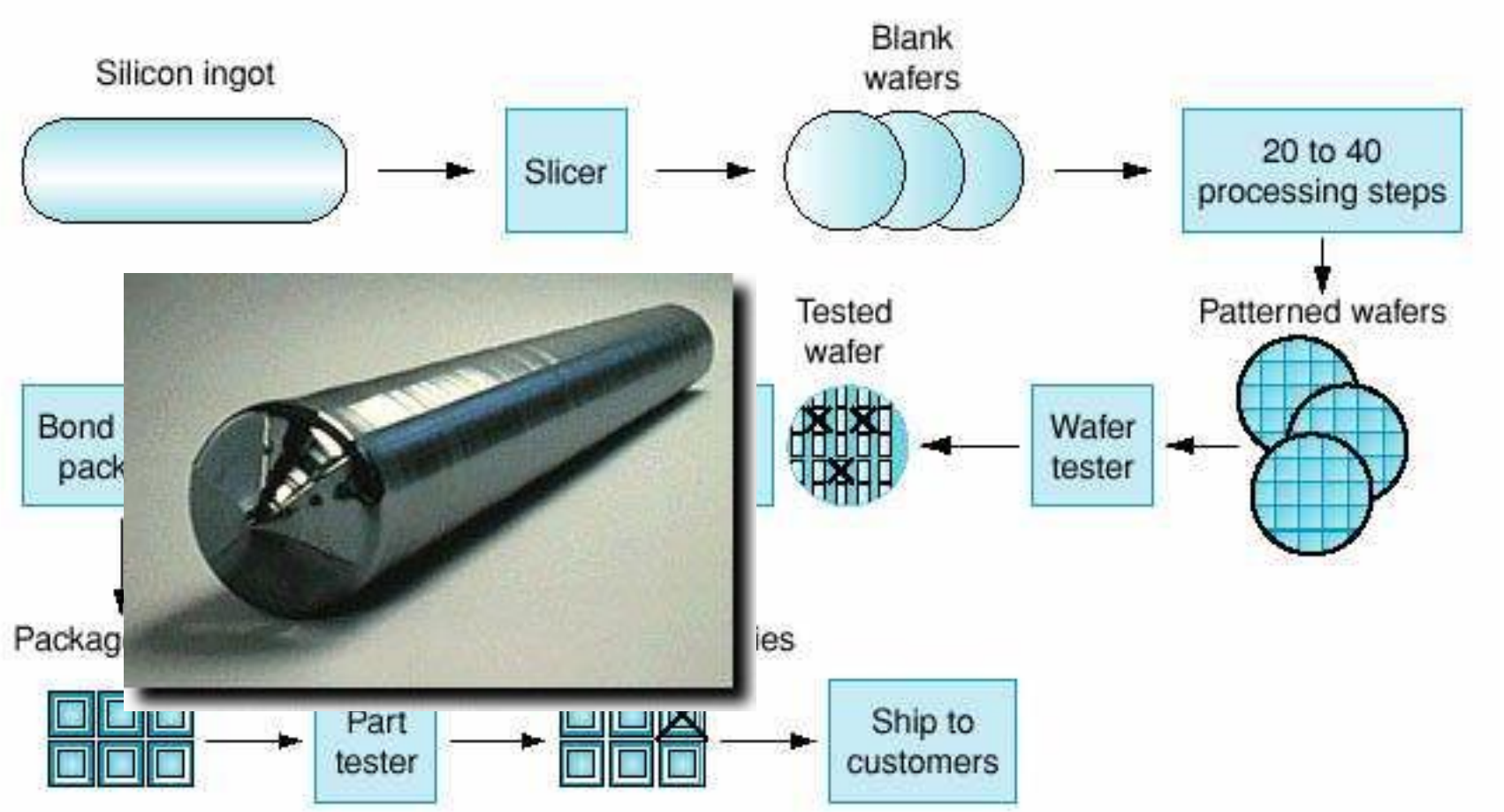
- Silicon fabrication lab

AMD's 65 nm fabrication lab (control and clean room)

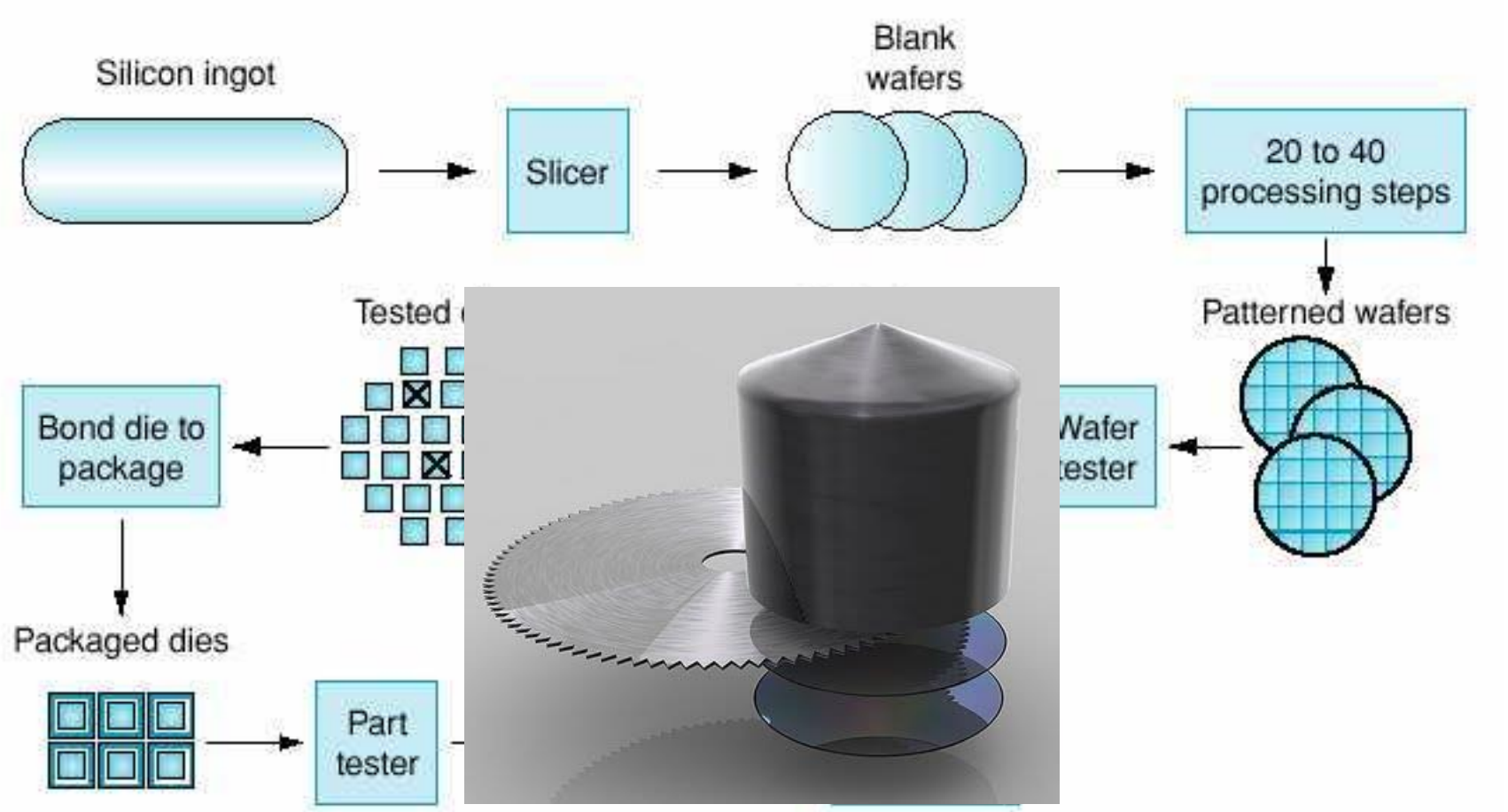
Find an interesting video at:
http://www.bloomberg.com/news/articles/2016-06-09/how-intel-makes-a-chip

Source: http://www.dailytech.com

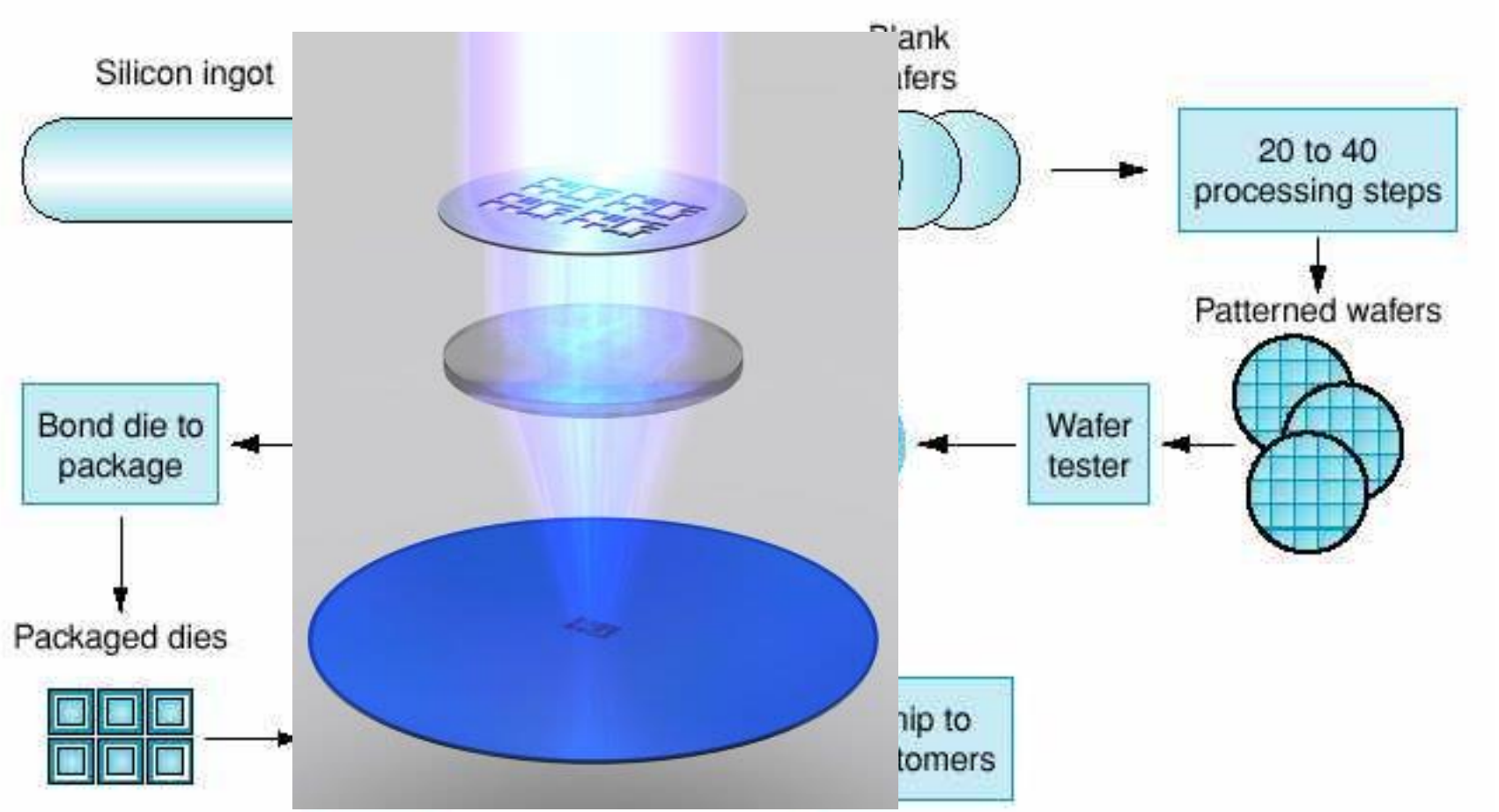
VLSI process for full custom ICs



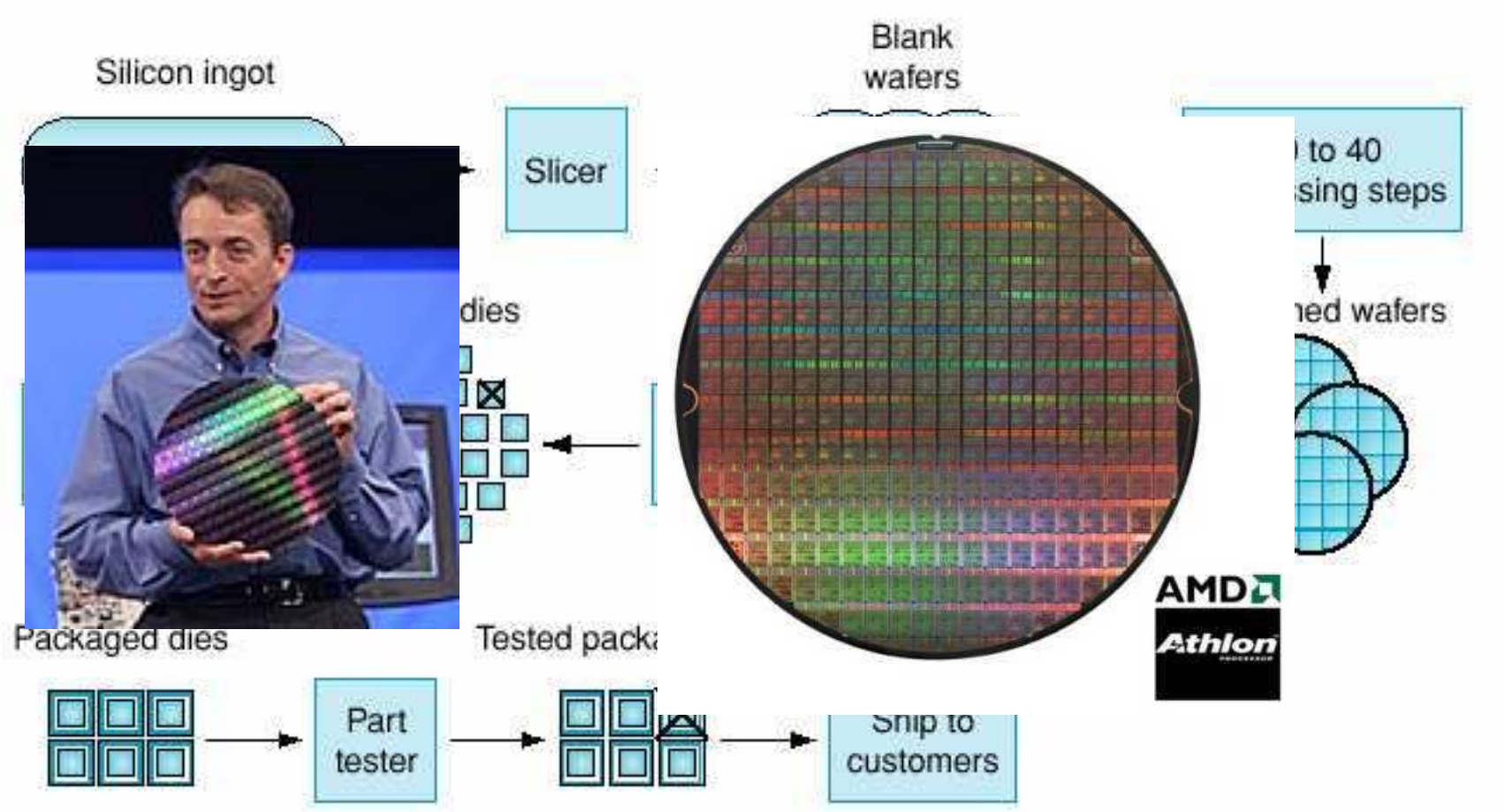
VLSI process for full custom ICs



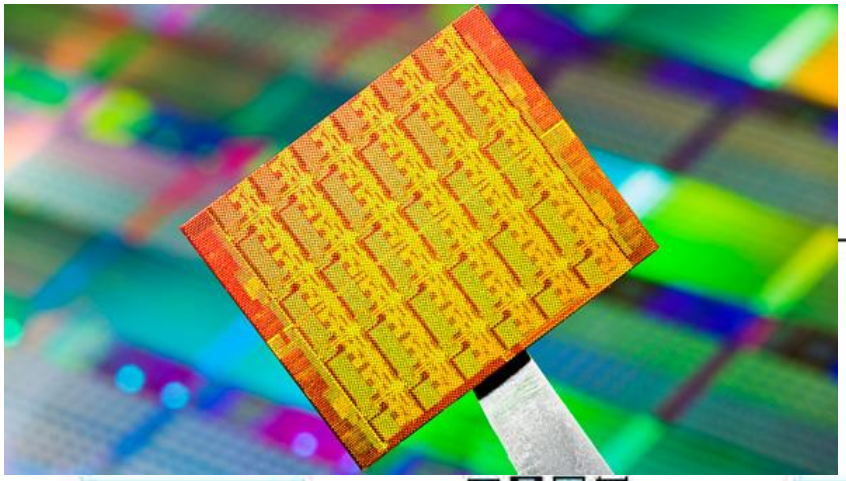
VLSI process for full custom ICs



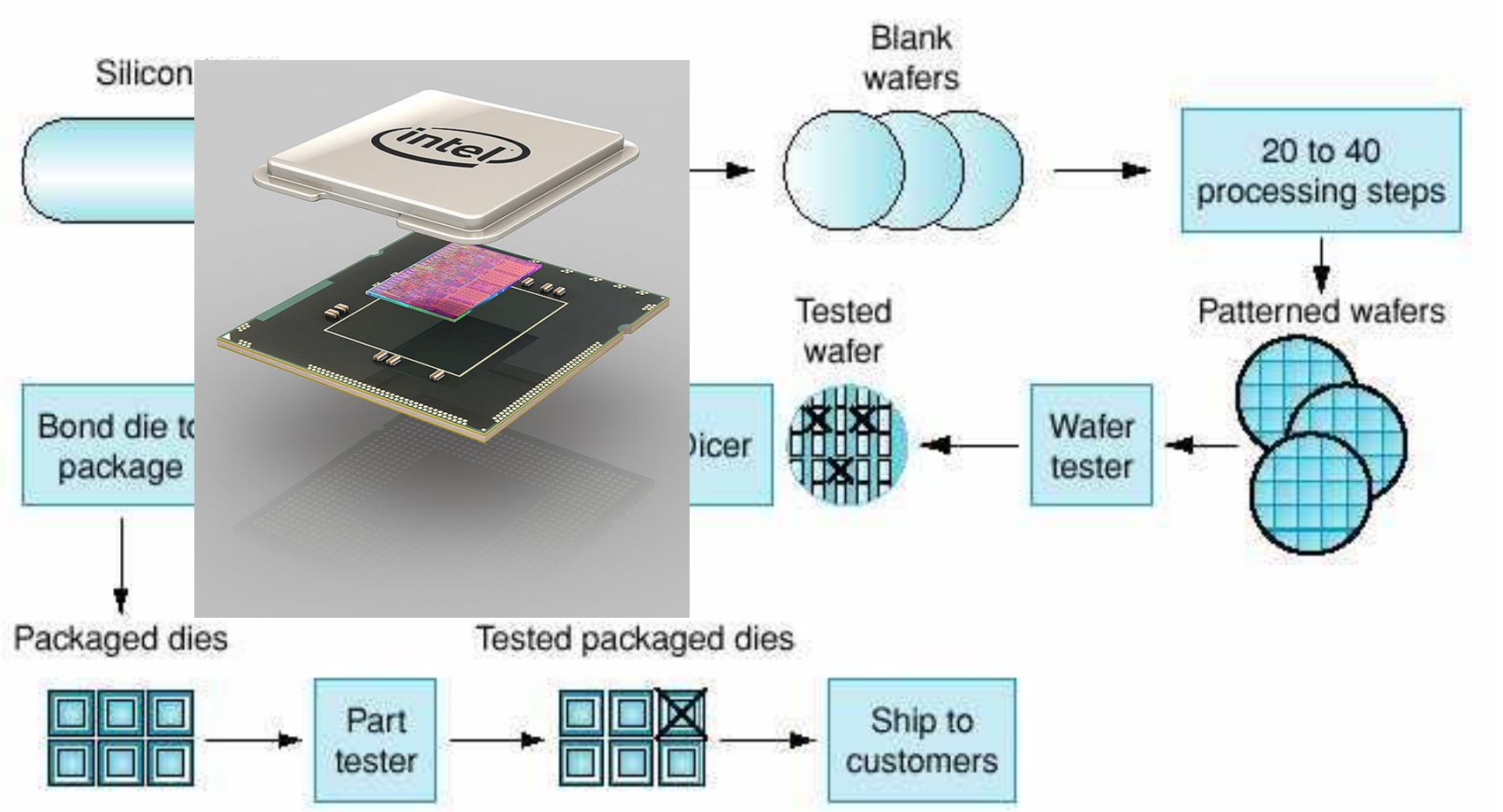
VLSI process for full custom ICs



VLSI process for full custom ICs

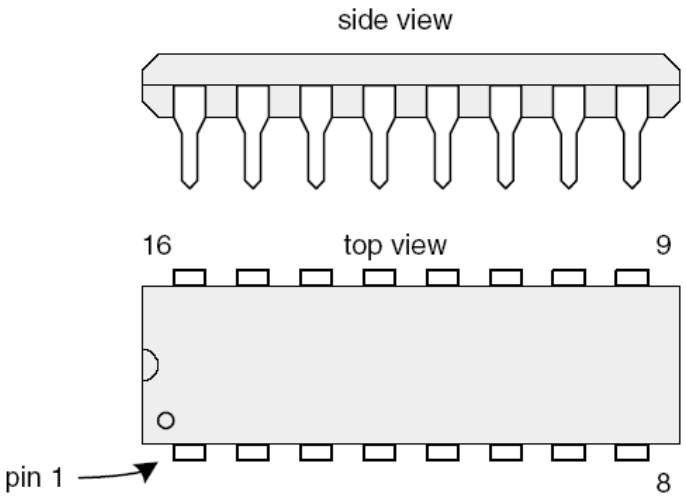


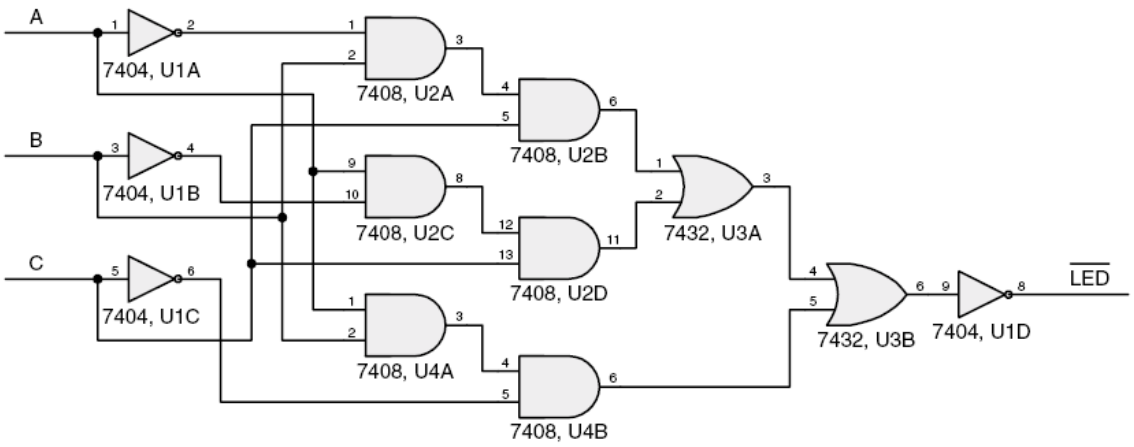
VLSI process for full custom ICs



TTL gates

- For very simple hardware only
- 74 series
  - 7404: hex NOT
  - 7408: quad 2-inpu AND
  - 74374: Flip-flop
  - 74193: 4-bit counter



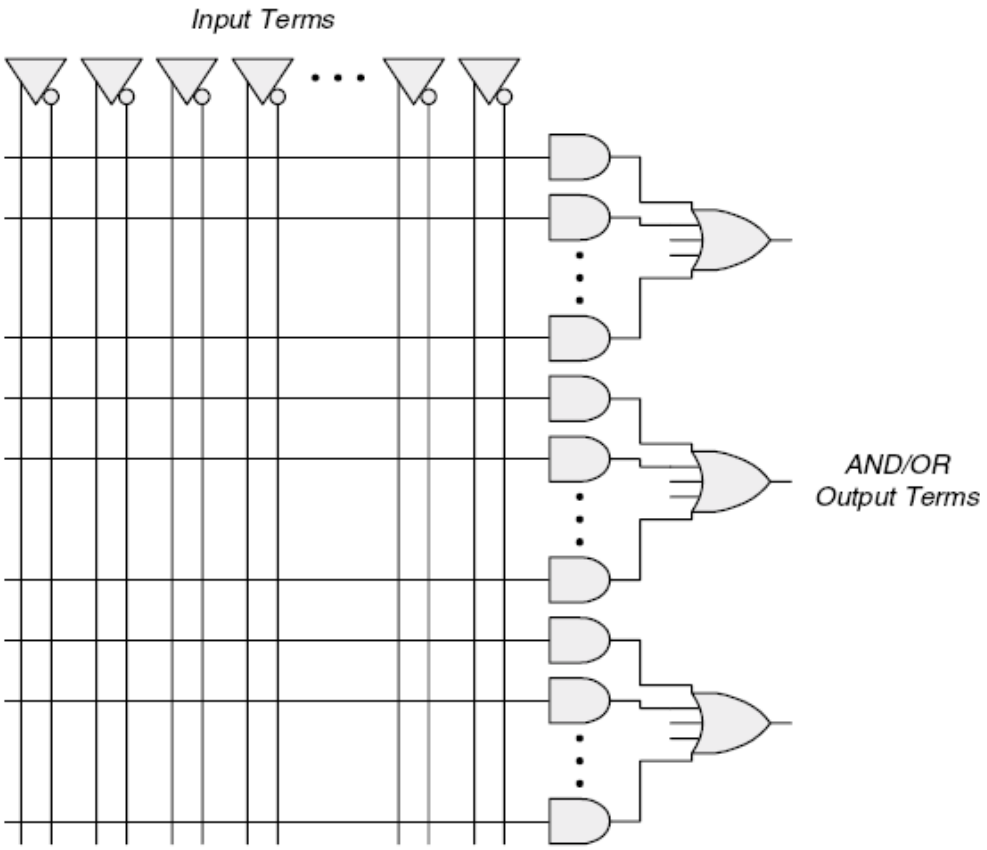


Programmable logic devices

- Some degrees of reconfigurability in ICs
- Fabricate gates, memories, interconnects into a single chip
- Let the final user to implement logic functions by appropriately connecting these devices
- PLD chips are themselves constructed by a standard cell or full-custom method
  - But final function implementation is done by the end user
- Programmable Logic Devices (PLD) are the most common target for HDL codes
  - In comparison to standard cell and full-custom chips

Programmable devices

- You know simple PLDs from the Logic Design course
- *We will review them again shortly*
- Example: PAL
  - Very simple programmable IC
  - The base of more complex programmable ICs



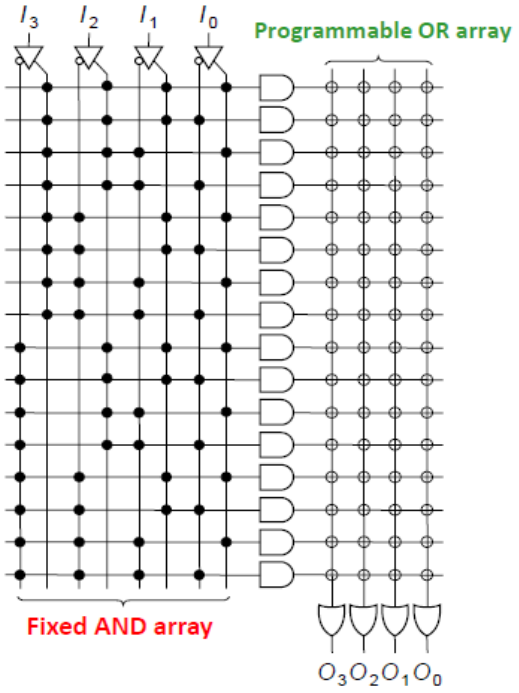
Advantages of PLDs

- Field Programmable
  - Reduced TTM and design cost
  - Accessible everywhere: easy-to-implement functions
- Erasable and reprogrammable
  - Updating a device or correction of errors
    - By a simple patch
  - Used for full-custom prototyping

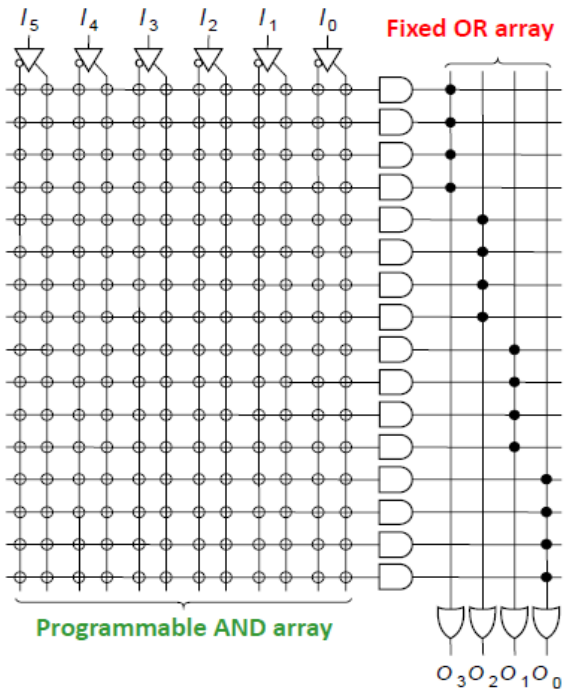
Programmable logic technologies

- Simple Programmable Logic Device (SPLD)
  - Read Only Memory (ROM)
  - Programmable Array Logic (PAL)
  - Programmable Logic Array (PLA)
- Complex Programmable Logic Device (CPLD)
- Field- Programmable Gate Array (FPGA)

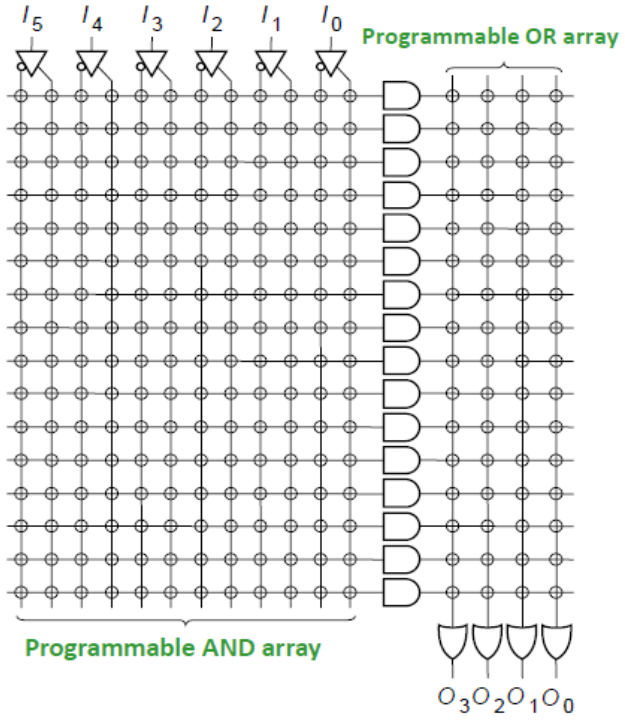
ROM, PAL and PLA



PROM

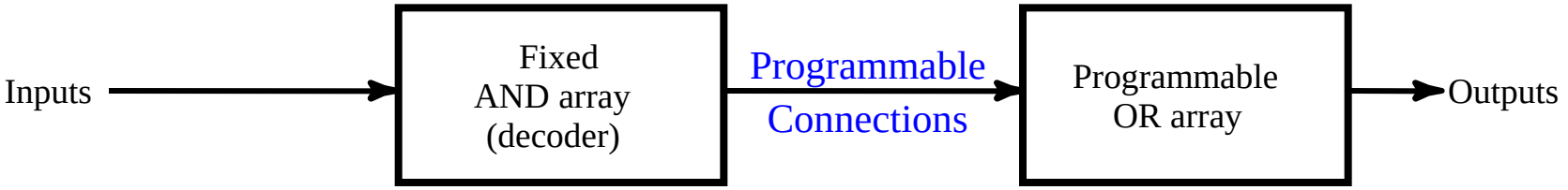


PAL

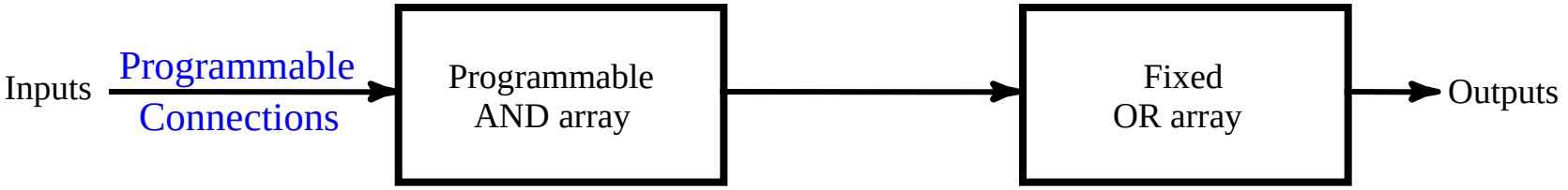


PLA

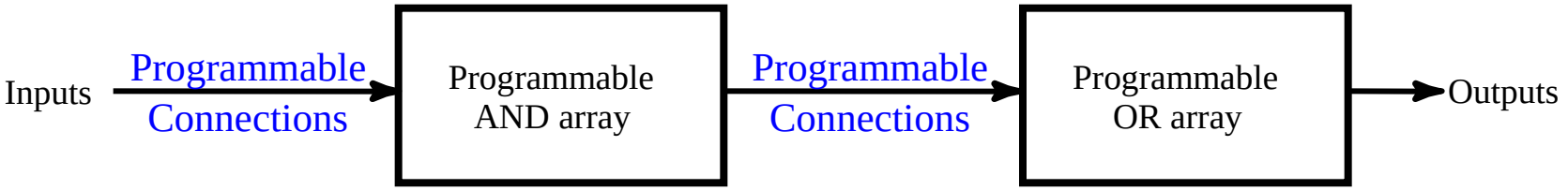
ROM, PAL and PLA configurations



(a) Programmable read-only memory (PROM)

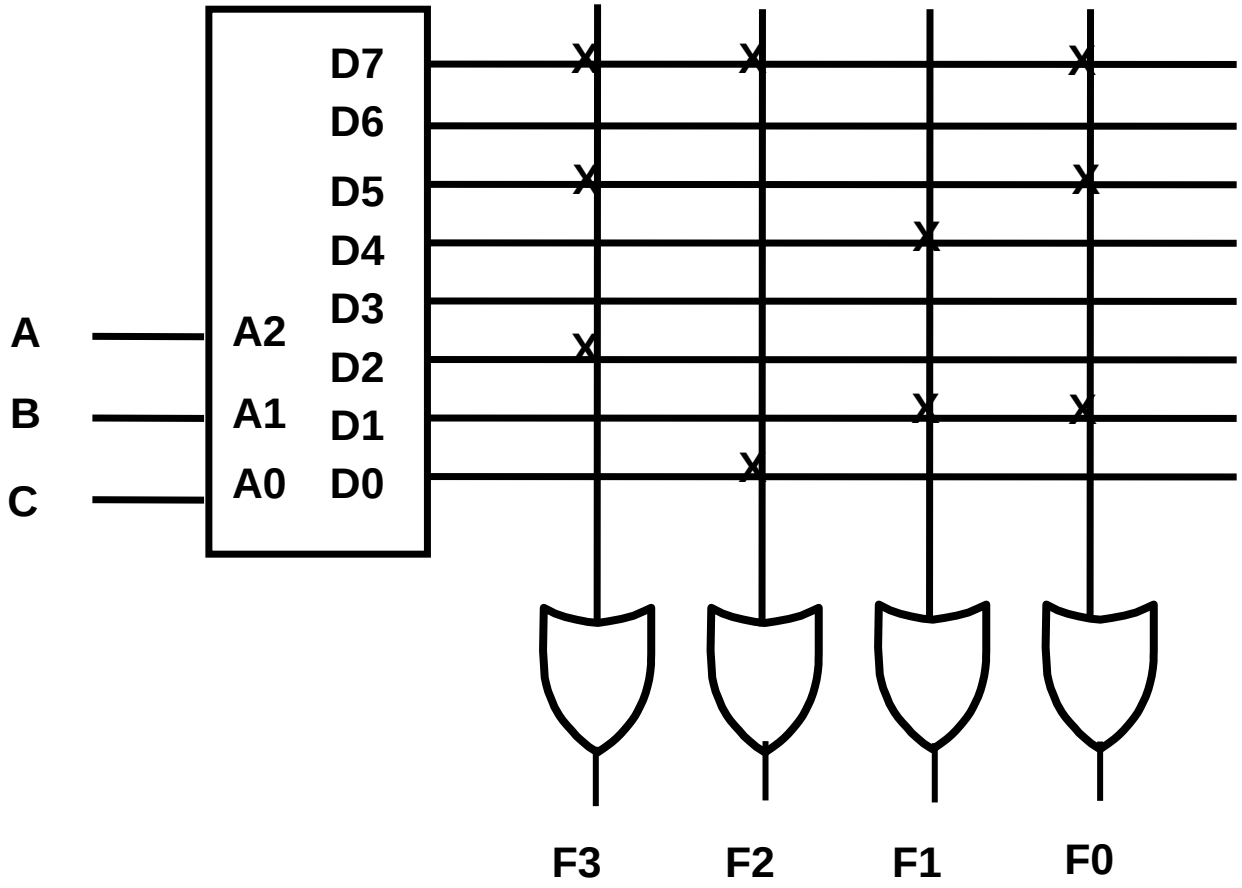


(b) Programmable array logic (PAL) device

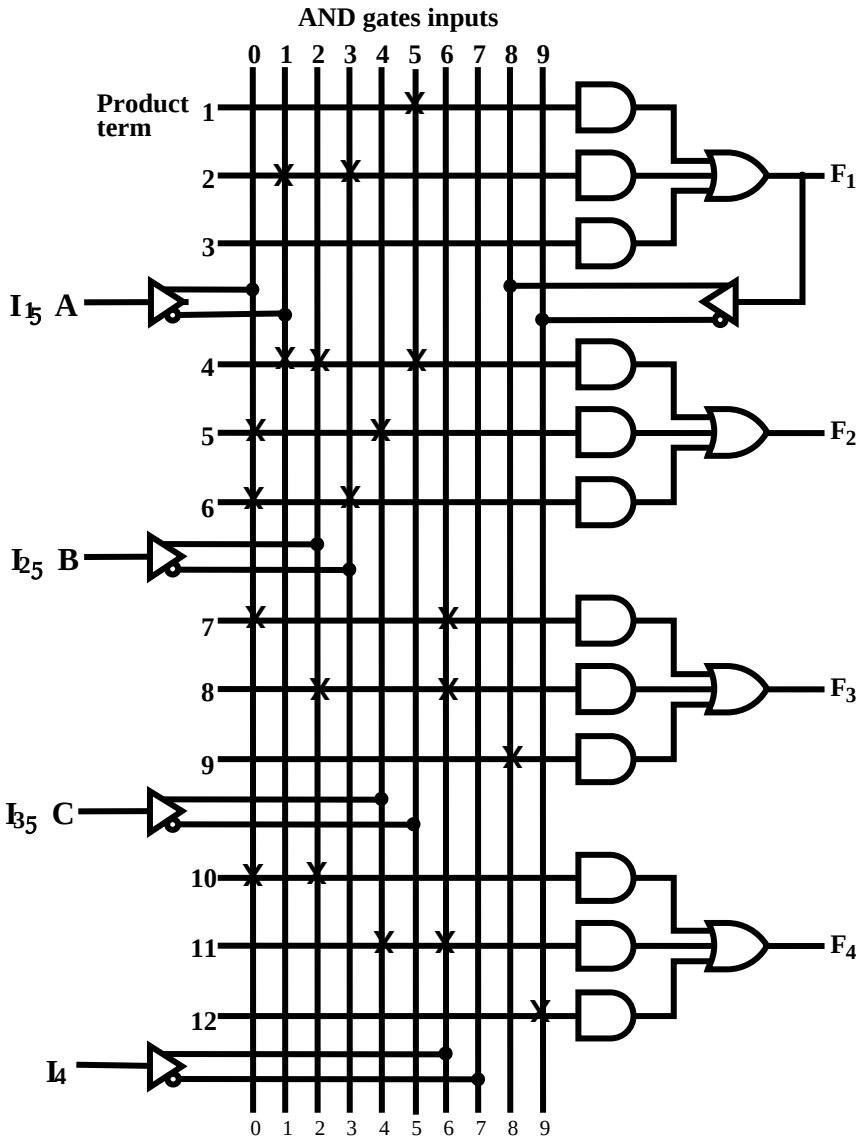


(c) Programmable logic array (PLA) device

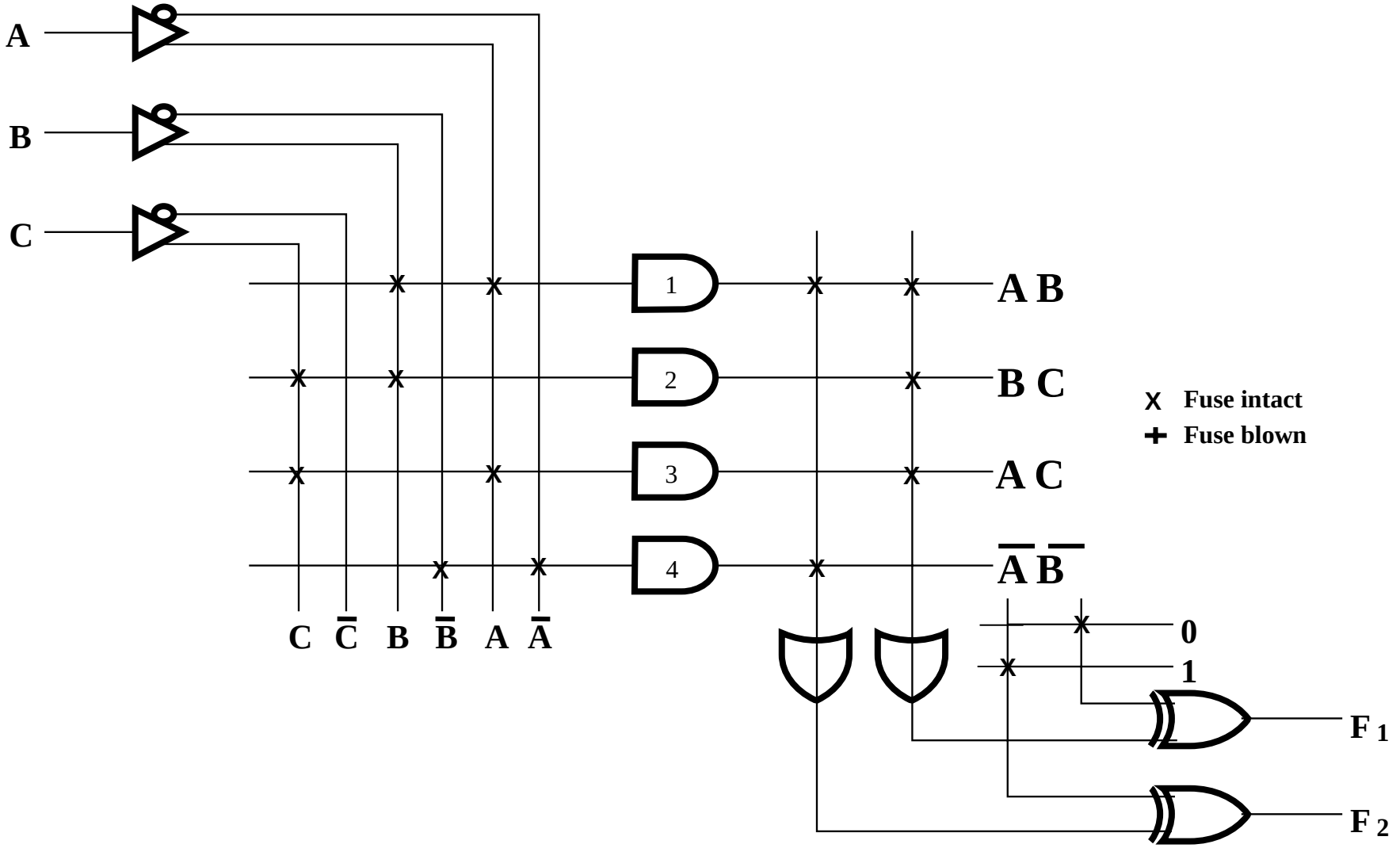
ROM



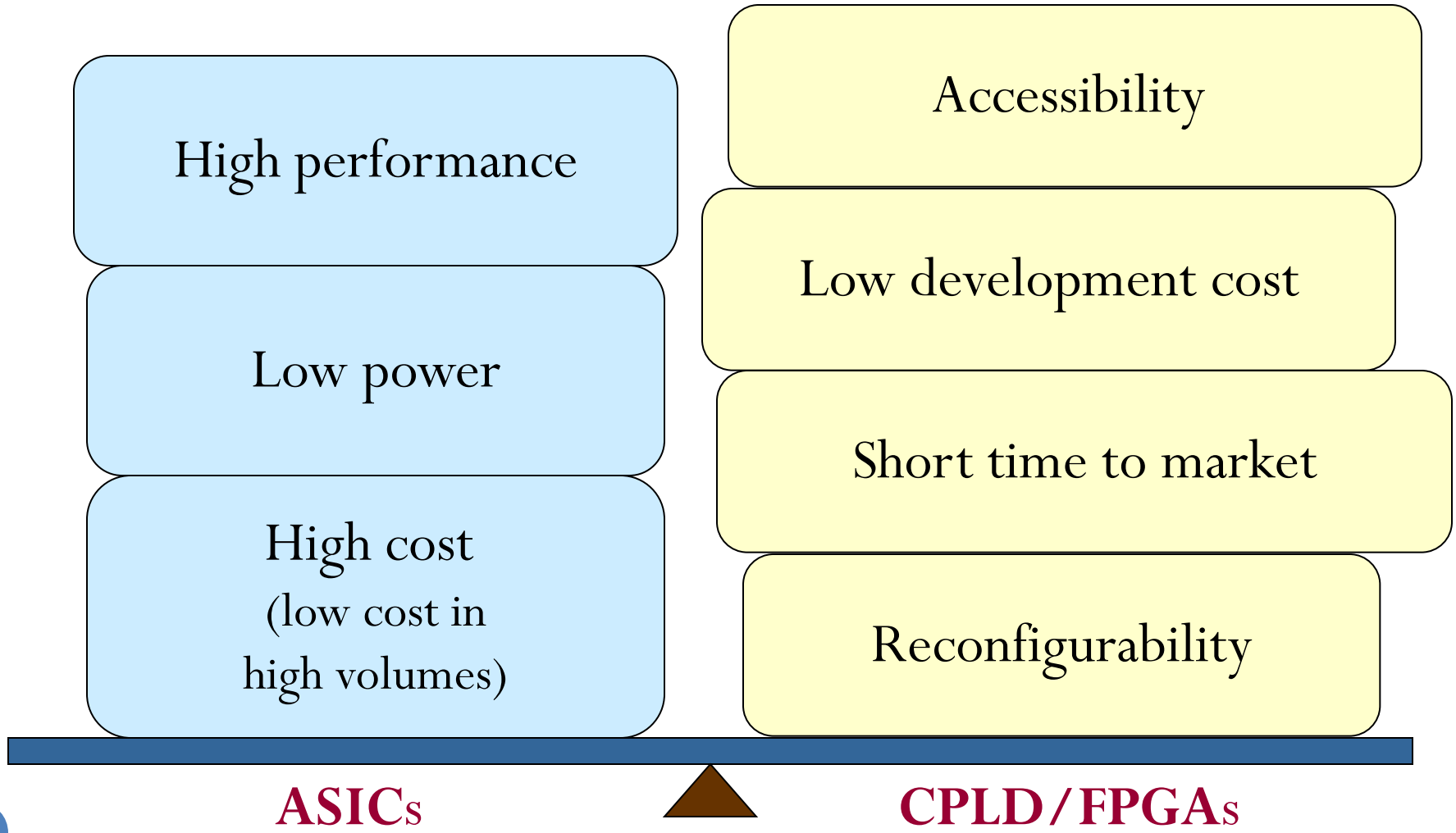
PAL


AND gates inputs
0 1 2 3 4 5 6 7 8 9
Product term
1
2
3
I1 A
4
5
6
I2 B
7
8
9
I3 C
10
11
12
I4
F1
F2
F3
F4
0 1 2 3 4 5 6 7 8 9

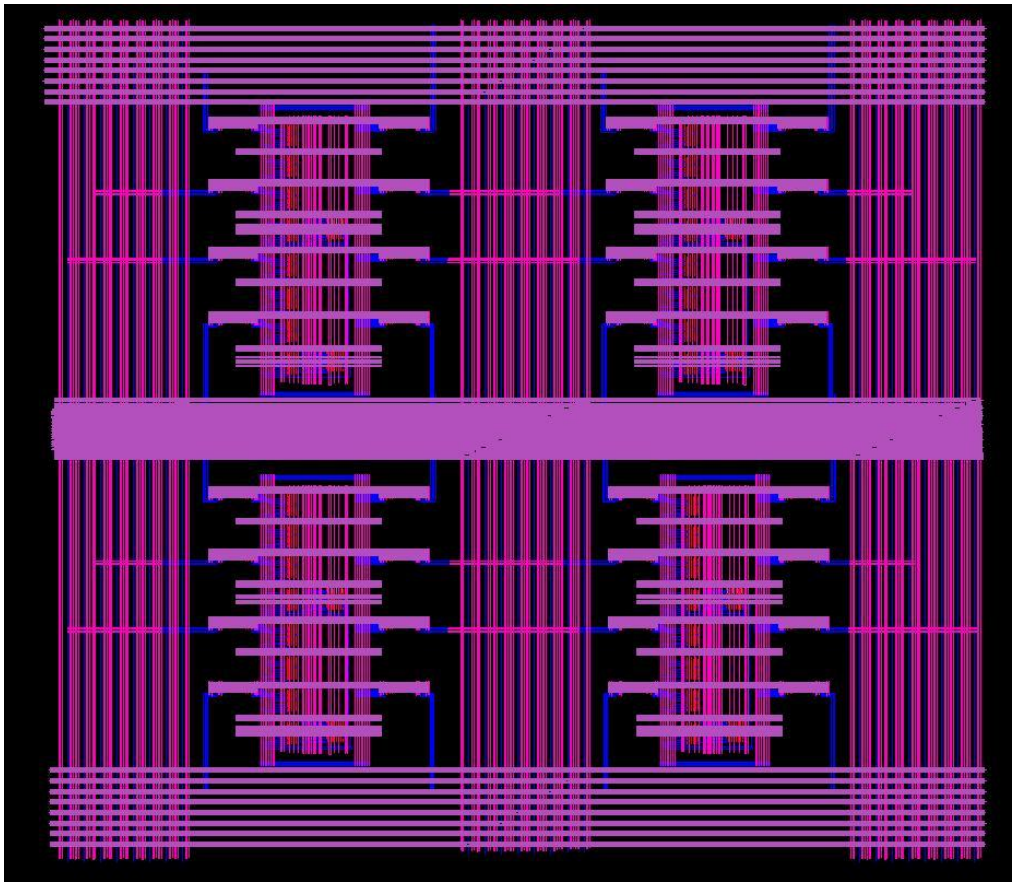
PLA

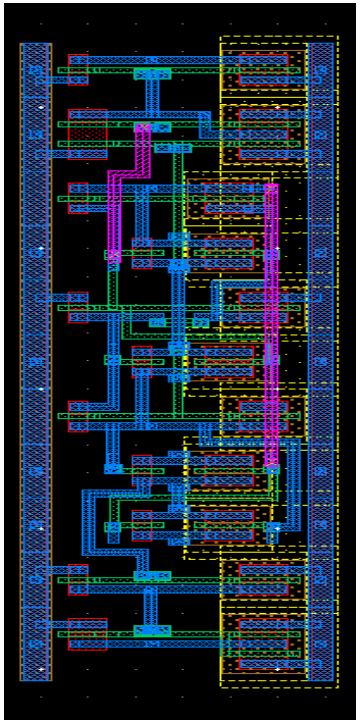


Technology trade-offs



Full adder





	PLA	ASIC
Latency=	56 PS	3.7 PS
Energy=	182 PJ	47PJ

PLD architectures

- PAL and PLA are simple devices and called SPLD (simple PLD)
- Two types complex programmable devices:

CPLDs

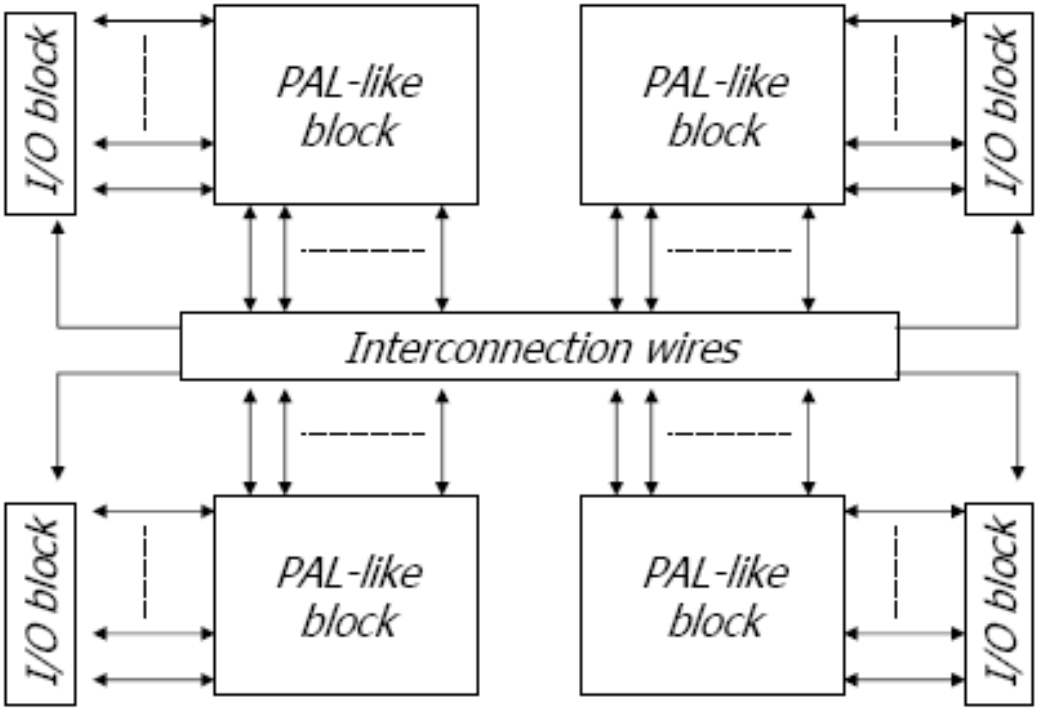
- Often composed of some large blocks
  - Each block is a PAL plus some storage elements
- Connection among blocks by a central interconnection part

FPGAs

- Often composed of tens to hundreds of smaller logic blocks
  - Each block has a few lookup tables plus some storage elements
- The blocks are surrounded by a sea of interconnects

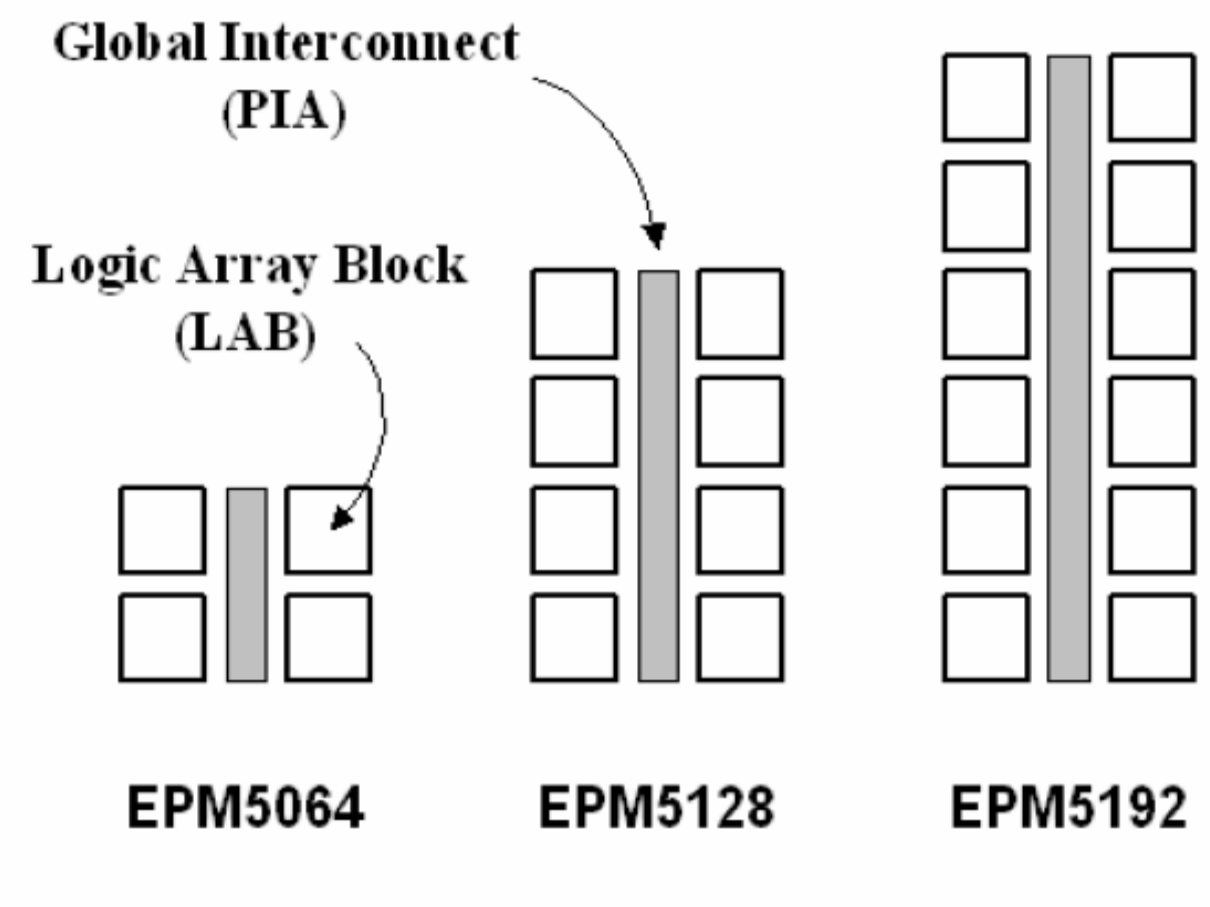
CPLD

- Each block is like a large PAL with some memory elements



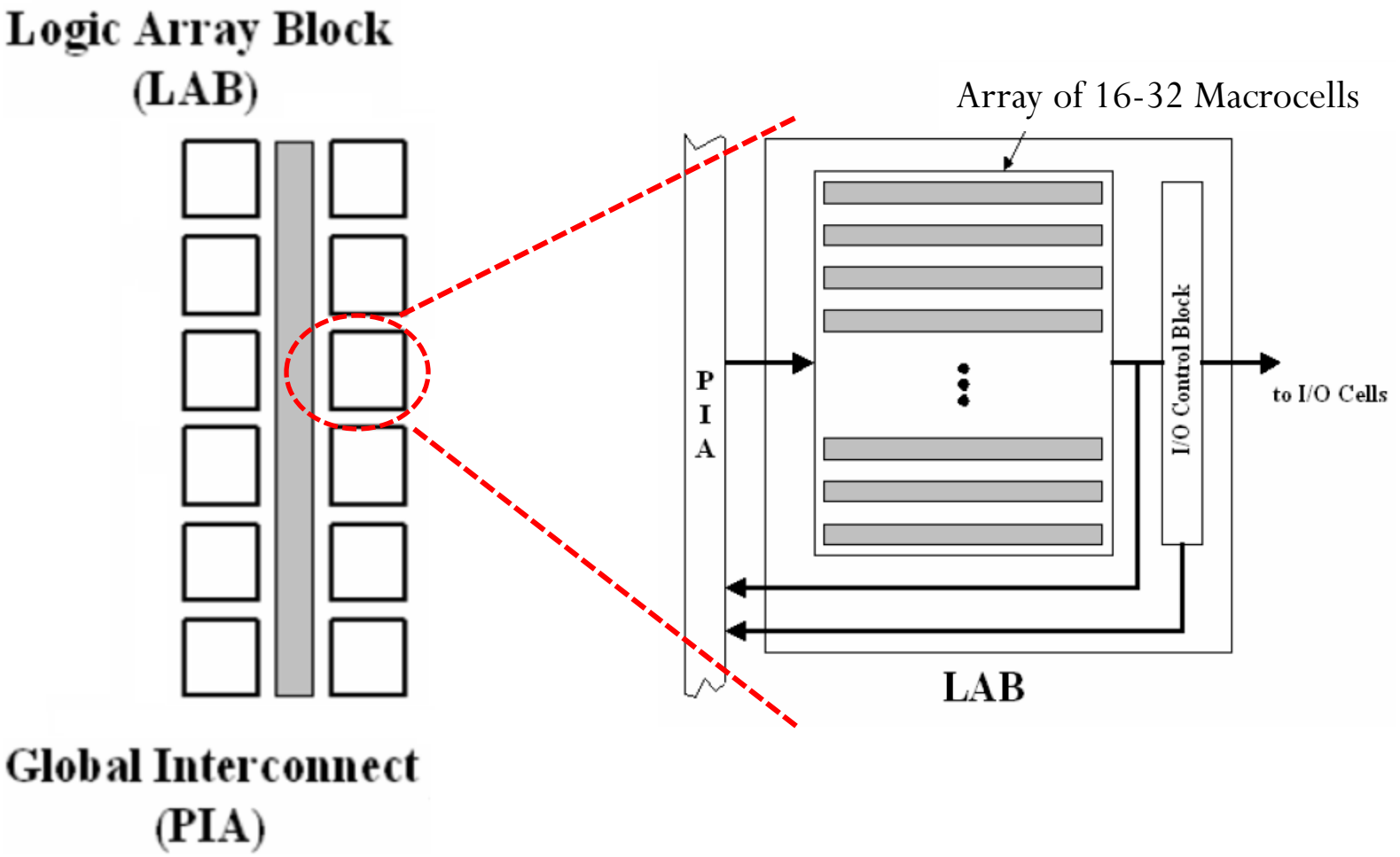
CPLD example

Altera® MAX 5000



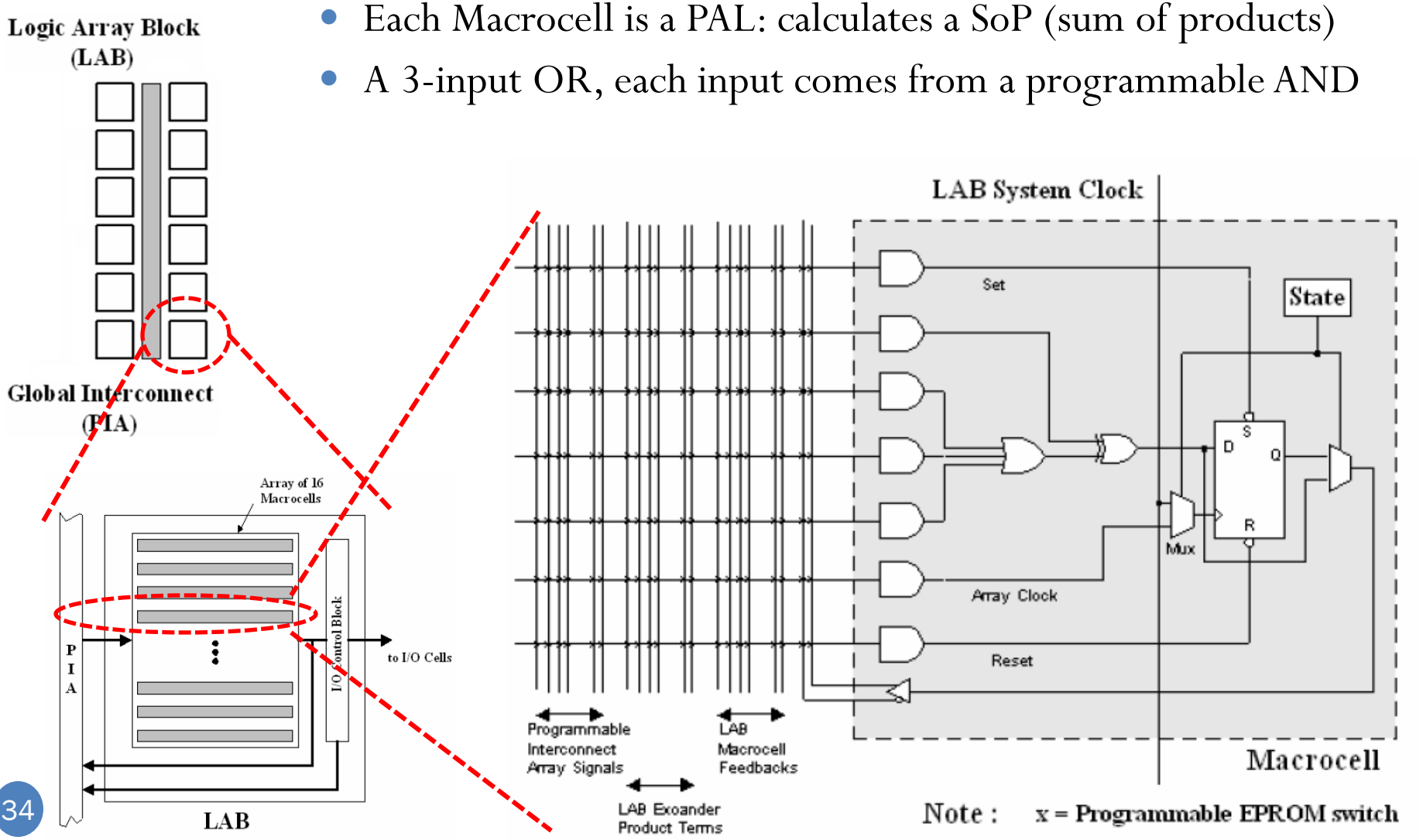
Altera® MAX 5000

- Each LAB contains 16-32 Macrocells



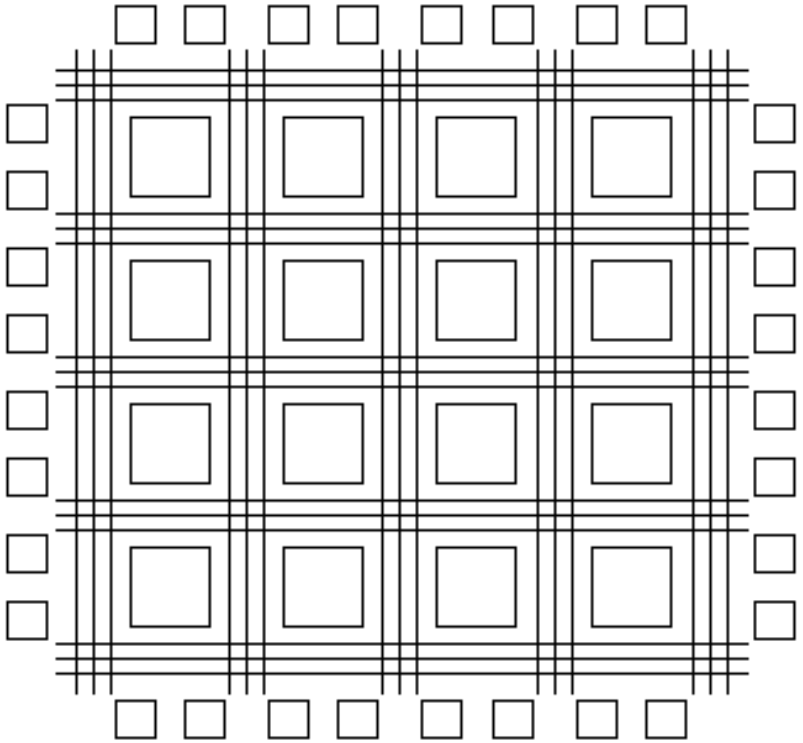
Altera® MAX 5000

- Each Macrocell is a PAL: calculates a SoP (sum of products)
- A 3-input OR, each input comes from a programmable AND



FPGA

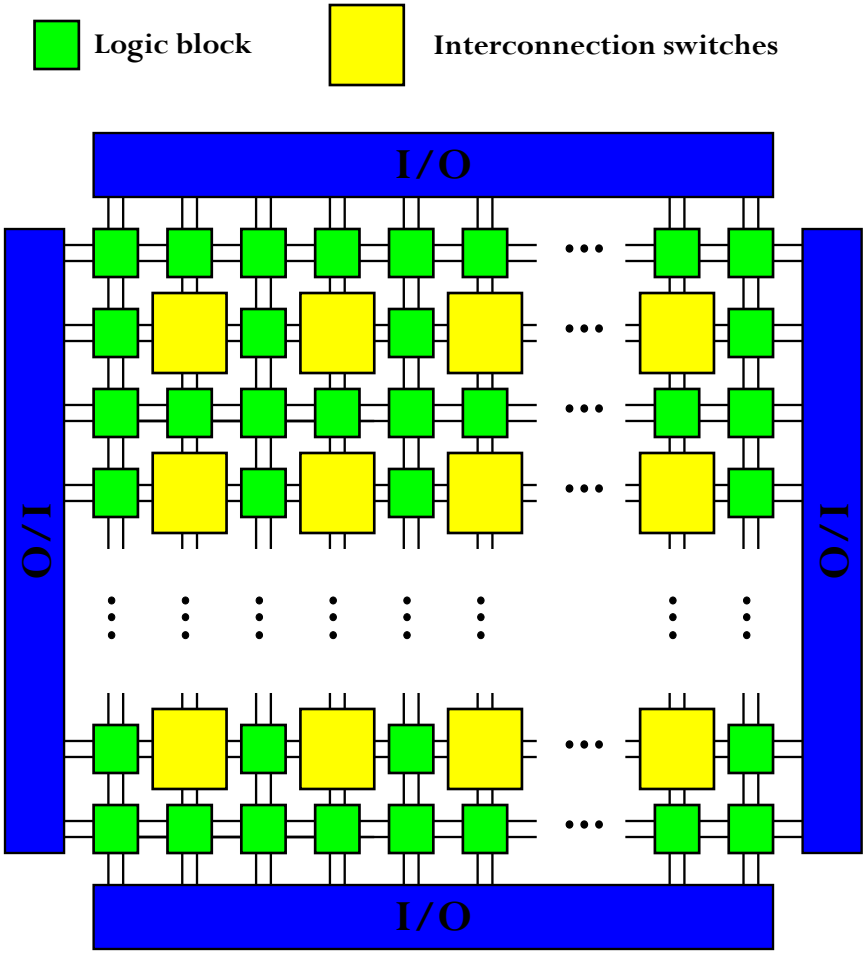
- An array of logic cells in a sea of interconnects



FPGA - generic structure

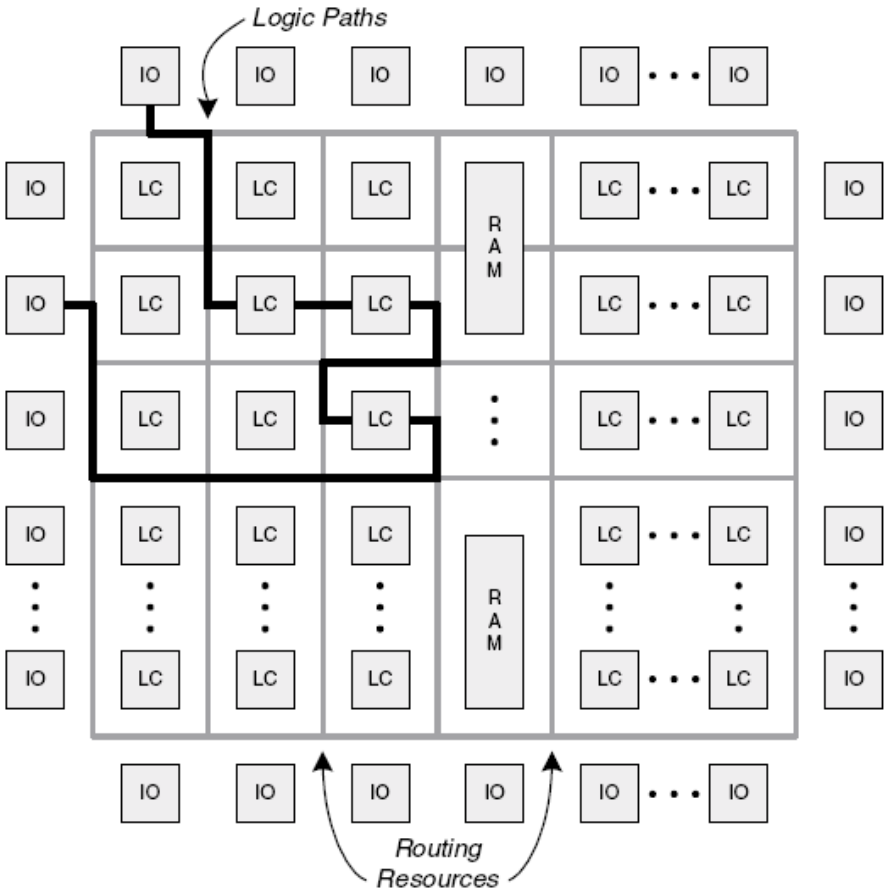
FPGA building blocks:

- Programmable logic blocks
  Implement combinatorial and sequential logic
- Programmable interconnect
  Wires to connect inputs and outputs to logic blocks
- Programmable I/O blocks
  Special logic blocks at the periphery of device for external connections



FPGA

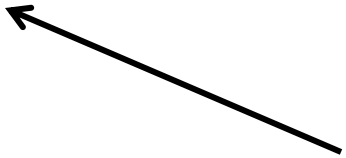
- FPGA: Filed Programmable Gate Array



LC= logic cell, can be a PAL

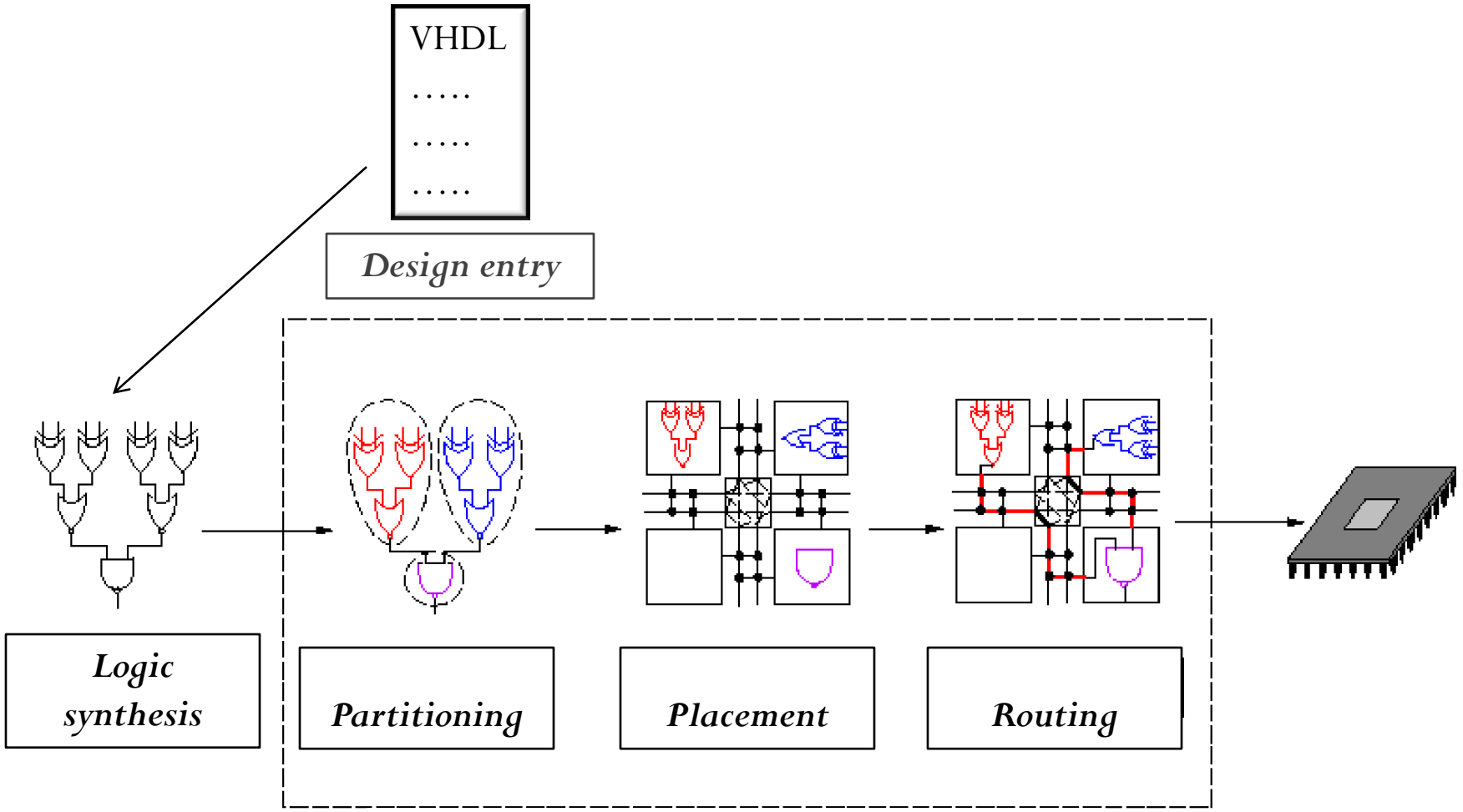
Digital design flow for FPGAs

- Design entry
- Logic synthesis
- Partitioning
- Placement
- Routing
- Pin assignment



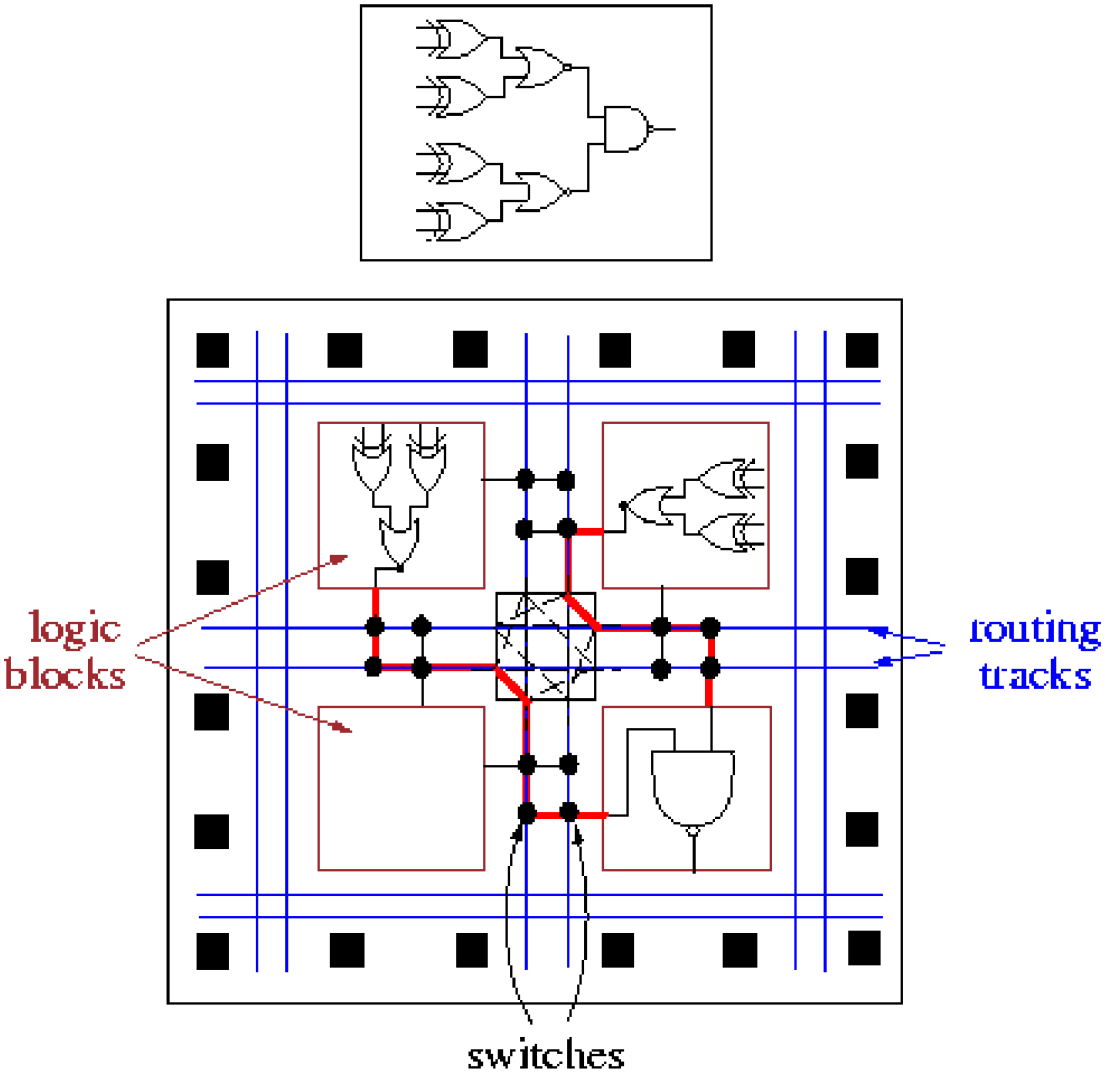
Physical Design

Digital design flow for FPGAs



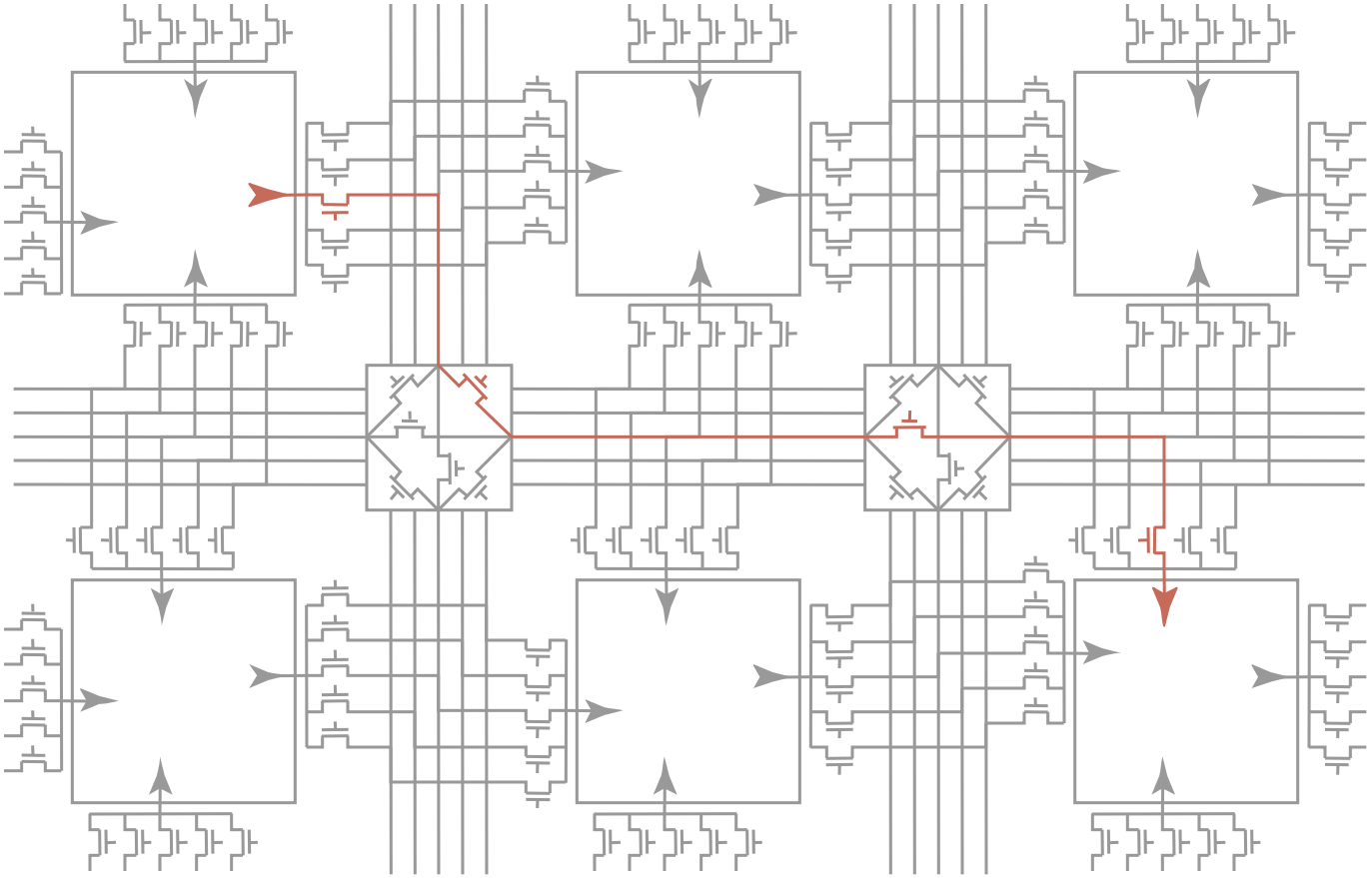
Picture Source: CEIT212 at Amirkabir U. of Tech., Lecture 10, by Dr Saheb-zamani, with modifications

FPGA physical design



Picture Source: CEIT212 at Amirkabir U. of Tech., Lecture 10, by Dr Saheb-zamani

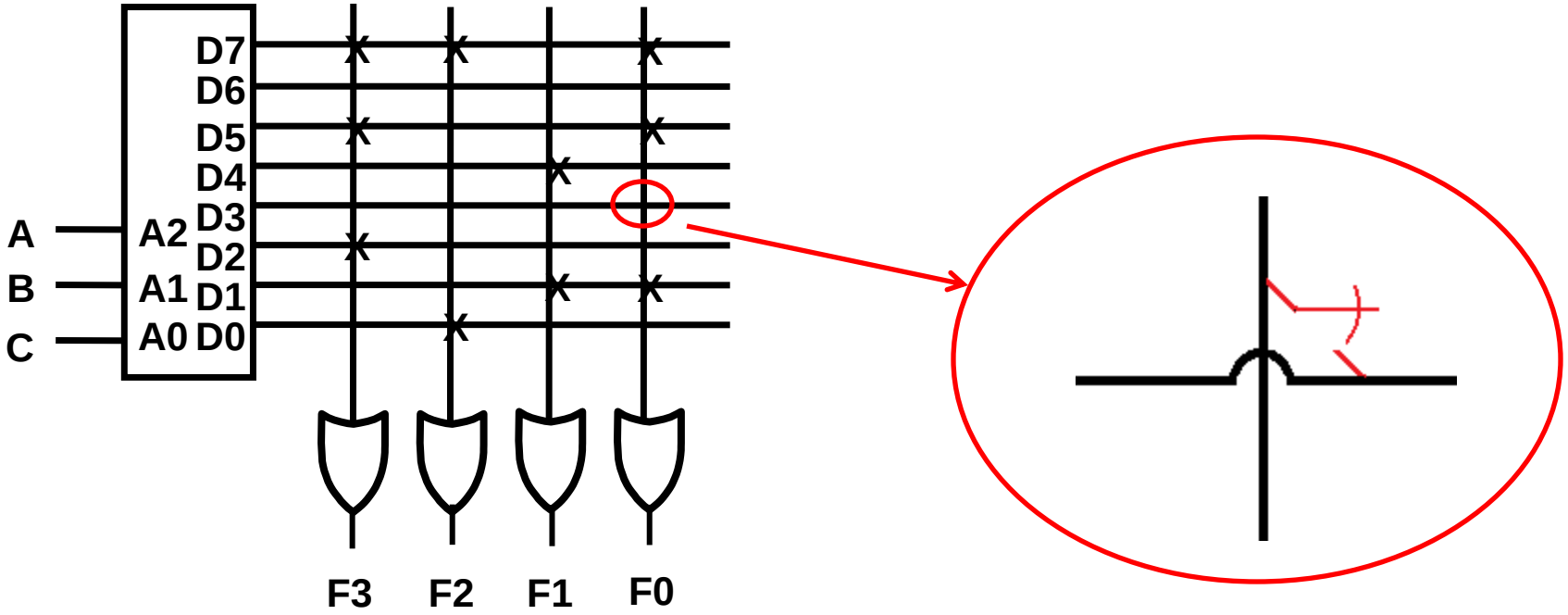
Programmable routing



Source: ECE 554, University of Wisconsin - Madison

Programming technology

- Must use a programmable technology to implement the reconfigurable parts



Programmable parts

- PAL and PLA connection points
- Multiplexers
- Interconnects among different components in a programmable chip
- Lookup table entries

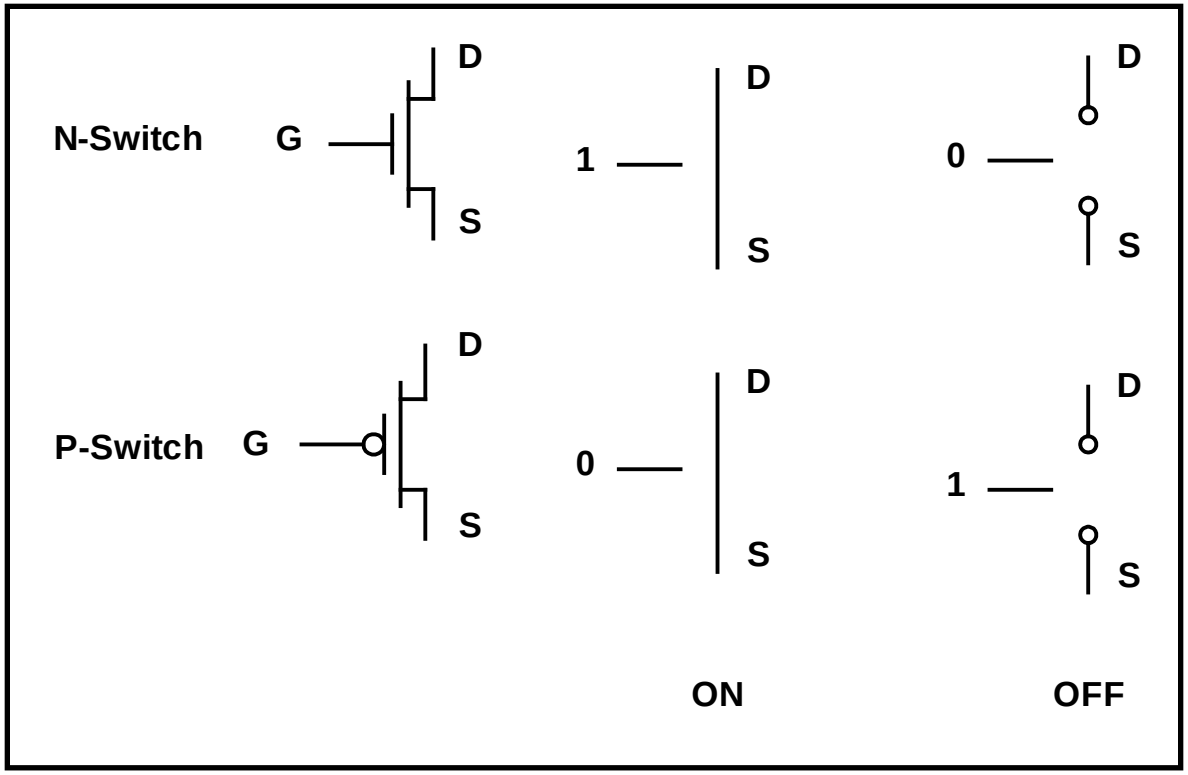
→ These parts will be introduced soon!

Programming technologies

- How the programmable parts are constructed
- Three major technologies
  - SRAM+ transistor switches
  - ROM
  - Antifuse

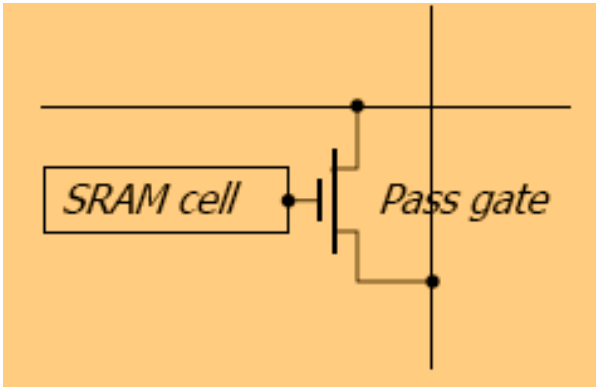
Programming technology- SRAM

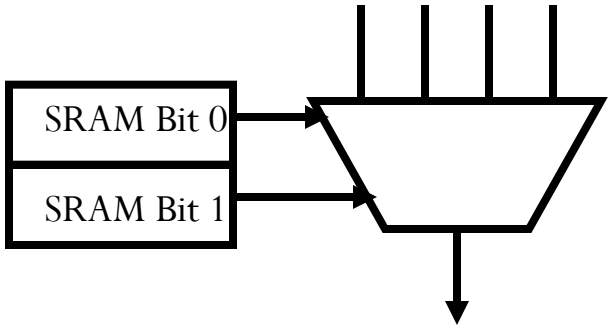
Recall the transistor functionality as a switch



Programming technology- SRAM

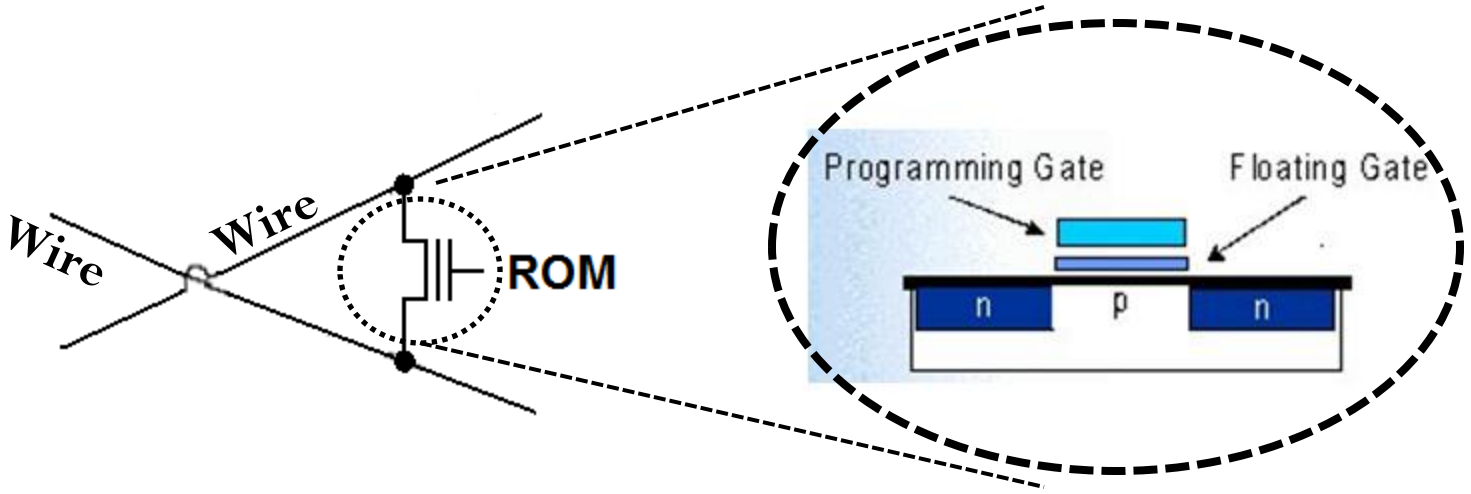
- The switch should be controlled by some memory element
  - To keep the configuration
- A Static Random Access Memory (SRAM) is used
  - Each switch is a pass transistor controlled by the state of an SRAM bit
  - Needs to be configured at power-on





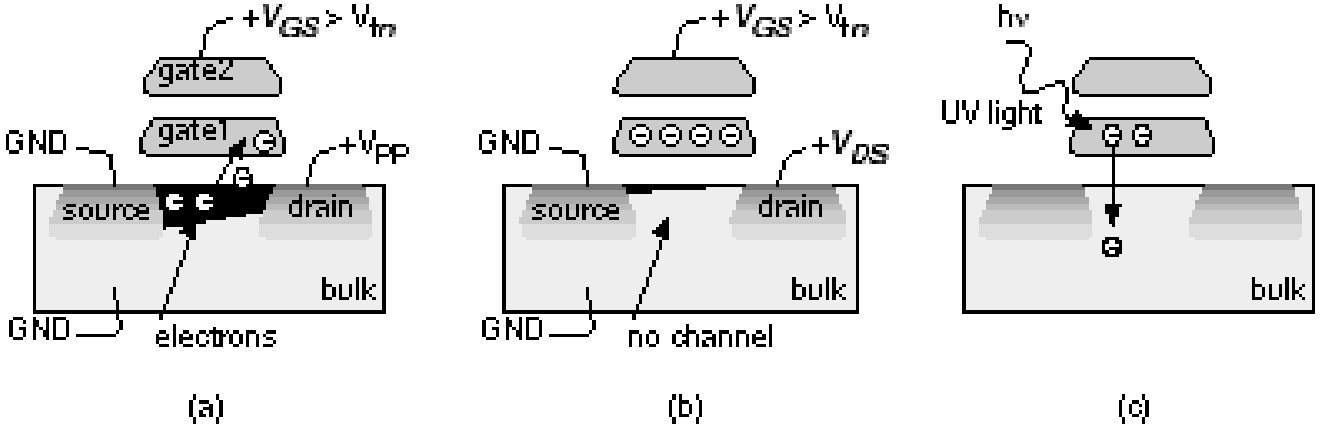
Programming technology- ROM

- Flash Erasable Programmable ROM (Flash)
  - Device itself holds the program
  - Reprogrammable, even in-circuit
  - The configuration is kept, even if the circuit is shut down



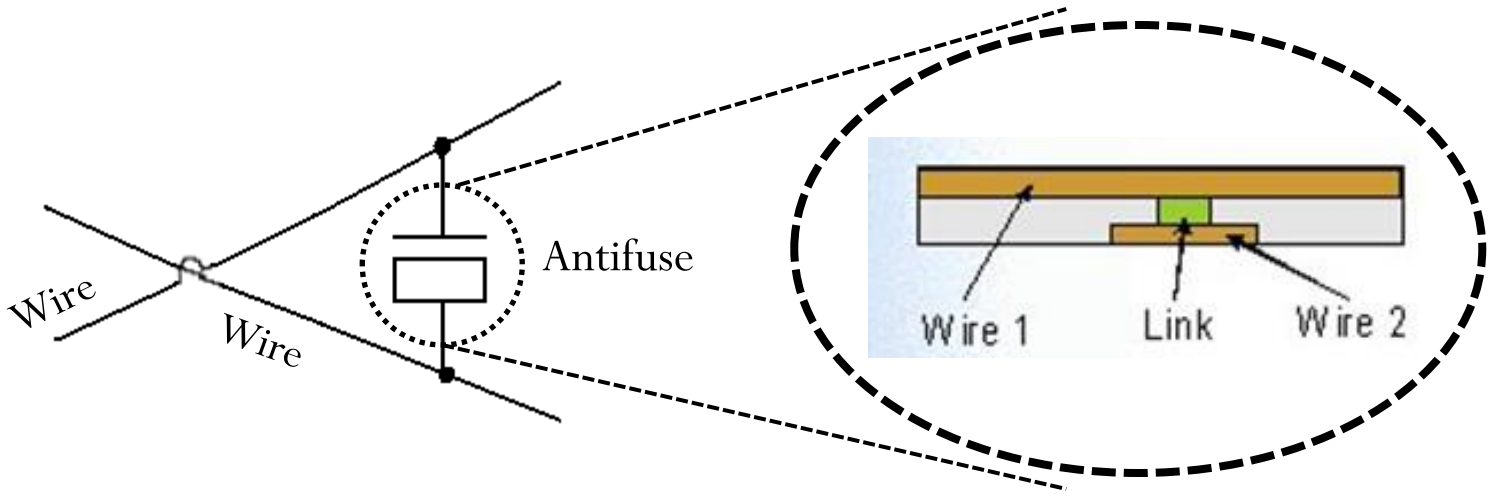
Programming technology- ROM

- ROM: a transistor switch has and additional floating-gate
  - Can be turned off by injecting negative charge onto the floating gate: negative charge prevent channel formation
  - Can be turned on by discharging the floating gate
- EPROM: discharging by UV light
- EEPROM: discharging by electrical voltage



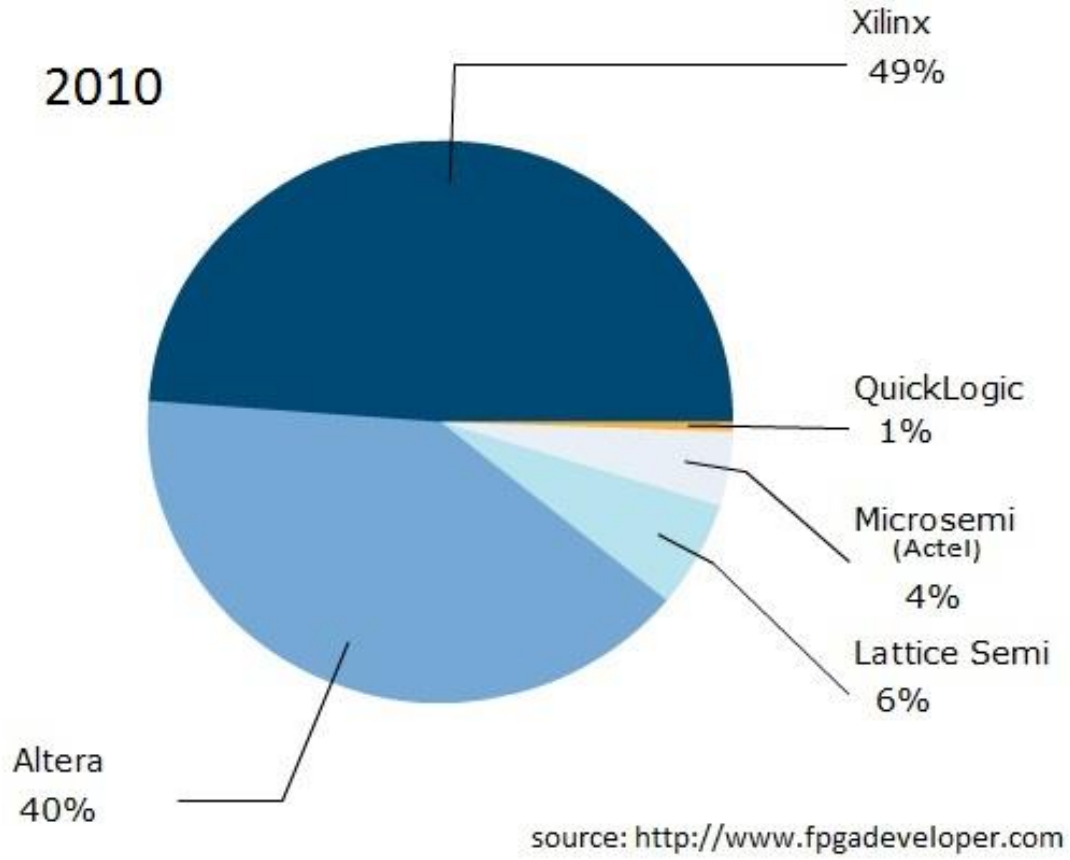
Programming technology- Antifuse

- Fusible Links ("Antifuse")
  - Forms a low resistance path when electrically programmed
- Lower area and higher speed than SRAM and ROM
- Once the fuse is programmed, the state never changes
  - One-time programmable

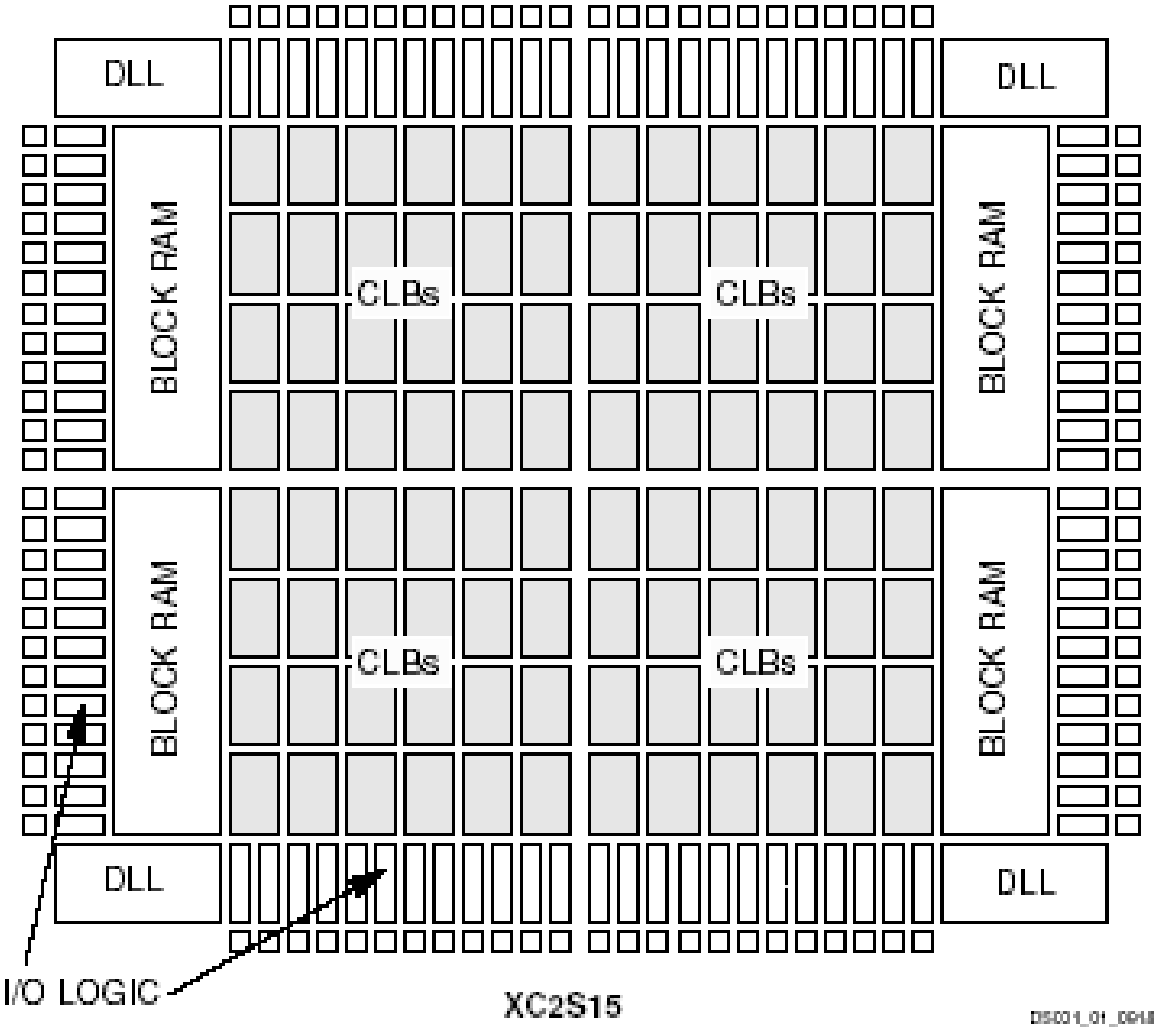


FPGA market

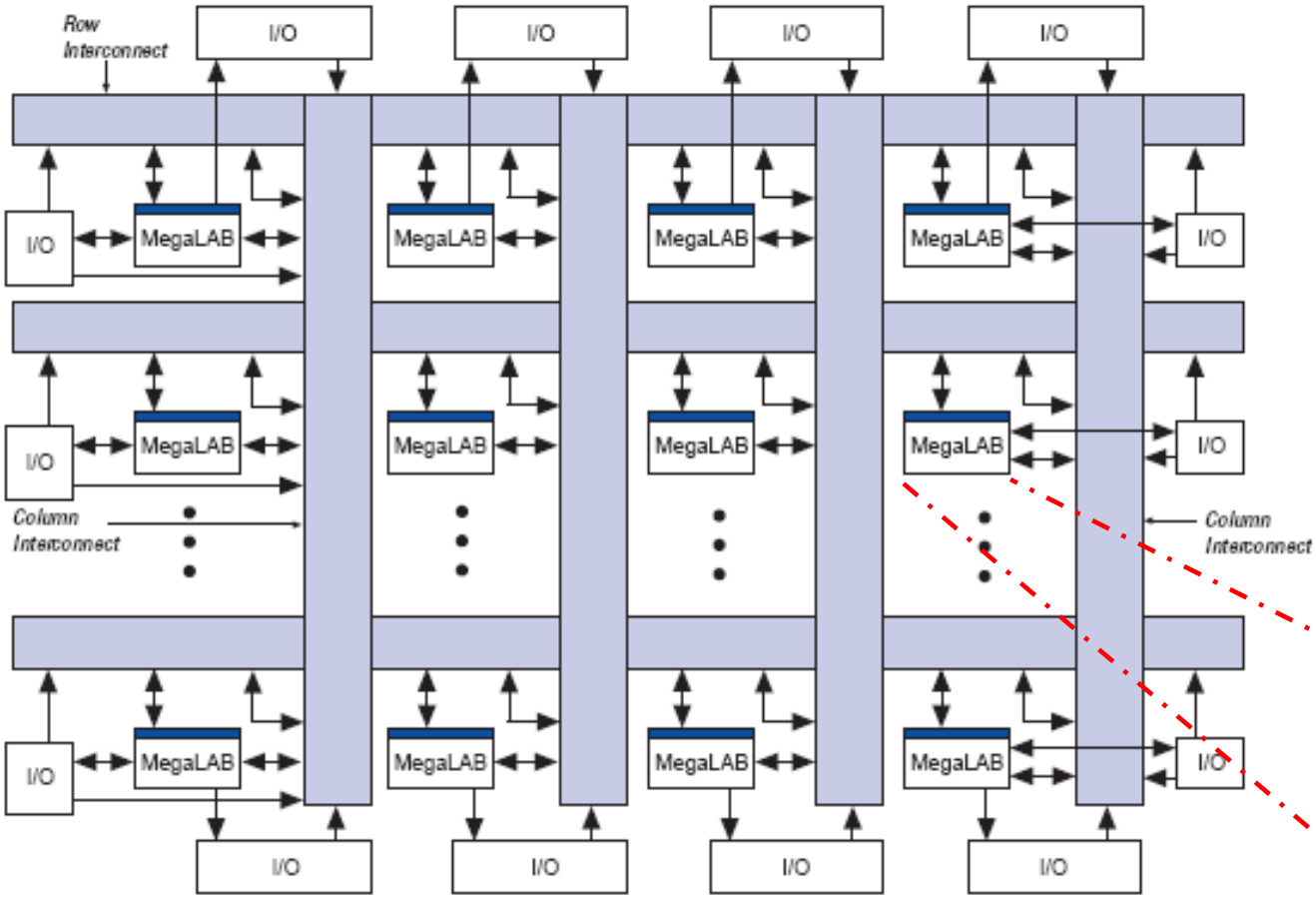
- Several companies produce FPGAs and CPLDs
- Two major companies: Altera and Xilinx



FPGA example: Xilinx Spartan-II



FPGA example: Altera Apex 20K



APEX™