Microprocessor System Design

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8088 Microprocessor

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Outline

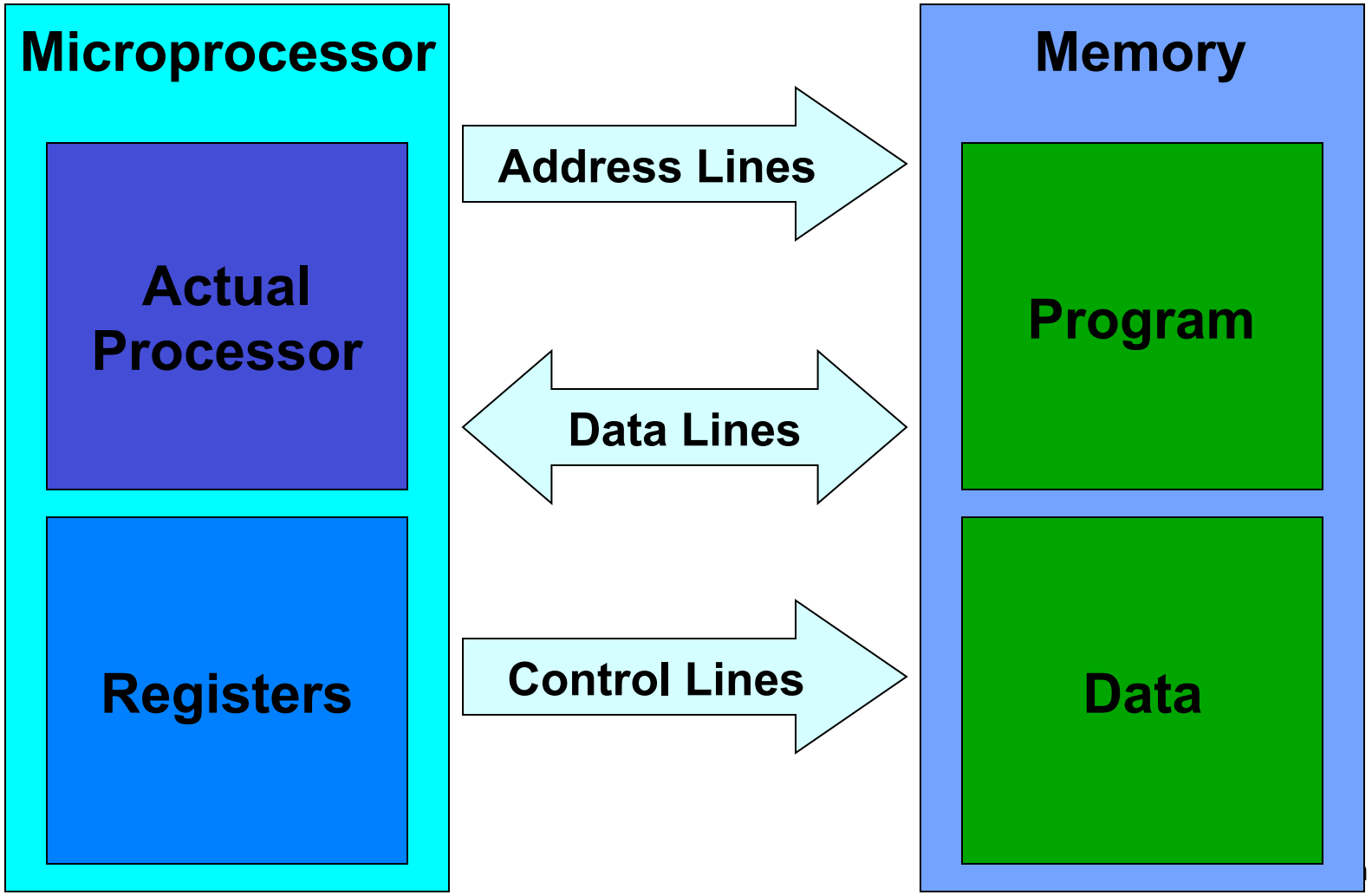
- **Pin configuration**
- **Minimal / Maximal mode**
- **Address latch enable**
- **Bi-directional data bus**

The Microprocessor

- An integrated circuit with millions of transistors interconnected with very small aluminum wires.
- Controls and directs activities of the computer.
- Execute stored programs.

Von Neumann Architecture

in some other architectures program and data are separated in 2 memories



The 8086 Family:the Late 1970's

- **Could address up to 1 mb of memory at a time when other CPU's could only address 64 kb.**
- **The 16 bit external bus too powerful.**
- **The 8088 replaced the 8086 and had only an 8 bit external bus.**
- **The 8088 CPU was the first chip used in IBM's microcomputers.**

- 8088
  - Data is organized into byte widths
  - The 1MB memory is organized as 1M x 8-bits
- 8086/80186
  - Data is organized into word widths
  - The 1MB memory is organized as 512k x 16-bits

The 80286 Family:1983

- **Wanted to make the 286 backward compatible with the 8088's.**
- **So had 2 modes:**
  - **Real mode-less powerful.**
  - **Protected mode-very powerful.**
    - » **Could access up to 16 mb of memory.**
    - » **Needed a special operating system.**
    - » **But most users only had DOS.**

پ 80286/80386SX

ت Data is organized into word widths

ت The 16MB memory is organized as 8M x 16-bits

The 386 DX: 1985

- **First true 32 bit chip, all buses 32 bits wide**
- **Capable of running in real mode, 286 protected mode and its own 386 protected mode**
- **In 386 protected mode it had** 2 new functions**:**
  - Virtual memory**- could use hard drive to pretend that computer had up to 4 GB of data!**
  - Virtual 8086- **8086 bubbles created for DOS**

- 80386DX/80486
  - Data is organized into double word widths
  - The 4GB memory is organized as 1G x 32-bits

The 386 SX:1988

- **How different from the 386DX?**
  - **External data bus reduced to 16 bits**
  - **Address bus reduced to 24 bits, which limited memory use to 16 mb**
  - **First popular laptops were based on the 386SX but was called the 386 SL and ran on 3.3 volts**

The 486DX:1989

- **How different from the 386 family?**
  - **A built in math coprocessor.**
    - » **Performs high math functions.**
  - **A built in 8K cache on same chip.**
    - » **This was an SRAM cache that stores code read in the past. When the CPU asks for the code again, it doesn't have to go to DRAM to get it.**

486SX:1991

- **Same as 486 DX except the math co-processor is disabled.**

The Pentiums:1993

- Had 64 bit external data bus that split internally as 2 dual pipelined 32 bit buses
- Supported an 8K write through cache for programs
- Most early Pentiums ran at 3.3 volts. This conserved heat. Voltage regulators on the motherboard can decrease voltage
- Includes clock doubling through the setting of jumpers

Recent Pentiums:after 1996

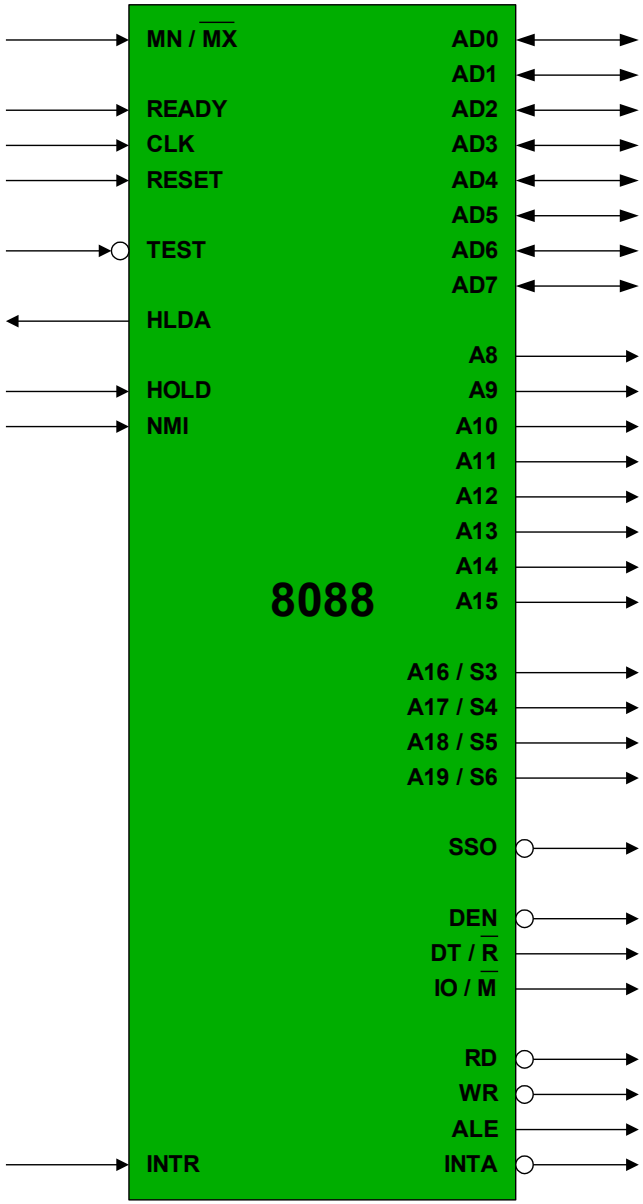
- **MMX- helps with multimedia products**
- **Increased multipliers/clocks**
- **Improved processing- better cache branch predicting**
- **Improved superscalar architecture**
- **SSE/SSE2 instructions**

- Pentium Pro/Pentium 1-4
  - Data is organized into quad word widths
  - The 4GB memory is organized as 512MB x64-bits
- (on P2-4, actual address bus is 36 bits)

8088 Microprocessor

Minimum Mode

Pin Configuration



Power and Ground Pins

- **Vcc – pin 40**
- **Gnd – pin 1 and 20**

Address Pins

- **AD0..AD7**
- **A8..A15**
- **A19/S6, A18/S5, A17/S4, A16/S3**

Data Pins

- **AD0..AD7**

Control Pins

- **MN/MX' (input)**
  - **Indicates what mode the processor is to operate in**
- **READY (input)**
  - **When given an input LOW, it will go into a wait state**
- **CLK (input)**
  - **Provides basic timing for the processor**
- **RESET (input)**
  - **Causes the processor to immediately terminate its present activity**
  - **To reset the microprocessor, this must be HIGH for at least 4 clock cycles**

Control Pins

- **TEST' (input)**
  - **Connect this to HIGH**
- **HOLD (input)**
  - **Connect this to LOW**
- **HLDA (output)**

Control Pins

- **INTR (input)**
  - **Interrupt request**
- **INTA' (output)**
  - **Interrupt Acknowledge**
- **NMI (input)**
  - **Non-maskable interrupt**

Control Pins

- **DEN' (output)**
  - **Data Enable**
  - **It is LOW when processor wants to receive data or processor is giving out data**
- **DT/R' (output)**
  - **Data Transmit/Receive**
  - **When HIGH, direction of data lines is from microprocessor to memory/devices**
  - **When LOW, direction of data lines is from memory/devices to microprocessor**
- **IO/M' (output)**
  - **Device/Memory**
  - **When HIGH, microprocessor wants to access I/O Device**
  - **When LOW, microprocessor wants to access memory**

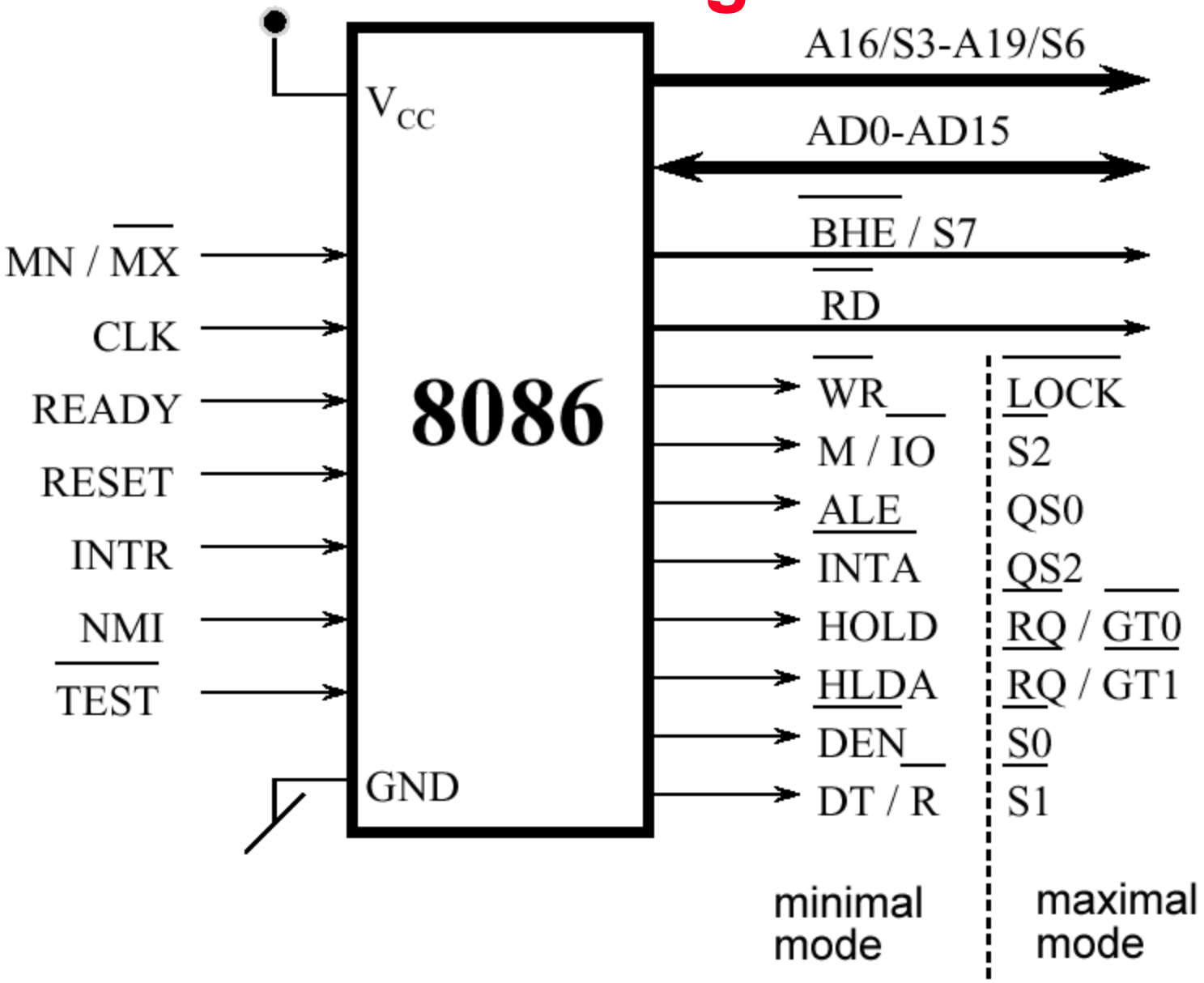
Control Pins

- **RD' (output)**
  - **When LOW, it indicates that the microprocessor is performing a read access**
- **WR (output)**
  - **When LOW, it indicates that the microprocessor is performing a write access**
- **ALE (output)**
  - **Address Latch Enable**
  - **Provided by the microprocessor to latch address**
  - **When this is HIGH, microprocessor is using AD0..AD7, A19/S6, A18/S5, A17/S4, A16/S3 as address lines**

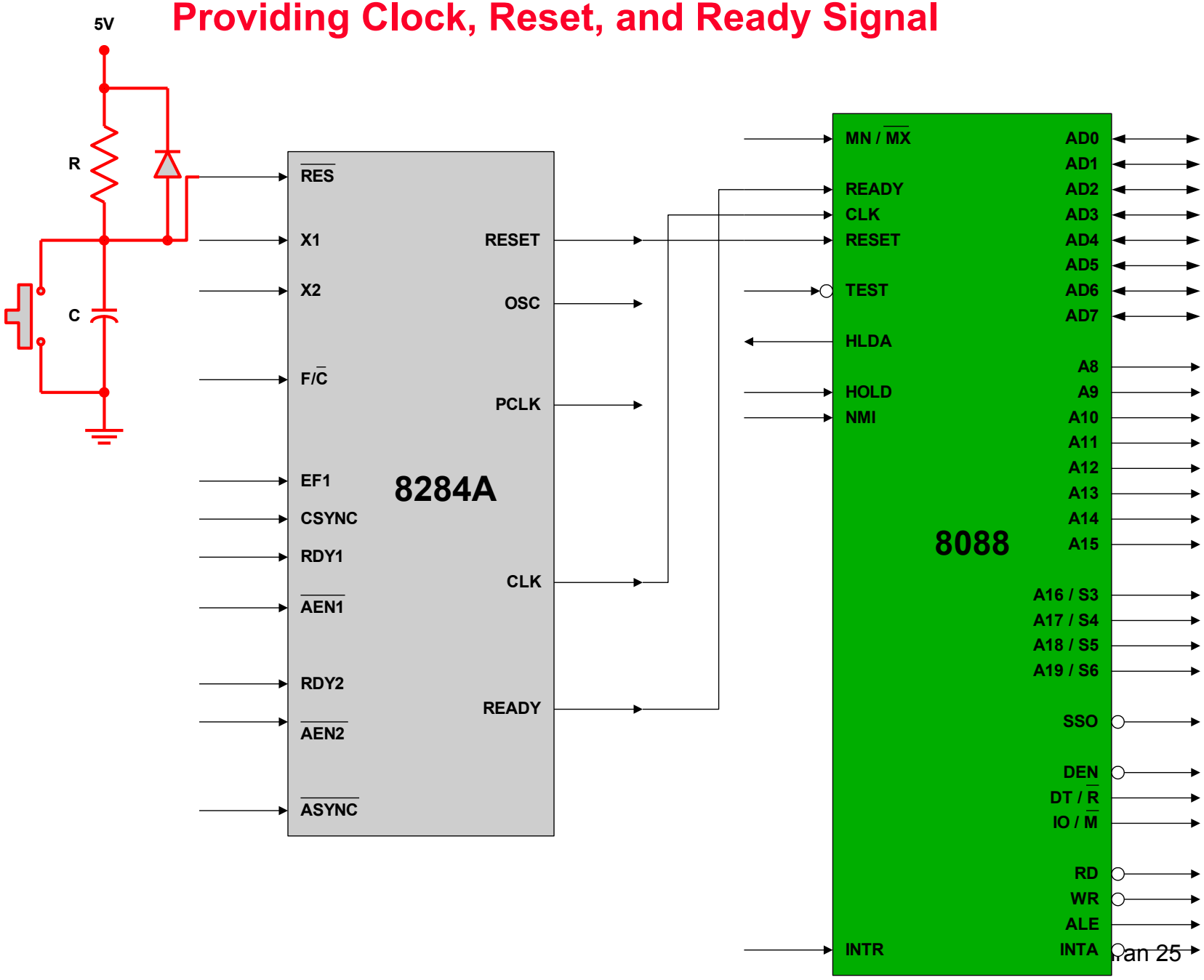
Clock Signal

- needed by the microprocessor to synchronize signals
- ideally a square wave having a constant frequency

8086 Signals



Providing Clock, Reset, and Ready Signal



Minimum Mode