UNIVERSITY OF TEHRAN

School of Electrical and Computer Engineering

Digital Logic Design Laboratory, ECE 045, Fall 96

Course Regulations

Discipline:

- Students should be present at the beginning of the lab sessions. Arriving 10 minutes late can be tolerated for up to three times in the semester. Beyond that, every 10 minutes delay will be penalized by 10% of the lab experiment grade.
- Coming to lab after 45 minutes from start of a session is considered as an absence.
- Students who miss a lab session will lose the portion of the experiment grade that corresponds to that particular session.
- Three missed laboratory sessions will be reported as a failed grade.
- Use of cellphone is prohibited during the labs (except for taking snapshot, or as a paperweight) and violators will be asked to leave the lab and marked as a missed lab.

Grading Policy:

- The course consists of 5 experiments (12 sessions).
- Grade of each experiment has 4 parts:
  - Prelab (10%)
  - Quiz (5%)
  - Labwork (60%)
  - Report (25%)
- Prelab: A prelab consists of answering questions in the lab worksheet. Prelabs should be done individually and must be in good and correct Farsi.
- Labwork: Labwork is what the students should do during the lab sessions and is clearly stated in the lab worksheet.
- Report: After completing an experiment, students should write a report consisting of four major parts:
  - **Abstract**: in which a summary of the entire experiment is reflected in one or two paragraphs.
  - **Methodology and procedure**: in which the flow of labwork and the procedure that you followed for reaching the results should be presented. In this part, equipment used, parts used, and wiring and breadboarding should be discussed. You should describe the design process (not limited to implementation), ideas and the reasoning behind the decisions you had to make. Furthermore, the use of simulation tools (if any) and device programmers and synthesis tools should be mentioned.
  - **Results**: in which measurement and / or simulation results should be mentioned. Note that the results should include the waveform of simulations and screenshots of circuits and snapshots of waveforms, seen on the scope. Also the reported results should be discussed and justified in the report.

- **Conclusions**: in which you document what you have learned and why things work the way they do. Discuss the reasons behind discrepancies in actual and simulation results. Also make a discussion of why you think what was presented in this lab experiment is important and why you need to learn this. As part of your conclusions, include a paragraph discussing questions that you were asked by the TA during the lab session, and the answers you provided. If corrections to your answers were made, include those as well.

- Reports should be done in groups (one report for every group of two students) and should be in typed format, and must be in good and correct English.
- Do not copy paste anything to your reports (even from lab instruction). Also do not include source codes and schematics of your design.
- You should upload your reports and design files(only Verilog files and schematics) in this format: "D_M_G.doc" and "D_M_G.zip"
  - 'D' is '0' for Saturday sections, '1' for Sunday sections, '2' for Monday and '3' for Tuesday sections.
  - 'M' is '0' for afternoon sections and '1' for evening sections.
  - 'G' is the number of your group in your section.

- Upload deadline for Lab files/Report is the day you deliver your project.
- Upload of 'Report' and 'Lab files' is ANDed with the grade you take from your report and work in lab; meaning if you don't upload them you will get '0' mark.

Code of ethics:

- It is assumed that the students will follow the engineering ethics. In case of violation, such as prelab/lab/report sharing, appropriate measures will be taken.