Microprocessor System Design
DRAM Interfacing

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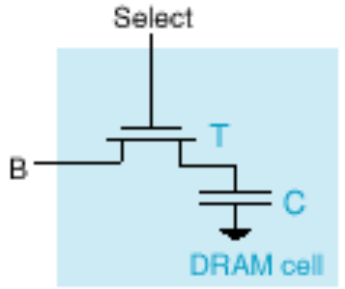
Outline

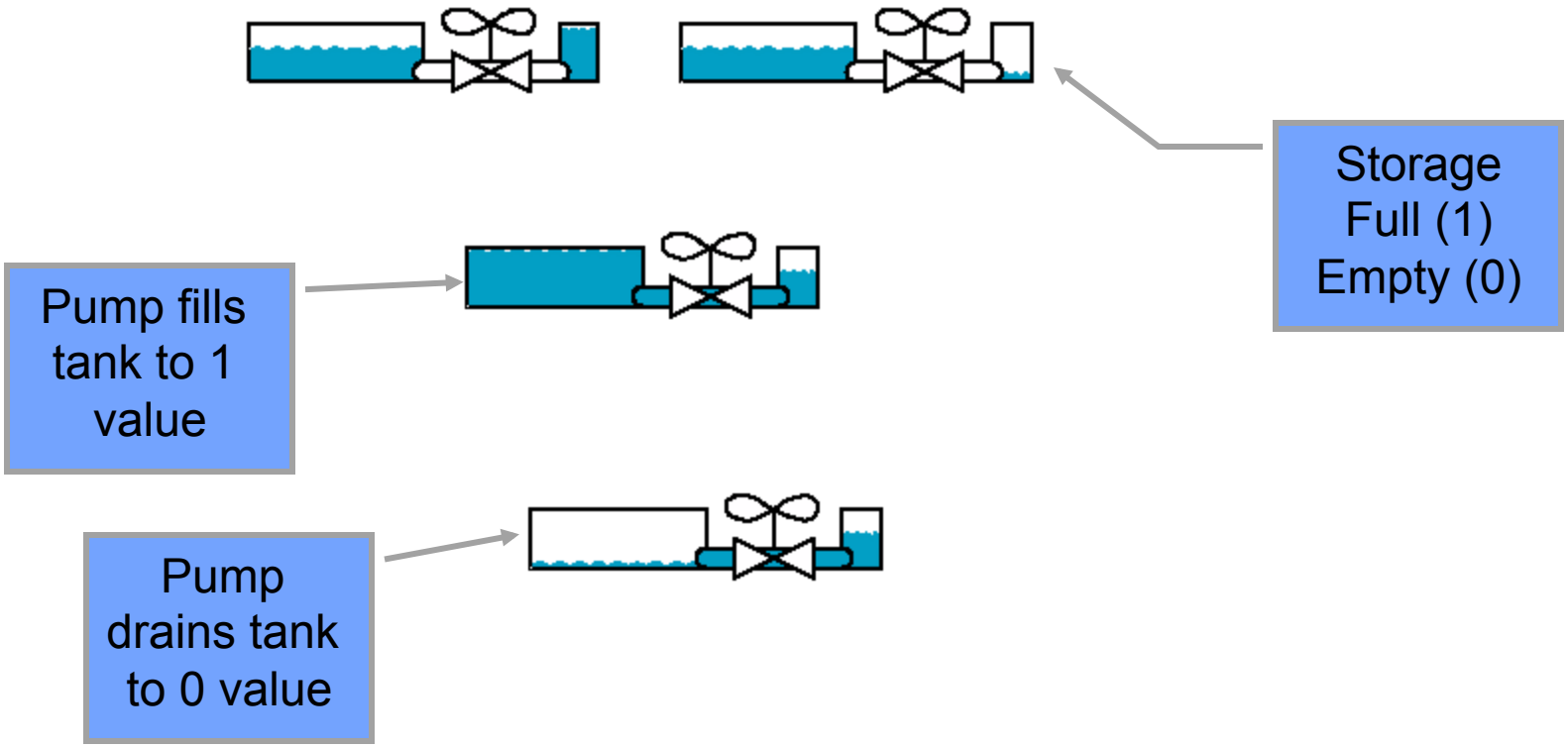
- A Dynamic cell
- Reading / Writing DRAM
- RAS / CAS signals
- DRAM in PC
  - RAS, CAS and address select generation
  - Address multiplexing
- Wait state generation for IO access

Dynamic RAM



- Capacitor can hold charge
- Transistor acts as gate
- No charge is a 0
- Can close switch & add charge to store a 1
- Then open switch (disconnect)
- Can read by closing switch
  - Sense amps

Hydraulic Analogy



Reading

Outside water begins at intermediate level (black wavy line)

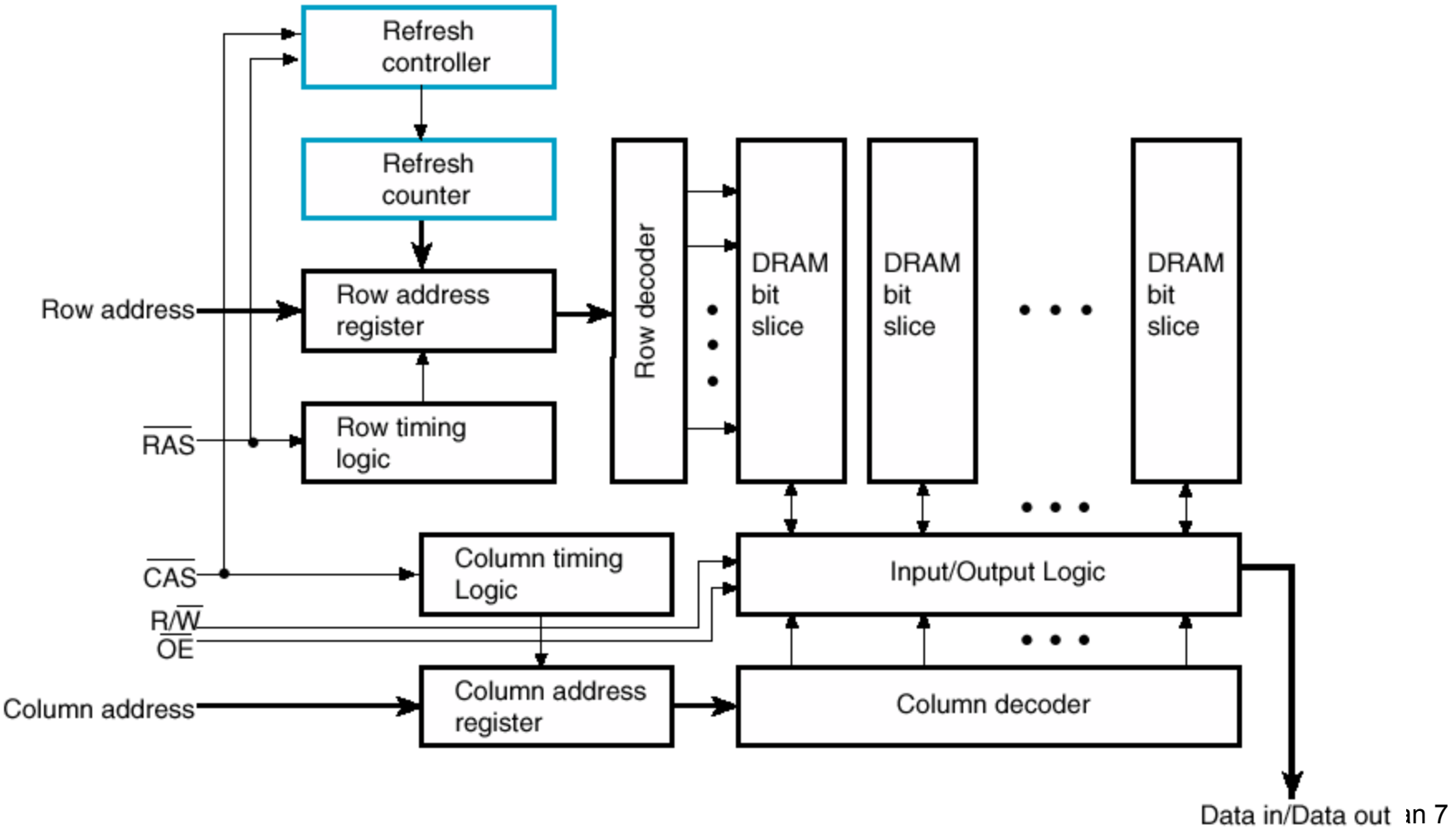
Tank had a 1 value – raises water level

Tank had a 0 value – lowers water level

DRAM Refreshing

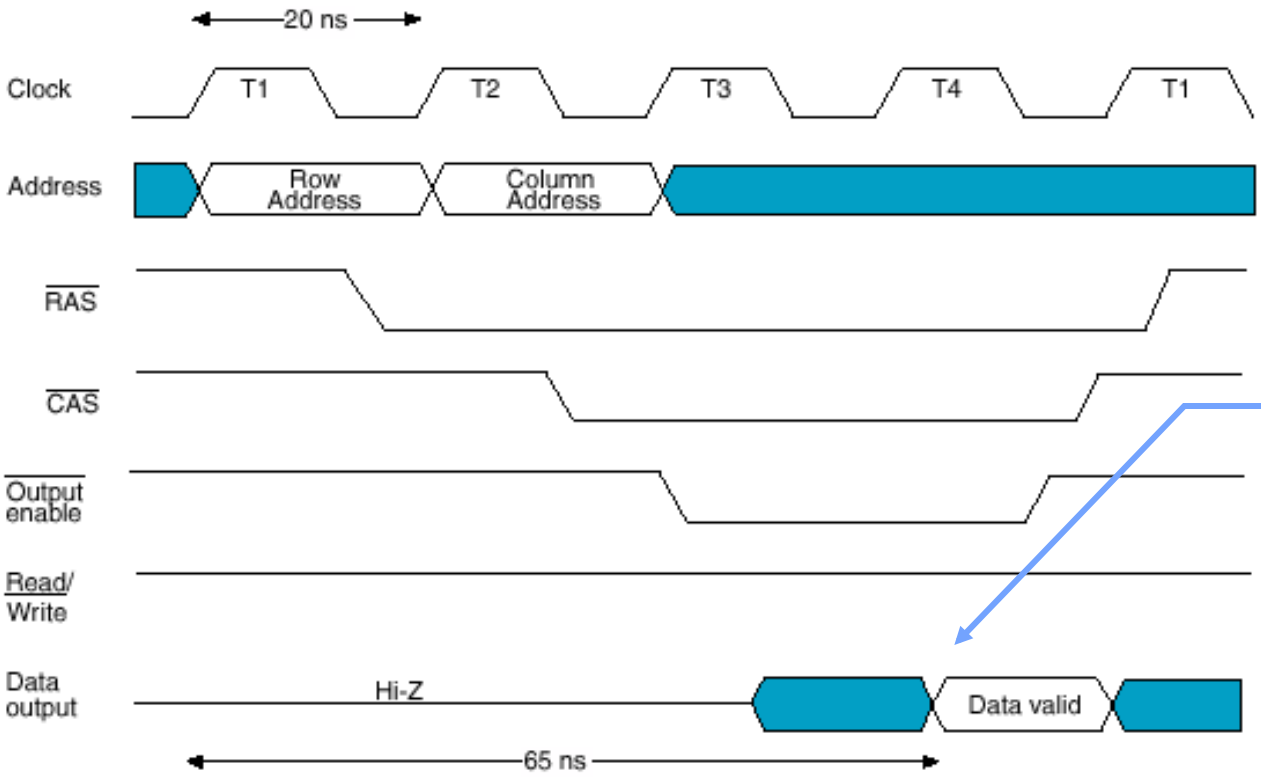
- **Refresh**
  - **Destructive read**
  - **Also, there's steady leakage**
  - **Charge must be restored periodically**

DRAM Logical Diagram



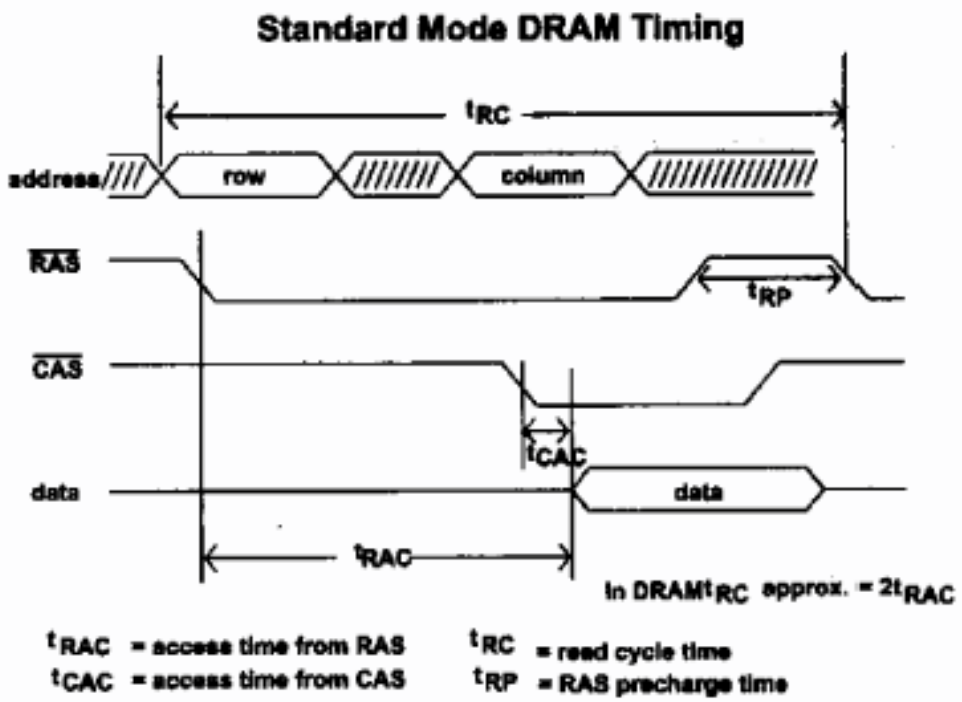
DRAM Read Signaling

- **Lower pin count by using same pins for row and column addresses**



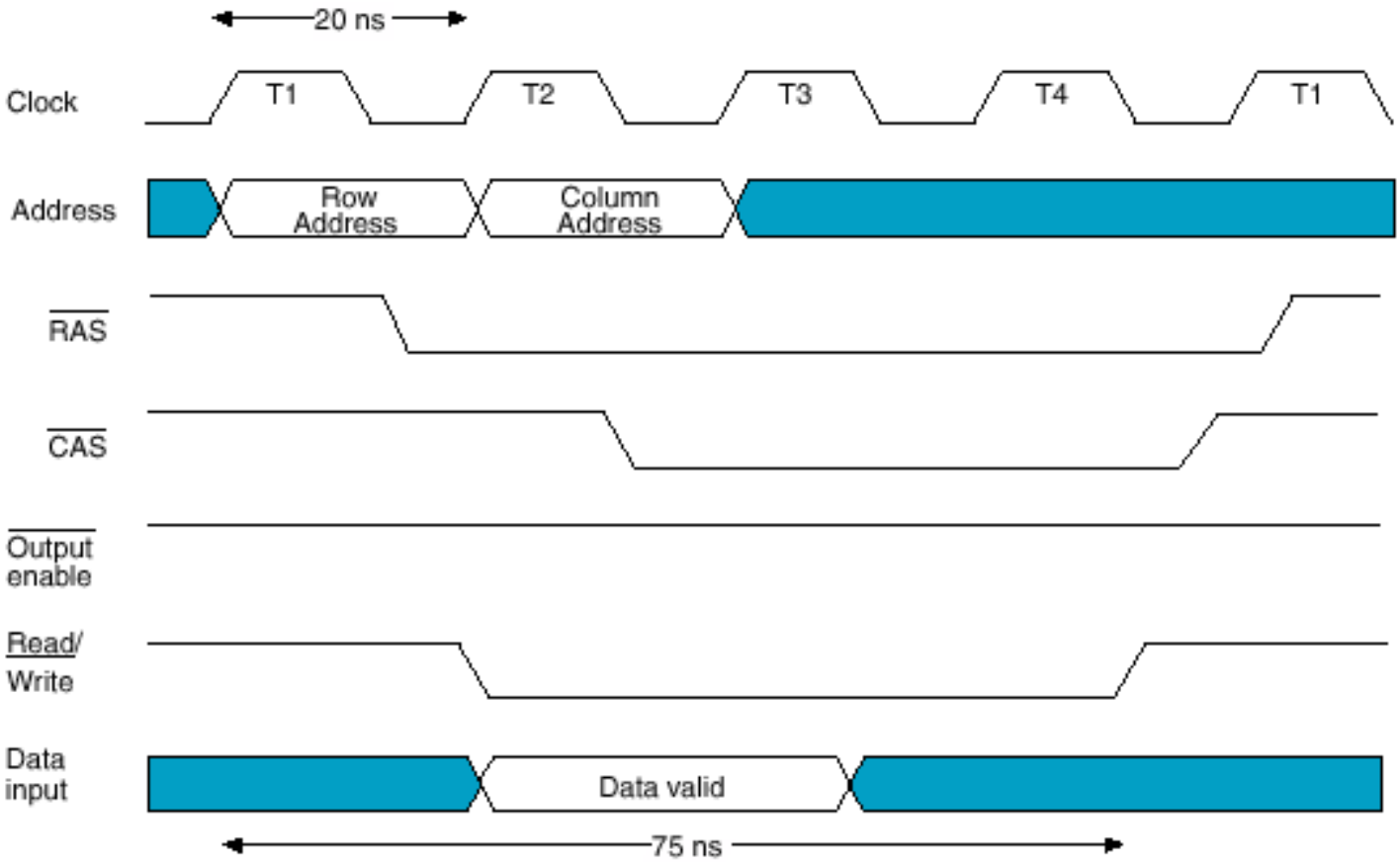
Delay until data available

Standard DRAM Timing

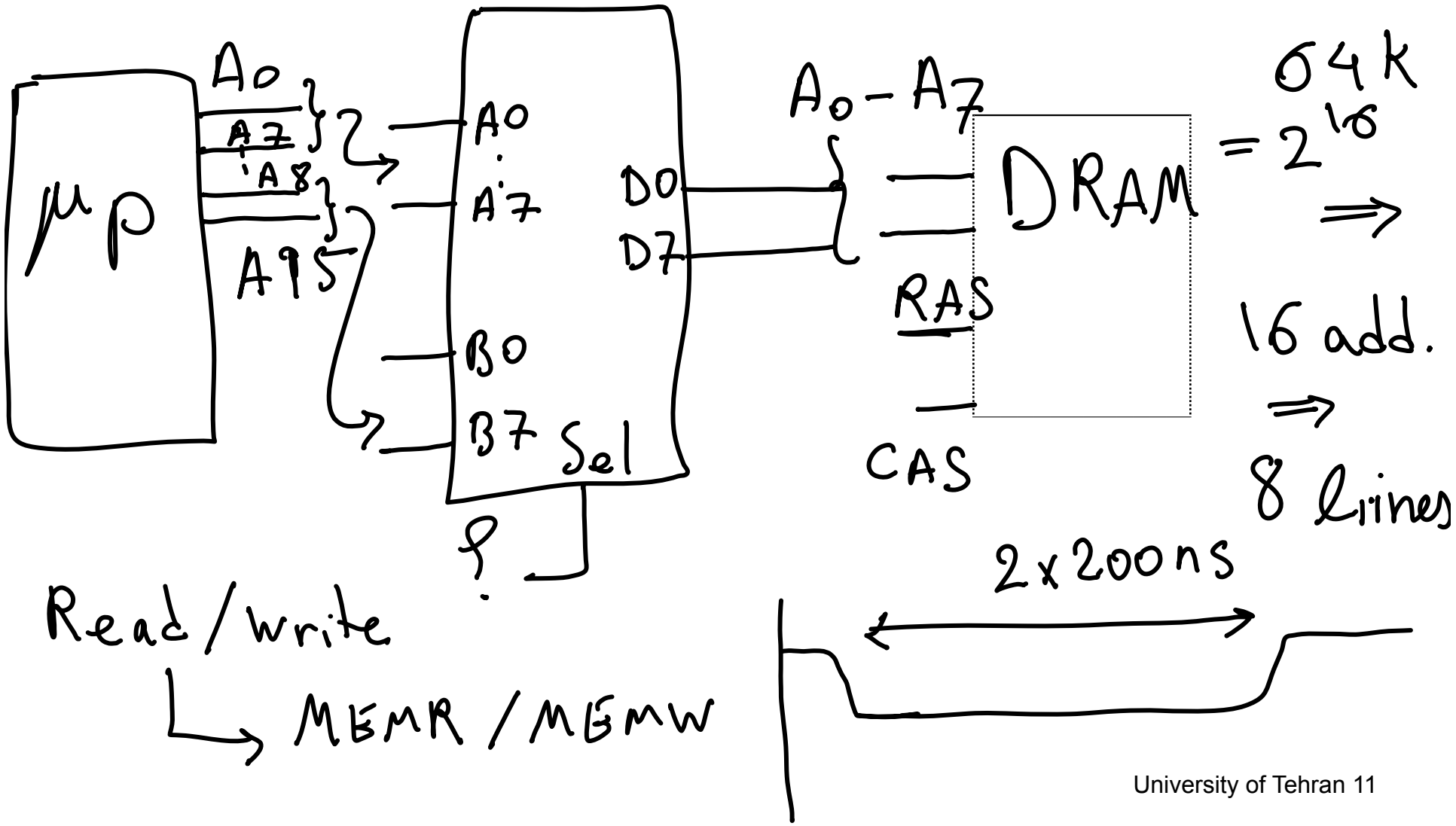


DRAM	RAS Access (t_{RAC}) (ns)	Read Cycle (t_{RC}) (ns)	RAS Precharge (t_{RP}) (ns)
MCM44100-60	60	110	45
MCM44100-70	70	130	50
MCM44100-80	80	150	60

DRAM Write Timing



DRAM Address Select

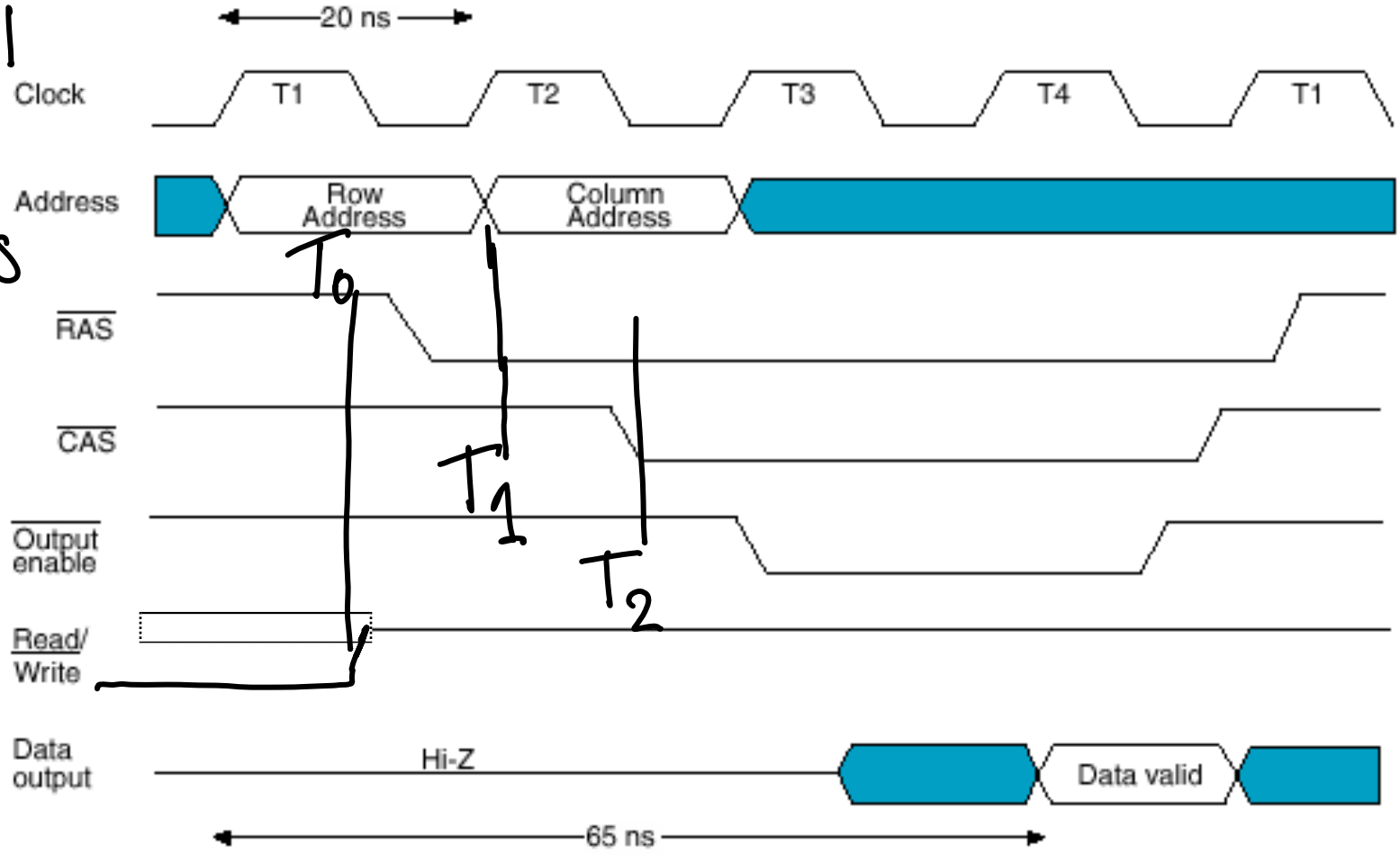


DRAM Timing (signal generation)

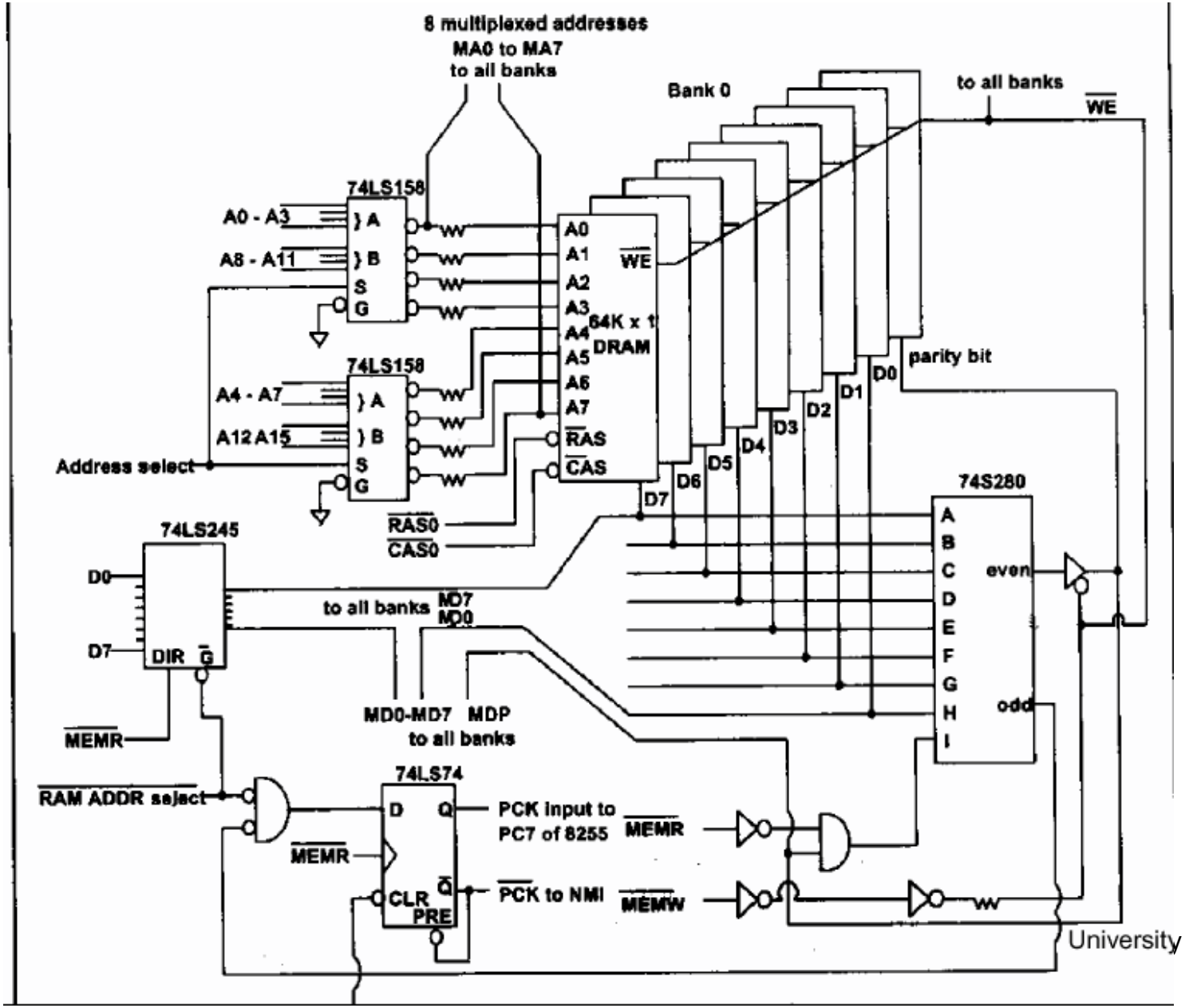
T_0 : Row, Read, RAS

T_1: Col

T_2: CAS



DRAM Connections in PC



Parity?

PC RAM Interface

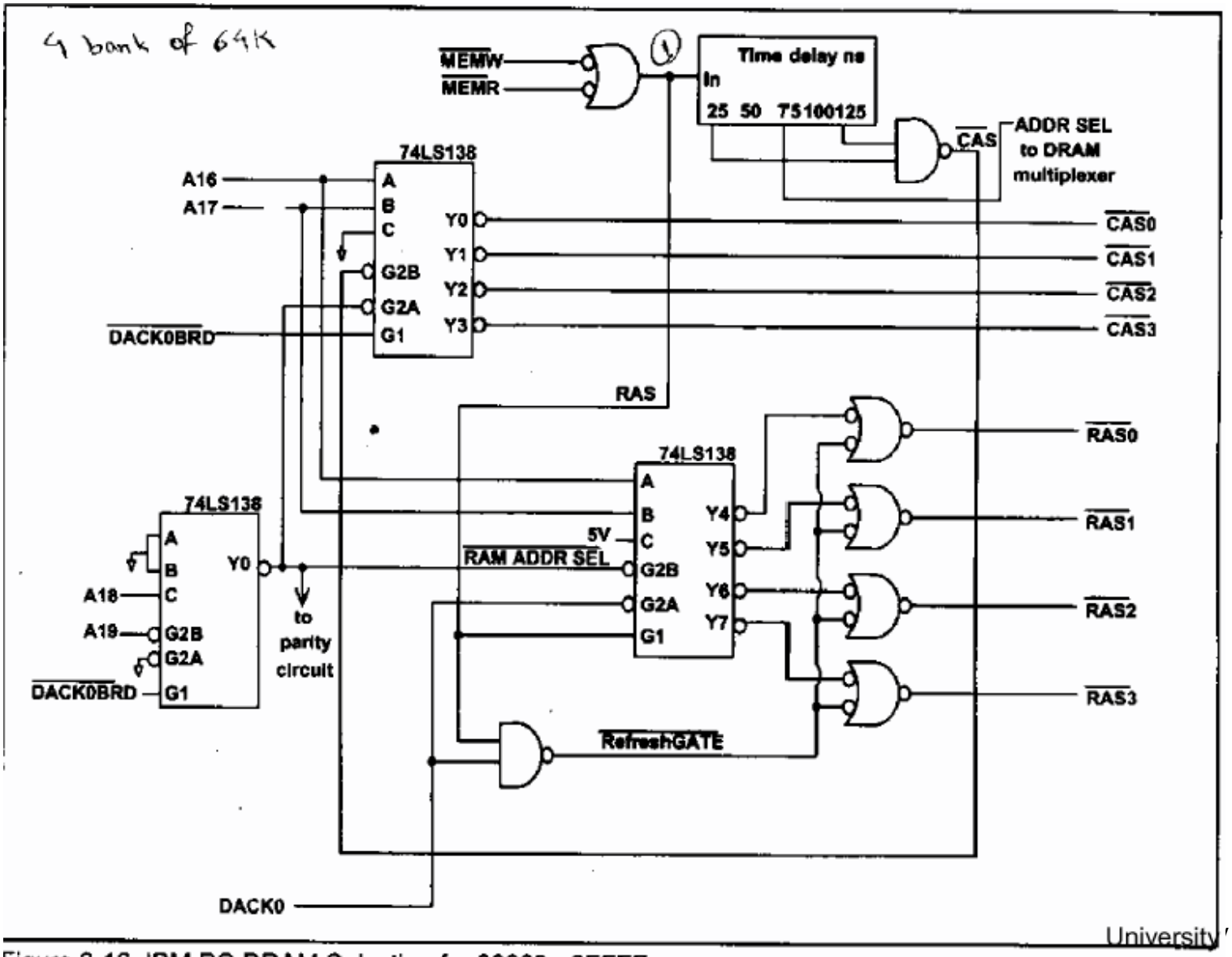


Figure 3-16. IBM PC DRAM Selection for 00000 - 3FFFF

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Wait State Generation

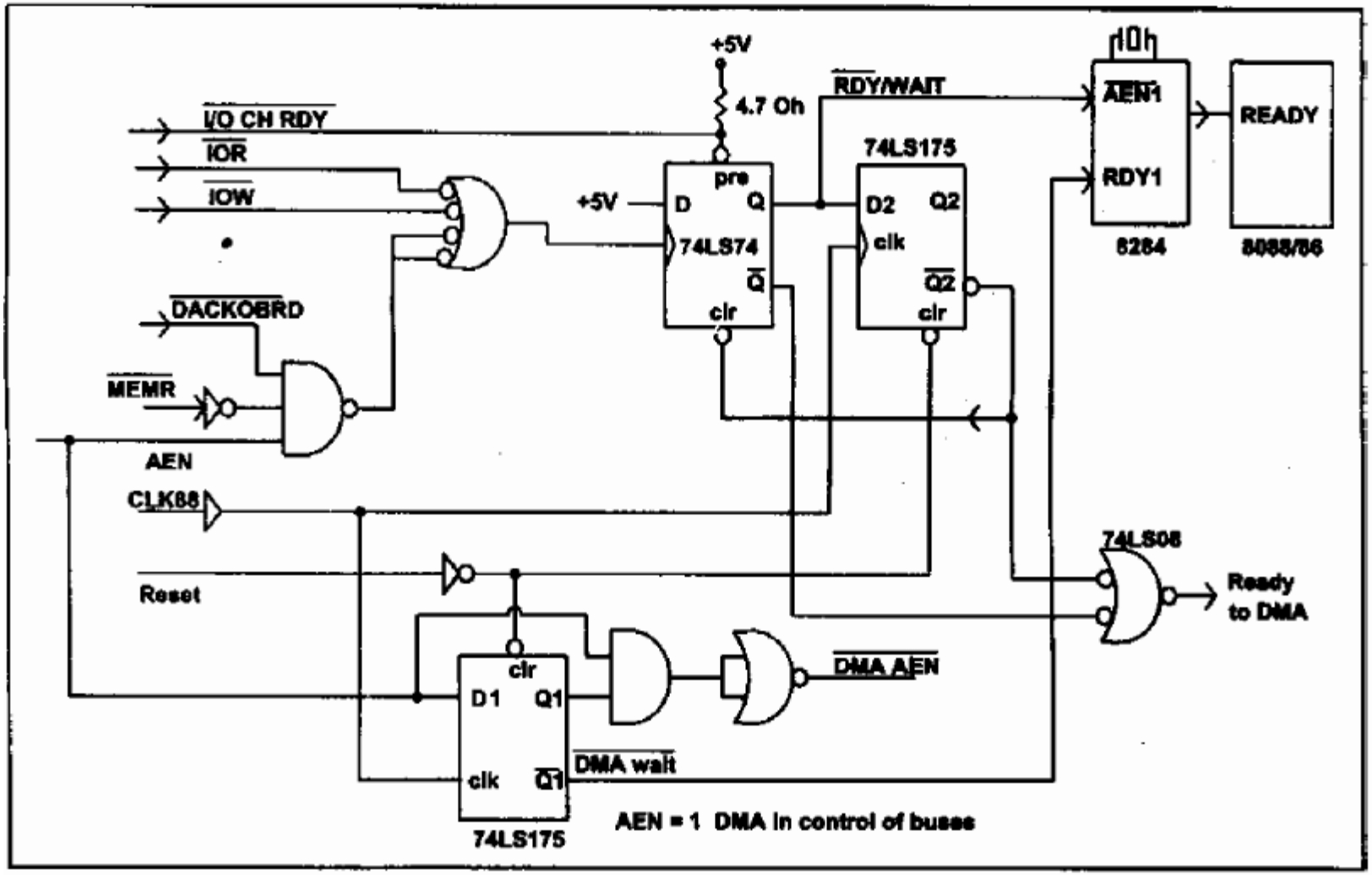

Figure 3-21. Wait-State Generation Circuitry

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DRAM Refresh

- Many strategies
- Logic on chip
- Here a row counter