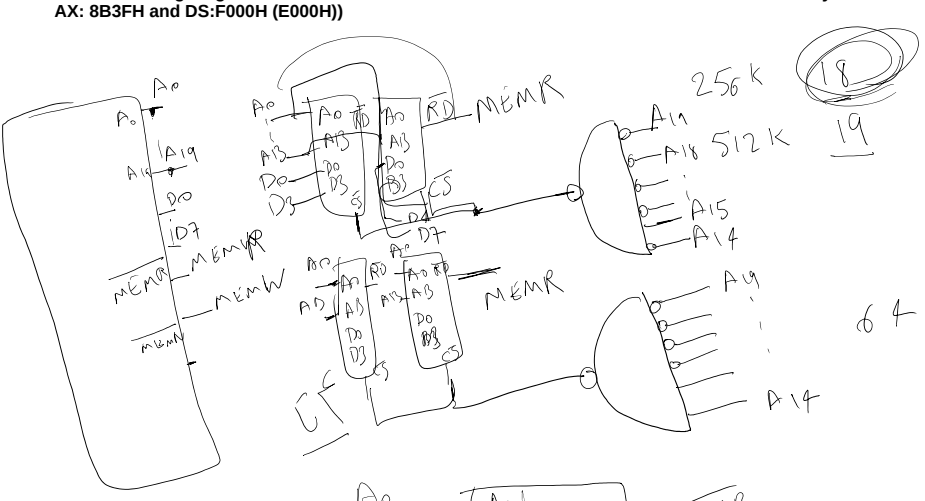
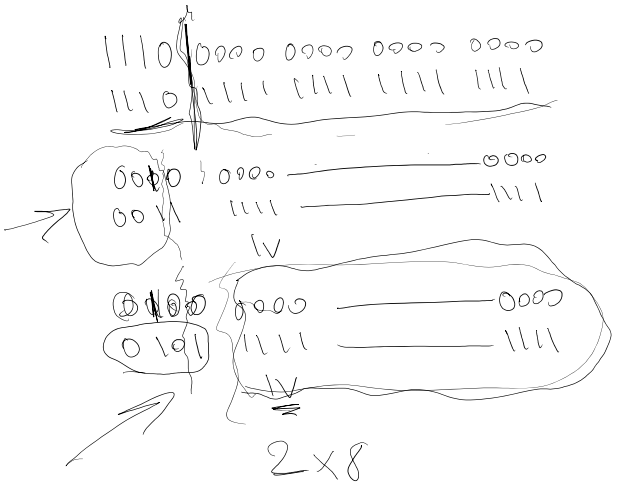
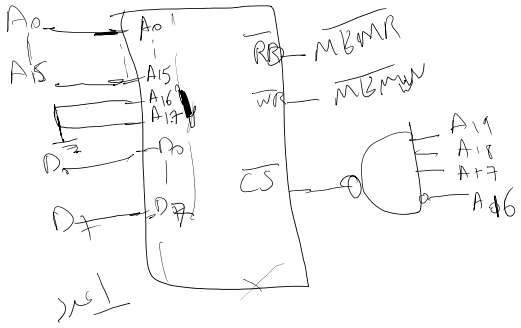
1. **What is the problem with partial decoding?**
2. **There are four types of memory modules:**
   - **16k x 4 bit ROM for 28000-2FFFF (08000 – 0FFFF)**
   - **256k x 8 bit SRAM for F0000-FFFFF (E0000 – EFFFF)**
   - **512k x 2 bit SRAM for 00000-1FFFF (20000 – 3FFFF)**
   - **64K x 1bit SRAM for 60000 – 7FFFF (40000 – 5FFFF)**
   1. **How many modules are required from each type for an 8088 processor.**
   2. **Design the circuit.**
3. **for 8086:**
   4. **Repeat the problem (how many modules and design)**
   5. **Draw the timing diagram of 8086 for the execution of this instruction and show which memory modules will be activated (MOV [300H],AX – where AX: 8B3FH and DS:F000H (E000H))**

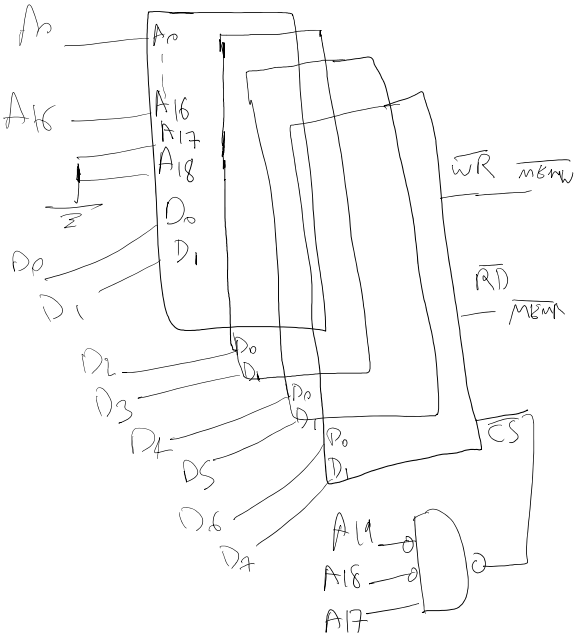




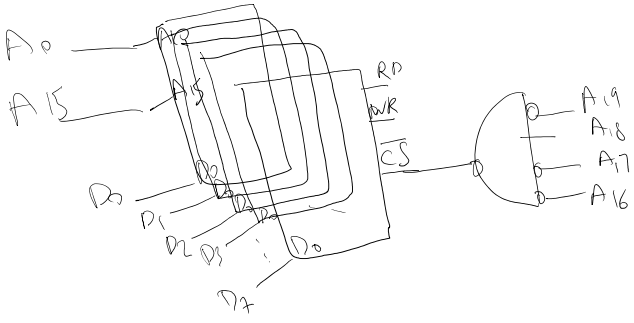
256k x 8 bit SRAM for F0000-FFFFF (E0000 – EFFFF)

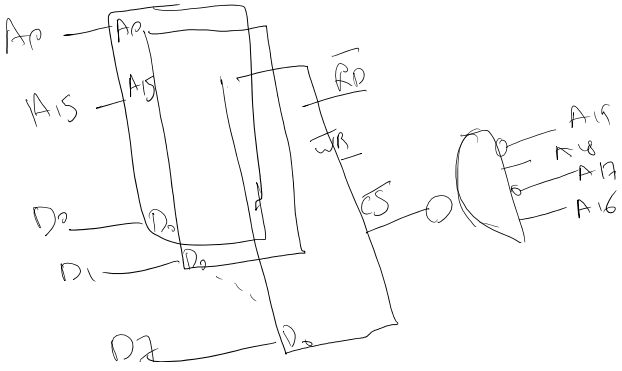


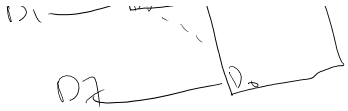
- **512k x 2 bit SRAM for 00000-1FFFF (20000 – 3FFFF)**



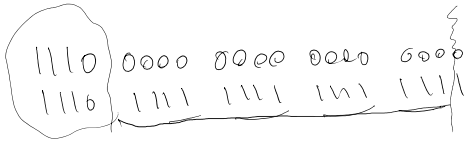
- **64K x 1bit SRAM for 60000 – 7FFFF (40000 – 5FFFF)**

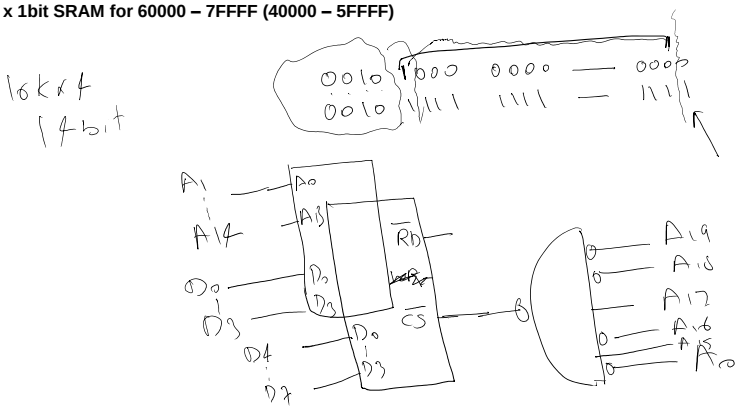


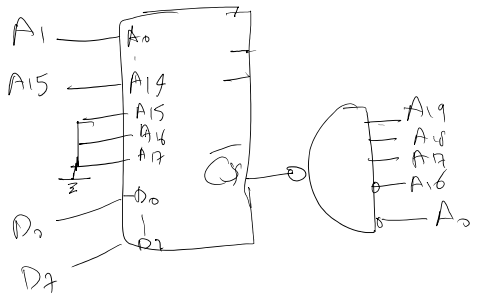


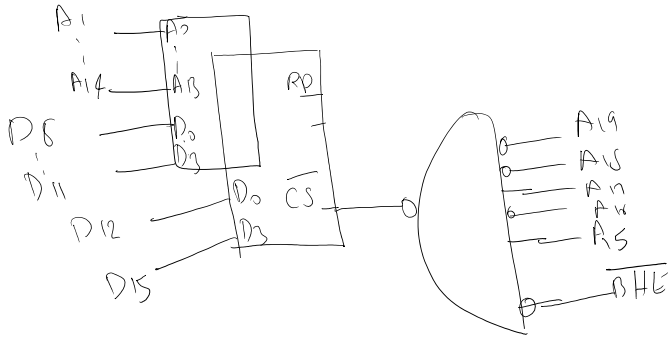


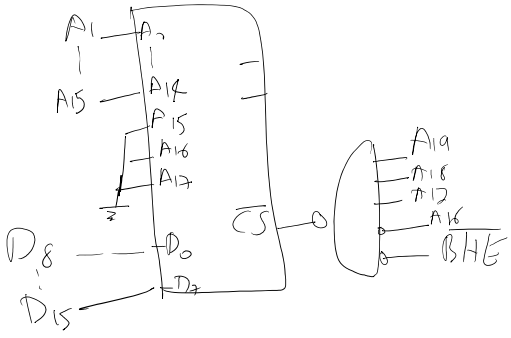
- **for 8086:**
- **16k x 4 bit ROM for 28000-2FFFF (08000 – 0FFFF)**
- **256k x 8 bit SRAM for F0000-FFFFF (E0000 – EFFFF)**
- **512k x 2 bit SRAM for 00000-1FFFF (20000 – 3FFFF)**
- **64K x 1bit SRAM for 60000 – 7FFFF (40000 – 5FFFF)**



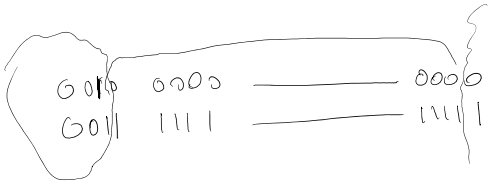


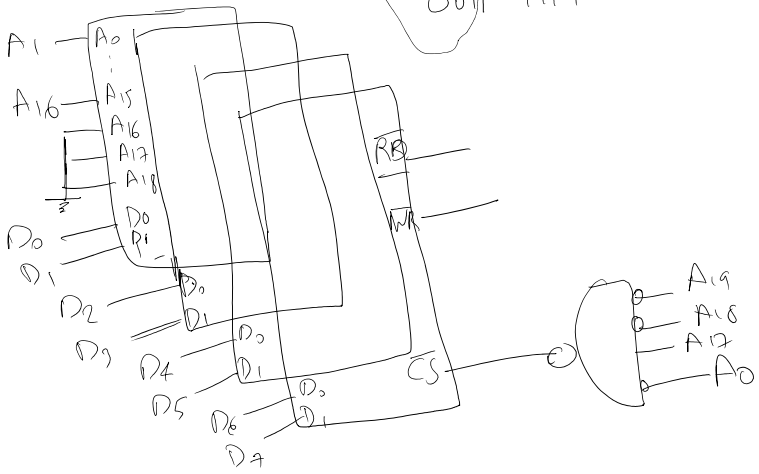


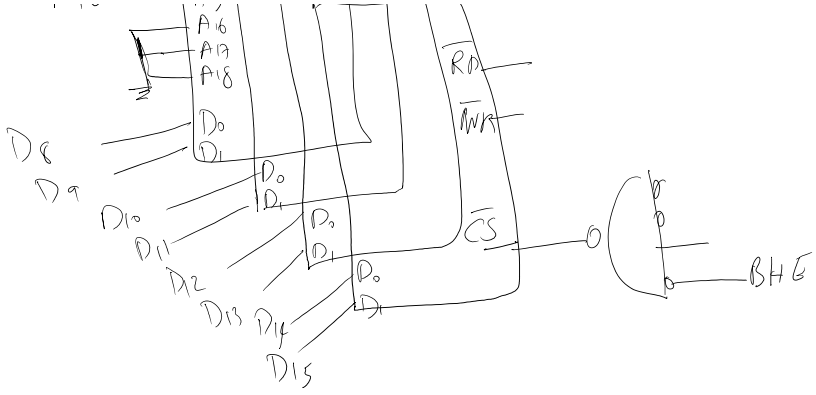




512k x 2 bit SRAM for 00000-1FFFF (20000 – 3FFFF)







. 64K x 1bit SRAM for 60000 – 7FFFF (40000 – 5FFFF)