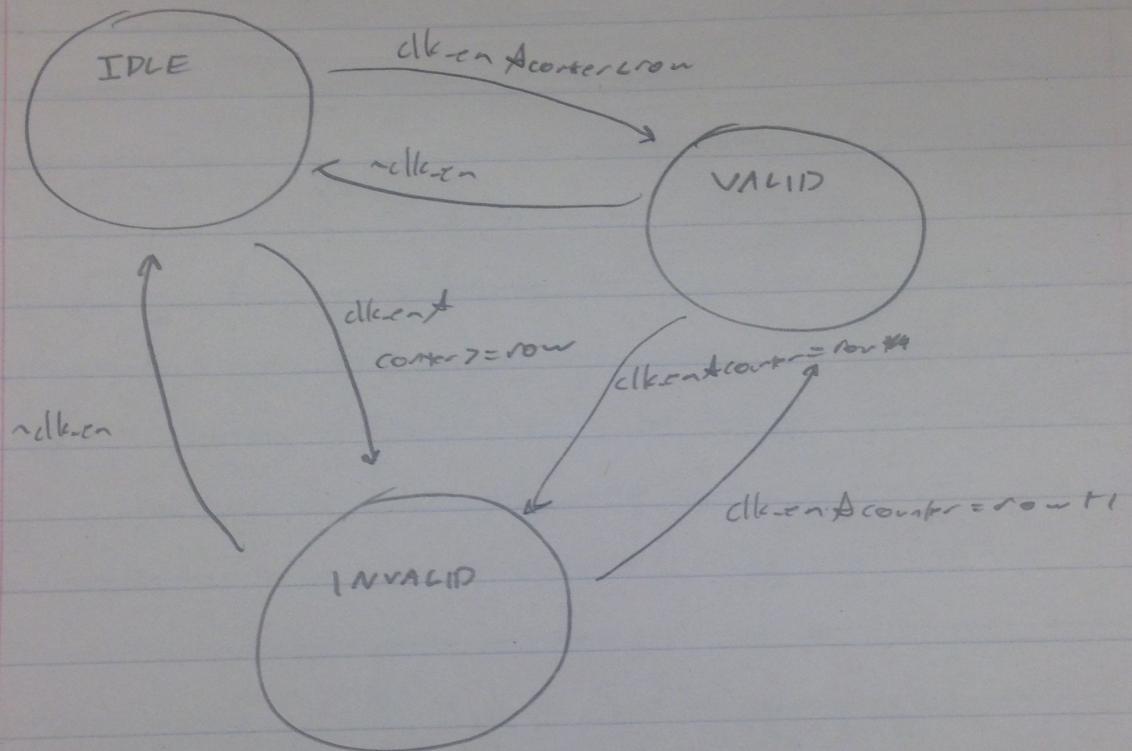
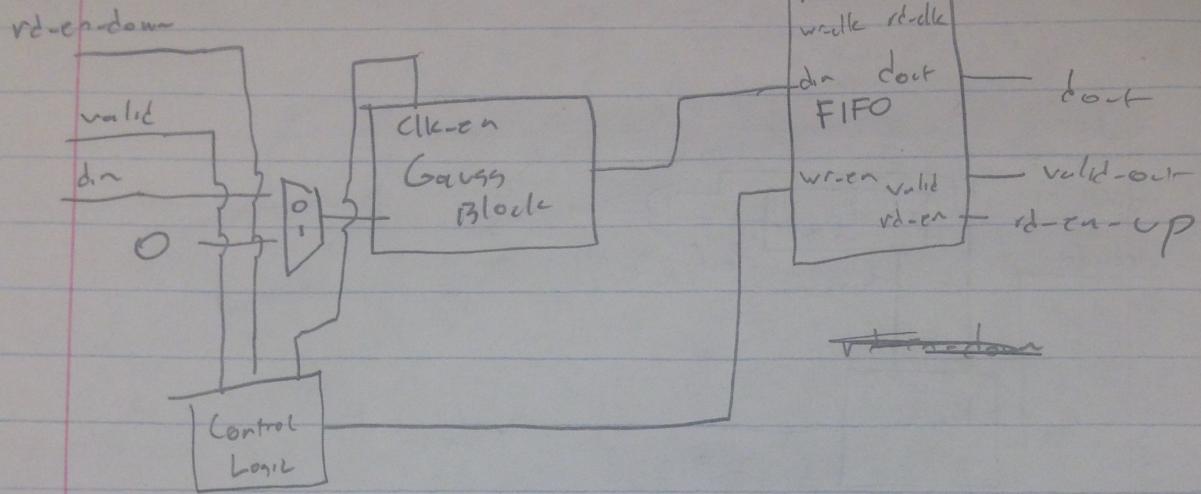


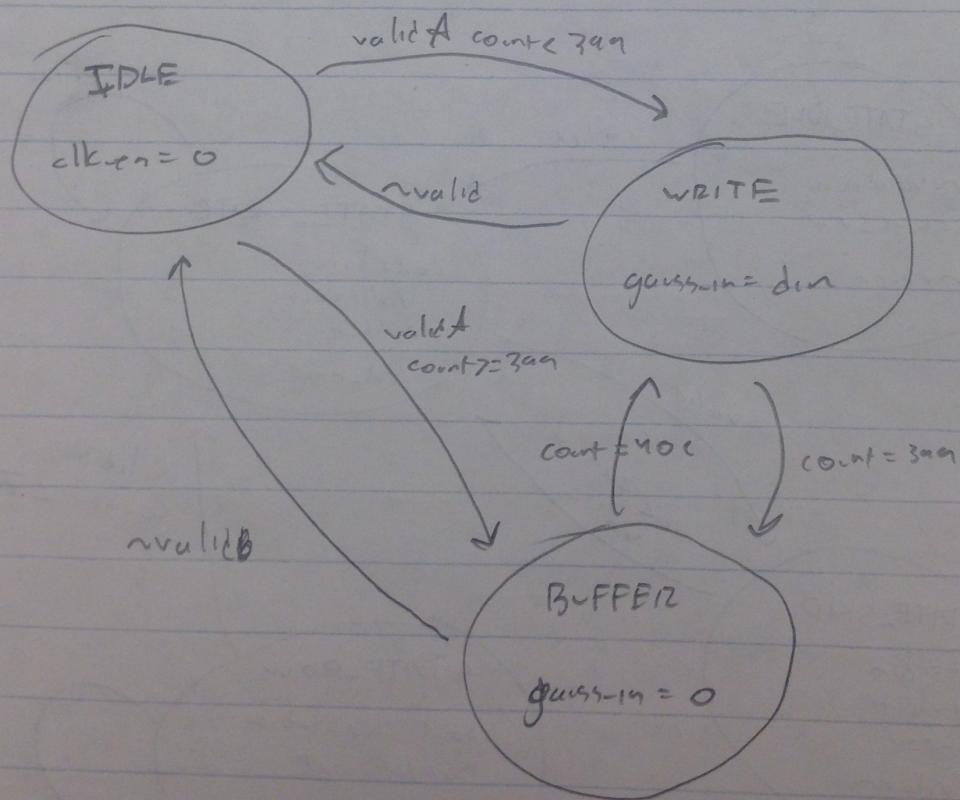
Output Control Logic



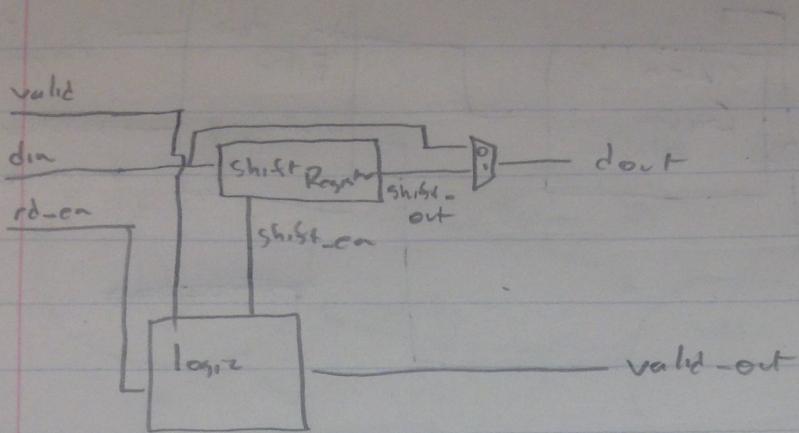
Gaussian



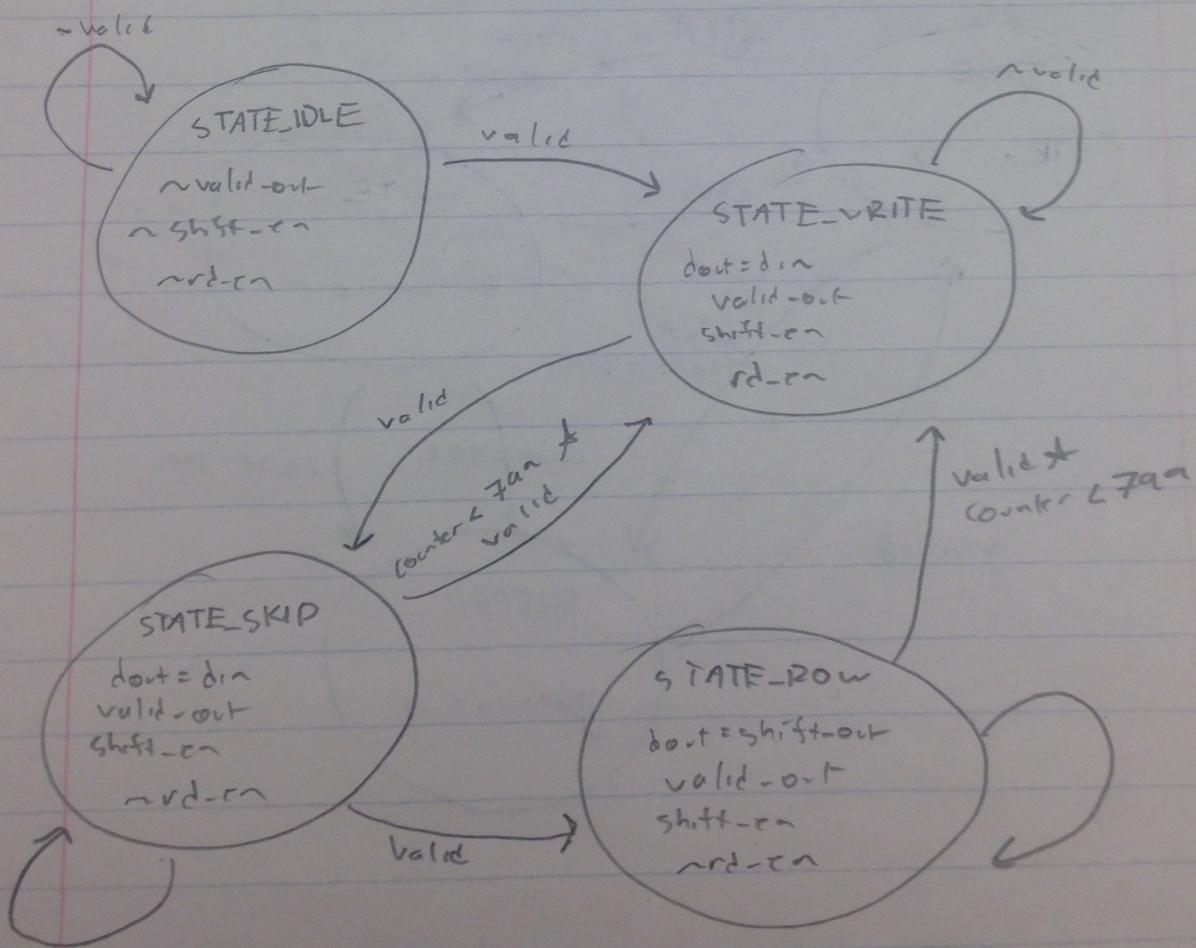
Input Control Logic



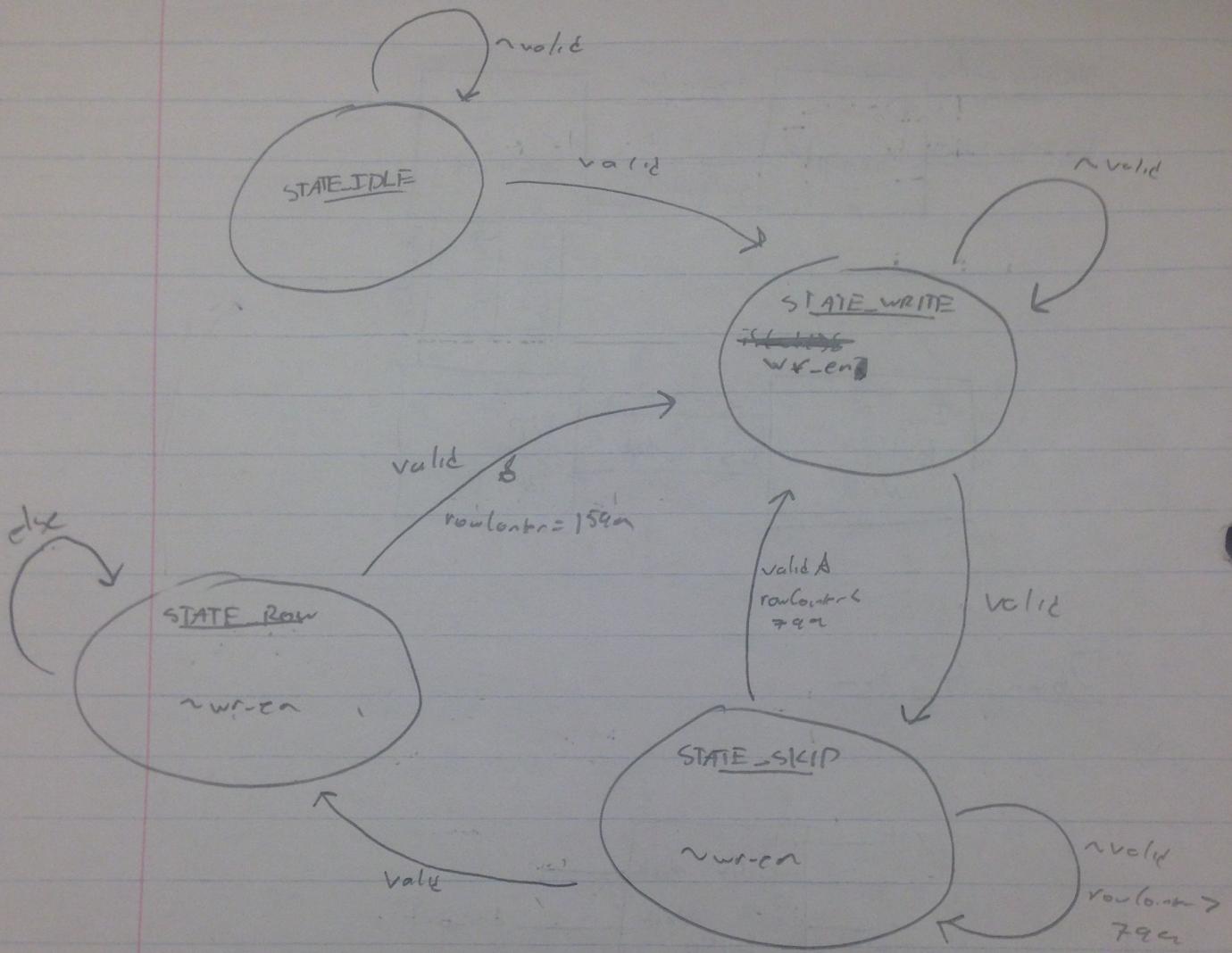
Up Sampler



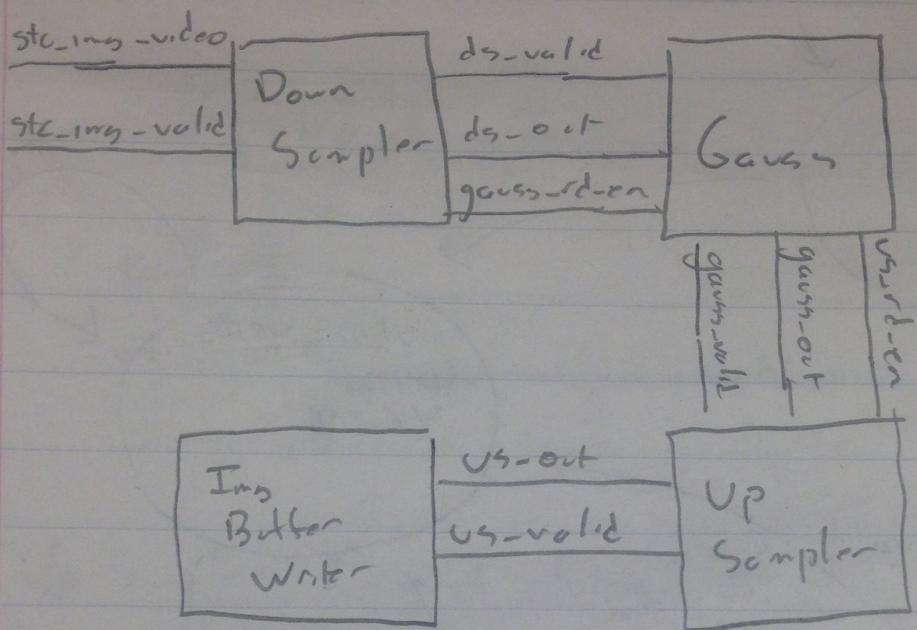
Up Sampler Control State Diagram



Down Sampler State Diagram



Overview



Down Sampler

