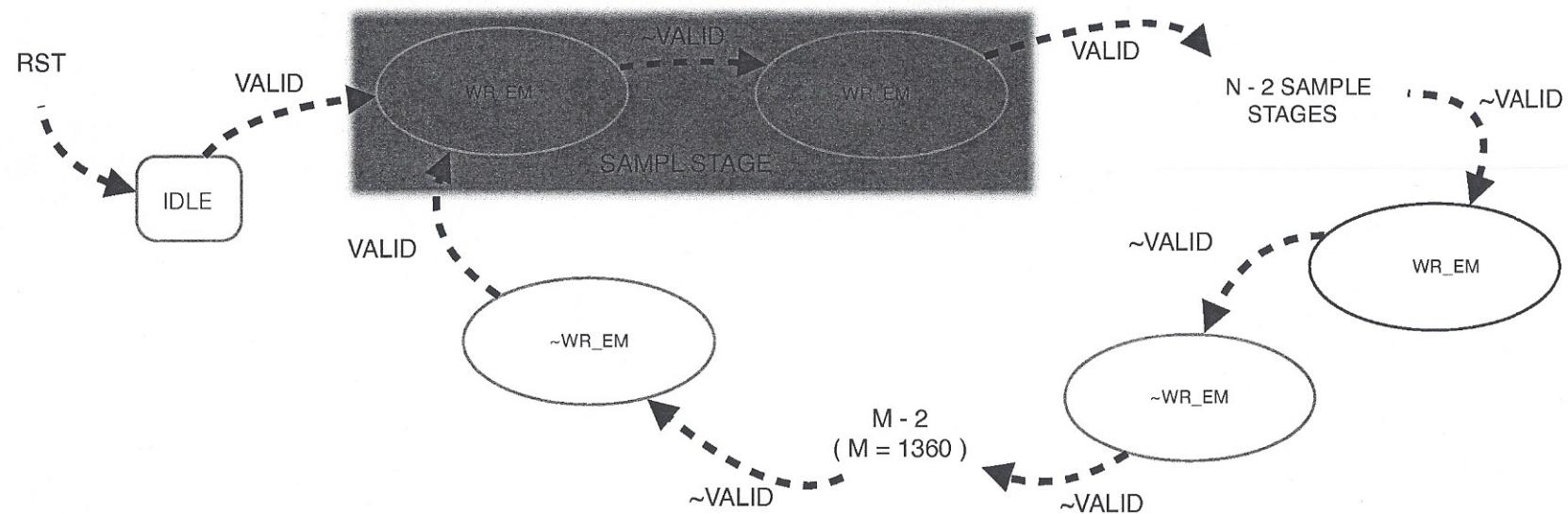
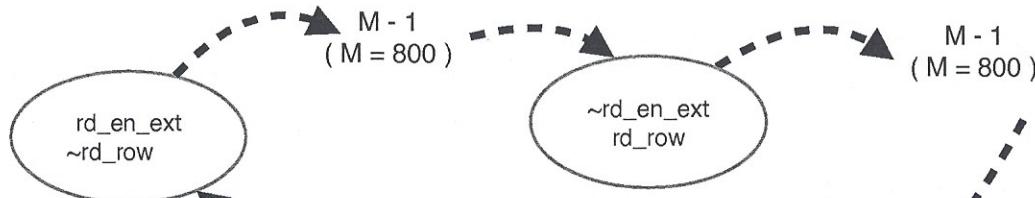


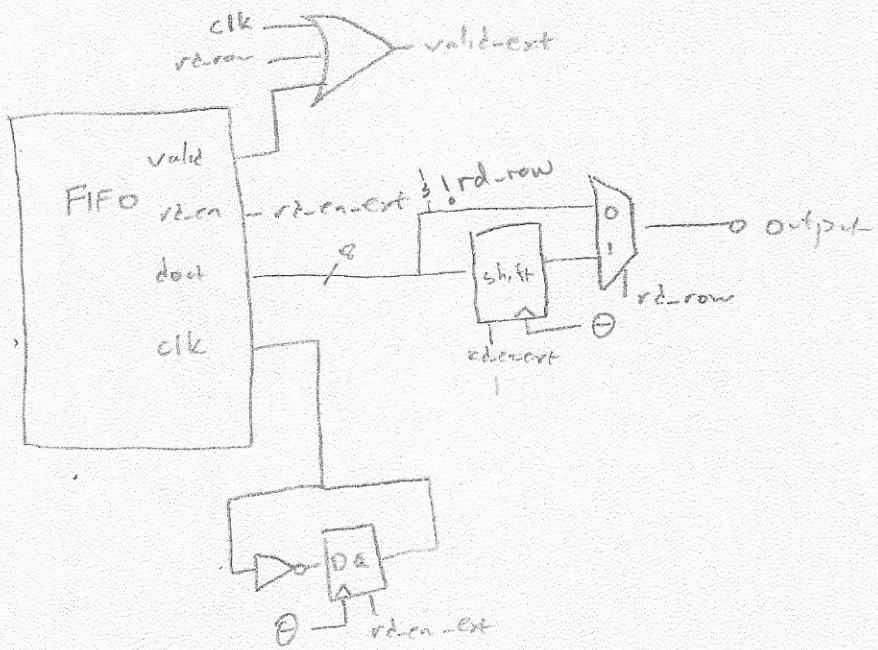
## Down Sampler



## Up Sampler



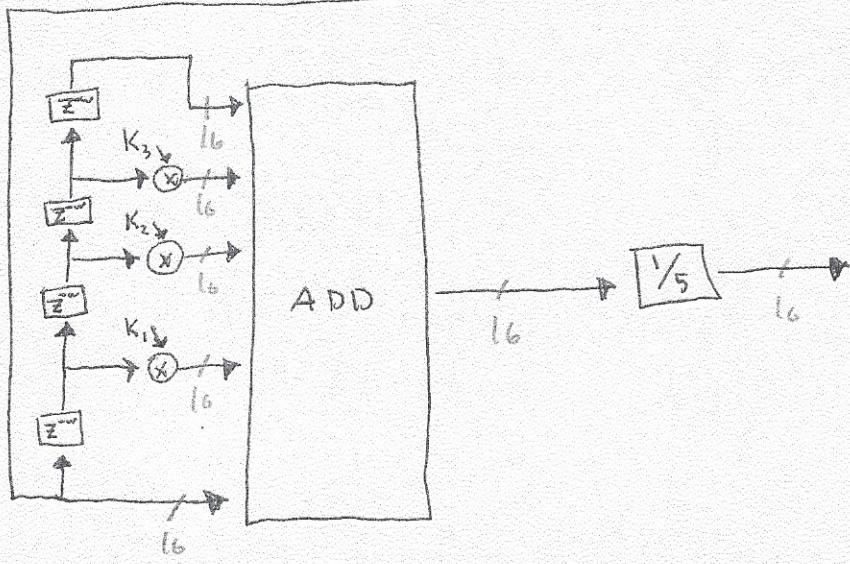
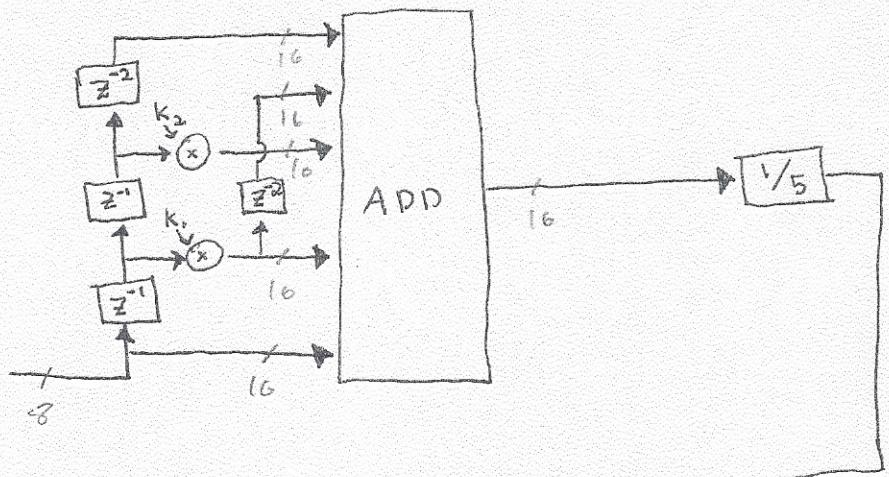
## Up Sampler



*R. Müller*

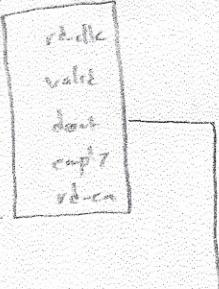
\* Need to count row and assert rd-row after  
going across a whole row

Gaussian Filter.

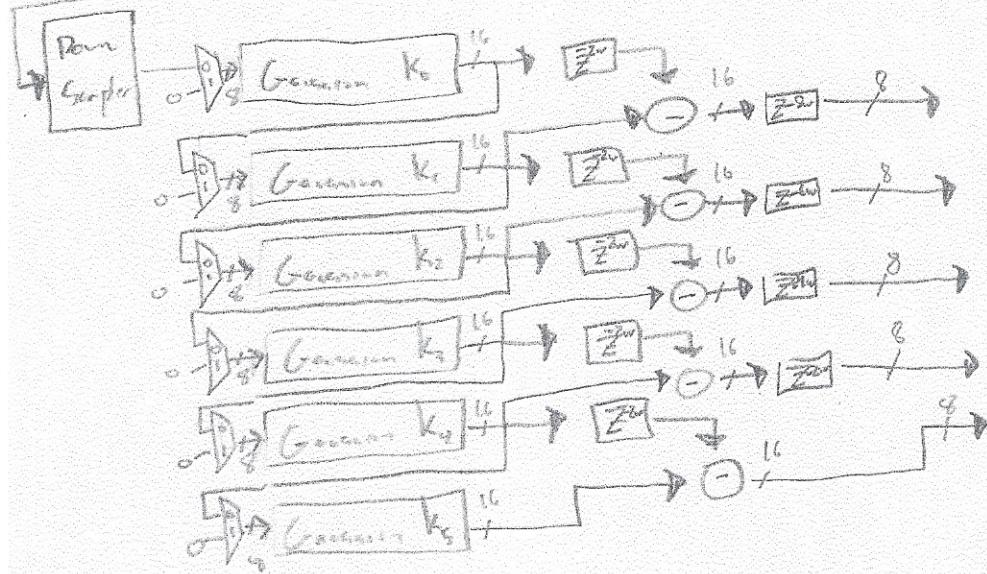
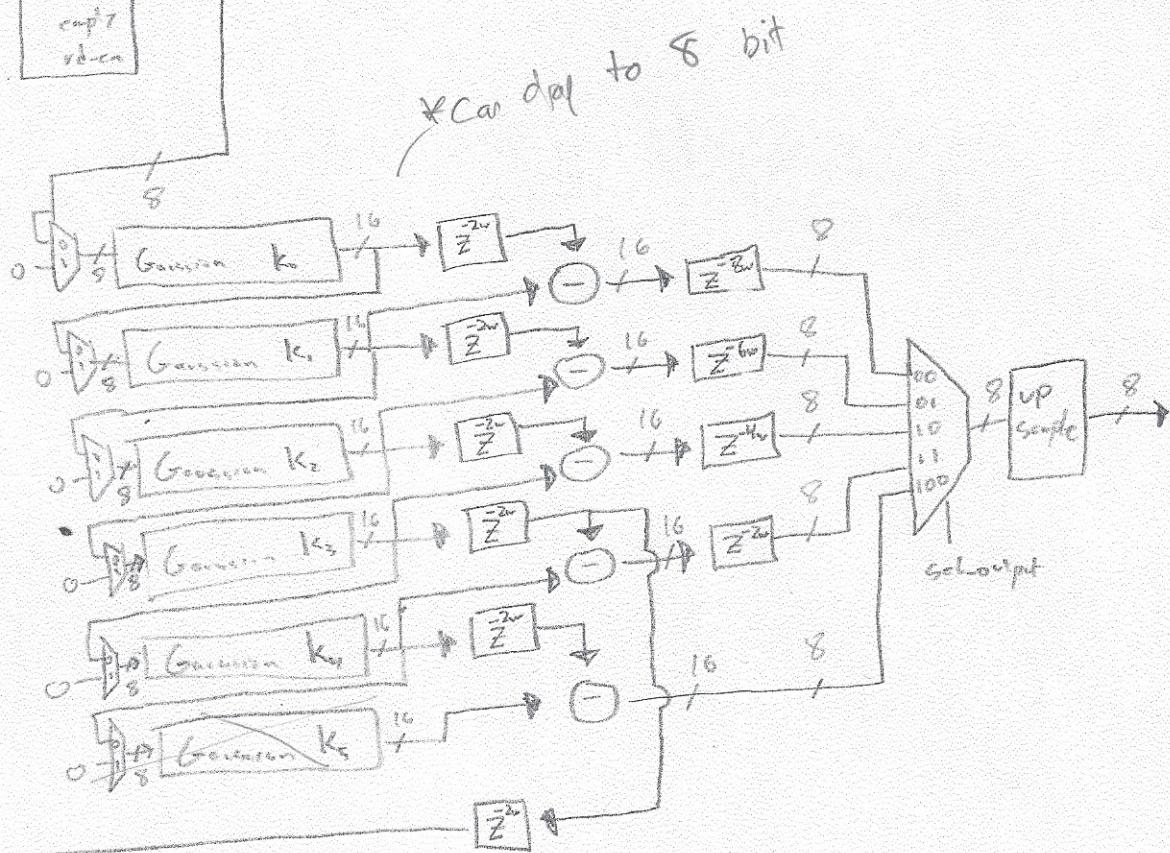


Yahya M. Al-Bayati

Down sampler

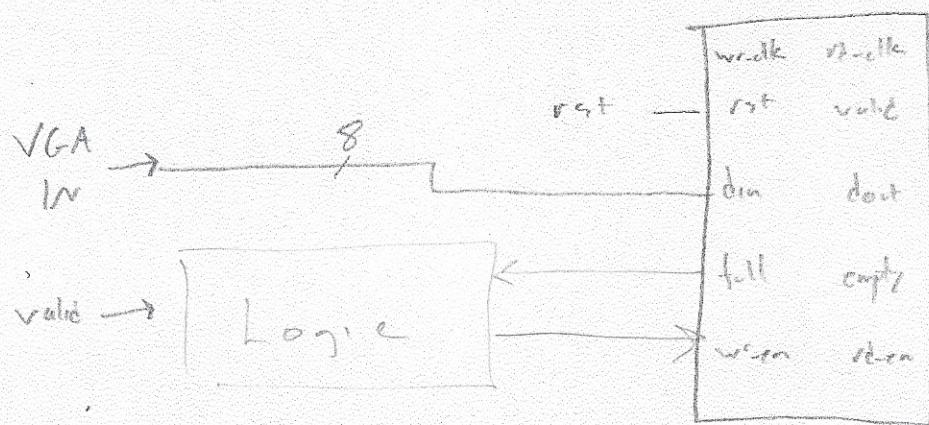


## Dog Module



TJ Hiltz

## Down Sampler



- Control word handle writing only every other pixel every other row.

Rec:

X	X	X	X	X	X	X
X	X	X	X	X	X	X
X	X	X	X	X	X	X

T. M. Wilcox

## DoG Module

For the added '0's needed for padding in the Gaussian Filter muxes will be used. For the incoming signal for test a VGA input may be used. This is possible due to the added buffer used for each row. Additionally, the test input will be able to be used, this will add a notch layer which can be used for test. The Computer can be passed and analyzed. For the input will be assumed to be a VGA input.

### Test

② Take known pic and run through a matlab rep. 1/3 compare bit by bit with 1/3 of Gaussian 1/3 for DoG.

Gaussian 1/3  
① Input a solid color to see if the same solid color is seen on the output.

Down Sampler: Take known input of pixels and retrieve the correct pixels after the filter has omitted the correct pattern.

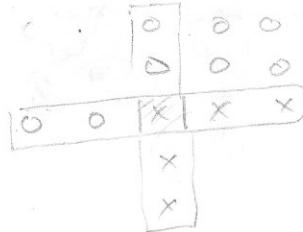
Up Sampler: Take the known sample and verify that it expands and gets the correct output.

### RTL

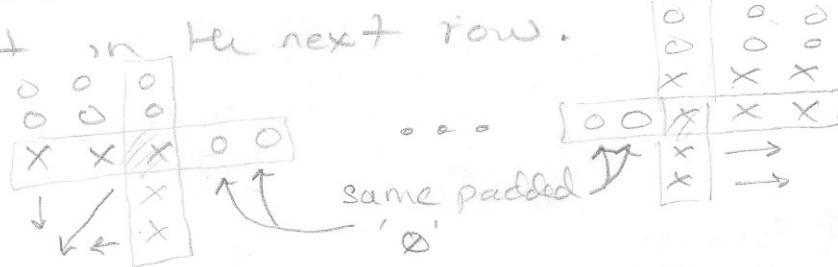
$$\begin{aligned} & z_A, z_B, z_C, z_D \\ \%_p \leftarrow & \frac{1}{p} + \left[ \frac{z_A * k_1}{5} \right] + z_B + \left[ \frac{z_C * k_2}{5} \right] + z_D + \left[ \frac{z_A' * k_1'}{5} \right] + \left[ \frac{z_B' * k_2'}{5} \right] \\ & + \left[ \frac{z_C' * k_3'}{5} \right] + z_D' \\ z_A \leftarrow & \%_p, z_B \leftarrow z_A, z_C \leftarrow z_A * k_1, z_D \leftarrow z_B, z_A' \leftarrow A, \\ z_B' \leftarrow & z_A, z_C' \leftarrow z_B, z_D' \leftarrow z_C \end{aligned}$$

## Gaussian Filter

Gaussian filter  
A reset will be used to pad for the first Valid bit.

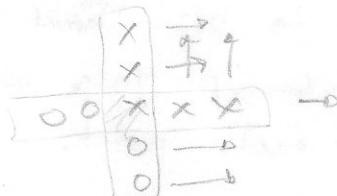


This allows the gassion operation until the end of a row. Then two 0's must be injected at the end of the row to allow a calculation of the last element in the row and the 1st element in the next row.



Two rows of '0's

Two rows of 3  
of Padding must be added to the bottom  
for the same reason.



The coefficients will add up to one for both stages. Since the filter is symmetric only two multipliers are needed for each stage. To divide by 5 one can employ

The fact that  $\frac{1}{8} + \frac{1}{16} + \frac{1}{128} \approx 0.1953125$  to 8 bits of precision. This value can be input into multiple look values.

## Down Sample

Two counters will be used. One will only permit every other bit, while the other will only admit every other row. The 1st counter will enable writing to the FIFO & the 2nd will control the counter of the 1st.

c	o	o	o	o
r	x	x	x	
:				
:	x	x	x	
:				

## UP Sampler

For every input, 'ABC', the output will be 'AABBCC' and for every row 'AABBCC' then the output will be 'AABBCC'. To do this, the CLK signal

of the FIFO will need to be half the speed of  
External side of the Shift register on the external. This will provide the double output of each input.

Additionally, the control signal rd-row will output the previous row. This signal will be controlled by a counter. The valid-ext signal will be valid if the CLK, rd-row, or the valid o/p from the FIFO is enabled.