SAMPLE VERILOG CODE

FULL ADDER

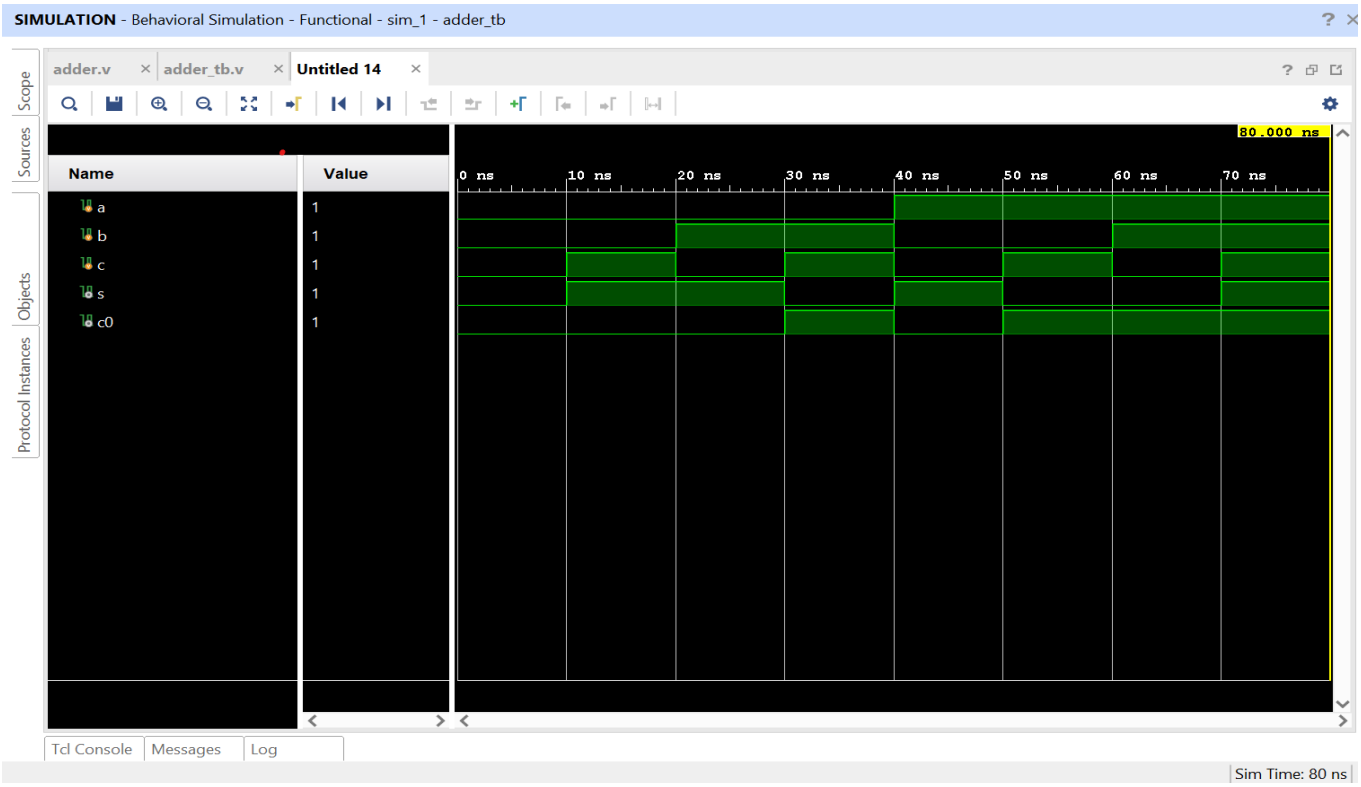
Source code:

```
`timescale 1ns / 1ps
module adder(
   input a,b,c,output s,c0
   );
   assign {c0,s}=a+b+c;
endmodule
```

Testbench:

```
`timescale 1ns / 1ps
module adder_tb();
reg a,b,c;
wire s,c0;
adder dut(a,b,c,s,c0);
initial
begin
{a,b,c}=3'd0;
#10 {a,b,c}=3'd1;
#10 {a,b,c}=3'd2;
#10 {a,b,c}=3'd3;
#10 {a,b,c}=3'd4;
#10 {a,b,c}=3'd5;
#10 {a,b,c}=3'd6;
#10 {a,b,c}=3'd7;
end
endmodule
```

Results:


SIMULATION - Behavioral Simulation - Functional - sim_1 - adder_tb
adder.v
adder_tb.v
Untitled 14
Scope
Sources
Objects
Protocol Instances
Name
Value
a
b
c
s
c0
1
1
1
1
1
0 ns
10 ns
20 ns
30 ns
40 ns
50 ns
60 ns
70 ns
80.000 ns
Tcl Console
Messages
Log
Sim Time: 80 ns