

EE2003 - Computer Organization

Vivado Installation

Important Instructions before installing Vivado:

- Vivado 2020.2 installation requires 73GB of disk space. After installation, it will consume around 47GB of disk space. Make sure that you are comfortable with this. If you don't have enough space, don't install it.
- Follow the instructions carefully. You need to register your account to install it. I have provided instructions for both Windows and Linux. For mac users, Vivado is not supported :/
- You can also simply copy-paste Vivado from IE Lab directly.

Download link:

https://www.xilinx.com/member/forms/download/xef.html?filename=Xilinx_Unified_2020.2_118_1232_Lin64.bin

Instructions:

Step1: Click [Xilinx Unified Installer 2020.2: Windows Self Extracting Web Installer](#) (EXE - 248.44 MB) for Windows and click [Xilinx Unified Installer 2020.2: Linux Self Extracting Web Installer](#) (BIN - 354.08 MB) for Linux users

Step2: Register your account and download the installer

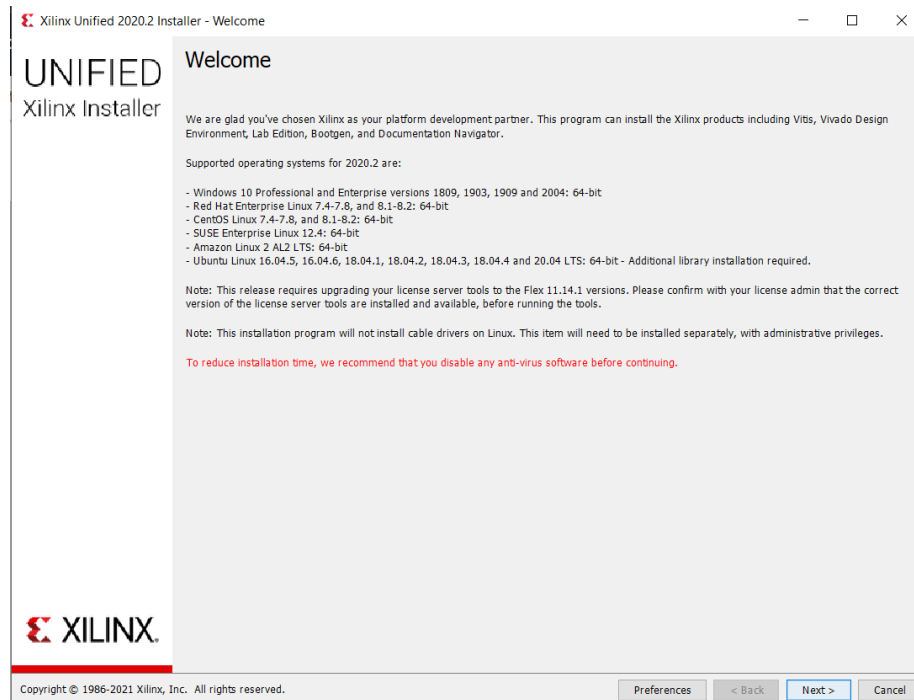
Step3: Open the installer.

For Windows, simply double-click to open.

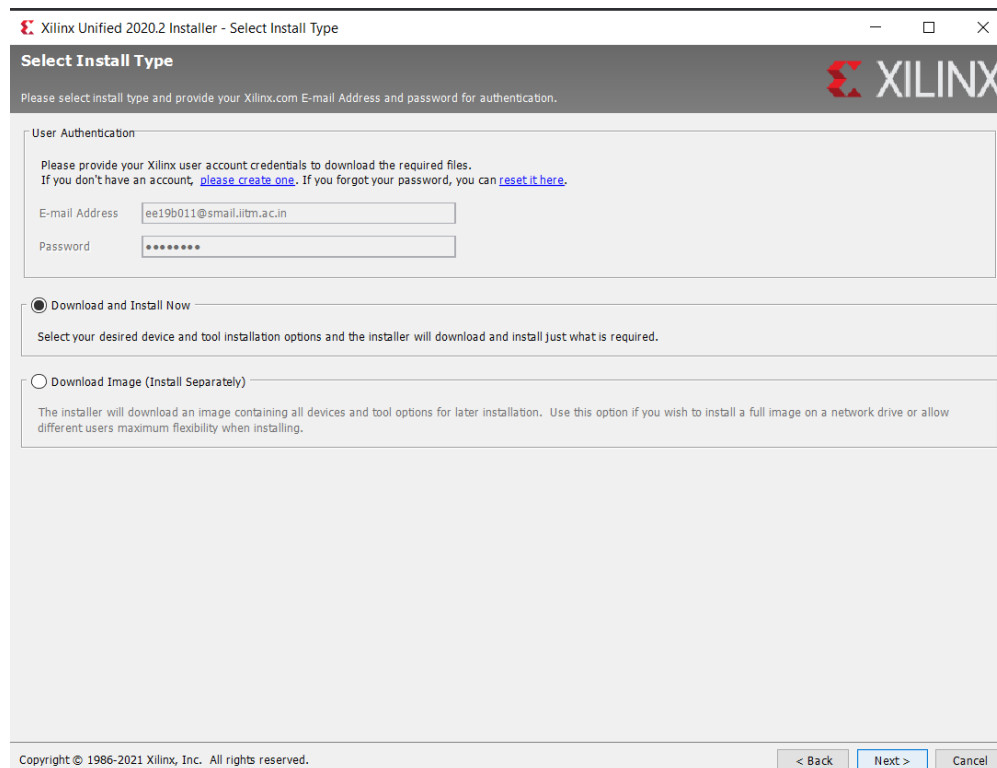
For Linux, run these commands in terminal

```
~$ sudo apt install libtinfo5 libncurses5  
  
~$ chmod +x Xilinx_Unified_2020.2_118_1232_Lin64 &&  
./Xilinx_Unified_2020.2_118_1232_Lin64
```

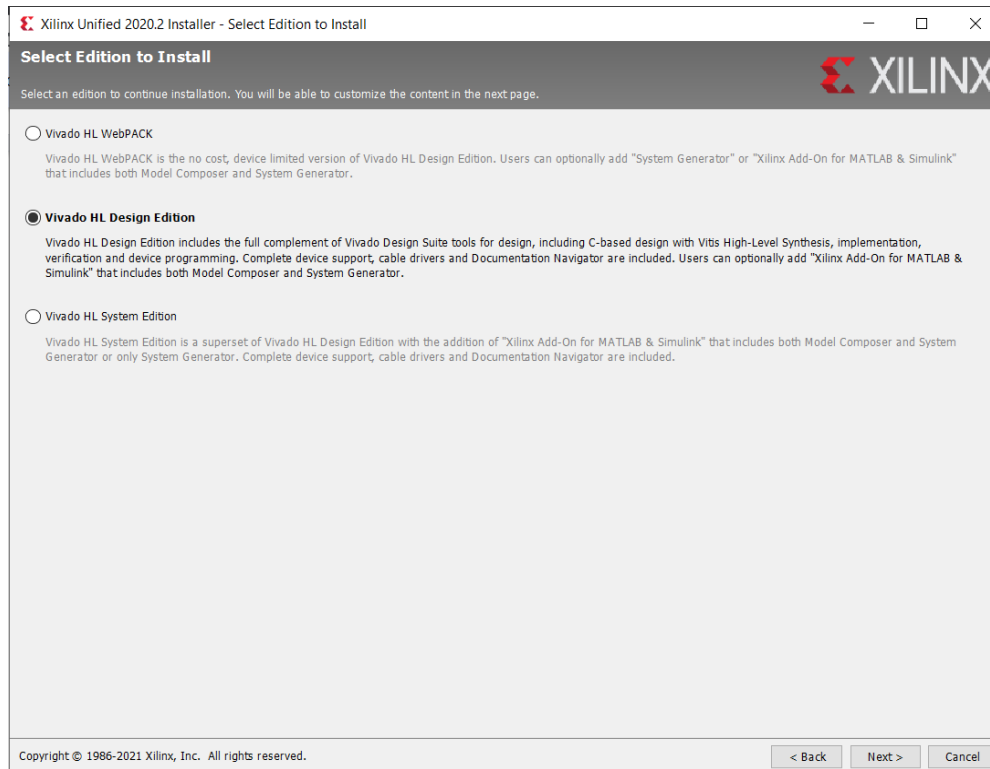
Step4: Click Next



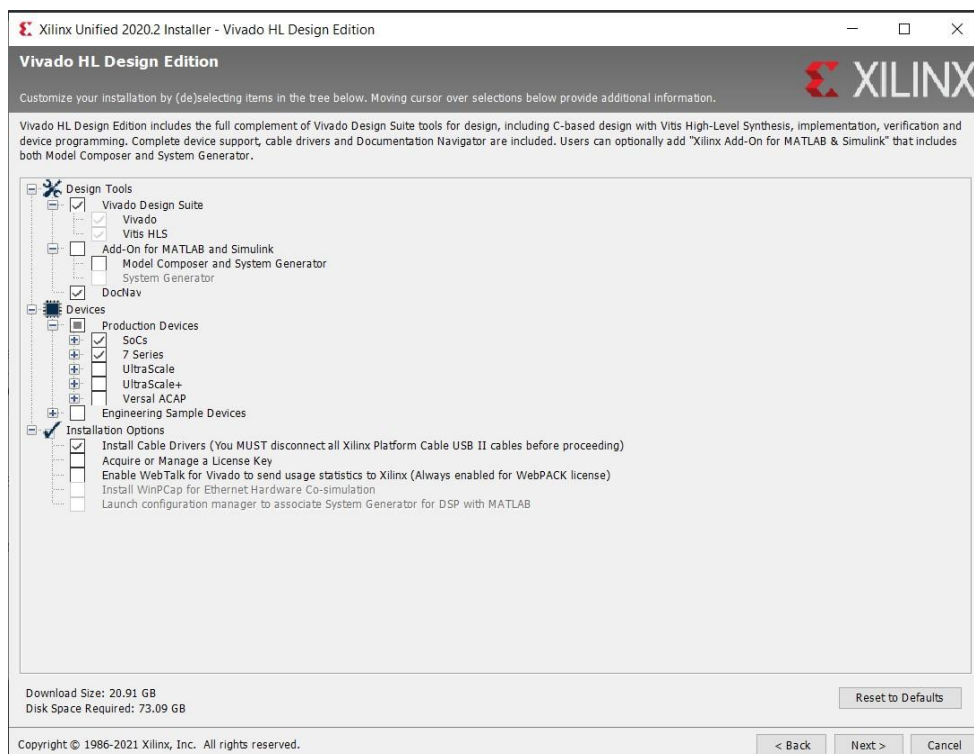
Step5: Enter your email id and password registered in the Xilinx website



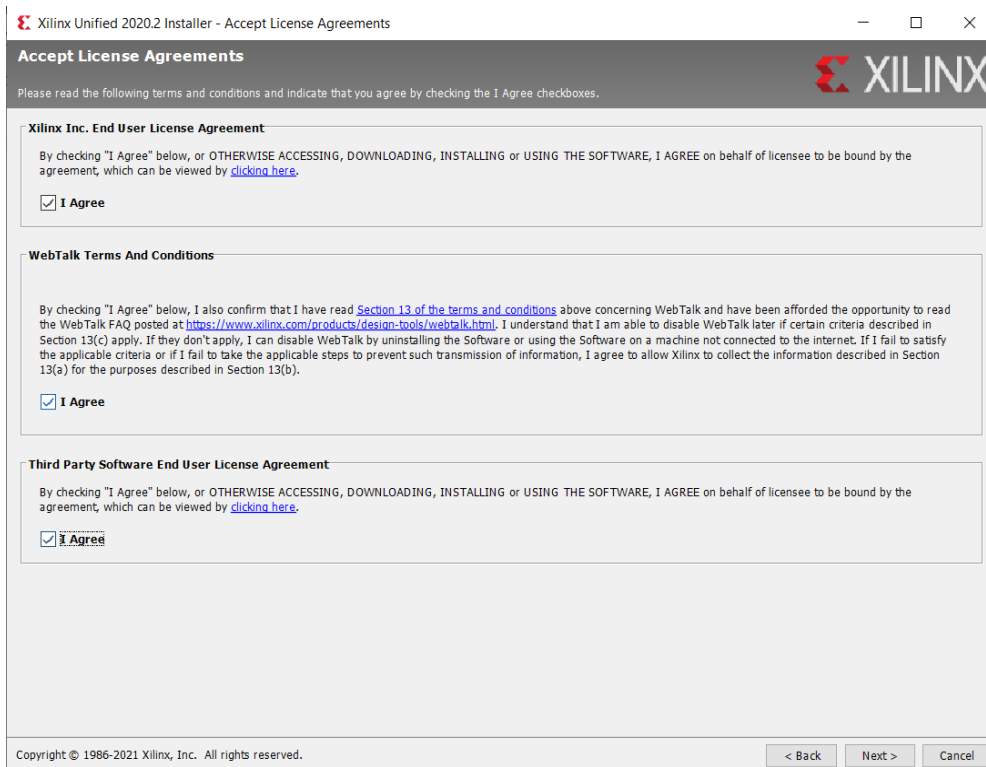
Step6: Select Vivado HL Design Edition



Step7: Select the checkboxes as provided



Step8: Agree on all the terms



Accept License Agreements

Please read the following terms and conditions and indicate that you agree by checking the I Agree checkboxes.

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Third Party Software End User License Agreement

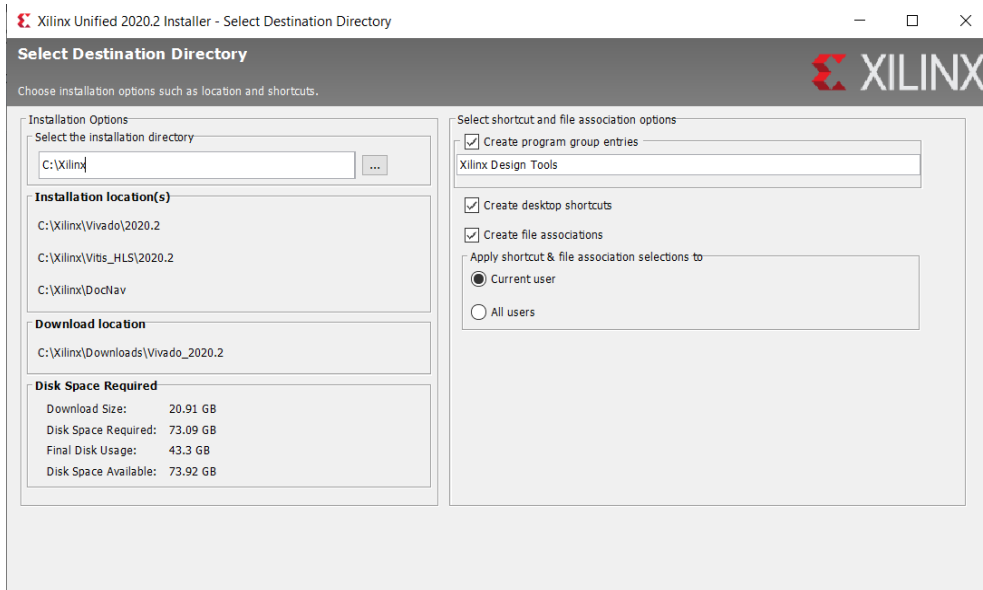
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< Back Next > Cancel

Step9: Choose your installation directory and click Next.



Select Destination Directory

Choose installation options such as location and shortcuts.

Installation Options

Select the installation directory

C:\Xilinx

Installation location(s)

C:\Xilinx\Vivado\2020.2

C:\Xilinx\Vitis_HLS\2020.2

C:\Xilinx\DocNav

Download location

C:\Xilinx\Downloads\Vivado_2020.2

Disk Space Required

Download Size:	20.91 GB
Disk Space Required:	73.09 GB
Final Disk Usage:	43.3 GB
Disk Space Available:	73.92 GB

Select shortcut and file association options

☒ Create program group entries

Xilinx Design Tools

☒ Create desktop shortcuts

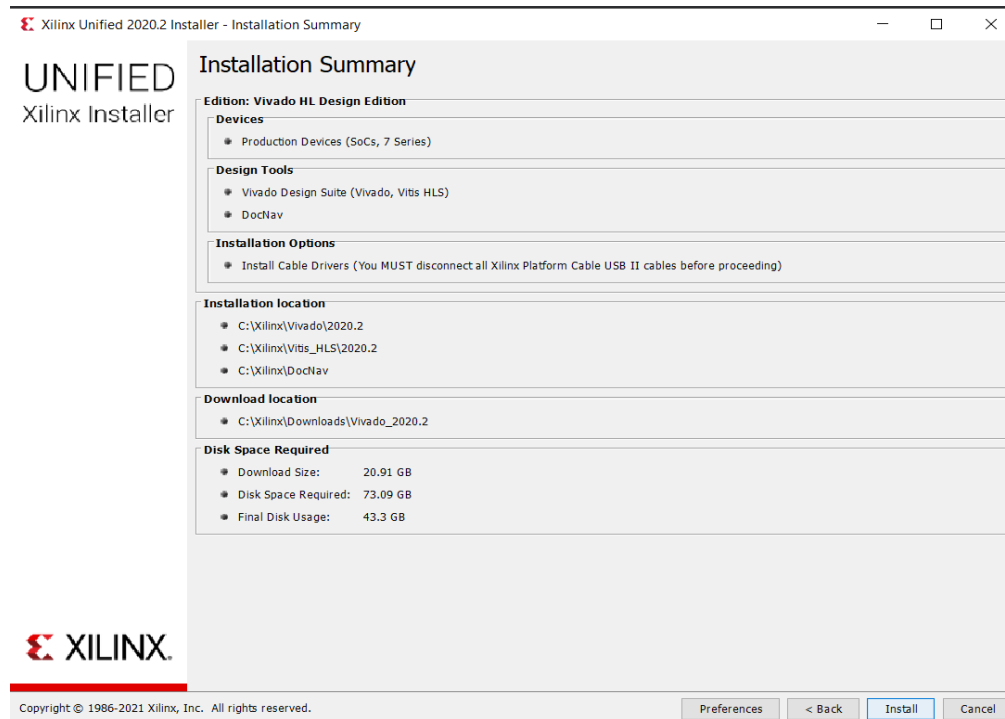
☒ Create file associations

Apply shortcut & file association selections to

☒ Current user

☐ All users

Step10: Click Install. Note the download location.



Step11: ONLY FOR LINUX USERS

Once installation is finished, you must run these commands.

```
// Run this in terminal
~$ sudo <YOUR INSTALLATION DIRECTORY PATH
>/Vivado/2020.2/data/xicom/cable_drivers/lin64/install_script/install_drivers
/install_drivers

// Make Vivado available in all sessions
~$ echo 'export PATH=$PATH<YOUR INSTALLATION DIRECTORY
PATH>/Vivado/2020.2/bin:$PATH' >> .bashrc

// Now you should be able to run Vivado
~$ vivado
```

Step12: Save PYNQ-Z1 board files

Board file link: https://github.com/cathalmccabe/pyng-z1_board_files/raw/master/pyng-z1.zip

Extract the above file and paste it under

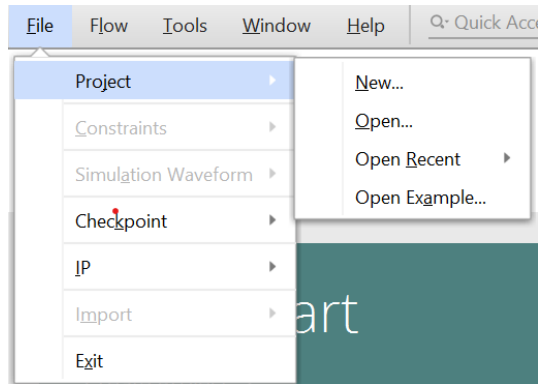
```
<Xilinx installation  
directory>\Vivado\<version>\data\boards\board_files
```

Installation is complete!

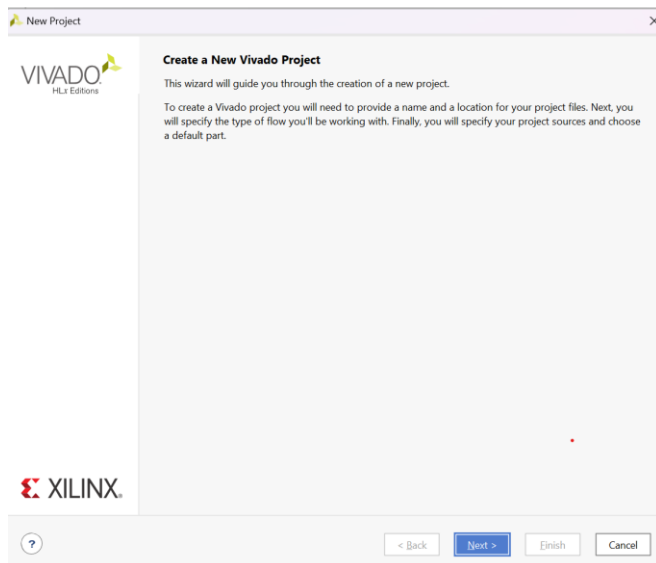
STEPS FOR RUNNING PROJECT WITH EXAMPLE IN VIVADO:

1.Open vivado


2.Open file →project → new



3.click next



4. enter project name say “adder” and direct project location-> RTL project

 New Project ✕

Project Name
Enter a name for your project and specify a directory where the project data files will be stored.

Project name:


Project location:

☒ Create project subdirectory
Project will be created at: C:/Users/kmsar/adder

?

< Back Next > Finish Cancel

5. choose fpga board → next → finish

 New Project ✕

Default Part
Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category:

Package:

Temperature:

Family:

Speed:

Static power:

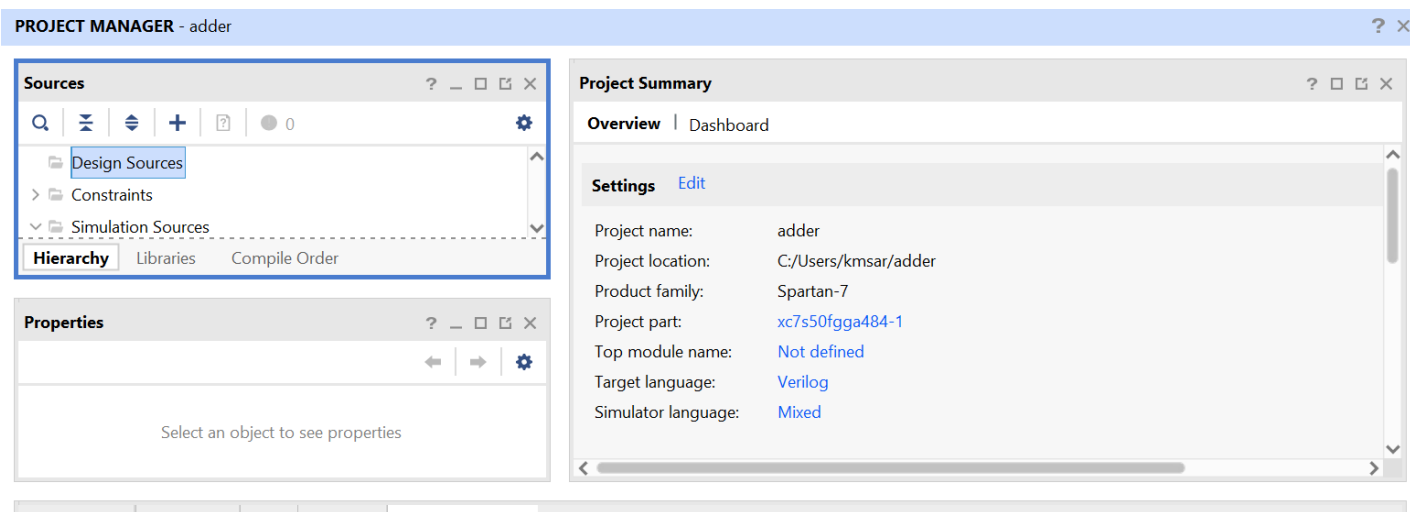
Search:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	Gb Tr
xc7s50csga324-1Q	324	210	32600	65200	75	0	120	0
xc7s50fgga484-2	484	250	32600	65200	75	0	120	0
xc7s50fgga484-1	484	250	32600	65200	75	0	120	0
xc7s50fgga484-1IL	484	250	32600	65200	75	0	120	0
xc7s50fgga484-1Q	484	250	32600	65200	75	0	120	0
xc7s50ftgb196-2	196	100	32600	65200	75	0	120	0
xc7s50ftgb196-1	196	100	32600	65200	75	0	120	0
xc7s50ftgb196-1IL	196	100	32600	65200	75	0	120	0
xc7s50ftgb196-1Q	196	100	32600	65200	75	0	120	0

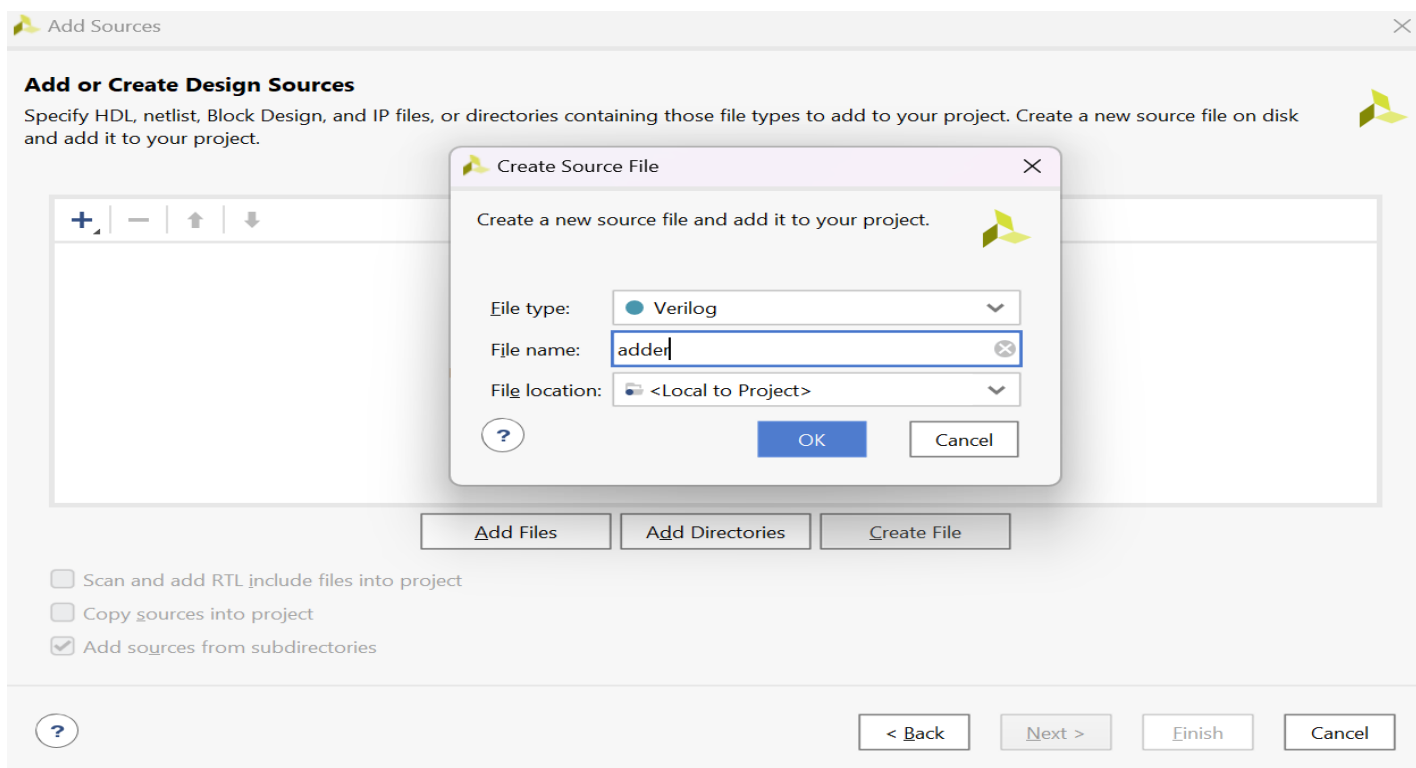
?

< Back Next > Finish Cancel

6. right click design sources → add new sources → add or create design sources → next



7. click “create file” → type file name (here adder) → ok



8.add your IO ports(not mandatory as you can add in program too)→ok

Define Module

Define a module and specify I/O Ports to add to your source file.
For each port specified:
MSB and LSB values will be ignored unless its Bus column is checked.
Ports with blank names will not be written.

Module Definition

Module name:

I/O Port Definitions

Port Name	Direction	Bus	MSB	LSB
a	input	<input type="checkbox"/>	0	0
b	input	<input type="checkbox"/>	0	0
c	outp...	<input type="checkbox"/>	0	0

9.double click “adder” and type the program and check your syntax by the indication of green color. If it is showing red color then there is some error in program.

PROJECT MANAGER - adder

Sources

- Design Sources (1)
 - adder (adder.v)
- Constraints

Source File Properties

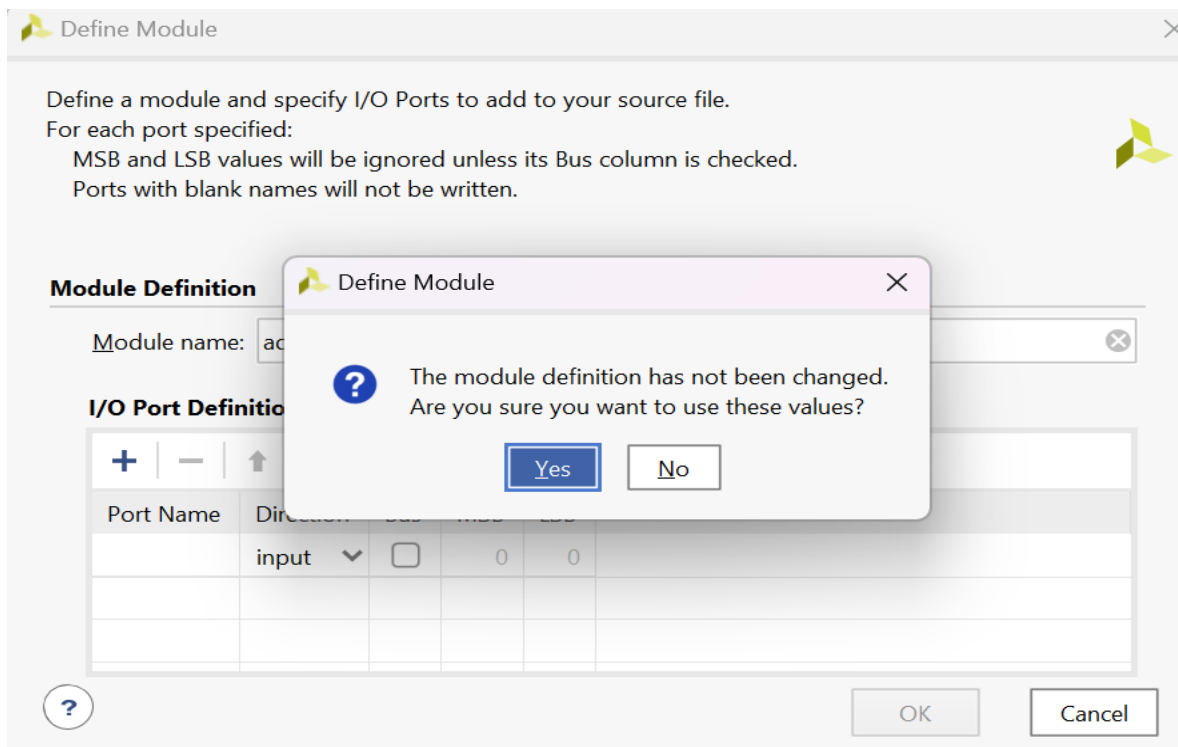
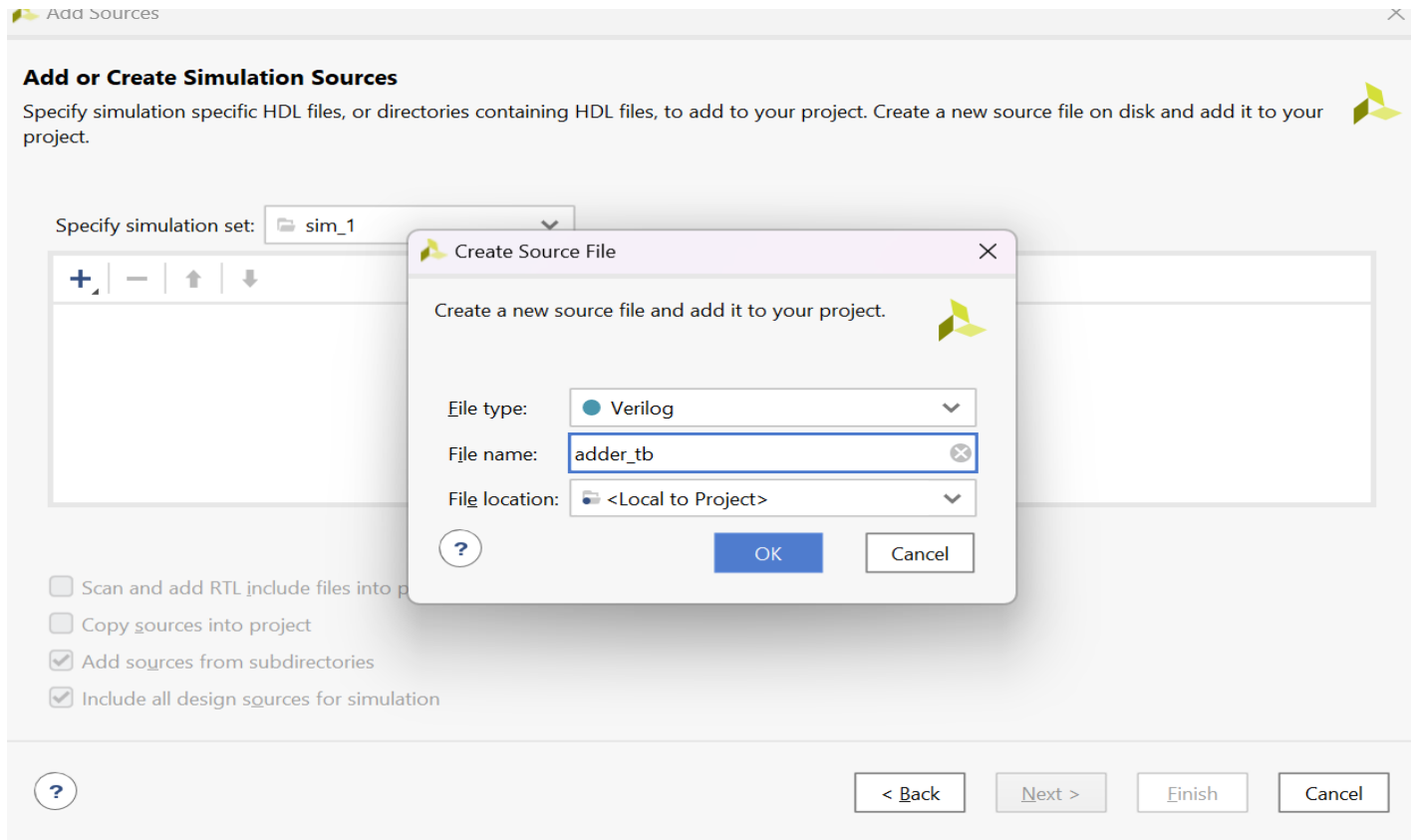
- adder.v
 - Enabled

Project Summary **adder.v**

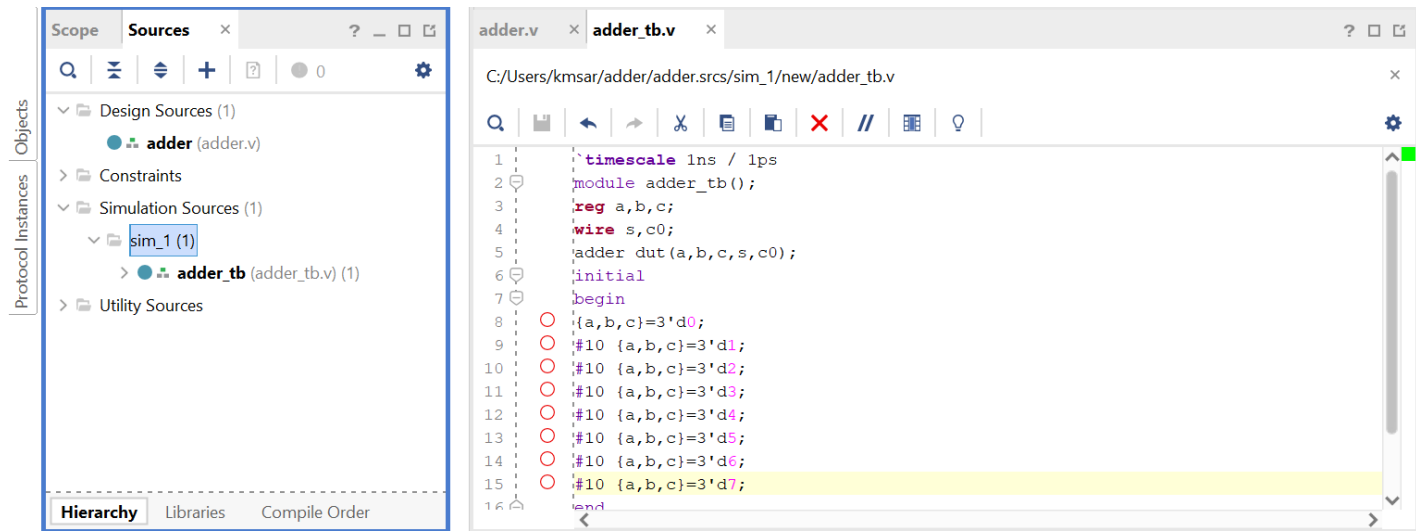
C:/Users/kmsar/adder/adder.srsrcs/sources_1/new/adder.v

```
20 ///////////////////////////////////////////////////////////////////
21
22
23 module adder(
24     input a,b,c,output s,c0
25 );
26     assign {c0,s}=a+b+c;
27 endmodule
28
```

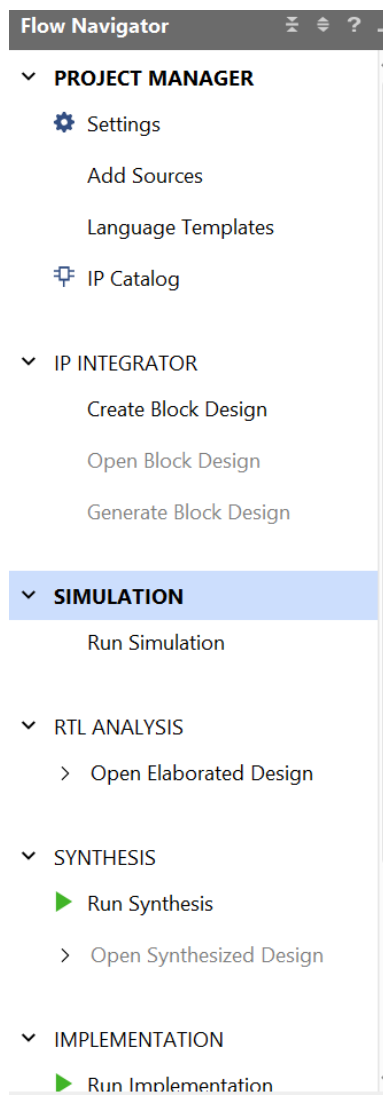
10.To add testbench right click “simulation sources”→add sources→add or create simulation sources→create file(here adder_tb) with no IO ports (as test bench has no IO ports)→finish



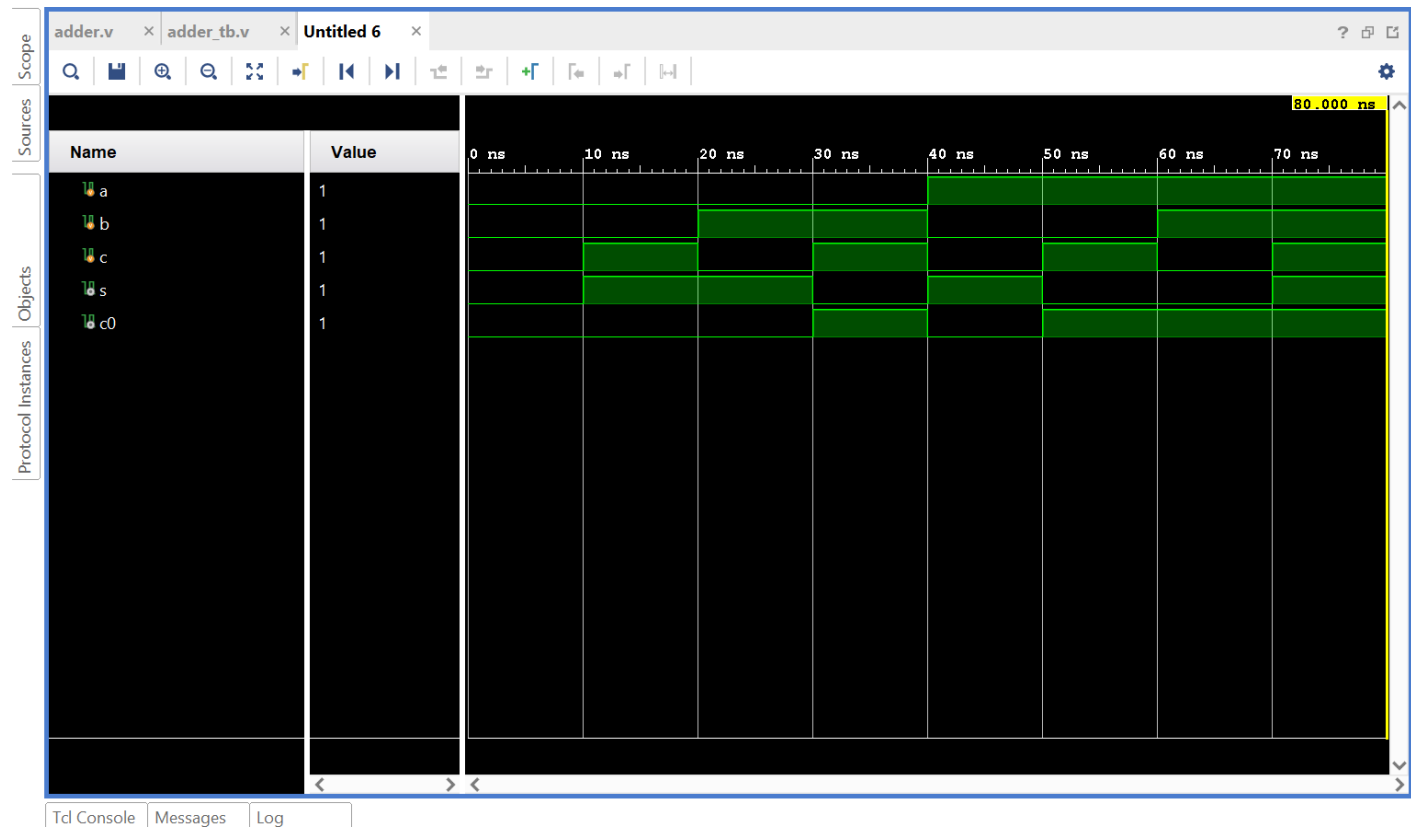
11. Click Sim_1 → click your simulation file (here adder_tb) → type the testbench code



12. Run simulation after saving testbench



13.Observe the waveforms and compare the waveforms with theoretical outputs



=====END=====