BTS–III(R/S)–01–23–1435 Reg. No. [redacted]

B.Tech. Degree III Semester Regular/Supplementary Examination January 2023

CS 19-202-0302 LOGIC DESIGN

(2019 Scheme)

Time: 3 Hours Maximum Marks: 60

Course Outcome
On successful completion of the course, the students will be able to:

CO1: Understand about the basic number systems and the conversion between them.
CO2: Manipulate Boolean expressions and simplify them.
CO3: Design combinational circuits for any given problem.
CO4: Design sequential circuits, flip-flops etc.
CO5: Design circuits like counters, registers etc.
CO6: Familiarize with the basic principles of memory, design of memory etc.
CO7: Gain knowledge about the basics of integrated circuits.

Bloom's Taxonomy Levels (BL): L1 – Remember, L2 – Understand, L3 – Apply, L4 –Analyze, L5 – Evaluate, L6 – Create
PO – Programme Outcome

PART A

(Answer *ALL* questions)

			(8 × 3 = 24) Marks	BL	CO	PO
I.	(a)	Convert the decimal number 2795.36 to base 2, 8, and 16.	3	L1	1	1,2,4
	(b)	Show that the dual of Exclusive-OR gate is equal to its complement.	3	L1	2	1,2,4
	(c)	How are the carry bits generated in a 4-bit fast adder circuit? Derive the carry input for each stage.	3	L2	3	1,2,4
	(d)	Derive the characteristic equations of JK, RS, D and T flip flops?	3	L2	4	1,2,4
	(e)	Design a Johnson counter with 12 timing signals.	3	L3	5	1,2,4
	(f)	Define the term steering logic in synchronous counters and what is the main disadvantage of ripple counter over synchronous counter?	3	L2	5	1,2,4
	(g)	Differentiate between PLA and PAL. Draw the PLA for the function $F1 = (AC + BC)'$	3	L2	6	1,2,4
	(h)	What are the different TTL circuits based on power dissipation and propagation delay?	3	L2	7	1,2,4

PART B

(4 × 12 = 48)

II.		Simplify the Boolean function $F(A,B,C,D,E) = \Sigma(0,2,4,6,9,11,13,15,16,20,25,27,29,31)$ using K-map and draw the NAND realization of the logic circuit.	12	L3	2	1,2,3,4, 12
		OR				
III.		Simplify $F(A,B,C,D,E,F,G) = \Sigma(20, 28,52,60)$ using Quine-McCluskey method.	12	L3	2	1,2,4,12

(P.T.O.)

			Marks	BL	CO	PO
IV.		Design a combinational circuit that compares two 4-bit numbers.	12	L4	3	1,2,3,4, 12
		OR				
V.		Design a sequential circuit using reduced state table whose specification is given in the following state diagram.	12	L4	3	1,2,12

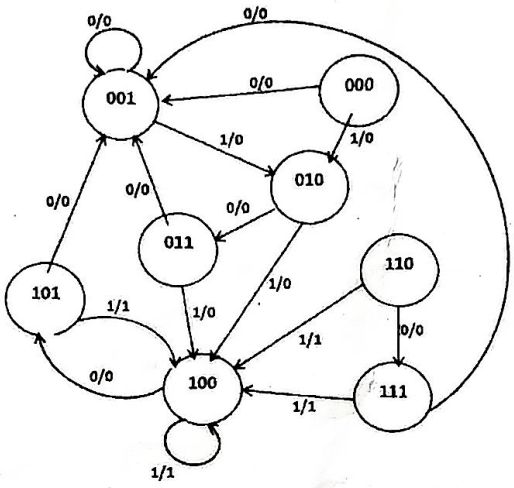

Fig: State Diagram

VI.		Design a BCD counter using RS-flip flops and draw the waveforms of the counting operation.	12	L4	5	1,2,3,4, 12
		OR				
VII.		Draw and explain the working of a 4-bit bidirectional shift register.	12	L2	5	1,2,4,12
VIII.	(a)	Explain the working of basic RTL NOR gate with diagram.	6	L2	7	1,2,4,12
	(b)	Explain the interfacing of CMOS driver and TTL load?	6	L2	7	1,2,4,12
		OR				
IX.		Explain the working of a TTL circuit with an example.	12	L2	7	1,2,12

Blooms's Taxonomy Levels
L1 - 12%, L2 - 50%, L3 - 19%, L4 - 19%.

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