BTS-III(S)-04.18-0784 Reg. No. | | | | | | | | |

A

B.Tech. Degree III Semester Supplementary Examination April 2018

CS 15 - 1302 LOGIC DESIGN
(2015 Scheme)

Time: 3 Hours Maximum Marks: 60

PART A
(Answer ***ALL*** questions)

(10 × 2 = 20)

I. (a) Convert $(AB2)_{16}$ to octal.
(b) Evaluate $(DA4C)_{16} - (648)_{16}$ using (r - 1)'s complement.
(c) Find the complement of $AB' + C'D'$ and reduce it to a minimum number of literals.
(d) Differentiate between canonical and standard forms of Boolean functions.
(e) Design a 4 × 16 decoder constructed two 3 × 8 decoder.
(f) Write notes on triggering of flip flops.
(g) Write a short note on state tables of a sequential circuit.
(h) Draw the PLA block diagram and explain its features.
(i) What is meant by Propagation delay?
(j) Differentiate between RTL and DTL.

PART B

(4 × 10 = 40)

II. Simplify the following expression using the K-Map method and realize using NOR gates. $F(w, x, y, z) = \sum m(1, 5, 6, 12\ 13, 14) + d(2, 4)$.

OR

III. Prove the theorems of Boolean algebra by using postulates.

IV. Simplify the following Boolean function into (i) sum-of-products form and (ii) product-of-sums form: $F(A, B, C, D) = \sum(0, 1, 2, 5, 8, 9, 10)$.

OR

V. Implement the following Boolean function with NAND gates: $F(x, y, z) = (1, 2, 3, 4, 5, 7)$.

VI. Implement the following function using a multiplexer (Use B as input).
$F(A, B, C, D) = \sum(0, 1, 3, 4, 8, 9, 15)$.

OR

VII. Design a 4 bit binary ripple counter using JK flip flops.

VIII. Explain the operation of 2 input CMOS NOR gate and CMOS inverter in detail.

OR

IX. Explain with circuit diagram a typical 2 input TTL NAND gate.

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