BTS-III(S)-11.20-0662 Reg. No. | | | | | | | | |

A

B.Tech. Degree III Semester Supplementary Examination November 2020

CS 15-1302 LOGIC DESIGN
(*2015 Scheme*)

Time: 3 Hours Maximum Marks: 60

PART A
(Answer *ALL* questions)

(10 × 2 = 20)

I. (a) Convert 2705_8 to its decimal and hexadecimal equivalent.
(b) Simplify the following Boolean expression to minimum number literals:
(i) ABC + A'B + ABC'
(ii) x'yz + xz
(c) Draw the NAND logic diagram of boolean function , F = AB+BC+D.
(d) Draw the realization of half subtractor using gates.
(e) What is a priority encoder?
(f) Explain toggle flip-flop.
(g) Draw the realization of twisted ring counter using D flipflop.
(h) Differentiate between PROM and PAL.
(i) Write the procedure for obtaining stable state of asynchronous sequential circuit.
(j) What is propagation delay of a gate? Define setup time and hold time.

PART B

(4 × 10 = 40)

II. (a) Using 10's complement, subtract 3250-72532. (2)
(b) Write the rules of BCD addition and perform the BCD addition of (4)
(i) $(8)_{10} + (9)_{10}$
(ii) $(3)_{10} + (7)_{10}$
(c) What are codes? Explain Weighted code and Unweighted codes with two examples. (4)

OR

III. (a) Simplify the followng Boolean functions using K-map (5)
(i) F(w,x,y,z) = Σ(0,1,2,4,5,6,8,9,12,13,14)
(ii) F = ABCD + ACD + AD
(b) Minimize the following switching function using the Quine McCluskey method (5)
F(A,B,C,D) = Σ m(1,2,3,5,6,7,8,9,12,13,15).

IV. (a) Explain the working of a 4-bit BCD adder with block diagram (7)
(b) Write the procedure involved in design of combinational circuit. (3)

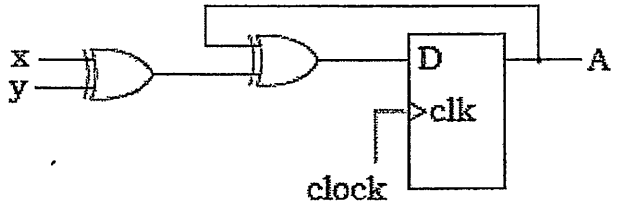
OR

V. (a) Explain the working of a 4-bit magnitude comparator. (5)
(b) Implement the following function with a multiplexer (5)
f(A,B,C ,D) = Σ (0,1,3,4,11,12,13.14,15).

(P.T.O.)

VI. (a) Explain the working of SR latch with NAND gate with the help of logic diagram and function table.Which state is forbidden state? (6)

(b) Draw the state table and state diagram for the circuit diagram. (4)



OR

VII. Design a counter that has repeated sequence of six states 0,1,2,4,5,6 using JK flip-flop. (10)

VIII. (a) Design a combinational circuit using a ROM.The circuit accepts three bit numbers and outputs a binary number equal to the square of the input number. (6)

(b) Explain the woking of PLA. (4)

OR

IX. Explain the working of RTL and DTL circuit. Explain how fan-out of DTL gate can be increased? (10)

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