BTS –III(S)– 05.17 – 0720 Reg. No. | | | | | | | | |

A

B.Tech. Degree III Semester Supplementary Examination May 2017

CS 15-1302 LOGIC DESIGN

(*2015 Scheme*)

Time: 3 Hours Maximum Marks:60

PART A

(Answer *ALL* questions)

(10 × 2 = 20)

I. (a) Perform the following number conversions:
(i) 567 in Octal to Hex
(ii) 234.54 in decimal to binary.
(b) Differentiate between canonical and standard forms of Boolean functions.
(c) What are universal gates? Why are they called so?
(d) What is carry look-ahead addition? What is the need?
(e) Explain the design procedure of a combinational circuit.
(f) Differentiate between synchronous and asynchronous circuits.
(g) What is master slave flip flop?
(h) Differentiate between PLA and PAL.
(i) Write about ROM, PROM, EPROM and EEPROM.
(j) Define the following terms: Fan out, Propagation delay and Noise margin.

PART B

(4 × 10 = 40)

II. Simplify the following function using Quine McCluskey method.
$F(A,B,C,D) = \sum(0,2,3,5,7,8,9,10,11,13,15)$.

OR

III. Simplify the following expression using the K-Map method and implement it using logic gates.
(i) $F = ACE + A^1CD^1E + A^1C^1DE$.
(ii) $d = DE^1 + A^1D^1E + AD^1E^1$.

IV. Derive the expressions for a 4-bit magnitude comparator and implement it using logic gates.

OR

V. (a) Design a decimal adder using 4-bit binary parallel adders.
(b) Design an excess 3 to BCD code converter using a 4-bit binary parallel adder.

VI. Design a 4-bit Johnson counter. How does it differ from a ring counter?

OR

VII. Design a 4-bit binary ripple counter using JK flip flops.

VIII. Design a RAM consisting of four words of four bits each. Also show the logic diagram of a typical binary cell.

OR

IX. Draw and explain the circuit for a TTL gate with Totem pole output driver.

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