BTS-III(S)-(11.20/04.21)-1687 Reg. No. | | | | | | | | |

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B.Tech. Degree III Semester Supplementary Examination November 2020/April 2021

CS 15-1302 LOGIC DESIGN
(*2015 Scheme*)

Time: 3 Hours Maximum Marks: 60

PART A
(Answer ***ALL*** questions)

(10 × 2 = 20)

I. (a) Perform the following:

(i) Convert decimal 27.315 to binary.

(ii) Using 10's complement, subtract 3250-72532.

(b) Define minterm and maxterm. Express the Boolean function F = A + B'C as sum of minterm.

(c) Reduce the Boolean expression A'C'+ABC+AC' to three literals.

(d) Draw the realization of Full adder using gates and obtain expressions for the output function.

(e) Implement the following function using a multiplexer.

$F(A, B, C, D) = \sum(1,2,6,7)$

(f) Differentiate between latches and flip-flop.

(g) Differentiate between synchronous and asynchronous sequential circuits.

(h) Define Shift register and draw a 4-bit shift register using D flip-flop.

(i) What is meant by PLDs? Explain any two types of PLDs.

(j) Define the terms: (i) Power Dissipation
(ii) Propagation delay

PART B

(4 × 10 = 40)

II. (a) What is a gray code? What are the advantages of gray code? Find the gray code of $(1011)_2$ (3)

(b) Find the complement of function F = x(y'z' + yz). (2)

(c) Simplify the following expression using the K-Map method. (5)

$F(A,B,C,D) = \sum(0,6,8,13,14)$

$d(A,B,C,D) = \sum(2,4,10)$

OR

III. Simplify the following Boolean function using the tabulation method.

(a) $F(A, B, C, D) = \sum(0, 1, 3, 7, 8, 9, 11, 15)$. (5)

(b) $F(A, B, C, D) = \sum(0, 5, 7, 8, 9, 10, 11, 14, 15)$. (5)

(P.T.O.)

IV. (a) Design a 4-bit binary adder and explain the working with example A = 1011 and B = 0011. (5)

(b) Draw the realization of half subtractor using gates and explain the working. (5)

OR

V. (a) Explain the working of Decimal adder with block diagram and explain the need of correction function. (5)

(b) Implement (i) 8 × 1 MUX using 2 × 1 MUX. (5)

(ii) 8 × 1 MUX using 4 × 1 MUX.

VI. (a) Explain the working of SR latch using NOR gate with the help of logic diagram abd function table. (6)

(b) Define the terms state equation, state table and state diagram. Mention the advantages of state reduction. (4)

OR

VII. (a) Design a 2 bit synchronous up counter using JK flipflops. (5)

(b) Design a 4 bit ring counter using D flip-flop. (5)

VIII. Differentiate PLA and PAL. Draw the PLA for functions: (10)

$F1 = AB' + AC + A'BC'$

$F2 = (AC + BC)'$

OR

IX. (a) Draw and explain the working of Basic RTL NOR gate. (5)

(b) Explain the working of CMOS transmission gate circuit. (5)

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