BTS–IV–04.19–0655 Reg. No. | | | | | | | | | |

B

B.Tech. Degree IV Semester Examination April 2019

CS 15-1403 COMPUTER ARCHITECTURE AND ORGANIZATION

(*2015 Scheme*)

Time : 3 Hours Maximum Marks : 60

PART A

(Answer ***ALL*** questions)

(10 × 2 = 20)

I. (a) Explain the operating steps involved in the execution of a complete instruction.

(b) What is meant by stack? Explain the basic stack operations.

(c) Differentiate between RISC and CISC architectures.

(d) What do you mean by carry look ahead addition?

(e) List out the control sequence for execution of the instruction ADD (R3), R1.

(f) What is meant by prefetching of micro instructions?

(g) Differentiate between write through and write back protocols.

(h) What is memory interleaving? What are the advantages?

(i) What is an interrupt? List out the sequence of events involved in handling an interrupt request from a single device.

(j) Write about any two widely used bus standards.

PART B

(4 × 10 = 40)

II. (a) With a neat diagram, explain the functional units of a computer. (6)

(b) Evaluate (A + B) * (C + D) using (i) only three address instructions, (ii) only two address (iii) only one address instructions (iv) only zero address instructions. (4)

OR

III. (a) What is meant by addressing mode? Explain any three addressing modes with an example for each. (7)

(b) What is meant by I/O mapped I/O ? How does it differ from memory mapped I/O? (3)

IV. (a) Explain in detail about the hardwired control unit with necessary diagrams. (5)

(b) Explain the Booth's algorithm for fast multiplication with an example. (5)

OR

V. (a) Explain the purpose of carry save addition of summands in multiplication. (6)

(b) Explain the principle of restoring division with an example. (4)

VI. (a) With necessary diagrams, explain the mechanism of address translation in virtual memory based on paging. (6)

(b) What is translation lookaside buffer? (4)

OR

VII. (a) Explain the internal organization of a memory chip which has 16 words of 8 bits each. (6)

(b) Explain any two cache memory mapping functions. (4)

VIII. (a) Explain about interrupt nesting with necessary diagrams. (5)

(b) Explain briefly about the Universal Serial bus. (5)

OR

IX. (a) What is meant by exceptions? What are the different types of exceptions? (4)

(b) Differentiate between centralised and distributed bus arbitration in DMA. (6)

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