BTS-IV-04.18-0721 Reg. No. | | | | | | | | |

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B.Tech. Degree IV Semester Examination April 2018

CS 15-1403 COMPUTER ARCHITECTURE AND ORGANIZATION

(2015 Scheme)

Time: 3 Hours Maximum Marks: 60

PART A

(Answer ***ALL*** questions)

(10 × 2 = 20)

I. (a) Explain the single bus structure with a neat diagram.

(b) List out the various steps needed to execute the instruction ADD LOC A, R0.

(c) Differentiate between big-endian and littile-endian assignments with an example.

(d) What do you mean by prefetching of micro instructions?

(e) Define emulation.

(f) Explain the various steps in executing a complete instruction.

(g) With a diagram explain the operation of a typical ROM cell.

(h) Differentiate between SRAM and DRAM.

(i) What is an interrupt? List out the sequence of events involved in handling an interrupt request from a single device.

(j) Differentiate between the operations of synchronous and asynchronous bus.

PART B

(4 × 10 = 40)

II. (a) With a neat diagram, explain the functional units of a computer. (6)

(b) Differentiate between register transfer notation and assembly language notation with examples. (4)

OR

III. (a) Explain any three addressing modes with an example for each. (6)

(b) What is meant by stack? Explain the basic stack operations. (4)

IV. (a) Explain, in detail, about the microprogrammed control unit with necessary diagrams. (5)

(b) Explain the Booth's algorithm for fast multiplication. (5)

OR

V. (a) What is meant by carry look ahead addition? Design a 4 bit carry look ahead adder. (6)

(b) Explain the principle of non restoring division with an example. (4)

VI. (a) What is the principle of cache memory? Explain the different cache memory mapping functions. (6)

(b) Explain any two replacement algorithms. (4)

OR

(P.T.O.)

VII.	(a)	What is memory interleaving? Explain with diagrams. What are the advantages?	(4)
	(b)	With a neat diagram explain about virtual memory address translation based on paging.	(6)
VIII.	(a)	What are vectored interrupts? How are they handled?	(5)
	(b)	Explain briefly about the peripheral component interconnect bus.	(5)
		OR	
IX.	(a)	Explain how nested interrupts are handled.	(5)
	(b)	Explain about the functions of a DMA controller.	(5)

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