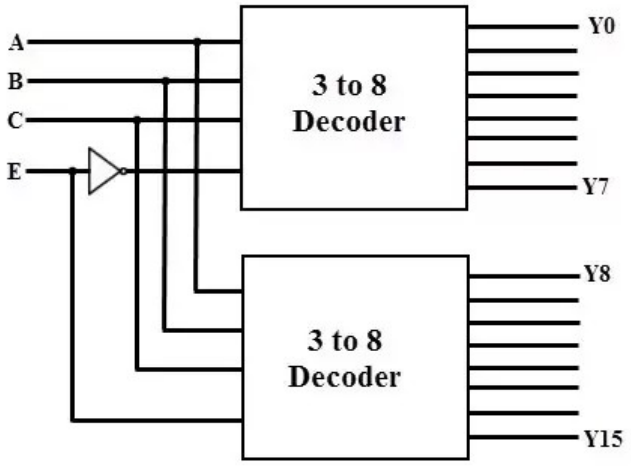
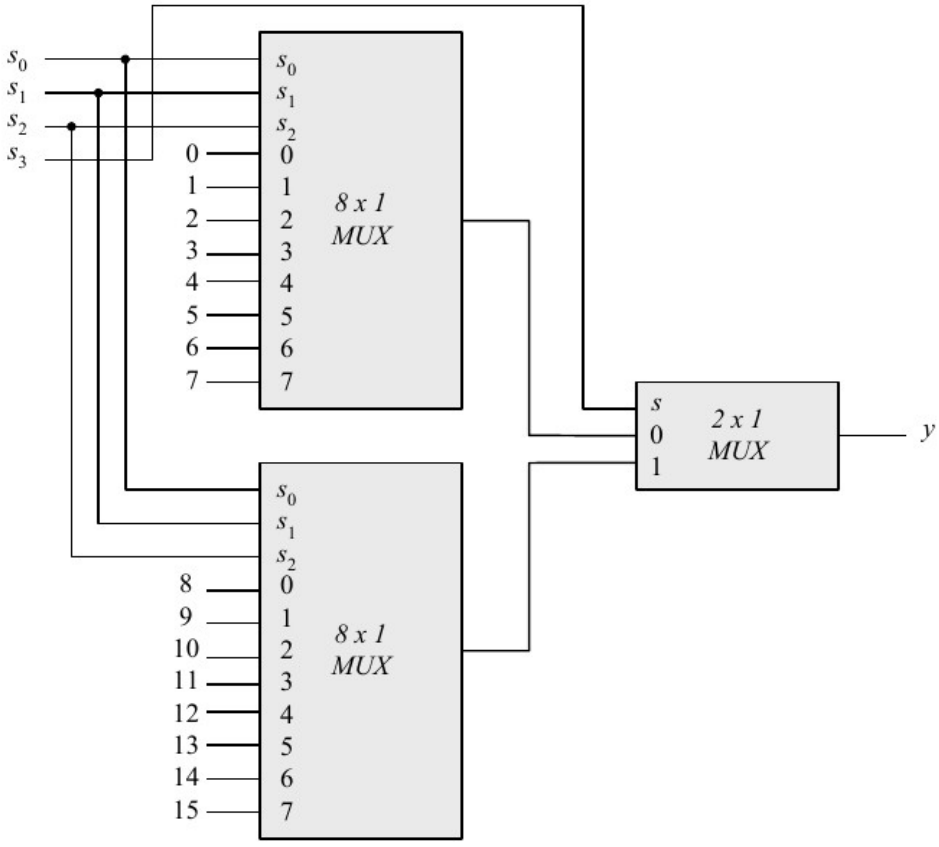
LD – Second Internal Answer key

PART-B

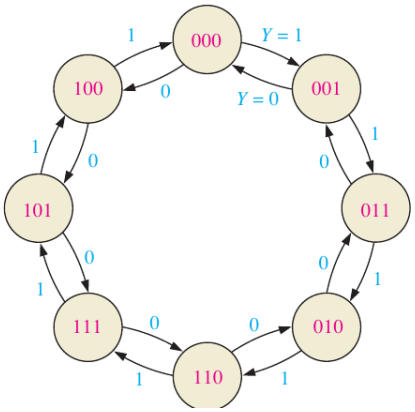
2 (a)Design a 4 x 16 decoder using two 3 x 8 decoders.



(b)Construct a 16 x 1 multiplexer with two 8 x 1 and one 2 x 1 multiplexers.



3. (a)Develop a synchronous 3-bit up/down counter with a Gray code sequence using J-K flip-flops. The counter should count up when an UP/DOWN control input is 1 and count down when the control input is 0.



Transition table for a J-K flip-flop.

Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Next-state table for 3-bit up/down Gray code counter.

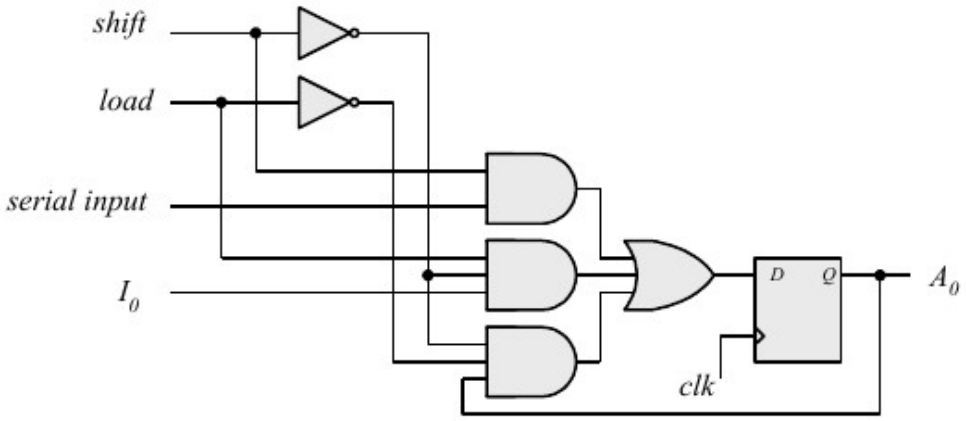
Present State			Next State					
			Y = 0 (DOWN)			Y = 1 (UP)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

Y = UP/$\overline{\text{DOWN}}$ control input.

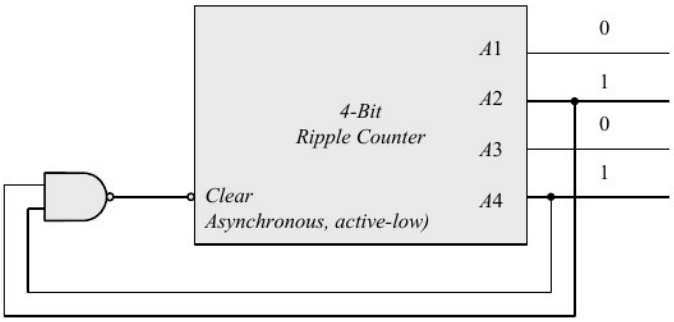
$$J_0 = Q_2Q_1Y + Q_2\overline{Q}_1\overline{Y} + \overline{Q}_2\overline{Q}_1Y + \overline{Q}_2Q_1\overline{Y} \qquad K_0 = \overline{Q}_2\overline{Q}_1\overline{Y} + \overline{Q}_2Q_1Y + Q_2\overline{Q}_1Y + Q_2Q_1\overline{Y}$$
$$J_1 = \overline{Q}_2Q_0Y + Q_2Q_0\overline{Y} \qquad K_1 = \overline{Q}_2Q_0\overline{Y} + Q_2Q_0Y$$
$$J_2 = Q_1\overline{Q}_0Y + \overline{Q}_1\overline{Q}_0\overline{Y} \qquad K_2 = Q_1\overline{Q}_0\overline{Y} + \overline{Q}_1\overline{Q}_0Y$$

3(b)Design a four-bit shift register with parallel load using D flip-flops. There are two control inputs: shift and load. When shift = 1, the content of the register is shifted by one position. New data are transferred into the register when load = 1 and shift = 0. If both control inputs are equal to 0, the content of the register does not change.

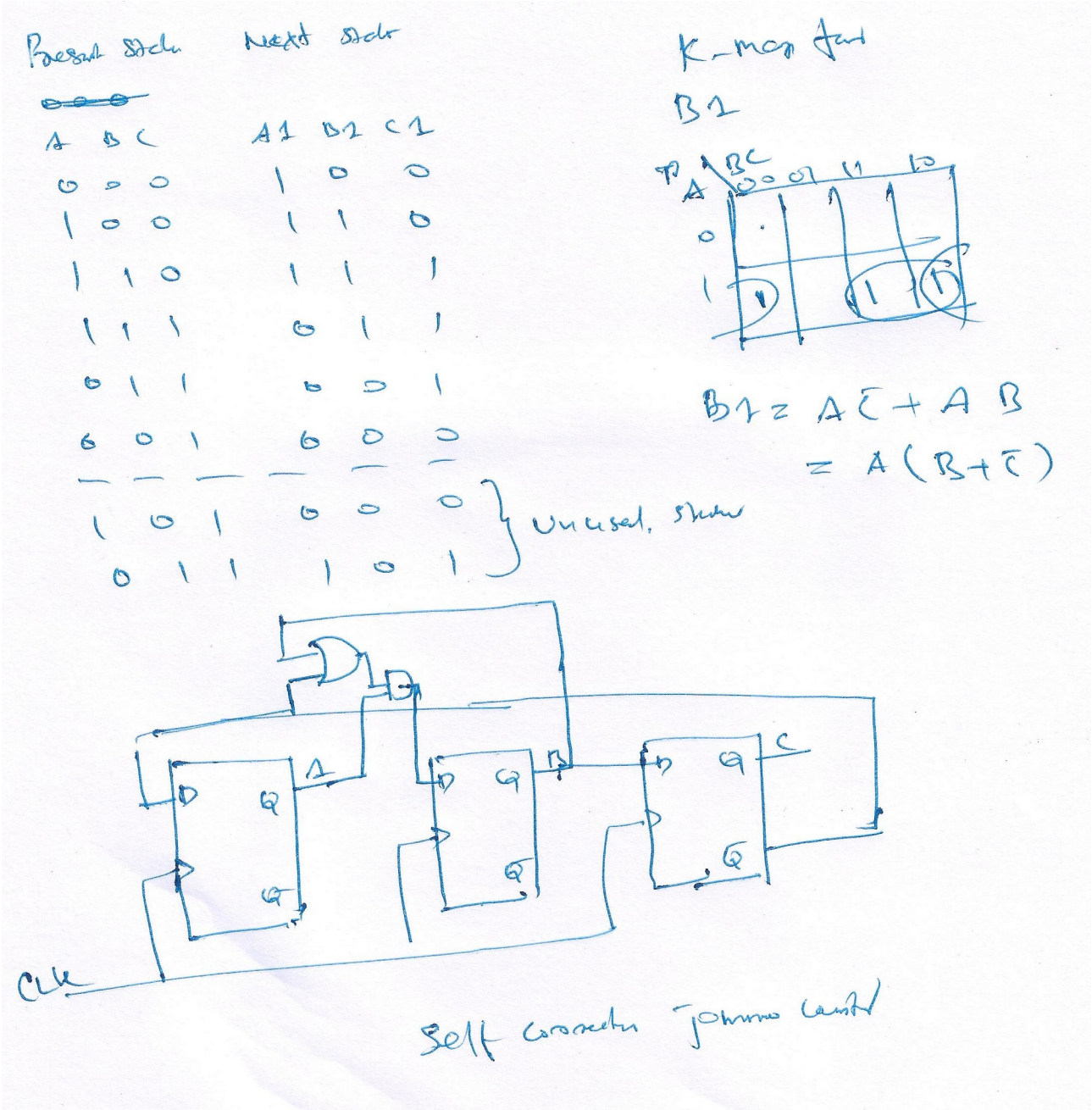
First stage of register:



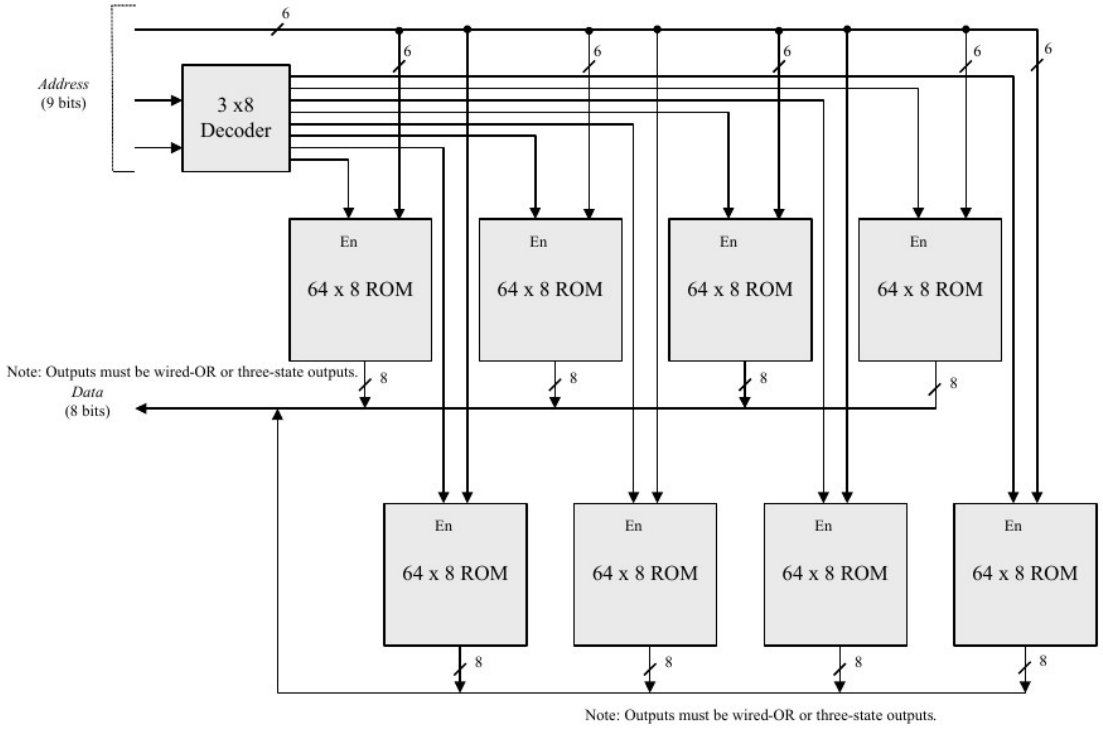
4{a}Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010.



4(b)Design a 3-bit self correcting Johnson counter



5(a) Using 64 * 8 ROM chips with an enable input, construct a 512 * 8 ROM with eight chips and a decoder.



5(b) List the programming table for the BCD-to-excess-3-code converter for
(i)PAL
(ii) PL A

PLA

$w = A + BC + BD$
$w' = A'B' + A'C'D'$
$x = B'C + B'D + BC'D'$
$x' = B'C'D' + BC\ \ BD$
$y = CD + C'D'$
$y' = C'D + CD'$
$z = D'$
$z' = D$
Use w, x', y, z (7 terms)

	Product term	Inputs A B C D	Outputs F_1 F_2 F_3 F_4
A	1	1 - - -	1 - - -
BC	2	- 1 1 -	1 1 - -
BD	3	- 1 - 1	1 1 - -
$B'C'D'$	4	- 0 0 0	- 1 - -
CD	5	- - 1 1	- - 1 -
$C'D'$	6	- - 0 0	- - 1 -
D'	7	- - - 0	- - - 1
			T C T T

PAL

Product term	AND Inputs A B C D	Outputs
1	1 - - -	$w = A + BC + BD$
2	- 1 1 -	
3	- 1 - 1	
4	- 0 1 -	$x = B'C + B'D + BC'D'$
5	- 0 - 1	
6	- 1 0 0	
7	- - 1 1	$y = CD + C'D'$
8	- - 0 0	
9	- - - -	
10	- - - 0	$z = D'$
11	- - - -	
12	- - - -	