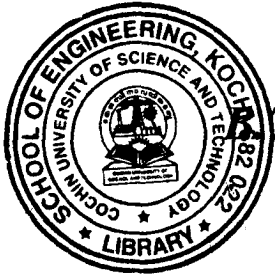


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Tech. Degree IV Semester Examination April 2017

CS 15-1403 COMPUTER ARCHITECTURE AND ORGANISATION (2015 Scheme)

Time : 3 Hours

Maximum Marks : 60

PART A

(Answer *ALL* questions)

(10 × 2 = 20)

- I. (a) List the steps needed to perform the execution of the machine instruction STORE R1, LOC.
- (b) What are the condition code flags available? How do they help in detecting anomalies in results?
- (c) What is the principle of operation of Carry Look ahead adders? Calculate the maximum delay experienced when four 4-bit adders are cascaded to form a 16 bit adder in carry look ahead fashion.
- (d) What are the relative merits and demerits of horizontal and vertical micro instruction formats?
- (e) Explain the LRU replacement strategy and its implementation.
- (f) What is the role of TLB in a virtual memory system?
- (g) What are the different ways available to enable and disable interrupts?
- (h) Discuss the system of device identification followed in vectored interrupt system.
- (i) A computer system has main memory consisting of 1M words. It also has a 4K work cache organized in the block set associative manner, with 4 blocks per set and 64 words per block.
 - (i) How many bits are there in main memory address?
 - (ii) Calculate the number of bits in each of TAG, SET and WORD fields of the main memory address format.
- (j) Differentiate between the features of asynchronous and synchronous DRAMS.

PART B

(4 × 10 = 40)

- II. (a) A list of student marks which contains j test scores for each student along with student id. Assume there are n students. Write an assembly language program for computing the sums of scores on each test and store these sums in the memory locations SUM, SUM+4, SUM+8 etc. (5)
- (b) Explain how parameter passing is achieved using stack. What is the role of Frame Pointer (FP) in it? (5)

OR**(P.T.O.)**

- III. (a) Register R1 and R2 of a computer contain the decimal values 1200 and 4600 respectively. What is the effective address of the memory operand in each of the following instructions? (4)
- (i) LOAD 20 (R1), R5
 - (ii) STORE R5, 30 (R1, R2)
 - (iii) ADD-(R2), R5
 - (iv) SUB (R1)+,R5
- (b) Implement the high level language statement $C=A+B$ using different instruction formats. (3)
- (c) What are the two schemes followed for byte addressability? (3)
- IV. (a) With the help of a block diagram, explain the microinstruction sequencing with next address field. How is Bit-Oring effectively used there? (5)
- (b) Write the control sequence steps required for executing the following instruction in single bus structure of CPU. (5)
- OR**
- V. (a) Multiply the following signed 2's complement numbers using booth's algorithm. Multiplicand = 110101 and Multiplier = 011011. How does bit pair recording make the multiplication faster? (5)
- (b) With the help of a block diagram, explain restoring division method. What is the modification for non restoring? (5)
- VI. (a) What is meant by locality of reference? Explain the various mapping functions used in cache implementation. (5)
- (b) Draw and explain the internal organization of a 2MX8 DRAM chip. (5)
- OR**
- VII. (a) How does the address translation mechanism work in a virtual memory system? (5)
- (b) Explain the working of a Static RAM (SRAM) cell. How are the read and write operations implemented? (5)
- VIII. (a) How is an ISR different from an ordinary subroutine execution? (3)
- (b) How is the processor handling the problem of simultaneous requests and interrupt nesting? (7)
- OR**
- IX. (a) Draw the block diagram and explain how a typical serial port works. (4)
- (b) What is the need of bus arbitration in DMA? Differentiate between centralized and distributed bus arbitration. (6)