BTS-IV(SS)-02.20-0062 Reg. No. | | | | | | | | |

B

B.Tech. Degree IV Semester Special Supplementary Examination February 2020

CS 15-1403 COMPUTER ARCHITECTURE AND ORGANIZATION

(*2015 Scheme*)

Time: 3 Hours Maximum Marks: 60

PART A

(Answer *ALL* questions)

(10 × 2 = 20)

I. (a) Differentiate between straight line and branching.
(b) List out the various steps needed to execute the instruction ADD (R3, R1).
(c) Write notes on stacks and queues.
(d) What are the advantages and disadvantages of hardwired control?
(e) Define emulation.
(f) Explain the need for carry look ahead addition.
(g) What is memory interleaving? What are the advantages?
(h) Differentiate between static and dynamic memory.
(i) What are vectored interrupts?
(j) Write notes on Universal Serial bus.

PART B

(4 × 10 = 40)

II. (a) With a neat diagram, explain the functional units of a computer. (6)
(b) Differentiate between CISC and RISC architectures. (4)

OR

III. (a) Explain any three addressing modes with an example for each. (6)
(b) Evaluate (A+B) * (C+D) using (i) three address (ii) two address instructions. (4)

IV. (a) Explain the Booths algorithm for fast multiplication with an example. (6)
(b) Explain the timing diagram of a memory read operation. (4)

OR

V. (a) Explain the single bus architecture of the data path inside a processor. (6)
(b) Explain the principle of restoring division with an example. (4)

VI. (a) What is cache coherence problem? Explain any two cache memory mapping functions. (5)
(b) Explain any two replacement algorithms and compare their performance with an example. (5)

OR

VII. (a) What is translation lookahead buffer? Explain with a diagram. What are the advantages? (4)
(b) With a neat diagram explain how virtual address is translated to physical address. (6)

VIII. (a) Explain any two methods of handling simultaneous requests by devices. (6)
(b) Explain briefly about the SCSI bus. (4)

OR

IX. (a) What are exceptions? Explain any two types of exceptions. (5)
(b) Differentiate between centralized and distributed bus arbitration in DMA. (5)

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