BTS–IV(S)–04.22–0230 Reg. No. | | | | | | | | |

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B.Tech. Degree IV Semester Supplementary Examination
April 2022

CS 15-1403 COMPUTER ARCHITECTURE AND ORGANIZATION

(*2015 Scheme*)

Time: 3 Hours Maximum Marks: 60

PART A

(Answer *ALL* questions)

(10 × 2 = 20)

I. (a) Differentiate between Big-Endian and Little-Endian Assignments with an example.

(b) List out the various steps needed to execute the machine instruction LOAD R2, LOC.

(c) Write notes on Program-Controlled I/O.

(d) What do you mean by prefetching of microinstructions?

(e) Define emulation.

(f) Explain the concept of fast addition.

(g) What is translation lookahead buffer? What are the advantages?

(h) Differentiate between SRAM and DRAM.

(i) What are exceptions? List out any two types of exceptions.

(j) What is the difference between a subroutine and an interrupt-service routine?

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PART B

(4 × 10 = 40)

II. (a) Define stack. Explain with an example the sequence of operations in a stack when a subroutine is encounterd. (6)

(b) Differentiate between Register Transfer Notation and Assembly-Language Notation. (4)

OR

III. (a) What are addressing modes? Explain any two addressing modes with an examples. (6)

(b) Differentiate between CISC and RISC architectures with their advantages. (4)

IV. (a) Explain the functioning of a microprogrammed control unit with necessary diagrams. (6)

(b) Explain the steps in fetching and executing the instruction ADD R3, R4, R5. (4)

OR

V. (a) Design a 4 bit fast adder with look ahead carry. (5)

(b) Explain the principle of non-restoring division with an example. (5)

VI. (a) What is the concept of cache memory? Explain any two cache memory mapping functions. (5)

(b) Explain how address translation is done in paging. (5)

OR

VII. (a) Explain the internal organization of a 16 x 8 memory chip. (5)

(b) What is the need for page replacement? Explain any two page replacement algorithms. (5)

VIII. (a) Explain any two methods of handling simultaneous interruot requests by devices. (5)

(b) Explain briefly about the PCI bus standard. (5)

OR

IX. (a) What are vectored interrupts? How are they handled by the processor? (5)

(b) What is DMA? Explain the fuctioning of DMA controller. (5)

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