FIR and Adaptive Filter Implementation on a FPGA Board

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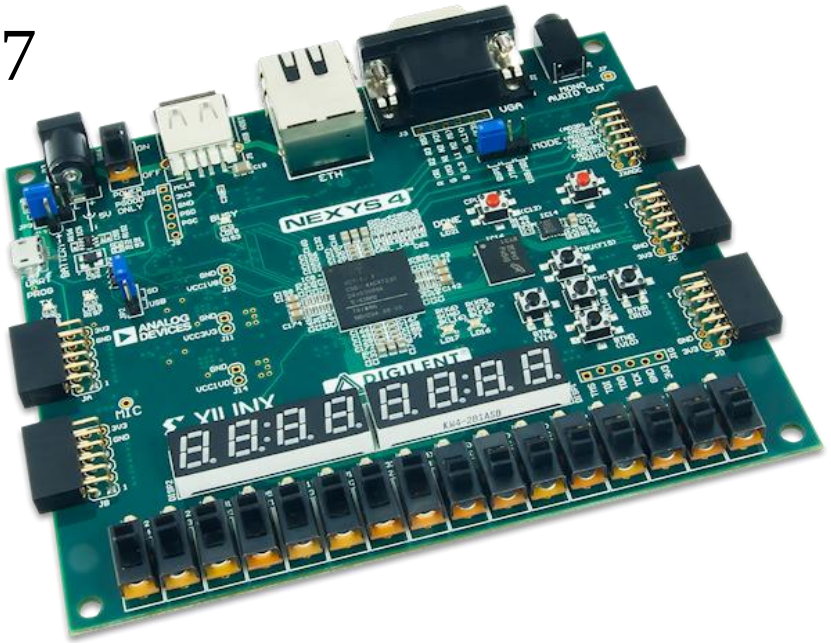
Outline

- Introduction
- Filters
  - FIR Filter
  - LMS Adaptive Filter
  - Block FIR Filter
  - Block LMS Adaptive Filter
- Conclusion
- Reference

Introduction

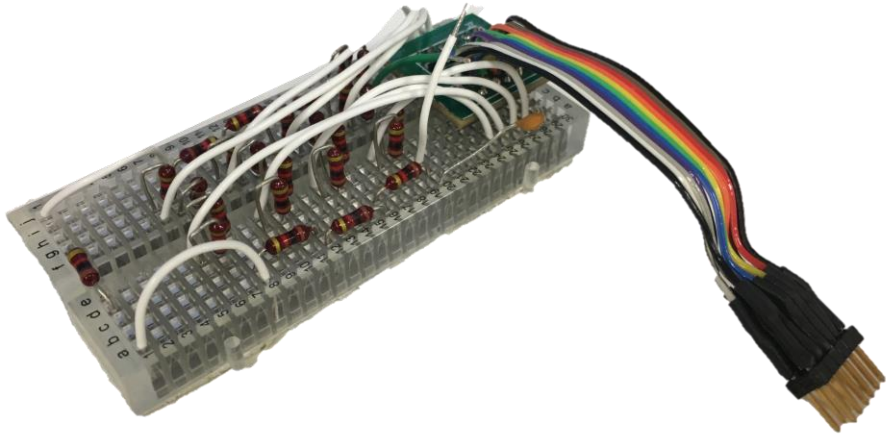
- Development Tools

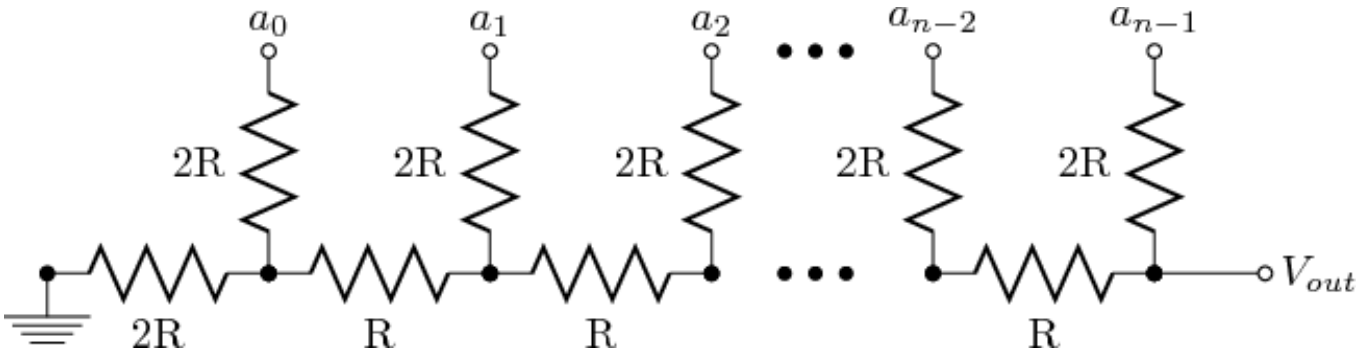
- Xilinx Vivado 2016.2
- Matlab and Verilog
- Digilent Nexys 4 Artix-7



Introduction

- R2R Digital to Analog Converter (DAC)



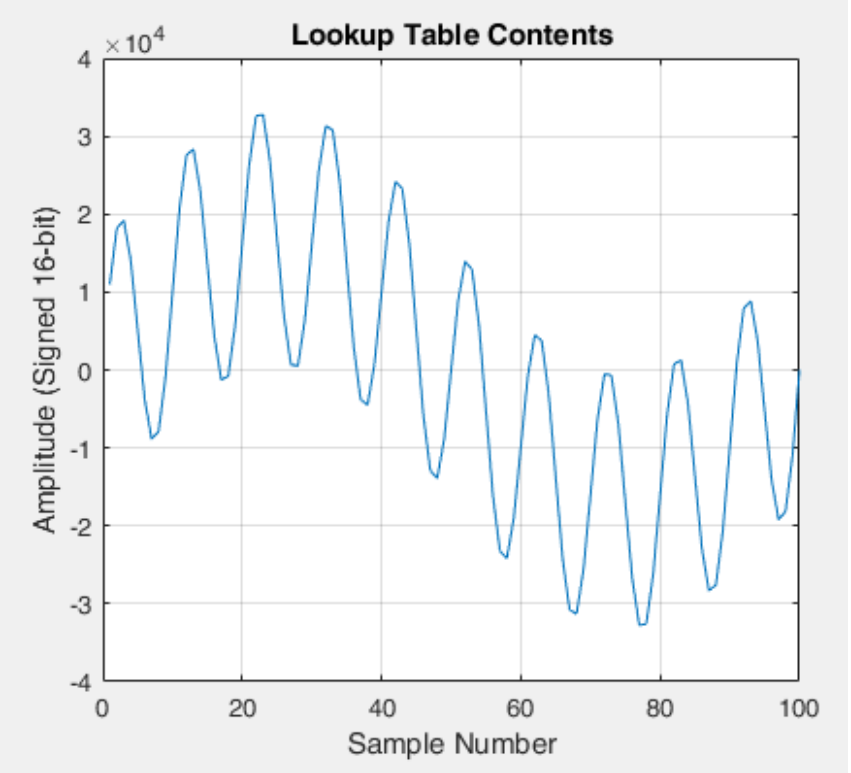


Introduction
- Clock Enable

- For the non-block filters, clock enable generator is used to slow down the frequency to 44KHz (audio sample rate).
- It is not used in the block filters.

Introduction
- Tone/Waveform Generator

- Provides input signal for each filter design.
- 100 samples. Looped forever.
- For the non-block filters, the table is sampled at 44KHz producing a combination of 440Hz and 4.4KHz.
- For the block filters, it is sampled at the system frequency. Which is 60MHz and 50MHz for Block FIR and Block LMS respectively.

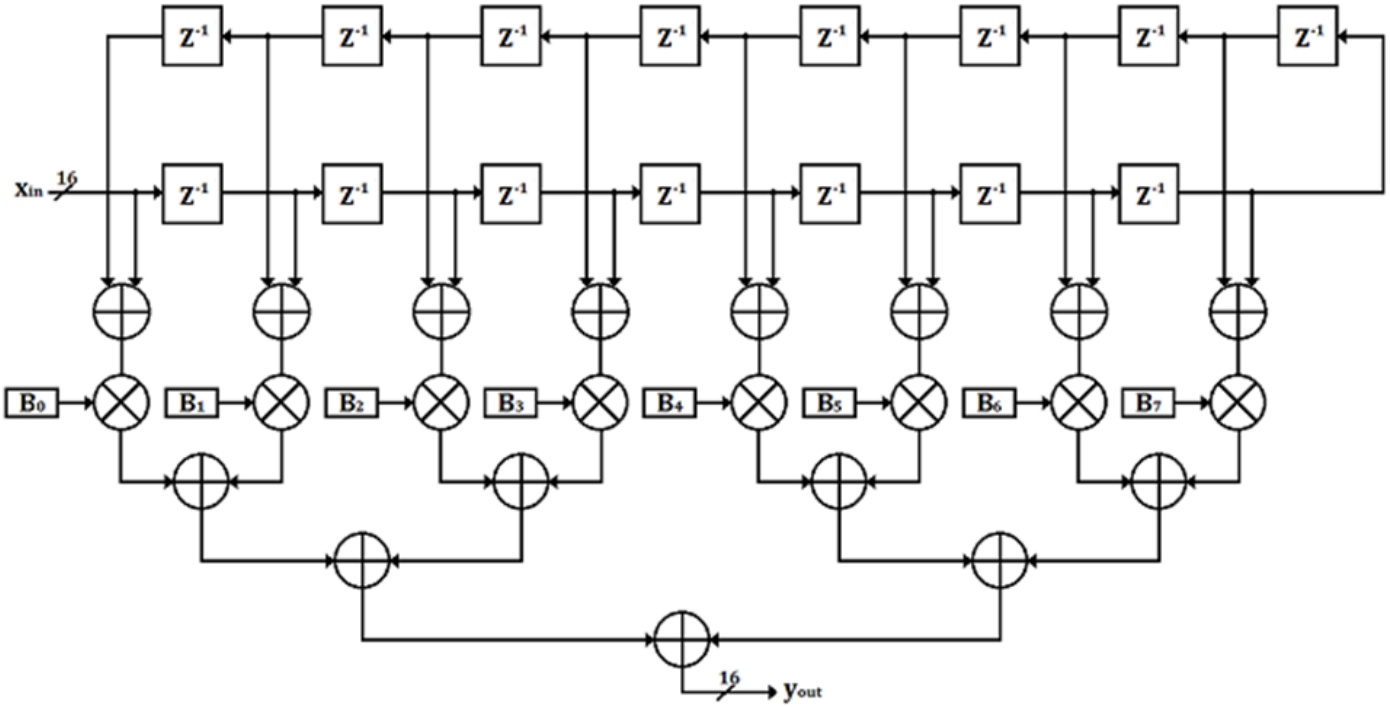


FIR Filter

- The simplest of the 4 filters.
- Uses pre-adders to take advantage of coefficient symmetry. Reduces the number of multipliers from 16 to 8.
- Implements an adder tree to calculate the final output.
- The Xilinx software optimized out the multipliers due to the small filter footprint.

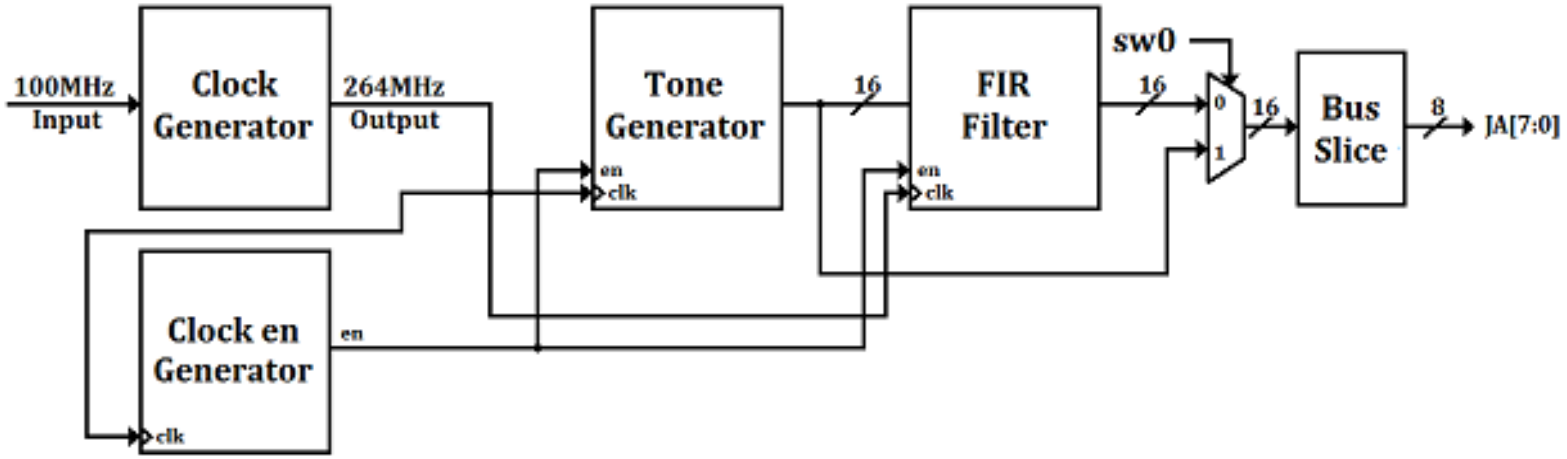
FIR Filter

- Filter Diagram



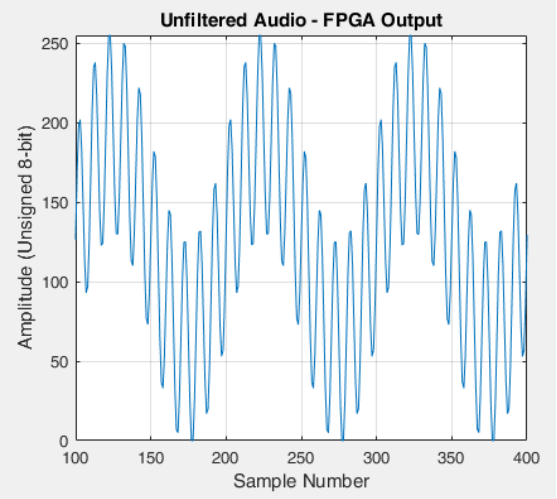
FIR Filter

- System Diagram

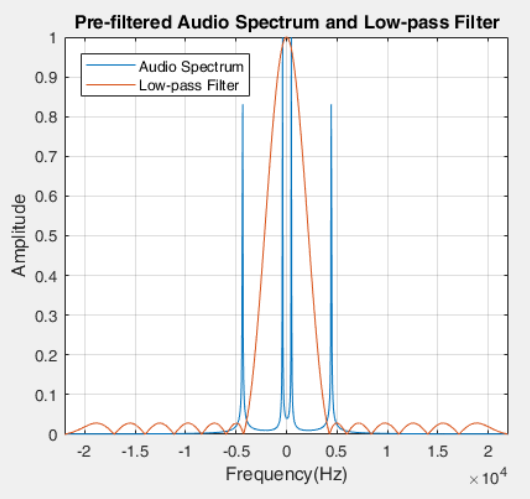


FIR Filter

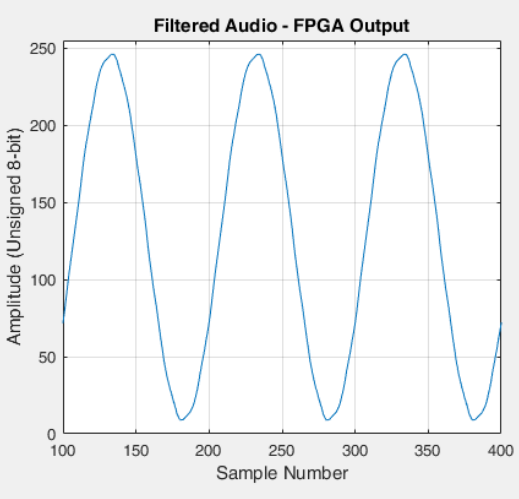
- Simulation: Matlab Waveforms



Unfiltered Audio



Pre-filtered Audio Spectrum with Low-pass Filter Overlay

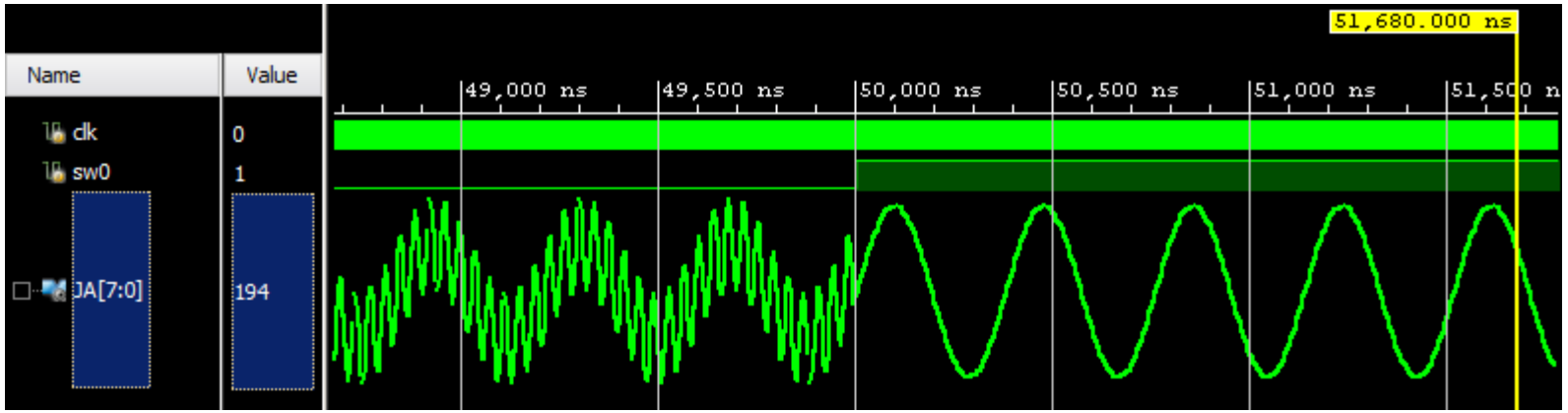


Filtered Audio

Santa Clara University

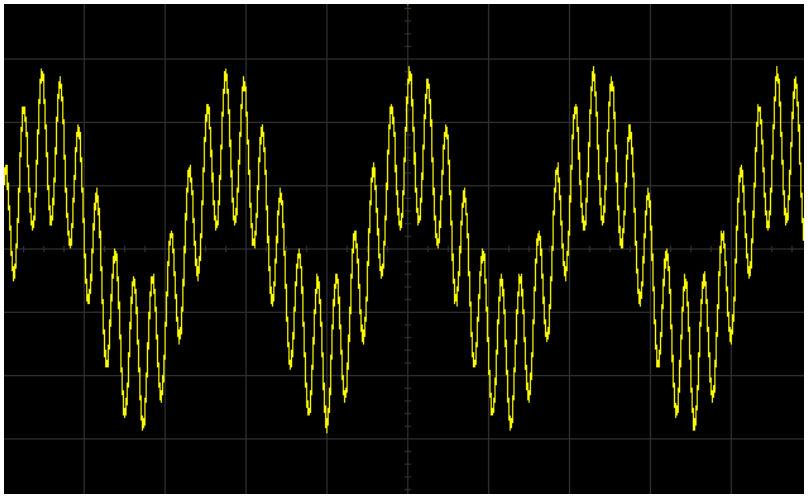
FIR Filter

- Simulation: Vivado Waveforms

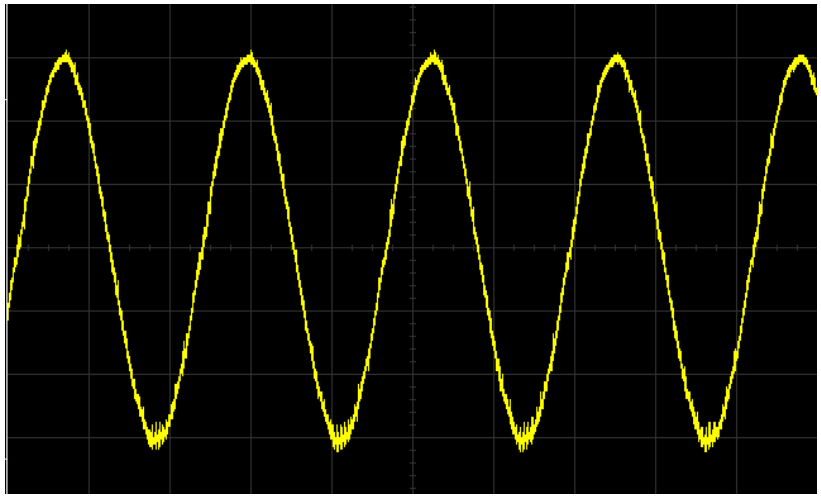


FIR Filter

- Implementation Oscilloscope Waveforms



Before Filtering



After Filtering

FIR Filter

- Performance

- Resource Usage

Resource	Utilization	Available	Utilization %
LUT	1072	63400	1.69
FF	287	126800	0.23
IO	10	210	4.76
BUFG	2	32	6.25
MMCM	1	6	16.67

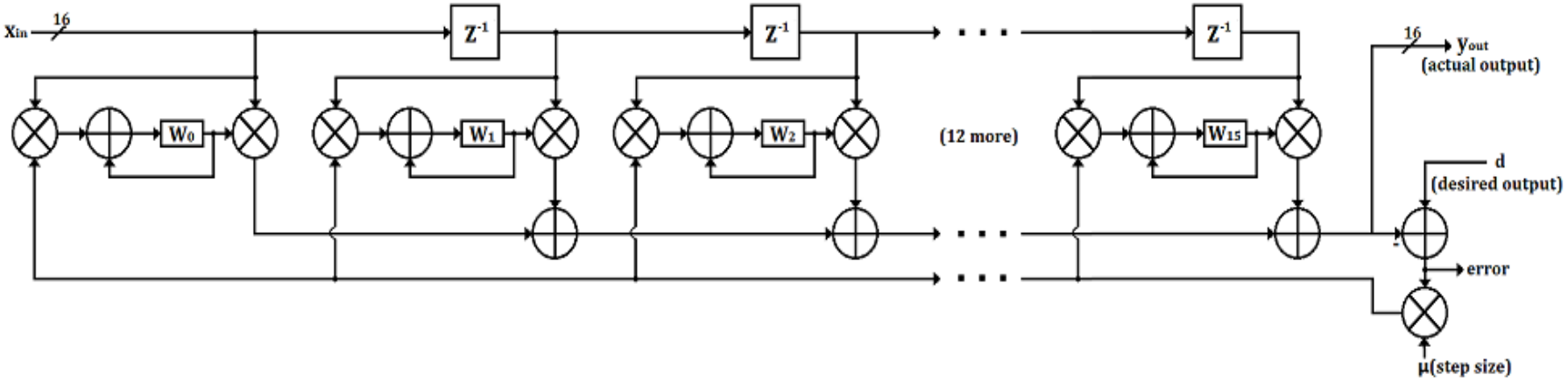
- Maximum Clock Frequency
  - 264MHz

LMS Adaptive Filter

- Implements the Least Mean Square (LMS) algorithm.
- The slowest of the 4 filters.
- Cannot take advantage of coefficient symmetry. Uses 2 multipliers per coefficient and an additional removable 1 multiplier for μ (step size). The number of multipliers is 2*16 (+1) = 32 (or 33).

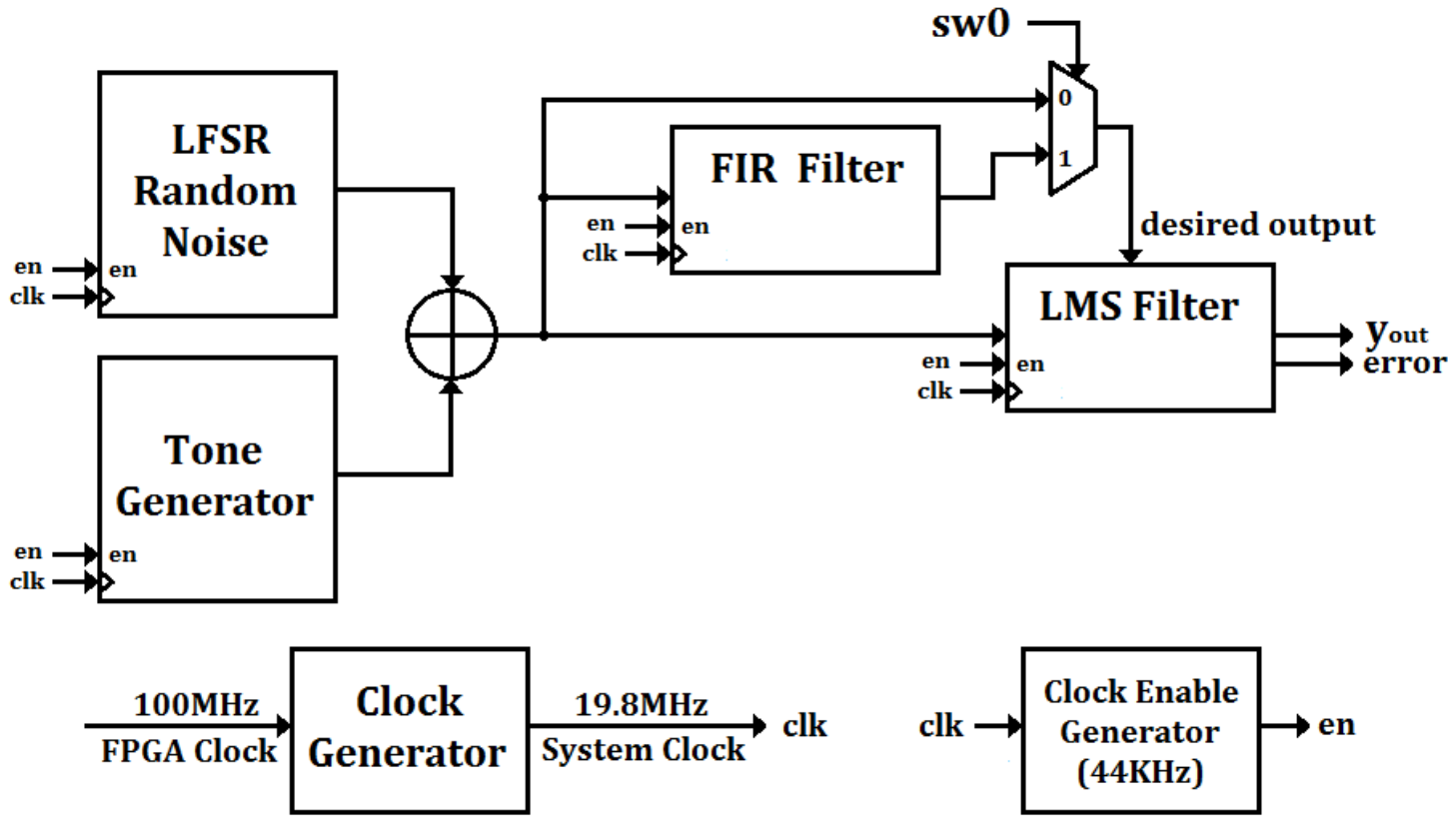
LMS Adaptive Filter

- Filter Diagram



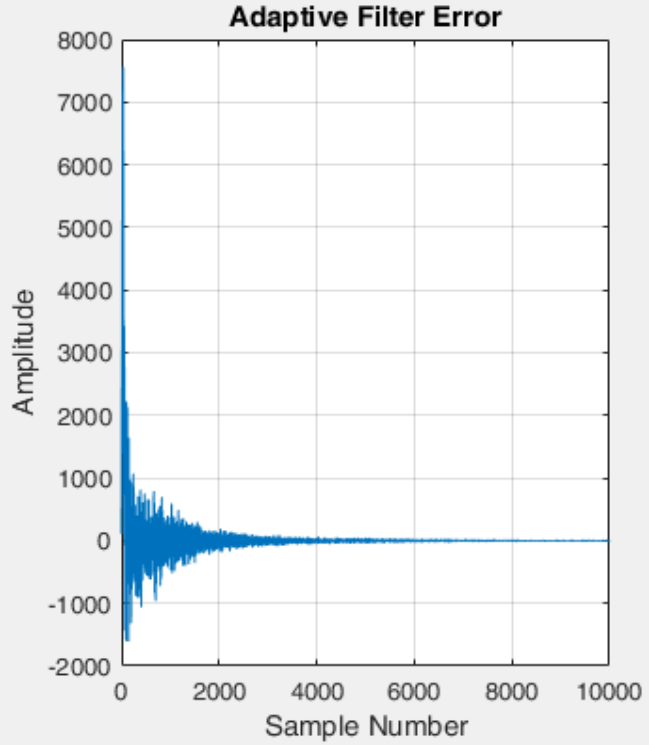
LMS Adaptive Filter

- System Diagram

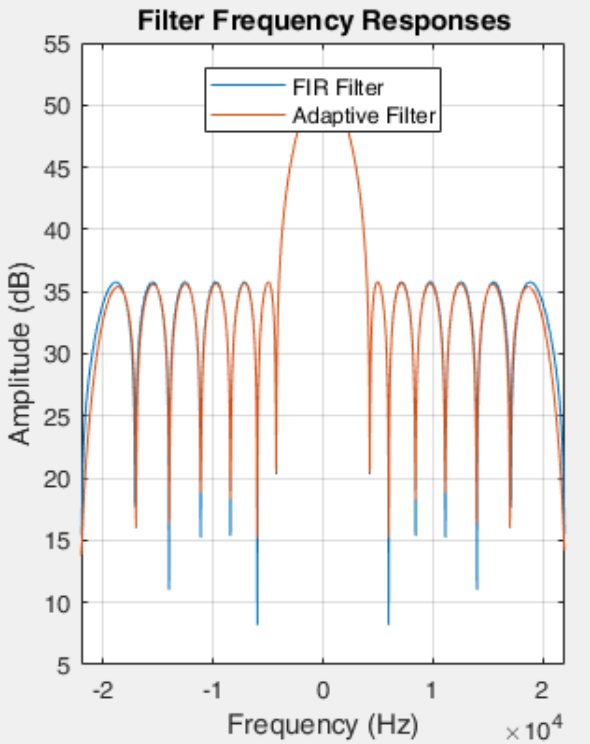


LMS Adaptive Filter

- Simulation: Matlab Waveforms



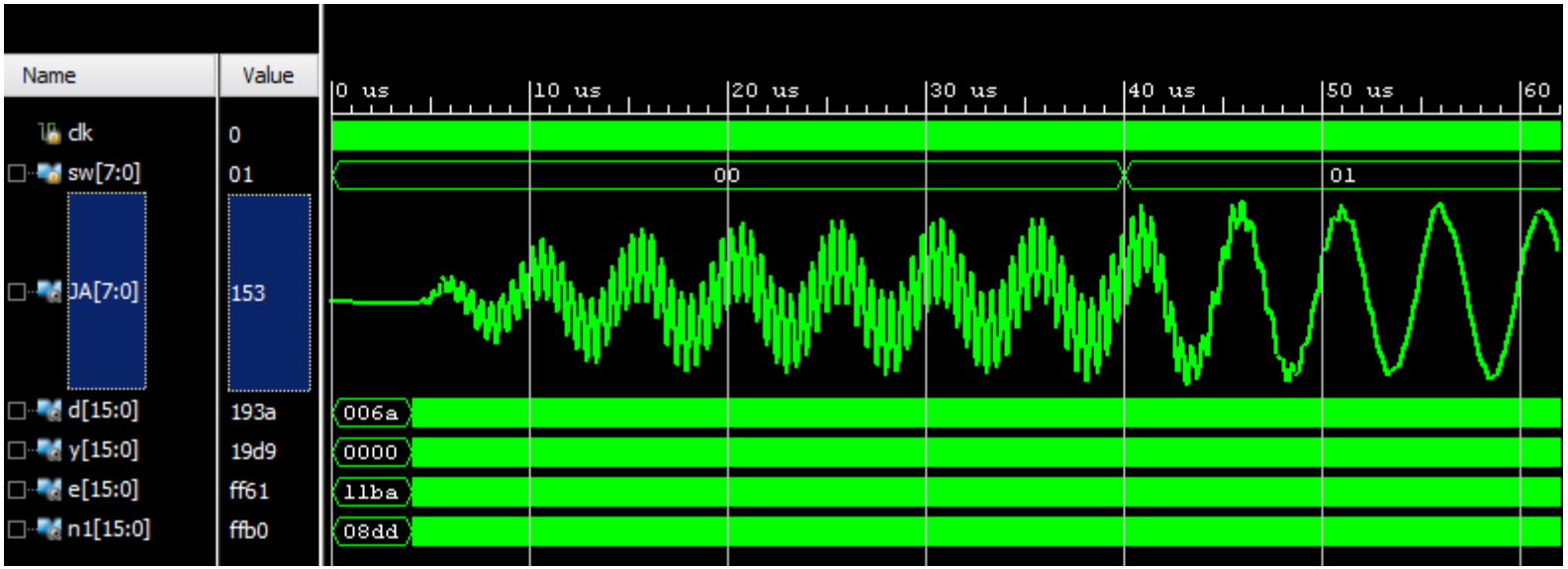
Adaptive Filter Error



Filter Frequency Responses

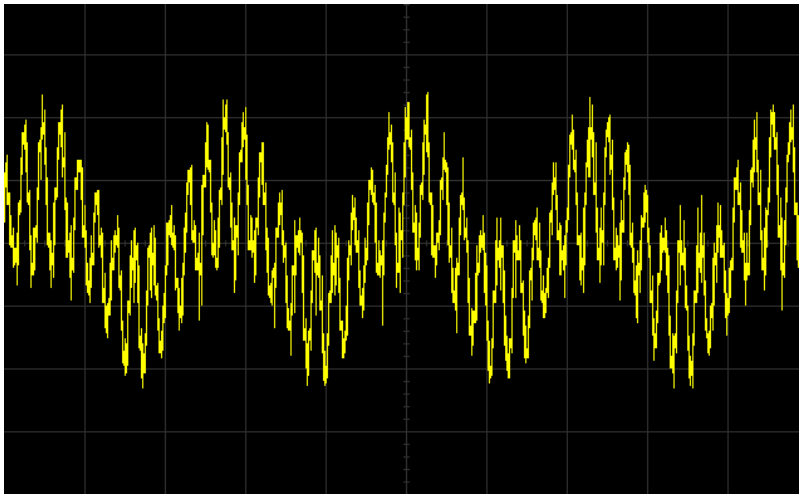
LMS Adaptive Filter

- Simulation: Vivado Waveforms

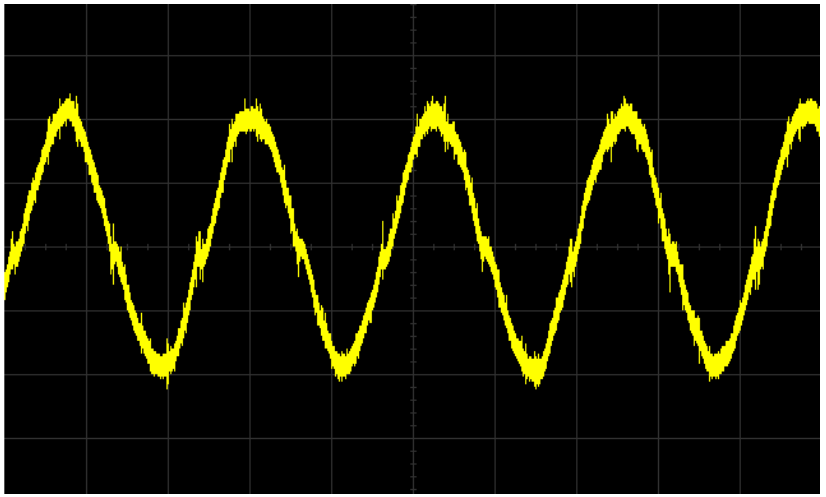


LMS Adaptive Filter

- Implementation Oscilloscope Waveforms



Tone Table as the Desired Output



FIR Filter as the Desired Output

LMS Adaptive Filter
- Performance

- Resource Usage

Resource	Utilization	Available	Utilization %
LUT	1686	63400	2.66
LUTRAM	1	19000	0.01
FF	569	126800	0.45
DSP	32	240	13.33
IO	10	210	4.76
BUFG	2	32	6.25
MMCM	1	6	16.67

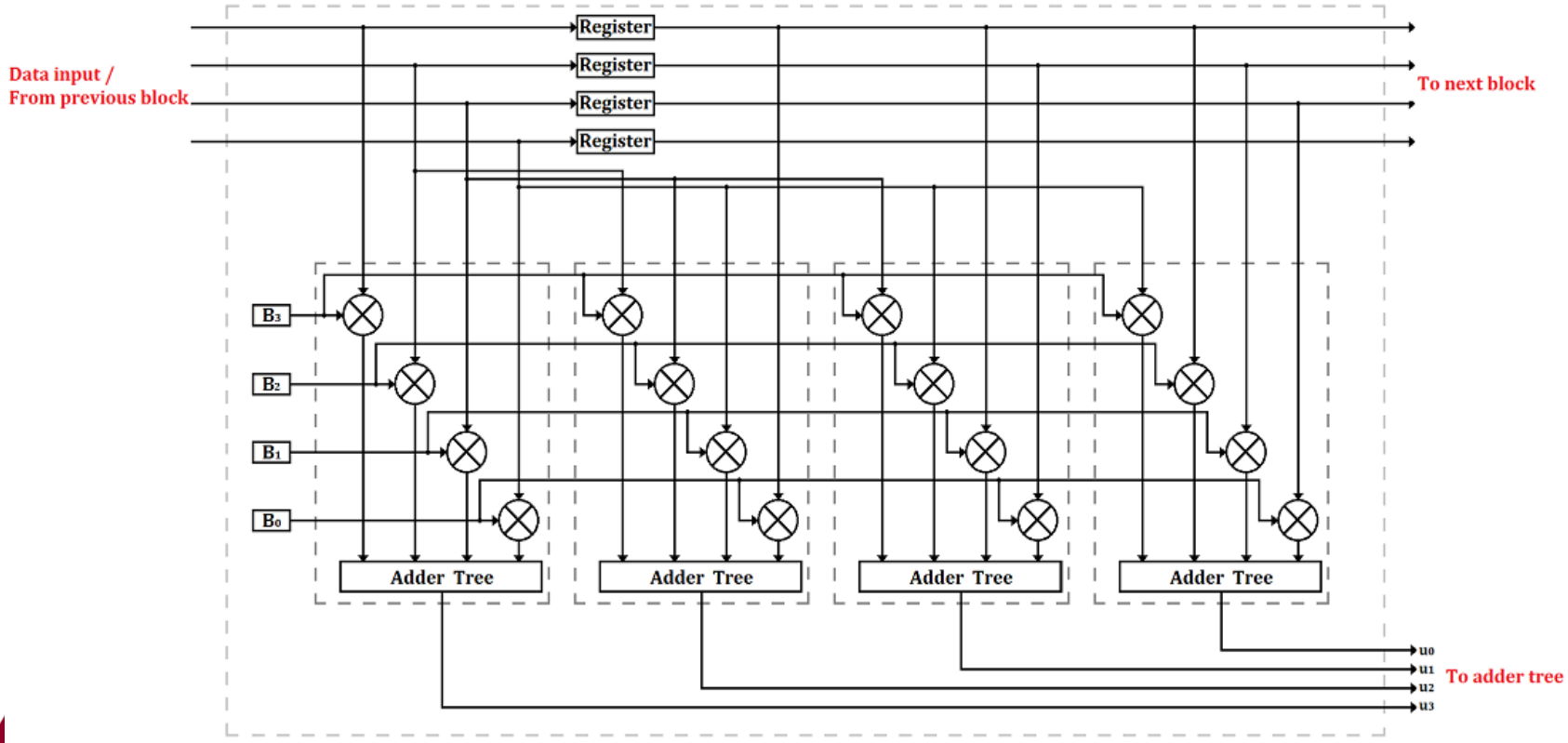
- Maximum Clock Frequency
  - 19.8MHz

Block FIR Filter

- Has a block length of 4.
- Processes 4 inputs and 4 outputs per clock cycle.
- Uses 64 multipliers.
- Not as fast as the FIR filter due to the larger footprint.

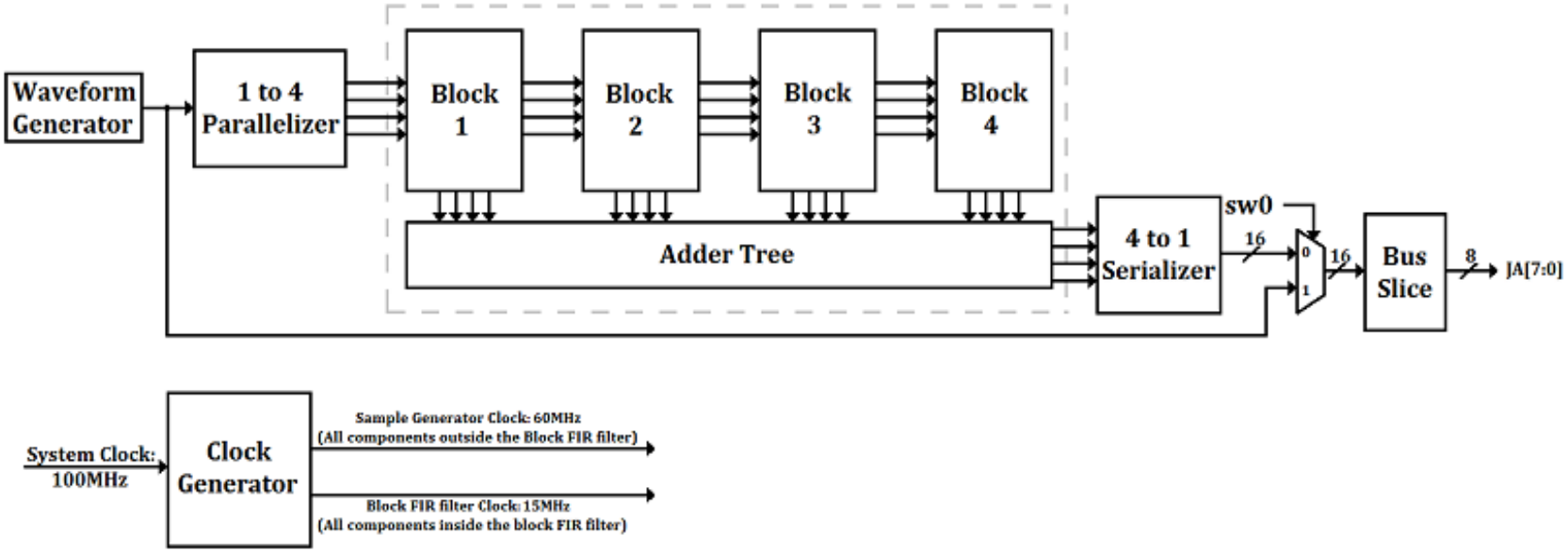
Block FIR Filter

- Filter Diagram



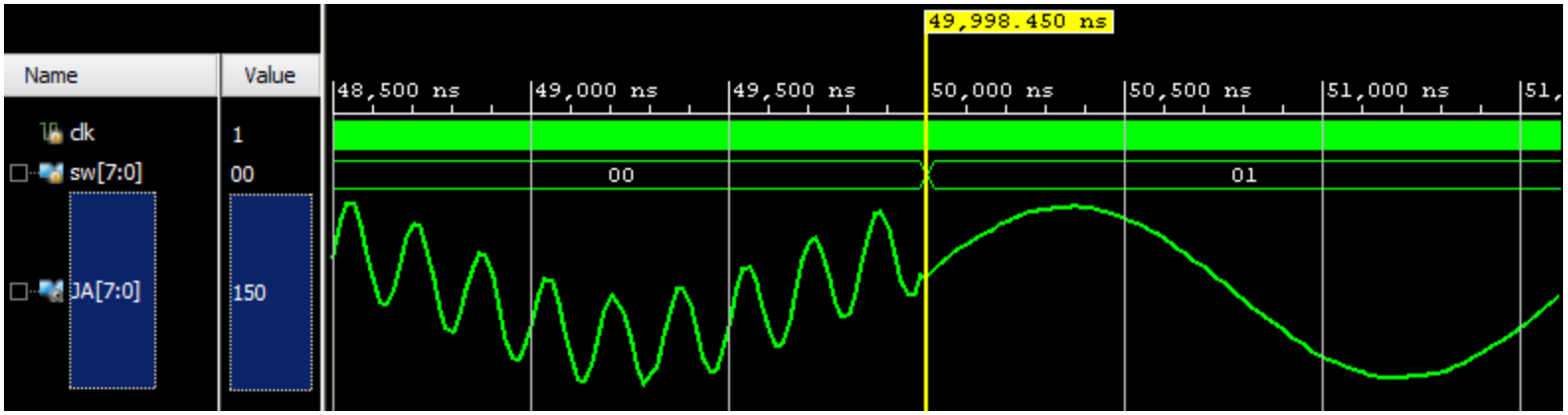
Block FIR Filter

- System Diagram



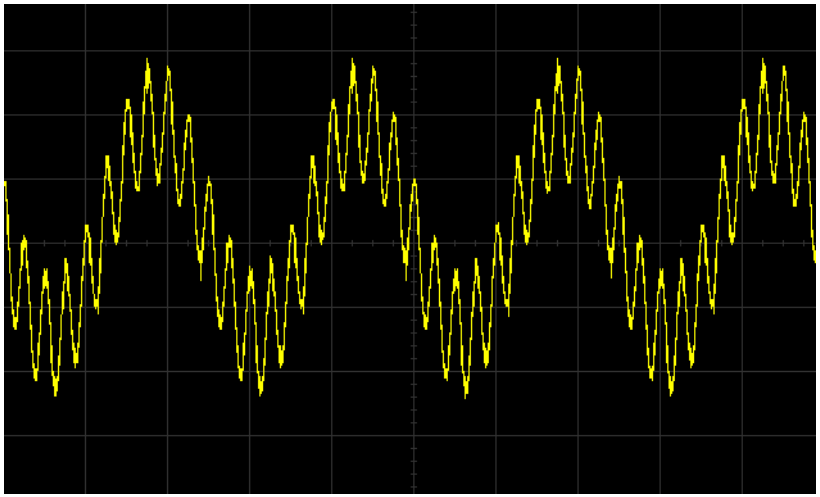
Block FIR Filter

- Simulation: Vivado Waveforms

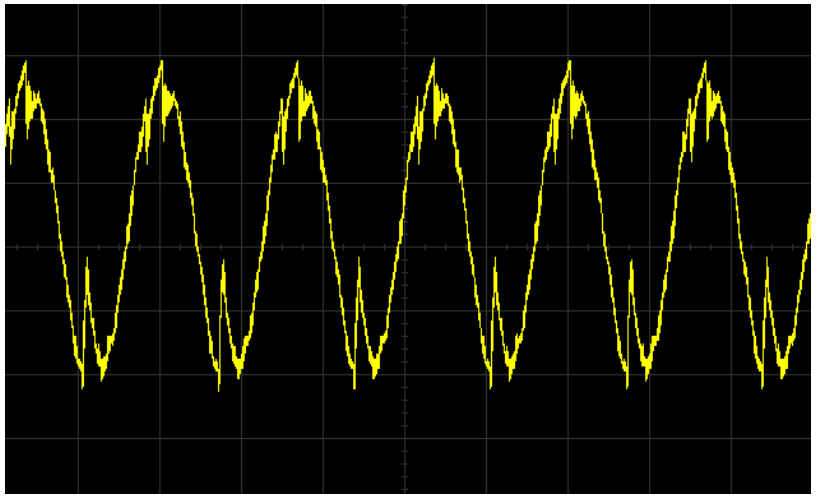


Block FIR Filter

- Implementation Oscilloscope Waveforms



Before Filtering



After Filtering

Block FIR Filter

- Performance

- Resource Usage

Resource	Utilization	Available	Utilization %
LUT	293	63400	0.46
FF	287	126800	0.23
DSP	64	240	26.67
IO	10	210	4.76
BUFG	3	32	9.38
MMCM	1	6	16.67

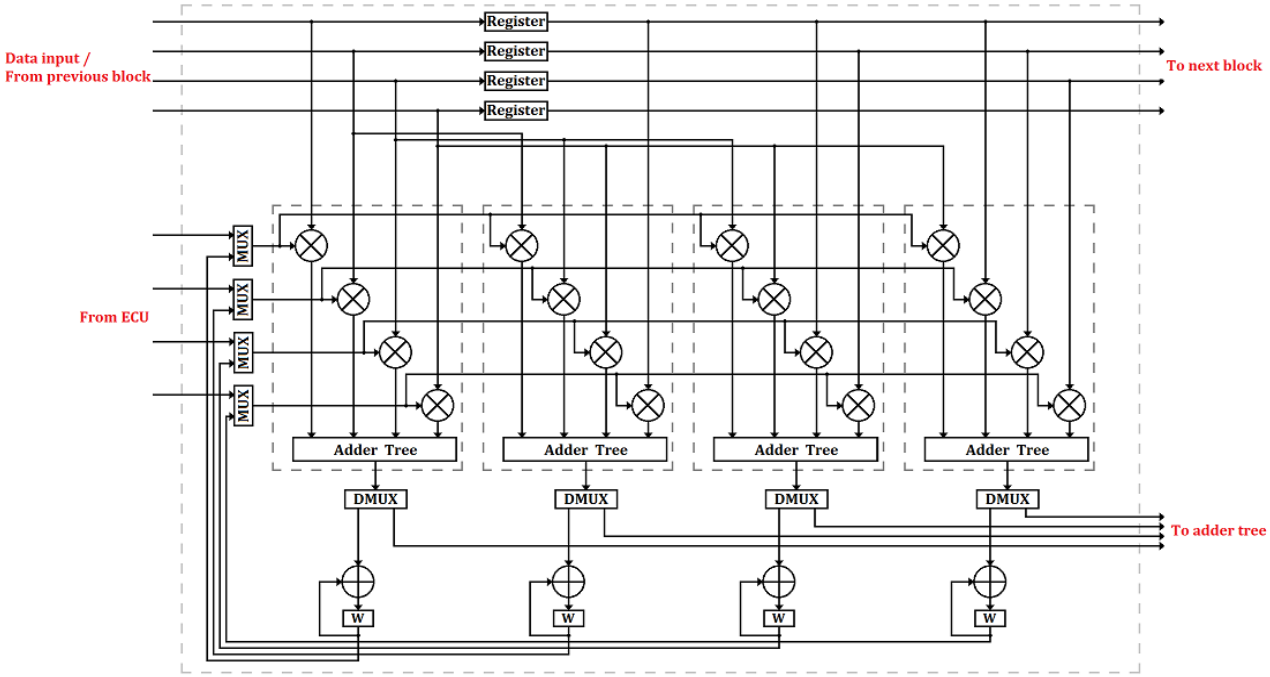
- Maximum Clock Frequencies
  - Sample Generator: 60MHz
  - Filter: 15MHz

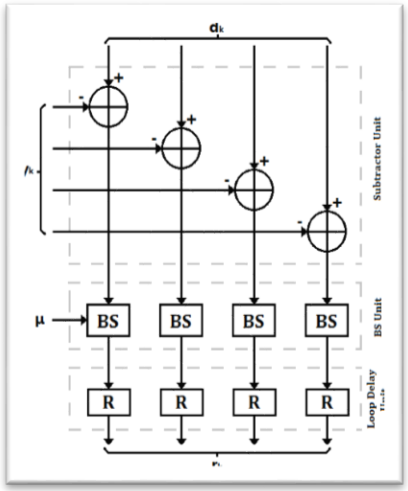
Block LMS Adaptive Filter

- The most complex of the 4 filters.
- Processes 4 inputs and 4 outputs every 2 clock cycles.
- The only filter with two stages. One for updating the coefficients, and the other for calculating the output.
- Uses 64 multipliers.
- More than twice as fast as the LMS filter.

Block LMS Adaptive Filter

- Filter Diagram

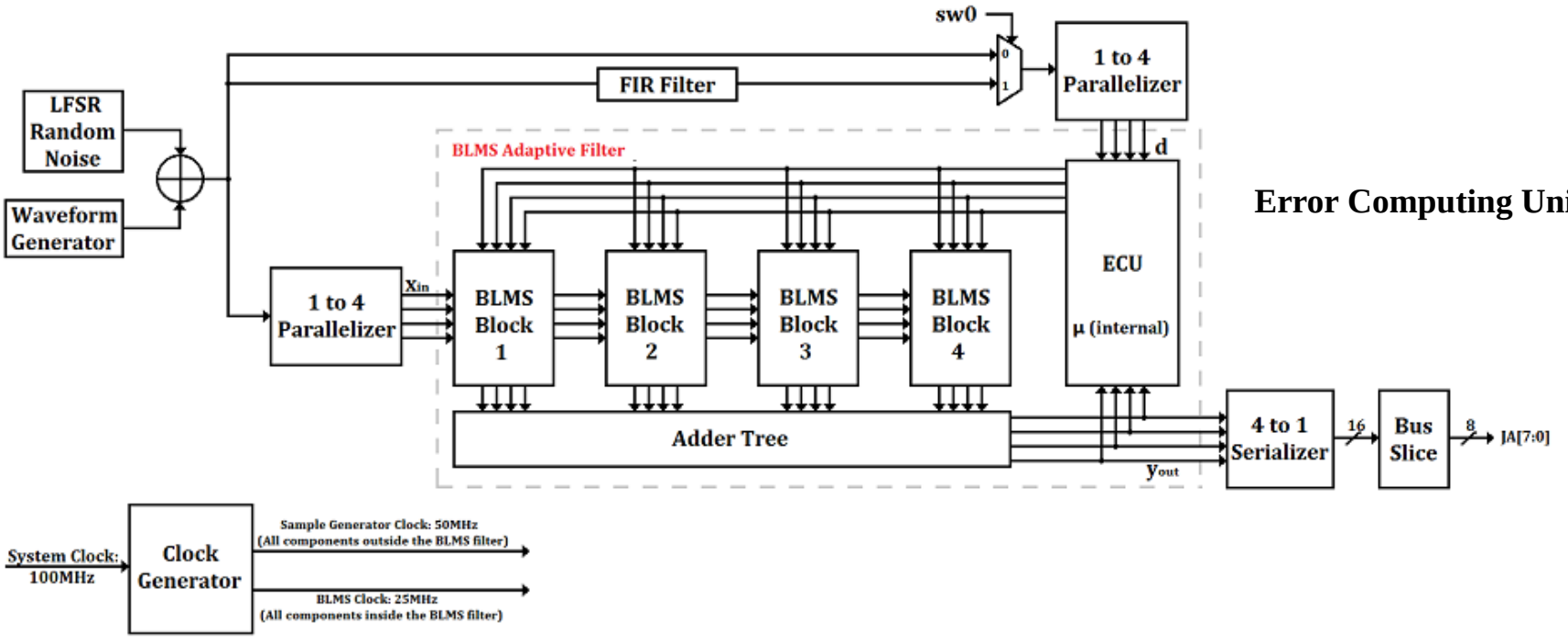




Error Computing Unit

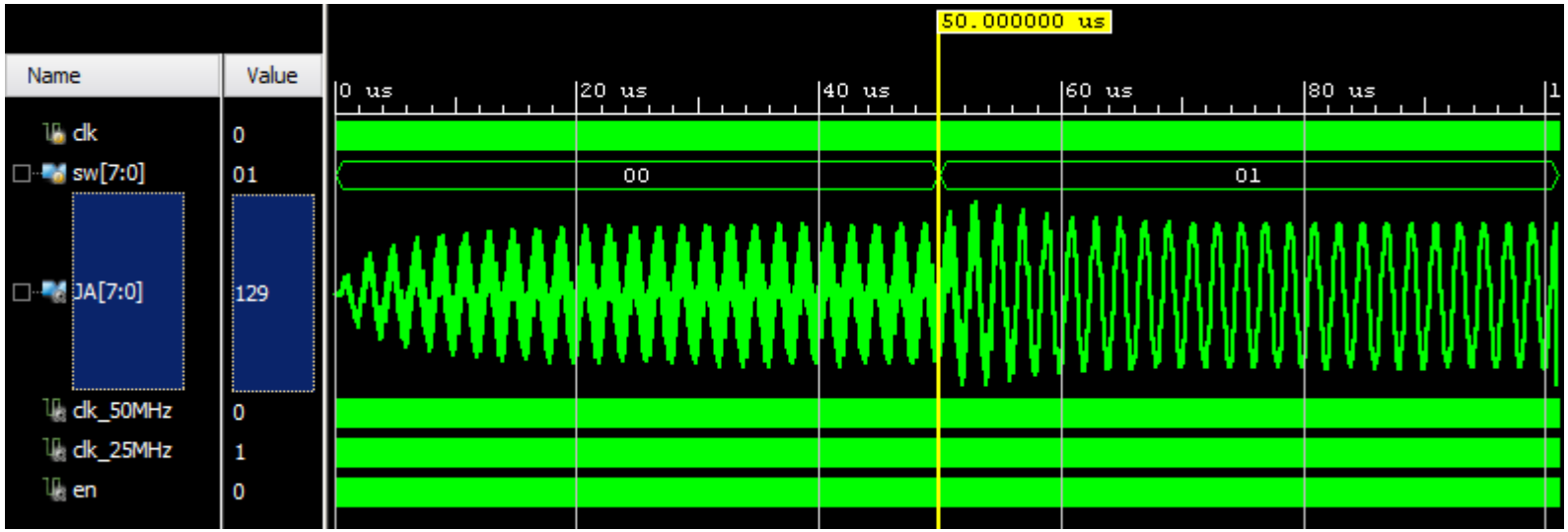
Block LMS Adaptive Filter

- System Diagram



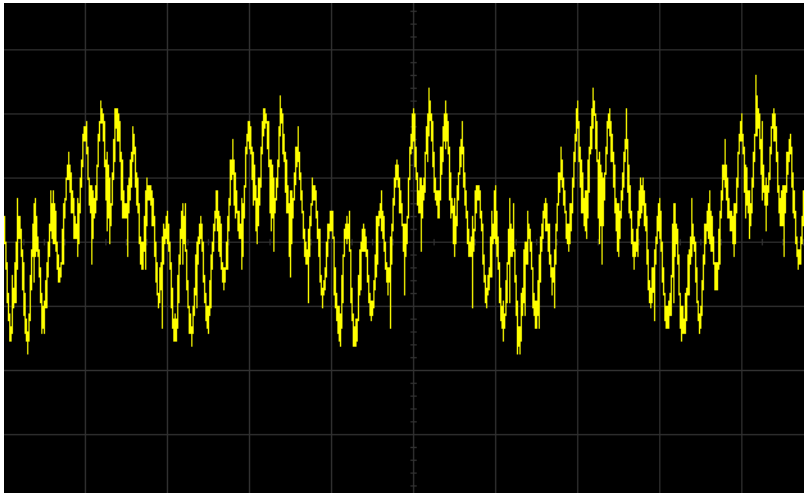
Block LMS Adaptive Filter

- Simulation: Vivado Waveforms

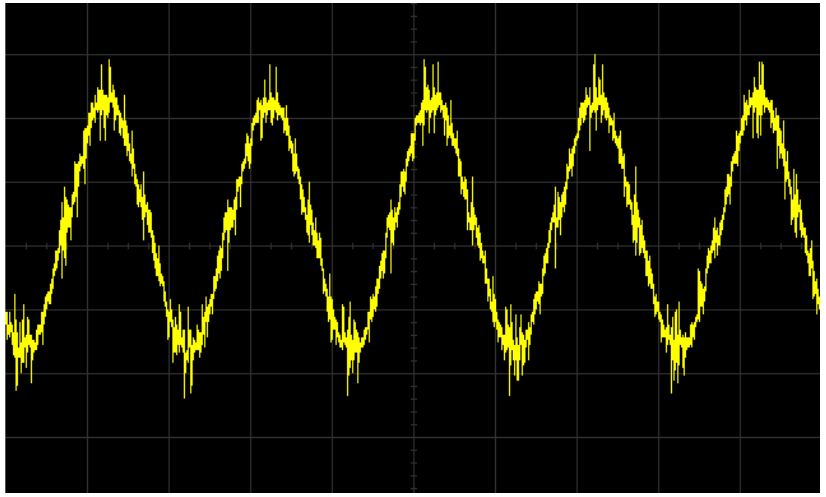


Block LMS Adaptive Filter

- Implementation Oscilloscope Waveforms



Tone Table as the Desired Output



FIR Filter as the Desired Output

Block LMS Adaptive Filter

- Performance

- Resource Usage

Resource	Utilization	Available	Utilization %
LUT	1973	63400	3.11
LUTRAM	1	19000	0.01
FF	1044	126800	0.82
DSP	64	240	26.67
IO	10	210	4.76
BUFG	3	32	9.38
MMCM	1	6	16.67

- Maximum Clock Frequencies
  - Sample Generator: 50MHz
  - Filter: 25MHz

Conclusion

Filters		FIR Filter	LMS Adaptive Filter	Block FIR Filter	Block LMS Filter
Resource Usage	Multiplier	0	32	64	64
	LUT	1072	1686	293	1973
	FF	287	569	287	1044
Maximum Frequency	Sample Generator	264MHz	19.8MHz	60MHz	50MHz
	Filter			15MHz	25MHz

Reference

- Multiplier-based structure for BLMS adaptive filters, http://shodhganga.inflibnet.ac.in/bitstream/10603/120732/13/13_chapter3.pdf
- LMS Adaptive Filtering, https://ocw.mit.edu/courses/mechanical-engineering/2-161-signal-processing-continuous-and-discrete-fall-2008/lecture-notes/lecture_25.pdf
- Resistor ladder, https://en.wikipedia.org/wiki/Resistor_ladder

Thanks for Listening!