



Instituut voor Engineering en Applied Science
Opleiding Elektrotechniek

HARDWARE DESIGN OF A WIRELESS AND PORTABLE HIGH-DENSITY SEMG ACQUISITION SYSTEM

*FOR THE DETERMINATION OF THE OPTIMAL LOCATION
OF EMG ELECTRODES IN MYOELECTRIC
PROSTHESIS.*

Bachelor thesis

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Rotterdam, 15 November 2019

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Version management

The version is updated to a new number after report has been evaluated by someone.

Version	Date	Author	Modification
1	15-05-2019	Oliver Kersten	Added chapters
2	03-09-2019	Oliver Kersten	Changed document setup, requirements and system design
3	28-09-2019	Oliver Kersten	Added GUI results
4	15-10-2019	Oliver Kersten	Added: reflection, conclusion, summary, information about PCB design

Abbreviation List

MCU	Micro-controller
FSR	Full-scale range
MFB	Multiple feedback
IA	Instrumentation amplifier
ADC	Analog to digital converter
AFE	Analog front end
SD	Single differential (also known as bipolar configuration)
MP	monopolar
BW	Bandwidth
HD-SEMG	High-Density SEMG system, an EMG system containing a high number of EMG channel where the electrodes are densely placed together.
USP	Unique selling point
CSA	Cross-sectional area
FDA	Fully differential amplifier
Sps/ch	Number of samples per second per channel
SEMG	Surface Electromyography
ASIC	application-specific integrated circuits
HMI	Human Machine Interface, interaction between human and product that visualizes a human interaction, e.g. the speed display on a car.
SH	Sample and hold device

Summary

Myoelectric prostheses are artificial limbs that use electromyographic (EMG) signals to control its function, this could be a bionic hand, arm, knee or ankle. The EMG signal is rectified, smoothed, and a threshold value set to activate the motor in one or another direction to open or close the bionic hand. This method is also known as direct control or 'DC'. The placement of the EMG electrodes inside the prosthesis starts by placing test electrodes over agonist/antagonist residual muscle pairs of the limb. The place of the electrodes and the gain is adjusted until an independent signal above the threshold value is acquired at each electrode during different hand gestures. The problem with this method is that it is based on a trial and error method and the optimal location where the patient has the most control over the agonist/antagonist may never even be found. This results that in most cases, the electrodes settings in DC systems need to be adjusted while the prosthesis is being used by the patient to maintain high performance. By correctly placing the electrodes on the patient limb, this problem should be minimised or even resolved. This was converted into the following hypothesis "The performance of direct control can be improved by correctly locating the agonist/antagonist of the residual limb where the patient has the most amount of control over during different hand gestures". Rather than answering this hypothesis, this thesis intends to present a prototype that can be used to verify this hypothesis and later to be used in clinical settings. This can be accomplished by visualizing the electrical surface potential distribution (EMG) generated by all limb's muscles during different hand-gestures (also known as a HD-SEMG recordings). This system was given the following minimum requirement: 64 monopolar channels, an EMG BW of 10 – 500Hz and a simulations sample frequency of 2kSps/ch. Multiple AFE designs were presented and tested on IRN, baseline noise, CMRR, gain and phase shift. This resulted in the following system design: an IA with a 'quashi' high pass filter for dc-offset rejection, followed by a unity gain high-pass filter for additional dc-offset rejection, a MFB FDA low-pass filter for antialiasing filtering, a daisy-chainable 24-bit 8 channel simulations sampling ADC to provide a single data communication line to the MCU for all the 64 channel which will send the data through USB 2.0 to the PC to be visualized. The system was validated to have the following system specifications, see Table 9.

	CMRR (dB)	IRN (μV_{rms})	Gain (V/V)	EMG BW (Hz)	Baseline Noise (mV_{rms}) SD - MP	Input impedance	Sample Frequency Sps/ch	
System specifications	105	2,09	239	10-2000Hz	3,1	29	100GΩ	250

Table 1 Design specification summary

Table 9 states that the system is only capable of sampling frequency 250Sps/ch. The design is capable of sampling at 2kSps/ch. However, the data obtained at this frequency is corrupted by voltage spikes measured by the ADC inputs. A prototype was only developed consisting of just a few channels due to budget problems and time limitation, but the prototype was enough to validate the system specifications.

Before a fully functional design is created using the presented design concept, the hypothesis needs to be validated using existing equipment.

- If this hypothesis is validated to be correct, the most significant improvement would be to eliminate the voltage spike by replacing the isolation power source by a battery. Other improvements are to replace the AFE and ADC with the RITAN RH2164. This module is 64 monopolar ASIC which would cut the material price by more than a half and be just a fraction of the current size.
- If the hypothesis is validated to be incorrect, the design presented in this thesis could be used to design an MPR system. MPR systems use machine learning algorithms to recognise patterns of muscle activation enclosed in the EMG signals and to decode the hand gesture intention of the user, which is a much more intuitive method to control the prosthesis compared to DC.

Summary (Dutch)

Een myoelektrische protheses is een artificiële lidmaat, dat gebruikmaakt van elektromyografische signalen om zijn functies te besturen, dit kan een bionische hand, arm, knie of enkel zijn. Het EMG signaal wordt gerectificeerd, gladgestreken en een referentie waarde wordt ingesteld om de motor in de bionische hand de hand te doen openen of sluiten. Deze methode is ook wel bekend als directe controle "DC". De plaatsing van de EMG electroden in prothese begint met het plaatsen van test electroden over de agonist en antagonist van spierparen van de stomp. De plaats en de versterking van deze electroden wordt aangepast totdat er een individueel signaal boven de referentie waarde is verkregen aan iedere electrode bij het uitvoeren van verschillende handgebaren. Het probleem met deze methode is dat de plaats van de electoden in de prothese grotendeels gebaseerd is op experimentele basis, en de positie waarover de patiënt het meeste controle over zijn agonist en antagonist niet gevonden wordt. Dit resulteert dat er in de meeste gevallen de instellingen van het systeem aangepast moeten worden, zodat de patiënt optimale prestatie van de prothese ondervindt. Door het correct plaatsen van de electrode aan de hand van geavanceerde metingen kan dit probleem verminderd worden of helemaal verholpen worden. Dit heeft geleid tot de volgende hypothese: "The prestatie van direct controle kan verhoogd worden door het correct plaatsen van de electroden over de agonist en antagonist op de stomp waarde de patiënt het meeste controle over heeft tijdens het uitvoeren van verschillende handgebaren". Het doel van dit afstudeer verslag is op dit moment nog niet het beantwoorden van de hypothese, maar het ontwerpen van een systeem dat deze hypothese kan bevestigen en in wellicht de toekomst gebruikt kan worden in klinische omgeving om de positie van de electroden te verbeteren. Dit systeem moet het potentiaal verschil dat door alle spieren in de stomp gegenereerd wordt. De minimale eisen van dit systeem zijn: 64 monopolar kanalen, EMG bandbreedte van 10 - 500Hz en een sample frequentie van 2kSps/kanaal. Er zijn meerdere concepten in dit verslag ontworpen en getest op de volgende parameters: IRN, baseline ruis, CMRR, versterking en fase verschuiving. Dit heeft uiteindelijk geleid tot het volgende ontwerp: een IA met een 'quashi' hoog doorlaat filter om potentiaal verschillend tussen de electroden te doen verminderen, dit wordt gevolgd door een 2^{de} orde hoog doorlaat filter voor verdere onderdrukking van het potentiaal verschil, waarna een MFB differentiaal versterkende laag doorlaat filter is geplaatst. Een 24-bit 8 kanaal ADC was gekozen, met een 'daisy-chain' functie om een enkele data transmissie lijn te creëren tussen alle ADC en de micro-controller. De micro-controller verzond de data via USB 2.0 naar de PC waarop alle data wordt gevisualiseerd. In Tabel 9 zijn de systeem specificaties van huidige systeem samengevat.

	CMRR (dB)	IRN (μV_{rms})	Versterking (V/V)	EMG BW (Hz)	Baseline Ruis (mV_{rms}) SD - MP	Ingang impedantie	Sample frequentie Sps/kanaal	
Systeem specificaties	105	2,09	239	10- 2000Hz	3,1	29	100GΩ	250

Tabel 2 Systeem specificaties

Al hoewel de tabel specificert dat het systeem in staat is om een sample frequentie van 250Sps/kanaal te bereiken, is het systeem wel degelijk in staat om de gewenste sample frequentie van 2kSps/kanaal te bereiken. Echter op deze frequentie wordt verkregen data overrompeld door voltage pieken waardoor het gewenste signaal niet verkregen kan worden. Daarnaast is alleen een prototype ontwikkeld dat maar enkele kanalen heeft door tijdgebrek en financiële tekorten, maar dit was genoeg om de specificaties te bevestigen. Voordat een volwaardig ontwerp wordt gemaakt gebaseerd op het voorgestelde concept, is het noodzakelijk dat de hypothese van afstudeer allereerst bevestigd of ontkracht wordt met bestaande apparatuur.

- Mocht de hypothese bevestigd worden dan zijn de volgende systeem verbeteringen voorgesteld: eerst moet voltage pieken uit het signaal verwijderd worden zodat het systeem wel in staat is om de gewenste 2kSps/kanaal te behalen. Dit kan door de huidige isolatie transformator te veranderen door een batterij. Daarnaast kan een deel van het systeem vervangen worden door een de RITAN RH2164, dit zou de materiaal kosten halveren en het systeem oppervlakte wordt met meer dan 50% verminderd.

- Mocht de hypothese ontkrachting worden dan kan het systeem gebruikt worden om een myoelectrische patroon herkenningsysteem te ontwikkelen. Dit systeem gebruik machine learning algoritmes om patronen in de EMG signalen te herken, om zo op een veel intuïtieve methode om de bionische hand te besturen.

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1 Introduction

This project will be designed according to the V-model. This is a design method consisting of 7 design phases, 1 requirement, 2 architecture, 3 detailed design, 4 implementation, 5 unit-test, 6 integration and 7 requirement tests. Detailed information about every phase can be found in the method of approach (attachment A).

1.1 Ambition

Myoelectric prostheses are artificial limbs that use myoelectric signals to control its function, this could be a bionic hand, arm, knee or ankle. The most common application for a myoelectric prosthesis is lower arm prosthesis (bionic hands) in patients with a transradial amputation (congenital disability or as a result of a trauma). These individuals often retain much of the extrinsic musculature of the forearm that is typically used to control the hand and wrist. Flexors and extensors of the limb are used to generate independent electromyographic (EMG) signals to control the motors inside the hand. Each EMG signal is rectified, smoothed and a threshold value set to activate the motor in one or another direction to open or close the bionic hand. The speed of the motor can be proportionally controlled, by considering the amplitude of the EMG signal (the higher the amplitude, the faster the motor turns). This method is also known a direct control or 'DC'.

The placement of the EMG electrodes inside the prosthesis starts by placing the test electrodes over agonist/antagonist residual muscle pairs on the limb. Using an analysing tool the place of the electrodes and the gain is adjusted until an independent signal above the threshold value is acquired at each electrode during different hand gestures. The problem with this method is that the place of these EMG electrodes is based on a trial and error method and the optimal place where the patient has the most control over the agonist/antagonist may never even be found. This results that in most cases the electrodes settings in DC systems need to be adjusted while the prosthesis is being used by the patient to maintain high performance. By correctly placing the electrodes on the patient limb this problem should be minimized or even resolved. This can be transformed into the following hypothesis for this thesis "The performance of direct control can be improved by correctly locating the agonist/antagonist of the residual limb where the patient has the most amount of control over during different hand gestures".

This thesis intends to develop a system that can perform this task and can be accomplished by visualizing the electrical surface potential distribution (EMG) generated by all limb' muscles during different hand-gestures (also known as an HD-SEMG recording).

Different systems on the market exist that are already capable of obtaining HD-SEMG measurements. However, most of these systems are not portable, wireless, or use semi-adhesive electrode (can cause skin irritation). This thesis intends to tackle these issues in a new design. We do not intend to design a new method for measuring EMG signals but use existing designs to develop our own system. As this thesis forms the beginning of this project, this thesis will mainly focus on the design and development of the hardware for this system.

1.2 Document styles (better translation)

All references are included with the IEEE bibliography.

1.3 Overview

This thesis takes the reader along the design process of an HD-SEMG acquisition system developed at BIO-engineering in Wroclaw, Poland.

This thesis is divided into the following chapters:

- **Chapter one:** Introduction

In this chapter, the problem statement and goal of this thesis are explained.

- **Chapter two:** Definition

In this chapter, the idea is translated into system requirements. These requirements will be used to validate the performance at the end. Technical background information about EMG is presented. Research is conducted about alternative methods to measure human muscle activation without the use of electrodes.

- **Chapter three:** Architecture phase

In this chapter the idea concept is developed into system functions and units, further is described what specification these units will have and how these unit interact with each other.

- **Chapter four:** Design

In the chapter, the units and system functions are developed into hard/software designs. Simulations will be added to test the performance of the product.

- **Chapter five:** Implementation

In the chapter, the units and system functions are developed into hard/software is built. Thus PCB's are soldered and flowcharts are developed into code

- **Chapter Six:** Validation

In this chapter, the designed Hardware and software will be validated to see if matches the requirements set up in the first chapter.

- **Chapter Seven:** Conclusion

In this chapter, a conclusion of the overall design process is presented, and future improvements are suggested.

2 Introduction of Electromyography

Designing a system for the detection and analysis of EMG signals is impossible without a proper understanding of the physiology of an EMG signal. This chapter contains information about the structure of skeletal muscle, how the origin of SEMG signals and factors that affect SEMG recordings. A General setup of an SEMG acquisition system is presented further on in this chapter.

2.1 Electromyography

The cerebellum controls the muscular system of the body in the brain. A muscle contraction originates from the cerebellum where an impulse is sent (action potential), this action potential will travel thru the spinal cord, through a motor neuron where it will finally innervate the muscle fibre. A single motor neuron can innervate a couple of hundred muscle fibres in a small muscle (hand muscle) till a couple of thousand muscle fibres in a larger muscle. A single motor neuron and its branches are called a motor unit. Once the electric signal reaches the muscle fibre, the electrical signals are converted into a chemical signal which causes the muscle fibre to contract.

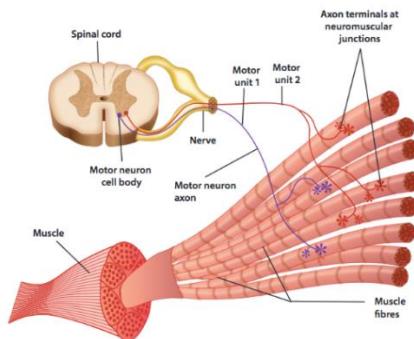


Figure 1 Motor unit [40]

A muscle fibre is made up out of many myofibrils. The myofibril contains contractile units called sarcomeres. The sarcomere is made up out of alternating thick and thin protein filaments. The thick filament is called myosin and is connected to the centre of the sarcomere (the M-line). The thin filament is made up out of the protein actin and is attached to the Z-line of the sarcomere. The myosin filament has a paddle-shaped structure, and these paddles connect to the actin filament creating a 'cross-bridge'. The myosin filament pulls the actin filament along its length using ADP and ATP. This causes the sarcomere to shorten thus contracting the muscle.

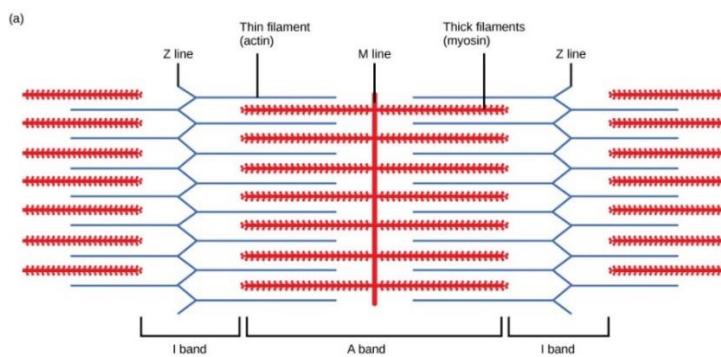


Figure 2 Muscle fibre [39]

A muscle fibre membrane has a resting potential of 70–90 mV, which is negative inside the cell in respect to the extracellular environment, is measured [1]. The maintenance of this potential is mediated by the sodium-potassium pump (NaK ATP-ase) working against the concentration gradients of ions flowing through the membrane [2]. The resting potential is generated by a higher concentration of Na^+ ions on the outside of the cell compared to the higher concentration of K^+ ions inside the cell.

When the action potential reaches the neuromuscular junction, a chemical (acetylcholine) is released in the synaptic cleft (the gap between muscle terminal synaptic and the muscle fibre membrane). Acetylcholine causes the muscle fibre membrane to become excited so that a potential gradient is locally generated in muscle fibre.

An inward current density (depolarisation zone) corresponds to this potential gradient. The depolarisation zone propagates along the muscle fibres from the neuromuscular junctions to the tendons' endings. This propagating intracellular action potential (IAP) causes an ionic transmembrane current profile also propagating along the sarcolemma [3].

The ionic transmembrane current (or external stimuli) cause the permeability of the cell membrane to change (see figure 3), allowing Na^+ ions to rush into the cell, making the inside of the cell more positive in charge (depolarisation phase). Incoming Na^+ ions cause K^+ ions to flow out of the cell, increasing the membrane potential towards the Na Nernst potential. A depolarisation potential of up to +20mV can be reached. Once the membrane has reached the Na Nernst potential the Na^+ channels are closed. However, the K^+ ions keep on flowing out of the cell (repolarisation phase). Finally, the sodium-potassium pump is activated, restoring a higher concentration of Na^+ ions on the outside of the cell compared to a higher concentration of K^+ ions on the inside of the cell (active transport of three Na^+ ions out and two K^+ in).

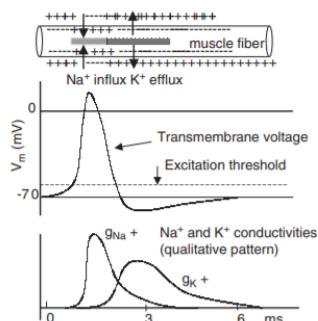


Figure 3 Ionic transfer of the cell membrane during contraction [6]

The electromyographic (EMG) signal is a representation of the electric potential field differences generated by the depolarization of the outer muscle fibre membrane (the sarcolemma). Surface electromyography is a summation of all the electric potential fields generated in the muscle fibre membranes superimposed on the skin.

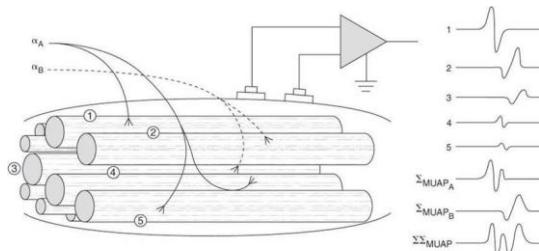


Figure 4 Motor unit action potential measured at the skin [38]

The amplitude of the EMG signal measured at the skin ranges from 0.1 - 2000 μ V [4]. For lean athletes, the amplitude could even be up to of 5mV [4]. EMG signals appear between 0 – 1000Hz [41]. The frequency range from 5 – 20 Hz does contain SEMG information, but it also contains information concerning the firing rate of motor units and movement artifacts (will be discussed later), which may not be of interest. About 95% of SEMG power density is accounted for by harmonics up to 400Hz. Thus the recommended EMG bandwidth is between the 10 – 500 Hz [4],[6],[7], [8], [9].

2.2 Construction of an electromyography acquisition system

Figure 5 shows the general block diagram of a single channel SEMG amplifier. The block diagram is based on [7]. However, it was simplified as certain design blocks were not necessary in this design (blank filter and slew-rate limiter). The system starts with electrodes measuring the EMG signal, afterwards the signal is amplified, filter and digitised using electronics components, finally the data will be visualized on the PC.

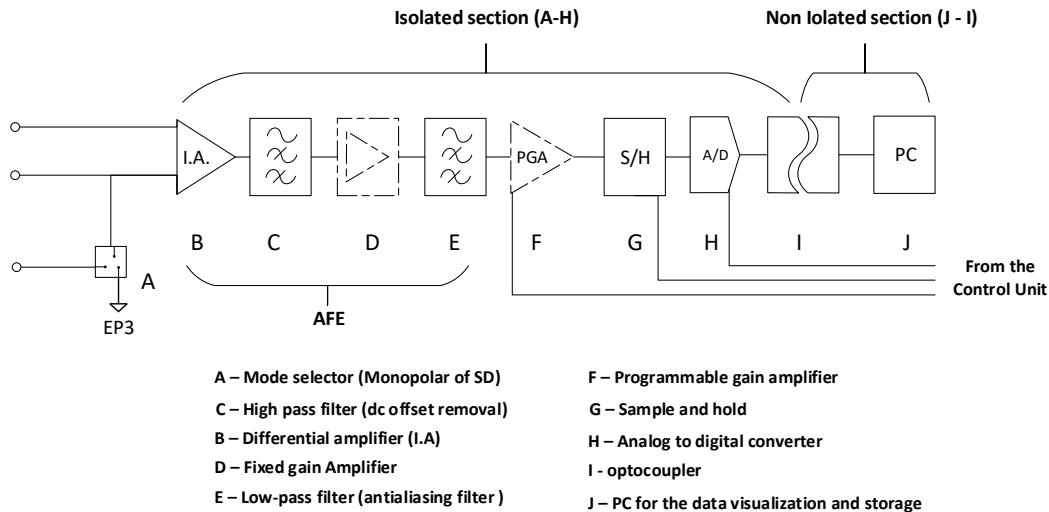


Figure 5 Block diagrams of a sing channel of a sEMG amplifier. The channel can detect EMG signals in monopolar and in single differential configuration. The dotted block D and F are optional blocks, however one of the two blocks is always required in the design.

2.2.1 Electrodes

2.2.1.1 Electrode Configuration

Electrode configuration for the detection of surface EMG refers to the number of electrodes used in the recording area and the arrangement of the electrodes [8]. The most common electrode configurations are the ‘monopolar’ and ‘bipolar’ configuration, see figure 6.

The monopolar configuration detects the electrode potential direct on the skin under electrode (e1) in respect to a second electrode placed at an electrical natural location (e2) (a bony place). The monopolar configuration assures that the actual surface potential underneath the electrode is measured, but it might also record other interferences, e.g. powerline interference or muscle crosstalk.

The single differential configuration (also known as bipolar configuration) detects the difference between 2 electrodes (e1 and e2) placed over the muscle, with respect to a third electrode place at an electrical neutral location (e3). Interferences that appeared on both inputs are greatly attenuated or even completely removed by the differential amplifier.

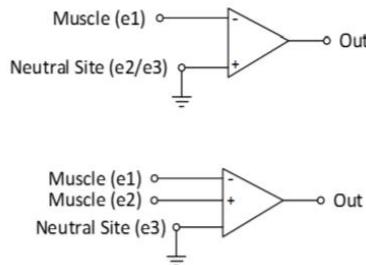


Figure 6 Monopolar (top) and single differential (bottom) configuration, [8].

A drawback of standard SEMG recording techniques (monopolar/bipolar) is the lack of spatial selectivity. This can be seen as the recording of the contribution of sources that are near or far from the electrodes, e.g. muscle crosstalk) and its sensibility to noise and common-mode signals (e.g. power line interference). In SEMG recording, this can be increased by applying a spatial filter to the recording channels. The most commonly used filters are Laplace filters, this is a class of high-pass spatial filter which approximate the second spatial derivative of the surface potential [8].

These spatial filters are applied by assigning weights to each monopolar recording channel. The simplest spatial filter is the double differential filter, consisting of 3 equally spaced electrodes, where the channels will have the respected weight of 1, -2 and 1 (Figure 7).

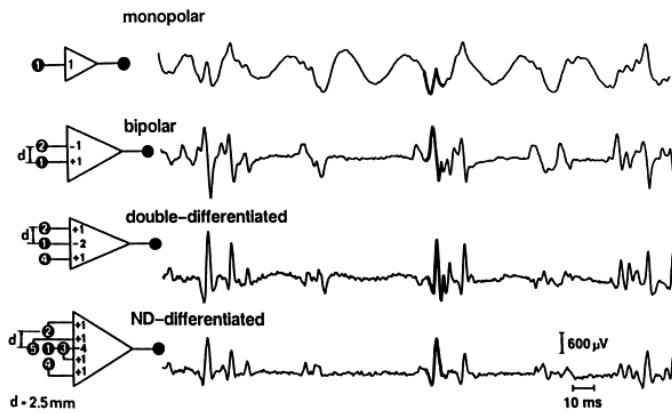


Figure 7 Spatial filter configurations, [9].

By adding more channels and assigning different weights to each channel, a higher spatial filter can be designed, such as the '**Normal Double Differential**' filter (NDD) and '**inverse binomial**' filter of the second-order (IB^2).

$$\begin{bmatrix} 1 & -1 \end{bmatrix}$$

Single differential

$$\begin{bmatrix} 1 & -2 & 1 \end{bmatrix}$$

Double differential

$$\begin{bmatrix} 0 & 1 & 0 \\ 1 & -4 & 1 \\ 0 & 1 & 0 \end{bmatrix}$$

NDD-filter

$$\begin{bmatrix} -1 & 2 & -1 \\ 2 & 12 & 2 \\ -1 & 2 & -1 \end{bmatrix}$$

IB² filter

Figure 8 Mathematical expression of the Laplace filters

2.2.2 System design block

This paragraph will describe the function of each design block presented in figure 5.

1) Analog front end (AFE)

The function of the AFE is to amplify and filter the measured raw SEMG signal. The AFE is comprised out of three parts: the differential amplifier (instrumentation amplifier), a dc offset suppression and a low-pass filter (antialiasing).

1.1) Differential amplifier (instrumentation amplifier)

The function of the differential amplifier (IA) is to amplify the difference between the two electrodes by a constant gain (common-differential signals) and provide the output as a single-ended signal referred to the reference. The differential amplifier will eliminate common-mode signals (e.g. powerline interference due to parasitic coupling of the body to mains and ground), see figure 9.

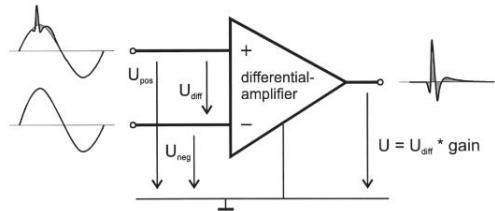


Figure 9 Differential amplification. The common-mode interference (50 Hz) is present at both inputs of the amplifier. By subtracting these signals, the noise is almost completely suppressed by the amplifier (principle of common-mode rejection. CMR). The signal of interest causes different potentials at the inputs and is therefore amplified, [41].

Strong rejection of the common-mode signal is one of the essential characteristics of a differential amplifier (IA). This phenomenon is known as common-mode rejection ratio (CMRR) and can be defined as the ratio of the differential gain over the common-mode gain. Ideally, the differential amplifier would have an infinite high CMRR. However, generally, differential amplifiers generally have a CMRR between the 90 – 120dB due to input impedances variations.

Part of the common-mode signal is converted into a differential signal, due to imbalances between the two input voltage dividers as a result of the differences between the electrode–skin impedances at the amplifier inputs (Fig. 10). The unbalance generates two different partitions of the common-mode voltage at the amplifier inputs. The resulting differential signal is amplified by the amplifier differential gain (A_d), is independent of the CMRR of the amplifier, and is usually the main source of power line interference. This mechanism is often called “the voltage divider effect” [7].

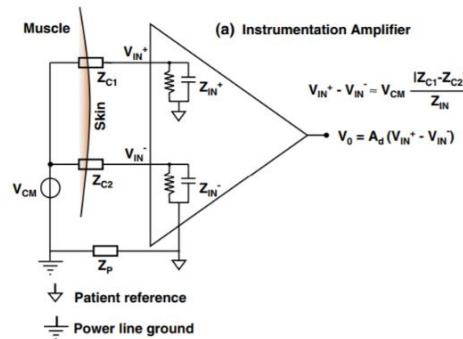


Figure 10 Voltage divider effect,[7]

The ‘voltage divider effect’ can be reduced by choosing a differential amplifier with an input impedance of at least 100 times greater than the maximum electrode impedance. As dry electrode can have an impedance of $1M\Omega$, the input impedance of the amplifier should be at least $100M\Omega$.

Equation (1) provides an estimate of the minimum CMRR required (2) to detect a superimposed common-mode voltage at the AFE less than 10% of the minimum EMG ac voltage [10].

$$\frac{|V_{ac50hz}|_{max}}{CMRR_{afe}} > \frac{1}{10} * |V_{ac_{emg}}|_{max} \quad (1)$$

Where $|V_{ac50hz}|_{max}$ is $0,5mV < |V_{ac50hz}|_{max} < 2,5mV$ [10]. The minimum amplitude of EMG is $10\mu V$ [4].

$$CMRR_{afe} = 10 * \left(\frac{|V_{ac_{50Hz}}|_{max}}{|V_{ac_{emg}}|_{max}} \right) = 10 * \frac{2,5 * 10^{-3}}{10 * 10^{-6}} = 70 dB \quad (2)$$

1.2) High-pass filter

The function of the high-pass filter is to suppress dc offset voltages (half-cell potential variations), motion (body and cable motions) and ECG artifacts, all these interferences appear below < 20Hz.

1.3) Low-pass filter (Bandwidth/Anti-aliasing)

The function of the low-pass filter is to set the EMG bandwidth and to prevent the ADC from aliasing. The Aliasing effect causes the discrete form of two different continuous signals which cannot be distinguished from each other. When this happens, the original signal is no longer constructible from its digital equivalent causing information losses and results in problems during the analysis of the signal [6]. Aliasing is caused by high-frequency signals, e.g. RF and EMI.

The most commonly used analog filters are the Chebyshev, Butterworth and the Bessel filter. Each filter type has its own characteristics, see figure 11.

- 1) The Chebyshev filter is designed to have a fast roll-off, by allowing a ripple in the frequency response. When the ripple amplitude is increased the roll-off of the filter becomes sharper. The ripple effect is an undesirable effect, thus a trade-off must be made between these two parameters to obtain the desired filter response. There are 2 types of Chebyshev filter, type 1: where the ripple is only allowed in the passband, type 2: where the ripple is only allowed in the stopband.
- 2) The Butterworth filters are designed to have a flat passband and with no ripple. The filter provides a smooth roll-off, with a roll off of rate 20dB/decade for every pole added to the filter.
- 3) The Bessel filter provides a flat response in both magnitude and phase and provides a nearly linear-phase response in the passband; however, this filter has the flattest roll-off.

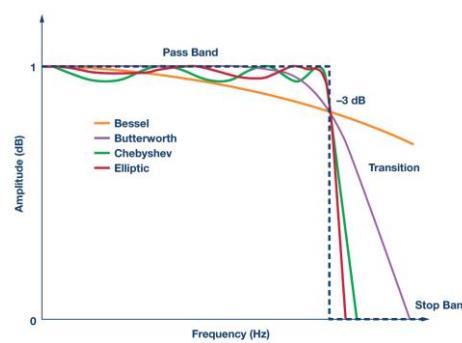


Figure 11 Filter types, [11]

2) Analog to digital converter

The conversion from an analog signal to a digital signal is performed by an analog-to-digital converter (ADC), this involves two processes, amplitude and time sampling. After the conversion the analog signal is only known in time instances equally spaced in time. The time between two samples is known as the sampling period T, and it is the inverse of the sampling frequency (1/T). To ensure no loss of the signal during the conversion, the signal must be sampled at least 2x the signals highest frequency (Nyquist theorem). Thus, for EMG system, the sampling frequency must be at least 1kHz (EMG bandwidth 10 – 500 Hz).

Signal quantisation is a process that codes the amplitude of the analog signal and is converted into a binary code (digital). Where each binary code corresponds to an analog voltage level. The number of voltage levels depends on the resolution of an ADC, this can be calculated using formula $2^n = \text{voltage levels}$, where n is the resolution of the ADC in bits.

When the number of channels increases, analog multiplexing techniques based on sample-and-hold (SH) or analog switches could be added to reduce the total number of ADC. Fast ADC devices are needed with multiplexing devices, such a SAR (successive approximation register) ADC, as the A/D conversion only takes a few microseconds. SH topology freeze all the input until all the channels are digitised, the inputs are frozen by storing the charge temporarily in a capacitor. Problems that could occur with these techniques are charge losses in SH devices, and voltage spikes could be introduced during switching.

To overcome the problems associated with multiplexing devices, multichannel simultaneous sampling ADC devices based on high-resolution sigma-delta modulators can be used [12]. The delta-sigma technique increases the digital resolution with respect to a SAR ADC (16 bits) up to 24 bits. This technique requires a noise shaping digital filter to produce the output digital word [12].

Sigma-Delta ADC implements an oversampling feature, the sampling frequency of the inputs signals is a clock multiple of the output frequency. This technique drastically reduces the quantisation noise within the baseband and maximises the real number of noise-free bits of resolution of the digitizing process [12].

3) Safety requirements

Generally, SEMG amplifiers are divided into two parts: 1) the isolated part, which is applied to the patient and 2) the non-isolated part, which is connected to devices that are powered through mains (e.g. computers, scopes, etc.). Isolation of the patient is required as leakage current of enough intensity through the cardiac region may cause ventricular fibrillation (IEC-60601). This norm states that the maximum current entering a person during a fault condition should be below 50 μ A.

An optical isolation barrier separates the two parts of the circuit with isolation up to 4–6 kV to satisfy the safety standards for medical equipment. The power supply and the analog and/or digital signals must cross the isolation barrier through special circuits to allow the amplifier to operate. Medical grade transformer-isolated power supplies, isolated dc/dc converters or batteries are used to provide power to the isolated part of the circuit [7]. Digitised signal interaction between the PC and the ADC are isolated using optocouplers (i.e. circuits based on a photo transmitter and a photoreceiver). The optocouplers allow signals to transfer in both directions of the isolation barrier.

4) Visualisation

After the EMG signals have been digitized and sent to the PC, the data usually will undergo further processing to extract information concerning the amplitude of the EMG signal, e.g. root mean square value (RMS) average rectified value (AVR), linear envelope (LE) and power spectral density (Fast Fourier transformation). Bio-potential signals appear on the surface of the body as distributions (images or maps) of electrical potentials. Muscle cells will generate electrical potential that results in surface EMG maps which can be detected with electrode grids applied above a muscle [1]. When a grid of electrodes is placed densely together, the representation is called a high-density surface EMG (HD-SEMG) or EMG imaging. The measured signal intensity under each electrode in a grid, where each electrode represents a pixel of an image, is represented by different colours to create an image based on the signal amplitude (see figure 12).

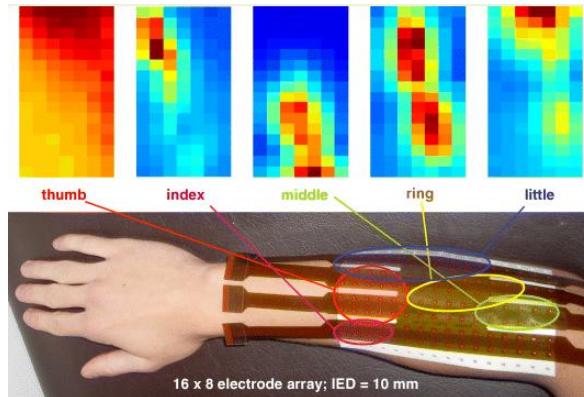


Figure 12. The electrode array of 8 columns x 16 rows with IED = 10 mm covering the dorsal side of a forearm. The five maps represent the spatial distribution of the RMS of 112 monopolar EMG signal (the most lateral column is not available) computed over a 1-s epoch during extension of each of the fingers [13].

2.3 Research

2.3.1 Introduction

The most common technique to measure human muscle activation is via electromyography (EMG), this is a process of recording the electric potentials generated by the muscles. Electromyography can be used by physical therapists to study biofeedback, functional anatomy of muscles, firing characteristics of motor units: and excitability of motoneurons. Electromyography can also be related to the amount of force developed by a muscle and the reflex connection of muscle [14]. Since the first EMG recording was performed in 1890, electronics have improved significantly in size and performance, this has resulted that electronic components in an EMG amplifier are not the dominant source of noise anymore. The electrode, which is the transducer of the EMG signal, is the most important source of noise in EMG recordings. Noise and other interferences measured by the electrodes could obscure the EMG signal, as they can be several magnitudes larger than the EMG signal itself. There are different methods to reduce these interferences and noises, a different solution would be to investigate whether it is possible to measure muscle activation without the use of electrodes. This resulted in the following research question: *Which alternative methods can be used to measure human muscle activation without the use of electrodes*. As the emphasis of this thesis is to develop a wireless and portable devices, this research will only consider technology that can fit this description.

2.3.2 Electrodes

Before alternative methods are presented, an understand must be obtained why electrodes detect and produce noise. This starts by learning more about the construction and physical characteristics of electrodes, followed by detailed information about the noise and interferences present in electrodes EMG recordings.

2.3.2.1 Construction of an electrode

The surface electrodes can be described as a transducer converting an ionic current of the body (charge) into an electric current flowing the electrode. The charge in the body is carried by ions, whereas in the electrodes, wires and rest of the electronics the charge is carried by electrons. In order to transfer the ionic current of the body into an electric current in the electrode and electrolyte is required in between of the electrode and the skin, this can be a body liquid containing ions (sweat) or an electrolyte solution (gel). For a charge to transfer from the electrolyte (ionic solution) to the electrode, a reaction of oxidation-reduction needs to occur.

There are two types of electrodes, invasive (needle) and non-invasive (surface). An invasive electrode can be used to analyse specific motor units of muscle fibres. Non-invasive electrodes (surface) measured the surface potential of the muscle. Surface electrodes can be classified into two sub-types: wet and dry electrodes.

- Dry electrodes exist in a pin or bar-shaped electrodes made of noble metals (e.g. gold, platinum or silver), carbon electrodes, and sintered silver or silver chloride electrodes [8].

- Wet electrodes consist of a dry electrode and an electrolyte gel to reduce the skin impedance and improve signal quality. The most popular wet electrodes are the disposable silver/silver-chloride (Ag/AgCl) which come in various sizes.

The disadvantage of a wet electrode is that it isn't possible to closely place the electrodes together, due to the relatively huge size of the disposable wet electrode. In long term biopotential monitoring wet electrode dry out, degrading the signal quality. Dry electrodes have a higher and more variable skin-electrode impedance. This causes more noise to be recorded. Typically, a wet electrode can have an impedance up to several hundred kΩ and dry electrode have an impedance up to several MΩ.

When a metal (electrode) is placed in an electrolyte solution, a layer of charge forms around the metal object in the solution. As the charge neutrality differs in the region near the electrode from the rest of the electrolyte solution, a potential difference is created also known as the *half-cell potential* (electrode polarisation potential). The *half-cell potential* can vary between different metals. Thus the same metal must be used between the recording electrodes, as the charge layer on both electrodes will cancel each other. Movement of the electrode may change the electrolyte concentration locally and thereby create changes in the half-cell potential for a short time until the concentration has re-established. The variations in half-cell potential causes baseline shifts, if the baseline shift is too large between the electrodes it can cause the amplifier to saturate.

The half-cell potential is persevered when no electric current flows between an electrode and the solution of its ions. The difference between the potential at zero current and the measured potentials while current is passing is known as the overvoltage and is the result of an alteration in the charge distribution in the solution in contact with the electrodes or the ion-selective membrane [5]. This effect is known as electrode polarisation and can diminish the electrode performance. Perfectly polarizable electrodes pass a current between the electrode and the electrolytic solution by changing the charge distribution within the solution near the electrode [5]. Nonpolarized electrodes, allow the current to pass freely across the electrode-electrolyte interface without changing the charge distribution in the electrolytic solution adjacent to the electrode. These types of electrodes can be described theoretically, but neither of the two can be fabricated in practice, it is always a close approximation to their characteristics. Silver -Silver chloride electrodes show characteristics similar to a perfectly nonpolarizable electrode, whereas other noble materials as platinum are often highly polarizable.

Figure 5 shows the equivalent model of an electrode (electrode-skin impedance). R_d and C_d represent the impedance of the electrode-electrolyte interface and the polarisation effect, R_s is the resistance of associated with the type of electrode material and the series resistance associated with the interfacial effects. E_{ch} is the half-cell potential of the electrode material used.

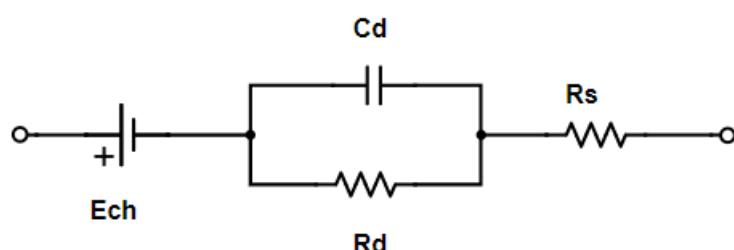


Figure 13 Biopotential electrode (electrode skin interface)

The total impedance of an electrode is frequency dependant, at low frequencies R_s and R_d are dominant and at high frequencies, C_d bypasses the effect of R_d , so that the impedance is close to R_s . The impedance is dependent on the electrode size and shape and the electrode material. High electrode-skin impedance can lead to reduced signal amplitude, waveform distortion and powerline interference in the recorded EMG [5]. A big contributor to a high electrode skin impedance is the high impedance of the epidermal layer (outer layer of the

skin, e.g. dead skin cells, oils, etc.). Different methods are described in [8] to lower the skin impedance by preparing the skin before placement of the electrodes.

2.3.2.1.1 Noise and interferences in electrodes

The fundamental property of a resistor is the generation of a certain amount of thermal noise (Johnson noise) and is caused by the random thermal agitation of charged particles. Generally, the movement of the particles will cancel each other at equilibrium. However, always a certain imbalance remains, causing random noise voltages. As the electrode and the skin contains resistive components (see model above) thermal noise will be generated.

There are three types of motion artifacts: physical displacement of the electrode across the skin, change in skin characteristics due to deformation, and motion of the cable. The first motion artifact is due to the change in the ionic charge layer between the electrode and the skin [15]. The second motion artifact is a result of the change in the geometry in the underlying skin. The ionic potentials and the resistive and capacitive properties of the skin change as the skin deforms in response to the muscle contraction. The last motion artifact produced by the cables used to connect the electrodes to an external system. Movements of the cables through an electric/magnetic field can introduce current in the wire. To minimize the effects of motion artifact proper skin preparation through skin cleaning and abrasion is advised by SENIAM and the use of gel electrodes is suggested which dampens the motion between the electrode and the skin [15].

Powerline interference (and its harmonics) are the largest source of interference in EMG recording. Any subject is coupled to the AC power mains and ground thru parasitic capacitance (50Hz in Europe and 60 Hz in North America). This effect can be reduced by choosing a differential amplifier (IA) with a high input impedance and high common-mode rejection ratio (CMRR).

Other sources of noise are skin thickness, muscle crosstalk and the body itself. The thickness of subcutaneous fat and tissue directly affects EMG amplitude, where increasing thickness results in a decreasing amplitude [16]. Muscle crosstalk refers to the signal that is detected by an electrode over a specific muscle but is generated by another mostly nearby muscle. The human body can also be a source of noise, as the biopotential signal can originate from various sources (muscle EMG, heart EKG and brain ECG) it is crucial to classify which signal is of interest and which are noise.

2.3.3 Alternative methods

Ultrasound imaging uses soundwaves to produce pictures of the inside of the body. It is only possible to measure soft human tissue using ultrasound, e.g. muscles, swellings, infection of the body and to examine a baby in a pregnant woman. Ultrasound scanner consists of three parts, 1) a video display, 2) a computer console and 3) a transducer. An ultrasound transducer consists of a large array of piezoelectric crystals when a voltage is applied to these crystals a high-frequency sound pressure waves are generated, also known as ultrasound waves. These ultrasound waves will reflect at tissue interfaces, these echoes are measured by piezoelectric crystals and contain information about the tissue (distance, size or type of tissue) and can be used to analyse the characteristics of the muscle. Typically, HMI applications using ultrasound, muscle thickness (cross-sectional area, CSA) and direction of muscle movements are obtained and interpreted using image processing. As ultrasound waves can detect much deeper muscles (surface electrode only detect muscle close to the surface), it becomes possible to identify deep arm muscles associated with complex finger movement. However, the link between ultrasound measures of muscle thickening and EMG measures of activation is not clear [17]. This technique allowed a musician to play the piano with this myoelectric prosthesis, whereas this wasn't possible with surface EMG as it couldn't precisely control the individual fingers needed to play piano [18]. There are some concerns using ultrasound to measure muscle activity, mostly associated with long term monitoring. Although it is based on non-ionizing radiation, so it does not have the same health risks as X-rays or other types of body imaging systems that use ionizing radiation. As ultrasound wave contain energy, it can heat the tissue slightly, producing small pockets of gas in body fluids or tissues. The long-term consequences of these effects are still unknown [19].

After extensive literature research, ultrasound was found to be the only reported alternative to measure muscle activation without the use of electrodes. There are some alternative EMG measuring concepts published, that improve some of the problems related to noise, compared to the general setup of using electrodes and potential amplifiers. This concept uses a current amplifier and prevents the potential of building up and thus suppresses lateral current causing interelectrode crosstalk. With the proposed current amplifier one has a new tool that allows to significantly improve the spatial resolution of arrays of electrodes [20].

2.3.4 Conclusion

One major problem with the measurement of muscle activation with EMG and electrodes is the recorded noise and interferences by the electrodes can obscure the EMG data. This research only found one other viable option to measure human muscle activation without the use of electrodes to be ultrasound. As much as ultrasound can measure deep muscles that are correlated with complex body movements, there is very little evidence on how the CSA of the muscle associated is with muscle activation. Thus the only viable option to measure human muscle activation remains with EMG and electrodes. Interferences and noise recorded by electrodes can be minimized by properly cleaning the skin before use and using high-performance electronic components.

3 Definition phase

3.1.1 System Context

Figure 10 shows the context of the system. This context diagram explains the function of all inputs and outputs of the system and how they relate to the users of the system. The system will interact with three different terminators, the prosthetist/operator (who produces the prosthesis), the patient and the manufacturer.

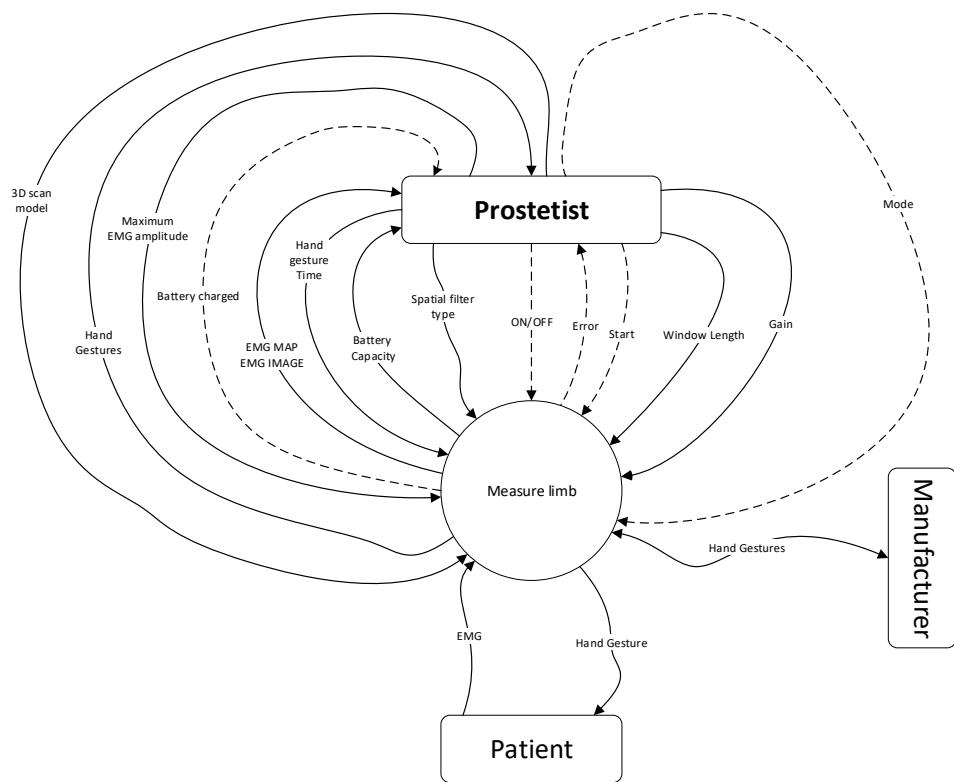


Figure 14 Data context diagram

The process starts with the prosthetist making a 3D-model of the patients' limb using a 3D scanner, the model will be uploaded to the system. On the 3D-model the system will eventually visualise the measured muscle potential distribution of the patient' limb during different hand-gestures (flow 'EMG MAP'), the result should look similar to figure 8. Different colours represent the amount of muscle activity, e.g. green is no muscle activity, and red is the maximum muscle activity. The colour range between 'no muscle activity' and 'maximum muscle activity' is set by the prosthetist, and can be set from 50mV until 1V (the flow 'Maximum muscle activity'). The prosthetist will use the 3D-model combined with the measured 'EMG MAP' data to mark the exact location for the EMG electrode. Once the location(s) for the electrode(s) are marked the prosthetist will use CAD/CAM software to finalise the prosthesis socket for the patient.

After the system recorded the raw EMG signals, the data is further processed. The prosthetist is able to add more gain to the signal as each person differs in the amount of muscle activity they can generate (flow 'Gain', selectable gain are 1,2, 3 or 4) and spatial filters can be added to enhance the SEMG signal source.

After the data has been processed the amplitude of the muscle activity is calculated (e.g. Root-Mean-Square) over a specific amount of time (flow 'window length'). The duration of the 'window length' can be adjusted by the prosthetist, and can vary between the 0,1 and the 3,0 seconds. Finally, the data of all the recording electrode are combined to create the EMG MAP to be visualised around the 3D model.

The prosthodontist can select between two different modes: when the flow 'Mode' is 'HIGH' then 'Automatic mode' is enabled, otherwise 'Free-mode' is enabled. These two modes mainly differ in how the data is presented to the prosthodontist. The system will start one of these modes after the 'start' command has been activated through the application, and by default 'Free-mode' is selected.

- In 'Automatic mode' the system tells the patient to perform different hand gestures. These hand gestures are entered into the system by the manufacturer, and they are the 6 most common hand gestures performed by a person. The prosthodontist can enter into the system how long each hand gesture needs to be held by the patient, this varies from 1 sec until 10 sec (flow 'Hand gesture Time'). Once the patient performs all the hand gestures, the prosthodontist will receive the measured data (flow 'EMG MAP'). The data will be presented to the prosthodontist as a single image per hand gesture on the 3D model, containing the averaged muscle activity during the specific performed hand gestures. These images can be placed above each other to locate the exact location for the electrodes.
- In 'Free-mode' the measured data is shown in real-time on the 3D model to the prosthodontist.

The primary power source of the system will be a battery, to make the system wireless and isolated from mains for patient protection. The battery's capacity is continuously monitored and updated by the system. The current battery capacity will be displayed on the device itself (only when it is turned ON) and via the PC application to the prosthodontist. An error notification (flow 'error') will be sent to the prosthodontist to recharge the system if the battery capacity drops below the 10%, it will not be possible to start a new conversion if the battery capacity is below the 10%. The system will have an indicator light to inform the user that the system is fully charged.

3.1.2 Specification of requirements (SoR)

The system context provided by the client was converted into the following system requirements. As mentioned in the introduction, this thesis will mainly focus on the design of the hardware for this system. Thus the requirements were divided into two groups: hardware (HD-SEMG acquisition system) and software (user interface). In attachment B the acceptance test was added, this document describes how these system requirements need to be tested to verify the system performance (the interface requirements will not be described or tested). *The following listed requirements were partially based on [7], where general requirements/specifications of a HD-SEMG system are presented..*

3.1.2.1 HD-SEMG acquisition system

- REQA-01:** Minimum CMMR > 70 dB within the EMG bandwidth, see chapter 2.
- REQA-02:** Sampling rate 2kS/s/ch. As EMG signals can have a frequency up to 500Hz, the minimum sample frequency needs to be 1000Hz (Nyquist Theorem). However, the sampling frequency was set to 2000Hz, to ensure higher data resolution for signal processing.
- REQA-03:** Input referred noise (IRN) < 4 μ Vrms [23,24,25,26]. This is Intrinsic noise that is generated inside the electronics itself, e.g. transistor flickering and quantisation noise of the ADC, this noise cannot be eliminated.
- REQA-04:** Dynamic input range of EMG signal with an amplitude up to 5mV, this is the maximum EMG amplitude generated by lean athletes.
- REQA-05:** Minimum operating time of the device is 2-hours on one battery cycle.
- REQA-06:** Minimum wireless data transportation range of 2m, from the device to the PC.
- REQA-07:** Indication that the battery is fully charged.
- REQA-08:** Low gain mismatch among channels (<0,5%).

3.1.2.2 User interface

- REQB-01:** Muscle activity is shown using a colour bar, where green is no activity and red is a lot of activity. The range of the colour spectrum can be set manually.
- REQB-02:** Battery capacity is displayed in %
- REQB-03:** Notification is sent to the user when battery capacity is <10% and new measurement session cannot be started if the battery capacity is below 10%.
- REQB-04:** Different spatial filter can be selected: LSD, LDD, NDD and IB2.
- REQB-05:** Window length can be selected between 0.1 and 3 seconds.
- REQB-06:** Maximum EMG amplitude can be selected between the 10mV and the 1000mV. Both values were determined by multiplying the G_{AFE} (this value is explained in chapter 4) with the minimum and maximum EMG amplitudes, and taking the RMS of these values.
- REQB-07:** Additional gain can be selected, ranging from 1-4x (in steps of 1).

3.1.2.3 Non-functional requirements

- REQC-01:** Material costs of maximum €1000
- REQC-02:** Maximum device dimensions are 15x10x4 cm.
- REQC-03:** Maximum allowed weight is 200 gram, this is without the electrode grid.
- REQC-04:** EMG electrode size < 10mm diameter.
- REQC-05:** Inter electrode distance (IED) < 10 mm.
- REQC-06:** 64 EMG channel, this amount of channels was based on the sleeve used in [22].
- REQC-07:** Electrode configuration needs to be in monopolar, as monopolar configuration assures that the actual surface potential underneath the electrode is measured.

3.1.2.4 Scope of the project

If project budget or project duration don't allow the student to develop a fully functional prototype during the internship, the student is not obligated to test the non-functional requirement that cannot be tested without a fully functional system e.g. REQC-02, REQC-03, REQC-04, REQC-05 and REQC-06. As these requirements do not

provide any further evidence about the performance of the system. The same problem account for REQA-08, this requirement can only be tested if a prototype with multiple channels is developed.

3.1.3 Data flow diagram

The data context diagram was divided into 5 sub-systems.

The function of the sub-system are:

- 1) Mange system, this block will check if different system parameters are valid to start a new measurement session, e.g. the battery needs to be above a certain level.
- 2) Check battery level, this block will measure the batteries capacity and tell management system unit when the battery is running low.
- 3) Measure EMG, the block will amplify, filter and digitise the EMG signal.
- 4) the block will post-process the digitized data.
- 5) this block will show the patient which hand movement the user needs to make and how long he needs to hold them for.

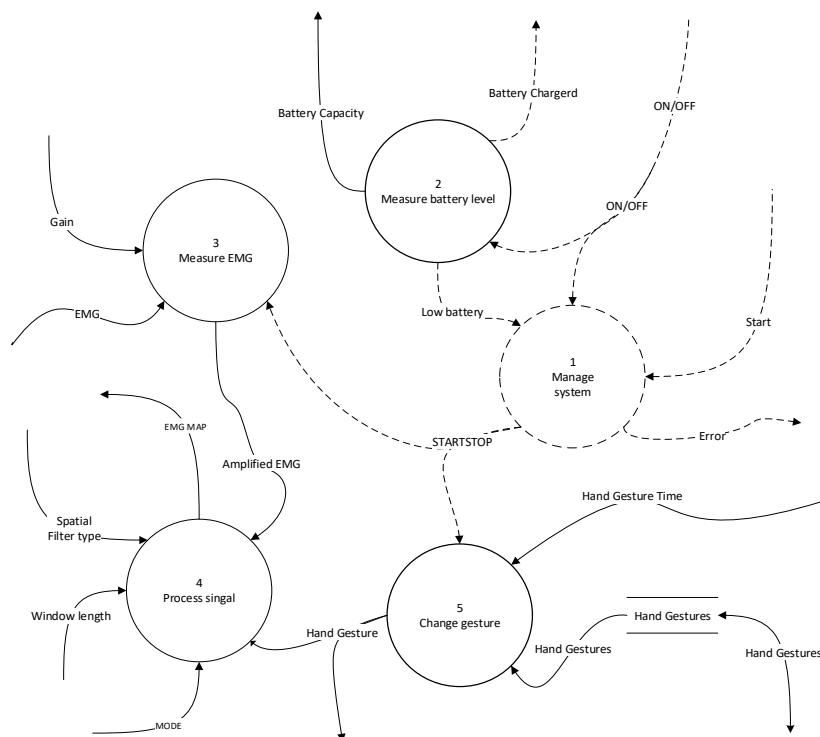


Figure 15 Data flow diagram Level 0

In Attachment D the units of the Data flow diagram are further designed into smaller sub-units. As both unit 4 & 5 are software implementations these will not be any further addressed in this thesis.

4 Design Phase

In this chapter, the unit from the data flow diagram will be designed into functional design block. Components will be selected which can implement the function in each design block.

4.1 Measure battery level

The function of the unit 'measure battery level' is to monitor the current battery level and to provide the rest of the circuit with an isolated power supply. Unfortunately, this unit had to be eliminated from the current design, as the device could not be made wireless due to the bandwidth limitation of the Bluetooth transceiver module (see chapter 4.3 for further details). However, this module was developed entirely before the

knowledge that the unit had to be eliminated. To prevent further confusion whilst reading this thesis the detailed design of this unit is fully described in attachment B.

4.2 Measure EMG

The function of unit ‘Measure EMG’ is to amplify, filter and digitise the EMG signal for further processing in the next unit (‘process signal’). The unit ‘Measure EMG’ can be designed using the following design blocks, see figure 16 (based on figure 5 in chapter 2). After the data is collected by the unit, the data is sent to a PC to be verified and to analyse if the measured data is correct (this part is different from the unit ‘process signal’, but it implies certain feature of the unit that are used in that unit).

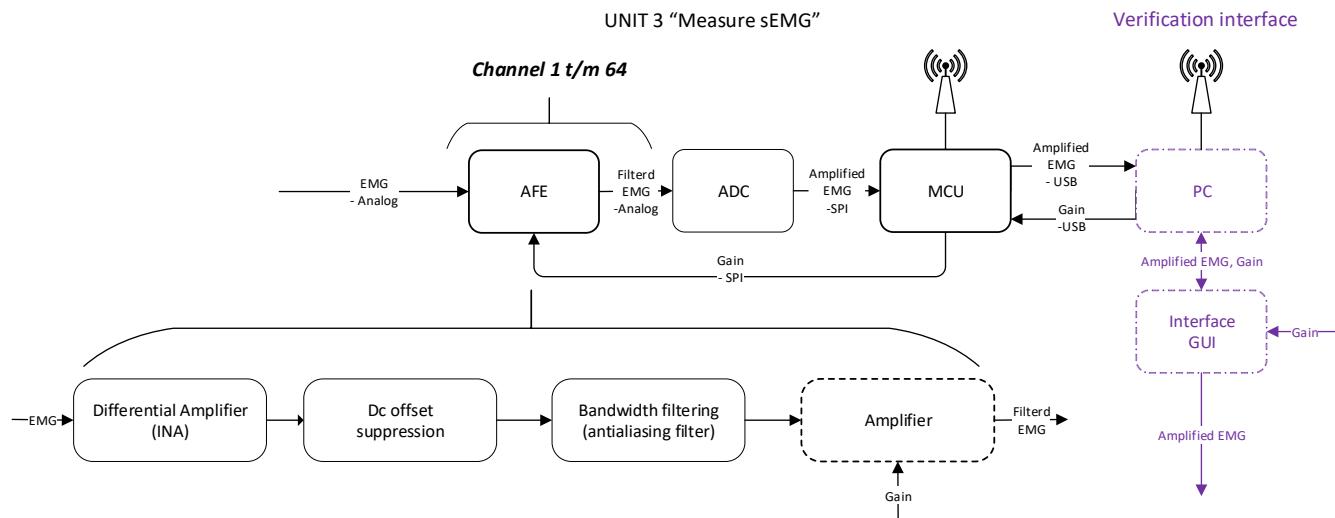


Figure 16 Design block diagram of unit ‘Measure EMG’

The AFE must be designed to have the following specifications:

1) Full Scale Range (FSR)

The FSR of the AFE module was set to 5V.

PSPEC1: FRS is 5V.

2) Gain AFE

As mentioned in Chapter 2, EMG signals generally have an amplitude between 0.1uV and 2000uV [1]. The maximum gain of the AFE was calculated in (3). The AFE voltage limit was set to 90% of the FSR.

$$G_{AFE\ max} = \frac{V_{AFE\ out\ max}}{|V_{AC\ EMG}|_{max}} = \frac{0.9 * 5V}{4mVpp} = 1125\ V/V \quad (2)$$

The amplifying module will add a signal gain of 1 - 4 V/V (REQA-3). The nominal AFE gain was set in (3).

$$G_{AFE\ nominal} = \frac{G_{AFE\ max}}{Amplifier\ (PGA)_{max\ gain}} = \frac{1125}{4} \approx 250\ V/V \quad (3)$$

PSPEC2: $G_{AFE\ EMG\ BW} = 250\ V/V$

3) Amplification

A variable signal gain of 1-4 V/V, this gain will be multiplied by the $G_{AFE\ nominal}$.

PSPEC3: Variable gain 1-4x.

4) EMG bandwidth

The EMG bandwidth was set from 10 Hz – 500 Hz. Based on the SENIAM recommendations the EMG bandwidth is between the 10 – 500 Hz.

PSPEC4: AFE_{BW} 10 – 500Hz.

A full description of how these specifications are tested is described in the unit test document (part of the test document), see attachment C.

The AFE design block can be designed using discrete components or with application-specific integrated circuits (ASIC). The advantage of these ASIC is that they provide an excellent performance level in terms of size and power consumption. On the contrary, the analog characteristics (e.g., CMRR, input impedance, gain accuracy, noise floor) delineate a quality level equal to the medium level of EMG amplifier based on discrete component implementations [7]. As this project strives to achieve the highest-level EMG amplifier (AFE), the choice was made to design an AFE based on discrete components rather than to use an ASIC.

In this chapter, multiple AFE design will be presented. To conclude which AFE design will be used in the final design, all the different AFE designs will be evaluated on CMRR, input-referred noise (IRN), group delay, power consumption, size and price. The evaluation process and the result will be discussed in chapter 7. To minimise differences between the different designs, all the capacitors in the filtering stages be an X7R-series (5%) and the resistors must have a tolerance of 0,1%.

The design of our AFE is based on the following reports, see table 2. The following reports were selected as they provide detailed information about both the system design and validation.

Biopotential amplifier solutions overview

Feature	Method or technique	Details	Reference
Multi-channel system		16 channels (using the ADS1298), CMRR 100dB, fixed gain 50V/V with additional gain (1,2,3,4,5,6,8,12), EMG BW 20 – 1800Hz	[36]
		EMG BW 8 – 1kHz, 8 channels, RLD and isolation	[37]
High density system	Monopolar	Dual voltage supply, supply, Bandwidth: 5-1Khz, gain 500x, 11 electrodes, Laplace filter	[28]
		Dual voltage supply, Analog isolation, Bandwidth: 15 - 1800 Hz, Fixed gain 20x, selectable gain of 1x,2x,4x,8x,16x,31x,64x, CMRR 100 dB and an input range of 0 – 30 mV	[21]
	Versatile system (Monopolar and Bipolar)	A modular MP/SD HD-EMG system. Dual supply (battery), BW 30 – 500Hz, Gain 192 V/V, 64 – 424 electrodes, CMRR 95 dB and a sampling frequency of 2,4kSps.	[10]

Table 3 Research summary about HD-SEMG

The literature about the design of a single channel EMG system is extensively reported, but there are just a few reports written about the design of HD-SEMG systems or multichannel EMG systems (with detailed description about the verification of the parameters of the system, e.g. CMRR, IRN, etc.). The design of a single channel

EMG system can be used to design an HD-SEMG system, but this could cause different problems as the requirements for a single channel EMG amplifier are very different from a HD-SEMG system.

4.2.1 AFE

4.2.1.1 Design 1

Design 1 is based on the AD8232, this is an integrated signal conditioning block for ECG or other biopotential signals [1]. This signal conditioning block comes with a built-in instrumentation amplifier (fixed gain of 100), an op-amp for signal filtering and a reference voltage buffer.

The AD8232 also has some extra functionalities such as a leadoff detection, driven-right leg (common-mode noise reduction) and power-down mode. The module is available in 4mmx4mm (LSCSP) and in a smaller version, the AD8233 with a size of only 2mmx2mm (WLCSP). The AD8232 offers a CMRR of 105 dB at 50 Hz without any dc-offset, and the CMRR is reduced to 80 dB at 50 Hz with a dc-offset of +/- 300mV. The downside of this component is the low dynamic input range as the power supply is limited to +3,5V. The input impedance of the AD8232 is $10 \parallel 7,5 \text{ [G}\Omega\text{] } \parallel \text{ pF}$.

4.2.1.1.1 DC-offset

The AD8232 offers a built-in integrator to suppress dc offset (more information about the integrator is explained in chapter 5.1.3.1.3.1). The datasheets of the AD8232 suggest multiple topologies to suppress the dc offset. Additional RC networks can be placed after the integrator to improve dc offset suppression. The different filter topologies are shown in figure 17.

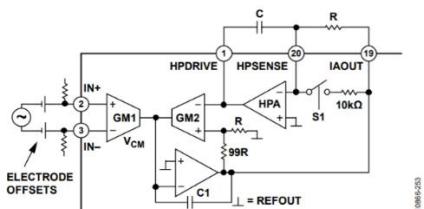


Figure 17.1 Integrator filter, [27]

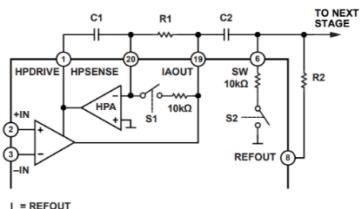


Figure 17.2 the integrator filter and high pass filter, [27]

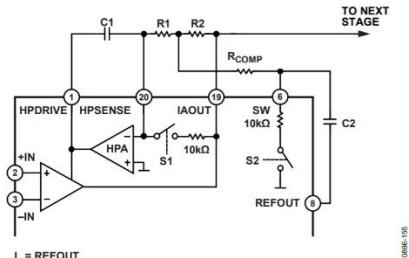


Figure 17.3 Integrator filter and alternative topology for the high pass filter. The alternative topology allows lower cut-off frequency with lower R and C values, [27]

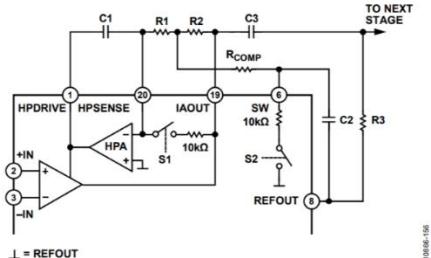


Figure 17.4 Integrator filter and a 2-pole high-pass filter, [27]

The characteristics of each filter are summarised in figure 18.

Table 4. Comparison of High-Pass Filtering Options

	Filter Order	Component Count	Low Frequency Rejection	Capacitor Sizes/Values	Signal Distortion ¹	Output Impedance ²
Figure 53	1	2	Good	Large	Low	Low
Figure 55	2	4	Better	Large	Medium	Higher
Figure 56	2	5	Better	Smaller	Medium	Low
Figure 57	3	7	Best	Smaller	Highest	Higher

¹ For equivalent corner frequency location.

² Output impedance refers to the drive capability of the high-pass filter before the low-pass filter. Low output impedance is desirable to allow flexibility in the selection of values for a low-pass filter, as explained in the Low-Pass Filtering and Gain section.

Filter topology two was chosen as this topology offers a high output impedance and lower signal distortion compared to the other filter topologies. The cut-off frequency of the integrator is calculated in (4).

$$F_c = \frac{100}{2 * \pi * \sqrt{R_1 C_1}} \quad (4)$$

$$R_1 = \frac{100}{2 * \pi * F_c * C_1} \gg \frac{100}{2 * \pi * 10 * 4700n} = 340k\Omega$$

In (3) the cut-off frequency is 100 greater than in a normal one-pole filter equation, this is due to the gain of the instrumentation amplifier. The second high-pass filter (cut-off frequency of 5Hz) is calculated in (5). Due to impedance loading between the filters, which will increase the lower EMG BW, the second high pass filter was set to 5 Hz to ensure the low-cut-off frequency.

$$R_2 = \frac{1}{2 * \pi * F_c * C_1} \gg \frac{1}{2\pi * 5 * 4700nF} = 3.4 k\Omega \quad (5)$$

4.2.1.1.2 Low-pass filter

Design one will use the Butterworth low-pass filter, as this filter type offers the most flat passband with the best filter roll-off. The Butterworth filter will be designed on top of the Sallen-key circuit configuration (figure 19).

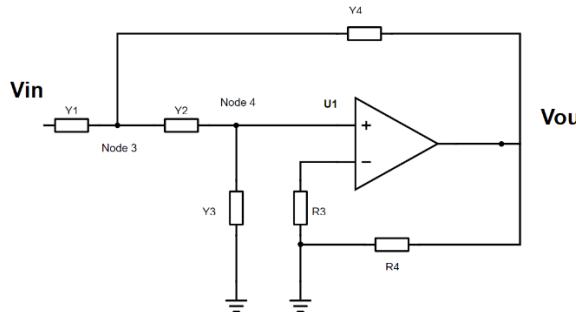


Figure 19 Sallen-Key filter, Y1-Y4 are admittances to set the desired filter type (high/-low-pass) and R3,R4 are used to set the gain of the filter.

The following two formulas (3) are required to calculate a Sallen-key topology Butterworth low-pass filter (the derivation of these formulas from figure 16 is extensively described in [30]). In this formula R1, R2 and C1, C2 can be expressed in a ratio of m and n of each other, K is the gain of the amplifier.

$$F_c = \frac{1}{2 * \pi * R * C * \sqrt{mn}} \text{ and } Q = \frac{\sqrt{mn}}{m + 1 + mn(1 - K)} \quad (6)$$

The design of the filter starts by setting the desired value for Q and K (gain), followed by giving either m or n a value and calculating the other one. After values for Q, m, n and Fc are obtained, values for R and C can be calculated.

A gain of 2.5x is needed to obtain the G_{AFE} of 250 V/V, thus $K = 2.5x$. The following values for Fc, A, Q and n were chosen to determine m (7).

$$F_c = 500 \text{ Hz}, \quad Q = \frac{1}{2}\sqrt{2}, \quad K = 2.5, \quad n = 1, \quad m = ? \quad (7)$$

$$Q = \frac{\sqrt{mn}}{m + 1 + mn(1 - K)} = \frac{\sqrt{m}}{m + 1 + m(1 - K)} = \frac{1}{2}\sqrt{2} \Rightarrow m = 0.3647$$

To calculate R (in eq. 8) a value for C of $1nF$ was chosen. The formula is changed to obtain R instead of F_c .

$$(8) \quad R = \frac{1}{2 * \pi * F_c * C * \sqrt{mn}} = \frac{1}{2\pi * 500Hz * 1nF * \sqrt{0.3647}} = 524k$$

$$RR2 = R \gg 524k\Omega, \quad R1 = mR2 = 185k = 164k\Omega$$

The last step is to convert these values into values within the E-24 series, thus $R2 = 180 k\Omega$ and $R1 = 510k\Omega$.

Design two can be summarised using the following design blocks, see figure 20.

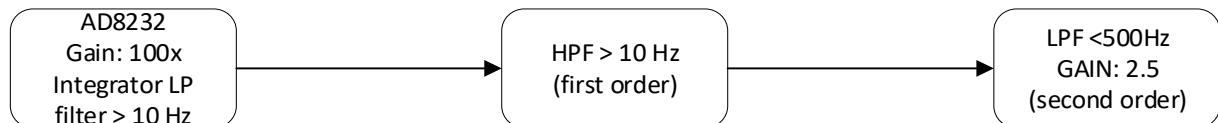


Figure 20 Building block design 1

The AD8232 circuit was analysed using the AD8232 filter design tool of ANALOG DEVICES. The results of this simulation is shown in figure 21. The lower cut-off frequency is located at 9,96 Hz and the upper cut-off frequency is located at 525 Hz using our calculated values.

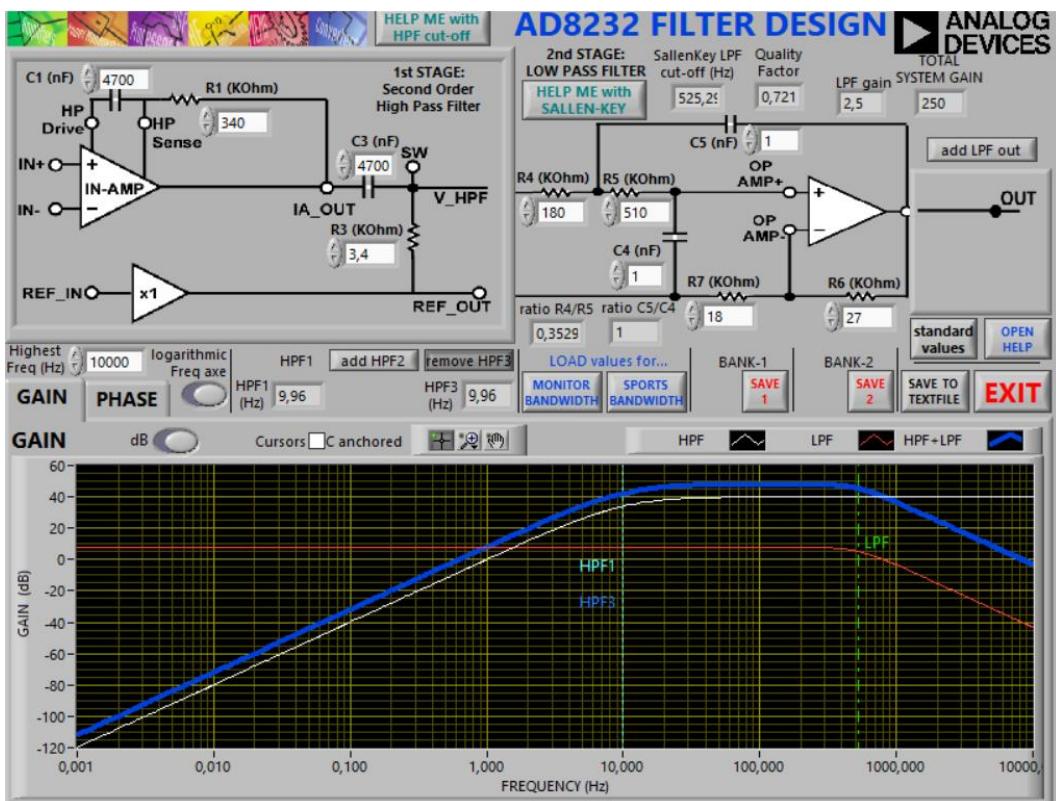


Figure 21 Results AD8232 filter design tool

4.2.1.1.3 Right leg drive (RLD)

The AD8232 offers a right leg drive (RLD) amplifier (figure 22), which will invert the common-mode signal that is present at the IA inputs. The right-leg drive output voltage is injected into the patient, this counteracts with common-mode voltage variations, thus improves the common-mode rejection of the system. The selected capacitor was 1nF (see datasheet AD8232 for detailed explanation).

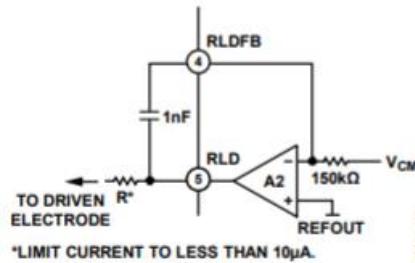


Figure 22 Right leg drive (RLD) AD8232 [27].

To prevent dangerous currents from entering the patient body (IEC-60601), a series resistor must be connected to the output of the RLD to limit the < 50µA in a fault condition. The minimum resistor is calculated in (9) for a maximum current of 10µA.

$$I_{leak} = \frac{V_{cc}}{R} \gg \frac{3,5V}{10\mu A} = 350k\Omega \text{ (min)} \quad (9)$$

R was set to 390kΩ to ensure optimal safety.

To protect the patient against leakage current entering the body during a fault condition (IEC-61006), a resistor needs to be added in front of the IA inputs. The datasheet suggests that each input needs to be equipped with a 180k resistor for protection, that limits the maximum current in a fault condition to less than 19µA.

This design was converted into the following schematic, see figure 23. The AD8232 will be powered by a +3.5V voltage supply, as this ensures the maximum dynamic range.

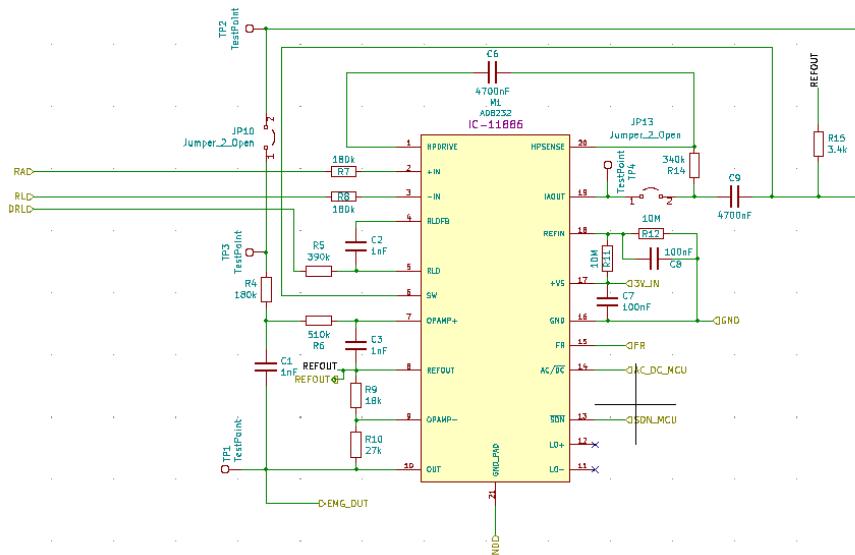


Figure 23 Schematic AD8232

4.2.1.2 Design 2

In this paragraph, four AFE designs will be presented. These AFE designs will all have the same IA and dc-offset filter stage, however they will differ in further signal filtering stages (number of filters, filter order, active or passive filter and single-ended or differential ended output signal).

Design 1 used the built-in RLD of the AD8232 to improve common-mode noise reduction. An RLD circuit could be implemented into design 2 using discrete components, different reports about the designs of an RLD-circuit are published [42],[43].

In high-density SEMG system this wouldn't be the best solution as per channel at least one extra op-amp is required, this results in an overall increase in the size of the AFE. An alternative method to match the common-mode noise reduction of an RLD is to implement a direct grounding method [43]. In this method, the subject is connected to the isolated ground of the EMG circuit. The only disadvantage of this implementation is that a bipolar voltage supply is required that could decrease the overall efficiency as more voltage regulators are needed to create the two voltage rails. Design 2 will use the direct grounding method to improve common-mode noise, as this method affect the overall size of each AFE module the least.

4.2.1.2.1 INA

Instrumentation amplifier configuration (INA) are used for differential signal amplification in the AFE. Table 1 states different commercially available INA that are suitable for high-density SEMG recordings.

Model	CM MR	PSRR [dB]	Slew Rate	Full power BW [kHz]	Max gain	Input Impedance [G pF]	Power [Vcc icc]	Price	Package	Gain bandwidth product
INA118	110	N.A.	0.9	7	1000	100 1	36/0.35mA	€9.75 €	DIP, SIOC-8	G = 1000 1kHz, G = 100 20kHz G = 10 100kHz
AD620	>90	>100	1.2	12	1000	10 2	18V/1.3mA	€10.97	SIOC-8	G = 1000 20kHz, G = 100 40kHz, G = 10 100kHz
AD8422	>90	N.A.	0.8	12	1000	200 2	5V/0.33mA	€7.10	MSOP-8	G = 1000 3kHz, G = 100 40kHz, G = 10 200kHz
INA333	>90	>60	0.16	>0.35	1000/0.5%	100 3	5V/0.05mA	€3.66	VSSOP-8, WSON	G = 10 10k, G = 100 2K G = 1000 600Hz
INA326	>60	>70	Filter limited	1	1000/+0.2%	10 2	5V/3.4mA	€3.96	MSOP-8, MSOP-10	G = 1,10,100,100 1kHz
AD8231	>95	>110	1.1	10	128	10 5	5V/4mA	€3.76	LFCSP	G = 128 20 kHz, G = 64 30 kHz G = 32 100kHz
AD8277	>100	>60	0.6	>2	1000	0.8 2	5V/0.32mA	€2.38	MSOP-8, SIOC	G 5,10,100,1000 >2kHz
AD8235	>60	>85	0.009	>0.8	100	440 1.6	5V/1.3mA	€3.50	WLCSP-11	G = 200 100Hz, G = 100 400Hz, G = 10 4kHz
AD8553	>100	>100	0.005	N.A.	1000	0.05 1	5V/0.07mA	€3.50	MSOP	G 1,10,100,1000 1kHz
LT1789	>110	>95	0.023	>1	100	1.6 1.6	5V/0.07mA	€3.36	SO-8	G = 10 20k, G = 100 10K G = 1000 1kHz
LT1167	140	150	1.3	>10	1000	1000 1.6	5V / 0.95	€5.97	SO-8, DIP	G = 1,10,100,1000 >10kHz
LT6800	>110	>100	0.2	200	100	N.A.	5V/1.3mA	-	MSOP-8	N.A.
MAX4194/7	>85	>80	0.06	>150	100	1 4	5V/0.095mA	€2.58	SO-8	G = 100 300Hz
MAX4208	>140	>100	0.08	0.8	5000	2 N.A.	5V/2.3mA	€3.36	SO-8	G = 60 1kHz
MAX4461	>80	>10	0.25	2.5	100	2 N.A.	5V/2.8mA	€1.77	TDFN, SOT23-6, SO-8	G = 1000 10K, G = 100 100k
INAx126	>90	N.A.	0.4	1.8	500	10 4	36V/0.175mA	€4.65	PDIP, SIOC, VSSOP	G = 5 100Hz, G=100 250Hz, G=1000 1kHz

Table 1 INA suitable for HD-SEMG recording. Table 1 is based on table 3.5 out of the book: Surface Electromyography: physiology, engineering and applications. Extra INA's have been added to the original table, the extra added INA were used in the design of a multi-channel/high-density SEMG acquisition system [10],[21],[28]. The prices included in this table are based on the prices of mouser.com, these prices could variate after publication.

To choose the correct INA the following specifications have been selected for the INA:

1. Gain bandwidth product of at least 1kHz at a gain of 100.
2. Gain accuracy of <0.1%.
3. Power consumption < 1mA.
4. CMRR > 90 dB at 50 Hz.
5. Price of INA < €5.
6. Input impedance of >100GΩ.
7. Slew rate of minimal 0.05 V/μS.

Price and package size play a very import role in the selection of the IA, as the device needs to be as small as possible and low in costs. However, the performances (CMRR, Power consumption and input impedance) should not be compromised over the choice of a small and low-cost IA. When choosing an IA high CMRR by itself does not give a guarantee of high-power line rejection since this is also a function of Z_{in} .

From Table 1 INA333, LT1167, LT1789, INA126 and the AD8422 meet these requirements.

The LT1167, provides both high input impedance ($100G\parallel 1.6pF$) and CMRR (140dB), but the high-power consumption is a drawback in portable products.

The INA126, provides both high CMRR (90 dB) and very broad supply voltage (+/-18V).

The INA333 is very low power ($50\mu A$), very high input impedance ($100G\parallel 3pF$) and excellent CMRR (100dB). The lower power consumption makes this product an ideal choice in portable products. The INA333 implements a chopper technique to reduce the input offset error, drift over time and the effect of 1/f noise.

The final choice was made to use the INA333, as it offers the best performance at its price point and package size. The INA333 provides a supply voltage of 1,8V – 5,5V or a bipolar voltage supply of +/-0,9V - +/-2,75V. The INA333 will be supplied with a bipolar voltage supply to implement the direct grounding method.

4.2.1.2.2 Dc offset

The electrode-skin interface generates a dc voltage potential, this dc voltage changes due to imbalances in the impedance of the electrode-skin interface. dc offset needs to be eliminated from the SEMG signal as it can cause the IA or other stages to saturate.

Dc offset can be suppressed with the following three methods:

- A) The dc offset voltage is rejected by placing a high-pass filter placed in front of the IA (see figure 24.1). The disadvantage of this method is that a 1% mismatch in the resistors (both $1M\Omega$), could mean a loss of -60 dB in the CMRR [].
- B) The dc offset voltage is rejected by an integrator that is connected between the reference input and the output of the IA (see figure 24.2). The integrator drives to make the inverting input equal to the non-inverting input. With this topology, it is still possible that the instrumentation amplifier can saturate in the first stage of the IA due to dc offset.
- C) The last method of eliminating dc offset voltage is by implementing a ‘Quashi’ high pass filter (see figure 24.3), which maintains the high CMRR of dc-coupled high input impedance instrumentation amplifiers [5]. In this design, the gain is obtained by an external resistor in series with a capacitor (RC- network) to create a high pass filter to suppress dc offset voltages (low frequencies).

The gain of the amplifier can be expressed with the following formula:

$$Z_G = R_{gain\ INA} + j\omega \cdot C_{gain\ INA}$$

Thus, dc gain is 1, while the high-frequency gain remains $G = 1 + \frac{2R_2}{R_{gain}}$.

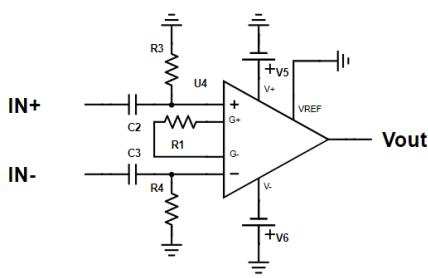


Figure 24.1 High-pass input filter

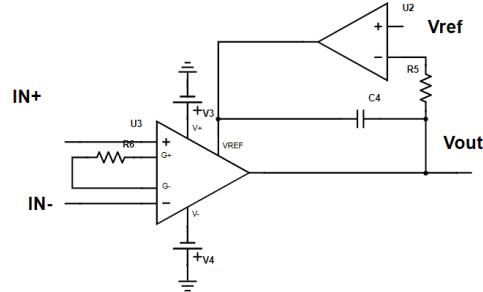


Figure 24.2 Integrator filter

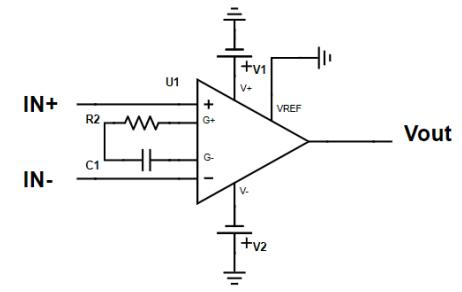


Figure 24.3 Quashi filter

Method two requires an extra op-amp to implement the integrator. This would increase the number of components used and the size of the PCB, thus this option was eliminated. Method three was chosen over method one, as this topology requires the least amount of components and maintains high CMRR even with dc offset.

To protect the patient against leakage current entering the body during a fault condition, resistors have to be added in front of the IA that is connected to the electrode. The current must be limited to less than 50 μ A in a fault condition (IEC-60601), (10) calculates the minimum required input resistor to meet this standard.

$$R_{patient} = \frac{Vcc_{max}}{I_{max}} = \frac{2.5V}{50\mu A} = 51k\Omega \quad (10)$$

Figure 25 shows the CMRR of the INA333 for different gain settings vs frequency. A higher gain results in a better CMRR at higher frequencies.

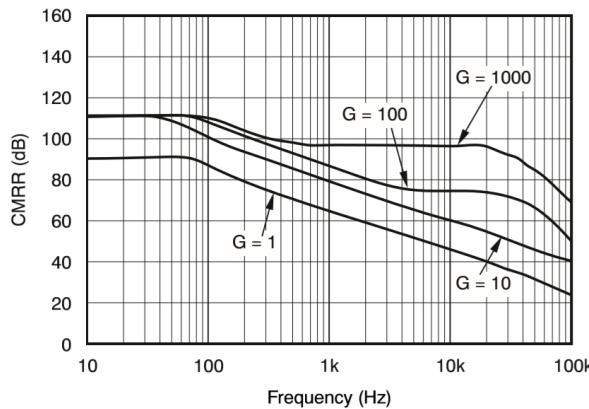


Figure 25 INA333 CMRR vs Frequency [29]

To ensure high CMRR of >100 dB at 50 Hz the G_{INA} must be set to $G > 10 V/V$ ($R_{gain\ INA} < 10k\Omega$). The voltage gain increases significantly after the zero cut-off frequency (see formula (11)) to reach the pole cut-off frequency (see formula (12)). The zero cut-off frequency is significantly influenced by $R_{patient}$ Resistor, see (11). See figure 27 for more information about both cut-off frequency locations.

$$F_{zero\ cut-off\ frequency\ INA} = \frac{1}{2\pi * C_{gain\ INA} * (R_{gain\ INA} + R_{patient})} = \quad (11)$$

$$F_{pole\ cut-off\ frequency\ INA} = \frac{1}{2\pi * C_{gain\ INA} * R_{gain\ INA}} = \quad (12)$$

In (13) the minimum capacitor is calculated for a gain of 10x with a cut-off frequency of 10 Hz.

$$C_{gain \ min \ INA} = \frac{1}{2\pi * F_{pole \ cut-off \ frequency \ INA} * R_{gain \ INA}} = \frac{1}{2\pi * 10Hz * 10k} = 1,6\mu F \quad (13)$$

To minimise mismatches between the different SEMG channels, it is essential that both the capacitor (C_{gain}) and the resistor (R_{gain}) have minimum tolerance. Table 3 states different capacitor tolerances values near the calculated $C_{gain \ min \ INA}$ value.

Capacitance	Tolerance 1	Smallest size	Tolerance 2	Smallest size
1µF	5%	0603	10%	0402
2.2 µF	5%	0805	10%	0402
4.7 µF	5%	0805	10%	0402
10 µF	5%	0805	10%	0603
22 µF	5%	0805	10%	0805

Table 4 available at Farnell and mouser, other suppliers may have different sizes available

An increase in C_{gain} will significantly lower the zero cut-off frequency to 1,18Hz (2.2uF), to 0,55Hz (4,7uF), to 0,26Hz (10uF) to 0,11Hz (22uF) all at a G_{INA} of 10x (R_{gain} of 10kΩ) (using formula (2)). A higher zero cut-off frequency is more desirable as it assures better dc offset suppression at lower frequencies. Thus higher IA gain requires a larger capacitor, a larger capacitor will significantly lower the zero cut-off frequency. However, a larger IA gain will reduce the gain required in the further stages. A compromise was made between these factors, a G_{INA} of 25x with a C_{gain} of 4,7uF was chosen in the to assure a cut-off frequency <10Hz.

R_{gain} is calculated in (14) for a gain of 25x, source of the formula for the IA gain [29].

$$R_{gain} = \frac{100k}{gain - 1} = 4166\Omega \quad (14)$$

The closest resistors near this calculated value with a tolerance of 0.05% are 4,3kΩ or 3.9kΩ. This will result respectably in a gain of 24,24x (at 4,3kΩ) or 26,64x (at 3,9kΩ). A R_{gain} resistor of 4,3k was chosen as this is the closest gain near 25 V/V. The cut-off frequency is calculated in (15),

$$F_{pole \ cut-off \ frequency \ INA} = \frac{1}{2\pi * C_{gain} * R_{gain}} \gg \frac{1}{2\pi * 4,3k\Omega * 4,7\mu F} = 7,87 \text{ Hz} \quad (15)$$

with a zero cut-off frequency located at 0,61Hz. A schematic of the first stage and dc offset suppression circuit is shown in figure 26.

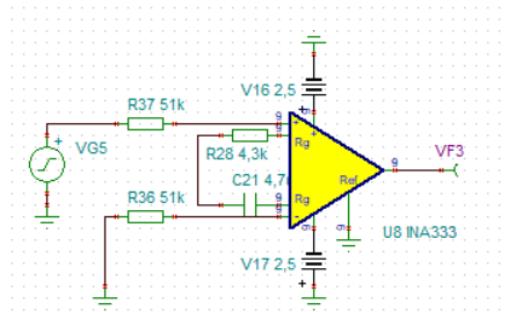


Figure 26 First stage gain and dc offset suppression

The simulation test results are shown in figure 27. The cut-off frequency is located at 10.3 Hz, the zero cut-off frequency is located at 0,35Hz, and at low frequencies (<100mHz) the gain is 1.

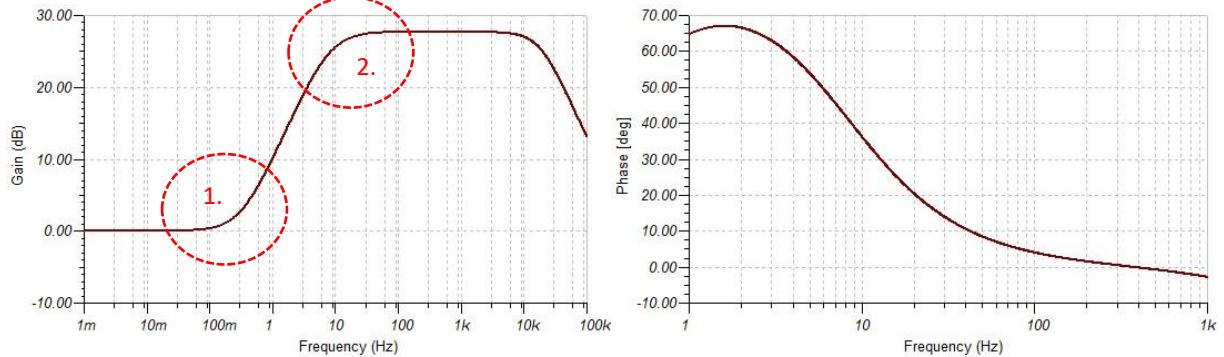


Figure 27 Frequency response dc-offset suppression circuit (IA), 1) the zero cut-off frequency and 2) pole cut-off frequency.

4.2.1.2.3 Design 2.1

Design 2.1 consists of a second order Butterworth high-/low-pass filter (Sallen-key configuration). The function of the second high-pass filter is for additional dc offset suppression, and the purpose of the low-pass filter is for the antialiasing. Design 2.1 can be summarised using the following design blocks.

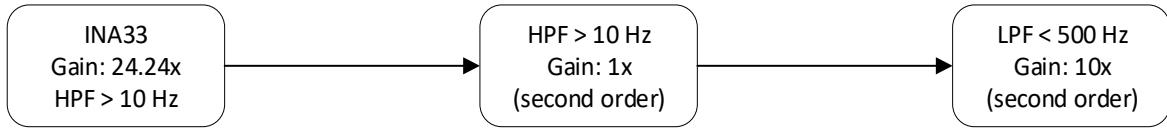


Figure 28 Building block design 1

4.2.1.2.3.1 Filter calculation

4.2.1.2.3.2 High-pass filter

The high-pass Butterworth filter was calculated in (16) using the same method as described in chapter 4.2.1.1.2, but a different Q formula was used to calculate the high-pass filter instead of the low-pass filter. The formula was derived from [30]. Due to impedance loading between design block, this will cause an increase of lower EMG BW, the second high pass filter was set to 5 Hz to ensure the low EMG BW cut-off frequency.

$$F_c = 10\text{Hz}, \quad A = 1, \quad Q = 0.5\sqrt{2} \quad \text{and } n = 1 \quad (16)$$

$$Q = \frac{\sqrt{mn}}{n + 1 + mn(1 - A)} = \frac{\sqrt{1 * m}}{1 + 1 + m(1 - 1)} = \frac{1}{2}\sqrt{2} \gg m = 0.5$$

$$F_c = \frac{1}{2\pi * R * C * \sqrt{mn}} \gg R = \frac{1}{2\pi * F_c * C * \sqrt{mn}} = \frac{1}{2\pi * 5\text{Hz} * 100nF * \sqrt{0.5}} \\ = 430k\Omega$$

$$R2 = R \gg 430k\Omega, \quad R1 = m * R2 \gg 220k\Omega, \quad C_{1,2} = 100nF$$

4.2.1.2.3.3 Low-pass filter

The low-pass Butterworth filter was calculated in (17) using the same method as described in chapter 4.2.1.1.2. The following values for F_c , A , Q and n were chosen to determine m :

$$(17) \quad F_c = 500\text{Hz}, \quad k = 10, \quad Q = 0.5\sqrt{2}, \quad m = 0.762, \quad \text{and } n = 1$$

$$R = \frac{1}{2 * \pi * F_c * C * \sqrt{mn}} = \frac{1}{2 * \pi * 500\text{Hz} * 2,2nF * \sqrt{0.0762}} = 524k\Omega$$

$$R2 = R \gg 524, \quad R1 = mR \gg = 39.92k, \quad C_{1,2} = 2.2nF$$

The last step is to convert these values into values within the E-24 series, thus $R2 = 510\text{k}\Omega$ and $R1 = 39\text{k}\Omega$.

4.2.1.2.3.4 Amplifier

All the Butterworth filters will be designed using the OPA333 as the op-amp. The OPA333 was selected as it offers a very low quiescent current of only $17\mu\text{A}$, excellent low voltage offset of $10\mu\text{V}$ and a slew-rate similar that of the INA333 ($0,16\text{ V}/\mu\text{s}$). The AD860X-series op-amp was also considered as it offers a much higher slew rate ($5\text{V}/\mu\text{s}$) and bandwidth ($>1\text{Mhz}$), but it consumes more power (0.85mA) and has a higher voltage offset of $500\mu\text{V}$. The choice was made as to use the OPA333, due to its very low power consumption.

4.2.1.2.3.5 Simulation

4.2.1.2.3.5.1 Simulation model

To simulate the performance of the designed circuit, a simulation model was created in LT-Spice. The simulation model replicates an SEMG signal obtained at the skin using the electrode-skin interface model, this model also includes the capacitive coupling of the body to mains and earth to simulate PLI (see figure 29).

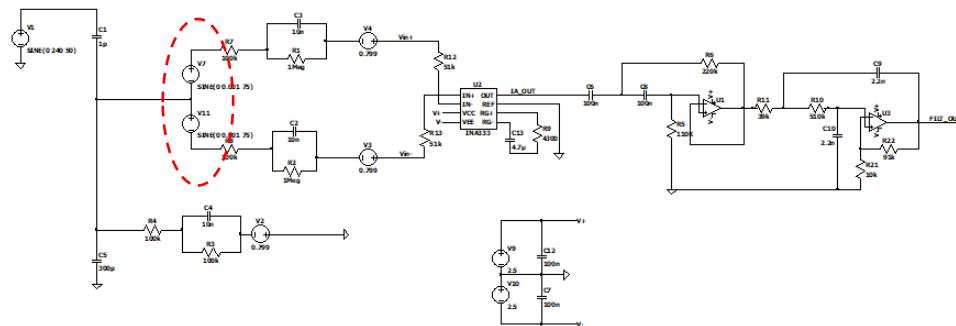


Figure 29 Circuit simulation of Design 2.1 in LT-Spice

A EMG signal of 2mVpp 75Hz was generated in the simulation (source $V11$ and $V7$, red circle). At the inputs of the INA333, the SEMG signal is corrupted by the powerline interference (see figure 30, channel vin+ and vin-), this is shown in the FFT of simulated signals (see figure 31). In the output signal of the INA333 the powerline interference is eliminated from the signal due to the CMRR effect (see figure 30). The input signal in figure 30 is multiplied by $25x$ to verify the gain of the INA.

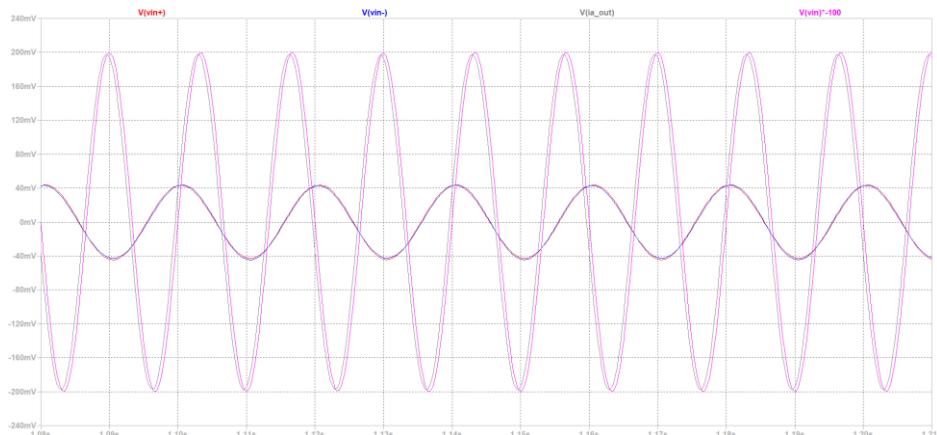


Figure 30 Scope results of output and input signals.

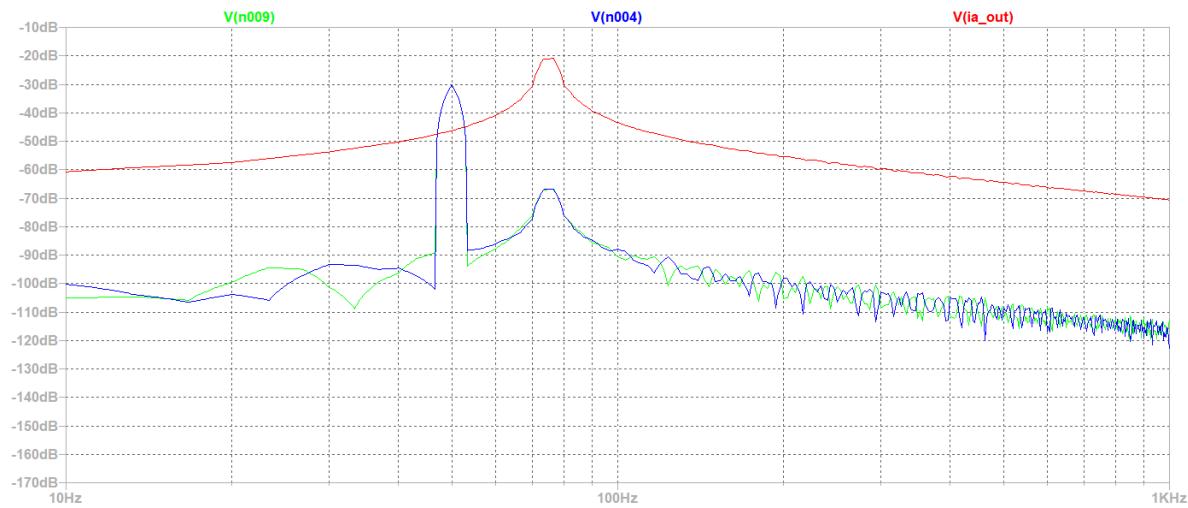


Figure 31 FFT of design 2.1

4.2.1.2.3.5.2 Frequency response

Figure 32 shows the frequency response of the simulated circuit in TINA SPICE (see figure 2.1). Within the pass-band frequency, the gain is measured at 47.7 dB, what corresponds a gain of 240 V/V. The upper cut-off is located at 524Hz, and the lower cut-off frequency is located at 9.1 Hz.

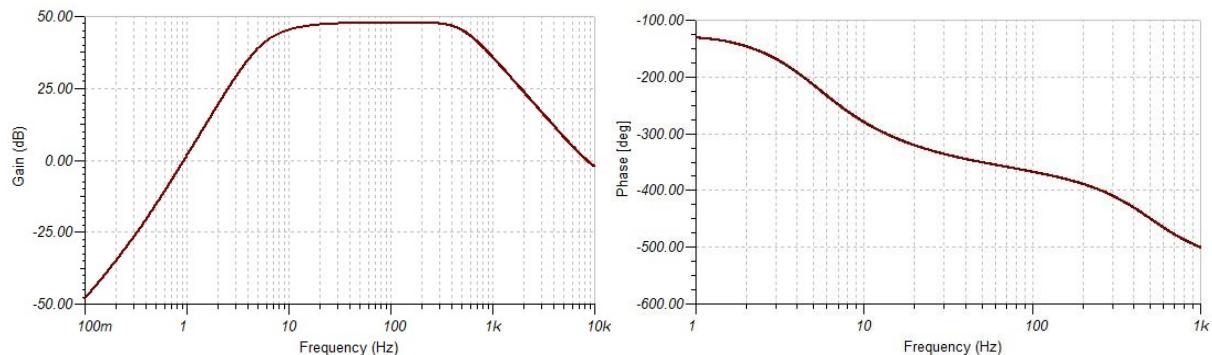


Figure 32 Frequency and phase shift of design 2.1

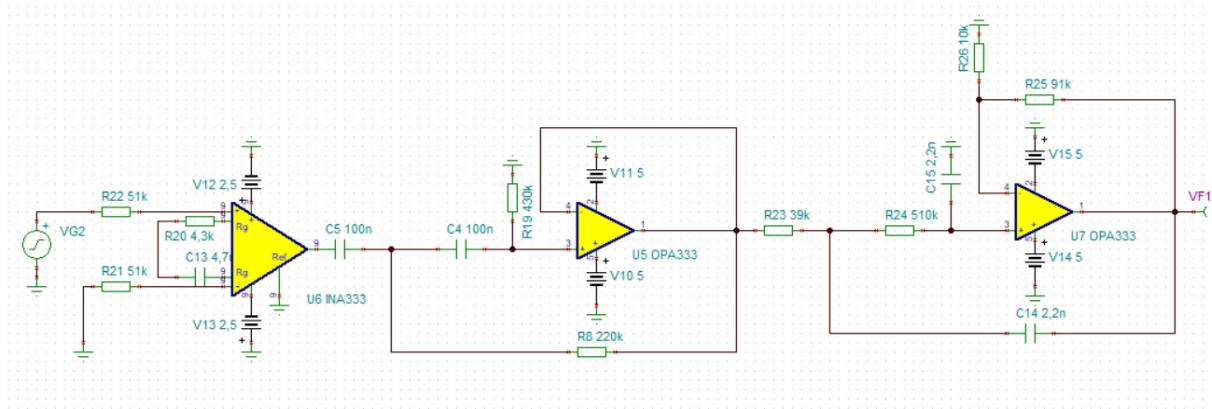


Figure 33 Schematic design 2.1

4.2.1.2.4 Design 2.2

The purpose of this design is to replicate the same design used in design 1, but fully design with discrete components. Design 2.2 will consist of a first-order high-pass filter and a second-order Butterworth low-pass filter (see figure 34).

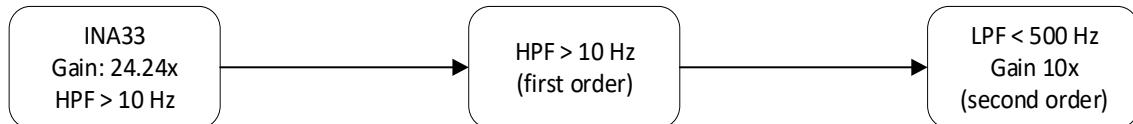


Figure 34 Building blocks alternative design 2.2

The design blocks were converted into the following schematic, see figure 35.

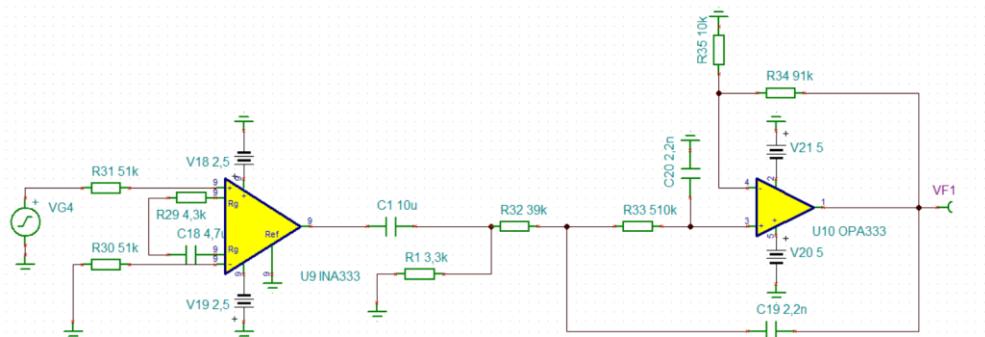


Figure 35 Schematic design 2.2

4.2.1.2.4.1 High-pass filter

The high-pass filter was designed with a cut-off frequency of 5Hz, thus a capacitor of $10 \mu\text{F}$ and a resistor of $3.3\text{k}\Omega$ are needed. Due to impedance loading between the filters, which will increase the lower EMG BW, the second high pass filter was set to 5 Hz to ensure the low EMG BW cut-off frequency.

4.2.1.2.4.2 Low-pass filter

See calculations chapter 4.2.1.2.3 (design 2.1).

4.2.1.2.4.3 Simulation

The circuit was simulated and the results are shown in figure 36. The upper cut-off frequency is located at 526 Hz, the lower cut-off frequency is located at 10.2Hz and the gain is 47.7dB.

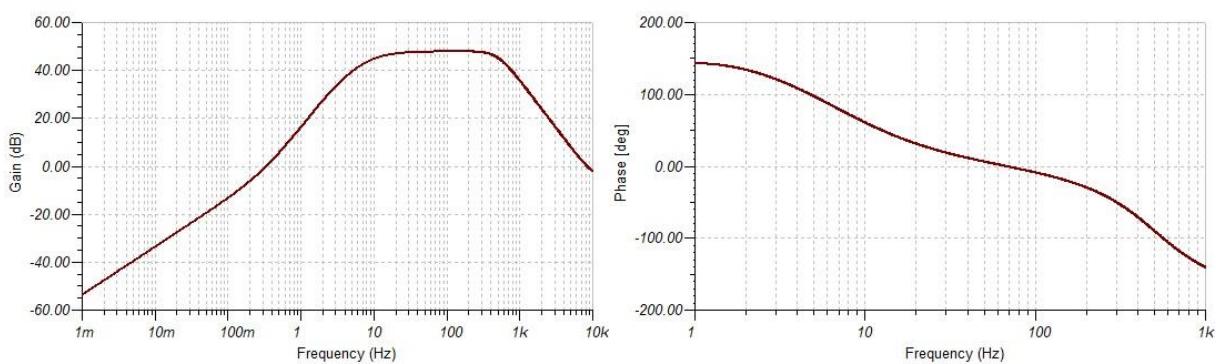


Figure 36 Frequency response design 2.2

4.2.1.2.5 Design 2.3

The previous designs were all designed as single-ended outputs, design 2.3 will use the differential-ended output. A differential ADC will convert the difference between the positive and negative inputs of the ADC while the positive and the negative input signals are 180° out of phase with respect to each other. The advantage of using a differential ADC is, 1) the dynamic input range is increased by two without increasing the supply rails and 2) the SNR is improved with respect to single-ended and pseudo-differential ADC configurations. The design consists of a unity gain high-pass filter, followed by an FDA multiple feedback low-pass filter.

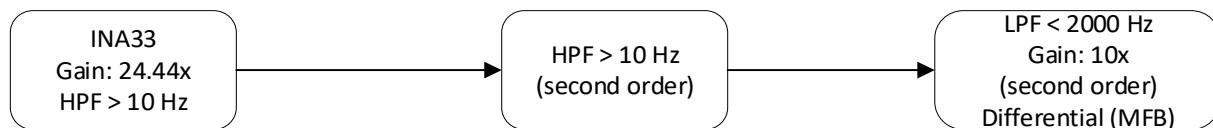


Figure 37 Design block differential driving ADC filter

4.2.1.2.5.1 High pass filter

See calculations chapter 4.2.1.2.3 (design 2.1).

4.2.1.2.5.2 Differential filter calculation

An example design of an FDA low-pass filter is shown in figure 38. This filter design consists of a second-order MFB low-pass filter and a first-order RC low-pass filter (R4 and C3).

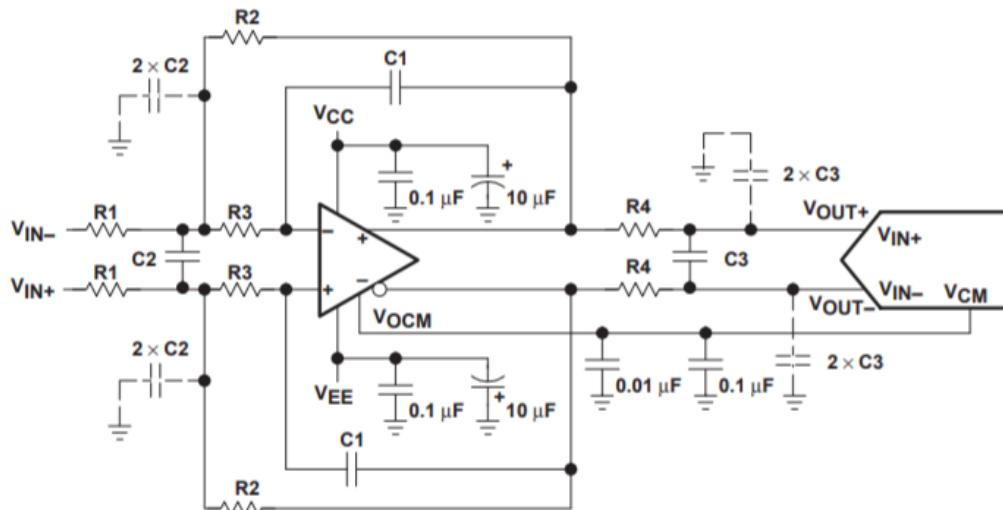


Figure 38 Third-order low-pass differential driving filter [31]

To ensure minimum group delay the cut-off frequency was set to 4 times the cut-off EMG bandwidth

$$f_{LPF} = 4 \cdot BW_{EMG} = 4 \cdot 500 = 2000 \text{ Hz}$$

The FDA low-pass filter is calculated (18), this formula's where derived from [31].

$$K = \frac{R2}{R1}, \quad Q = \frac{\sqrt{2mn}}{1 + m(1 + 10)}, \quad F_c = \frac{1}{2 * \pi * R * C * \sqrt{m(2n)}} \quad (18)$$

$$R2 = R, \quad R3 = mR, \quad C1 = C, \quad \text{and} \quad C2 = nC$$

The first step is to set a value for C1 and C2 to determine n. For n 10 was chosen, setting C1 to 3.3nF and C2 to 33nF. After this, the values for K and M can be selected to calculate the desired value for Q.

$$f_{LPF} = 2000 \text{Hz}, \quad K = 4, \quad m = 0.9 \quad \text{and } n = 10$$

$$Q = \frac{\sqrt{2mn}}{1 + m(1 + 4)} = \frac{\sqrt{2 * 33 * 3}}{1 + 3(1 + 4)} = 0.45$$

$$C_{1,2} = 1nF, f_{LPF} = 2000 \text{ Hz}, m = 0.9, n = 10 \gg \frac{1}{2\pi * 2000 \text{Hz} * 3.3n * \sqrt{2 * 10 * 1.1}} = 8.2k\Omega$$

This resulted in the following values:

$$R1 = 1.1k\Omega, \quad R2 = 5.6k\Omega, \quad R3 = 11k\Omega, \quad C1 = 2.2nF, \quad \text{and } C2 = 47nF$$

The first-order low-pass filter cut-off frequency must be set to well above the cut-off frequency of the MFB ($F_c * 10$), typically $R3$ is set to a low resistance value of $< 100\Omega$. This resulted into $R3 = 50\Omega$ and $C4 = 33nF$.

The THS4521 of Texas instruments [44] will be used as the FDA. The THS4521 offers a quiescent current of 1,1 mA per channel, a slew rate of 420 V/ μ S and is available in a VSSOP package (3mm x 3mm)

Design 2.3 was converted into the following schematic, see figure 39.

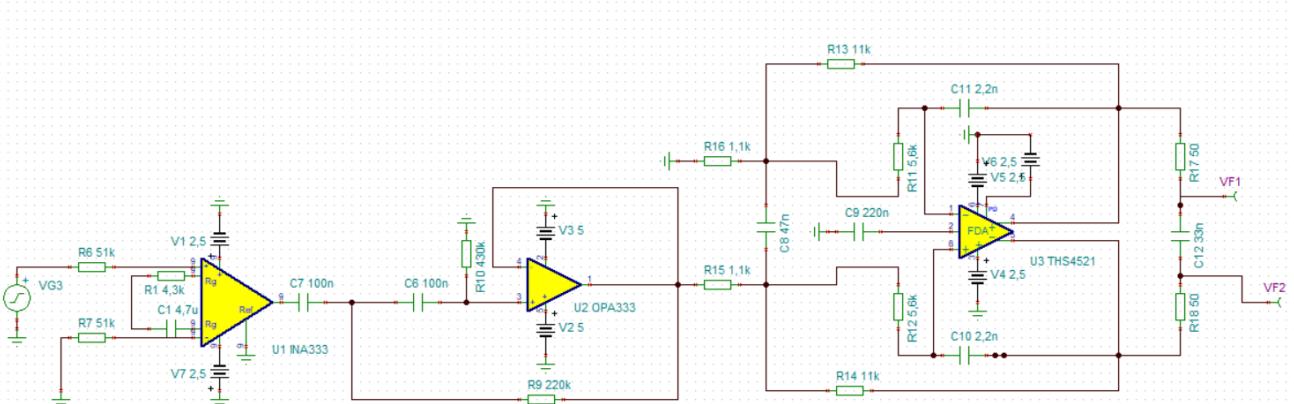


Figure 39 Schematic alternative design 1.3

4.2.1.2.5.3 Simulation

Design 2.3 was simulated in TINA SPICE, the gain and phase shift are shown in figure 40. The lower cut-off frequency is located at 10,7 Hz, and the upper cut-off frequency is located at 1994 Hz. The simulation results show a gain of 41 dB (118 V/V) in the EMG BW. This is not the expected gain, as this is only a the output measured at one side of the FDA low pass filter. The difference between these two outputs would increase the gain to 47.6dB (+/-240 V/V).

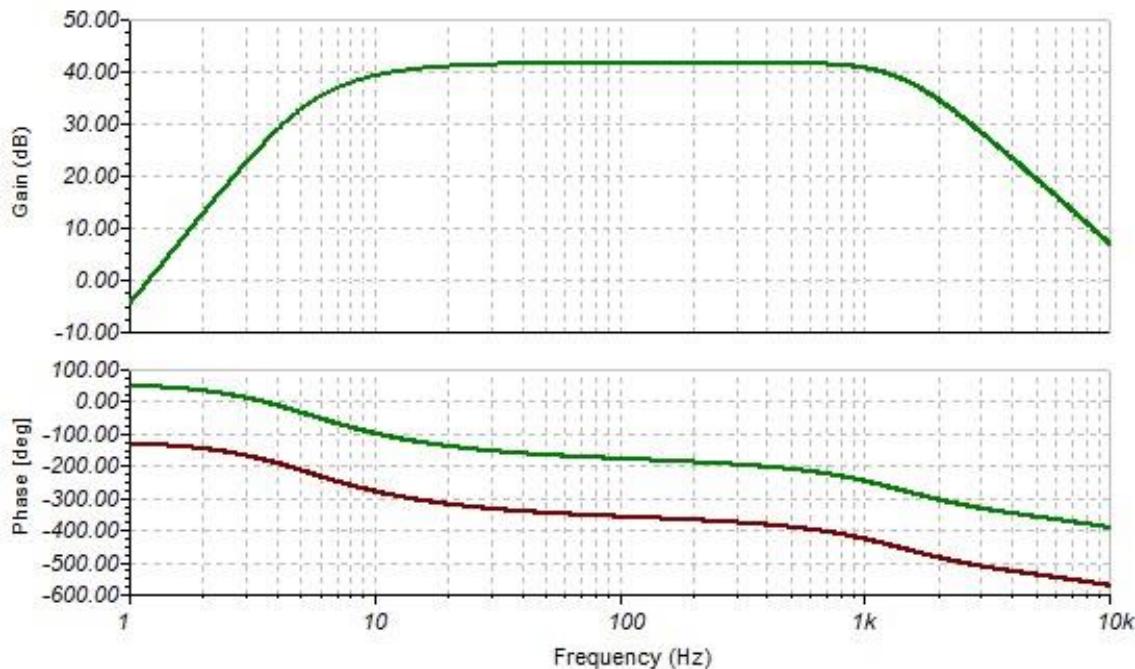


Figure 40 Simulation results design 2.3

Figure 41 shows the result when a sine wave with an amplitude of 2mV was applied to the input of the circuit.

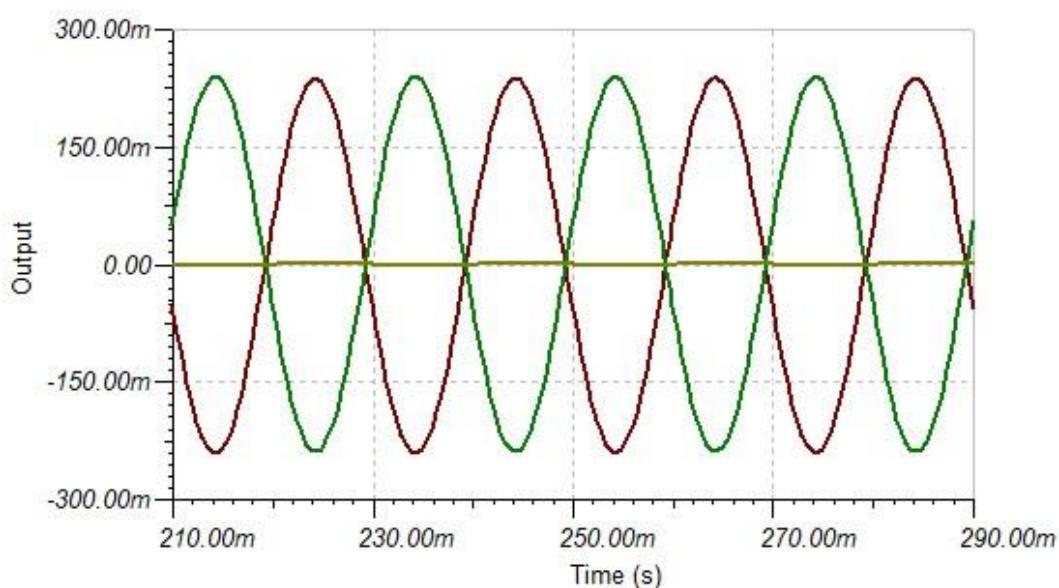


Figure 41 AC transient output of the FDA low pass filter

4.2.1.2.6 Design 2.4

Design 2.4 will only consist of an INA with a ‘quahsi’ high pass filter and a first order low-pass filter, which will significantly reduce the size of the AFE compared to the other designs.

To achieve the $G_{AFE,nominal}$ in only the IA-stage, a resistor of $400\ \Omega$ and a capacitor of $47\ \mu F$ are required to obtain the “quahsi” filter with a cut-off frequency of 10Hz . A $47\ \mu F$ capacitor is only available with a 10% tolerance in size of 1206 [3216 Metric]. This tolerance will easily introduce differences between the recording channels, an alternative method is to use add a PGA after the IA-stage to achieve the $G_{AFE,nominal}$ with a lower capacitor tolerance value. A PGA with a gain of $3x$ will be used, thus $\frac{G_{AFE,nominal}}{3} = 83x$. This can be achieved by using a 1200Ω resistor and capacitor of 22nF (available with 5% tolerance in 0805).

The low-pass filter resistor was set to 14k and the capacitor was set to 22nF to acquire a cut-off frequency of 500 Hz .

Design 2.1 can be summarised using the following design blocks, see figure 42.

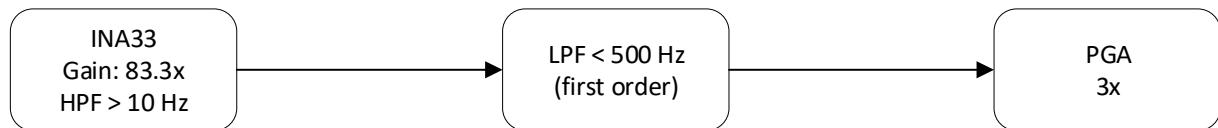


Figure 42 Building blocks alternative design 2

This design was converted into the following schematic, see figure 43.

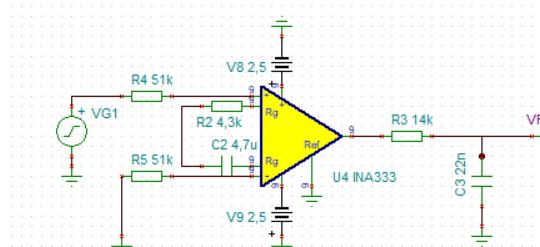


Figure 43 Schematic alternative design 2

Figure 44 shows the frequency response of design 2.4, the lower cut-off frequency is located at 8Hz , and the upper cut-off frequency is located at 519Hz .

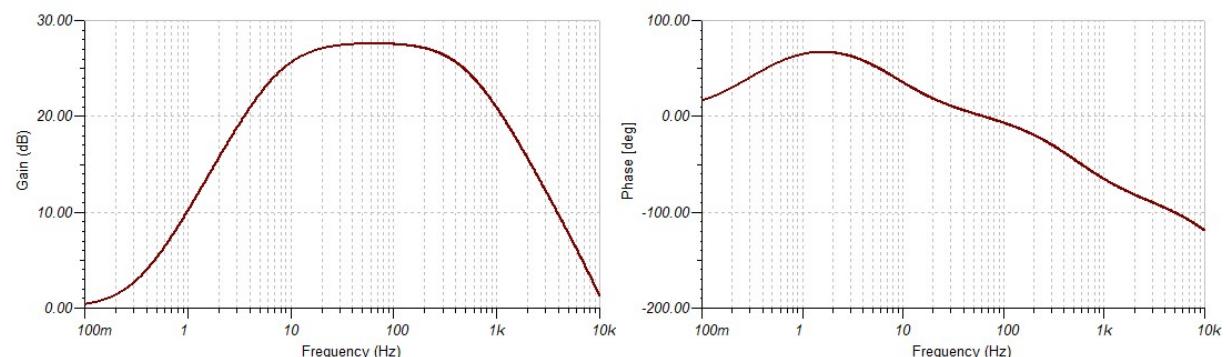


Figure 44 Frequency response design 2.4

4.2.2 ADC

The function of the ADC is to digitize the analog SEMG signal, so it can be further processed by the MCU and finally by the PC to be visualized.

The ADC chip selection was based on the followed listed requirements:

- A) SoC multichannel device with simultaneous sampling.
- B) Daisy chain feature in order to implement a single communication line for data retrieval.
- C) Low-power consumption.
- D) ADC inputs that allow: differential, pseudo-differential and single-ended input signals.
- E) A sample frequency of at least 2kSps per channel.
- F) FRS of 5V.
- G) ADC resolution of >16Bit

The ADS127X-series (2, 4 or 8 differential channels), ADS129X-series (2, 4 or 8 differential channels), AD7739 (4 differential channels) and the LTC2449 (4 or 8 differential channels) meet these requirements. All the ADC use an SPI interface. The ADS127X, AD7739 and the LTC2449 all offer a unipolar analog voltage supply of +5V, all thought the AD7739 has a unipolar analog supply it allows bipolar signals up to +/-2.5V at its inputs. The ADS1298 allows both a unipolar (+5V) and a bipolar (+/-2,5V) analog voltage supply. The ADS1278 offers data rate output up to 144kSps, the ADS1298 provides data rates up to 32kSps, the AD7739 offers data output rates up to 4kSps, and the LTC2449 offers data output rates up to 8kSps. ADS1278 cost 36,4€, the ADS1298 cost roughly the same and is priced at €33,4, the AD7739 costs €15,7 and the LTC2449 costs €13,8.

The final choice was made to use the ADS1298 as the ADC in this project, due to the following two reasons: 1) the output signal of the AFE needs to be amplified by 1,2, 3 or 4x (REQ-5), this can be accomplished by using the internal built-in programmable gain amplifier of the ADS1298 (1,2,3,4,6,8 or 12x). 2) The direct grounding method results in a bipolar signal output (ADS1298 offers bipolar input), if the ADC was powered by a unipolar voltage supply a voltage level shifter would be required in between of the AFE and the ADC.

Figure 45.1 shows how multiple ADS1298 can be combined using a daisy-chain method. The number of devices that can be chained together depends on the clock frequency generated by the host processor, this formula can be found in the datasheet.

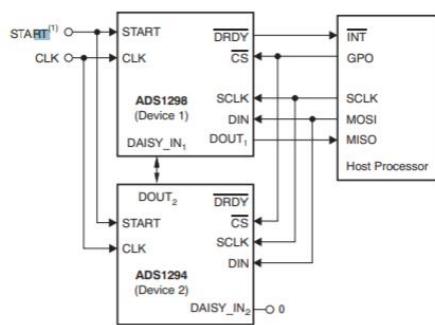


Figure 45.1 Daisy chain configuration of the ADS1298 [32]

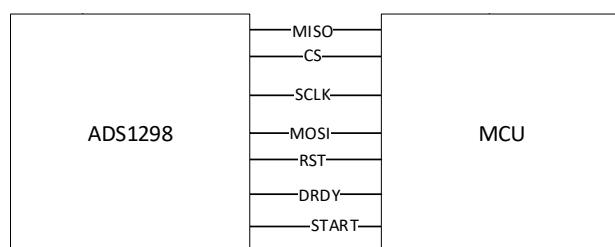


Figure 45.2 Connection lines between MCU and ADS1298

In figure 45.2 the connection schematic between the MCU and the ADS1298 is shown, besides the SPI lines to communicate with the ADS1298, 3 additional lines are required to obtain data from the ADS1298 (RESET, DRDY and START). More about all these is described in chapter 5.

4.2.3 Processor (MCU)

The data of the ADS1298 is obtained by a micro-controller via the SPI communication protocol. The choice was made to use a 32-bit micro-controller over an 8-bit micro-controller, as it offers much higher clock frequencies, thus is faster in processing data. Table 9 states different specifications of multiple 32-bit micro-controllers, these microcontrollers were chosen as they are available in development boards.

	SAM3X8E	ATSAMD21J	STM32F411x(C),(D),(E)
Core	32 bit cortex M3	32 bit cortex M0+	32 bit cortex M4
Frequency	84Mhz	48Mhz	Up tp 100Mhz
Number of Pins	100	64	100
Flash memory	512Kbytes	256KBytes	512Kbytes
SRAM	96Kbytes	32KBytes	128Kbytes
Analog/digital	12 bit (1Msps) + PGA + differential	12 bit (350ksps) + PGA Single ended and differential	3*12 bit
Digital/analog	12 bit (1Msps)	10 Bit (350ksps)	12Bit (MPSP)
Communication interfaces	2 * SPI 1 I2S 2 I2C 4 USARTS USB 2.0 180Mbps, 4kbyte FIFO	2* USART 2* I2C 2* SPI USB 2.0 12Mbps	3 * I2C 3 * USART 5 * SPI/I2S (max 50Mbit/s),SPI3, SPI3 and I2C USB 2.0 full speed (180Mbps) SDIO
Programming software	Atmel Studio 7.0 Atmel ICE	Atmel Studio 7.0 Atmel ICE	Atholic studio or CubeMx J-link
Price IC (€)	8,97	3.04	5.39
Price Development board (€)	29,41	27,11	14.32

Table 5 32-bit micro-controllers

The choice was made to use the SAM3X8E for two reasons, 1) a large FIFO buffer , 2) the SAM3X8E was preferred by the client.

4.3 Data transportation

This paragraph will describe the interface between the MCU and the PC. In the introduction, it was mentioned that a wireless interface between these two modules was preferred.

For wireless data transportation, two protocols can be used, the data can be sent using Bluetooth or WIFI. Bluetooth is a very affordable way of achieving a Personal Area Network (PAN) up to 20m, whereas WIFI has a much broader range up to 100m and allows the data to be accessed from all over the world. Bluetooth offers data rates up to a few Mb/s whereas WIFI offers data rates up to a few hundred Mb/s. However, increased data rates of WIFI result in a significant increase in power consumption. The software implementation of TCP/IP stacks for the WIFI on a micro-controller uses up a lot of Flash memory. Bluetooth is a straightforward software implementation, the microcontroller needs to send the data via UART (RS-232) to the Bluetooth module, and the Bluetooth module will take care of the rest of the data transportation. The choice was made to use a Bluetooth connection, as it offers low power consumption (BLE) and the easy software implementation.

The ADS129X-series will send per conversion 3 bytes (header) + 3*n bytes of data, where n is the number of channels, thus the ADS1298 will output 27 bytes (216 bits) per conversions. The final product will contain at least 64 SEMG channel (REQA-5), and each channel will be sampled at 2kSps. For a 64 channel system, 8 ADS1298 modules are required. The following formula calculates the required baud rate (bps) to send the data from the MCU to Bluetooth module using UART:

$$27 \text{ bytes} * 8 \text{ modules} * 2\text{kSps} = 432000 \text{ bytes per sec} * 10 = 4.32Mbps$$

The newest Bluetooth modules (5.0) offer data speeds up to 2Mb/s, what is significantly faster than the 4.2 version which only offered data speeds up to 1Mb/s. However, the 2Mb/s of Bluetooth 5.0 would still not cover our required data rate of at least 4.32Mbps to send the data in real-time to the PC.

The choice was made to eliminate the wireless data connection rather than to implement a WIFI data connection. The goal of this project was to create a portable and wireless HD-SEMG acquisition system, that could work at anytime and anywhere, but for a WIFI connection everywhere a stable network is required for the system to function correctly. As this device could be used in environments where no network is available, the choice was made to use an alternative solution for the data transportation. A USB 2.0 High-speed data communication was selected, a USB 2.0 data connection can offer data speeds up to 480 Mb/s, this would meet our required baud rate. No additional hardware (FTDI UART to Serial conversion IC) is required to send the data to the PC, as the SAM3X8E offers a built-in USB 2.0 high-speed port.

This small change had a significant impact on the total system design, as the wireless data transportation was removed from the current design, so was the need for a battery and a battery management system.

4.4 Isolation

A general setup of the system isolation is presented in figure 46. The isolation isolates the patient of AC mains and ground, to prevent dangerous current from entering the body during a fault condition. Two isolation barrier were included in the design, one for the analog voltage supply and the second one for the digital communication lines. Instead of a battery providing the analog circuit with isolation, an isolated dc/dc converter was added to the design, because unit ‘measure battery level’ was eliminated from the design. Digital isolation had to be included in the design as the digital lines are connected to the PC which is connected to AC mains.

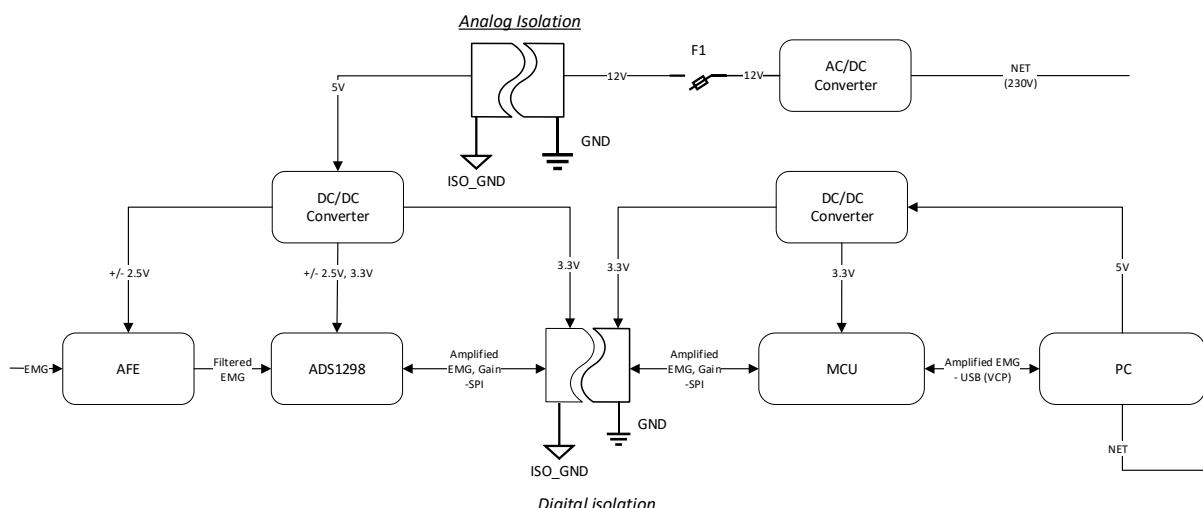


Figure 46 Patient Isolation protection block diagram

4.4.1 Digital isolation

The digital output lines of the ADS1298 (SPI) will be isolated with the si8663. The si86xx series is a digital signal isolator, using a modulated RF carrier to provide the isolation barrier. An example of the modulation is shown in figure 47. The si86xx-series are IEC 60601-1 approved [33].

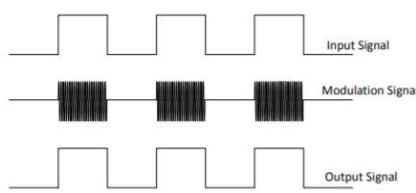


Figure 47 Modulation scheme [33].

The si8663 will provide isolation for the data lines of the ADS1298 (e.g. MISO, MOSI, SCLK and CS), the si8663 provides three isolated input lines and three isolated output lines. The si866X-series provides an isolated data rates up to 150 Mb/s, which is well within the required data rate of. The si8606 will provide a bidirectional communication path for the GPIO pins of the ADS1298.

4.4.2 Analog isolation

A possibility was to use a battery to provide the system with an isolated voltage, as we wanted to design a very stable functioning system a better option was to use an DC power adapter. The R2S-1205 will supply the analog isolation, converting +12 DC volts from the net into an isolated voltage of +5V. The +12V will be supplied by a DC power adapter (230VAC – 12VDC, 2.1mm dc power jack). The R2S-1205 was selected as it is already medical certified. Before the input of the R2S-1205 an fuse was placed for additional security (max 2A).

4.5 Power supply

An overview of the power supply units are presented in figure 48.

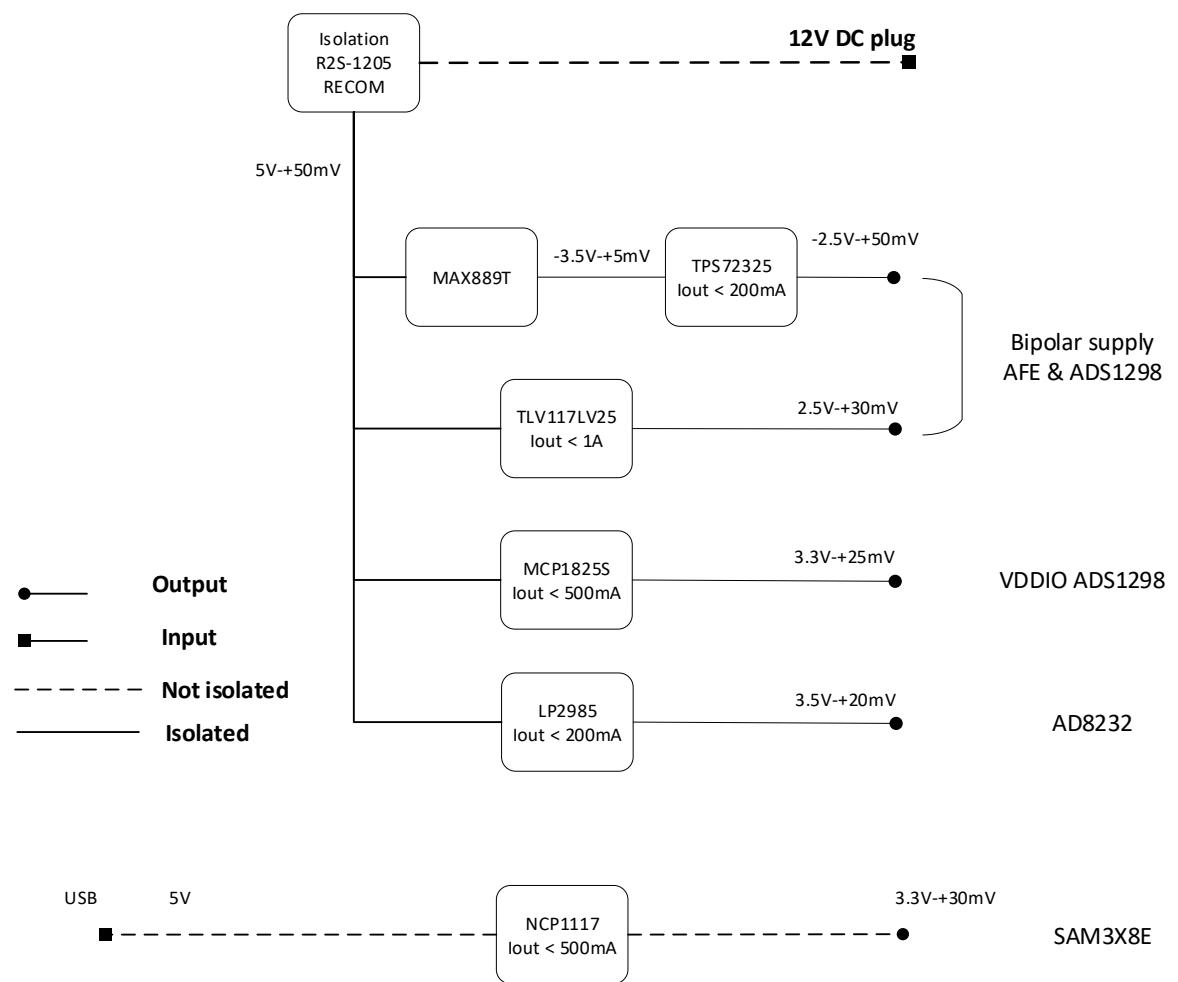


Figure 48 Power supply units

4.6 Design summary

The new design can be summarised in the following design blocks, see figure 49. As mentioned earlier, the unit ‘measure battery level’ had to be eliminated from the current design. Eventually the design will be simplified as only one AFE design will be selected that will be used in the final design.

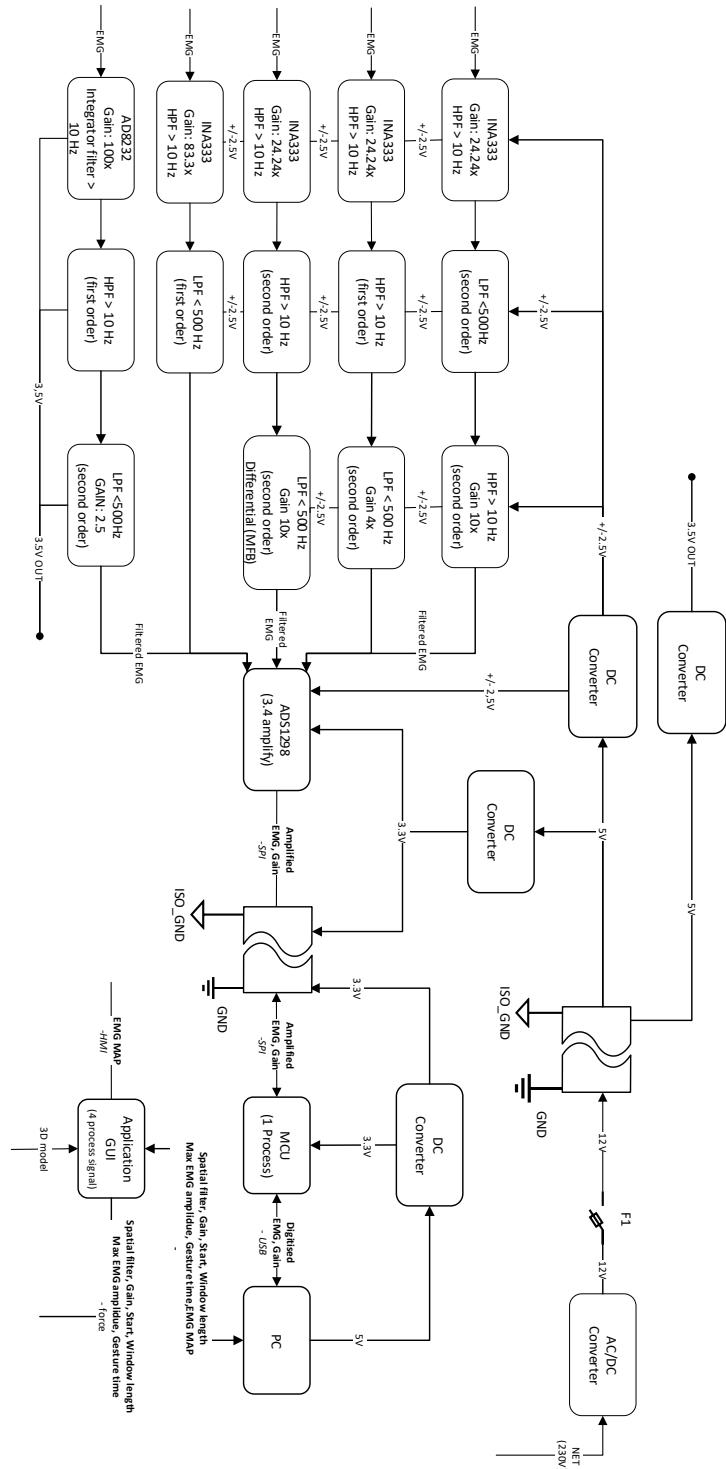


Figure 49 Architecture diagram of the system

5 Implementation phase

5.1 Hardware design

The designs presented in figure 49 was converted into one PCB (see figure 50). On the PCB the SAM3X8E (MCU) was not included, instead a development board was used (Arduino DUE). Once the set-up has proven to work effectively and the final AFE design is chosen, a new PCB will be designed which will include the SAM3X8E. The schematics of the PCB are included in attachment J, and was designed using KICAD. The following pins need to be connected between the MCU and the PCB (DUE pin-10 CS, pin-4 DRDY, pin-5 RESET, pin 1,3,4 MISO, MOSI and SCLK).

The best option would be to use a 4-layer PCB, where the inner two layers are the ground and power planes. Shorter return paths and lower loop impedances are capable with a 4-layer PCB, reducing the EMI significantly compared to a 2-layer board. The price of a 2-layer board is considerably lower than a 4-layer board, €5,- compared to > €45,- euro (PCB GOGO). As this was only a test PCB the cheaper option was chosen and a 2-layer board was chosen.

The top layer plane on the isolated side was set to 2.5V and the bottom layer was set to GND (isolated GND) to ensure that the return current flow is undisturbed. In-between of each design block of the design, solder jumpers were included, so the parts of each could be tested individually. To each side of the solder jumper, PCB test pins were attached, to easily connect measuring probes or other equipment. The output of each design was kept as short as possible to the ADC inputs. The capacitor connected to the VSS and VDD lines were kept as short as possible to prevent noise on the inputs of the ADC. The VREFP and VREFN capacitors of the ADS1298 were chosen with the lowest tolerance (X7R-series) and placed as close as possible to the pins of the ADS1298 to ensure no noise on the ADC.

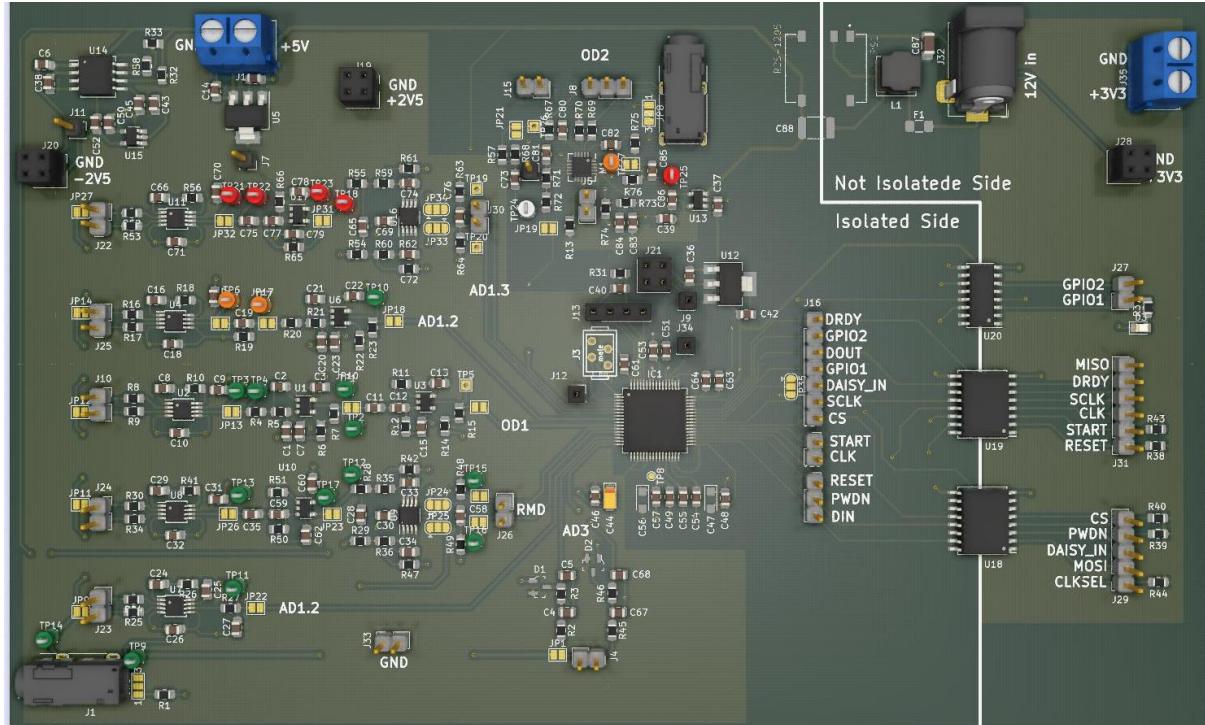


Figure 50 AFE test design board (front)

5.2 Unit test

In this paragraph the designed AFE will be tested to validate whether they have met the unit specifications.

5.2.1 Test procedure

5.2.1.1 Gain (bandwidth)

To determine the EMG bandwidth of the AFE, the AC voltage gain was calculated at different frequencies. A sine wave of 10 mV_{pp} with an offset of $(V_{cc} + V_{ss}) / 2$ with a range between the 0.1Hz-10kHz is generated by the function generator, this signal will be connected to the positive input electrode of the AFE. The negative input of the AFE will be connected to the ground electrode. The set-up of this test is shown in figure 51.

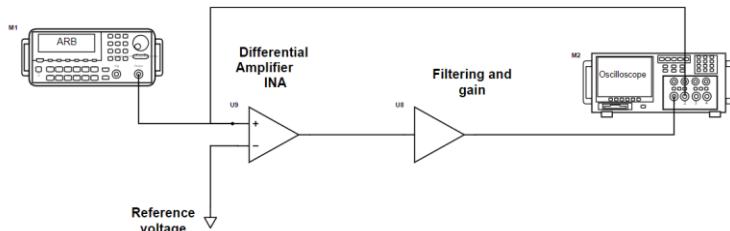


Figure 51 Gain and bandwidth setup

The gain of the AFE can be calculated using the following formula:

$$\text{Gain (dB)} = 20 \log \left(\frac{V_{out \text{ peak-to-peak}}}{V_{in \text{ peak-to-peak}}} \right)$$

The Digilent Analog Discovery 2 was used to calculate the AC gain. This device has two function generator and two oscilloscope channels, a network analyser tool application (Waveforms) was used to measure the gain and the phase shift of the designs. Function generator 1 and oscilloscope channel 1 need to be connected to the input of the design and the output needs to be connected to oscilloscope channel 2. A detailed description of the connection is explained in the test document (see attachment C).

5.2.2 Test results

5.2.2.1 Design 1

Figure 52.1 and 52.2 shows the measured gain and phase shift of design 1. The maximum gain is 47,86 dB, this corresponds to 248 V/V, the lower cut-off frequency (-3dB) was located at 11Hz and the upper cut-off frequency (-3dB) was located at 520Hz. The gain error within the EMG bandwidth (20- 500Hz) is 0.046%. The total phase shift within the EMG bandwidth (20- 500Hz) is 115°.

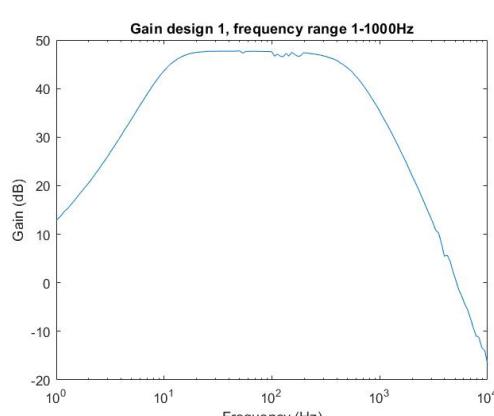


Figure 52.1 Gain Design 1

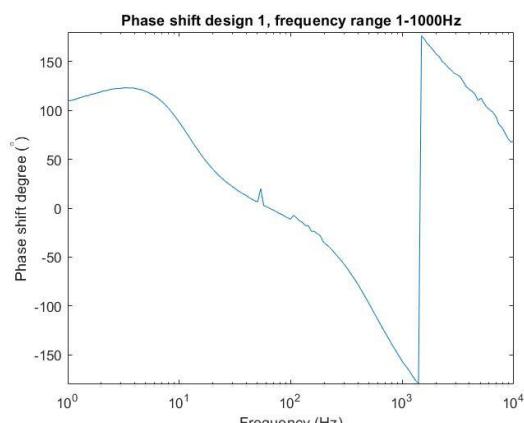


Figure 52.2 Phase shift design 1

5.2.2.2 Design 2.1

Figure 53.1 and 53.2 shows the measured gain and phase shift of design 2.1. The maximum gain is 47,6 dB, this corresponds to 240 V/V, the lower cut-off frequency was located at 10.1Hz and the upper cut-off frequency was located at 525Hz. The gain error within the EMG bandwidth (20- 500Hz) is 0.041%. The total phase shift within the EMG bandwidth (20- 500Hz) is 142°.

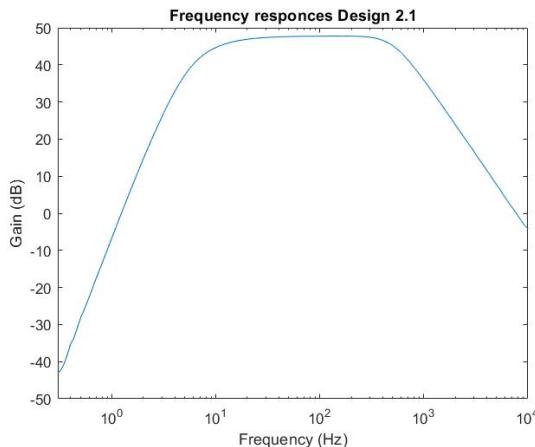


Figure 53.1 Gain design 2.1

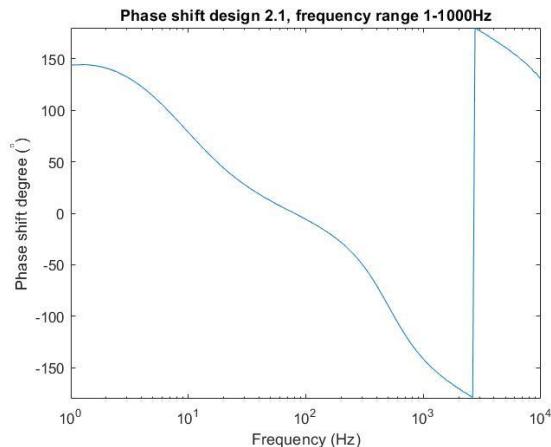


Figure 53.2 Phase shift design 2.1

5.2.2.3 Design 2.2

Figure 54.1 and 54.2 shows the measured gain and phase shift of design 2.1. The maximum gain is 47,74 dB, this corresponds to 240 V/V, the lower cut-off frequency is located at 14,1Hz and the upper cut-off frequency is located at 524Hz. The gain error within the EMG bandwidth (20- 500Hz) is 0.05%. The total phase shift within the EMG bandwidth (20- 500Hz) is 138°. Although the lower EMG BW is higher than the allowed error (10Hz, 30% error), this is still a viable option as most of the EMG energy is located between the 50 and 150Hz.

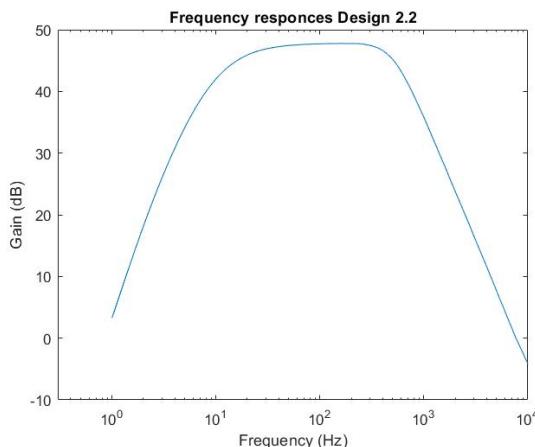


Figure 54.1 Gain design 2.2

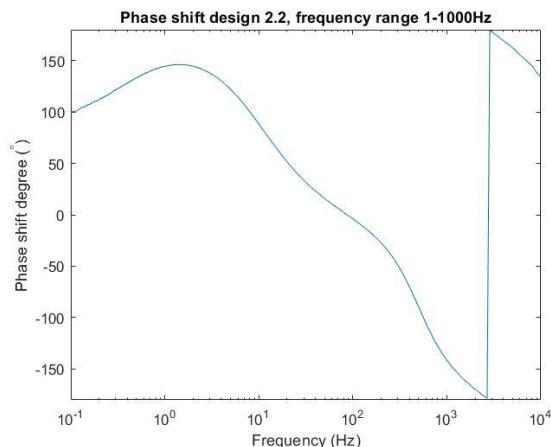


Figure 54.1 Phase shift design 2.2

5.2.2.4 Design 2.3

Figure 55.1 and 55.2 shows the measured gain and phase shift of design 2.1. The maximum gain is 47,55dB, this corresponds to 239 V/V, the lower cut-off frequency is located at 10.3Hz and the upper cut-off frequency is located at 2025Hz. The gain error within the EMG bandwidth (20- 500Hz) is 0.025%. The total phase shift within the EMG bandwidth (20- 500Hz) is 60°.

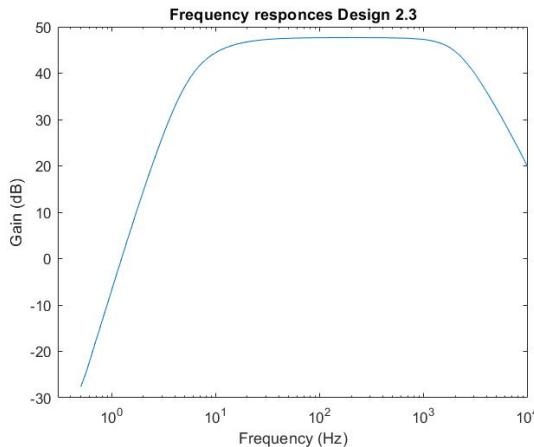


Figure 55.1 Gain design 2.3

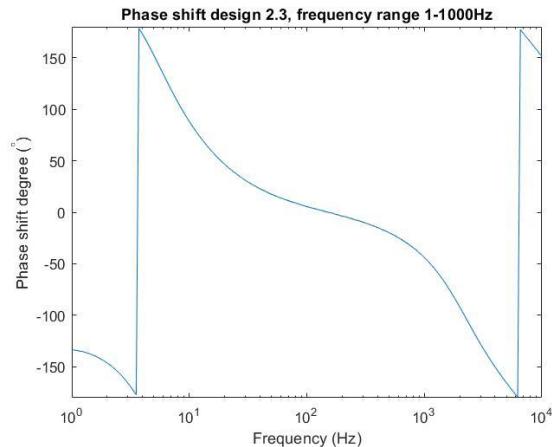


Figure 55.2 Phase shift design 2.3

5.2.2.4.1 Design 2.4

Figure 56.1 and 56.2 shows the measured gain and phase shift of design 2.1. The maximum gain is 47,6 dB, this corresponds to 241 V/V, the lower cut-off frequency is located at 13.1Hz and the upper cut-off frequency is located at 502Hz. The gain error within the EMG bandwidth (20- 500Hz) is 0.076%. The total phase shift within the EMG bandwidth (20- 500Hz) is 91°.

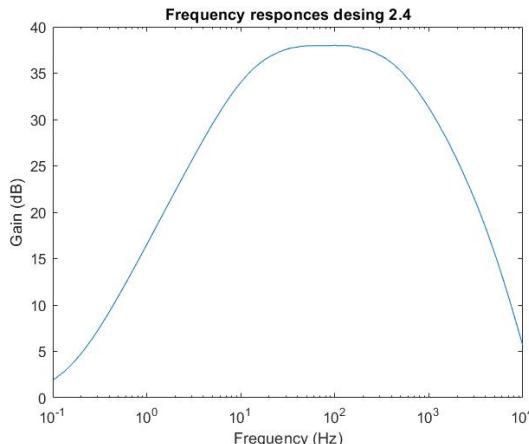


Figure 56.1 Gain design 2.4

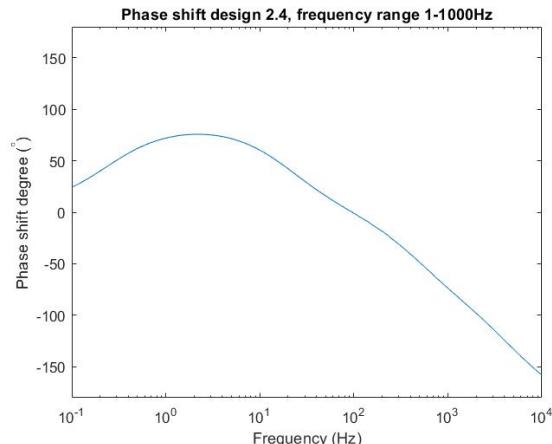


Figure 56.2 Phase shift design 2.4

5.3 Software

5.3.1 Measure EMG

This section will explain how the ADS1298 is programmed and how the data is transferred to the PC. The ADS1298 will send per conversion three header bytes plus $3*n$ bytes of channel data, where n are the number of used channel. Thus the ADS1298 will send 27 Bytes (216 Bits) of data per conversion. The header will contain 2 bytes with the lead-off status of each channel and the GPIO pin status (see figure 57).

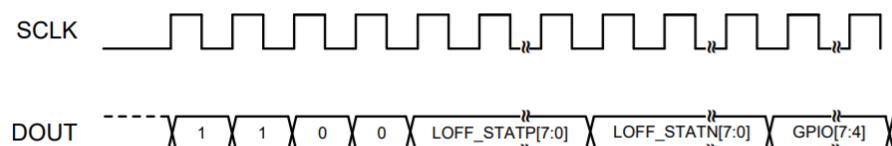


Figure 57 Headed data [32]

The minimum clock frequency for SCLK in RDATAC (read data continuous mode, every time a DRDY interrupt occurs new conversion is available) mode can be calculated using the following formula:

$$F_{sclk} = F_{data} * (n + 1) * 24, \text{ where } n \text{ is number of channels}$$

For a 64 channel system a minimum F_{sclk} of 3.2MHz is required. Higher SPI data rates are also possible as long as the F_{sclk} stays below the 20MHz. As the prototype will only have 8 channels the minimum F_{sclk} was set to 2MHz to ensure that all the data is captured and send to the PC before the next DRDY occurs.

To correctly communicate with the ADS1298 the polarity SPI setting must be set to SPI Mode 1, this means CPOL = 0 and CPHA = 1. This is a very important step to follow. See figure 58 for the SPI stetting of an SAM3X8E MCU.

```
SPI_StructInit(&spi);
spi.SPI_Mode = SPI_Mode_Master;
spi.SPI_Direction = SPI_Direction_2Lines_FullDuplex;
spi.SPI_DataSize = SPI_DataSize_8b;
spi.SPI_CPOL = SPI_CPOL_Low;
spi.SPI_CPHA = SPI_CPHA_2Edge;
spi.SPI_NSS = SPI_NSS_Soft;
spi.SPI_BaudRatePrescaler = SPI_BaudRatePrescaler_32;
spi.SPI_FirstBit = SPI_FirstBit_MSB;
SPI_Init(SPI1, &spi);
```

Figure 58 SPI settings, the red circle indicated the SPI settings that are very important

5.3.2 Register setting of the ADS1298.

The ADS1298 offers 20 registers for enabling or disabling specific functions. A summary of all the command to control the ADS1298 is included in attachment J.

5.3.2.1 Lead-off detection

The ADS1298 offers a built-in function that can monitor the connection of the electrodes with the skin. This is done by injecting an excitation signal and measuring the output to determine the status of the electrode connection, leadoff detection can either be detected with an ac or dc signal. To accomplish lead-off detection, both the positive and negative sense register (LOFF_SENSEP = 0Fh & LOFF_SENSEN = 10h) of that specific channel must be set to '1'. The status of each lead is reported in the lead status register (LOFF_STATP = 12h & LOFF_STATN = 13h), where '0' is lead-on and '1' is lead-off. For the determination of lead-off a current is passed in a particular direction, the direction is determined by selecting either pull-up or pull-down resistors on each channel (LOFF_FLIP = 11h).

The thresholds value for the lead-off detection and ac or dc mode are set in the LOFF register (04h). However, first, the comparators to validate the thresholds values must be turned on the CONFIG4 register (17h).

By default, lead-off detection is turned off in the register settings, as a lead-off detection is not used in the current design of the project, these registers do not have to be activated.

5.3.2.2 Testing/calibration function.

The ADS1298 provides different options for internal noise testing and calibration. The test signal frequency and amplitude of the signal can be rest in the CONFIG2 register.

5.3.2.3 Electrocardiogram (ECG) related functions

As the ADS1298 is mainly marketed for ECG application, as it offers various ECG specific related functions to detect or improve ECG signals measurements. The ADS1298 offers Built-in Right leg drive, Wilson Center Terminal (WCT) and Pace detection. Both WCT and Pace detection are ECG specific related functions, and will not be further explained as they are not of use in the project. However, the right leg drive can also be

implemented in EMG application to improve common-mode signal rejection. By default, the right leg drive, Wilson Center Terminal and pace detection is turned off, unless set differently by the user.

5.3.2.3.1 Right leg drive

Right leg drive is a technique to reduce the common-mode signal by feeding the inverted common-mode signal back into the body. As this function is mainly used in ECG application, it also can be used in EMG application to improve common-mode rejection.

First, the RLD measurement must be enabled (RLD_MEAS) to route right leg drive input (RLD_IN) to the channel with multiplexer setting 010. Next, the right leg drive signal source must be selected (RLDREF_INT bit), '0' for external and '1' for internal ((AVDD-AVSS)/2). The right leg drive buffer must be powered ON by setting PD_RLD bit to 1 (default is turned OFF, thus is 0). For the lead-off detection of the right leg drive electrode, the RLD_LOFF_SENSE bit must be enabled. The current status of the lead-off of the right leg drive can be read from the RLD_STAT bit. In the current design, a direct grounding method was used to improve common-mode rejection, thus the right leg drive will stay disabled

5.3.2.4 global register

These global registers determine the basic setting of the ADS1298 and must be set before use.

5.3.2.4.1 CONFIG1 (address = 01h)

This register contains 8 bits that can be used to set different settings of the ADS1298 related to the sample frequency of the ADS1298. Bit 7 control whether the device is in high resolution mode or low power mode, as the device is being designed as energy efficient the low power mode was selected. Thus this bit must be set to 0. Bit 2 – 0 control the sampling frequency of the ADC (F_{MOD}). In high-resolution mode $F_{MOD} = F_{CLK} / 4$ and in low power mode $F_{MOD} = F_{CLK} / 8$ ($F_{CLK} = 2.048\text{MHz}$). For the sampling frequency of 2kSPS (REQA-02), these bits need to be set to 03h (LP Mode)

Thus to CONFIG1 register, 00000011 = 03h must to be written.

5.3.2.4.2 CONFIG2 (address = 02h)

In CONFIG2 register no bits need to be addressed, as these are related to the WTC and a test signal, which is both not being used.

5.3.2.4.3 CONFIG3 (address = 03h)

This register contains 8 bits that can be used to set control the internal reference buffer voltage and the RLD of the ADS1298. As the RLD function is not used, only the reference buffer bit needs to be addressed. This means that bit 7 must be set to 1 to power on the internal reference buffer, and bit 5 must also be set to 1 as a reference voltage of 2,4V is used.

Thus to CONFIG3 register, 11000000 = C0h must be written.

5.3.2.4.4 CHnSET (address = 05h – 0Ch)

These registers control the setting for channel 1-8, it controls the power mode (ON/OFF), PGA gain and multiplexer of each channel. Depending on the gain set by the user, either 10h (1x), 20h (2x), 30h (3x), 40h (4x) needs to be written to these registers. To turn a channel OFF 80h must be written to each channel.

5.3.3 Operating the ADS1298

Operating the ADS1298 involves going through a set of sequential steps to obtain the data. A flow-diagram of these sequential step is shown in figure 59. In the current set-up, the internal oscillator of the ADS298 will be used.

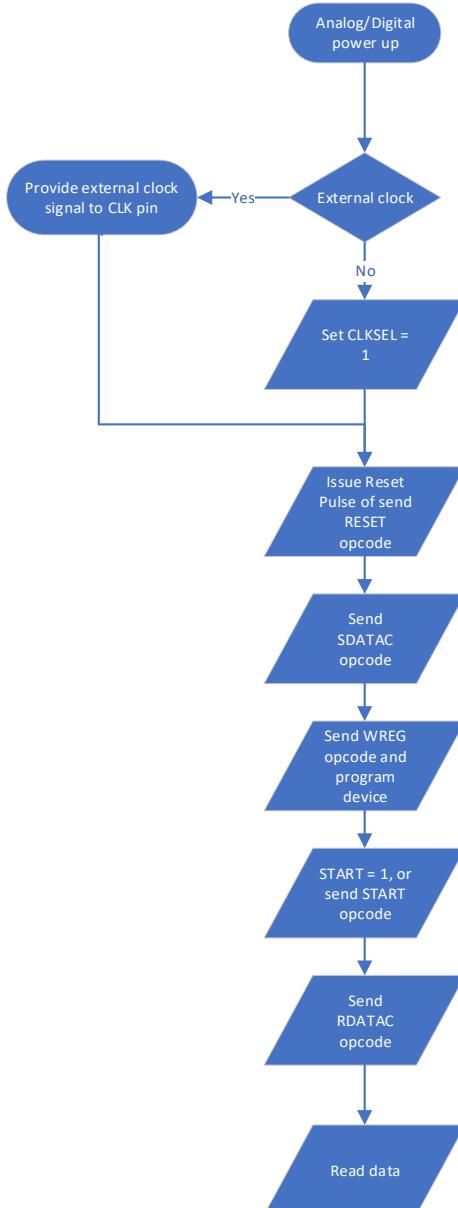


Figure 59 Flow diagram ADS1298

5.3.4 Micro-controller

Figure 60 explains the flow chart of micro-controller to communicate with the ADS1298. This is a simple program to read data from the ADS1298 that is required to verify the system requirements.

The program starts with the MCU initialising the I/O, SPI and data communication (USB), next the ADS1298 is initialised using the method explained in the previous chapter (both setting and programming sequence), this is followed by enabling the interrupt pin to measure when the data is ready to start reading it.

Every time a falling edge interrupt occurs on the DRDY pin of the ADS1298, the MCU collects the data (27 bytes) and sends them to the PC (only 24 bytes as the header data is not being used in the application). The data will be sent to the PC in the following sequence: sample 1 “ byte1, byte2byte26, byte27\r\n”. The data will be sent to the PC via CDC (virtual com port).

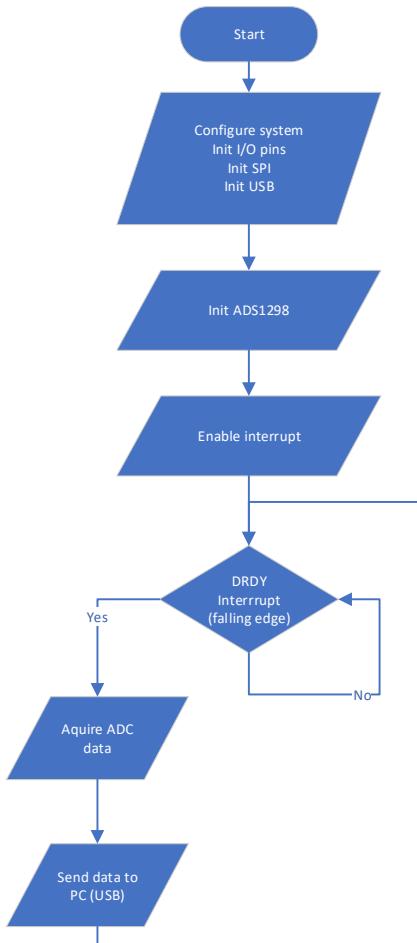


Figure 60 Flow chart micro-controller programming

The code corresponding to this flow chart was developed in attachment J.

Figure 61 shows how CONFIG0 register (ID) is read, this register contains the facility number (ADS1294,1296 or 1298) and the number of active channels (4,6 or 8). Using the READ_ID function (see attachment G) 92h is read from this register and this corresponds to ADS129X family with 8 channels. This test verifies successful communication between the MCU and the ADS1298.

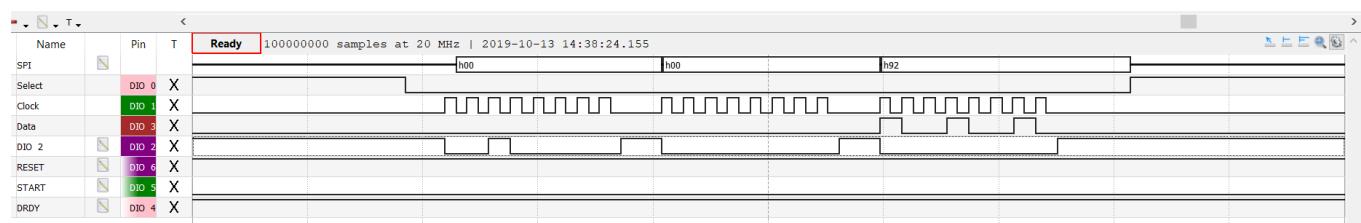


Figure 61 Read device ID

Figure 62 shows how the data is collected after a DRDY interrupt, 27 bytes are received, three header bytes and 24 register bytes. After a falling edge is issued on the DRDY line an interrupt occurs and all the 27 bytes are read.



Figure 62 DRDY, 27 bytes of data

Figure 63 shows the sample time between 2 samples (DRDY), the time is $499\mu\text{s}$ this corresponds to 2kSps. Thus REQA-03 has been achieved (see attachment F for an enhanced image of figure 58).

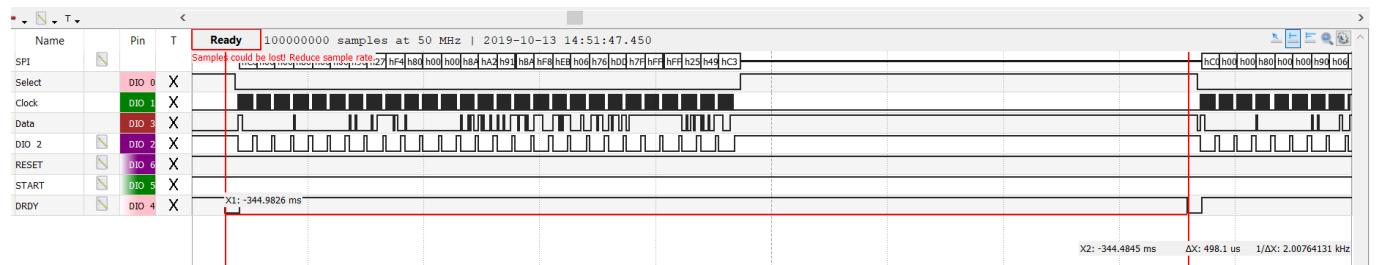


Figure 63 Sample frequency

5.3.5 Test interface

To verify the measured data a test interface was developed in GUI. In the verification software, a few parameters need to be measured to validate the system requirements. These parameters are the signal amplitude (peak-to-peak) and Root-mean-square (RMS). Figure 64 displays the flowchart of the GUI. In the GUI the 'User' can enter the number of samples they want to collect, by default this value is set to 1000 samples. Once the user has pressed the start button, the GUI starts to collect the number of samples entered to read by the user. Once this is complete the read data bytes are converted into voltages per channel and shown in a graph.

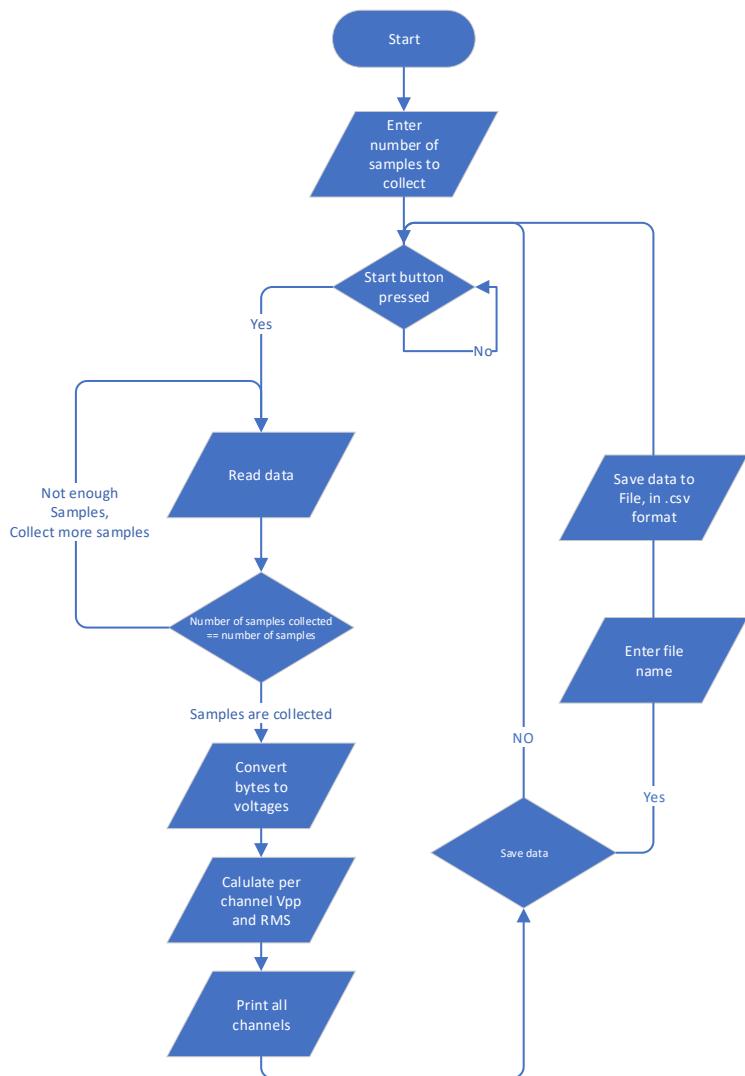


Figure 64 Flow chart GUI

The source code of this python application is attached in attachment J. To use this code on your PC, you must change the USB com-port address in the code to the MCU com port connect on your PC. The original idea was to develop a GUI to plot the data in real-time on the PC, but this was not possible as the data is being updated too slow, e.g. 1000 sample where selected (signal of 1Hz 0,5Vpp), this should take about 4 seconds to plot at 250Sps (just a test sample frequency), but the data took 15-20 seconds before all the collected samples were plotted. Thus the choice was made to not plot the data in real-time, but to collect all the data first and to plot the data afterwards.

The GUI was developed in Python 3.7. MATLAB was also considered as MATLAB offers pre-made functions for peak-to-peak and RMS calculation and an easy method to develop GUIs. However, because MATLAB isn't free for the general public Python was chosen.

In the application, the user can select to display all the channels or just to display a single channel by clicking on tick boxes of each channel. After the data is collected and displayed in the graph the user can choose to save the data to a .csv file to be saved and analysed in another program such as MATLAB.



Figure 65 Visualization application, 1) Button to start new measuring session, 2) Graph to plot the data, 3) button to calculate and print the RMS and Peak-to-peak voltage of the channels, 4) Check boxes to turn channel ON or OFF, 5) Button to close the application, 6) Save data to .csv files and 7) Number of samples to be collected.

To verify the GUI, a dc voltage of -1V was connected to channel 1 and to channel 2 a sine wave of 1Hz 0,5Vpp was connected, other channels of the ADS1298 were turned off in the firmware code (10h – 90h) and the sample rate of the ADS1298 was set to 250Sps. These signals were directly connected to the inputs of the ADS1298, by disconnecting the AFE from the ADS1298 inputs. The first test was to verify if the GUI was capable to display various channel, this was tested by turning channel-2 ON or OFF and measuring the data. This resulted in the following two figures.

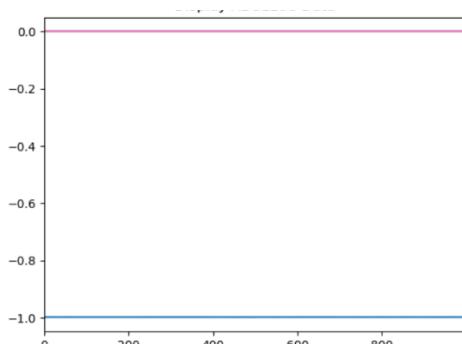


Figure 66.1 Display all channels, except channel 2

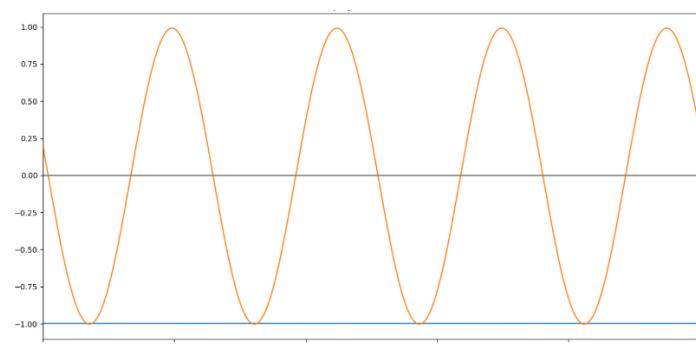


Figure 67.2 Display all channels, including channel 2

The second test was to verify if the GUI was able to process the data at a sample rate 2kSps. This was done by increasing the sampling frequency from 250Sps to 2kSps (06h to 03h to CONFIG1 register). At Sample rates above the 250Sps, suddenly voltage spikes occurred on the signal (see figure 66 and 67), this problem would increase more when the sample rate was increased. As channel 2 - 8 were turned off (powered down), these channels should actually not be displaying anything in figure 67. Thus it is a very strange behaviour of the ADS1298. Using an FFT analysis (see figure 68.2) of the data obtained in figure 68.1, it was ruled out that this was caused by the 50Hz noise.

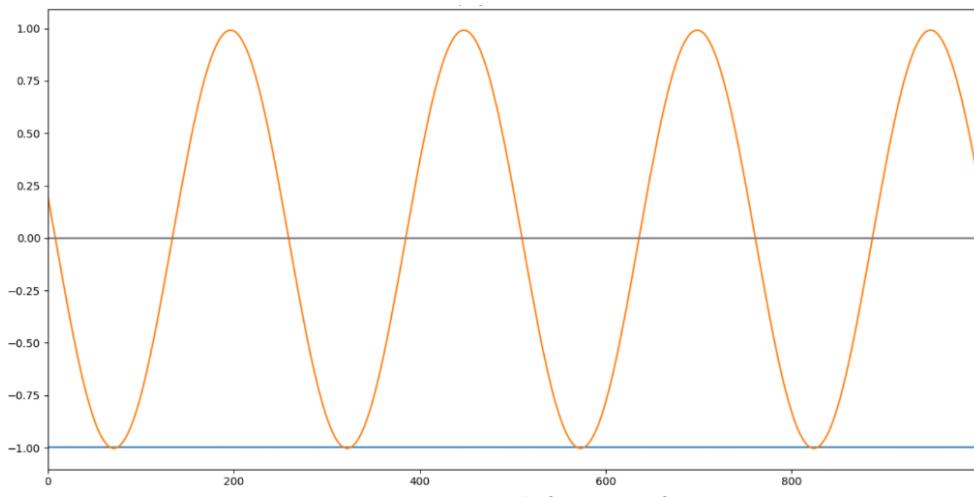


Figure 68 Sample frequency of 250Sps

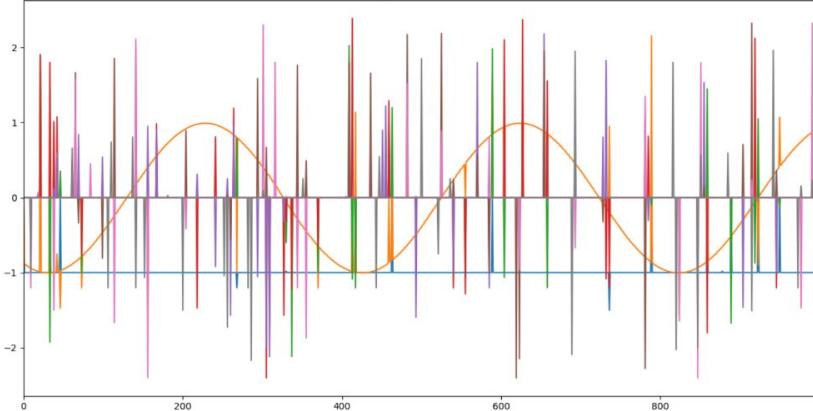


Figure 69.1 Sample frequency of 1kSps

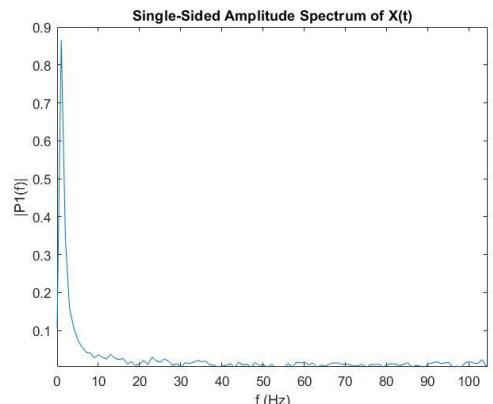


Figure 70.2 Sample frequency of 1kSps

When the sample rate was reduced to 250Sps back, the GUI was tested to verify whether it was capable of calculating the correct peak-to-peak voltage (Vpp) and the RMS of the measured signal. The results show that the GUI measured a Vpp 0.984Vpp and a Vrms of 0.704V. These values confirm that the calculation of both parameters worked correctly. As the formula to calculate Vpp uses a min-max calculation of all the data set, no correct values could be obtained at sample rates above the 250Sps due to the voltage spikes.

In figure 68 the first voltage spike appears at sample number 7 of channel 2 (the sine wave). The SPI data send from the ADS1298 to the MCU was compared to the USB data obtained by the PC (see figure 61), to verify of one of the two caused the problem during transportation. Figure 68 clearly indicates that the ADS1298 send the same as was obtained by the PC. Thus the problem is clearly not caused during the data transportation between the modules.

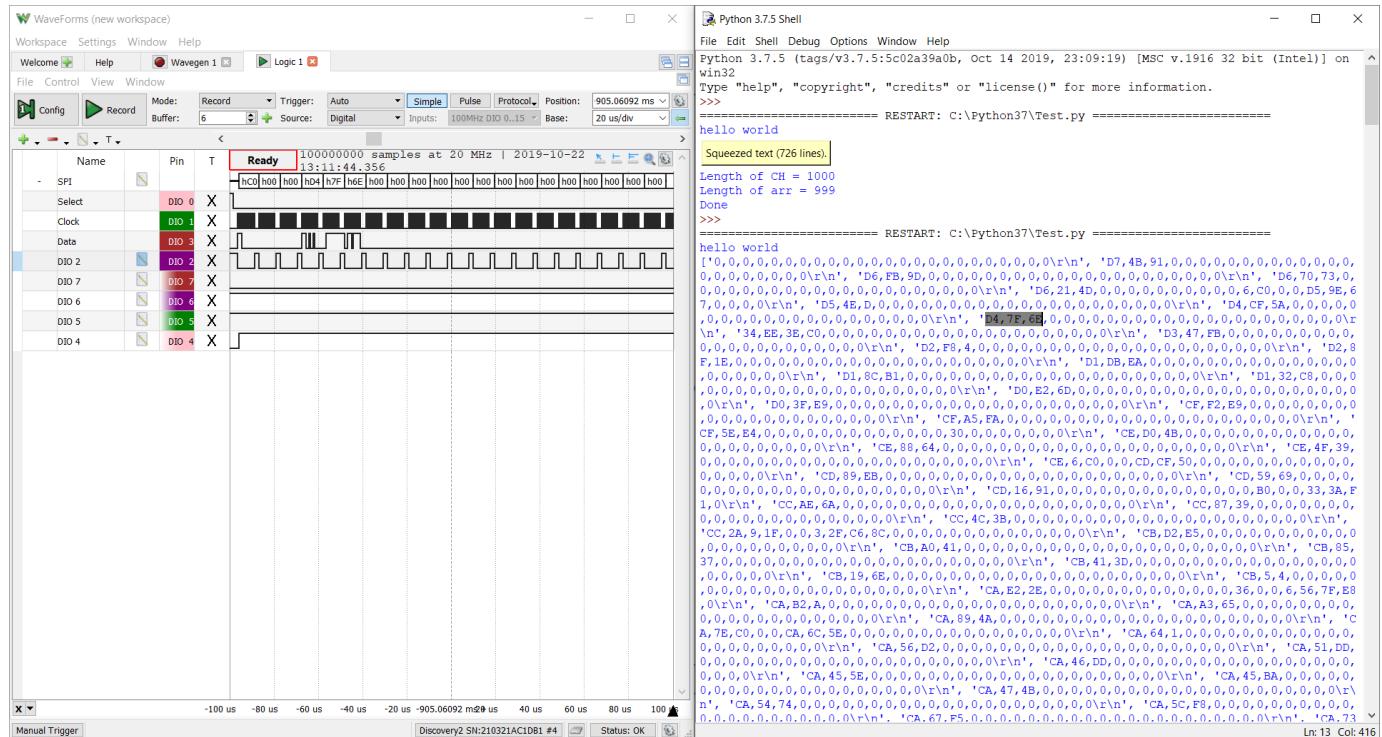


Figure 71 Verification of problem with voltage spikes

To figure out whether the problem was caused by the designed PCB or the PC, the PCB was replaced by the ADS1298_FE kit, unfortunately the same problem occurred. Thus the problem could be caused by improper isolation either or via the USB port.

The ultimate solution was to change to MCU with the MMB0 EMV board of TI (also part of the ADS1298ECG_FE kit), this module resolved the problem so that at 2kSps there were no voltage spike visible on the signal. The developed GUI was not able to communicate with the EMV board, as a dedicated application was required to obtain the measured data via the EVM board. The dedicated software of the EMV module collects all the raw hex data bytes. It is possible to save these bytes to a .csv file and use MATLAB to configure these bytes into voltages (this was done using the following file: rawhex_to_voltage_ads1298.m(see attachment J)). However, this solution is only a temporarily solution, to be able to perform the tests required to choose a signal AFE design. Once this final design is chosen a new PBC will be designed to resolve this problem.

6 Validation

This chapter will give a short summary of how the different parameters of each design will be tested and the results of each tested parameter will be presented later on in this chapter. A full report of the test procedures is included in attachment F.

6.1 Test procedure

As mentioned in chapter 5 all the designed AFE will be tested to identify which design will be used in our final design. The designed AFE will be evaluated on gain (bandwidth), common-mode rejection ratio (CMRR), input-referred noise (IRN), size, price and how they perform in real-life situations.

6.1.1.1 Common Mode Rejection Ratio

To measure the CMRR of the differential amplifier, a function generator will generate a signal with an amplitude of 1 V_{pp} , this signal is connected to both inputs of the AFE (see figure 69). The ground lead of the function will be connected to the ground electrode of the EMG circuit. The frequency range is from 10Hz – 1000Hz. At different frequencies, the output signal is measured by the ADS1298 to calculate the CMRR of the AFE.

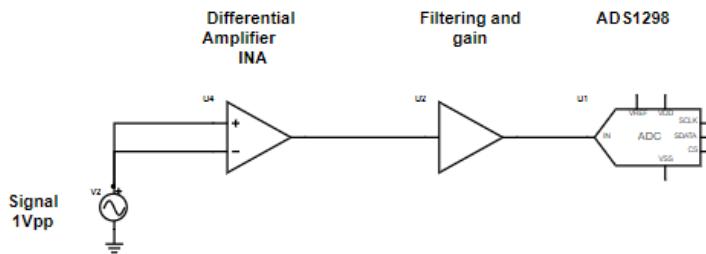


Figure 72 Common mode rejection ratio test

The formula to calculate CMRR is:

$$CMR = Gain (\text{dB}) - CMG (\text{dB})$$

Where:

$$CMG (\text{common-mode gain}) = 20 * \log\left(\frac{V_{out \text{ RMS}}}{V_{in \text{ RMS}}}\right)$$

The term CMR is a logarithmic expression of the common-mode rejection ratio (CMRR). The Gain in the formula is calculated in the previous paragraph.

6.1.1.2 Input referred Noise

The test set-up of measuring IRN is displayed in figure 71.

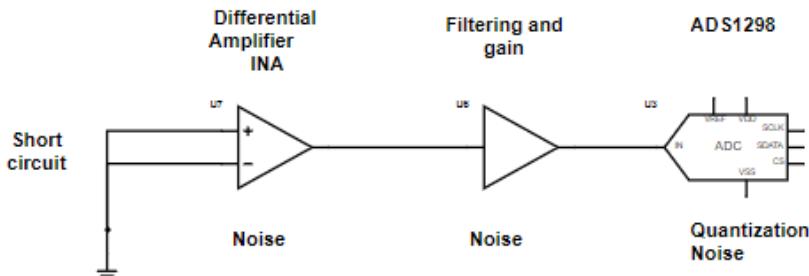


Figure 73 Input referred noise test

The following formula is needed to calculate the IRN of the AFE:

$$IRN_{rms} = \frac{OutputNoise_{rms}}{Gain}$$

6.1.1.3 Practical test

Each AFE prototype will be tested to see how they perform in a practical test. In this test, two types of electrodes were used, a dry and a gel-type electrode. The dry electrode was custom made by a jeweller and is made-up out of 100% silver. For the gel electrodes, the disposable Ag-AgCl electrodes were used. The dry electrodes will only be tested in bipolar configuration and the gel electrodes will be tested both in monopolar and bipolar connection. The subject preparation was performed following the recommendations of the Surface Electromyography for the Non-Invasive Assessment of Muscles (SENIAM) guidelines.

6.2 Results

6.2.1 Input range

Figure 68 shows the results when a 5mV 200Hz signal was applied to the input (REQA-05), where design 2.3 shows the least phase shift and design 2.1 and 2.2 show the most phase shift (expected with the results obtained in the previous paragraph). This measurement confirms that design 2.1-2.4 allow a maximum 5mV input EMG signal without reaching the supply rails (REQA-05).

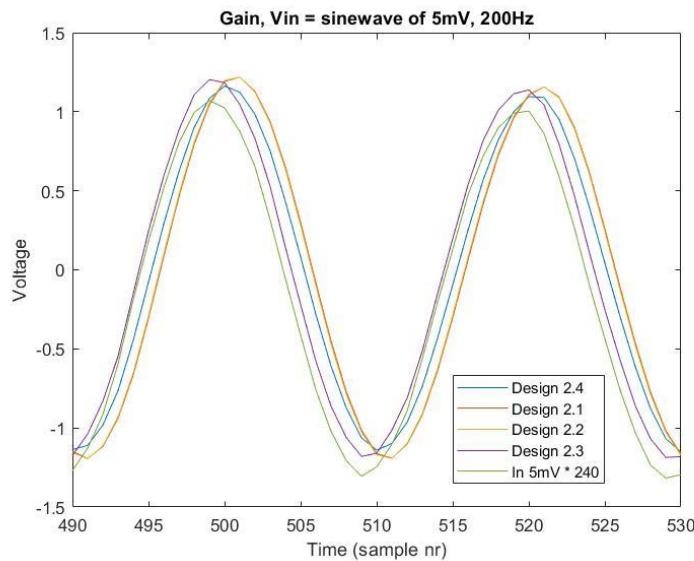


Figure 74 Phase shift and gain of design 2.1-2.4 with an input signal of 5mV 200Hz.

The lower part of the output signal in design 1 was clipped at -0.8V (see figure 69), the same problem occurred when a sine wave of 1Vpp with an offset of 1.65 volt was directly applied to the positive input of the ADS1298 and a dc voltage of 1.65V was applied to the negative input of the ADS1298. The cause of this problem is that the analog voltage rails of the ADS1298 (+/-2.5V) are too low to measure the full dynamic range of the AD8232 (GND - +3.5V). This problem can be resolved by increasing the positive analog supply rail of the ADS1298 to +3.5V and the negative analog supply of the ADS1298 to -1.5V, if these voltages converters are not available +3.3V and -1.8V would be a better option.

The output of design 1 was measured using an oscilloscope to confirm the cause of the signal clipping, the scope result indicated a clear sine wave without any signal clipping. Thus we can conclude that design 1 can tolerate an input signal up to 5mV (REQ-05).

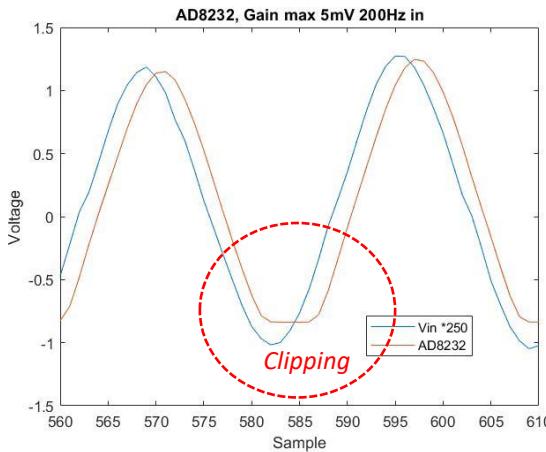


Figure 75 Phase shift and gain signal

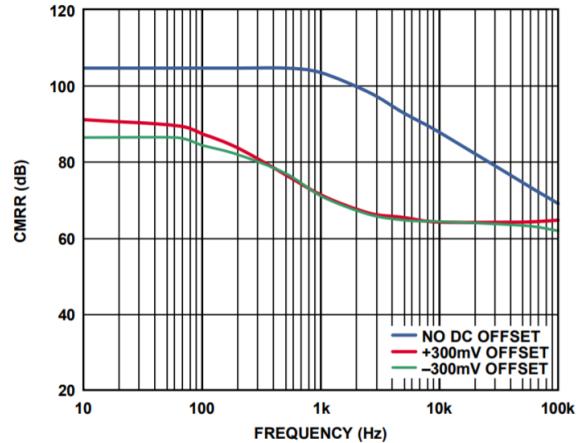


Figure 76 CMRR vs Frequency AD8232 [27]

6.2.1.1 Common-mode rejection ratio (CMRR)

Figure 74 shows the measured CMRR of each design in the frequency range of 10-1000Hz. The measured CMRR of the design 1 (AD8232) is significantly lower than all the other designs (2.1-2.4), it barely meets **REQA-02** (min. 70dB in EMG BW). The datasheet of the AD8232 states that the CMRR should be around the 105dB within the 10-1000Hz frequency range (see figure 76). The first test result of design 1 resulted in a CMRR < 70 dB. A possible cause of the low CMRR was due to the high resistor tolerance of the patient protection resistor of the IA (1%), after improving the resistor tolerance to 0.05% the CMRR improved to just over the 70dB, a small improvement.

Design 2.1-2.4 all use the same IA design. It's difficult to compare the different designs (2.1-2.4) based on the results of one CMRR result test per design. In [10] the CMRR of a similar IA design of a HD-SEMG system was measured using the same method as described in this report, the report states a +/- 10dB around the average CMRR among all the measured EMG channels. Thus the CMRR of design 2.1-2.4 cannot be compared between each other. Instead, it can be used to find the average CMRR among the designs and to be used to compare it against design 1. The average CMRR between design 2.1-2.4 at 50Hz, is 108dB with a minimum of 105dB and a maximum of 112dB. The measured CMRR of designs 2.1-2.4 shows a similar curve to what is shown in the datasheet of the INA333 (or see figure 25). Design 2.1-2.4 meet **REQA-02**.

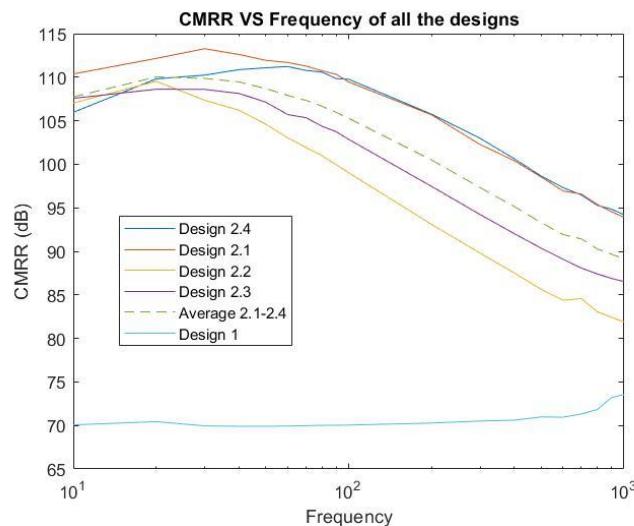


Figure 77 CMRR of the designs measured between 10 - 1000Hz, with a 1Vpp signal applied to both inputs

6.2.1.2 Input referred noise (IRN)

The input-referred noise of each design was measured using the method described in chapter 6.1. Figure 75 shows the measured input-referred noise of each design.

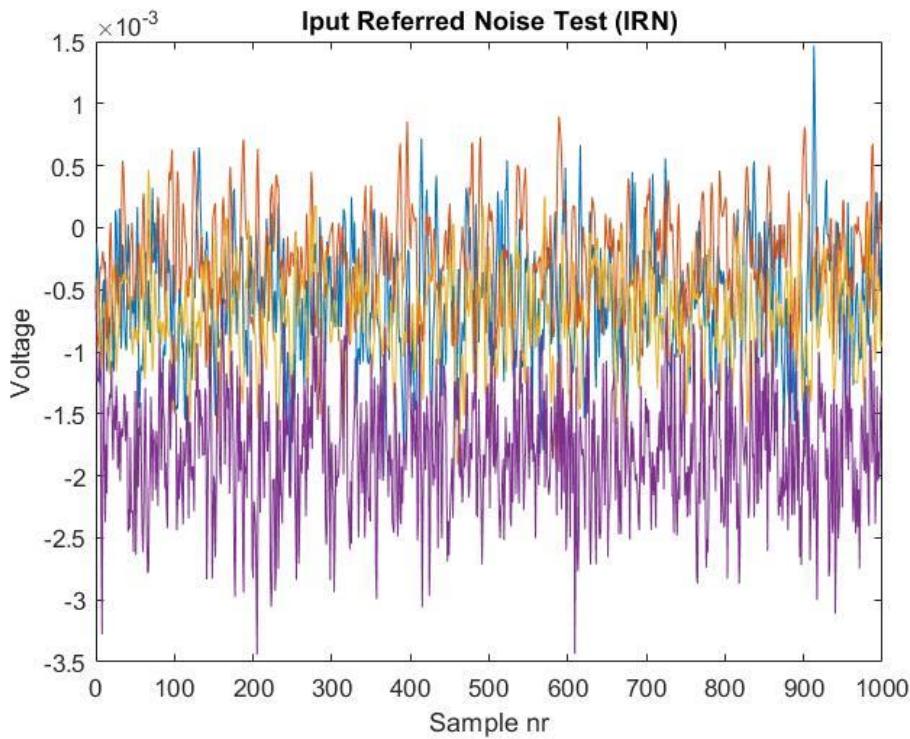


Figure 78 Input referred noise of each channel

Design	RMS out	IRN (μV_{rms})
Design 1	$1.4mV_{rms}$	$5.61 \mu V_{rms}$
Design 2.1	$379 \mu V_{rms}$	$1.57 \mu V_{rms}$
Design 2.2	$385 \mu V_{rms}$	$1.60 \mu V_{rms}$
Design 2.3	$502 \mu V_{rms}$	$2.09 \mu V_{rms}$
Design 2.4	$468 \mu V_{rms}$	$1.95 \mu V_{rms}$

Table 6 Input referred noise results.

Based on the results shown in Table 5, only design 1 would not meet the required input-referred noise requirement of $< 4\mu V_{rms}$ (REQA-04). The lowest IRN was expected at design 2.3 due to the differential configurations, but this was higher than the other design (2.1, 2.2 and 2.4), a possible cause could be the longer traces between the filter outputs and the ADC inputs compared to the other designs. The input referred noise could have been lower if the prototype board was shielded better, e.g. a metal casing.

6.2.1.3 Practical test

6.2.1.3.1 Baseline noise

The baseline noise of each design was measured when the electrode was attached to the body (both in SD and MP configuration), the electrodes were placed on the bicep Brianchii and the reference electrode was placed on the elbow. Using an oscilloscope the source of the baseline noise was analysed (using FFT scope), the source of the noise was identified to be the PLI and its harmonicons (see figure 76).

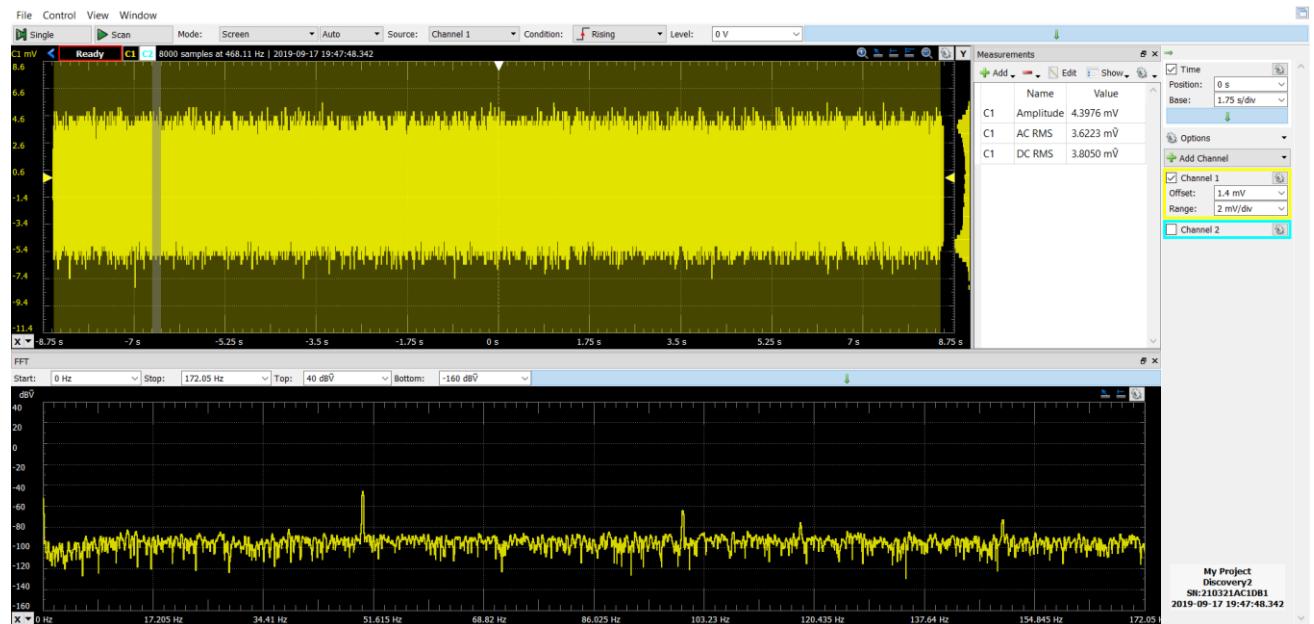


Figure 79 Baseline noise of design 2.1, electrodes in SD configuration

Table 6 shows summary of the baseline noise of each design. The baseline noise is very dependent on how well the skin was prepared before the electrodes were attached to the body.

Design	Baseline noise (mVrms)	
	Single Differential (SD)	Monopolar (MP)
Design 1	6.1	51
Design 2.1	3.6	29
Design 2.2	3.8	28
Design 2.3	3.1	29
Design 2.4	3.6	29

Table 7 Baseline noise summary

When the direct ground method was applied to design in SD mode (connecting the reference voltage output ($V_{CC}/2$) to the reference electrode instead of the RLD output of the AD8232) the baseline noise significantly increased to almost 100mV peak-to-peak (0,034Vrms), see figure 7. A possible cause for this problem is the low measured CMRR of the AD8232. This means that a direct grounding method cannot be used in the AD8232.

6.2.1.3.2 Design 1

Figure 77.1 and 77.2 shows the results of design 1 in SD and MP using gel electrodes. In the results it can be seen in figure 77.2 that the signal EMG output signal is clipped at 0,8V.

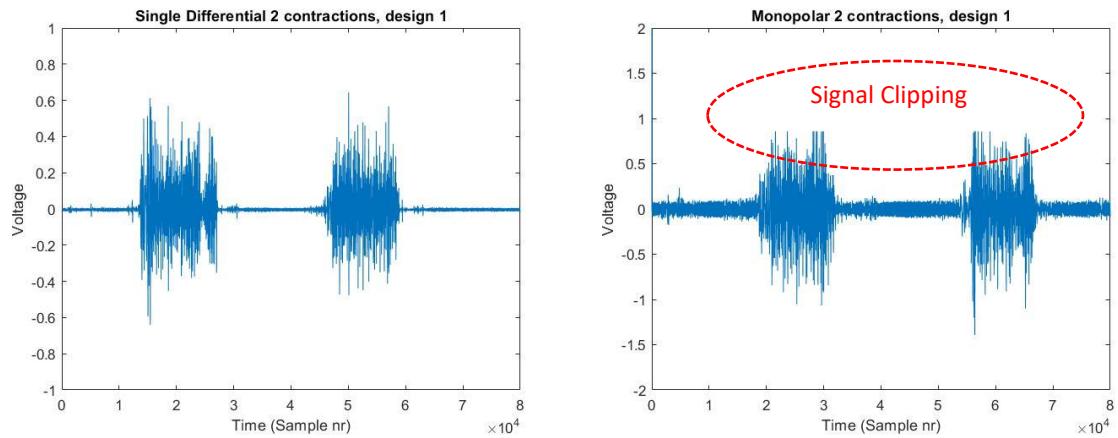


Figure 80 Practical test results from design 1

6.2.1.3.3 Design 2.1

Figure 78.1 and 78.2 shows the results of design 1 in SD and MP using gel electrodes.

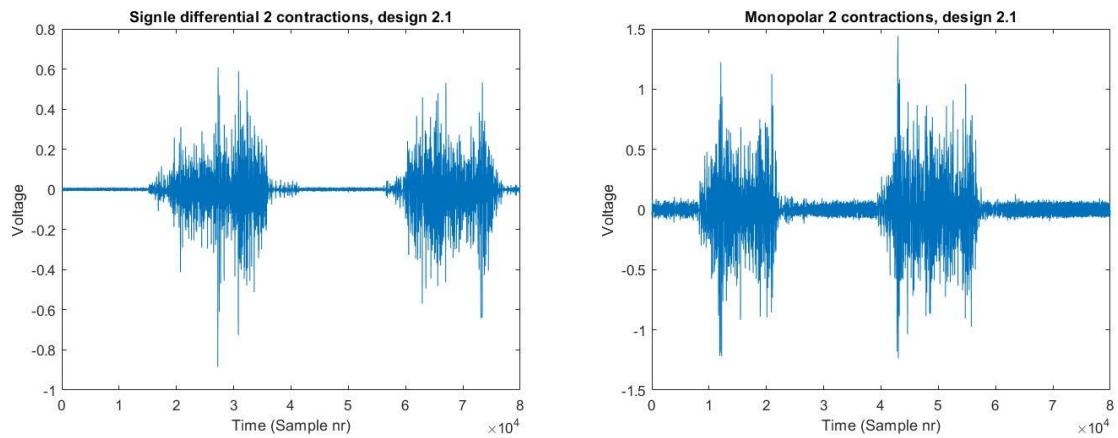


Figure 81 Practical test results from design 2.1

6.2.1.3.4 Design 2.2

Figure 79.1 and 79.2 shows the results of design 1 in SD and MP using gel electrodes.

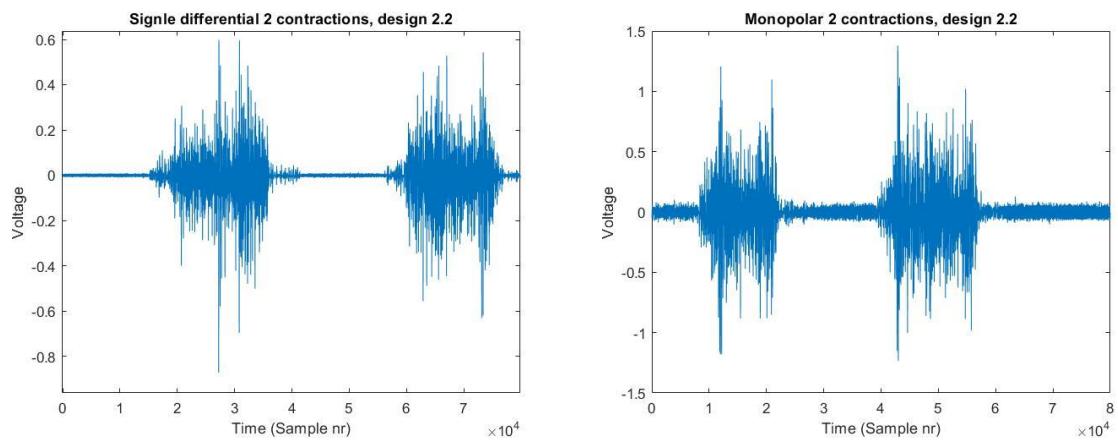


Figure 82 Practical test results from design 2.2

6.2.1.3.5 Design 2.3

Figure 80.1 and 80.2 shows the results of design 1 in SD and MP using gel electrodes.

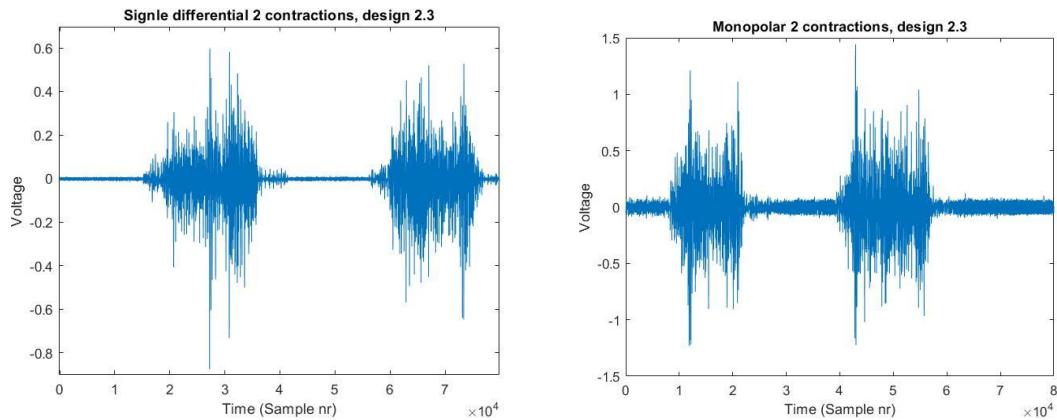


Figure 83 Practical test results from design 2.3

6.2.1.3.6 Design 2.4

Figure 81.1 and 82.2 shows the results of design 1 in SD and MP using gel electrodes.

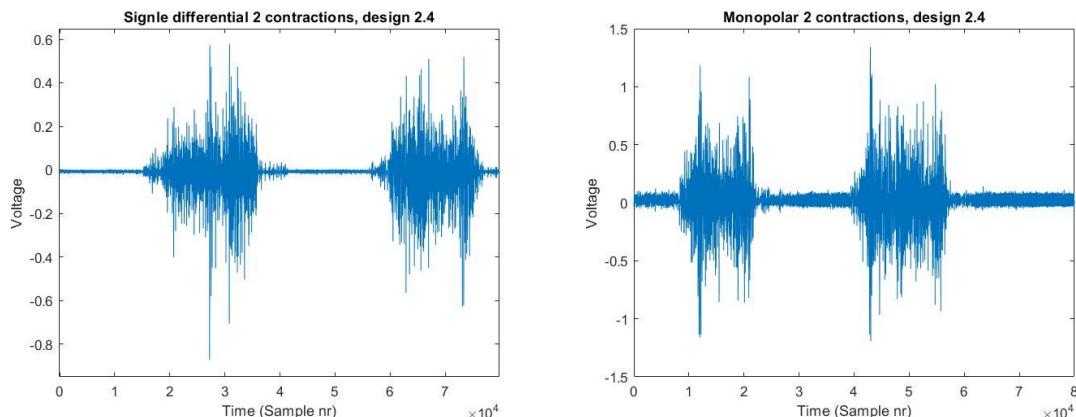


Figure 84 Practical test results from design 2.4

6.2.1.4 Dry Electrodes

When the designs were tested using the dry electrodes, different problems occurred during the testing procedure. It was almost impossible to obtain a stable EMG output signal during the tests. This was probably caused by bad electrode-skin contact, this resulted in motion, and electrode artifacts that caused in the signal to switch between the supply rails or the signal to become corrupted by noise (figure 82). A possible cause could be that the electrode was made out of 100% Silver and not out of Silver-Silver Chloride electrode. The chloride layer would help to reduce these problems.

However, when the electrode obtained a good EMG signal design 2.2 showed lower baseline noise than design 1, this could be due to the higher input impedance of design 2.2 compared to design 1, or it could just be luck. Thus, the results of this test were not taking into account for the choice of the final AFE design.

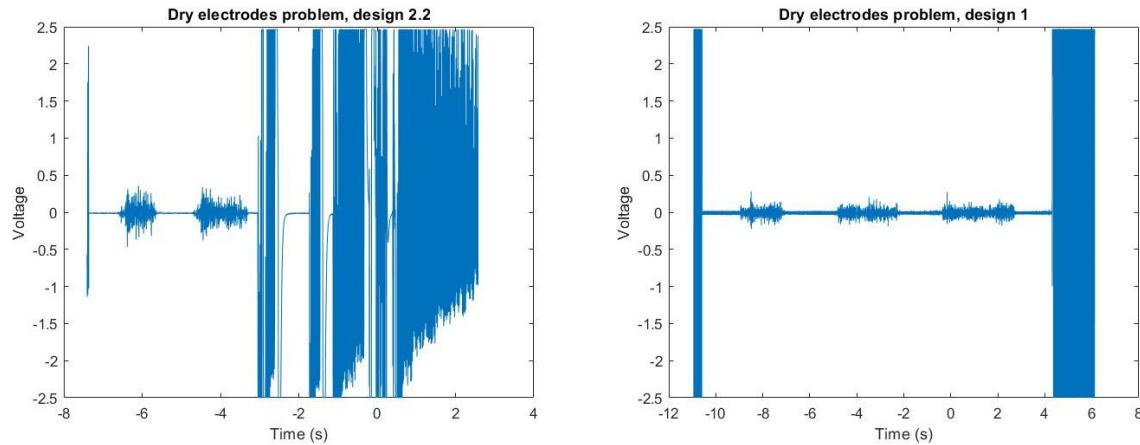


Figure 85 Tests using dry electrodes

6.3 Design 2

As mentioned in chapter 3, the choice for the final AFE design depends on the result of the measured parameters and some additional tests of each AFE design. Based on the result the first design to be eliminated was design 1: Although the design did offer minimal gain error within the EMG BW, the practical test showed very decent results and the low material price (see Table 8), the design was eliminated due multiple reasons: 1) the relatively low CMRR of just 71dB compared to the other designs, 2) an IRN above the maximum allowed IRN of 4 μ Vrms and 3) the high baseline noise in MP configuration compared to the other designs, almost 20mV higher. To obtain a satisfactory result in terms of baseline noise from design 1 the RLD had to be implemented (direct grounding resulted in high baseline noise).

The next design to be eliminated was design 2.4: Although the circuit design was significantly smaller and cheaper than the other remaining designs, this design was mainly rejected due to the high gain error within the EMG bandwidth. Both designs 2.1 and 2.2 are much cheaper and smaller to build than design 2.3. However, they do offer higher EMG gain BW error and group delay compared to design 2.3. As this product will be used mainly for analysing/research purposes, system performance would probably be the most important factor to choose between the different designs. Thus design 2.3 was selected to be used as the AFE design.

	Price
Design 1	6.86€
Design 2.1	12.1€
Design 2.2	9.76€
Design 2.3	15.24€
Design 2.4	5.86€

Table 8 AFE design prices

A new PCB was designed consisting of only design 2.3. The new design is very similar to the design presented in chapter 5.1, the only difference is that instead of the 5 design presented in this thesis a new prototype was developed containing just three EMG channels. The channels are configured as two MP and one MP/SD channel. The two MP channels can be connected to either the inputs of that are connected to the SD inputs or to the MP inputs, using J13 and J14. This allows the user to implement and test a SD spatial filter compared to a SD channel configuration. In the previous design voltages spikes occurred at the signal when a sampling frequency >250Sps was chosen, this problem could partly be caused by incorrect grounding, loop-impedances or by the isolation module. On all the power supply outputs a parallel LC filter was added to reduce these voltage spikes and an EMI filter was added to the isolated power supply. The problems could be partially be resolved by switching to a four layer board. However, due to budget limitation, it wasn't possible to change to a four layer board. The three channels allow to test gain mismatch between multiple recording channels, as this is needed to test.

This resulted in that the board size wasn't significantly reduced compared to the previous design, as room needed to be maintained in between of the AFE designs to provide electronics with power (2 layer PCB, with the top layer being V_{SS}). The new design did allow us to place the AFE and the ADS1298 more closely together, which hopefully improves the test results of IRN to $< 1\mu\text{Vrms}$.

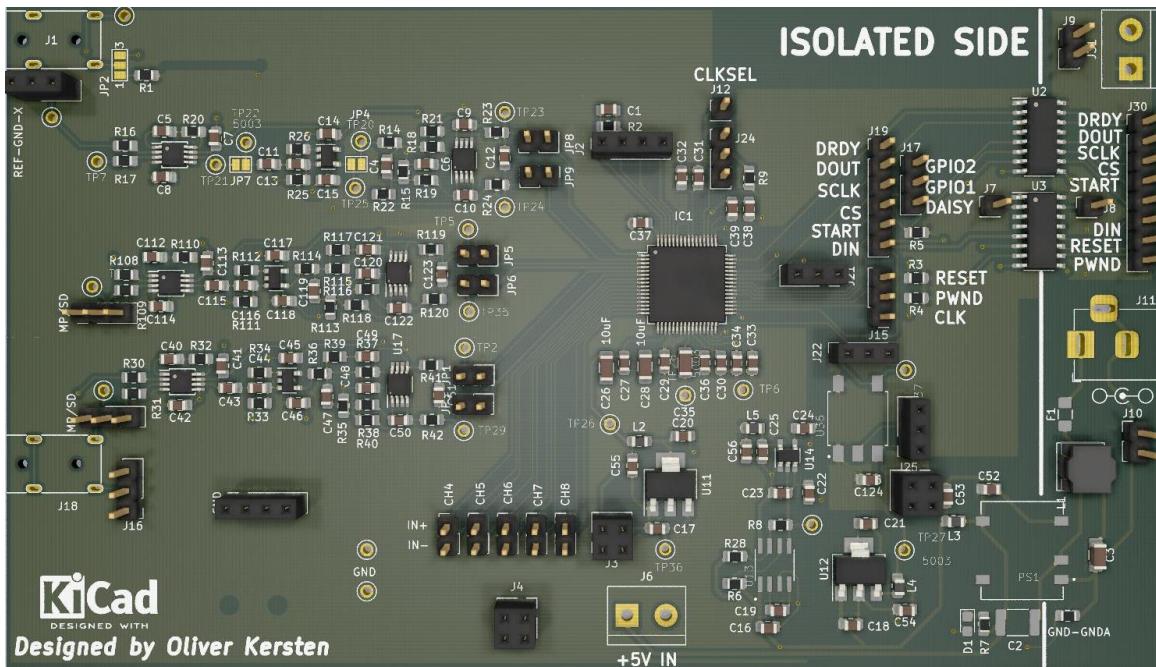


Figure 86 Design V2

The design files can be found in attachment J, under HD_SEMG_prototype_V2. Due to time limitation the new PCB could not be tested to validate if the previous problems related to the voltage spikes were resolved in the new design.

The problem with the voltage spikes was caused by the power supply of the Arduino to power the PCB design 1 (the isolation was not used as this made it easier for testing). When a different MCU was used (STM32F411) the problem was resolved (see code in attachment J). With the STM32F411 another problem was introduced, there were some difficulties with opening the VCP on the PC (in python, but the data can be shown using tera term). The code for the STM32F411 was partly generated in CubeMX, this could be causing the problem with the VCP.

6.4 Price

This paragraph calculates an estimate of the what the final prototype would cost. The total price of a 64 channel monopolar HD-SEMG acquisition:

- 1) AFE: the price of design 2.3 is 15,24€ per AFE, thus the total price would be around the 975,-€ *(64 channels). *note the price of different part used in the AFE (IA, op-amps, resistors and capacitors) would be cheaper when bought in bulk (>10 pieces), the price reduction would be around the 75€ - 150€.
- 2) EMG electrodes: The cost of a button shaped electrode (100% silver) is around the 15€ per electrode (made by a jeweller), 64 electrodes plus the reference and ground electrode would add up to a total of around the €900,- (66*-/+15€). Although other type of electrodes materials would be cheaper, silver was chosen as this has low noise level compared to other electrodes material. The sleeve where the electrodes are placed in costs around the €100.
- 3) ADC: Per 8 EMG channel 1 ADS1298 (ADC) is required, thus a total of 8 ADS1298 are needed, which leads to a total of 280€ (35,4€ per ADS1298)
- 4) PCB: To save space on the final design a 6 layer PCB would be required, as both side of the PCB can be used to solder the AFE design on. The price of the PCB is around the 100€, with additional assembly service costs this would be around the 290€*. *this price was quoted at PCB-gogo, the price is without additional cost to ship the components to the PCB-gogo assembly location.
- 5) Additional parts, e.g. the MCU, USB cable, Isolation, power supply and casing, these costs would add up around the €300.

The total production price of this prototype would be around the €2500, a general rule to convert the production cost in a retail price is to convert the production price by 300-400%, this would mean that the retail price of this product be around the €10k. This value indicated that REQC-01 (material price < €1000) was not achieved during this project. Even when the cheapest option was chosen the price would only be reduced by €500.

6.5 Requirement traceability

Table 7 states a summary of the acceptance test results. Note some requirement where marked red, these requirements were eliminated as certain parts could not be achieved (unit 'measure battery level'). Requirements regarding the total design, e.g. 64 channel electrode, weight and size, were not achieved as a fully working prototype was not developed during the internship due to time and budget limitations. However, the most important requirement where achieved, REQ-A-02.-05, these confirm the system performance.

Specification	Test case	Result
REQA-02: Minimum CMMR > 70 dB within the EMG bandwidth, see chapter 2.	14	v
REQA-03: Sampling rate 2kS/s/ch	16	v
REQA-04: Input referred noise (IRN) < 4µVrms.	15	v
REQA-05: Dynamic input range of EMG signal with an amplitude up to 5mV.	13	v
REQA-08: Minimum operating time of the device is 2-hours on one battery cycle.	-	Was eliminated along with the wireless data transportation, due to simplicity of the current design.
REQA-09: Minimum wireless data transportation range of 2m, from the device to the PC.	-	Was eliminated due to bandwidth limitations of the wireless data transceiver module
REQA-10: Indication that the battery is fully charged.	-	
REQC-01: Material costs < 1000 €	9	x
REQC-02: Device dimensions need to be within 15x10x4 cm.	11	x
REQC-03: Weight < 200 gram.	11	x
REQC-04: EMG electrode size < 10mm diameter	10	x
REQC-05: Inter electrode distance (IED) < 10 mm	10	x
REQC-06: 64 EMG channel	10	x
REQC-07: Electrode configuration needs to be in monopolar	12	v

Table 9 Summary requirements

7 Conclusion and recommendation

7.1 Conclusion

The goal of this thesis was to present a solution to correctly locate the agonist/antagonist of the residual limb where the patient has the most amount of control over during different hand gestures. This should be accomplished by developing a 64 channel HD-SEMG acquisition system with an EMG BW of 10 – 500Hz and a simulations sample frequency of 2kSps/ch. However, this goal has only partly been accomplished. This thesis did not succeed in the development of a fully functional 64 monopolar channel HD-SEMG prototype, but it did succeed in the development of a concept that can be used to develop the desired system. This design concept consists of a IA with a ‘quashi’ high pass filter for dc-offset rejection, followed by a unity gain high-pass filter for additional dc-offset rejection, a MFB FDA low-pass filter for antialiasing filtering, a daisy-chainable 24-bit 8 channel simulations sampling ADC to provide a single data communication line to the MCU for all the 64 channel which will send the data through USB 2.0 to the PC to be visualized. The current design was validated to have the following system specification, see Table 9.

	CMRR (dB)	IRN (μV_{rms})	Gain (V/V)	EMG BW (Hz)	Baseline Noise (mV_{rms}) SD - MP	Input impedance	Sample Frequency Sps/ch	
System specifications	105	2,09	239	10-2000Hz	3,1	29	100GΩ	250

Table 10 Design specification summary

Table 9 states that the system is only capable of sampling frequency 250Sps/ch. The design is capable of sampling at 2kSps/ch. However, the data obtained at this frequency is corrupted by voltage spikes measured by the ADC inputs. This is most likely caused by improper isolation of the analogue voltage supply of the ADC. Thus a new solution should be found to solve this problem, so that the design is capable of a sampling frequency larger than 250Sps/ch.

7.2 Recommendations

The hypothesis where this thesis is based on "The performance of direct control be improved by correctly the locating the agonist/antagonist of the residual limb where the patient has the most amount of over", should be adequately validated using existing equipment before a fully functional prototype is developed in the next stage. This can be accomplished by developing a PC application that can communicate with existing HD-SEMG systems, e.g. OT bioelettronica offers MATLAB communication with almost all their products (see their website for source codes). In MATLAB a custom GUI can easily be designed to verify if the hypothesis is correct.

If the hypothesis is confirmed, the following system improvements are recommended:

- *The dc-offset suppression can be further improved by lowering the G_{ina} (gain will be compensated in the MFB filter). By lowering the G_{ina} the zero cut-off frequency can be increased to above the 1Hz (depending on the capacitor value choice) compared to the 0,6Hz in the current design. To maintain high CMRR at 50 Hz (>100dB) the G_{ina} should not be lowered below the 10 V/V. The THS4521 would not be affected by this change as it offers a slew rate up to 490 V/ μ s which is well within the required slew rate.*
- *As the ADS1298 offers a built-in RLD circuit to improve the rejection of common-mode signals. It should be validated if the baseline noise could be further reduced using the RLD compared to the direct grounding method implemented in the current design.*
- *A possibility is to replace the current design (AFE & ADC) with a RITAN HD2164 module, this is a 64 channel ASIC, this module comes in a package size of only 7.0mm x 9.0mm at a price of roughly €400,-. This would significantly reduce the current board size and cut the material cost of the project by more than a half. There are some disadvantages about this module, 1) the lower CMRR of 81dB, 2) the lower input impedance (10G Ω) and 3) the BGA packaging makes it almost impossible to solder this module by hand. This module would make the design more compatible with current solutions such as the OT BIOELECTRONICA Sessantaquattro (a 64 channel SEMG amplifier with a size of 96x60x20mm), whereas the design presented in this thesis is nowhere near this size. Further research should be conducted to verify if this module is capable of being used in this application.*
- *The ideal inter-electrode distance (IED) of the grid placed around limb should be carefully investigated, in regards to how this correlates with the IED of Ottobock 12E200 electrodes.*
- *Use a battery to provide the isolated side with power instead of the isolated dc/dc converter, this could prevent the voltage spikes from occurring on the signal.*

If the hypothesis of this thesis turns out to be wrongful or has minimal performance improvement, the design could be used to develop an MPR system, as there is a much larger demand and a market for and the current design has no USP compared to similar products already on the market. As Bionic hands are nowadays designed with more degrees of freedom (DOF), that allows the user to perform a very broad range of hand gestures, including wrist flexion. One major problem with DC systems is that the user needs to perform co-contractions over the selected pair of channels to switch between different hand gestures. To overcome these problems myoelectric pattern recognition systems (MPR) have been developed. MPR systems use machine learning algorithms to recognize patterns of muscle activation enclosed in the EMG signals and to decode the hand gesture intention of the user. This method provides a much more intuitive control to the user. To date, there are a few commercially available MPR systems (Complete control COAPT and Ottobock Myoplus).

A relatively big problem with current MPR systems is it's the unreliability. Unintentionally patients contract different arm muscles very lightly during movement, which can be recognised by the MPR system as the user wanting to perform a hand gesture. This can lead to the bionic hand suddenly opening whilsts a cup of coffee is being held. An excellent solution to this problem would be to design a versatile MPR/DC system. So the user can access the best of both worlds when needed, that is DC control during highly reliable tasks and MPR when

the user wants to switch easily between different hand gestures. The versatile MPR /DC system should be based on design 1 as the AFE. As this design is the smallest (using the alternative package AD8233) and provides good EMG bandwidth gain error.

Further testing should be conducted to find a method of how multiple RLD of design 1 can be combined together, as if the direct grounding method would be used due to its simplicity the SNR of the EMG signal would be unacceptable. The battery management system presented in this thesis could be used in the MPR system.

The next person to continue with this project has the choice to continue with either one of the two suggest solutions, which could be based on the confirmation of the hypothesis. In my opinion, I would recommend proceeding with the development of a versatile MPR/DC system, as there is a bigger market for and the current HD-SEMG system has no USP compared to other product on the market.

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Attachment A: Method of Approach

A.1 Introduction

A myoelectric prosthesis is an artificial limb that uses myoelectric signals to control its function, this could be a bionic hand, arm, knee or ankle. The most common application for myoelectric prosthesis is lower arm prosthesis (bionic hands) in patients with a transradial amputation (congenital disability or as a result of a trauma). These individuals often retain much of the extrinsic musculature of the forearm that is typically used to control the hand and wrist. Flexors and extensors of the limb are used to generate independent electromyographic (EMG) signals to control the motors inside the hand. Each EMG signal is rectified, smoothed and a threshold value set to activate the motor in one or another direction to open or close the bionic hand. The speed of the motor can be proportionally controlled, by considering the amplitude of the EMG signal (the higher the amplitude, the faster the motor turns). This method is also known a direct control or 'DC'. The most commonly used EMG electrodes inside myoelectric prosthesis are the Ottobock® 13E200 electrodes, and most prostheses consist of two EMG electrodes.

The placement of the EMG electrodes inside the prosthesis starts by placing the electrode over agonist/antagonist residual muscle pairs on the limb. Using an analysing tool (Ottobock MyoBoy®) the place of the electrodes and the gain is adjusted until an independent signal above the threshold value is acquired per electrode during different hand gestures. The problem with this method is that the place of these EMG electrodes is based on a trial and error method and the place where the patient has the most control over the agonist/antagonist may never even be found. This could result in a less satisfactory experience of the myoelectric prosthesis.

The goal of this thesis is to design a product that is capable of visualizing the electrical potential distribution (EMG) generated by all limb' muscles during different hand-gestures. This can be accomplished by developing an HD-SEMG acquisition system, containing a large number of EMG electrodes densely placed together (more about this will be explained further on).

Different systems on the market exist that are already capable of obtaining HD-SEMG measurements. However, these systems are not portable, wireless, or use semi-adhesive electrode (which can cause skin irritation, that can be prevented with dry electrode). This thesis intends to tackle these issues in a new design. We do not intend to design a new method for measuring EMG signals but use existing designs to develop our own system. As this thesis forms the beginning of this project, this thesis will mainly focus on the design and development of the hardware for this system.

A.2 Project activities

To successfully design this project, this project is divided into 6 phases:

1) Initiation phase

In this phase, a global idea of the to design project is developed.

2) Definition phase

This phase will start by defining all the requirements of the system based on the client's needs. An acceptance test is written, this test document specifies how the system requirements can be tested to validate the performance of the system.

3) Design phase

This phase will start with the design of an architecture model, this model is based on the requirements made in the previous phase. The architecture model presents a global overview of all the system parts (units). After the architecture model is finished an integration test document needs to be written. This document specifies how all the units are integrated together. Process specifications are given to each unit and the unit is further developed into schematics and flow

diagrams. A unit test document is written, this document specifies how the unit can be validated if meets the process specifications. The next step is to make a detailed design of all the units, this can include a simulation, schematic, PCB or a flowchart.

4) Realization phase

In this phase the designed had/soft-ware is realized, PCB are soldered and software is coded.

5) Testing Phase

In this phase, all the written test documents are executed, starting with the unit test, followed by the integration test and as last the acceptance test. If a test fails the unit has to be re-designed in order to meet these requirements.

6) Presentation phase

The final documentation of the project is finished and a presentation is given about the developed product.

A.3 Project quality

It is very important that during this project, the design process is done according to the V-model. This model limits the room for any mistakes. In the beginning, it is essential to document the design process thoroughly, as this helps to find the cause of a possible error in a further stage of the process. This means that choices for specific designs and parts need to be documented. The made documentation must be checked by someone else, so see if it's clear what the writer of this thesis means and if it is correctly designed. The mindset of 'I have enough time, I can do it later' could occur, but this needs to be avoided as the manufacturing and integration of parts can take longer than expected. The fastest things are done the better it is.

A.4 Project Border

To set the project borders a Moscow analyse is made.

Must	Should	Could	Won't
Universal, the fitting around the arm needs to be able to fit around different sized limbs, as each amputation or deformity makes the limb very different.	A wireless connection to a PC	Measured data visualised on a 3d model of the limb	Needles to obtain the EMG signal from the limb
Visualize data on a 2D model.	The casing around the electronics	Show the patient which movements he needs to make	Use of single-use electrodes (stickers) and the help of conductive gel
Grid mapping of EMG signals > 64 electrodes		LDC to indicate battery level and connection to other devices	
Rechargeable dry EMG electrodes			

A.5 Tasks

In the project, the following part needs to be made:

- **Documentation:**
 - A) Method of Approach
 - B) Requirement and acceptance test
 - C) Research report: High-density surface EMG, monopolar or bipolar configuration, and what the effect of this is on dry EMG electrodes.
 - D) Architecture and integration test
 - E) Unit test
 - F) Detailed design report
 - G) Final report

- **Project design:**
 - A) EMG circuit
 - B) User interface
 - C) Short Circuit protection
 - D) Battery charging circuit
 - E) Measurement circuit
 - F) Wireless data transportation

A.6 Organisation

Contact details of the involved parties of the internship

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Phone number	-

University details

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Telephone number:	-

A.7 Costs and benefits

In Table 1 a cost overview of this project is presented. The advantage of this project is that the student will obtain the last 30 ECTS to get his electrical engineering degree. The benefit for the market is that the prosthesis can better locate the optimum location for the EMG electrode in the prosthesis.

Table 11 Price indication to develop a HD-SEMG system

Part	Amount	Price (€)
Opamps/IA	20	500
Bluetooth module	2	10
PCB	-	250
FPGA/Micro-controller	1	100/20
Pins/buttons	100	30
Wires	5m	150
Battery	1	10
Resistors, capacitors, LED crystals	-	25
Socket liner	1	100
Total		+/- 1000 €

A.8 Risks analysis

This chapter will list possible problems that may be faced in this project, a possible solution is given to minimise the consequence of these problems.

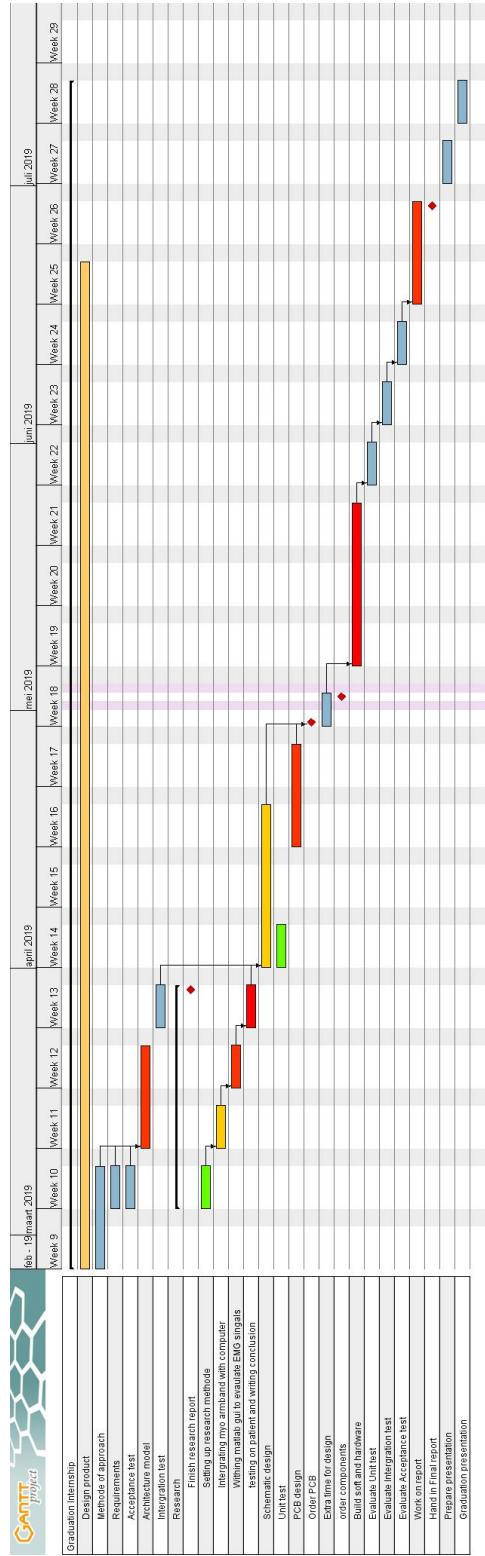
Legend: C = chance, I = impact, E = effect.

Tabel 2 Risk assessment

Risk	C	x	I	=	E	Solution	C	x	I	=	E
Unrealistic goal	2		2		4	Consolidate with the boss or other employees if your wishes and ideas are realistic to design.	1		2		2
Lack in knowledge when building project	2		2		2	Make excellent documentation, with flowcharts, circuits and above all do good research. Ask other employees for help.	1		2		2
Part not on time finished	2		3		6	Make a good planning where there is room for mistakes.	2		2		4
Sickness	1		3		3	Make planning with sufficient time extra time to allow sickness.	1		2		2
Parts not available	2		3		6	Buy part from a well known dealer, such as Farnell or mouser, because of the fast delivery time, the parts are mostly available with correct documentation and footprints.	1		1		2
Fault in design of PCB	1		3		3	Test designed circuit if possible first on breadboard of copperplate.	1		1		1

A.9 Planning

The planning of this project is presented in figure 76.



Attachment B: Data flow diagram

Data flow diagram

B.1 Process signal:

The sub-system of 'Process signal' can be further developed into five sub-systems. This process starts by removing noise from the signal, e.g. power line interference, motion artifacts, high-frequency noise. This step will be done using digital signal processing techniques. The next step, a spatial filter will be applied to the data, this will enhance the EMG signal source. There is also a possibility not to apply a spatial filter. The next step is the calculate the amplitude of the EMG signal by calculating the Root-mean-Square of each recording channel. The final step is to combines all the calculated amplitudes of each channel into an image map to the prosthesis.

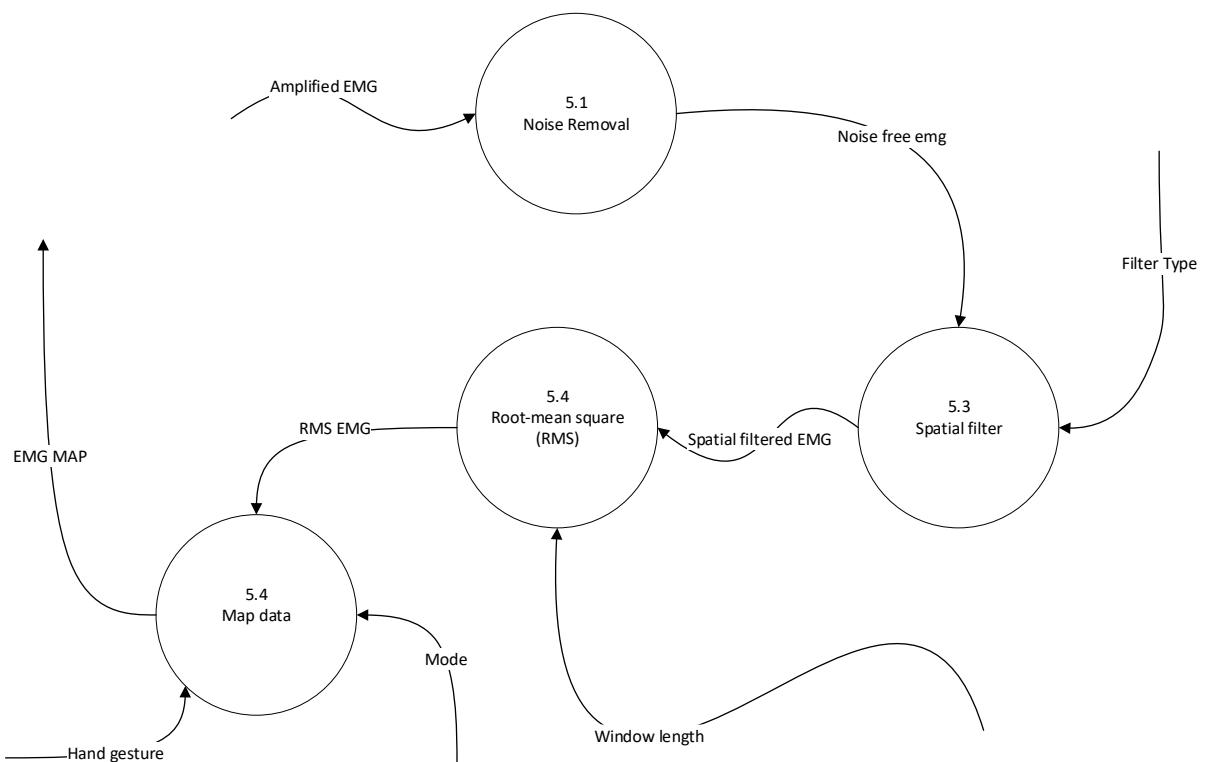
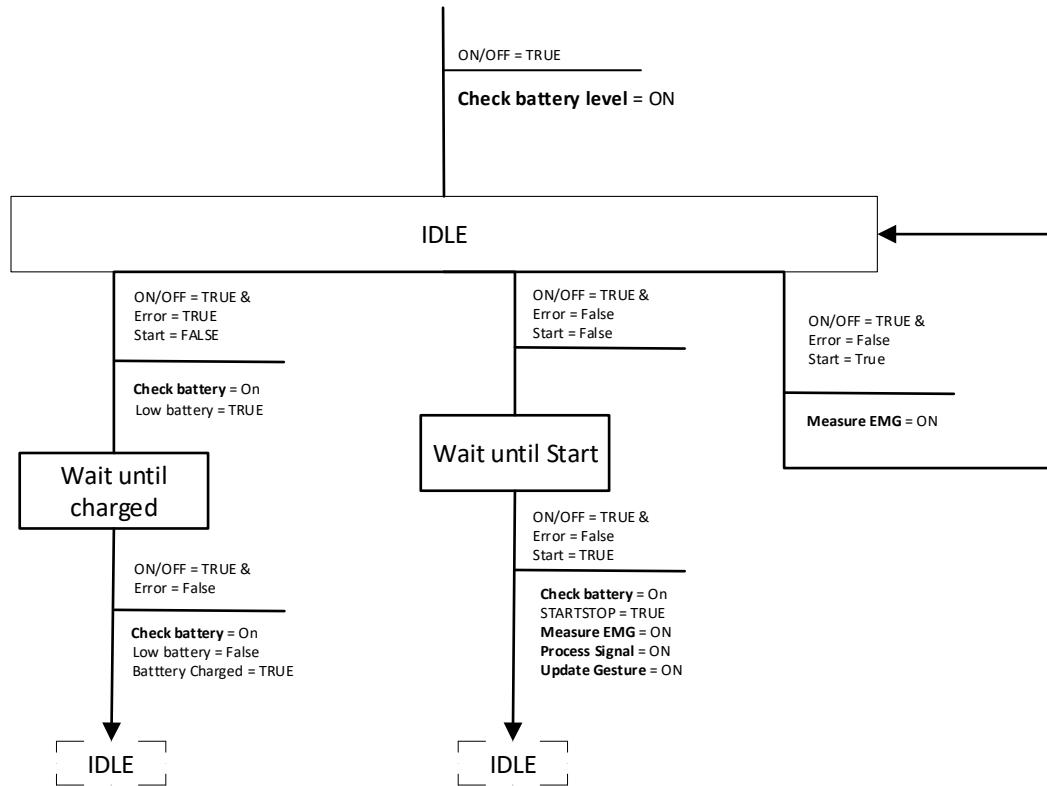


Figure 88

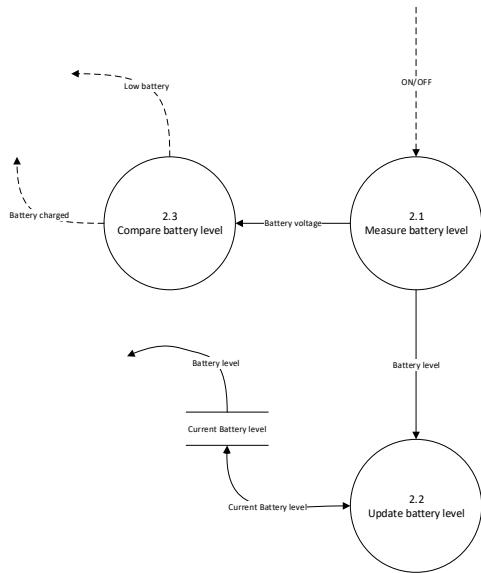
B.2 Mange system

Mange system will tell the user if all the system parameters are correct to start a new measurement session.



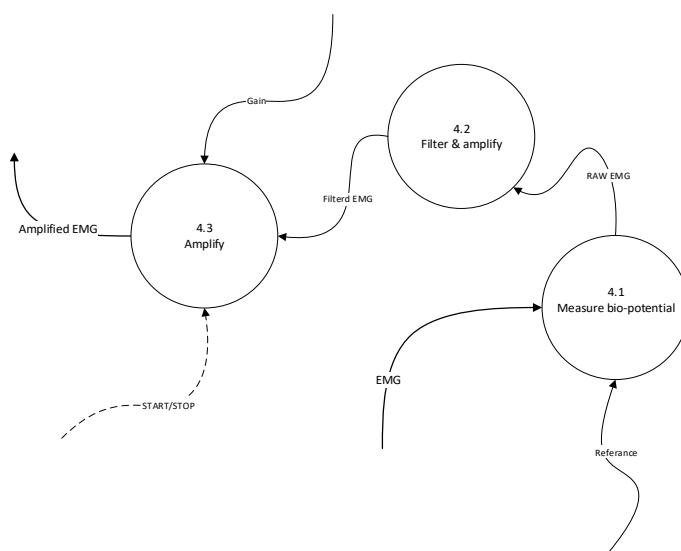
B.3 Measure Battery level

The function of 'Measure battery level' is to constantly monitor how capacity is left in the battery. If the battery capacity drops below a specific capacity the user will be alerted to charge the battery (<10%). Once the battery is fully charged the operator will be notified that the battery is fully charged.



B.4 Measure EMG

The function of the unit 'measure EMG' is to obtain, filter and amplify the EMG signal. Process 4.3 is an optional gain selected by the user ranging from 1-4x.



B5: Change gesture

This unit will update the gesture the patient needs to make, only if gesture mode was selected (MODE = 1), otherwise this unit disabled. A timer will check if the time set by the user (flow 'hand gesture time') has passed, if the time has passed the output (low 'Time passed') change form logic level (0 to 1 and vice versa). If unit update gesture receives a change on the flow 'Time passed' the unit will update the current displayed gesture to the next gesture.

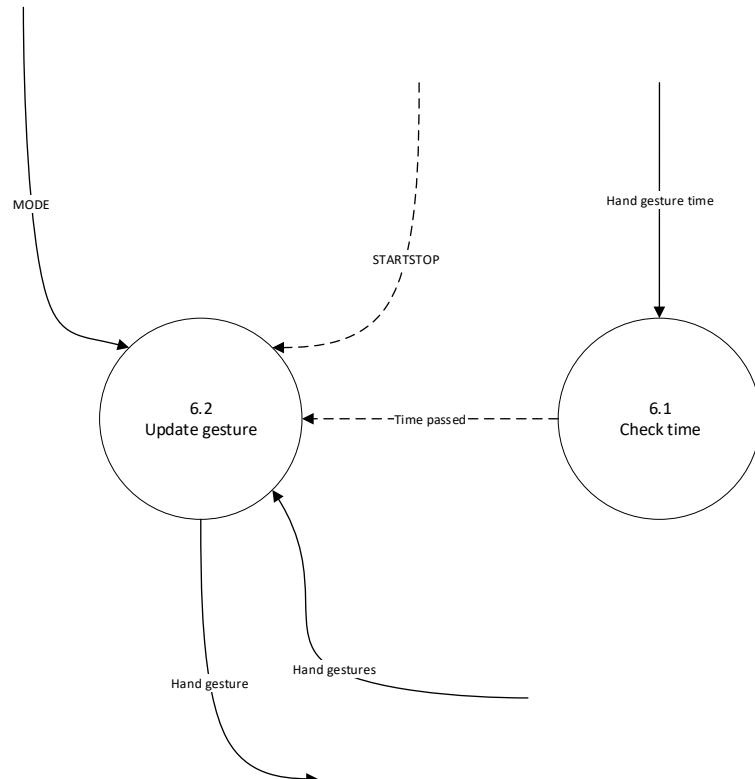


Figure 89 Change gesture

Attachment C: Unit 'Measure battery level'

The function of the unit 'measure battery level' is to monitor the current battery level and to provide the circuit with an isolated power supply. A block diagram of the unit is described in figure 17.

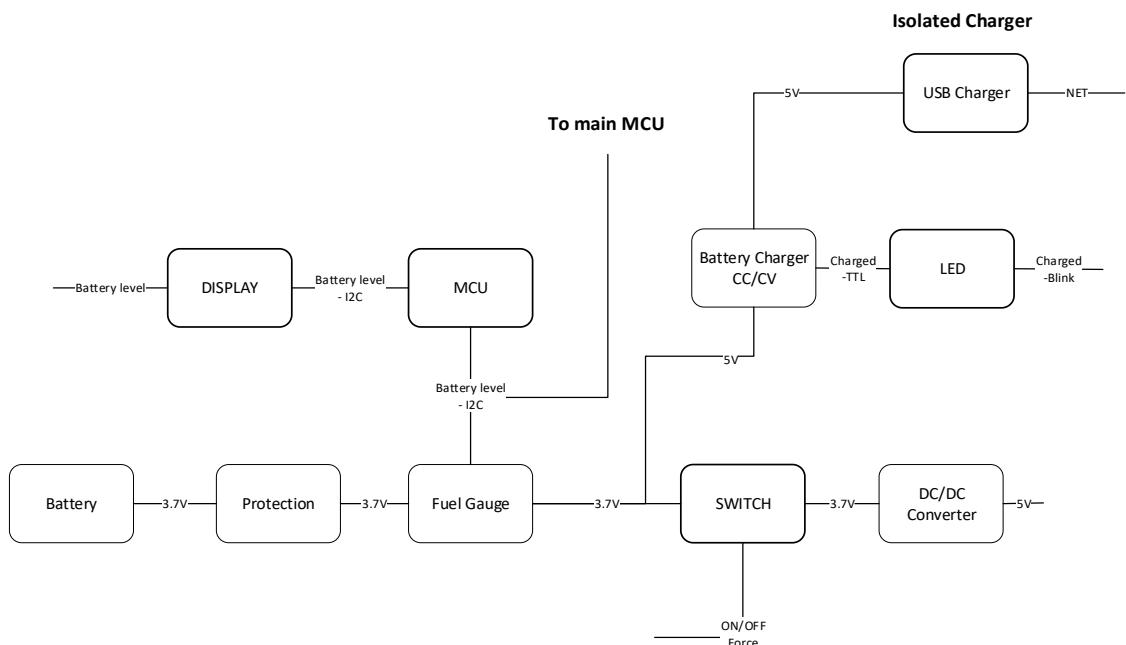


Figure 90 System block of measure battery

The following specification were given to unit 'measure battery' level:

- PSPEC-2.1: Short-circuit protection
- PSPEC-2.2: Battery over-charge and over-discharge protection (See battery type: 2,8V and 4,2V)
- PSPEC-2.3: Battery charge current of 300mA
- PSPEC-2.4: Battery fully charged indication (4,2V)
- PSPEC-2.5: Efficiency of > 80 %
- PSPEC-2.6: Output voltage of 5V
- PSPEC-2.7: Output current of 300mA.
- PSPEC-2.8: Battery capacity is displayed in %
- PSPEC-2.9: Output 'Battery level' is measured in %, with a range of 0 – 100% (100% battery is fully charged, 0% battery empty). The allowed tolerance is 2%.
- PSPEC-2.10: The measured current needs to be measured in mA, with a significance of 2 decimals and an allowed error of 2%.
- PSPEC-2.11: The measured accumulated current needs to be measured in mAh, with a significance of 2 decimals and an allowed error of 2%.

A full description of how these parameters will be tested and the results are described in the unit test document (attachment C).

C1.1 Battery

Rechargeable battery types available on the market are Lead-acid, Lithium-Ion (Li-Ion), Lithium-polymer (Li-po) and nickel-metal hydride (NiMH). The use of Lead-acid battery for this project is not considered any further as these batteries are cheap. However, they are not suited for a portable project due to their enormous size.

The lion and Li-po batteries both require a constant voltage/current method to charge them.

REQA-08 states that the device needs to have an operating time of at least 2 hours on one battery cycle and REQA-07 states that the device current consumption should be below 300mA. With these two values, the batteries' capacity for this project can be calculated with the following formula:

$$Q = t \text{ (hours)} * A \text{ (mA)} = 300 \text{ mA} * 2h = 600mAh$$

In the lousy scenario, the efficiency of the device would only be 50%, with the following formula the new needed capacity can be calculated.

$$Q_{new}(mAh) = \frac{Q_{old} \text{ (capacity in mAh)}}{n \text{ (efficiency in %)}} = \frac{600mAh}{0.5} = 1200mA$$

Thus for this device, a battery with a capacity of 2000mA would be needed to meet REQA-08.

In table 7 a comparison between Li-po, NiMH and li-Ion batteries is made. The Li-Ion battery has the highest battery capacity volume and at the lower price. For this reason, a Lion 18650 battery with a nominal voltage of 3,7 V and 2600mA was chosen.

Table 12 Battery types

Battery Type	Price	Voltage	Size (width, length, Height)	Capacity	wH/kg
Lion	5,95 €*	3.7V	18mm x 18mm x 65 mm (18650)	2600mA	90 – 110
Lipo	4.95 €*	3.7V	26.5mm x 36,9 mm x 5mm	400mA	130- 200
Lipo	12.95€*	3.7V	5.6mm x 49.2mm x 68.8mm	2Ah	130 - 200
NiMH	3.25€*	1.2V	Type AA	4100mA	55 - 65

*All prices are from sparkfun.com

C1.2 Protection circuit

As mention in the previous paragraph Li-Ion batteries are very sensitive to over(dis)charging and short-circuiting, without proper protection of these parameters, the battery will be damaged with a possibility even to explode. Thus an adequate protection circuit is included in this design to protect the Li-on battery from possible damage.

The datasheet of the 18650 Li-Ion battery states that the battery should not be charged over 4.2V, discharged below 2.8V, charged with current 0.52A (optimal) and not be discharged with a current higher than 2.6A. Following these requirements, the AP9101C was selected. The AP9101 offers overcharge protection of 3.5V to 4,5V, under-voltage protection of 2V to 3.4V and short circuit protection. The AP9101C offers 2 built-in comparators that check if the battery voltage is below or above the over-discharge voltage threshold (ODV) or the overcharge voltage threshold (OCV). If the battery voltage drops below or rises above these voltages levels, the outputs DO (gate control for discharge) and CO (gate control charge) change in logic level, this results in one of the MOSFETs being turned off which will interrupt the current flow.

For the MOSFET transistors, the ECH8693 (dual N-channel MOSFET) was chosen due to its small size.

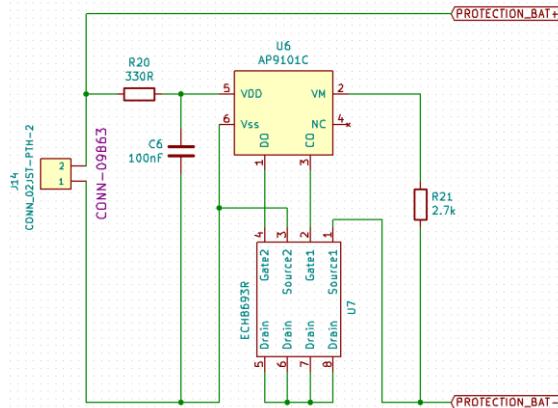


Figure 91 Battery protection circuit, the label on the schematic are outputs of the circuit protection, the JST connector is the battery input

C1.3 Fuel gauge

The function of the fuel gauge is to monitor how much capacity is left in the battery (system function: measure battery level 2.1 in chapter 2.1.1.2), to prevent the system from shutting down due to lack in power. For the fuel gauge, the DS-2745 was selected due to its low cost, single-cell operation and its universal capability to be used with different battery types. The DS2745 can measure four battery parameters, the temperature (IC), voltage, current-flow (both directions) and the accumulated current. The accumulated current is the amount of current that has entered or left the battery over a specific amount of time. The current measurement and the accumulated current (coulomb counting) are accomplished by measuring the voltage drop over the sense resistor (R6 figure x) between the SNS and VSS pin. The MCU can access these parameters via the I2C protocol.

Figure 50 shows the circuit of the DS2745. The inputs PROTECTION_BAT- and PROTECTION_BAT+ are connected to the battery cells positive and negative sides, and the output +BATT is connected to the circuit positive supply. The output SCK and SDA are connected to the MCU. A debug header is included into the circuit to verify if the data obtained by the MCU corresponds to the send data by the DS-2745.

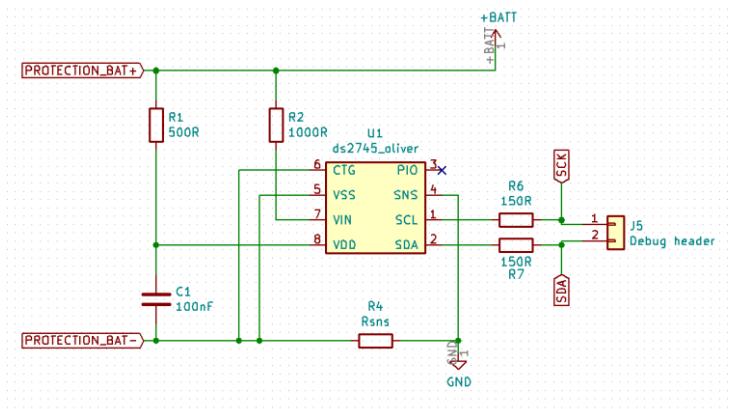


Figure 92 Fuel gauge circuit

C1.4 Battery charger

The MCP73831 is a Li-Ion/Li-Po CC/CV battery charger. For the USB connection, a USB type C adapter was chosen, due to its simplicity for the user as this adapter type doesn't have a top or bottom side. The MCP73831 offers programmable charge current from 15mA up to 500mA. The charge current was calculated in (6), this formula is derived from [].

(6)

$$I_{reg} = \frac{1000V}{R_{prog}} \gg R_{prog} = \frac{1000V}{I_{reg}} \gg \frac{1000V}{300mA} = 3.3k\Omega$$

The MCP7318 contains a status pin. The status pin has three different stages, H(High), L(Low) and High Z (High Impedance). If the battery is charging (not full) the status pin will be in stage L(Low), this will turn on the LED1. When the battery charging is complete (battery voltage > 4,2V) the status pin will be H(high), this will turn on LED2. If no battery is attached to the circuit the status pin will be High Z, this means that both LEDs will burn moderate.

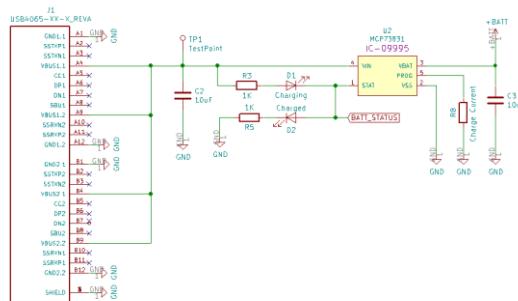


Figure 93 Battery charger circuit

C1.5 DC-DC converter

The function of the DC-DC converter is to provide the circuit (AFE, ADC and MCU) with a stable output voltage from the battery, as the battery's voltage varies between the 2.8 and the 4.2V. For the DC/DC converter a switch-mode power supply (SMPS) was chosen over a LDO-converter, as the SMPS offers much higher efficiency (> 90%) For the SMPS the TSP61090 was chosen as it allowed a vast input voltage range (1.8V-5V) whereas other SMPS (TPS61090) only allows a 10% range around a fixed input voltage (3.3V). This range wouldn't cover the battery voltage range of the li-ion battery (2.8 – 4.2V). The TSP61090 offers a low-battery indication (LBO), for example, alert the user of a low battery.

The datasheet of the TSP61090 offers a circuit design with all the capacitor, inductor and resistor value calculated, only the feedback resistor (R3, R4) for the output voltage needs to be calculated. The output voltage is calculated in (7).

$$R3 = R4 * \left(\frac{Vo}{Vfb} - 1 \right) = 200k * \left(\frac{5V}{500mA} - 1 \right) = 1.8M\Omega \quad (7)$$

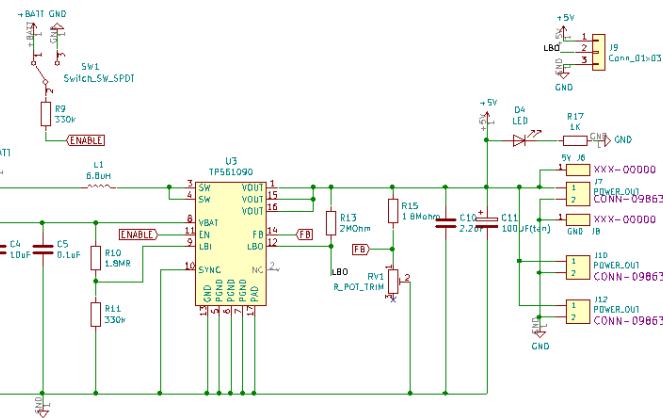


Figure 94 Circuit SMPS

C1.6 MCU & display

The function of the MCU is to read the data from the fuel-gauge and show the data on the OLED display.

There are three types of displays suitable for this project LCD, OLED and E-paper displays. E-paper display are displays that mimic the appearance of ink on paper. These displays can be found in an e-reader like the kindle or the Kobo. The advantage of this display is its low power consumption and its ability to view the display at any angle even in sunlight. Even when the power to the display is disconnected, the text on the display doesn't disappear. The disadvantage of this display is that takes a very long time to refresh the page. As much as the interesting features of the E-paper display, the OLED display was chosen due to its much smaller size (0.66 inches to 1.54 inches of E-paper). The size of the display is an essential factor as we only have to display the current battery capacity, thus don't need much space. An OLED display with a size of 128 by 32 pixels (0.91 inches) was chosen.

For the MCU the ATTiny-85 was chosen, due to its low power consumption ($300\mu\text{A}$), small package size (QFN), low cost and the low number of digital pins (only 5 digital pins).

Figure 4 shows the circuit used for the display and the ATTiny-85.

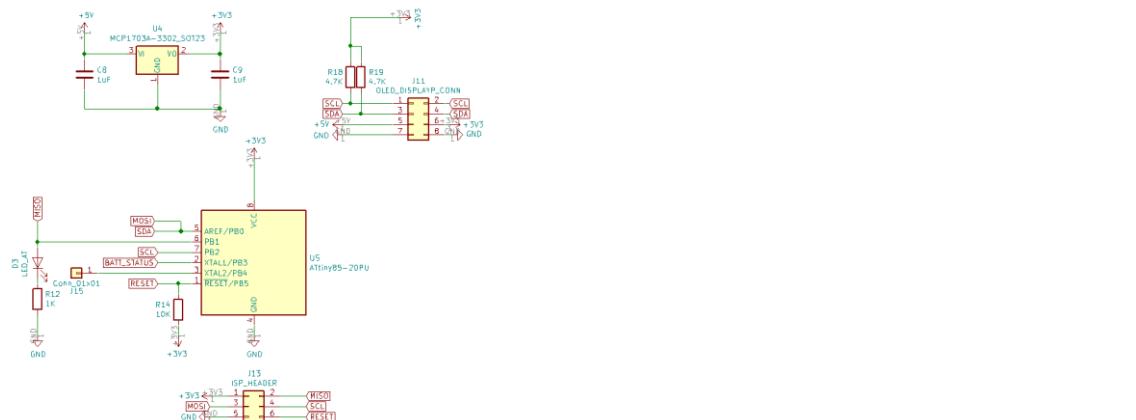


Figure 95 MCU battery management system

C2 Detail design

The unit was designed into the following schematics, See full schematics in attachment D.

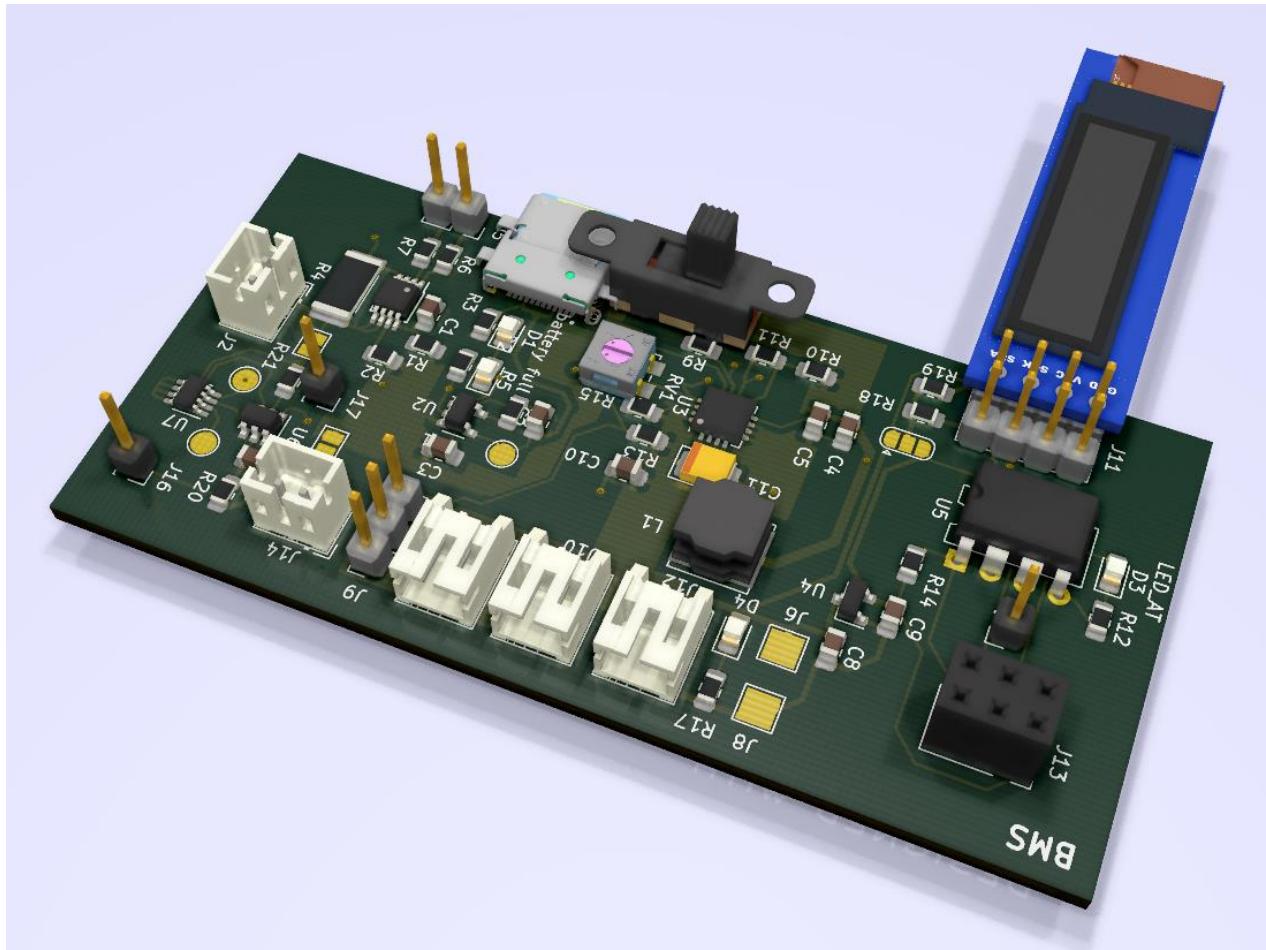


Figure 96 PCB design unit 'Mange battery'

C3 Software

C3.1 Measure Battery level

Although in the previous chapter the measure battery level was removed from the design, the software will still be explained in this part as it was developed prior to the knowledge of the wireless data connection could not be implemented.

C3.1.1 Fuel gauge

C3.1.1.1 Data registers

Figure 59 shows the I2C read protocol of the DS-2745. The protocol is used by the MCU to read register data from the DS-2745 starting at MAddr. Data0 represents the data in register MAddr, Data1 represents the data in MAddr + 1 and DataN represents the last byte read by the host.

```
S SAddr W A MAddr A Sr SAddr R A Data0 A Data1 A ... DataN N P
```

Figure 97 Protocol DS-2745 read register [34]

A list of all the data register of the DS-2745 is shown in figure 51.

ADDRESS (HEX)	DESCRIPTION	READ/WRITE	POR DEFAULT
00	Reserved	—	
01	Status/Config Register	R/W	1100000b
02 to 08	Reserved	—	
09 to 0D	Reserved	—	
0A	Temperature Register MSB	R	
0B	Temperature Register LSB	R	
0C	Voltage Register MSB	R	
0D	Voltage Register LSB	R	
0E	Current Register MSB	R	
0F	Current Register LSB	R	
10	Accumulated Current Register MSB	R/W	No Change
11	Accumulated Current Register LSB	R/W	No Change
12 to 61	Reserved	—	
61	Offset Bias Register	R/W	00h
62	Accumulation Bias Register	R/W	00h
63 to FF	Reserved	—	

Figure 98 Data registers DS-2745 [34]

The following section will explain how real battery parameters (mV and mA) can be obtain from the register values:

1) Voltage

To obtain the measured voltage in mV of the voltage registers (0x0C and 0x0D) the following conversion has to be used:

$$Voltage (mV) = (uint16_t)(Voltage\ MSB \ll 3)|(Voltage\ LSB \gg 5) * 4.88$$

To obtain the voltage in V, the combined register value need to be multiplied by 0,0048.

2) Current

To obtain the measured current in mA of the current registers (0x0E and 0x0F) the following conversion has to be used:

$$Current (mA) = (uint16_t)(Current\ MSB \ll 3)|(Current\ LSB \gg 5) * 0,0015625 / Rsns$$

Where $Rsns$ is the resistance value of the current sense resistor.

3) Accumulated current

To obtain the measured current in mA of the accumulated current registers (0x10 and 0x11) the following conversion has to be used:

$$Accumulated\ Current (mA) = (uint16_t)(Current\ MSB \ll 8)|(Current\ LSB) * 0,00625 / Rsns$$

For a detailed explanation about the used formulas we suggest you read to datasheet of the DS-2745.

C3.1.1.1 Write DS-2745

The accumulated current register is an up/down counter holding a current count of charge stored in the battery, this register allows to read or written by the host. This accumulated current register can store an accumulated current starting at 0000h until FFFFh. To insure that both limits are not reached, the register needs to be set to the battery capacitance of the used battery.

The following steps are needed to set the Accumulated current register to the battery's capacity:

1) Convert the battery capacity into an accumulated current value:

The total accumulated current is stored into a 16-bit value. The following conversion is used to obtain the accumulated current register value with the known battery capacity (2.6A) and Rsns (in our case 10mΩ).

$$(uint16_t)ACR_{value} = \text{round} \left(\frac{\text{BatteryCapacity} * \text{Rsns}}{0.00000625} \right)$$

2) Divide into two bytes:

The Accumulated current is stored into two 8-bit registers (address 0x10 and 0x11), thus the 16-bit value needs to be converted into two bytes that can be written into this register. This can be done with the following manner:

$$\text{Lower_ACR_Byte (LSB)} = (\text{uint8}_t)(ACR_{value} \& 0xFF)$$

$$\text{Upper_ACR_Byte (MSB)} = (\text{uint8}_t)(ACR_{value} \gg 8)$$

3) Write bytes to register

The last step is to write the bytes into the correct registers. In figure X the write I2C data protocol for the DS-2745 is shown. Data0 represents the data written into MAddr (register address), Data1 represents the data written into MAddr + 1 and DataN represents the data written into MAddr + N. The master indicates the end of the write transmission by sending a STOP command after receiving the last acknowledge bit.

This means that the following protocol will be used to write the ACR register: Start, SAddr (0x90), MAddr (0x10), Data0 is *Upper_ACR_Byte* and Data1 is *Lower_ACR_Byte* and as last the STOP will be send.

S SAddr W A MAddr A Data0 A Data1 A ... DataN A P

Figure 99 I2C protocol [34]

C3.1.1 OLED display

The OLED display is controlled by the SSD1306, the SSD1306 on his turn controlled by a host (μ C) via the I2C or SPI protocol. There are 2 important registers that are used to control the SSD1306, the command register (80h) and the data register (40h). The command register is used to set different setting on the OLED display, e.g. the contrast, memory addressing mode or to turn the display ON or OFF. The data register is used to control the pixels on the OLED display, e.g. to turn a pixel ON or OFF.

These register can both be accessed using the following I2C protocol.

S	Slave Address	W	A	Register Address	A	Data Byte	N	P
	0x3C	1		0x40 or 0x80				

The OLED display contains 128 horizontal pixel by 32 vertical pixel. The vertical pixels are divided into 4 pages with each page segment containing 8 pixels (figure X). The segments on each page are turned ON or OFF by send a byte to the data register (40h), e.g. when 01h is send the first pixel will be turned ON and when FFh is send all the pixels in that segment will be turned ON.

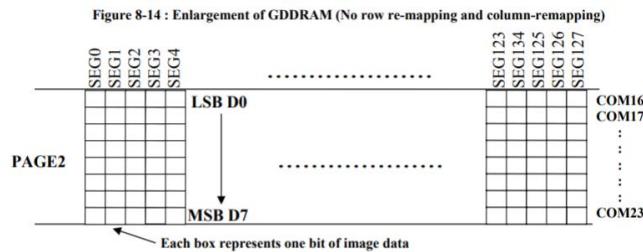


Figure 100 OLED display pixels [35]

C3.1.1.1 Initialize display

The SSD1306 is able to control different sized OLED displays, thus the SSD1306 must to be initialized to match the setting of the used display size. Flow-diagram in figure 20 initializes the basic configuration of the used OLED display (128x32) via the I2C protocol, this flow diagram is based on the example flow diagram in the datasheet of the SSD1306, however additional features such as brightness were left out as these were not needed in this application. A detailed description about all the registers can be found in the datasheet [3].

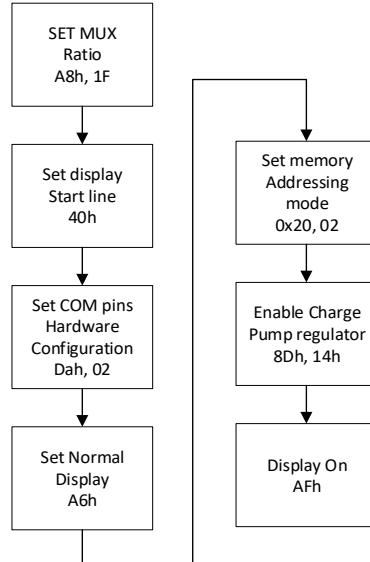


Figure 101

C3.1.1.1.2 Display visualized

The display will be programmed to display 4 battery parameters on the display, on each page a single battery parameter will be displayed. On the first page the battery voltage (mV), the second page the current flowing in/out of the battery (in mA), the third page the accumulated current (how much capacity is left in the battery in mA) and on the fourth and last page the current battery percentage (0 – 100%) will be displayed. A prototype of this display design is shown in figure 28.



Figure 102

C3.1.1.1.2 Software

In this section the micro-controller code will be described that is used to display the battery percentage on the display. The flow diagram was worked out in C-code in Atmel Studio 7, see attachment J.

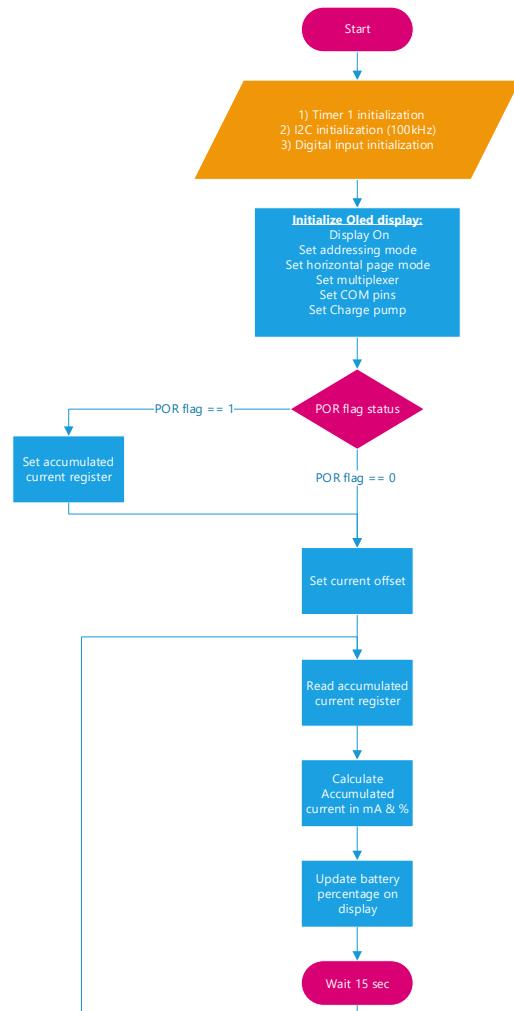


Figure 103 Flow diagram read battery parameters.

Attachment D: Price calculation of the designed AFE

The price of each AFE design was calculated, see table 5 (see attachment C for full description). In the filter stages of each design capacitors with an X7R series were used (10%) and for the resistor, a tolerance of 0,1% was used to minimise differences between recording channels.

Design 1

Part	Price (€)	number	Total
AD8232	3.09	1	3.09
Gain Resistors	0.71	1	0.71
Gain Capacitors	0.57	1	0.51
Filter Resistors	0.30*	5	1,80
Filter Capacitors	0.434;0.165	1,2	0.764
Total			6,874 €

Design 2.1

Part	Price (€)	Number	Total
INA333	3.77	1	3,77
OPA333	2.21	2	4,42
Gain Resistors	0.71	1	0.71
Gain Capacitors	0.57	1	0.51
Filter Resistors	0.30*	6	2,1
Filter Capacitors	0.188;0.109	2,2	0.594
Total			12,1 €

Design 2.2

Part	Price (€)	Number	Total
INA333	3.77	1	3,77
OPA333	2.21	1	2,21
Gain Resistors	0.71	1	0.71
Gain Capacitors	0.57	1	0.51
Filter Resistors	0.30*	5	1,8
Filter Capacitors	0.434;0.165	1,2	0.764
Total			9,764 €

Design 2.3

Part	Price (€)	Number	Total
INA333	3.77	1	3,77
OPA333	2.21	1	2,21
THS4521	2,92	1	2,92
Gain Resistors	0.71	1	0.71
Gain Capacitors	0.57	1	0.51
Filter Resistors	0.30*	10	3,0
Filter Capacitors	0.188,0.338,0.469,0.136	2,2,2,1	2.12
Total			€ 15,24

Design 2.4

Part	Price (€)	Number	Total
INA333	3.77	1	3.77
Gain Resistors	0.71	1	0.71
Gain Capacitors	0.57	1	0.51
Filter Resistors	0.30*	1	0.30
Filter Capacitors	0,571	1	0.571
		Total	5,86 €

Table 13 INA333 circuit price

Attachment E: Useful links

Useful links:

Programming of the ADS1298:

SAM3X8E ADS1298 ECG shield (Arduino code not working, but can be used for flow diagram):
<http://openelectronicslab.github.io/OpenHardwareExG/>

Teensy 3.2 ADS1298ECG-FE module interface:

<https://www.mccauslandcenter.sc.edu/crnl/open-source-eegecgemg>

<https://os.mbed.com/users/vinajarr/code/TEST-ADS1298/file/7087441eb776/Source/ADS1298/ADS1298.cpp/>

https://flex.flinders.edu.au/file/08b2128d-31c2-4765-862c-8c3e2b2439a2/1/Scheina%20Thesis%20Edited%2002_01_2018.pdf

<http://michals-diy-electronics.blogspot.com/2018/06/hello-world-with-ads1298.html>

<https://e2e.ti.com/support/data-converters/f/73/t/758923>

<https://github.com/Serj1032/STM32F4xx-ADS1298/blob/master/Src/ADS1298.c>

Programming of STM411 micro-controller:

<https://forbot.pl/blog/kurs-stm32-f4-1-czas-poznac-hal-spis-tresci-kursu-id14114>

Appendix F: Test document

In this document lists the test procedures of the acceptance test (system requirements), integration test and the unit test (unit specifications) and the results of these tests. This document will start with the unit-test, followed by the integration test and finally the acceptance test (V-model)

F1 test preparations

To perform the test correctly the following hardware and software is required.

F1.1 Test environment 1

For this acceptance test, a room with the following dimensions is needed: 5x4x3m.

F1.1.1 Hardware preparations

The following hardware is needed to perform the acceptance test:

- 1) Function generator, minimum specs: signal generator form 0.1Hz to 1Mhz, signal offset 0-5V, resolution >14Bits
- 2) Oscilloscope, minimum specs: bandwidth 10Mhz.
- 3) Logic analyser, minimum specs: > 10Msps.
- 4) Power supply, minimum specs: 0-5V, 0-2A.
- 5) 2 Probe connectors.

In this project, the listed hardware above was all combined into one hardware module, the Diligent analog discovery 2. The Analog discovery 2 is a PC based oscilloscope, with waveforms (a pc application) the measured data is visualized. Waveforms offers built-in functions such as voltmeter, power supply, network analyser, oscilloscope, waveform generator, logic analyser, impedance measurement, spectrum analyser and a pattern analyser. The Analog discovery 2 offers a 14-bit oscilloscope and waveform generator resolution, 100MS/s, 30MHz bandwidth oscilloscope and a 12Mhz bandwidth waveform generator. The Diligent Analog discovery 2 was expanded with the BNC adapter module, see figure x.

- 6) 3 digital multimeters, minimum specs: voltage > 5V, current >2A and resistance 1 to 1M. In this test, the Uni-t UT58A was used.
- 7) A Ruler, 30 cm (displayed in mm)
- 8) Scale
- 9) Measuring tape, minimum length is 5 meters.
- 10) Board to board wires.
- 11) Atmel ICE and USB cable.
- 12) USB charger socket and a micro-USB and USB-C cable.
- 13) A PC or laptop
- 14) EMG electrodes
- 15) EMG connection cable
- 16) MMB0 motherboard of TI

F1.1.1 Software preparation

The following software is needed to perform the acceptance test:

- 1) On the PC or laptop, the following software must be installed: Atmel studio 7, Waveforms, MATLAB, Analyzer2Go and Teratherm, Microsoft Excel, ADS129XECG-FE firmware, evaluation software designed in the project (eval_EMG.m).

F2 Unit Test

This chapter describes how all the unit were tested to validate if they meet the unit specifications.

F2.1 Measure EMG

Summary of all the unit specifications of unit 'Measure EMG'.

PSPEC1: FRS is 5V

PSPEC2: $G_{AFE\ EMG\ BW} = 250\ V/V$

PSPEC3: Variable gain 1-4x.

PSPEC4: AFE_{BW} 10 – 500Hz.

F2.1.1 Test case 1

F2.1.1.1 Specification

In test case 1 the following specifications will be tested.

PSPEC2: $G_{AFE\ EMG\ BW} = 250\ V/V$

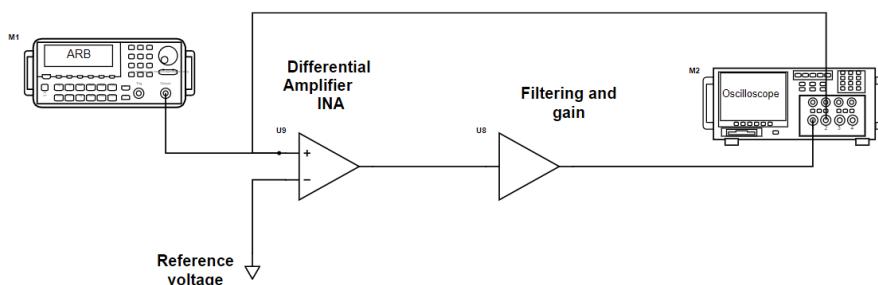
PSPEC4: AFE_{BW} 10 – 500Hz.

F2.1.1.2 Test criteria

For PSPEC2 an error of 5% is allowed to pass this test, for PSPEC4 an error of 30% is allowed in the lower BW (7-13Hz) and a 10% error is allowed in the upper BW (450-500Hz).

F2.1.1.3 Test Procedure

Connect the output of the waveform generator to the positive input of the INA333 and connect the negative input to ground. Next connect channel 1 of the oscilloscope to the output of the waveform generator output (use a BNC splitter connector) and connect the channel 2 of the oscilloscope to the output of the circuit.



As explained in the introduction, the Digilent analog discovery 2 will be used as a waveform generator and oscilloscope in this test. Connect the device to the PC via the USB connector and the probes as explained in the previous section.

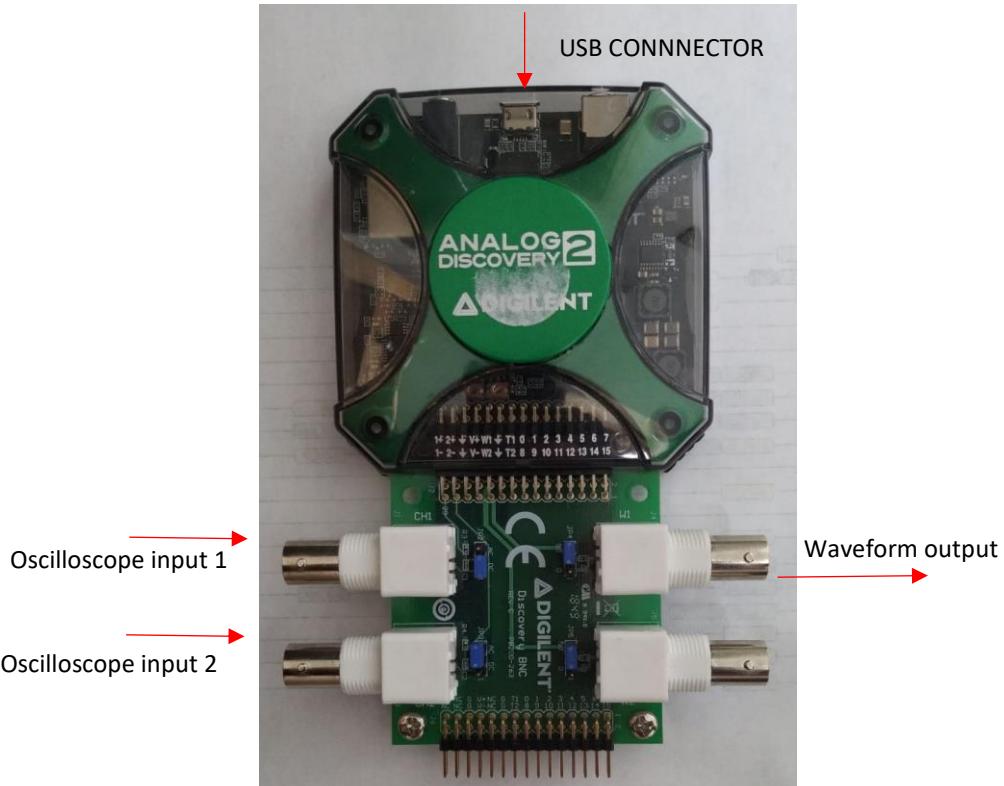


Figure 104 Analog discovery 2

Open waveform 2015 on the PC and open the network analyser.



Figure 105 Waveform home screen

Network analyser tool:

- 1) Set the frequency range of the network analyser, set the frequency range from 100mHz till 10kHz, and set the number of samples to 201 (40dB).
- 2) Set the waveform of the waveform generator to 10mV with no offset.
- 3) Set the magnitude and phase limits. Set the magnitude limit from -50dB to 50dB and the Phase limit from 0 to 360 degrees with no offset.
- 4) Start the measurement session by clicking on the 'single' button.
- 5) Wait until the measurements session is done
- 6) Click on the tab 'file', go to export and export the data to a .csv format and give the file a suitable name

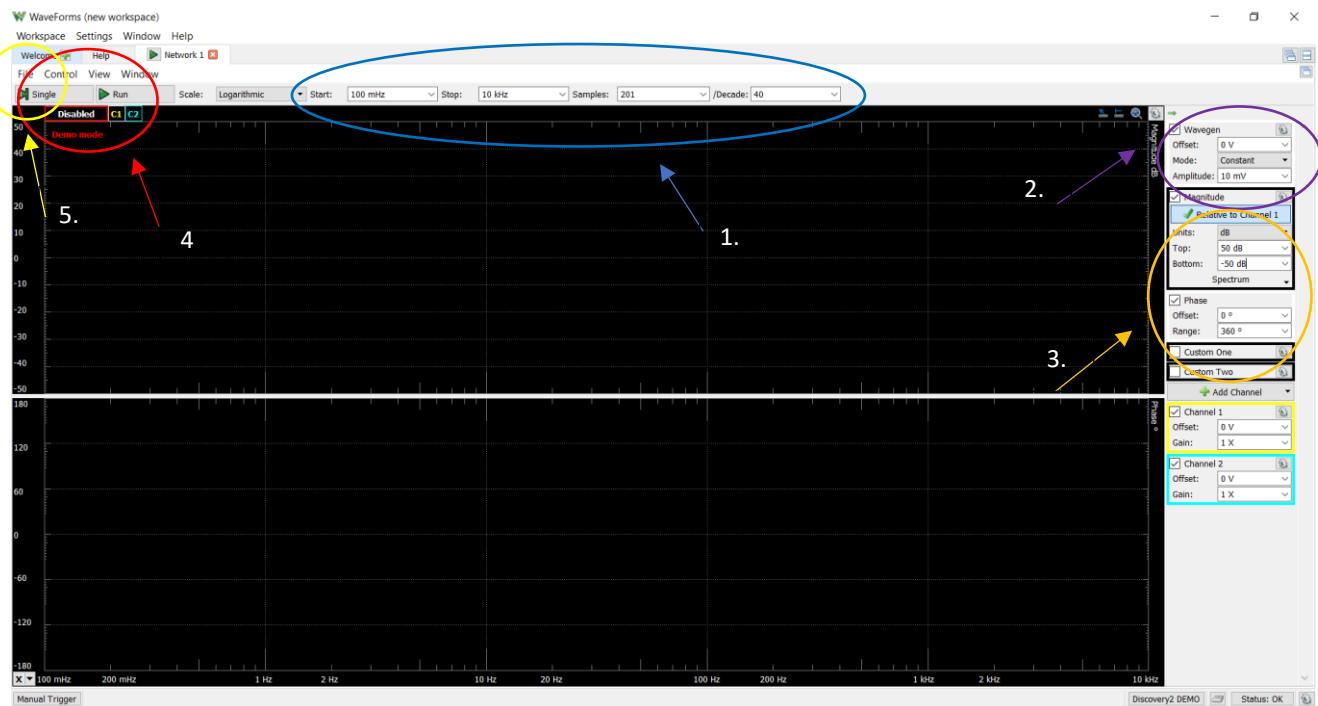


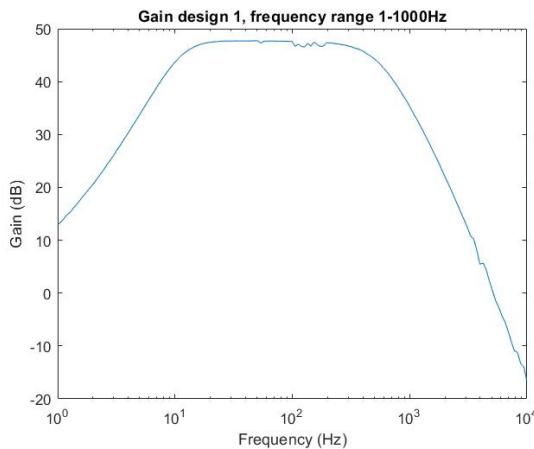
Figure 106 Network analyser Waveforms

Open the .csv file in MATLAB and use the frequency_phase_plot.m and plot the data to a figure.

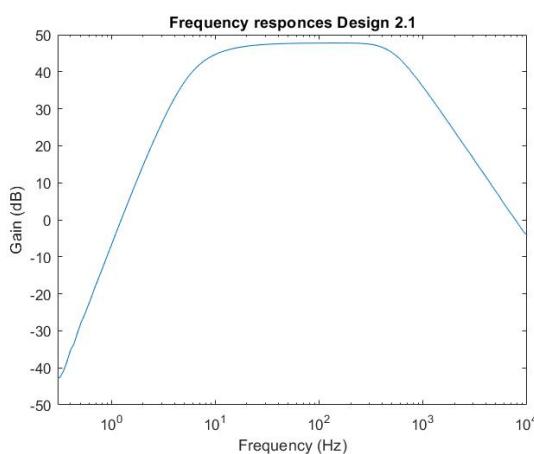
F2.1.1.4 Results

Result: see each design.

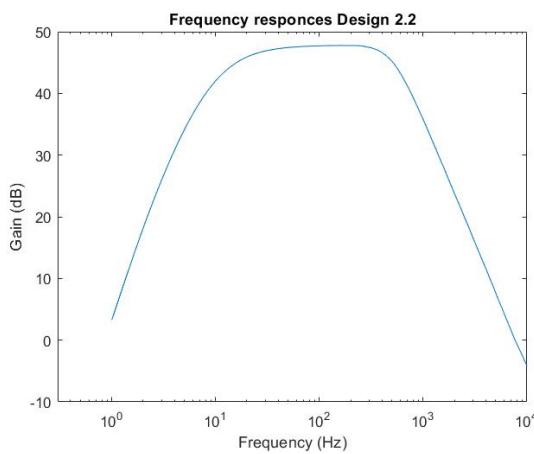
Design 1: $G_{AFE\ EMG\ BW} = 248\ V/V$, $AFE_{BW}\ 11 - 500\ Hz$, passed



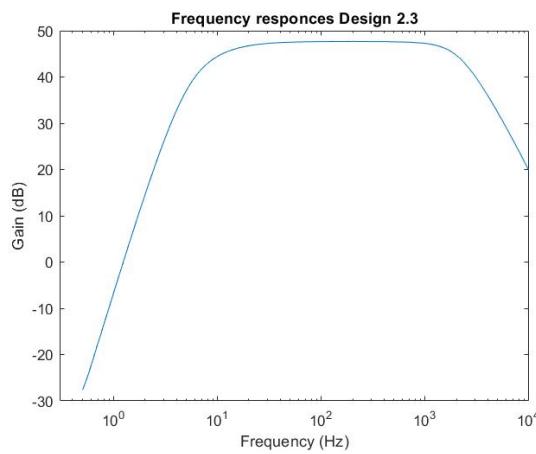
Design 2.1: $G_{AFE_{EMG\ BW}} = 240 \text{ V/V}$, $AFE_{BW} 10.1 - 500\text{Hz}$, passed



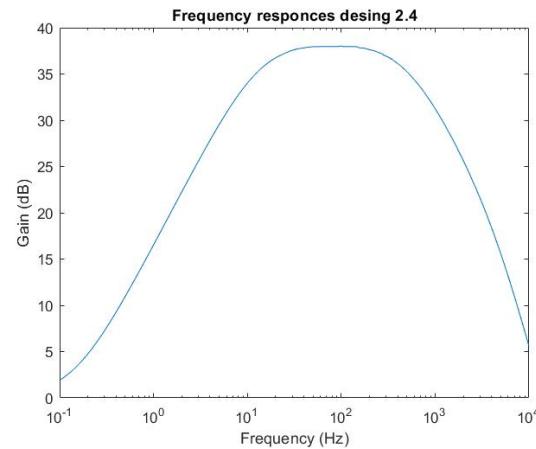
Design 2.2: $G_{AFE_{EMG\ BW}} = 240 \text{ V/V}$, $AFE_{BW} 14 - 500\text{Hz}$, failed. Although this test did not meet the allowed error of 13 Hz, this would still be a viable design as most EMG energy is located between the 50Hz and 150Hz.



Design 2.3: $G_{AFE_{EMG\ BW}} = 239 \text{ V/V}$, $AFE_{BW} 10.3 - 500\text{Hz}$, passed



Design 2.4: $G_{AFE_{EMG\ BW}} = 241 \text{ V/V}$, $AFE_{BW} 13.1 - 500\text{Hz}$, passed



F2.1.2 Test case 2

F2.1.2.1 Requirement

PSPEC3: Variable gain 1-4x.

F2.1.2.2 Test criteria

A gain error of 5% is allowed to succeed pass this test

F2.1.2.3 Test Procedure

Disconnect the outputs of the filter from the inputs of the ADS1298 by disordering the jumpers between the filter outputs and the ADC inputs. Connect the negative input of the ADS1298 to GND and connect the positive input to the probe of the function generator. Connect the GND of the function generator to the ground electrode.

Connect the Analog discovery 2 to the PC and connect the probe from waveform generator 1. Open Waveform 2015 and open the wavegen tool. First select the amplitude, frequency and offset of the signal, set this to 100mV, 20Hz and 0V offset. Next click on start.

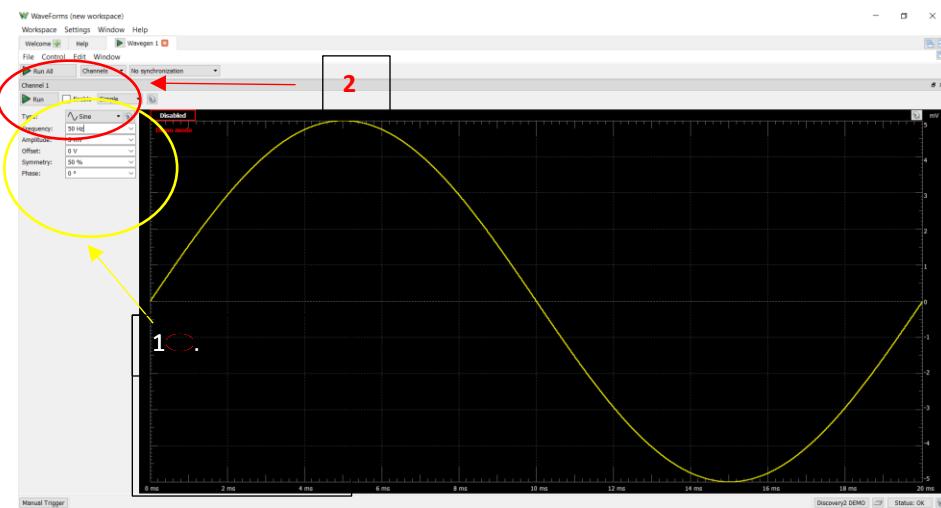


Figure 107 Wavegen1 Waveforms

F2.1.2.4 Results

Result: Succeeded

Table 1 shows the gain results of the test, the small error is caused by the signal generated by the signal generator.

Table 14 gain results

Gain	V_{in}	V_{out}
1x	100mV _{pp}	99.68mV _{pp}
2x	100mV _{pp}	199.54mV _{pp}
3x	100mV _{pp}	298.95.mV _{pp}
4x	100mV _{pp}	398.78mV _{pp}

F2.1.3 Test case 3

F2.1.2.1 Requirement

PSPEC1: FRS is 5V

F2.1.2.2 Test criteria

A gain error of 5% is allowed to pass this test

F2.1.2.3 Test Procedure

Measure the positive and negative analog supply voltages of the ADS1298

F2.1.2.4 Results

Result: Succeeded

A negative voltage of the ADS1298 was measured at -2.48V and the positive voltage of the ADS1298 was measured at 2.51V. Thus this unit test passed successful.

F2.2 Manage battery level

Summary of all the specification of unit 'Manage battery level':

PSPEC-2.1: Short-circuit protection

PSPEC-2.2: Battery over-charge and over-discharge protection (See battery type: 2,8V and 4,2V)

PSPEC-2.3: Battery charge current of 300mA

PSPEC-2.4: Battery fully charged indication (4,2V)

PSPEC-2.5: Efficiency of > 80 %

PSPEC-2.6: Output voltage of 5V

PSPEC-2.7: Output current of 300mA.

PSPEC-2.8: Battery capacity is displayed in %

PSPEC-2.9: Output 'Battery level' is measured in %, with a range of 0 – 100% (100% battery is fully charged, 0% battery empty). The allowed tolerance is 2%.

PSPEC-2.10: The measured current needs to be measured in mA, with a significance of 2 decimals and an allowed error of 2%.

PSPEC-2.11: The measured accumulated current needs to be measured in mAh, with a significance of 2 decimals and an allowed error of 2%.

F2.2.1 Test case 4

F2.2.2.1 Requirement

PSPEC-2.5: Efficiency of > 80 %

PSPEC-2.6: Output voltage of 5V

PSPEC-2.7: Output current of 300mA.

F2.2.2.2 Test equipment

Digital multimeters

Lab bench power

Connectors

F2.2.2.3 Test criteria

A gain error of 5% is allowed to pass this test

F2.2.2.4 Test Procedure

- 1) Disconnect the battery from the circuit.
- 2) Connect the outputs of the lab bench power supply thru a digital multimeter to the power supply input terminal. The digital multimeter needs to be connected as a current meter. Connect to the voltage output terminal of the unit to a voltage and a current meter. The current meter should be placed in series with the load and the voltage meter should be placed parallel to the load.
- 3) Set the lab bench power supply to output a voltage 3,7V and limit the maximum current to 2A. Connect the following resistor loads to the output: 149Ω, 49Ω, 44Ω, 39Ω, 34Ω, 24Ω, 15Ω. At each load value measure the input and output current and voltage of the unit on the digital multimeters. Redo this test with the following lab bench power supply voltages: 3.2V and 4.2V.

The efficiency can be calculated with the following formula:

$$n (\%) = \frac{P_{out}}{P_{in}} * 100 \gg \frac{U_{uit} * I_{uit}}{U_{in} * I_{in}} * 100$$

- 4) If the power supply is able to maintain a stable 5V output with a 16Ω resistor connected to the output ($5V/16\Omega = 330mA$), PSPEC-2.7 is achieved. If the output voltage decreases by >5% when the 16 resistor is connected, the requirement has failed.

F2.1.2.5 Results

Result: Succeeded				
Load resistance	V _{in} (V)	I _{in} (mA)	V _{out} (V)	Efficiency (%)
149	4044	62,7	5136	70
49	4044	167,4	5083	78
44	4028	189,1	5083	77
39	4028	180	5090	92
34	3952	200	5067	96
24	3845	295	5030	93
15	3532	510	5053	94

Table 15 Efficiency Vbat test 4,2V

Test 1, power supply is set to 4,2V. The test results shows that the unit is capable to maintain a stable 5V output at different loads.

Load resistance	V _{in} (V)	I _{in} (mA)	V _{out} (V)	Efficiency (%)
149	3498	71	5114	71
49	3467	170	5099	90
44	3445	190	5090	90
34	3356	240	5099	95
24	3189	360	5074	93
15	2763	650	4982	92

Table 16 Efficiency test Vbat 3,7V

Test 1, power supply is set to 4,2V.

Load resistance	V _{in} (V)	I _{in} (mA)	V _{out} (V)	Efficiency (%)
149	2927	86,9	5120	69
49	2927	200	5095	90
44	2895	230	5073	88
39	2869	260	5017	87
34	2782	300	5058	90
15	2293	650	4460	89

Table 17 Efficiency test Vbat 3.2V

Figure 34 shows the efficiency of the power supply compared to the output current during different input voltages of 4.2V (Red), 3.7V (Blue) and 3.2V (Yellow). The purple line indicates the average efficiency between the different efficiency, this is around 85%. Thus PSPEC2.5 was achieved.

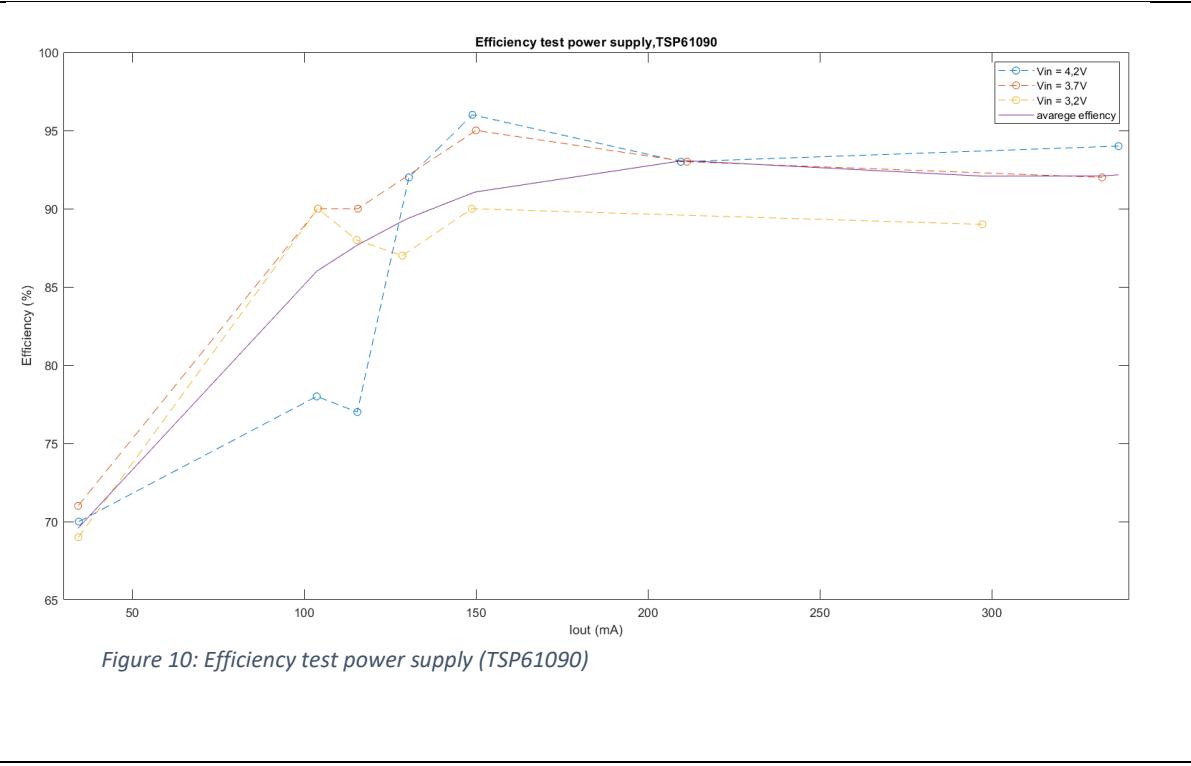


Figure 10: Efficiency test power supply (TSP61090)

F2.1.3 Test case 5

F2.1.3.1 Requirement

PSPEC-2.1: Short-circuit protection

PSPEC-2.2: Battery over-charge and over-discharge protection (See battery type: 2,8V and 4,2V)

PSPEC-2.3: Battery charge current of 300mA

PSPEC-2.4: Battery fully charged indication (4,2V)

F2.1.3.2 Test equipment

Lab bench power supply, digital multimeter and cables.

F2.1.3.3 Test criteria

For PSPEC-2.1 – 2.3 an error of 5% was allowed to pass this test.

F2.1.3.4 Test Procedure

- 1) Disconnect the battery from the circuit. Connect the output leads of the lab bench power supply thru a digital multimeter to the units power input terminal. The digital multimeter needs to be connected as a current meter. Connect to the output terminal of the unit a voltage and a current meter. The current meter should be placed in series with the load and the voltage meter should be placed parallel to the load.
- 2) Set the lab bench power supply to output a voltage of 4,15V, slowly increase the voltage level in steps of 0,01V. While increasing the voltage level measure the output voltage simultaneous. Find the voltage level at which the output voltage is cut-off (0V), write down this value to determine the overcharge voltage threshold (PSPEC-2.2). Reduce the lab bench power supply to 3V, and slowly start to decrease the voltage by 0,01V until the output voltage is cut-off (0V). Write down this voltage level to measure the over-discharge voltage threshold. Use both voltage levels to verify if PSPEC-2.2 has been achieved

- 3) Short-circuit the outputs of the unit together. If no output voltage cut-off at the output and no current is flowing into the power-supply (verify via the input current meter) the short-circuit protection works (PSPEC-2.1).
- 4) Disconnect the lab bench power supply and reconnect the battery to the units power input terminal, keep the current meter in-between of the battery and the units power unit input terminal. Connect the USB C cable to the USB input and start charging the battery. Measure the current level flowing into the battery, write down this value to verify PSPEC-2.3. Keep the USB C charger connected to the circuit until the green light start to light up, once this has happened measure the battery voltage to verify that the battery voltage has reached 4,2V (PSPEC-2.4).

F2.1.3.5 Results

Result: Succeeded

The over-charge voltage threshold was measured at 4,25V and the over-discharge voltage threshold was measured at 2.8V. Thus PSPEC-2.2 was achieved

Short circuit protection worked perfectly, thus PSPEC-2.1 was achieved.

The battery charge current was measured at 296mV, thus PSPEC-2.3 was achieved

The problem that occurred during the recharging of the Li-Ion battery was that battery wouldn't reach its maximum voltage level of 4,2V, even after 6+ hours of charging the battery voltage would remained at around the 4V (the battery was still being charged with roughly 200mA).

The Li-Ion battery was replaced with by a Li-Po battery to test if this would work better, with the Li-Po battery the circuit performed perfectly. Within a couple of hours the battery reached the maximum voltage of 4,21V and the green light turned on indicating the battery was fully charged. Thus PSPEC-2.4 was achieved.

The Li-Ion battery will be replaced with a Li-po (3200mAh) battery permanently.

F2.1.4 Test case 6

F2.1.4.1 Requirement

PSPEC-2.8: Battery capacity is displayed in %

PSPEC-2.9: Output 'Battery level' is measured in %, with a range of 0 – 100% (100% battery is fully charged, 0% battery empty). The allowed tolerance is 2%.

PSPEC-2.10: The measured current needs to be measured in mA, with a significance of 2

PSPEC-2.11: The measured accumulated current needs to be measured in mAh, with a significance of 2 decimals and an allowed error of 2%.

F2.1.4.2 Test equipment

Logic analyser (analog discovery 2), lab bench power supply, board-to-board wires and multimeters.

F2.1.4.3 Test criteria

PSPEC2.9, PSPEC-2.11 & PSPEC-2.10 all allowed an error of 2% to pass this test, this value is compared to the digital value send over the I2C lines.

No error was given to PSPEC-2.8 as the exact battery capacity cannot be accounted for.

F2.1.4.4 Test Procedure

- 1) Disconnect the Battery from the circuit. Connect the output leads of the lab bench power supply thru a digital multimeter to the units power input leads. The digital multimeter needs to be connected as a current meter. Turn the power supply off using the switch placed on the unit and power the OLED display using an external power supply (e.g. Arduino or breadboard power supply). Connect the output of the DC-2745 (JST terminal) to a voltage and a current meter.
- 2) Connect a logic analyser to the SCL and SDA line of the DS-2745, open in waveform the logic analyser application to analyse the send data between the MCU and the DS-2745.
- 3) Set the lab bench power supply to output a voltage of 4.1V and connect to the output a load of 149Ω resistor (5W). Measure the output current and see if this matches to the displayed value on the OLED display.

F2.1.4.5 Results

Result: Partly succeeded and partly failed.

The first problem that occurred during this test was that the DS-2745 would not respond to the slave address provided by the datasheet (90h). After using a I2C scanner (using an Arduino) the correct slave address was found at 48h. The same problem kept occurring even when the DS-2745 was replaced with by a new one.

In this test a lab bench power supply provided the units inputs with a 4,1V, using a multimeter this was verified to be exactly 4.112 V. Figure 33 shows the I2C data line capture between the micro-controller and the DS-2745 during this test. The first data line is the SCL line and the second data line is the SDA line. The DS2745 will return 4 battery parameters (temperature, voltage, current and accumulated current) divided over 8 bytes (each parameter is divided over two bytes).

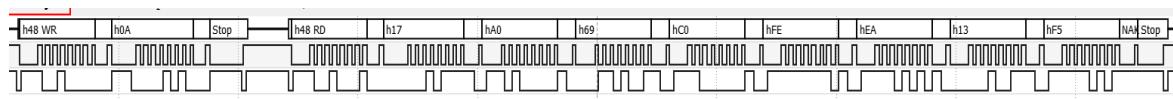


Figure 108 DS-2745 Data lines.

Using the explained formula's in attachment B, the hexadecimal value can be converted into real values.

Voltage: MSB value is 69h and the LSB value is C0h. The combines values correspond to 01101001110 in binary, and corresponds to 846 in decimal. $846 * 4.88mV = 4128.488 mV$ should be displayed on the display.

Current: MSB value is FEh and the LSB value is EAh. This corresponds to 65258 in decimal, this corresponds to -43,4375 mA.

These values correspond to the values printed on the display, both printed values on the display indicate an error of <0.1% (see figure 30). All the values are printed on the display with a significance of 2 decimals, as the PSPEC-2.10 & 2.11 state.



Figure 109 Measured values by the DS-2745 display on the OLED display, where line 1 is the battery voltage, line 2 is the current flowing in or out, line 3 is the amount of mAh left in the battery (this value is initially programmed to 3200mAh) and line 4 is the battery % left in the battery.

However the measured current does not correspond to the actual current flowing, the multi-meter measured a current of -28mA (corresponds with what we expected $4.112V/149\Omega = -27mA$). Thus an error of 16mA was measured. Different current measurements were performed at different input voltages and loads, to analyse how much current error occurred at these values (see table 12).

Resistance	Vin	Measured current multimeter	Measured current on display	Error
149	4.112 V	27mA	-43.3mA	1.59x
49	2.98V	63	-96	1.53x
149	3.55V	23mA	-37mA	1.61x
49	3.49V	73	-113	1.58x
10	2.7V	250	-403	1.61x
No load	4.01 V	0.0	-2.1	-

Table 18 Test current measurement ds-2745

The average error is around the 1,6x the actual current flow. Even when the input and output are switched around (to simulate a current entering the battery), the error remained around the 1,6x.

A possible cause of this problem could be the current sense resistor of $10m\Omega$ has a very huge resistance error of > 50%. After re-soldering different $10m\Omega$ current sense resistors the current error maintained between the 1,5x and 1,6x. Thus the problem was not the current sense resistor.

The second solution would be to compensate the measurement error by setting the offset in the current offset bias register of the DS-2745. After multiple offset values were tested, the error was still not resolved, even when the maximum offset was set, the maximum current offset of 2mA could be achieved.

The final solution to this problem was to multiply the measured current and the accumulated current by multiplying the error with the measured value to obtain the correct value.

Although all the values where display on the display, PSPEC-2.10 & 2.11 didn't display the correct value which is why these where marked as failed. A good option would be to replace this chip with another one.

The current battery capacity is correctly displayed with 2 decimals. However it could

F2.2 Test traceability

Specification	Test case	Result
PSPEC1: <i>FRS is 5V.</i>	1	v
PSPEC2: . $G_{AFE\ EMG\ BW} = 250\ V/V$	1	v
PSPEC3: <i>Variable gain 1-4x.</i>	2	v
PSPEC4: $A_{FE\ BW}$ 10 – 500Hz.	3	v
PSPEC-2.1: Short-circuit protection.	5	v
PSPEC-2.2: Battery over-charge and over-discharge protection (See battery type : 2,8V and 4,2V).	5	v
PSPEC-2.3: Battery charge current of 300mA.	5	v
PSPEC-2.4: Battery fully charged indication (4,2V).	5	v
PSPEC-2.5: Efficiency of > 80 %.	4	v
PSPEC-2.6: Output voltage of 5V.	4	v
PSPEC-2.7: Output current of 300mA.	4	v
PSPEC-2.8: Battery capacity is displayed in %.	6	v
PSPEC-2.9: Output ‘Battery level’ is measured in %, with a range of 0 – 100% (100% battery is fully charged, 0% battery empty). The allowed tolerance is 2%.	6	v
PSPEC-2.10: The measured current needs to be measured in mA, with a significance of 2 decimals and an allowed error of 2%.	6	x
PSPEC-2.11: The measured accumulated current needs to be measured in mAh, with a significance of 2 decimals and an allowed error of 2%.	6	x

F3 Integration Test

As unit 'measure battery level' was eliminated from the current design, there were only two integration tests left, 1) between the ADC and the MCU and 2) between the MCU and the PC.

F3.1 Test case 7

Integration test between the ADC (ADS1298) and the MCU.

F3.1.1 Products

- Logic analyser

F3.1.2 Test Procedure

Connect the MCU to the PC and open Atholic True Studio and upload the Read_ID folder onto the MCU. Open the terminal window and look at the printed ID value on the terminal. If the ID value is 92h (146 decimal or 10011010 binary) this indicated that the ADS129X family was detected and that eight-channel were indicated. The printed value on the screen can be verified using a logic analyser, the logic analyser should be connected to the DOUT, DIN, SCLK and CS lines.

F3.1.3 Results

Result: Succeeded

The correct value was printed on the screen (92h) and this was verified using the logic analyser, see figure 3



F3.2 Test case 8

Integration test between the MCU and the PC.

F3.2.1 Test Procedure

Connect the MCU to the PC and open the serial terminal to start the communication. Once the serial communication has established enter 'S' via the serial monitor to start data receival, stop the data receival after a second using the 'P' command. Count the number of bytes printed on the screen, to verify if the communication works between the MCU and the PC

F3.2.2 Results

Result: Succeeded

On the terminal window 24 bytes were printed, thus it can be concluded that this integration has been succeeded.

F4 Acceptance test

F4.1 Requirements

This paragraph summarises all the requirements.

F4.1.1.1 HD-SEMG acquisition system

REQA-02: Minimum CMMR > 70 dB within the EMG bandwidth, see chapter 2.

REQA-03: Sampling rate 2kS/s/ch

REQA-04: Input referred noise (IRN) < 4 μ Vrms.

REQA-05: Dynamic input range of EMG signal with an amplitude up to 5mV.

REQA-07: Current consumption of < 300mA.

REQA-08: Minimum operating time of the device is 2-hours on one battery cycle.

REQA-09: Minimum wireless data transportation range of 2m, from the device to the PC.

REQA-10: Indication that the battery is fully charged.

*note the requirements marked red, will not be tested as this function (linked to unit 'Manage battery') was eliminated from the current design.

F4.1.1.2 User interface

REQB-01: Muscle activity can be shown using a colour bar, where green is no activity and red is a lot of activity.

REQB-02: Battery capacity is displayed in %

REQB-03: Notification is sent to the user when battery capacity is <10% and new measurement session cannot be started if the battery capacity is below 10%.

REQB-04: Different spatial filter can be selected: LSD, LDD, NDD and IB2.

REQB-05: Window length can be selected between the 0.1 and 3 seconds.

REQB-06: Maximum EMG amplitude can be selected between the 10mV and the 500mV.

REQA-07: Additional gain can be selected, ranging from 1-4x (in steps of 1).

*These requirements will not be tested in the acceptance as this thesis focuses on the development of the hardware for the system.

F4.1.2 Non-function requirements

REQC-01: Material costs < 1000 €

REQC-02: Device dimensions need to be within 15x10x4 cm.

REQC-03: Weight < 200 gram.

REQC-04: EMG electrode size < 10mm diameter

REQC-05: Inter electrode distance (IED) < 10 mm

REQC-06: 64 EMG channel

REQC-07: Electrode configuration needs to be in monopolar

F4.2 Test case 9

F4.2.1 Requirement

REQC-01: Material costs < 1000 €

F4.2.1 Test criteria

An error of 10% is allowed to pass this test successfully.

F4.2.2 Test Procedure

F4.2.3 Results

Result: Not succeeded

The price of our 64 channel prototype is around the €2500, see chapter 6.4 for a detailed description of this value.

F4.3 Test case 10

F4.3.1 Requirement

REQC-04: EMG electrode size < 10mm diameter

REQC-05: Inter electrode distance (IED) < 10 mm

REQC-06: 64 EMG channel

F4.3.2 Test criteria

For both REQC-04 & -05 an error of 10% is allowed to pass this test successfully.

F4.3.3 Test Procedure

Using a calliper measured the size of the electrode in mm.

Using a calliper measure the IED between two electrodes (centre to centre)

Count the number of electrode inputs.

F4.3.4 Results

Result: Not succeeded

As mentioned before these requirements require a fully functional prototype in order to be tested, as this was not acquired during the internship period due to project funding and time, these requirements could not be tested.

F4.4 Test case 11

F4.4.1 Requirement

REQC-02: Device dimensions need to be within 15x10x4 cm.

REQC-03: Weight < 350 gram.

F4.4.2 Products

To perform this test case the following equipment is required:

- 30 cm ruler
- Scale (set to grams, minimum range is 1kg)

F4.4.3 Test criteria

For requirement REQC-02 an error of 5% is allowed to pass this requirement successfully.

F4.4.4 Test Procedure

Using the ruler measure all the sides (LxHxW) of the prototype in mm.

Reset the scale (target button) to ensure that the device has no offset, place the device on the scale and measure the weight in grams.

F4.4.5 Results

Result: Not succeeded

As mentioned before these requirements require a fully functional prototype to be tested, as this was not acquired during the internship period due to project funding and time, these requirements could not be tested.

F4.5 Test case 12

F4.5.1 Requirement

REQC-07: Electrode configuration needs to be in monopolar

F4.5.1 Test criteria

F4.5.1 Test Procedure

Connect channel input 1 a function generator and connect the reference electrode to ground. Set the function generator to output a signal of 5mV.

F4.5.1 Results

Result: Succeeded

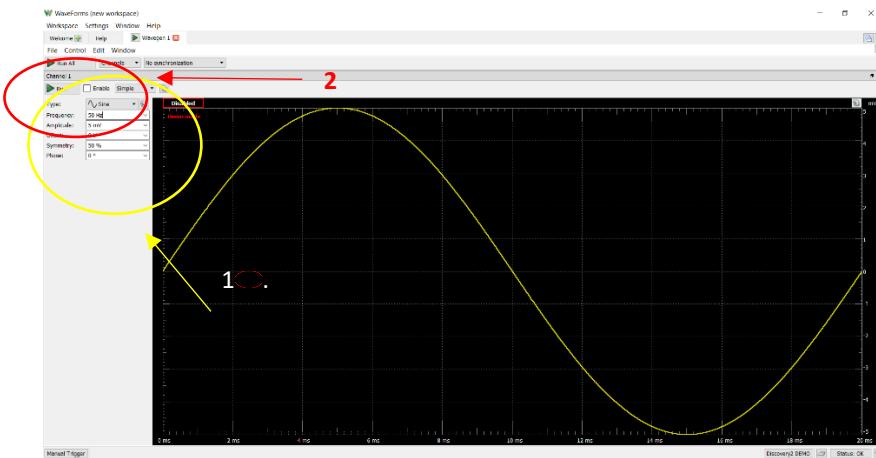
F4.6 Test case 13

F4.6.1 Requirement

REQA-05: Dynamic input range of EMG signal with an amplitude up to 5mV.

F4.6.2 Test criteria

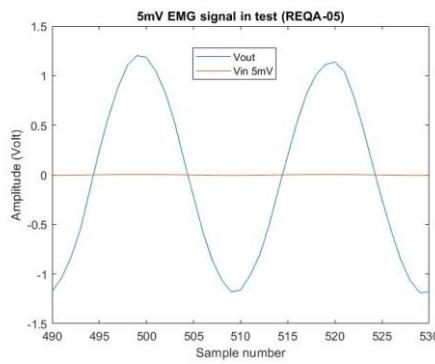
F4.6.3 Test Procedure



8.1.1 Results

Result: Succeeded

When a input signal of 5mV is applied to the input (CH1) a output signal with an amplitude of 1.3V was measured. This is within the maximum of analog supply voltages of the ADS1298 (+/-2.4V), thus it can be concluded that this requirement has been successful passed.



F4.7 Test case 14

F4.7.1 Requirement

REQA-02: Minimum CMRR > 70 dB within the EMG bandwidth, see chapter 2.

F4.7.2 Test criteria

An error of 5% is allowed to pass this test successfully.

F4.7.3 Test Procedure

Short circuit both input leads together, and connect the output of the function generator to it. Connect the GND of the function generator to the ground electrode. Open the wavegen application in waveforms and set signal waveform to an amplitude of 500mV and a frequency of 10Hz. An example of this setup is shown in figure 4.

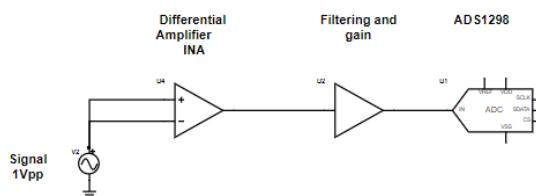


Figure 111 Setup of CMRR test

Measure the RMS output at the following frequencies:

10Hz-100Hz in steps of 10Hz, and 100Hz-1000Hz in steps of 100Hz.

The formula to calculate CMRR is:

$$CMR = Gain \text{ (dB)} - CMG \text{ (dB)}$$

Where:

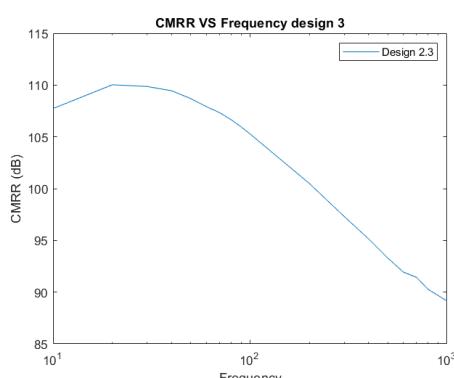
$$CMG \text{ (common-mode gain)} = 20 * \log\left(\frac{V_{out \text{ RMS}}}{V_{in \text{ RMS}}}\right)$$

The Gain (dB) can be measured from

F4.7.4 Results

Result: Succeeded

The results show that a CMRR of at least 70dB within the EMG BW was achieved.



F4.8 Test case 15

F4.8.1 Requirement

REQA-04: Input referred noise (IRN) < 4 μ Vrms.

F4.8.2 Test criteria

To pass this test an error of 5% is allowed to pass this test successfully.

F4.8.3 Test Procedure

Short circuit both inputs together (CH1 and PREF) to the ground electrode.

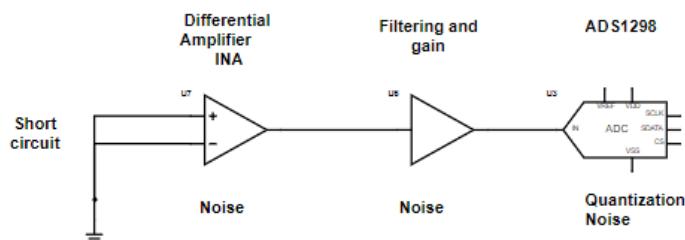


Figure 112 IRN test setup

The following formula is needed to calculate the IRN of the AFE:

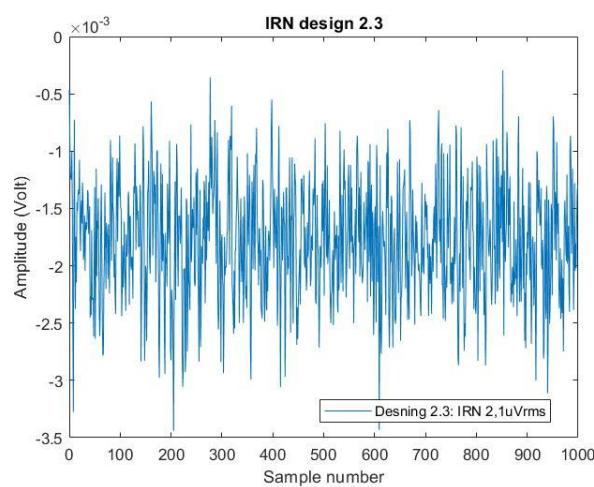
$$IRN_{rms} = \frac{OutputNoise_{rms}}{Gain}$$

Using the developed software calculate the RMS

F4.8.4 Results

Result: Succeeded

The test results indicate an IRN of only 2.1 μ Vrms, thus this requirement has been successful.



F4.9 Test case 16

F4.9.1 Requirement

REQA-03: Sampling rate 2kS/s/ch

F4.9.2 Equipment

To perform this test case the following equipment is required:

- Logic analyser

F4.9.3 Test criteria

A 1% error is allowed to pass this test successfully.

F4.9.4 Test Procedure

Connect the logic analyser to the following pins DRDY, MOSI, MISO and clock SCLK. Open in waveform 2015 the logic analyser tool (set the device setting to setting 4). Set to the logic analyser to record data at 100M samples per second at a rate of 20MHz. Click on record, once the recording has completed, measure the time between two falling edges of DRDY to calculate the sample rate.

F4.9.5 Results

Result: Succeeded

Figure 4 indicates a time of $499\mu\text{s}$ in between of the two falling edges of DRDY, this corresponds to a sampling frequency of 2004Hz. Thus it can be concluded that this test has been successful.

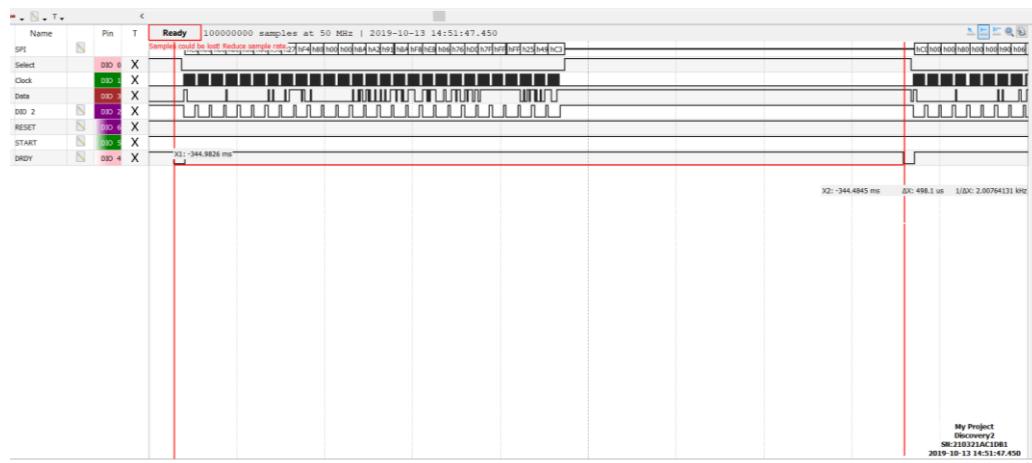


Figure 113 Sample rate ADS1298

Attachment G: Reflection

Om te beginnen ben ik het bedrijf erg dankbaar, de mogelijkheid die het bedrijf mij heeft gegeven om een zelf bedachte vraagstelling uit te kunnen werken en de voorzieningen die het bedrijf voor mij heeft getroffen tijdens de stage (appartement). Het was een zeer leerzame ervaring om in een internationale werkomgeving te kunnen werken, dit heeft mij veel bijgebracht over de verschillende culturen en gewoontes tussen verschillende landen.

Helaas heeft de begeleiding en communicatie tijdens de stage periode voor mij op veel punten te kort geschoten, dit komt vooral door de bedrijfsbegeleider. Zo is er alleen tijdens de eerste paar weken van de stage een wekelijke vergadering geweest tussen mij en de bedrijfsbegeleider, tijdens deze vergaderingen zijn kort het doel van het project en de vooruitgang van de afgelopen week besproken. In de resterende stage periode is de bedrijfsbegeleider niet meer langs gekomen voor een wekelijks gesprek. Dit heeft deels geleid dat ik tijdens de stage verkeerde ontwerp keuzes had genomen waardoor het ontwerp van het product veel vertraging had opgelopen. Deze verkeerde keuzes hadden wellicht voorkomen kunnen worden als ik veel meer input vanuit de bedrijfsbegeleider had gehad en in discussie met hem had kunnen gaan over belangrijke ontwerp keuzes die ik had genomen.

Een voorbeeld hiervan was dat ik pas tegen het einde van de stage had gedacht dat ik de norm IEC-60601 in het product moest implementeren, deze norm beperkt het maximale stroom dat een persoon kan binnen gaan tijdens kortsluiting. Dit had geleid had ik het gehele ontwerp had moeten veranderen, omdat bepaalde onderdelen door deze norm beïnvloed werden.

Zelf ben ik hier ook deels in verantwoordelijk, zo had ik ook actie kunnen ondernemen om een gesprek aan te gaan met de bedrijfsbegeleider en hem aan te spreken op het punt dat ik de begeleiding vanuit hem te weinig vond. De bedrijfscultuur in Polen is veel hiërarchischer dan in Nederland, hierdoor vond ik het erg lastig om de bedrijfsbegeleider hierop aan te spreken

Dit heeft mij ook geleerd om een stuk zelfstandig te zijn en de keuzes met eventuele gevolgen voor eigen rekening te nemen, daarnaast heb ik geleerd dat ik een assertieve houding aannemen en het kenbaar moet maken als ik niet tevreden ben met de huidige gang van zaken.

Attachment H: Competence accountability (Dutch)

In deze paragraaf wordt de competentie verantwoording afgelegd.

1) Analyseren

De probleem stelling is vertaald in een plan van eisen, deze eisen zijn smart opgesteld. De probleem stelling is samen in overleg met de klant vertaald in een systeem context. In de scope van de project zijn eventuele afwegingen gemaakt wat de minimale oplevering moet zijn. Tijdens het formuleren van de systeem eisen zijn tekortkoming van verschillende systemen op de markt in meegenomen, zoals het gebruik van droge electroden en het ontwerpen van een draadloos en draagbaar apparaat. Daarnaast zijn diverse eisen gebaseerd op wiskundige vergelijkingen.

2) Ontwerpen

De eisen zijn vertaald in een ontwerp aan de hand van system engineering, de units zijn verder vertaald in componenten die de functies van de units kan vervullen. Tijdens het ontwerp proces zijn diverse grote verandering aan de originele doelstellingen toegebracht, zo was de originele doelstelling om een draadloos systeem te ontwikkelen. Helaas was het niet mogelijk om een draadloos systeem te realiseren door bandbreedte imitatie. Bij het ontwerpen van het product is nagedacht over de veiligheid van het product, hierbij gaat het om norm IEC-60106, deze norm specificeert de maximale stroom dat een lichaam mag binnengaan tijdens kortsluiting.

3) Realiseren

Het product is ontwerpen aan de hand van het V-model, zo is eerst de units gemaakt en getest, vervolgens in de interactie tussen de units getest en als laatste het gehele systeem getest. Tijdens de stage is een ontwikkeld product in zijn geheel testbaar is, echter voldeed het opgeleverde niet in alle opzichten aan de opgestelde eisen. Zo was het niet mogelijk om het systeem te gebruiken met de gewenste sample frequentie van 2kSps/ch, echt kon het wel als geheel getest worden op 250Sps/ch. Echter voor correct uitvoeren van de testen was een sample frequentie van tenminste, dus was er een alternatieve methode gevonden om dit alsnog uit te voeren.

4) Beheren

Nadat het project opgeleverd was, was alle benodigde documentatie aan het bedrijf overgedragen, in de versie beheer van het verslag zijn de benodigde project wijzigingen terug te vinden. Helaas zijn binnen het bedrijf geen afspraken gemaakt over hoe een projectdocument opgebouwd moet zijn.

5) Managen

Om het project zorgvuldig uit te kunnen voeren is er een plan van aanpak is op een systematische wijze geschreven, dit document begint met een beschrijving van het project probleem en doelstelling, vervolgens worden de project grenzen aan gegeven door onder andere een MoSCOW analyse, waarna project risico's met oplossing worden behandeld en gecategoriseerd, het document wordt afgesloten met een project planning. Halverwege de stage was de planning was de planning geëvalueerd, hieruit was gebleken dat het project ver achter liep op de planning, dit was opgelost door meer uren te werken en huidige struikel blokken over te slaan en met een ander onderdeel verder te gaan. Helaas was de project planning hierop niet opnieuw op aangepast.

6) Adviseren

Er is een advies gegeven over hoe het project vervolgd kan worden, het eerste advies bevat punten waarop het systeem verbeterd kan worden. Het tweede advies is een alternatief advies om het huidige ontwerp te gebruiken om een ander product te ontwikkelen, dit advies is gegeven omdat het huidige ontworpen systeem ten opzicht van vergelijkbare producten op de markt geen unieke specificaties vertoont waardoor de kans groot is dat weinig klanten geïnteresseerd zullen zijn in het product.

Dus er kan geconcludeerd worden dat de opdracht gever voorzien is van advies over hoe het project vervolg moet worden, dit onderbouwd met gegronde argumenten en er is een kritische blik naar het product gekeken.

7) Onderzoeken

Er zijn verschillende methoden om spier activatie te meten. De meeste gebruikelijke methode is via electroden en het meten van elektromyografie (potentiaal verschillend). Echter wordt via electrode veel ruis gemeten dat een vele malen grotere amplitude dan het EMG signaal zelf kan hebben. Dus er is onderzoek gedaan welke andere methoden er zijn die gebruikt kunnen worden om spier activatie te meten zonder electroden. Het onderzoek concludeerde dat er maar 1 alternatieve methode is om spier activatie te meten zonder electroden. Helaas heeft deze methode nog geen verband gevonden tussen spier activatie en spier omvang waardoor het nog niet gebruikt kan worden.

8) Professionaliseren

Aan het afstudeer verslag is een competentie verantwoording en een reflectie verslag aan toegevoegd. Zoals in het reflectie verslag staat aangegeven heeft de begeleiding vanuit het bedrijf op veel punten te kort geschoten, zo is er tijdens de stage periode niet geëvalueerd of zowel ik als het bedrijf tevreden was over de vooruitgang van mijn project of de werkhouding van met en had ik mij hierop kunnen verbeteren. Zelf had ik hierop moeten aandringen, maar dit was niet gebeurt vanwege dat ik toch te bescheiden was.

Attachment I: ADS1298 system commands

System commands: These commands are basic commands for resetting, starting and stopping conversions and waking up of standby or entering standby mode. These modes require one opcode to send from the host to the ADS1298 and can at any time.

- **WAKEUP:** The WAKEUP opcode exits low-power standby mode. Additional start-up time is required after exiting from standby mode.
- **STANDBY:** The STANDBY opcode command enters the low-power standby mode. All parts of the circuit are turned off, except for the reference section.
- **RESET:** The RESET opcode reset all register settings to the respective default values.
- **START:** This opcode starts data conversions. The start pin can be tied to low to control the conversion on command (see figure 52).

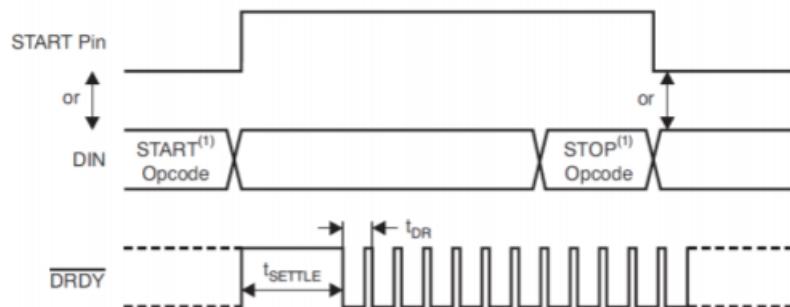


Figure 114 Start of conversions ads1298

- **STOP:** The STOP opcode stops conversions.

Data Read Commands: The following commands are used for reading data from the ADS1298.

- **RDATA:** This command sets the ADS1298 into read continuous data mode without the need of sending subsequent opcodes. This mode is the default mode of the device on power-up and reset. For this opcode to work the start command must be sent or the start pin must be set to high. A data ready status pin (DRDY) toggles whenever new data is available.
- **SDATA:** This command cancels the RDATA command, after sending this command the ADS1298 can be programmed to the correct settings or set to RDATA mode.
- **RDATA:** This command is used for reading conversion data on command. First either the START pin must be set to high or the START command must be sent. After each DRDY interrupt the RDATA command must be sent before the data is sent out from the ADS1298. RDATA is best used in applications where register settings must be read or changed often between conversion cycles.

Read data continuous mode was chosen as the operating mode.

Register read/write commands

- **WREG:** This opcode writes the register data. The WREG command is a two-byte opcode followed by the input of the register data. The first byte contains the command opcode and the register address, this has the following format: 010r rrrr, where r rrrr is the starting register address. The second byte of the opcode specifies the number of register to write to, this has the following format: 000n nnnn, where n nnnn is the number of register to write to -1. After the opcodes byte the register data follows, where the data is send in MSB-first format.
- **RREG:** This opcode read the register data. The RREG command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address, this has the following format: 010r rrrr, where r rrrr is the starting register address. The second byte of the opcode specifies the number of register to read from, this has the following format: 000n nnnn, where n nnnn is the number of register to write to -1.

Attachment J: firmware and software codes

Source code of the firmware, Python GUI application, schematics and MATLAB code. To save paper in this report a link has been added to a GitHub page, where all the data is placed in separate folders.

Github link to my page:

<https://github.com/oliverkersten/Graduation-project-files>