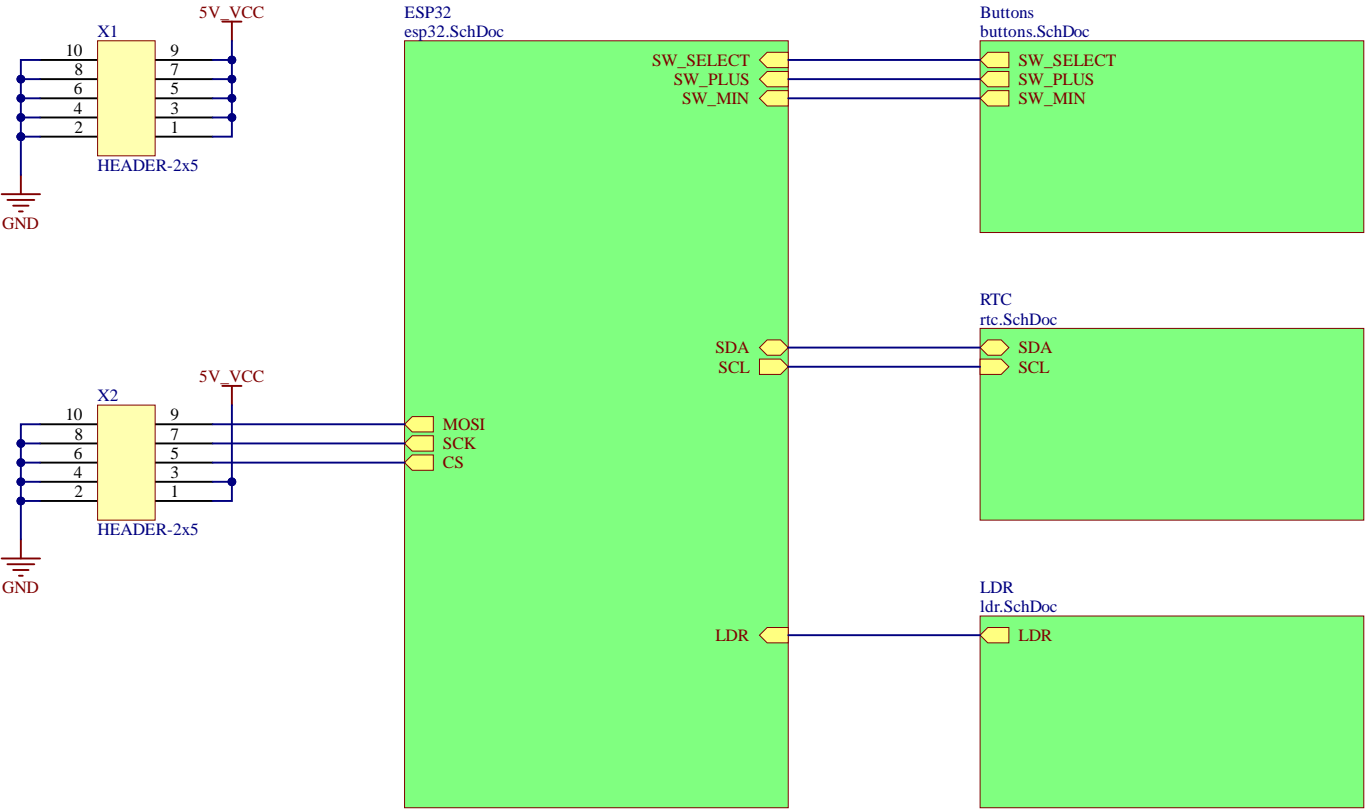
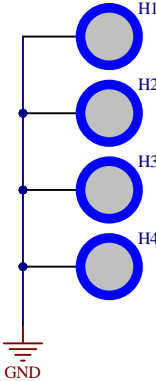



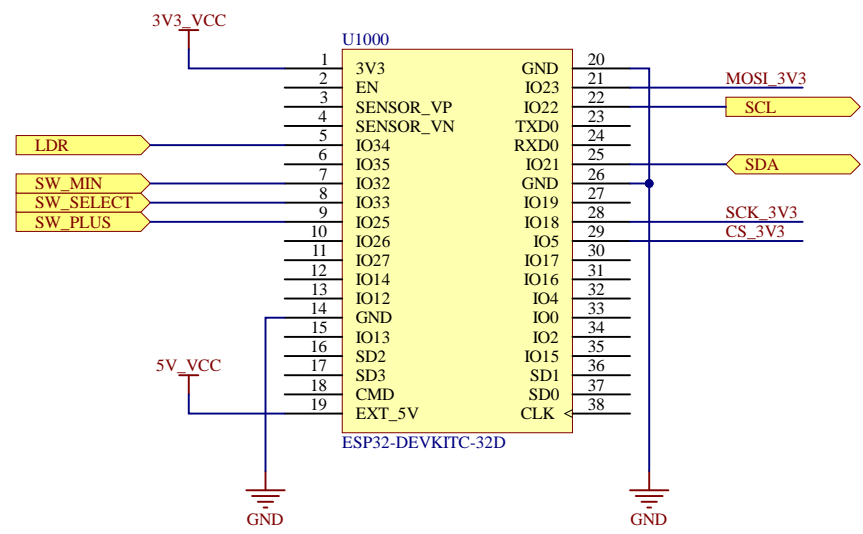
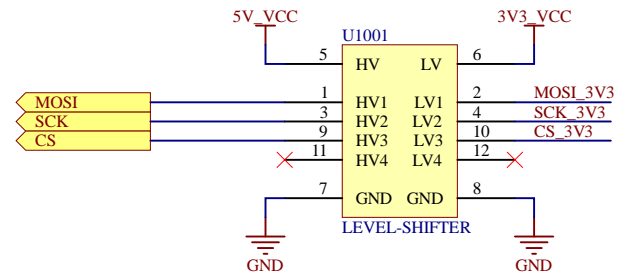
FIDUCIALS




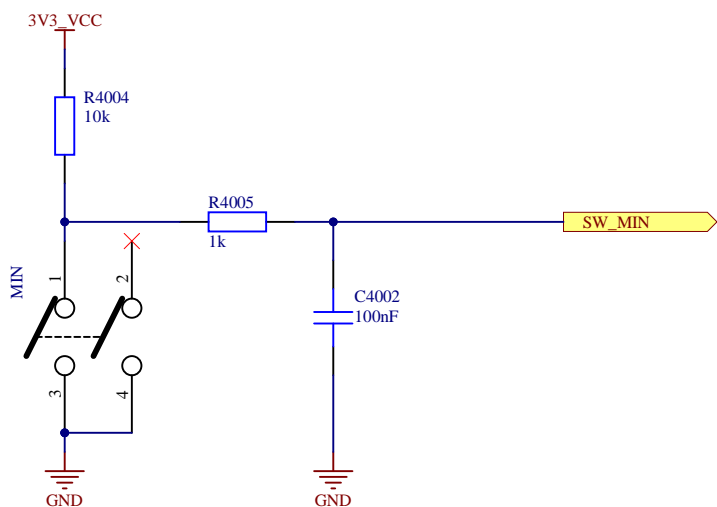
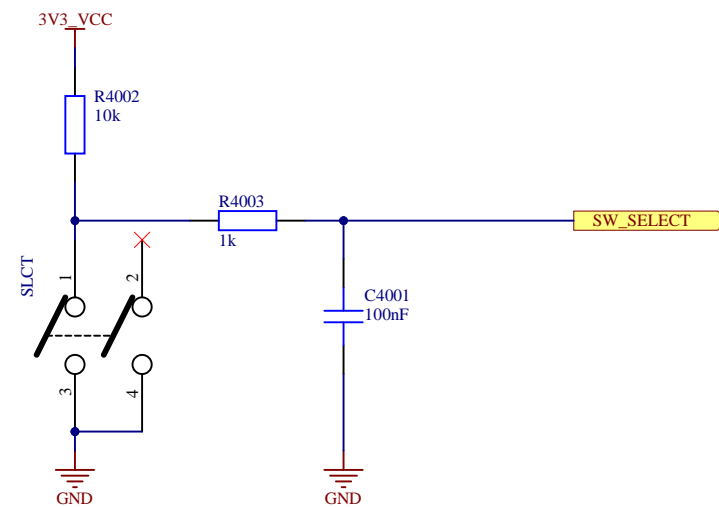
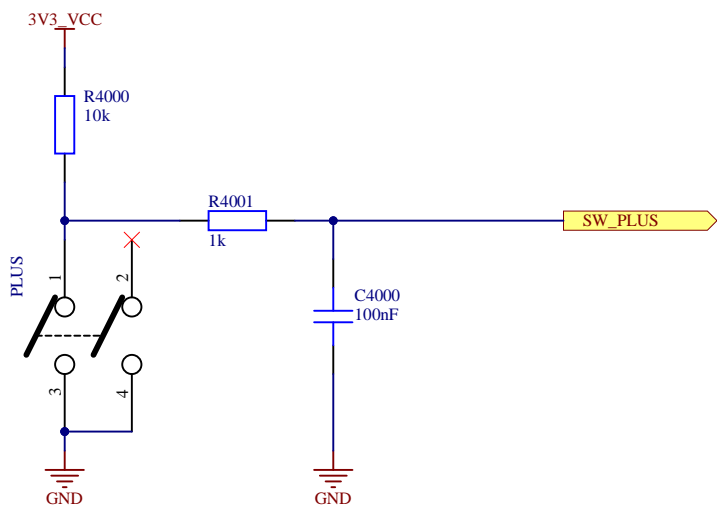
MOUNTING HOLES




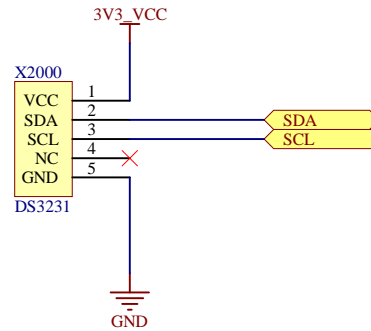
Project: Smart Clock - Main Board		Author: Noël Visser		
Page Contents: main-board.SchDoc		Checked by: -	Revision: R01	
Size: A4		Page: Sheet 1 of 5		
Date: 28/08/2020	Website: github.com/noelvisser/esp32-smart-clock			




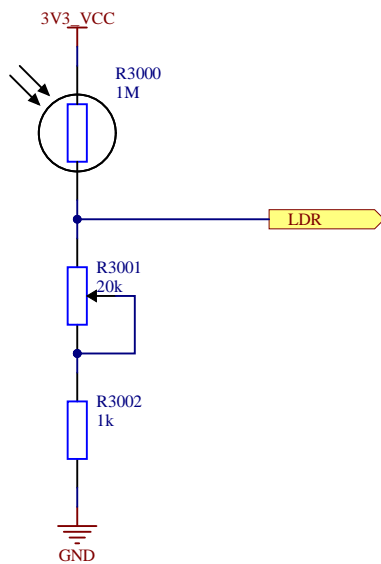
Project: Smart Clock - Main Board		Author: Noël Visser		
Page Contents: esp32.SchDoc		Checked by: -	Revision: R01	
Size: A4		Page: Sheet 2 of 5		
Date: 28/08/2020	Website: github.com/noelvisser/esp32-smart-clock			




Project: Smart Clock - Main Board		Author: Noël Visser		
Page Contents: buttons.SchDoc		Checked by: -	Revision: R01	
Size: A4		Page: Sheet 3 of 5		
Date: 28/08/2020		Website: github.com/noelvisser/esp32-smart-clock		



Project: Smart Clock - Main Board		Author: Noël Visser		
Page Contents: rtc.SchDoc		Checked by: -	Revision: R01	
Size: A4		Page: Sheet 4 of 5		
Date: 28/08/2020	Website: github.com/noelvisser/esp32-smart-clock			



Project: Smart Clock - Main Board		Author: Noël Visser		
Page Contents: ldr.SchDoc		Checked by: -	Revision: R01	
Size: A4		Page: Sheet 5 of 5		
Date: 28/08/2020	Website: github.com/noelvisser/esp32-smart-clock			

Design Rules Verification Report

Filename : C:\Git\esp32-smart-clock\hardware\smart-clock\smart-clock-main-board\smart-

Warnings 2
Rule Violations 0

Warnings	
Multilayer Pads with 0 size Hole found	2
Total	2

Rule Violations	
Clearance Constraint (Gap=0.102mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint (All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.102mm) (Max=1816.048mm) (Preferred=0.102mm) (All)	0
Minimum Annular Ring (Minimum=0.076mm) (All)	0
Hole Size Constraint (Min=0.2mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.25mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.102mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=1816.048mm) (Preferred=12.7mm) (All)	0
Total	0

Multilayer Pads with 0 size Hole found	
Pad FD2-1(97.5mm,38mm) on Multi-Layer	
Pad FD1-1(11mm,2.5mm) on Multi-Layer	