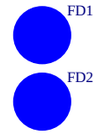
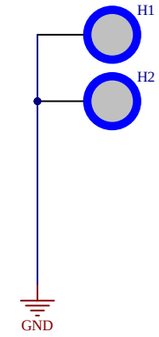
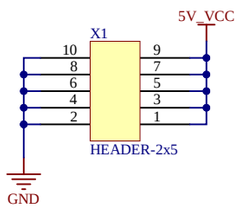
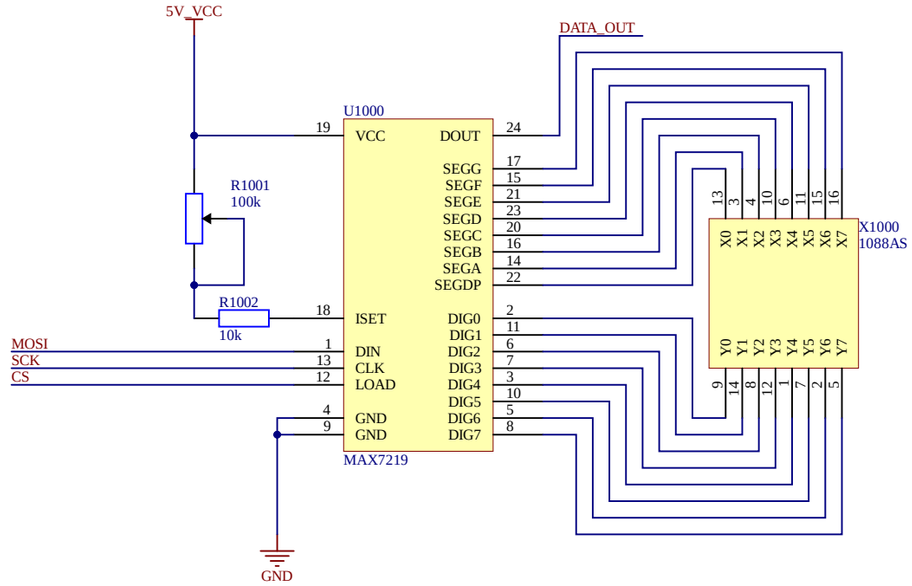
FIDUCIALS

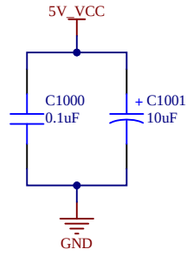


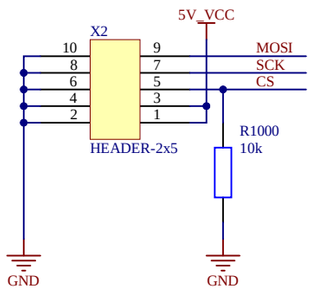
MOUNTING HOLES

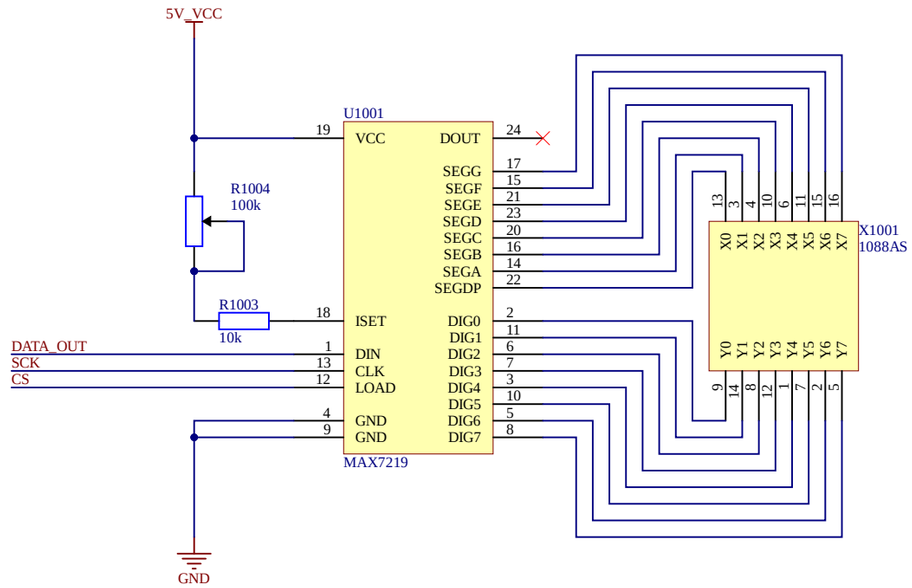


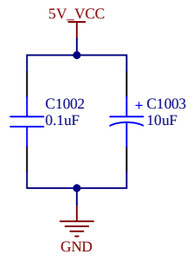












Project: Smart Clock - Display	Author: Noël Vissers
Page Contents: display.SchDoc	Checked by: - / Revision: R01
Size: A3	Page: Sheet 1 of 1
Date: 28/08/2020	Website: github.com/noelvissers/esp32-smart-clock

Design Rules Verification Report

Filename : C:\Git\esp32-smart-clock\hardware\smart-clock\smart-clock-display\smart-clock

Warnings 2
Rule Violations 0

Warnings	
Multilayer Pads with 0 size Hole found	2
Total	2

Rule Violations	
Clearance Constraint (Gap=0.102mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.102mm) (Max=1816.048mm) (Preferred=0.102mm) (All)	0
Power Plane Connect Rule(Direct Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.3mm) (Conductor Width=0.102mm) (Air Gap=0.102mm)	0
Minimum Annular Ring (Minimum=0.076mm) (All)	0
Hole Size Constraint (Min=0.2mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.25mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.102mm) (IsPad),(All)	0
Silk to Silk (Clearance=0mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	0
Height Constraint (Min=0mm) (Max=1816.048mm) (Prefered=12.7mm) (All)	0
Total	0

Multilayer Pads with 0 size Hole found
Pad FD2-1(97.155mm,47.09mm) on Multi-Layer
Pad FD1-1(12.7mm,2.64mm) on Multi-Layer