0.5A / contact
4x for LCD digital logic (2A max)
5x for BL (2.5A x Vbat watts)

JP11
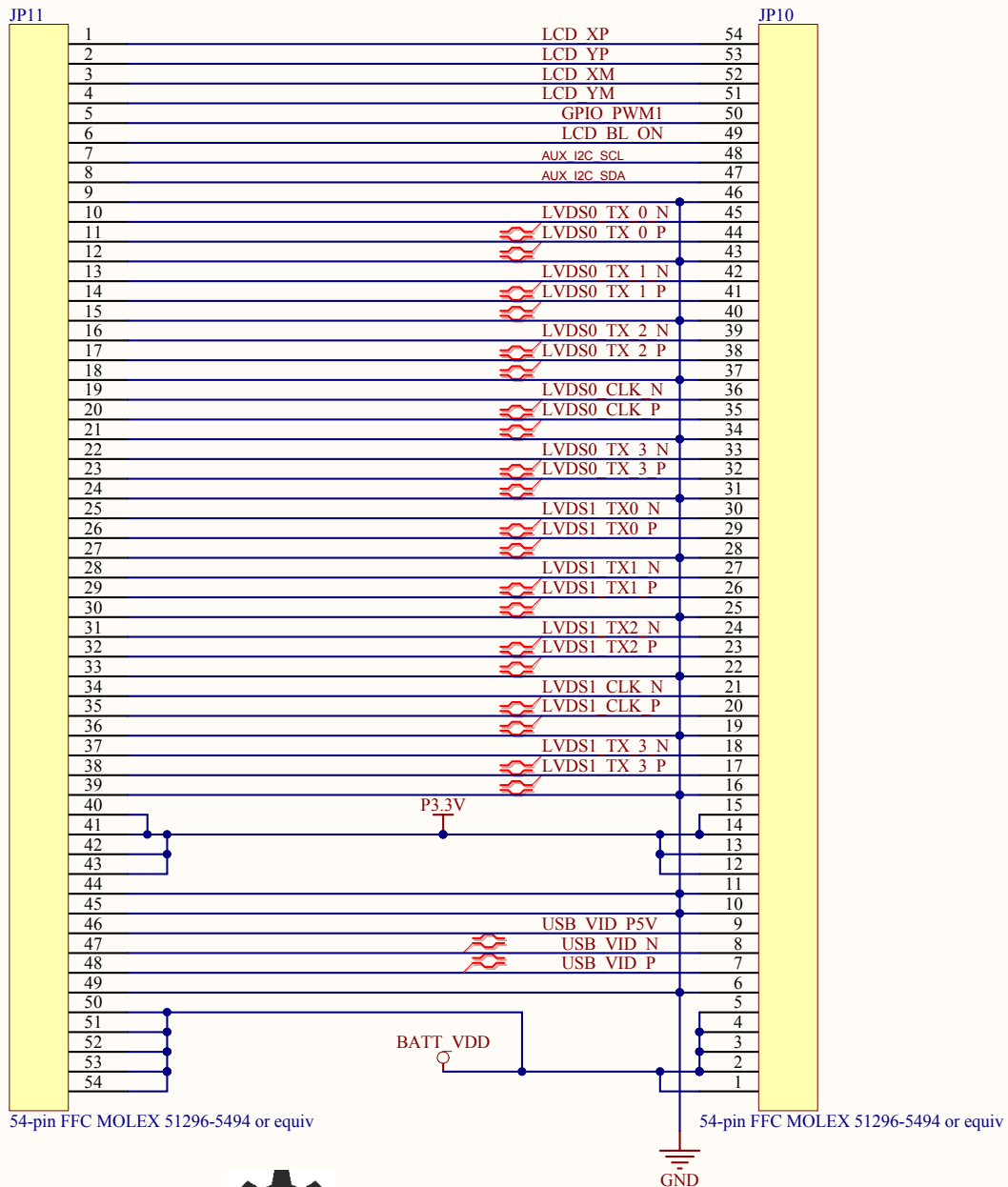
JP10

Pin	Signal	Pin
1	LCD_XP	54
2	LCD_YP	53
3	LCD_XM	52
4	LCD_YM	51
5	GPIO_PWM1	50
6	LCD_BL_ON	49
7	AUX_I2C_SCL	48
8	AUX_I2C_SDA	47
9		46
10	LVDS0_TX_0_N	45
11	LVDS0_TX_0_P	44
12		43
13	LVDS0_TX_1_N	42
14	LVDS0_TX_1_P	41
15		40
16	LVDS0_TX_2_N	39
17	LVDS0_TX_2_P	38
18		37
19	LVDS0_CLK_N	36
20	LVDS0_CLK_P	35
21		34
22	LVDS0_TX_3_N	33
23	LVDS0_TX_3_P	32
24		31
25	LVDS1_TX0_N	30
26	LVDS1_TX0_P	29
27		28
28	LVDS1_TX1_N	27
29	LVDS1_TX1_P	26
30		25
31	LVDS1_TX2_N	24
32	LVDS1_TX2_P	23
33		22
34	LVDS1_CLK_N	21
35	LVDS1_CLK_P	20
36		19
37	LVDS1_TX_3_N	18
38	LVDS1_TX_3_P	17
39		16
40		15
41		14
42		13
43		12
44		11
45		10
46	USB_VID_P5V	9
47	USB_VID_N	8
48	USB_VID_P	7
49		6
50		5
51		4
52		3
53		2
54		1

P3.3V

BATT_VDD

54-pin FFC MOLEX 51296-5494 or equiv

54-pin FFC MOLEX 51296-5494 or equiv

GND

Title LVDS to eDP adapter DVT1

Size A	Number	Revision

Date:	3/27/2014	Sheet of
File:	F:\largework\..\cable.SchDoc	Drawn By:

Board name: Novena 54 LVDS cable

Contact: bunnie@kosagi.com

immersion gold

Stiffener to 0.3mm thick

Stiffener to 0.3mm thick

navena 54 LVDS v1

rev3

coverlay region

hdmie 3.0 stiffene

Silk: white
Coverlay: clear
Contact Finish: Immersion gold
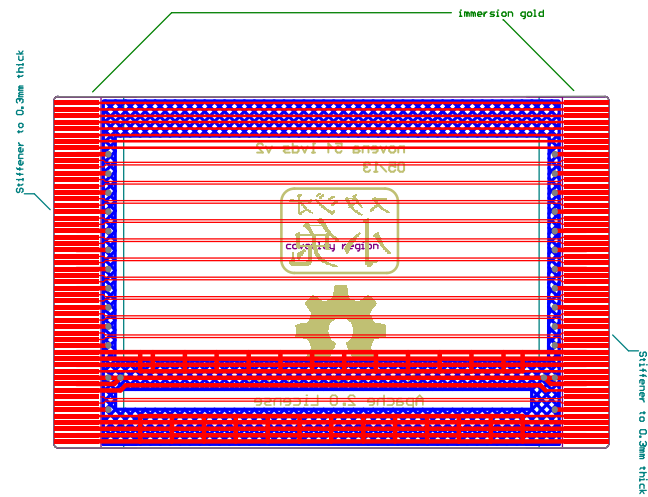
Material and thickness

Coverlay 27.5 um

Copper 35 um

Top-bottom pair

stiffener (PI)

copper

Stiffener area: 0.3mm +/-0.05mm TOTAL thickness

PI: 25 um

Kapton (PI)

Copper 35 um

Coverlay 27.5 um
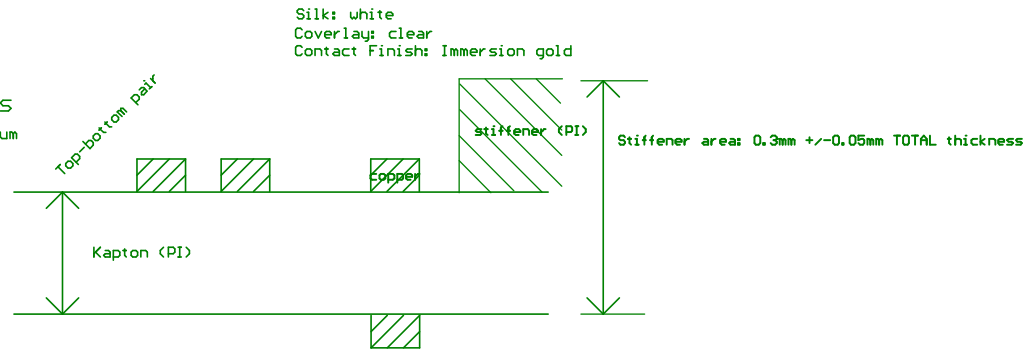
Mech via: 0.25mm hole / 0.5mm pad smallest

Route: 0.1mm / 0.1mm smallest