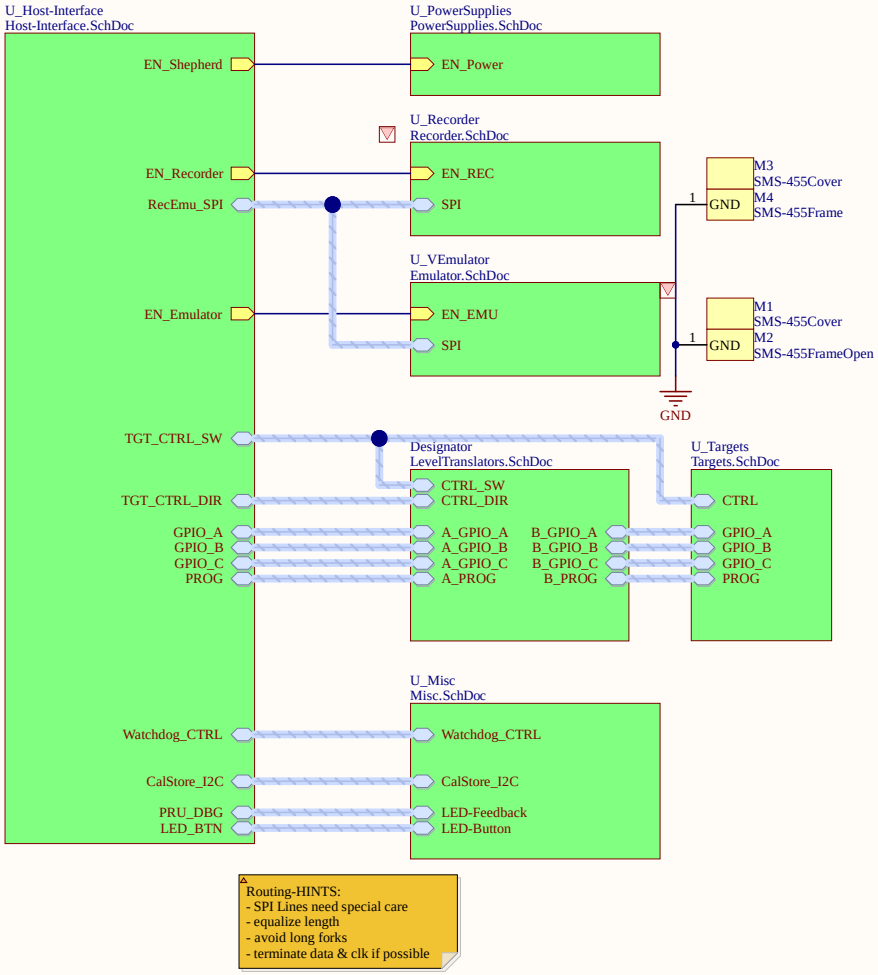
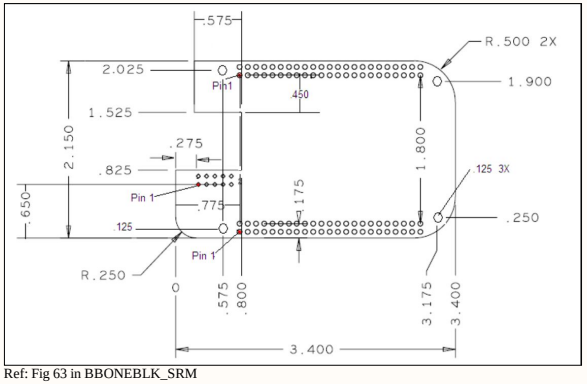


Routing-HINTS:
- SPI Lines need special care
- equalize length
- avoid long forks
- terminate data & clk if possible



Ref: Fig 63 in BBONEBLK_SRM

PCB Manufacturing Constraints

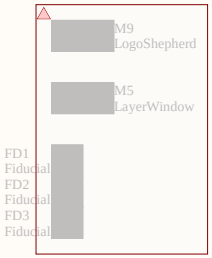
- Size 54.1 x 75.2 mm, 4 Layer
- 0.15 mm Track Width
- 0.15 mm Copper Clearance
- 0.38 mm Edge Clearance
- 0.35 mm Toolsize / non plated Hole
- 0.25 mm Plated Hole (End-)Size
- 0.125 mm Annular Ring
- 2.54 mm milling radius
- Solder Paste Pads are optimized for a 90 - 110 um Stencil

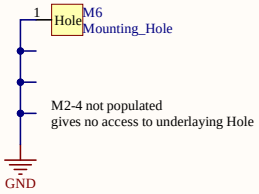
Assembly (v2.2)

- 2 Variations, recorder / emulator are self-contained and optional
  - with Rec & Emu -> 276 parts, 42 unique
  - with Emu -> 253 parts, 46 unique
- Mech-15 contains Pick and Place Info
  - cross (+) marks origin of part,
  - chamfered edge and circle mark pad 1 of ICs
  - "C" marks cathode of diodes
- Mech-2 contains Top Part Designators
- smallest part 0402
- smallest pitch 0.5 mm, QFN
- only top layer populated

Manual Assembly
- Mech-13 contains info about non-reflow parts (8 items)

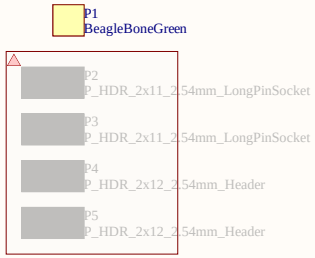
Misc





M2-4 not populated
gives no access to underlaying Hole

BOM-Additions



External-BOM

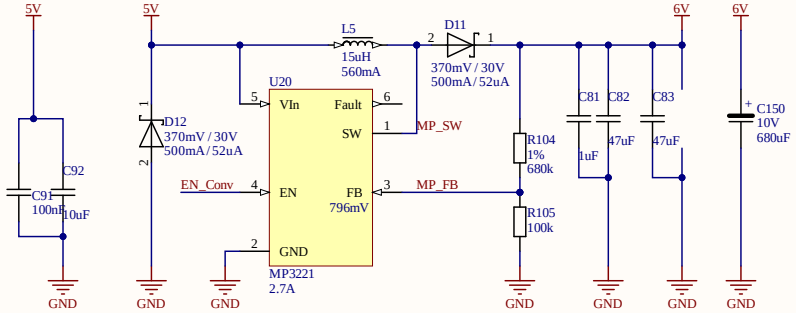
USB-Stick 256 GB
Ethernet Cables
POE-Adapter
uSD-Card (for flashing)

Calibration Resistors
1k-0603-0.05% 667-ERA-3ARW102V
100R-0603-0.05% 754-RG1608N-101-W-T1

Pinheader Connection BBone Variants
2x23 Header -> 77313-802-46LF 1.3 €
2x23 LongPinSocket
Samtec SSQ-123-23-G-D or 03-G-D 6 € (Default in BOM)
Major League SSHQ-123-D-10-G-LF 3 €
2x11 LongPinSocket & 2x12 Header
Samtec SSQ-111-03-G-D 3 €
Amphenol 10129381-924003BLF 0.4 €

Title	Shepherd - Overview NES Lab / TU Dresden	
Size: A4	Number	Revision
Date: 8.01.2022		Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\overview.SchDoc		Drawn By: Ingmar

BoostConverter

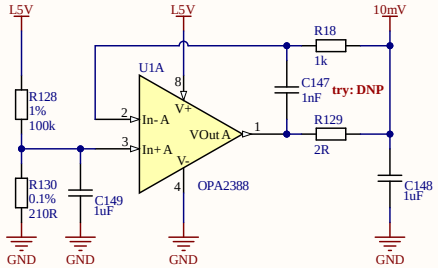


Vout 6.2088 V, 1% range is [6.102; 6.318] V

I_out [36; 166] mA
dV_out <= 9.2 - 42 uV (min/max load) Output-Ripple

L_Opt = 20 uH

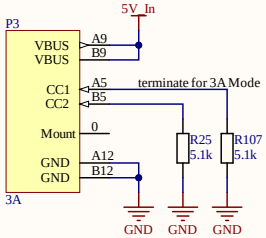
Reference-Offset

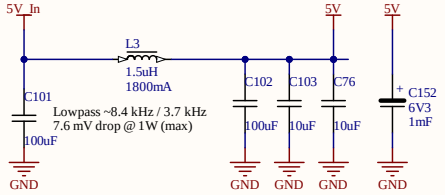


Lowpass ~1.6 Hz

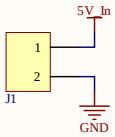
Lowpass ~1.6 kHz

External Power Input

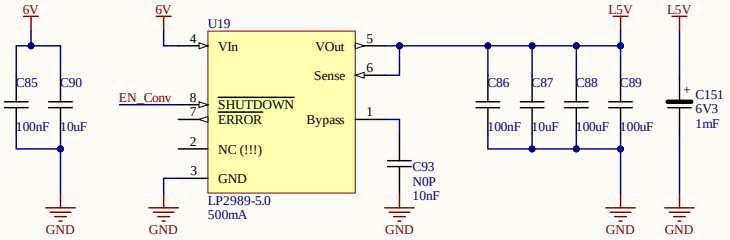


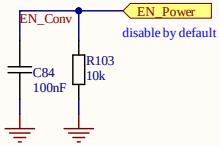


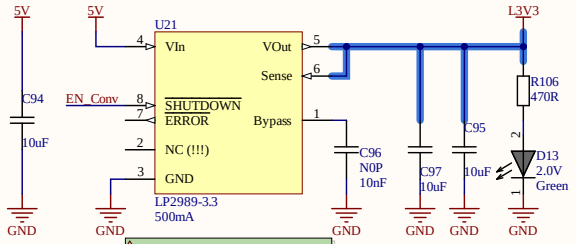
MAX 5V



LowNoise LDOs







Recommended:
- 10nF NP0 Bypass (low Leakage)
- VIn >= VOut + 1V

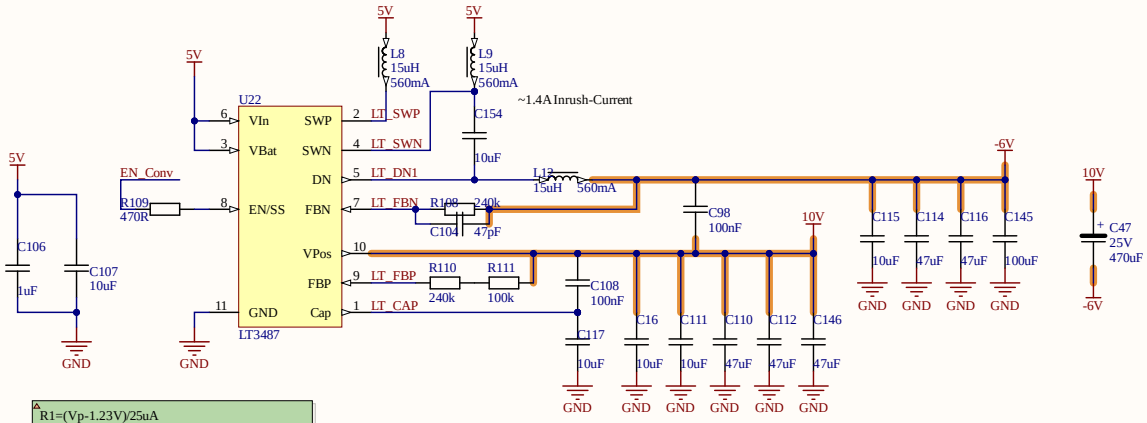
Consumption:
- Disabled < 2 mA
- Enabled 67 mA @ 5.1 V (Emu & Rec)
- BB 390 mA during boot, 170 to 240 mA later

Shepherd ON	272 mW (Emu only)	
	18mW @ 3V	144mW @ 5V
	36mW @ 6V	37mW @ 16V
Shepherd ON	401 mW (Emu & Rec)	
	18mW @ 3V	198mW @ 5V
	36mW @ 6V	101mW @ 16V
Shepherd MAX	1121mW (both targets drain 50mA)	
	20mW @ 3V	795mW @ 5V
	36mW @ 6V	101mW @ 16V

Main Voltages:

A5V/L5V	-> 5.000 V	Should be Spot On
L3V3	-> 3.300 V	Should be Spot On
6V	-> 5.38 V	[5.29; 5.47] V with 1% Res
10V	-> 9.73 V	[9.56; 9.90] V with 1% Res
-6V	-> -6 V,	[5.94; 6.06] V with 1% Res

Boost & Inverter



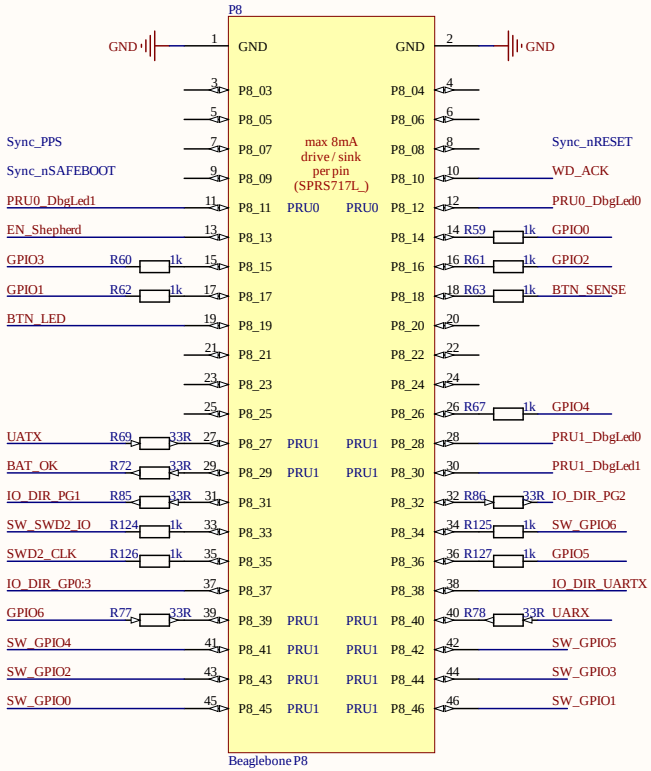
R1=(Vp-1.23V)/25uA
R1=350.8 kOhm (10V)
340kOhm -> 9.73V @1%

R2=-Vn/25uA
R2=240 kOhm (-6V)

Regulator drives at least 50mA on both Outputs

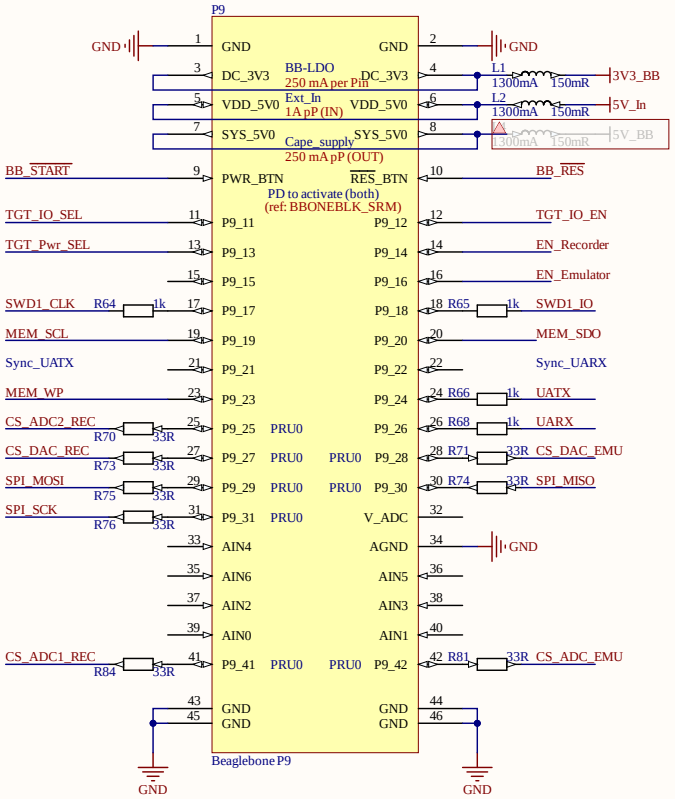
Title	Shepherd - Power Supplies NES Lab / TU Dresden		
Size	Number		Revision
A4			
Date:	8.01.2022	Sheet of	shepherd_v2.PrjPcb
File:	C:\Users\..\PowerSupplies.SchDoc	Drawn By:	Ingmar

Beaglebone Pinheader P8

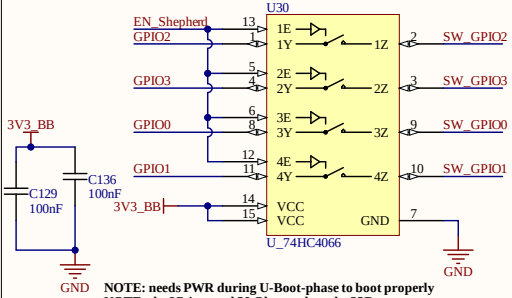


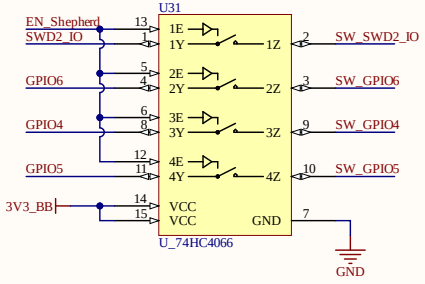
NOTE: order looks messed up, but ensures a proper boot
P8-31:46 are responsible for bootconfig of beaglebone
Most Important: P8 - 31:34 & 41:46

Beaglebone Pinheader P9



Uninterrupted U-Boot-Config





NOTE: needs PWR during U-Boot-phase to boot properly
NOTE: the IC-internal 50 Ohm replace the 33R

Pin-Mapping is documented in

-> concept_hw_beagle_pinout.xls

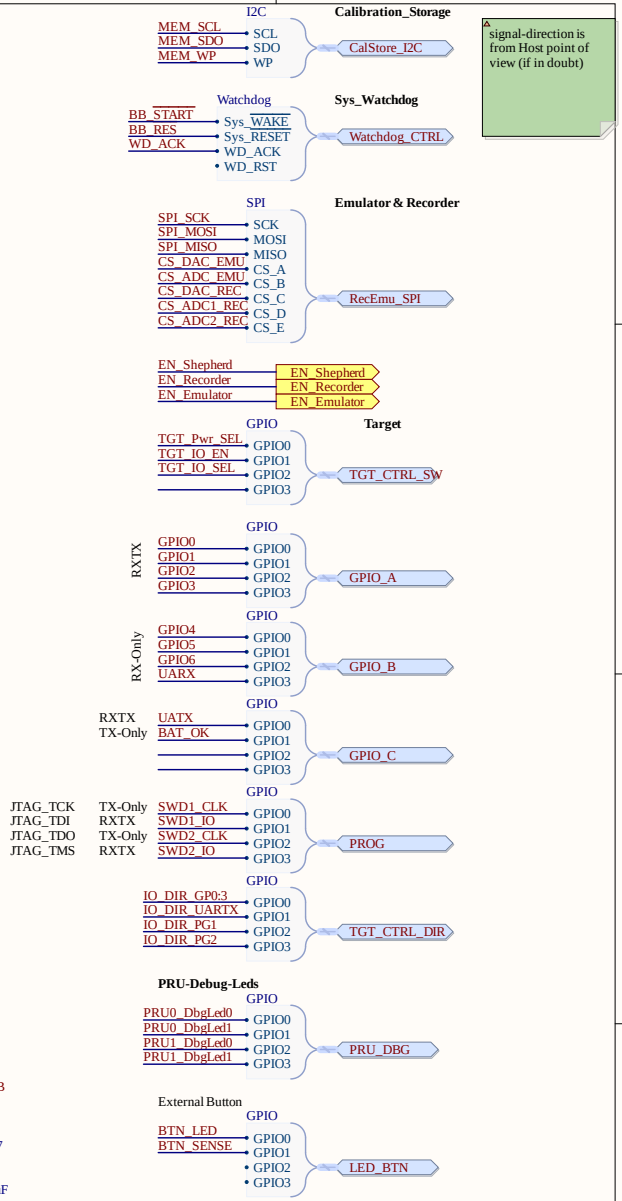
target_io is doubled for pru-timestamping - pru-io is not flexible, no dir-change during runtime

Behaviour on Shutdown:

3V3	0V
VDD5V	0V
SYS5V	1.16V
PWR_BTN	3.74V
nRES_BTN	0.15V

nSTART: BB_PCB has nothing discrete except switch to GND

nRST: BB_PCB has 10k PU & 2.2 uF Buffer & switch to GND



Title	Shepherd - Host Interface NES Lab / TU Dresden		
Size A4	Number	Revision	
Date:	8.01.2022	Sheet of	shepherd_v2.PrjPcb
File:	C:\Users\..\Host-Interface.SchDoc	Drawn By:	Ingmar

Signal-Propagation-Delay
DAC8562 7-10 us Settling, 0.75 V/us Slew
OPAx388 2 us Settling (0.01%), 5.0 V/us Slew rate
INA190 0.8 us Settling (0.001%), 35 V/us Slew rate
ADS8691 665 ns conversion, 335 ns acquisition

Noise-Estimate
ADS8691:
- unipolar mode 0 .. 5.12V @ 18bit, LSB = 19.53 uV
- integral nonlin +- 2 LSB
- 90 dB SNR
AD8421:
- Inp. Voltage Noise 3.2 nV/sqrtHz
- Outp. Voltage Noise 60 nV / sqrtHz
OPA388 / OPA2388:
- Noise 7nV/sqrtHz, 100fA/sqrtHz
- no 1/f-Noise: 140 nVpp
DAC8562:
- noise density 90 nV / sqrtHz
- output noise 2.6 uVpp
- crosstalk 5 / 15uV (Ext / Int Reference)
- 16 bit, LSB = 76 uV

InAmpNoise Peak2Peak Voltage with 16kHz BW and variable Input-Resistor
-> see maxima-sheet "OpAmpNoiseCalculation.wxmx"

InpRes	AD8421	AD8429
0.1 kOhm	2.9 uV	1.76 uV
1 kOhm	5.05 uV	4.72 uV
10 kOhm	14.0 uV	21.1 uV
100 kOhm	48 uV	167 uV

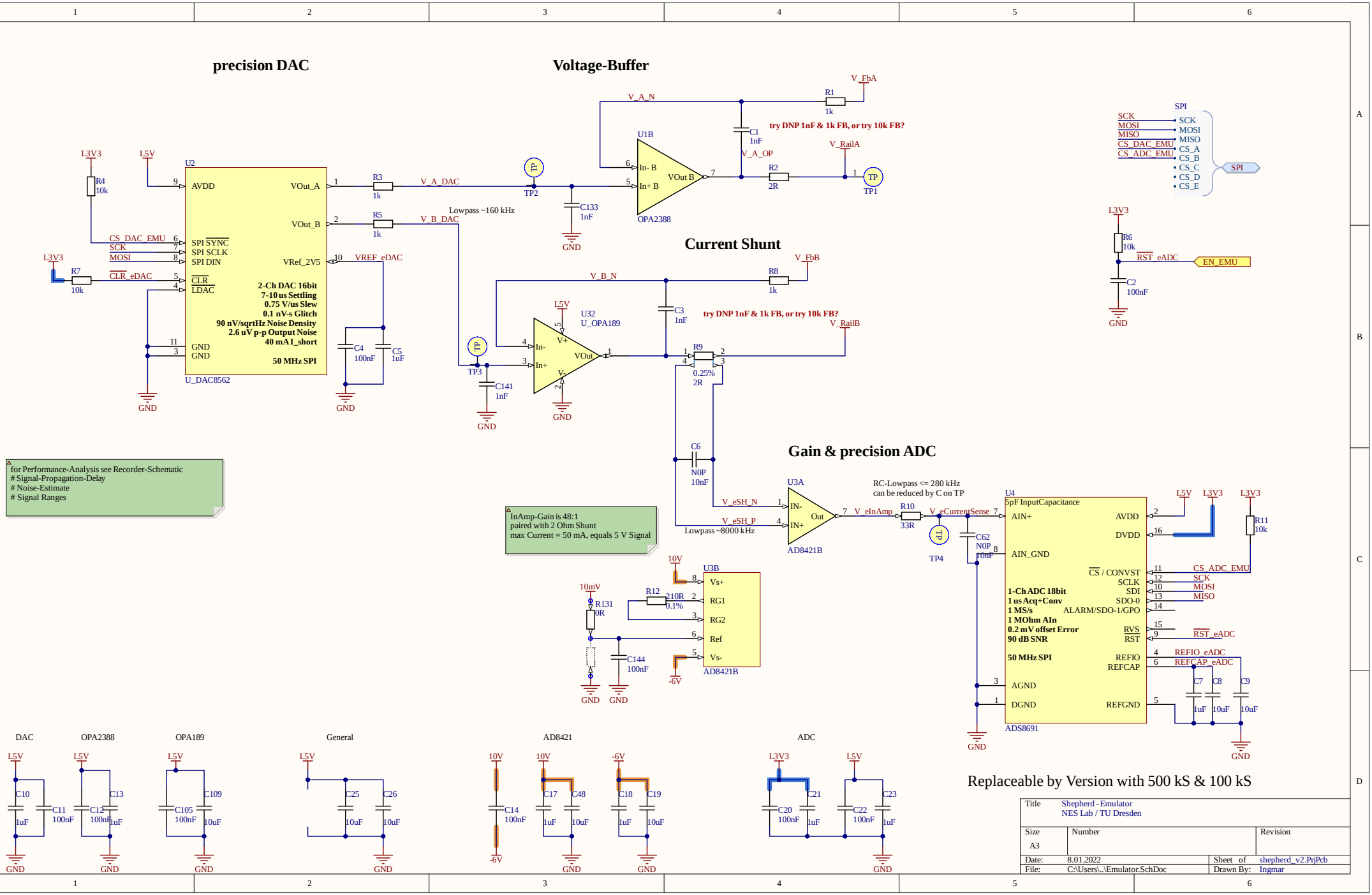
Signal Ranges
DAC8562 -> 0 .. AVDD (max) ->
default Gain=1 for VRefExt or 2 for VRefInt (modd
V_out = (Dln / 2^16) * VRef * Gain

Voltage Buffer
Emulate V_Sim of Converter
Harvest-Port
precision ADCs
precision DAC
Harvest Voltage-Matching
Current Sensing

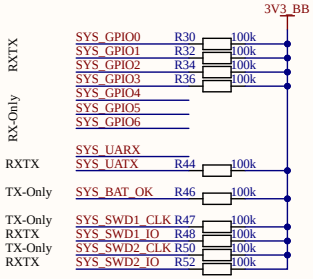
InAmp-Gain is 48:1
paired with 2 Ohm Shunt
max Current = 50 mA, equals 5 V Signal

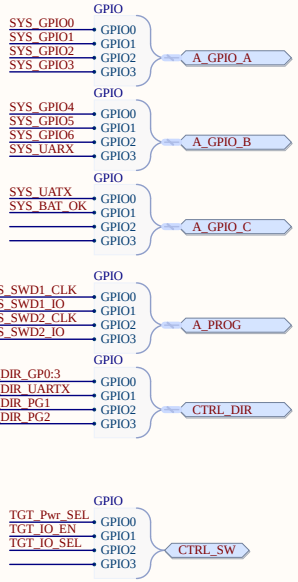
DAC
OPA2388
OPA189
AD8421
Upper ADC
Lower ADC

Title	Shepherd - Recorder NES Lab / TU Dresden	
Size A3	Number	Revision
Date: 8.01.2022		Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\Recorder.SchDoc		Drawn By: Kai

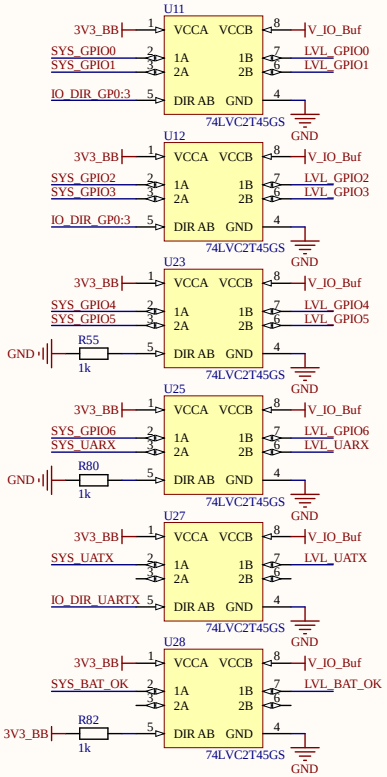

precision DAC
Voltage-Buffer
Current Shunt
Gain & precision ADC
U_DAC8562
OPA2388
U_OPA189
AD8421B
ADS8691
Lowpass ~160 kHz
Lowpass ~8000 kHz
RC-Lowpass <= 280 kHz
can be reduced by C on TP
try DNP 1nF & 1k FB, or try 10k FB?
for Performance-Analysis see Recorder-Schematic
Signal-Propagation-Delay
Noise-Estimate
Signal Ranges
InAmp-Gain is 48:1
paired with 2 Ohm Shunt
max Current = 50 mA, equals 5 V Signal
SPI
DAC
OPA2388
OPA189
General
AD8421
ADC
Replaceable by Version with 500 kS & 100 kS
Title Shepherd - Emulator
NES Lab / TU Dresden
Size A3
Number
Revision
Date: 8.01.2022
Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\Emulator.SchDoc
Drawn By: Ingmar

SideA - Pull Ups

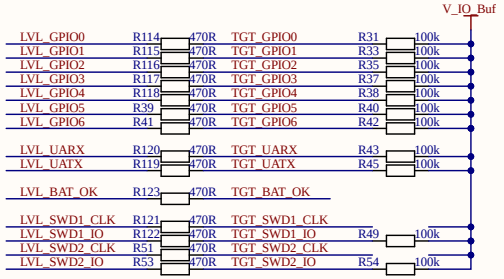


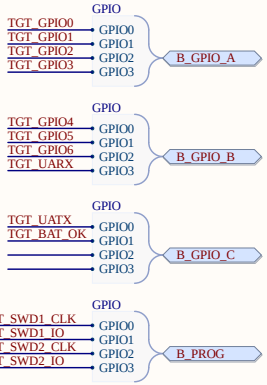


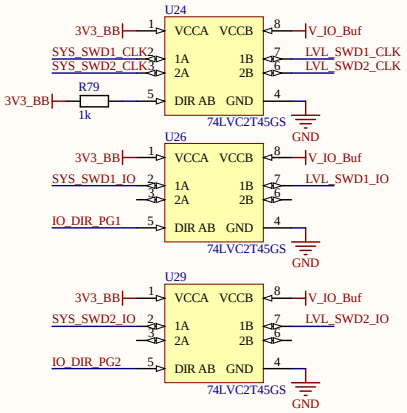
Level Translators

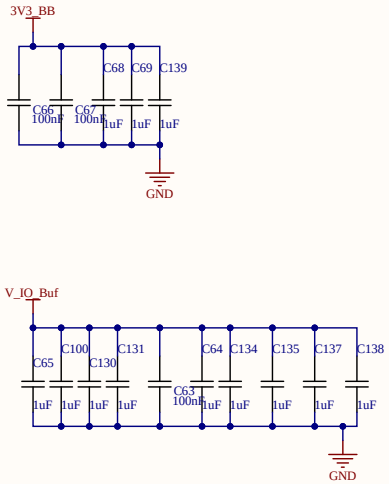


SideB - Pull Ups

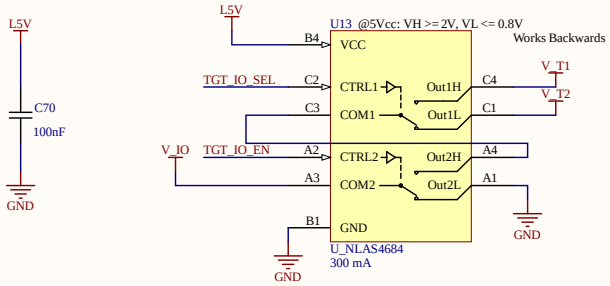




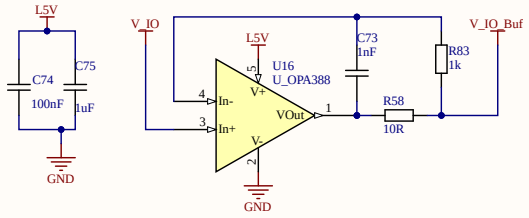




IO-Voltage - Reverse Routing Switch



IO-Voltage - Buffer



Title	Shepherd - Level Translators NES Lab / TU Dresden	
Size A3	Number	Revision
Date: 8.01.2022	Sheet of shepherd_v2.PrjPcb	
File: C:\Users\..\LevelTranslators.SchDoc	Drawn By: Ingmar	

Signal Switches

SEL	Tar1	Tar2
0	VA	VB
1	VB	VA

only VB has current-tracking
-> so SEL=1 enables tracking of Target 1
0 enables tracking of Target 2

GPIO
TGT_PWR_SEL
TGT_IO_EN
TGT_IO_SEL
GPIO0
GPIO1
GPIO2
GPIO3
CTRL

GPIO
TGT_GPIO0
TGT_GPIO1
TGT_GPIO2
TGT_GPIO3
GPIO_A

GPIO
TGT_GPIO4
TGT_GPIO5
TGT_GPIO6
TGT_UARX
GPIO_B

GPIO
TGT_UATX
TGT_BAT_OK
GPIO_C

GPIO
TGT_SWD1_CLK
TGT_SWD1_IO
TGT_SWD2_CLK
TGT_SWD2_IO
PROG

U34 U_PI5A4158ZA 100 mA
L5V, GND
TGT_IO_SEL, TGT_GPIO6, TGT_UARX
T1_GPIO6, T2_GPIO6, T1_UARX, T2_UARX

U36 U_PI5A4158ZA 100 mA
TGT_IO_SEL, TGT_GPIO0, TGT_GPIO1
T1_GPIO0, T2_GPIO0, T1_GPIO1, T2_GPIO1

U37 U_PI5A4158ZA 100 mA
TGT_IO_SEL, TGT_UATX, TGT_BAT_OK
T1_UATX, T2_UATX, T1_BAT_OK, T2_BAT_OK

U38 U_PI5A4158ZA 100 mA
TGT_IO_SEL, TGT_GPIO2, TGT_GPIO3
T1_GPIO2, T2_GPIO2, T1_GPIO3, T2_GPIO3

U39 U_PI5A4158ZA 100 mA
TGT_IO_SEL, TGT_SWD1_CLK, TGT_SWD2_CLK
T1_SWD1_CLK, T2_SWD1_CLK, T1_SWD2_CLK, T2_SWD2_CLK

U40 U_PI5A4158ZA 100 mA
TGT_IO_SEL, TGT_GPIO4, TGT_GPIO5
T1_GPIO4, T2_GPIO4, T1_GPIO5, T2_GPIO5

U41 U_PI5A4158ZA 100 mA
TGT_IO_SEL, TGT_SWD1_IO, TGT_SWD2_IO
T1_SWD1_IO, T2_SWD1_IO, T1_SWD2_IO, T2_SWD2_IO

L5V
C122 100nF, C123 100nF, C124 100nF, C125 100nF, C126 100nF
C127 100nF, C128 100nF
GND

Power Switches

U33 U_NLAS4684 300 mA
L5V, GND
V_RailA, TGT_PWR_SELC2, V_FbA
V_T1, V_T2, V_FB1, V_FB2
V_T1 NT2 V_FB1
V_T2 NT3 V_FB2

U35 U_NLAS4684 300 mA
L5V, GND
V_RailB, TGT_PWR_SELC2, V_FbB
(current-tracking)
V_T1, V_T2, V_FB1, V_FB2

@5Vcc: VH >= 2V, VL <= 0.8V

Target Ports

P10 P_HDR_2x9_2.54mm_header
V_T1, C118 100nF, L3V3, C119 1uF, GND
T1_GPIO0, T1_GPIO1, T1_GPIO2, T1_GPIO3, T1_GPIO4, T1_GPIO5, T1_GPIO6, T1_UARX, T1_UATX, T1_BAT_OK
T1_SWD1_CLK, T1_SWD1_IO, T1_SWD2_CLK, T1_SWD2_IO

P11 P_HDR_2x9_2.54mm_header
V_T2, C120 100nF, L3V3, C121 1uF, GND
T2_GPIO0, T2_GPIO1, T2_GPIO2, T2_GPIO3, T2_GPIO4, T2_GPIO5, T2_GPIO6, T2_UARX, T2_UATX, T2_BAT_OK
T2_SWD1_CLK, T2_SWD1_IO, T2_SWD2_CLK, T2_SWD2_IO

rotation save & "shielded"

LED-Feedback for PWR-State

L3V3
TargetA D16 2.0V Green
TargetB D17 Green 2.0V
R112 1k, R113 1k
U15A HCT2G04
TGT_PWR_SEL, TGT_PWR_nSEL
InvertBuffer
GND

LED-Feedback for IO-State

L3V3
U15B HCT2G04
U14 TC7WH08FK
TGT_IO_EN, TGT_IO_SEL, TGT_IO_nSEL
R56 1k, R57 1k
D3 2.0V Amber, D4 2.0V Amber
TargetA, TargetB
C71 100nF, C72 1uF
GND

Programming-Hints:
- Equalize DACs before switching
- unused GPIO should be switched to Input (target and bbone)
- level translators can be switched to other target for low leakage

Leakage Analysis (max per Pin):

NLAS4684	1-2 nA
NXS0101	1 uA
LSF010x	1-5 uA

Max Current:

Target Switches	300mA
3V3 (unmonitored)	250mA

V_Target -> OPA#388 VoltageBuffers source 30-60mA, current measurement up to 50mA

Programming Target:

SWD	-> nRF52, STM32L4
SBW	-> MSP430, MSP432, CC430

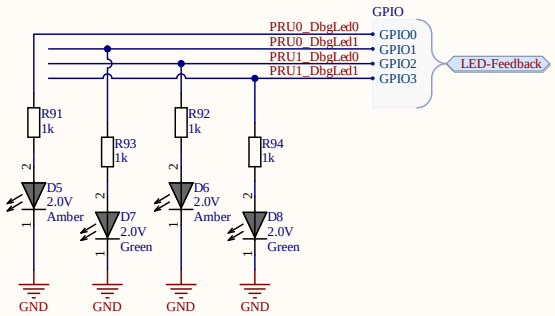
SBW-TDIO, -TCK (nRST/NMI)

Title	Shepherd - Target Interface NES Lab / TU Dresden	
Size A3	Number	Revision
Date: 8.01.2022		Sheet of shepherd_v2.PrjPcb
File: C:\Users\..\Targets.SchDoc		Drawn By: Ingmar

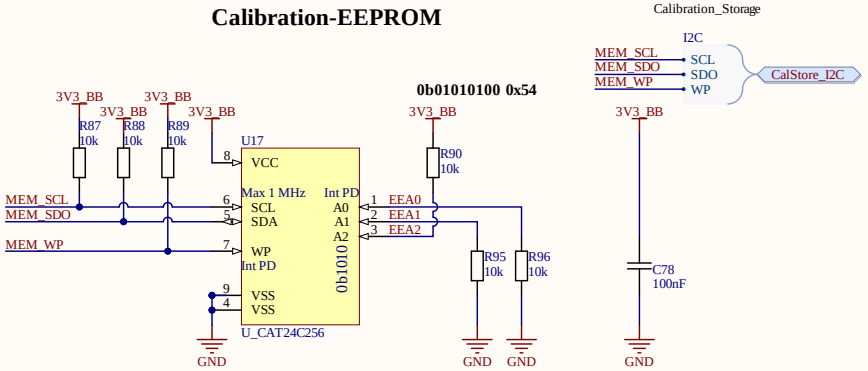
TODO:
Separate into smaller Individual Schem

Possible Changes:
- LED Button could be designed with just 3 Leads, or even 2
- One LED per PRU is enough

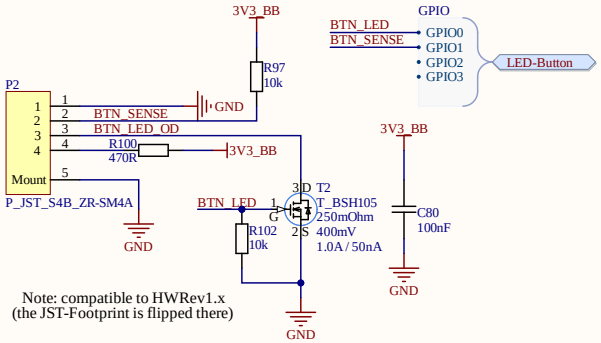
PRU-LED-Feedback



Calibration-EEPROM



Local Control Button

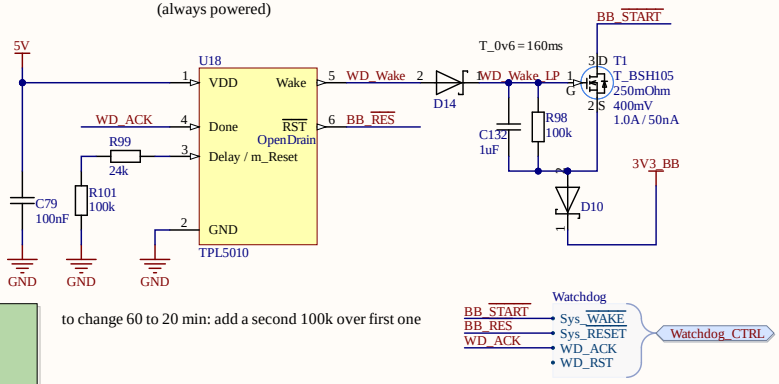


Note: compatible to HWRev1.x
(the JST-Footprint is flipped there)

schematic changed to avoid internal voltages on cable

Watchdog

(always powered)



BB-Behaviour on Shutdown:

3V3	0V
VDD5V	0V
SYS5V	1.16V

nSTART: BB_PCB has nothing discrete except pull-switch to GND, normally 5V Signal
-> use 3V3 as Pull-Down to only get affected by wake-signal when BB is powered off -> seems fine

nRST: BB_PCB has 10k PU & 2.2 uF Buffer & pull-switch to GND

to change 60 to 20 min: add a second 100k over first one

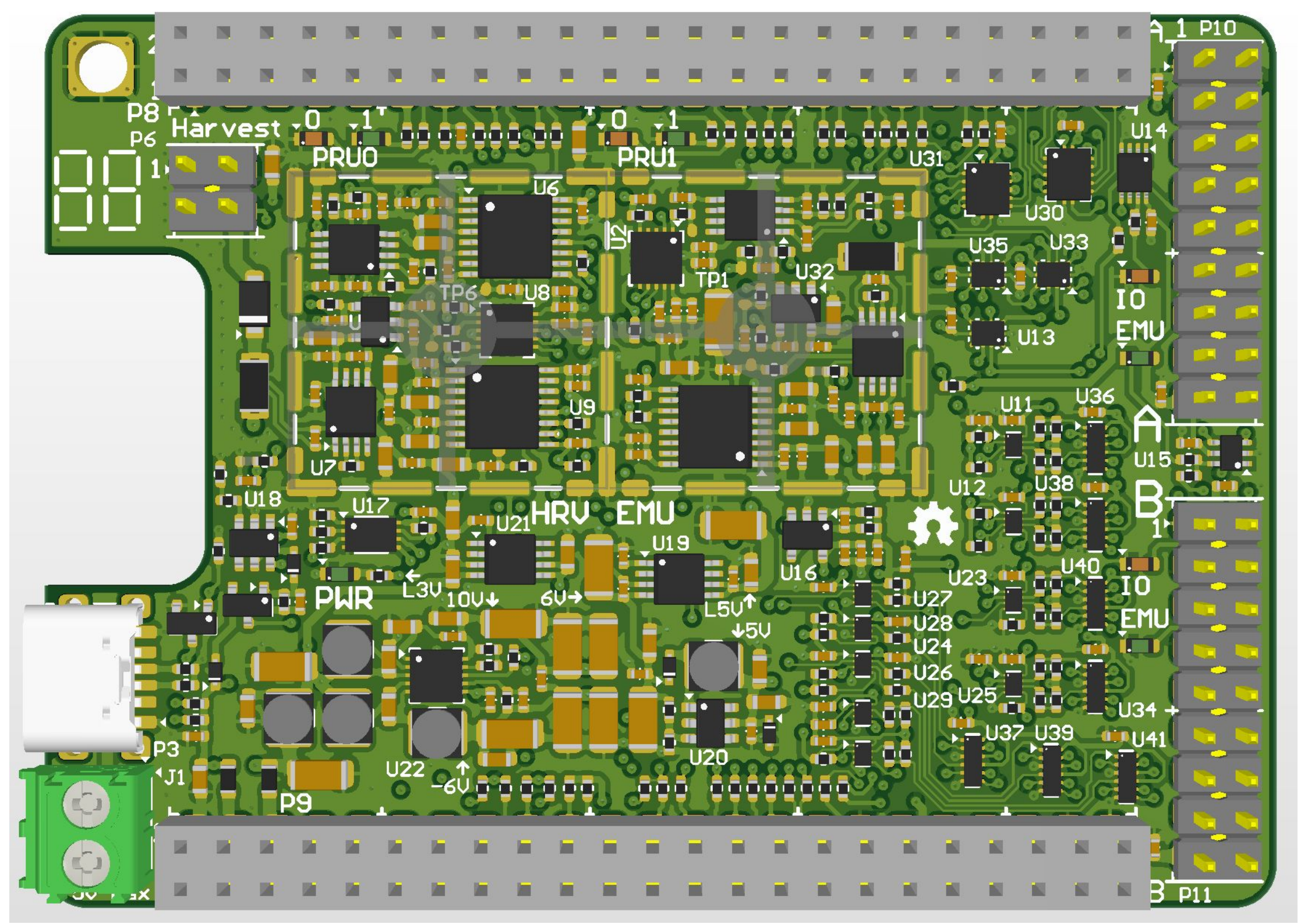
Watchdog - Advantages:
- nodes are in remote rooms, often without access
- Fallback if we can't control POE-Power of ports (most likely)
- with a WD the BB can shut down and be woken up periodically
- routine: BB aks server for tasks, waits or goes to sleep if NOP

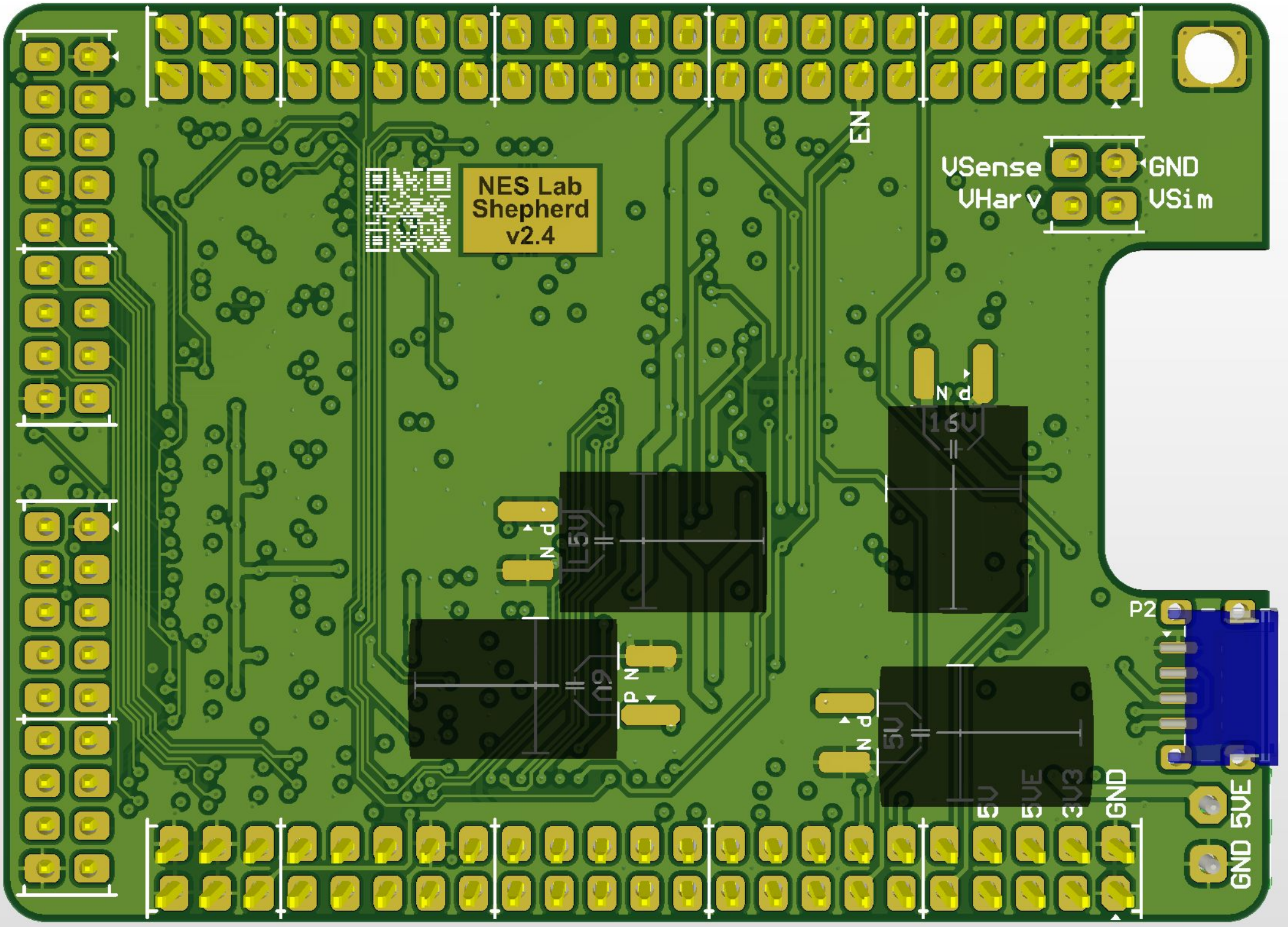
TPL5000 Watchdog behaviour:
- time-delay is configured via resistor (100ms .. 2h)
- "wake" is triggered for 31 ms on timer-match -> LowPass to 150 ms
- wake only reaches BB if 3V3_BB is at GND-Level (BB Shutdown)
- system has to confirm wake by triggering "done"
- if "done" is not triggered before next "wake" a reset occurs

R_Delay	T_Delay
057 kOhm	10 min
077 kOhm	20 min
092 kOhm	30 min
125 kOhm	60 min
150 kOhm	90 min
170 kOhm	120 min

A RTC (i.e. PCF2129 with Linux-Drivers) with alarm-timer and watchdog would be prefered, but both functions are only triggered ONCE without interaction. So if the BB gets woken but fails to boot there will never be a reset.

Title	Shepherd - Misc NES Lab / TU Dresden	
Size: A4	Number	Revision
Date: 8.01.2022	Sheet of	shepherd_v2.PrjPcb
File: C:\Users\..\Misc.SchDoc	Drawn By:	Ingmar


P8
P6
Harvest
0
1
PRU0
PRU1
U6
U8
U9
U7
TP6
TP1
U31
U30
U14
U35
U33
U32
U13
IO
EMU
U11
U36
U15
U12
U38
U18
U17
U21
HRV
EMU
U19
U16
U23
U40
U27
U28
U24
U26
U29
U25
U34
U37
U39
U41
U20
U22
PWR
L3V
10V
6V
L5V
5V
-6V
P3
J1
P9
P10
P11
A
B


NES Lab
Shepherd
v2.4
EN
VSense
VHarv
GND
VSim
P2
GND
5VE
GND
5VE
3V3
5V
16V
19V