Flash 16Mbit (2Mx8)

3V Only Serial Flash Memory with Dual

■ FEATURES

- Single supply voltage 2.7~3.6V
- Standard, Dual SPI
- Speed
  - Read max frequency: 33MHz
  - Fast Read max frequency: 50MHz; 100MHz
  - Fast Read Dual max frequency: 50MHz / 100MHz (100MHz / 200MHz equivalent Dual SPI)
- Low power consumption
  - Active current: 35 mA
  - Standby current: 30μA
- Reliability
  - 100,000 typical program/erase cycles
  - 20 years Data Retention
- Program
  - Byte programming time: 7μs (typical)
  - Page programming time: 1.5 ms (typical)
- Erase
  - Chip erase time 90 sec (typical)
  - Block erase time 1 sec (typical)
  - Sector erase time 90 ms (typical)
- Page Programming
  - 256 byte per programmable page
- Auto Address Increment (AAI) WORD Programming
  - Decrease total chip programming time over Byte Program operations
- Lockable 4K OTP security sector
- SPI Serial Interface
  - SPI Compatible: Mode 0 and Mode 3
- End of program or erase detection
- Write Protect ($\overline{WP}$)
- Hold Pin ($\overline{HOLD}$)
- All Pb-free products are RoHS-Compliant

■ ORDERING INFORMATION

Product ID	Speed	Package		COMMENTS
F25L16PA –50PAG	50MHz	8 lead SOIC	200mil	Pb-free
F25L16PA –100PAG	100MHz	8 lead SOIC	200mil	Pb-free
F25L16PA –50DG	50MHz	8 lead PDIP	300mil	Pb-free
F25L16PA –100DG	100MHz	8 lead PDIP	300mil	Pb-free

■ GENERAL DESCRIPTION

The F25L16PA is a 16Megabit, 3V only CMOS Serial Flash memory device organized as 2M bytes of 8 bits. The device supports the standard Serial Peripheral Interface (SPI), and a Dual SPI. ESMT's memory devices reliably store memory data even after 100,000 programming and erase cycles.

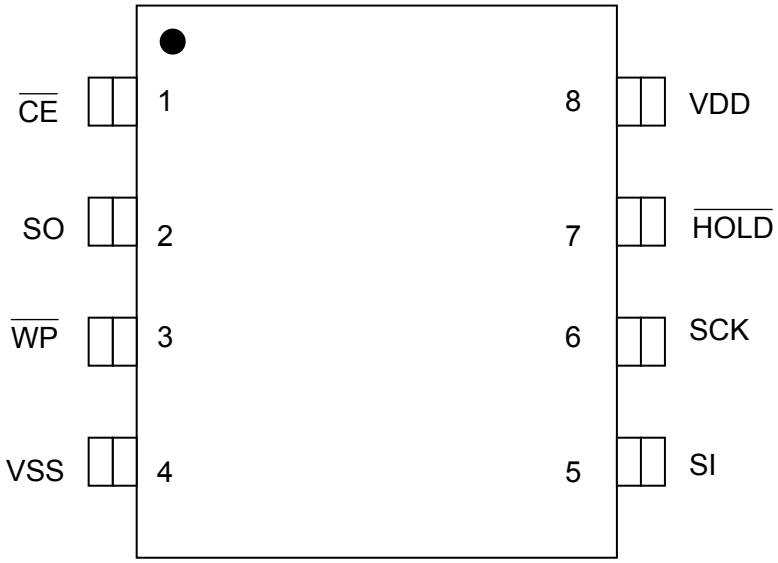
The memory array can be organized into 8,192 programmable pages of 256 byte each. 1 to 256 byte can be programmed at a time with the Page Program instruction. The device also can be programmed to decrease total chip programming time with Auto Address Increment (AAI) programming.

The device features sector erase architecture. The memory array is divided into 512 uniform sectors with 4K byte each; 32 uniform blocks with 64K byte each. Sectors can be erased individually without affecting the data in other sectors. Blocks can be erased individually without affecting the data in other blocks. Whole chip erase capabilities provide the flexibility to revise the data in the device. The device has Sector, Block or Chip Erase but no page erase.

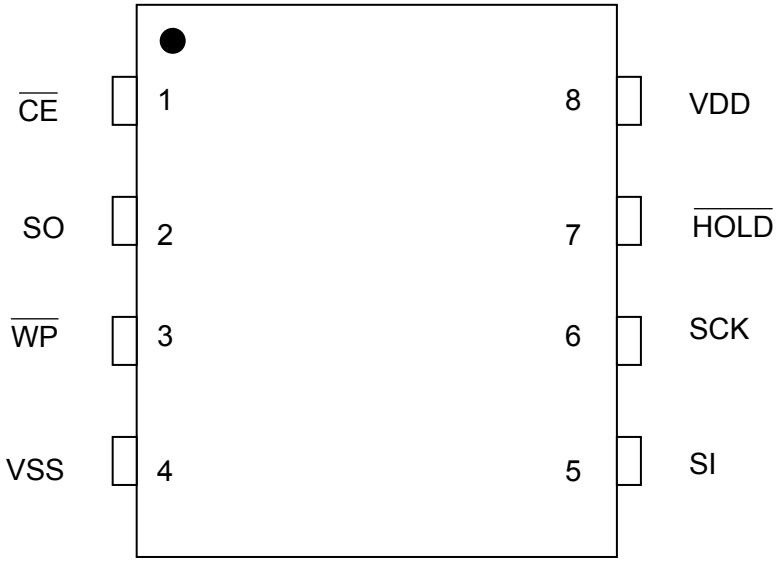
The sector protect/unprotect feature disables both program and erase operations in any combination of the sectors of the memory.

■ PIN CONFIGURATIONS

8-PIN SOIC



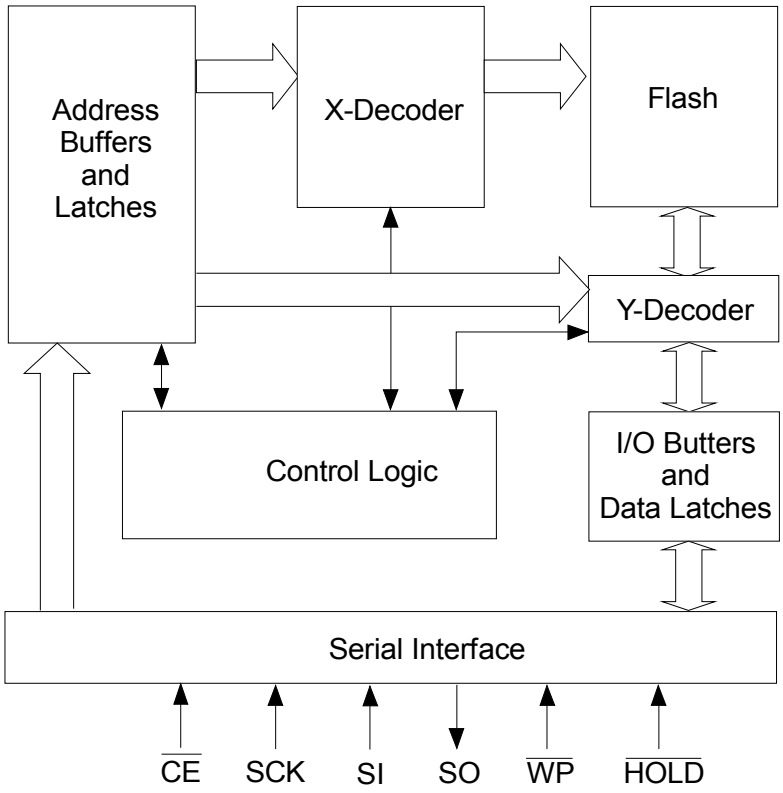
8-PIN PDIP



■ PIN DESCRIPTION

Symbol	Pin Name	Functions
SCK	Serial Clock	To provide the timing for serial input and output operations
SI	Serial Data Input	To transfer commands, addresses or data serially into the device. Data is latched on the rising edge of SCK.
SO	Serial Data Output	To transfer data serially out of the device. Data is shifted out on the falling edge of SCK.
$\overline{CE}$	Chip Enable	To activate the device when $\overline{CE}$ is low.
$\overline{WP}$	Write Protect	The Write Protect ($\overline{WP}$) pin is used to enable/disable BPL bit in the status register.
$\overline{HOLD}$	Hold	To temporality stop serial communication with SPI flash memory without resetting the device.
VDD	Power Supply	To provide power.
VSS	Ground	

■ FUNCTIONAL BLOCK DIAGRAM



■ SECTOR STRUCTURE

Table 1: F25L16PA Sector Address Table

Block	Sector	Sector Size (Kbytes)	Address range	Block Address				
				A20	A19	A18	A17	A16
31	511	4KB	1FF000H – 1FFFFFH	1	1	1	1	1
	:	:	:					
	496	4KB	1F0000H – 1F0FFFH					
30	495	4KB	1EF000H – 1EFFFFH	1	1	1	1	0
	:	:	:					
	480	4KB	1E0000H – 1E0FFFH					
29	479	4KB	1DF000H – 1DFFFFH	1	1	1	0	1
	:	:	:					
	464	4KB	1D0000H – 1D0FFFH					
28	463	4KB	1CF000H – 1CFFFFH	1	1	1	0	0
	:	:	:					
	448	4KB	1C0000H – 1C0FFFH					
27	447	4KB	1BF000H – 1BFFFFH	1	1	0	1	1
	:	:	:					
	432	4KB	1B0000H – 1B0FFFH					
26	431	4KB	1AF000H – 1AFFFFH	1	1	0	1	0
	:	:	:					
	416	4KB	1A0000H – 1A0FFFH					
25	415	4KB	19F000H – 19FFFFH	1	1	0	0	1
	:	:	:					
	400	4KB	190000H – 190FFFH					
24	399	4KB	18F000H – 18FFFFH	1	1	0	0	0
	:	:	:					
	384	4KB	180000H – 180FFFH					
23	383	4KB	17F000H – 17FFFFH	1	0	1	1	1
	:	:	:					
	368	4KB	170000H – 170FFFH					
22	367	4KB	16F000H – 16FFFFH	1	0	1	1	0
	:	:	:					
	352	4KB	160000H – 160FFFH					
21	351	4KB	15F000H – 15FFFFH	1	0	1	0	1
	:	:	:					
	336	4KB	150000H – 150FFFH					
20	335	4KB	14F000H – 14FFFFH	1	0	1	0	0
	:	:	:					
	320	4KB	140000H – 140FFFH					
19	319	4KB	13F000H – 13FFFFH	1	0	0	1	1
	:	:	:					
	304	4KB	130000H – 130FFFH					

Table 1: F25L16PA Sector Address Table – continued I

Block	Sector	Sector Size (Kbytes)	Address range	Block Address				
				A20	A19	A18	A17	A16
18	303	4KB	12F000H – 12FFFFH	1	0	0	1	0
	:	:	:					
	288	4KB	120000H – 120FFFH					
17	287	4KB	11F000H – 11FFFFH	1	0	0	0	1
	:	:	:					
	272	4KB	110000H – 110FFFH					
16	271	4KB	10F000H – 10FFFFH	1	0	0	0	0
	:	:	:					
	256	4KB	100000H – 100FFFH					
15	255	4KB	0FF000H – 0FFFFFH	0	1	1	1	1
	:	:	:					
	240	4KB	0F0000H – 0F0FFFH					
14	239	4KB	0EF000H – 0EFFFFH	0	1	1	1	0
	:	:	:					
	224	4KB	0E0000H – 0E0FFFH					
13	223	4KB	0DF000H – 0DFFFFH	0	1	1	0	1
	:	:	:					
	208	4KB	0D0000H – 0D0FFFH					
12	207	4KB	0CF000H – 0CFFFFH	0	1	1	0	0
	:	:	:					
	192	4KB	0C0000H – 0C0FFFH					
11	191	4KB	0BF000H – 0BFFFFH	0	1	0	1	1
	:	:	:					
	176	4KB	0B0000H – 0B0FFFH					
10	175	4KB	0AF000H – 0AFFFFH	0	1	0	1	0
	:	:	:					
	160	4KB	0A0000H – 0A0FFFH					
9	159	4KB	09F000H – 09FFFFH	0	1	0	0	1
	:	:	:					
	144	4KB	090000H – 090FFFH					
8	143	4KB	08F000H – 08FFFFH	0	1	0	0	0
	:	:	:					
	128	4KB	080000H – 080FFFH					
7	127	4KB	07F000H – 07FFFFH	0	0	1	1	1
	:	:	:					
	112	4KB	070000H – 070FFFH					
6	111	4KB	06F000H – 06FFFFH	0	0	1	1	0
	:	:	:					
	96	4KB	060000H – 060FFFH					

Table 1: F25L16PA Sector Address Table – continued II

Block	Sector	Sector Size (Kbytes)	Address range	Block Address				
				A20	A19	A18	A17	A16
5	95	4KB	05F000H – 05FFFFH	0	0	1	0	1
	:	:	:					
	80	4KB	050000H – 050FFFH					
4	79	4KB	04F000H – 04FFFFH	0	0	1	0	0
	:	:	:					
	64	4KB	040000H – 040FFFH					
3	63	4KB	03F000H – 03FFFFH	0	0	0	1	1
	:	:	:					
	48	4KB	030000H – 030FFFH					
2	47	4KB	02F000H – 02FFFFH	0	0	0	1	0
	:	:	:					
	32	4KB	020000H – 020FFFH					
1	31	4KB	01F000H – 01FFFFH	0	0	0	0	1
	:	:	:					
	16	4KB	010000H – 010FFFH					
0	15	4KB	00F000H – 00FFFFH	0	0	0	0	0
	:	:	:					
	0	4KB	000000H – 000FFFH					

■ STATUS REGISTER

The software status register provides status on whether the flash memory array is available for any Read or Write operation, whether the device is Write enabled, and the state of the memory Write protection. During an internal Erase or Program operation, the status register may be read only to determine the completion of an operation in progress. Table 2 describes the function of each bit in the software status register.

Table 2: SOFTWARE STATUS REGISTER

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection (See Table 3)	1	R/W
3	BP1	Indicate current level of block write protection (See Table 3)	1	R/W
4	BP2	Indicate current level of block write protection (See Table 3)	1	R/W
5	RESERVED	Reserved for future use	0	N/A
6	AAI	Auto Address Increment Programming status 1 = AAI programming mode 0 = Page Program mode	0	R
7	BPL	1 = BP2,BP1,BP0 are read-only bits 0 = BP2,BP1,BP0 are read/writable	0	R/W

Note:
1. Only BP0, BP1, BP2 and BPL are writable.
2. All register bits are volatility
3. All area are protected at power-on (BP2=BP1=BP0=1)

WRITE ENABLE LATCH (WEL)

The Write-Enable-Latch bit indicates the status of the internal memory Write Enable Latch. If this bit is set to "1", it indicates the device is Write enabled. If the bit is set to "0" (reset), it indicates the device is not Write enabled and does not accept any memory Write (Program/ Erase) commands. This bit is automatically reset under the following conditions:

- Power-up
- Write Disable (WRDI) instruction completion
- Page Program instruction completion
- Auto Address Increment (AAI) Programming is completed and reached its highest unprotected memory address
- Sector Erase instruction completion
- Block Erase instruction completion
- Chip Erase instruction completion
- Write Status Register instructions

BUSY

The BUSY bit determines whether there is an internal Erase or Program operation in progress. A "1" for the BUSY bit indicates the device is busy with an operation in progress. A "0" indicates the device is ready for the next valid operation.

Auto Address Increment (AAI)

The Auto-Address-Increment-Programming-Status bit provides status on whether the device is in AAI Programming mode or Page Program mode. The default at power up is Page Program mode.

Table 3: F25L16PA Block Protection Table

Protection Level	Status Register Bit			Protected Memory Area	
	BP2	BP1	BP0	Block Range	Address Range
0	0	0	0	None	None
Upper 1/32	0	0	1	Block 31	1F0000H – 1FFFFFH
Upper 1/16	0	1	0	Block 30~31	1E0000H – 1FFFFFH
Upper 1/8	0	1	1	Block 28~31	1C0000H – 1FFFFFH
Upper 1/4	1	0	0	Block 24~31	180000H – 1FFFFFH
Upper 1/2	1	0	1	Block 16~31	100000H – 1FFFFFH
All Blocks	1	1	0	Block 0~31	000000H – 1FFFFFH
All Blocks	1	1	1	Block 0~31	000000H – 1FFFFFH

Block Protection (BP2, BP1, BP0)

The Block-Protection (BP2, BP1, BP0) bits define the size of the memory area, as defined in Table 3, to be software protected against any memory Write (Program or Erase) operations. The Write Status Register (WRSR) instruction is used to program the BP2, BP1, BP0 bits as long as $\overline{WP}$ is high or the Block-Protection-Look (BPL) bit is 0. Chip Erase can only be executed if Block-Protection bits are all 0. After power-up, BP2, BP1 and BP0 are set to1.

Block Protection Lock-Down (BPL)

$\overline{WP}$ pin driven low (V_{IL}), enables the Block-Protection-Lock-Down (BPL) bit. When BPL is set to 1, it prevents any further alteration of the BPL, BP2, BP1, and BP0 bits. When the $\overline{WP}$ pin is driven high (V_{IH}), the BPL bit has no effect and its value is "Don't Care". After power-up, the BPL bit is reset to 0.

■ HOLD OPERATION

$\overline{HOLD}$ pin is used to pause a serial sequence underway with the SPI flash memory without resetting the clocking sequence. To activate the $\overline{HOLD}$ mode, $\overline{CE}$ must be in active low state. The $\overline{HOLD}$ mode begins when the SCK active low state coincides with the falling edge of the $\overline{HOLD}$ signal. The HOLD mode ends when the $\overline{HOLD}$ signal's rising edge coincides with the SCK active low state.

If the falling edge of the $\overline{HOLD}$ signal does not coincide with the SCK active low state, then the device enters Hold mode when the SCK next reaches the active low state.

Similarly, if the rising edge of the $\overline{HOLD}$ signal does not coincide with the SCK active low state, then the device exits in Hold mode when the SCK next reaches the active low state. See Figure 1 for Hold Condition waveform.

Once the device enters Hold mode, SO will be in high impedance state while SI and SCK can be V_{IL} or V_{IH}.

If $\overline{CE}$ is driven active high during a Hold condition, it resets the internal logic of the device. As long as $\overline{HOLD}$ signal is low, the memory remains in the Hold condition. To resume communication with the device, $\overline{HOLD}$ must be driven active high, and $\overline{CE}$ must be driven active low. See Figure 23 for Hold timing.

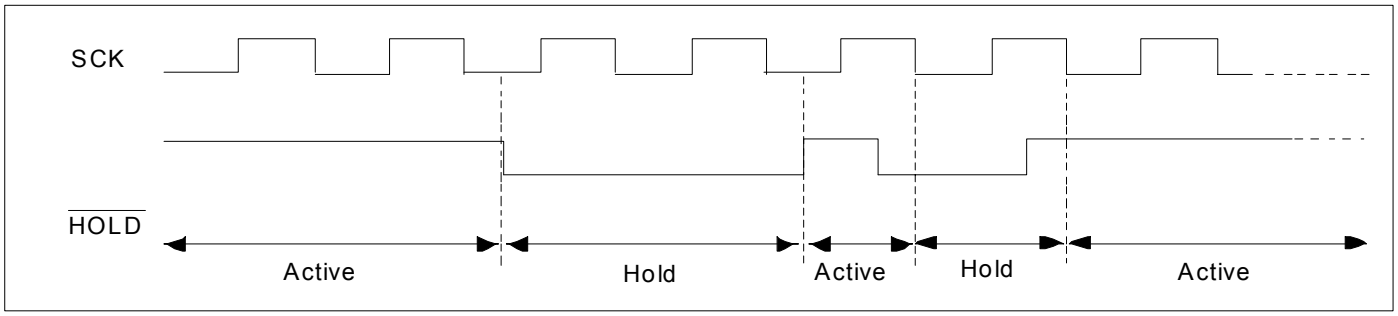


Figure 1: HOLD CONDITION WAVEFORM

■ WRITE PROTECTION

F25L16PA provides software Write Protection.

The Write-Protect pin ($\overline{WP}$) enables or disables the lock-down function of the status register. The Block-Protection bits (BP2, BP1, BP0, and BPL) in the status register provide Write protection to the memory array and the status register. See Table 4 for Block-Protection description.

Write Protect Pin ($\overline{WP}$)

The Write-Protect ($\overline{WP}$) pin enables the lock-down function of the BPL bit (bit 7) in the status register. When $\overline{WP}$ is driven low, the execution of the Write Status Register (WRSR) instruction is determined by the value of the BPL bit (see Table 4). When $\overline{WP}$ is high, the lock-down function of the BPL bit is disabled.

Table 4: CONDITIONS TO EXECUTE WRITE-STATUS-REGISTER (WRSR) INSTRUCTION

$\overline{WP}$	BPL	Execute WRSR Instruction
L	1	Not Allowed
L	0	Allowed
H	X	Allowed

■ INSTRUCTIONS

Instructions are used to Read, Write (Erase and Program), and configure the F25L16PA. The instruction bus cycles are 8 bits each for commands (Op Code), data, and addresses. Prior to executing any Page Program, Auto Address Increment (AAI) Programming, Write Status Register, Sector Erase, Block Erase, or Chip Erase instructions, the Write Enable (WREN) instruction must be executed first. The complete list of the instructions is provided in Table 5. All instructions are synchronized off a high to low transition of $\overline{CE}$. Inputs will be accepted on the rising edge of SCK starting with the most significant bit. $\overline{CE}$ must be driven low before an instruction is entered and must be driven high after the last bit of the instruction has been shifted in (except for Read, Read ID, Read Status Register, Read Electronic Signature instructions). Any low to high transition on $\overline{CE}$, before receiving the last bit of an instruction bus cycle, will terminate the instruction in progress and return the device to the standby mode.

Instruction commands (Op Code), addresses, and data are all input from the most significant bit (MSB) first.

Table 5: DEVICE OPERATION INSTRUCTIONS

Operation	Max. Freq	Bus Cycle [1~3]													
		1		2		3		4		5		6		N	
		S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}	S_{IN}	S_{OUT}
Read	33 MHz	03H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	X	D_{OUT0}	X	D_{OUT1}	X	cont.
Fast Read	50MHz	0BH	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	X	X	X	D_{OUT0}	X	cont.
Fast Read Dual Output[12,13]		3BH		A_{23}-A_{16}		A_{15}-A_8		A_7-A_0		X		$D_{OUT0\sim1}$		cont.	
Sector Erase[4] (4K Byte)		20H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	-	-	-	-	-	-
Block Erase[4,] (64K Byte)		D8H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	-	-	-	-	-	-
Chip Erase		60H / C7H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Page Program (**PP**)		02H	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	D_{IN0}	Hi-Z	D_{IN1}	Hi-Z	Up to 256 bytes	Hi-Z
Auto Address Increment word programming[5] (AAI)		ADH	Hi-Z	A_{23}-A_{16}	Hi-Z	A_{15}-A_8	Hi-Z	A_7-A_0	Hi-Z	D_{IN0}	Hi-Z	D_{IN1}	Hi-Z	-	-
Read Status Register (**RDSR**) [6]		05H	Hi-Z	X	D_{OUT}	-	-	-	-	-	-	-	-	-	-
Enable Write Status Register (**EWSR**) [7]		50H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Write Status Register (**WRSR**) [7]		01H	Hi-Z	D_{IN}	Hi-Z	-	-	-.	-	-	-	-	-	-	-
Write Enable (**WREN**) [10]		06H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Write Disable (**WRDI**)/ Exit secured OTP mode		04H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Enter secured OTP mode (**ENSO**)	100MHz	B1H	Hi-Z	-	-	-	-	-.	-	-	-	-	-	-	-
Read Electronic Signature (**RES**) [8]		ABH	Hi-Z	X	14H	-	-	-	-	-	-	-	-	-	-
RES in secured OTP mode & not lock down		ABH	Hi-Z	X	34H	-	-	-.	-	-	-	-	-	-	-
RES in secured OTP mode & lock down		ABH	Hi-Z	X	74H	-	-	-.	-	-	-	-	-	-	-
Jedec Read ID (**JEDEC-ID**) [9]		9FH	Hi-Z	X	8CH	X	20H	X	15H	-	-	-	-	-	-
Read ID (**RDID**) [11]		90H	Hi-Z	00H	Hi-Z	00H	Hi-Z	00H	Hi-Z	X	8CH	X	14H	-	-
								01H	Hi-Z	X	14H	X	8CH	-	-
Enable SO to output RY/$\overline{BY}$ Status during AAI (**EBSY**)		70H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-
Disable SO to output RY/$\overline{BY}$ Status during AAI (**DBSY**)		80H	Hi-Z	-	-	-	-	-	-	-	-	-	-	-	-

Note:

1. Operation: S_{IN} = Serial In, S_{OUT} = Serial Out, Bus Cycle 1 = Op Code
2. X = Dummy Input Cycles (V_{IL} or V_{IH}); - = Non-Applicable Cycles (Cycles are not necessary); cont. = continuous
3. One bus cycle is eight clock periods.
4. Sector Earse addresses: use A_{MS} -A_{12}, remaining addresses can be V_{IL} or V_{IH}
   Block Earse addresses: use A_{MS} -A_{16}, remaining addresses can be V_{IL} or V_{IH}
5. To continue programming to the next sequential address location, enter the 8-bit command, followed by the data to be programmed.
6. The Read-Status-Register is continuous with ongoing clock cycles until terminated by a low to high transition on $\overline{CE}$.
7. The Enable-Write-Status-Register (EWSR) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the EWSR instruction to make both instructions effective.
8. The Read-Electronic-Signature is continuous with on going clock cycles until terminated by a low to high transition on $\overline{CE}$.
9. The Jedec-Read-ID is output first byte 8CH as manufacture ID; second byte 20H as top memory type; third byte 15H as memory capacity.
10. The Write-Enable (WREN) instruction and the Write-Status-Register (WRSR) instruction must work in conjunction of each other. The WRSR instruction must be executed immediately (very next bus cycle) after the WREN instruction to make both instructions effective. Both EWSR and WREN can enable WRSR, user just need to execute one of it. A successful WRSR can reset WREN.
11. The Manufacture ID and Device ID output will repeat continuously until $\overline{CE}$ terminates the instruction.
12. Dual commands use bidirectional IO pins. D_{OUT} and cont. are serial data out; others are serial data in.
13. Dual output data:
    IO_0 = (D_6, D_4, D_2, D_0), (D_6, D_4, D_2, D_0)
    IO_1 = (D_7, D_5, D_3, D_1), (D_7, D_5, D_3, D_1)
    D_{OUT0} D_{OUT1}

Read (33MHz)

The Read instruction supports up to 33 MHz, it outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on $\overline{CE}$. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 16Mbit density, once the data from address location 1FFFFFH had been read, the next output will be from address location 00000H.

The Read instruction is initiated by executing an 8-bit command, 03H, followed by address bits [A_{23} -A_0]. $\overline{CE}$ must remain active low for the duration of the Read cycle. See Figure 2 for the Read sequence.

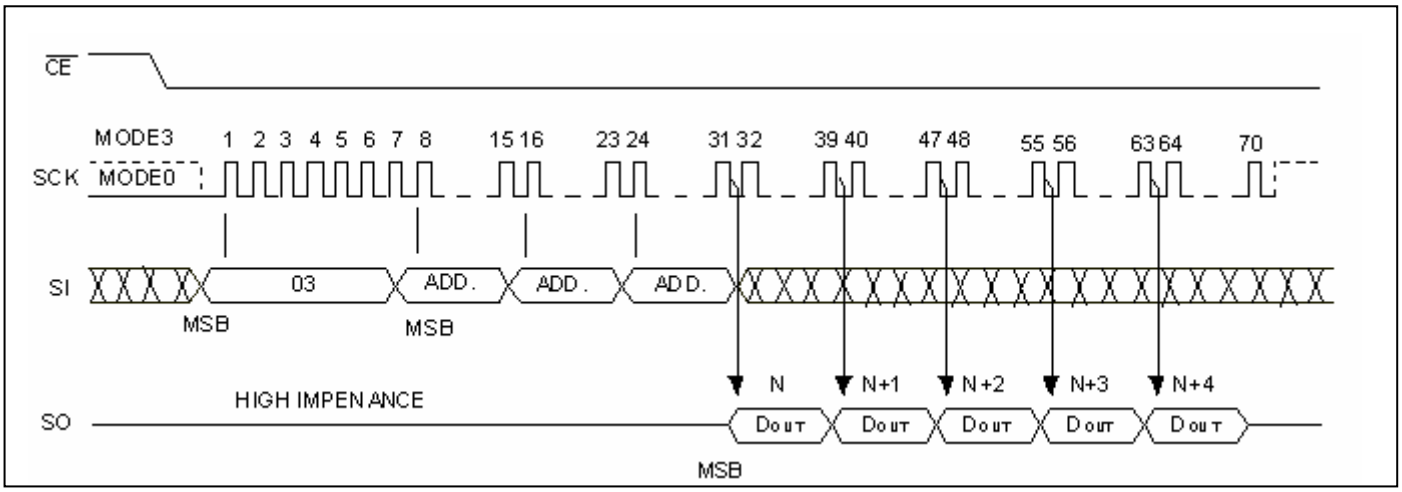


Figure 2: READ SEQUENCE

Fast Read (50 MHz; 100 MHz)

The Fast Read instruction supporting up to 100 MHz is initiated by executing an 8-bit command, 0BH, followed by address bits [A_{23} -A_0] and a dummy byte. $\overline{CE}$ must remain active low for the duration of the Fast Read cycle. See Figure 3 for the Fast Read sequence.

Following a dummy byte (8 clocks input dummy cycle), the Fast Read instruction outputs the data starting from the specified address location. The data output stream is continuous through all addresses until terminated by a low to high transition on $\overline{CE}$. The internal address pointer will automatically increment until the highest memory address is reached. Once the highest memory address is reached, the address pointer will automatically increment to the beginning (wrap-around) of the address space, i.e. for 16Mbit density, once the data from address location 1FFFFFH has been read, the next output will be from address location 000000H.

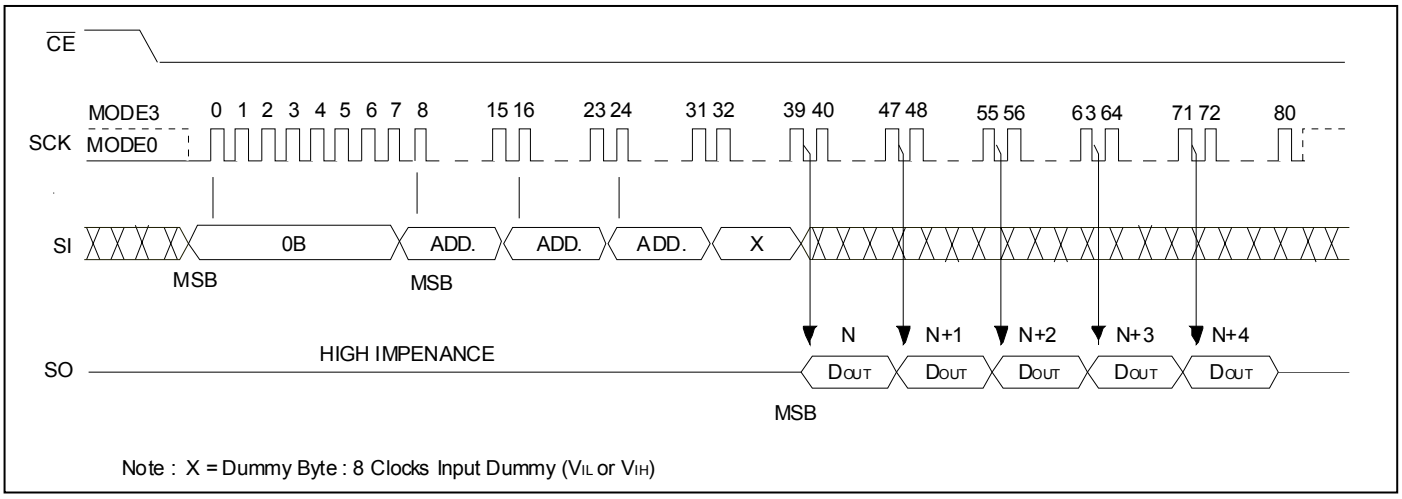


Figure 3: FAST READ SEQUENCE

Fast Read Dual Output (50 MHz; 100 MHz)

The Fast Read Dual Output (3BH) instruction is similar to the standard Fast Read (0BH) instruction except the data is output on SI and SO pins. This allows data to be transferred from the device at twice the rate of standard SPI devices. This instruction is for quickly downloading code from Flash to RAM upon power-up or for applications that cache code- segments to RSM for execution.

The Fast Read Dual Output instruction is initiated by executing an 8-bit command, 3BH, followed by address bits [A_{23} -A_0] and a dummy byte. $\overline{CE}$ must remain active low for the duration of the Fast Read Dual Output cycle. See Figure 4 for the Fast Read Dual Output sequence.

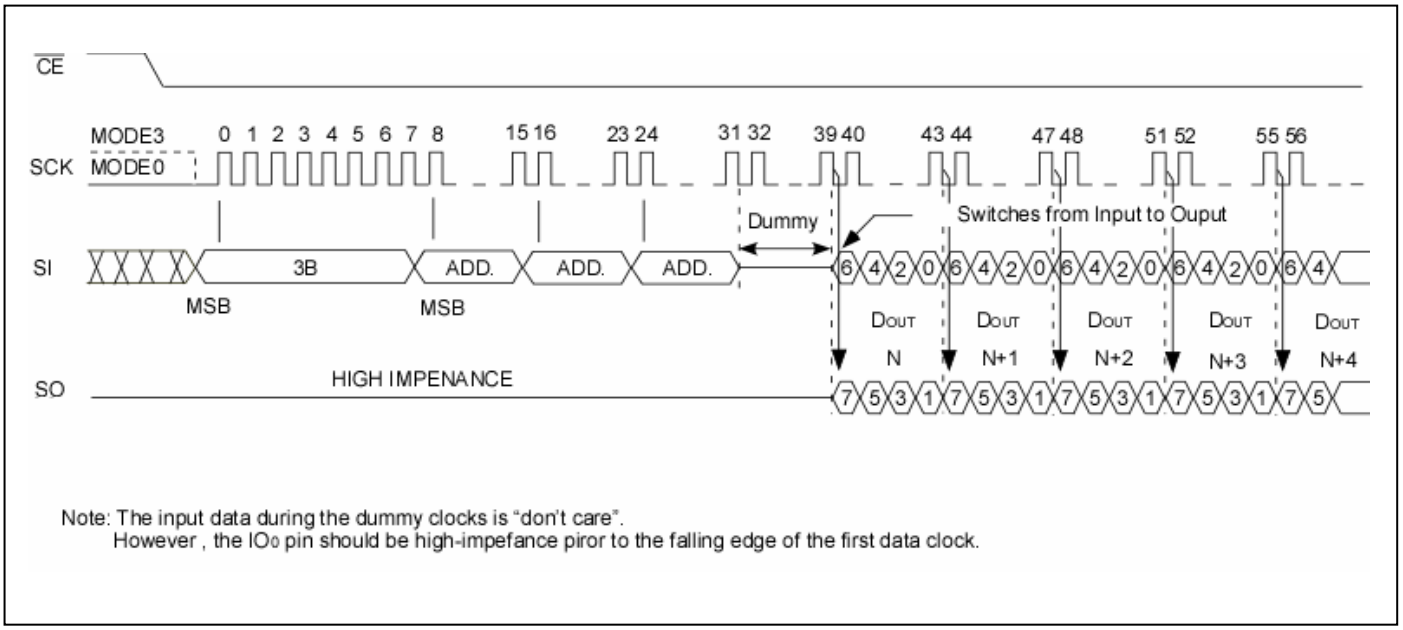


Figure 4: Fast Read Dual Output Sequence

Page Program (PP)

The Page Program instruction allows many bytes to be programmed in the memory. The bytes must be in the erased state (FFH) when initiating a Program operation. A Page Program instruction applied to a protected memory area will be ignored.

Prior to any Write operation, the Write Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the Page Program instruction. The Page Program instruction is initiated by executing an 8-bit command, 02H, followed by address bits [A_{23}-A_0]. Following the address, at least one byte Data is input (the maximum of input data can be up to 256 bytes). If the 8 least significant address bits [A_7-A_0] are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits [A_7-A_0] are all zero).

If more than 256 bytes Data are sent to the device, previously latched data are discarded and the last 256 bytes Data are guaranteed to be programmed correctly within the same page. If less than 256 bytes Data are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page.

$\overline{CE}$ must be driven high before the instruction is executed. The user may poll the BUSY bit in the software status register or wait T_{PP} for the completion of the internal self-timed Page Program operation. While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. It is recommended to wait for a duration of T_{BP1} before reading the status register to check the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished, the Write-Enable-Latch (WEL) bit in the Status Register is cleared to 0. See Figure 5 for the Page Program sequence.

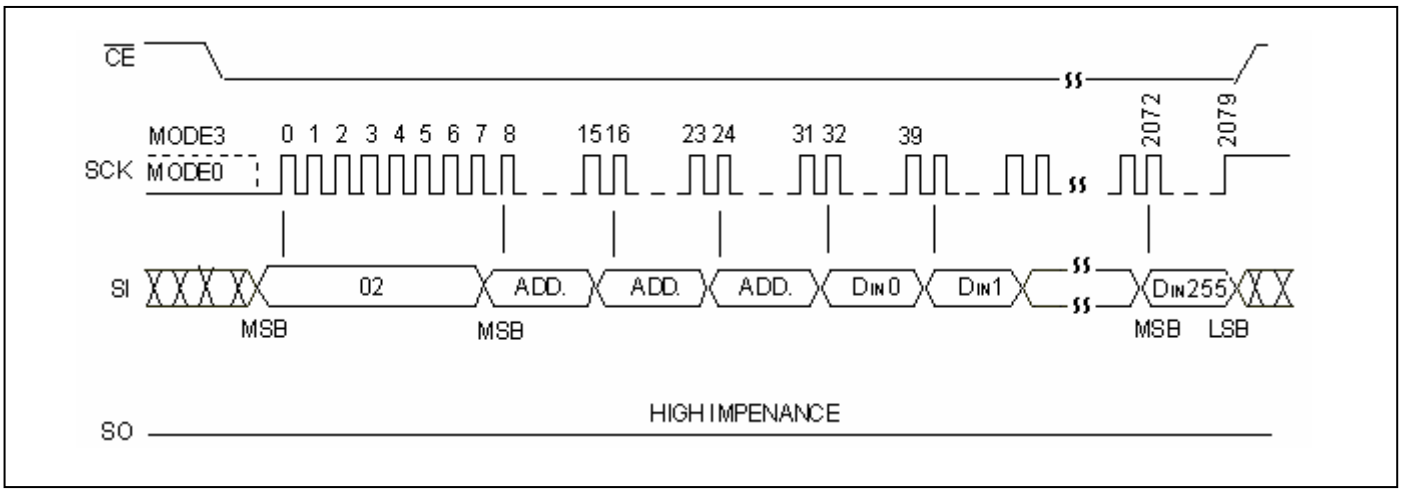


Figure 5: PAGE PROGRAM SEQUENCE

Auto Address Increment (AAI) WORD Program

The AAI program instruction allows multiple bytes of data to be programmed without re-issuing the next sequential address location. This feature decreases total programming time when the multiple bytes or entire memory array is to be programmed. An AAI program instruction pointing to a protected memory area will be ignored. The selected address range must be in the erased state (FFH) when initiating an AAI program instruction. While within AAI WORD programming sequence, the only valid instructions are AAI WORD program operation, RDSR, WRDI. Users have three options to determine the completion of each AAI WORD program cycle: hardware detection by reading the SO; software detection by polling the BUSY in the software status register or wait T_{BP}. Refer to End of Write Detection section for details.

Prior to any write operation, the Write Enable (WREN) instruction must be executed. The AAI WORD program instruction is initiated by executing an 8-bit command, ADH, followed by address bits [A_{23} -A_0]. Following the addresses, two bytes of data is input sequentially. The data is input sequentially from MSB (bit 7) to LSB (bit 0). The first byte of data (D0) will be programmed into the initial address [A_{23} -A_1] with A_0 =0; the second byte of data (D1) will be programmed into the initial address [A_{23} -A_1] with A_0 =1. $\overline{CE}$ must be driven high before the AAI WORD program instruction is executed. The user must check the busy status before entering the next valid command. Once the device indicates it is no longer busy, data for next two sequential addresses may be programmed and so on. When the last desired byte had been entered, check the busy status using the hardware method or the RDSR instruction and execute the WRDI instruction, to terminate AAI. User must check busy status after WRDI to determine if the device is ready for any command. Please refer to Figure 8 and Figure 9.

There is no wrap mode during AAI programming; once the highest unprotected memory address is reached, the device will exit AAI operation and reset the Write-Enable-Latch bit (WEL = 0) and the AAI bit (AAI=0).

End of Write Detection

There are three methods to determine completion of a program cycle during AAI WORD programming: hardware detection by reading the SO, software detection by polling the BUSY bit in the Software Status Register or wait T_{BP}. The Hardware End of Write Detection method is described in the section below.

Hardware End of Write Detection

The Hardware End of Write Detection method eliminates the overhead of polling the BUSY bit in the Software Status Register during an AAI Word program operation. The 8-bit command, 70H, configures the SO pin to indicate Flash busy status during AAI WORD programming (refer to Figure 6). The 8-bit command, 70H, must be executed prior to executing an AAI WORD program instruction. Once an internal programming operation begins, asserting $\overline{CE}$ will immediately drive the status of the internal flash status on the SO pin. A “0”
Indicates the device is busy; a “1” Indicates the device is ready for the next instruction. De-asserting $\overline{CE}$ will return the SO pin to tri-state. The 8-bit command, 80H, disables the SO pin to output busy status during AAI WORD program operation and return SO pin to output Software Status Register data during AAI WORD programming (refer to Figure 7).

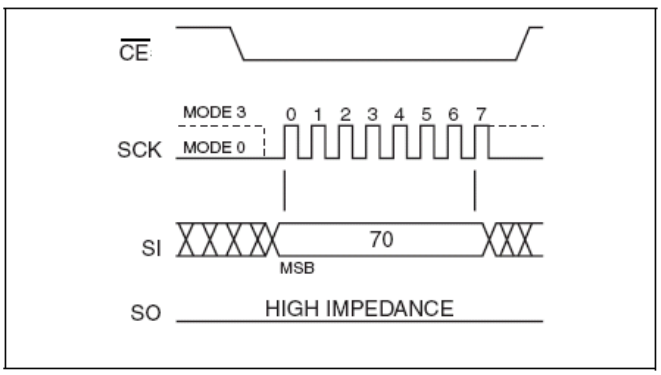


Figure 6: ENABLE SO AS HARDWARE RY / $\overline{BY}$ DURING AAI PROGRAMMING

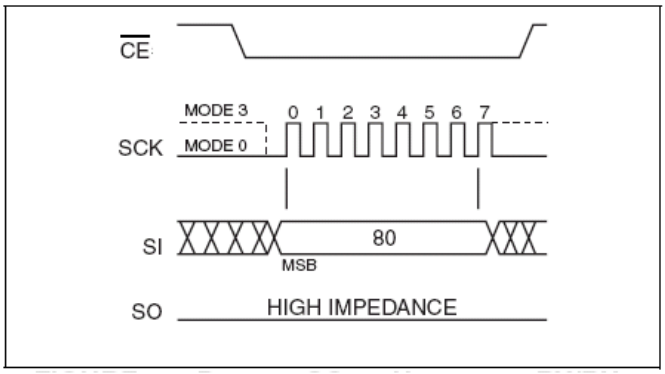


Figure 7: DISABLE SO AS HARDWARE RY / $\overline{BY}$ DURING AAI PROGRAMMING

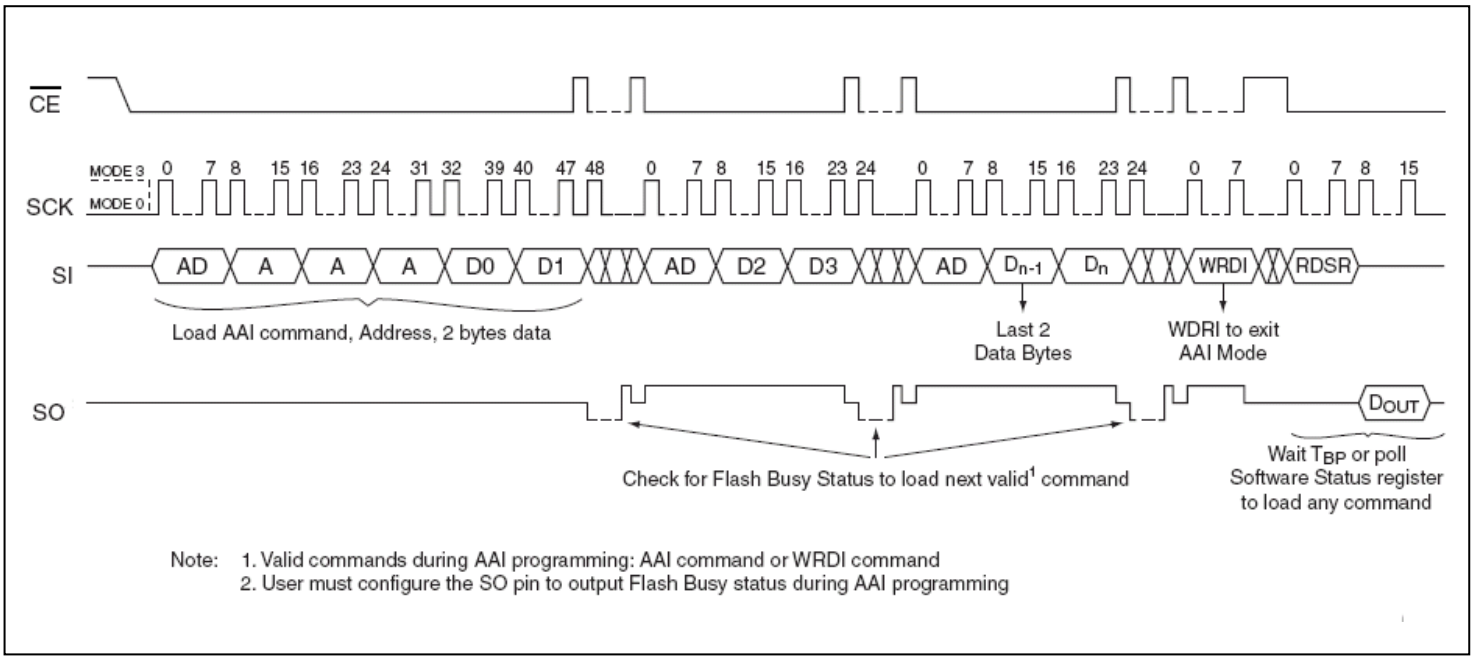


Figure 8: AAI WORD PROGRAM SEQUENCE WITH HARDWARE END OF WRITE DETECTION

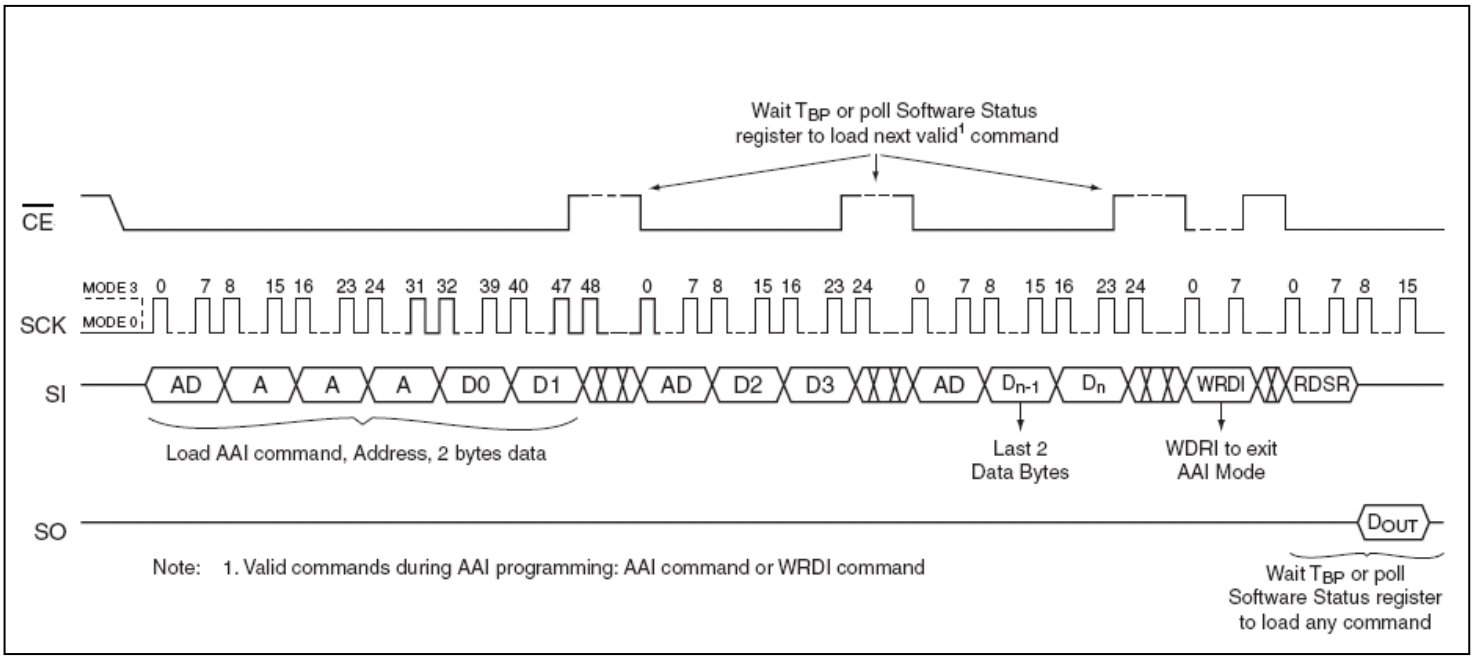


Figure 9: AAI WORD PROGRAM SEQUENCE WITH SOFTWARE END OF WRITE DETECTION

64K Byte Block Erase

The 64K-byte Block Erase instruction clears all bits in the selected block to FFH. A Block Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the any command sequence. The Block Erase instruction is initiated by executing an 8-bit command, D8H, followed by address bits [A_{23} -A_0]. Address bits [A_{MS} -A_{16}] (A_{MS} = Most Significant address) are used to determine the block address (BA_X), remaining address bits can be V_{IL} or V_{IH}. $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the BUSY bit in the Software Status Register or wait T_{BE} for the completion of the internal self-timed Block Erase cycle. See Figure 10 for the Block Erase sequence.

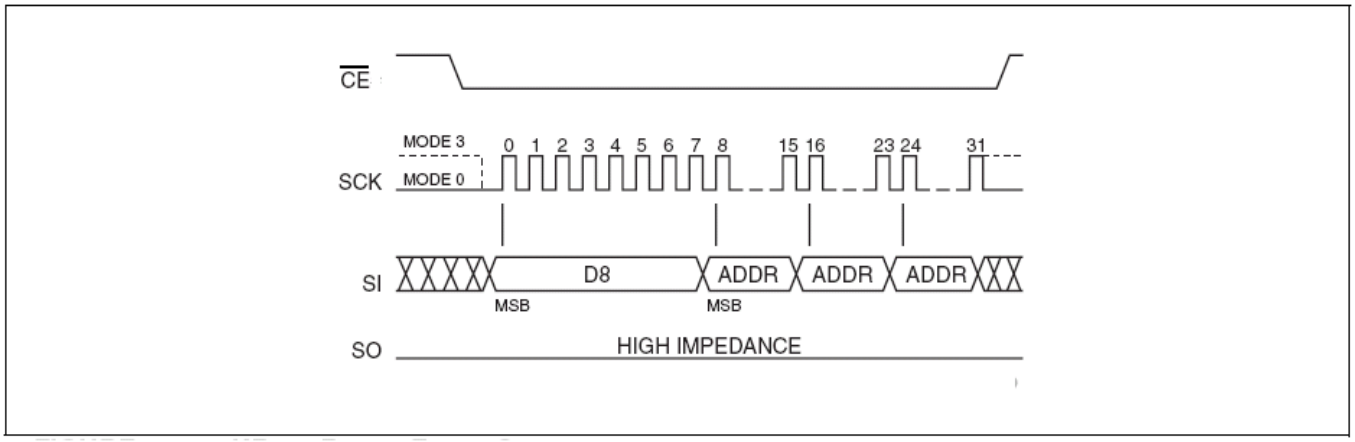


Figure 10: 64K-byte BLOCK ERASE SEQUENCE

4K Byte Sector Erase

The Sector Erase instruction clears all bits in the selected sector to FFH. A Sector Erase instruction applied to a protected memory area will be ignored. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the any command sequence. The Sector Erase instruction is initiated by executing an 8-bit command, 20H, followed by address bits [A_{23} -A_0]. Address bits [A_{MS} -A_{12}] (A_{MS} = Most Significant address) are used to determine the sector address (SA_X), remaining address bits can be V_{IL} or V_{IH}. $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the BUSY bit in the Software Status Register or wait T_{SE} for the completion of the internal self-timed Sector Erase cycle. See Figure 11 for the Sector Erase sequence.

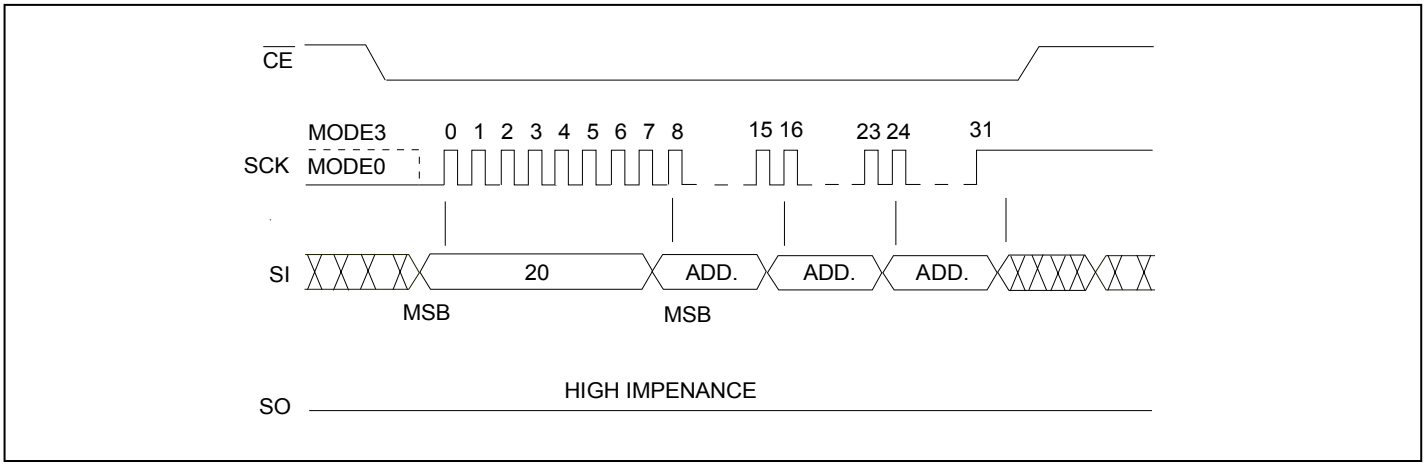


Figure 11: SECTOR ERASE SEQUENCE

Chip Erase

The Chip Erase instruction clears all bits in the device to FFH. A Chip Erase instruction will be ignored if any of the memory area is protected. Prior to any Write operation, the Write Enable (WREN) instruction must be executed. $\overline{CE}$ must remain active low for the duration of the Chip-Erase instruction sequence. The Chip Erase instruction is initiated by executing an 8-bit command, 60H or C7H. $\overline{CE}$ must be driven high before the instruction is executed. The user may poll the BUSY bit in the Software Status Register or wait T_{CE} for the completion of the internal self-timed Chip Erase cycle. See Figure 12 for the Chip Erase sequence.

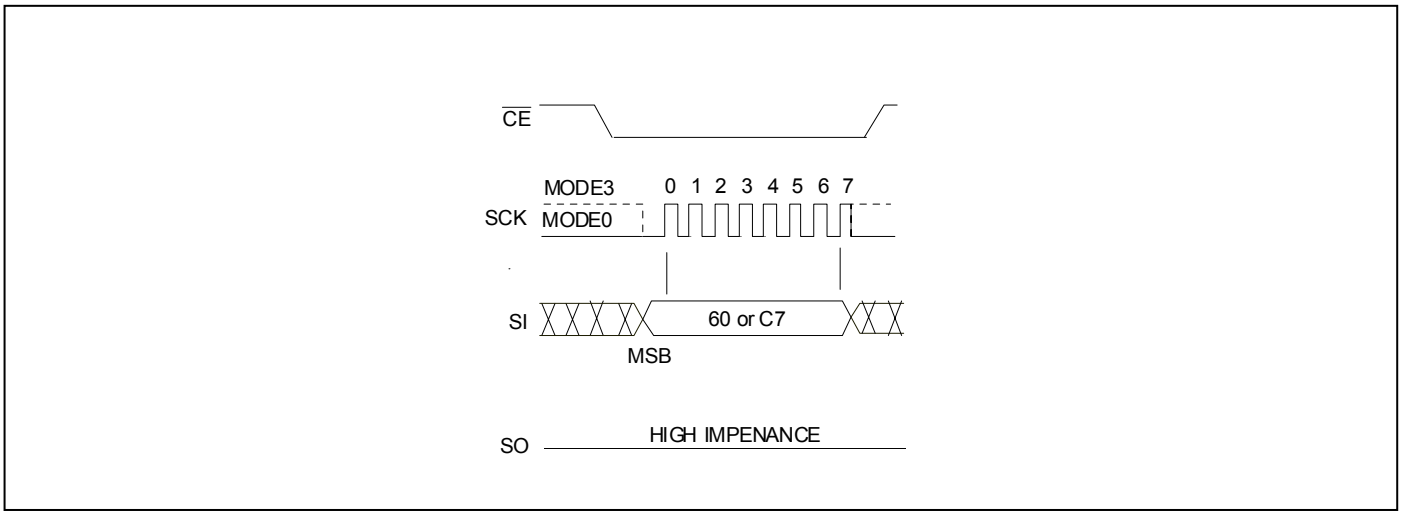


Figure 12: CHIP ERASE SEQUENCE

Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows reading of the status register. The status register may be read at any time even during a Write (Program/Erase) operation.
When a Write operation is in progress, the BUSY bit may be checked before sending any new commands to assure that the new commands are properly received by the device.

$\overline{CE}$ must be driven low before the RDSR instruction is entered and remain low until the status data is read. Read Status Register is continuous with ongoing clock cycles until it is terminated by a low to high transition of the $\overline{CE}$. See Figure 13 for the RDSR instruction sequence.

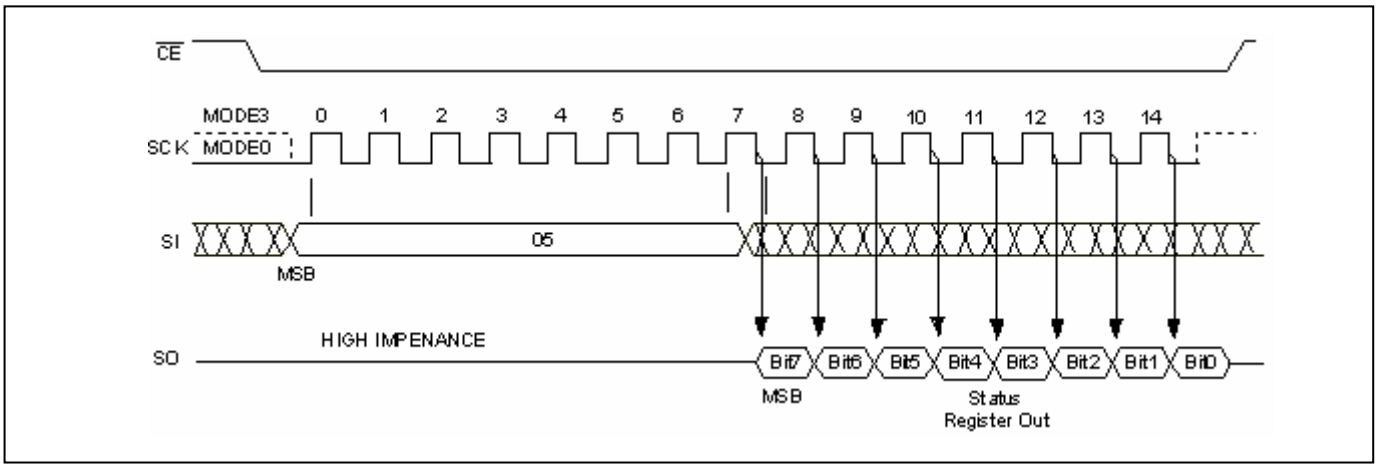


Figure 13: READ-STATUS-REGISTER (RDSR) SEQUENCE

Write Enable (WREN)

The Write Enable (WREN) instruction sets the Write-Enable-Latch bit in the Software Status Register to 1 allowing Write operations to occur.
The WREN instruction must be executed prior to any Write (Program/Erase) operation. $\overline{CE}$ must be driven high before the WREN instruction is executed.

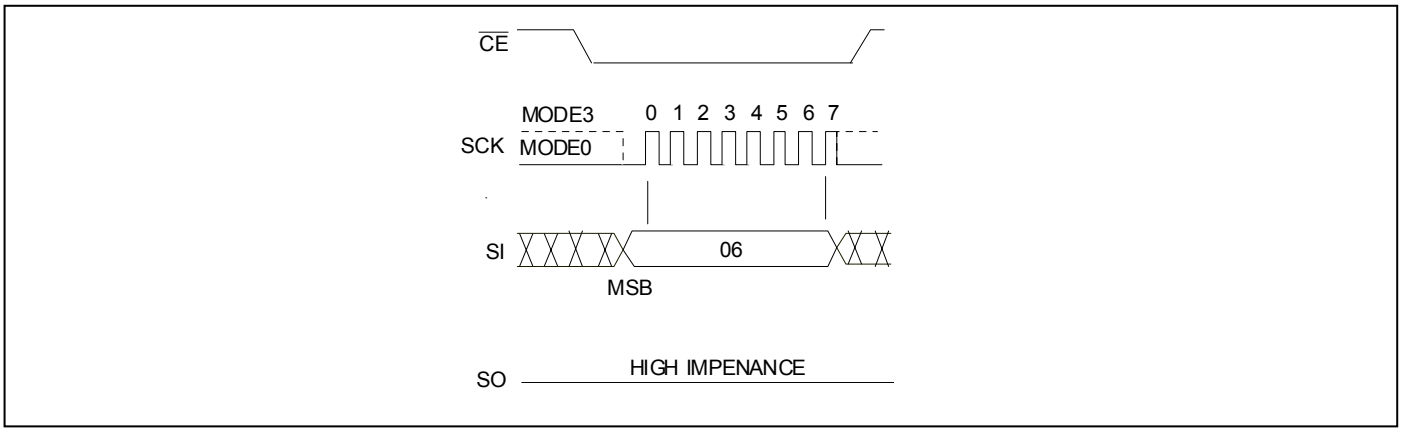


Figure 14: WRITE ENABLE (WREN) SEQUENCE

Write Disable (WRDI)

The Write Disable (WRDI) instruction resets the Write-Enable-Latch bit to 0 disabling any new Write operations from occurring. $\overline{CE}$ must be driven high before the WRDI instruction is executed.

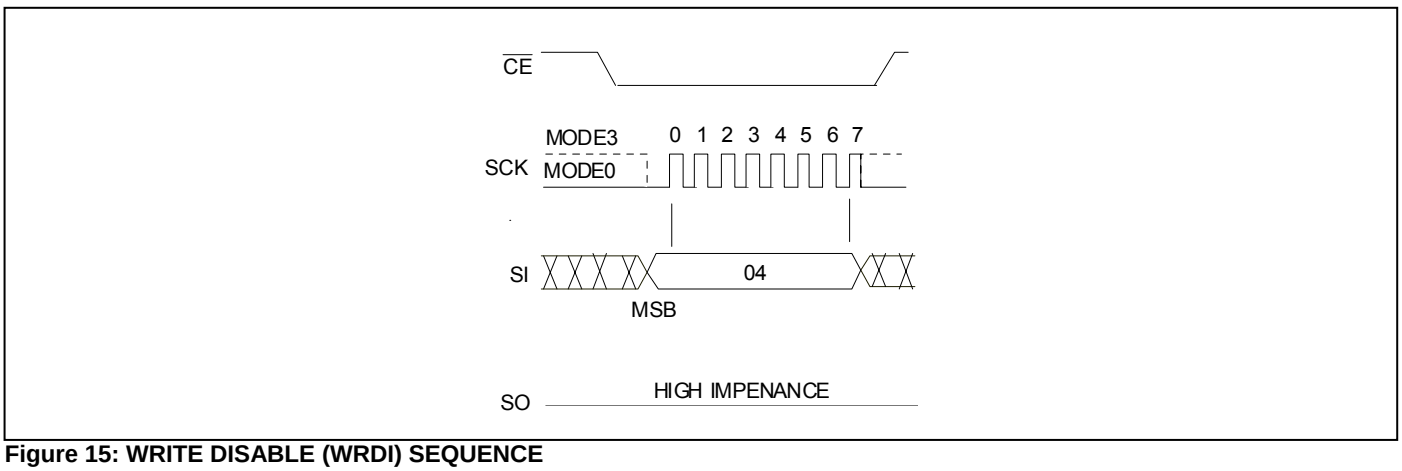


Figure 15: WRITE DISABLE (WRDI) SEQUENCE

Enable Write Status Register (EWSR)

The Enable Write Status Register (EWSR) instruction arms the Write Status Register (WRSR) instruction and opens the status register for alteration. The Enable Write Status Register instruction does not have any effect and will be wasted, if it is not followed immediately by the Write Status Register (WRSR) instruction. $\overline{CE}$ must be driven low before the EWSR instruction is entered and must be driven high before the EWSR instruction is executed.

Write-Status-Register (WRSR)

The Write Status Register instruction writes new values to the BP2, BP1, BP0, and BPL bits of the status register. $\overline{CE}$ must be driven low before the command sequence of the WRSR instruction is entered and driven high before the WRSR instruction is executed. See Figure 16 for EWSR or WREN and WRSR instruction sequences.

Executing the Write Status Register instruction will be ignored when $\overline{WP}$ is low and BPL bit is set to "1". When the $\overline{WP}$ is low, the BPL bit can only be set from "0" to "1" to lock down the status register, but cannot be reset from "1" to "0".

When $\overline{WP}$ is high, the lock-down function of the BPL bit is disabled and the BPL, BP0, BP1,and BP2 bits in the status register can all be changed. As long as BPL bit is set to 0 or $\overline{WP}$ pin is driven high (V_{IH}) prior to the low-to-high transition of the $\overline{CE}$ pin at the end of the WRSR instruction, the bits in the status register can all be altered by the WRSR instruction. In this case, a single WRSR instruction can set the BPL bit to "1" to lock down the status register as well as altering the BP0; BP1 and BP2 bits at the same time. See Table 4 for a summary description of $\overline{WP}$ and BPL functions.

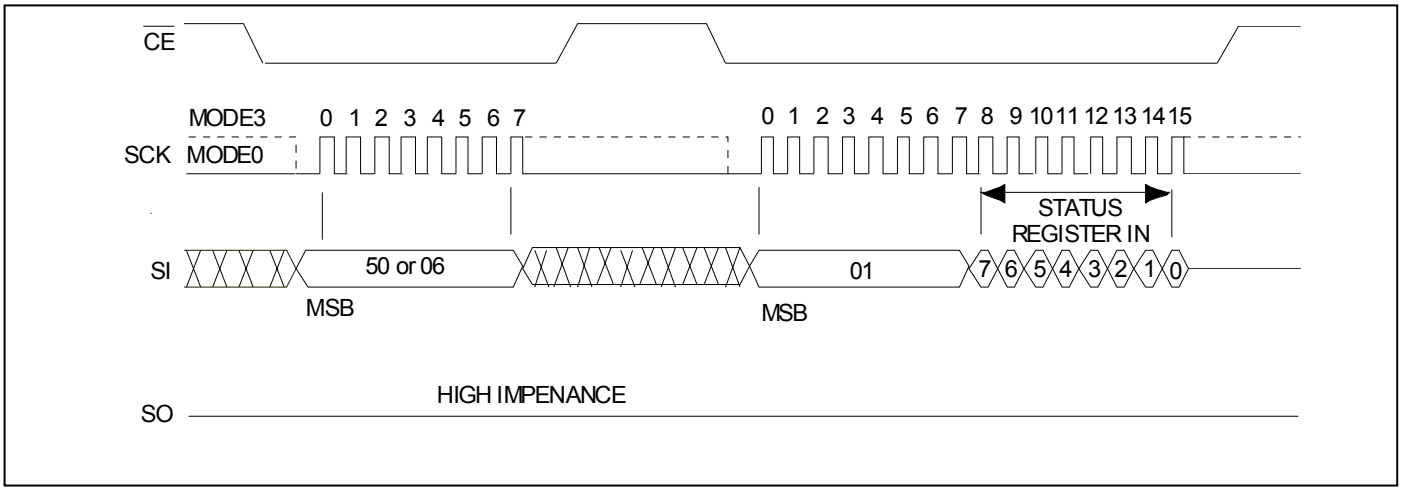
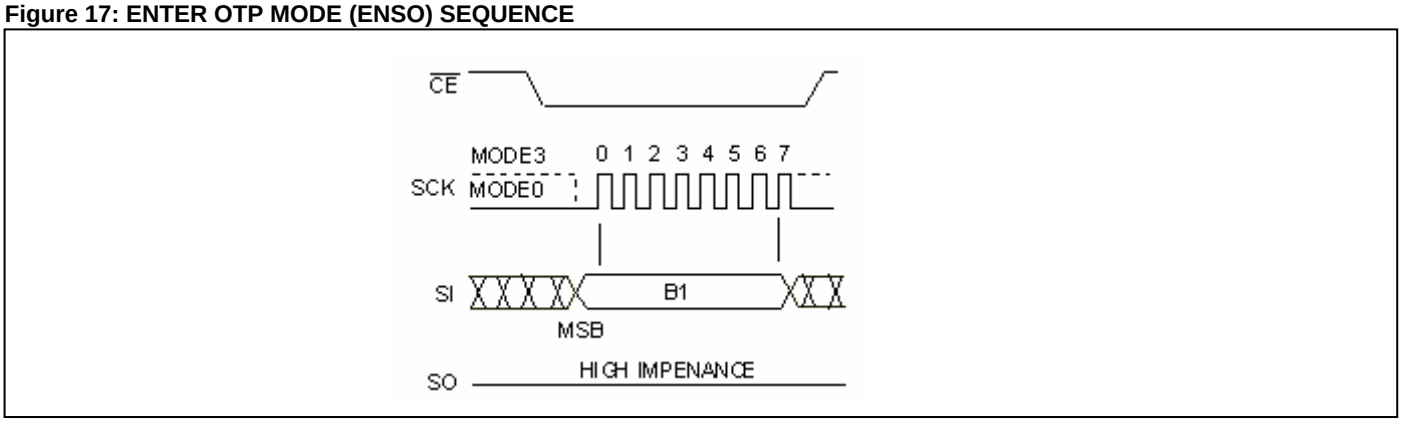


Figure 16: ENABLE-WRITE-STATUS-REGISTER (EWSR) or WRITE-ENABLE(WREN) and WRITE-STATUS-REGISTER (WRSR)

Enter OTP Mode (ENSO)

The ENSO (B1H) instruction is for entering the additional 4K bytes secured OTP mode. The additional 4K bytes secured OTP sector is independent from main array, which may use to store unique serial number for system identifier. User must unprotect whole array (BP0=BP1=BP2=0), prior to any Write (Program/ Erase) operation in OTP sector. After entering the secured OTP mode, only the secured OTP sector can be accessed and user can follow the standard Read or Write procedure except for Block Erase and Chip Erase. The secured OTP data cannot be updated again once it is lock down. In secured OTP mode, WRSR command will ignore the input data and lock down the secured OTP sector (OTP_lock bit =1). To exit secured OTP mode, user must execute WRDI command. RES can be used to verify the secured OTP status as shown in Table 6.

Figure 17: ENTER OTP MODE (ENSO) SEQUENCE



Read-Electronic-Signature (RES)

The RES instruction can be used to read the 8-bit Electronic Signature of the device on the SO pin. The RES instruction can provide access to the Electronic Signature of the device (except while an Erase, Program or WRSR cycle is in progress), Any RES instruction executed while an Erase, Program or WRSR cycle is in progress is no decoded, and has no effect on the cycle in progress. In OTP mode, user also can execute RES to confirm the status.

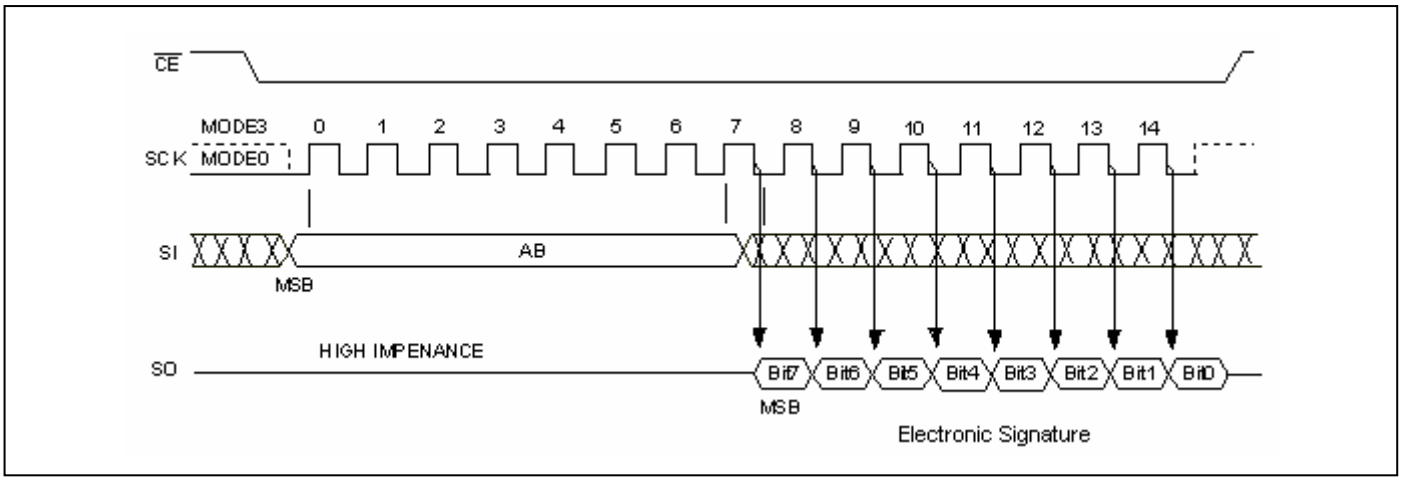


Figure 18: Read-Electronic-Signature (RES)

Table 6: Electronic Signature DATA

Command	Mode	Electronic Signature Data
RES	Normal	14H
	In secured OTP mode & non lock down (OTP_lock =0)	34H
	In secured OTP mode & lock down (OTP_lock =1)	74H

JEDEC Read-ID

The JEDEC Read-ID instruction identifies the device as F25L16PA and the manufacturer as ESMT. The device information can be read from executing the 8-bit command, 9FH. Following the JEDEC Read-ID instruction, the 8-bit manufacturer's ID, 8CH, is output from the device. After that, a 16-bit device ID is shifted out on the SO pin. Byte1, 8CH, identifies the manufacturer as ESMT. Byte2, 20H, identifies the memory type as SPI Flash. Byte3, 15H, identifies the device as F25L16PA. The instruction sequence is shown in Figure 19. The JEDEC Read ID instruction is terminated by a low to high transition on $\overline{CE}$ at any time during data output. If no other command is issued after executing the JEDEC Read-ID instruction, issue a 00H (NOP) command before going into Standby Mode ($\overline{CE}$ =V_{IH}).

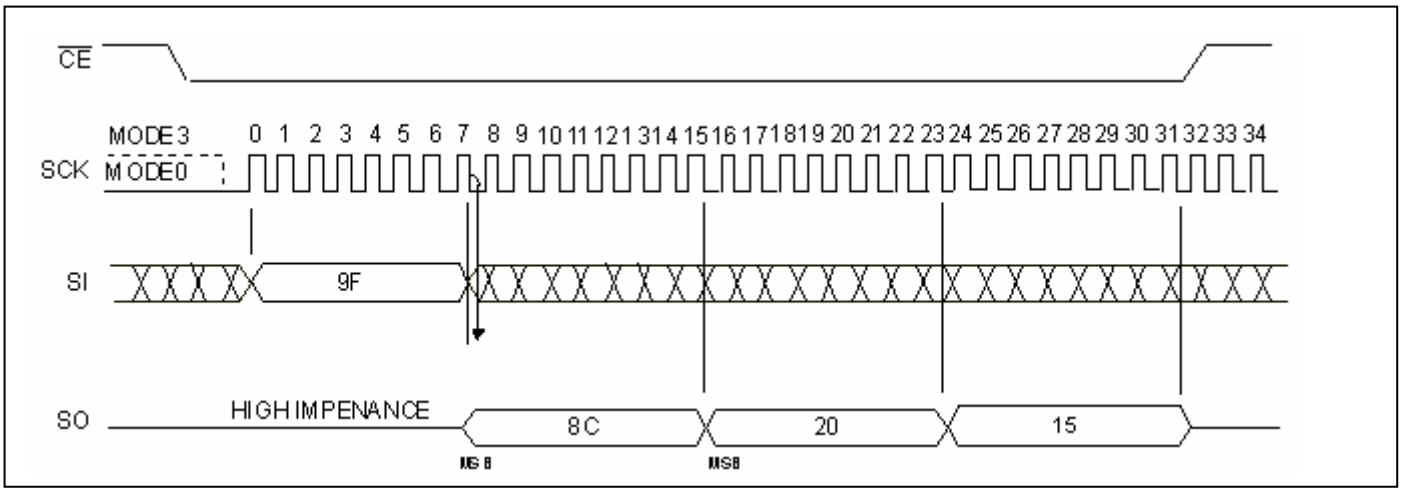


Figure 19: Jedec Read ID Sequence

Table 7: JEDEC READ-ID DATA

Manufacturer's ID (Byte 1)	Device ID	
	Memory Type (Byte 2)	Memory Capacity (Byte 3)
8CH	20H	15

Read-ID (RDID)

The Read-ID instruction (RDID) identifies the devices as F25L16PA and manufacturer as ESMT. This command is backward compatible to all ESMT SPI devices and should be used as default device identification when multiple versions of ESMT SPI devices are used in one design. The device information can be read from executing an 8-bit command, 90H, followed by address bits [A_{23} -A_0]. Following the Read-ID instruction, the manufacturer's ID is located in address 00000H and the device ID is located in address 00001H.

Once the device is in Read-ID mode, the manufacturer's and device ID output data toggles between address 00000H and 00001H until terminated by a low to high transition on $\overline{CE}$.

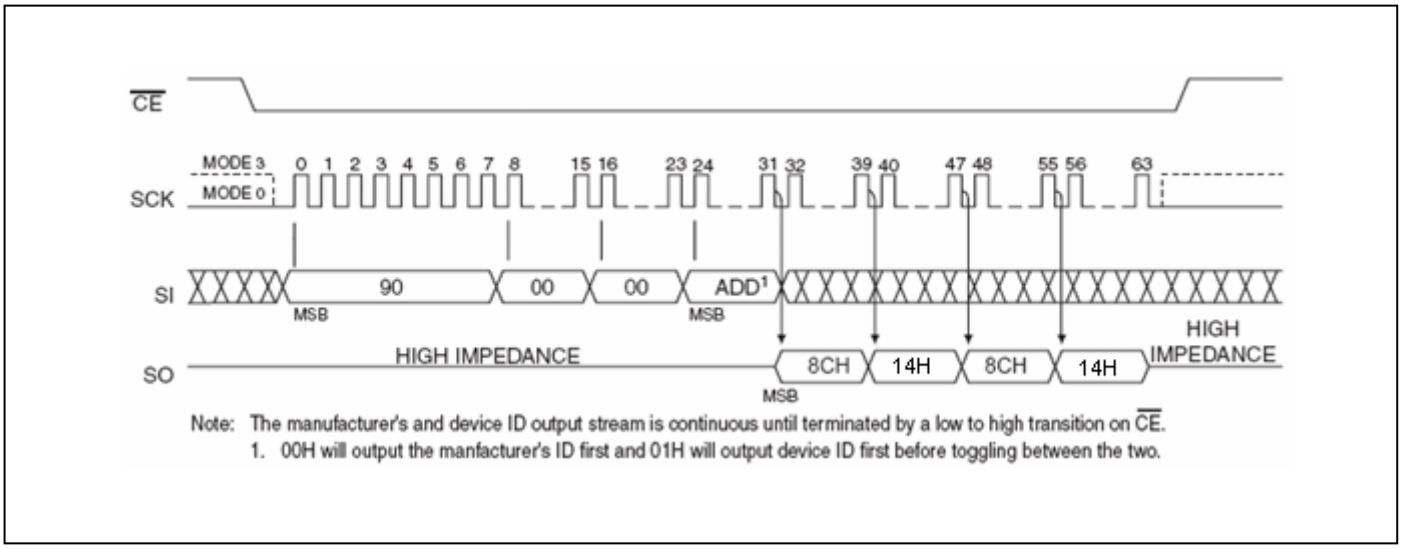


Figure 20: Read ID Sequence

Table 8: PRODUCT ID DATA

Address	Byte1	Byte2
00000H	8CH	14H
	Manufacturer's ID	Device ID ESMT F25L16PA
00001H	14H	8CH
	Device ID ESMT F25L16PA	Manufacturer's ID

■ ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings
(Applied conditions are greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this datasheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to VDD+0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -2.0V to VDD+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.0W
Surface Mount Lead Soldering Temperature (3 Seconds) . . . . . 240°C
Output Short Circuit Current (Note 1). . . . . 50 mA

(Note 1: Output shorted for no more than one second. No more than one output shorted at a time.)

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 5 ns
Output Load . . . . . C_L = 15 pF for ≧75MHz
. . . . . .C_L = 30 pF for ≦50MHz
See Figures 25 and 26

OPERATING RANGE

Parameter	Symbol	Value	Unit
Operating Supply Voltage	V_{DD} (for F_{CLK} ≦ 50MHz)	2.7 ~ 3.6	V
	V_{DD} (for F_{CLK} = 100MHz)	3.0 ~3.6	
Ambient Operating Temperature	T_A	0 ~ 70	℃

Table 9: DC OPERATING CHARACTERISTICS

Symbol	Parameter		Limits			Test Condition
			Min	Max	Unit	
I_{DDR1}	Read Current @33 MHz	Standard		15	mA	$\overline{CE}$ =0.1 V_{DD}/0.9 V_{DD}, SO=open
		Dual		18		
I_{DDR2}	Read Current @ 50MHz	Standard		20	mA	$\overline{CE}$ =0.1 V_{DD}/0.9 V_{DD}, SO=open
		Dual		23		
I_{DDR3}	Read Current @ 100MHz	Standard		25	mA	$\overline{CE}$ =0.1 V_{DD}/0.9 V_{DD}, SO=open
		Dual		28		
I_{DDW}	Program and Erase Current			35	mA	$\overline{CE}$ =V_{DD}
I_{SB}	Standby Current			30	µA	$\overline{CE}$ =V_{DD}, V_{IN} =V_{DD} or V_{SS}
I_{LI}	Input Leakage Current			1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current			1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
V_{IL}	Input Low Voltage			0.8	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage		0.7 x V_{DD}		V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage			0.2	V	I_{OL}=100 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage		V_{DD}-0.2		V	I_{OH}=-100 µA, V_{DD}=V_{DD} Min

Table 10: LATCH UP CHARACTERISTIC

Symbol	Parameter	Minimum	Unit	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 11: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Unit
$T_{PU-READ}$[1]	V_{DD} Min to Read Operation	10	µs
$T_{PU-WRITE}$[1]	V_{DD} Min to Write Operation	10	µs

Table 12: CAPACITANCE (T_A = 25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
C_{OUT}[1]	Output Pin Capacitance	V_{OUT} = 0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	6 pF

Note 1: This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

Table 13: AC OPERATING CHARACTERISTICS

Symbol	Parameter	Normal 33MHz		Fast 50 MHz		Fast 100 MHz		Unit
		Min	Max	Min	Max	Min	Max	
F_{CLK}	Serial Clock Frequency		33		50		100	MHz
T_{SCKH}	Serial Clock High Time	13		9		5		ns
T_{SCKL}	Serial Clock Low Time	13		9		5		ns
T_{CES}[1]	$\overline{CE}$ Active Setup Time	5		5		5		ns
T_{CEH}[1]	$\overline{CE}$ Active Hold Time	5		5		5		ns
T_{CHS}[1]	$\overline{CE}$ Not Active Setup Time	5		5		5		ns
T_{CHH}[1]	$\overline{CE}$ Not Active Hold Time	5		5		5		ns
T_{CPH}	$\overline{CE}$ High Time	100		100		100		ns
T_{CHZ}	$\overline{CE}$ High to High-Z Output		9		9		9	ns
T_{CLZ}	SCK Low to Low-Z Output	0		0		0		ns
T_{DS}	Data In Setup Time	3		3		3		ns
T_{DH}	Data In Hold Time	3		3		3		ns
T_{HLS}	$\overline{HOLD}$ Low Setup Time	5		5		5		ns
T_{HHS}	$\overline{HOLD}$ High Setup Time	5		5		5		ns
T_{HLH}	$\overline{HOLD}$ Low Hold Time	5		5		5		ns
T_{HHH}	$\overline{HOLD}$ High Hold Time	5		5		5		ns
T_{HZ}	$\overline{HOLD}$ Low to High-Z Output		9		9		9	ns
T_{LZ}	$\overline{HOLD}$ High to Low-Z Output		9		9		9	ns
T_{OH}	Output Hold from SCK Change	0		0		0		ns
T_V	Output Valid from SCK		12		8		7	ns

Note 1: Relative to SCK.

■ ERASE AND PROGRAMMING PERFORMANCE

Parameter	Symbol	Limit		Unit
		Typ[2]	Max[3]	
Sector Erase Time	T_{SE}	90	200	ms
Block Erase Time	T_{BE}	1	2	s
Chip Erase Time	T_{CE}	10	30	s
Byte Programming Time (for AAI program)	T_{BP}	7	30	us
Page Programming Time	T_{PP}	1.5	5	ms
Byte Programming Time – 1st byte[4] (for page program)	T_{BP1}	100	150	us
Byte Programming Time – after 1st byte[4] (for page program)	T_{BP2}	6	12	us
Chip Programming Time		50	100	s
Erase/Program Cycles[1]		100,000	-	Cycles
Data Retention		20	-	Years

Notes:

1. Not 100% Tested, Excludes external system level over head.
2. Typical values measured at 25°C, 3V.
3. Maximum values measured at 85°C, 2.7V.
4. For multiple bytes after first byte within a page, $T_{BPN} = T_{BP1} + T_{BP2 *N}$ (typical) and $T_{BPN} = T_{BP1} + T_{BP2 *N}$ (max), where N = number of bytes programmed. T_{BP1} (typical) is also the recommended delay time before reading the status register after issuing a page program instruction.

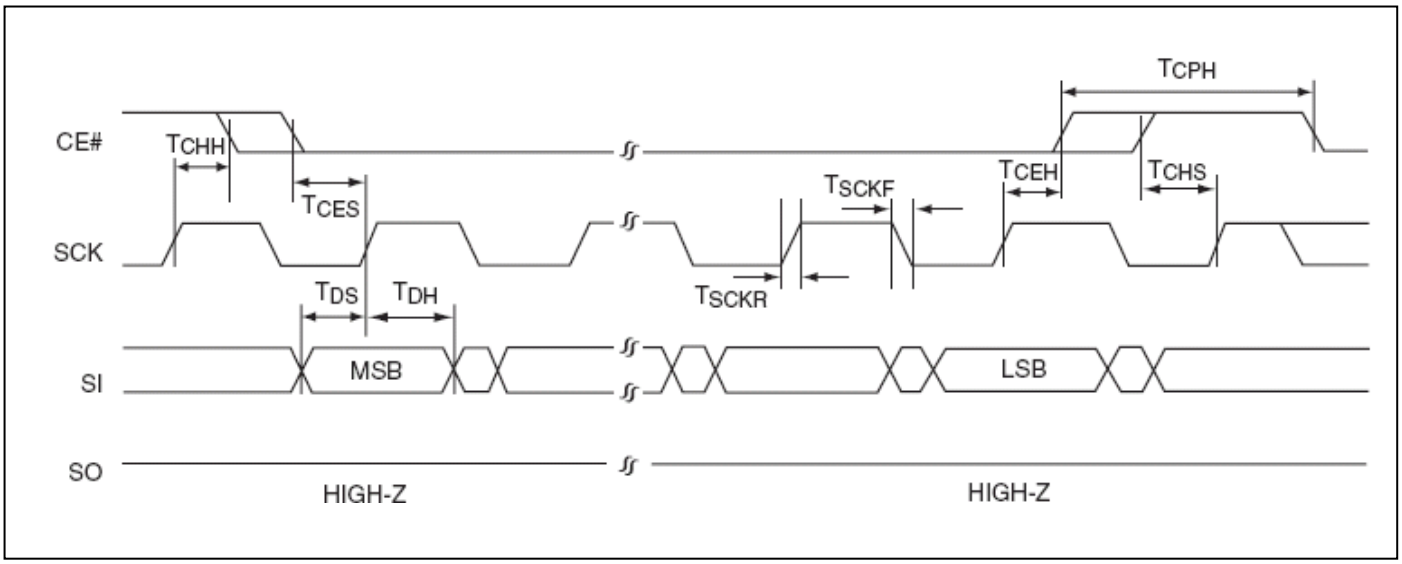


Figure 21: SERIAL INPUT TIMING DIAGRAM

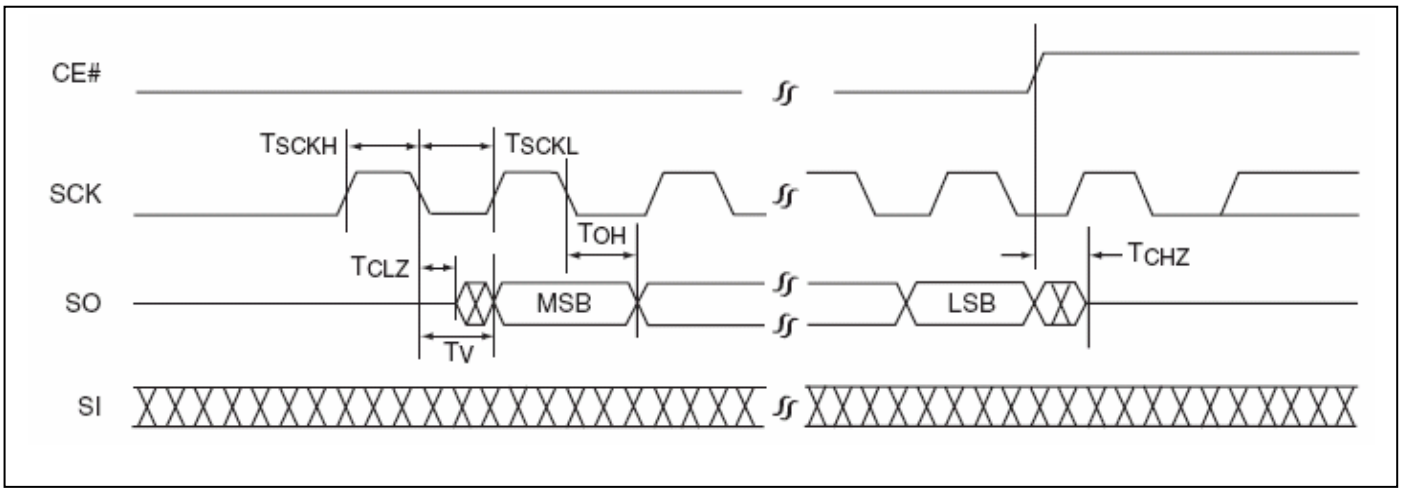


Figure 22: SERIAL OUTPUT TIMING DIAGRAM

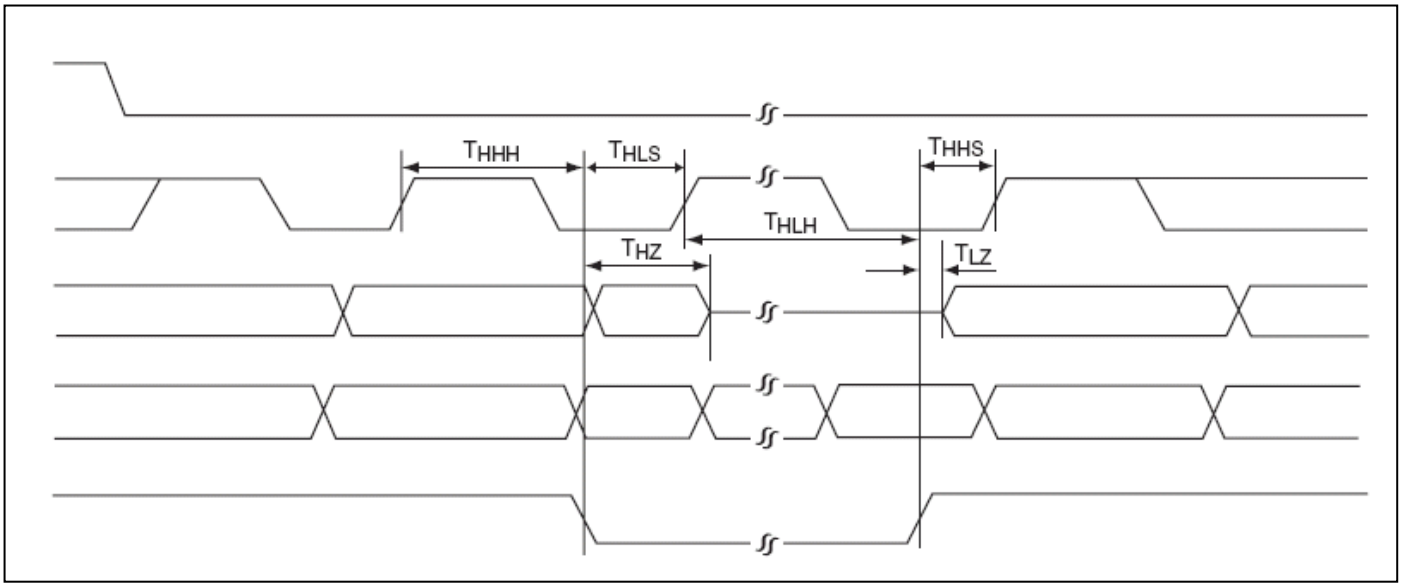


Figure 23: HOLD TIMING DIAGRAM

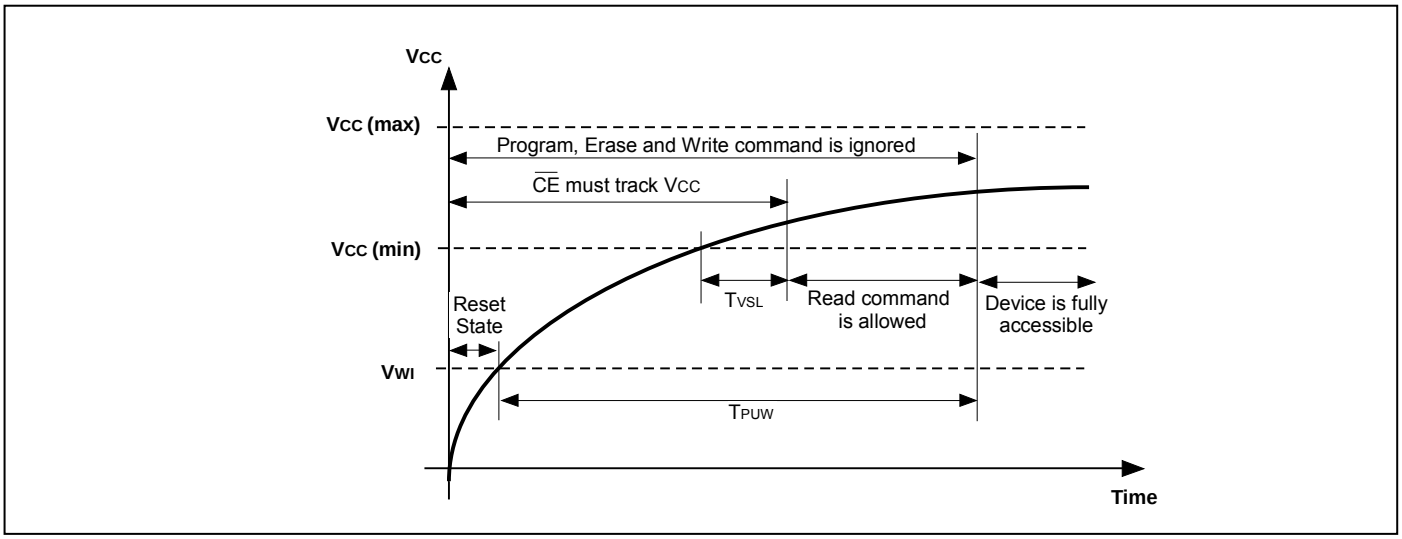


Figure 24: Power-Up Timing Diagram

Table 14: Power-Up Timing and V_{WI} Threshold

Parameter	Symbol	Min.	Max.	Unit
V_{CC}(min) to $\overline{CE}$ low	T_{VSL}	200		us
Time Delay before Write instruction	T_{PUW}		10	ms
Write Inhibit Threshold Voltage	V_{WI}	1	2	V

Note: These parameters are characterized only.

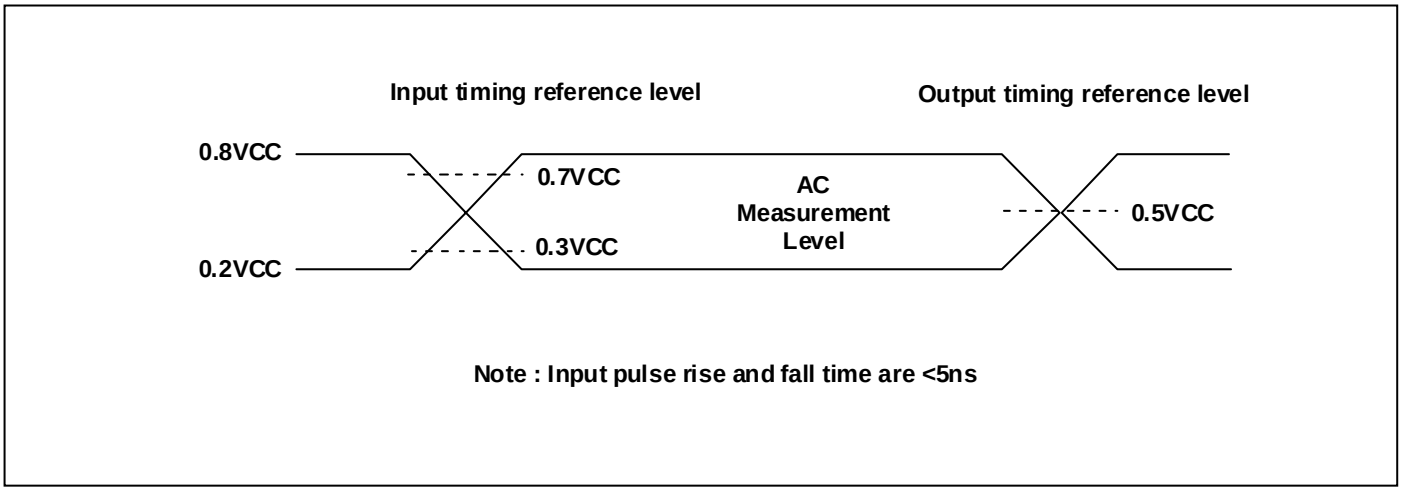


Figure 25: AC INPUT/OUTPUT REFERENCE WAVEFORMS

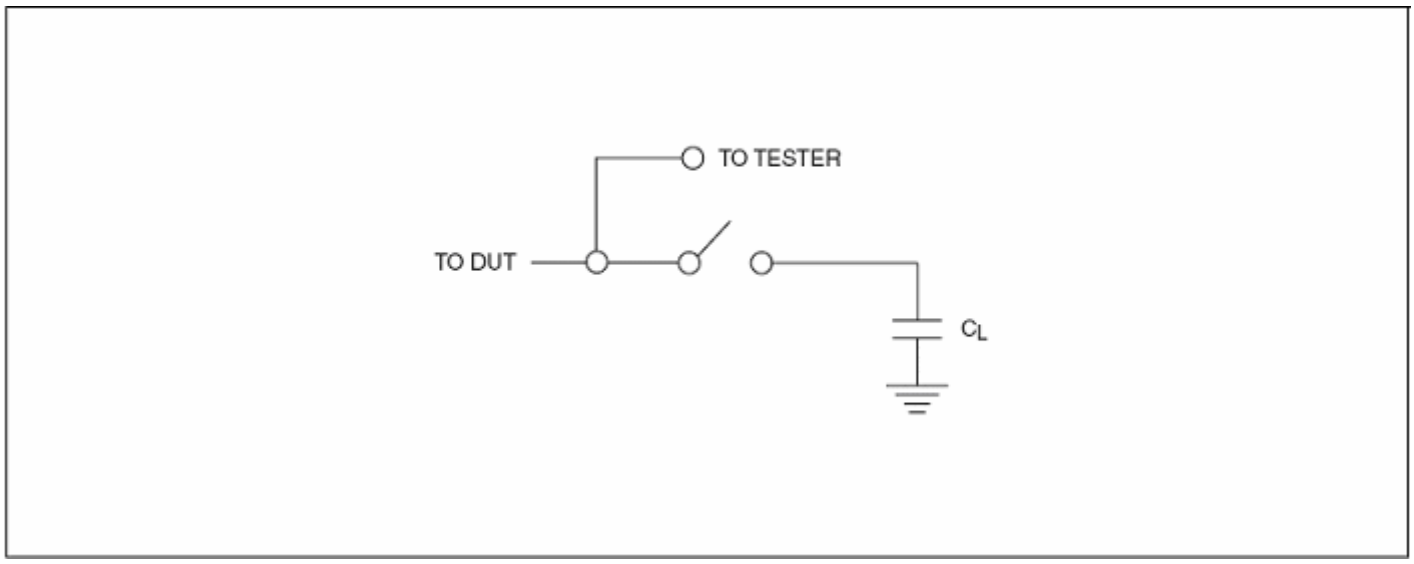
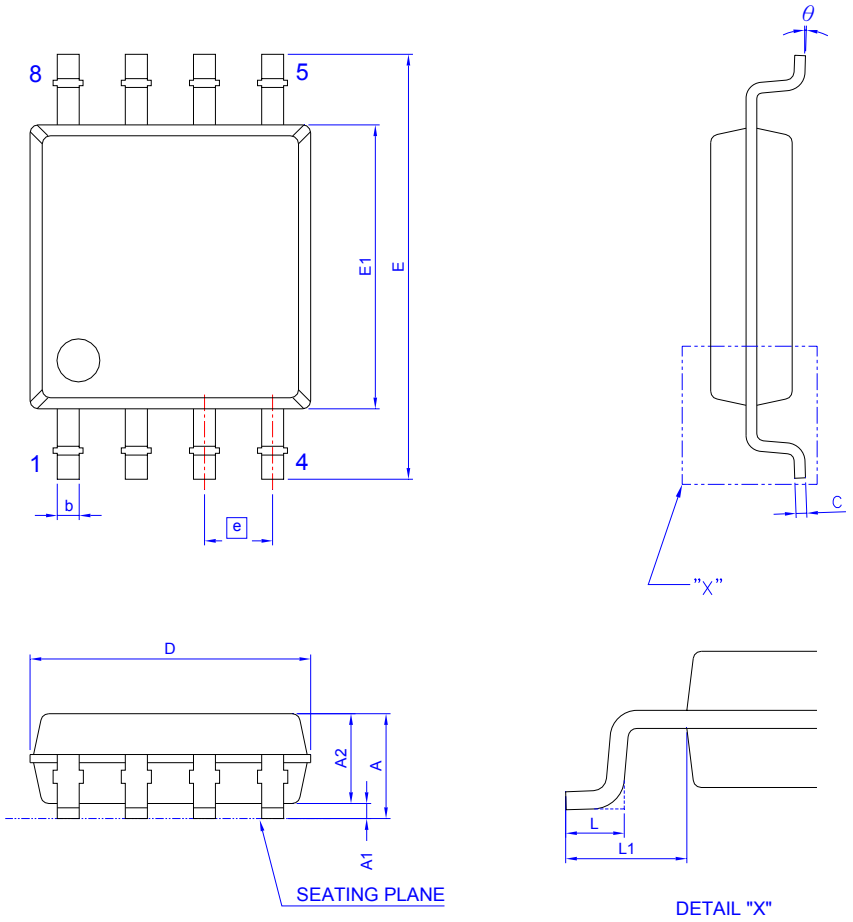


Figure 26: A TEST LOAD EXAMPLE

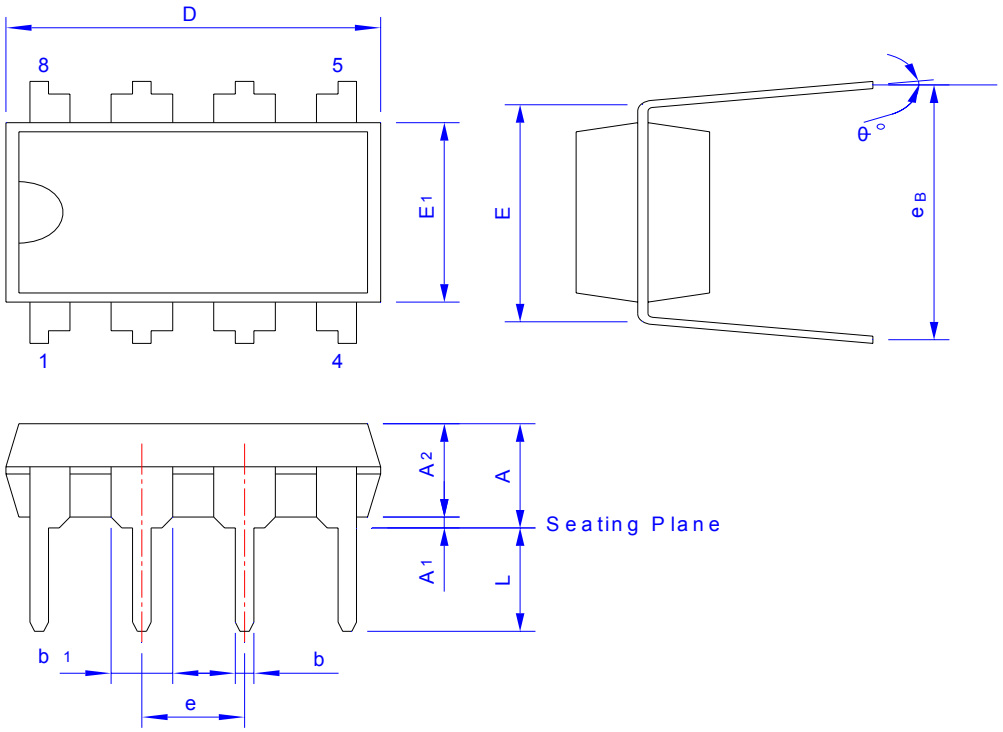
PACKING DIMENSIONS
8-LEAD SOIC 200 mil (official name – 209 mil)



Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	---	---	2.16	---	---	0.085	E	7.70	7.90	8.10	0.303	0.311	0.319
A_1	0.05	0.15	0.25	0.002	0.006	0.010	E_1	5.18	5.28	5.38	0.204	0.208	0.212
A_2	1.70	1.80	1.91	0.067	0.071	0.075	L	0.50	0.65	0.80	0.020	0.026	0.032
b	0.36	0.41	0.51	0.014	0.016	0.020	e	1.27 BSC			0.050 BSC		
c	0.19	0.20	0.25	0.007	0.008	0.010	L_1	1.27	1.37	1.47	0.050	0.054	0.058
D	5.13	5.23	5.33	0.202	0.206	0.210	θ	0°	---	8°	0°	---	8°

Controlling dimension : millimenter

PACKING DIMENSIONS
8-LEAD P-DIP (300 mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	——	——	5.00	——	——	0.21
A_1	0.38	——	——	0.015	——	——
A_2	3.18	3.30	3.43	0.125	0.130	0.135
D	9.02	9.27	10.16	0.355	0.365	0.400
E	7.62 BSC.			0.300 BSC.		
E_1	6.22	6.35	6.48	0.245	0.250	0.255
L	9.02	9.27	10.16	0.115	0.130	0.150
e	2.54 TYP.			0.100 TYP.		
e_B	8.51	9.02	9.53	0.335	0.355	0.375
b	0.46 TYP.			0.018 TYP.		
b_1	1.52 TYP.			0.060 TYP.		
θ^o	0^o	7^o	15^o	0^o	7^o	15^o

Controlling dimension : Inch.

Revision History

Revision	Date	Description
1.0	2008.02.25	Original
1.1	2008.03.18	1. Add PDIP package. 2. Add T_{BP1} and T_{BP2}.
1.2	2008.07.17	1. Add Dual Output function 2. Add power-up timing specification 3. Add Revision History 4. Modify tSE timing

Important Notice

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.