

Reduced ARM ISA

Storage space

In this exercise, ARM uses

- 4 Gigabytes (2^{32} bytes) of memory
- A register file of 16 registers of 32 bits each. They are called r0, r1, up to r15.

Reduced instruction set description

Transfer instructions			
Instruction	Mnemonic	Operation	Example
Load word	ldr rd, [rn, #offset]	$rd \leftarrow \text{mem}[rn + \text{offset}]$	ldr r5, [r0, #32] $r5 \leftarrow \text{mem}[32+r0]$
Store word	str rd, [rn, #offset]	$\text{mem}[rn + \text{offset}] \leftarrow rd$	str r4, [r2, #16] $\text{mem}[16+r2] \leftarrow r4$
Move	mov rd, rn	$rd \leftarrow rn$	mov r3, r4 $r3 \leftarrow r4$
Move immediate	mov rd, #imm	$rd \leftarrow \text{imm}$	mov r3, #15 $r3 \leftarrow 15$
Arithmetic-logical instructions			
Instruction	Mnemonic	Operation	Example
Add Immediate	add rd, rn, #imm	$rd \leftarrow rn + \text{imm}$	addi r5, r2, #-15 $r5 \leftarrow r2 + (-15)$
Add	add rd, rn, rm	$rd \leftarrow rn + rm$	add r2, r3, r4 $r2 \leftarrow r3 + r4$
Subtract	sub rd, rn, rm	$rd \leftarrow rn - rm$	sub r4, r5, r6 $r4 \leftarrow r5 - r6$
And Immediate	and rd, rn, #imm	$rd \leftarrow rn \wedge \text{imm}$	andi x5, x2, #2 $r5 \leftarrow r2 \wedge 2$
And	and rd, rn, rm	$rd \leftarrow rn \wedge rm$	and r2, r3, r4 $r2 \leftarrow r3 \wedge r4$
Or Immediate	or rd, rn, #imm	$rd \leftarrow rn \vee \text{imm}$	ori r5, r2, #2 $r5 \leftarrow r2 \vee 2$
Or	or rd, rn, rm	$rd \leftarrow rn \vee rm$	or r2, r3, r4 $r2 \leftarrow r3 \vee r4$
Shift Left Logical Immediate	lsl rd, rn, #imm	$rd \leftarrow rn \ll \text{imm}$	lsl r2, r3, #2 $r2 \leftarrow r3 \ll 2$
Shift Right Logical immed	lsr rd, rn, #imm	$rd \leftarrow rn \gg \text{imm}$	lsr r2, r3, #2 $r2 \leftarrow r3 \gg 2$

Control and comparison instructions			
Instruction	Mnemonic	Operation	Example
Compare	cmp rd, rn	flags \leftarrow flags(rd - rn)	cmp r1, r0
Branch Equal	beq label	if EQcond(flags) then pc \leftarrow label	beq loop
Branch Less Than	blt label	if LTcond(flags) then pc \leftarrow label	blt loop
Jump	b label	pc \leftarrow label	b loop
Jump and Link	bl label	r14 \leftarrow pc+4, pc \leftarrow label	bl loop
Jump Register	bx rd	pc \leftarrow rd	bx r14

The ARM processor stores a number of **flags** (flip-flops) that as conditions after executing some specific arithmetical-logical operations. Flag Z asserts if the result of an operation has been 0, flag N when the result is negative, flag C on carry out etc. Executing operations between values, those flags can be set. Control instructions **EQcond(flags)** test equality in a former instruction (via subtract). **LTCond(flags)** tests one has been smaller than the other.

Exercise

Given a list of common actions in assembly programming. Give for each action (a list of) instruction which would make it work. Describe the operands that are used.

Load a specific number into a register \rightarrow Load 5 into register 5
Move the content of one register to another \rightarrow Move the content of register 0 to register 6
Load a memory position content into a register \rightarrow Load mem[64] into register 4
Store a register content into a specific memory position \rightarrow r3 content in memory position 32