OpenROM: An Open-Source ROM Compiler

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Introduction

Education

2018 - 2023 UC Santa Cruz
BS. Computer Engineering

Work

2022 - 2023 Epilog.ai (Self driving cars)
Computer Engineer

2023 - now Zipline
Embedded Systems Engineer

Hobbies

Soundsystem Collective
Hobby Chemistry
Open-source FPGA projects

Background: Open Silicon and OpenRAM

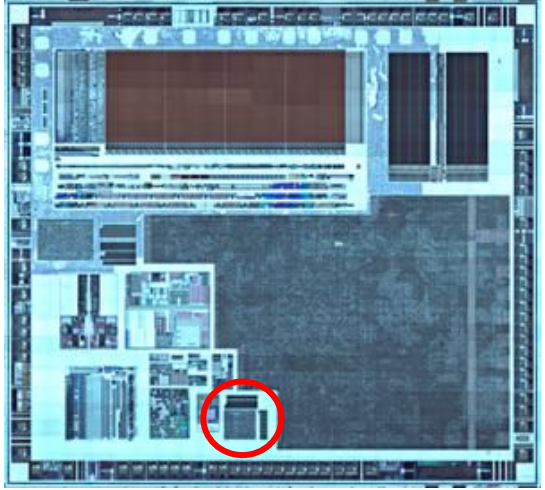
- SKY130 Open-sourced by Google and SkyWater Technologies in Nov 2020
- Growing ecosystem of open-source PDKs and EDA tooling
- OpenRAM first announced in 2016 as a platform for open-source memory development

Introduction: What is a Memory Compiler?

- EDA tool to assist designers in creating memory cells
- Generates a layout (GDSII) and schematic (SPICE)
- Runs DRC, LVS, characterization.
- Often provided by fab or proprietary design tools

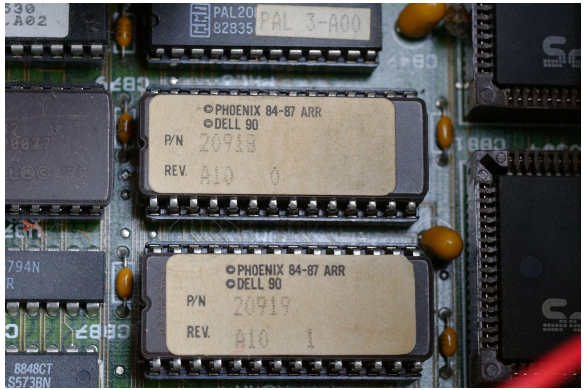
Introduction:
What is Mask ROM?

- Historically used for data storage
- Large NRE cost
- Phased out in favor of CD-ROM
- Replaced by flash memory in modern applications
- Sticks around to store FSB



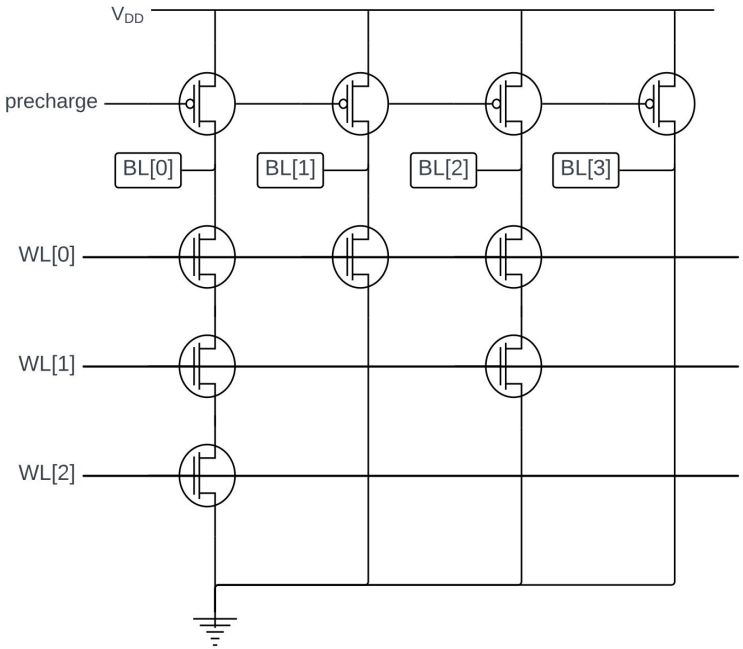
STM32F100 Die. Courtesy of siliconpr0n.org

NES Game Cartridge

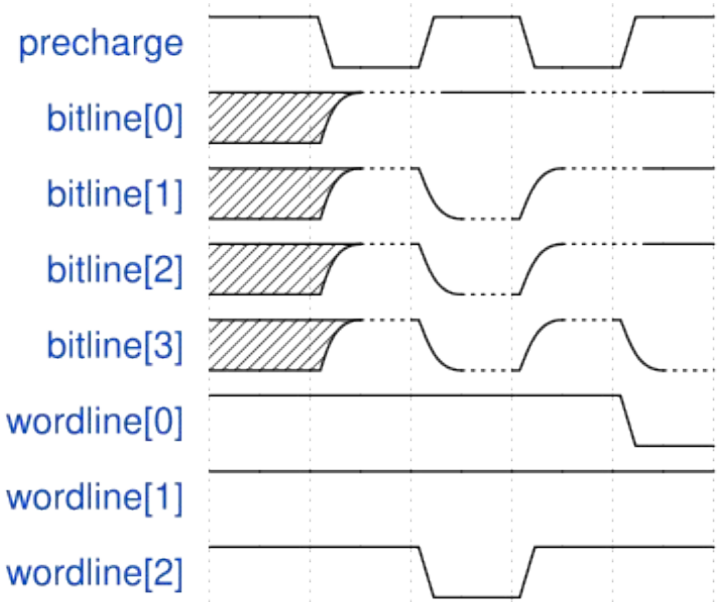


Dell 310 ROM BIOS chip

Introduction: NAND Read-Only Memory

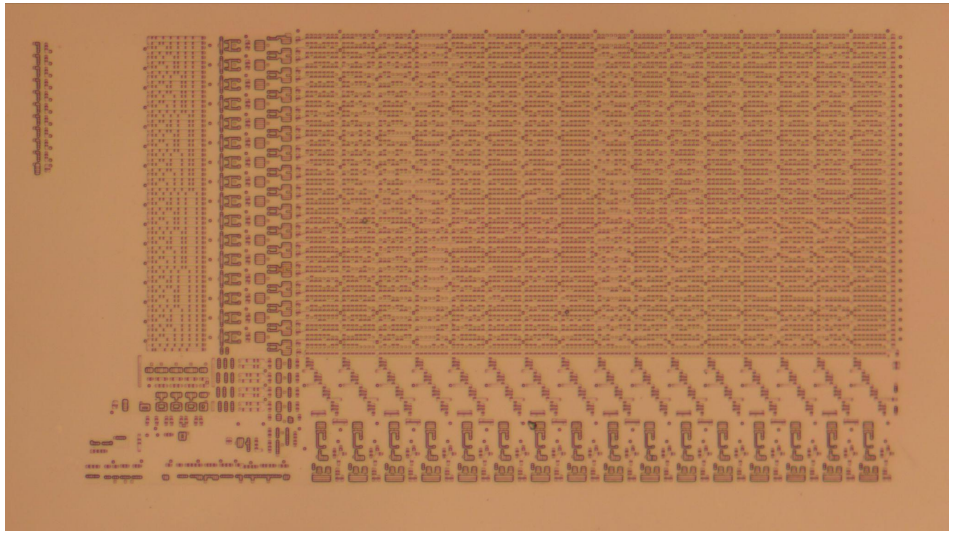


Schematic for NAND ROM array

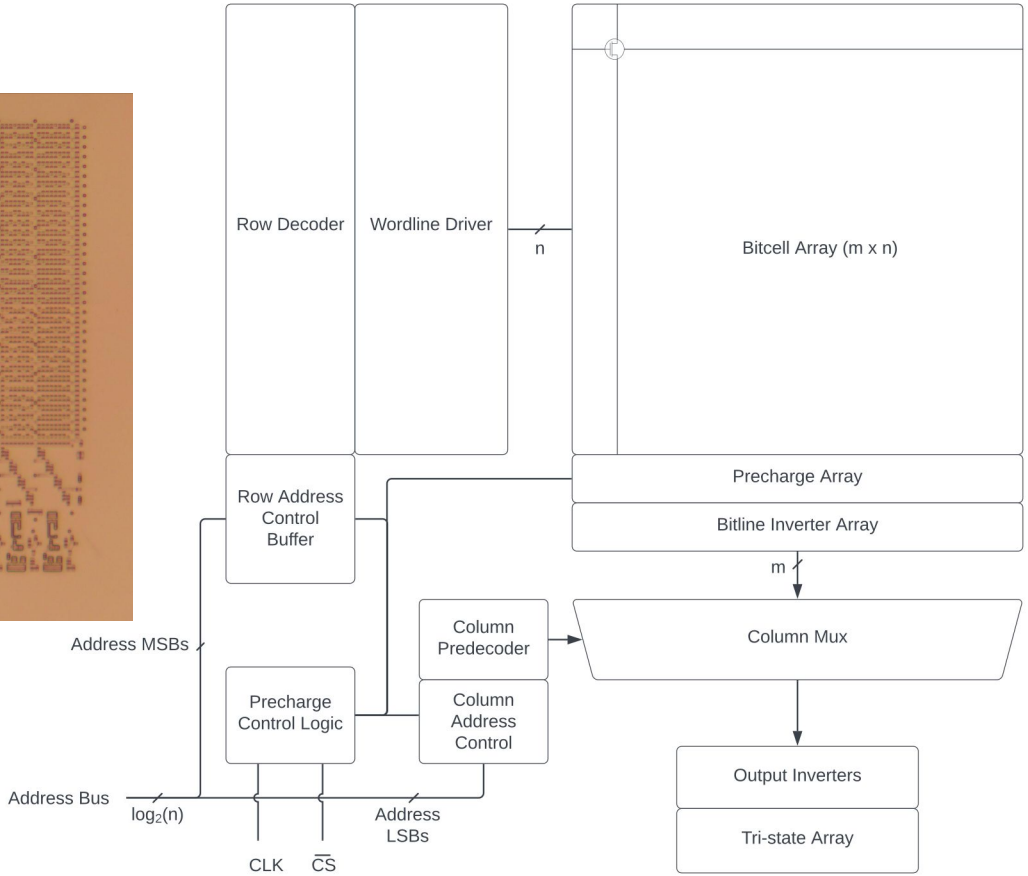


Read behavior of NAND ROM

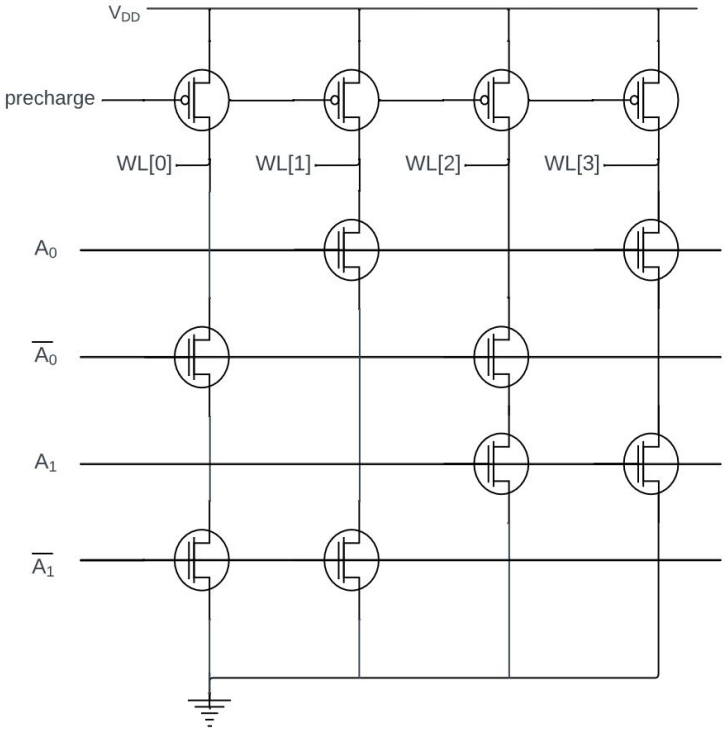
Hardware Architecture

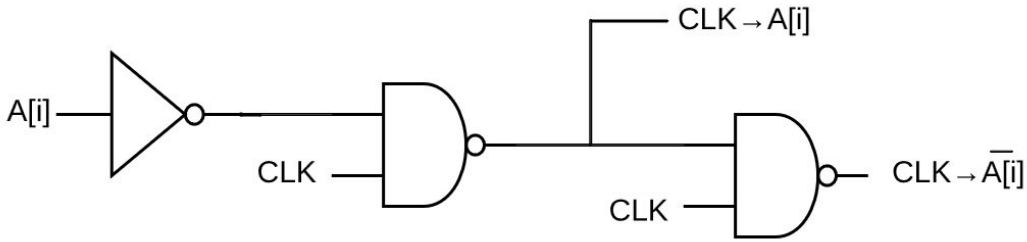


TI MSP430F149 MROM courtesy of Travis Goodspeed.



NAND Decoder

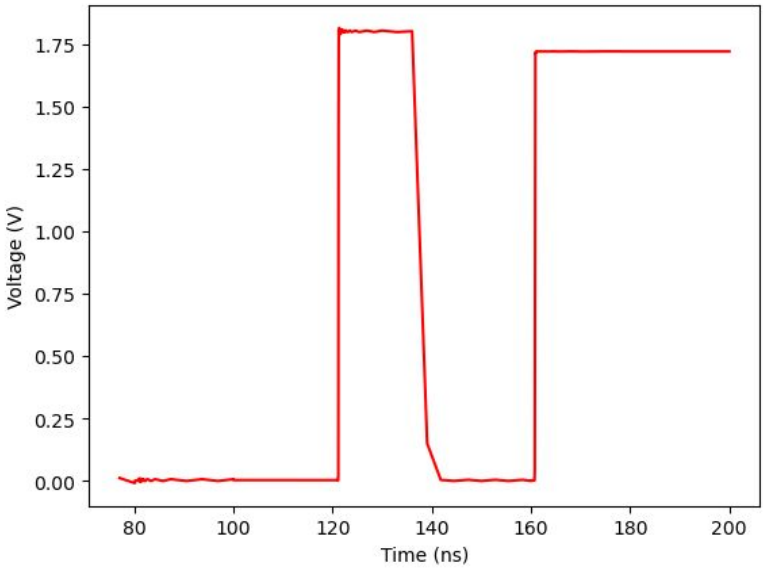




- Decoder converts N bit input signal into 2^N output signals
- NAND dynamic decoder conveniently re-uses the basic structure of NAND ROM
- Decoder requires monotonic address inputs

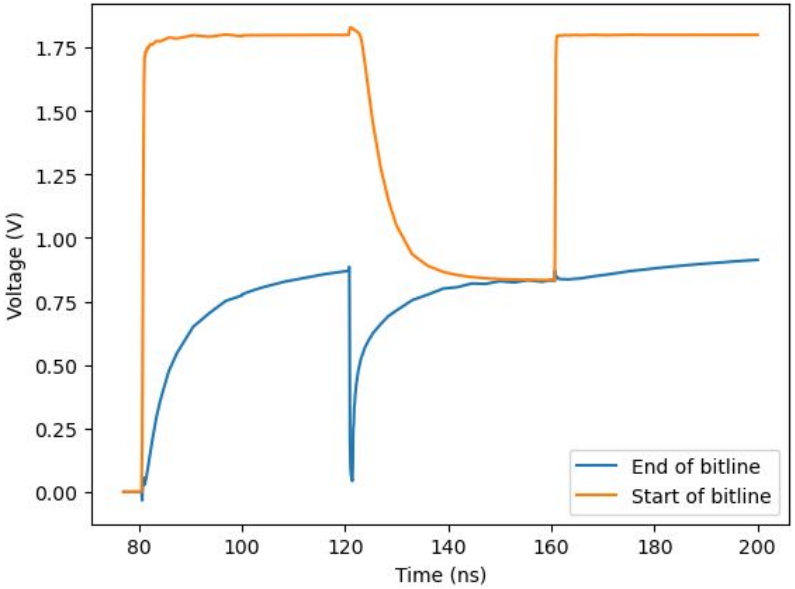
Functional Simulation

- Initial simulations failed to read data
- Solved by buffering data before column mux
- Further testing revealed partial read failures
- Data output falls half way through read cycle

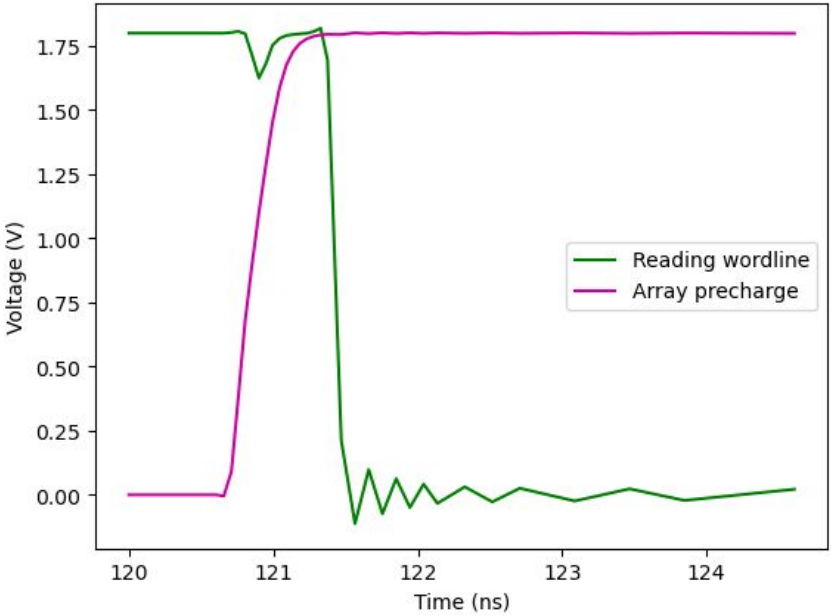


Data output signal during partial read failure

Read Failure Investigation



Bitline voltage during partial read failure



Active worldline vs. Precharge signal

Characterization

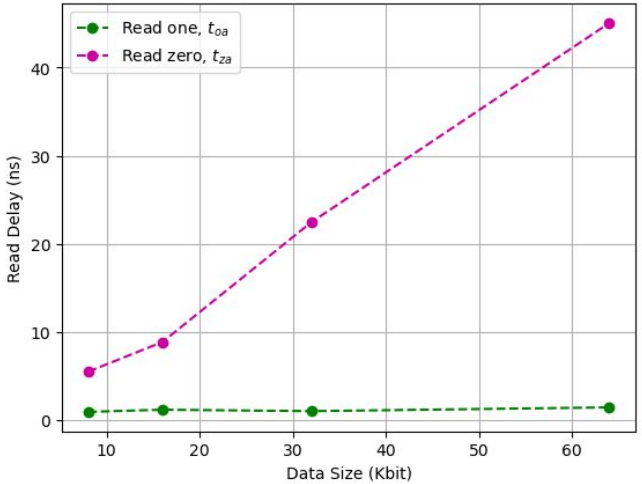
Timing characteristics

- Minimum clock period ~14ns @ 1kB
- Set-up time ~100ps @ 1kB
- Hold time ~3.7ns @ 1kB

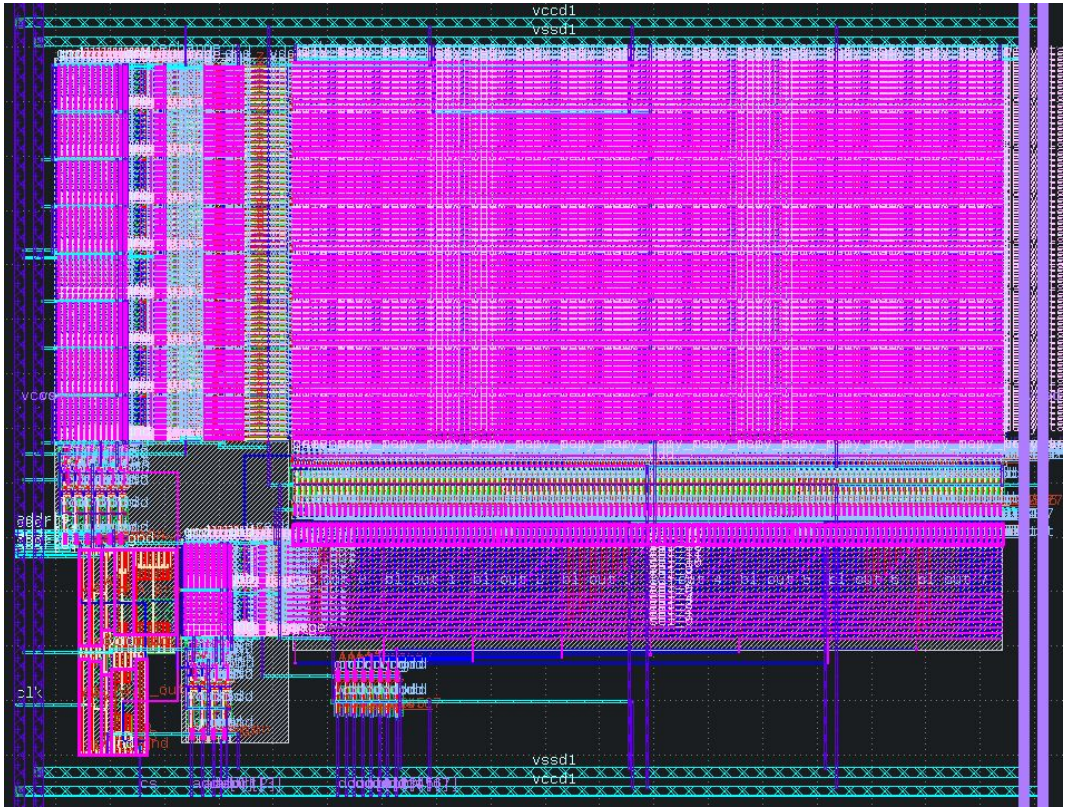
Decode delay still the largest performance limitation

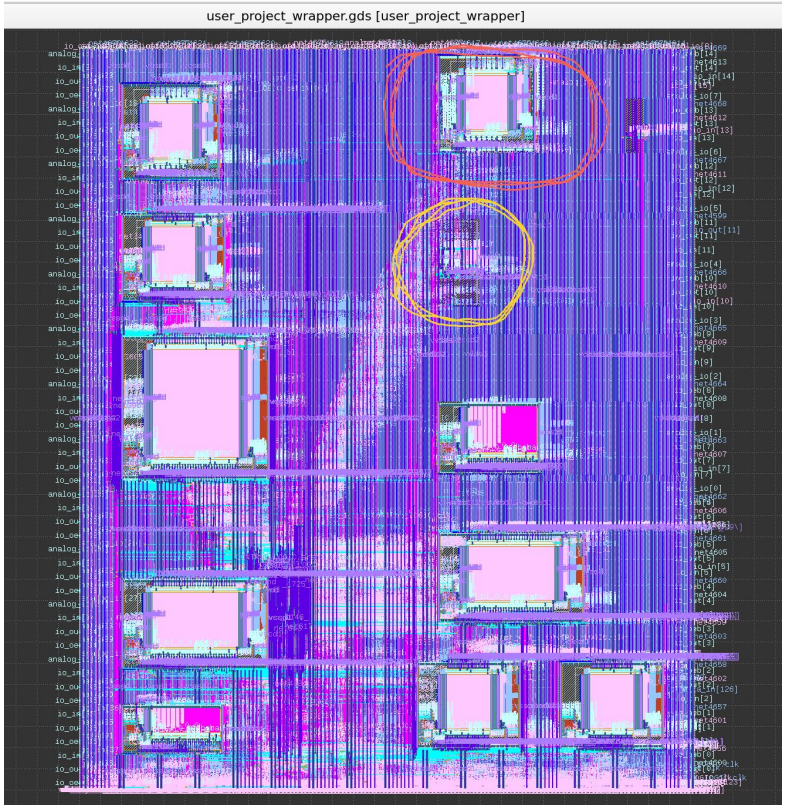
Setup/hold without capturing inputs/outputs in DFF

Power consumption not characterized with PEX



Final Hardware Revision and Tapeout





Thank You!