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# L11_1 LC2K-Datapath

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# Learning Objectives

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- Ability to trace and explain the flow of data in a single-cycle processor diagram, using the blocks from the previous lecture.
- Identify the timing and operation of control circuit for a single-cycle processor.

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# LC2Kx Datapath Implementation

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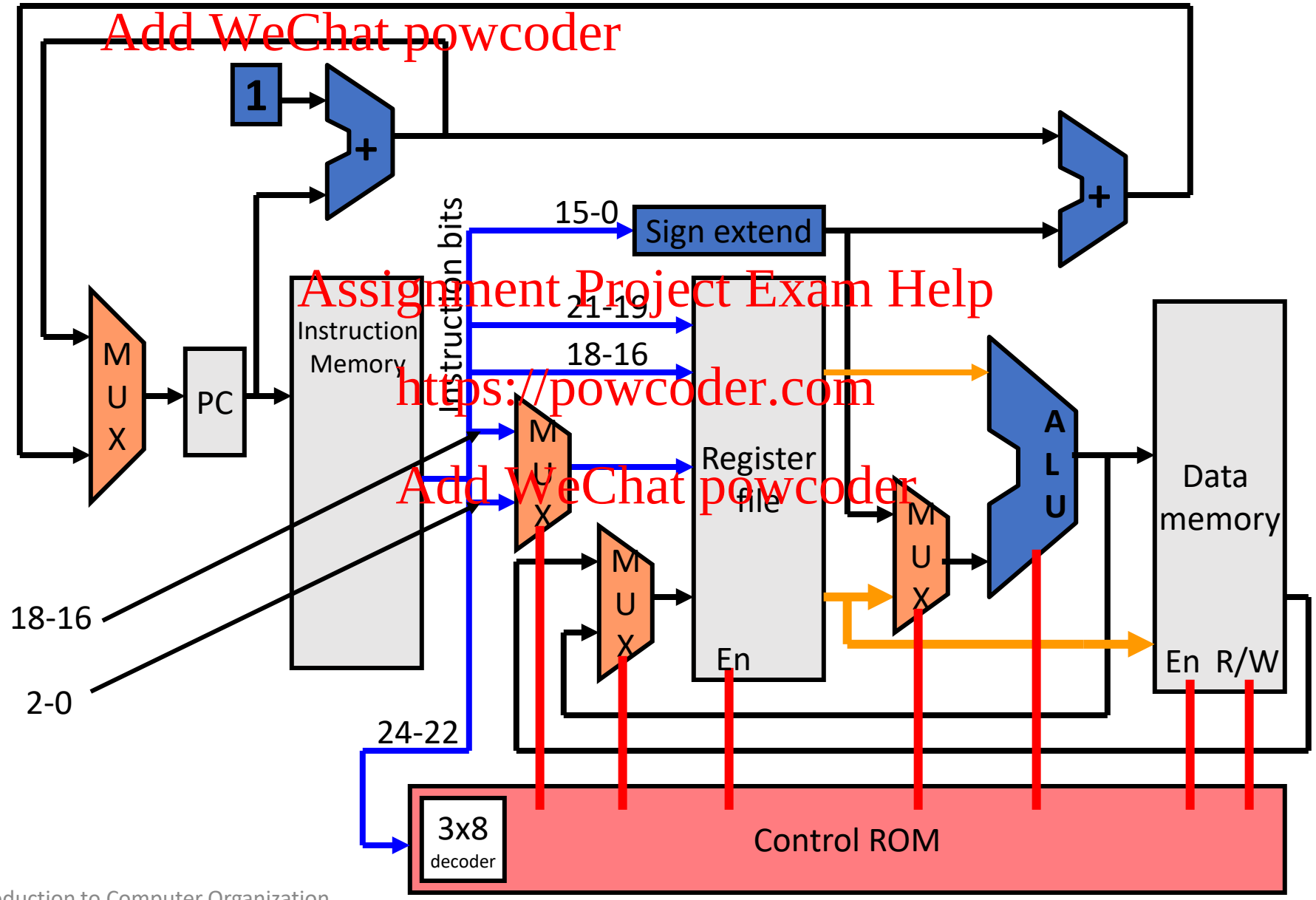
Single-Cycle Review



# Executing an SW Instruction

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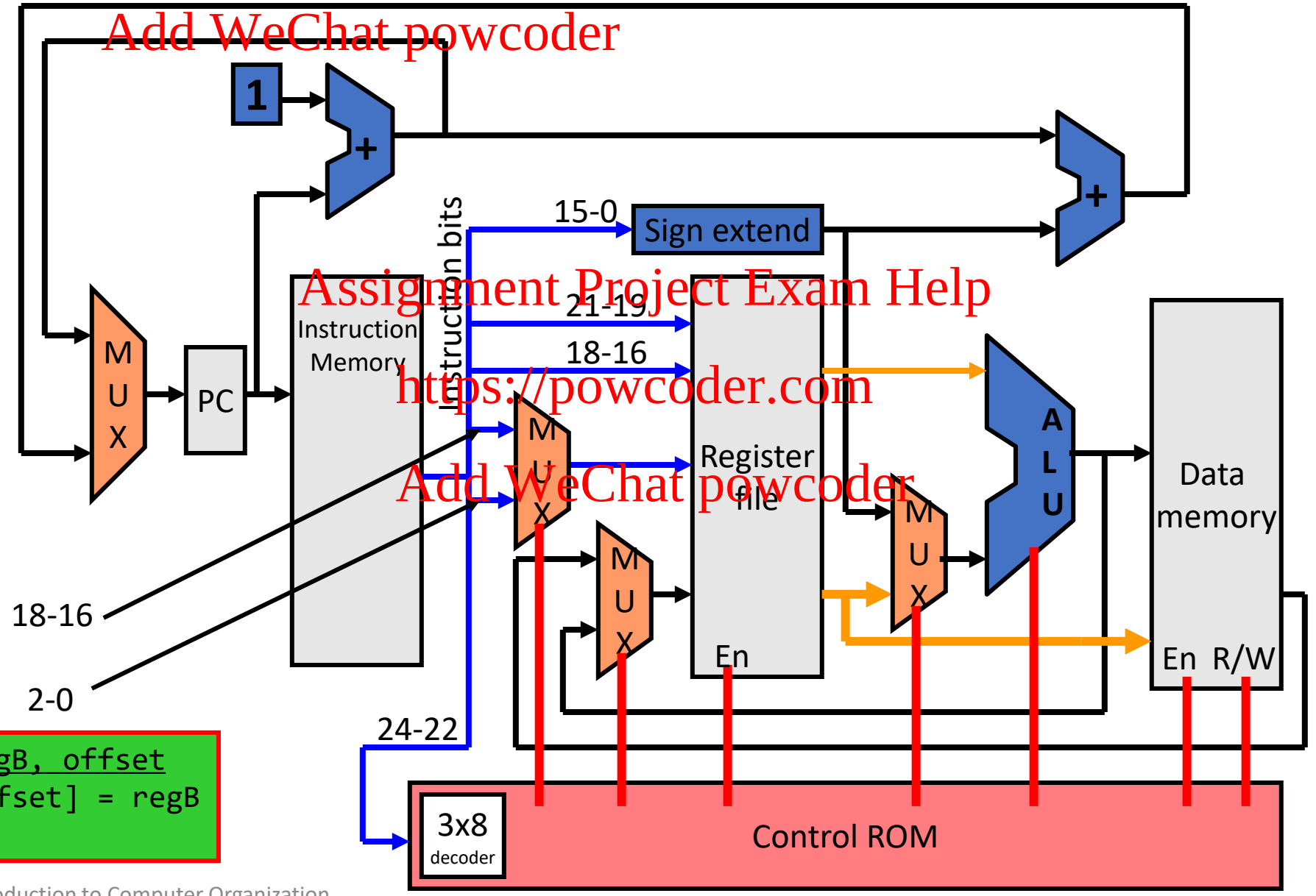
Single-Cycle




```
sw regA, regB, offset
M[regA + offset] = regB
PC = PC + 1
```

# Executing an SW Instruction

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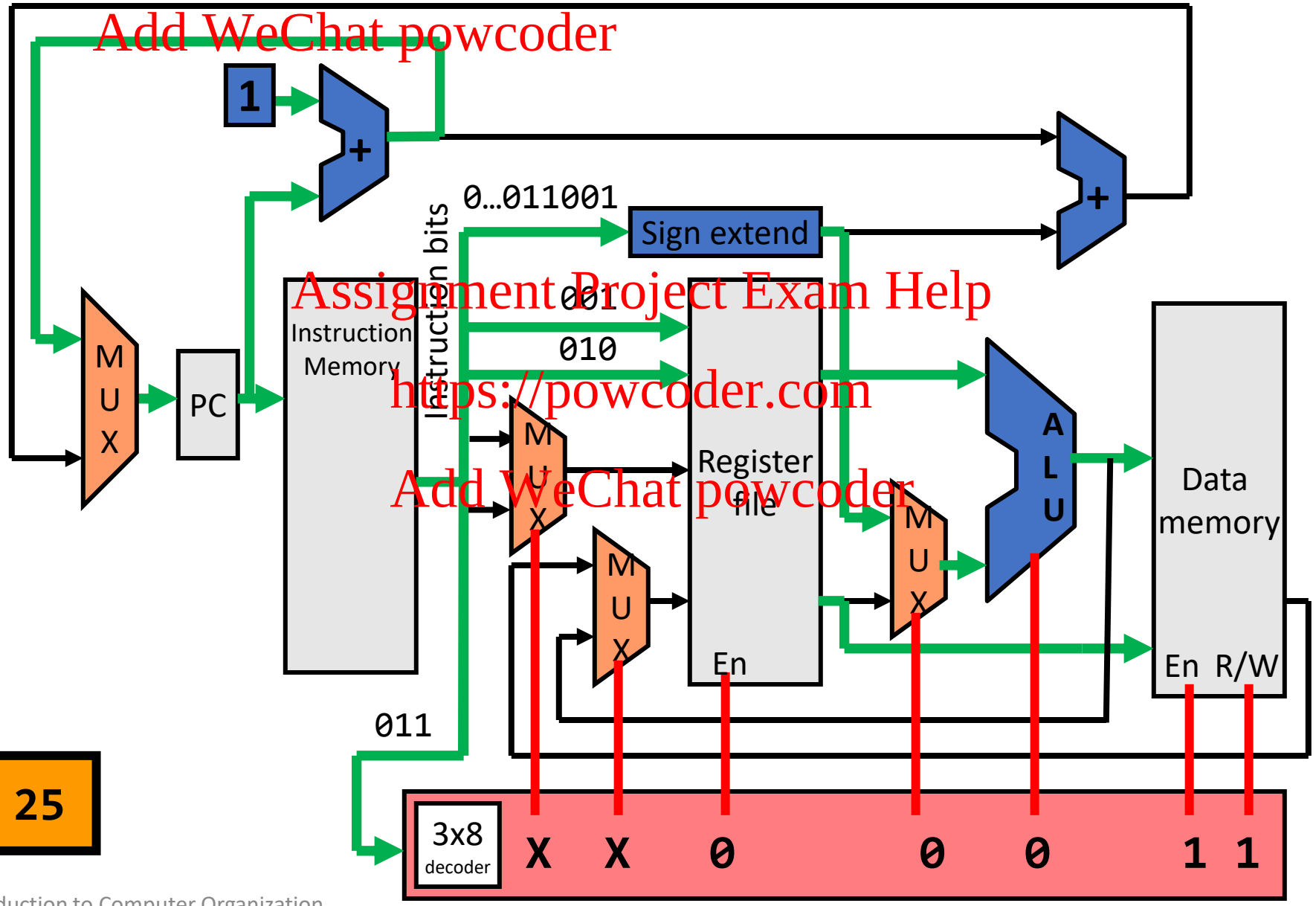
Single-Cycle




**sw 1 2 25**

# Executing a BEQ Instruction

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Single-Cycle

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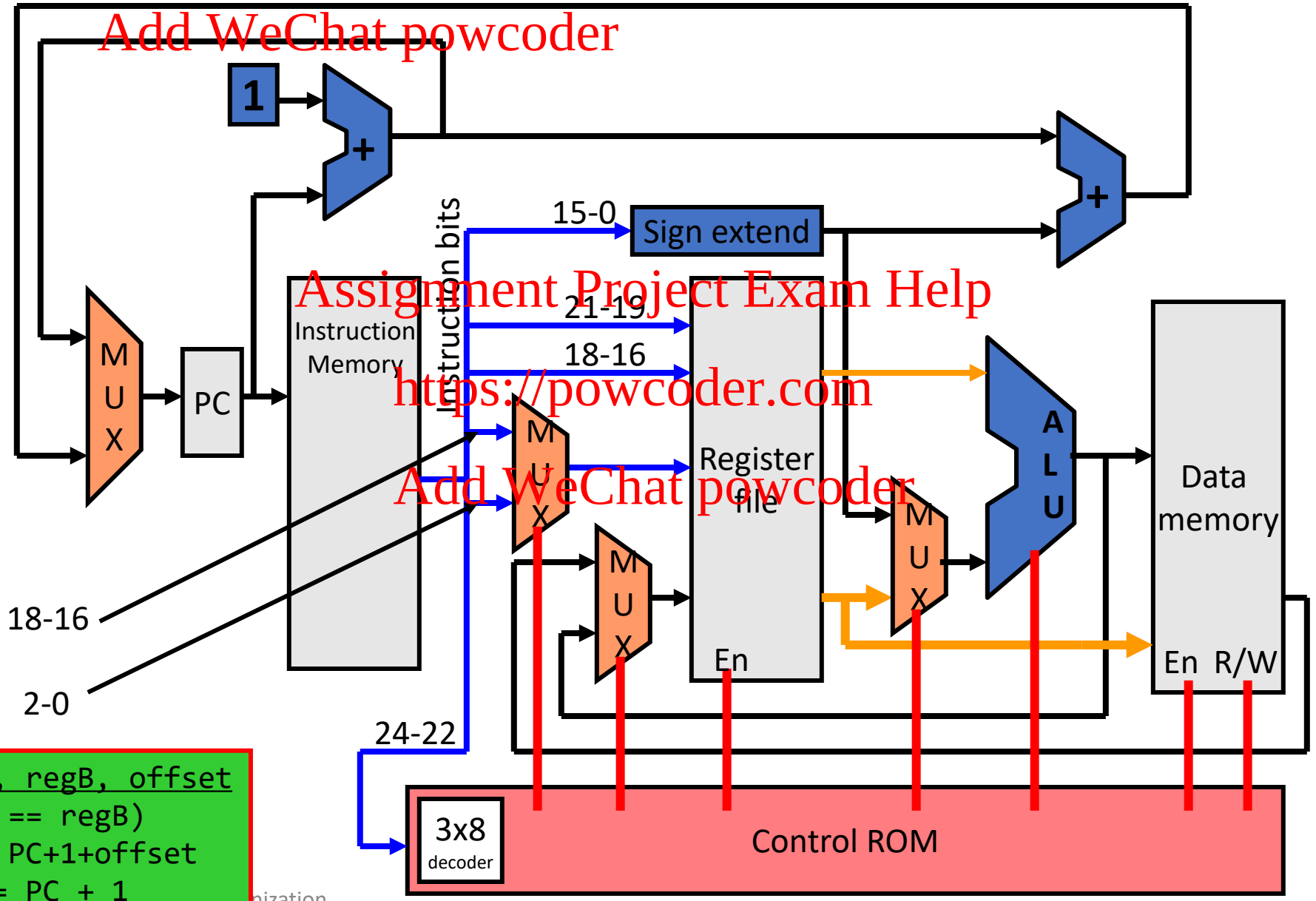


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```
beq regA, regB, offset
if (regA == regB)
    PC = PC+1+offset
else PC = PC + 1
```

# Executing "not taken" BEQ Instruction

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Single-Cycle

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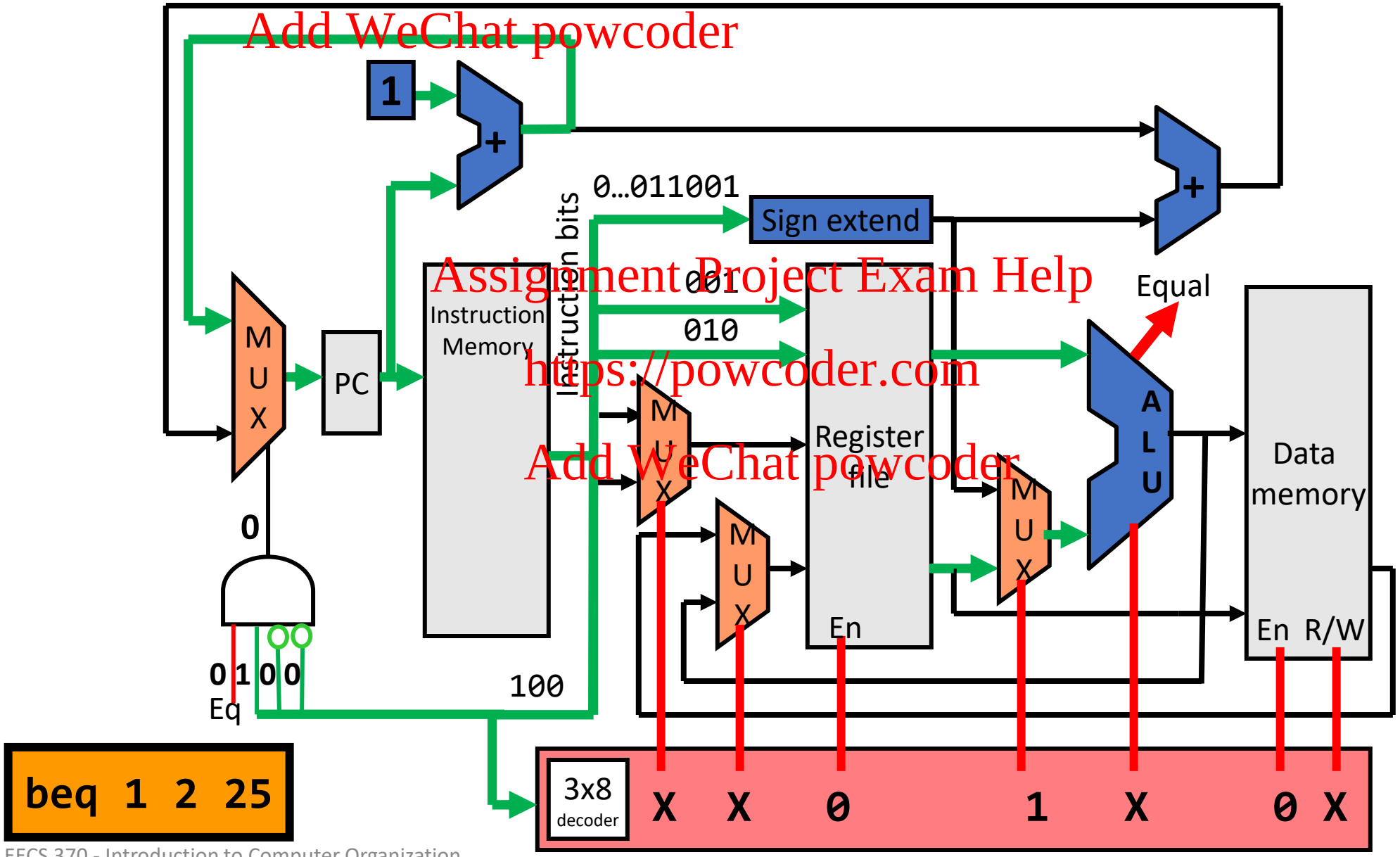


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# Executing "taken" BEQ Instruction

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Single-Cycle

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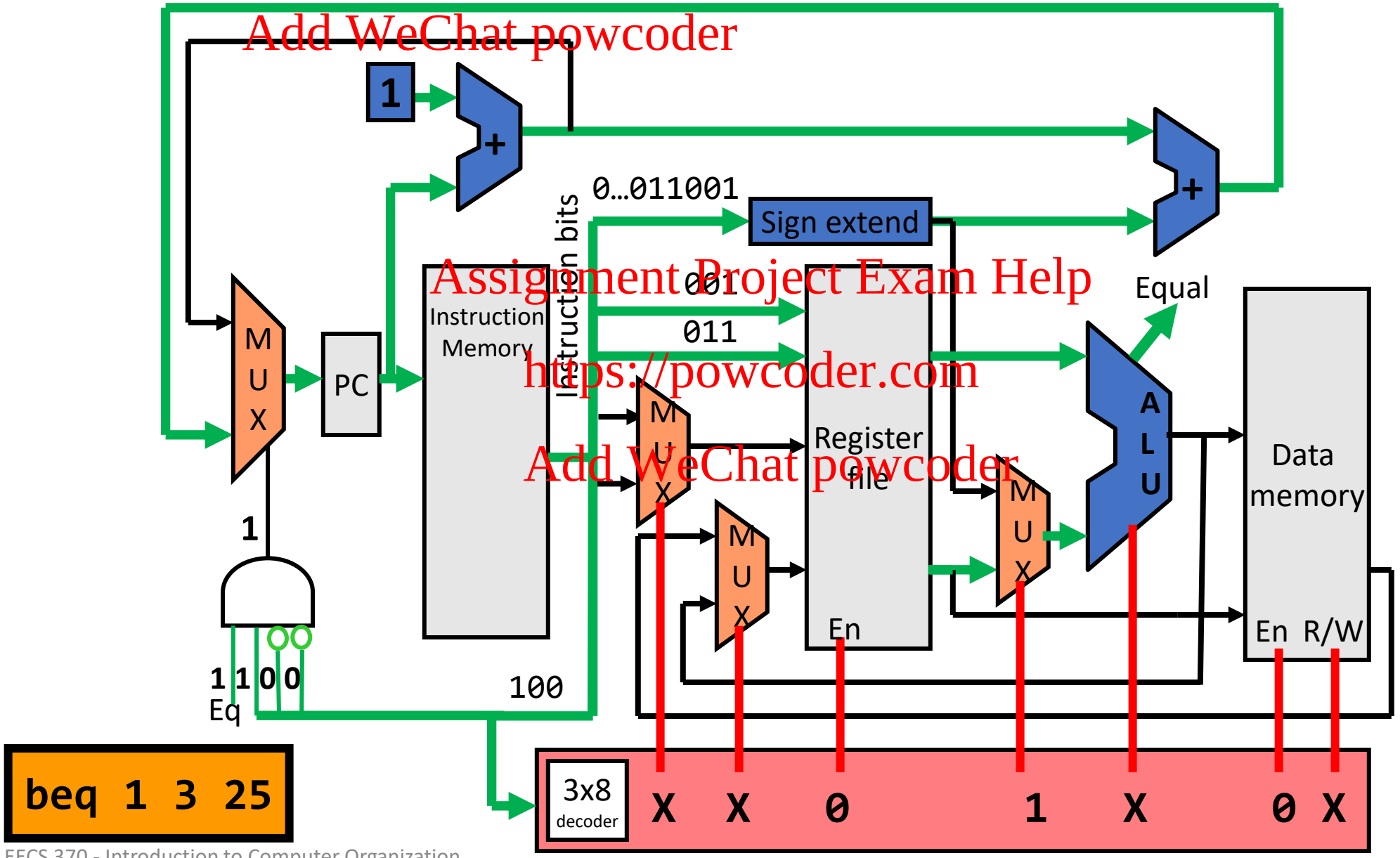


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```
beq 1 3 25
```

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# So Far, So Good

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- Every architecture seems to have at least one ugly instruction.
  - JALR doesn't fit into our nice clean datapath

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- To implement JALR we need to

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  - Write PC+1 into regB
  - Move regA into PC

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- Right now there is:
  - No path to write PC+1 into a register
  - No path to write a register to the PC

# Executing a JALR Instruction

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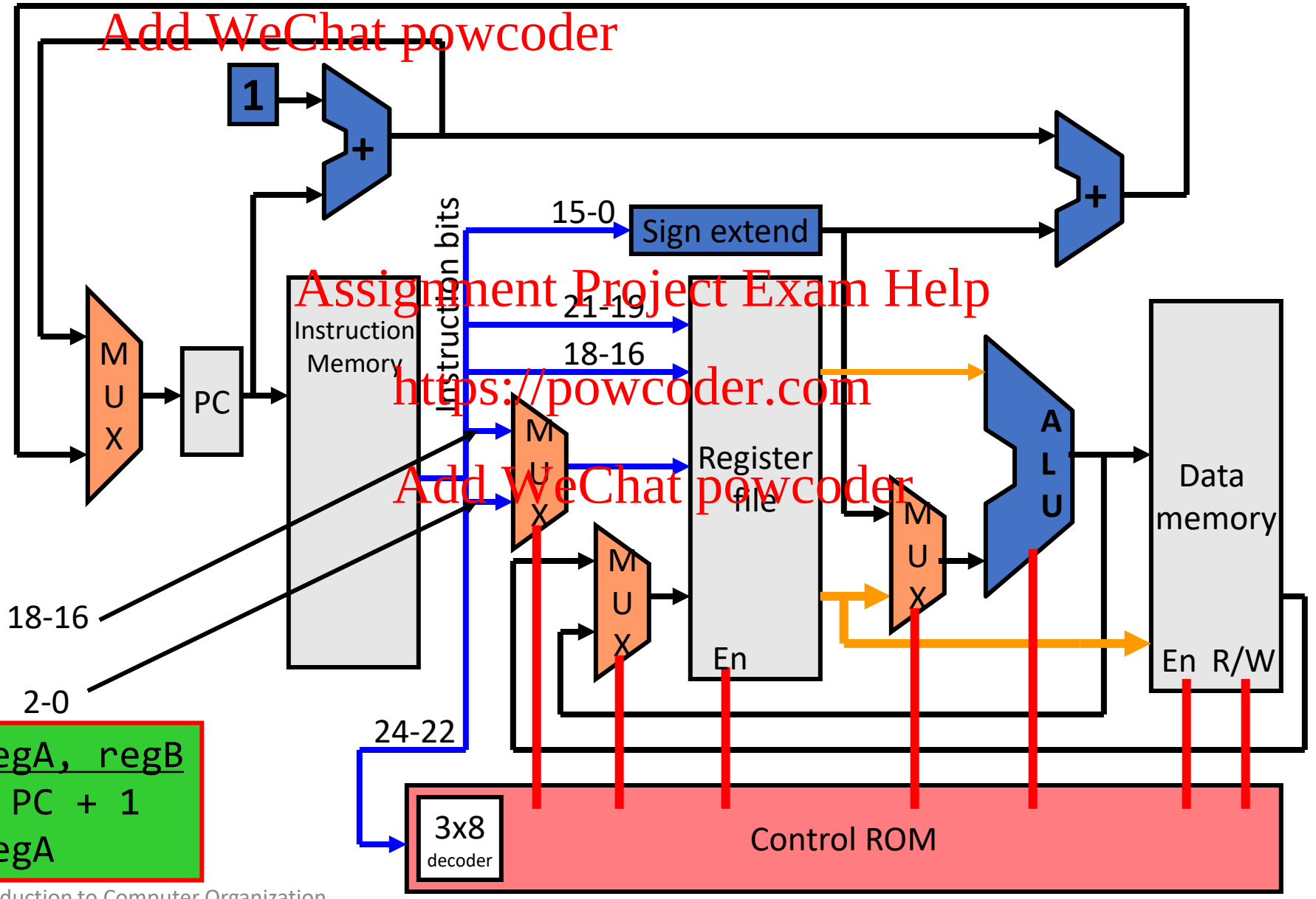
Single-Cycle

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```
jalr regA, regB
regB = PC + 1
PC = regA
```

# Executing a JALR Instruction

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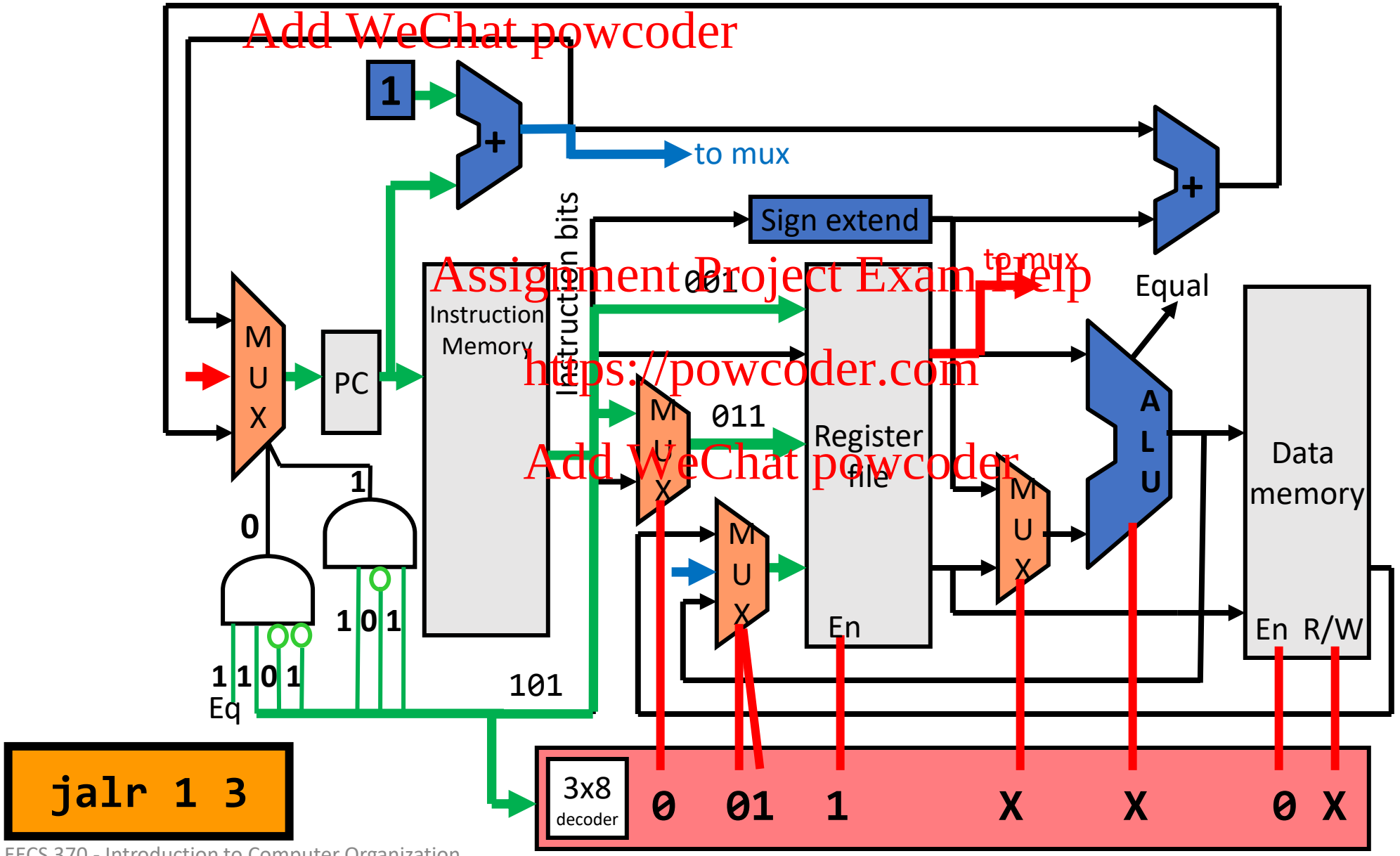
Single-Cycle



# What If negA = negB for a **JALR** ?

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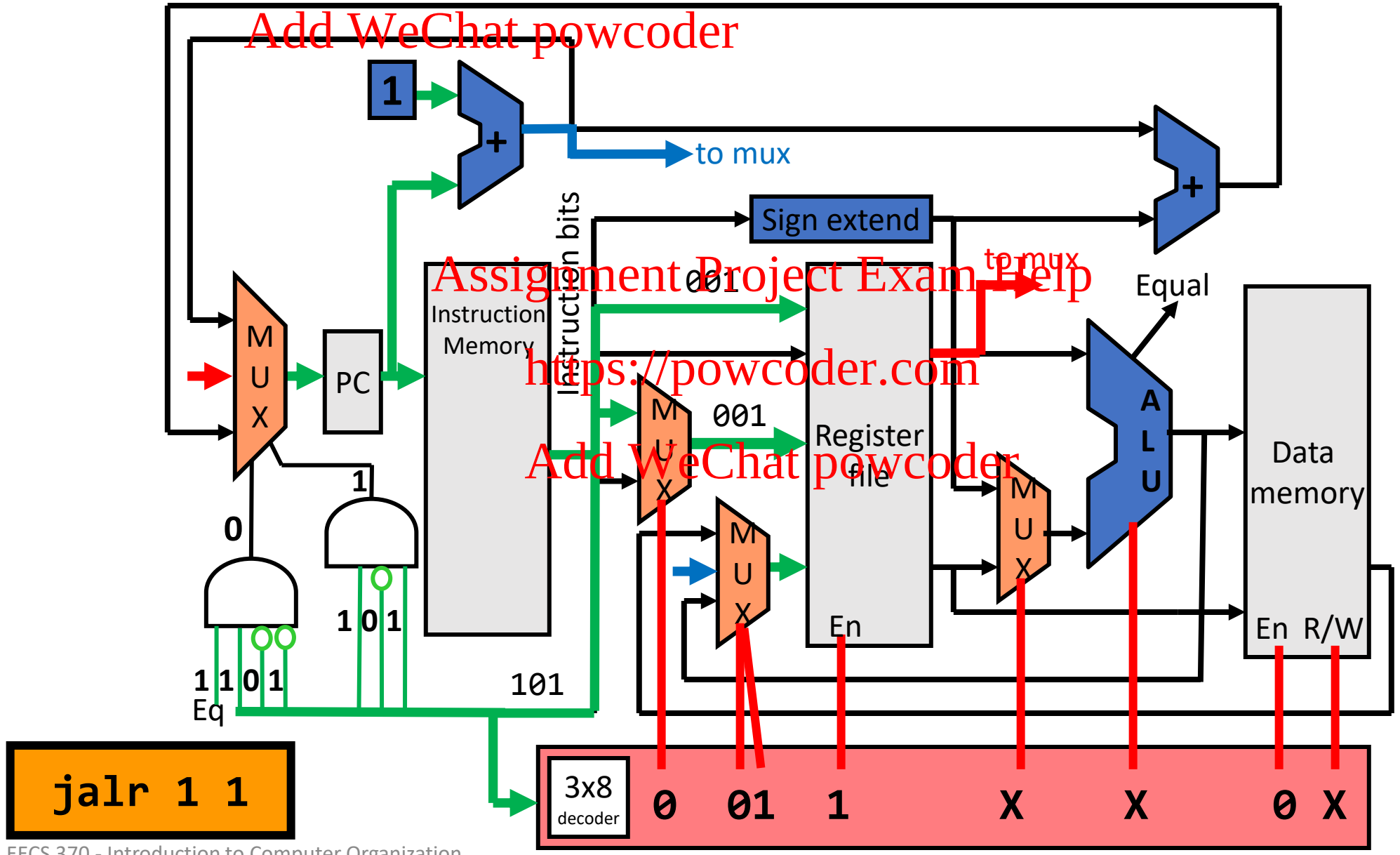
Single-Cycle



# Changes for a JALR 1 1 Instruction

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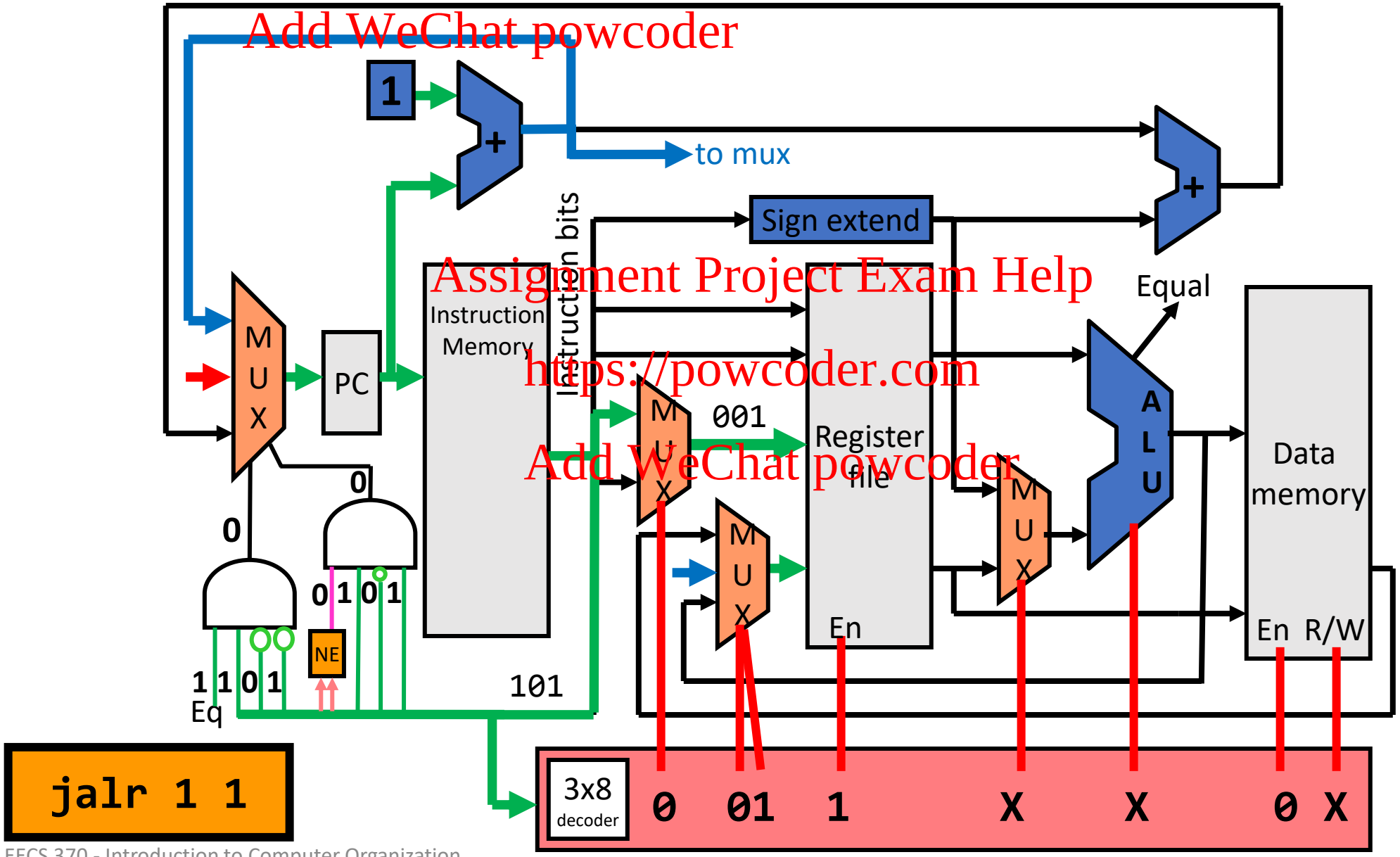
Single-Cycle



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# What is Wrong with Single Cycle?

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- **All instructions run at the speed of the slowest instruction.**
- Adding a long instruction can hurt performance
  - What if you wanted to include multiply?
- You cannot reuse any parts of the processor
  - We have 3 different adders to calculate PC+1, PC+1+offset and the ALU
- No benefit in making the common case fast
  - Since every instruction runs at the slowest instruction speed
  - This is particularly important for loads as we will see later

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# Single Cycle Timing

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Problem: What is latency for LC2K instruction execution?

Latencies:
1 ns – Register read/write time
2 ns – ALU/adder
2 ns – memory access (read or write)
0 ns – MUX, PC access, sign extend, ROM, wires

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| Inst. | get instr | read register | ALU operation | memory read/write | write register | total |
|---|---|---|---|---|---|---|
| add | | | | | | |
| beq | | | | | | |
| sw | | | | | | |
| lw | | | | | | |

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# Single Cycle Timing

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Problem: What is latency for LC2K instruction execution?

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| Inst. | get instr | read register | ALU operation | memory read/write | write register | total |
|---|---|---|---|---|---|---|
| add | 2 ns | 1 ns | 2 ns | | 1 ns | 6 ns |
| beq | 2 ns | 1 ns | 2 ns | | | 5 ns |
| sw | 2 ns | 1 ns | 2 ns | 2 ns | | 7 ns |
| lw | 2 ns | 1 ns | 2 ns | 2 ns | 1 ns | 8 ns |

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# Computing Execution Time

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Assume: 100 instructions executed

- 25% of instructions are loads,
- 10% of instructions are stores,
- 45% of instructions are adds, and
- 20% of instructions are branches.

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| Inst. | total |
|---|---|
| add | 6 ns |
| beq | 5 ns |
| sw | 7 ns |
| lw | 8 ns |

Single-cycle execution:

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??

Optimal execution:

??

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# Computing Execution Time

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Assume: 100 instructions executed

- 25% of instructions are loads,
- 10% of instructions are stores,
- 45% of instructions are adds, and
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| Inst. | total |
|---|---|
| add | 6 ns |
| beq | 5 ns |
| sw | 7 ns |
| lw | 8 ns |

Single-cycle execution:

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100 * 8ns = **800** ns

Optimal execution:

25*8ns + 10*7ns + 45*6ns + 20*5ns = **640** ns

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# Logistics

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- There are 3 videos for lecture 11
  - L11_1 – LC2K-Datapath_Single-Cycle
  - L11_2 – Multi-Cycle_0
  - L10_3 – Multi-Cycle_1
- There is one worksheet for lecture 10
  1. L11 worksheet

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# L11_2 Multi-Cycle

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# Learning Objectives

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- Identify the patterns seen in single-cycle LC2K processor.
- Mapping to the datapath to enable different execution times for different instructions.
- Ability to trace and explain the flow of data in a multi-cycle processor diagram and the timing and operation of the control circuit for a multi-cycle processor.

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# Multiple-Cycle Execution

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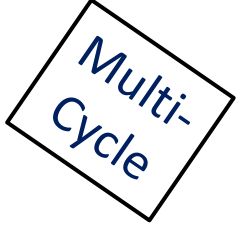


- Each instruction takes multiple cycles to execute
  - Cycle time is reduced
  - Slower instructions take more cycles
  - Faster instruction take fewer cycles
    - We can start next instruction earlier, rather than just waiting
  - Can reuse datapath elements each cycle
- What is needed to make this work?
  - Since you are re-using elements for different purposes, you need more and/or wider MUXes.
  - You may need extra registers if you need to remember an output for 1 or more cycles.
  - Control is more complicated since you need to send new signals on each cycle.

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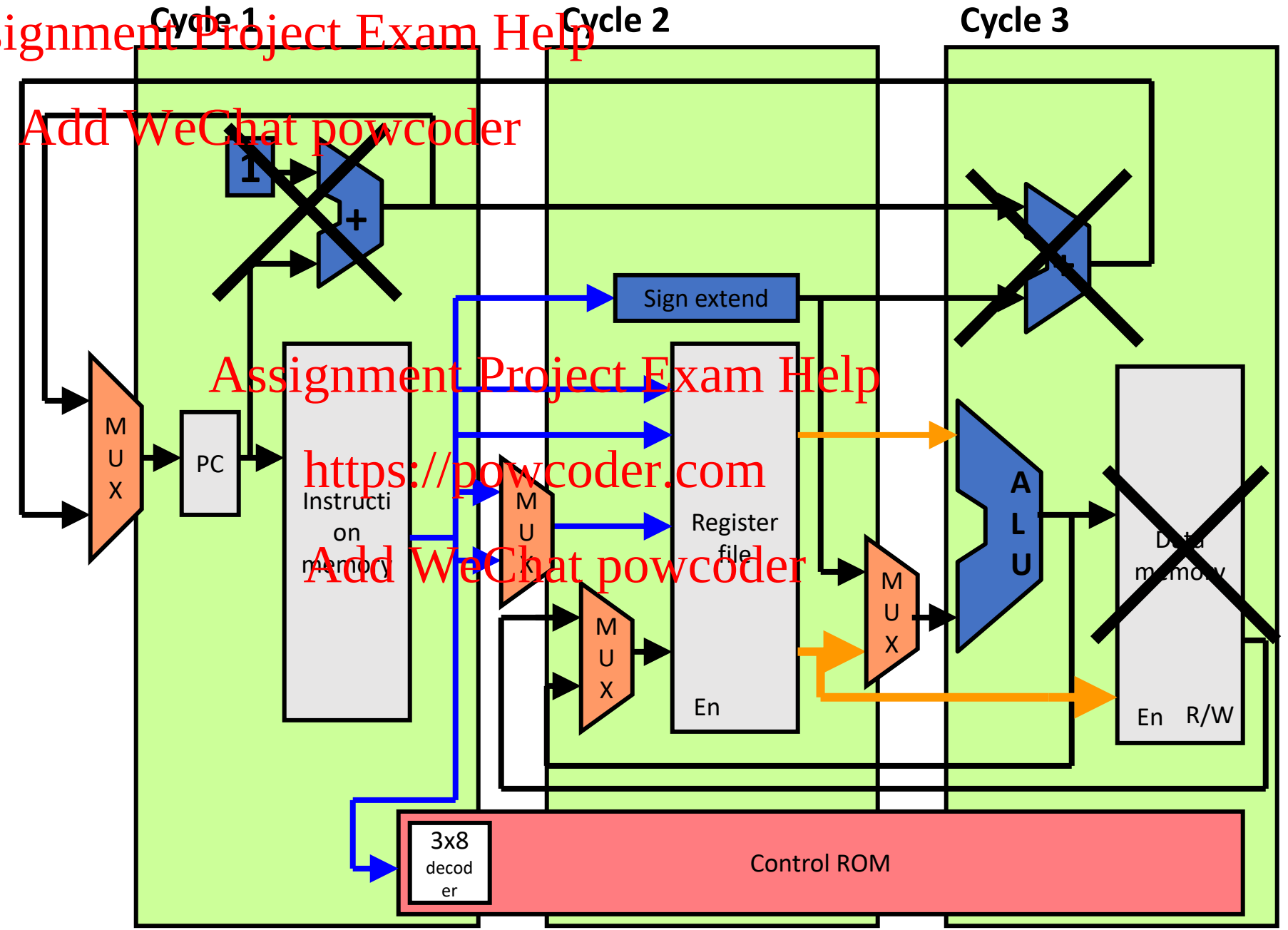
Multi-Cycle

add instruction will take 4 cycles (but cycles will be shorter). Only use the # of shorter cycles needed for the instruction

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# Multicycle LC2K Datapath

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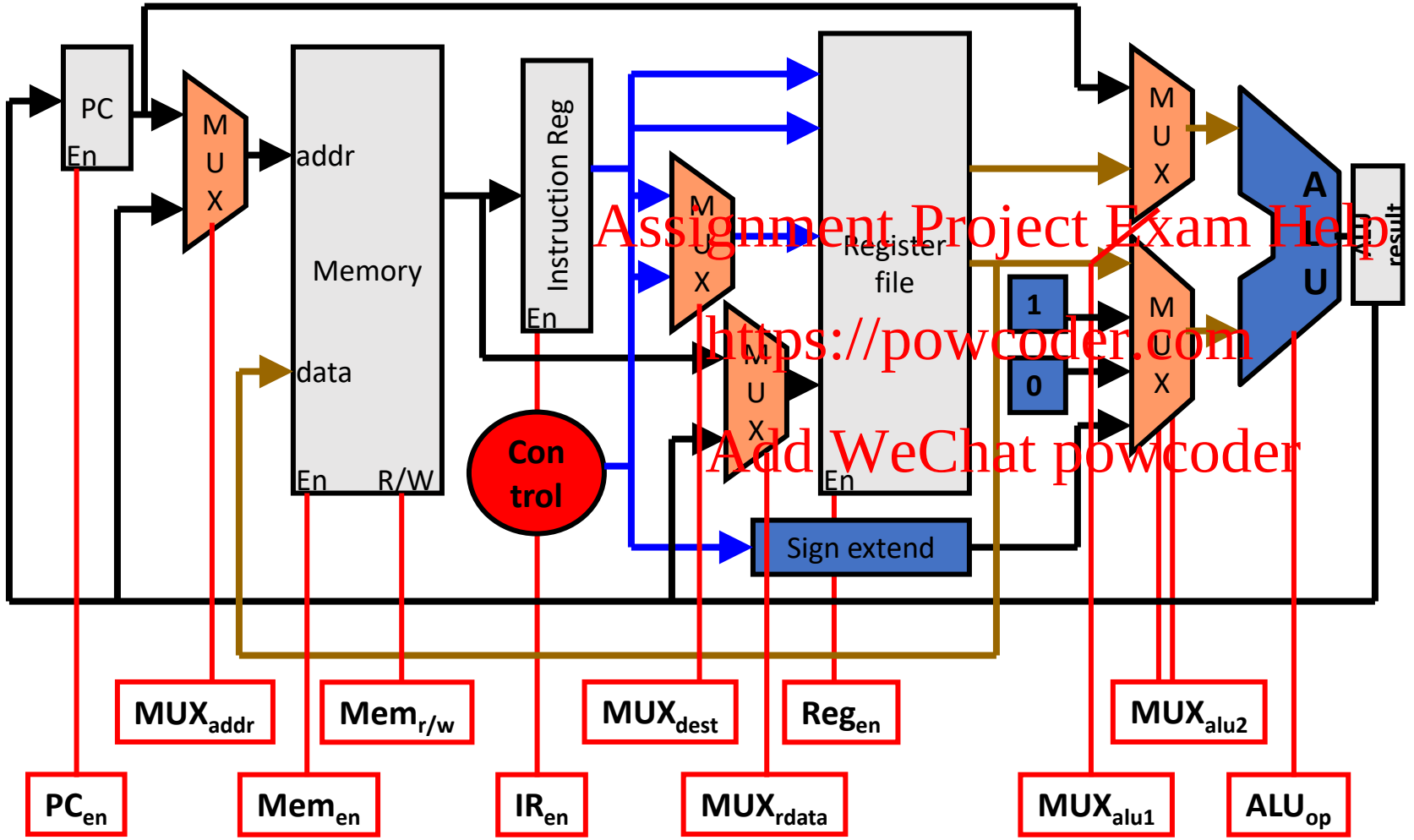


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# FSM – Multi-Cycle Control Signals

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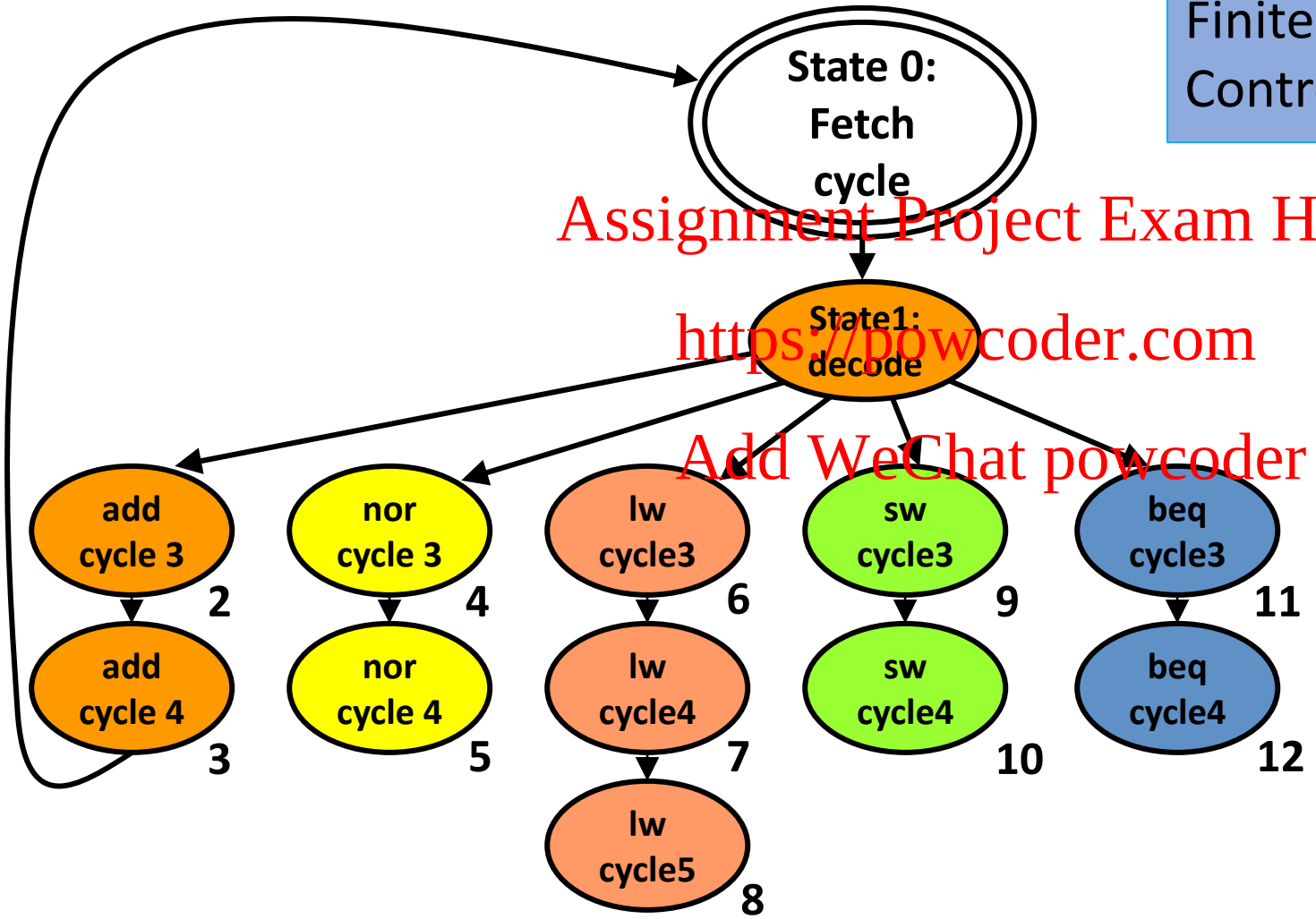
Multi-Cycle

Finite State Machine
Control signals (transition functions)

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# Implementing FSM

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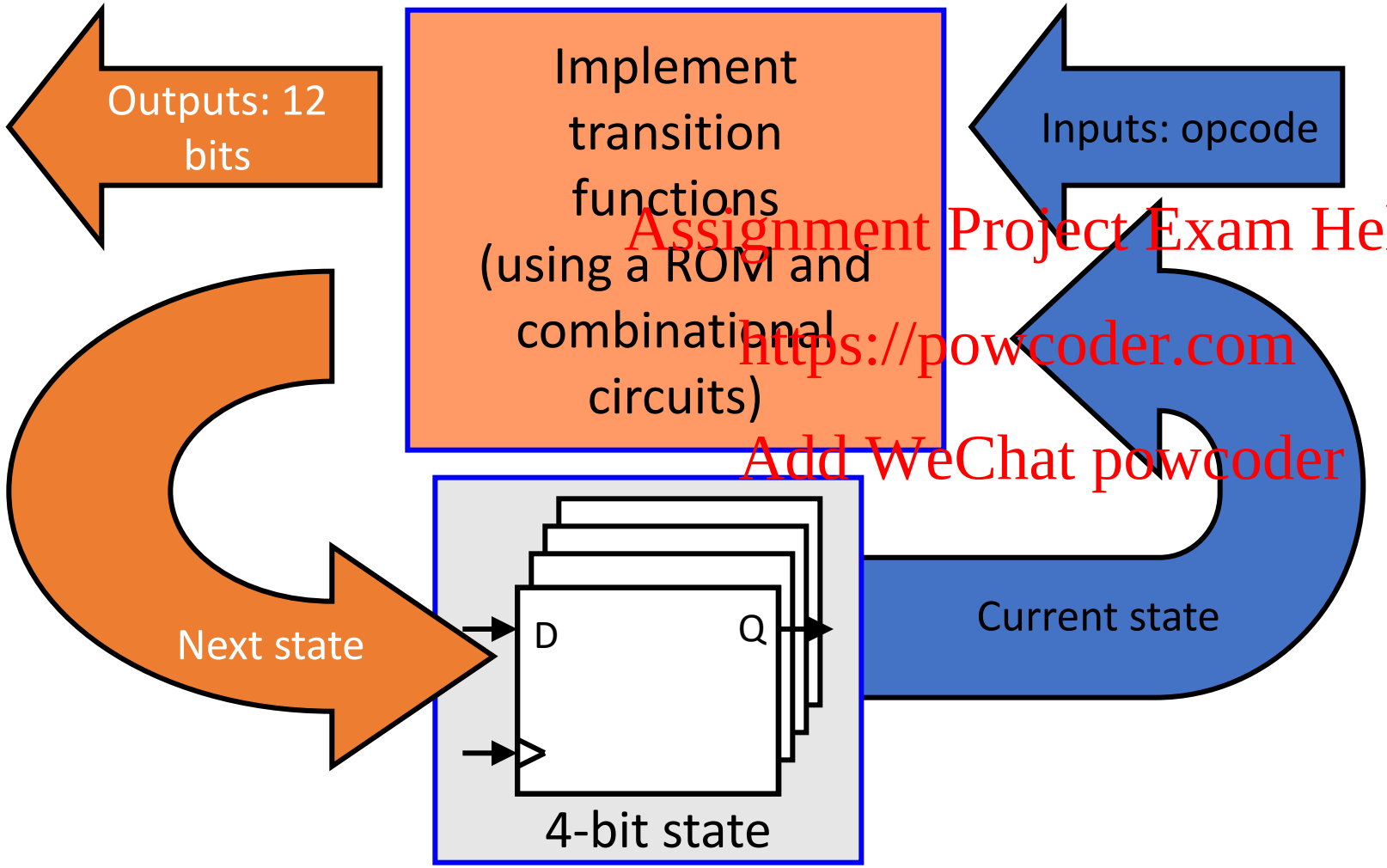
Multi-Cycle

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**Outputs**
Control lines for MUXs, ALU, Enable bits, R/W

Next state

**Inputs**
Opcode

Current state

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# Building the Control ROM

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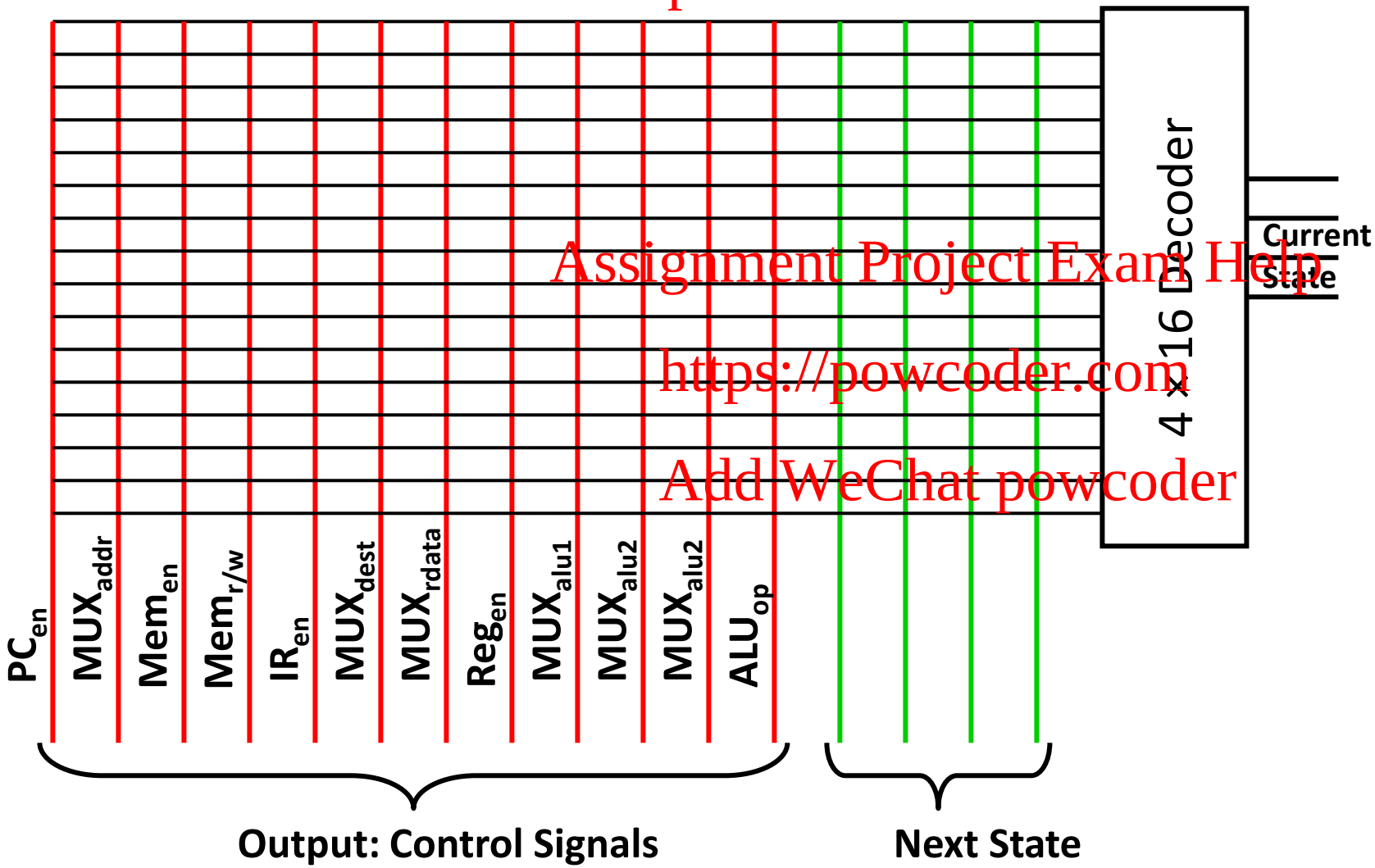


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Multi-Cycle

Decoder Input: What happened to opcode???

Optimization using combinational logic. We will see it later, but opcode will *not* be input to the decoder

First slide of L3_3
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Multi-Cycle

# First Cycle (State 0) Fetch Instruction

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What operations need to be done in the first cycle of executing any instruction?

- Read memory[PC] and store into instruction register.
  - Must select PC in memory address MUX ($MUX_{addr}$ = 0) – *B in diagram*
  - Enable memory operation ($Mem_{en}$ = 1) – *C in diagram*
  - R/W should be (read) ($Mem_{r/w}$ = 0) – *D in diagram*
  - Enable Instruction Register write ($IR_{en}$ = 1) – *H in diagram*
- Calculate PC + 1
  - Send PC to ALU ($MUX_{alu1}$ = 0) – *I in diagram*
  - Send 1 to ALU ($MUX_{alu2}$ = 01) – *J in diagram*
  - Select ALU add operation ($ALU_{op}$ = 0) – *K in diagram*
- $PC_{en}$ = 0; $Reg_{en}$ = 0; $MUX_{dest}$ and $MUX_{rdata}$ = X
  - *A, E, F, G in diagram, respectively*

Next State: Decode Instruction

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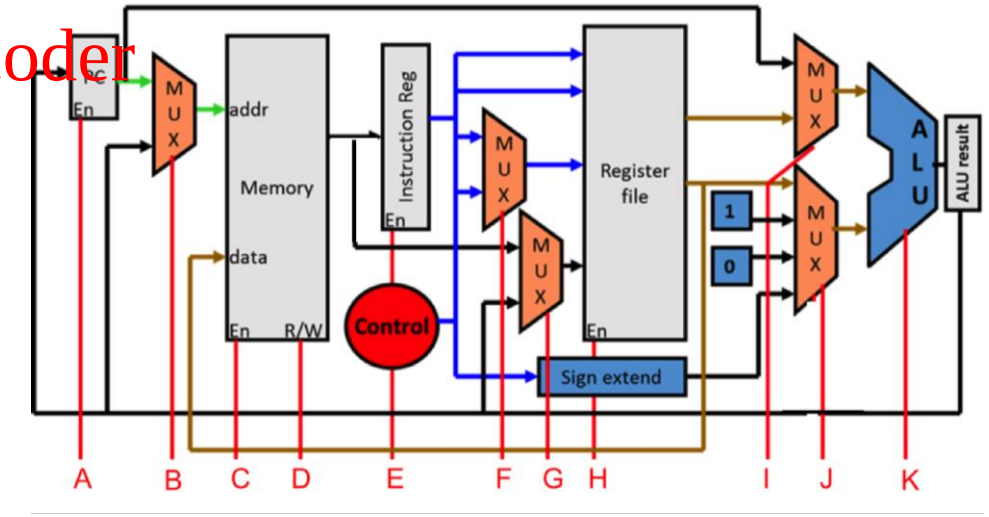

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# First Cycle (State 0) Operation

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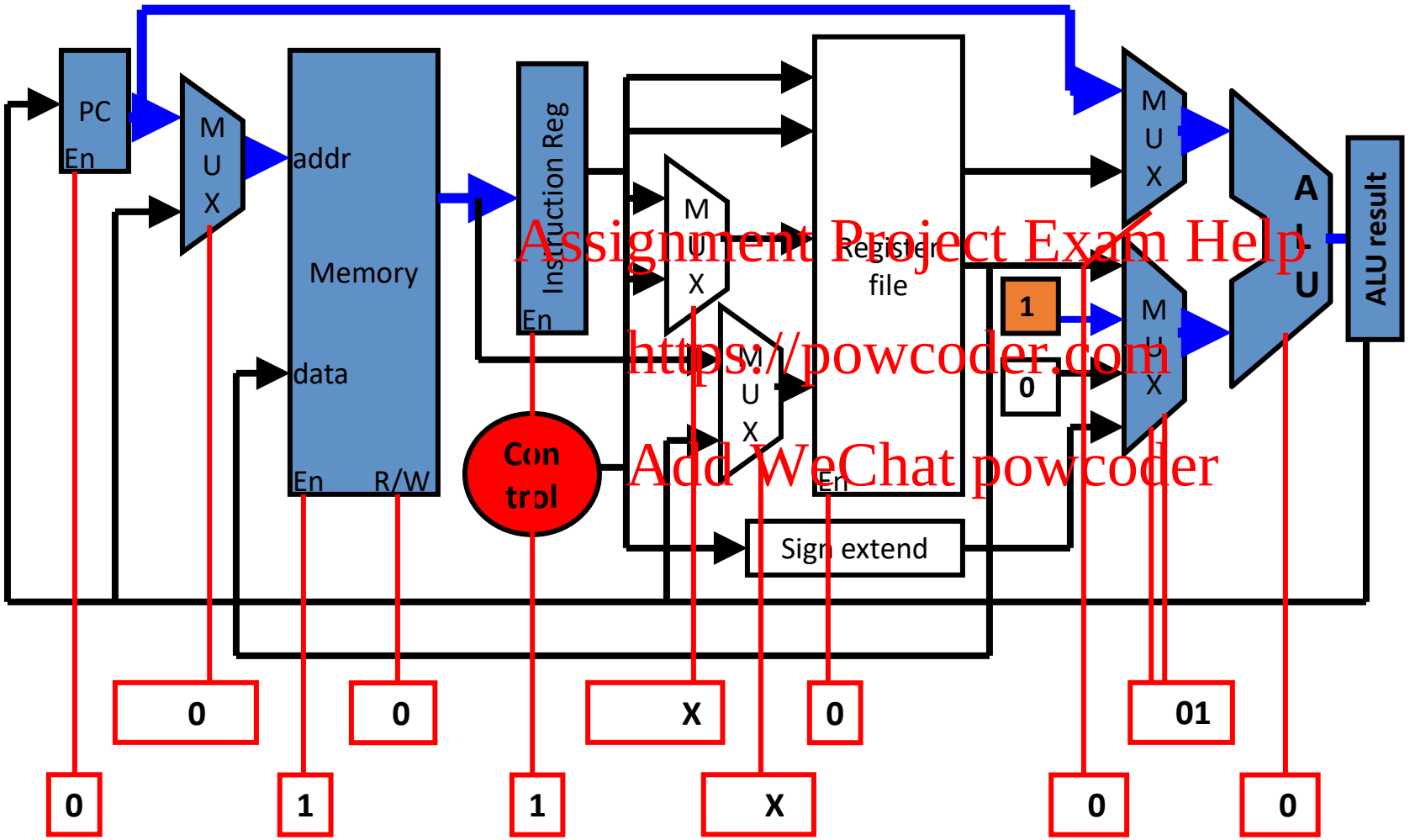
Multi-Cycle

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This is the same for all instructions, i.e., any opcode.
We do not know what the instruction is before decoding.

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# Building the Control ROM – State 0

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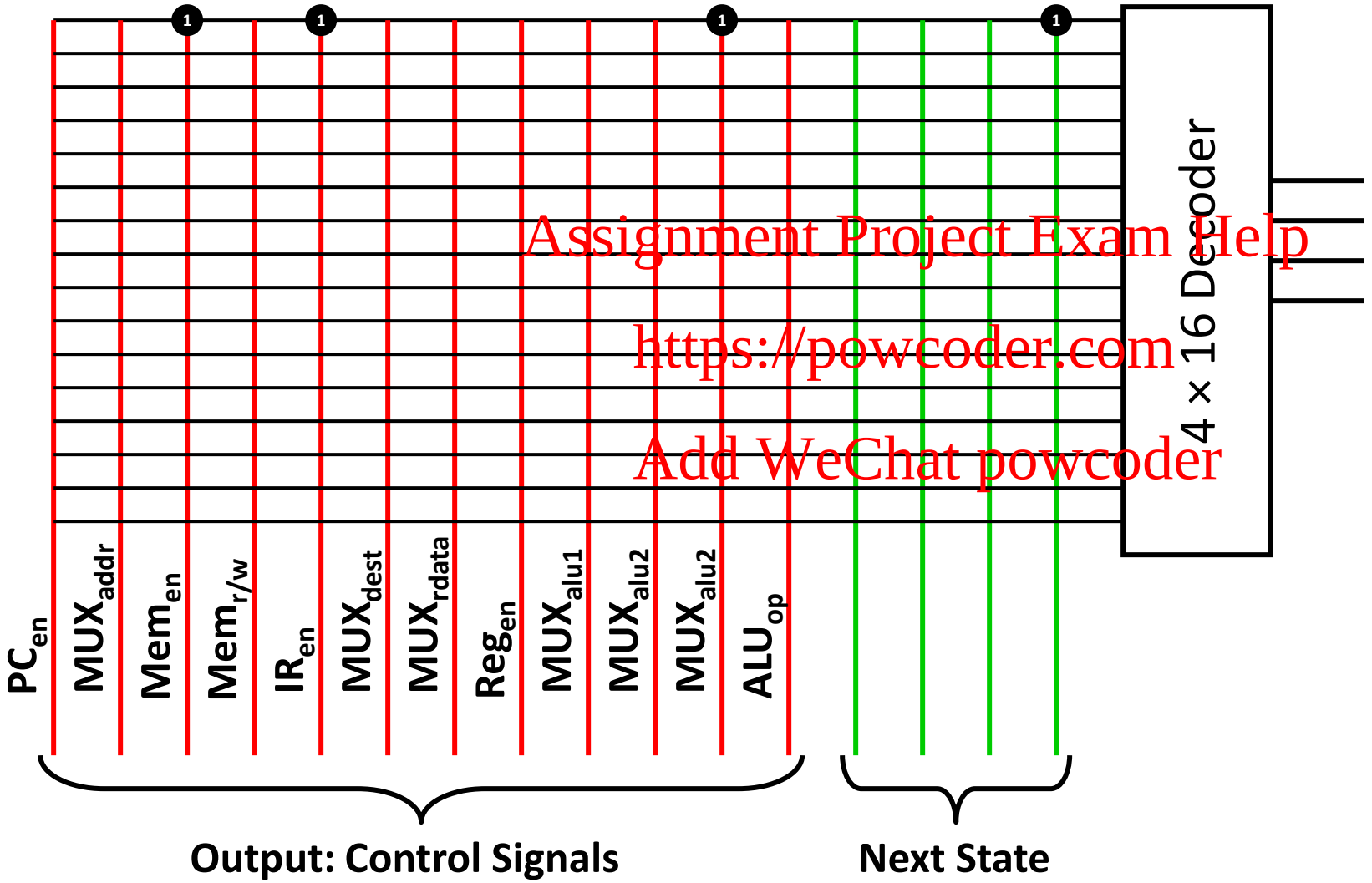
Multi-Cycle

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1 Represents ROM memory for state.

Marks output lines (vertical) that will be 1 when that line in the decoder (horizontal) is selected by the input

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# State 1: Instruction Decode

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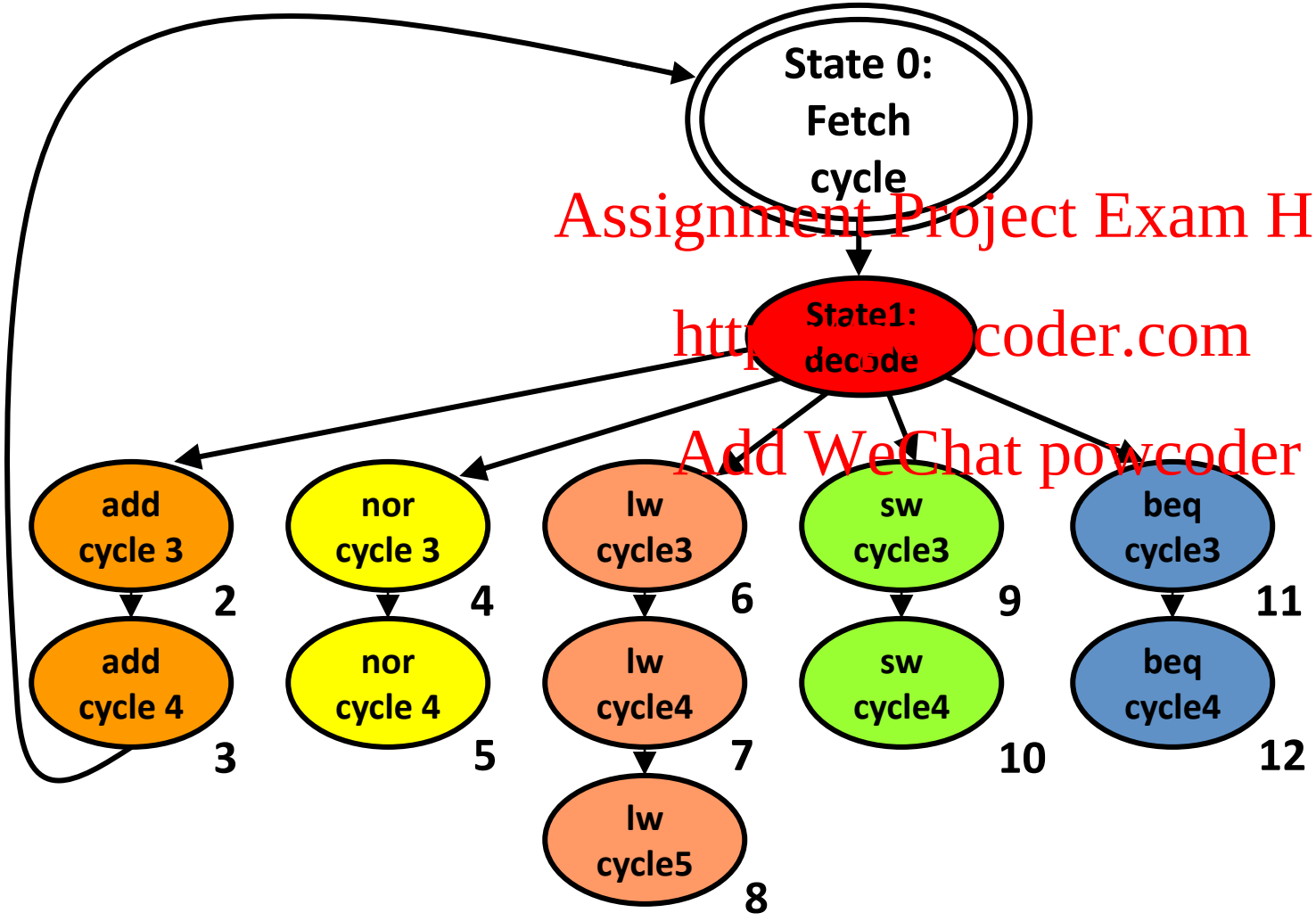


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# State 1: Output Function

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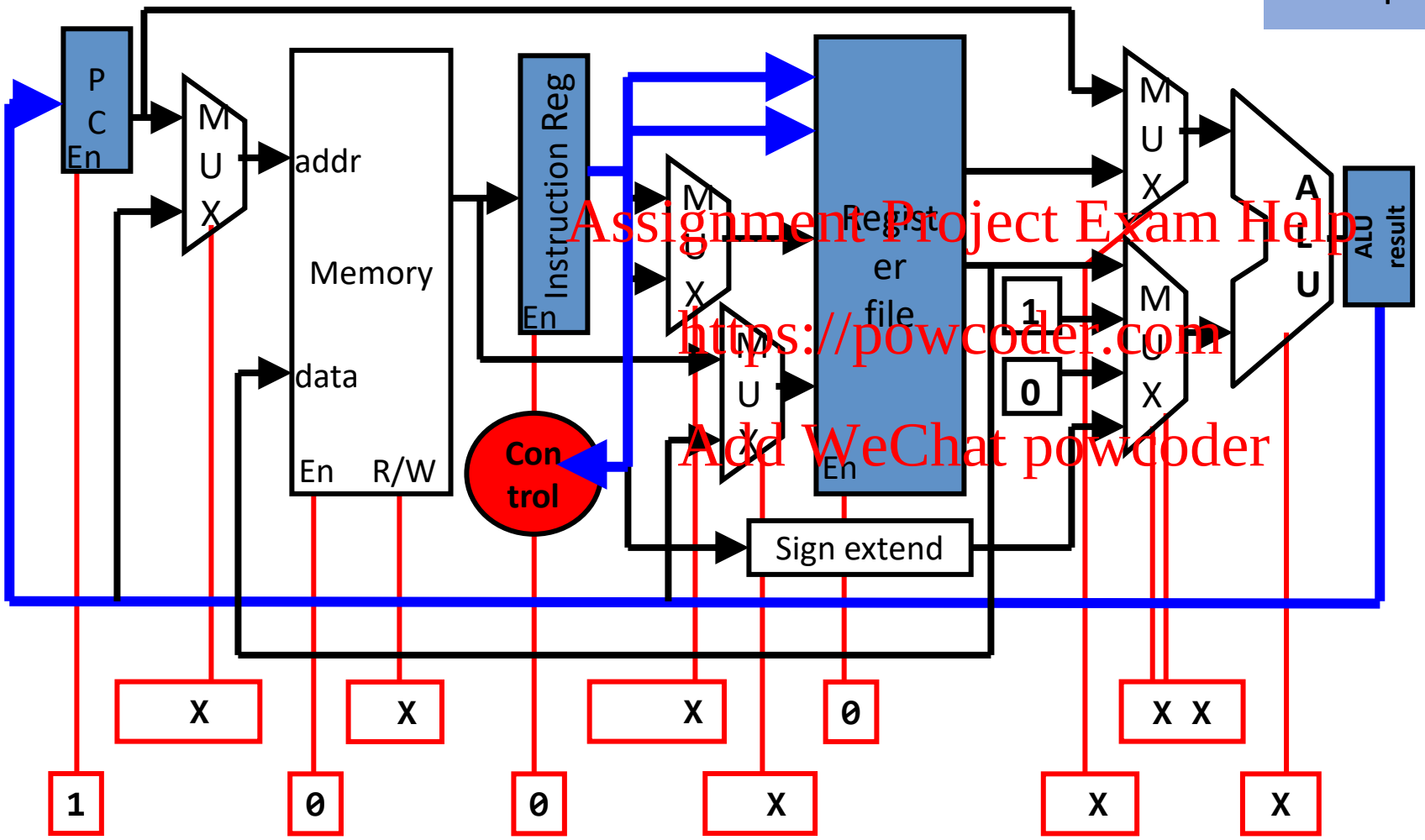
Multi-Cycle

Update PC
Read registers (regA and regB)
Use opcode to determine next state

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# Building the Control ROM – State 1

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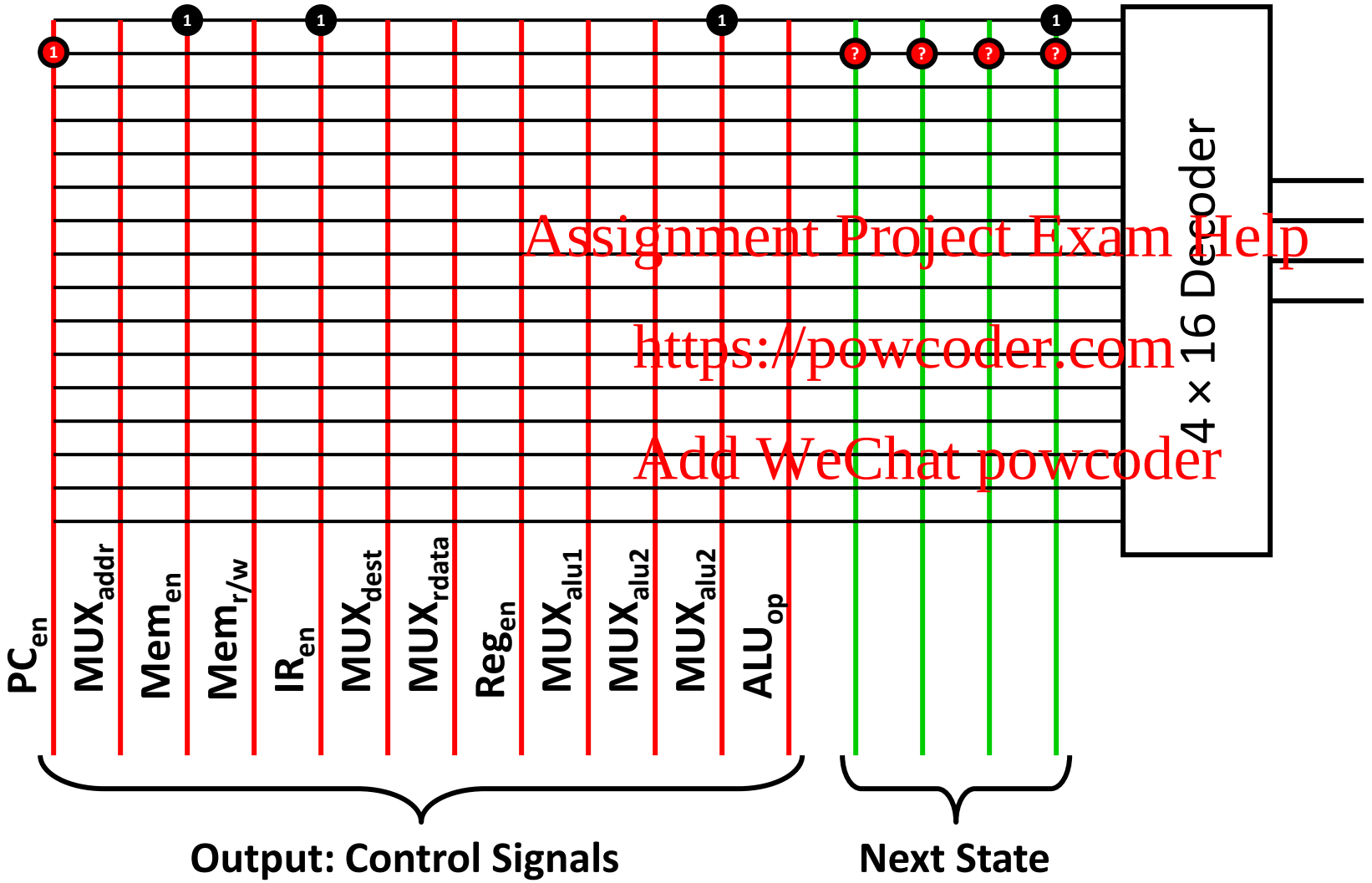
Multi-Cycle

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? How will this be set?

We will revisit this later…

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# State 2: Add Cycle 3

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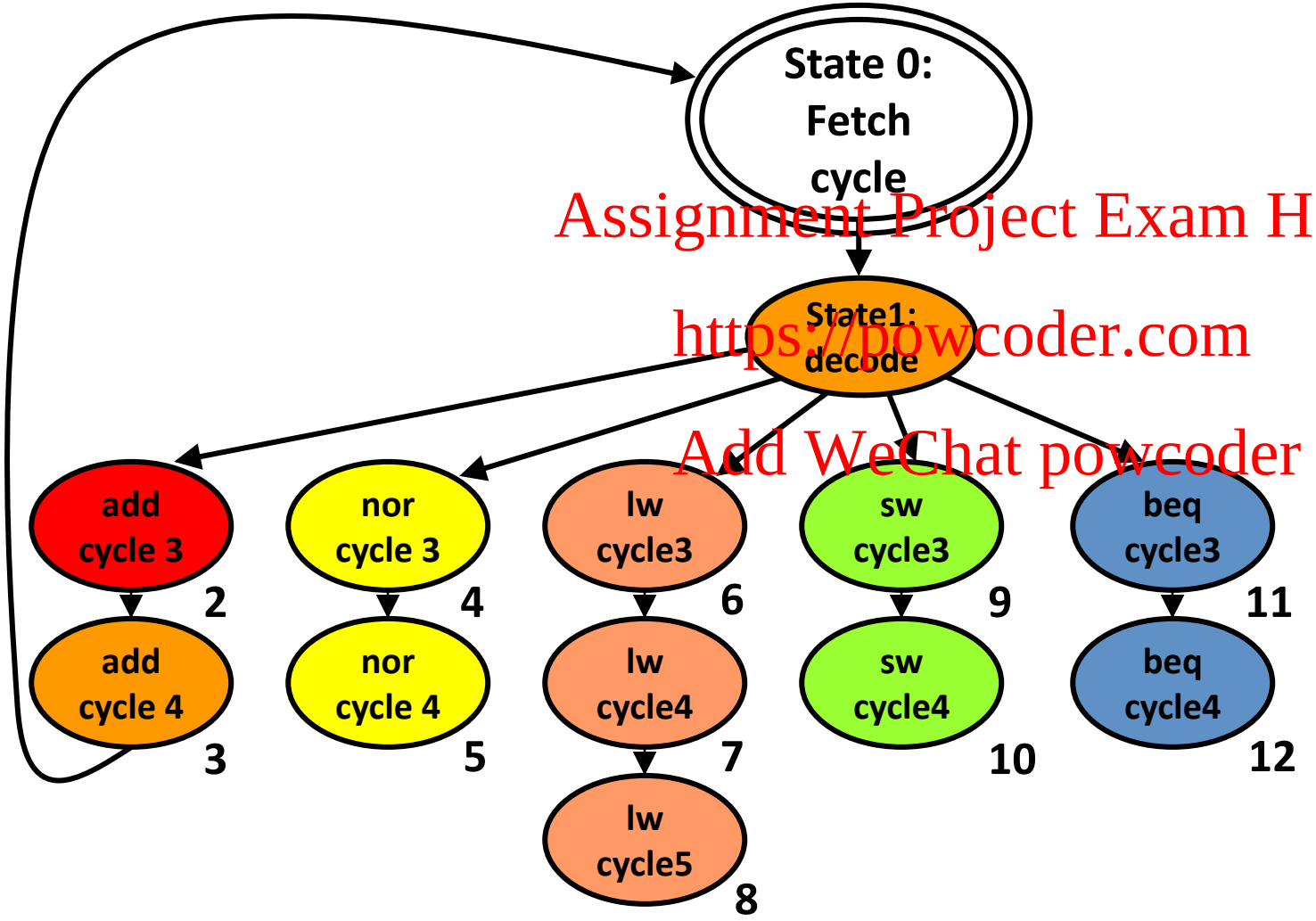


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# State 2: Add Cycle 3 Operation

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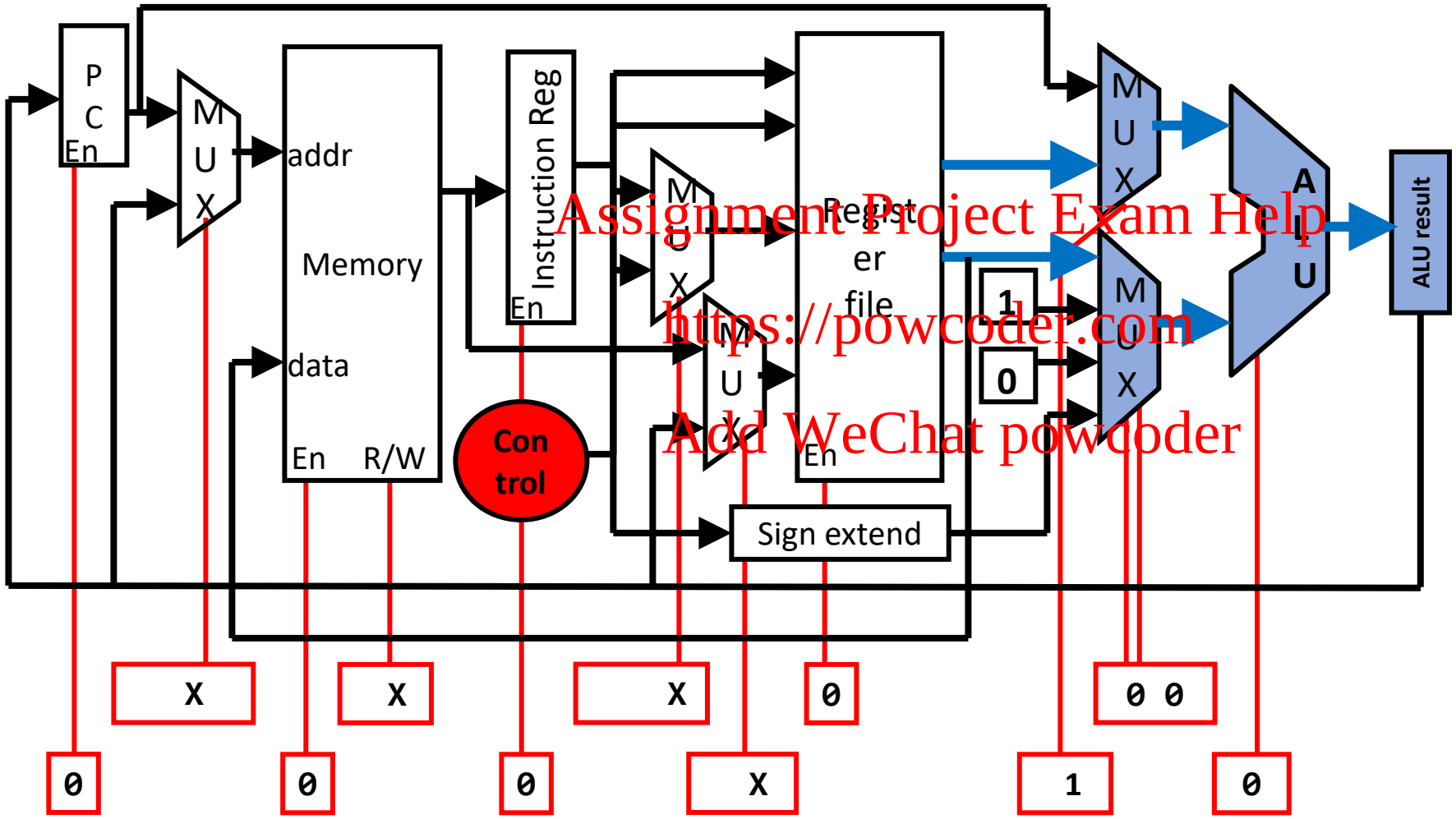
Multi-Cycle

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Send control signals to MUX to select values of regA and regB and control signal to ALU to add

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# Building the Control ROM – State 2

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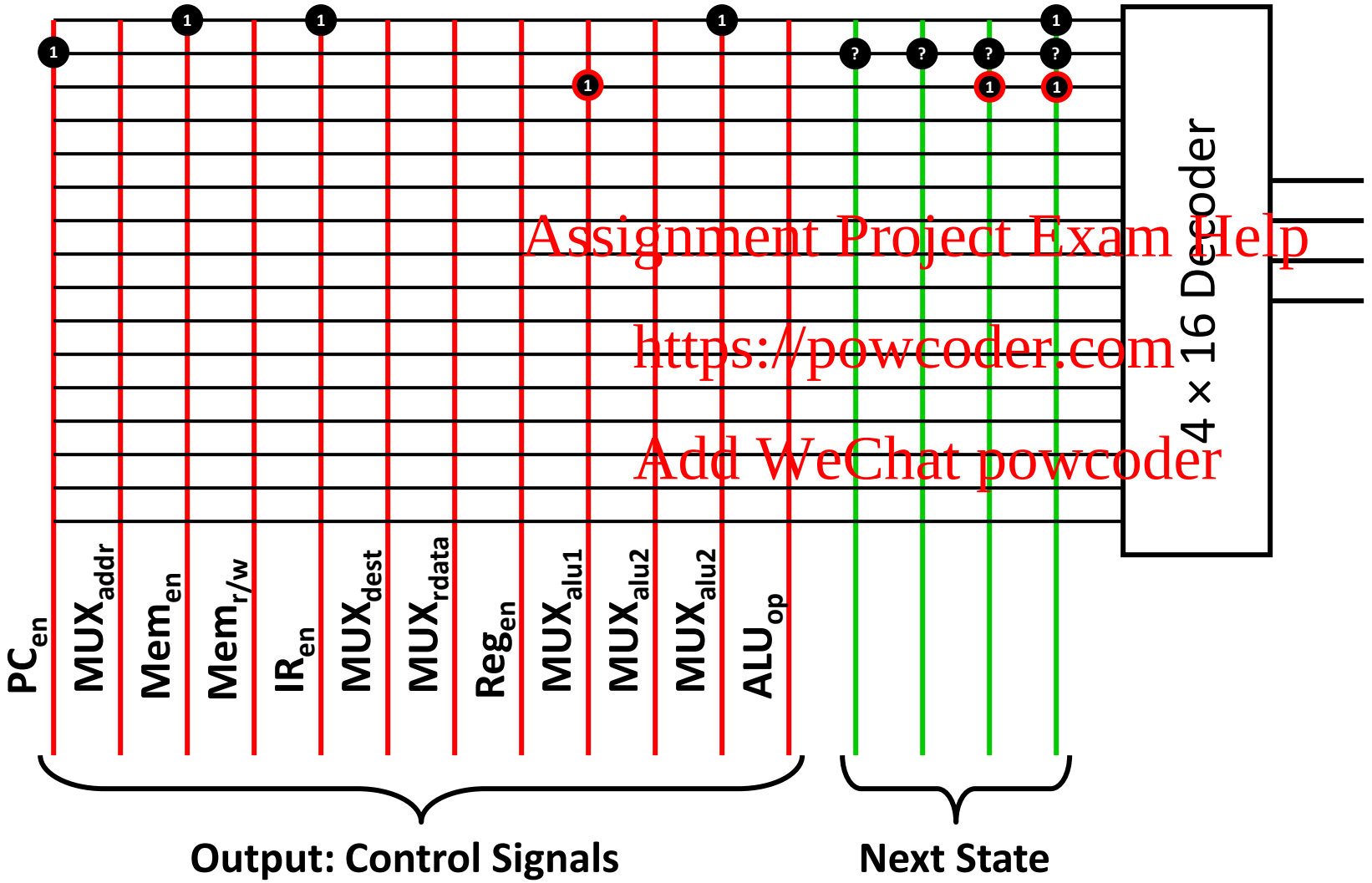
Multi-Cycle

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? How will this be set?

We will revisit this later…

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# State 3: Add Cycle 4

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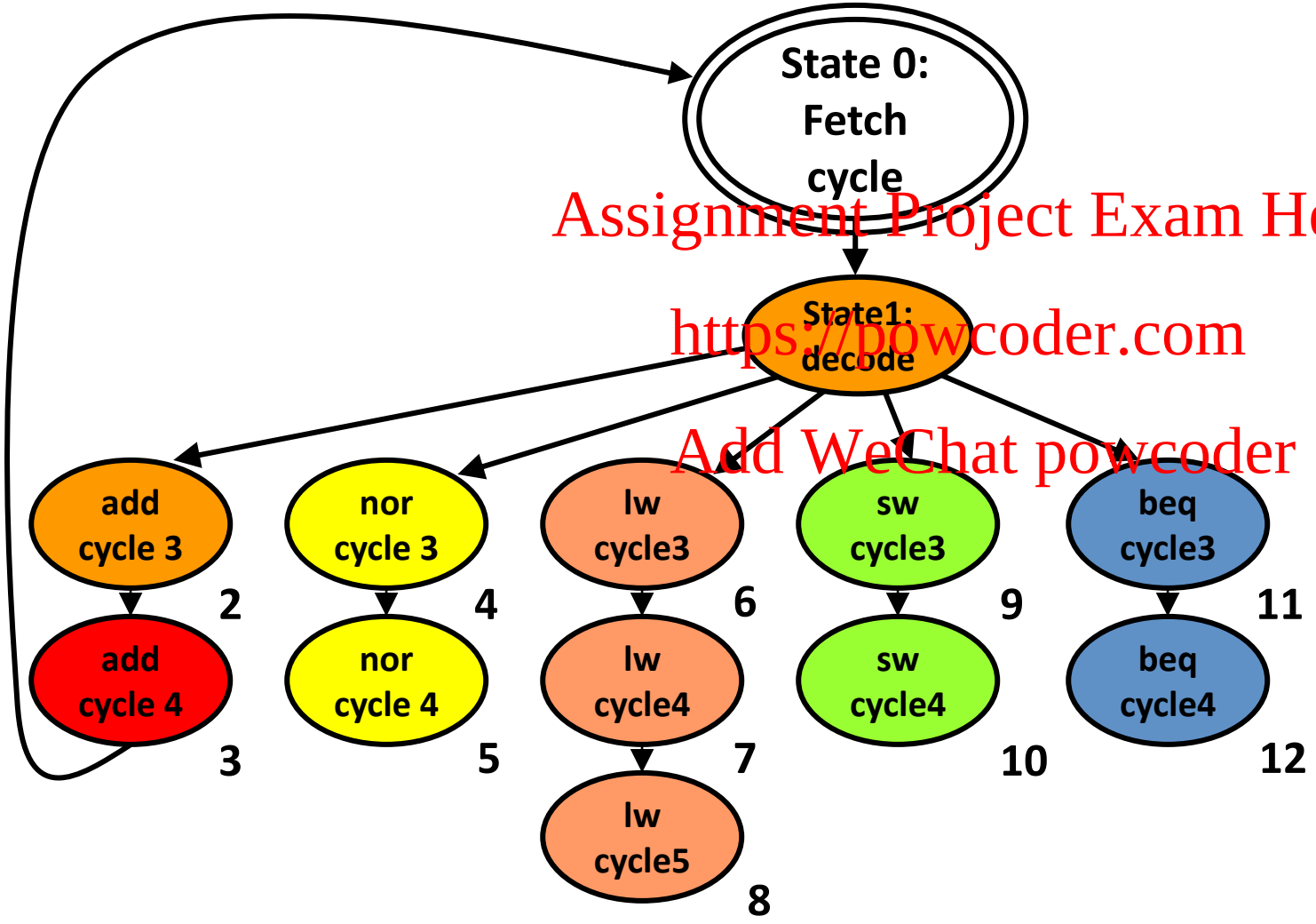


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# State 3: Add Cycle 4 Operation

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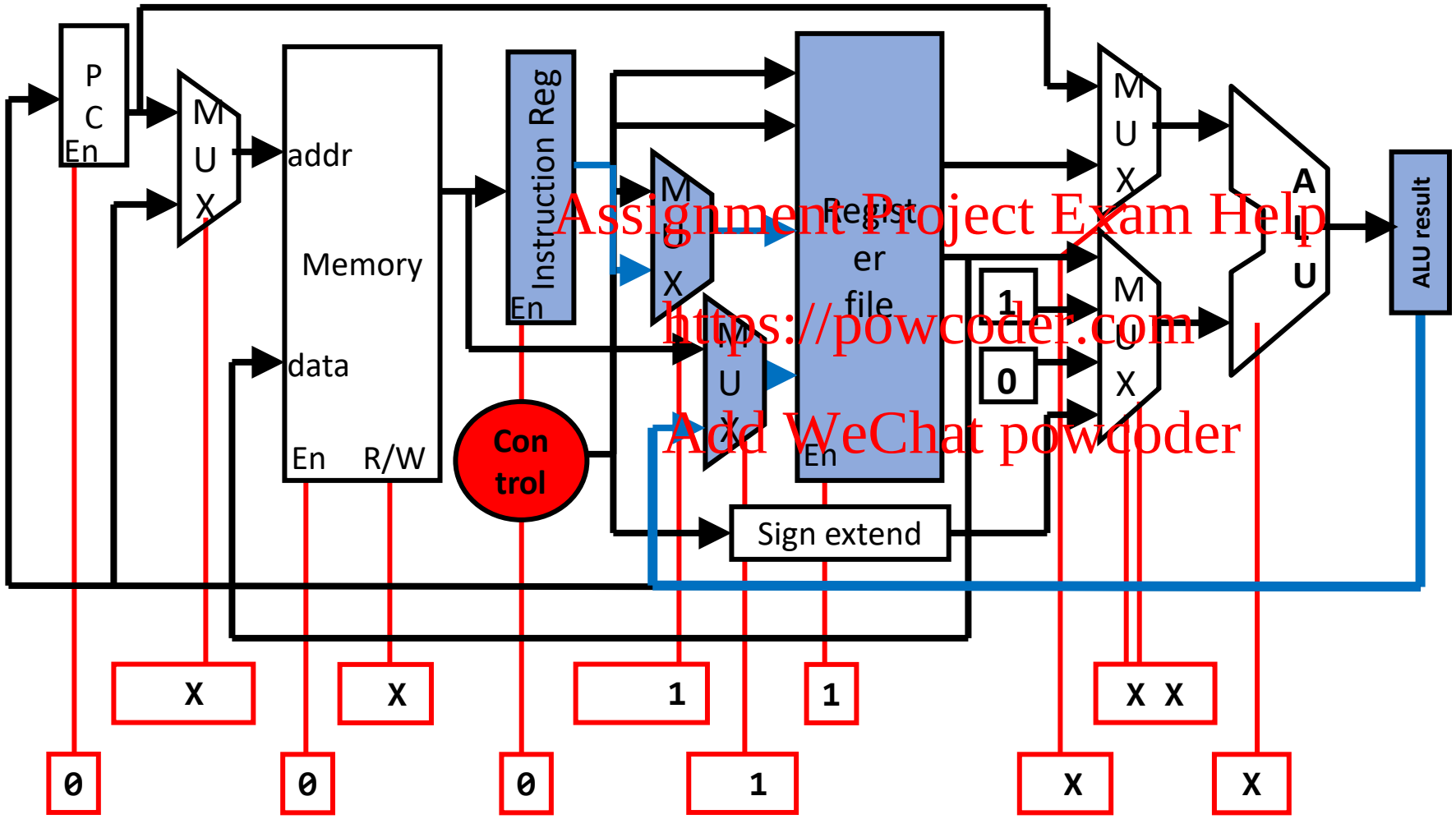
Multi-Cycle

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Send control signal to address MUX to select dest and to data MUX to select ALU output, then send write enable to register file.

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# Building the Control ROM – State 3

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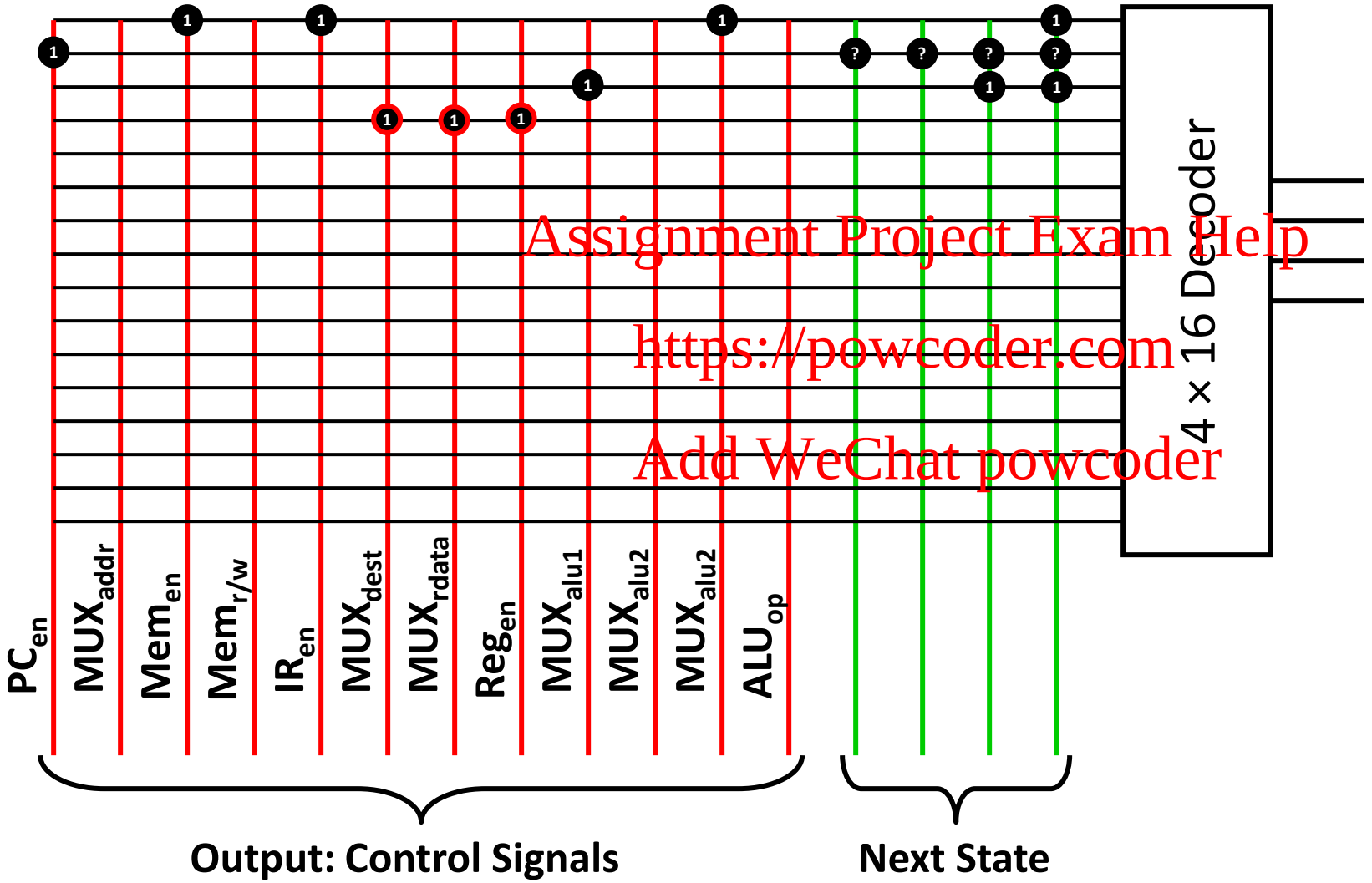
Multi-Cycle

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? How will this be set?

We will revisit this later…

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# Return to State 0

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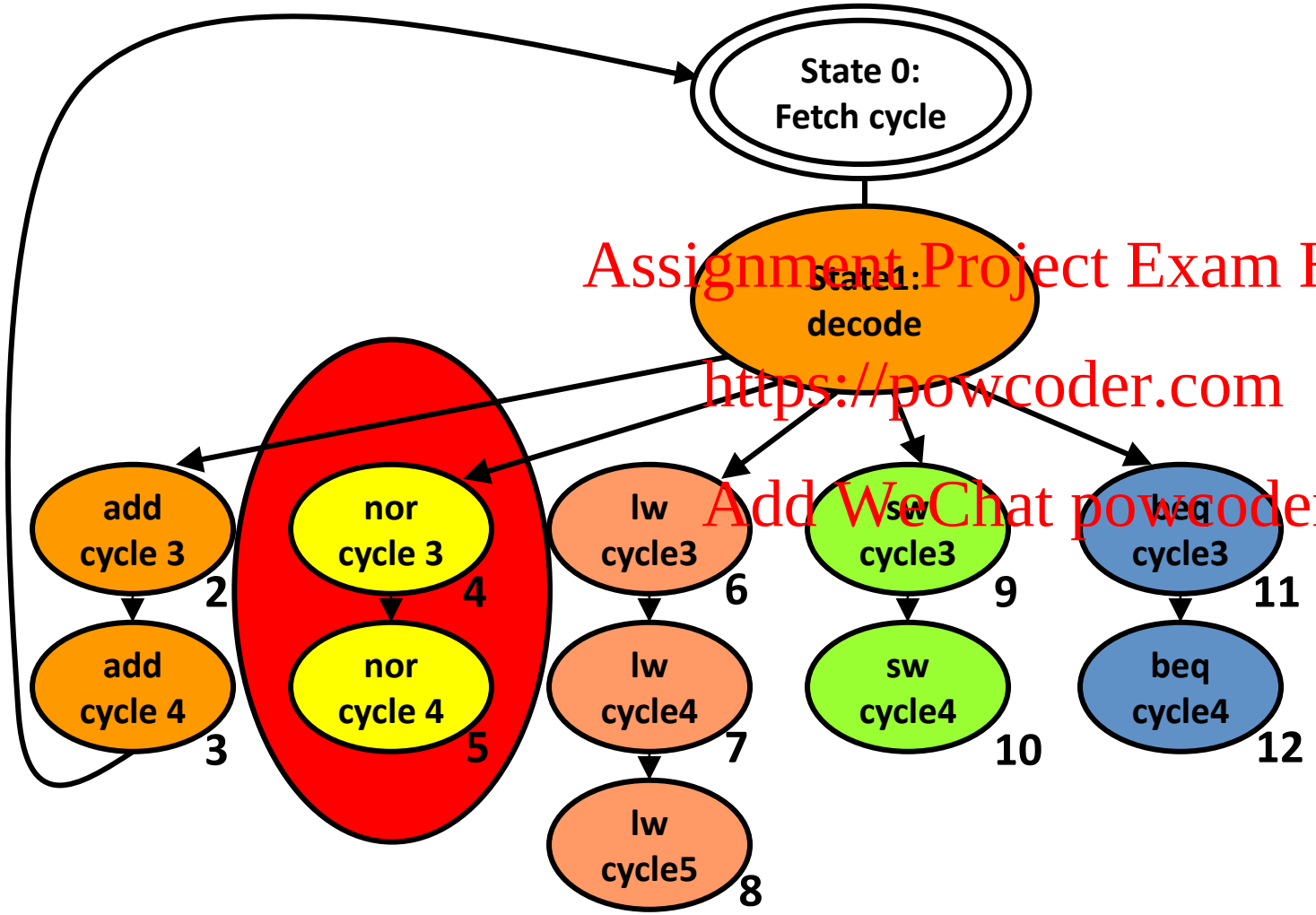
Multi-Cycle

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Fetch cycle to execute next instruction

What about nor?

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# Building the Control ROM – nor (States 4,5)

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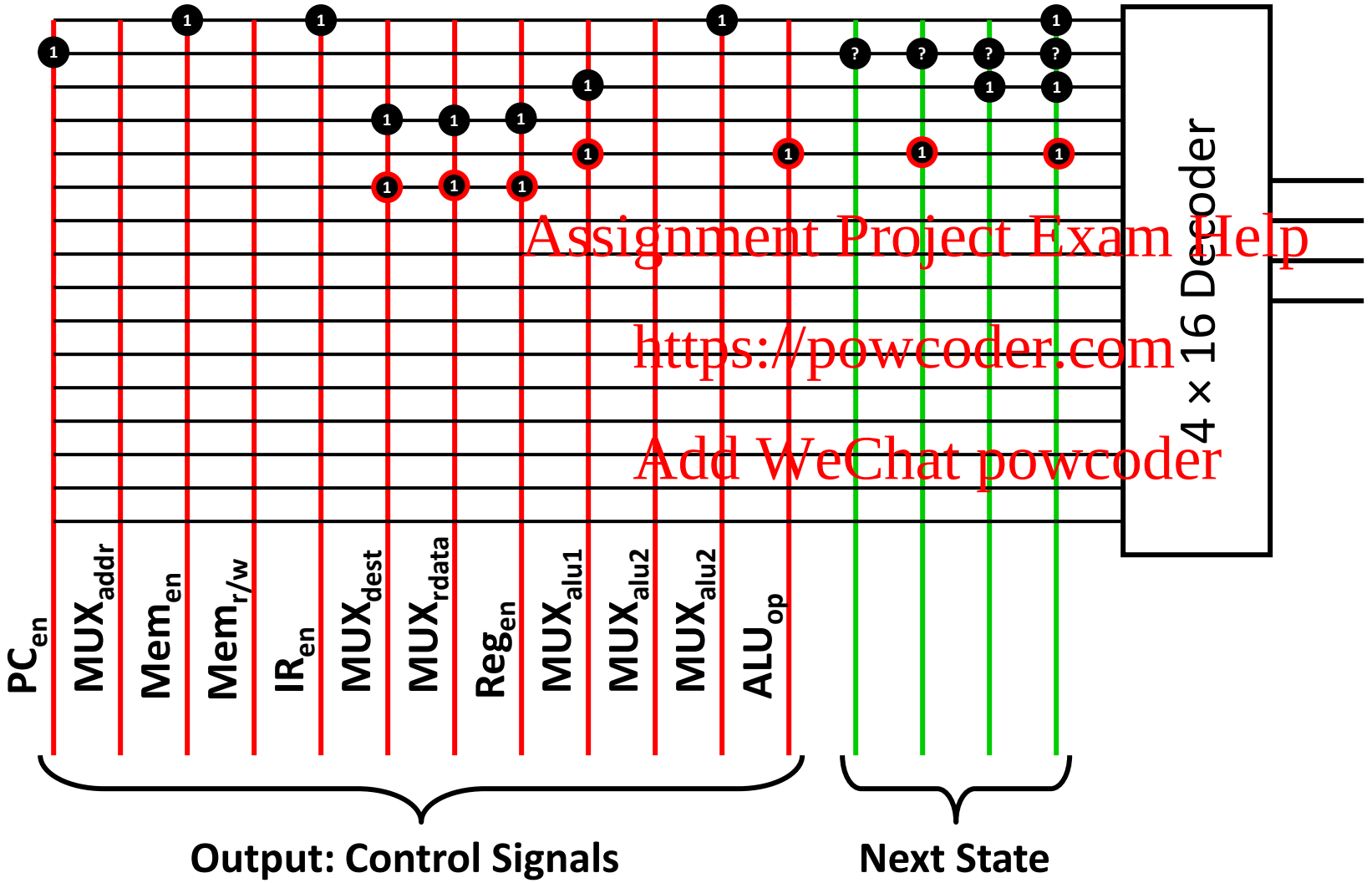
Multi-Cycle

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# What About the Transition from State 1?

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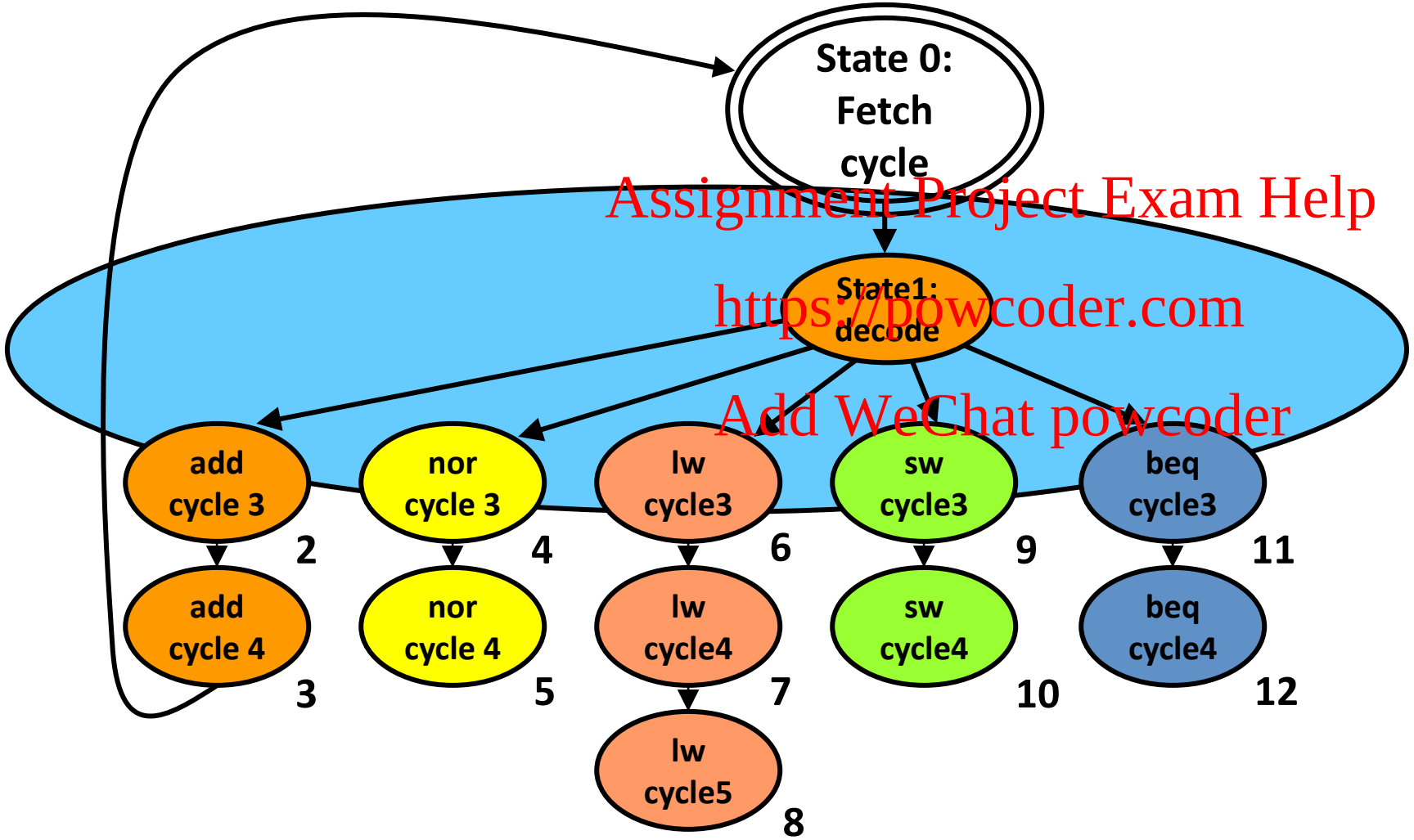
Multi-Cycle

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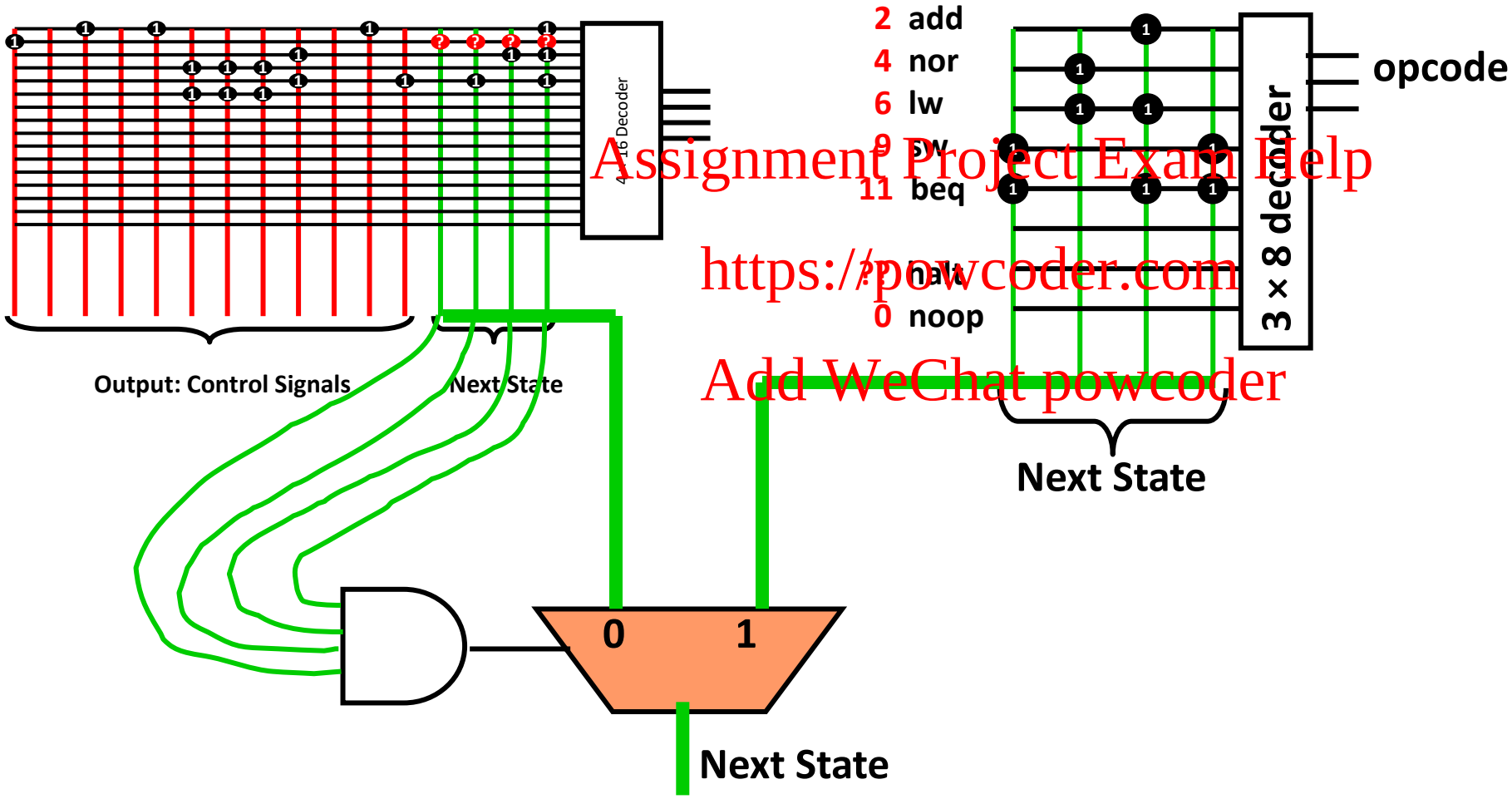


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# Building the Control ROM

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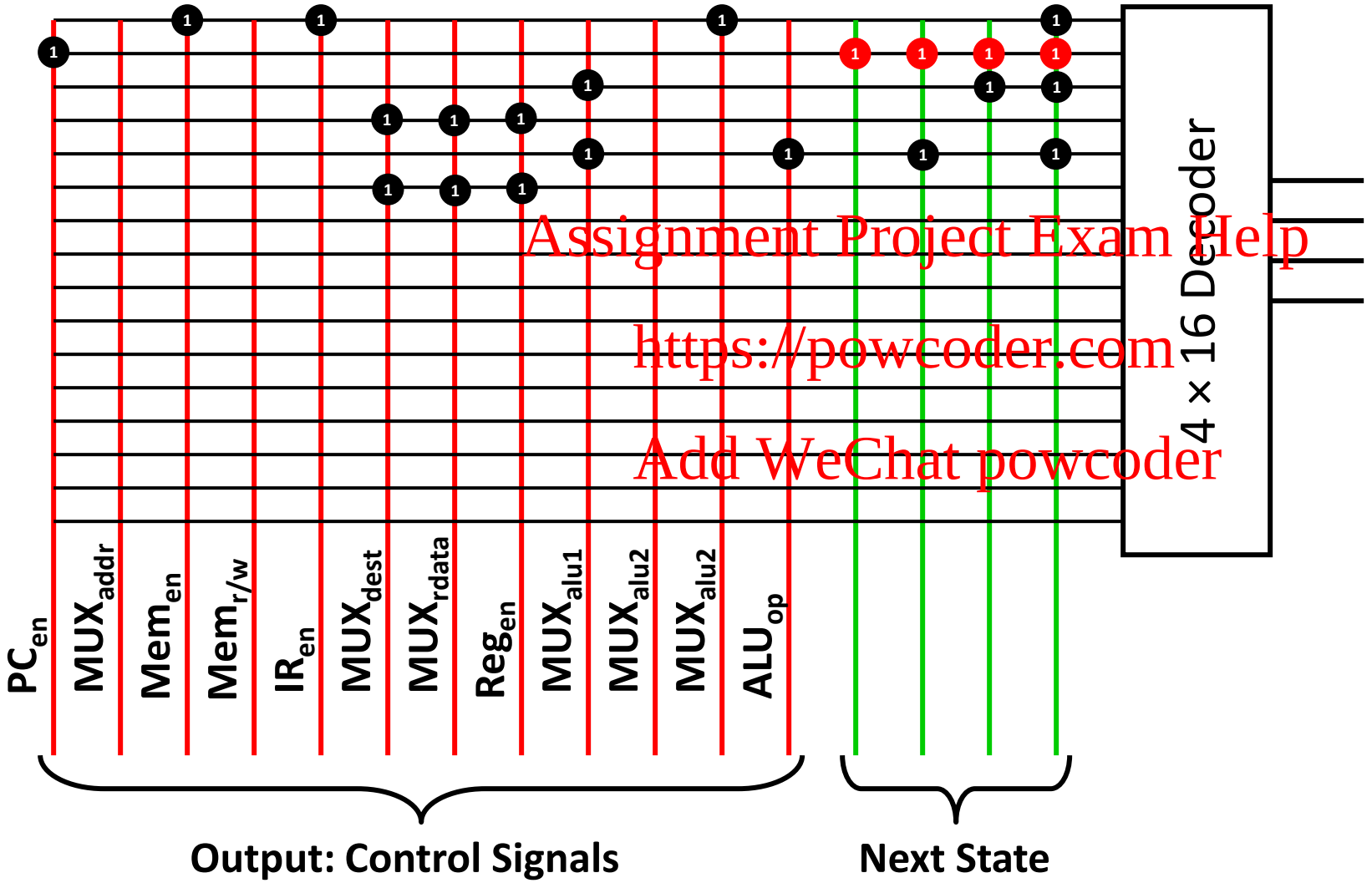
Multi-Cycle

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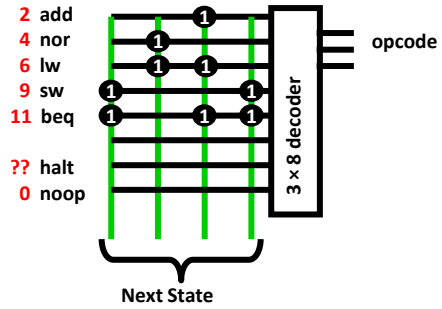
1 1111 state means "use the opcode to decide the next state"



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# FSM – Multi-Cycle Clock

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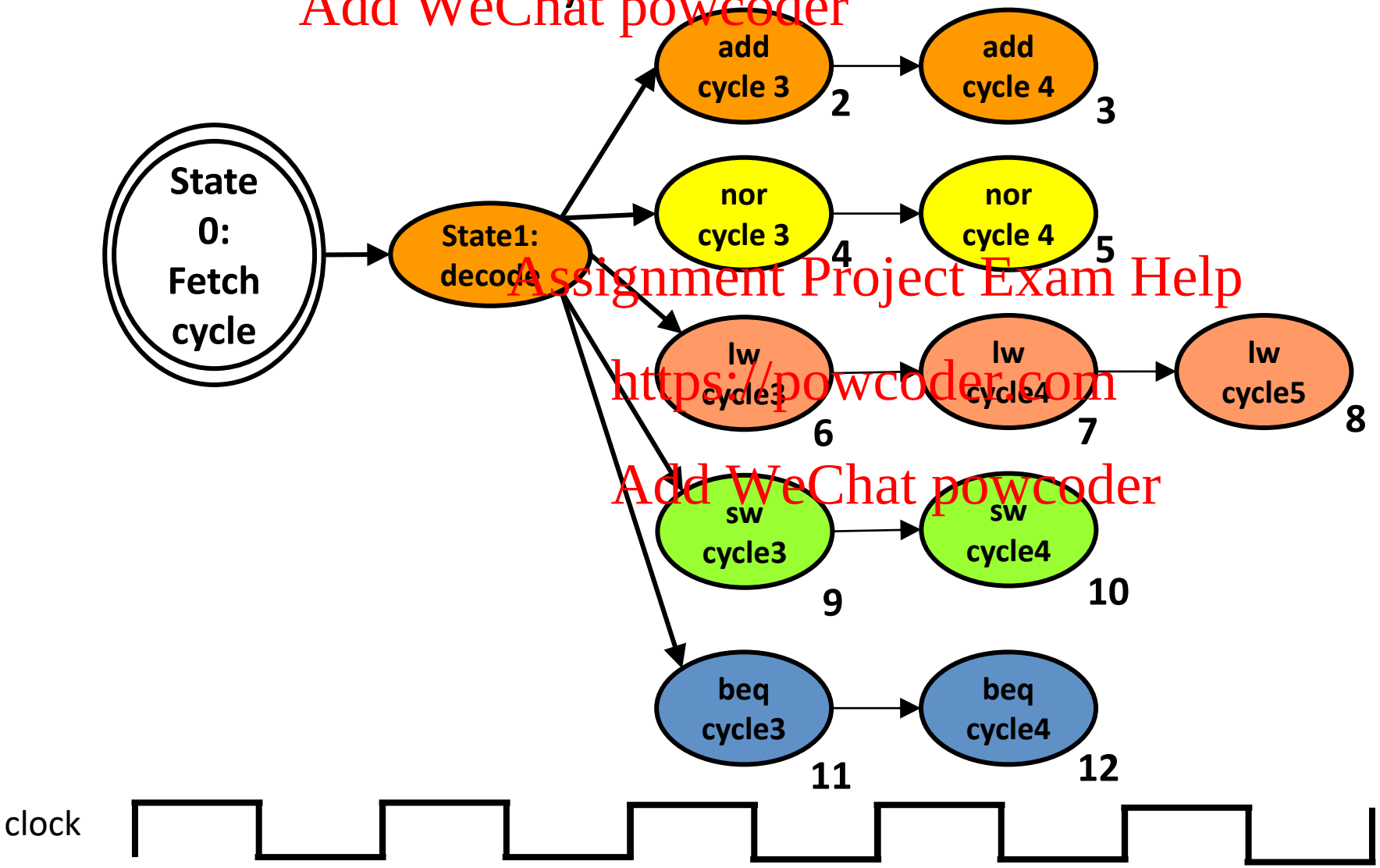
Multi-Cycle

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# State 6: LW Cycle 3

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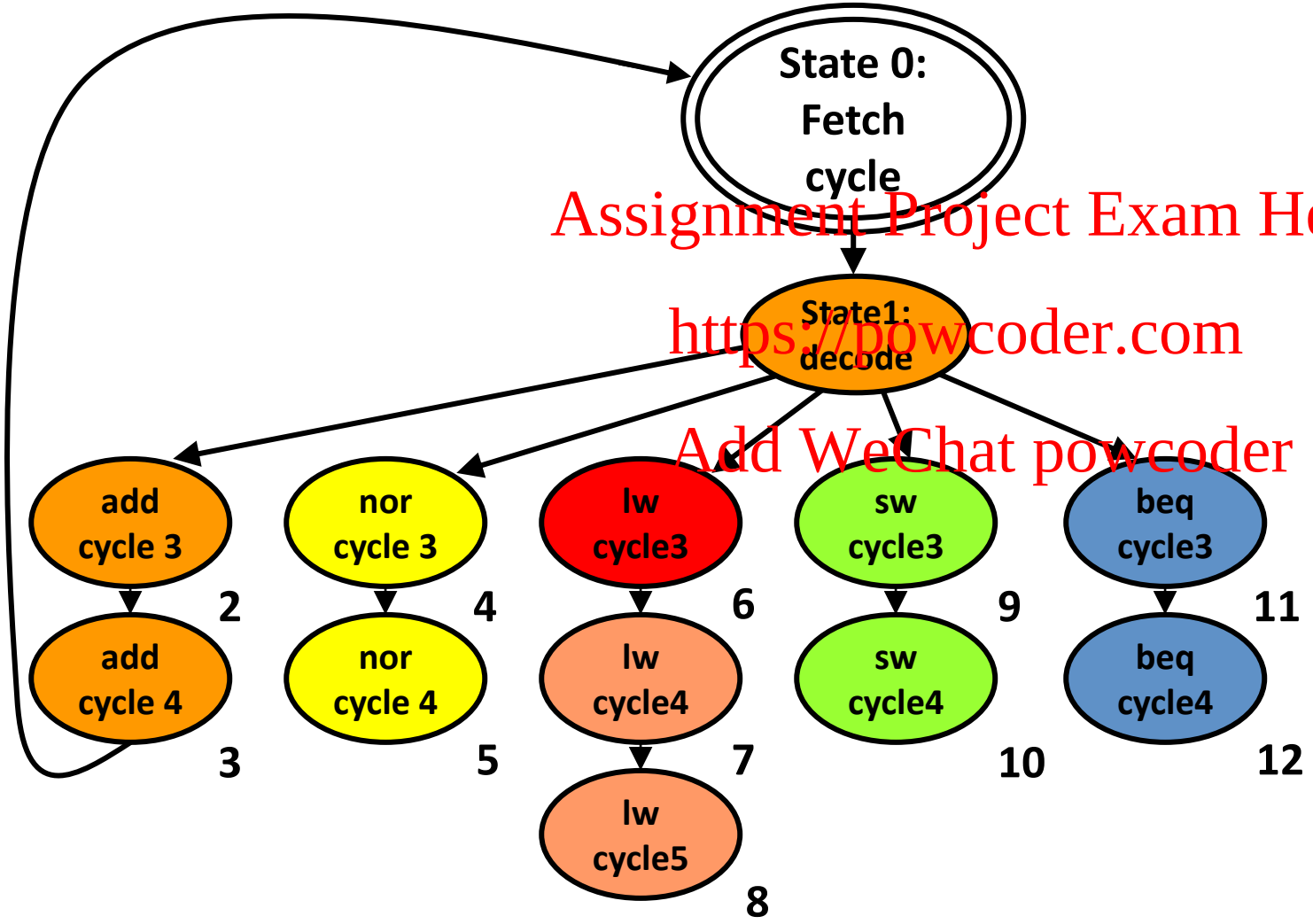


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# State 6: LW Cycle 3 Operation

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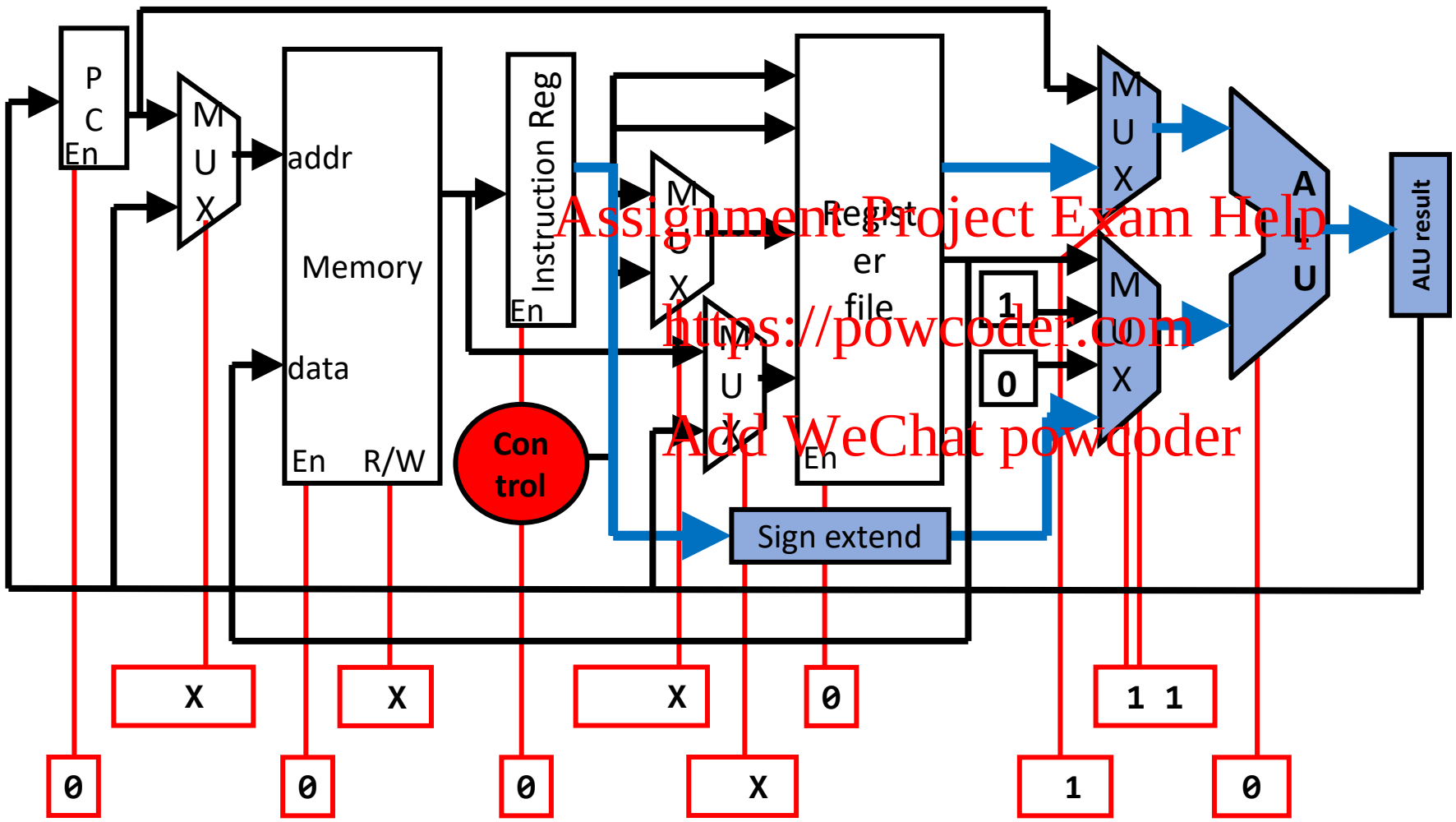
Multi-Cycle

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Calculate address for memory reference

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# Building the Control ROM – State 6 `lw`

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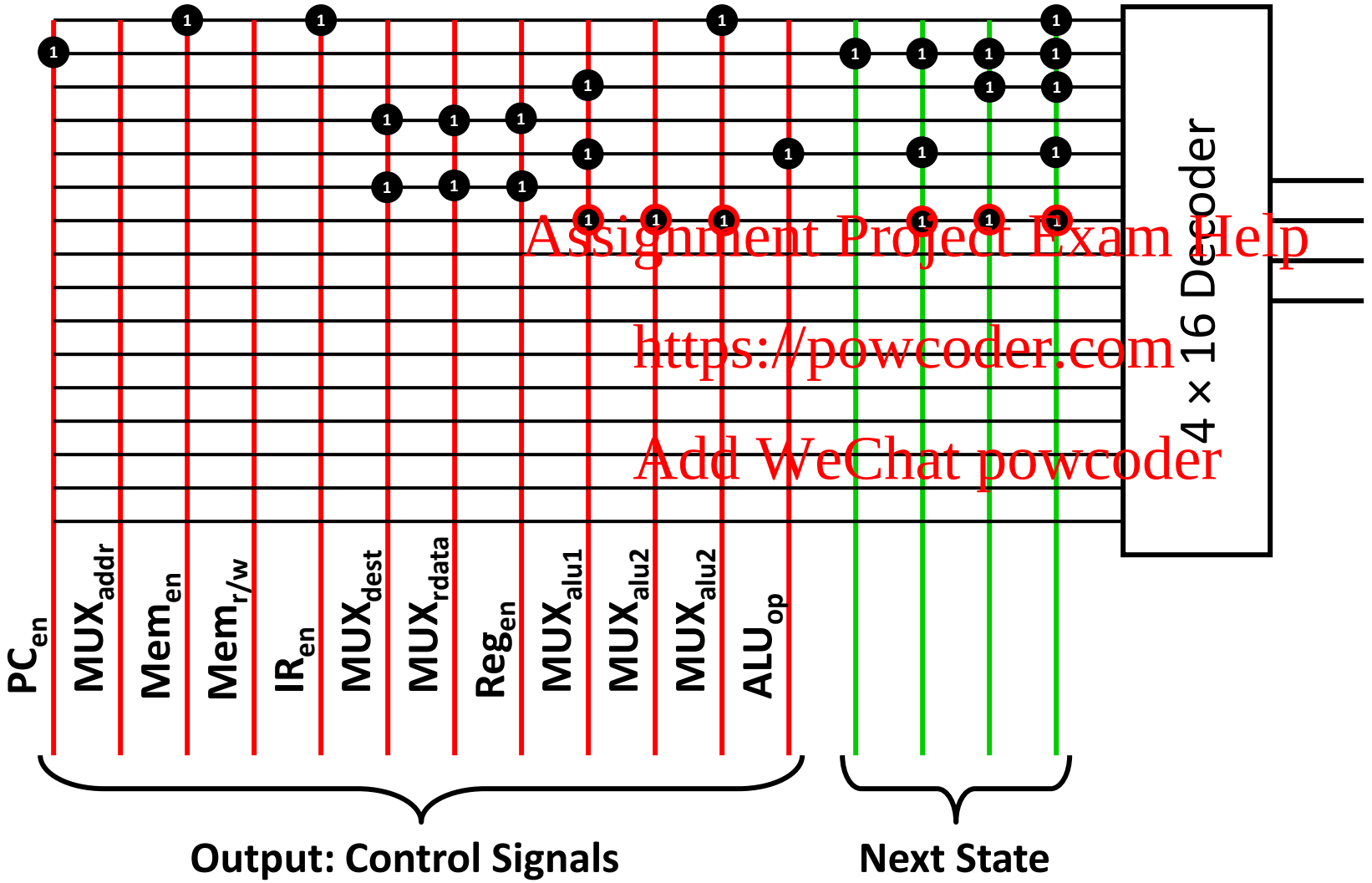
Multi-Cycle

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# State 7: LW Cycle 4 Operation

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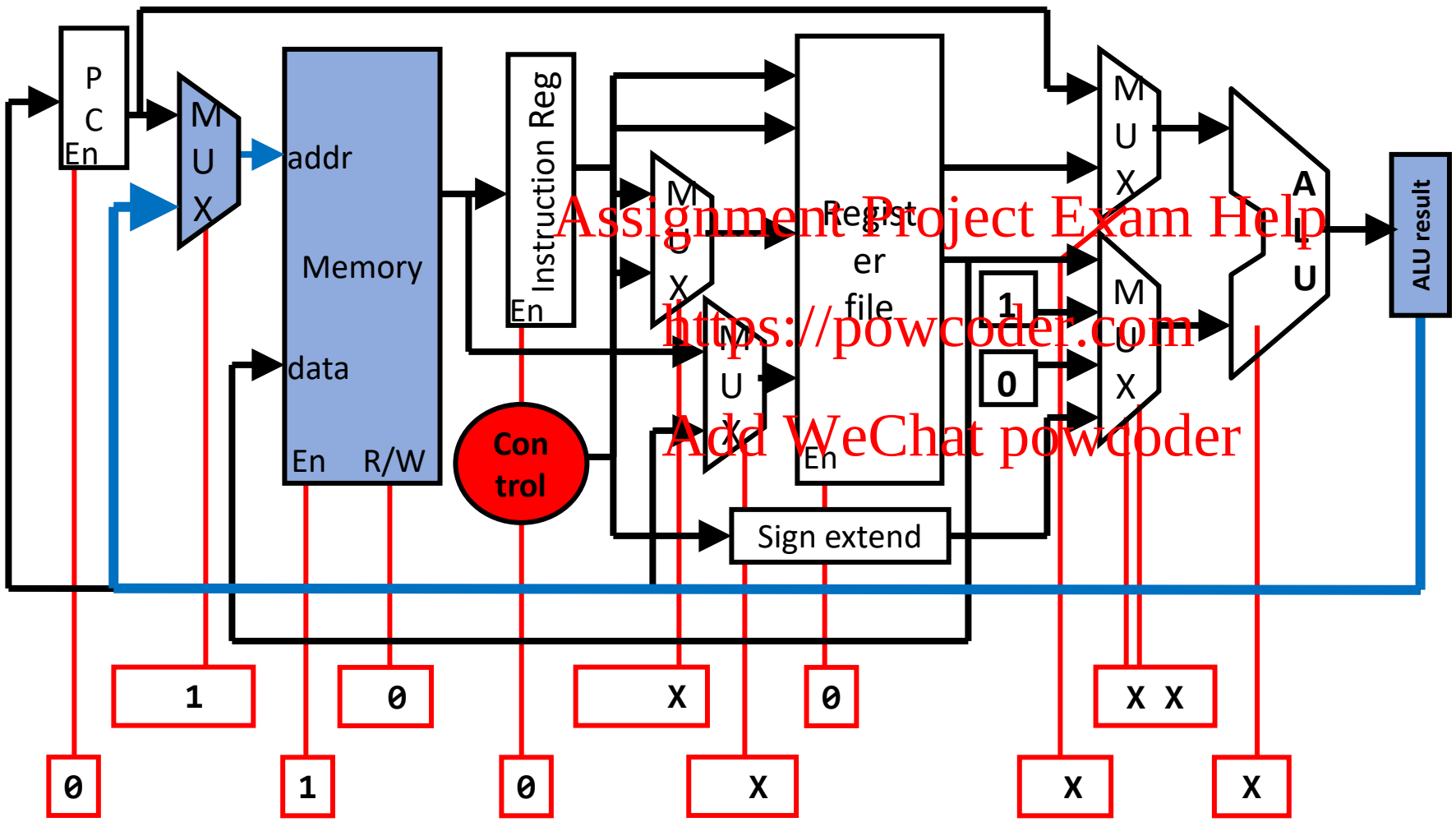
Multi-Cycle

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Read memory location

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# Building the Control ROM – State 7 `lw`

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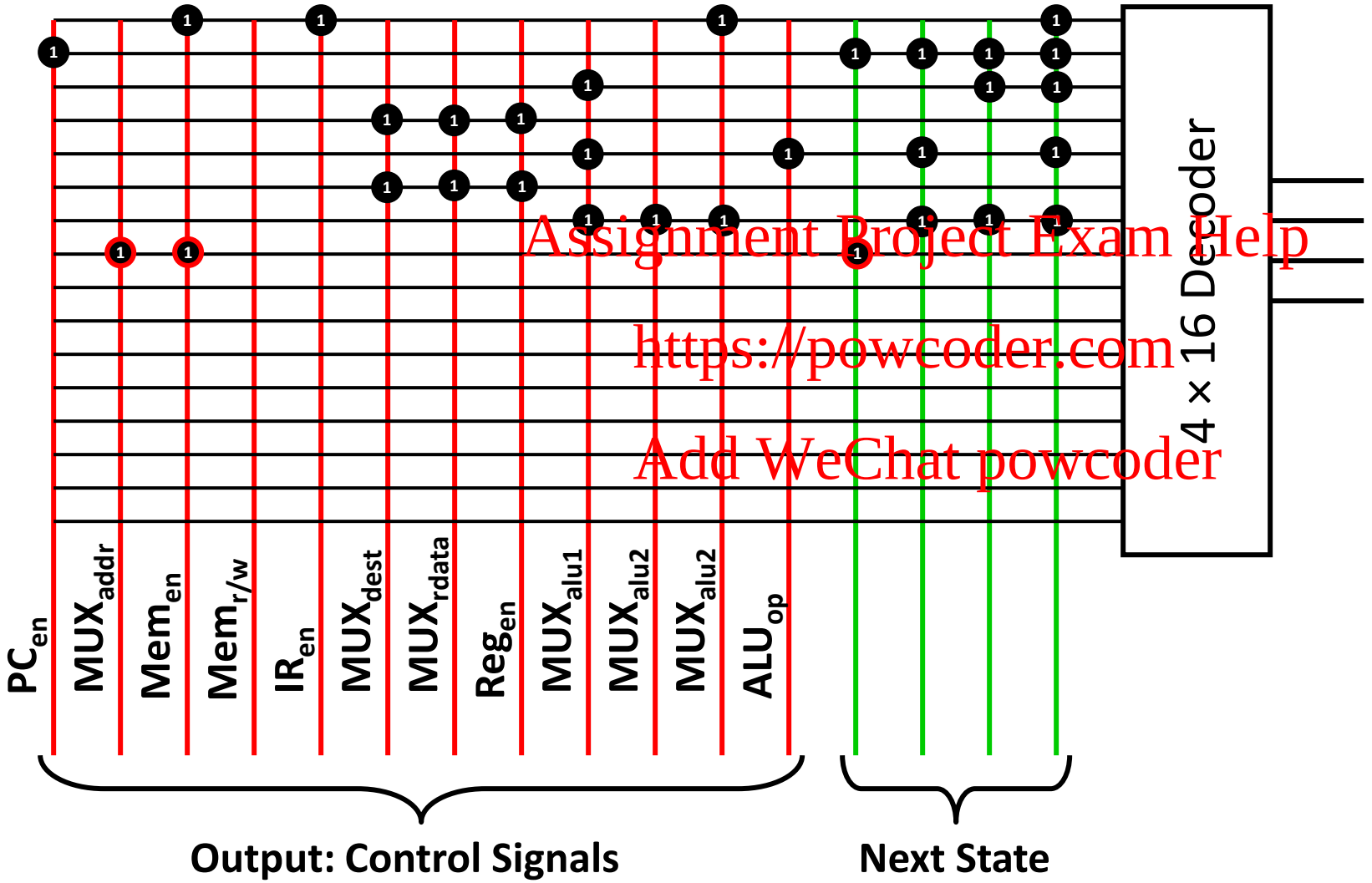
Multi-Cycle

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# State 8: LW Cycle 5 Operation

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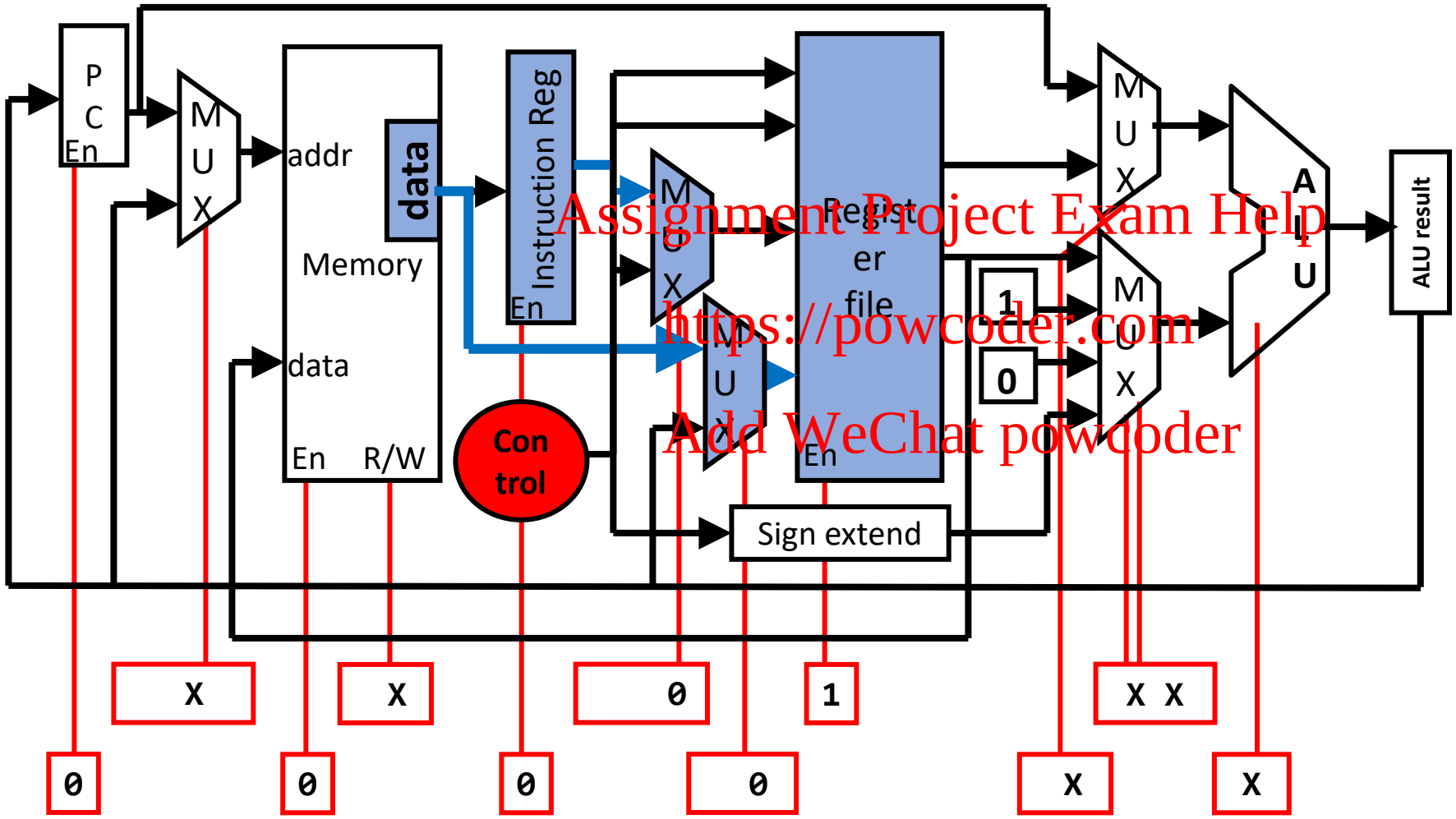
Multi-Cycle

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Write memory value to register file

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# Building the Control ROM – State 8 `lw`

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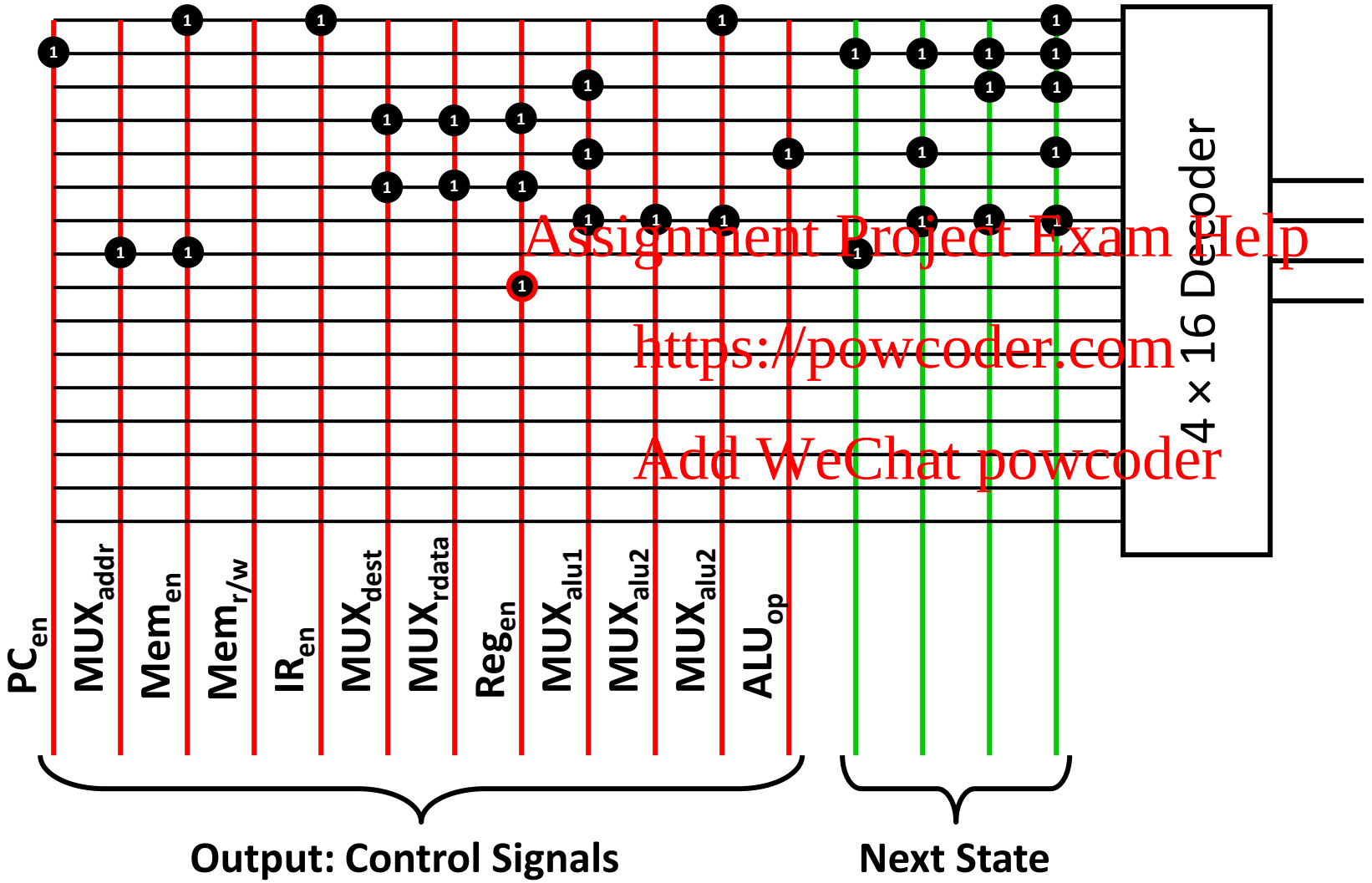
Multi-Cycle

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# Return to State 0

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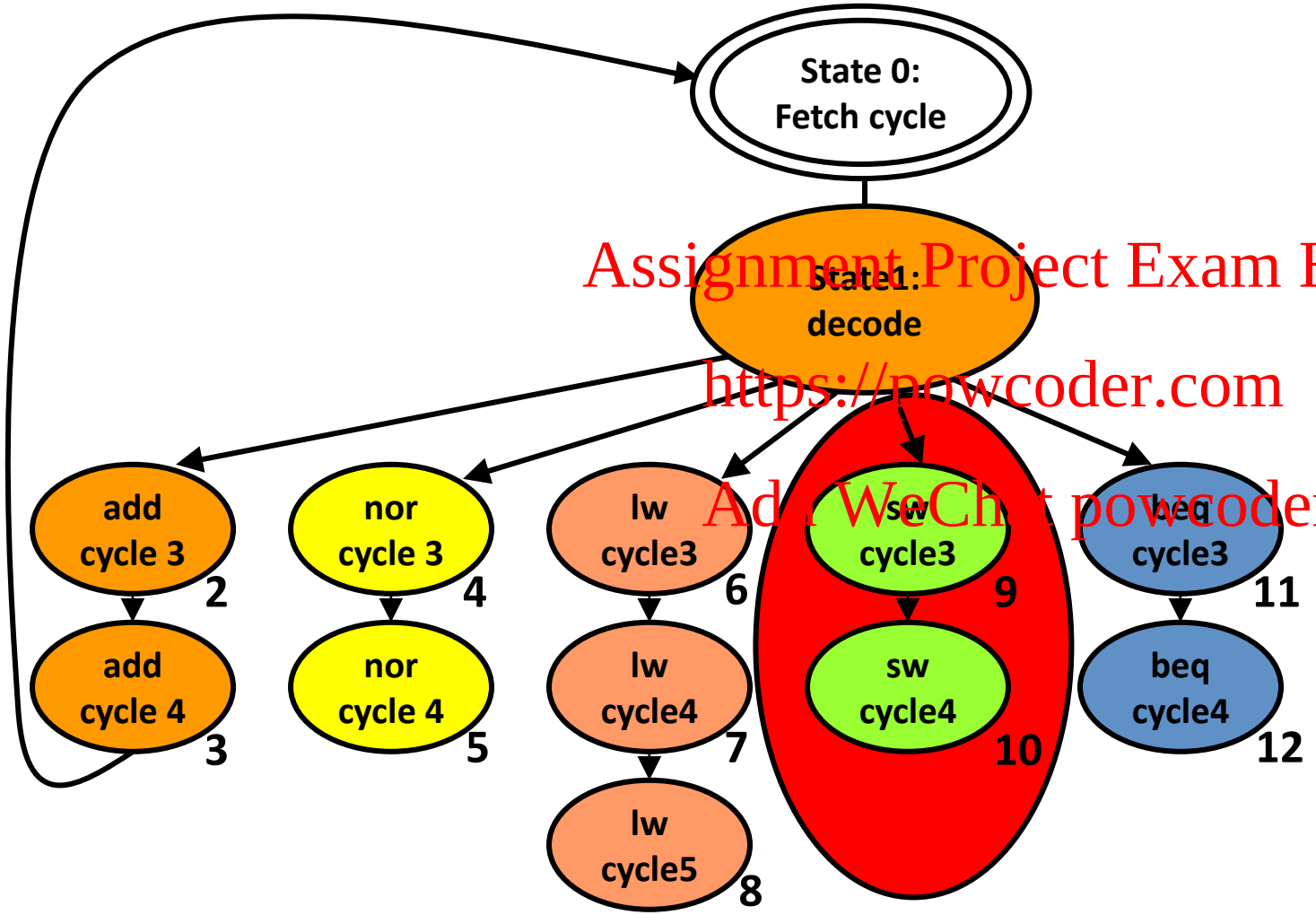
Multi-Cycle




Fetch cycle to execute next instruction

What about sw?

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# Building the Control ROM – `sw` (States 9,10)

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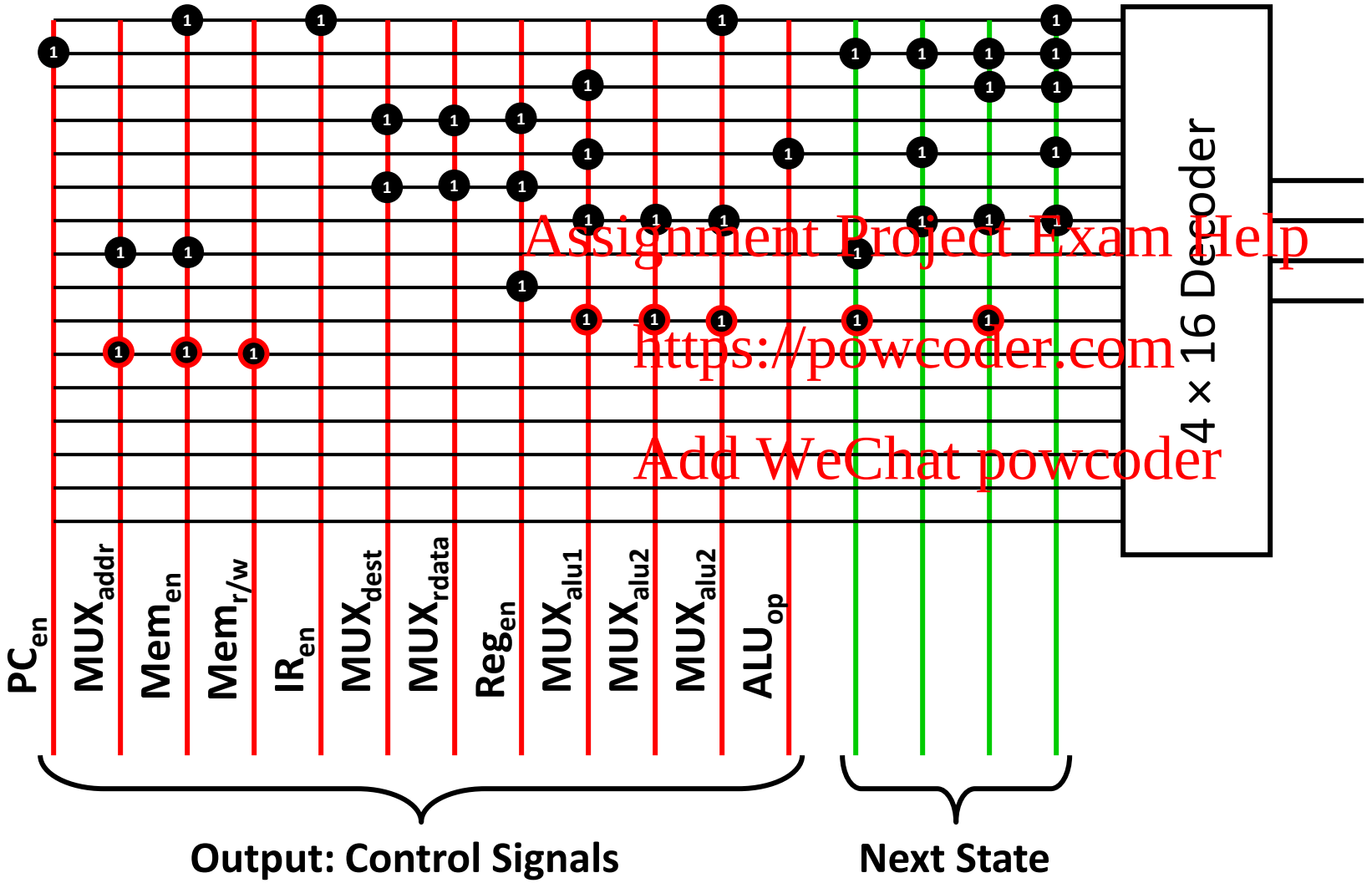
Multi-Cycle

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# Return to State 0

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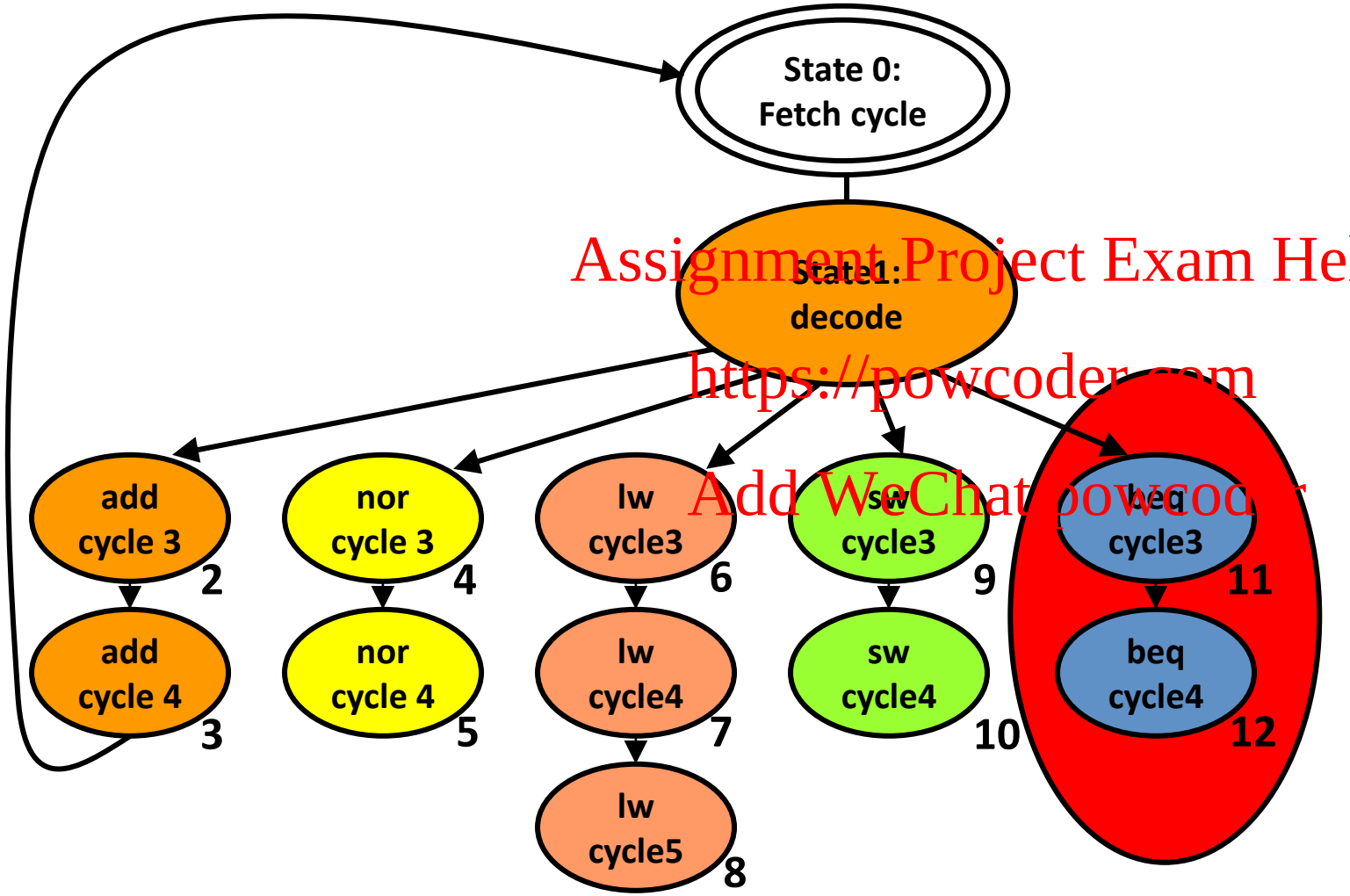
Multi-Cycle




Fetch cycle to execute next instruction

What about beq?

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# State 11: BEQ Cycle 3 Operation

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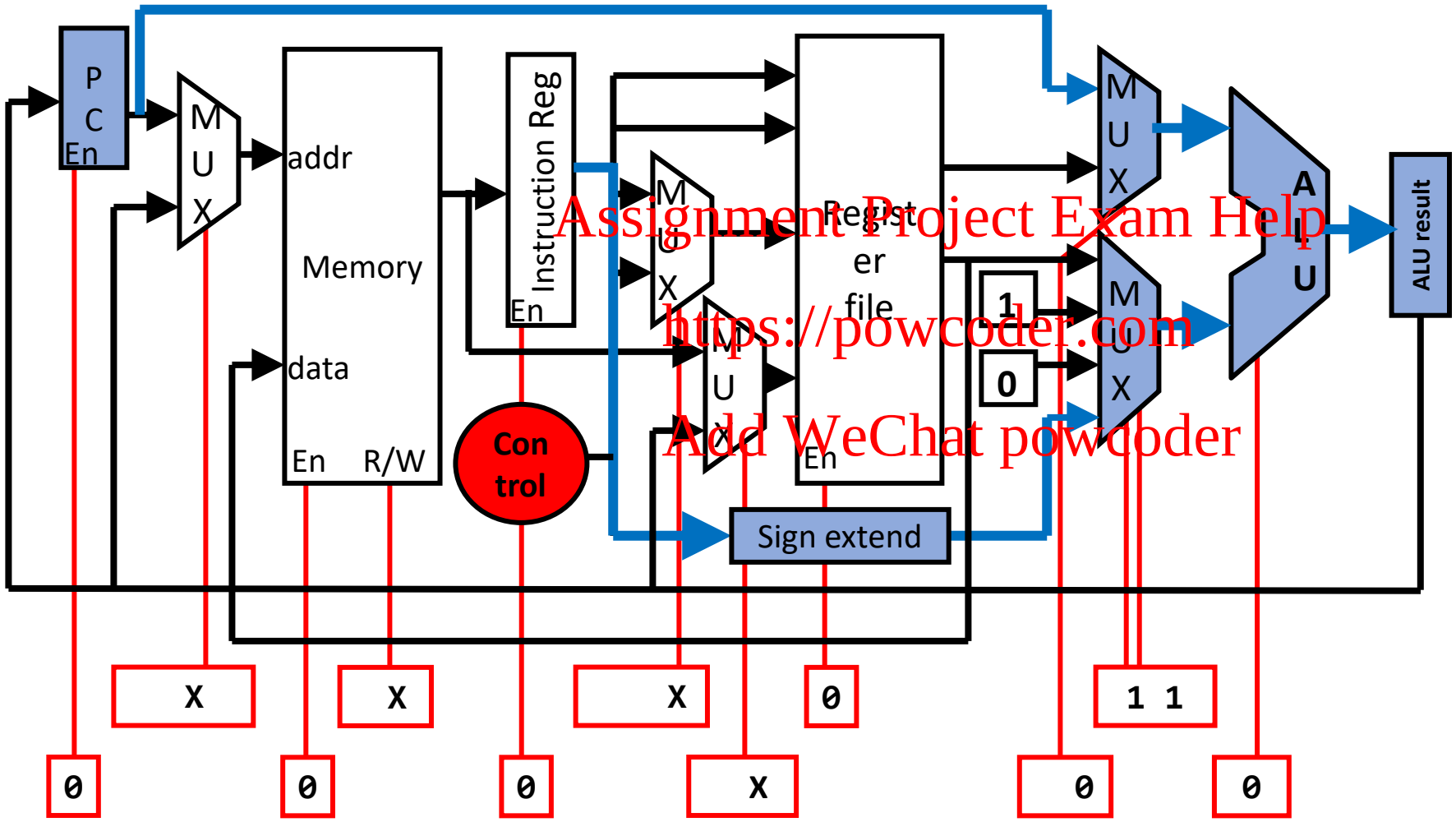
Multi-Cycle

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Calculate target address for branch

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# Building the Control ROM State 11 – beq

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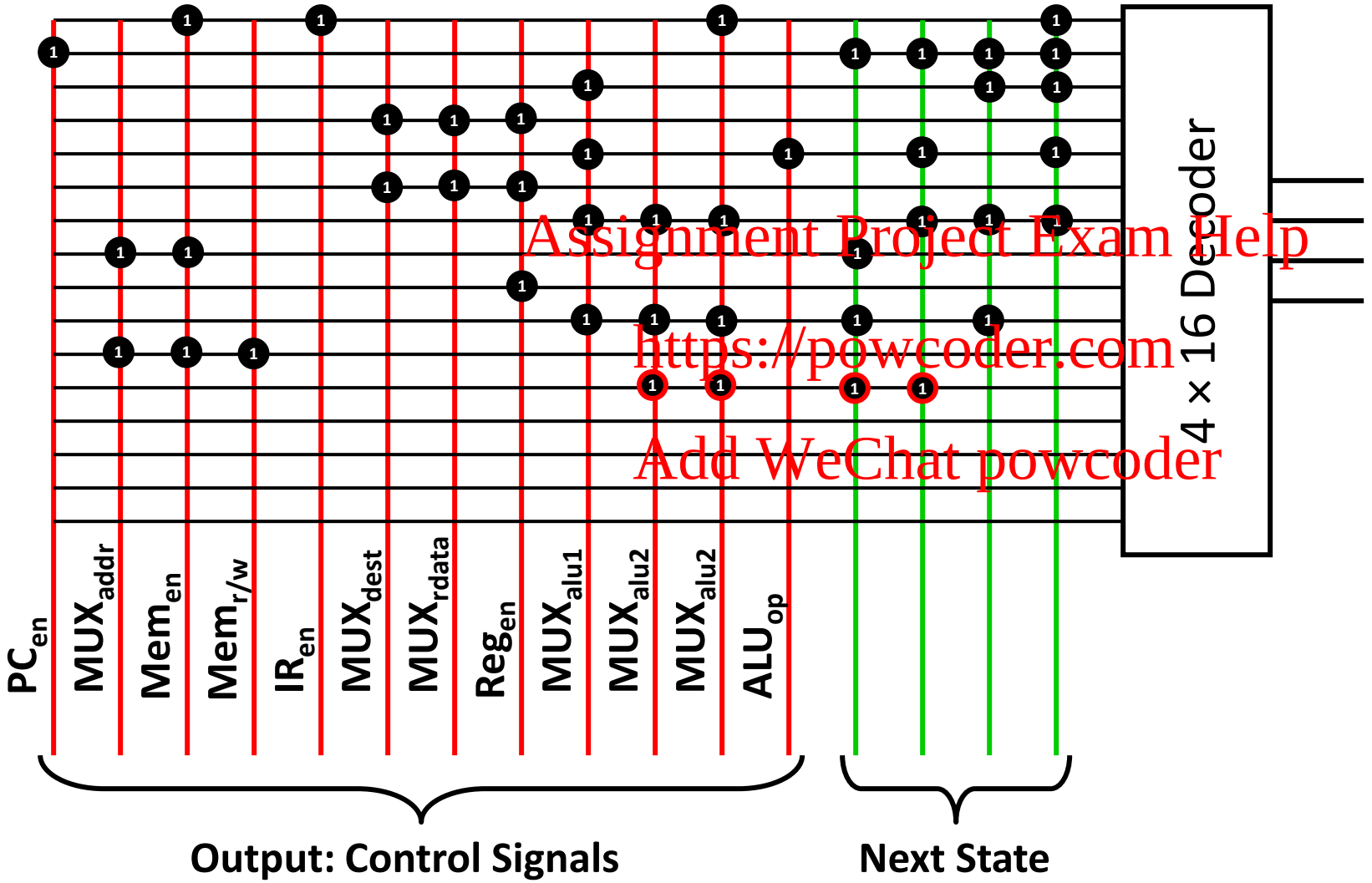
Multi-Cycle

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# State 12: BEQ Cycle 4 Operation

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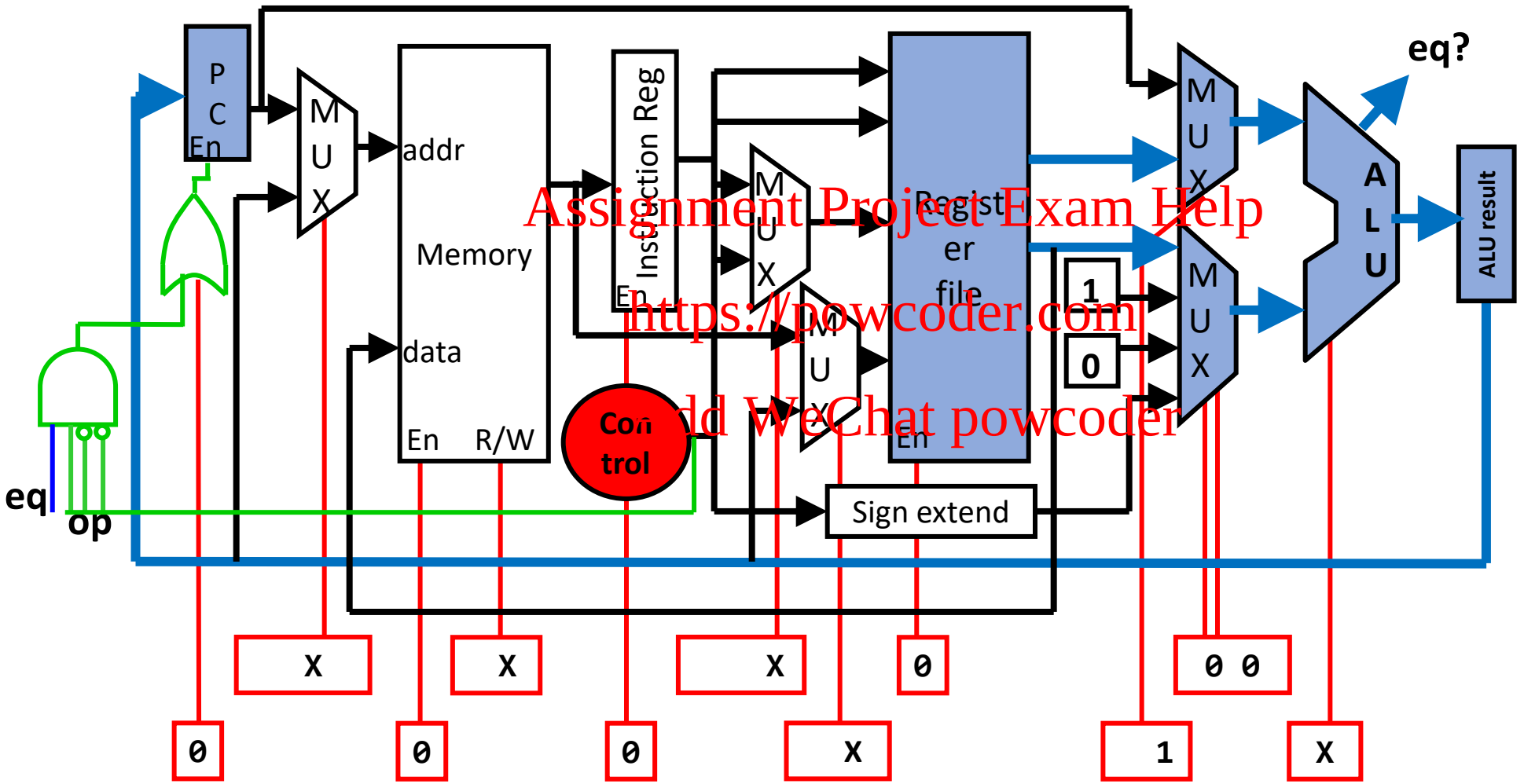
Write target address to PC
if ($data_{regA}$ == $data_{regB}$)

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# Building the Control ROM State 12 – beq

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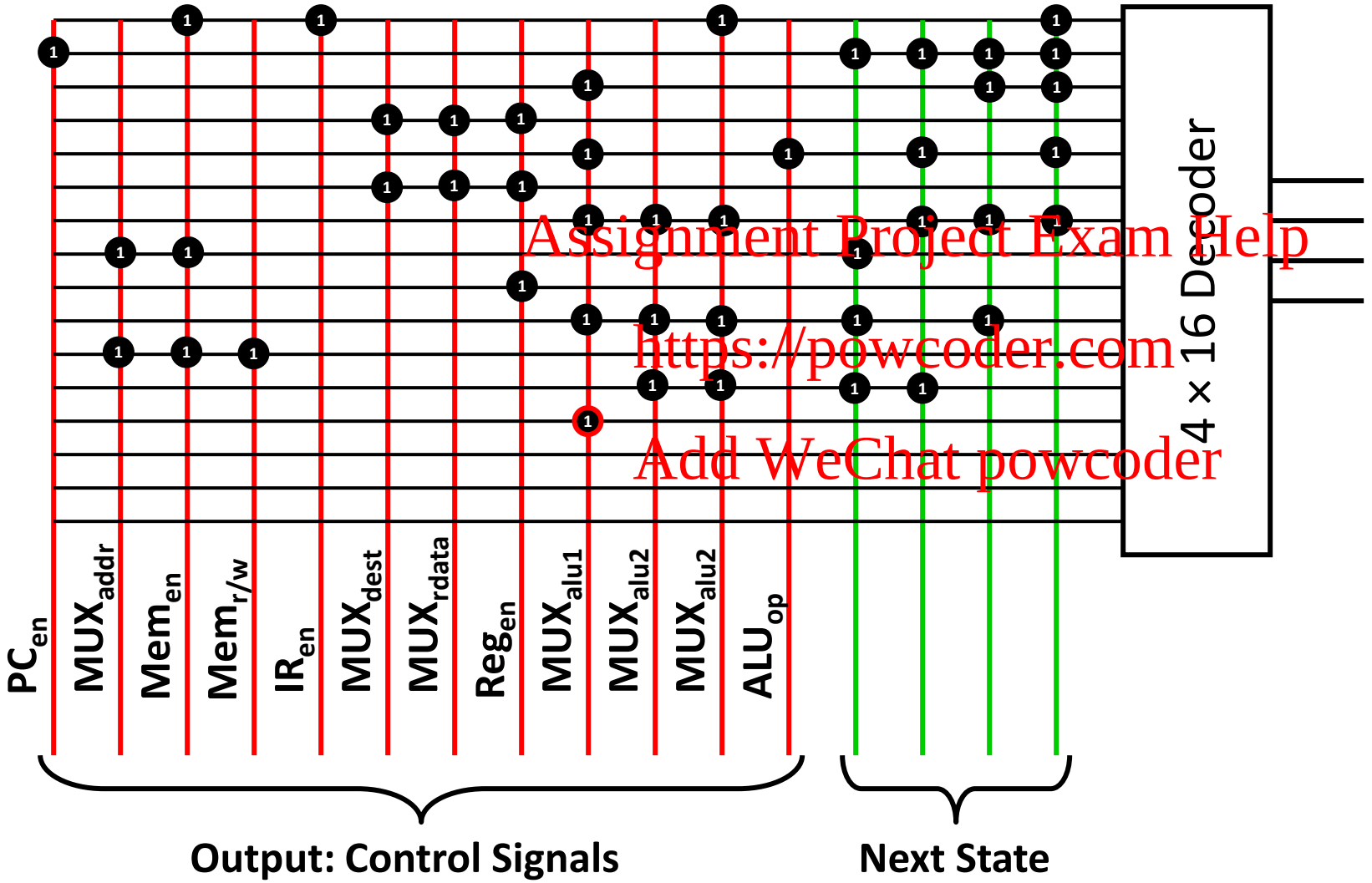
Multi-Cycle

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# Logistics

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- There are 3 videos for lecture 11
  - L11_1 – LC2K-Datapath_Single-Cycle
  - L11_2 – Multi-Cycle_0
  - L10_3 – Multi-Cycle_1
- There is one worksheet for lecture 10
  1. L11 worksheet

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