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19. Caches: Direct Mapped

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EECS 370 – Introduction to Computer Organization – Fall 2020

<https://powcoder.com>

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Announcements

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Upcoming deadlines:

HW4

due Nov 10th

Project 3

due Nov. 12th

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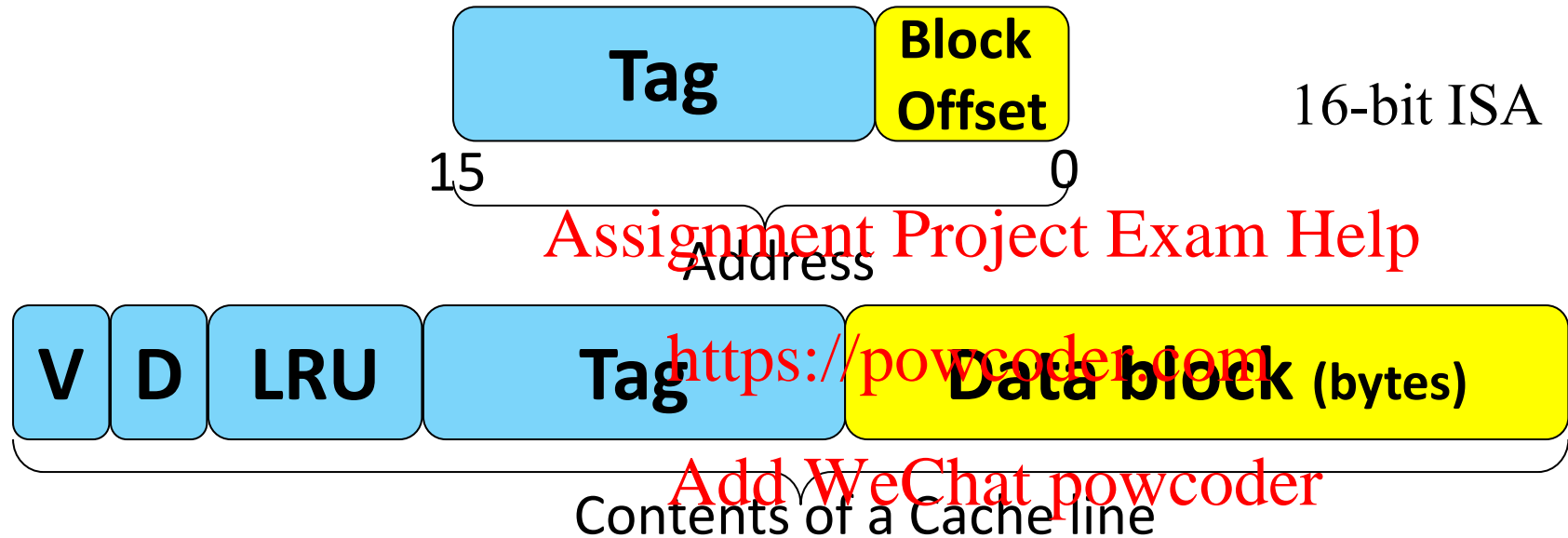
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Recap: Cache Blocks and Write policy

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Review: Cache Organization



Cache blocks:

- Captures spatial locality (increase cache hit rate)

- Reduces tag overhead (number and size of tags)

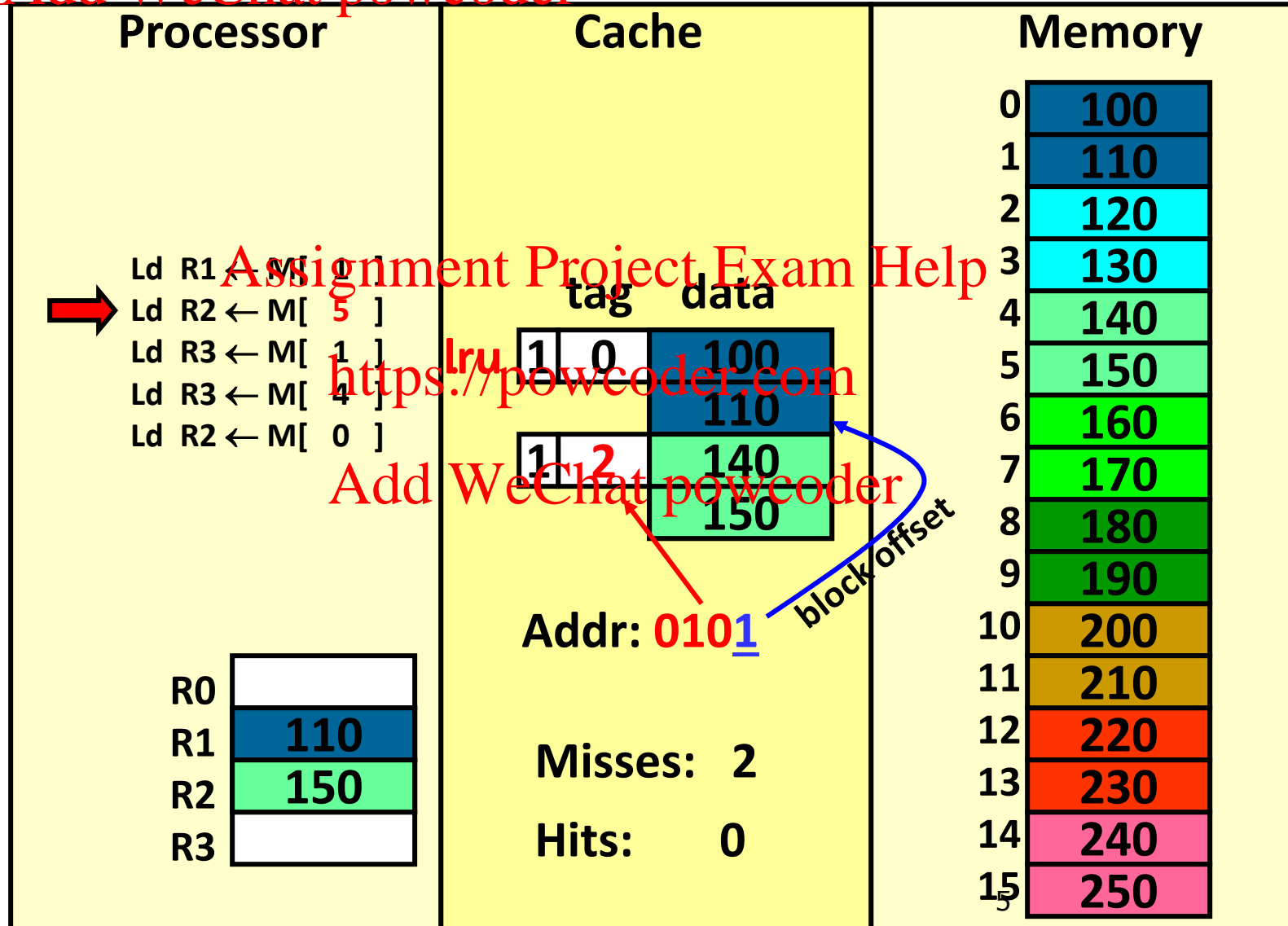
- Need not store block offset in the cache line

- Determine byte to be read/written from the address directly

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Review: How to find tag from address?

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Review: Writes

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Write-allocate vs. no-write-allocate caches

Policy that decides what to do with a cache-miss on a store instruction.

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Write-allocate: First bring data from memory into the cache, then write

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No-write-allocate: do not bring data in the cache, just write directly to the memory, not to the cache

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Review: Writes

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Write-through vs. write-back caches

Policy that decides when to **write to cache vs. memory vs. both**

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Write-through: write to both cache and memory

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Write-back: write only to cache, keep track of dirty cache line, write to memory when dirty cache line is evicted

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Review: Writes

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Store w No Allocate	Write-Back	Write-Through
Hit?	Write Cache	Write to Cache + Memory
Miss?	Write to Memory	Write to Memory
Replace block?	If evicted block is dirty, write to Memory	Do Nothing

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Store w Allocate	Write-Back	Write-Through
Hit?	Write Cache	Write to Cache + Memory
Miss?	Read from Memory to Cache, Allocate to LRU block Write to Cache	Read from Memory to Cache, Allocate to LRU block Write to Cache + Memory
Replace block?	If evicted block is dirty, write to Memory	Do Nothing

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Direct Mapped Caches <https://powcoder.com>

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Fully-associative caches

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A block can go
to **any** location

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Address:



3 bits

1 bit

Memory

Tag

Block_offset

0	100	00 0	0
1	110	00 0	1
2	120	00 1	0
3	130	00 1	1
4	140	01 0	0
5	150	01 0	1
6	160	01 1	0
7	170	01 1	1
8	180	10 0	0
9	190	10 0	1
10	200	10 1	0
11	210	10 1	1
12	220	11 0	0
13	230	11 0	1
14	240	11 1	0
15	250	11 1	1

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Fully-associative caches

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We designed a fully-associative cache

- A memory location can be copied to any cache line.
- We check every cache tag to determine whether the data is in the cache.

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This approach can be too slow sometimes

- Parallel tag searches are expensive and can be slow. Why?

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Direct mapped caches

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We can redesign the cache to eliminate the requirement for parallel tag lookups

- Direct mapped caches partition memory into as many regions as there are cache lines
- Each memory region maps to a single cache line in which data can be placed
- You then only need to check a single tag – the one associated with the region the reference is located in

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Mapping memory to cache (Direct-mapped)

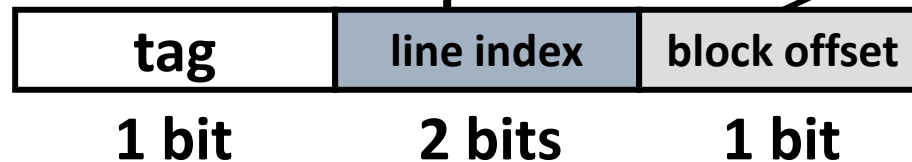
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A block can go to
only **one** location

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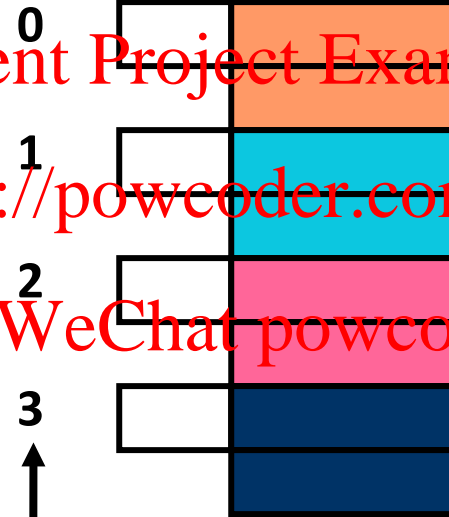
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Address:



Cache

tag data



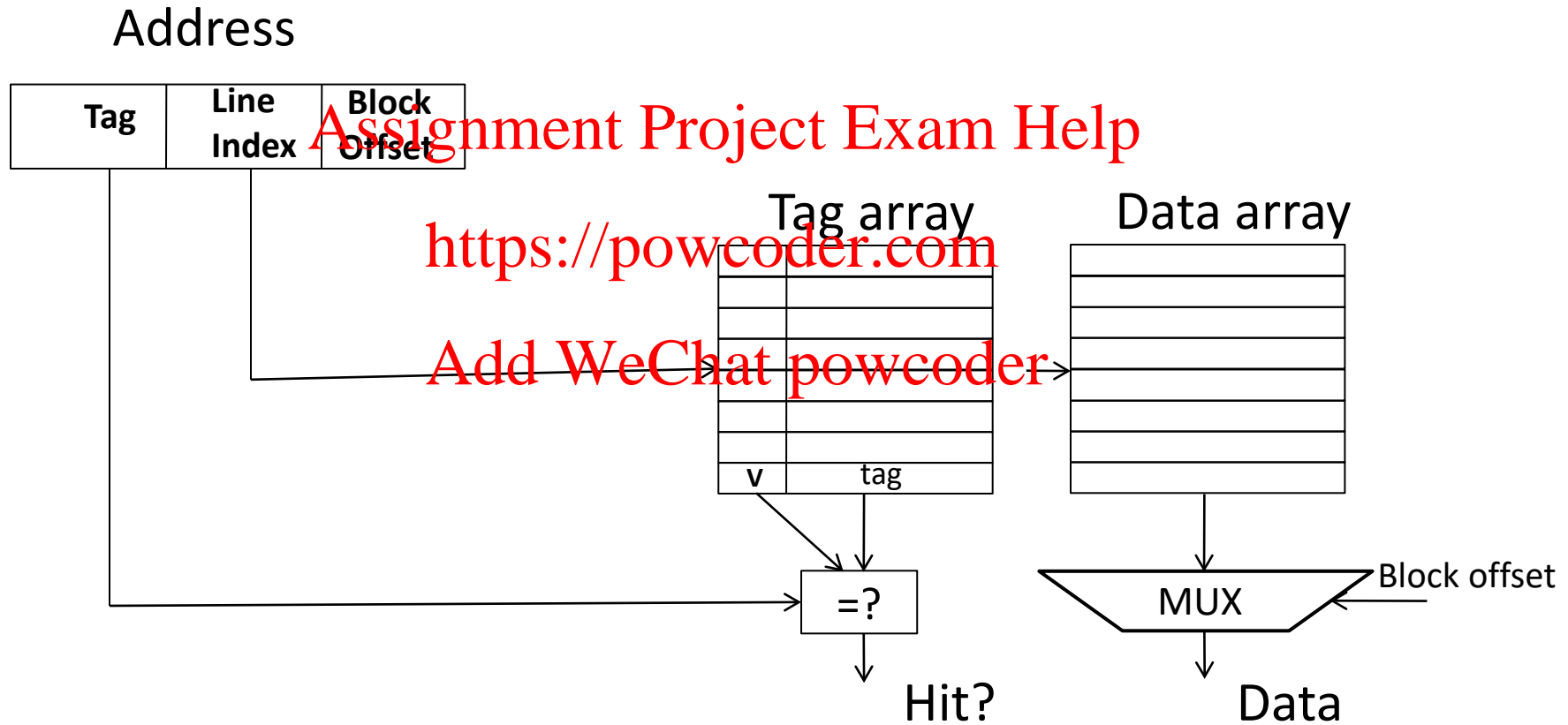
Memory

	Tag	Index	Block_offset
0	78	0	00
1	29	0	00
2	120	0	01
3	123	0	01
4	71	0	10
5	150	0	10
6	162	0	11
7	173	0	11
8	18	1	00
9	21	1	00
10	33	1	01
11	28	1	01
12	19	1	10
13	200	1	10
14	210	1	11
15	225	1	11

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Direct-mapped cache: Placement & Access

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Direct mapped caches

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Two blocks in memory that map to the same cache index cannot be present in the cache at the same time (conflict)

One index → one entry

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Can lead to 0% hit rate if more than one block accessed in an interleaved manner map to the same index

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Assume addresses A and B have the same index bits but different tag bits

A, B, A, B, A, B, A, B, ...

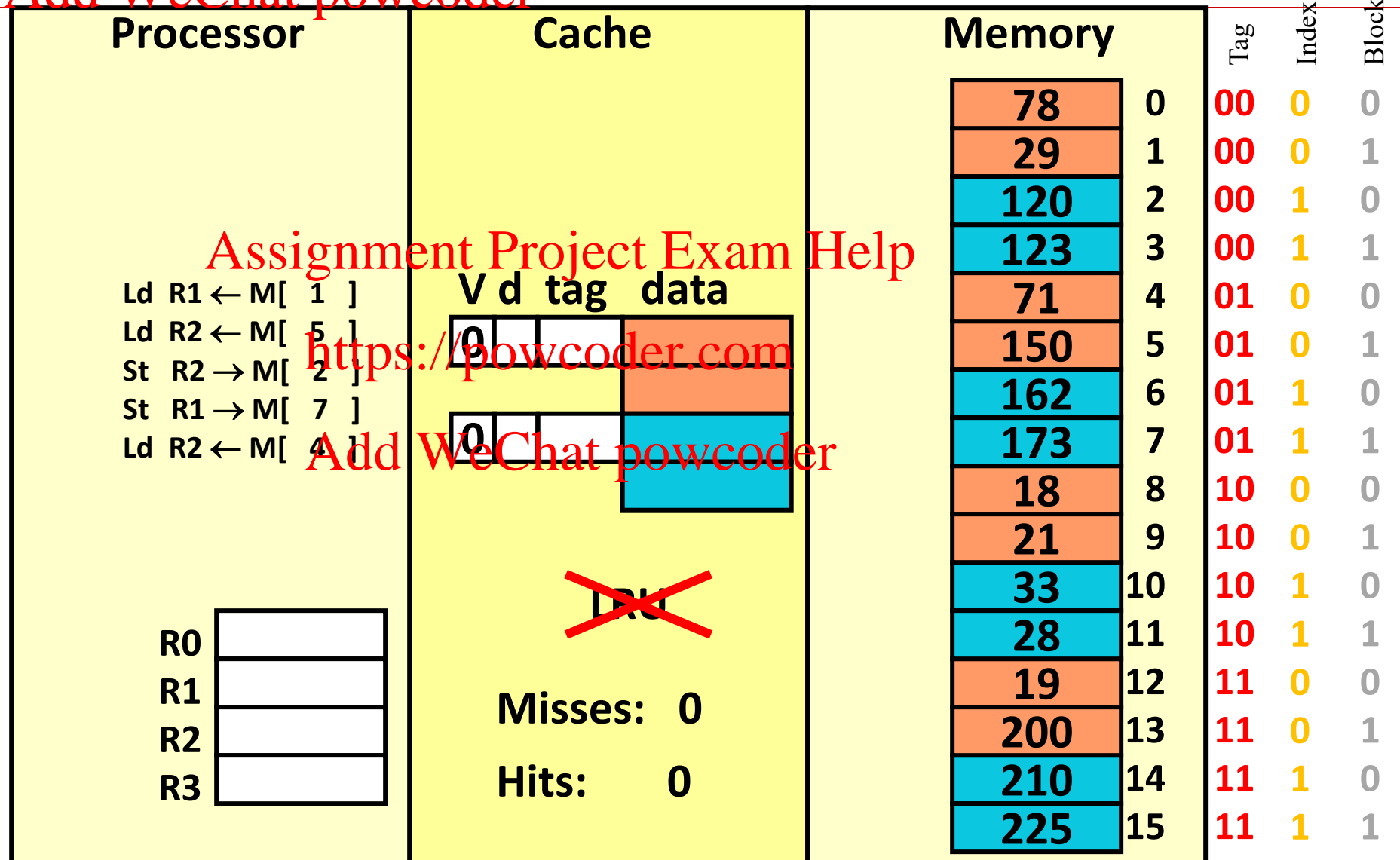
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All accesses are conflict misses

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Direct-mapped cache

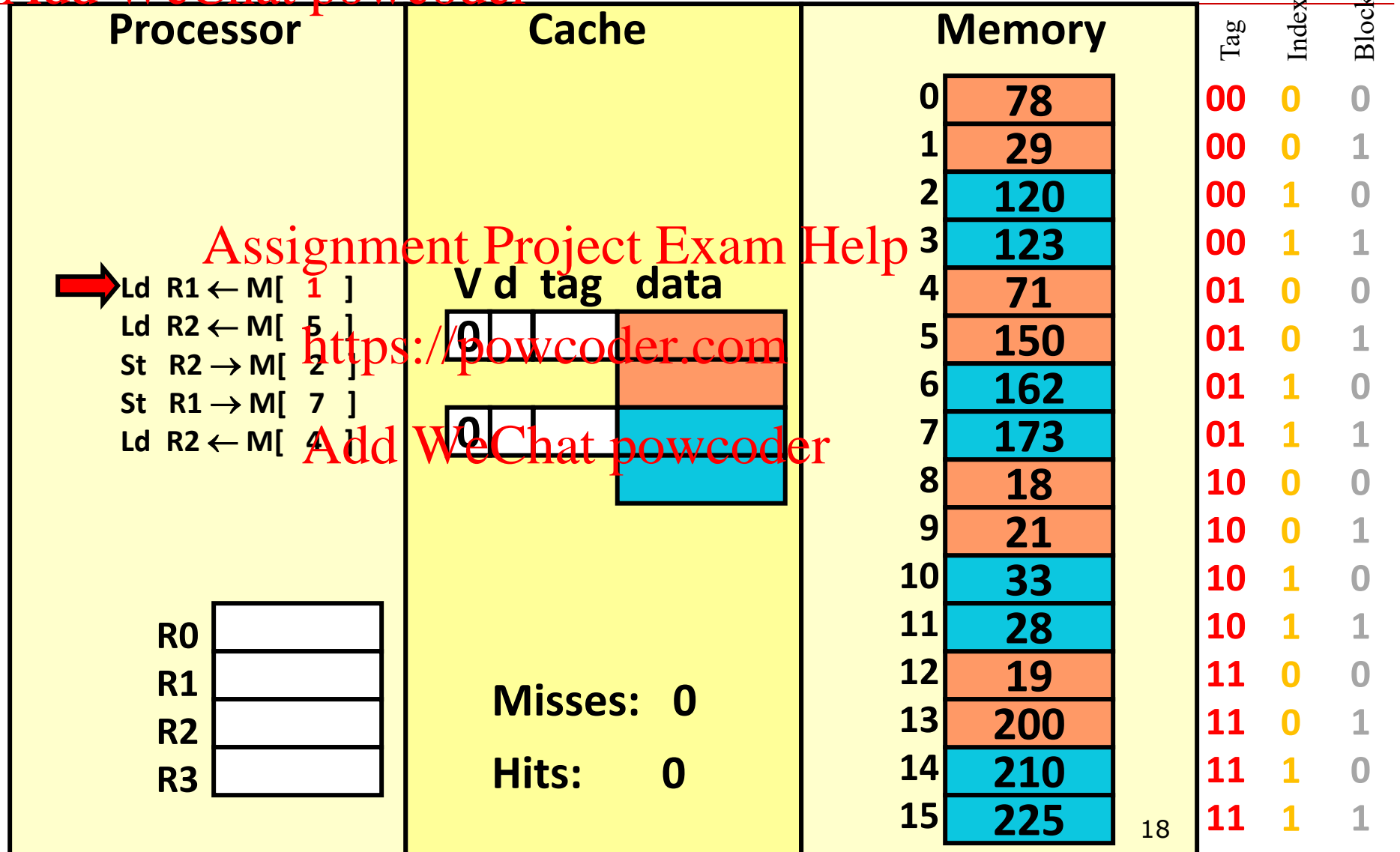
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Direct-mapped (REF 1)

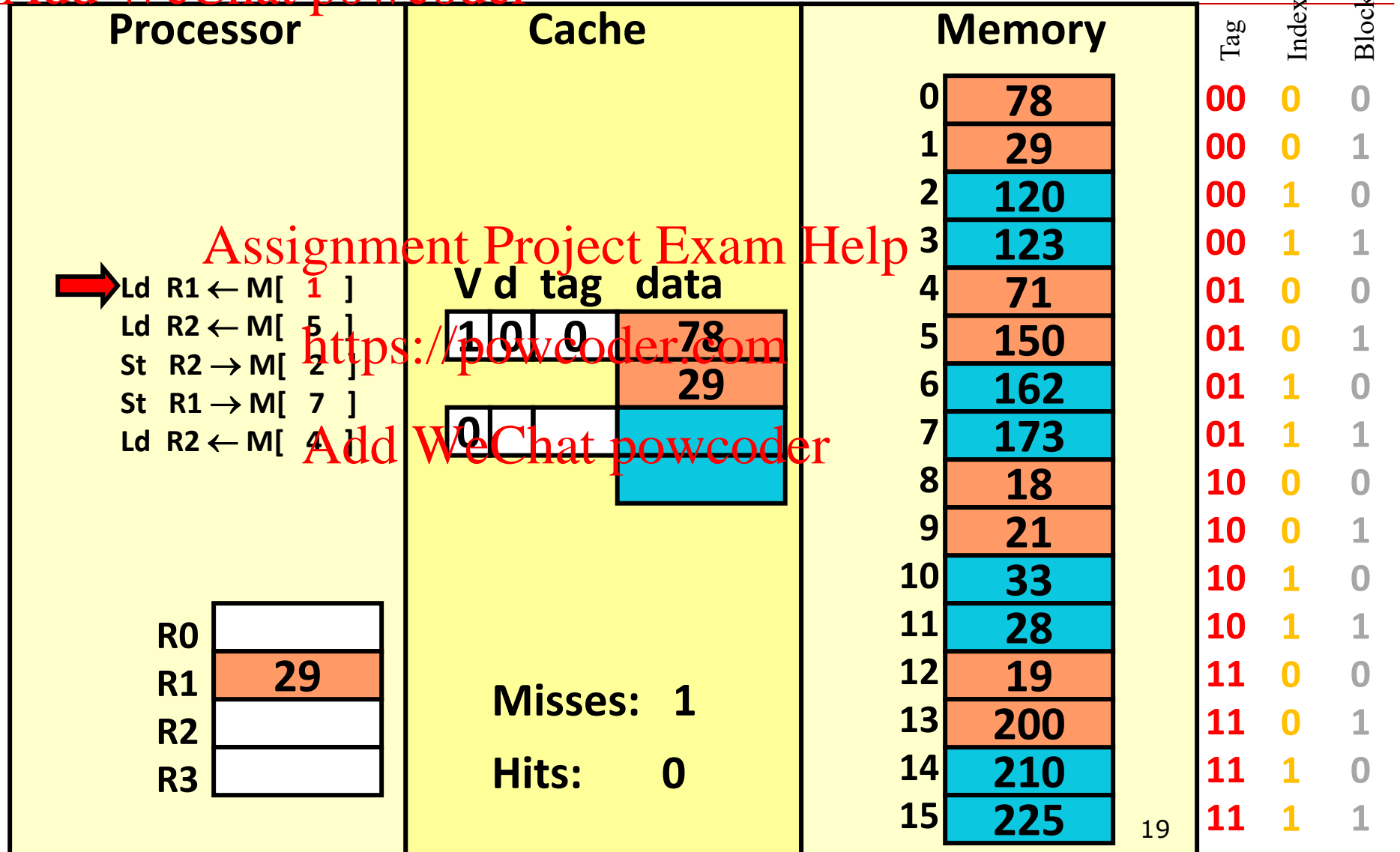
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Direct-mapped (REF 1)

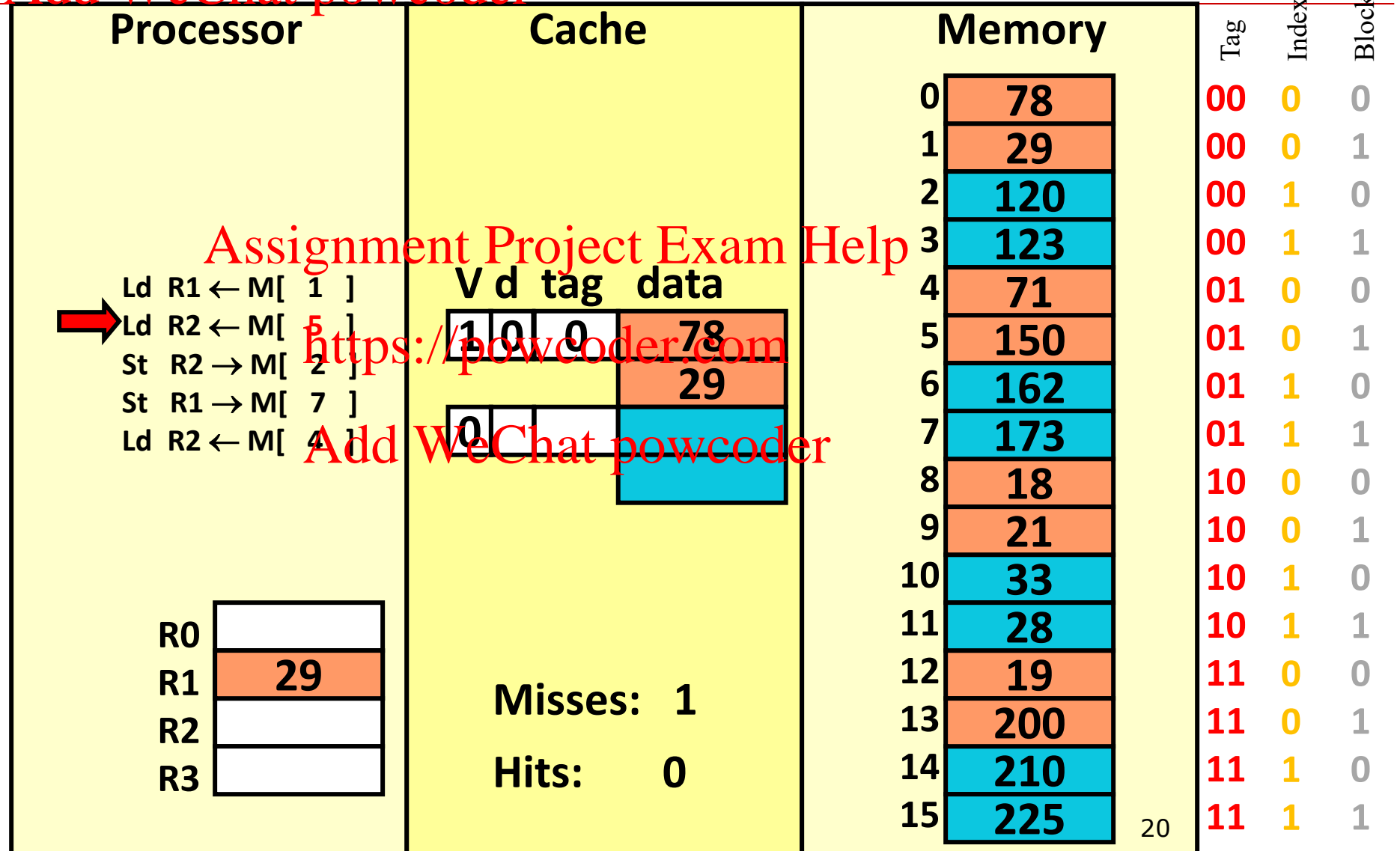
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Direct-mapped (REF 2)

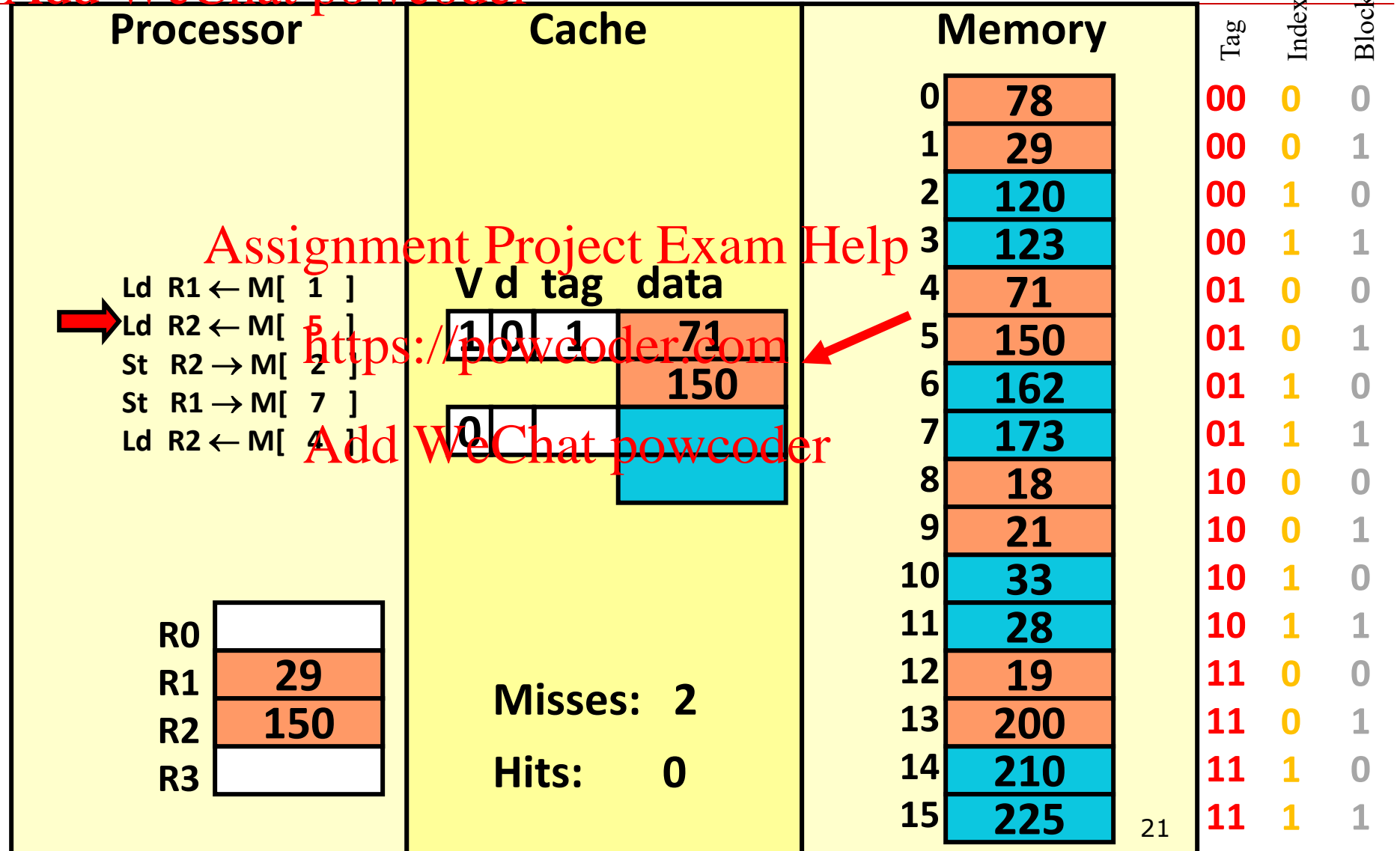
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Direct-mapped (REF 2)

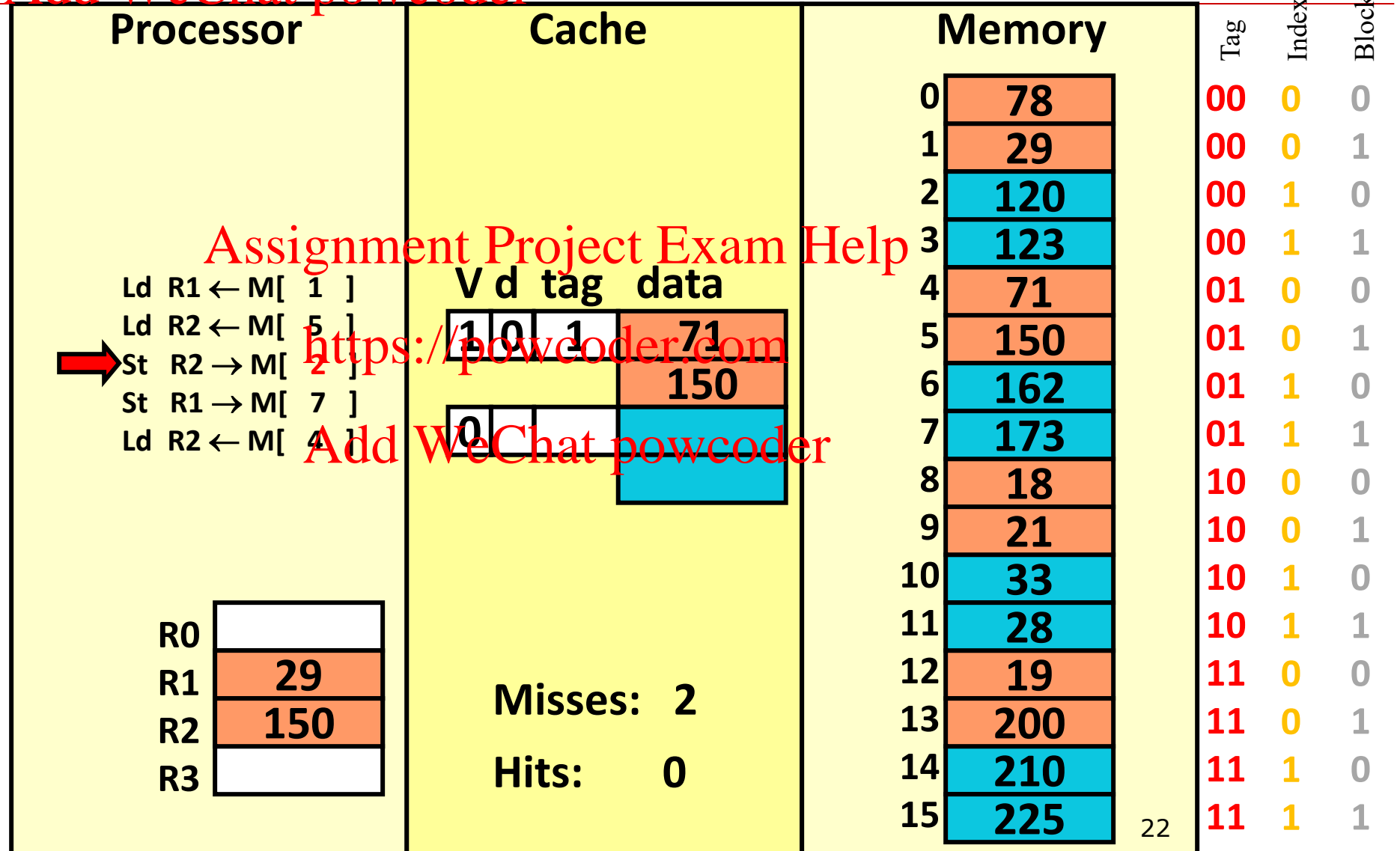
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Direct-mapped (REF 3)

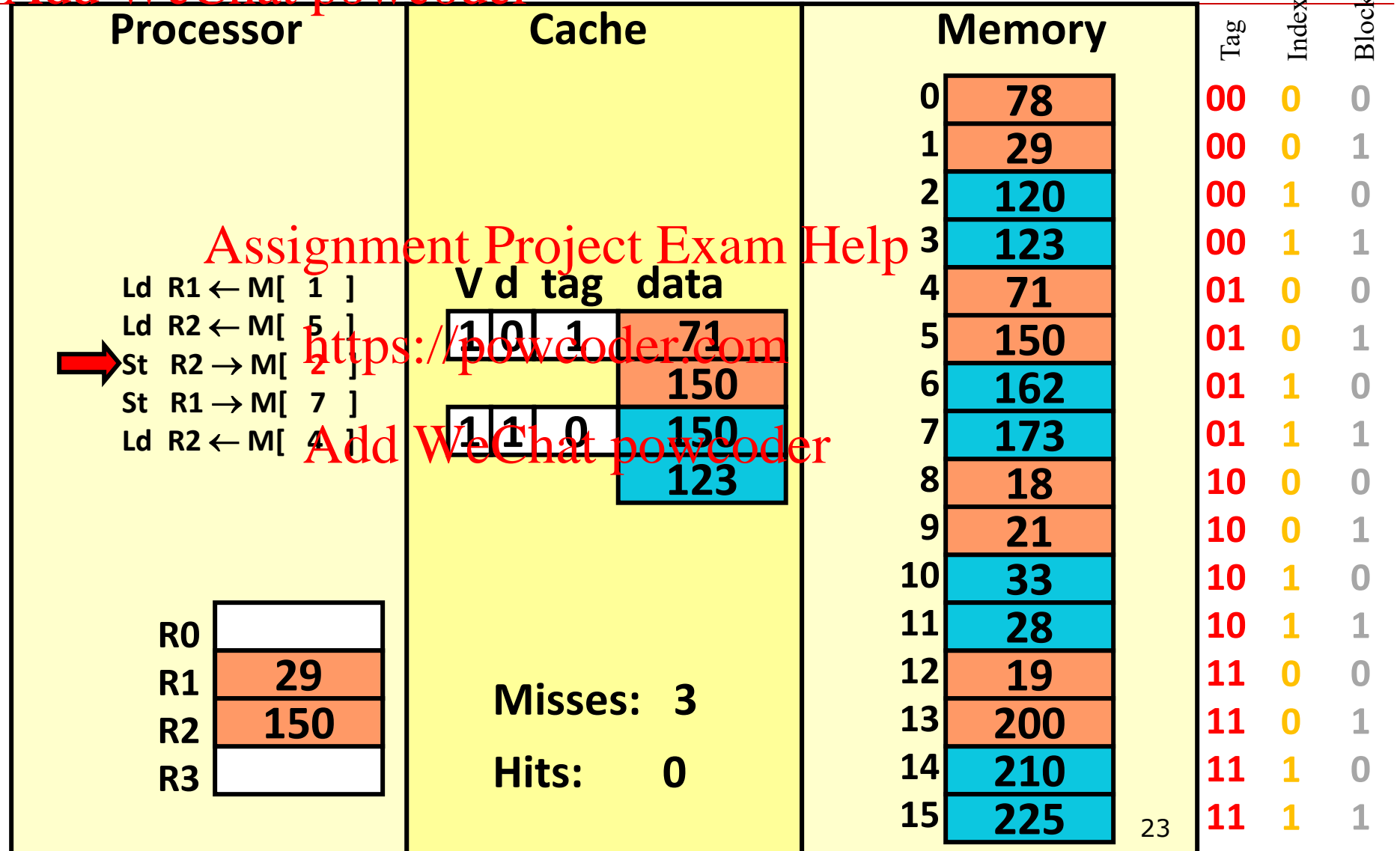
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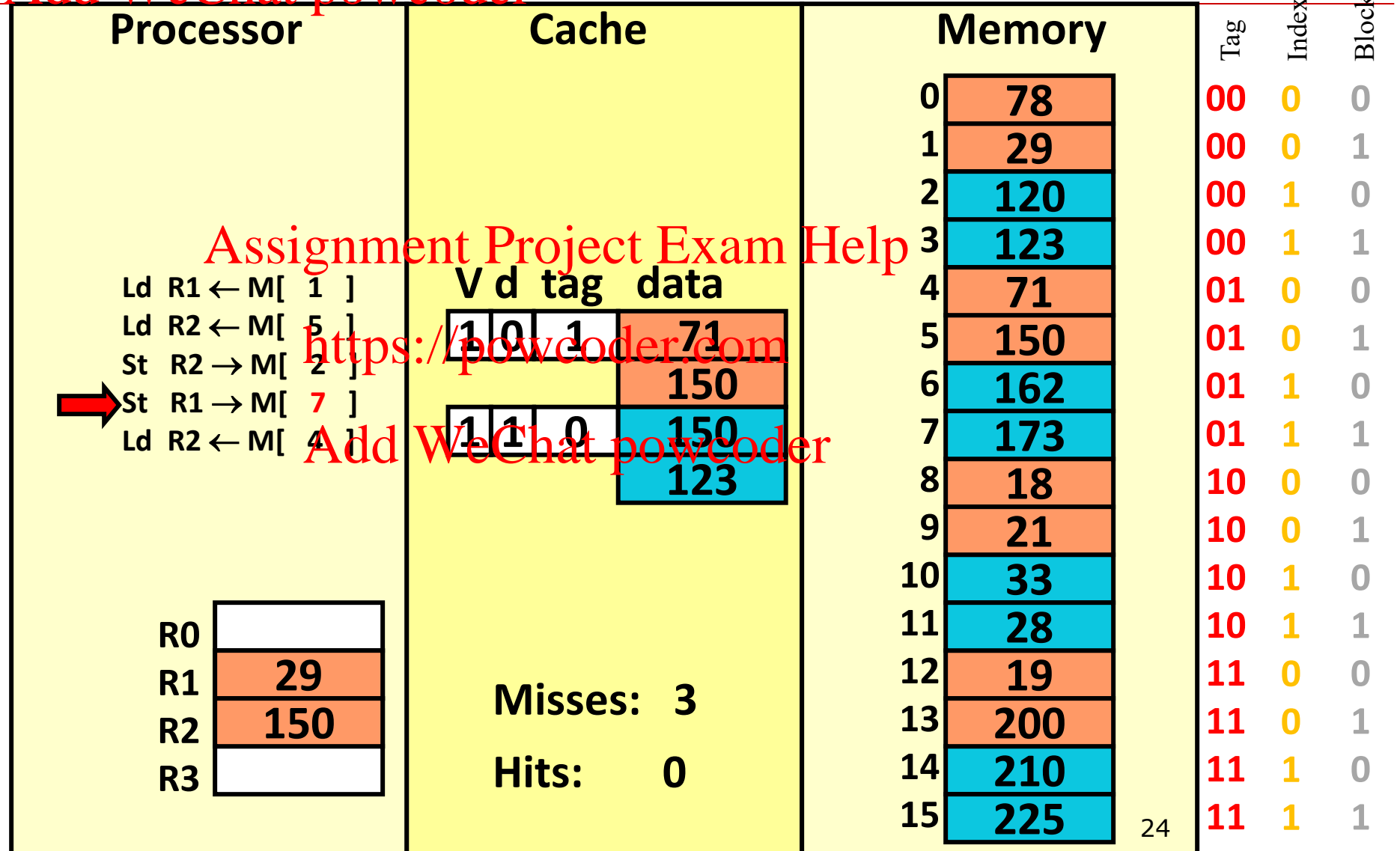
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Direct-mapped (REF 4)

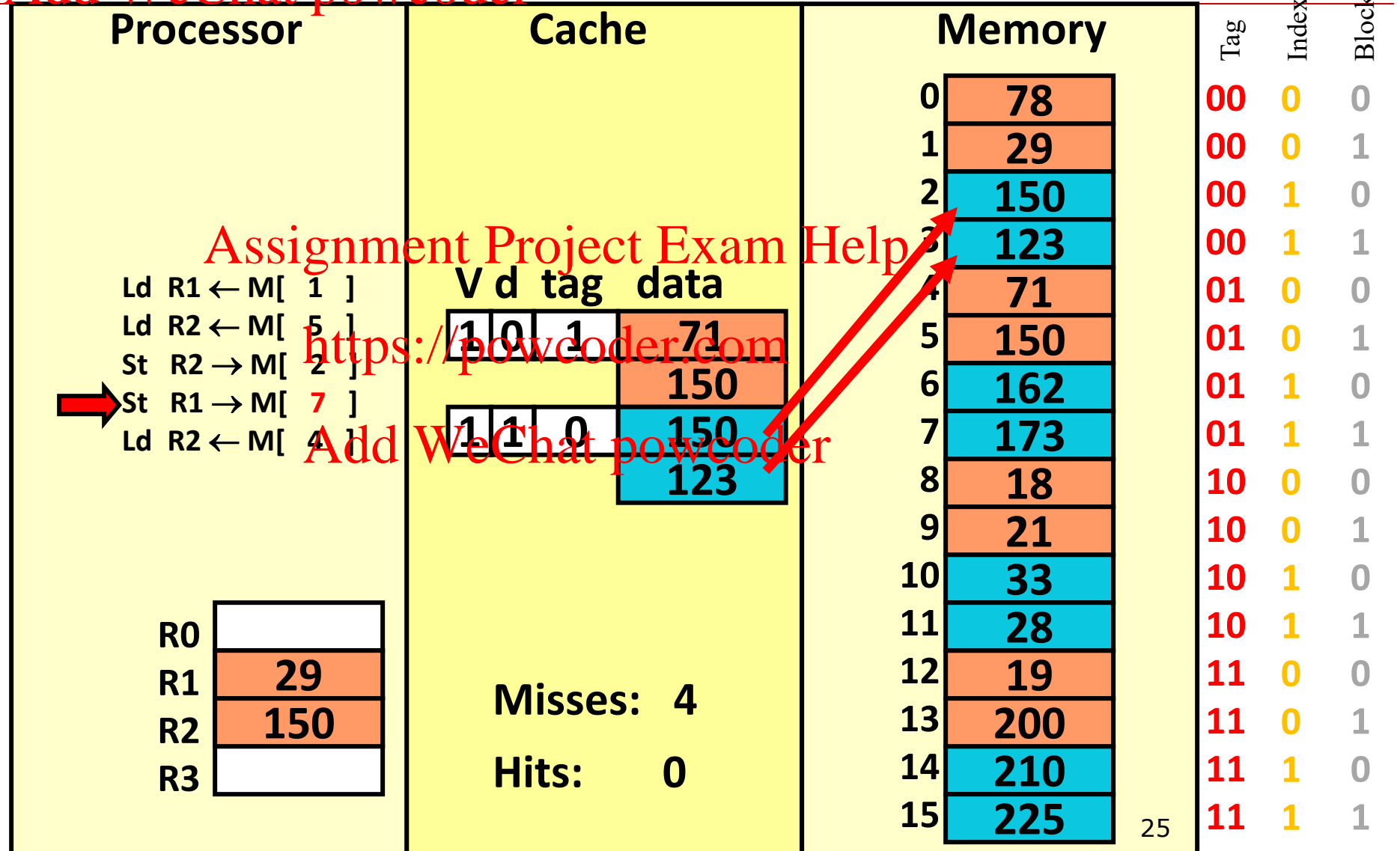
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Direct-mapped (REF 4)

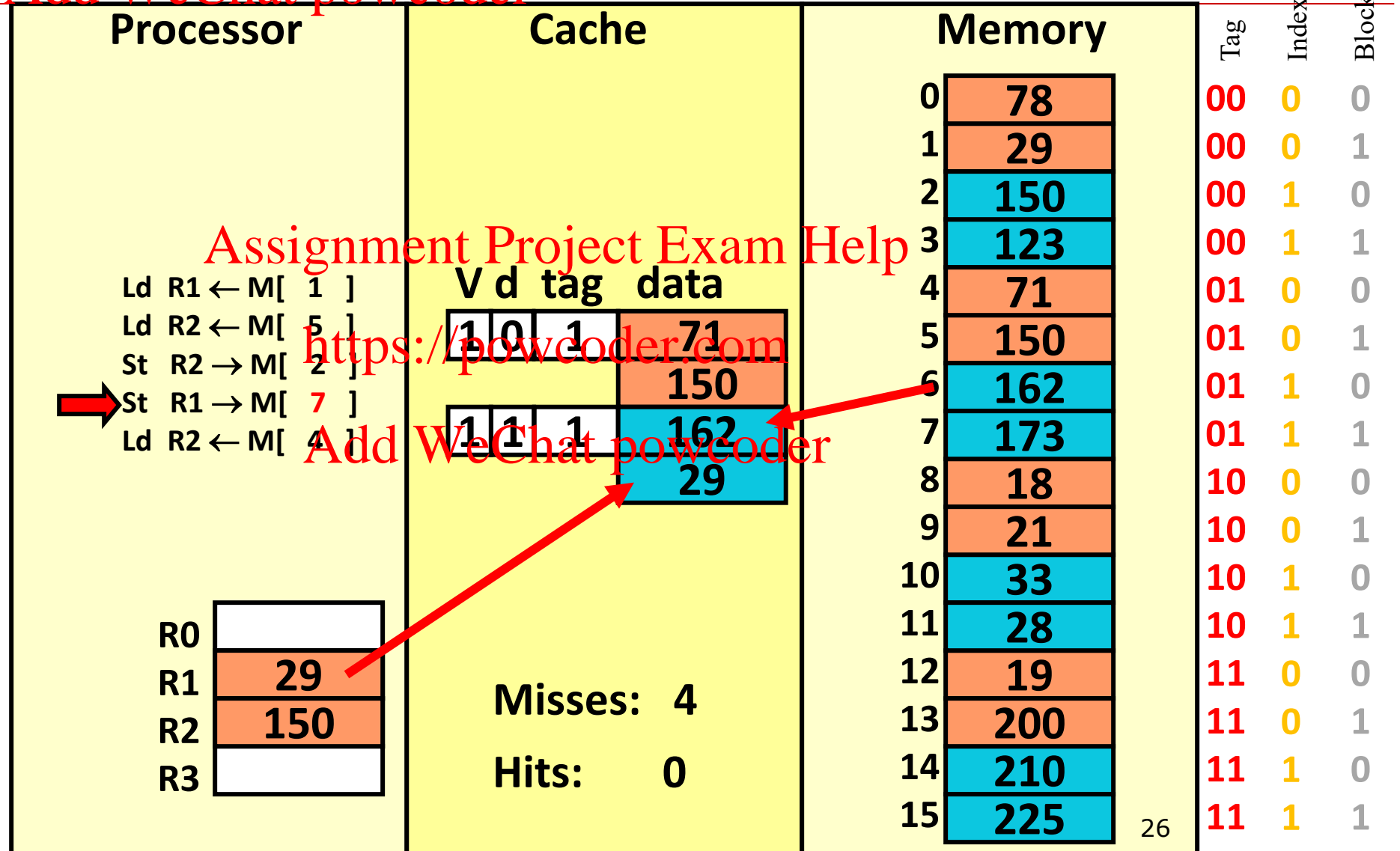
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Direct-mapped (REF 4)

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Direct-mapped (REF 5)

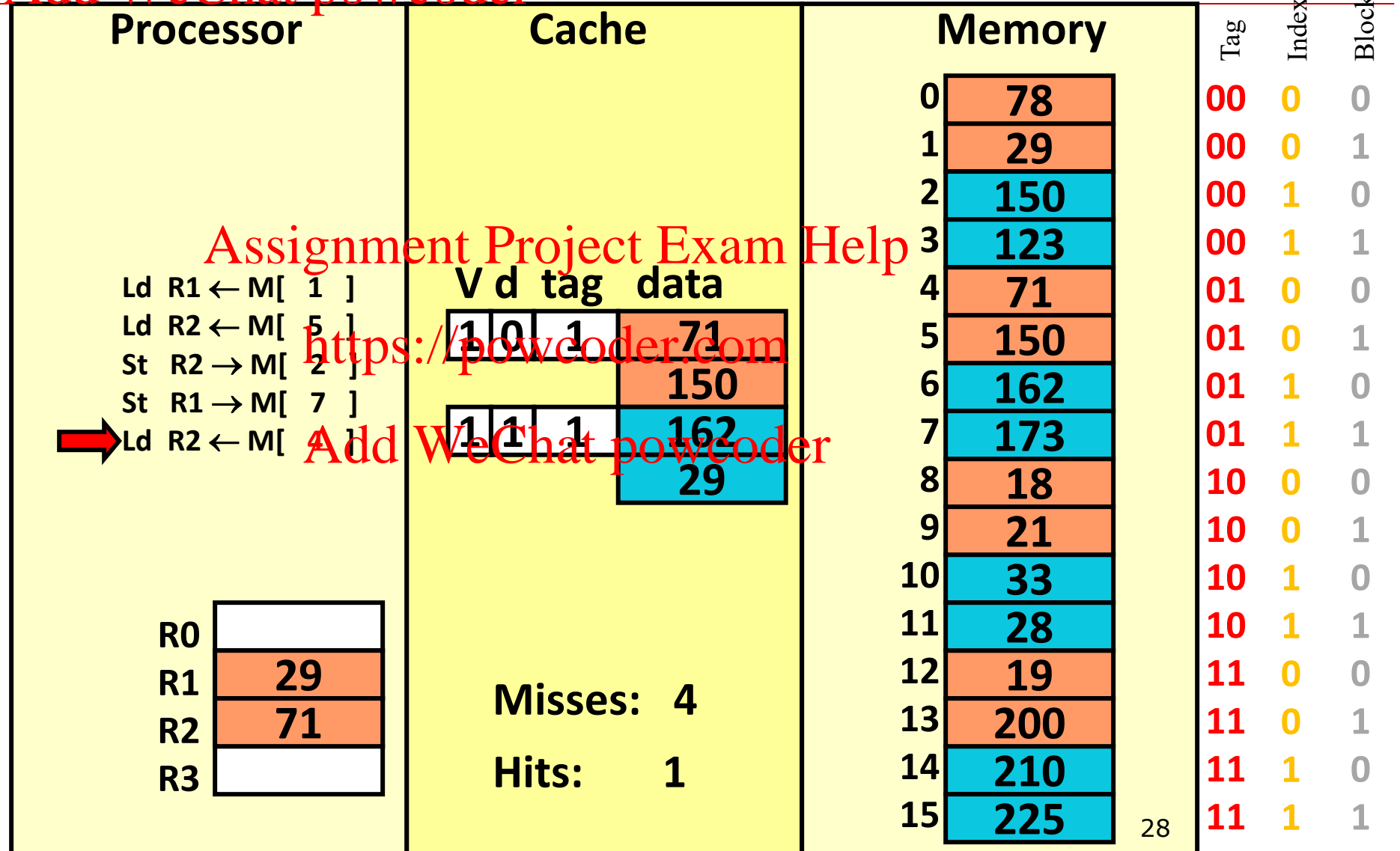
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Processor	Cache	Memory	Tag	Index	Block_offset
		0 78	00	0	0
		1 29	00	0	1
		2 150	00	1	0
		3 123	00	1	1
		4 71	01	0	0
		5 150	01	0	1
		6 162	01	1	0
		7 173	01	1	1
		8 18	10	0	0
		9 21	10	0	1
		10 33	10	1	0
		11 28	10	1	1
		12 19	11	0	0
		13 200	11	0	1
		14 210	11	1	0
		15 225	11	1	1
		27			
Ld R1 ← M[1] Ld R2 ← M[5] St R2 → M[2] St R1 → M[7] → Ld R2 ← M[1]	V d tag data 1 0 1 71 1 0 1 150 1 1 1 162 1 1 1 29 Misses: 4 Hits: 0				
R0 R1 29 R2 150 R3					

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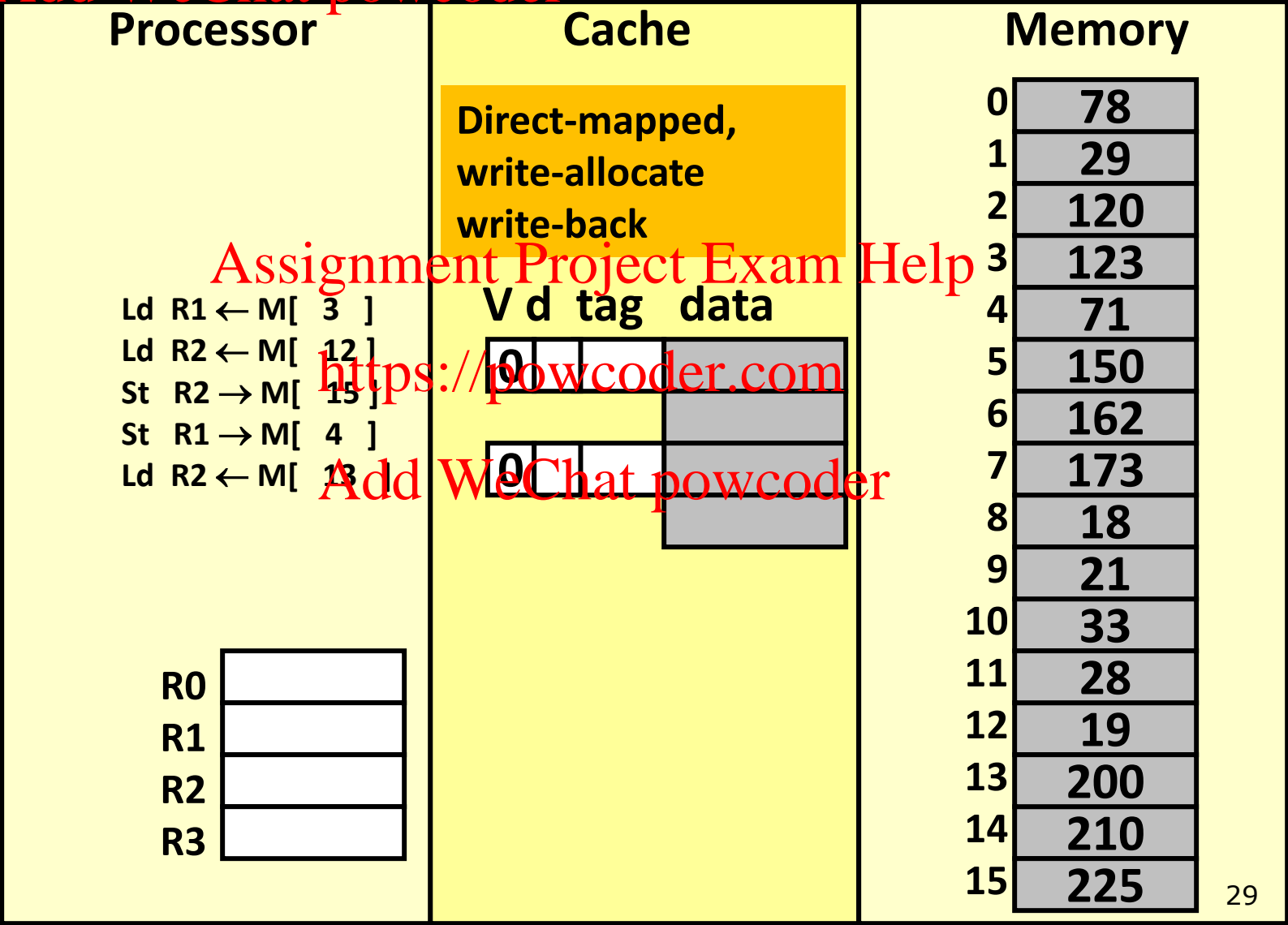
Direct-mapped (REF 5)

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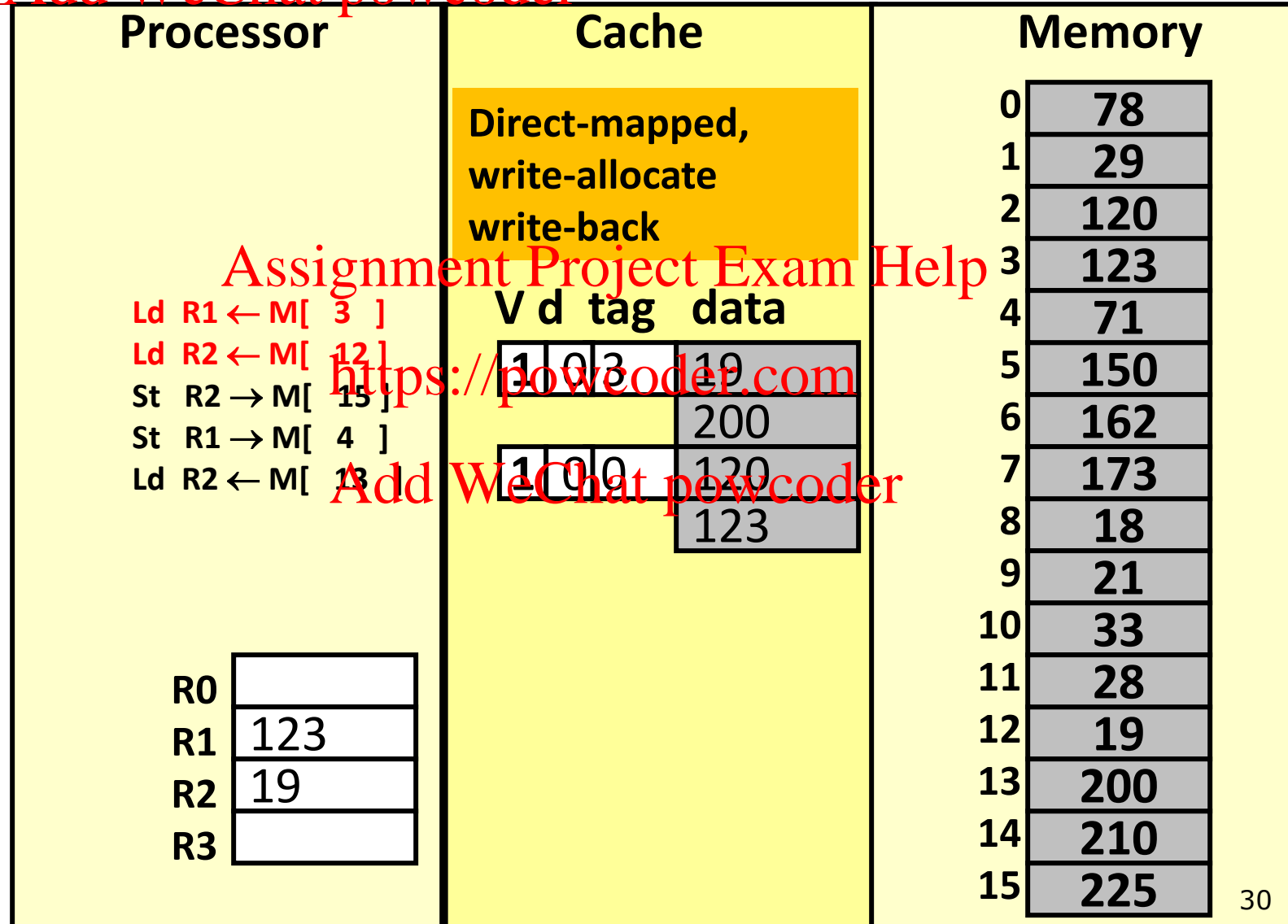
Class Problem – What is the state of the cache after executing the following instruction sequence?

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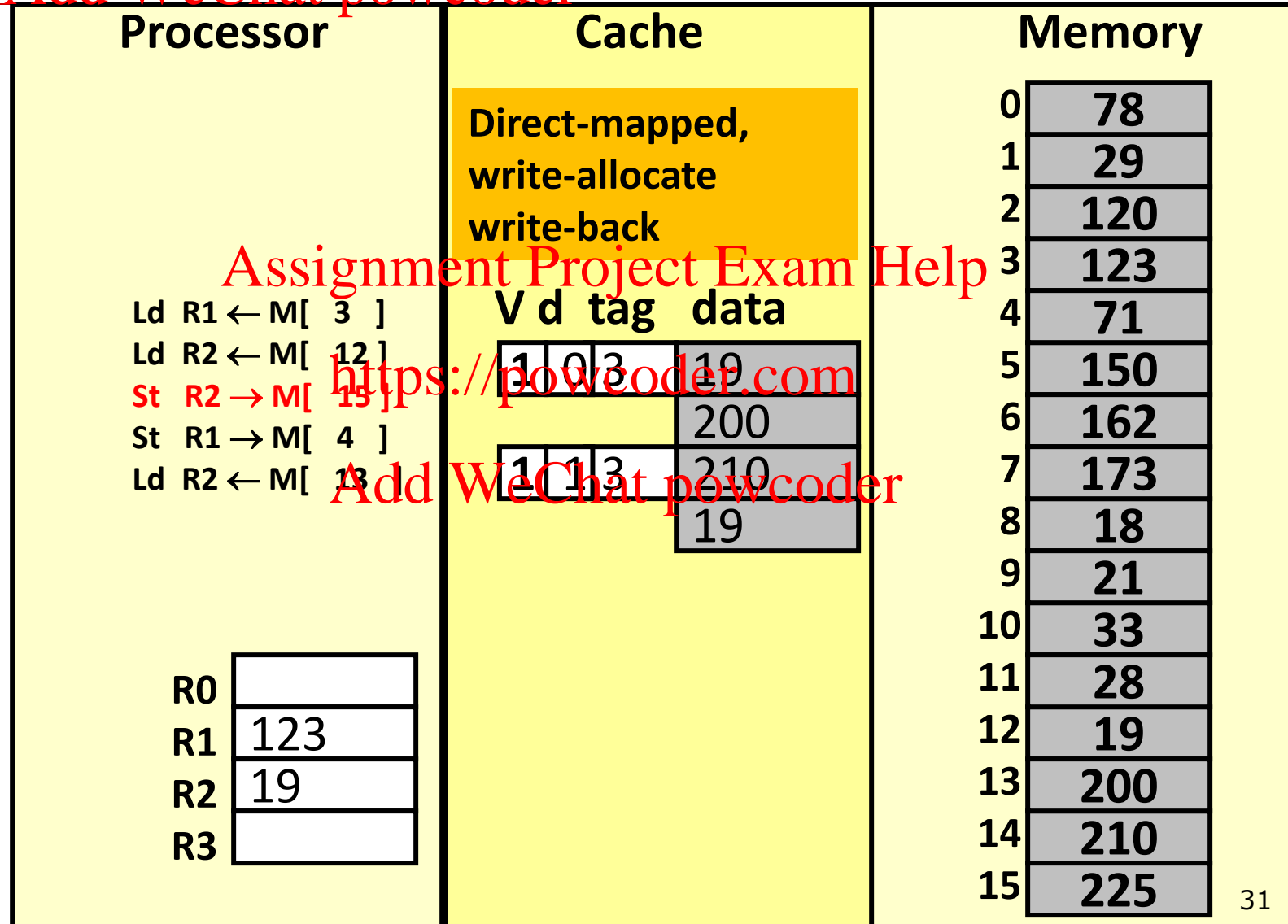
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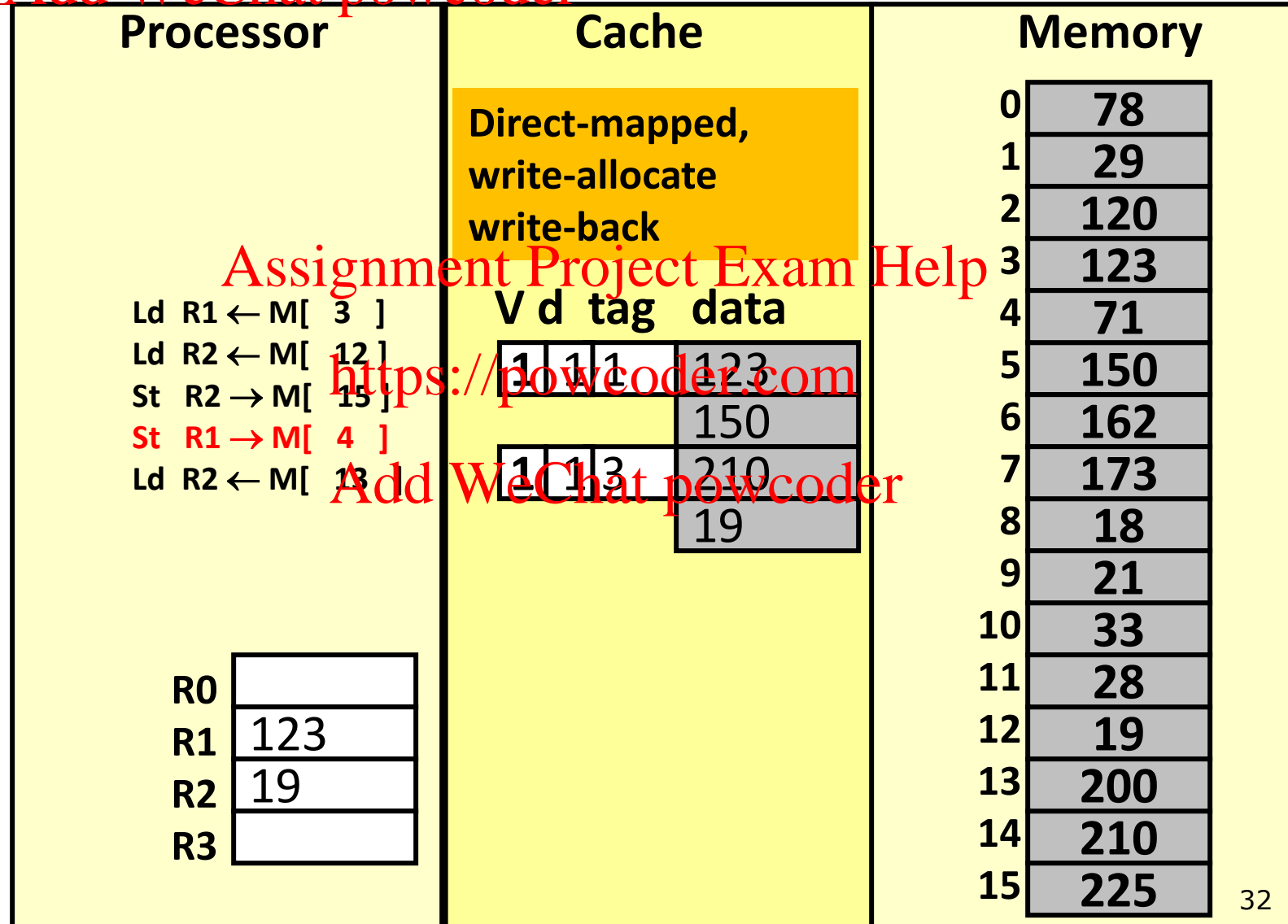
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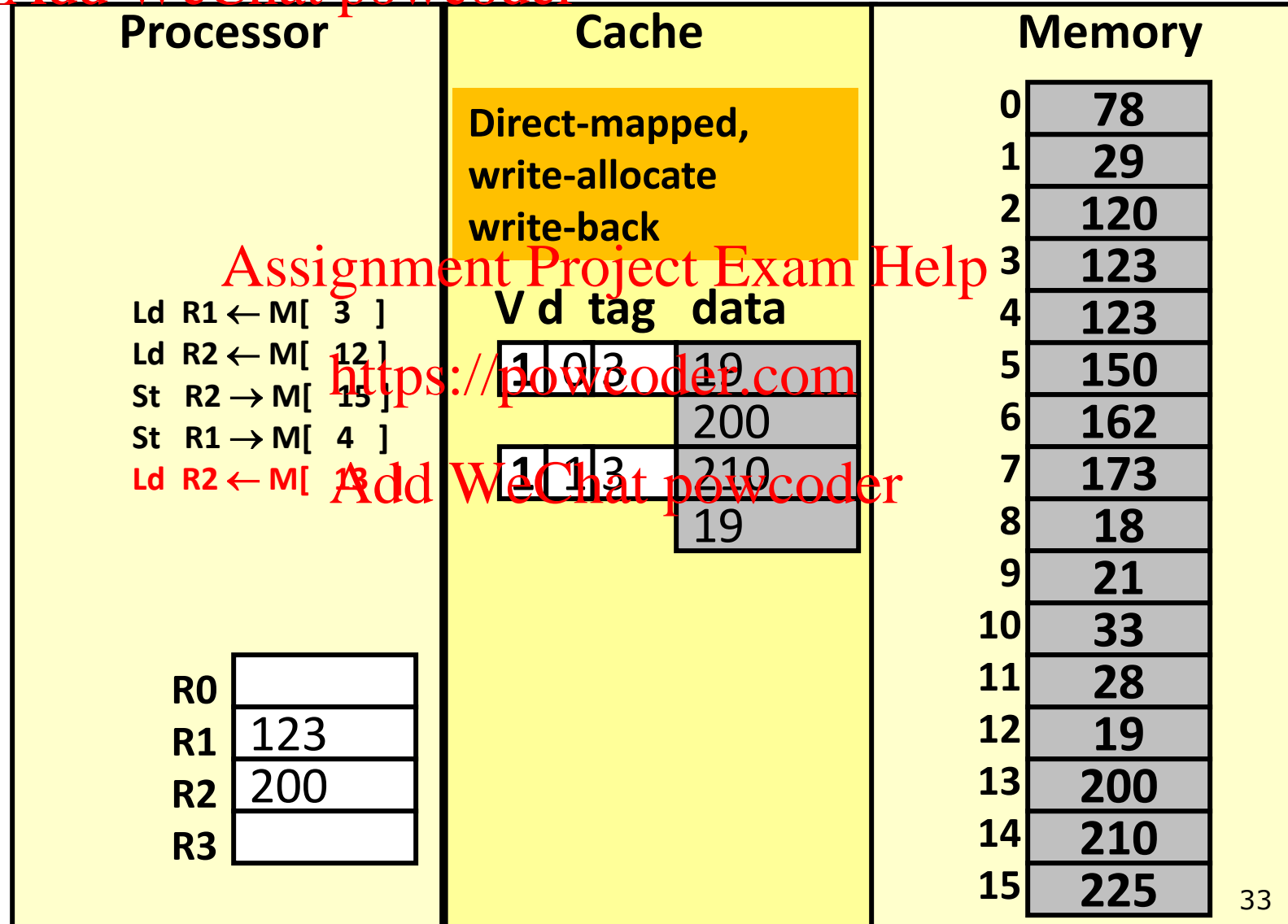
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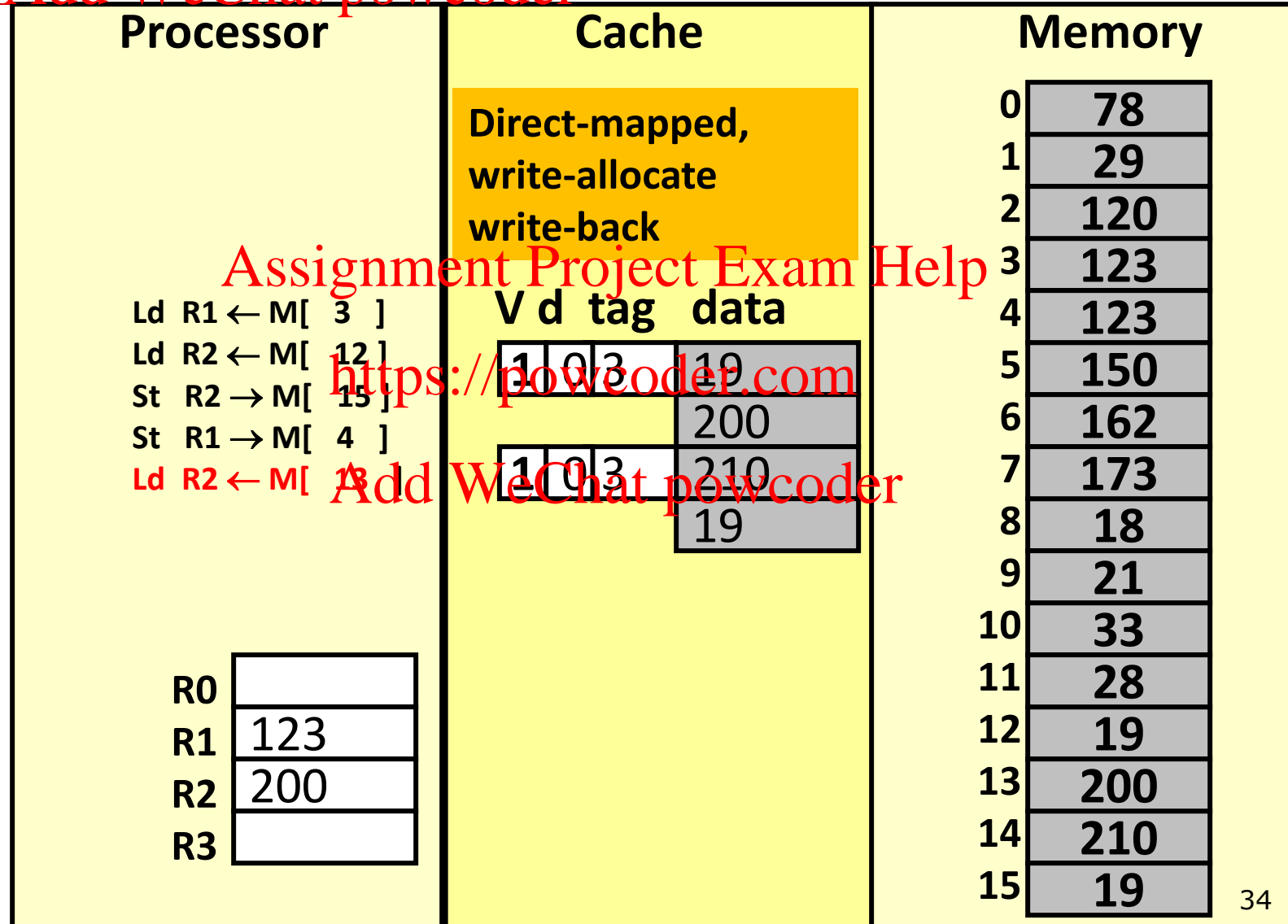
Class Problem – What is the state of the cache after executing the following instruction sequence?

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Class Problem – What is the state of the cache after executing the following instruction sequence?

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Class Problem

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How many tag bits are required for:

32-bit address, byte addressed, direct-mapped 32k cache, 128 byte block size, write-back

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What are the overheads of this cache?

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Class Problem

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How many tag bits are required for:

32-bit address, byte addressed, direct-mapped 32k cache, 128 byte block size, write-back

Bytes in block = 128 \Rightarrow Block offset size = 7 bits (*byte addressable*)

Lines = 32k / 128 = 256 \Rightarrow Line index = 8 bits

Tag bits = 32 - 7 - 8 = 17 bits

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What is the overhead of this cache?

17 bits (Tag) + 1 bit (Valid) + 1 bit (Dirty) = 19 bits / line

19 bits / line * 256 lines = 4864 bits

4864 bits / 32KB = 1.9% overhead

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What about cache for instructions?

Instructions should be cached as well

We have two choices:

1. Treat instruction fetches as normal data and allocate cache lines when fetched
2. Create a second cache (called the instruction cache or ICache) which caches instructions only

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How do you know which cache to use?

What are advantages of a separate ICache?

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Integrating Caches into a Pipeline

How are caches integrated into a pipelined implementation?

Replace instruction memory with Icache

Replace data memory with Dcache

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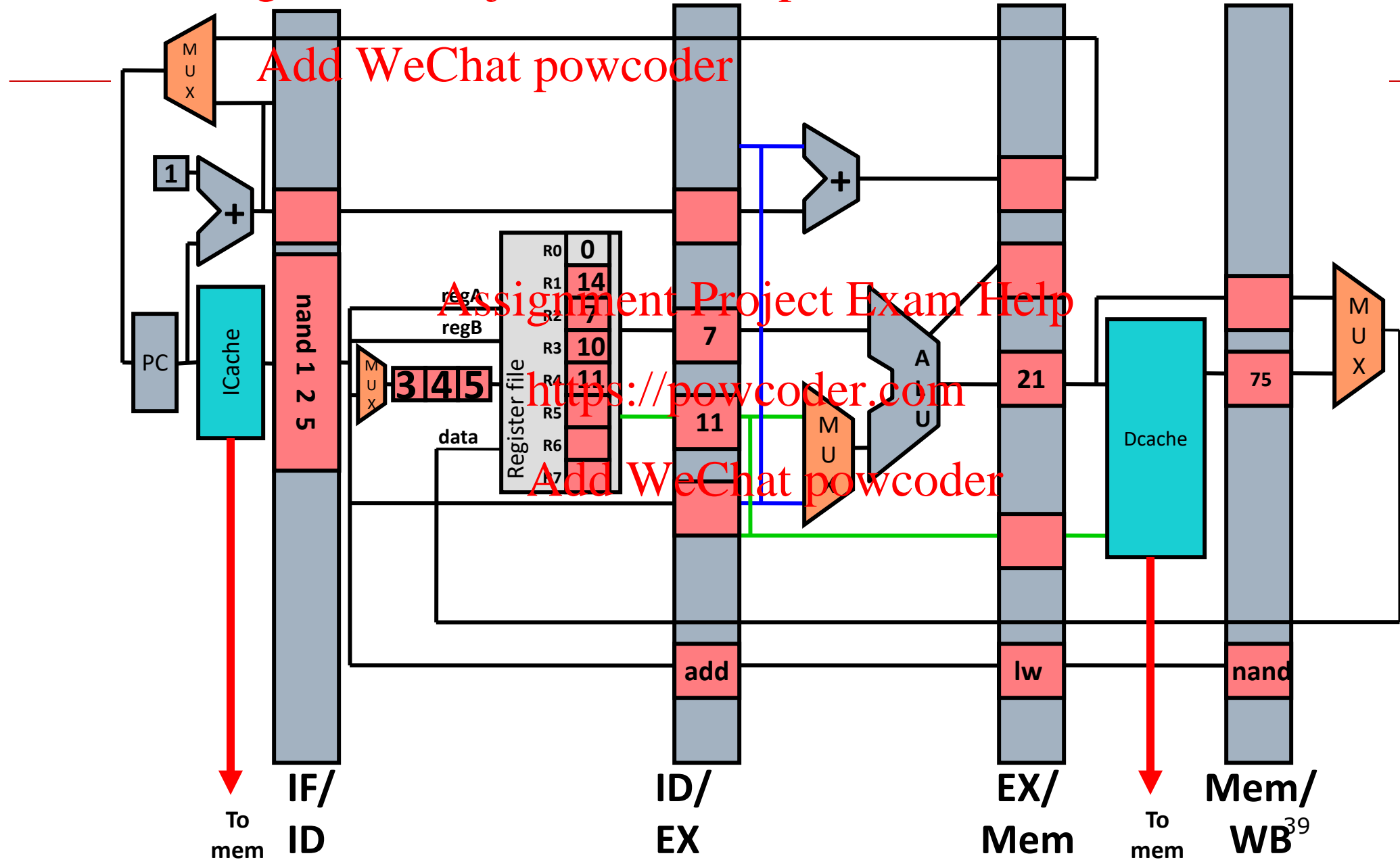
Issues:

Memory accesses now have variable latency

Both caches may miss at the same time

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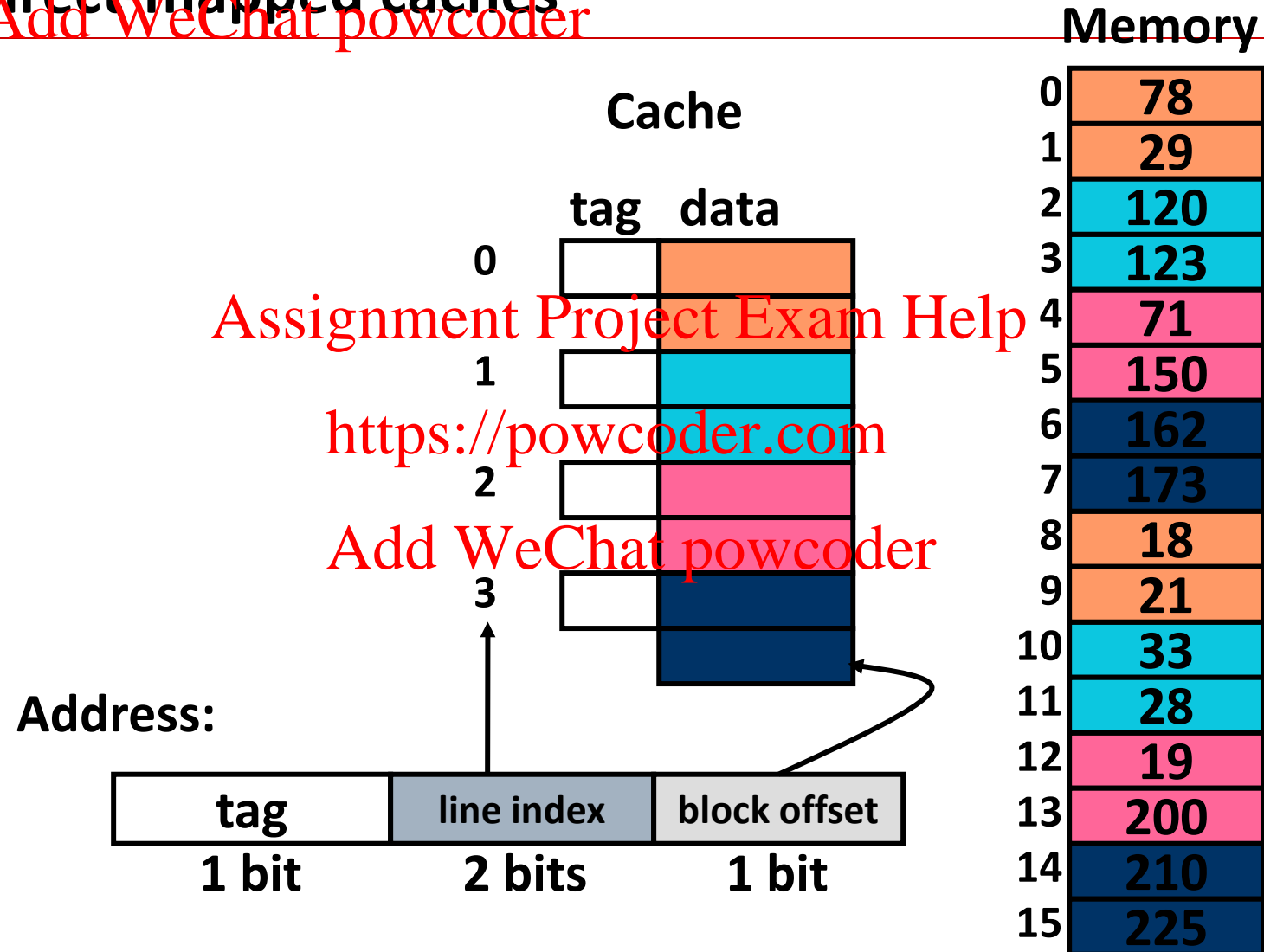
LC2K Pipeline with Caches



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Summary: Direct-mapped caches

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Next lecture: Get the advantage of both...

Set **associative** caches:

- Partition memory into regions

 - like direct mapped but fewer partitions

- Associate a region to a set of cache lines

 - Check tags for all lines in a set to determine a HIT

- Treat each line in a set like a small fully associative cache

- LRU (or LRU-like) policy generally used

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Set-associative cache

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